1994
(REV. 2)

CRYSTAL SEMICONDUCTOR COMMUNICATION DATABOOK

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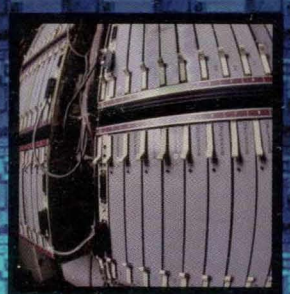
CRYSTAL



CRYSTAL

Crystal Semiconductor Corporation

Communication Products Data Book

October 1994

TRADEMARKS

Crystal Semiconductor Corporation has made every effort to supply trademark information about company names, products, and services mentioned in this book. Trademarks indicated below are derived from various sources.

CRYSTAL is a registered trademark of Crystal Semiconductor Corporation.

SMART *Analog*, Crystal Clear, and CrystalWare are trademarks of Crystal Semiconductor Corporation.

Trademarks in this book belong to their respective companies.

PATENTS

Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.A.:

4,709,225; 4,746,899; 4,748,418; 4,804,863; 4,805,198; 4,849,662; 4,851,841; 4,918,454; 4,939,516; 4,941,156; 4,943,807; 4,988,954; 5,012,244; 5,039,989; 5,055,846; 5,061,925; 5,068,660; 5,079,550; 5,087,914; 5,088,107; 5,111,451; 5,117,200; 5,121,080; 5,140,279; 5,150,386; 5,157,395; 5,172,115; 5,187,390; 5,196,850; 5,198,782; 5,208,597; 5,212,659; 5,220,483; 5,239,210; 5,245,344; 5,247,210; 5,248,970; 5,257,026; 5,258,758; 5,268,651; 5,274,375.

Germany:

3,642,070; 3,733,682; 3,736,735; 3,737,279; 3,933,552; 4,002,871; 4,127,096; 4,202,180.

Great Britain:

2,184,621; 2,195,848; 2,198,305; 2,198,306; 2,223,879; 2,232,547.

France:

2,591,753; 2,604,839; 2,606,564; 2,606,565; 2,673,779.

Japan:

1,684,670; 1,736,807; 1,747,991.

CONTENTS

Consumer and Professional Audio Products

Crystal Semiconductor pioneered and brought delta-sigma conversion technology to production in a variety of digital audio A/D and D/A converter products. These products span the full range of price-performance requirements, from professional (e.g., ≥107 dB ICs, the CS5390 ADC and CS4303 DAC) to consumer (e.g., 8-pin, 16-bit, stereo DAC, the CS4330).

Products: For data sheets, call (512) 445-7222

Volume Control

- CS3310 - Stereo, digital volume control (110 dB SNR)

DAC

- CS4225 - Digital audio conversion system
- CS4303 - 107 dB, stereo, 18-bit DAC
- CS4328 - Stereo, 18-bit, delta-sigma DAC
- CS4330/1/3 - stereo, delta-sigma DAC, single +5V

ADC

- CS5330/1 - 96 dB, single +5V, stereo, 18-bit ADC (lowest power: 100 mW)
- CS5336/8/9 - 95 dB, stereo, 16-bit, ADC
- CS5349 - 90 dB, single +5V, stereo, 16-bit ADC
- CS5389 - 107 dB, stereo, 18-bit delta-sigma ADC
- CS5390 - 110 dB, stereo, 20-bit delta-sigma ADC

Digital Interface

- CS8401A/2A - Digital audio interface transmitter (supports AES/EBU, IEC958, S/PDIF, EIAJ CP-340 formats)
- CS8411/12 - Digital audio interface receiver (supports AES/EBU, IEC958, S/PDIF, EIAJ CP-340 formats)
- CS8425 - 'A-LAN' Audio Local Area Network transceiver (I2C bus, parallel interface, or stand-alone transceiver)

Multimedia Audio Products

Crystal Semiconductor's pioneering work in mixed-signal integration has brought low-cost, stereo, 16-bit A/D and D/A conversion to the world of computer multimedia. Crystal's 16-bit solutions have been established as the industry standard, and cost less than traditional 8-bit alternatives.

Crystal's multimedia codecs achieve new levels of integration by combining CD-quality 16-bit converters, anti-aliasing filters, smoothing filters, and programmable gain and volume control on a single chip. The core converters are based on Crystal's proprietary delta-sigma techniques.

Both the CS4248 and the CS4231 integrate the PC ISA bus interface on-chip, as well as analog and digital mixers. The CS4231 includes a variety of enhanced features such as added mixing and on-chip ADPCM compression.

Products: For data sheets, call (512) 445-7222

Audio Codec

- CS4215-Multimedia codec, stereo 16-bit A/D and D/A, microphone gain, headphone driver, A-law/m-law option.
- CS4216 -Multimedia codec, stereo 16-bit A/D and D/A programmable input gain and output volume control
- CS4231/31A - Parallel (ISA/EISA) interface multimedia codec, stereo, 16-bit A/D and D/As,ADPCM, MPC mixer, on-chip FIFOs, full-duplex operation, 16-mA bus driver; pin-compatible upgrade to CS4248.
- CS4248 - Parallel (ISA/EISA) interface multimedia codec,stereo, 16-bit A/D and D/As, on-chip FIFOs, analog- and digital-mixing capability

DSP Audio

- CS4920 - Audio decompression with integrated stereo DAC and clock manager

Music Synthesis Products

Crystal Semiconductor offers two high-performance wavetable music synthesizer products. These digital signal processor (DSP)-based devices offer sound-generation capabilities typically found only in professional-quality keyboards and electric pianos. The CS8905 and CS9203 are ideal for applications such as music keyboards, karaoke equipment, arcade games, MIDI sound modules and personal computer (PC) add-in boards.

Several complete system solutions are available from Crystal. First, the CS8905 may be used as a General MIDI-compatible synthesizer (16-note polyphony, 16-part multitimbral) with a 1-Mbyte wavetable sample set, suitable for cost-sensitive applications such as PC add-in boards. A high-polyphony, multi-timbral version may be implemented using the CS9203; this solution performs General MIDI-compliant music synthesis (24-note polyphony, 16 timbres), with either 2 or 4 Mbytes of wavetable sample data supplied under license by Crystal. The CS8905 can optionally be used with the CS9203 as a programmable effects processor, performing Roland® Sound Canvas (GS)-compatible reverb and chorus.

Products:	For data sheets, call (512) 445-7222

CS8905 - Programmable Music Processor

CS9203 - Advanced Music Synthesizer

CRD9203R - CS8905/9203-Based System Solution

T1/E1 Products

Crystal Semiconductor offers a broad family of low-power CMOS PCM line interface circuits, with each device optimized for a unique system application. The CS61535A, CS61574A, CS61575 and CS61584 are recommended for use in new designs.

Crystal Semiconductor's leadership continues with the-best in-class: transmission-line impedance matching, short-circuit current limiting, pulse shapes, jitter attenuation, jitter tolerance and low power consumption. Our CS2180B T1 Transceiver is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (D4, SLC96, T1DM, and ESF).

Products:	Datasheets are in this databook

CS2180A/B - T1 framers

CS61304A - T1/E1 Line Interface. Enhanced, drop-in replacement for LXT304.

CS61305A - T1/E1 Line Interface. Enhanced, drop-in replacement for LXT305.

CS6152 - Low-power T1 Analog Line Interface for use with external clock recovery circuits

CS61534 - T1/E1 Line Interface Unit

CS61535/35A - Low-power T1/E1 Line Interface with transmit-path jitter attenuation.

CS61544 - T1 Line Interface unit

CS61574 - T1/E1 Line Interface unit

CS61574A/75 - Low-power T1/E1 Line Interface with receive-path jitter attenuation.

CS61577 - T1/E1 Line Interface. Enhanced, drop-in replacement for CS61574.

CS6158/58A - T1/E1 Line Interface

CS61584 - Low-power, highly-programmable, dual-channel, 3.3V & 5V, T1/E1 Line Interface

DTMF Receiver

The CS8870 DTMF receiver is compatible with industry-standard 8870 devices.

Product:	Datasheet is in this data book

CS8870 - DTMF Receiver with adjustable receive sensitivity and detection/release times.

LAN Products

Crystal Semiconductor offers a complete Ethernet hardware solution, consisting of the CS8900 ISA-bus, 10BaseT controller (with AUI port), and the CS83C92C coaxial-cable transceiver.

The CS8900 is a low-cost Ethernet LAN Controller optimized for ISA Personal computers. Its highly-integrated design eliminates the need for costly external components required by other Ethernet controllers. The CS8900 includes on-chip RAM, 10Base-T transmit and receive filters, and a no-glue ISA-Bus interface with 24 mA drivers.

The CS8900's patented PacketPage™ architecture automatically adapts to changing network traffic patterns and available system resources. the result is increased system efficiency and minimized CPU overhead.

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40 percent less power than the DP8392A and DP8392B. This translates into increased reliability and compatibility with surface-mount technology. The CS83C92C is the first Ethernet transceiver that is fully compliant with ISO/IEEE 802.3.

Products:	Datasheets are in this databook.

CS8900 -ISA-bus Ethernet Network Interface Controller

CS83C92A/C - IEEE 802.3-compatible CMOS coaxial transceiver interface

Voiceband & Baseband Products

Crystal Semiconductor offers a broad variety of technology for processing voiceband and radio baseband signals. The CS645x series of products are representative of Crystal's ability to apply its delta-sigma converter technology to specific communication applications. Crystal will develop custom codec circuits for high-volume applications.

The CS6450 supports CDPD and TDMA cellular phones, and provides a baseband interface between a DSP and a radio module.

The CS6453 supports high-performance modems, and provides a voiceband interface between a DSP and a direct access arrangement.

Products:	Datasheets are in this databook.

CS6450 - I&Q Baseband codec for AMPS/TDMA/CDPD applications

CS6453 - Low-cost, single-channel, alternating voice/data codec for V.34/V.17 modem applications

Personal Communication

Crystal Semiconductor is a leading supplier of mixed-signal technology to the new and emerging Personal Digital Assistant and personal communications marketplaces, offering both standard off-the-shelf, and custom/customer specific integrated circuits.

Crystal's first standard product is the CS8130 Multi-Standard Infrared Transceiver. The CS8130 adds an IR port to a standard UART, and implements the IrDA physical-layer. Other standards supported are HP-SIR, ASK and TV remote. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud. The CS8130 uses an external PIN diode and transmit LED.

Crystal's technology portfolio includes all of the building blocks required for PDA mixed-signal controllers. These technologies include audio codecs, radio baseband codecs, screen digitizers, clock generators, phase-lock loops, and DC-measurement ADCs. Crystal will design custom PDA controllers for high-volume opportunities.

Products:	Datasheets are in this databook.

CS8130 -Multi-Standard infrared transceiver for IrDA, HPSIR, ASK and TV-remote applications.

Echo Cancellation

The CS6400 and CS6401 are voiceband echo cancellation products which can be used in full-duplex speakerphones, cellular phones, base stations, personal digital assistants, video-teleconferencing and long-distance telephone lines. These circuit contain embedded, low-cost, application-specific DSPs, and can cancel up to 64 ms of acoustic or network echo.

Products:	Datasheets are in this databook.

CS6400 - Low-cost, echo-canceling codec with integrated DSP, linear codec, and program ROM.

CS6401 - Programmable echo-canceller, with external program ROM.

General Purpose A/D Converters

Crystal's general-purpose ADCs are more accurate and stable than any previously available. Traditional data converters required regular equipment calibration by service technicians to adjust for drift in analog components. Integrated digital correction architectures make Crystal's SMART*Analog* products self-calibrating, dramatically reducing maintenance requirements. For example, the CS5030 has a Total Unadjusted Error of ±1 LSB and a reference tempco of 1ppm/°C over the -55° C to 125°C temperature range.

Products: For data sheets, call (512) 445-7222

- CS5012A/4/6 - 12/14/16-bit, self-calibrating A/D converters
- CS5030/1 - 12-bit, 500 kHz absolute-accurate A/D converters
- CS5032- 12-bit, 500 kHz A/D converter
- CS5101A/2A - 16-bit, 100/20-kHz sampling A/D converters
- CS5317 - 16-bit, 20 kHz oversampling A/D converter
- CS5412 - 12-bit, 1 MHz A/D converter
- CS5480 - 10-bit, 40 MHz A/D converter
- CS5490 - 12-bit, 20 MHz A/D converter
- CS7870/5 - 12-bit, 100 kHz sampling A/D converters

Measurement A/D Converters

Low-frequency measurement devices based on 'delta-sigma' architectures are a new type of ADCs pioneered by Crystal. These SMART*Analog* devices combine data conversion with on-chip digital signal processing to perform sophisticated filtering of the analog input. The result is a single device that replaces a significant amount of expensive discrete analog glue circuitry used for signal conditioning. Manufacturers of industrial data-acquisition systems are saving money by using a separate measurement ADC for each analog input channel. Previously, such systems would have used a single very-high-speed ADC centralized to process many input channels.

Products: For data sheets, call (512) 445-7222

- CS5321 - High-dynamic-range delta-sigma modulator
- CS5322/23 - 24-bit variable bandwidth A/D converter chipset
- CS5324 - 120 dB A/D converter
- CS5501/3 - 16/20-bit, measurement A/D converter
- CS5504 - 20-bit, two-channel A/D converter
- CS5505/6/7/8 - 16/20-bit, A/D converters
- CS5509 - 16-bit, low-cost A/D converter
- CS5516/20 - 16/20-bit, bridge transducer A/D converter

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COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING, ALPHA ONLY
A-COMMERCIAL HIGH-REL (160 HOUR BURN-IN AT 125 °C OR EQUIVALENT)
B-MILITARY 883B PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2 NUMBERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED, ALPHA CHARACTER ONLY, NO NUMERICS

P = PLASTIC DIP	S = 0.3" SOIC
C = CERAMIC SIDEBRAZE	E = CERAMIC LCC
D = CERDIP	J = J-LEAD CERAMIC CHIP CARRIER
L = PLASTIC LEADED CHIP CARRIER, J-LEAD	G = GULLWING CERAMIC CHIP CARRIER
U = UNPACKAGED DIE	Q = PLASTIC QUAD FLATPACK

TEMPERATURE SPECIFICATION - REQUIRED, ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:
C = 0 °C to 70 °C
I = -40 °C to 85 °C
M = -55 °C to 125 °C

TEMPERATURE/ACCURACY - REQUIRED, ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY GOOD	BETTER	BEST
0 °C to 70 °C	J	K	L
-40 °C to °85 C	A	B	C
-55 °C to °125 C	S	T	U

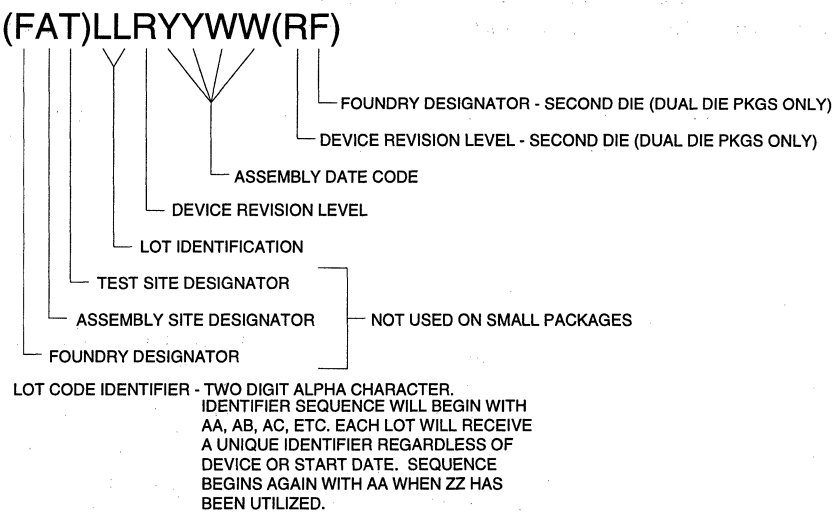
UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
42 = CODECS
43 = D/A CONVERTERS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATA COMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS EXCEPT FOR
"CXT" = QUARTZ CRYSTALS
"CDB" = EVALUATION BOARDS
"CX" = CUSTOM PRODUCTS
"CRD" = REFERENCE DESIGNS

REV6

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits. In 1991, Crystal became a wholly owned subsidiary of Cirrus Logic.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This commitment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability are active concerns of each Crystal employee. Quality is ingrained in every operation throughout the product life cycle. Some of the key operations are discussed below.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations worldwide. Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883, Method 2010, Class B. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Qualification Criteria Table)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and routinely monitored. Any major design or process changes are re-qualified.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass" (Crystal On-line Marketing, Production, and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continuously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semi-annual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883, METHOD 2010, Class B. Test die are electrically tested to verify compliance to key process parameters based upon design rule specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until disposition by a material review board. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

Qualification Criteria Table

	Method	Production Level III	Production Level II	World Class Level I	Units
Quality Performance					
Outgoing Quality (elec./vis-mech/ship.)	Crystal Spec.	2500	1500	500	DPM
Fault Coverage (Digital)		n/a	n/a	95%	%
Datasheet Test Coverage (Digital)	Datasheet	100%	100%	100%	%
Datasheet Test Coverage (Analog)	Datasheet	100%	100%	100%	%
ESD - Human Body Model	MIL 3015	1500	2000	4000	V
ESD - Machine Model	MIL3015	--	--	300	V
Latchup - Power Supply[1]	JEDEC 17	Vcc+1V	Vcc+50%	Vcc+50%	V
Latchup - I/O[1]	JEDEC 17	±50	±100	±200	mA
Reliability Performance					
Infant Mortality (48hrs@125°C or equiv.)[2]	MIL 1005	--	--	1000	DPM
Early Life (168hrs@125°C or 1yr. equiv.)[3]	MIL 1005	1/167[4]	500	300	FITS
Operating Life (1000hrs@125°C or 10yr, equiv.)[3]	MIL 1005	500	300	100	FITS
Moisture Performance					
Moisture Resistance - THB (plastic pkgs)	JEDEC 22B	500/5%	1k/5%	1k/3%	hrs/%LTPD per lot[5]
Autoclave (plastic pkgs)	JEDEC 22B	96/5%	144/5%	144/3%	hrs/%LTPD per lot[5]
Mechanical Performance					
Temp Cycle (plastic pkgs)	MIL 1010	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock (plastic pkgs)	MIL1011	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Temp Cycle w/ Hermeticity (hermetic pkgs)	MIL1010/14	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock w/ Hermeticity (hermetic pkgs)	MIL 1011/14	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Soak &VPR (surface mount plastic pkgs)	Crystal Spec.	3/5%	3/3%	3/1%	#cy/%LTPD per lot[5]
Xray	Crystal Spec.	2.50%	2.50%	0.65%	%AQL per lot[5]
Dimensions	MIL 2016	2.50%	2.50%	0.65%	%AQL per lot[5]
Solderability	MIL 2003	2.50%	2.50%	0.65%	%AQL per lot[5]
Lead Integrity & Lead Pull	MIL 2004	2.50%	2.50%	0.65%	%AQL per lot[5]
Mark Permanency	MIL2015	2.50%	2.50%	0.65%	%AQL per lot[5]
Product Integrity					
Design Rule and LVS Checks	Crystal Spec.	yes	yes	yes	
Design for Reliability & Packaging	Crystal Spec.	yes	yes	yes	
Product Characterization	Crystal Spec.	limited	full	statistical	
Test guardbands	Crystal Spec.	some	100%	100%	
Construction Analysis					
Wafer cross section & topo	Crystal Spec.	yes	yes	yes	
SEM metallization	MIL 2018	yes	yes	yes	
Package	Crystal Spec.	yes	yes	yes	

Notes:
1. at High Temperatures (exc. Lev.IV)
2. Point Estimate
3. 55°C, 0.7eV, 60%UCL
4. #fails/n
5. LTPD and AQL criteria in table above apply to each lot tested.
   CUM LTPD and AQL numbers are also required for Level II:

Individual Lot	Cum Lot Requirement
5% LTPD	3% LTPD
3% LTPD	1% LTPD
2.5% AQL	1.0% AQL

6. Individual product performance may be obtained by contacting a Crystal Sales Representative.

• Notes •

INTRODUCTION

Crystal Semiconductor offers a complete Ethernet hardware solution, consisting of the CS8900 ISA-bus, 10BASE-T controller (with AUI port), and the CS83C92C coaxial-cable transceiver.

CS8900 Ethernet Controller

The CS8900 is a low-cost Ethernet LAN Controller optimized for ISA PC motherboards. Its highly-integrated design results in the industry's smallest-footprint solution. The small footprint results from the 14mm by 14mm 100-pin TQFP package, and through the elimination of external components. The CS8900 includes on-chip RAM, 10BASE-T transmit and receive filters, and a no-glue ISA-Bus interface with 24 mA drivers. In addition to saving cost and board space, the internal filters simplify the task of achieving FCC Part 15 Class B certification.

Crystal provides a complete set of certified CS8900 drivers for all major operating systems and network operating systems. Motherboard applications are further supported by the following leadership performance-oriented features: advanced power management, full-duplex operation, Stream Transfer™, and DMA-auto-switch. The CS8900's patented PacketPage™ architecture automatically adapts to changing network traffic patterns and available system resources. The result is increased system efficiency and minimized CPU overhead.

CS83C92 Ethernet Transceiver

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40 percent less power than the DP8392A and DP8392B. This translates into increased reliability and compatibility with surface-mount technology. The CS83C92C is the first Ethernet transceiver that is fully compliant with ISO/IEEE 802.3.

CONTENTS

Coaxial Transceiver Interface

Features

- Implemented in High Voltage, Low Power CMOS
- Compatible with National's DP8392A
- CS83C92C is Compliant With ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive & Transmit Mode Collision Detection
- Standard 16-pin DIP Package & 28 pin PLCC

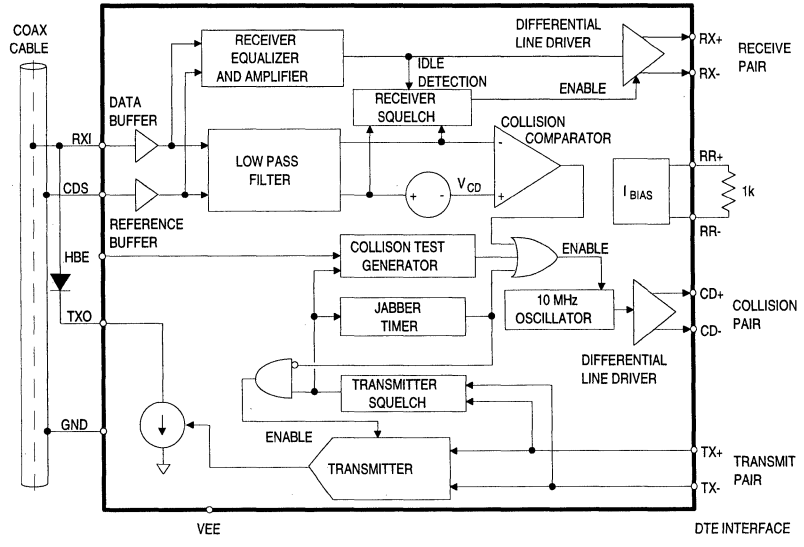
General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Manchester Code Converter. The CS83C92A is fully compatible with the DP8392A but the CS83C92A is built in CMOS technology (hence the 83"C"92). The CS83C92C is a higher performance grade which is compliant with IEEE 802.3 specifications.

For Ethernet applications, the CS83C92 is mounted on the COAX cable, and connects to the station equipment via an AUI cable. In a Cheapernet network, the CS83C92 is usually mounted on the LAN adapter card in the station equipment where it connects to the thin COAX through a BNC connector.

ORDERING INFORMATION:

CS83C92A-CP	PDIP	CS83C92C-CP	PDIP
CS83C92A-CL	PLCC	CS83C92C-CL	PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (referenced to ground)		VEE	-	-12.0	V
Package Power Rating at 25°C	(Note 1)	P_P	-	3.5	W
Input Voltage (All pins except RXI)		V_{IN}	GND + 0.3	VEE - 0.3	V
Input Voltage on RXI		V_{IN}	GND + 0.3	-12	V
I/O Current	(RXI, RR+, TX+, TX-, CDS, HBE)	I_{OUT}	-	±10	mA
	(TXO)		-	+10 / -100	mA
(Note 2)	(CD+, CD-, RX+, RX-)		-	+40 / -10	mA
Ambient Operating Temperature		T_A	0	70	°C
Storage Temperature		T_{stg}	-65	150	°C
ESD Protection	(All pins)		1000	-	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Plastic DIP package only, package is PC board mounted. Derate at the rate of 28.6 mW/°C.
2. Transient currents of up to 200mA will not cause SCR latch-up.

CS83C92A ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter		Symbol	Min	Typ	Max	Units
Recommended Supply Voltage		VEE	-	-9.0	-	V
Supply Current (V_{EE} to GND)	Nontransmitting	I_{EE}	-	-55	-70	mA
	Transmitting		-	-100	-120	mA
Receiver Input Bias Current (RXI)		I_{RXI}	-2	-	+25	µA
Transmitter Output DC Current (TXO)		I_{TDC}	37	41	45	mA
Transmitter Output AC Current (TXO)		I_{TAC}	±28	-	I_{TDC}	mA
Collision Threshold (Receive Mode)		V_{CD}	-1.45	-1.53	-1.58	V
Differential Output Voltage (RX±, CD±)	(Note 3)	V_{OD}	±475	-	±1200	mV
DC Common Mode Output Voltage (RX±, CD±)	(Note 4)	V_{OC}	-	-2.0	-	V
Idle State Differential Offset Voltage (RX±, CD±)		V_{OB}	-	-	±40	mV
Transmitter Squelch Threshold (TX±)	(Note 5)	V_{TS}	-175	-225	-300	mV
RXI Capacitance		C_X	-	1.2	-	pF
Shunt Resistance - Nontransmitting (RXI)		R_{RXI}	100	-	-	kΩ
Shunt Resistance - Transmitting		R_{TXO}	10	-	-	kΩ

Notes: 3. Improved Spec. as required to meet ISO/IEEE 802.3 specifications.
4. V_{OC} has no impact on system performance since twisted pairs are transformer isolated.
5. For a minimum pulse width of ≥ 40 ns.

2

CS83C92C ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter	Symbol	Min	Typ	Max	Units
Recommended Supply Voltage	VEE	-	-9.0	-	V
Supply Current (V_{EE} to GND) Nontransmitting	I_{EE}	-	-55	-65	mA
Transmitting		-	-100	-120	mA
Receiver Input Bias Current (RXI)	I_{RXI}	-2	-	+25	µA
Transmitter Output DC Current (TXO)	I_{TDC}	37	41	45	mA
Transmitter Output AC Current (TXO)	I_{TAC}	±28	-	I_{TDC}	mA
Collision Threshold (Receive Mode)	V_{CD}	-1.45	-1.53	-1.58	V
Differential Output Voltage (RX±, CD±) (Note 3)	V_{OD}	±550	-	±1200	mV
DC Common Mode Output Voltage (RX±, CD±) (Note 4)	V_{OC}	-	-2.0	-	V
Idle State Differential Offset Voltage (RX±, CD±)	V_{OB}	-	-	±40	mV
Transmitter Squelch Threshold (TX±) (Note 5)	V_{TS}	-175	-225	-300	mV
Tap Capacitance (Note 6)	C_X	-	1.2	4	pF
Shunt Resistance - Nontransmitting (RXI)	R_{RXI}	100	-	-	kΩ
Shunt Resistance - Transmitting	R_{TXO}	10	-	-	kΩ
Current Sink Limit (-10 V on coax) (Notes 3, 6)	It_{10}	-	-	±250	mA
Harmonic Content Relative to Fundamental (Note 7)					
2nd and 3rd Harmonics	-20	-	-	-	dB
4th and 5th Harmonics	-30	-	-	-	dB
6th and 7th Harmonics	-40	-	-	-	dB

Notes:
3. Improved Spec. as required to meet ISO/IEEE 802.3 specifications.
4. V_{OC} has no impact on system performance since twisted pairs are transformer isolated.
5. For a minimum pulse width of ≥ 40 ns.
6. Measured with external diode in place (between coax center conductor and TXO pin). The maximum diode capacitance is 1pF. Tap capacitance guaranteed by characterization.
7. Guaranteed through characterization, and production measurement of rise and fall times.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
DC Supply Voltage, VEE (GND = 0V)	8.55	-	9.45	V
Operating Temperature	0	-	70	°C
RR± Resistor	990	-	1010	Ω

CS83C92A SWITCHING CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0 V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter	Symbol	Min	Typ	Max	Units
Receiver Startup Delay (RXI to RX±)	t_{RON}	-	4	5	bits
Receiver Propagation Delay (RXI to RX±)	t_{Rd}	-	15	50	ns
Differential Outputs Rise Time (RX±, CD±)	t_{Rr}	-	4	7	ns
Differential Outputs Fall Time (RX±, CD±)	t_{Rf}	-	4	7	ns
Receiver and Cable Total Jitter	t_{RJ}	-	±2	-	ns
Transmitter Start-up Delay	t_{TST}	-	1	-	bits
Transmitter Propagation Delay	t_{Td}	-	25	50	ns
Transmitter Rise Time - 10% to 90% (TXO)	t_{Tr}	20	25	30	ns
Transmitter Fall Time - 10% to 90% (TXO)	t_{Tf}	20	25	30	ns
t_{Tr} and t_{Tf} Mismatch	t_{TM}	-	0.5	-	ns
Transmitter Skew (TXO) (Note 8)	t_{TS}	-	±0.5	-	ns
Transmit Turn-on Pulse Width at V_{TS} (TX±) (Note 9)	t_{TON}	-	20	40	ns
Transmit Turn-off Pulse Width above V_{TS} (TX±)	t_{TOFF}	-	250	-	ns
Collision Turn-on Delay	t_{CON}	-	7	-	bits
Collision Turn-off Delay	t_{COFF}	-	-	20	bits
Collision Frequency (CD±)	f_{CP}	8.0	-	12.5	MHz
Collision Pulse Width (CD±)	t_{CP}	35	-	70	ns
CD Heartbeat Delay (TX± to CD±)	t_{HON}	0.6	-	1.6	µs
CD Heartbeat Duration (CD±)	t_{HW}	0.5	1.0	1.5	µs
Jabber Activation Delay (TX± to TXO and CD±)	t_{JA}	20	29	60	ms
Jabber Reset Timeout (TX± to TXO and CD±)	t_{JR}	250	500	750	ms

Notes: 8. Difference in propagation delay in outputing a positive edge as opposed to a negative edge.
9. For minimum pulse amplitude of ≥ -300mV.

2

CS83C92C SWITCHING CHARACTERISTICS (T_A = 0° to 70°C, VEE = -9.0 V ±5%, GND = 0V, CD±, RX± pull downs = 510Ω)

Parameter		Symbol	Min	Typ	Max	Units
Receiver Startup Delay (RXI to RX±)		t_{RON}	-	4	5	bits
Receiver Propagation Delay (RXI to RX±)		t_{Rd}	-	15	50	ns
Differential Outputs Rise Time (RX±, CD±)	(Note 3)	t_{Rr}	-	4	7	ns
Differential Outputs Fall Time (RX±, CD±)	(Note 3)	t_{Rf}	-	4	7	ns
Receiver and Cable Total Jitter	(Note 10)	t_{RJ}	-	±2	±6	ns
Transmitter Start-up Delay	(Note 3)	t_{TST}	-	1	2	bits
Transmitter Propagation Delay		t_{Td}	5	25	50	ns
Transmitter Rise Time - 10% to 90% (TXO)	(Note 3)	t_{Tr}	20	25	30	ns
Transmitter Fall Time - 10% to 90% (TXO)	(Note 3)	t_{Tf}	20	25	30	ns
t_{Tr} and t_{Tf} Mismatch	(Note 3)	t_{TM}	-	0.5	2.0	ns
Transmitter Skew (TXO)	(Note 8, 10)	t_{TS}	-	±0.5	±2	ns
Transmit Turn-on Pulse Width at V_{TS} (TX±)	(Note 9)	t_{TON}	15	20	40	ns
Transmit Turn-off Pulse Width above V_{TS} (TX±)	(Note 11)	t_{TOFF}	200	-	-	ns
Collision Turn-on Delay	(Note 3)	t_{CON}	-	7	13	bits
Collision Turn-off Delay		t_{COFF}	-	-	20	bits
Collision Frequency (CD±)		f_{CP}	8.5	-	11.5	MHz
Collision Pulse Width (CD±)		t_{CP}	40	-	60	%
CD Heartbeat Delay (TX± to CD±)		t_{HON}	0.6	-	1.6	µs
CD Heartbeat Duration (CD±)		t_{HW}	0.5	1.0	1.5	µs
Jabber Activation Delay (TX± to TXO and CD±)		t_{JA}	20	29	60	ms
Jabber Reset Timeout (TX± to TXO and CD±)		t_{JR}	250	500	750	ms

Notes: 10. Maximum spec guranteed by design and characterization.
11. Represents 802.3 requirement for IDL condition. CS83C92 will recognize IDL condition in the range of 130ns to 200ns.

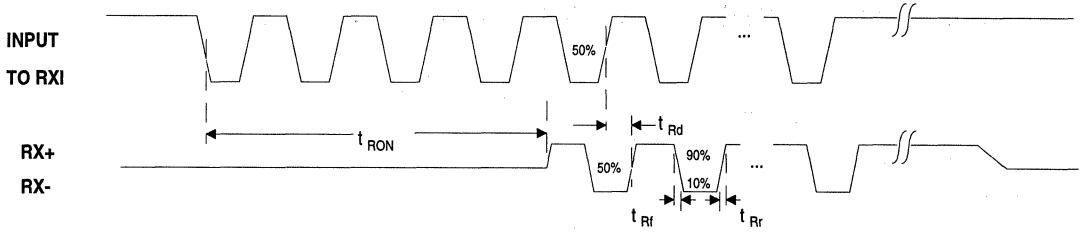


Figure 1. Receiver Timing

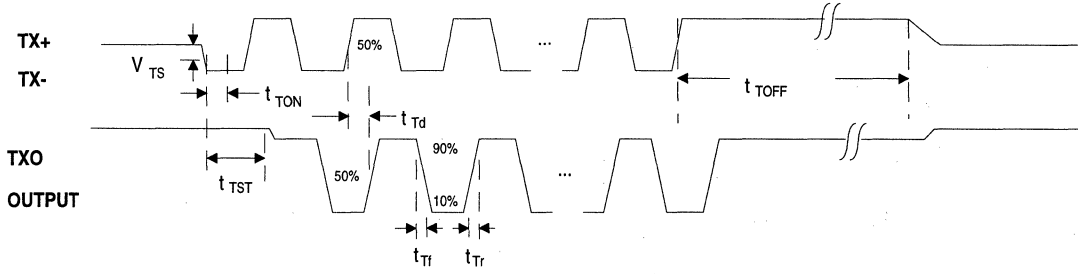


Figure 2. Transmitter Timing

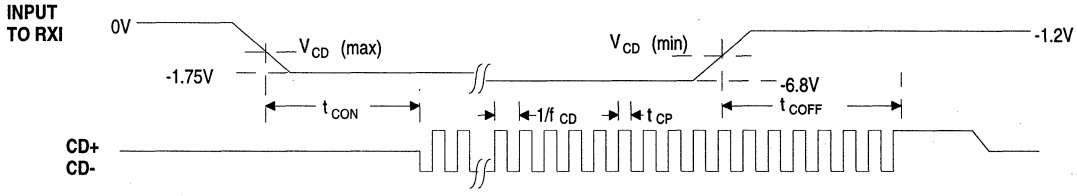


Figure 3. Collision Timing and Test Ciruit

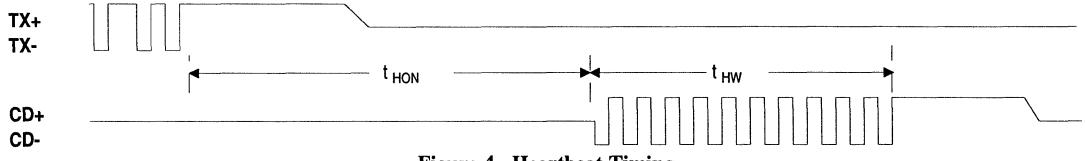


Figure 4. Heartbeat Timing

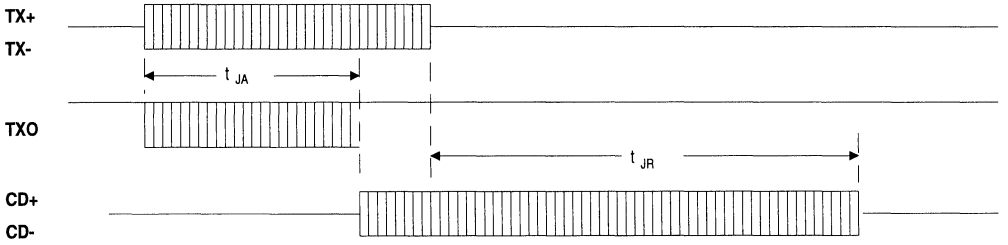


Figure 5. Jabber Timing

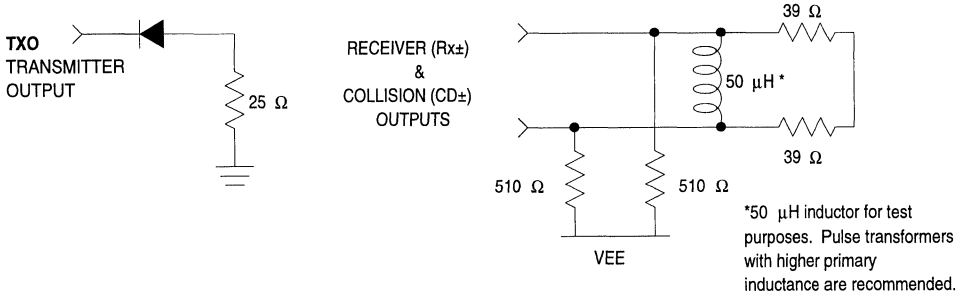


Figure 6. Test Loads

THEORY OF OPERATION

The CS83C92 interfaces the LAN station equipment to an Ethernet or Cheapernet COAX cable. The CS83C92 transmitter provides the current drive and pulse shaping required to drive signals onto the COAX, as well as squelch for signals received from the transmit pair, TX±. The receiver section provides equalization and squelch for signals on the COAX. Collisions are continually monitored and indicated by a 10MHz clock output on the CD± pair. The device also has a jabber timer which disables the transmitter and signals the DTE if packets longer than the legal length are transmitted.

In an Ethernet LAN, the CS83C92 mounts on the COAX cable, and connects to the station equipment through a transceiver drop cable (AUI cable). The transceiver drop cable can be up to 50 meters long. For Cheapernet applications, the CS83C92 is usually located in the station equipment, and connects to the Cheapernet COAX (such as RG58) through a BNC connector.

Transmitter

The transmitter accepts differential signals at the TX± inputs from the Manchester Code Converter, and drives these signals onto the network from the TXO output at the signal levels required by IEEE 802.3.

The TXO pin is open drain, and is pulled up to ground by the COAX termination resistors. The rise and fall times of the output pulses are internally conditioned to achieve slew rates of 25ns to reduce harmonics in the transmitted signal. Output drive current levels are set by a bandgap voltage reference and an external 1kΩ 1% resistor connected between the RR± pins. When not transmitting, the TXO output is disabled to prevent noise on the network. An external 1N916 diode must be added to reduce loading and capacitance (in both powered and unpowered conditions) to comply with ISO and IEEE specifications. With the diode in place, the tap capacitance contributed by the CS83C92 is typically less than 3 pF.

The transmit squelch circuit blocks signals input from TX± with pulse widths of less than 15ns or amplitudes of less than -175mV. The squelch circuit turns the transmitter off if the signal stays more positive than -175mV for more than 200ns (end of packet detection).

The TX± pins are transformer coupled to the Manchester Code Converter. In Ethernet applications where a transceiver drop cable (or Access Unit Interface, AUI) is used, a 78Ω resistor should be placed across the end of the cable, near the transformer. This resistor may be eliminated for Cheapernet applications where no AUI cable is used.

Receiver

The receiver input, RXI, connects to the COAX center conductor. The CS83C92 amplifies and equalizes the input signal and passes signals which exceed the receiver squelch level to the Receiver Pair, RX±. Up to five bits may be received at RXI and not transmitted on the RX± pair. The sixth bit will be transmitted, but may have code violations. The seventh and subsequent bits will be transmitted according to specificaton.

The receiver squelch circuit prevents false triggering of the receiver due to noise on the COAX. Signals input to the RXI pin that cause the output of an internal low-pass filter to exceed -140mV$_{DC}$ (typical) will exceed the DC squelch level, and be passed through to the RX± pair. Should the positive pulse width exceed 200ns (typical) the receiver will turn off (end of packet detection). The receiver will stay off if the output of the low-pass filter rises above the squelch threshold within 1µs.

RX± comprise a differential line driver which interfaces to the Manchester Code Converter via an isolation transformer. RX± go to a differential zero state when idle to prevent DC current from saturating the isolation transformer.

For Ethernet applications, the RX± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92 is generally located on the same card as the Manchester Code Conveter, and 1500Ω pull-down resistors may be used to reduce power consumption.

Collison Detection

The collison detector monitors the COAX center conductor and senses the voltage conditions indicative of a collison. A collison can be detected when two or more stations are concurrently transmitting, whether or not the local transmitter is activated. The detector signals a collison by sending a 10MHz clock signal out on the Collison Pair, CD±, to the Manchester Code Converter.

The CDS pin provides a coaxial ground reference voltage for the collision detector. This pin should be connected to the shield of the COAX, rather than power supply ground, to prevent inaccuracies due to ground drops. A collison is detected when the output voltage of the receiver low-pass filter exceeds the collison voltage threshold, V_{CD}.

The 10MHz clock is internally generated, and used for collison indication and the heartbeat test. This oscillator requires no external components.

If enabled (HBE high), the Heartbeat Test will cause transmission of the 10MHz clock on the CD± pair for 1.0µs, 1.1µs after the end of each transmission if: both the transmitter and receiver were enabled; there was not a collision detected; jabber has not occured.

For Ethernet applications, the CD± pins are tied to the VEE supply through 500Ω or 510Ω resistors. In Cheapernet applications, the CS83C92 is generally located on the same card as the Manchester Code Converter, and the use of 1500Ω pull-down resistors will reduce power consumption.

Jabber Timer

The Jabber Timer monitors the operation of the transmitter using an internal oscillator as a time base. If the transmitter operates continuously for more than 29ms, the jabber timer disables the transmitter and enables the Collison Detector outputs. The Jabber Timer continues to monitor the transmitter squelch output. After the Manchester Code Converter has been silent for 750ms, the output on CD± is terminated, and the transmitter is reenabled for the next valid packet.

P. C. Board Layout

The CS83C92 is built in CMOS technology. It consumes and dissipates far less power than equivalent bipolar circuits. Still, heat dissipation and device reliability will be improved if the VEE pins are connected to a copper plane on the PC board. However, the application demands that the CS83C92 handle significant currents in the process of driving signals onto the cable. Soldering all of the VEE pins onto a copper plane is required to provide a surface area which aids in heat dissipations.

For Ethernet applications, the isolation transformers, the DC to DC converter, and the transceiver are located in the Transceiver assembly, attached to the COAX. For Cheapernet applications, these components are usually mounted on the same board as the Ethernet Controller (CS8900). The 78Ω and 39.2Ω load

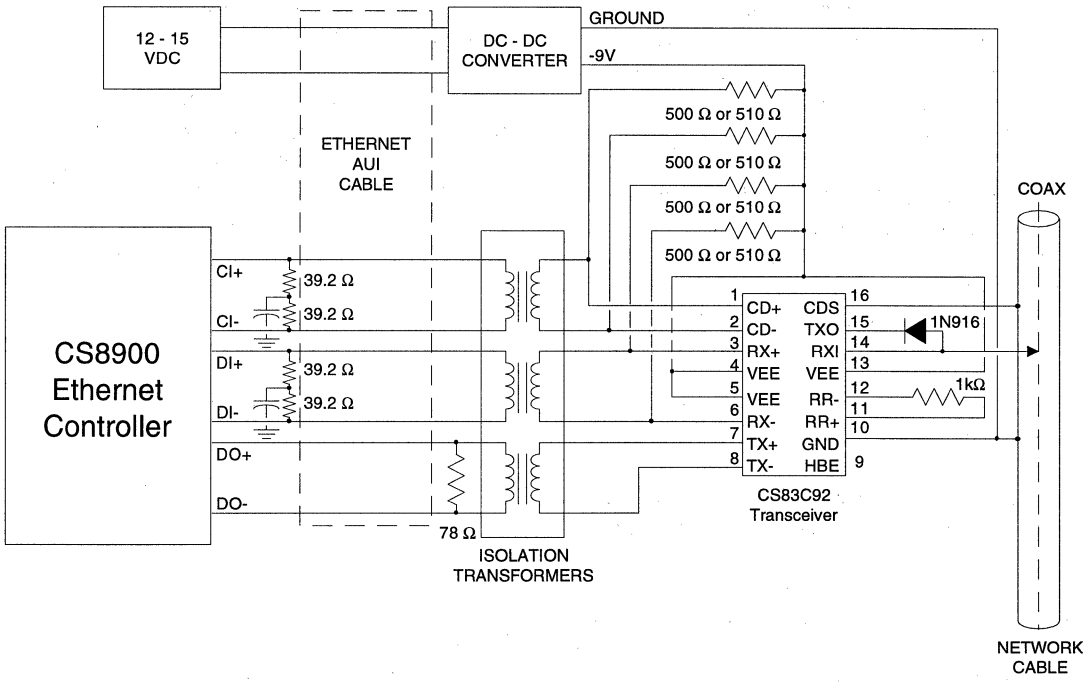


Figure 7. CS83C92 System Connection Diagram

resistors terminate the AUI cable, and are not required in systems where the AUI cable is not used (where the distance between the CS8900 and Transceiver is short).

For the PLCC package, it is recommended that a small printed circuit board V_{EE} plane be connected to pins 5-11, and a second one be connected to pins 20-25. To reduce the thermal resistance, the area of the plane on each set of pins should be ≥ 0.19 square inches (approx. 0.5" x 0.375"). Figure 8 illustrates a recommended component side layout for these planes.

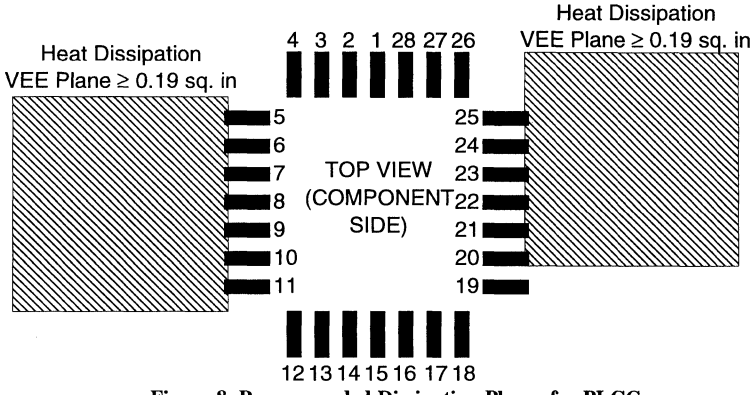
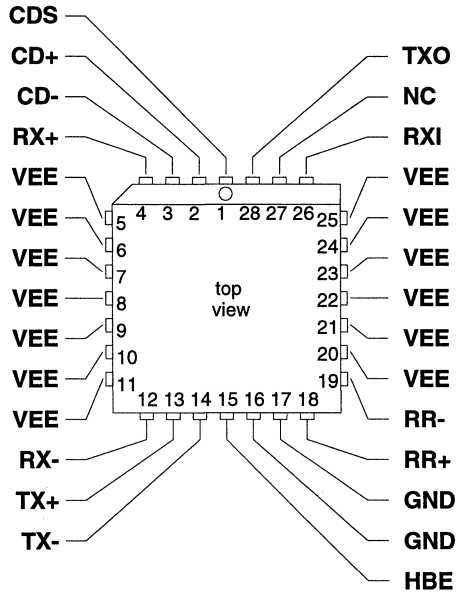


Figure 8. Recommended Dissipation Planes for PLCC

PIN DESCRIPTIONS

CS83C92

Collison Detect Output +	CD+	1	16	CDS	Collison Detect Sense
Collison Detect Output -	CD-	2	15	TXO	Transmitter Output
Receive Data Output +	RX+	3	14	RXI	Receive Input
Negative Power Supply	VEE	4	13	VEE	Negative Power Supply
Negative Power Supply	VEE	5	12	RR-	External Resistor -
Receive Data Output -	RX-	6	11	RR+	External Resistor +
Transmit Data Input+	TX+	7	10	GND	Ground
Transmit Data Input -	TX-	8	9	HBE	Heartbeat Enable



Power Supplies

VEE - Negative Power Supply

The -9V supply is connected to these pins. A 0.1µF decoupling capacitor should be connected between this pin and GND. All of the VEE pins should be soldered to a copper VEE plane.

GND - Ground

Power supply ground; connects to COAX shield.

Inputs

TX+, TX- - Transmit Inputs

Balanced differential line receiver which accepts the signal from the Manchester Code Converter. Signals exceeding transmitter squelch limits are output at TXO with the proper pulse shape. The common mode voltage on TX± is internally set and must not be externally established.

RXI - Network Receiver Input

Connects to the COAX center conductor. Signals meeting receiver squelch limits are recovered and output on RX±. RXI also detects the collison voltage level.

Outputs

TXO - Network Transmitter Output

TXO connects to the coax center conductor, and drives signals which meet TX± squelch requirements onto the coax. An external 1N916 diode, or equivalent, must be placed between the TXO pin and the coax center conductor to reduce capacitance and inhibit current flow at the TXO pin when the voltage on the coax center conductor is more negative than the power supply voltage applied to the CS83C92.

CD+, CD- - Collison Outputs

A balanced differential output which drives an internally generated 10MHz signal to the station equipment when a collison is detected, when excessive transmission occurs, or during a CD heartbeat condition. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92 is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

RX+, RX- - Receive Data Outputs

A balanced differential output which drives the data recovered from the network to the MCC. These outputs are open source: when driving a 78Ω transmission line, these pins should be pulled to VEE with 500Ω or 510Ω resistors; for Cheapernet applications, where the CS83C92 is not driving a 78Ω load, use of 1.5kΩ resistors will save power.

Control

HBE - Heartbeat Enable

When the HBE pin is connected to ground, the Collision Detect Heartbeat test is enabled. Connecting the HBE pin to VEE disables the Collision Detect test.

RR+, RR- - External Resistor

A 1kΩ, 1% resistor should be connected across these pins to set internal operating current levels.

CDS - Collision Detect Sense

The CDS pin connects directly to the COAX shield, providing a reference for the collision detection voltage level.

Miscellaneous

NC - No Connect (PLCC only).

This pin should be left floating.

Highly-Integrated ISA Ethernet Controller

Features

- Single-Chip IEEE 802.3 Ethernet Controller with Direct ISA-Bus Interface
- Efficient PacketPage™ Architecture Operates in I/O and Memory Space, and as DMA Slave
- Full Duplex Operation
- On-Chip RAM Buffers Transmit & Receive Frames
- 10BASE-T Port with Analog Filters, Provides:
  - Automatic Polarity Detection and Correction
- AUI Port for 10BASE2, 10BASE5 and 10BASE-F
- Programmable Transmit Features:
  - Automatic Re-transmition on Collision
  - Automatic Padding and CRC Generation
- Programmable Receive Features:
  - StreamTransfer™ for Reduced CPU Overhead
  - Auto-Switch Between DMA and On-Chip Memory
  - Early Interrupts for Frame Pre-Processing
  - Automatic Rejection of Erroneous Packets
- EEPROM Support for Jumperless Configuration
- Boot PROM Support for Diskless Systems
- Boundary Scan and Loopback Test
- LED Drivers for Link Status and LAN Activity
- Standby and Suspend Sleep Modes

Description

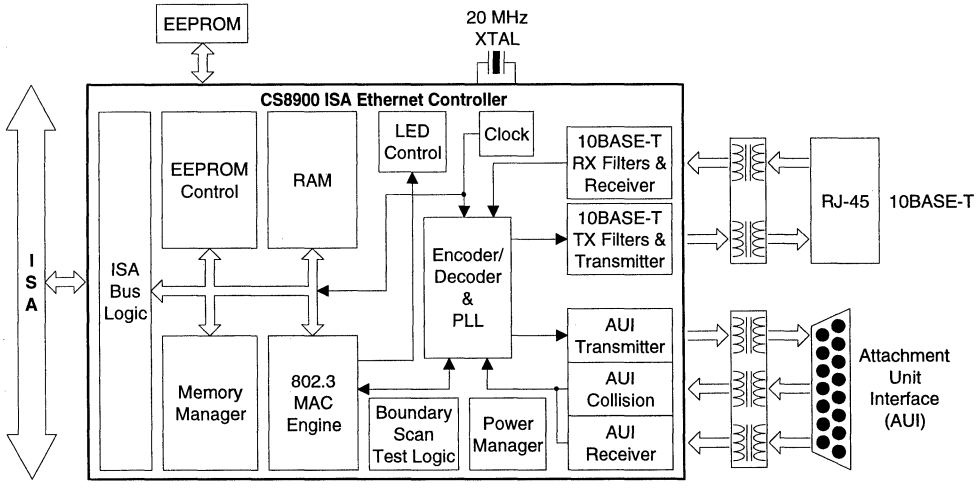
The CS8900 is a low-cost Ethernet LAN Controller optimized for Industry Standard Architecture (ISA) Personal Computers. Its highly-integrated design eliminates the need for costly external components required by other Ethernet controllers. The CS8900 includes on-chip RAM, 10BASE-T transmit and receive filters, and a direct ISA-Bus interface with 24 mA Drivers.

In addition to high integration, the CS8900 offers a broad range of performance features and configuration options. Its unique PacketPage architecture automatically adapts to changing network traffic patterns and available system resources. The result is increased system efficiency and minimized CPU overhead.

The CS8900 is available in a thin 100-pin TQFP package ideally suited for small form-factor, cost-sensitive Ethernet applications, such as desktop and portable motherboards and adapters. With the CS8900, system engineers can design a complete Ethernet circuit that occupies less than 1.5 square inches (10 sq cm) of board space.

ORDERING INFORMATION:

CS8900-CQ	0 to 70° C	100-pin TQFP
CDB8900		Evaluation Kit



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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CONTENTS

1.0 INTRODUCTION

1.1 General Description

The CS8900 is a true single-chip Ethernet solution, incorporating all of the analog and digital circuitry needed for a complete Ethernet circuit. Major functional blocks include: a direct ISA-bus interface; an 802.3 MAC engine; integrated buffer memory; a serial EEPROM interface; and a complete analog front end with both 10BASE-T and AUI.

Direct ISA-Bus Interface

Included in the CS8900 is a direct ISA-bus interface with full 24 mA drive capability. Its configuration options include a choice of four interrupts and three DMA channels (one of each selected during initialization). It provides 0-wait-state performance for most operations on ISA buses running at up to 11 MHz.

Integrated Memory

The CS8900 incorporates a 4-Kbyte page of on-chip memory, eliminating the cost and board area associated with external memory chips. Unlike most other Ethernet controllers, the CS8900 buffers entire transmit and receive frames on chip, eliminating the need for complex, inefficient memory management schemes. In addition, the CS8900 operates in either Memory space, I/O space, or with external DMA controllers, providing maximum design flexibility.

802.3 Ethernet MAC Engine

The CS8900's Ethernet Media Access Control (MAC) engine is fully compliant with the IEEE 802.3 Ethernet standard (ISO/IEC 8802-3, 1993). It handles all aspects of Ethernet frame transmission and reception, including: collision detection, preamble generation and detection, and CRC generation and test. Programmable MAC features include automatic re-transmission on collision, and automatic padding of transmitted frames.

EEPROM Interface

The CS8900 provides a simple and efficient serial EEPROM interface that allows configuration information to be stored in an optional EEPROM, and then loaded automatically at power-up. This eliminates the need for costly and cumbersome switches and jumpers.

Complete Analog Front End

The CS8900's analog front end incorporates a Manchester encoder/decoder, clock recovery circuit, 10BASE-T transceiver, and complete Attachment Unit Interface (AUI). It provides manual and automatic selection of either 10BASE-T or AUI, and offers three on-chip LED drivers for link status, bus status, and line activity.

The 10BASE-T transceiver includes drivers, receivers, and analog filters, allowing direct connection to low-cost isolation transformers. It supports 100, 120, and 150 Ω shielded and unshielded cables, extended cable lengths, and automatic receive polarity reversal detection and correction.

The AUI port provides a direct interface to 10BASE-2, 10BASE-5 and 10BASE-FL networks, and is capable of driving a full 50-meter AUI cable.

1.2 System Applications

The CS8900 is designed to work well in either motherboard or adapter applications.

Motherboard LANs

The CS8900 requires the minimum number of external components needed for a full Ethernet

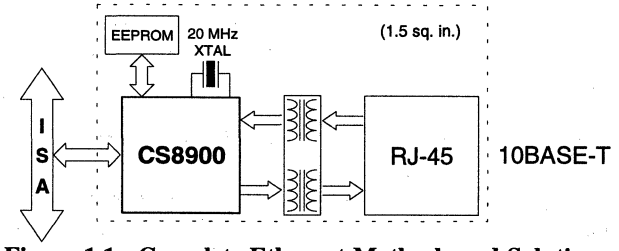


Figure 1.1. Complete Ethernet Motherboard Solution

node. Its small-footprint package and high level of integration allow System Engineers to design a complete Ethernet circuit that occupies as little as 1.5 square inches of PCB area (Figure 1). In addition, the CS8900's power-saving features and CMOS design make it a perfect fit for power-sensitive portable and desktop PCs. Motherboard design options include:

- An EEPROM can be used to store node-specific information, such as the Ethernet Individual Address and node configuration.
- The 20 MHz crystal oscillator may be replaced by a 20 MHz clock signal.

Ethernet Adapter Cards

The CS8900's highly efficient PacketPage architecture, with StreamTransfer™ and Auto-Switch DMA options, make it an excellent choice for high-performance, low-cost ISA adapter cards (Figure 2). The CS8900's wide range of configuration options and performance features allow engineers to design Ethernet solutions that meets their particular system requirements. Adapter card design options include:

- A Boot PROM can be added to support diskless applications.
- The 10BASE-T transmitter and receiver impedance can be adjusted to support 100, 120, or 150 Ω twisted pair cables.
- An external Latchable-Address-bus decode circuit can be added to operate the CS8900 in Upper-Memory space.

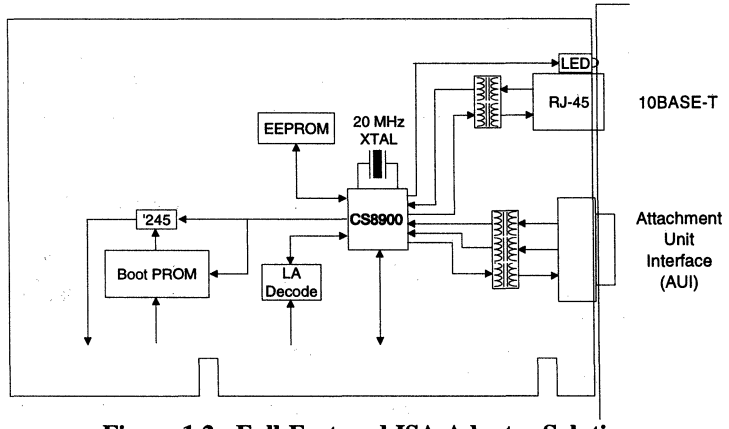


Figure 1.2. Full-Featured ISA Adapter Solution

- On-chip LED ports can be used for either optional LEDs, or as programmable outputs.

1.3 Key Features and Benefits

Very Low Cost

The CS8900 is designed to provide the lowest-cost Ethernet solutions available for ISA desktop motherboards, portable motherboards, and adapter cards. Cost-saving features include:

- Integrated RAM eliminates the need for expensive external memory chips.
- On-chip 10BASE-T filters allow designers to use simple isolation transformers instead of more costly filter/transformer packages.
- The serial EEPROM port, used for configuration and initialization, eliminates the need for expensive switches and jumpers.
- The CS8900 is designed to be used on a 2-layer circuit board instead of a more expensive multi-layer board.
- The 8900-based solution offers the smallest footprint available, saving valuable printed circuit board area.
- A set of certified software drivers is available at no charge, eliminating the need for costly software development.

High Performance

The CS8900 is a full 16-bit Ethernet controller designed to provide optimal system performance by minimizing time on the ISA bus and CPU overhead per frame. It offers equal or superior performance for less money when compared to other Ethernet controllers. The CS8900's PacketPage architecture allows software to select whichever access method is best suited to each particular CPU/ISA-bus configuration. When compared to older I/O-space designs, PacketPage is faster, simpler and more efficient.

To boost performance further, the CS8900 include several key features that increase throughput and lower CPU overhead, including:

- StreamTransfer cuts up to 87% of interrupts to the host CPU during large block transfers.
- Auto-Switch DMA allows the CS8900 to maximize throughput while minimizing missed frames.
- Early interrupts allow the host to preprocess incoming frames.
- On-chip buffering of full frames cuts the amount of host bandwidth needed to manage Ethernet traffic.

Low Power and Low Noise

For low power needs, the CS8900 offers three power-down options: Hardware Standby, Hardware Suspend, and Software Suspend. In Standby mode, the chip is powered down with the exception of the 10BASE-T receiver, which is enabled to listen for link activity. In either Hardware or Software Suspend mode, the receiver is disabled and power consumption drops to the micro-Amp range.

In addition, the CS8900 has been designed for very low noise emission, thus shortening the time required for EMI testing and qualification.

Complete Support

The CS8900 comes with a suite of software drivers for immediate use with most industry standard network operating systems. In addition, complete evaluation kits and manufacturing packages are available, significantly reducing the cost and time required to produce new Ethernet products.

1.4 Typical Connection Diagram

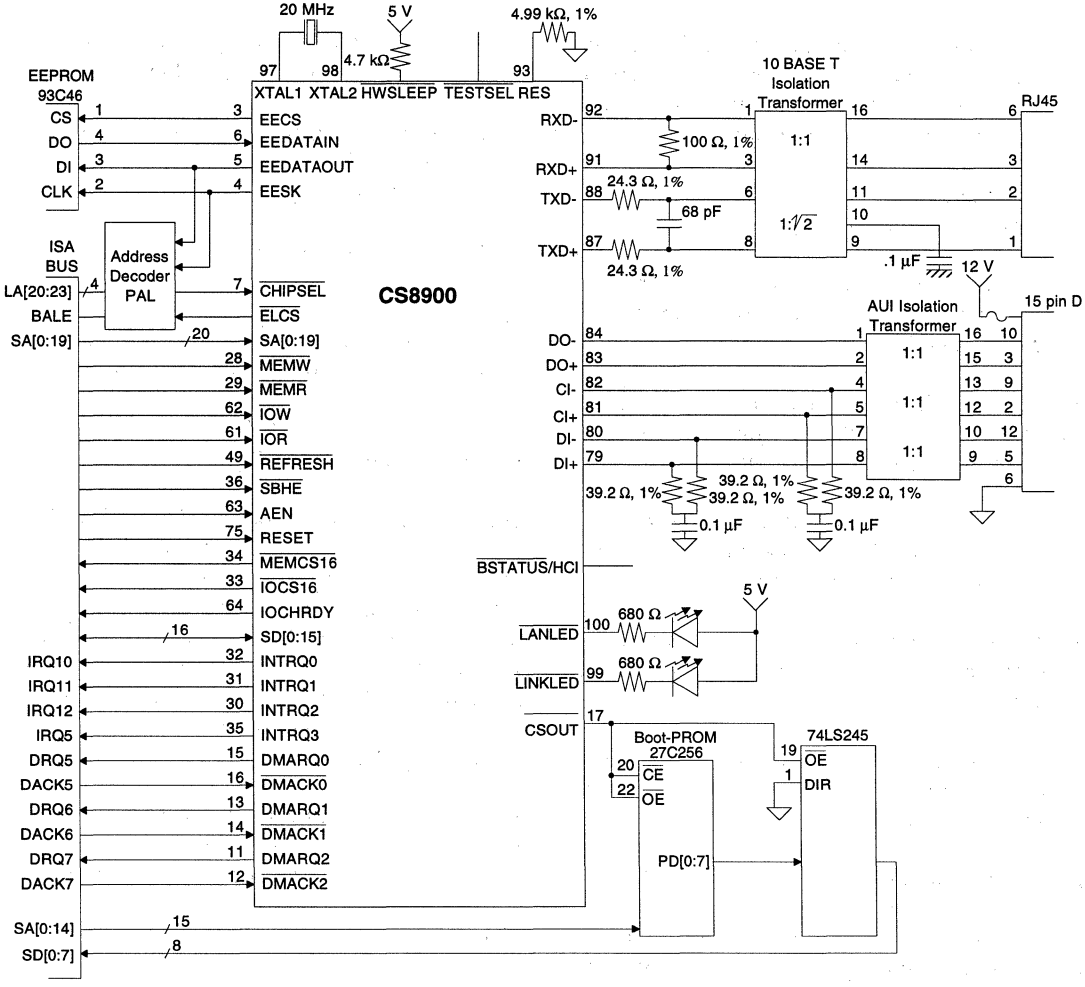
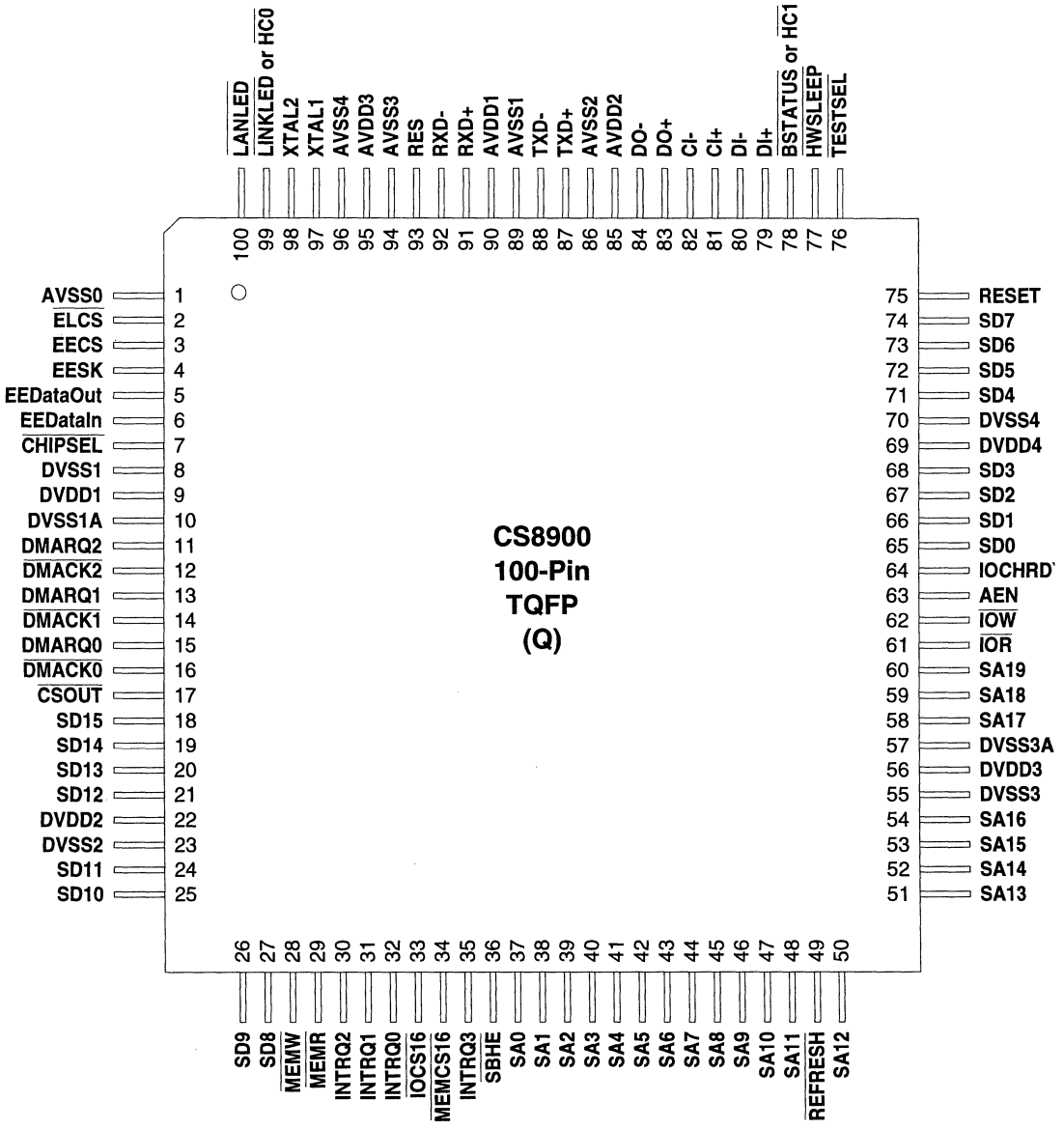


Figure 1.3. Typical Connection Diagram

2.0 PIN DESCRIPTION

2.1 Pin Diagram



2.2 Pin Description

ISA Bus Interface

Symbol	Pin Number	Type	Description
SA0-SA11 SA12-SA16 SA17-SA19	37-48 50-54 58-60	I	**System Address Bus:** Lower 20 bits of the 24-bit System Address Bus used to decode accesses to CS8900 I/O and Memory space, and attached Boot PROM. SA0-SA15 are used for I/O Read and Write operations. SA0-SA19 are used in conjunction with external decode logic for Memory Read and Write operations.
SD0-SD3 SD4-SD7 SD8-SD11 SD12-SD15	65-68 71-74 27-24 21-18	B24	**System Data Bus:** Bi-directional 16-bit System Data Bus used to transfer data between the CS8900 and the host.
RESET	75	I	**Reset:** Active-high asynchronous input used to reset the CS8900. Must be stable for at least 400ns before the CS8900 recognizes the signal as a valid reset.
AEN	63	I	**Address Enable:** When TESTSEL is high, this active-high input indicates to the CS8900 that the system DMA controller has control of the ISA bus. When AEN is high, the CS8900 will not perform slave I/O space operations. When TESTSEL is low, this pin becomes the shift clock input for the Boundary Scan Test.
MEMR	29	I	**Memory Read:** Active-low input indicates that the host is executing a Memory Read operation.
MEMW	28	I	**Memory Write:** Active-low input indicates that the host is executing a Memory Write operation.
MEMCS16	34	OD24	**Memory Chip Select 16-bit:** Open-drain, active-low output generated by the CS8900 when it recognizes an address on the ISA bus that corresponds to its assigned Memory space (CS8900 must be in Memory Mode with the MemoryE bit (Register 17, BusCTL, Bit A) set for MEMCS16 to go active).
REFRESH	49	I	**Refresh:** Active-low input indicates to the CS8900 that a DRAM refresh cycle is in progress. When REFRESH is low, MEMR, MEMW, IOR, IOW, DMACK0, DMACK1, and DMACK2 are ignored.
IOR	61	I	**I/O Read:** When IOR is low and a valid address is detected, the CS8900 outputs the contents of the selected 16-bit I/O register onto the System Data Bus. IOR is ignored if REFRESH is low.
IOW	62	I	**I/O Write:** When IOW is low and a valid address is detected, the CS8900 writes the data on the System Data Bus into the selected 16-bit I/O register. IOW is ignored if REFRESH is low.
IOCS16	33	OD24	**I/O Chip Select 16-bit:** Open-drain, active-low output generated by the CS8900 when it recognizes an address on the ISA bus that corresponds to its assigned I/O space.

Pin Types:

dI	=	Differential Input Pair	I	=	Input	G	=	Ground
dO	=	Differential Output Pair	O	=	Output	ts	=	Tri-State
B	=	Bi-Directional with Tri-State Output	P	=	Power	w	=	Internal Weak Pullup
OD	=	Open Drain Output						

Digital outputs are followed by drive in mA (Example: OD24 = Open Drain Output with 24 mA drive).

ISA Bus Interface (continued)

Symbol	Pin Number	Type	Description
IOCHRDY	64	OD24	**I/O Channel Ready:** When driven low, this open-drain, active-high output extends I/O Read and Memory Read cycles to the CS8900. This output is functional when the IOCHRDYE bit in the Bus Control register (Register 17) is clear. This pin is always high when the IOCHRDYE bit is set.
$\overline{\text{SBHE}}$	36	I	**System Bus High Enable:** Active-low input indicates a data transfer on the high byte of the System Data Bus (SD8-SD15).
INTRQ0 INTRQ1 INTRQ2 INTRQ3	32 31 30 35	O24ts	**Interrupt Request:** Active-high output indicates the presence of an interrupt event. Interrupt Request goes low once the Interrupt Status Queue (ISQ) is read as all 0's. Only one Interrupt Request output is used (selected during configuration). The remaining three Interrupt Request outputs are placed in a high-impedance state. (See sections 3.2 and 4.8.)
DMARQ0 DMARQ1 DMARQ2	15 13 11	O24ts	**DMA Request:** Active-high, tri-stateable output used by the CS8900 to request a DMA transfer. Only one DMA Request output is used (selected during configuration). The remaining two DMA Request outputs are placed in a high-impedance state.
$\overline{\text{DMACK0}}$ $\overline{\text{DMACK1}}$ $\overline{\text{DMACK2}}$	16 14 12	I	**DMA Acknowledge:** Active-low input indicates acknowledgment by the host of the corresponding DMA Request output.
$\overline{\text{CHIPSEL}}$	7	I	**Chip Select:** Active-low input generated by external Latchable Address bus decode logic when a valid memory address is present on the ISA bus. If Memory Mode operation is not needed, $\overline{\text{CHIPSEL}}$ should be tied low.

EEPROM and Boot PROM Interface

Symbol	Pin Number	Type	Description
EESK	4	O4	**EEPROM Serial Clock:** Serial clock used to clock data into or out of the EEPROM.
EECS	3	O4	**EEPROM Chip Select:** Active-high output used to select the EEPROM.
EEDataIn	6	Iw	**EEPROM Data In:** Serial input used to receive data from the EEPROM. Connects to the DO pin on the EEPROM. EEDataIn is also used to sense the presence of the EEPROM.
$\overline{\text{ELCS}}$	2	B4w	**External Logic Chip Select:** Bi-directional signal used to configure external Latchable Address (LA) decode logic. If external LA decode logic is not needed, $\overline{\text{ELCS}}$ should be tied low.
EEDataOut	5	O4	**EEPROM Data Out:** Serial output used to send data to the EEPROM. Connects to the DI pin on the EEPROM. When $\overline{\text{TESTSEL}}$ is low, this pin becomes the output for the Boundary Scan Test.
$\overline{\text{CSOUT}}$	17	O4	**Chip Select for External Boot PROM:** Active-low output used to select an external Boot PROM when the CS8900 decodes a valid Boot PROM memory address.

Pin Types:

dI = Differential Input Pair		I = Input		G = Ground	
dO = Differential Output Pair		O = Output		ts = Tri-State	
B = Bi-Directional with Tri-State Output		P = Power		w = Internal Weak Pullup	
OD = Open Drain Output					

Digital outputs are followed by drive in mA (Example: OD24 = Open Drain Output with 24 mA drive).

10BASE-T Interface

Symbol	Pin Number	Type	Description
TXD+ TXD-	87 88	dO	**10BASE-T Transmit:** Differential output pair drives 10 Mb/s Manchester-encoded data to the 10BASE-T transmit pair.
RXD+ RXD-	91 92	dI	**10BASE-T Receive:** Differential input pair receives 10 Mb/s Manchester-encoded data from the 10BASE-T receive pair.

Attachment Unit Interface (AUI)

Symbol	Pin Number	Type	Description
DO+ DO-	83 84	dO	**AUI Data Out:** Differential output pair drives 10 Mb/s Manchester-encoded data to the AUI transmit pair.
DI+ DI-	79 80	dI	**AUI Data In:** Differential input pair receives 10 Mb/s Manchester-encoded data from the AUI receive pair.
CI+ CI-	81 82	dI	**AUI Collision In:** Differential input pair connects to the AUI collision pair. A collision is indicated by the presence of a 10 MHz +/-15% signal with duty cycle no worse than 60/40.

Pin Types:

dI	=	Differential Input Pair	I	=	Input	G	=	Ground
dO	=	Differential Output Pair	O	=	Output	ts	=	Tri-State
B	=	Bi-Directional with Tri-State Output	P	=	Power	w	=	Internal Weak Pullup
OD	=	Open Drain Output						

Digital outputs are followed by drive in mA (Example: OD24 = Open Drain Output with 24 mA drive).

General Pins

Symbol	Pin Number	Type	Description
XTAL1 XTAL2	97 98	I/O	**Crystal:** A 20 MHz crystal should be connected across these pins. If a crystal is not used, a 20 MHz signal should be connected to XTAL1 and XTAL2 should be left open. (See section 9.0 and 13.0.)
$\overline{\text{HWSLEEP}}$	77	I	**Hardware Sleep:** Active-low input used to enable the two hardware sleep modes: Hardware Suspend and Hardware Standby. (See section 3.7.)
$\overline{\text{LINKLED}}$ or $\overline{\text{HC0}}$	99	OD10	**Link Good LED or Host Controlled Output 0:** When the HCE0 bit of the Self Control register (Register 15) is clear, this active-low output is low when the CS8900 detects the presence of valid link pulses. When the HCE0 bit is set, the host may drive this pin low by setting the HCBO in the Self Control register.
$\overline{\text{BSTATUS}}$ or $\overline{\text{HC1}}$	78	OD10	**Bus Status or Host Controlled Output 1:** When the HCE1 bit of the Self Control register (Register 15) is clear, this active-low output is low when receive activity causes an ISA bus access. When the HCE1 bit is set, the host may drive this pin low by setting the HCB1 in the Self Control register.
$\overline{\text{LANLED}}$	100	OD10	**LAN Activity LED:** During normal operation, this active-low output goes low for 6 ms whenever there is a receive packet, a transmit packet, or a collision. During Hardware Standby mode, this output is driven low when the receiver detects network activity.
$\overline{\text{TESTSEL}}$	76	I	**Test Enable:** Active-low input used to put the CS8900 in Boundary Scan Test mode. For normal operation, this pin should be high.
RES	93	I	**Reference Resistor:** This input should be connected to a 4.99 KΩ +/-1% resistor needed for biasing of internal analog circuits.
DVDD1 DVDD2 DVDD3 DVDD4	9 22 56 69	P	**Digital Power:** Provides 5 V +/- 5% power to the digital circuits of the CS8900.
DVSS1 DVSS1A DVSS2 DVSS3 DVSS3A DVSS4	8 10 23 55 57 70	G	**Digital Ground:** Provides ground reference (0 V) to the digital circuits of the CS8900.
AVDD1 AVDD2 AVDD3	90 85 95	P	**Analog Power:** Provides 5 V +/- 5% power to the analog circuits of the CS8900.
AVSS0 AVSS1 AVSS2 AVSS3 AVSS4	1 89 86 94 96	G	**Analog Ground:** Provide ground reference (0 V) to the analog circuits of the CS8900.

Pin Types:

dI = Differential Input Pair		I = Input		G = Ground	
dO = Differential Output Pair		O = Output		ts = Tri-State	
B = Bi-Directional with Tri-State Output		P = Power		w = Internal Weak Pullup	
OD = Open Drain Output					

Digital outputs are followed by drive in mA (Example: OD24 = Open Drain Output with 24 mA drive).

3.0 FUNCTIONAL DESCRIPTION

3.1 Overview

During normal operation, the CS8900 performs two basic functions: Ethernet packet transmission and reception. Before transmission or reception is possible, the CS8900 must be configured.

Configuration

The CS8900 must be configured for packet transmission and reception at power-up or reset. Various parameters must be written into its internal Configuration and Control registers, such as: Memory Base Address; Ethernet Physical Address; what frame types to receive; and, which media interface to use. Configuration data can either be written to the CS8900 by the host (across the ISA bus), or loaded automatically from an external EEPROM. Operation can begin after configuration is complete.

Sections 3.3 and 3.4 describe the configuration process in detail. Section 4.5 provides a detailed description of the bits in the Configuration and Control Registers.

Packet Transmission

Packet transmission occurs in two phases. The first phase consists of the host moving the Ethernet frame into the CS8900's buffer memory. It begins with the host issuing a Transmit Command, informing the CS8900 that a frame is to be transmitted and telling it when (i.e. after 5, 381, or 1021 bytes or the full frame has been transffered to the CS8900) and how the frame should be sent (i.e. with or without CRC, with or without pad bits, etc.). The Host follows the Transmit Command with the Transmit Length, indicating how much buffer space is required. Once buffer space is available, the host writes the Ethernet frame into the CS8900's internal memory, either as a Memory or I/O space operation.

The second phase of transmission consists of the CS8900 converting the frame into an Ethernet packet, and then transmitting it onto the network. The process starts with the CS8900 transmitting the preamble and Start-of-Frame delimitter as soon as the proper number of bytes has been transfered into its transmit buffer (5, 381, 1021 bytes or full frame, depending on configuration). This is followed by the Destination Address, Source Address, Length field and LLC data (all supplied by the host). If the frame is less than 64 bytes, including CRC, the CS8900 adds pad bits if configured to do so. As a final step, the CS8900 appends the proper 32-bit CRC value.

Section 5.5 provides a detailed decription of packet transmission.

Packet Reception

Like packet transmission, reception occurs in two phases. The first phase consists of the CS8900 receiving an Ethernet packet and storing it in on-chip memory. Packet reception begins with the receive frame passing through the analog front end and Manchester decoder where Manchester data is convered to NRZ data. Next, the preamble and Start-of-Frame delimiter are stripped off and the frame is sent through the address filter. If the frame's Destination Address matches the criteria programmed into the address filter, the packet is stored in the CS8900's internal memory. The CS8900 then checks the CRC, and, depending on the configuration, informs the processor that a frame has been received.

The second phase consists of the host transferring the receive frame across the ISA bus and into host memory. Receive frames can be transfered either as Memory space operations, I/O space operations, or as DMA operations using host DMA. In addition, the CS8900 provides the capability to switch between Memory or I/O

operation and DMA operation by using Auto-Switch DMA and StreamTransfer.

Sections 5.1 through 5.4 provide a detailed description of packet reception.

3.2 ISA Bus Interface

The CS8900 provides a direct interface to ISA buses running at clock rates from 8 to 11 MHz. Its on-chip bus drivers are capable of delivering 24 mA of drive current, allowing the CS8900 to drive the ISA bus directly, without added external "glue logic".

The CS8900 is optimized for 16-bit data transfers, operating in either Memory space, I/O space or as a DMA slave.

Note: ISA-bus operation below 8 MHz should use the CS8900's Receive DMA mode to minimize missed frames. See Section 5.1 for a description of Receive DMA operation.

Memory Mode Operation

When configured for Memory Mode operation, the CS8900's internal RAM is mapped into a contiguous 4-Kbyte block of host memory, providing the host with direct access to the CS8900's internal registers and frame buffers. The host initiates Read operations by driving the $\overline{\text{MEMR}}$ pin low and Write operations by dirving the $\overline{\text{MEMW}}$ pin low.

For additional information about Memory Mode, see section 4.6.

I/O Mode Operation

When configured for I/O Mode operation, the CS8900 is accessed through eight, 16-bit I/O ports that are mapped into 16 contiguous I/O locations in the host system's I/O space. I/O Mode is the default configuration for the CS8900 and is always enabled.

For an I/O Read or Write operation, the AEN pin must be low, and the 16-bit I/O address on the ISA System Address bus (SA0 - SA15) must match the address space of the CS8900. For a Read, $\overline{\text{IOR}}$ must be low, and for a Write, $\overline{\text{IOW}}$ must be low.

For additional information about I/O Mode, see section 4.7.

Interrupt Request Signals

The CS8900 has four interrupt request output pins that can be connected directly to any four of the ISA bus Interrupt Request signals. Only one interrupt output is used at a time. It is selected during initialization by writing the interrupt number (0 to 3) into PacketPage Memory base + 0022h. Unused interrupt request pins are placed in a high-impedance state. The selected interrupt request pin goes high when an enabled interrupt is triggered. The pin goes low after the Interrupt Status Queue (ISQ) is read as all 0's (see section 4.8 for a description of the ISQ).

Table 3.1 presents one possible way of connecting the interrupt iequest pins to the ISA bus that utilizes commonly available interrupts and facilitates board layout.

CS8900 Interrupt Request Pin	ISA Bus Interrupt	PacketPage base + 0022h
INTRQ3 (Pin 35)	IRQ5	0003h
INTRQ0 (Pin 32)	IRQ10	0000h
INTRQ1 (Pin 31)	IRQ11	0001h
INTRQ2 (Pin 30)	IRQ12	0002h

Table 3.1. Interrupt Assignments

DMA Signals

The CS8900 interfaces directly to the host DMA controller to provide DMA transfers of receive frames from CS8900 memory to host memory. The CS8900 has three pairs of DMA pins that can be connected directly to the three 16-bit DMA channels of the ISA bus. Only one DMA channel is used at a time. It is selected during initialization by writing the number of the desired channel (0, 1 or 2) into PacketPage Memory base + 002Ch. Unused DMA pins are placed in a high-impedance state. The selected DMA request pin goes high when the CS8900 has receive frames to transfer to the host memory via DMA. If the DMABurst bit (register 17, BusCTL, Bit B) is set, the pin goes low after the DMA operation is complete. If the DMABurst bit is clear, the pin goes low 32 µs after the start of a DMA transfer.

The DMA pin pairs are arranged on the CS8900 to facilitate board layout. Crystal recommends the configuration in table 3.2 when connecting these pins to the ISA bus.

CS8900 DMA Signal (Pin #)	ISA DMA Signal	PacketPage base + 0024h
DMARQ0 (Pin 15)	DRQ5	0000h
$\overline{\text{DMACK0}}$ (Pin 16)	$\overline{\text{DACK5}}$	
DMARQ1 (Pin 13)	DRQ6	0001h
$\overline{\text{DMACK1}}$ (Pin 14)	$\overline{\text{DACK6}}$	
DMARQ2 (Pin 11)	DRQ7	0002h
$\overline{\text{DMACK2}}$ (Pin 12)	$\overline{\text{DACK7}}$	

Table 3.2. DMA Assignments

For a description of DMA mode, see section 5.2.

3.3 Reset and Initialization

Reset

Seven different conditions cause the CS8900 to reset its internal registers and circuits.

External Reset, or ISA Reset: There is a chip-wide reset whenever the RESET pin is high for at least 400 ns. During a chip-wide reset, all circuitry and registers in the CS8900 are reset.

Power-Up Reset: When power is applied, the CS8900 maintains reset until the voltage at the supply pins reaches approximately 2.5 V. The CS8900 comes out of reset once Vcc is greater than approximately 2.5 V *and* the crystal oscillator has stabilized.

Power-Down Reset: If the supply voltage drops below approximately 2.5 V, there is a chip-wide reset. The CS8900 comes out of reset once the power supply returns to a level greater than approximately 2.5 V *and* the crystal oscillator has stabilized.

EEPROM Reset: There is a chip-wide reset if an EEPROM checksum error is detected (see section 3.4).

Software Initiated Reset: There is a chip-wide reset whenever the RESET bit (Register 15, SelfCTL, Bit 6) is set.

Hardware (HW) Standby or Suspend: The CS8900 goes though a chip-wide reset whenever it enters or exits either HW Standby mode or HW Suspend mode (see section 3.7 for more information about HW Standby and Suspend).

Software (SW) Suspend: Whenever the CS8900 enters SW Suspend mode, all registers and circuits are reset except for the ISA I/O Base Address register (located at PacketPage base + 0020h) and the SelfCTL register (Register 15). Upon exit, there is a chip-wide reset.

Initialization

After each reset (except EEPROM Reset), the CS8900 checks the sense of the EEDataIn pin to see if an external EEPROM is present. If EEDataIn is high, an EEPROM is present and the CS8900 automatically loads the configuration data stored in the EEPROM into its internal registers (see next section). If EEDataIn is low, an EEPROM is not present and the CS8900 comes out of reset with the default configuration shown in table 3.3.

PacketPage Address	Register Contents	Register Description
0020h	0300h	I/O Base Address*
0022h	0000h	Interrupt Number
0024h	0000h	DMA Channel
0026h	0000h	DMA Start of Frame Offset
0028h	0000h	DMA Frame Count
002Ah	0000h	DMA Byte Count
002Ch	0000 0000h	Memory Base Address
0030h	0000 0000h	Boot PROM Base Address
0034h	0000 0000h	Boot PROM Address Mask
0102h	0003h	Register 3 - RxCFG
0104h	0005h	Register 5 - RxCTL
0106h	0007h	Register 7 - TxCFG
0108h	0009h	Register 9 - TxCMD
010Ah	000Bh	Register B - BufCFG
010Ch	000Dh	Reserved
010Eh	000Fh	Reserved
0110h	0011h	Reserved
0112h	0013h	Register 13 - LineCTL
0114h	0015h	Register 15 - SelfCTL
0116h	0017h	Register 17 - BusCTL
0118h	0019h	Register 19 - TestCTL

* I/O base address is unefected by Software Suspend mode.

Table 3.3. Default Configuration

3.4 Configuration with EEPROM

A low-cost serial EEPROM can be used to store configuration information that is loaded into the CS8900 after each reset (except EEPROM reset). The use of an EEPROM is optional and is not needed for all applications (e.g. motherboard designs).

The CS8900 operates with any of six standard EEPROM's shown in table 3.4.

EEPROM Type	Size (16-bit words)
'C46 (non-sequential)	64
'CS46 (sequential)	64
'C56 (non-sequential)	128
'CS56 (sequential)	128
'C66 (non-sequential)	256
'CS66 (sequential)	256

Table 3.4. Supported EEPROM Types

The interface to the EEPROM consists of four signals shown in table 3.5.

CS8900 Pin (Pin #)	CS8900 Function	EEPROM Pin
EECS (Pin 3)	EEPROM Chip Select	Chip Select
EESK (Pin 4)	1 MHz EEPROM Serial Clock output	Clock
EEDataOut (Pin 5)	EEPROM Data Out (data to EEPROM)	Data In
EEDataIn (Pin 6)	EEPROM Data In (data from EEPROM)	Data Out

Table 3.5. EEPROM Interface

EEPROM Readout

After reset, if the EEDataIn pin is high, the CS8900 reads the first word of EEPROM data by:

1. asserting EECS;

2. clocking out a Read-Register-00h command on EEDataOut (EESK provides a 1 MHz serial clock signal); and
3. clocking the data in on EEDataIn.

The first word of data in the EEPROM determines: if the data in the EEPROM is valid; what type of EEPROM it is; and, how many bytes of configuration data are stored in the EEPROM.

Checking for Valid EEPROM data: The presence of valid EEPROM data is indicated by a readout of either a binary 101X-XXX0 or 101X-XXX1 as the low byte of the first word (X = do not care). Any other readout value terminates initialization from the EEPROM. If an EEPROM is attached but is not to be used for configuration, Crystal recommends that the low byte of the first word be programmed with 00h.

Note: The LSB of 0 (101X-XXX0) indicates a sequential EEPROM (i.e. once the EEPROM is given an address, successive readouts are from sequential addresses without giving the EEPROM a new address). The LSB of 1 (101X-XXX1) indicates a non-sequential EEPROM (i.e. requires an address before each readout). The CS8900 works equally well with either a sequential or non-sequential EEPROM.

Determining EEPROM Type: The CS8900 determines the EEPROM type by checking the sense of EEDataIn on the tenth rising edge of EESK. If EEDataIn is low, the EEPROM is a 'C46 or 'CS46. If EEDataIn is high, the EEPROM is a 'C56, 'CS56, 'C66, or 'CS66.

Determining Number of Bytes to be read from the EEPROM: The high byte of the first word stored in the EEPROM is known as the Link Byte. It indicates how many bytes in the EEPROM are to be used for configuration. The Link Byte does not include the first two bytes stored in the EEPROM (the two bytes at EEPROM address 00h). Link Byte values of 00h, 01h, and 02h are not allowed.

EEPROM Memory Organization

Configuration data stored in the EEPROM is organized as a contiguous block of 16-bit words. The first word (described above) is used to determine the type of EEPROM and the number of bytes of configuration data it contains. The remaining words are organized into one or more groups of words. The first word in each group indicates the number of words in that group, as well as where in PacketPage memory space the remaining words in the group are to be loaded. Figure 3.1 show the format of the first word in each group.

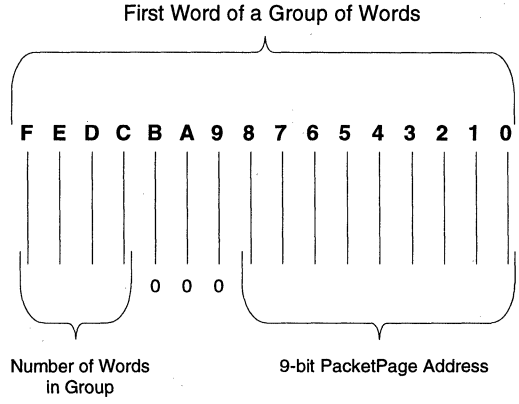


Figure 3.1. First Word in Group

Number of words in each group: The number of words in each group, including the first word in the group, is 2 greater than the value stored in bits F through C (e.g. if bits F through C contain 0001, there are three words in the group).

9-bit PacketPage Address: The 9-bit PacketPage Address defines the starting location in the CS8900's internal memory space where the group of words is to be stored (Bits B though 9

are forced to 0, restricting the address range to the first 512 bytes of PacketPage memory space).

Loading Configuration Data

After the CS8900 reads the first word in the group, it transfers the remaining words in the group into its internal registers. The low byte of the first word transferred is stored at the address indicated by the 9-bit PacketPage address. The remaining bytes in the group are stored in successive PacketPage memory locations.

EEPROM Checksum

Once the CS8900 has processed all of the configuration data stored in the EEPROM, it performs a checksum calculation to verify that the configuration is valid. To do this, it sums, without carry, all of the bytes of configuration data in the EEPROM, from address 00h through the Checksum Value. If the resulting total is 0, the readout is valid. If the total is not 0, the readout is not valid and the CS8900 initiates a partial reset to restore the default configuration.

The Checksum Value (stored in the low byte position of the last word in the data block) is the 2's complement of the addition, without carry, of all the bytes preceding it, including the first word at address 00h. The EEPROM address of the Checksum Value is determined by dividing the value stored in the Link Byte by 2 (to convert the byte count to the word count).

EEPROM Readout Completion

Once the readout of the EEPROM is complete, the INITD bit (Register 16, SelfST, bit 7) is set. The EEPROMOK bit (Register 16, SelfST, bit A) is set if the readout and checksum are correct, and is clear if the default configuration is used (see table 3.3 for default configuration).

EEPROM Example

Table 3.6 on the following page shows a simple example of how configuration data is stored in the EEPROM. The example is for a 'C46 EEPROM, with "little endian" byte ordering.

Word Address	Value	Description
		FIRST WORD in DATA BLOCK
00h	A120h	The low byte, A1h, indicates a 'C46 EEPROM is attached. The high byte, 20h, indicates the number of bytes to be used in this block of configuration data.
		FIRST GROUP of WORDS
01h	2020h	Three words to be loaded, beginning at 0020h in PacketPage memory.
02h	0300h	I/O Base Address
03h	0003h	Interrupt Number
04h	0001h	DMA Channel Number
		SECOND GROUP of WORDS
05h	502Ch	Six words to be loaded, beginning at 002Ch in PacketPage memory.
06h	E000h	Memory Base Address - low word
07h	000Fh	Memory Base Address - high word
08h	0000h	Boot PROM Base Address - low word
09h	000Dh	Boot PROM Base Address - high word
0Ah	C000h	Boot PROM Address Mask - low word
0Bh	000Fh	Boot PROM Address Mask high word
		THIRD GROUP of WORDS
0Ch	2158h	Three words to be loaded, beginning at 0158h in PacketPage memory.
0Dh	0010h	Individual Address - low word
0Eh	0000h	Individual Address - middle word
0Fh	0000h	Individual Address - high word
		CHECKSUM Value
10h	2900h	The high byte, 29h, is the Checksum Value. In this example, the checksum includes word addresses 00h through 0Fh. The hexadecimal sum of the bytes is D7h, resulting in a 2's complement of 29h. The low byte, 00h, provides a pad to the word boundary.
11h	FFFFh	End of data blocks*.

*FFFFh is a special code indicating that there are no more words in the EEPROM.

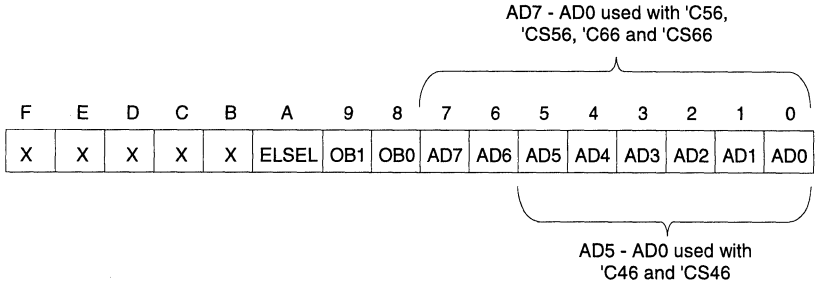
Table 3.6. EEPROM Example

3.5 Programming the EEPROM

After initialization, the host can access the EEPROM through the CS8900 by writing one of seven commands to the EEPROM Command register (PacketPage base + 0040h). Figure 3.2 shows the format of the EEPROM commands.

EEPROM Commands

The seven commands used to access the EEPROM are: Read, Write, Erase, Erase/Write Enable, Erase/Write Disable, Erase-All, and Write-All. They are described in table 3.7.



Bit	Name	Description
[F:B]		Reserved
[A]	ELSEL	**External Logic Select:** When clear, the EECS pin is used to select the EEPROM. When set, the ELCS pin is used to select the external LA decode circuit.
[9:8]	OB1, OB0	**Opcode:** Indicates what command is being executed (see next section).
[7:0]	AD7 to AD0	**EEPROM Address:** Address of EEPROM word being accessed.

Figure 3.2. EEPROM Command Format

Command	Opcode (bits 9,8)	EEPROM Address (bits 7 to 0)	Data	EEPROM Type	Execution Time
Read Register	1,0	word address	yes	all	25 µs
Write Register	0,1	word address	yes	all	10 ms
Erase Register	1,1	word address	no	all	10 ms
Erase/Write Enable	0,0	XX11-XXXX	no	'CS46, 'C46	9 µs
		11XX-XXXX	no	'CS56, 'C56, 'CS66, 'C66	9 µs
Erase/Write Disable	0,0	XX00-XXXX	no	'CS46, 'C46	9 µs
	0,0	00XX-XXXX	no	'CS56, 'C56, 'CS66, 'C66	9 µs
Erase-All Registers	0,0	XX10-XXXX	no	'CS46, 'C46	10 ms
	0,0	10XX-XXXX	no	'CS56, 'C56, 'CS66, 'C66	10 ms
Write-All Registers	0,0	XX01-XXXX	yes	'CS46, 'C46	10 ms
	0,0	01XX-XXXX	yes	'CS56, 'C56, 'CS66, 'C66	10 ms

Table 3.7. EEPROM Commands

EEPROM Command Execution

During the execution of a command, the two Opcode bits, followed by six bits of address (for a 'C46 or 'CS46) or eighth bits of address (for a 'C56, 'CS56, 'C66 or 'CS66), are shifted out of the CS8900, into the EEPROM. If the command is a Write, the data in the EEPROM Data register (PacketPage base + 0042h) follows. If the command is a Read, the data in the specified EEPROM location is written into the EEPROM Data register. If the command is an Erase or Erase-All, no data is transferred to or from the EEPROM Data register. Before issuing any command, the host must wait for the SI-BUSY bit (Register 16, SelfST, bit 8) to clear. After each command has been issued, the host must wait again for SI-BUSY to clear.

Enabling Access to the EEPROM

The Erase/Write Enable command provides protection from accidental writes to the EEPROM. The host must write an Erase/Write Enable command before it attempts to write to or erase any EEPROM memory location. Once the host has finished altering the contents of the EEPROM, it must write an Erase/Write Disable command to prevent unwanted modification of the EEPROM.

Writing and Erasing the EEPROM

To write data to the EEPROM, the host must execute the following series of commands:

1. Issue an Erase/Write Enable command.
2. Issue an Erase command.
3. Load the data into the EEPROM Data register.
4. Issue a Write command.
5. Issue an Erase/Write Disable command.

During the Erase command, the CS8900 writes FFh to the specified EEPROM location. During the Erase-All command, the CS8900 writes FFh to all locations. During the Write and Write-All commands, the CS8900 writes only the "0" bits (i.e. those bits whose value is to be 0). As such, the host must issue an Erase command before writing a new value to the EERPOM.

Storing Additional Data in the EEPROM

If there is sufficient room, the user may store additional data in the EEPROM (up to address 7Fh, depending on EEPROM size). However, the first block of data in the EEPROM is always used for the CS8900, and address space 80h to AFh is reserved.

3.6 Boot PROM Operation

The CS8900 supports an optional Boot PROM used to store code for remote booting from a network server.

Accessing the Boot PROM

To retrieve the data stored in the Boot PROM, the host issues a Read command to the Boot PROM's memory space, either as a Memory or I/O space access. The CS8900 decodes the command and drives the $\overline{\text{CSOUT}}$ pin low, causing the data stored in the Boot PROM to be shifted into the bus transceiver. The bus transceiver then drives the data out onto the ISA bus.

Configuring the CS8900 for Boot PROM Operation

Figure 3.3 show how the CS8900 should be connected to the Boot PROM and '245 driver. To configure the CS8900's internal registers for Boot PROM operation, the Boot PROM Base Address must be loaded into the Boot PROM Base Address register (PacketPage base + 0030h) and the Boot PROM Address Mask must be loaded into the BootPROM Address Mask register (PacketPage base + 0034h). The Boot PROM

Base Address provides the starting location in host memory where the Boot PROM is mapped. The Boot PROM Address Mask indicates the size of the attached Boot PROM and is limited to 4 Kbyte increments. The lower 12 bits of the Address Mask are ignored and should be 000h.

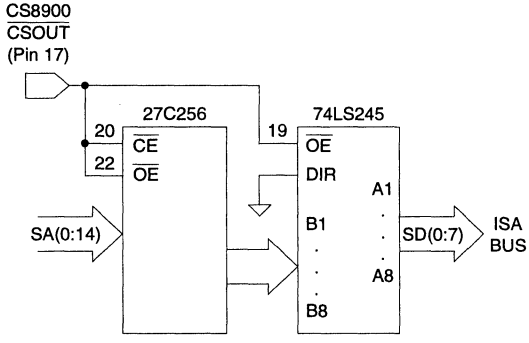


Figure 3.3. Boot PROM Connection Diagram

In the EEPROM example shown in table 3.6, the Boot PROM starting address is D0000h and the Address Mask is FC000h. This configuration describes a 16 Kbyte (128 Kbit) PROM mapped into host memory from D0000h to D3FFFh.

3.7 Low-Power Modes

For power-sensitive applications, the CS8900 supports three low-power modes: Hardware Standby, Hardware Suspend, and Software Suspend. All three low-power modes are controlled through the SelfCTL register (Register 15).

Hardware Standby

Hardware (HW) Standby is designed for use in systems, such as portable PC's, that may be temporarily disconnected from the 10BASE-T cable. It allows the system to conserve power while the LAN is not in use, and then automatically restore Ethernet operation once the cable is reconnected.

In HW Standby mode, all analog and digital circuitry in the CS8900 is turned off, except for the 10BASE-T receiver which remains active to listen for link activity. If link activity is detected, the LANLED pin is driven low, providing an indication to the host that the network connection is active. The host can then activate the CS8900 by de-asserting the HWSLEEP pin. During this mode, all ISA bus accesses are ignored.

To enter HW Standby mode, the HWSLEEP pin must be low *and* the HWSleepE bit (Register 15, SelfCTL, Bit 9) *and* the HWstandbyE bit (Register 15, SelfCTL, Bit A) must be set. When the CS8900 enters HW Standby, all registers and circuits are reset except for the SelfCTL register. Upon exit from HW Standby, the CS8900 performs a complete reset, and then goes through normal initialization.

Hardware Suspend

During Hardware Suspend mode, the CS8900 uses the least amount of current of the three low-power modes. All internal circuits are turned off and the CS8900's core is electronically isolated from the rest of the system. Accesses from the ISA bus and Ethernet activity are both ignored.

HW Suspend mode is entered by driving the HWSLEEP pin low and setting the HWSleepE bit (Register 15, SelfCTL, bit 9) while the HWstandbyE bit (Register 15, SelfCTL, bit A) is clear. To exit from this mode, the HWSLEEP pin must be driven high. Upon exit, the CS8900 performs a complete reset, and then goes through a normal initialization procedure.

Software Suspend

Software (SW) Suspend mode can be used to conserve power in applications, like adapter cards, that do not have power management circuitry available. During this mode, all internal circuits are shut off except the I/O Base Address register (PacketPage base + 0020h) and the SelfCTR register (Register 15).

To enter SW Suspend mode, the host must set the SWSuspend bit (Register 15, SelfCTL, bit 8). To exit SW Suspend, the host must write to the CS8900's assigned I/O space (the Write is only used to wake the CS8900, the Write itself is ignored). Upon exit, the CS8900 performs a complete reset, and then goes through a normal initialization procedure.

Any harware reset takes the chip out of any sleep mode.

Table 3.8 describes the how to enter and exit the three low-power modes.

3.8 LED Outputs

The CS8900 provides three output pins that can be used to control LEDs or external logic.

$\overline{\text{LANLED}}$: $\overline{\text{LANLED}}$ goes low whenever the CS8900 transmits or receives a frame, or when it detects a collision. $\overline{\text{LANLED}}$ remains low until there has been no activity for 6 ms (i.e. each transmission, reception, or collision produces a pulse lasting a minimum of 6 ms).

$\overline{\text{LINKLED}}$ or $\overline{\text{HC0}}$: $\overline{\text{LINKLED}}$ or $\overline{\text{HC0}}$ can be controlled by either the CS8900 or the host. When controlled by the CS8900, $\overline{\text{LINKLED}}$ is low whenever the CS8900 receives valid 10BASE-T link pulses. To configure this pin for CS8900 control, the HC0E bit (Register 15, SelfCTL, Bit C) must be clear. When controlled by the host, $\overline{\text{LINKLED}}$ is low whenever the HCB0 bit (Register 15, SelfCTL, Bit E) is set. To configure it for host control, the HC0E bit must be set. Table 3.9 summarizes this operation.

CS8900 Configuration					CS8900 Operation
HWSLEEP (Pin 77)	HWstandbyE (SelfCTL, Bit A)	HWSleepE (SelfCTL, Bit 9)	SWSuspend (SelfCTL, Bit 8)	Link Activity	
Low	1	1	N/A	Not Present	HW Standby mode: 10BASE-T receiver listens for link activity
Low	1	1	N/A	Present	HW Standby mode: $\overline{\text{LANLED}}$ low
Low	0	1	N/A	N/A	HW Suspend mode
Low to High	N/A	1	0	N/A	CS8900 resets and goes through Initialization
High	N/A	N/A	0	N/A	Not in low-power mode
High	N/A	N/A	1	N/A	SW Suspend mode
Low	N/A	0	1	N/A	SW Suspend mode
Low	N/A	0	0	N/A	Not in low-power mode

Note: Both HW Standby and HW Suspend take precedence over SW Suspend.

Table 3.8. Low-Power Mode Operation

HC0E (Bit C)	HCB0 (Bit E)	Pin Function
0	N/A	Pin configured as $\overline{\text{LINKLED}}$: Output is low when valid 10BASE-T link pulses are detected. Output is high if valid link pulses are not detected
1	0	Pin configured as $\overline{\text{HC0}}$: Output is high
1	1	Pin configured as $\overline{\text{HC0}}$: Output is low

Table 3.9. $\overline{\text{LINKLED}}$/$\overline{\text{HCO}}$ Pin Operation

$\overline{\text{BSTATUS}}$ or $\overline{\text{HC1}}$: $\overline{\text{BSTATUS}}$ or $\overline{\text{HC1}}$ can be controlled by either the CS8900 or the host. When controlled by the CS8900, $\overline{\text{BSTATUS}}$ is low whenever the host reads the RxEvent register (PacketPage base + 0124h), signaling the transfer of a receive frame across the ISA bus. To configure this pin for CS8900 control, the HC1E bit (Register 15, SelfCTL, Bit D) must be clear. When controlled by the host, $\overline{\text{BSTATUS}}$ is low whenever the HCB1 bit (Register 15, SelfCTL, Bit F) is set. To configure it for host control, HC1E must be set. Table 3.10 summarizes this operation.

HC1E (Bit D)	HCB1 (Bit F)	Pin Function
0	N/A	Pin configured as $\overline{\text{BSTATUS}}$: Output is low when a receive frame begins transfer across the ISA bus. Output is high otherwise.
1	0	Pin configured as $\overline{\text{HC1}}$: Output is high
1	1	Pin configured as $\overline{\text{HC1}}$: Output is low

Table 3.10. $\overline{\text{BSTATUS}}$/$\overline{\text{HC1}}$ Pin Operation

LED Connection

Each LED output is capable of sinking 10 mA to drive an LED directly through a series resistor. The output voltage of each pin is less than 0.4 V when the pin is low. Figure 3.4 shows a typical LED circuit.

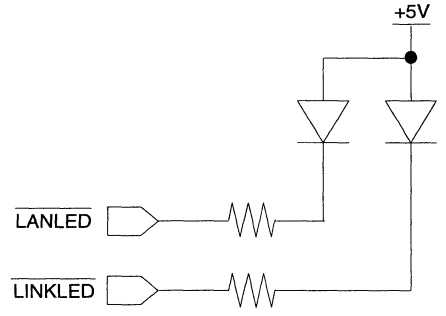


Figure 3.4. LED Connection Diagram

3.9 Media Access Control

Overview

The CS8900's Ethernet Media Access Control (MAC) engine is fully compliant with the IEEE 802.3 Ethernet standard (ISO/IEC 8802-3, 1993). It handles all aspects of Ethernet frame transmission and reception, including: collision detection, preamble generation and detection, and CRC generation and test. Programmable MAC features include automatic retransmission on collision, and padding of transmitted frames.

Figure 3.5 shows how the MAC engine interfaces to other CS8900 functions. On the host side, it interfaces to the CS8900's internal data/address/control bus. On the network side, it interfaces to the internal Manchester encoder/decoder (ENDEC). The primary functions of the MAC are: frame encapsulation and decapsulation; error detection and handeling; and, media access management.

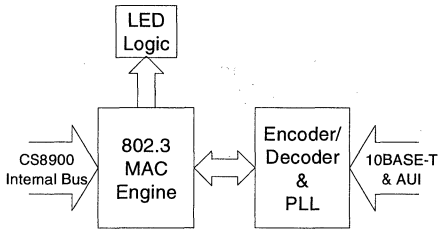


Figure 3.5. MAC Interface

Frame Encapsulation and Decapsulation

The CS8900's MAC engine automatically assembles transmit packets and disassembles receive packets. It also determines if transmit and receive frames are of legal minimum size.

Transmission: Once the proper number of bytes have been transferred to the CS8900's memory (either 5, 381, 1021 bytes, or full frame), and providing that access to the network is permitted, the MAC automatically transmits the 7-byte preamble (1010101b...), followed by the Start-of-Frame Delimiter (SFD, 10101011b), and then the serialized frame data. It then transmits the Frame Check Sequence (FCS). The data after the SFD and before the FCS (Destination Address, Source Address, Length, and data field) is supplied by the host. FCS generation by the CS8900 may be disabled by setting the InhibitCRC bit (Register 9, TxCMD, bit C).

Figure 3.6 shows the Ethernet frame format.

Reception: The MAC receives the incoming packet as a serial stream of NRZ data from the Manchester encoded/decoder. It disregards the first 8 bits of data and then begins checking for the SFD. Once the SFD is detected, the MAC assumes all subsequent bits are frame data. It reads the DA and compares it to the criteria programmed into the address filter (see section 4.9 for a description of Address Filtering). If the DA passes the address filter, the frame is loaded into the CS8900's memory. If the BufferCRC bit (Register 3, RxCFG, bit B) is set, the received FCS is also loaded into memory. Once the entire packet has been received, the MAC validates the FCS. If an error is detected, the CRCerror bit (Register 4, RxEvent, Bit C) is set.

Enforcing Minimum Frame Size: The MAC provides minimum frame size enforcement of both transmit and receive packets. When the TxPadDis bit (Register 9, TxCMD, Bit D) is clear, transmit frames will be padded with additional bits to ensure that the receiving station receives a legal frame (64 bytes, including CRC). When TxPadDis is set, the CS8900 will not add pad bits and will transmit frames less that 64 bytes. If a frame is received that is less than 64 bytes (including CRC), the Runt bit (Register 4, RxEvent, Bit D) will be set indicating the arrival of an illegal frame.

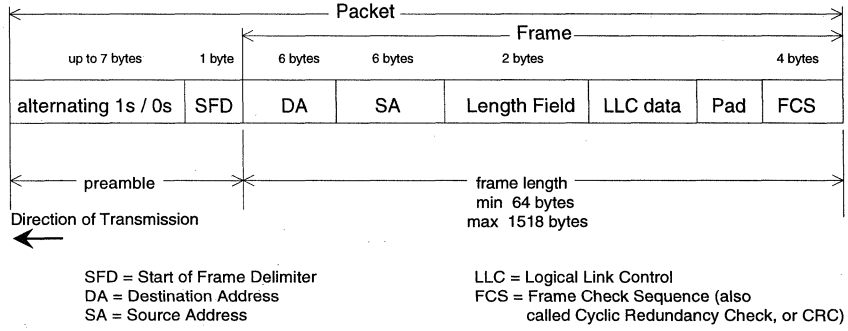


Figure 3.6. Ethernet Frame Format

Transmit Error Detection and Handling

The MAC engine monitors Ethernet activity and reports and recovers from a number of error conditions. For transmission, the MAC reports the following errors in the TxEvent register (Register 8) and BufEvent register (Register C):

Loss of Carrier: Whenever the CS8900 is transmitting on the AUI port, it expects to see its own transmission "looped back" to its receiver. If it is unable to monitor its transmission after the end of the preamble, the MAC reports a loss-of-carrier error by setting the Loss-of-CRS bit (Register 8, TxEvent, Bit 6). If the Loss-of-CRSiE bit (Register 7, TxCFG, Bit 6) is set, the host will be interrupted.

SQE Error: After the end of transmission on the AUI port, the MAC expects to see a collision within 64 bit times. If no collision is detected, the SQEerror bit (Register 8, TxEvent, Bit 7) is set. If the SQEerroriE bit is set (Register 7, TxCFG, Bit 7), the host is interrupted. An SQE error may indicate a fault on the AUI cable or a faulty transceiver (it is assumed that the attached transceiver supports this function).

Out-of-Window (Late) Collision: If a collision is detected after the first 512 bits have been transmitted, the MAC reports a late collision by setting the Out-of-window bit (Register 8, TxEvent, Bit 9). The MAC then forces a bad CRC and terminates the transmission. If the Out-of-windowiE bit (Register 7, TxCFG, Bit 9) is set, the host is interrupted. A late collision may indicate an illegal network configuration.

Jabber Error: If a transmission continues longer than about 26 ms, the MAC disables the transmitter and sets the Jabber bit (Register 8, TxEvent, Bit A). The output of the transmitter returns to idle and remains there until the host issues a new Transmit Command. If the JabberiE bit (Register 7, TxCFG, Bit A) is set, the host is interrupted. A Jabber condition inticates that there may be something wrong with the CS8900 transmit function To prevent possible network faults, the host should clear the transmit buffer. Possible options include:

- Reset the chip with either software or hardware reset (see section 3.3).
- Issue a Force Transmit Command by setting the Force bit (Register 9, TxCMD, bit 8).
- Issue a Transmit Command with the TxLength field set to zero.

Transmit Collision: The MAC counts the number of times an individual packet must be re-transmitted due to network collisions. The collision count is stored in bits B through E of the TxEvent register (Register 8). If the packet collides 16 times, transmission of that packet is terminated and the 16coll bit (Register 8, TxEvent, Bit F) is set. If the 16colliE bit (Register 7, TxCFG, Bit F) is set, the host will be interrupted on the 16th collision. A running count of transmit collisions is recorded in the TxCOL register (Register 12).

Transmit Underrun: If the CS8900 starts transmission of a packet but runs out of data before reaching the end of frame, the TxUnderrun bit (Register C, BufEvent, Bit 9) is set. The MAC then forces a bad CRC and terminates the transmission. If the TxUnderruniE bit (Register B, BufCFG, Bit 9) is set, the host is interrupted.

Receive Error Detection and Handling

The following receive errors are reported in the RxEvent register (Register 4):

CRC Error: If a frame is received with a bad CRC, the CRCerror bit (Register 4, RxEvent, Bit C) is set. If the CRCerrorA bit (Register 5, RxCTL, Bit C) is set, the frame will be buffered by CS8900. If the CRCerroriE bit (Register 3, RxCFG. Bit C) is set, the host is interrupted.

Runt Frame: If a frame is received that is shorter than 64 bytes, the Runt bit (Register 4, RxEvent, Bit D) is set. If the RuntA bit (Register 5, RxCTL, Bit D) is set, the frame will still be buffered by CS8900. If the RuntiE bit (Register 3, RxCFG. Bit D) is set, the host is interrupted.

Extra Data: If a frame is received that is longer than 1518 bytes, the Extradata bit (Register 4, RxEvent, Bit E) is set. If the ExtradataA bit (Register 5, RxCTL, Bit E) is set, the first 1518 bytes of the frame will still be buffered by CS8900. If the ExtradataiE bit (Register 3, RxCFG. Bit E) is set, the host is interrupted.

Dribble Bits and Alignment Error: Under normal operating conditions, the MAC may detect up to 7 additional bits after the last full byte of a receive packet. These bits, known as dribble bits, are ignored. If dribble bits are detected, the Dribblebit bit (Register 4, RxEvent, Bit 7) is set. If both the Dribblebit bit and CRCerror bit (Register 4, RxEvent, Bit C) are set at the same time, an alignment error has occurred.

Media Access Management

The Ethernet network topology is a single shared medium with several attached stations. The Ethernet protocol is designed to allow each station equal access to the network at any given time. Any node can attempt to gain access to the network by first completing a deferral process (described below) after the last network activity, and then transmitting a packet that will be received by all other stations. If two nodes transmit simultaneously, a collision occurs and the colliding packets are corrupted. Two primary tasks of the MAC are to avoid network collisions, and then recover from them when they occur. In addition, when the CS8900 is using the AUI, the MAC must support the SQE Test funtion described in section 7.2.4.6 of the Ethernet standard.

Collision Avoidance: The MAC continually monitors network traffic by checking for the presence of carrier activity (carrier activity is indicated by the assertion of the internal Carrier Sense signal generated by the ENDEC). If carrier activity is detected, the network is assumed busy and the MAC must wait until the current packet is finished before attempting transmission. The CS8900 support two schemes for determining when to initiate transmission: Two-Part Deferral, and Simple Deferral. Selection of the deferral scheme is determined by the 2-part-DefDis bit (Register 13, LineCTL, Bit D). If the 2-partDefDis bit is clear, the MAC uses a two-part deferral process defined in section 4.2.3.2.1 of the Ethernet standard (ISO/IEC 8802-3, 1993). If the 2-partDefDis bit is set, the MAC uses a simplified deferral scheme. Both schemes are described below:

- ***Two-Part Deferral:*** In the two-part deferral process, the 9.6 µs Inter Packet Gap (IPG) timer is started whenever the internal Carrier Sense signal is de-asserted. If activity is detected during the first 6.4 µs of the IPG timer, the timer is reset and then restarted once the activity has stopped. If there is no activity during the first 6.4 µs of the IPG timer, the IPG timer is allowed to time out (even if network activity is detected during the final 3.2 µs). The MAC then begins transmission if a transmit packet is ready and if it is not in Backoff (Backoff is described later in this section). If no transmit packet is pending, the MAC continues to monitor the network. If activity is detected before a transmit frame is ready, the MAC defers to the transmitting station and resumes monitoring the network.

  The two-part deferral scheme was developed to prevent the posibility of the IPG being shortened due to a temporary loss of carrier. Figure 3.7 diagrams the two-part deferral process.

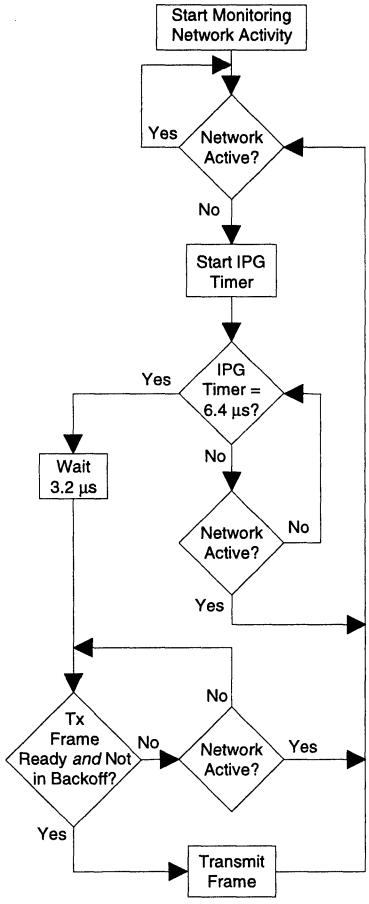


Figure 3.7. Two-Part Deferral

- ***Simple Deferral:*** In the simple deferral scheme, the IPG timer is started whenever Carrier Sense is de-asserted. Once the IPG timer is finished (after 9.6 µs), if a transmit frame is pending and if the MAC is not in Backoff, transmission begins (even if network activity is detected during the 9.6 µs IPG). If no transmit packet is pending, the MAC continues to monitor the network. If activity is detected before a transmit frame is ready, the MAC defers to the transmitting station and resumes monitoring the network.

Figure 3.8 diagrams the simple deferral process.

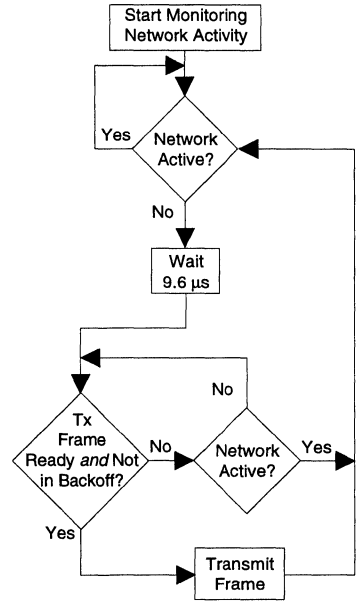


Figure 3.8. Simple Deferral

Collision Resolution: If a collision is detected while the CS8900 is transmitting, the MAC responds in one of three ways depending on whether it is a normal collision (within the first 512 bits of transmission) or a late collision (after the first 512 bits of transmission):

- ***Normal Collisions:*** If a collision is detected before the end of the preamble and SFD, the MAC finishes the preable and SFD, transmits the jam sequence (32-bit pattern of all 0's), and then initiates Backoff. If a collision is detected after the transmission of the preamble and SFD but before 512 bit times, the MAC immediately terminates transmission, transmits the jam sequence, and then initiates Backoff. In either case, if the Onecoll bit (Register 9, TxCMD, Bit 9) is clear, the MAC will attempt to transmit a packet a total of 16 times (the initial attempt plus 15 re-

transmissions) due to normal collisions. On the 16th collision, it sets the 16coll bit (Register 8, TxEvent, Bit F) and discards the packet. If the Onecoll bit is set, the MAC discards the packet without attempting any re-transmission.

- ***Late Collisons:*** If a collision is detected after the first 512 bits have been transmitted, the MAC immediately terminates transmission, transmits the jam sequence, discards the packet, and sets the Out-of-window bit (Register 8, TxEvent, Bit 9). The CS8900 does not initiate backoff or attemp to re-transmit the frame. For additonal information about Late Collisions, see *Out-of-Window Error* in this section.

Backoff: After the MAC has completed transmitting the jam sequence, it must wait, or "Back off", before attemping to transmit again. The amount of time it must wait is determined by one of two Backoff alogorithms: the Standard Backoff algorithm (ISO/IEC 4.2.3.2.5) or the Modified Backoff algorithm. The host selects which algorithm through the ModBackoffE bit (Register 13, LineCTL, Bit B).

- ***Standard Backoff:*** The Standard Backoff algorithm, also called the "Truncated Binary Exponential Backoff", is described by the equation:

$$0 \le r \le 2^k$$

where r (a random integer) is the number of slot times the MAC must wait (1 slot time = 512 bit times), and k is the smaller of n or 10, where n is the number of re-transmission attempts.

- ***Modified Backoff:*** The Modified Backoff is described by the equation:

$$0 \le r \le 2^k$$

where r (a random integer) is the number of slot times the MAC must wait, and k is 3 for $n < 3$ and k is the smaller of n or 10 for $n \ge 3$, where n is the number of re-transmission attempts.

The advantage of the Modified Backoff algorithm over the Standard is that it reduces the possibility of multiple collisions on the first three re-tries. The disadvantage is that it extends the maximum time needed to gain access to the network for the first three re-tries.

The host may choose to disable the Backoff algorithm altogether by setting the DisableBackoff bit (Register 19, TestCTL, Bit B). When disabled, the CS8900 only waits the 9.6 µs IPG time before starting transmission.

SQE Test: If the CS8900 is transmitting on the AUI, the external transceiver should generate an SQE Test signal on the CI+/CI- pair following each transmission. The SQE Test is a 10 MHz signal lasting 5 to 15 bit times and starting within 0.6 to 1.6 µs after the end of transmission. During this period, the CS8900 ignores receive carrier activity (see SQE Error in this section for more information).

3.10 Encoder/Decoder (ENDEC)

The CS8900's integrated encoder/decoder (ENDEC) circuit is compliant with section 7 of the Ethernet standard (ISO/IEC 8802-3, 1993). Its primary functions include:

- Manchester encoding of transmit data;
- informing the MAC when valid receive data is present (Carrier Detection); and,
- recovering the clock and NRZ data from incoming Manchester-encoded data.

Figure 3.9 provides a block diagram of the ENDEC and how it interfaces to the MAC, AUI and 10BASE-T transceiver.

Encoder

The encoder converts NRZ data from the MAC and a 20 MHz Transmit Clock signal into a serial stream of Manchester data. The Transmit Clock is produced by an on-chip oscillator circuit that is driven by either an external 20 MHz crystal oscillator or a TTL-level CMOS clock input. If a CMOS input is used, the clock should be 20 MHz ±0.01% with a duty cycle between 40% and 60%. The requirements for the crystal are described in section 15.0 (Crystal Oscillator specifications). The encoded signal is routed to either the 10BASE-T transceiver or AUI, depending on configuration.

Carrier Detection

The internal Carrier Detection circuit informs the MAC that valid receive data is present by asserting the internal Carrier Sense signal as soon it detects a valid bit pattern (1010b or 0101b for 10BASE-T, and 1b or 0b for AUI). During normal packet reception, Carrier Sense remains asserted while the frame is being received, and is de-asserted 1.3 to 2.3 bit times after the last low-to-high transition of the End-of-Frame (EOF) sequence. Whenever the receiver is idle (no receive activity), Carrier Sense is de-asserted. The CRS bit (Register 14, LineST, Bit E) reports the state of the Carrier Sense signal.

Clock and Data Recovery

When the receiver is idle, the phase-lock loop (PLL) is locked to the internal clock signal. The assertion of the Carrier Sense signal interrupts the PLL. When it restarts, it locks on the incoming data. The receive clock is then compared to the incoming data at the bit cell center and any phase difference is corrected. The PLL remains locked as long as the receiver input signal is valid. Once the PLL has locked on the incoming clock, the ENDEC converts the Manchester data to NRZ and passes the decoded data to the MAC for further processing.

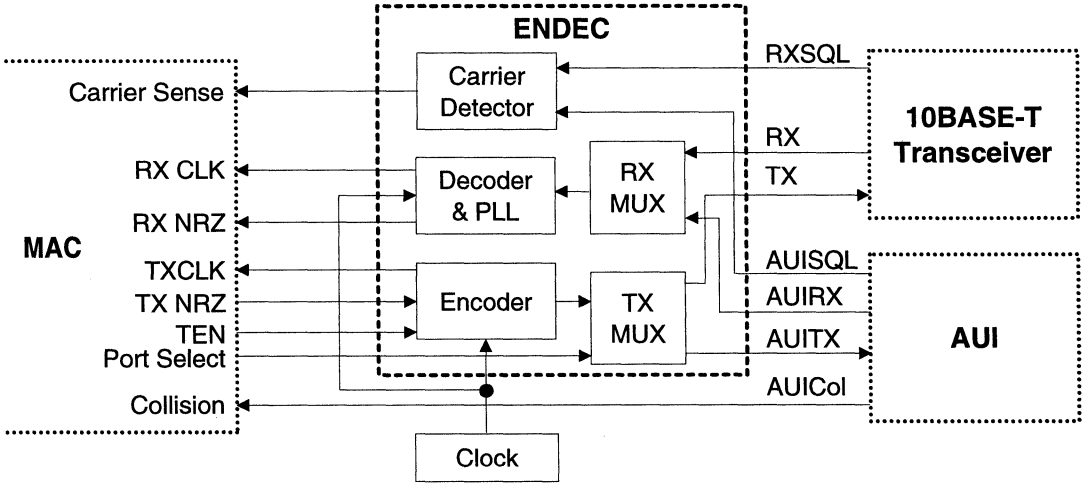


Figure 3.9. ENDEC

Interface Selection

Physical interface selection is determined by the AUIonly bit (Bit 8) and the AutoAUI/10BT bit (Bit 9) in the LineCTL register (Register 13). Table 3.11 describes the possible configurations.

AUIonly (Bit 8)	AutoAUI/10BT (Bit 9)	Physical Interface
0	0	10BASE-T Only
1	N/A	AUI Only
0	1	Auto-Select

Table 3.11. Interface Selection

10BASE-T Only: When configured for 10BASE-T-only operation, the 10BASE-T transceiver and its interface to the ENDEC are active, and the AUI is powered down.

AUI Only: When configured for AUI-only operation, the AUI and its interface to the ENDEC are active, and the 10BASE-T transceiver is powered down.

Auto-Select: In Auto-Select mode, the CS8900 automatically selects the 10BASE-T interface and powers down the AUI if valid packets and link pulses are detected by the 10BASE-T receiver. If valid packets and link pulses are not detected, the CS8900 selects the AUI. Whenever the AUI is selected, the 10BASE-T receiver remains active to listen for link pulses or packets. If 10BASE-T activity is detected, the CS8900 switches back to 10BASE-T.

3.11 10BASE-T Transceiver

The CS8900 includes an integrated 10BASE-T transceiver that is compliant with section 14 of the Ethernet standard (ISO/IEC 8802-3, 1993). It includes all analog and digital circuitry needed to interface the CS8900 directly to a simple isolation transformer (see section 11.0 for a

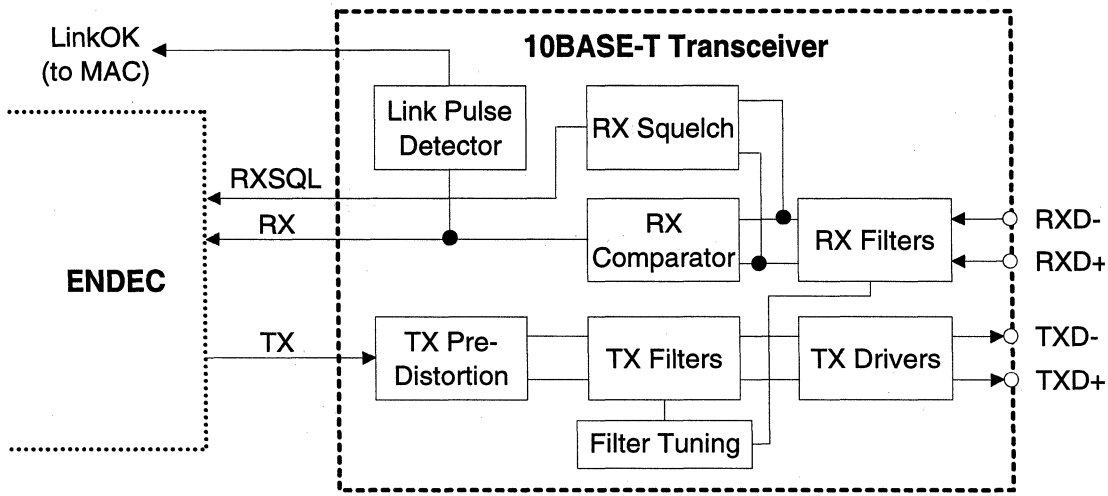


Figure 3.10. 10BASE-T Transceiver

connection diagram). Figure 3.10 provides a block diagram of the 10BASE-T transceiver.

10BASE-T Filters

The CS8900's 10BASE-T transceiver includes integrated low-pass transmit and receive filters, eliminating the need for external filters or a filter/transformer hybrid. On-chip filters are gm/c implementations of fifth-order Butterworth low-pass filters. Internal tuning circuits keep the gm/c ratio tightly controlled, even when large temperature, supply, and IC process variations occur. The nominal 3 dB cutoff frequency of the filters is 16 MHz, and the nominal attenuation at 30 MHz (3rd harmonic) is typically -27 dB.

Transmitter

When configured for 10BASE-T operation, Manchester encoded data from the ENDEC is fed into the transmitter's pre-distortion circuit where initial wave shaping and pre-equalization is performed. The output of the pre-distortion circuit is fed into the transmit filter where final wave shaping occurs and unwanted noise is removed. The signal then passes to the differential driver where it is amplified and driven out of the TXD+/TXD- pins.

In the absence of transmit packets, the transmitter generates link pulses in accordance with section 14.2.1.1. of the Ethernet standard. Transmitted link pulses are positive pulses, one bit time wide, typically generated at a rate of one every 16 ms. The 16 ms timer starts whenever the tramsmitter completes an End-of-Frame (EOF) sequence. Thus, there is a link pulse 16 ms after an EOF unless there is another transmitted packet. Figure 3.11 diagrams the operation of the Link Pulse Generator.

Receiver

The 10BASE-T receive section consists the receive filter, squelch circuit, polarity detection and correction circuit, and link pulse detector.

Squelch Circuit: The 10BASE-T squelch circuit determines when valid data is present on the RXD+/RXD- pair. Incoming signals passing through the receive filter are tested by the squelch circuit. Any signal with amplitude less than the squelch threshold (either positive or negative, depending on polarity) is rejected.

Extended Range: The CS8900 supports an Extended Range feature that reduces the 10BASE-T receive squelch threshold by approximately 6 dB. This allows the CS8900 to operate with 10BASE-T cables that are longer than 100 meters (100 meters is the maximum length specified by the Ethernet standard). The exact additional distance depends on the quality of the cable and the amount of electro-magnetic noise in the surrounding environment. To activate this feature, the host must set the LoRxSquelch bit (Register 13, LineCTL, Bit E). For more infor-

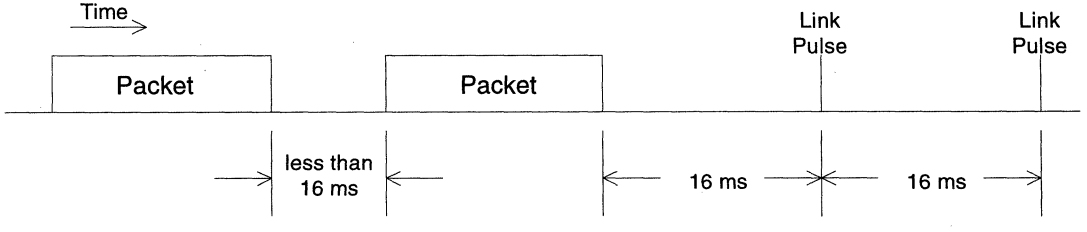


Figure 3.11. Link Pulse Transmission

mation about Extended Range, see the *CS8900 Technical Reference Manual.*

Link Pulse Detection

To prevent disruption of network operation due to a faulty link segment, the CS8900 continually monitors the 10BASE-T receive pair (RXD+/ RXD-) for packets and link pulses. After each packet or link pulse is received, an internal Link-Loss timer is started. As long as a packet or link pulse is received before the Link-Loss timer finishes (between 25 and 150 ms), the CS8900 maintains normal operation. If no receive activity is detected, the CS8900 disables packet transmission to prevent "blind" transmissions onto the network (link pulses are still sent while packet transmission is disabled). To reactivate transmission, the receiver must detect a single packet (the packet itself is ignored), or two link pulses separated by more than 2 to 7 ms and no more than 25 to 150 ms (see section 10.0 for 10BASE-T timing).

The state of the link segment is reported in the LinkOK bit (Register 14, LineST, Bit 7). If the HC0E bit (Register 15, SelfCTL, Bit D) is clear, it is also indicated by the output of the $\overline{\text{LINKLED}}$ pin. If the link is "good", the LinkOK bit is set and the $\overline{\text{LINKLED}}$ pin is driven low. If the link is "bad" the LinkOK bit is clear and the $\overline{\text{LINKLED}}$ pin is high. To disable this feature, the host must set the DisableLT bit (Register 19, TestCTL, Bit 7). If DisableLT is set, the CS8900 will transmit and receive packets independent of the link segment.

Receive Polarity Detection and Correction

The CS8900 automatically checks the polarity of the receive half of the twisted pair cable. If the polarity is correct, the PolarityOK bit (Register 14, LineST, bit C) is set. If the polarity is reversed, the PolarityOK bit is clear. If the PolarityDis bit (Register 19, TestCTL, Bit C) is clear, the CS8900 automatically corrects a reversal. If the PolarityDis bit is set, the CS8900 does not correct a reversal. The PolarityOK bit and the PolarityDis bit are independent.

To detect a reversed pair, the receiver examines received link pulses and the End-of-Frame (EOF) sequence of incoming packets. If it detects at least one reversed link pulse and at least four frames in a row with negative polarity after the EOF, the receive pair is considered reversed. Any data received before the correction of the reversal is ignored.

Collision Detection

The CS8900 detects a 10BASE-T collision whenever the receiver and transmitter are active simultaneously. When a collision is present, the Collision Detection circuit informs the MAC by asserting the internal Collision signal (see section 3.10 for collision handling).

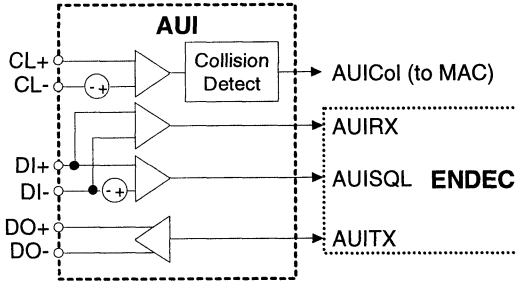
3.12 Attachment Unit Interface (AUI)

The CS8900 Attachment Unit Interface (AUI) provides a direct interface to external 10BASE2, 10BASE5, and 10BASE-FL Ethernet transceivers. It is fully compliant with Section 7 of the Ethernet standard (ISO/IEC 8802-3), and as such, is capable of driving a full 50-meter AUI cable.

The AUI consists of three pairs of signals: Data Out (DO+/DO-), Data In (DI+/DI-), and Collision In (CI+/CI-). To select the AUI, the host should set the AUI bit (Register 13, LineCTL, Bit 9). The AUI can also be selected automatically as described in the previous section (section 3.11, *Interface Selection*). Figure 3.12 provides a block diagram of the AUI. (For a connection diagram, see section 12.0).

AUI Transmitter

The AUI transmitter is a differential driver designed to drive a 78 ohm cable. It accepts data from the ENDEC and transmits it directly on the DO+/DO- pins. After transmission has started, the CS8900 expects to see the packet "looped-back" (or echoed) to the receiver, causing the Carrier Sense signal to be asserted. This Carrier Sense presence indicates that the transmit signal is getting through to the transceiver. If the Carrier Sense signal remains de-asserted throughout the transmission, or if the Carrier Sense signal is de-asserted before the end of the transmission, there is a Loss-of-Carrier error and the Loss-of-CRS bit (Register 8, TxEvent, Bit 6) is set.



3.12. AUI

AUI Receiver

The AUI receiver is a differential pair circuit that connects directly to the DI+/DI- pins. It is designed to distinguish between transient noise pulses and incoming Ethernet packets. Incoming packets with proper amplitude and pulse width are passed on to the ENDEC section, while unwanted noise is rejected.

Collision Detection

The AUI collision circuit is a differential pair receiver that detects the presence of collision signals on the CI+/CI- pins. The collision signal is generated by an external Ethernet transceiver whenever a collision is detected on the Ethernet segment. (Section 7.3.1.2 of ISO/IEC 8802-3, 1993, defines the collision signal as a 10 MHz +/- 15% signal with a duty cycle no worse than 60/40). When a collision is present, the AUI Collision circuit informs the MAC by asserting the internal Collision signal.

3.13 External Clock Oscillator

A 20 MHz crystal oscillator or CMOS clock input is required by the CS8900. If a CMOS clock input is used, it should be connected the to XTAL1 pin, with the XTAL2 pin left open. The clock signal should be 20 MHz ±0.01% with a duty cycle between 40% and 60%. The requirements for the crystal are described in section 13.0 (Crystal Oscillator specifications).

4.0 PACKETPAGE ARCHITECTURE

4.1 PacketPage Overview

The CS8900 architecture is based on a unique, highly-efficient method of accessing internal registers and buffer memory known as PacketPage. PacketPage provides a unified way of controlling the CS8900 in Memory or I/O space that minimizes CPU overhead and simplifies software. It provides a flexible set of performance features and configuration options, allowing designers to develop Ethernet circuits that meet their particular system requirements.

Integrated Memory

Central to the CS8900 architecture is a 4-Kbyte page of integrated RAM known as PacketPage memory. PacketPage memory is used for temporary storage of transmit and receive frames, and for internal registers. Access to this memory is done directly, through Memory space operations (Memory Mode), or indirectly, though I/O space operations (I/O Mode). In most cases, Memory Mode will provide the best overall performance, because ISA Memory operations require fewer cycles than I/O operations. I/O Mode is the CS8900's default configuration and is used when memory space is not available or when special operations are required (e.g. waking the CS8900 from the Software Sleep state requires the host to write to the CS8900's assigned I/O space).

The user-accessible portion of PacketPage memory is organized in the following six sections:

PacketPage Address	Contents
0000h - 0045h	Bus Interface Registers
0100h - 013Fh	PacketPage Registers
0140h - 014Fh	TxCMD/TxLength Registers
0150h - 015Dh	Filter Registers
0400h	Receive Frame Register
0A00h	Transmit Frame Register

Bus Interface Registers

The Bus Interface registers are used to configure the CS8900's ISA-bus interface and to map the CS8900 into the host system's I/O and Memory space. Most of these registers are written only during initialization, remaining unchanged while the CS8900 is in normal operating mode. The exceptions to this are the DMA registers which are modified continually whenever the CS8900 is using DMA.

PacketPage Registers

The PacketPage registers are the primary means on controlling and statusing the CS8900. They are described in more detail in section 4.2.

TxCMD/TxLength Registers

The TxCMD/TxLength registers are used to initiate Ethernet frame transmission. (See section 5.5 for a description of frame transmission.)

Filter Registers

The Filter registers store the Individual and Logical Addresses used by the Destination Address (DA) filter. For a description of the DA filter, see section 4.9.

Receive and Transmit Frame Register

The Receive and Transmit Frame Registers are used to transfer Ethernet frames to and from the host. The host simply writes to and reads from these registers and internal buffer memory is dynamically allocated between transmit and receive as needed. This provides more efficient use of buffer memory and better overall network performance. As a result of this dynamic allocation, only one receive frame (starting at PacketPage base + 0400h) and one transmit frame (starting at PacketPage base + 0A00h) are directly accessable.

PacketPage Memory Map

Table 4.1 shows the CS8900 PacketPage memory address map:

PacketPage Address	# of Bytes	Type	Description	Cross Reference
0000h	4	Read-only	Product Identification Code	Note 1
0004h	28	Read-only	Reserved (each word read as I/O base address)	
0020h	2	Read/Write	I/O Base Address	
0022h	2	Read/Write	Interrupt Number (0, 1, 2, or 3)	Section 3.2
0024h	2	Read/Write	DMA Channel Number (0, 1, or 2)	Section 3.2
0026h	2	Read-only	DMA Start Of Frame	Section 5.2
0028h	2	Read-only	DMA Frame Count (12 bits)	Note 2
002Ah	2	Read-only	RxDMA Byte Count	Note 3
002Ch	4	Read/Write	Memory Base Address (24 bits)	Note 4
0030h	4	Read/Write	Boot PROM Base Address	Section 3.6
0034h	4	Read/Write	Boot PROM Address Mask	Section 3.6
0038h	8	Read-only	Reserved (each word read as I/O base address)	
0040h	2	Read/Write	EEPROM Data	Section 3.5
0042h	2	Read/Write	EEPROM Opcode	Section 3.5
0044h	2	Read/Write	Reserved	
0046h	186	Read-only	Reserved (each word read as I/O base address)	
0100h	32	Read/Write	Configuration & Control Registers (2 bytes per register)	Section 4.5
0120h	32	Read-only	Status & Event Registers (2 bytes per register)	Section 4.5
0140h	4	Read-only	Reserved (each word read as I/O base address)	
0144h	2	Write-only	TxCMD (transmit command)	Register 9
0146h	2	Write-only	TxLength (transmit lenght)	Section 5.5
0150h	8	Read/Write	Logical Address Filter (hash table)	Section 4.9
0158h	8	Read/Write	Individual Address	Note 5
0160h	672	Read-only	Reserved (each word read as I/O base address)	
0400h	2	Read-only	RxStatus (receive status)	Note 6
0402h	2	Read-only	RxLength (receive length, in bytes)	Note 7
0404h	2	Read-only	Receive Frame Register	Section 5.1
0A00h	2	Read/Write	Transmit Frame Register	Section 5.5

All registers are accessed as words only.
Notes on following page.

Table 4.1. PacketPage Memory Address Map

Notes for PacketPage Memory Address Map:

(1) Product Identification Code: The first four bytes of the PacketPage memory contain a unique 32-bit product ID code that identifies the chip as a CS8900. The host can use this number to determine which software driver to load and to check what features are availabe. The following table decribes the product ID code:

PacketPage Address	Register Contents	Comments
0000h	0000-1110	First byte of the EISA registration number for Crystal Semiconductor
0001h	0110-0011	Second byte of the EISA registration number for Crystal Semiconductor
0002h	0000-0000	First 8 bits of the Product ID number
0003h	000X-XXXX	Last 3 bits of the Product ID number (5 "X" bits are the revision number)

(2) RxDMA Frame Count: The lower 12 bits of the Frame Count define the number of valid frames received since the last readout of this location. The upper 4 bits are not applicable and are read Fh.

(3) RxDMA Byte Count: The RxDMA Byte Count is the valid number of bytes DMAed since the last readout.

(4) Memory Base Address: The lower three bytes (002Ch, 002Dh, and 002Eh) are used for the 24-bit memory base address. The upper byte (002Fh) is reserved and is read FFh.

(5) Individual Address: The 48-bit Individual Address (IA) begins at 0158h. The first bit of the IA (Bit IA[00]) must be "0". The bit ordering for the IA is:

PacketPage Address	MSB in byte	LSB in byte
0158h	IA[07]	IA[00]
0159h	IA[0F]	IA[08]
015Ah	IA[17]	IA[10]
015Bh	IA[1F]	IA[18]
015Ch	IA[27]	IA[20]

(6) RxStatus: RxStatus (receive status) is the same as the RxEvent register (Register 4), except RxStatus is not cleared when RxEvent is read.

(7) RxLength: RxLength (receive length) is the length, in bytes, of the data to be transferred to the host across the ISA bus.

4.2 PacketPage Registers

The PacketPage registers are the primary registers used to control and status the CS8900. They are organized into two groups: Configuration/Control Registers and Status/Event Registers. All PacketPage Registers are 16-bit words as shown in Figure 4.1. Bit 0 indicates whether it is a Configuration/Control Register (Bit 0 = 1) or a Status/Event Register (Bit 0 = 0). Bits 0 through 5 provide an internal address code that describes the exact function of the register. Bits 6 through F are the actual Configuration/Control and Status/Event bits.

Configuration and Control Registers

Configuration and Control registers are used to setup the following:

- how frames will be transmitted and received;
- what frames will be transmitted and received;
- which events will cause interrupts to the host processor; and,
- how the Ethernet physical interface will be configured.

These registers are read/write and are designated by odd numbers (e.g. Register 1, Register 3, etc.).

The Transmit Command Register (TxCMD) is a special type of register. It appears in two separate locations in the PacketPage memory map. The first location, PacketPage base + 0108h, is within the block of Configuration/Control Registers and is read-only. The second location, PacketPage base + 0144h, is where the actual transmit commands are issued and is write-only. See section 4.5 (Register 9) and section 5.5 for a more detailed description of the TxCMD register.

Status and Event Registers

Status and Event registers report the status of transmitted and received frames, as well as information about the configuration of the CS8900. They are read-only and are designated by even numbers (e.g. Register 2, Register 4, etc.).

The Interrupt Status Queue (ISQ) is a special type of Status/Event register. It is located at PacketPage base + 0120h and is the first register the host reads when responding to an Interrupt.

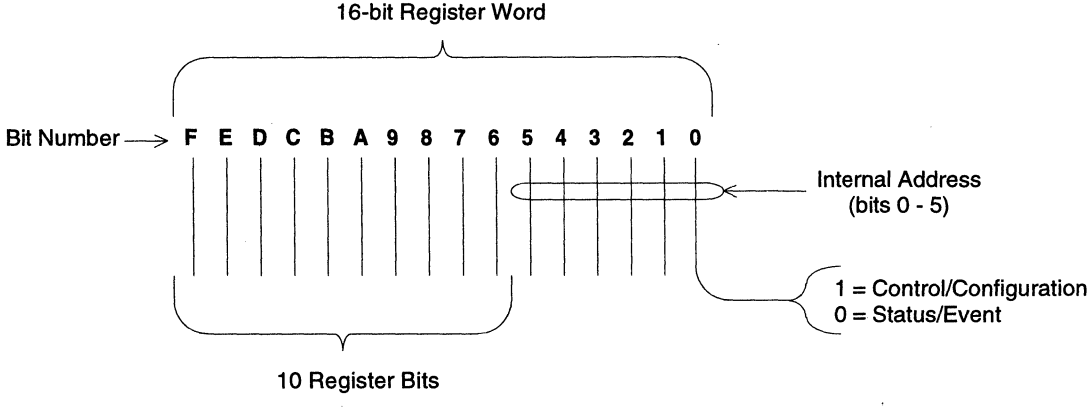


Figure 4.1. PacketPage Register Format

A more detailed description of the ISQ can be found in section 4.8.

Included with the Status and Event registers are three 10-bit counters. RxMISS (Register 10) counts missed receive frames, TxCOL (Register 12) counts transmit collisions, and TDR (Register 1C) is a time domain reflectometer useful in locating cable faults. For more information about these counters, see section 4.10.

Table 4.2 provides a summary of PacketPage Register types.

4.3 PacketPage Bit Definitions

This section provides a description of the special bit types used in the PacketPage registers. Sections 4.4 and 4.5 provide a detailed description of the bits in each register.

Act-Once Bits

There are four bits that cause the CS8900 to take a certain action only once when set. These "Act-Once" bits are: Skip_1 (Register 3, RxCFG, Bit 6), RESET (Register 15, SelfCTL, Bit 6), ResetRxDMA (Register 17, BusCTL, Bit 6), and SWint-X (Register B, BufCFG, Bit 6). To cause the action again, the host must set the bit again. Act-Once bits are always read as clear.

Temporal Bits

Temporal bits are bits that are set and cleared by the CS8900 without intervention of the host processor. This includes all status bits in the three status registers (Register 14, LineST; Register 16, SelfST; and, Register 18, BusST), the RxDest bit (Register C, BufEvent, Bit F), and the Rx128 bit (Register C, BufEvent, Bit F). Like all Event bits, RxDest and Rx128 are cleared when read by the host.

Interrupt Enable Bits and Events

Interrupt Enable bits end with the suffix iE and are located in three Configuration registers: RxCFG (Register 3), TxCFG (Register 7), and BufCFG (Register B). Each Interrupt Enable bit corresponds to a specific event. If an Interrupt Enable bit is set and its corresponding event occurs, the CS8900 generates an interrupt to the host processor.

Suffix	Type	Description	Comments
CMD	Read/Write	**Command:** Written once per frame to initiate transmit.	
CFG	Read/Write	**Configuration:** Written at setup and used to determine what frames will be transmitted and received and what events will cause interrupts.	
CTL	Read/Write	**Control:** Written at setup and used to determine what frames will be transmitted and received and how the physical interface will be configured.	
Event	Read-only	**Event:** Reports the status of transmitted and received frames.	cleared when read
ST	Read-only	**Status:** Reports information about the configuration of the CS8900.	
	Read-only	**Counters:** Counts missed receive frames and collisions. Provides time domain reflectometer for locating coax cable faults.	cleared when read

Table 4.2. PacketPage Regiser Types

The bits that report when various events occur are located in three Event registers and two counters. The Event registers are RxEvent (Register 4), TxEvent (Register 8), and BufEvent (Register C). The counters are RxMISS (Register 10) and TxCOL (Register 12). Each Interrupt Enable bit and its associated Event are identified in table 4.3.

Interrupt Enable Bit (register name)	Event Bit or Counter (register name)
ExtradataiE (RxCFG)	Extradata (RxEvent)
RuntiE (RxCFG)	Runt (RxEvent)
CRCerroriE (RxCFG)	CRCerror (RxEvent)
RxOKiE (RxCFG)	RxOK (RxEvent)
16colliE (TxCFG)	16coll (TxEvent)
AnycolliE (TxCFG)	"Number-of-Tx-collisions" counter is incremented (TxEvent)
JabberiE (TxCFG)	Jabber (TxEvent)
Out-of-windowiE (TxCFG)	Out-of-window (TxEvent)
TxOKiE (TxCFG)	TxOK (TxEvent)
SQEerroriE (TxCFG)	SQEerror (TxEvent)
Loss-of-CRSiE (TxCFG)	Loss-of-CRS (TxEvent)
MissOvfloiE (BufCFG)	RxMISS counter overflows past 1FFh
TxColOvfloiE (BufCFG)	TxCOL counter overflows past 1FFh
RxDestiE (BufCFG)	RxDest (BufEvent)
Rx128iE (BufCFG)	Rx128 (BufEvent)
RxMissiE (BufCFG)	RxMISS (BufEvent)
TxUnderruniE (BufCFG)	TxUnderrun (BufEvent)
Rdy4TxiE (BufCFG)	Rdy4Tx (BufEvent)
RxDMAiE (BufCFG)	RxDMAFrame (BufEvent)

Table 4.3.

An Event bit will be set whenever the specified event happens, whether or not the associated Interrupt Enable bit is set. All Event registers are cleared upon read-out by the host.

Accept Bits

There are nine Accept bits located in the RxCTL register (Register 5), each of which is followed by the suffix A. Accept bits indicate what types of frames will be accepted by the CS8900. (A frame is said to be "accepted" by the CS8900 when the frame data are placed in either on-chip memory, or in host memory by DMA.) Four of these bits have corresponding Interrupt Enable (iE) bits. An Accept bit and an Interrupt Enable bit are independent operations. It is possible to set either, neither, or both bits. The four corresponding pairs of bits are:

iE Bit in RxCFG	A Bit in RxCTL
ExtradataiE	ExtradataA
RuntiE	RuntA
CRCerroriE	CRCerrorA
RxOKiE	RxOKA

If one of the above Interrupt Enable bits is set and the corresponding Accept bit is clear, the CS8900 generates an interrupt when the associated receive event occurs, but then does not accept the receive frame (the length of the receive frame is set to zero).

The other five Accept bits in RxCTL are used for destination address filtering (see section 4.9). The Accept mechanism is explained in more detail in section 5.1.

4.4 PacketPage Register Summary

The figure on the following page (Figure 4.2) provides a summary of the PacketPage registers. Section 4.5 gives a detailed description of each PacketPage register.

Control and Configuration Bits										Register	
F	E	D	C	B	A	9	8	7	6	Number (Offset)	Name
Reserved (read as I/O base address)										1	
	Extra dataiE	RuntiE	CRC erroriE	Buffer CRC	AutoRx DMAE	RxDMA only	RxOKiE	StreamE	Skip_1	3 (0102h)	RxCFG
	Extra dataA	RuntA	CRC errorA	Broad castA	Individ ualA	Multi castA	RxOKA	Promis cuousA	IAHashA	5 (0104h)	RxCTL
16colliE				AnycolliE	JabberiE	Out-of-windowiE	TxOKiE	SQEerror iE	Loss-of-CRSiE	7 (0106h)	TxCFG
		TxPadDis	Inhibit CRC			Onecoll	Force	TxStart		9 (0108h)	TxCMD
RxDestiE		Miss OvfloiE	TxCol OvfloiE	Rx128iE	RxmissiE	TxUnder runiE	Rdy4TxiE	RxDMAiE	SWint-X	B (010Ah)	BufCFG
Reserved (read as I/O base address)										D - 11	
	LoRx Squelch	2-part DefDis	Polarity Dis	Mod BackoffE		Auto AUI/10BT	AUIonly	SerTxON	SerRxON	13 (0112h)	LineCTL
HCB1	HCB0	HC1E	HC0E		HW StandbyE	HW SleepE	SW Suspend		RESET	15 (0114h)	SelfCTL
		RxDMA size	IOCH RDYE	DMA Burst	MemoryE	UseSA			Reset RxDMA	17 (0116)	BusCTL
FastTest	FDX			Disable Backoff	AUIloop	ENDEC loop		Disable LT		19 (0118)	TestCTL
Reserved (read as I/O base address)										1B - 1F	

Status and Event Bits										Register	
F	E	D	C	B	A	9	8	7	6	Number (Offset)	Name
Interrupt Status Queue										0 (0120h)	ISQ
Reserved (read as I/O base address)										2	
	Extra data	Runt	CRC error	Broad cast	Individal Adr	Hashed	RxOK	Dribble bits	IAHash	4 (0124h)	RxEvent
Hash Table Index (alternate RxEvent meaning if Hashed = 1 and RxOK =1)						Hashed	RxOK	Dribble bits	IAHash	4 (0124h)	RxEvent alternate
Reserved (read as I/O base address)										6	
16coll	Number-of-Tx-collisions				Jabber	Out-of-window	TxOK	SQE error	Loss-of-CRS	8 (0128h)	TxEvent
Reserved (read as I/O base address)										A	
RxDest				Rx128	RxMiss	TxUnder run	Rdy4Tx	RxDMA Frame	SWint	C (012Ch)	BufEvent
Reserved (read as I/O base address)										E	
10-bit Receive Miss (RxMISS) counter, cleared when read										10 (0130h)	RxMISS
10-bit Transmit Collision (TxCOL) counter, cleared when read										12 (0132h)	TxCOL
	CRS		Polarity OK			10BT	AUI	LinkOK		14 (0134h)	LineST
			EEsize	EL present	EEPROM OK	EEPRO present	SIBUSY	INITD	3.3V Active	16 (1136h)	SelfST
							Rdy4Tx NOW	TxBid Err		18 (0138h)	BusST
Reserved (read as I/O base address)										1A	
10-bit AUI Time Domain Reflectometer (TDR) counter, cleared when read										1C (013Ch)	TDR
Reserved (read as I/O base address)										1E	
Note: All bit positions that are blank are reserved and should not be used.											

Figure 4.2. PacketPage Register Summary

4.5 PacketPage Register Descriptions

Register 3: Receiver Configuration (RxCFG, Read/Write) ***Address: PacketPage base + 0102h***

F	E	D	C	B	A	9	8	7	6	5-0
	Extra dataiE	RuntiE	CRC erroriE	Buffer CRC	AutoRx DMAE	RxDMA only	RxOKiE	StreamE	Skip_1	000011

RxCFG determines how frames will be transferred to the host and what frame types will cause interrupts.

BIT	NAME	DESCRIPTION
5-0	000011	These bits provide an internal address used by the CS8900 to identify this as the Receiver Configuration Register. To write to this register, these bits must be 000011, where the LSB corresponds to Bit 0.
6	Skip_1	When set, this bit causes the last committed received frame to be deleted from the receive buffer. (For the definition of a committed received frame, see section 5.1). To skip another frame, the host must re-write a "1" to this bit. This bit is not to be used if RxDMAonly (Bit 9) is set. Skip_1 is an Act-Once bit.
7	StreamE	When set, StreamTransfer mode is used to transfer receive frames that are back-to-back AND that pass the Destination Address filter (see section 4.9). When StreamE is clear, StreamTransfer mode is not used.
8	RxOKiE	When set, there is an RxOK Interrupt if a frame is received without errors.
9	RxDMAonly	The Receive-DMA mode is used for all receive frames when this bit is set.
A	AutoRxDMAE	When set, the CS8900 will automatically switch to Receive-DMA mode if the conditions specified in section 5.3 are met. RxDMAonly (Bit 9) has precedence over AutoRxDMAE.
B	BufferCRC	When set, the received CRC is included with the data stored in the receive-frame buffer, and the four CRC bytes are included in the receive-frame length (PacketPage base + 0402h). When clear, neither the receive buffer nor the receive length include the CRC.
C	CRCerroriE	When set, there is a CRCerror Interrupt if a frame is received with a bad CRC.
D	RuntiE	When set, there is a Runt Interrupt if a frame is received that is shorter than 64 bytes. The CS8900 always discards any frame that is shorter than 8 bytes.
E	ExtradataiE	When set, there is an Extradata Interrupt if a frame is received that is longer than 1518 bytes. The operation of this bit is independent of the received packet integrity (good or bad CRC).

This register's initial state after reset is: 0000 0000 0000 0011

Register 4: Receiver Event (RxEvent, Read-only) ***Address: PacketPage base + 0124h***

F	E	D	C	B	A	9	8	7	6	5-0
	Extra data	Runt	CRC error	Broad cast	Individ ualAdr	Hashed	RxOK	Dribble bits	IAHash	000100

Alternate meaning if bits 8 and 9 are both set.

F	E	D	C	B	A	9	8	7	6	5-0
Hash Table Index (see section 4.9)						Hashed = 1	RxOK = 1	Dribble bits	IAHash	000100

RxEvent reports the status of the current received frame.

BIT	NAME	DESCRIPTION
5-0	000100	These bits provide an internal address used by the CS8900 to identify this as the Receiver Event Register. When reading this register, these bits will be 000100, where the LSB corresponds to Bit 0.
6	IAHash	If the received frame's Destination Address is accepted by the hash filter, then this bit is set if, and only if, RxOK (Bit 8) is set and IAHashA (Register 5, RxCTL, Bit 6) is set. IAHash cannot be set unless Hashed (Bit 9) is set.
7	Dribblebits	If set, the received frame had from one to seven bits after the last received full byte. An "Alignment Error" occurs when Dribblebits and CRCerror (Bit C) are both set.
8	RxOK	If set, the received frame had a good CRC and valid length (there is not a CRCerror (Bit C), Runt (Bit D), and Extradata event (Bit D)). Bits C, D, or E, may be set as part of the hash index as explained above. When RxOK is set, then the length of the received frame is contained at PacketPage base + 0402h. If RxOKiE (Register 3, RxCFG, Bit 8) is set, there is an interrupt.
9	Hashed	If set, the received frame had a Destination Address that was accepted by the hash filter. If Hashed AND RxOK (Bit 8) are set, Bits F through A of RxEvent become the Hash Table Index for this received frame. If Hashed AND RxOK are not both set, then Bits F through A are individual event bits as defined below.
A	IndividualAdr	If the received frame had a Destination Address which matched the Individual Address found at PacketPage base + 0158h, then this bit is set if, and only if, RxOK (Bit 8) is set AND IndividualA (Register 5, RxCTL, Bit A) is set.
B	Broadcast	If the received frame had a Broadcast Address (FFFF FFFF FFFFh) as the Destination Address, then this bit is set if, and only if, RxOK is set AND BroadcastA (Register 5, RxCTL, Bit B) is set.
C	CRCerror	If set, the received frame had a bad CRC. If CRCerroriE (Register 3, RxCFG, Bit C) is set, there is an interrupt.
D	Runt	If set, the received frame was shorter than 64 bytes. If RuntiE (Register 3, RxCFG, Bit D) is set, there is an interrupt.
E	Extradata	If set, the received frame was longer than 1518 bytes. All bytes beyond 1518 are discarded. If ExtradataiE (Register 3, RxCFG, Bit E) is set, there is an interrupt.

This register's initial state after reset is: 0000 0000 | 0000 0100

NOTE: All RxEvent bits are cleared upon readout. The host is responsible for processing all event bits.

Register 5: Receiver Control (RxCTL, Read/Write) ***Address: PacketPage base + 0104h***

F	E	D	C	B	A	9	8	7	6	5-0
	Extra dataA	RuntA	CRC errorA	Broad castA	Individ ualA	Multi castA	RxOKA	Promis cuousA	IA HashA	000101

RxCTL has two functions: Bits 8, C, D, and E define what types of frames to accept. Bits 6, 7, 9, A, and B configure the Destination Address filter.

BIT	NAME	DESCRIPTION
5-0	000101	These bits provide an internal address used by the CS8900 to identify this as the Receiver Control Register. To write to this register, these bits must be 000101, where the LSB corresponds to Bit 0. For a received frame to be accepted, the Destination Address of that frame must pass the filter criteria found in Bits 6, 7, 9, A, and B (see section 4.9).
6	IAHashA	When set, receive frames are accepted when the Destination Address is an Individual Address that passes the hash filter.
7	PromiscuousA	Frames with any address are accepted when this bit is set.
8	RxOKA	When set, the CS8900 accepts frames with correct CRC and valid length (valid length is: 64 bytes <= length <= 1518 bytes).
9	MulticastA	When set, receive frames are accepted if the Destination Address is an Multicast Address that passes the hash filter.
A	IndividualA	When set, receive frames are accepted if the Destination Address matches the Individual Address found at PacketPage base + 0158h to PacketPage base + 015Dh.
B	BroadcastA	When set, receive frames are accepted if the Destination Address is FFFF FFFF FFFFh.
C	CRCerrorA	When set, receive frames that pass the Destination Address filter, but have a bad CRC, are accepted. When clear, frames with bad CRC are discarded.
D	RuntA	When set, receive frames that are smaller than 64 bytes, and that pass the Destination Address filter are accepted. When clear, received frames less that 64 bytes in length are discarded. The CS8900 discards any frame that is less than 8 bytes.
E	ExtradataA	When set, receive frames that are longer than 1518 bytes, and that pass the Destination Address filter are accepted. The CS8900 accepts only the first 1518 bytes and ignores the rest. When clear, frames longer that 1518 bytes are discarded.

This register's initial state after reset is: 0000 0000 0000 0101

NOTE: It may become necessary for the host to change the Destination Address (DA) filter criteria without resetting the CS8900. This can be done as follows:

1. Clear SerRxON (Register 13, LineCTL, Bit 6) to prevent an additional receive frames while the filter is being changed.
2. Modify the DA filter bits (B, A, 9, 8, 7, and 6) in this register.
   Modify the Logical Address Filter at PacketPage base + 0150h, if necessary.
   Modify the Individual Address at PacketPage base + 0158h, if necessary.
3. Set SerRxON to re-enable the receiver.

It is possible for the CS8900 to miss frames while the host is changing the DA filter.

Register 7: Transmit Configuration (TxCFG, Read/Write) ***Address: PacketPage base + 0106h***

F	E	D	C	B	A	9	8	7	6	5-0
16colliE				AnycolliE	JabberiE	Out-of-windowiE	TxOKiE	SQE erroriE	Loss-of-CRSiE	000111

Each bit in TxCFG is an interrupt enable. When set, the interrupt described below is enabled. When clear, there is no interrupt.

BIT	NAME	DESCRIPTION
5-0	000111	These bits provide an internal address used by the CS8900 to identify this as the Transmit Configuration Register. To write to this register, these bits must be 000111, where the LSB corresponds to Bit 0.
6	Loss-of-CRSiE	If the CS8900 starts transmitting on the AUI and it does not see the Carrier Sense signal at the end of the preamble, an interrupt is generated if this bit is set. Carrier Sense activity is reported by the CRS bit (Register 14, LineST, Bit E).
7	SQEerroriE	When set, an interrupt is generated if there is an SQE error. (At the end of a transmission on the AUI, the CS8900 expects to see a collision within 64 bit times. If this does not happen, there is an SQE error.)
8	TxOKiE	When set, an interrupt is generated if a packet is completely transmitted.
9	Out-of-windowiE	When set, an interrupt is generated if a late collision occurs (a late collision is a collision which occurs after the first 512 bit times). When this occurs, the CS8900 forces a bad CRC and terminates the transmission.
A	JabberiE	When set, an interrupt is generated if a transmission is longer than approximately 26 ms.
B	AnycolliE	When set, if one or more collisions occur during the transmission of a packet, an interrupt occurs at the end of the transmission.
F	16colliE	If the CS8900 encounters 16 normal collisions while attempting to transmit a particular packet, the CS8900 stops attempting to transmit that packet. When this bit is set, there is an interrupt upon detecting the 16th collision.

This register's initial state after reset is:

0000 0000	0000 0111

NOTE: Bit 8 (TxOKiE) and Bit B (AnycolliE) are interrupts for normal transmit operation.
Bits 6, 7, 9, A, and F are interrupts for abnormal transmit operation.

Register 8: Transmitter Event (TxEvent, Read-only) ***Address: PacketPage base + 0128h***

F	E	D	C	B	A	9	8	7	6	5-0
16coll	Number-of-Tx-collisions				Jabber	Out-of-window	TxOK	SQE error	Loss-of-CRS	001000

TxEvent gives the event status of the last packet transmitted.

BIT	NAME	DESCRIPTION
5-0	001000	These bits provide an internal address used by the CS8900 to identify this as the Transmitter Event Register. When reading this register, these bits will be 001000, where the LSB corresponds to Bit 0.
6	Loss-of-CRS	If the CS8900 is transmitting on the AUI and doesn't see Carrier Sense (CRS) at the end of the preamble, there is a Loss-of-Carrier error and this bit is set. If Loss-of-CRSiE (Register 7, TxCFG, Bit 6) is set, there is an interrupt.
7	SQEerror	At the end of a transmission on the AUI, the CS8900 expects to see a collision within 64 bit times. If this does not happen, there is an SQE error and this bit is set. If SQEerroriE (Register 7, TxCFG, Bit 7) is set, there is an interrupt.
8	TxOK	This bit is set if the last packet was completely transmitted (Jabber (Bit A), out-of-window-collision (Bit 9), and 16Coll (Bit F) must all be clear). If TxOKiE (Register 7, TxCFG, Bit 8) is set, there is an interrupt.
9	Out-of-window	This bit is set if a collision occurs more than 512 bit times after the first bit of the preamble. When this occurs, the CS8900 forces a bad CRC and terminates the transmission. If Out-of-windowiE (Register 7, TxCFG, Bit 9) is set, there is an interrupt.
A	Jabber	If the last transmission is longer than 26 msec, then the packet output is terminated by the jabber logic and this bit is set. If JabberiE (Register 7, TxCFG, Bit A) is set, there is an interrupt.
E-B	Number-of-Tx-collisions	These bits give the number of transmit collisions that occurred on the last transmitted packet. Bit B is the LSB. If AnycolliE (Register 7, TxCFG, Bit B) is set, there is an interrupt when any collision occurs.
F	16coll	This bit is set if the CS8900 encounters 16 normal collisions while attempting to transmit a particular packet. When this happens, the CS8900 stops further attempts to send that packet. If 16colliE (Register 7, TxCFG, Bit F) is set, there is an interrupt.

This register's initial state after reset is: 0000 0000 | 0000 1000

NOTES:

1. In any event register, like TxEvent, all bits are cleared upon readout. The host is responsible for processing all event bits.
2. TxOK (Bit 8) and the Number-of-Tx-Collisions (Bits E-B) are used in normal packet transmission. All other bits (6, 7, 9, A, and F) give the status of abnormal transmit operation.

Register 9: Transmit Command (TxCMD, Read-only) ***Address: PacketPage base + 0108h***

F	E	D	C	B	A	9	8	7	6	5-0
		TxPadDis	InhibitCRC			Onecoll	Force	TxStart		001001

TxCMD tells the CS8900 how the next packet should be sent. It must be written to initiate each transmission. The host is not allowed to write directly to PacketPage base + 0108h. Instead, the host must write to PacketPage base + 0144h.

BIT	NAME	DESCRIPTION
5-0	001001	These bits provide an internal address used by the CS8900 to identify this as the Transmit Command Register. When reading this register, these bits will be 001001, where the LSB corresponds to Bit 0.
7, 6	TxStart	This pair of bits determines how many bytes are transferred to the CS8900 before the MAC starts the packet transmit process.

Bit 7	Bit 6	
0	0	Start transmission after 5 bytes are in the CS8900
0	1	Start transmission after 381 bytes are in the CS8900
1	0	Start transmission after 1021 bytes are in the CS8900
1	1	Start transmission after the entire frame is in the CS8900

8	Force	When set in conjunction with a new transmit command, any transmit frames waiting in the transmit buffer are deleted. If a previous packet has started transmission, that packet is terminated within 64 bit times with a bad CRC.
9	Onecoll	When this bit is set, any transmission will be terminated after only one collision. When clear, the CS8900 allows up to 16 normal collisions before terminating the transmission.
C	InhibitCRC	When set, the CRC is not appended to the transmission.
D	TxPadDis	When TxPadDis is clear, if the host gives a transmit length less than 60 bytes and InhibitCRC is set, then the CS8900 pads to 60 bytes. If the host gives a transmit length less than 60 bytes and InhibitCRC is clear, then the CS8900 pads to 60 bytes and appends the CRC. When TxPadDis is set, the CS8900 allows the transmission of runt frames (a frame less than 64 bytes). If InhibitCRC is clear, the CS8900 appends the CRC. If InhibitCRC is set, the CS8900 does not append the CRC.

This register's initial state after reset is: 0000 0000 | 0000 1001

NOTE: The CS8900 does not transmit a frame if TxLength < 3.

Register B: Buffer Configuration (BufCFG, Read/Write) ***Address: PacketPage base + 010Ah***

F	E	D	C	B	A	9	8	7	6	5-0
RxDestiE		Miss OvfloiE	TxCol OvfloiE	Rx128iE	RxMissiE	TxUnder runiE	Rdy4TxiE	RxDMAiE	SWint-X	001011

Each bit in BufCFG is an interrupt enable. When set, the interrupt described below is enabled. When clear, there is no interrupt.

BIT	NAME	DESCRIPTION
5-0	001011	These bits provide an internal address used by the CS8900 to identify this as the Buffer Configuration Register. To write to this register, these bits must be 001011, where the LSB corresponds to Bit 0.
6	SWint-X	When set, there is an interrupt requested by the host software. The CS8900 provides the interrupt, and sets the SWint (Register C, BufEvent, Bit 6) bit. The CS8900 acts upon this command at once. SWint-X is an Act-Once bit. To generate another interrupt, re-write a "1" to this bit.
7	RxDMAiE	When set, there is an interrupt when a frame has been received AND DMA is complete. With this interrupt, the RxDMAFrame bit (Register C, BufEvent, Bit 7) is set.
8	Rdy4TxiE	When set, there is an interrupt when the CS8900 is ready to accept a frame from the host for transmission. (See section 5.5 for a discription of the transmit bid process.)
9	TxUnderruniE	When set, there is an interrupt if the CS8900 runs out of data before it reaches the end of the frame (called a transmit underrun). When this happens, event bit TXUnderrun (Register C, BufEvent, Bit 9) is set and the CS8900 makes no further attempts to transmit that frame. If the host still wants to transmit that particular frame, the host must go through the transmit request process again.
A	RxMissiE	When set, there is an interrupt if one or more received frames is lost due to slow movement of receive data out of the receive buffer (called a receive miss). When this happens, the RxMiss bit (Register C, BufEvent, Bit A) is set.
B	Rx128iE	When set, there is an interrupt after the first 128 bytes of a frame have been received. This allows a host processor to examine the Destination Address, Source Address, Length, Sequence Number, and other information before the entire frame is received. This interrupt should not be used with DMA. Thus, if either AutoRxDMA (Register 3, RxCFG, Bit A) or RxDMAonly (Register 3, RxCFG, Bit 9) is set, the Rx128iE bit must be clear.
C	TxColOvfiE	If set, there is an interrupt when the TxCOL counter increments from 1FFh to 200h. (The TxCOL counter (Register 18) is incremented whenever the CS8900 sees that the RXD+/RXD- pins (10BASE-T) or the CI+/CI- pins (AUI) go active while a packet is being transmitted.)

Continued on the next page.

Register B: Buffer Configuration (BufCFG) continued

BIT	NAME	DESCRIPTION
D	MissOvfloiE	If MissOvfloiE is set, there is an interrupt when the RxMISS counter increments from 1FFh to 200h. (A receive miss is said to have occurred if packets are lost due to slow movement of receive data out of the receive buffers. When this happens, the RxMiss bit (Register C, BufEvent, Bit A) is set, and the RxMISS counter (Register 10) is incremented.)
F	RxDestiE	When set, there is an interrupt when a receive frame passes the Destination Address filter criteria defined in the RxCTL register (Register 5). This bit provides an early indication of an incoming frame. It is earlier than Rx128 (Register C, BufEvent, Bit B).

This register's initial state after reset is:

0000 0000	0000 1011

Register C: Buffer Event (BufEvent, Read-only) ***Address: PacketPage base + 012Ch***

F	E	D	C	B	A	9	8	7	6	5-0
RxDest				Rx128	RxMiss	TxUnder run	Rdy4Tx	RxDMA Frame	SWint	001100

BufEvent gives the status of the transmit and receive buffers.

BIT	NAME	DESCRIPTION
5-0	001100	These bits provide an internal address used by the CS8900 to identify this as the Buffer Event Register. When reading this register, these bits will be 001100, where the LSB corresponds to Bit 0.
6	SWint	If set, there has been a software initiated interrupt. This bit is used in conjunction with the SWint-X bit (Register B, BufCFG, Bit 6).
7	RxDMA Frame	If set, one or more received frames have been transferred by slave DMA. If RxDMAiE (Register B, BufCFG, Bit 7) is set, there is an interrupt.
8	Rdy4Tx	If set, the CS8900 is ready to accept a frame from the host for transmission. If Rdy4TxiE (Register B, BufCFG, Bit 8) is set, there is an interrupt. (See section 5.5 for a discription of the transmit bid process.)
9	TxUnderrun	This bit is set if CS8900 runs out of data before it reaches the end of the frame (called a transmit underrun). If TxUnderruniE (Register B, BufCFG, Bit 9) is set, there is an interrupt.
A	RxMiss	If set, one or more receive frames have been lost due to slow movement of data out of the receive buffers. If RxMissiE (Register B, BufCFG, Bit A) is set, there is an interrupt.
B	Rx128	This bit is set after the first 128 bytes of an incoming frame have been received. This bit will allow the host the option of pre-processing frame data before the entire frame is received. If Rx128iE (Register B, BufCFG, Bit B) is set, there is an interrupt.
F	RxDest	When set, this bit shows that a receive frame has passed the Destination Address Filter criteria as defined in the RxCTL register (Register 5). This bit is useful as an early indication of an incoming frame. It will be earlier than Rx128 (Register C, BufEvent, Bit B). If RxDestiE (Register B, BufCFG, Bit F) is set, there is an interrupt.

This register's initial state after reset is: 0000 0000 | 0000 1100

NOTE: With any event register, like BufEvent, all bits are cleared upon readout. The host is responsible for processing all event bits.

Register 13: Line Control (LineCTL, Read/Write) ***Address: PacketPage base + 0112h***

F	E	D	C	B	A	9	8	7	6	5-0
	LoRx Squelch	2-part DefDis	PolarityDis	Mod BackoffE		Auto AUI/10BT	AUIonly	SerTxON	SerRxON	010011

LineCTL determines the configuration of the MAC engine and physical interface.

BIT	NAME	DESCRIPTION
5-0	001101	These bits provide an internal address used by the CS8900 to identify this as the Line Control Register. To write to this register, these bits must be 010011, where the LSB corresponds to Bit 0.
6	SerRxON	When set, the receiver is enabled. When clear, no incoming packets pass through the receiver. If SerRxON is cleared while a packet is being received, reception is completed and no subsequent receive packets are allowed until SerRxON is set again.
7	SerTxON	When set, the transmitter is enabled. When clear, no transmissions are allowed. If SerTxON is cleared while a packet is being transmitted, transmission is completed and no subsequent packets are transmitted until SerTxON is set again.
8	AUIonly	Bits 8 and 9 are used to select either the AUI or the 10BASE-T interface according to the following:

AUIonly (Bit 8)	AutoAUI/10BT (Bit 9)	Physical Interface
1	N/A	AUI
0	0	10BASE-T
0	1	Auto-Select

9	AutoAUI/10BT	See AUIonly (Bit 8) description above.
B	ModBackoffE	When clear, the ISO/IEC standard backoff algorithm is used (see section 3.9). When set, the Modified Backoff algorithm is used. (The Modified Backoff algorithm extends the backoff delay after each of the first three Tx collisions.)
C	PolarityDis	The 10BASE-T receiver automatically determines the polarity of the received signal at the RXD+/RXD- input (see section 3.11). When this bit is clear, the polarity is corrected, if necessary. When set, no effort is made to correct the polarity. This bit is independent of the PolarityOK bit (Register 14, LineST, Bit C), which reports whether the polarity is normal or reversed.
D	2-partDefDis	Before a transmission can begin, the CS8900 follows a deferral procedure. With the 2-partDefDis bit clear, the CS8900 uses the standard two-part deferral as defined in ISO/IEC 8802-3 paragraph 4.2.3.2.1. With the 2-partDefDis bit set, the two-part deferral is disabled.
E	LoRxSquelch	When clear, the 10BASE-T receiver squelch thresholds are set to levels defined by the ISO/IEC 8802-3 specification. When set, the thresholds are reduced by approximately 6 dB. This is useful for operating with "quiet" cables that are longer than 100 meters.

This register's initial state after reset is: 0000 0000 0000 1101

Register 14: Line Status (LineST, Read-only) ***Address: PacketPage base + 0134h***

F	E	D	C	B	A	9	8	7	6	5-0
	CRS		PolarityOK			10BT	AUI	LinkOK		010100

LineST reports the status of the Ethernet physical interface.

BIT	NAME	DESCRIPTION
5-0	001110	These bits provide an internal address used by the CS8900 to identify this as the Line Status Register. When reading this register, these bits will be 010100, where the LSB corresponds to Bit 0.
7	LinkOK	If set, the 10BASE-T link has not failed. When clear, the link has failed, either because the CS8900 has just come out of reset, or because the receiver has not detected any activity (link pulses or received packets) for at least 50 ms.
8	AUI	If set, the CS8900 is using the AUI.
9	10BT	If set, the CS8900 is using the 10BASE-T interface.
C	PolarityOK	If set, the polarity of the 10BASE-T receive signal (at the RXD+ / RXD- inputs) is correct. If clear, the polarity is reversed. If PolarityDis (Register 19, TestCTL, Bit C) is set, then the polarity is automatically corrected, if needed. The PolarityOK status bit shows the true state of the incoming polarity independent of the PolarityDis control bit. Thus, if PolarityDis is clear and PolarityOK is clear, then the receive polarity is inverted, and corrected.
E	CRS	This bit tells the host the status of an incoming frame. If CRS is set, a frame is currently being received. CRS remains asserted until the end of frame (EOF). At EOF, CRS goes inactive in about 1.3 to 2.3 bit times after the last low-to-high transition of the recovered data.

This register's initial state after reset is:

0001 0010	0000 1110

Register 15: Self Control (SelfCTL, Read/Write) ***Address: PacketPage base + 0114h***

F	E	D	C	B	A	9	8	7	6	5-0
HCB1	HCB0	HC1E	HC0E		HW StandbyE	HW SleepE	SW Suspend		RESET	010101

SelfCTL controls the operation of the LED outputs and the low-power modes.

BIT	NAME	DESCRIPTION
5-0	001111	These bits provide an internal address used by the CS8900 to identify this as the Chip Self Control Register. To write to this register, these bits must be 010101, where the LSB corresponds to Bit 0.
6	RESET	When set, a chip-wide reset is initiated immediately. RESET is an Act-Once bit. This bit is cleared as a result of the reset.
8	SWSuspend	When set, the CS8900 enters the software initiated Suspend mode. Upon entering this mode, there is a partial reset. All registers and circuits are reset except for the ISA I/O Base Address Register and the SelfCTL Register. There is no transmit nor receive activity in this mode. To come out of software Suspend, the host issues an I/O Write within the CS8900's assigned I/O space (see section 3.7 for a complete description of the CS8900's low-power modes).
9	HWSleepE	When set, the $\overline{\text{HWSLEEP}}$ input pin is enabled. If $\overline{\text{HWSLEEP}}$ is high, the CS8900 is "awake", or operative (unless in SWSuspend mode, as shown above). If $\overline{\text{HWSLEEP}}$ is low, the CS8900 enters either the Hardware Standby or Hardware Suspend mode. When clear, the CS8900 ignores the $\overline{\text{HWSLEEP}}$ input pin (see section 3.7 for a complete description of the CS8900's low-power modes).
A	HWStandbyE	If HWSleepE is set AND the $\overline{\text{HWSLEEP}}$ input pin is low, then when HWStandbyE is set, the CS8900 enters the Hardware Standby mode. When clear, the CS8900 enters the Hardware Suspend mode (see section 3.7 for a complete description of the CS8900's low-power modes).
C	HC0E	The $\overline{\text{LINKLED}}$ or $\overline{\text{HC0}}$ output pin is selected with this control bit. When HC0E is clear, the output pin is LINKLED. When HC0E is set, the output pin is $\overline{\text{HC0}}$ and the HCB0 bit (Bit E) controls the pin.
D	HC1E	The $\overline{\text{BSTATUS}}$ or $\overline{\text{HC1}}$ output pin is selected with this control bit. When HC1E is clear, the output pin is BSTATUS and indicates receiver ISA Bus activity. When HC1E is set, the output pin is $\overline{\text{HC1}}$ and the HCB1 bit (Bit F) controls the pin.
E	HCB0	When HC0E (Bit C) is set, this bit controls the $\overline{\text{HC0}}$ pin. If HCB0 is set, $\overline{\text{HC0}}$ is low. If HCB0 is clear, HC0 is high. $\overline{\text{HC0}}$ may drive an LED or a logic gate. When HC0E (Bit C) is clear, this control bit is ignored.
F	HCB1	When HC1E (Bit D) is set, this bit controls the $\overline{\text{HC1}}$ pin. If HCB1 is set, $\overline{\text{HC1}}$ is low. If HCB1 is clear, HC1 is high. $\overline{\text{HC1}}$ may drive an LED or a logic gate. When HC1E (Bit D) is clear, this control bit is ignored.

This register's initial state after reset is: 0000 0000 | 0000 1111

Register 16: Self Status (SelfST, Read-only) ***Address: PacketPage base + 0136h***

F	E	D	C	B	A	9	8	7	6	5-0
			EEsize	ELpresent	EEPROM OK	EEPROM present	SIBUSY	INITD	3.3V Active	010110

SelfST reports the status of the EEPROM interface and the initialization process.

BIT	NAME	DESCRIPTION
5-0	010000	These bits provide an internal address used by the CS8900 to identify this as the Chip Self Status Register. When reading this register, these bits will be 010110, where the LSB corresponds to Bit 0.
6	3.3VActive	If the CS8900 is operating on a 3.3V supply, this bit is set. If the CS8900 is operating on a 5V supply, this bit is clear.
7	INITD	If set, the CS8900 initialization, including read-in of the EEPROM, is complete.
8	SIBUSY	If set, the EECS output pin is high indicating that the EEPROM is currently being read or programmed. The host must not write to PacketPage base + 0040h nor 0042h until SIBUSY is clear.
9	EEPROM present	If the EEDataIn pin is low after reset, there is no EEPROM present, and the EEPROMpresent bit is clear. If the EEDataIn pin is high after reset, the CS8900 "assumes" that an EEPROM is present, and this bit is set.
A	EEPROMOK	If set, the checksum of the EEPROM readout was OK.
B	ELpresent	If set, external logic for Latchable Address bus decode is present.
C	EEsize	This bit shows the size of the attached EEPROM and is valid only if the EEPROMpresent bit (Bit 9) AND EEPROMOK bit (Bit A) are both set. If clear, the EEPROM size is either 128 words ('C56 or 'CS56) or 256 words (C66 or 'CS66). If set, the EEPROM size is 64 words ('C46 or 'CS46).

This register's initial state after reset is:
(X = Depends on Configuration.)

000X X0X0	0X01 0000

Register 17: Bus Control (BusCTL, Read/Write) ***Address: PacketPage base + 0116h***

F	E	D	C	B	A	9	8	7	6	5-0
		RxDMA size	IOCH RDYE	DMA Burst	MemoryE	UseSA			Reset RxDMA	010111

BusCTL controls the operation of the ISA-bus interface.

BIT	NAME	DESCRIPTION
5-0	010001	These bits provide an internal address used by the CS8900 to identify this as the Bus Control Register. To write to this register, these bits must be 010111, where the LSB corresponds to Bit 0.
6	ResetRxDMA	When set, the RxDMA offset pointer at PacketPage base + 0026h is reset to zero. When the host sets this bit, the CS8900 does the following: 1. Terminates the current receive DMA activity, if any. 2. Clears all internal receive buffers. 3. Zeroes the RxDMA offset pointer. The CS8900 acts upon this command only once when this bit is set. ResetRxDMA is an Act-Once bit. To cause the pointer to reset again, the host must re-write a "1".
9	UseSA	When set, the $\overline{\text{MEMCS16}}$ pin goes low whenever the address on the SA bus [13..19] match the CS8900's assigned Memory base address AND the CHIPSEL pin is low. When clear, $\overline{\text{MEMCS16}}$ is driven low whenever CHIPSEL goes low. For $\overline{\text{MEMCS16}}$ pin to be enabled, the CS8900 must be in Memory Mode with the MemoryE bit (Register 17, BusCTL, Bit A) set.
A	MemoryE	When set, the CS8900 may operate in Memory Mode. When clear, Memory Mode is disabled. I/O Mode is always enabled.
B	DMABurst	When clear, the CS8900 performs continuous DMA until the receive frame is completely transferred from the CS8900 to host memory. When set, each DMA access is limited to 30 µs, after which time the CS8900 gives up the bus for 0.8 µs before making a new DMA request.
C	IOCHRDYE	When set, the CS8900 does not use the IOCHRDY output pin, and the pin is always high. This allows an external pull-up to force the output high. When clear, the CS8900 drives IOCHRDY low to request additional time during I/O Read and Memory Read cycles. IOCHRDY does not affect I/O Write, Memory Write, nor DMA Read.
D	RxDMAsize	This bit determines the size of the receive DMA buffer (located in host memory). When set, the DMA buffer size is 64 Kbytes. When clear, it is 16 Kbytes.

This register's initial state after reset is: 0000 0000 | 0001 0001

Register 18: Bus Status (BusST, Read-only) ***Address: PacketPage base + 0138h***

F	E	D	C	B	A	9	8	7	6	5-0
							Rdy4Tx NOW	TxBidErr		011000

BusST describes the status of the current transmit operation.

BIT	NAME	DESCRIPTION
5-0	010010	These bits provide an internal address used by the CS8900 to identify this as the Bus Status Register. When reading this register, these bits will be 011000, where the LSB corresponds to Bit 0.
7	TxBidErr	If set, the host has commanded the CS8900 to transmit a frame that the CS8900 will not send. Frames that the CS8900 will not send are: 1) Any frame greater than 1514 bytes, provided that InhibitCRC (Register 9, TxCMD, Bit C) is clear. 2) Any frame greater than 1518 bytes.
8	Rdy4TxNOW	Rdy4TxNOW signals the host that the CS8900 is ready to accept a frame from the host for transmission. This bit is similar to Rdy4Tx (Register C, BufEvent, Bit 8) except that there is no interrupt associated with Rdy4TxNOW. The host can poll the CS8900 and check Rdy4TxNOW to determine if the CS8900 is ready for transmit. (See section 5.5 for a discription of the transmit bid process.)

This register's initial state after reset is:

0000 0000	0001 0010

Register 19: Test Control (TestCTL, Read/Write) ***Address: PacketPage base + 0118h***

F	E	D	C	B	A	9	8	7	6	5-0
	FDX			Disable Backoff	AUIloop	ENDEC loop		DisableLT		011001

TestCTL controls the diagnostic test modes of the CS8900.

BIT NAME DESCRIPTION

5-0 010011 These bits provide an internal address used by the CS8900 to identify this as the Test Control Register. To write to this register, these bits must be 011001, where the LSB corresponds to Bit 0.

7 DisableLT When set, the 10BASE-T interface will not transmit Link Test pulses. DisableLT is used in conjunction with the LinkOK (Register 14, LineST, Bit 7) as follows:

LinkOK	DisableLT	
0	0	No packet transmission nor reception allowed. Transmitter sends link pulses.
0	1	DisableLT overrides LinkOK to allow packet transmission and reception.
1	N/A	DisableLT has no meaning if LinkOK = 1.

9 ENDECloop When set, the CS8900 enters internal loopback mode where the internal Manchester encoder output is connected to the decoder input. The 10BASE-T and AUI transmitters and receivers are disabled. When clear, the CS8900 is configured for normal operation.

A AUIloop When set, the CS8900 allows reception while transmitting. This facilitates loopback tests for the AUI. When clear, the CS8900 is configured for normal AUI operation.

B Disable Backoff When set, the backoff algorithm is disabled. The CS8900 transmitter looks only for completion of the inter packet gap before starting transmission. When clear, the backoff algorithm is used.

E FDX When set, 10BASE-T full duplex mode is enabled and CRS (Register 14, LineST, Bit E) is ignored. This bit must be set when performing loopback tests on the 10BASE-T port. When clear, the CS8900 is configured for standard half-duplex 10BASE-T operation.

This register's initial state after reset is: 0000 0000 | 0001 0001

4.6 Memory Mode Operation

To configure the CS8900 for Memory Mode, the PacketPage memory must be mapped into a contiguous 4-Kbyte block of host memory. The block must start at an X000h boundary, with the PacketPage base address mapped to X000h. When the CS8900 comes out of reset, its default configuration is I/O Mode. Once Memory Mode is selected, all of the CS8900's registers can be accessed directly.

Memory Mode Operation

The CS8900 allows Read/Write access to the internal PacketPage memory, and Read access of the optional Boot PROM. (See section 3.5 for a description of the optional Boot PROM.)

A memory access occurs when all of the following are true:

- The address on the ISA System Address bus (SA0 - SA19) is within the Memory space range of the CS8900 or Boot PROM.
- The $\overline{\text{CHIPSEL}}$ input pin is low.
- Either the $\overline{\text{MEMR}}$ pin or the $\overline{\text{MEMW}}$ pin is low.

Configuring the CS8900 for Memory Mode

There are two different methods of configuring the CS8900 for Memory Mode operation. One method allows the CS8900's internal memory to be mapped anywhere within the host system's 24-bit memory space. The other method limits memory mapping to the first 1 Mbyte of host memory space.

General Memory Mode Operation: Configuring the CS8900 so that its internal memory can be mapped anywhere within host Memory space requires the following:

- a simple circuit must be added to decode the Latchable Address bus (LA20 - LA23) and the BALE signal. (For information about this external circuit, as well as a sample design, see the *CS8900 Technical Reference Manual*).
- the host must configure the external logic with the correct address range as follows:
  1. Check to see if the INITD bit (Register 16, SelfST, bit 7) is set, indicating that initialization is complete.
  2. Check to see if the ELpresent bit (Register 16, SelfST, bit B) is set.
  3. Set the ELSEL bit of the EEPROM Command Register to activate the $\overline{\text{ELCS}}$ pin for use with the external decode circuit.
  4. Configure the external logic serially (see the *CS8900 Technical Reference Manual* for information about configuring the external logic).
- the host must write the memory base address into the Memory Base Address register (PacketPage base + 002Ch); and
- the host must set the MemoryE bit (Register 17, BusCTL, Bit A).

Limiting Memory Mode to the First 1 Mbyte of Host Memory Space: Configuring the CS8900 so that its internal memory can be mapped within the first 1 Mbyte of host memory space, only, requires the following:

- the $\overline{\text{CHIPSEL}}$ pin must be tied low;
- the ISA-bus $\overline{\text{SMEMR}}$ signal must be connected to the $\overline{\text{MEMR}}$ pin;

- the ISA-bus $\overline{\text{SMEMW}}$ signal must be connected to the $\overline{\text{MEMW}}$ pin;
- the host must write the memory base address into the Memory Base Address register (PacketPage base + 002Ch); and
- the host must set the MemoryE bit (Register 17, BusCTL, Bit A).

Basic Memory Mode Transmit

Memory Mode transmit operations occur in the following order (using interrupts):

1. The host bids for storage of the frame by writing the Transmit Command to the TxCMD register (memory base + 0144h) and the transmit frame length to the TxLength register (memory base + 0146h). If the transmit length is erroneous, the command is discarded and the TxBidErr bit (Register 10, BusST, Bit 7) is set.
2. The host reads the BusST register (Register 18, memory base + 0138h). If the Rdy4TxNOW bit (Bit 8) is set, the frame can be written. If clear, the host must wait for CS8900 buffer memory to become available. If Rdy4TxiE (Register B, BufCFG, Bit 8) is set, the host will be interrupted when Rdy4Tx (Register C, BufEvent, Bit 8) becomes set.
3. Once the CS8900 is ready to accept the frame, the host executes repetitive memory-to-memory move instructions (REP MOVS) to memory base + 0A00h to transfer the entire frame from host memory to CS8900 memory.

For a more detailed description of transmit, see section 5.5.

Basic Memory Mode Receive

Memory Mode receive operations occur in the following order (interrupts used to signal the presence of a valid receive frame):

1. A frame is received by the CS8900, triggering an enabled interrupt.
2. The host reads the Interrupt Status Queue (memory base + 0120h) and is informed of the receive frame.
3. The host reads RxStatus (memory base + 0400h) to learn the status of the receive frame.
4. The host reads RxLength (memory base + 0402h) to learn the frame's length.
5. The host reads the frame data by executing repetitive memory-to-memory move instructions (REP MOVS) from memory base + 0404h to transfer the entire frame from CS8900 memory to host memory.

For a more detailed description of receive, see section 5.1.

Polling the CS8900 in Memory Mode

If interrupts are not used, the host can poll the CS8900 to check if receive frames are present and if memory space is available for transmit. However, this is beyond the scope of this data sheet. See the *CS8900 Technical Reference Manual* for more information about polling.

4.7 I/O Space Operation

In I/O Mode, PacketPage memory is accessed through eight, 16-bit I/O ports that are mapped into 16 contiguous I/O locations in the host system's I/O space. I/O Mode is the default configuration for the CS8900 and is always enabled. On power up, the default value of the I/O

base address is set at 300h (300h is typically assigned to LAN peripherals). The I/O base address may be changed to any available XXX0h location, either by loading configuration data from the EEPROM, or during system setup. Table 4.4 shows the CS8900 I/O Mode mapping:

Offset	Type	Description
0000h	Read/Write	Receive/Transmit Data (Port 0)
0002h	Read/Write	Receive/Transmit Data (Port 1)
0004h	Write-only	TxCMD (Transmit Command)
0006h	Write-only	TxLength (Transmit Length)
0008h	Read-only	Interrupt Status Queue
000Ah	Read/Write	PacketPage Pointer
000Ch	Read/Write	PacketPage Data (Port 0)
000Eh	Read/Write	PacketPage Data (Port 1)

Table 4.4 I/O Mode Mapping

Receive/Transmit Data Ports 0 and 1

These two ports are used when transferring transmit data to the CS8900 and receive data from the CS8900. Port 0 is used for 16-bit operations and Ports 0 and 1 are used for 32-bit operations (lower-order word in Port 0).

TxCMD Port

The host writes the Transmit Command (TxCMD) to this port at the start of each transmit operation. The Transmit Command tells the CS8900 that the host has a frame to be transmitted, as well as how that frame should be transmitted. This port is mapped into PacketPage base + 0144h. See Register 9 in section 4.5 for more information.

TxLength Port

The length of the frame to be transmitted is written here immediately after the Transmit Command is written. This port is mapped into PacketPage base + 0146h.

Interrupt Status Queue Port

This port contains the current value of the Interrupt Status Queue (ISQ). The ISQ is located at PacketPage base + 0120h. For a more detailed description of the ISQ, see section 4.8.

PacketPage Pointer Port

The PacketPage Pointer Port is written whenever the host wishes to access any of the CS8900's internal registers. The first 12 bits (bits 0 through B) provide the internal address of the target register to be accessed during the current operation. The next three bits (C, D, and E) must be 0. The last bit (Bit F) indicates whether or not the PacketPage Pointer should be auto-incremented to the next word location. Figure 4.3 shows the structure of the PacketPage Pointer.

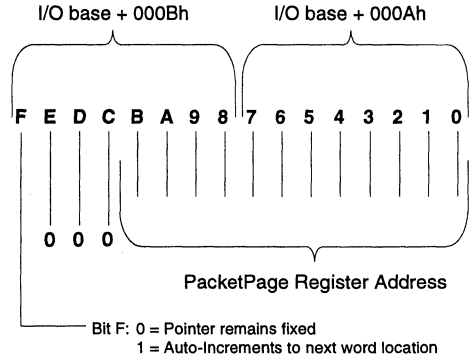


Figure 4.3. PacketPage Pointer Format

PacketPage Data Ports 0 and 1

The PacketPage Data Ports are used to transfer data to and from any of the CS8900's internal registers. Port 0 is used for 16-bit operations and Port 0 and 1 are used for 32-bit operations (lower word in Port 0).

I/O Mode Operation

For an I/O Read or Write operation, the AEN pin must be low, and the 16-bit I/O address on the ISA System Address bus (SA0 - SA15) must match the address space of the CS8900. For a Read, the $\overline{IOR}$ pin must be low, and for a Write, the $\overline{IOW}$ pin must be low.

Note: The ISA Latchable Address Bus (LA17 - LA23) is not needed for applications that use only I/O Mode and Receive DMA operation. For these applications, the $\overline{ELCS}$ pin is tied low.

Basic I/O Mode Transmit

I/O Mode transmit operations occur in the following order (using interrupts):

1. The host bids for storage of the frame by writing the Transmit Command to the TxCMD Port (I/O base + 0004h) and the transmit frame length to the TxLength Port (I/O base + 0006h).

2. The host reads the BusST register (Register 18) to see if the Rdy4TxNOW bit (Bit 8) is set. To read the BusST register, the host must first set the PacketPage Pointer at the correct location by writing 0138h to the PacketPage Pointer Port (I/O base + 000Ah). It can then read the BusST register from the PacketPage Data Port (I/O base + 000Ch). If Rdy4TxNOW is set, the frame can be written. If clear, the host must wait for CS8900 buffer memory to become available. If Rdy4TxiE (Register B, BufCFG, Bit 8) is set, the host will be interrupted when Rdy4Tx (Register C, BufEvent, Bit 8) becomes set. If the TxBidErr bit (Register 18, BusST, Bit 7) is set, the transmit length is not valid.

3. Once the CS8900 is ready to accept the frame, the host executes repetitive write instructions (REP OUT) to the Receive/Transmit Data Port (I/O base + 0000h) to transfer the entire frame from host memory to CS8900 memory.

For a more detailed description of transmit, see section 5.5.

Basic I/O Mode Receive

I/O Mode receive operations occur in the following order (In this example, interrupts are enabled to signal the presence of a valid receive frame):

1. A frame is received by the CS8900, triggering an enabled interrupt.

2. The host reads the Interrupt Status Queue Port (I/O base + 0008h) and is informed of the receive frame.

3. The host reads the frame data by executing repetitive read instructions (REP IN) from the Receive/Transmit Data Port (I/O base + 0000h) to transfer the frame from CS8900 memory to host memory. Preceding the frame data are the contents of the RxStatus register (PacketPage base + 0400h) and the RxLength register (PacketPage base + 0402h).

For a more detailed description of receive, see section 5.1.

Accessing Internal Registers

To access any of the CS8900's internal registers in I/O Mode, the host must first setup the PacketPage Pointer. It does this by writing the PacketPage address of the target register to the PacketPage Pointer Port (I/O base + 000Ah). The contents of the target register is then mapped into the PacketPage Data Port (I/O base + 000Ch).

If the host needs to access a sequential block of registers, the MSB of the PacketPage address of the first word to be accessed should be set to "1". The PacketPage Pointer will then move to

the next word location automatically, eliminating the need to setup the PacketPage Pointer between successive accesses (see Figure 4.3).

Polling the CS8900 in I/O Mode

If interrupts are not used, the host can poll the CS8900 to check if receive frames are present and if memory space is available for transmit. See the *CS8900 Technical Reference Manual* for more information about polling.

4.8 Interrupt Status Queue

The Interrupt Status Queue (ISQ) is used by the CS8900 to communicate Event reports to the host processor. Whenever an event occurs that triggers an enabled interrupt, the CS8900 sets the appropriate bit(s) in one of five registers, maps the contents of that register to the ISQ, and drives the selected interrupt request pin high (if an earlier interrupt is waiting in the queue, the interrupt request pin will already be high). When the host services the interrupt, it must first read the ISQ to learn the nature of the interrupt. It can then process the interrupt (the first read to the ISQ causes the interrupt request pin to go low.

Three of the registers mapped to the ISQ are event registers: RxEvent (Register 4), TxEvent (Register 8), and BufEvent (Register C). The other two registers are counter-overflow reports: RxMISS (Register 10), and TxCOL (Register 12). There may be more than one RxEvent report and/or more than one TxEvent report in the ISQ at a time. However, there may be only one BufEvent report, one RxMISS report and one TxCOL report in the ISQ at a time.

Event reports stored in the ISQ are read out in the order of priority, with RxEvents first (in order of occurrence), followed by TxEvents (in order of occurrence), BufEvent, RxMiss, and then TxCOL. The host only needs to read from one location to get the interrupt currently at the front of the queue. In Memory Mode, the ISQ is located at PacketPage base + 0120h. In I/O Mode, it is located at I/O base + 0008h. Each time the host reads the ISQ, the bits in the corresponding register are cleared and the next report in the queue moves to the front. Once the host starts reading the ISQ, it must read and process all Event reports in the queue. A read-out of a null word (0000h) indicates that all interrupts have been read.

The ISQ is read as a 16-bit word. The lower six bits (0 through 5) contain the register number (4, 8, C, 10, or 12). The upper ten bits (6 through F) contain the register contents. The host must always read the entire 16-bit word, because the CS8900 does not support 8-bit access to its internal registers. For further explanation of the ISQ, see the *CS8900 Technical Reference Manual.* Figure 4.4 shows the operation of the ISQ.

4.9 Destination Address Filter

The CS8900 is equipped with a Destination Address (DA) filter used to determine which receive frames will be accepted. (A receive frame is said to be "accepted" by the CS8900 when the frame data are placed in either on-chip memory, or in host memory by DMA). The DA filter can be configured to accept the following frame types:

Individual Address Frames: Frames whose DA matches the Individual Address (IA) stored at PacketPage base + 0158h, or whose DA matches one of the addresses programmed into the hash filter (the hash filter is described later is this section). The first bit of the DA is a "0" (DA[0] = 0) for all Individual Address frames (the "0" in the first bit position of the DA indicates that it is a Physical Address).

Multicast Frames: Frames whose DA passes though the hash filter (the hash filter is described later is this section). The first bit of the DA is a "1" (DA[0] = 1) for all Multicast frames (the "1" in the first bit position of the DA indicates that it is a Logical Address).

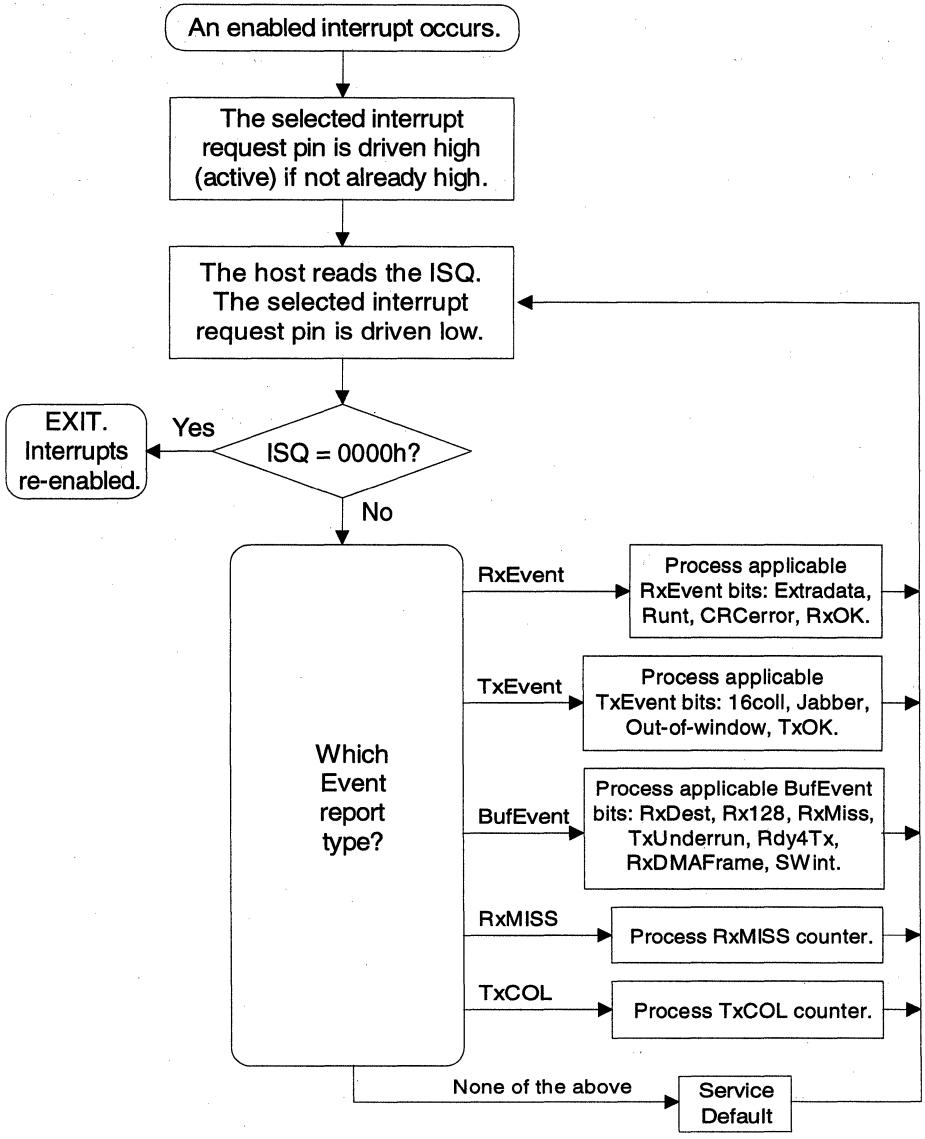


Figure 4.4 Interrupt Status Queue

Broadcast Frames: Frames with DA equal to FFFF FFFF FFFFh.

In addition, the CS8900 can be configured for Promiscuous Mode, in which case it will accept all receive frames, irrespective of DA.

Configuring the Destination Address Filter

The DA filter is configured by programming five DA filter bits in the RxCTL register (Register 5): IAHashA, PromiscuousA, MulticastA, IndividualA, and BroadcastA. Four of these bits are associated with four status bits in the RxEvent register (Register 4): IAHash, Hashed, IndividualAdr, and Broadcast. The RxEvent register reports the results of the DA filter for a given receive frame. The bits associated with DA filtering are summarized below:

Bit #	RxCTL Register 5	RxEvent Register 4
6	IAHashA	IAHash (used only if IAHashA = 1)
7	PromiscuousA	
9	MulticastA	Hashed
A	IndividualA	IndividualAdr (used only if IndividualA = 1)
B	BroadcastA	Broadcast (used only if BroadcastA = 1)

The IAHashA, MulticastA, IndividualA, and BroadcastA bits are used independently. As a result, many DA filter combinations are possible. For example, if MulticastA and IndividualA are set, then all frames that are either Multicast or Individual Address frames are accepted. The PromiscuousA bit, when set, overrides the other four DA bits, and allows all valid frames to be accepted. Table 4.5 summarizes the configuration options available for DA filtering.

Hash Filter

The hash filter is used to help determine which Multicast frames and which Individual Address frames should be accepted by the CS8900.

Hash Filter Operation: The DA of the incoming frame is passed through the CRC logic, generating a 32-bit CRC value. The 6 most significant bits of the CRC are latched into the 6-bit hash register (HR). The contents of the HR are passed through a 6-to-64-bit decoder, asserting one of the decoder's outputs. The asserted output is compared with a corresponding bit in the 64-bit Logical Address Filter, located at PacketPage base + 0150h. If the decoder output and the Logical Address Filter bit match, the frame passes the hash filter and the Hashed bit (Register 4, RxEvent, Bit 9) is set. If the two do not match, the frame fails the filter and the Hashed bit is clear. For additional information about the Destination Address filter, see the *CS8900 Technical Reference Manual.*

IAHashA	PromiscuousA	MulticastA	IndividualA	BroadcastA	Frames Accepted
0	0	0	1	0	Individual Address frames with DA matching the IA at PacketPage base + 0158h
1	0	0	0	0	Individual Address frames with DA that pass the hash filter (DA[0] must be "0")
0	0	1	0	0	Multicast frames with DA that pass the hash filter (DA[0] must be "1")
0	0	0	0	1	Broadcast frames
X	1	X	X	X	All frames

Table 4.5. Configuration Options Available for DA filtering.

Whenever the hash filter is passed by a "good" frame, the RxOK bit (Register 4, RxEvent, Bit 8) is set and the bits in the HR are mapped to the Hash Table Index bits (Register 4, RxEvent, Bits A through F).

4.10 Counters

The CS8900 has three 10-bit counters useful for managing network performance and locating potential problems.

RxMISS Counter

The RxMISS counter (Register 10, RxMISS, Bits 6 through F) records the number of receive frames that are lost (missed) due to the lack of available buffer space. If the MissOvfloiE bit (Register B, BufCFG, Bit D) is set, there is an interrupt when RxMISS increments from 1FFh to 200h. This interrupt provides the host with an early warning that the RxMISS counter should be read before it reaches 3FFh and starts over (by interrupting at 200h, the host has an additional 512 counts before RxMISS actually overflows). The RxMISS counter is cleared when read.

TxCOL Counter

The TxCOL counter (Register 12, TxCOL, Bits 6 through F) is incremented whenever the 10BASE-T Receive Pair (RXD+ / RXD-) or AUI Collision Pair (CI+ / CI-) become active while a packet is being transmitted. If the TxColOvfiE bit (Register B, BufCFG, Bit C) is set, there is an interrupt when TxCOL increments from 1FFh to 200h. This interrupt provides the host with an early warning that the TxCOL counter should be read before it reaches 3FFh and starts over (by interrupting at 200h, the host has an additional 512 counts before TxCOL actually overflows). The TxCOL counter is cleared when read.

TDR Counter

The TDR counter (Register 1C, TDR, Bits 6 through F) is a time domain reflectometer useful in locating cable faults in 10BASE-2 and 10BASE-5 coax networks. It counts at a 10 MHz rate from the beginning of transmission on the AUI to when a collision or Loss-of-Carrier error occurs. The TDR counter is cleared when read.

4.11 8 and 16-Bit Transfers

A data transfer to or from the CS8900 can be done in either I/O or Memory space, and can be either 16 bits wide (word transfers) or 8 bits wide (byte transfers). Because the CS8900's internal architecture is based on a 16-bit data bus, word transfers are the most efficient.

To transfer transmit frames to the CS8900 and receive frames from the CS8900, the host may mix word and byte transfers, provided it follows three rules:

1. The primary method used to access CS8900 memory is word access.

2. Word accesses to the CS8900's internal memory are kept on even-byte boundaries.

3. When switching from byte accesses to word accesses, a byte access to an even byte address must be followed by a byte access to an odd-byte address before the host may execute a word access (this will re-align the word transfers to even-byte boundaries). On the other hand, a byte access to an odd-byte address may be followed by a word access.

Failure to observe these three rules may cause data corruption.

Transferring Odd-Byte-Aligned Data

Some applications gather transmit data from more than one section of host memory. The boundary between the various memory locations may be either even or odd-byte aligned. When such a boundary is odd-byte aligned, the host should transfer the last byte of the first block to an even address, followed by the first byte of the second block to the following odd-address. It can then resume word transfers. An example of this is shown in figure 4.5.

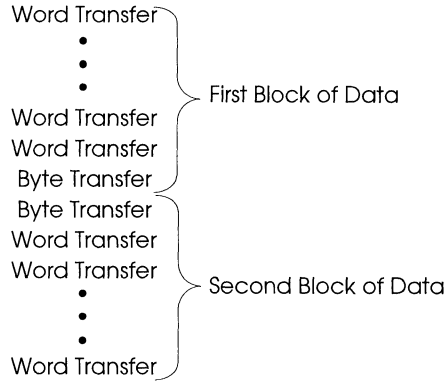


Figure 4.5. Odd-Byte Aligned Data

Random Access to CS8900 Memory

The first 124 bytes of a receive frame held in the CS8900's on-chip memory may be randomly accessed in Memory mode. After the first 124 bytes, only sequential access of received data is allowed. Either byte or word access is permitted, as long as all word accesses are executed to even-byte boundaries. For additional information about byte and word transfers, see the CS8900 Technical Reference Manual.

5.0 OPERATION

5.1 Basic Receive Operation

Overview

Once an incoming packet has passed through the analog front end and Manchester decoder, it goes through the following three-step receive process:

1. Pre-Processing
2. Temporary Buffering
3. Transfer to Host

Figure 5.1 shows the steps in frame reception.

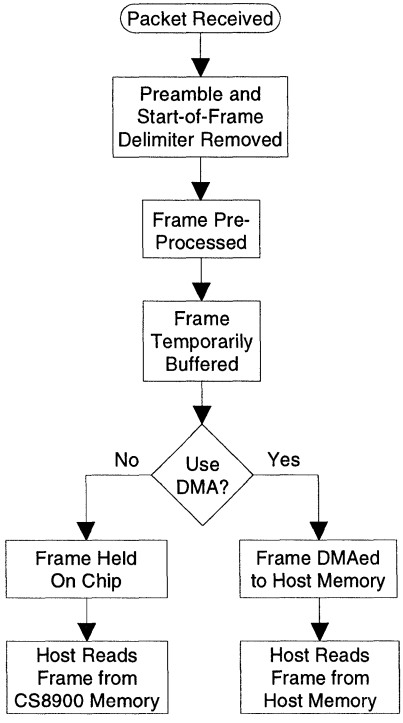


Figure 5.1. Frame Reception

As shown in the figure, all receive frames go through the same pre-processing and temporary buffing phases, regardless of transfer method. Once a frame has been pre-processed and buffered, it can be accessed by the host in either Memory or I/O space. In addition, the CS8900 can transfer receive frames to host memory via host DMA. This section describes receive frame pre-processing and Memory and I/O space receive operation. Sections 5.2 through 5.4 describe DMA operation.

Terminology: Packet, Frame, and Transfer

The terms Packet, Frame, and Transfer are used extensively in the following sections. They are defined below for clarity:

Packet: The term "packet" refers to the entire serial string of bits transmitted over an Ethernet network. This includes the preamble, Start-of-Frame Delimiter (SFD), Destination Address (DA), Source Address (SA), Length field, Data field, pad bits (if necessary), and Frame Check Sequence (FCS, also called CRC). Figure 3.6 shows the format of a packet.

Frame: The term "frame" refers to the portion of a packet from the DA to the CRC. This includes the Destination Address (DA), Source Address (SA), Length field, Data field, pad bits (if necessary), and Frame Check Sequence (FCS, also called CRC). Figure 3.6 shows the format of a frame. The term "frame data" refers to all the data from the DA to the CRC that is to be transmitted, or that has been received.

Transfer: The term "transfer" refers to moving data across the ISA bus, to and from the CS8900. During receive operations, only frame data are transferred from the CS8900 to the host (the preamble and SFD are stripped off by the CS8900's MAC engine). The CRC may or may not be transferred, depending on the configuration. All transfers to and from the CS8900 are

counted in bytes, but may be padded for double word alignment.

Receive Configuration

After each reset, the CS8900 must be configured for receive operation. This can be done automatically, using an attached EEPROM, or by writing configuration commands to the CS8900's internal registers (see section 3.4). The items that must be configured include:

- which physical interface to use;
- what types of frames to accept;
- what receive events cause interrupts; and,
- how received frames are transferred.

Configuring the Physical Interface: Configuring the physical interface consists of determining which Ethernet interface should be active, and enabling the receive logic for serial reception. This is done via the LineCTL register (Register 13) and is described in table 5.1.

Register 13, LineCTL		
Bit	**Bit Name**	**Operation**
6	SerRxON	When set, reception enabled.
8	AUIonly	When set, AUI selected (takes precedence over AutoAUI/10BT). When clear, 10BASE-T selected.
9	AutoAUI/ 10BT	When set, automatic interface selection enabled.
E	LoRx Squelch	When set, receiver squelch level reduced by approximately 6 dB.

Table 5.1. Physical Interface Configuration

Choosing what Frame Types to Accept: The RxCTL register (Register 5) is used to determine what frame types will be accepted by the CS8900 (a receive frame is said to be "accepted" when the frame is buffered, either on chip or in host memory via DMA). Table 5.2 describes the configuration bits in this register.

Register 5, RxCTL		
Bit	**Bit Name**	**Operation**
6	IAHashA	When set, Individual Address frames that pass the hash filter are accepted*.
7	Promis cuousA	When set, all frames are accepted*.
8	RxOKA	When set, frames with valid lenght and CRC and that pass the DA filter are accepted.
9	MulticastA	When set, Multicast frames that pass the hash filter accepted*.
A	IndividualA	When set, frames with DA that matches the IA at PacketPage base + 0158h are accepted*.
B	BroadcastA	When set, all broadcast frames are accepted*.
C	CRCerrorA	When set, frames wtih bad CRC that pass the DA filter are accepted.
D	RuntA	when set, frames shorter than 64 bytes that pass the DA filter are accepted.
E	ExtradataA	When set, frames longer than 1518 bytes that pass the DA filter are accepted (only the first 1518 bytes are buffered).

* Must also meet the criteria programmed into bits 8, C, D, and E.

Table 5.2. Frame Acceptance Criteria

Selecting what Events Cause Interrupts: The RxCFG register (Register 3) and the BufCFG register (Register B) are used to determine what receive events will cause interrupts to the host processor. Table 5.3 describes the interrupt enable (iE) bits in these registers.

Register 3, RxCFG		
Bit	**Bit Name**	**Operation**
8	RxOKiE	When set, there is an interrupt if a frame is received with valid length and CRC*.
C	CRCerroriE	When set, there is an interrupt if a frame is received with bad CRC*.
D	RuntiE	When set, there is an interrupt if a frame is received that is shorter than 64 bytes*.
E	ExtradataiE	When set, there is an interrupt if a frame is received that is longer than 1518 bytes*.

* Must also pass the DA filter before there is an interrupt.

Table 5.3. Interrupt Configuration

Register B, BufCFG		
Bit	**Bit Name**	**Operation**
7	RxDMAiE	When set, there is an interrupt if one or more frames are transferred via DMA.
A	RxMissiE	When set, there is an interrupt if a frame is missed due to insufficient receive buffer space.
B	Rx128iE	When set, there is an interrupt after the first 128 bytes of receive data have been buffered.
D	MissOvfloiE	When set, there is an interrupt if the RxMISS counter overflows.
F	RxDestiE	When set, there is an interrupt after the DA of an incoming frame has been buffered.

Table 5.3. Interrupt Configuration (cont.)

Choosing How to Transfer Frames: The RxCFG register (Register 3) and the BusCTL register (Register 17) are used to determine how frames will be transferred to host memory, as described in table 5.4.

Register 3, RxCFG		
Bit	**Bit Name**	**Operation**
7	StreamE	When set, StreamTransfer enabled.
9	RxDMAonly	When set, DMA slave operation used for all receive frames.
A	AutoRx DMAE	When set, Auto-Switch DMA enabled.
B	BufferCRC	When set, the received CRC is buffered.
Register 17, BusCTL		
Bit	**Bit Name**	**Operation**
B	DMABurst	When set, DMA operations hold the bus for up to approzimately 30 µs. When clear, DMA operations are continuous.
F	RxDMAsize	When set, DMA buffer size is 64 Kbytes. When clear, DMA buffer size is 16 Kbytes.

Table 5.4. Frame Transfer Method

Receive Frame Pre-Processing

The CS8900 pre-processes all receive frames using a four step process:

1. Destination Address filtering;
2. Early Interrupt Generation;
3. Acceptance filtering; and,
4. Normal Interrupt Generation.

Figure 5.2 provides a diagram of frame pre-processing.

Destination Address Filtering: All incoming frames are passed through the Destination Address filter (DA filter). If the frame's DA passes the DA filter, the frame is passed on for further pre-processing. If it fails the DA filter, the frame is discarded. See section 4.9 for a more detailed description of DA filtering.

Early Interrupt Generation: The CS8900 support the following two early interrupts that can be used to inform the host that a frame is being received:

- ***RxDest:*** The RxDest bit (Register C, BufEvent, Bit F) is set as soon as the Destination Address (DA) of the incoming frame passes the DA filter. If the RxDestiE bit (Register B, BufCFG, bit F) is set, the CS8900 generates a corresponding interrupt. Once RxDest is set, the host is allowed to read the incoming frame's DA (the first 6 bytes of the frame).
- ***Rx128:*** The Rx128 bit (Register C, BufEvent, Bit B) is set as soon as the first 128 bytes of the incoming frame have been received. If the Rx128iE bit (Register B, BufCFG, bit B) is set, the CS8900 generates a corresponding interrupt. Once the Rx128 bit is set, the RxDest bit is cleared and the host is allowed to read the first 128 bytes of the incoming frame. The Rx128 bit is cleared by the host reading the BufEvent register (either directly or through the Interrupt Status Queue) or by the CS8900 detecting the incoming frame's End-of-Frame (EOF) sequence.

Like all Event bits, RxDest and Rx128 are set by the CS8900 whenever the appropriate event occurs. Unlike other Event bits, RxDest and Rx128 may be cleared by the CS8900 without host intervention. All other event bits are cleared only by the host reading the appropriate event register, either directly or through the Interrupt Status Queue (ISQ). (RxDest and Rx128 can also be cleared by the host reading the BufEvent register, either directly or through the Interrupt Status Queue). Figure 5.3 provides a diagram of the Early Interrupt process.

Acceptance Filtering: The third step of pre-processing is to determine whether or not to accept the frame by comparing the frame with the criteria programmed into the RxCTL register (Register 5). If the receive frame passes the Acceptance filter, the frame is buffered, either on chip or in host memory via DMA. If the frame fails the Acceptance filter, it is discarded. The results of the Acceptance filter are reported in the RxEvent register (Register 4).

Normal Interrupt Generation: The final step of pre-processing is to generate any enabled interrupts that are triggered by the incoming frame. Interrupt generation occurs once the entire frame has been buffered (up to the first 1518 bytes). For more information about interrupt generation, see section 4.8.

Held vs. DMAed Receive Frames

All accepted frames are either held in on-chip RAM until processed by the host, or stored in host memory via DMA. A receive frame that is held in on-chip RAM is referred to as a held receive frame. A frame that is stored in host memory via DMA is a DMAed receive frame. This section describes buffering and transferring held receive frames. Sections 5.2 through 5.4 describes DMAed receive frames.

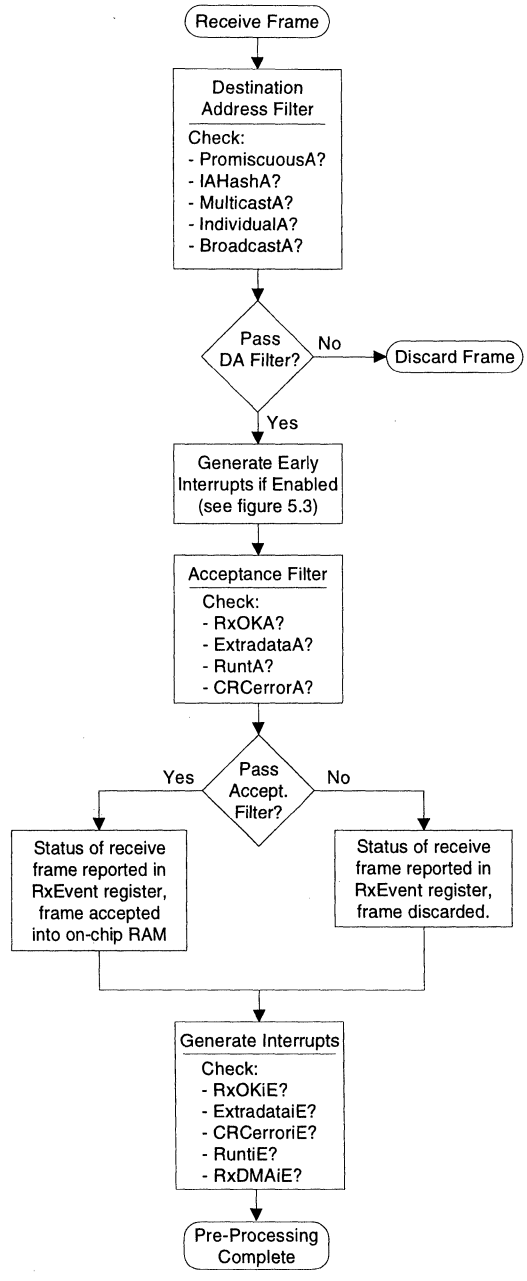


Figure 5.2. Receive Frame Pre-Processing

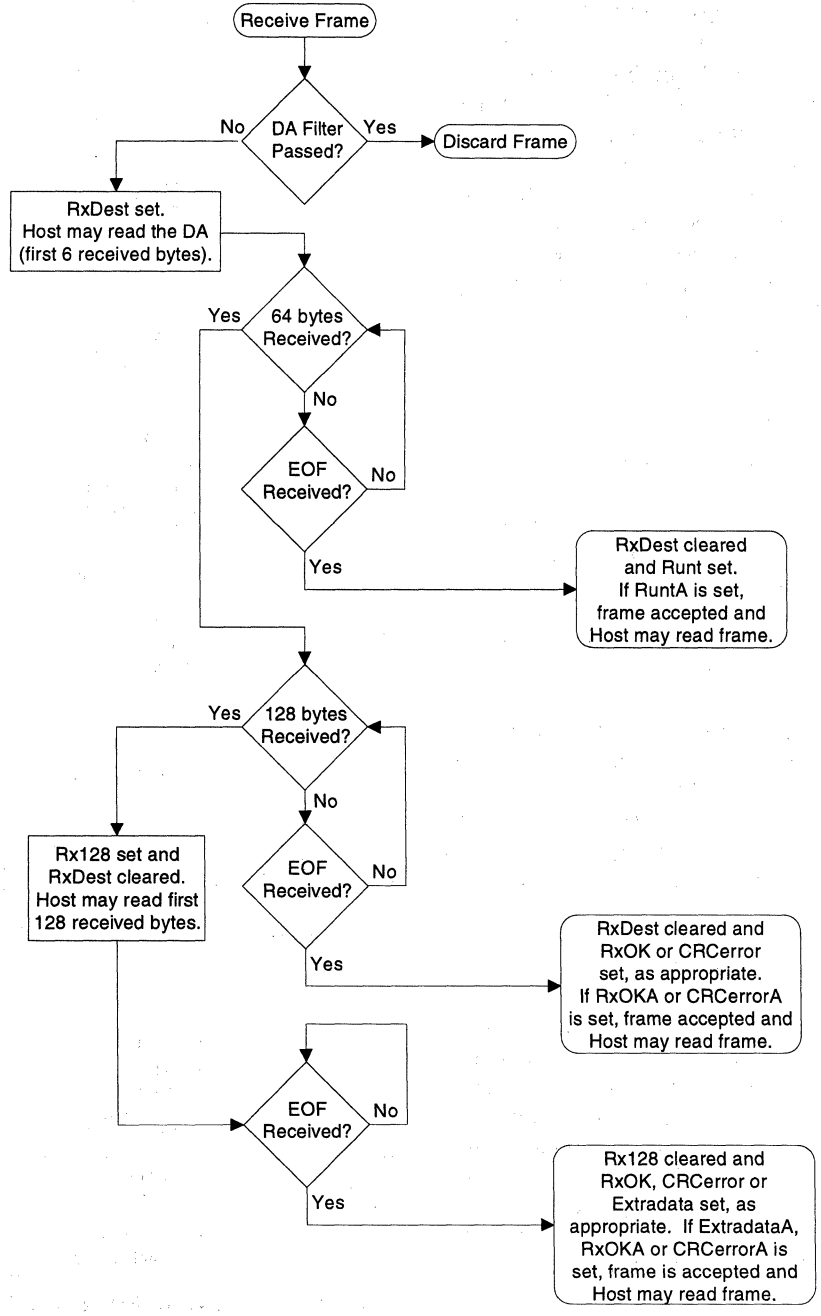


Figure 5.3. Early Interrupt Generation

Buffering Held Receive Frames

If space is available, an incoming frame will be temporarily stored in on-chip RAM, where it awaits processing by the host. Although this receive frame now occupies on-chip memory, the CS8900 does not commit the memory space to it until one of the following two conditions is true:

1. The entire frame has been received AND the host has learned about the frame by reading the RxEvent register (Register 4), either directly or through the ISQ.

Or:

2. The frame has been partially received, causing either the RxDest bit (Register C, BufEvent, Bit F) or the Rx128 bit (Register C, BufEvent, Bit B) to become set, AND the host has learned about the receive frame by reading the BufEvent register (Register C), either directly or through the ISQ.

Once the CS8900 commits buffer space to a particular held receive frame (termed a committed received frame), no data from subsequent frames can be written to that buffer space until the frame is freed from commitment. (The committed received frame may or may not have been received error free.)

A received frame is freed from commitment by any one of the following conditions:

1. The host reads the entire frame sequentially in the order that it was received (first byte in, first byte out).

Or:

2. The host reads part or none of the frame, and then issues a Skip command by setting the Skip_1 bit (Register 3, RxCFG, bit 6).

Or:

3. The host reads part of the frame and then reads the RxEvent register (Register 5), either directly or through the ISQ, and learns of another receive frame. (This condition is called an "implied Skip".)

Both early interrupts are disabled whenever there is a committed receive frame waiting to be processed by the host

Transferring Held Receive Frames

The host can readout held receive frames in Memory or I/O space. To transfer frames in Memory space, the host executes repetitive Move instructions (REP MOVS) from PacketPage base + 0404h. To transfer frames is I/O space, the host executes repetitive In instructions (REP IN) from I/O base + 0000h, with status and length preceding the frame.

There are three possible ways that the host can learn the status of a particular frame. It can:

1. Read the Interrupt Status Queue;

2. Read the RxEvent register directly (Register 4); or

3. Read the RxStatus register (PacketPage base + 0400h).

Receive Frame Visibility

Only one receive frame is visible to the host at a time. Its status can be read from the RxStatus register (PacketPage base + 0400h) and its length can be read from the RxLength register (PacketPage base + 0402h). For more information about Memory space operation, see section 4.6. For more information about I/O space operation, see section 4.7.

Example of Memory Mode Receive Operation

A common length for short frames is 64 bytes, including the 4 byte CRC. Suppose that such a frame has been received with the CS8900 configured as follows:

- The BufferCRC bit (Register 3, RxCFG, Bit B) is set causing the 4 byte CRC to be buffered with the rest of the receive data.
- The RxOKA bit (Register 5, RxCTL, Bit 8) is set, causing the CS8900 to accept good frames (a good frame is one with legal length and valid CRC).
- The RxOKiE bit (Register 3, RxCFG, Bit 8) is set, causing an interrupt to be generated whenever a good frame is received.

Then the transfer to the host would proceed as follows:

1. The CS8900 generates an RxOK interrupt to the host to signal the arrival of a good frame.
2. The host reads the ISQ (PacketPage base + 0120h) to asses the status of the receive frame and sees the contents of the RxEvent register (Register 4) with the RxOK bit (Bit 8) set.
3. The host reads the receive frame's length from the RxLength register (PacketPage base + 0402h).
4. The host reads the frame data by executing 32 consecutive MOV instructions from PacketPage base + 0404h.

The memory map of the 64 byte frame is given in table 5.5.

Memory Space Word Offset	Description of Data Stored in On-chip RAM
0400h	RxStatus Register (the host may skip reading 0400h since RxEvent was read from the ISQ.)
0402h	RxLength Register (In this example, the length is 40h bytes. The lenght count starts at 0404h, and runs through 0443h.)
0404h to 0409h	6-byte Source Address.
040Ah to 040Fh	6-byte Destination Address.
0410h to 011h	2-byte Type Field.
0412h to 043Fh	46 bytes of data.
0440h	CRC, bytes 1 and 2
0442h	CRC, bytes 3 and 4

Table 5.5. Example Memory Map

5.2 Receive DMA

Overview

The CS8900 supports a direct interface to the host DMA controller allowing it to transfer receive frames to host memory via slave DMA. The DMA option applies only to receive frames, and not transmit operation. The CS8900 offers three possible Receive DMA modes:

1. Receive-DMA-only mode: All receive frames are transferred via DMA.
2. Auto-Switch DMA: DMA is used only when needed to help prevent missed frames.
3. StreamTransfer: DMA is used to minimize the number of interrupts to the host.

This sections provides a description of Receive-DMA-only mode. Section 5.3 describes Auto-Switch DMA and Section 5.4 describes StreamTransfer.

Configuring the CS8900 for DMA Operation

The CS8900 interfaces to the host DMA controller through one pair of the DMA

request/acknowledge pins (see section 3.2 for a description of the CS8900's DMA interface).

Four 16-bit registers are used for DMA operation. These are described in table 5.6.

PacketPage Address	Register Description
0024h	**DMA Channel Number:** DMA channel number (0, 1, or 2) which defines the DMARQ/DMACK pin pair used.
0026h	**DMA Start of Frame:** 16-bit value which defines the offset from the DMA base address to the start of the most recently transferred received frame.
0028h	**DMA Frame Count:** The lower 12 bits define the number of valid frames transferred via DMA since the last readout of this register. The upper 4 bits are reserved and not applicable.
002Ah	**DMA Byte Count:** Defines the number of bytes that have been transferred via DMA since the last readout of this register.

Table 5.6. Receive DMA Registers

Receive-DMA-only mode is enabled by setting the RxDMAonly bit (Register 3, RxCFG, Bit 9).

Note: If the RxDMAonly bit and the AutoRxDMAE bit (Register 3, RxCFG, Bit A) are both set, then RxDMAonly takes precedence, and the CS8900 is in DMA mode for all receive frames.

DMA Receive Buffer Size

In receive DMA mode, the CS8900 stores received frames (along with their status and length) in a circular buffer located in host memory space. The size of the circular buffer is determined by the RxDMAsize bit (Register 17, BusCTL, Bit D). When RxDMAsize is clear, the buffer size is 16 Kbyte. When RxDMAsize is set, the buffer is 64 Kbyte. It is the host's task to locate and keep track of the DMA receive buffer's base address. The DMA Start of Frame register is the only circuit affected by this bit.

Receive DMA Only Operation

If space is available, an incoming frame will be temporarily stored in on-chip RAM. Once the entire frame has been received, pre-processed and accepted, the CS8900 signals the DMA controller that a frame is to be transferred to host memory by driving the selected DMA Request pin high. The DMA controller acknowledges the request by driving the DMA Acknowledge pin low. The CS8900 then transfers the contents of the RxStatus register (PacketPage base + 0400h) and the RxLength register (PacketPage base + 0402h) to host memory, followed by the frame data. If the DMABurst bit (Register 17, BusCTL, Bit B) is clear, the DMA Request pin will remain high until the entire frame is transferred. If the DMABurst bit is set, the DMA Request pin remains high for a maximum of 30 µs and then goes low for a minimum of 0.8 µs to give the CPU and other peripherals access to the bus.

- Once the transfer is complete, the CS8900 does the following:
- updates the DMA Start of Frame register (PacketPage base + 0026h);
- updates the DMA Frame Count register (PacketPage base + 0028h);
- updates DMA Byte Count register (PacketPage base + 002Ah);
- sets the RxDMAFrame bit (Register C, BufEvent, Bit 7); and,
- de-allocates the buffer space used by the transferred frame.

In addition, if the RxDMAiE bit (Register B, BufCFG, Bit 7) is set, there is a corresponding interrupt.

When the host processes DMAed frames, it must read either the DMA Frame Count register and the DMA Byte Count register together, or the DMA Start of Frame register and the DMA Frame Count register together. More detailed information concerning receive DMA operation may be found in the *CS8900 Reference Manual.*

Whenever a receive frame is missed (lost) due to insufficient receive buffer space, the RxMISS counter (Register 10) is incremented. A missed receive frame causes the counter to increment in either DMA or non-DMA modes.

Committing Buffer Space to a DMAed Frame

Although a receive frame may occupy space in the host memory's circular DMA buffer, the CS8900's Memory Manager does not commit the buffer space to it until the entire frame has been transferred AND the host learns of its existence by reading the Frame Count register (PacketPage base + 0028h).

Once the CS8900 commits DMA buffer space to a particular DMAed receive frame (termed a committed received frame), no data from subsequent frames can be written to that buffer space until the frame is freed from commitment. (The committed received frame may or may not have been received error free.)

A committed DMAed receive frame is freed from commitment by any one of the following conditions:

1. The host re-reads the DMA Frame Count register (PacketPage base + 0028h).

2. New frames have been transferred via DMA and the host reads the BufEvent register (either directly or from the ISQ) and sees that the RxDMAFrame bit is set (this condition is termed an "implied Skip").

3. The host issues a Reset-DMA command by setting the ResetRxDMA bit (Register 17, BusCTL, Bit 6).

DMA Buffer Organization

When DMA is used to transfer receive frames, the DMA Start of Frame register (PacketPage Base + 0026h) defines the offset from the DMA base to the start of the most recently transferred received frame. Frames stored in the DMA buffer are transferred as words and maintain double-word (32-bit) alignment. As a result of double-word alignment, there may be unfilled memory space between successive frames stored in the DMA buffer. These "holes" may be 1, 2 or 3 bytes, depending on the length of the frame preceeding the hole.

RxDMAFrame Bit

The RxDMAFrame bit (Register C, BufEvent, bit 7) is controlled by the CS8900 and is set whenever the value in the DMA Frame Count register is non-zero. The host cannot clear RxDMAFrame by reading the BufEvent register (Register C). Table 5.7 summarizes the criteria used to set and clear RxDMAFrame.

Receive DMA Example Without Wrap-Around

Figure 5.4 shows three frames stored in host memory by DMA without wrap-around.

	Non-Stream Transfer Mode	Stream Transfer Mode (see section 5.4)
To Set RxDMAFrame	The RxDMAFrame bit is set whenever the DMA Frame Count register (PacketPage base + 0028h) transitions to non-zero.	The RxDMAFrame bit is set at the end of a Stream Transfer cycle.
To Clear RxDMAFrame	The DMA Frame Count is zero.	The DMA Frame Count is zero.

Table 5.7. RxDMAFrame Bit

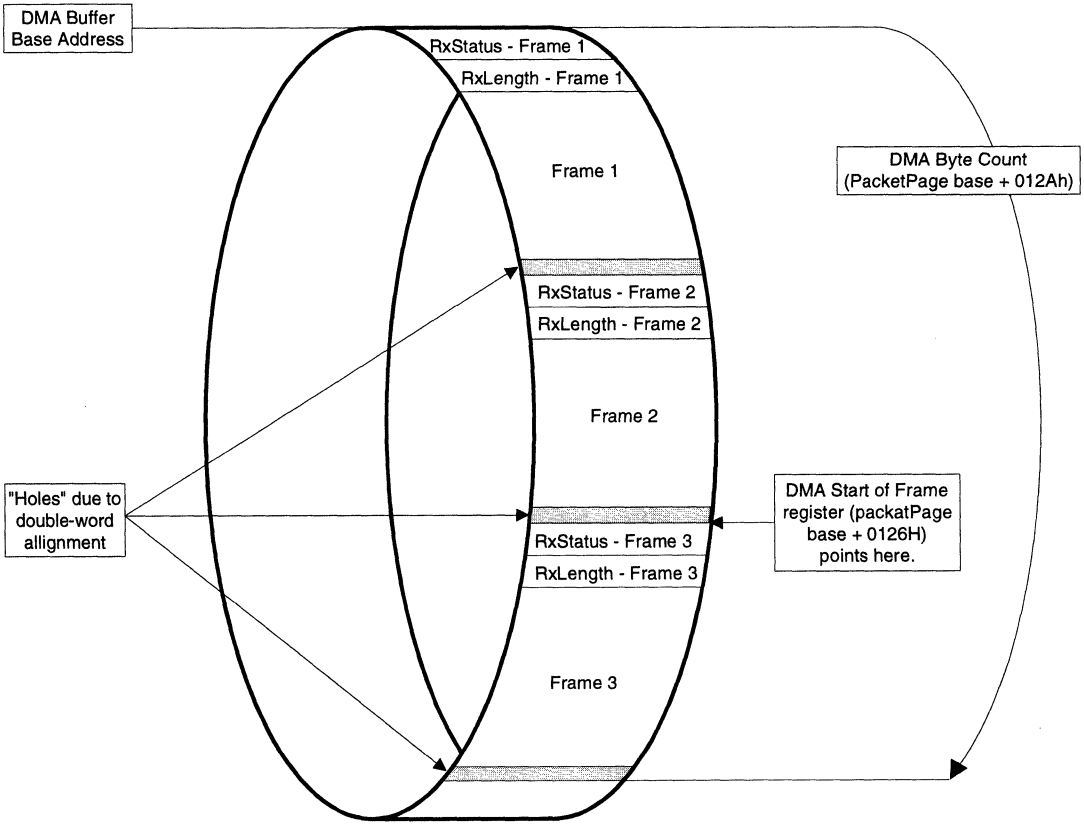


Figure 5.4. Example of Frames Stored in DMA Buffer

5.3 Auto-Switch DMA

Overview

The CS8900 supports a unique feature, called Auto-Switch DMA, that allows it to switch between Memory or I/O mode and Receive DMA automatically. This feature allows the CS8900 to realize the performance advantages of Memory or I/O mode, while minimizing the number of missed frames that could result due to slow processing by the host.

Configuring the CS8900 for Auto-Switch DMA

Auto-Switch DMA mode requires the same configuration as Receive DMA-only mode, with one exception. The AutoRxDMAE bit (Register 3, RxCFG, Bit A) must be set and the RxDMAonly bit (Register 3, RxCFG, Bit 9) must be clear (see section 5.2, Configuring the CS8900 for DMA Operation). In Auto-Switch DMA mode, the CS8900 operates in non-DMA mode if possible, only switching to slave DMA if necessary.

Note: If the AutoRxDMAE bit and the RxDMAonly bit (Register 3, RxCFG, bit 9) are both set, the CS8900 will use DMA for all receive frames.

Auto-Switch DMA Operation

Whenever a frame begins to be received in Auto-Switch DMA mode, the CS8900 checks to see if there is enough on-chip buffer space to store a maximum length frame. If there is, the incoming frame is pre-processed and buffered as normal. If there isn't, the CS8900's MAC engine compares the frame's Destination Address (DA) to the criteria programmed into the DA filter. If the incoming DA fails the DA filter, the frame is discarded. If the DA passes the DA filter, the CS8900 automatically switches to DMA mode and starts transferring the frame(s) currently being held in the on-chip buffer into host memory. This frees up buffer space for the incoming frame.

Figure 5.5 shows the steps the CS8900 goes through in determining when to automatically switch to DMA.

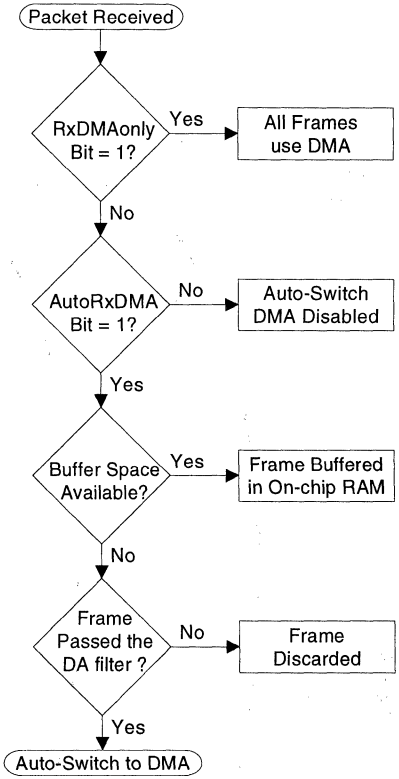


Figure 5.5. Conditions for Switching to DMA

Whenever the CS8900 automatically enters DMA, there is at least one complete frame already stored in the on-chip buffer. Because frames are transferred to the host in the same order as received (first in, first out), the beginning of the received frame that triggered the switch to DMA is not the first frame to be transferred. Instead, the oldest non-committed frame in the on-chip buffer is the first frame to use DMA. When DMA begins, any pending RxEvent reports in the Interrupt Status Queue are discarded,

because the host cannot process those events until the corresponding frames have been completely DMAed.

Receive DMA works only on entire received frames. The CS8900 does not use DMA to transfer partial frames. After a complete frame has been moved to host memory, the CS8900 updates the DMA Start of Frame register (PacketPage base + 0126h), the DMA Frame Count register (PacketPage base + 0128h) and the DMA Byte Count register, and then sets the RxDMAFrame bit (Register C, BufEvent, bit 7). If RxDMAiE (Register B, BufCFG, bit 7) is set, there is a corresponding interrupt.

DMA Channel Speed vs. Missed Frames

When the CS8900 starts DMA, the entire oldest non-committed frame must be placed in host memory before on-chip buffer space will be freed for the next incoming frame. Suppose that the oldest frame is relatively large, and the next incoming frame also large. Under these conditions, the incoming frame may be missed, depending on the speed of the DMA channel. If this happens, the CS8900 will increment the RxMiss counter (Register 10) and clear any event reports (RxEvent and BufEvent) associated with the missed frame.

Exit From DMA

Once the CS8900 has activated receive DMA, it remains is DMA mode until all of the following are true:

- The host processes all RxEvent and BufEvent reports pending in the ISQ.
- The host reads a zero value from the DMA Frame Count register (PacketPage base + 0028h).
- The CS8900 is not in the process of transferring a frame via DMA.

For more information about Auto-Switch DMA mode, see the CS8900 Technical Reference Manual.

Auto-Switch DMA Example

Figure 5.6 shows how the CS8900 enters and exits Auto-Switch DMA mode.

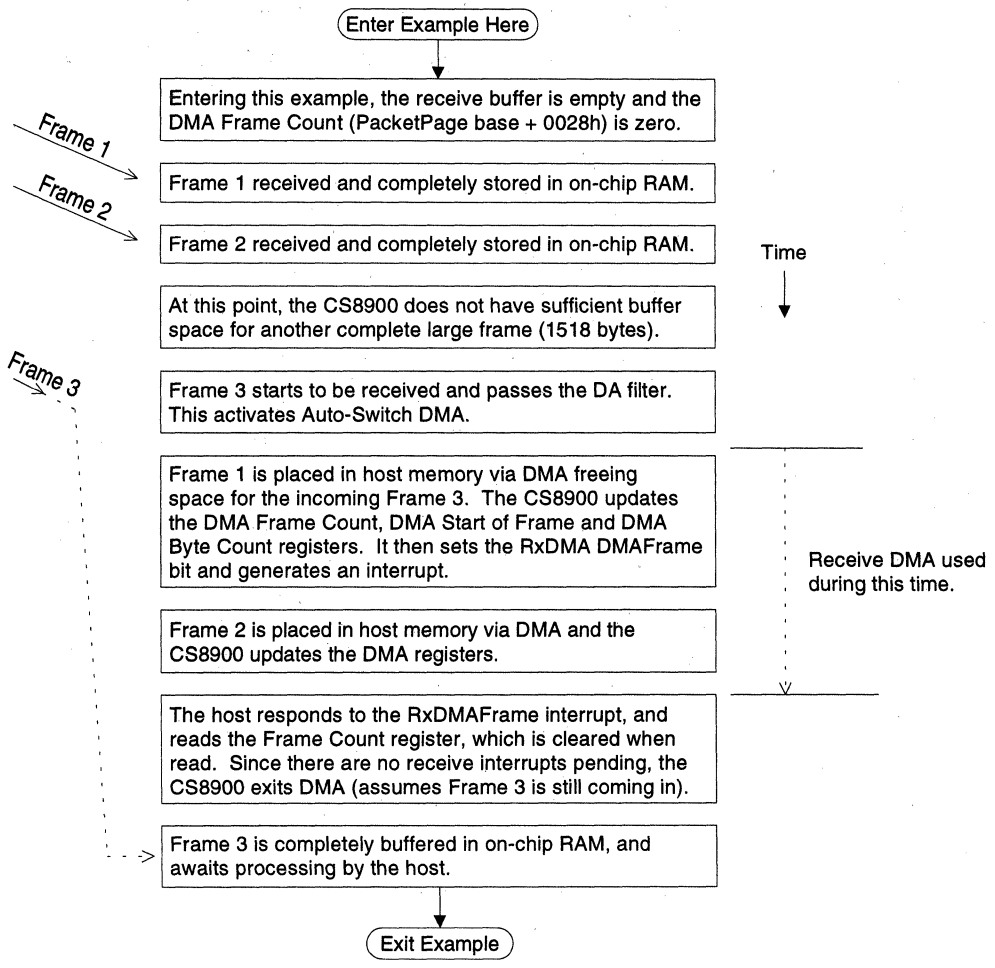


Figure 5.6. Example of Auto-Switch DMA

5.4 StreamTransfer

Overview

The CS8900 supports an optional feature, called StreamTransfer, that can reduce the amount CPU overhead associated with frame reception. It works during periods of high receive activity by grouping multiple receive events into a single interrupt, thereby reducing the number of receive interrupts to the host processor. During periods of peak loading, StreamTransfer will eliminate 7 out of every 8 interrupts, cutting interrupt overhead by up to 87%.

Configuring the CS8900 for StreamTransfer

StreamTransfer is enabled by setting the StreamE bit along with either the AutoRxDMAE bit or the RxDMAonly bit. StreamTransfer only applies to "good" frames (frames of legal length with valid CRC). Therefore, the RxOKA bit and the RxOKiE bit must both be set. Finally, StreamTransfer works on whole packets, and thus is not compatible with early interrupts. This requires that the RxDestiE bit and the Rx128iE bit both be clear.

Table 5.8 summarizes how to configure the CS8900 for StreamTransfer.

Register Name	Bit	Bit Name	Value
Register 3, RxCFG	7	StreamE	1
	8	RxOKiE	1
	9 or A	RxDMAonly or AutoRxDMA	1 or 1
Register 5, RxCTL	8	RxOKA	1
Register B, BufCFG	7	RxDMAiE	1
	F	RxDestiE	0
	B	Rx128iE	0

Table 5.8. StreamTransfer Configuration

StreamTransfer Operation

If StreamTransfer is enabled, the CS8900 will initiate a StreamTransfer cycle whenever two or more frames are received that:

1. pass the Destination Address filter;
2. are of legal length with valid CRC; and,
3. are spaced "back-to-back" (between 9.6 and 52 µs apart).

During a StreamTransfer cycle the CS8900 does the following:

- delays the normal RxOK interrupt associated with the first receive frame;
- switches to receive DMA mode;
- transfers up to eight receive frames into host memory via DMA;
- updates the DMA Start of Frame register (PacketPage base + 0026h);
- updates the DMA Frame Count register (PacketPage base + 0028h);
- updates DMA Byte Count register (PacketPage base + 002Ah);
- sets the RxDMAFrame bit (Register C, BufEvent, Bit 7); and,
- generates an RxDMAFrame interrupt.

Keeping StreamTransfer Mode Active

Once the CS8900 initiates a StreamTransfer cycle, it will continue to execute cycles as long as the following conditions hold true:

- all packets received are of legal length with valid CRC;

- each packet follows its predecessor by less than 52 µs; and,
- the DA of each packet passes the DA filter.

If any of these conditions are not met, the CS8900 exits StreamTransfer by generating RxOK and RxDMA interrupts. The CS8900 then returns to either Memory, I/O or DMA mode, depending on configuration.

Example of StreamTransfer

Figure 5.7 shows how 4 back-to-back frames, followed by 5 back-to-back frames, would be received without StreamTransfer. Figure 5.8 shows how a the same sequence of frames would be received with StreamTransfer.

Receive DMA Summary

Table 5.9 summarize the Receive DMA configuration options supported by the CS8900.

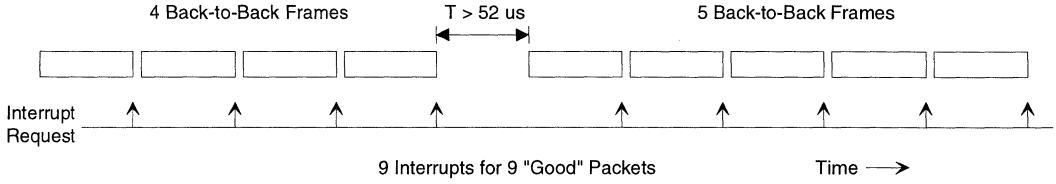


Figure 5.7. Receive Example Without StreamTransfer

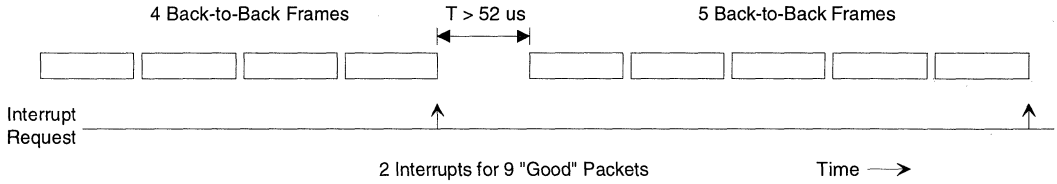


Figure 5.8. Receive Example With StreamTransfer

RxDMAonly (Register 3, RxCFG, Bit 9)	AutoRxDMAiE (Register 3, RxCFG, Bit A)	RxDMAiE (Register B, BufCFG, Bit 7)	RxOKiE (Register 3, RxCFG, Bit 8)	CS8900 Configuration
1	NA	0	NA	Receive DMA used for all receive frames, without interrupts.
1	NA	1	NA	Receive DMA used for all receive frames, with BufEvent interrupts.
0	1	0	0	Auto-Switch DMA used if necessary, without interrupts.
0	1	1	1	Auto-Switch DMA used if necessary, with RxEvent and BufEvent interrupts possible.
0	0	NA	NA	Memory or I/O Mode only.

Table 5.9. Receive DMA Configuration Options

5.5 Transmit Operation

Overview

Packet transmission occurs in two phases. The first phase consists of the host moving the Ethernet frame into the CS8900's buffer memory. It begins with the host issuing a Transmit Command, informing the CS8900 that a frame is to be transmitted and telling it when (i.e. after 5, 381, or 1021 bytes or the full frame has been transferred to the CS8900) and how the frame should be sent (i.e. with or without CRC, with or without pad bits, etc.). The host follows the Transmit Command with the Transmit Length, indicating how much buffer space is required. Once buffer space is available, the host writes the Ethernet frame into the CS8900's internal memory, using either Memory or I/O space.

The second phase of transmission consists of the CS8900 converting the frame into an Ethernet packet, and then transmitting it onto the network. The process starts with the CS8900 transmitting the preamble and Start-of-Frame delimiter as soon as the proper number of bytes has been transferred into its transmit buffer (5, 381, 1021 bytes or full frame, depending on configuration). This is followed by the data transferred into the on-chip buffer by the host (Destination Address, Source Address, Length field and LLC data). If the frame is less than 64 bytes, including CRC, the CS8900 adds pad bits if configured to do so. As a final step, the CS8900 appends the proper 32-bit CRC value.

Transmit Configuration

After each reset, the CS8900 must be configured for transmit operation. This can be done automatically, using an attached EEPROM, or by writing configuration commands to the CS8900's internal registers (see section 3.4). The items that must be configured include: which physical interface to use; and, what transmit events cause interrupts.

Configuring the Physical Interface: Configuring the physical interface consists of determining which Ethernet interface should be active (10BASE-T or AUI), and enabling the transmit logic for serial transmission. This is done via the LineCTL register (Register 13) and is described in table 5.10.

Register 13, LineCTL		
Bit	**Bit Name**	**Operation**
7	SerTxON	When set, transmission enabled.
8	AUIonly	When set, AUI selected (takes precedence over AutoAUI/10BT). When clear, 10BASE-T selected.
9	AutoAUI/ 10BT	When set, automatic interface selection enabled.
B	Mod BackoffE	When set, the modified backoff algorithm is used. When clear, the standard backoff algorithm is used.
D	2-part DefDis	When set, two-part deferral is disabled.

Table 5.10. Physical Interface Configuration

Selecting what Events Cause Interrupts: The TxCFG register (Register 7) and the BufCFG register (Register B) are used to determine what transmit events will cause interrupts to the host processor. Tables 5.11 and 5.12 describe the interrupt enable (iE) bits in these registers.

Register 7, TxCFG		
Bit	**Bit Name**	**Operation**
6	Loss-of-CRSiE	When set, there is an interrupt whenever the CS8900 fails to detect Carrier Sense after transmitting the preamble (applies to the AUI only).
7	SQEerroriE	When set, there is an interrupt whenever there is an SQE error.
8	TxOKiE	When set, there is an interrupt whenever a frame is transmitted successfully.
9	Out-of-windowiE	When set, there is an interrupt whenever a late collision is detected.
A	JabberiE	When set, there is an interrupt whenever there is a jabber condition.
B	AnycolliE	When set, there is an interrupt whenever there is a collision.
F	16colliE	When set, there is an interrupt whenever the CS8900 attempts to transmit a single frame 16 times.

Table 5.11. Transmit Interrupt Configuration

Register B, BufCFG		
Bit	Bit Name	Operation
8	Rdy4TxiE	When set, there is an interrupt whenever buffer space becomes available for a transmit frame (used with a Transmit Request).
9	TxUnder runiE	When set, there is an interrupt when the CS8900 runs out of data after transmit has started.
A	TxCol OvfloiE	When set, there is an interrupt whenever the TxCol counter overflows.

Table 5.12. Transmit Interrupt Configuration

Changing the Configuration

Once the host configures these registers it does not need to change them for subsequent packet transmissions. If the host does choose to change the TxCFG or BufCFG registers, it may do so at any time. The effects of the change would be noticed immediately. That is, any changes in the Interrupt Enables (iE) bits may affect the packet currently being transmitted.

If the host chooses to change bits in the LineCTL register after initialization, the ModBackoffE bit and any receive related bit (LoRxSquelch, SerRxON) may be changed at any time. However, Crystal recommends that the Auto AUI/10BT and AUIonly bits not be changed while the SerTxON bit is set. If any of these three bits are to be changed, the host should first clear the SerTxON bit (Register 13, LineCTL, Bit 7), and then set it once the changes are complete.

Enabling CRC Generation and Padding

Whenever the host issues a Transmit Request command, it must indicate whether or not the Cyclic Redundancy Check (CRC) value should be appended to the transmit frame, and whether or not pad bits should be added (if needed). Table 5.13 describes how to configure the CS8900 for CRC generating and padding.

Register 9, TxCMD		
Inhibit CRC (Bit C)	TxPad Dis (Bit D)	Operation
0	0	Pad to 64 bytes if necessary (including CRC).
1	0	Send a runt frame if specified length less than 60 bytes.
0	1	Pad to 60 bytes if necessary (without CRC).
1	1	Send runt if specified length less than 64. The CS8900 will not transmit a frame that is less than 3 bytes.

Table 5.13. CRC and Padding Configuration

Individual Packet Transmission

Whenever the host has a packet to transmit, it must issue a Transmit Request to the CS8900 which consists of the following three operation (in the exact order shown):

1. The host must write a Transmit Command to the TxCMD register (PacketPage base + 0144h). The contents of the TxCMD register may be read back from the TxCMD register (Register 9).

2. The host must write the frames length to the TxLength register (PacketPage base + 0146h).

3. The host must read the BusST register (Register 18)

The information written to the TxCMD register tells the CS8900 how to transmit the next frame. The bits that must be programmed in the TxCMD register are described in table 5.14.

Register 9, TxCMD			
Bit		Bit Name	Operation
6	7	Tx Start	
clear	clear		Start preamble after 5 bytes have been transferred to the CS8900.
clear	set		Start preamble after 381 bytes have been transferred to the CS8900.
set	clear		Start preamble after 1021 bytes have been transferred to the CS8900.
set	set		Start preamble after entire frame has been transferred to the CS8900.
8		Force	When set, the CS8900 discards any frame data currently in the transmit buffer.
9		Onecoll	When set, the CS8900 will not attempt to re-transmit any packet after a collision.
C		InhibitCRC	When set, the CS8900 does not append the 32-bit CRC value to the end of any transmit packet.
D		TxPadDis	When set, the CS8900 will not add pad bits to short frames.

Table 5.14. Tx Command Configuration

For each individual packet transmission, the host must issue a *complete* Transmit Request. Furthermore, the host must write to the TxCMD register before each packet transmission, even if the contents of the TxCMD register do not change. The Transmit Request described above may be in either Memory Space or I/O Space, as follows:

Memory Mode Transmit: Memory Mode transmit operations occur in the following order (using interrupts):

1. The host bids for storage of the frame by writing the Transmit Command to the TxCMD register (memory base + 0144h)

2. The host writes the transmit frame length to the TxLength register (memory base + 0146h). If the transmit length is erroneous, the command is discarded and the TxBidErr bit (Register 10, BusST, Bit 7) is set.

3. The host reads the BusST register (Register 18, memory base + 0138h). If the Rdy4TxNOW bit (Bit 8) is set, the frame can be written. If clear, the host must wait for CS8900 buffer memory to become available. If Rdy4TxiE (Register B, BufCFG, Bit 8) is set, the host will be interrupted when Rdy4Tx (Register C, BufEvent, Bit 8) becomes set.

Once the CS8900 is ready to accept the frame, the host executes repetitive memory-to-memory move instructions (REP MOVS) to memory base + 0A00h to transfer the entire frame from host memory to CS8900 memory.

I/O Mode Transmit: I/O Mode transmit operations occur in the following order (using interrupts):

1. The host bids for storage of the frame by writing the Transmit Command to the TxCMD Port (I/O base + 0004h)

2. The host writes the transmit frame length to the TxLength Port (I/O base + 0006h).

3. The host reads the BusST register (Register 18) to see if the Rdy4TxNOW bit (Bit 8) is set. To read the BusST register, the host must first set the PacketPage Pointer at the correct location by writing 0138h to the PacketPage Pointer Port (I/O base + 000Ah). It can then read the BusST register from the PacketPage Data Port (I/O base + 000Ch). If Rdy4TxNOW is set, the frame can be written. If clear, the host must wait for CS8900 buffer memory to become available. If Rdy4TxiE (Register B, BufCFG, Bit 8) is set, the host will be interrupted when Rdy4Tx (Register C, BufEvent, Bit 8) becomes set. If the TxBidErr bit (Register 18, BusST, Bit 7) is set, the transmit length is not valid.

4. Once the CS8900 is ready to accept the frame, the host executes repetitive write instructions

(REP OUT) to the Receive/Transmit Data Port (I/O base + 0000h) to transfer the entire frame from host memory to CS8900 memory.

Starting and Continuing Packet Transmission

Once the CS8900 successfully completes transmitting a frame, it sets the TxOK bit (Register 8, TxEvent, Bit 8). If the TxOKiE bit (Register 7, TxCFG, bit 8) is set, the CS8900 generates a corresponding interrupt.

Rdy4TxNOW vs. Rdy4Tx

The Rdy4TxNOW bit (Register 18, BusST, bit 8) is used to tell the host that the CS8900 is ready to accept a frame for transmission. It is used during the Transmit Request process or after the Transmit Request process to signal the host that space has become available when interrupts are not being used (i.e. the Rdy4TxiE bit (Register B, BufCFG, Bit 8) is not set). On the other hand, the Rdy4Tx bit is used with interrupts and requires the Rdy4TxiE bit be set.

Figure 5.10 provides a diagram of error free transmission without collision.

Committing Buffer Space to a Transmit Frame

When the host issues a transmit request, the CS8900 checks the length of the transmit frame is see if there is sufficient on-chip buffer space. If there is, it sets the Rdy4TxNOW bit. If not, and the Rdy4TxiE bit is set, it waits for buffer space to free up and then sets the Rdy4Tx bit. If Rdy4TxiE is not set, the CS8900 will set the Rdy4TxNOW bit when space becomes available.

Eventhough transmit buffer space may be available, the CS8900 does not commit buffer space to a transmit frame until all of the following are true:

1. The host must issues a Transmit Request;

2. The Transmit Request must be successful; and,

3. Either the host reads that the Rdy4TxNOW bit (Register 18, BusST, Bit 8) is set, or the host reads that the Rdy4Tx bit (Register C, BufEvent, bit 8) is set.

If the CS8900 has committed buffer space to a particular transmit frame, it will not allow subsequent frames to be writen to that buffer space as long as the transmit frame is committed.

After buffer space has been committ, the frame is subsequently transmitted unless any of the following occur:

1. The host completely writes the frame data, but transmission failed on the Ethernet line. There are three such failures, and these are indicated by three transmit error bits in the TxEvent register (Register 8): 16coll, Jabber, or Out-of-Window.

Or:

2. The host aborts the transmission by setting the Force (Register 9, TxCMD, bit 8) bit. In this case, the committed transmit frame, as well as any yet-to-be-transmitted frames queued in the on-chip memory are cleared and not transmitted. The host should make TxLength = 0 when using the Force bit.

Or:

3. There is a transmit under-run, and bit TxUnderrun bit (Register C, BufEvent, Bit 9) is set.

Successful transmission is indicated when the TxOK bit (Register 8, TxEvent, Bit 8) is set.

Transmit Frame Length

The length of the frame transmitted is determined by the value written into the TxLength register (PacketPage base + 0146h) during the Transmit Request. The length of the transmit frame may be modified by the configuration of the TxPadDis bit (Register 9, TxCMD, Bit D) and the InhibitCRC bit (Register 9, TxCMD, Bit C). Table 5.15 defines how these bids affect the length of the transmit frame. In addition, it show what frames the CS8900 will send.

Register 9, TxCMD		Host specified transmit length at 0146h (in bytes)			
TxPadDis (Bit D)	InhibitCRC (Bit C)	3 < TxLength < 60	60 > TxLength < 1514	1514 > TxLength < 1518	TxLength > 1518
0	0	Pad to 60 and add CRC	Send frame and add CRC [Normal Mode]	Will not send	Will not send
0	1	Pad to 60 and send without CRC	Send frame without CRC	Send frame without CRC	Will not send
1	0	Send without pads, and add CRC	Send frame and add CRC	Will not send	Will not send
1	1	Send without pads and without CRC	Send frame without CRC	Send frame without CRC	Will not send

Table 5.15. Transmit Frame Length

Notes: 1. If the TxPadDis bit is clear and InhibitCRC is set and the CS8900 is commanded to send a frame of length less than 60 bytes, the CS8900 pads.

2. The CS8900 will not send a frame with TxLength less than 3 bytes.

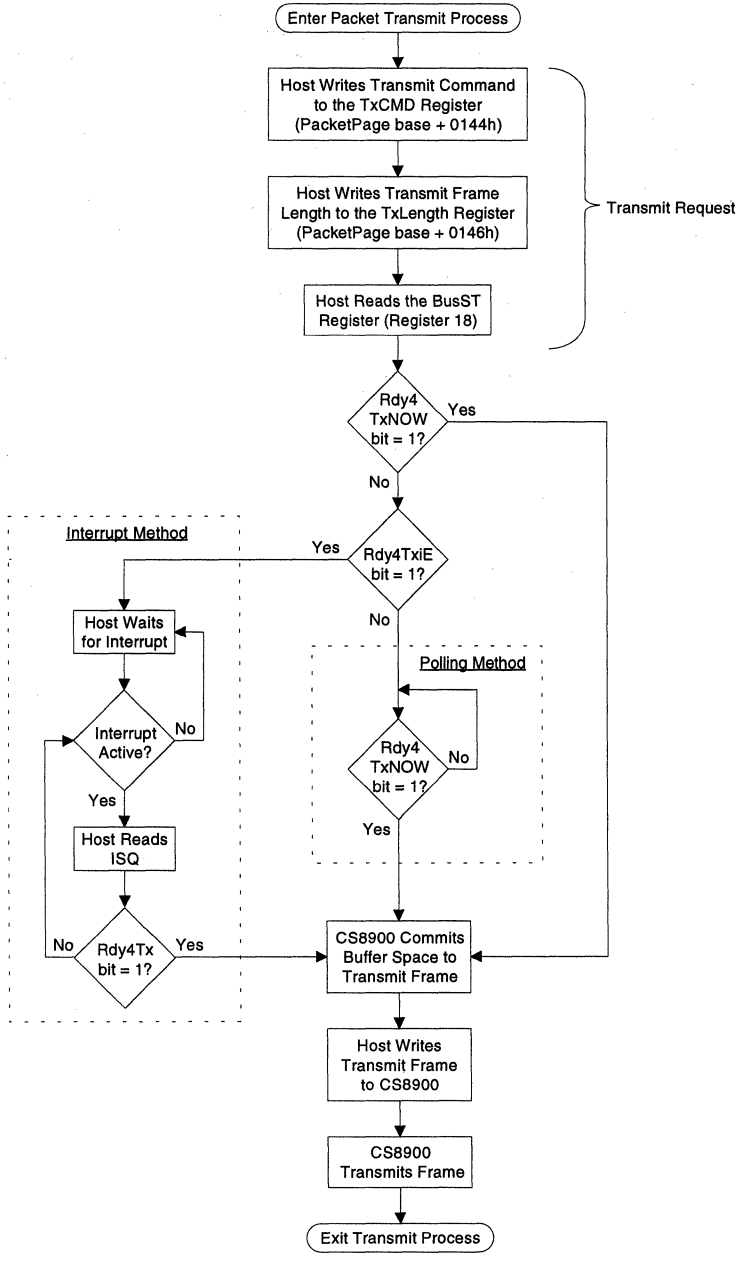


Figure 5.9. Transmit Operation

6.0 TEST MODES

6.1 Loopback & Collision Diagnostic Tests

Internal and external Loopback and Collision tests can be used to verify the CS8900's functionality when configured for either 10BASE-T or AUI operation.

Internal Tests

Internal tests allow the major digital functions to be tested, independent of the analog functions. During these tests, the Manchester encoder is connected to the decoder. All digital circuits are operational, and the transmitter and receiver are disabled.

External Tests

External test modes allow the complete chip to be tested without connecting it directly to an Ethernet network.

Loopback Tests

During Loopback tests, the internal Carrier Sense (CRS) signal, used to detect collisions, is ignored, allowing packet reception during packet transmission.

10BASE-T Loopback and Collision Tests

10BASE-T Loopback and Collision Tests are controlled by two bits in the Test Control register: FDX (Register 19, TxCTL, Bit E) and ENDECloop (Register 19, TxCTL, Bit 9). Table 6.1 describes these tests.

AUI Loopback and Collision Tests

AUI Loopback and Collision tests are controlled by two bits in the Test Control register: AUIloop (Register 19, TxCTL, Bit A) and ENDECloop (Register 19, TxCTL, Bit 9). Table 6.2 describes these tests.

Test Mode	FDX	ENDECloop	Description of Test
10BASE-T Internal Loopback	1	1	Transmit a frame and verify that the frame is received without error.
10BASE-T Internal Collision	0	1	Transmit frames and verify that collisions are detected and that internal counters function properly. After 16 collisions, verify that 16coll (Register 8, TxEvent, Bit F) is set.
10BASE-T External Loopback	1	0	Connect TXD+ to RXD+ and TXD- to RXD-. Transmit a frame and verify that the frame is received without error.
10BASE-T External Collision	0	0	Connect TXD+ to RXD+ and TXD- to RXD-. Transmit frames and verify that collisions are detected and that internal counters function properly. After 16 collisions, verify that 16coll (Register 8, TxEvent, Bit F) is set.

Table 6.1. 10BASE-T Loopback and Collision Tests

Test Mode	AUIloop	ENDECloop	Description of Test
AUI Internal Loopback	1	1	Transmit a frame and verify that the frame is received without error.
AUI External Loopback	1	0	Connect DO+ to DI+ and D0- to DI-. Transmit a frame and verify that the frame is received without error (since there is no collision signal, an SQE error will occur).
AUI Collision	0	0	Start transmission and observe DO+/DO- activity. Input a 10 MHz sine wave to CI+/CI- pins and observe collisions.

Table 6.2. AUI Loopback and Collision Tests

6.2 Boundary Scan

Boundary Scan test mode provides an easy and efficient board-level test for verifying that the CS8900 has been installed properly. Boundary Scan will check to see if the orientation of the chip is correct, and if there are any open or short circuits.

Boundary Scan is controlled by the $\overline{\text{TESTSEL}}$ pin. When $\overline{\text{TESTSEL}}$ is high, the CS8900 is configured for normal operation. When $\overline{\text{TESTSEL}}$ is low, the following occurs:

- the CS8900 enters Boundary Scan test mode and stays in this mode as long as $\overline{\text{TESTSEL}}$ is low;
- the CS8900 goes through an internal reset and remains in internal reset as long as $\overline{\text{TESTSEL}}$ is low;
- the AEN pin, normally the ISA bus Address Enable, is redefined to become the Boundary Scan shift clock input; and
- all digital outputs and bi-directional pins are placed in a high-impedance state (this electrically isolates the CS8900 digital outputs from the rest of the circuit board).

For Boundary Scan to be enabled, AEN must be low before $\overline{\text{TESTSEL}}$ is driven low.

A complete Boundary Scan test is made up of two separate cycles. The first cycle, known as the Output Cycle, tests all digital output pins and all bi-directional pins. The second cycle, known as the Input Cycle, tests all digital input pins and all bi-directional pins.

Output Cycle

During the Output Cycle, the falling edge of AEN causes each of the 17 digital output pins and each of the 17 bi-directional pins to be driven low, one at a time. The cycle begins with $\overline{\text{LINKLED}}$ and advances in order counterclockwise around the chip though all 34 pins. This test is referred to as a "walking 0" test.

The following is a list of output pins and bi-directional pins that are tested during the Output Cycle:

Pin Name	Pin #	Pin Name	Pin #
$\overline{\text{ELCS}}$	2	INTRQ1	31
EECS	3	INTRQ0	32
EESK	4	$\overline{\text{IOCS16}}$	33
EEDataOut	5	$\overline{\text{MEMCS16}}$	34
DMARQ2	12	INTRQ3	35
DMARQ1	13	IOCHRDY	64
DMARQ0	16	SD0 - SD7	65-68,71-74
$\overline{\text{CSOUT}}$	17	$\overline{\text{BSTATUS}}$	78
SD15-SD08	18-21,24-27	$\overline{\text{LINKLED}}$	99
INTRQ2	30	$\overline{\text{LANLED}}$	100

The output pins not included in this test are:

Pin Name	Pin #	Pin Name	Pin #
DO+	83	TXD-	88
DO-	84	RES	93
TXD+	87	XTAL2	98

Input Cycle

During the Input Cycle, the falling edge of AEN causes the state of each selected pin to be transferred to EEDataOut (that is, EEDataOut will be high or low depending on the input level of the selected pin). This cycle begins with HWSLEEP and advances clockwise through each of 33 input pins (all digital input pins except for AEN) and each of the 17 bi-directional pins, one pin at a time.

The following is a list of input pins and bi-directional pins that are tested during the Input Cycle:

Pin Name	Pin #	Pin Name	Pin #
ELCS	2	SBHE	36
EEDataIn	6	SA0 - SA11	37-48
CHIPSEL	7	REFRESH	49
DMACK2	12	SA12- SA19	50-54,58-60
DMACK1	14	IOR	61
DMACK0	16	IOW	62
SD08-SD15	18-21,24-27	SD0 - SD7	65-68,71-74
MEMW	28	RESET	75
MEMR	29	HWSLEEP	77

The input pins not included in this test are:

Pin Name	Pin #	Pin Name	Pin #
AEN	63	CI-	82
TESTSEL	76	RXD+	91
DI+	79	RXD-	92
DI-	80	XTAL1	97
CI+	81		

After the Input Cycle is complete, one more cycle of AEN returns all digital output pins and bi-directional pins to a high-impedance state.

Continuity Cycle

The combination of a complete Output Cycle, a complete Input Cycle, and an additional AEN cycle is called a Continuity Cycle. Each Continuity Cycle lasts for 85 AEN clock cycles. The first Continuity Cycle can be followed by additional Continuity Cycles by keeping TESTSEL low and continuing to cycle AEN. When TESTSEL is driven high, the CS8900 exits Boundary Scan mode and AEN is again used as the ISA-bus Address Enable.

Figure 6.1 shows a complete Boundary Scan Continuity Cycle.

Figure 6.2 shows Boundary Scan timing.

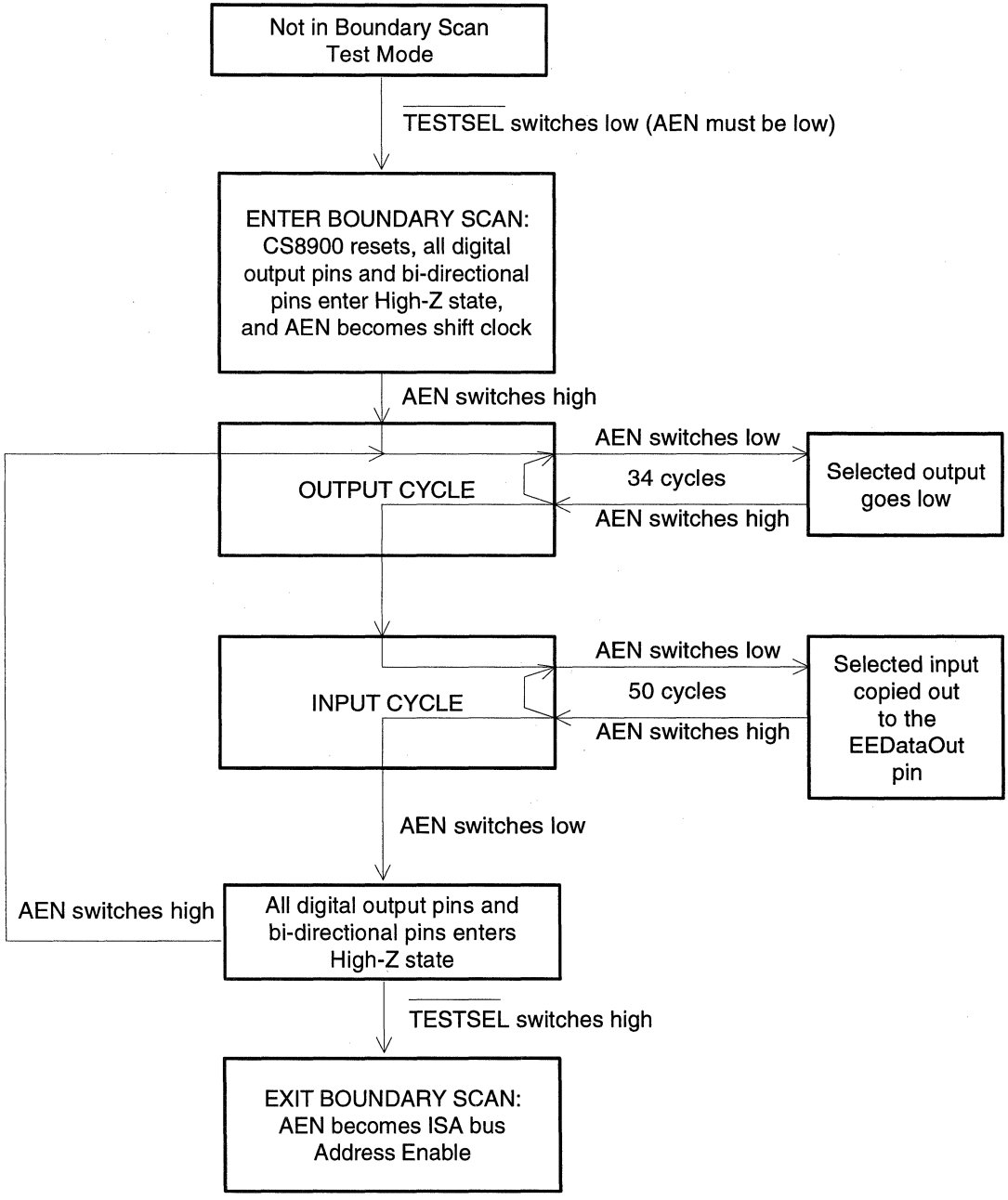


Figure 6.1. Boundary Scan Continuity Cycle

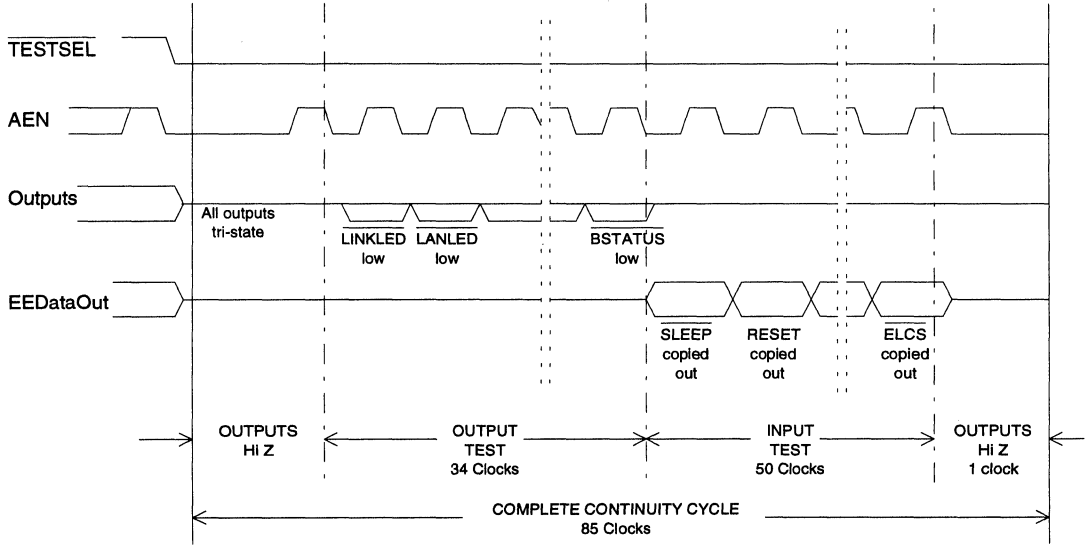


Figure 6.2. Boundary Scan Timing

7.0 ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Units
Power Supply:	Digital	$_DV_{DD}$	-0.3	6.0	V
	Analog	$_AV_{DD}$	-0.3	6.0	V
Input Current	(Except Supply Pins)			±10.0	mA
Analog Input Voltage			-0.3	$(_AV_{DD+})$ +0.3	V
Digital Input Voltage			-0.3	$(_DV_{DD+})$ +0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8.0 RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Units
Power Supply:	Digital	$_DV_{DD}$	4.75	5.25	V
	Analog	$_AV_{DD}$	4.75	5.25	V
Operating Ambient Temperature		T_A	0	+70	°C

9.0 DC CHARACTERISTICS

Over Recommended Operating Conditions

9.1 CRYSTAL (when using external clock)

Parameter	Symbol	Min	Max	Units
XTAL1 Input Low Voltage	V_{IXH}	-0.5	0.8	V
XTAL1 Input High Voltage	V_{IXH}	3.5	$_DV_{DD+}$ 0.5	V
XTAL1 Input Low Current	I_{IXL}	-40	-20	µA
XTAL1 Input High Current	I_{IXH}	20	40	µA

9.2 POWER SUPPLY

Parameter	Symbol	Min	Max	Units
Power Supply Current while Active	I_{DD}		120	mA
Hardware Standby Mode Current	$I_{DDSTNDBY}$			mA
Hardware Suspend Mode Current	$I_{DDHWSUS}$			µA
Software Suspend Mode Current	$I_{DDSWSUS}$			mA

9.0 DC CHARACTERISTICS (continued.)

Over Recommended Operating Conditions

9.3 DIGITAL INPUTS and OUTPUTS						
I/O Type	**Parameter**	**Symbol**	**Conditions and Comments**	**Min**	**Max**	**Units**
OD24	Output Low Voltage	V_{OL}	I_{OL} = 24 mA		0.4	V
OD24	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-10	10	µA
OD10	Output Low Voltage	V_{OL}	I_{OL} = 10 mA		0.4	V
OD10	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-10	10	µA
B24	Output Low Voltage	V_{OL}	I_{OL} = 24 mA		0.4	V
B24	Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4		V
B24	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-10	10	µA
B4	Output Low Voltage	V_{OL}	I_{OL} = 4 mA		0.4	V
B4	Output High Voltage	V_{OH}	I_{OH} = -2 mA	2.4		V
B4	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-10	10	µA
B4w	Output Low Voltage	V_{OL}	I_{OL} = 4 mA		0.4	V
B4w	Output High Voltage	V_{OH}	IOH = -2 mA	2.4		V
B4w	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-20	10	µA
O24ts	Output Low Voltage	V_{OL}	I_{OL} = 24 mA		0.4	V
O24ts	Output High Voltage	V_{OH}	I_{OH} = -2 mA	2.4		V
O24ts	Output Leakage Current	I_{LL}	$0 \le V_{OUT} \le V_{CC}$	-10	10	µA
O4	Output Low Voltage	V_{OL}	I_{OL} = 4 mA		0.4	V
O4	Output High Voltage	V_{OH}	I_{OH} = -2 mA	2.4		V
I	Input Low Voltage	V_{IL}			0.8	V
I	Input High Voltage	V_{IH}		2.4		V
I	Input Leakage Current	I_L	$0 \le V_{IN} \le V_{CC}$	-10	10	µA
Iw	Input Low Voltage	V_{IL}			0.8	V
Iw	Input High Voltage	V_{IH}		2.4		V
Iw	Input Leakage Current	I_L	$0 \le V_{IN} \le V_{CC}$	-20	10	µA

Pin Types:

d	=	Differential Input Pair	I	=	Input	G	= Ground
dO	=	Differential Output Pair	O	=	Output	ts	= Tri-State
B	=	Bi-Directional with Tri-State Output	P	=	Power	w	= Internal Weak Pullup
OD	=	Open Drain Output					

Digital outputs are followed by drive in mA (Example: OD24 = Open Drain Output with 24 mA drive).

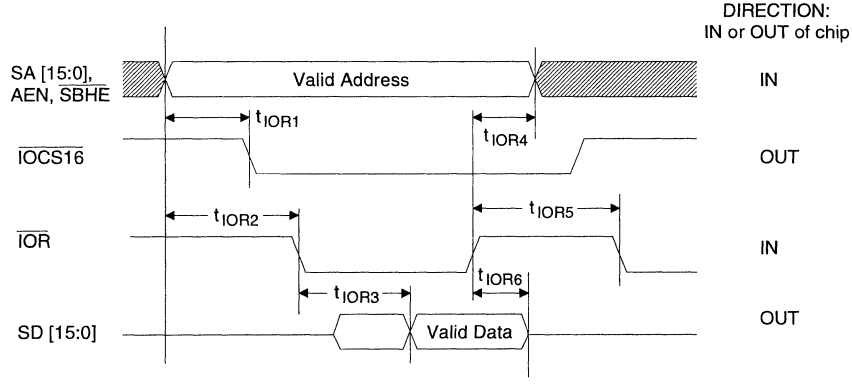
9.0 DC CHARACTERISTICS (continued)

Over Recommended Operating Conditions

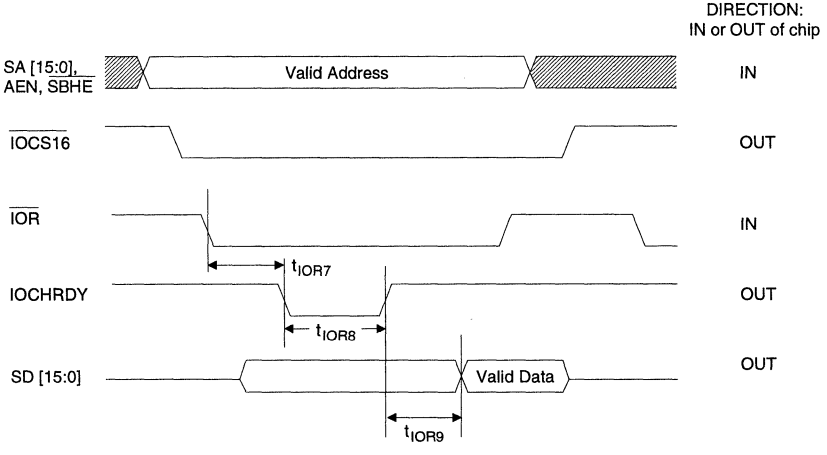
9.4 10BASE-T INTERFACE					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**
Transmitter Differential Output Voltage (Peak)	V_{OD}	2.2		2.8	V
Receiver Normal Squelch Level (Peak)	V_{ISQ}	300		525	mV
Receiver Low Squelch Level (LoRxSquelch bit set)	V_{SQL}	125		290	mV
9.5 AUI INTERFACE					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**
Transmitter Differential Output Voltage (DO+/DO- Peak)	V_{AOD}	±0.45		±1.2	V
Transmitter Undershoot Voltage	V_{AODU}			100	mV
Transmitter Output Short Circuit Current (V_{DD} or V_{SS})	I_{AOSC}			±150	mA
Transmitter Differential Idle Voltage (DO+/DO- Peak)	V_{IDLE}			40	mV
Receiver Squelch Level (DI+/DI- Peak)	V_{AISQ}	180		300	mV
Receiver Common Mode Voltage	V_{AICM}				V

10.0 SWITCHING CHARACTERISTICS

16-BIT I/O READ, IOCHRDY NOT USED				
Parameter	**Symbol**	**Min**	**Max**	**Units**
Address, AEN, $\overline{SBHE}$ active to $\overline{IOCS16}$ low	t_{IOR1}		35	ns
Address, AEN, $\overline{SBHE}$ active to $\overline{IOR}$ active	t_{IOR2}	20		ns
$\overline{IOR}$ low to SD valid	t_{IOR3}		135	ns
Address, AEN, $\overline{SBHE}$ hold after $\overline{IOR}$ inactive	t_{IOR4}	30		ns
$\overline{IOR}$ inactive to active	t_{IOR5}	60		ns
$\overline{IOR}$ inactive to SD 3-state	t_{IOR6}		30	ns

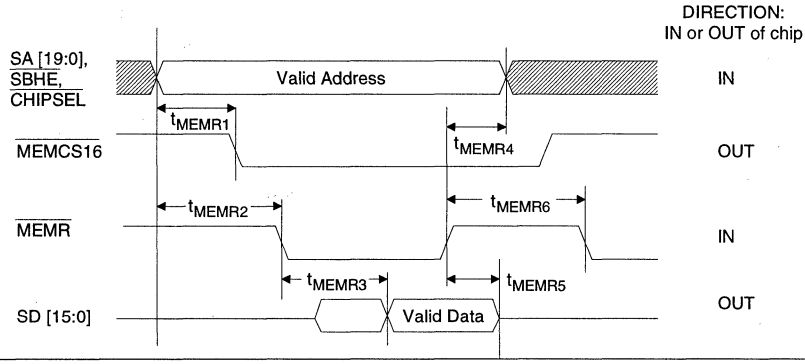


16-BIT I/O READ, WITH IOCHRDY				
Parameter	**Symbol**	**Min**	**Max**	**Units**
$\overline{IOR}$ active to IOCHRDY inactive	t_{IOR7}		25	ns
IOCHRDY low pulse width	t_{IOR8}	125	175	ns
IOCHRDY active to SD valid	t_{IOR9}		0	ns

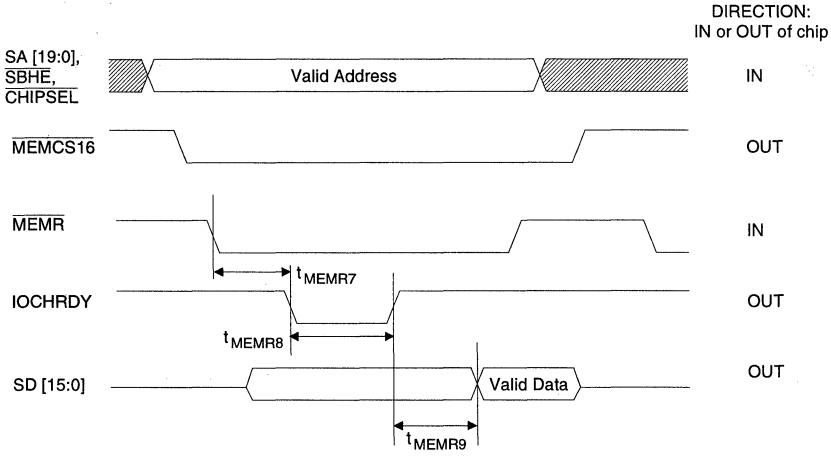


10.0 SWITCHING CHARACTERISTICS (continued)

16-BIT MEMORY READ, IOCHRDY NOT USED				
Parameter	**Symbol**	**Min**	**Max**	**Units**
SA [19:0], $\overline{SBHE}$, $\overline{CHIPSEL}$, active to $\overline{MEMCS16}$ low	t_{MEMR1}		30	ns
Address, $\overline{SBHE}$, $\overline{CHIPSEL}$ active to $\overline{MEMR}$ active	t_{MEMR2}	20		ns
$\overline{MEMR}$ low to SD valid	t_{MEMR3}		160	ns
Address, $\overline{SBHE}$, $\overline{CHIPSEL}$ hold after $\overline{MEMR}$ inactive	t_{MEMR4}	20		ns
$\overline{MEMR}$ inactive to SD 3-state	t_{MEMR5}		30	ns
$\overline{MEMR}$ inactive to active	t_{MEMR6}	60		ns



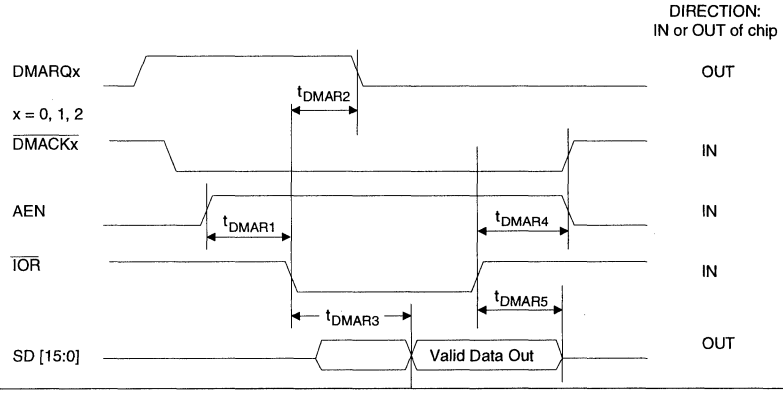
16-BIT MEMORY READ, WITH IOCHRDY				
Parameter	**Symbol**	**Min**	**Max**	**Units**
$\overline{MEMR}$ low to IOCHRDY inactive	t_{MEMR7}		35	ns
IOCHRDY low pulse width	t_{MEMR8}	125	175	ns
IOCHRDY active to SD valid	t_{MEMR9}		0	ns



10.0 SWITCHING CHARACTERISICS (continued)

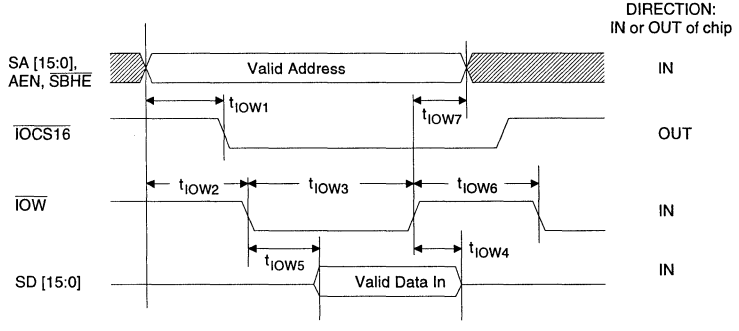
DMA READ

Parameter	Symbol	Min	Max	Units
AEN active to $\overline{IOR}$ low	t_{DMAR1}	20		ns
$\overline{IOR}$ low to DMARQx inactive	t_{DMAR2}		50	ns
$\overline{IOR}$ low to SD valid	t_{DMAR3}		135	ns
$\overline{DMACKx}$, AEN hold after $\overline{IOR}$ high	t_{DMAR4}	20		ns
$\overline{IOR}$ inactive to SD 3-state	t_{DMAR5}		30	ns



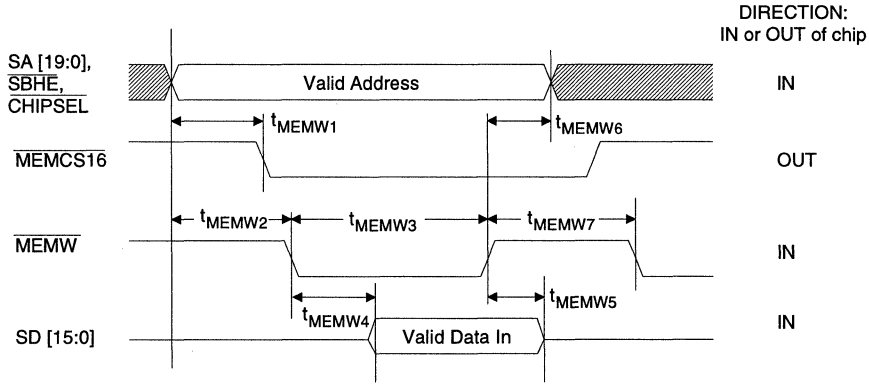
16-BIT I/O WRITE

Parameter	Symbol	Min	Max	Units
Address, AEN, $\overline{SBHE}$ valid to $\overline{IOCS16}$ low	t_{IOW1}		35	ns
Address, AEN, $\overline{SBHE}$ valid to $\overline{IOW}$ low	t_{IOW2}	25		ns
$\overline{IOW}$ pulse width	t_{IOW3}	110		ns
SD hold after $\overline{IOW}$ high	t_{IOW4}	10		ns
$\overline{IOW}$ low to SD valid	t_{IOW5}		10	ns
$\overline{IOW}$ inactive to active	t_{IOW6}	50		ns
Address hold after $\overline{IOW}$ high	t_{IOW7}	10		ns

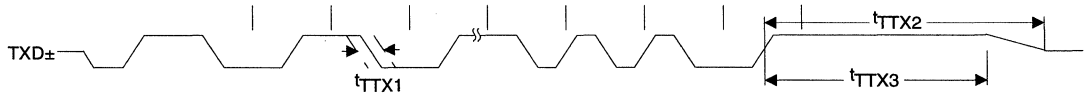


10.0 SWITCHING CHARACTERISTICS (continued)

16-BIT MEMORY WRITE				
Parameter	**Symbol**	**Min**	**Max**	**Units**
Address, $\overline{SBHE}$, $\overline{CHIPSEL}$ valid to $\overline{MEMCS16}$ low	t_{MEMW1}		30	ns
Address, $\overline{SBHE}$, $\overline{CHIPSEL}$ valid to $\overline{MEMW}$ low	t_{MEMW2}	20		ns
$\overline{MEMW}$ pulse width	t_{MEMW3}	125		ns
$\overline{MEMW}$ low to SD valid	t_{MEMW4}		40	ns
SD hold after $\overline{MEMW}$ high	t_{MEMW5}	10		ns
Address hold after $\overline{IOW}$ high	t_{MEMW6}	10		ns
$\overline{MEMW}$ inactive to active	t_{MEMW7}	50		ns

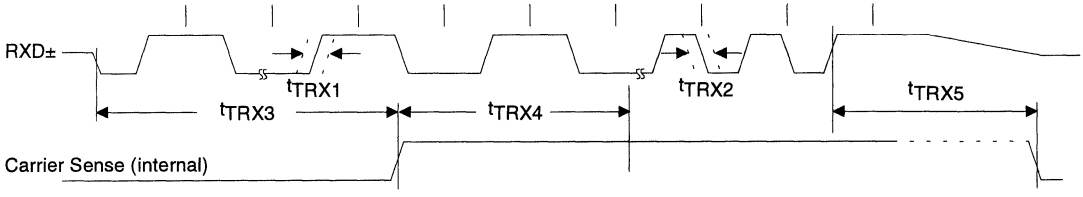


10BASE-T TRANSMIT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
TXD Pair Jitter into 100 Ohm Load	t_{TTX1}			8	ns
TXD Pair Return to ≤ 50 mV after Last Positive Transition	t_{TTX2}			4.5	µs
TXD Pair Positive Hold Time at End of Packet	t_{TTX3}	250			ns



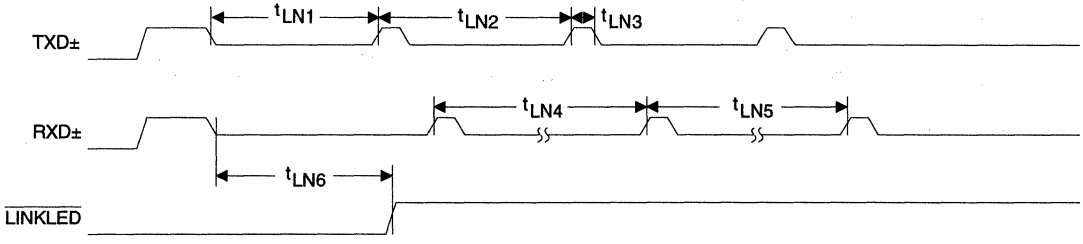
10.0 SWITCHING CHARACTERISTICS (continued)

10BASE-T RECEIVE					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Allowable Received Jitter at Bit Cell Center	t_{TRX1}			±13.5	ns
Allowable Received Jitter at Bit Cell Boundry	t_{TRX2}			±13.5	ns
Carrier Sense Assertion Delay	t_{TRX3}	300		600	ns
Invalid Preamble Bits after Assertion of Carrier Sense	t_{TRX4}	1		2	bits
Carrier Sense Deassertion Delay	t_{TRX5}	175		230	ns

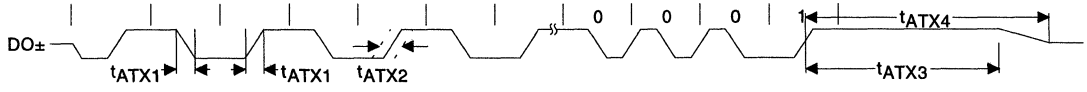


10.0 SWITHING CHARACTERISTICS (continued)

10BASE-T LINK INTEGRITY					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
First Transmitted Link Pulse after Last Transmitted Packet	t_{LN1}	8	16	24	ms
Time Between Transmitted Link Pulses	t_{LN2}	8	16	24	ms
Width of Transmitted Link Pulses	t_{LN3}	60	100	200	ns
Minimum Received Link Pulse Separation	t_{LN4}	2		7	ms
Maximum Received Link Pulse Separation	t_{LN5}	25		150	ms
Last Receive Activity to Link Fail (Link Loss Timer)	t_{LN6}	50		150	ms

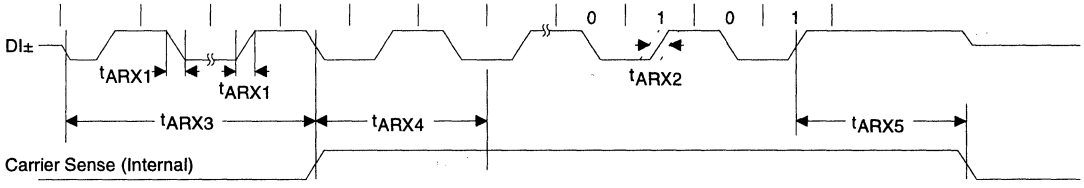


AUI TRANSMIT					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
DO Pair Rise and Fall Times	t_{ATX1}			5	ns
DO Pair Jitter at Bit Cell Center	t_{ATX2}			0.5	ns
DO Pair Positive Hold Time at Start of Idle	t_{ATX3}	200			ns
DO Pair Return to ≤ 40 mVp after Last Positive Transition	t_{ATX4}			8.0	µs

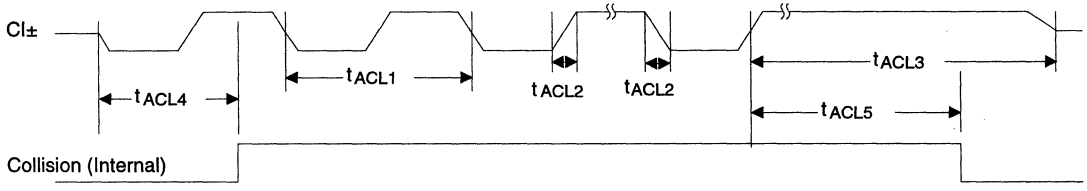


10.0 SWITCHING CHARACTERISTICS (continued)

AUI RECEIVE					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
DI Pair Rise and Fall Time	t_{ARX1}			10	ns
Allowable Bit Cell Center and Boundary Jitter in Data	t_{ARX2}			±18	ns
Carrier Sense Assertion Delay	t_{ARX3}	15		40	ns
Invalid Preamble Bits after Carrier Sense Asserts	t_{ARX4}	1		2	bits
Carrier Sense Deassertion Delay	t_{ARX5}	130	150	160	ns

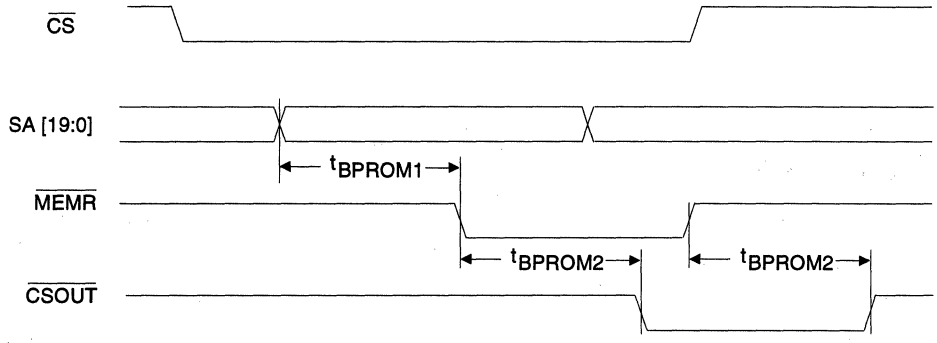


AUI COLLISION					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
CI Pair Cycle Time	t_{ACL1}	85	100	115	ns
CI Pair Rise and Fall Times	t_{ACL2}			10	ns
CI Pair Return to Zero from Last Positive Transition	t_{ACL3}	160			ns
Collision Assertion Delay	t_{ACL4}	10		30	ns
Collision Deassertion Delay	t_{ACL5}	215	225	235	ns

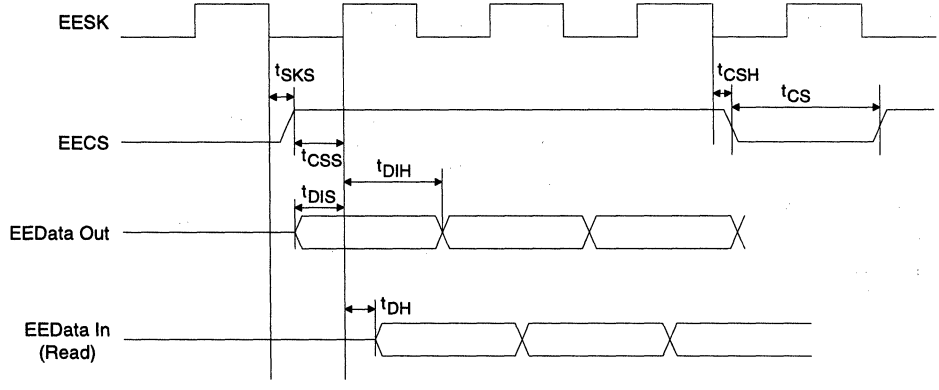


10.0 SWITCHING CHARACTERISTICS (continued)

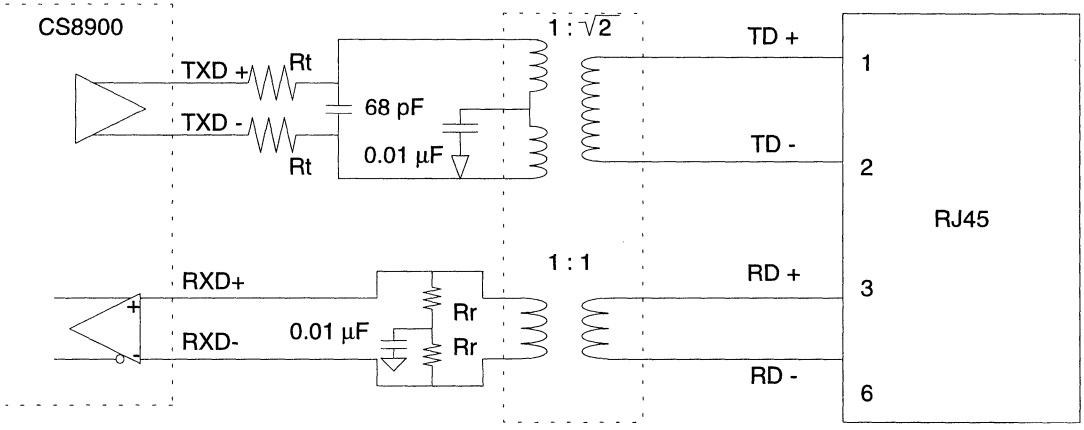
External Boot PROM Access					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Address active to $\overline{MEMR}$	t_{BPROM1}	20			ns
$\overline{MEMR}$ active to $\overline{CSOUT}$ low	t_{BPROM2}			35	ns
$\overline{MEMR}$ inactive to $\overline{CSOUT}$ high	t_{BPROM3}			40	ns



EEPROM					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
EESK Setup time relative to EECS	t_{SKS}	100	-	-	ns
EECS/ELCS_b Setup time wrt ↑ EESK	t_{CSS}	250	-	-	ns
EEDataOut Setup time wrt ↑ EESK	t_{DIS}	250	-	-	ns
EEDataOut Hold time wrt ↑ EESK	t_{DIH}	500	-	-	ns
EEDataIn Hold time wrt ↑ EESK	t_{DH}	10	-	-	ns
EECS Hold time wrt ↓ EESK	t_{CSH}	100	-	-	ns
Min EECS Low time during programming	t_{CS}	1000	-	-	ns



11.0 10BASE-T Wiring



NOTES:

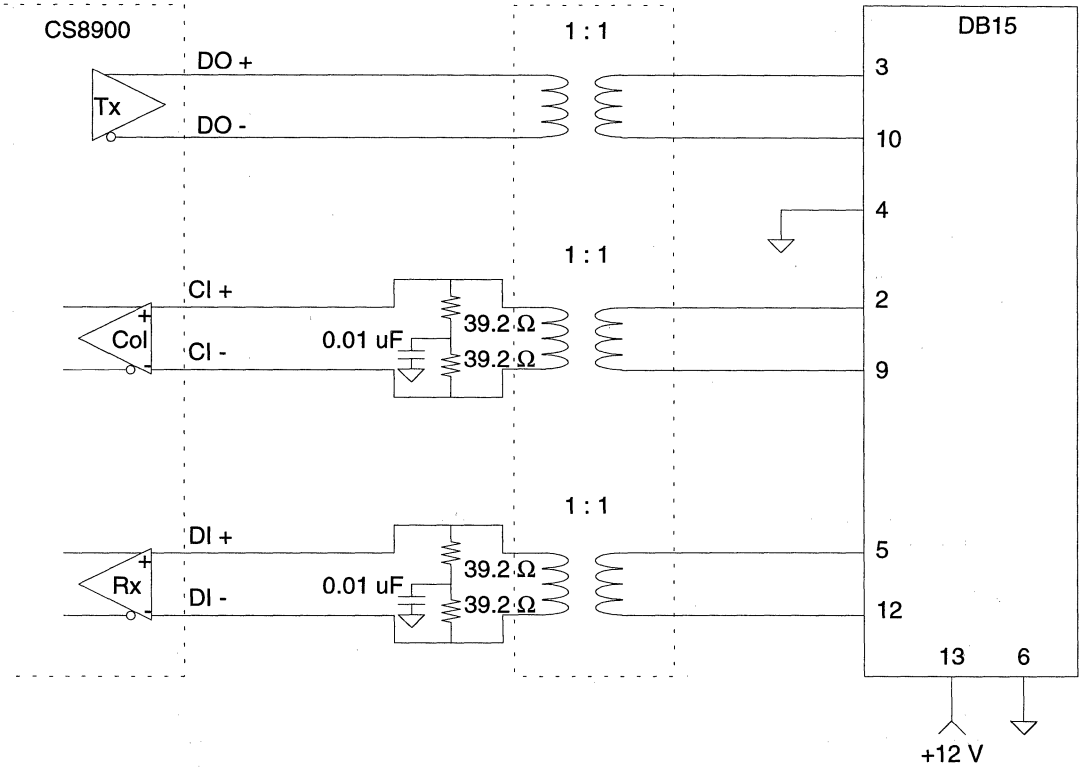
1. If a center tap transformer is used on the RXD+ and RXD- inputs, replace the pair of Rr resistors with a single 2xRr resistor.

2. The Rt and Rr resistors are +/- 1% tolerance.

3. The CS8900 supports 100, 120, and 150Ω unshielded twisted pair cables. The proper values of Rt and Rr, for a given cable impedance, are shown below:

Cable Impedance (Ω)	Rt (Ω)	Rr (Ω)
100	24.9	49.9
120	30.1	60.4
150	37.4	75

12.0 AUI Wiring

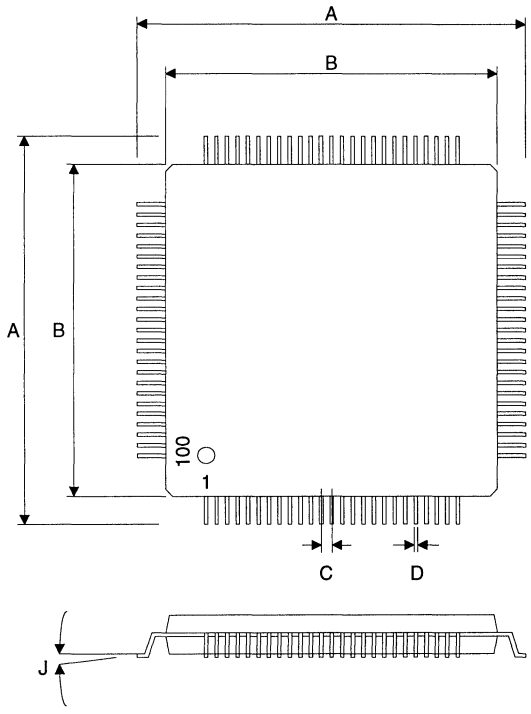


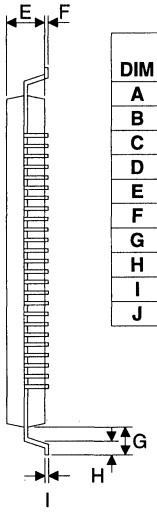
13.0 Crystal Oscillator Requirements

If a 20 MHz crystal oscillator is used, it must meet the following specifications:

Parameter	min	typ	max	unit
Parallel Resonant Frequency		20		MHz
Resonant Frequency Error (CL = 18 pF)	-50		+50	ppm
Resonant Frequency Change Over Operating Temperature	-40		+40	ppm
Crystal Capacitance			18	pF
Motional Crystal Capacitance		0.022		pF
Series Resistance			35	Ω
Shunt Capacitance			7	pF

14.0 PHYSICAL DIMENSIONS





100-pin TQFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

15.0 Glossary of Terms

Acronyms

AUI	Attachment Unit Interface
CRC	Cyclic Redundancy Check
CS	Carrier Sense
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DA	Destination Address
EEPROM	Electrically Erasable Programmable Read Only Memory
EOF	End-of-Frame
FCS	Frame Check Sequence
FDX	Full Duplex
IA	Individual Address
IPG	Inter-Packet Gap
ISA	Industry Standard Architecture
LA	ISA Latchable Address Bus (LA17 - LA23)
LLC	Logical Link Control
MAC	Media Access Control
MAU	Medium Attachment Unit
MIB	Management Information Base
RX	Receive
SA	Source Address *or* ISA System Address Bus (SA0 - SA19)
SFD	Start-of-Frame Delimiter
SNMP	Simple Network Management Protocol
SOF	Start-of-Frame
SQE	Signal Quality Error
TDR	Time Domain Reflectometer
TX	Transmit
UTP	Unshielded Twisted Pair

Definitions

Cyclic Redundancy Check

The method used to compute the 32-bit frame check sequence (FCS).

Frame Check Sequence

The 32-bit field at the end of a frame that contains the result of the cyclic redundancy check (CRC).

Frame

An Ethernet string of data bits that includes the Destination Address (DA), Source Address (SA), optional length field, Logical Link Control data (LLC data), pad bits (if needed) and Frame Check Sequence (FCS).

Definitions (continued)

Individual Address

The specific Ethernet address assigned to a device attached to the Ethernet media.

Inter-Packet Gap

Time interval between packets on the Ethernet. Minimum interval is 9.6 µs.

Jabber

A condition that results when a Ethernet node transmits longer than between 20 ms and 150 ms.

Packet

An Ethernet string of data bits that includes the Preamble, Start-of-Frame Delimiter (SFD), Destination Address (DA), Source Address (SA), optional length field, Logical Link Control data (LLC data), pad bits (if needed) and Frame Check Sequence (FCS). A packet is a frame plus the Preamble and SFD.

Receive Collision

A receive collision occurs when the CI+/CI- inputs are active while a packet is being received. Applies only to the AUI.

Signal Quality Error

When transmitting on the AUI, the MAC expects to see a collision signal on the CI+/CI- pair within 64 bit times after the end of a transmission. If no collision occurs, there is said to be an "SQE error". Applies only to the AUI.

Slot Time

Time required for an Ethernet Frame to cross a maximum length Ethernet network. One Slot Time equals 512 bit times.

Transmit Collision

A transmit collision occurs when the receive inputs, RXD+/RXD- (10BASE-T) or CI+/CI- (AUI) are active while a packet is being transmitted.

Acronyms Specific to the CS8900

BufCFG	Buffer Configuration - Register B
BufEvent	Buffer Event - Register C
BusCTL	Bus Control - Register 17
BusST	Bus State - Register 18
ENDEC	Manchester encoder/decoder
ISQ	Interrupt Status Queue
LineCTL	Ethernet Line Control - Register 13
LineST	Ethernet Line Status - Register 14
RxCFG	Receive Configuration - Register 3
RxCTL	Receive Control - Register 5
RxEvent	Receive Event - Register 4
SelfCTL	Self Control - Register 15
SelfST	Self Status - Register 16
TestCTL	Test Control - Register 19
TxCFG	Transmit Configuration - Register 7
TxCMD	Transmit Command - Register 9
TxEvent	Transmit Event - Register 8

Terms Specific to the CS8900

Act-Once bit

A control bit that causes the CS8900 to take a certain action once when a logic "1" is written to that bit. To cause the action again, the host must rewrite a "1".

Committed Receive Frame

A receive frame is said to be "committed" after the frame has been buffered by the CS8900, and the host has been notified, but the frame has not yet been transfered by the host.

Committed Transmit Frame

A transmit frame is said to be "committed" after the host has issued a Transmit Command, and the CS8900 has reserved buffer space and notified the host that it is ready for transmit.

Event or Interrupt Event

The term "Event" is used in this document to refer to something that can trigger an interrupt. Items that are considered "Events" are reported in the three Event registers (RxEvent, TxEvent, or BufEvent) and in two counter-overflow bits (RxMISS and TxCOL).

StreamTransfer

A method used to significantly reduce the number of interrupts to the host processor during block data transfers (Patent Pending).

Terms Specific to the CS8900 (continued)

PacketPage

A unified, highly-efficient method of controlling and statusing a peripheral controller in I/O or Memory space.

Standby

A feature of the CS8900 used to conserve power. When in Standby mode, the CS8900 can be awakened either by 10BASE-T activity or host command.

Suspend

A feature of the CS8900 used to conserve power. When in Suspend mode, the CS8900 can be awakened only by host command.

Transfer

The term "transfer" refers to moving frame data across the ISA bus to or from the CS8900.

Transmit Request

A Transmit Request is issued by the host to initiate the start of a new packet transmission. A Transmit Request consists of the following three steps in exactly the order shown:

1. The host writes a Transmit Command to the TxCMD register (PacketPage base + 0144h).

2. The host writes the transmit frame's length to the TxLength register (PacketPage base + 0146h).

3. The host reads BusST (Register 18) to see in the Rdy4TxNOW bit (Bit 8) is set.

Sub-Terms Specific to the CS8900 Used at the End of the Term

These terms have meaning only at the end of a term;

A	Accept
CMD	Command
CFG	Configure
CTL	Control
Dis	Disable
E	Enable
h	Indicates the number is hexadecimal
iE	Interrupt Enable
ST	Status

• Notes •

INTRODUCTION

T1, E1 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of low-power CMOS PCM line interface circuits, with each device optimized for a unique system application. Since introducing the industry's first T1 (1.544 MHz) and E1 (2.048 MHz) line interface circuits (the CS61534 and CS61544), Crystal has shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best-in-class transmitter return loss, short-circuit current limiting, pulse shapes, jitter attenuation, jitter tolerance and low power consumption. The CS61535A, CS61574A, CS61575 and CS61584 are recommended for use in new designs.

Line Interface Units Recommended for New Designs

CS61535A: Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio and M13 multiplexers.

CS61574A: Receive-side jitter attenuation supports line cards in synchronous switching systems (such as central offices, PBXs and 0/1 digital cross connects).

CS61575: Receive-side jitter attenuation with extended FIFO length supports loop-timing in AT&T 62411 compatible customer-premises equipment.

CS61584: The industry's first 3.3V or 5V, dual Line Interface Unit. Intended for high-density line cards. Fully software configurable between T1 and E1 rates with no changes required to external components.

Product	CS61535A	CS61574A	CS61575	CS61584
Number of Channels	1	1	1	2
Power Supply	5V	5V	5V	3.3V or 5V
Transmitter Matches Impedance of Line?	yes	yes	yes	yes
Transmitter Short-circuit Current Limiting/	yes	yes	yes	yes
Location of Jitter Attenuator	Transmit	Receive	Receive	Programmable (xmit, rcvr, none)
Jitter Attenuator FIFO length	32 bits	32 bits	192 bits	64 bits
Control Modes	Serial & hardware	Serial & hardware	Serial & hardware	Serial, parallel & hardware
100% software switchable between T1 & E1	-	-	-	yes
Optional B8ZS, HDB3, AMI Coder	yes	yes	yes	yes
Package	28-pin PDIP & PLCC	28-pin PDIP & PLCC	28-pin PDIP & PLCC	64-pin TQFP
JTAG	-	-	-	yes

Additional New Line Interface Units.
For Use in Existing Boards.

CS61304A and **CS61305A:** These ICs' low-impedance transmit drivers allow the ICs to be used in boards currently employing the LXT304A or LXT305A. Advantages over the LXT304/5A include lower power consumption, optional internal B8ZS/AMI/HDB3 coder and receive AIS detection.

CS61577: A 100% drop-in replacement for the CS61574 which uses the same transformers. Enhancements include transmitter short-circuit current limiting, driver immunity to reflected pulses, lower power consumption, optional B8ZS/AMI/HDB3 coder, and software selection between 75 Ω and 120 Ω E1 output options.

T1 Framer

Crystal Semiconductor's CS2180B T1 Framer is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (SF, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per-channel control options. Packages available include 40-pin DIP or 44-lead PLCC.

While maintaining 100% compatibility, Crystal has improved on industry-standard 2180 designs:

- Support of SLC-96 and T1DM formats
- Compliance with TR-TSY-000191 AIS detection criteria
- Compliance with Bellcore Loss-of-Carrier detection criteria
- Buffered serial data interface, eliminating need for SDI to be valid for both edges of SCLK
- Industrial temperature operating range

Quartz Crystals

To complement our family of T1/E1 Line Interface circuits, Crystal Semiconductor supplies pullable quartz crystals. The CXT6176 (for T1 applications) and the CXT8192 (for E1 applications) are designed for 100% compatibility with Crystal's line interface units and jitter attenuators.

CONTENTS

T1 Transceivers

Features

- Monolithic T1 Framing Device
- Both Transceivers support SF(D4®) and ESF framing formats
- CS2180B also supports SLC-96® and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Pin Compatible with CS2180A, DS2180A and DS2180

General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbed signaling. Clear channel mode can be selected on a per channel basis.

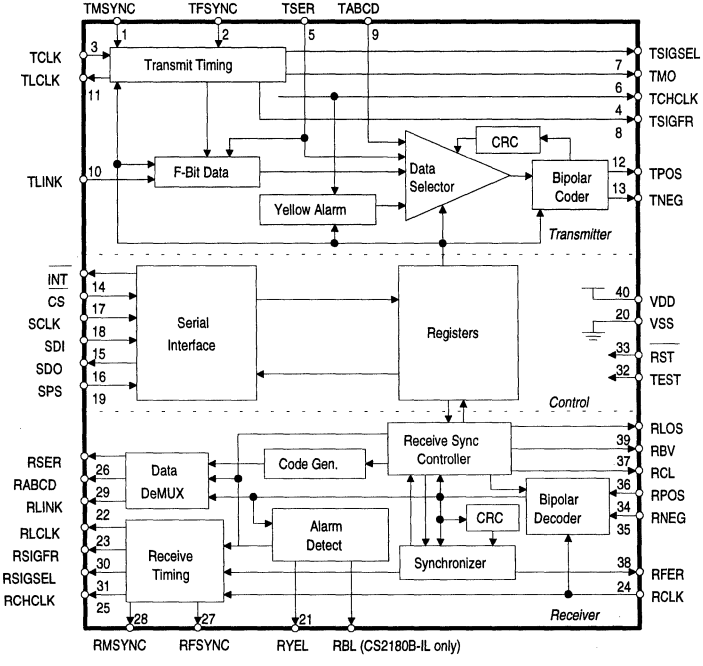
The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61535A, CS61574A and CS61575 PCM Line Interface ICs.

Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

Ordering Information:

CS2180B-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180B-IL	44 Pin PLCC	-40 to 85 °C
CS2180A-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180A-IL	44 Pin PLCC	-40 to 85 °C



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Referenced to GND)	V_{DD}	-	-	6.0	V
Input voltage, any pin	(Referenced to GND)	V_{IN}	-1.0	-	+7	V
Input Current, any pin	(Note 1)	I_{IN}	-10	-	+10	mA
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{STG}	-65	-	150	°C
Soldering Temperature for 10 s.		-	-	-	260	°C

Notes: 1. Transient current of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Voltage		V_{DD}	4.5	5.0	5.5	V
Supply Current	(Notes 2 and 3)	I_{DD}	-	3	10	mA
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 2 and 3)	P_C	-	15	85	mW

Notes: 2. TCLK = RCLK = 1.544 MHz. If RCLK is static and RST is high, PC will typically be 400 mW. Long term operation in this condition may degrade reliability.
3. Outputs open.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; V_{DD} = 5.0 V ±10%; GND = 0 V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	V_{DD} +0.3	V
Low-Level Input Voltage		H_{IL}	-0.3	-	+0.8	V
High-level Output Voltage	(Note 4)	V_{OH}	V_{DD} - 1.0	-	-	V
Low-Level Output Voltage	(I_{OUT} = 1.6 mA)	V_{OL}	-	-	0.4	V
Output Current @ 2.4 V	(Note 5)	I_{OH}	-	-	-1	mA
Output Current @ 0.4 V	(Note 6)	I_{OL}	+4	-	-	mA
Input Leakage Current		I_{IL}	-	-	1	µA
Output Leakage Current	(Note 7)	I_{LO}	-	-	1	µA
Input Capacitance		C_{IN}	-	-	5	pF
Output Capacitance		C_{OUT}	-	-	7	pF

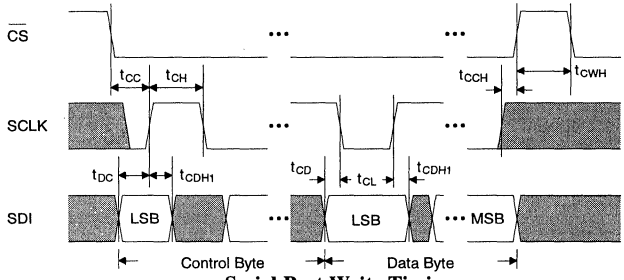
Notes: 4. I_{OUT} = -100 µA. This guarantees the ability to drive one TTL load (V_{OH} = 2.4 V @ I_{OUT} = -40 µA).
5. All outputs except $\overline{INT}$, which is open drain.
6. All outputs.
7. Applies to SDO when tristated.

SWITCHING CHARACTERISTICS - SERIAL PORT

(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

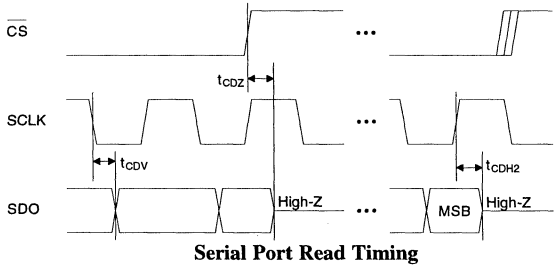
Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup	t_{DC}	50	-	-	ns
SCLK to SDI Hold	t_{CDH1}	50	-	-	ns
SDI to SCLK Falling Edge (Applies to CS2180A)	t_{CD}	50	-	-	ns
SCLK Low Time	t_{CL}	250	-	-	ns
SCLK High Time	t_{CH}	250	-	-	ns
SCLK Rise & Fall Times	t_R, t_F	-	-	500	ns
$\overline{CS}$ to SCLK Set up	t_{CC}	50	-	-	ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{CWH}	250	-	-	ns
SCLK to SDO Valid (Note 8)	t_{CDV}	-	-	200	ns
SCLK Rising to MSB of SDO Hold (Note 9)	t_{CDH2}	25	-	-	ns
$\overline{CS}$ to SDO High-Z	t_{CDZ}	-	-	75	ns

Notes: 8. Output load capacitance = 100 pF.
9. SDO goes High-Z after rising edge of SCLK for MSB, regardless of the state of $\overline{CS}$.



Serial Port Write Timing

10. For the CS2180A only, data bytes must be valid across low clock periods to prevent transients in operating modes. t_{CD} is not a requirement for the CS2180B. In the CS2180B data is latched on the rising edge of SCLK.
11. Shaded regions indicate *don't care* states.



Serial Port Read Timing

12. Serial port write must precede a port read to provide address information.
13. SDO will go High-Z: 1) if $\overline{CS}$ returns high at anytime; 2) after outputing MSB.

SWITCHING CHARACTERISTICS - TRANSMITTER

(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

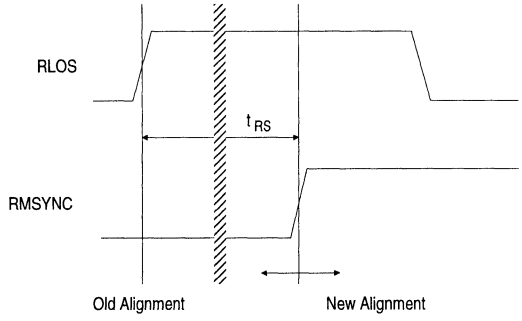
Parameter	Symbol	Min	Typ	Max	Units
TCLK Period	t_P	50	-	-	ns
TCLK Pulse Width	t_{WL}, t_{WH}	50	-	-	ns
TCLK Rise & Fall Times	t_F, t_R	50	-	-	ns
TSER, TABCD, TLINK Setup to TCLK Falling	t_{STD}	250	-	-	ns
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	250	-	-	ns
TFSYNC, TMSYNC Setup to TCLK Rising	t_{STS}	-	-	500	ns
TFSYNC, TMSYNC Pulse Width	t_{TSP}	50	-	-	ns
Propagation Delays					
TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}	250	-	-	ns
TCLK Rising to TCHCLK	t_{PTCH}	-	-	200	ns

SWITCHING CHARACTERISTICS - RECEIVER

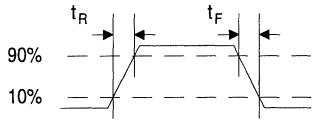
(T_A = -40 to 85 °C; V_{DD} = 5V ± 10%; V_{IH} = 2.0V; V_{IL} = 0.8V; Maximum input rise & fall times of 10 ns)

Parameter		Symbol	Min	Typ	Max	Units
Transition Time, All Outputs		t_{TTR}	-	-	20	ns
RCLK Period		t_P	250	648	-	ns
PCLK Pulse Width		t_{WL}, t_{WH}	100	324	-	ns
RCLK Rise & Fall Times		t_F, t_R	-	20	-	ns
RPOS, RNEG Setup to RCLK Falling		t_{SRD}	50	-	-	ns
RPOS, RNEG Hold to RCLK Falling		t_{HRD}	50	-	-	ns
Minimum RST Pulse Width on System Power Up or Restart		t_{RST}	1	-	-	µs
Propagation Delays						
RCLK to RMSYNC, RFSYNC,RSIGSEL, RSIGFR, RLCLK, RCHCLK		t_{PRS}	-	-	75	ns
RCLK to RSER, RABCD, RLINK		t_{PRD}	-	-	75	ns
RCLK to RYEL, RCL, RFER, RLOS, RBV		t_{PRA}	-	-	75	ns
Average Reframe Time	(Notes 14 and 15)					
193S	RCR.2 = 0	t_{RS}	-	3.75	-	ms
	RCR.2 = 1		-	7.25	-	ms
193E	RCR.2 = 0	t_{RS}	-	7.5	-	ms
	RCR.2 = 1		-	14.5	-	ms
T1DM		t_{RS}	-	750	-	µs
SLC-96®		t_{RS}	-	6.0	-	ms

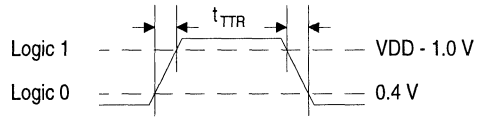
Notes: 14. Average reframe time is the time from the rising edge of RLOS until the rising edge of RMSYNC which updates the receiver output timing.
15. With error free data.



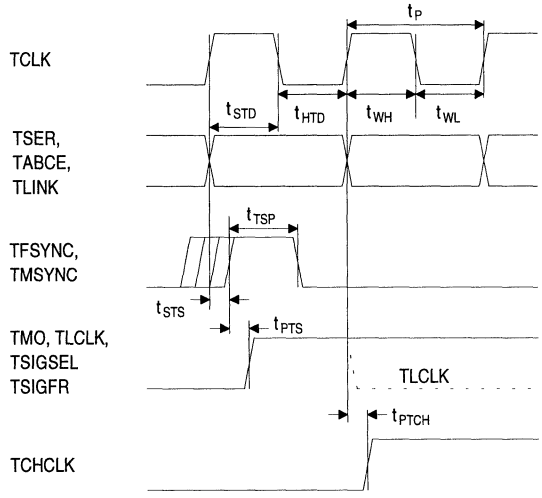
Reframe Timing.



Rise and Fall Times for RCLK & TCLK.

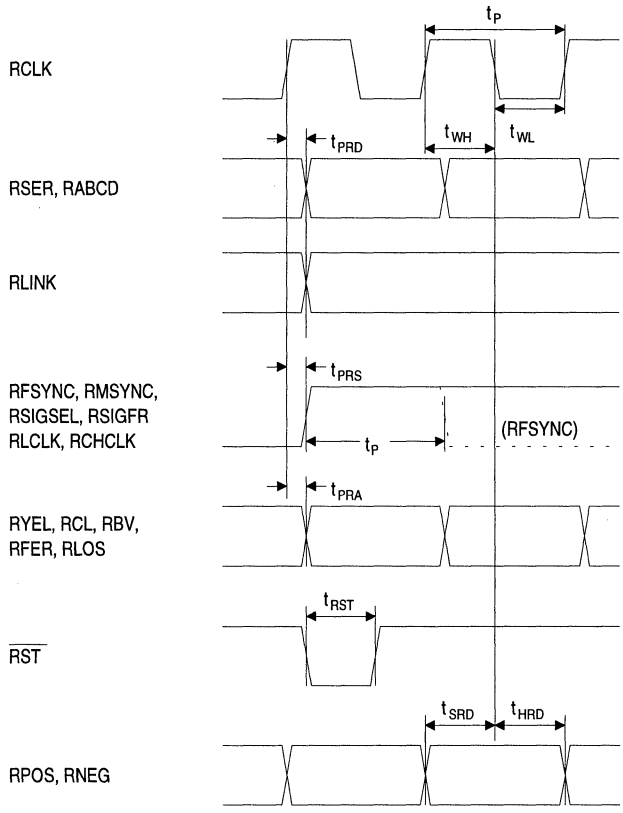


Transition Times for All Receiver Outputs.



Note: TMO, TLCLK, TSIGSEL and TSIGFR are generally coincident with the rising edge of TCLK.

Transmitter Timing.



Receiver Timing.

GENERAL DESCRIPTION

The CS2180A is a monolithic CMOS circuit that encodes and decodes T1 (1.544 MHz) digital transmission formats for SF(D4®) (193S: 12 frames per superframe), and ESF (193E: 24 frames per superframe) framing formats. The CS2180B also encodes and decodes the SLC-96® (SLC-96®: 72 frames per superframe) and DDS® T1DM (T1DM: 12 frames per superframe plus unique channel number 24) formats.

Both the CS2180A and the CS2180B provide full support for individual clear channels, bit-robbed signaling, alarm detection and generation, zero suppression, and idle channels. An overview of the 193S, 193E, SLC-96® and T1DM framing formats is provided in the Applications Section. The device provides independent transmit and receive sides, with a shared serial controller interface for use with a host processor. A hardware mode is also available for operation independent of a host controller. The SLC-96® and T1DM formats can be selected only via the CS2180B serial controller interface.

The serial interface provides access to 16 on-chip control and status registers. The control registers are used to configure global parameters such as the framing format and zero suppression mode, as well as transmitter or receiver specific parameters. A hardware interrupt is provided, which can be configured via interrupt mask and status registers to signal any combination of alarm conditions.

Transmitter commands include enabling external framing bit, CRC, or S-bit insertion, declaring individual DS0 channels clear and/or idle, and enabling yellow and blue alarm modes in different formats. The receiver can be configured to replace individual incoming channels with idle or digital milliwatt (μ-LAW) codes, and a large variety of resync options are provided. Bipolar violations, CRC and framing errors are automatically counted in another set of registers which can be arbitrarily reset via the serial interface to provide variable saturation points. The Receive Status Register (RSR) provides data on all error and alarm conditions, and in conjunction with the Receive Interrupt Mask Register (RIMR), can be configured to signal an interrupt on $\overline{INT}$ in response to any alarm condition.

3

Note: there are two different naming conventions in practice concerning the numbering of bits within a word. The most common convention in EE and Computer Science is to number the bits as 0 - 7, starting from the LSB. This is the convention used throughout this data sheet when referring to register bits. A different convention is used in the telecom literature when referring to the bits in a digital transmission stream. In this case, they are numbered 1 - 8, *starting from the MSB*. This convention is maintained in this data sheet whenever referring to the bits of a DS0 channel word.

CS2180B ENHANCEMENTS

Enhancements made in the CS2180B include the following. The SLC-96® and DDS® T1DM framing formats are supported in host mode. The AIS (Blue Code) detection is made compatible with TR-TSY-000191 requirements (unframed all ones), and a received-blue-alarm output pin is added to the PLCC package. The Receive Carrier Loss detection criteria is made compatible with the industry standard requirement of 175 ±75 zeros. The receiver line code decoder is now universal. The decoder will automatically decode either AMI or B8ZS. The CS2180B B8ZS control option controls only the transmitter's encoder. The universal decoder simplifies the provisioning of B8ZS in the network. Lastly, the serial control interface was simplified. When writing data bytes on SDI, it is no longer necessary to have SDI valid for both the rising and falling edges of SCLK. Rather, SDI need be stable only on the rising edge of SCLK.

HOST MODE

Serial Interface

For applications in which the device is to interface with a host processor, the CS2180A and CS2180B can be configured to run in host mode by tying the Serial Port Select pin (SPS) to the +5 V supply (VDD). This allows access to the serial port, providing a large number of configuration options via the 16 on-chip control and status registers.

Serial read/write timing, controlled by SCLK, is entirely independent of the transmit and receive timing. This allows the host microcontroller to monitor the status register and counters, modify configuration options, and issue commands asynchronously with the T1 system. A serial timing overview is provided in Figure 1.

All data transfers are initiated by setting Chip Select ($\overline{CS}$) low. Any read or write to the serial port is initiated by writing an 8-bit command word. The command word consists of 4 separate fields (see Figure 2). When reading from the port, data is output on the falling edge of SCLK, and held until the next falling edge.

CS2180A Only: All data is written to and read from the port LSB first. When writing to the port, input data is not latched, and the device registers are open to the bus during SCLK low. *To avoid transient corruption of the device registers, data must be valid for the entire low period of SCLK.*

CS2180B Only: All data is written to and read from the port LSB first. When writing to the port, SDI input data is sampled on the rising edge of SCLK.

D0 (LSB) is the R/$\overline{W}$ field, and specifies whether the current operation is to be a read or a write: 1 = read, 0 = write. The second 4 bits (D1 - D4) contain the address field. Written LSB first, they specify which of the sixteen registers to access. D5 (Device Select) should be set to zero when addressing the CS2180A or CS2180B. However, if the CS2180A or CS2180B shares the same serial interface lines with a Crystal TI Line Interface (see Figure 3), D5 will be set to a "1" when addressing the Line Interface device. The CS2180A and CS2180B will ignore any read/write commands with a "1" in D5, allowing both parts to share $\overline{CS}$. D6 is reserved, and must be set to 0 for normal operation.

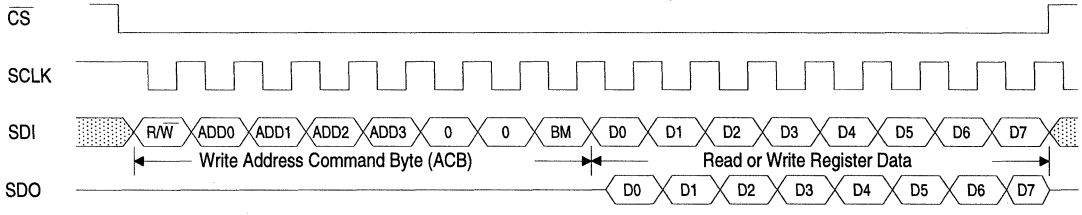


Figure 1. Serial Read/Write Timing

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BM	**0**	**DS**	**ADD3**	**ADD2**	**ADD1**	**ADD0**	**R/W**
0 Individual 1 Burst	Set to "0"	0 CS2180A/B 1 CS Line Dr.	(MSB)	Register Address Field		(LSB)	0 Write 1 Read

Figure 2. Address Command Byte (ACB)

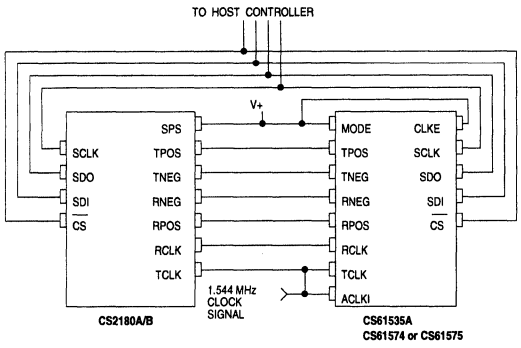


Figure 3. Interfacing with a Crystal T1 line Interface IC.

D7 (MSB) specifies burst mode if set to 1. When using burst mode, the address field of the command word must be "0000", any other value will invalidate the command, and the CS2180A and CS2180B will simply ignore it. This effectively means that the command for a burst write is 80 (hex) and a burst read is 81 (hex).

Burst mode allows the sixteen registers to be consecutively read or written. Writing all registers allows fast initialization at power-up or system reset. (Note that the Receiver Status Register, RSR, is read-only, so a write during burst mode will have no effect.) When using burst mode, registers are read or written in address order, 0000 (RSR) to 1111 (RMR3). Burst mode ends on the first rising edge of $\overline{CS}$. See Table 1 for a complete list of the CS2180A and CS2180B on-chip registers.

ADDR	REGISTER NAME AND DESCRIPTION		(T) TRANSMIT (R) RECEIVE
0000	RSR	**Receive Status Register** - A read only register which reports all active receiver alarm conditions.	R
0001	RIMR	**Receive Interrupt Mask Register** - A mask which allows selection of individual alarm conditions for generation of hardware interrupt	R
0010	BVCR	**Bipolar Violation Count Register** - A bipolar violation alarm is generated after this 8 bit counter surpasses it's user definable limit.	R
0011	ECR	**Error Count Register** - Two separate 4 bit counters, which record OOF errors, and frame bit or CRC errors. Like BVCR, each can be preset to a saturation point.	R
0100	CCR	**Common Control Register** - Selects global configuration options, such as: framing mode, zero suppression, or loopback.	T/R
0101	RCR	**Receive Control Register** - Selects receiver specific options, such as the resync algorithm or insertion of digital milliwatt codes.	R
0110	TCR	**Transmit Control Register** - Selects transmitter specific options, such as alarm generation, clear or idle channel enable, and external S-bit or CRC insertion.	T
0111 1000 1001	TIR1 TIR2 TIR3	**Transmit Idle Registers** - Each bit of the three TIR registers corresponds to an individual DS0 channel. When set, that channel is replaced with an idle code.	T
1010 1011 1100	TTR1 TTR2 TTR3	**Transmit Transparent Registers** - Each bit corresponds to a DS0 channel. When set, that signaling and B7 zero suppression is disabled for that channel.	T
1101 1110 1111	RMR1 RMR2 RMR3	**Receive Mark Registers** - Each bit correponds to a DS0 channel. When set, the channel data is replaced with an idle or digital milliwatt code.	R

Table 1. On-Chip Registers

7 (MSB)	6		5		4	3		2		1		0 (LSB)	
FM1	**FRSR2**		**EYELMD**		**FM**	**YELS**		**B8ZS**		**B7**		**LPBK**	
See Fig. 4b	0	B8ZS	0	FDL	See Fig. 4b	0	Bit 2	0	Disable	0	Transparent	0	Normal
	1	COFA	1	Bit 2		1	S-bit	1	Enable	1	B7 Stuffing	1	Loopback

Figure 4a. Common Control Register (CCR)

Common Control Register

The Common Control Register (CCR) determines global operating characteristics common to both the transmitter and receiver. It currently provides for selection of the framing mode (193S, 193E, SLC-96® or T1DM), the format of yellow alarms, the zero suppression format (B7 or B8ZS), loopback operation, and control of output to RSR.2. In the CS2180A, CCR.7 is reserved for future use, and should always be set 0 for proper operation. See Figure 4a for an overview of the CCR.

Loopback
CCR.0: LPBK

Setting LPBK (CCR.0) to "1" puts the CS2180A and CS2180B into loopback mode. While in loopback, the TPOS/TNEG and TCLK outputs are internally rerouted directly to the RPOS/RNEG and RCLK inputs, while an unframed, all "1's" stream is output on the TPOS/TNEG pins. All operating modes, except blue alarm transmission, remain functional during loopback. Note that enabling loopback will usually invoke an out-of-frame (OOF) error until the receiver can resync to the new framing alignment. See the section on the Receive Control Register (RCR) for a description of the resync options available.

Zero Suppression
CCR.1: B7
CCR.2: B8ZS

B7 and B8ZS select the zero suppression mode. Setting B7 (CCR.1) to "1" will enable bit 7 zero substitution. This causes any channel word with all zeros to be transmitted with bit 7 (2^{nd} LSB) forced to a "1". B7 mode only affects the transmitter, the receiver does not decode B7. Note that bit 7 stuffing can be disabled on an individual channel basis for clear channel transmission via the Transmit Transparent Registers TTR1 - TTR3 (see description of transmitter which follows).

B8ZS coding operates independent of channel boundaries, and is transparent to all other functions. When using B8ZS, the final transmission stream is examined before transmission, and any eight consecutive zeros will be replaced with a B8ZS code word before transmission.

CS2180A Only: If B8ZS (CCR.2) is set to a "1", B8ZS zero substitution will be enabled in both the transmitter and receiver. Incoming B8ZS codes will be intercepted by the receiver and replaced with 8 zeros before being processed by the rest of the receive side.

CS2180B Only: If B8ZS (CCR.2) is set to a "1", B8ZS zero substitution will be enabled in the transmitter. Independent of the setting of CCR.2, any incoming B8ZS codes will be intercepted by the receiver and replaced with 8 zeros before being processed by the rest of the receive side. The receiver is always capable of receving either AMI or B8ZS encoded data.

Note: For T1DM, CCR.1 and CCR.2 should be set to a "0" since DDS® equipment assures a 1-in-8 one's density.

193S Yellow Alarm Format
CCR.3: YELS

The CS2180A and CS2180B supports two different yellow alarm formats for 193S framing. Whichever format is selected, it will be used by both the transmit side, for yellow alarm generation, and the receive side, for alarm detection.

When using 193S framing, a "0" in YELS (CCR.3) will encode/decode yellow alarms as a "0" in bit 2 (2^{nd} MSB) of all channels. Setting CCR.3 to "1" will cause yellow alarms to be encoded/decoded as a "1" is the S-bit position of frame 12.

Note: For T1DM and SLC-96®, CCR.3 should be set to a "0".

Framing Format
CCR.4: FM
CCR.7: FM1

As shown in Figure 4b, CCR.4 and CCR.7 select the framing format. Note that in the CS2180A, CCR.7 must be set to "0", and the SLC-96® and T1DM formats are not available. See the text for the Transmit Control Register (TCR) and Receive Control Register (RCR) for further information on the particular options available for each framing format.

7	4	
FM1	**FM**	**Format Selected**
0	0	193S (D4)
0	1	193E (ESF)
1	0	SCL-96 (CS2180B only)
1	1	T1DM (CS2180B only)

Figure 4b. Framing Format Selection

Note: Changing the framing mode does not force the receiver to resynchronize. A forced resync should be done to insure correct receiver synchronization after the framing mode is changed.

193E Yellow Alarm Format
CCR.5: EYELMD

The CS2180A and CS2180B supports two different yellow alarm formats for 193E framing. Whichever format is selected, it will be used by both the transmit side, for yellow alarm generation, and the receive side, for alarm detection.

When using 193E framing, a "0" in EYELMD (CCR.5) will encode/decode yellow alarms as a repeating sequence of 00FF (hex) on the 4 kHz facility data link (FDL). If CCR.5 is set, 193E yellow alarms will be handled as a "0" in bit 2 (2^{nd} MSB) of all channels.

Control of RSR.2
CCR.6: FRSR2

CCR.6 allows you to change the meaning of D2 in the Receive Status Register (RSR.2). If CCR.6 is clear, RSR.2 will report the detection of B8ZS codes in the received T1 input. If CCR.6 is set to a "1", RSR.2 will be used to signal a Change of Frame Alignment (COFA). A COFA is reported when the last receiver resync resulted in a change of framing or multiframing alignment. Refer to the description of the Receive Status Register for further information.

TRANSMITTER

The transmit sides of the CS2180A and CS2180B have three types of inputs, the clock, sync, and data inputs. Control is handled through the serial port in host mode, and through the mode control pins in hardware mode (see the last section for a description of hardware mode operation).

Input Data

None of the data inputs are buffered, so the data at each input must be available at the appropriate time for the CS2180A and CS2180B to multiplex into the output stream. All inputs are sampled on the falling edge of TCLK. The delay from input to output is 10 TCLK cycles.

NRZ data for DS0 channels is input on TSER. Framing bits (F_T or FPS bits) and CRC data may either be generated internally or supplied by the host system. If this data is to be externally supplied, it must be inserted into the DS0 input stream at the appropriate frames and input via TSER.

S-bits may be generated internally, or externally provided via TLINK. FDL bits are always provided externally on TLINK. Bit-robbed signaling, when enabled, is always sampled at TABCD. The CS2180A and CS2180B muxes in data from these 3 sources (TSER, TLINK, and TABCD) automatically depending on the transmitter configuration.

Output Data

The completed T1 data stream, ready for line transmission, is output on TPOS/TNEG. For operation with a line interface which is transparent to line coding, the output can be set to dual-unipolar format by clearing bit 7 of the Transmit Control Register (TCR.7). TCR.7 should be set to a "1" for operation with a line interface which provides AMI or B8ZS coding. In this configuration, the data will be output on TPOS in NRZ format, and TNEG will remain low. When operating in hardware mode, output defaults to the dual-unipolar format. TPOS and TNEG may not be tied together, so an external OR gate is recommended if NRZ output is required while in hardware mode.

Frame/Multiframe Synchronization

The CS2180A and CS2180B maintain timing for frame and multiframe alignment with internal counters driven by TCLK. The timing signals generated by those counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. These counters determine when the CS2180A and CS2180B will insert F-bits and sample external signaling data. The frame and multiframe counters can be reset independently via TMSYNC and TFSYNC. If left to run without a sync pulse, the CS2180A and CS2180B will arbitrarily choose a framing alignment.

A low to high transition of TMSYNC, occurring near the rising edge of TCLK, resets the CS2180A's and CS2180B's counters to mark the bit-period concurrent with the next falling edge of TCLK as the F-bit of the first frame of a new superframe. All other timing will be set to match the superframe alignment automatically. TMSYNC may be pulsed once at start-up and left low, or left running in sync with superframe timing.

A low to high transition of TFSYNC, occurring near the rising edge of TCLK, resets the CS2180A's and CS2180B's counters to mark the bit-period concurrent with the next falling edge of TCLK as the F-bit of a new frame. If TMSYNC is used to set superframe alignment, frame alignment will also be set, and TFSYNC may be tied low. There is, of course, no harm in using both TMSYNC and TFSYNC together, as TFSYNC has no effect on multiframe alignment if it is in sync. If, however, TFSYNC is used out of sync with TMSYNC, the superframe align-

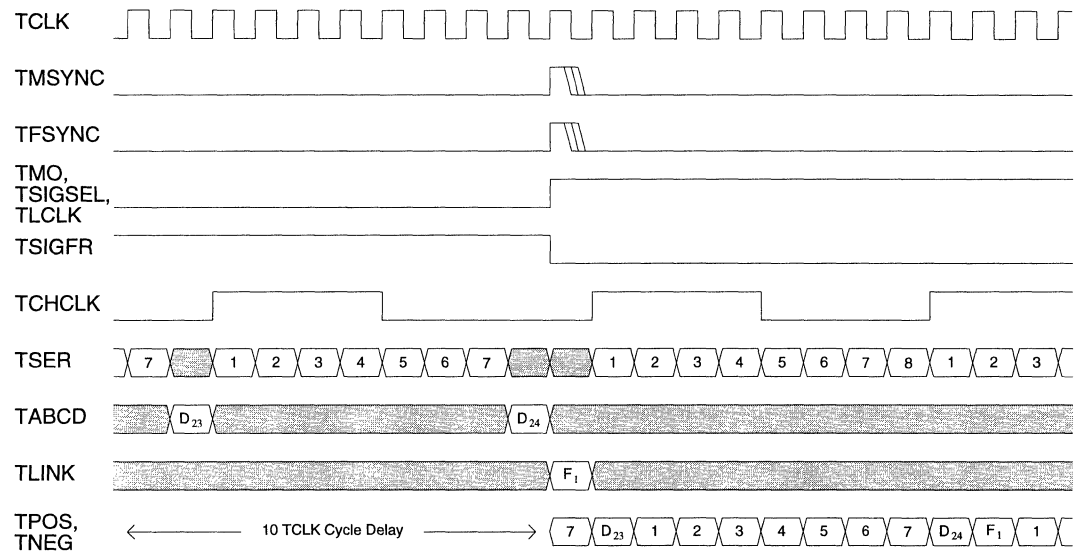


Figure 5. Bit Level Transmit Timing (193E, signaling enabled)

ment will be moved forward by the least number of bits necessary to be in alignment with the new frame boundary.

Figure 5 shows the bit-level timing (with signalling enabled). Note that the delay from input to output is 10 TCLK cycles. TCHCLK transitions high at the beginning of every DS0 channel (50% duty cycle).

193S Timing

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames). TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames (external S-bit insertion).

TSIGSEL runs at twice the frequency of TMO. Logical combination of TMO and TSIGSEL provides a way to distinguish the 6^{th} and 12^{th} frames for external multiplexing of signaling channels. TMO is high for channel A, and low for B. See Figure 6 for timing diagram.

193E Timing

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames). TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames (FDL insertion).

TSIGSEL runs at twice the frequency of TMO. Logical combination of TMO and TSIGSEL provides a way to distinguish the 6th, 12th, 18th, and 24th frames for external multiplexing of signaling channels. TMO is high for channels A and B, and TSIGSEL is high for channels A and C. See Figure 7 for timing diagram.

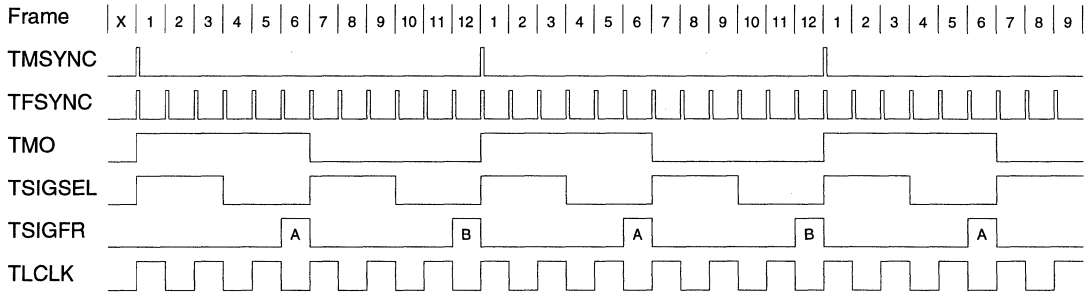


Figure 6. 193S Multiframe Transmit Timing

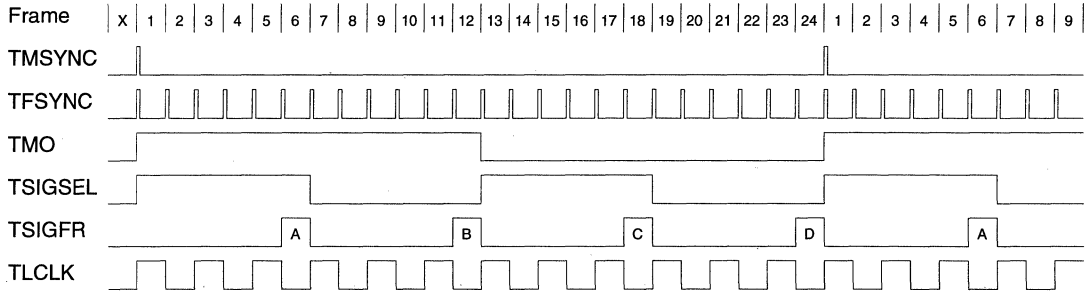


Figure 7. 193E Multiframe Transmit Timing

SLC-96® Timing

Figure A6 of the Application Section, shows the SLC-96® superframe structure. Note that in Figure A6, the first C bit (C1) resides in frame 12. A low to high transition of TMSYNC identifies Frame 1 of Figure A6.

Frame and multiframe timing is output on TCHCLK, TMO, TSIGSEL, TSIGFR and TLCLK. TSIGSEL can be used to identify the location of the DL bits. The TSIGSEL output is high during frames 58 to 11, and is low during frames 12 to 57. When TSIGSEL is low, the CS2180B accepts DL bits on TLINK at a 4 kHz rate, The DL bits which are input on TLINK are: C1-C11, DC, DC, DC, M1-M3, A1, A2, S1-S4. "DC" signifies "don't care" bits. The DC-bit positions correspond to the spoiler bits. The CS2180B internally generates the spoiler bits. The data input on TLINK in the DC position is ignored by the CS2180B. TLCLK is a 4 kHz clock for the TLINK input. TLCLK goes high during odd frames.

TMO transitions high at the beginning of every 12th frame. TSIGFR goes high during signaling frames (every 6 frames). The rising edge of TMO identifies the 6^{th} frame, and the falling edge of TMO identifies the 12^{th} frame for external multiplexing of signaling channels. See Figure 8 for timing diagram.

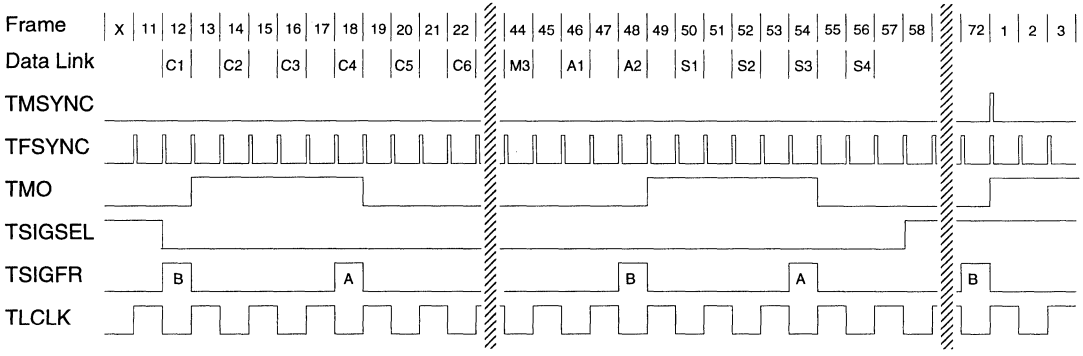


Figure 8. SLC-96® Multiframe Transmit Timing

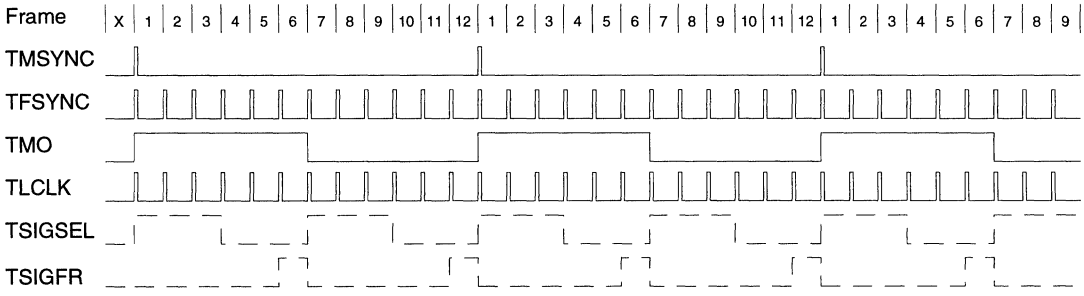


Figure 9. T1DM Multiframe Transmit Timing

T1DM Timing

Frame and multiframe timing is output on TCHCLK, TMO, and TLCLK. TMO transitions high at the beginning of every superframe (50% duty cycle). TSIGFR goes high during signaling frames (every 6 frames).

The channel 24 data link is input on TLINK using TLCLK. TLCLK is a 8 kHz clock with a duty cycle of 1 bit period high per frame. When TLCLK is high, TLINK will be sampled on the falling edge of TCLK. See Figure 9 and "Switching Characteristics - Transmitter" for timing diagrams.

TSIGSEL and TSIGFR serve no purpose in the T1DM mode and can be ignored. However, TSIGSEL and TSIGFR operate as in 193S mode.

7 (MSB)	6	5	4	3	2	1	0 (LSB)
ODF	**TFPT**	**TCP**	**RBSE**	**TIS**	**193SI**	**TBL**	**TYEL**
0 Bipolar	0 Internal	0 Internal	0 Disabled	0 7F (Hex)	0 Internal	0 Normal	0 Normal
1 NRZ	1 External	1 External	1 Enabled	1 FF (Hex)	1 External	1 Blue Alarm	1 Yel. Alarm

Figure10. Transmit Control Register (TCR)

Transmitter Control Register (TCR)

When in host mode, there are a number of options available for transmitter configuration which can be enabled via the Transmit Control Register (TCR), Transmit Transparent Registers (TTR1 - TTR3), and Transmit Idle Registers (TIR1 - TIR3). Serial read and write operations to access these registers are explained in the *Serial Interface* section above. When operating in hardware mode, all control bits in the TCR default to "0" (except TCR.4, which defaults to "1" to enable bit-robbed signaling), and dynamic control is limited to the mode control pins as described under hardware mode below.

The TCR provides control to enable bit-robbed signaling, external framing bit, CRC, or S-bit insertion, and yellow and blue alarm modes. It also provides for two different idle code formats, and selection of bipolar or NRZ output. Figure 10 shows an overview of the Transmit Control Register.

Transmit Yellow Alarm
TCR.0: TYEL

Setting TYEL (TCR.0) to a "1" causes the CS2180A and CS2180B to automatically generate and transmit a yellow alarm in the appropriate format. In 193S mode the yellow alarm format used will be determined by the setting of CCR.3. In 193E mode, the yellow alarm format will be determined by the setting of CCR.5. See Common Control Register, above, for description of the available yellow alarm formats for 193S and 193E modes. In SLC-96® mode, the CS2180B does not generate the yellow alarm code. rather, the user transmits the SLC-96® yellow alarm via the data link. In T1DM mode, the yellow alarm is transmitted in bit 5 of channel 24 (and CCR.3 should be set to a "0"). Clearing TCR.0 disables yellow alarm transmission.

Transmit Blue Alarm
TCR.1: TBL

Setting TBL (TCR.1) to a "1" generates a blue alarm; an unframed sequence of all "1's". If a framed, all "1's" signal is required, an FF (hex) idle code may be output on all channels via appropriate settings of TCR.3 and the TIR registers (see Transmit Idle Code Select below). Blue alarm (Alarm Indication Signal, or AIS) overrides all other transmission data, and a blue alarm is automatically output during loopback. Clearing TCR.1 disables blue alarm transmission.

193S, SLC-96® and T1DM S-bit Insertion
TCR.2: 193SI

TCR.2 is applicable to 193S, SLC-96® and T1DM modes, but not to the 193E mode.

In the 193S and T1DM modes, setting 193SI (TCR.2) to a "1" allows the S-bit (all even F-bits) to be externally supplied via TLINK. When TCR.2 is clear, the S-bit will be internally generated.

In the SLC-96® mode, setting 193SI (TCR.2) to a "1" allows the S-bit (selected even F-bits) to be externally supplied via TLINK, and the user must input all Fs, spoiler and DL bits. When TCR.2 is clear, the CS2180B generates the SLC-

96® spoiler bits and Fs bits, and the user inputs all other DL bits on TLINK using TLCLK.

Note: When using internal S-bit generation (TCR.2 = 0) in conjunction with external F_T bit insertion (TCR.6 = 1), the CS2180A and CS2180B will logically 'OR' the value at TSER with the internally generated value. This means that the data on TSER during S-bit periods should always be "0" to avoid corrupting the generated F_S pattern.

Transmit Idle Code Select
TCR.3: TIS

Individual DS0 channels can be replaced with idle codes by setting the corresponding bits in the Transmit Idle Registers (TIR1 - TIR3) described below. TIS (TCR.3) selects which of two codes to use. A "0" in TCR.3 will cause a 7F (hex) to be inserted into the channels specified in the TIR. Setting TCR.3 to a "1" will select an FF (hex) code. By asserting all 24 channels idle in the TIR, this setting can be used to generate a "framed" blue alarm. Whichever mode is selected, bit-robbed signaling will still effect idle channels unless they are programmed clear (see *Transmit Transparent Registers*, below).

Robbed Bit Signaling Enable
TCR.4: RBSE

A "0" in RBSE (TCR.4) will disable bit-robbed signaling. Setting TCR.4 to a "1" will enable signaling in all channels. In this mode, data on TABCD is inserted into the LSB of all DS0 channels during signaling frames. For mixed voice and data transmission, individual DS0 channels can be programmed clear by setting the corresponding bits in the Transmit Transparent Registers (TTR1 - TTR3) described below.

CRC Pass-through
TCR.5: TCP

In 193E framing mode, the CRC bits (F-bit of frames 2, 6, 10, 14, 18, and 22) may be either generated internally, or supplied by the user. Clearing TCP (TCR.5) causes the CS2180A and CS2180B to generate and insert the CRC bits automatically. If TCR.5 is set to a "1", data for the CRC channel may be externally supplied. When using this mode, CRC bits are sampled from TSER, and must be externally multiplexed into the DS0 channel data at the F-bit times of CRC frames.

F_T/FPS Pass Through
TCR.6: TFPT

When TFPT (TCR.6) is clear, the framing bits for 193S, T1DM and SLC-96® (F_T), or 193E (FPS) are generated internally and automatically inserted into the outgoing data stream. Setting TCR.6 to a "1" allows the framing bits to be externally provided. When using this mode, framing bits are sampled from TSER, and must be externally multiplexed into the DS0 channel data at the F-bit times of the appropriate frames. See note under TCR.2, above.

Output Data Format
TCR.7: ODF

ODF (TCR.7) allows the format of the output data at TPOS/TNEG to be set to either dual-unipolar or NRZ format. Clearing TCR.7 selects for dual-unipolar format on TPOS/TNEG. Setting TCR.7 to a "1" causes data to be output on TPOS in NRZ format, and TNEG is held low. When operating in hardware mode, output defaults to the dual-unipolar format. TPOS and TNEG may not be tied together, so an external OR gate is recommended if NRZ is required while in hardware mode.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
TTR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
TTR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
TTR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Transparent. (No Signaling or B7 Insertion.)

Figure11. Transmit Transparent Registers (TTR1 - TTR3)

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
TIR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
TIR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
TIR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Replaced with Idle Code. (See TCR.3)

Figure 12. Transmit Idle Registers (TIR1 - TIR3)

Transmit Transparent Registers (TTR)

The Transmit Transparent Registers allow individual DS0 channels to be programmed clear, disabling robbed bit signaling and B7 zero suppression for that channel (if selected, B8ZS is unaffected by transparent channels). There are 3 TTR registers: TTR1, TTR2, and TTR3. Each bit in the TTR registers corresponds to a DS0 channel: TTR1.0 = channel 1, TTR1.7 = channel 8, TTR2.7 = channel 16, etc. A channel is programmed clear by setting the bit which corresponds to that channel in the appropriate TTR register. See Figure 11.

Transmit Idle Registers (TIR)

By setting the appropriate bits in the Transmit Idle Registers, individual DS0 channels can be replaced with the idle code selected via TCR.3 (see above). If the idle channel is not also programmed clear (via TTR1 - TTR3), the code may be corrupted during signaling frames if robbed bit signaling is enabled (TCR.4 = 1). There are 3 TIR registers: TIR1, TIR2, and TIR3. Each bit in the TIR registers corresponds to a DS0 channel: TIR1.0 = channel 1, TIR1.7 = channel 8, TIR2.7 = channel 16, etc. A channel is programmed idle by setting the bit which corresponds to that channel in the appropriate TIR register. See Figure 12.

Transmission Insertion Hierarchy

Figures 13a - 13c give an overview of the decision hierarchy which determines the final composition of the output stream. It shows the various control options as inputs into decision branches of the flow chart, and the order in which the various optional signals are muxed into the final data stream.

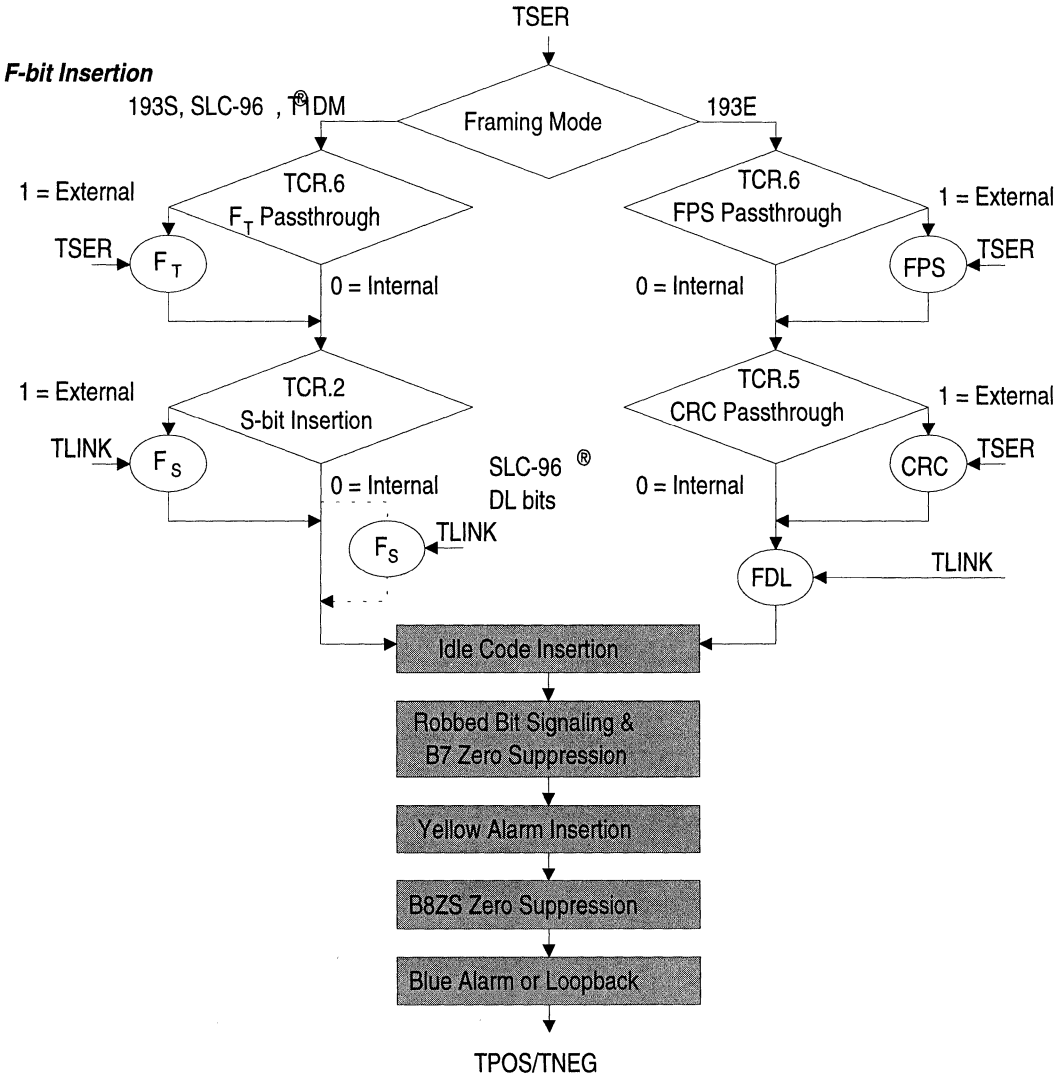


Figure 13a. Transmit Insertion Hierarchy: Framing Bits

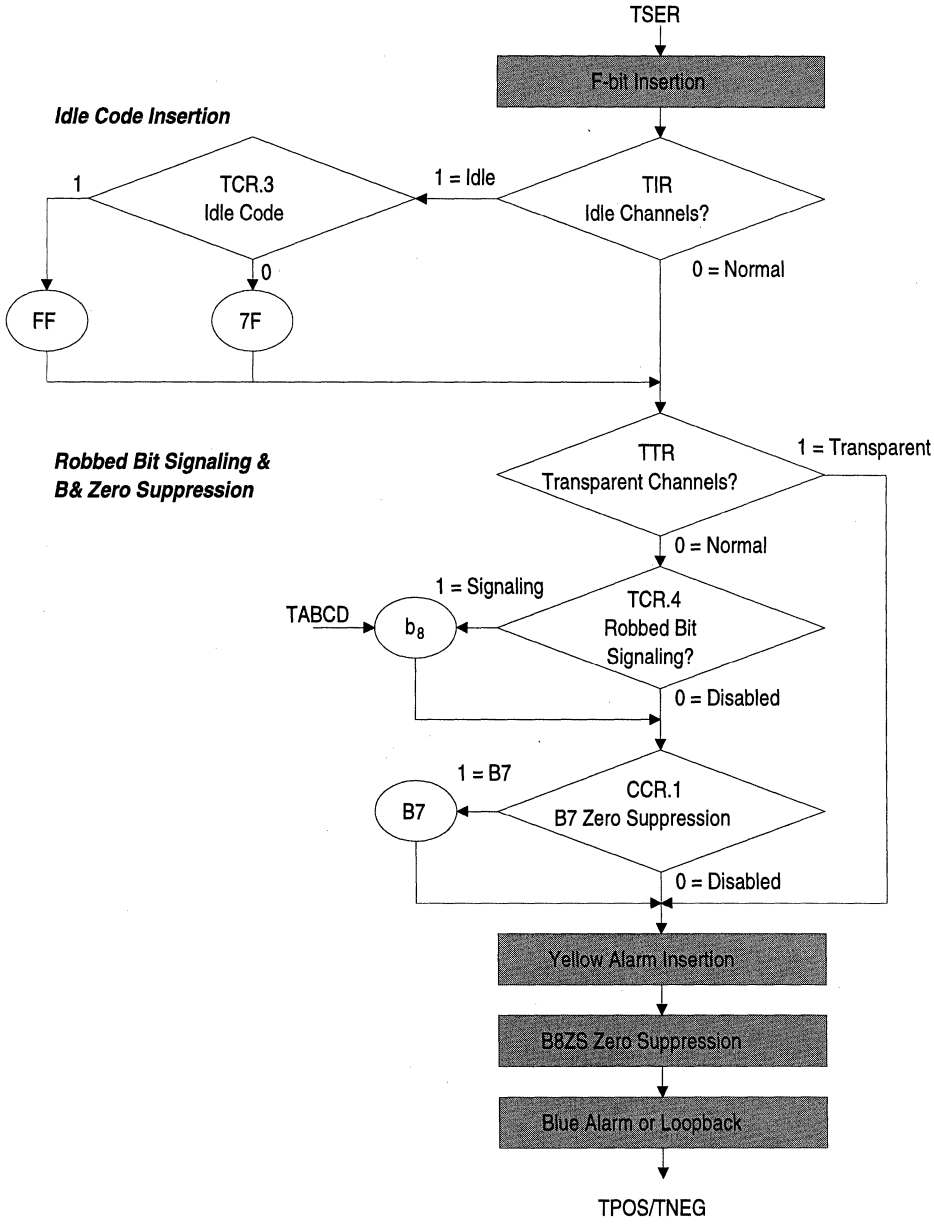


Figure 13b. Transmit Insertion Hierarchy: Idle Codes, Signaling, and B7

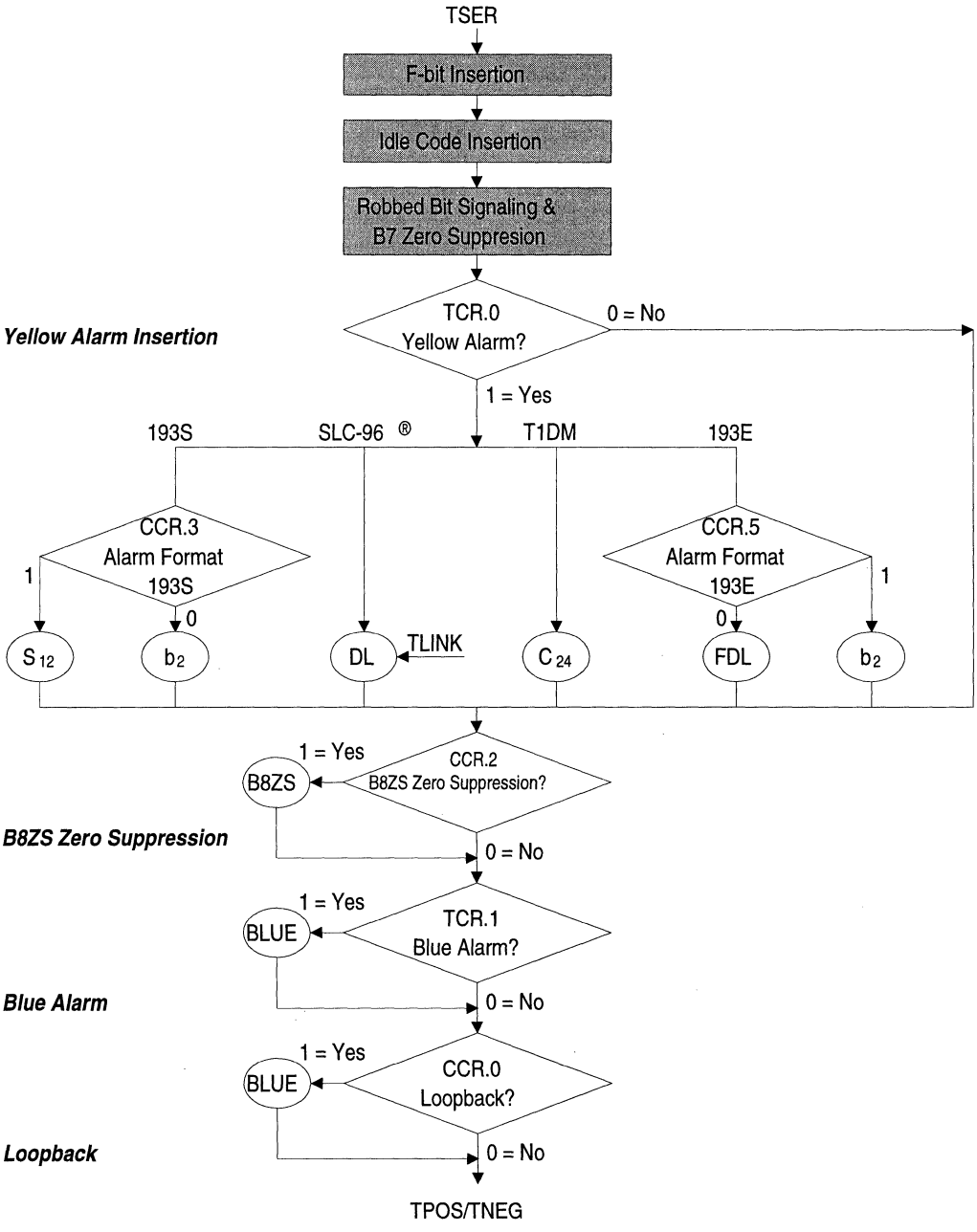


Figure 13c. Transmit Insertion Hierarchy: Alarms, B8ZS, and Loopback

RECEIVER

The receive sides of the CS2180A and CS2180B have only three inputs: the clock (RCLK), the incoming signal (RPOS/RNEG), and a reset pin ($\overline{RST}$). The receiver determines the framing synchronization of the incoming data, and outputs the timing information on the six timing clocks: RLCLK, RCHCLK, RFSYNC, RMSYNC, RSIGFR, and RSIGSEL. Alarms and error conditions are recorded in the Receive Status Register, and output in real time on the five status pins: RYEL, RCL, RBV, RFER, and RLOS. The decoded data is separated into it's component channel, link, and signaling components and output on RSER, RLINK, and RABCD respectively.

When in host mode, the Receive Control Register allows control of the sync algorithm, and insertion of idle or digital milliwatt (μ-LAW) codes into individual DS0 channels. The internal error counters can be accessed, and the Interrupt Mask Register can be programmed to specify the conditions under which a hardware interrupt is generated on $\overline{INT}$. When running in hardware mode, receiver status can still be monitored on the status pins; and access to the error counters, sync algorithm, interrupt mask, and the insertion of idle codes are disabled.

Input Data

The receiver accepts the incoming T1 stream via RPOS/RNEG in dual-unipolar format. Tying RPOS/RNEG together disables the bipolar violation alarm and allows reception of data in NRZ format. Input data is sampled on the falling edge of RCLK. Delay from input at RPOS/RNEG to output on RSER is 13 RCLK periods.

Output Data

The receiver will attempt to sync and decode the framing format selected via CCR.4 and CCR.7. The decoded T1 stream is output in NRZ format on RSER, and updated every RCLK period. Output data is latched on the rising edge of RCLK, and held until the next update.

Link and signaling data is always output on RLINK and RABCD respectively, independent of the transmitter configuration. RABCD outputs the LSB of every DS0 channel word, whether it is currently a signaling frame or not. The data is updated on the channel boundary, concurrent with the MSB, and held until the next update (8 or 9 bits). RLINK outputs either S-bit, SLC-96® DL or FDL bits, depending on the framing format. Data is updated 1 bit period prior to the F_S or FDL frame and held until the next update (2 frames).

Output Clocks

Several timing clocks are provided for identifying this data. The timing clocks are RLCLK, RCHCLK, RFSYNC, RMSYNC, RSIGFR, and RSIGSEL. Logical combination of these six signals allows easy extraction of any part of the received data stream. RMSYNC runs on a 50% duty cycle, and transitions high at the start of each new superframe output on RSER. RFSYNC transitions high at the start of every new frame. Individual DS0 channels are identified by RCHCLK, which runs on a 50% duty cycle and transitions high at the MSB of every individual time slot. Bit level timing is shown in Figure 14.

193S Timing

Link data can be identified by RLCLK, which goes high for all odd numbered frames. RSIGFR is high for signaling frames, and low at all other times. RSIGSEL runs at twice the frequency of RMSYNC. Logical combination of RMSYNC and RSIGSEL provides a way to distinguish the 6^{th} and 12^{th} frames for external multiplexing of signaling channels. RMSYNC is high for those frames containing A signaling bits, and low for frames containing B bits. Refer to Figure 15 for a timing diagram.

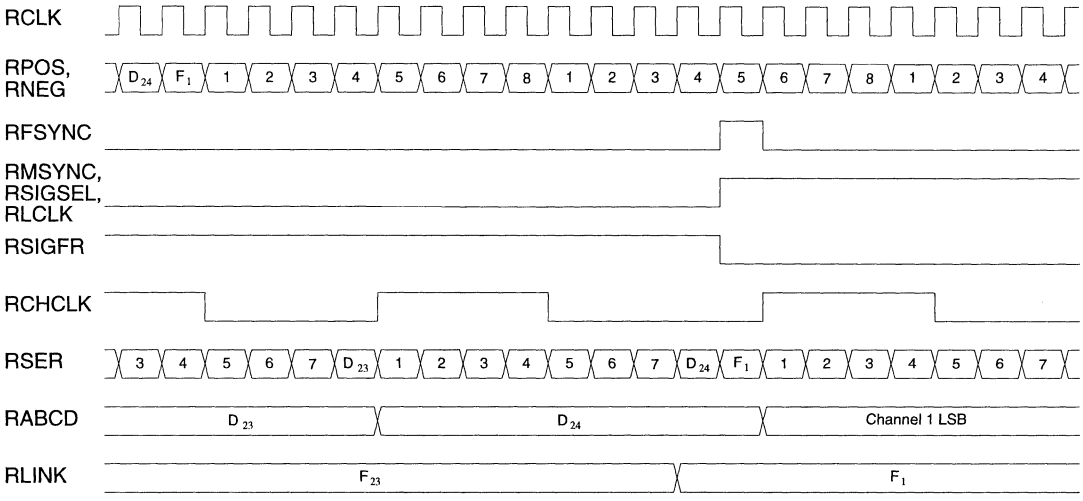


Figure 14. Bit Level Receive Timing (193E mode)

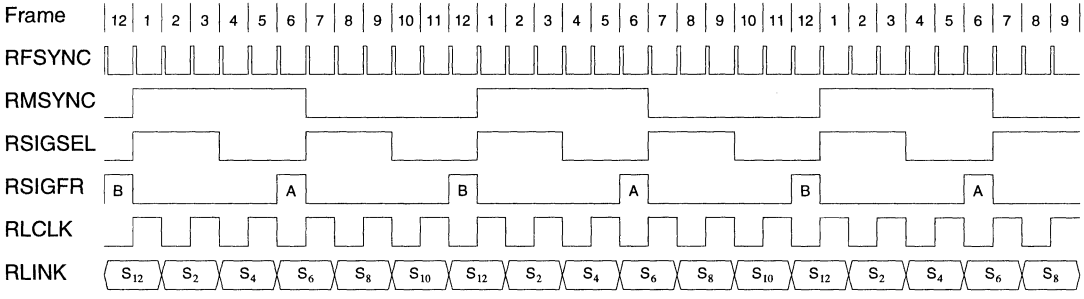


Figure 15. 193S Multiframe Receive Timing

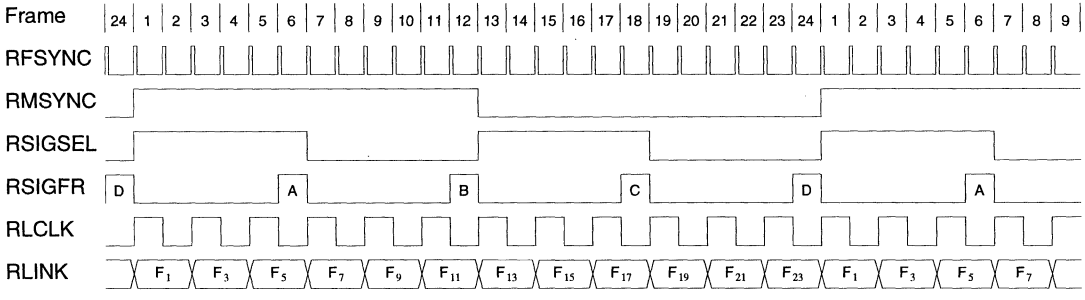


Figure 16. 193E Multiframe Receive Timing

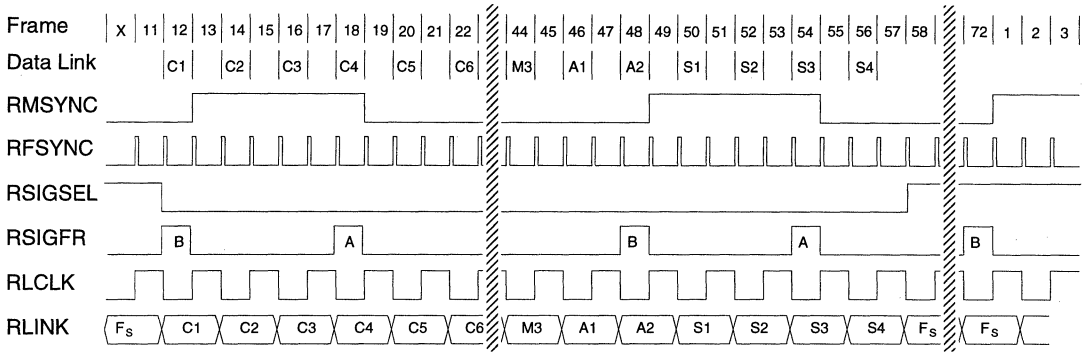


Figure 17. SLC-96® Multiframe Receive Timing

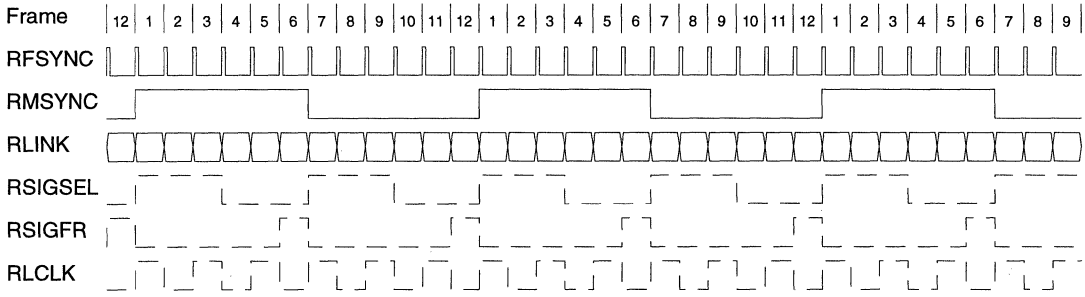


Figure 18. T1DM Multiframe Receive Timing

193E Timing

Link data can be identified by RLCLK, which goes high for all odd numbered frames. RSIGFR is high for signaling frames, and low at all other times. RSIGSEL runs at twice the frequency of RMSYNC. Logical combination of RMSYNC and RSIGSEL provides a way to distinguish the 6^{th}, 12^{th}, 18^{th}, and 24^{th} frames for external multiplexing of signaling channels. RMSYNC is high for frames containing A and B signaling bits, and RSIGSEL is high for frames with A and C bits. Refer to Figure 16 for a timing diagram.

SLC-96® Timing

The CS2180B will output 36 bits of the DL on RLINK using RLCLK. RSIGSEL can be used to locate the DL bits. RSIGSEL will be held high in those frames where Fs bits and the last spoiler bit are present (frames 58 to 11). RSIGSEL is held low in all other frames (frames 12 to 57). RSIGFR is high for signaling frames, and low at all other times. RMSYNC is high for frames containing A signaling bits, and low for frames containg B bits. Refer to Figure 17 for a timing diagram. In SLC-96® mode, the start of a new multiframe occurs on the second rising edge of RMSYNC which occurs while RSIGSEL is high. A multiframe synchronization signal can be generated from RMSYNC and RSIGSEL using the

7 (MSB)		6		5		4		3		2		1		0 (LSB)
ARC		OOF		RCI		RCS		SYNCC		SYNCT		SYNCE		RESYNC
0	OOF/RCL	0	2 out of 4	0	Disabled	0	Idle (7F)	0	Ft/FPS only	0	10 bits	0	Autoresync	rising edge
1	OOF only	1	2 out of 5	1	Enabled	1	Milliwatt	1	Fs/CRC	1	24 bits	1	Disabled	triggered.

Figure 19. Receive Control Register (RCR)

circuit shown in Figure A1 in the Applications section.

T1DM Timing

The 8 kHz link data can be sampled on RLINK using the falling edge of RFSYNC. Refer to Figure 18 and "Switching Characteristics–Receiver" for timing diagrams. RSIGFR, RSIGSEL and RLCLK serve no purpose in the T1DM mode and may be ignored.

Receive Control Register (RCR)

The RCR provides for insertion of either idle or digital milliwatt codes, and has six different control bits which enable a large number of options for tailoring the receiver resync behavior. Refer to Figure 19 for an overview of the RCR.

Receive Code Select/Insert
RCR.4: RCS
RCR.5: RCI

When enabled via RCI (RCR.5), the Receive Mark Registers are used to select individual DS0 channels for insertion of idle or digital milliwatt codes, as selected via RCS (RCR.4). There are three RMR registers: RMR1, RMR2, and RMR3 (Figure 20). Each bit in the RMR registers corresponds to a received DS0 channel: RMR1.0 = channel 1, RMR1.7 = channel 8, RMR2.7 = channel 16, etc. A channel is marked for code insertion by setting the bit which corresponds to that channel in the appropriate RMR register. When RCR.5 is clear, code insertion is disabled, and the contents of the RMR registers are ignored.

RCS (RCR.4) selects whether to insert an idle code, or a digital milliwatt code, into the individual DS0 channels marked in the three Receive Mark Registers (RMR1 - RMR3). Clearing RCR.4 will select for an idle code (7F hex) to be inserted into marked channels. Setting RCR.4 to a "1" will cause a digital milliwatt code (μ-LAW format) to be inserted into all marked channels.

Receiver Synchronization

The receiver monitors the incoming signal for loss of frame alignment (based on F_T or FPS bits only). Unless auto resync has been disabled via RCR.1 (see below), the receiver will automatically initiate a search for the correct framing alignment when loss of synchronization is detected, and RLOS (pin 39) will go high until a new framing alignment is declared.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
RMR1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
RMR2	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9
RMR3	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

"0" = Normal "1" = Corrsponding DS0 Channel is Replaced with Idle or Digital Milliwatt Code. (See RCR.4 and RCR.5)

Figure 20. Receive Mark Registers (RMR1 - RMR3)

When the receiver initiates an auto resync, RSIGFR is held low, but all other output timing will continue in the old alignment until the new framing is found. When the new framing alignment is qualified, the output timing will change to the new alignment at the beginning of the next superframe (or at the start of frame 13 in SLC-96® mode), and RLOS will return low one bit period before the F-bit of the second frame.

A receiver resync has no effect on the transmit side timing or configuration, and behavior of the output timing and RLOS pin is the same as that for an auto resync described above. This is in contrast to a reset initiated via the $\overline{RST}$ pin, which clears all internal registers on the falling edge, including the transmit side registers, resets the output timing while $\overline{RST}$ is low, and then initiates a receiver resync on the rising edge.

The time it takes the receiver to resync depends on resync algorithm selected via RCR.2 and RCR.3. The remaining bits in the RCR (1, 6, and 7) determine under what conditions an automatic resync will be initiated.

Forced Resync
RCR.0: RESYNC

RESYNC (RCR.0) can be used to force a receiver resync. Toggling RCR.0 will initiate a resync immediately on the rising edge. It must then be cleared and set again to initiate another resync. Toggling RCR.0 when going into loopback mode will force the receiver to resync to the new frame alignment immediately. This is faster than waiting for the internal hardware to recognize an out-of-frame (OOF) condition and initiating an automatic resync.

Note: A forced resync should be issued after a change in framing mode to insure correct synchronization.

Auto Resync Conditions
RCR.1: SYNCE
RCR.6: OOF
RCR.7: ARC

SYNCE (RCR.1) can be set to a "1" to completely disable automatic resync. If RCR.1 is clear, a resync will automatically be initiated when the conditions specified by RCR.6 and RCR.7 are detected.

OOF (RCR.6) specifies how many framing bits (F_T or FPS channels only) must be in error before the receiver declares an out-of-frame (OOF) condition. A resync is always initiated (unless disabled) when an OOF is detected. If RCR.6 is clear, an OOF is declared if 2 out of 4 F_T or FPS bits are in error. If RCR.6 is set to a one, an OOF is declared if 2 out of 5 framing bits are errored. Note that the setting of RCR.6 also effects the reporting of OOF events to the Receive Status Register (RSR) and Error Count Register (ECR). Refer to the appropriate sections below for details.

ARC (RCR.7) declares whether the receiver will initiate a resync on an OOF event only, or resync on both OOF and carrier loss (RCL). If RCR.7 is cleared, the receiver will commence resync upon detection of either an OOF event (as defined by RCR.6 above), or an RCL. If RCR.7 is set, the receiver will only resync in response to an OOF condition.

Resync Algorithm
RCR.2: SYNCT
RCR.3: SYNCC

SYNCT (RCR.2) allows you to declare how many bits must be qualified in the framing pattern before the receiver declares synchronization. When RCR.2 is clear, 10 consecutive F_T or FPS framing bits preceding an RMSYNC rising edge must be qualified. Setting RCR.2 to a "1" requires the CS2180A and CS2180B to qualify 24 consecutive F_T or FPS bits preceding an

RMSYNC rising edge before declaring synchronization.

SYNCC (RCR.3) allows you to modify the algorithm employed to search for and qualify the framing alignment. There are two different qualifying conditions available for each framing mode, and the meaning of RCR.3 depends on which framing mode has been selected via CCR.4.

193S Resync

When operating with the 193S framing format, RCR.3 selects whether or not the CS2180A and CS2180B will qualify the F_S bits during resync. If a non-standard S-bit pattern is being used, clearing RCR.3 will enable the device to first search for the F_T framing pattern to find frame alignment, and then only reset multiframe alignment if the F_S pattern can be found. This means that if a valid F_S pattern is not found, synchronization will be declared anyway, and the multiframe alignment indicated by RMSYNC may be false. The S-bits output on RLINK can be used to decode framing externally in such applications.

When using standard F_S signaling, setting RCR.3 to a "1" will cause the device to cross check the F_T and F_S patterns to find sync, and both patterns must be valid before sync is declared. Synchronization will be declared after the number of F_T bits selected by RCR.2 separated by valid F_S bits have been qualified. Note that in either setting, S-bit format yellow alarms are recognized by the synchronizer if they have been selected by setting CCR.3.

193E Resync

Clearing RCR.3 while in 193E mode will cause the CS2180A and CS2180B to use only the FPS framing pattern when looking for a valid framing alignment. If RCR.3 is set, the device will attempt to qualify the CRC bits after a candidate alignment has been found. If the CRC codes match, then the new alignment will be declared, if not, the device will try two more times. If the third CRC code does not qualify, then the device will start a new resync procedure and continue in this manner until a framing alignment can be verified with the CRC codes.

Note that after 24 ms, if there are still multiple candidates for framing alignment, the device will test the CRC codes to eliminate false candidates regardless of the setting of RCR.3. After the framing alignment has been found, it takes about 9 ms for the device to check the CRC codes for the first superframe. If that superframe fails, it takes about 3 ms to check each additional CRC code.

SLC-96® Resync

When operating with the SLC-96® framing format, the receiver should be programmed for F_S/F_T cross-coupling (RCR.3=1) and for minimum resync time (RCR.2=0). This causes the CS2180B to sync on the 10 valid F_T bits seprated by valid Fs bits in frames 65 through 11, and prevents false synchronization to data link and/or spoiler bits.

Note: The CS2180B does not check SLC-96® multiframe alignment once synchronization is declared. In applications such as test equipment where the input data framing format may change or the multiframe alignment may change when the frame alignment does not, the datalink processor should check the phase between RSIGSEL and the DL spoiler bits on RLINK and issue a forced resync when multiframe alignment is incorrect. In the SLC-96® applications, a forced resync should be issued after the device is configured. Since the CS2180B defaults to the 193S framing mode at power up it may sync to SLC-96® data while in the 193S mode. If this occurs the multiframe alignment may be incorrect after the CS2180B is programmed for SLC-96® mode even though the frame alignment is correct.

	7 (MSB)	6	5	4	3	2	1	0 (LSB)
	BVCS	**ECS**	**RYEL**	**RCL**	**FERR**	**B8ZSD**	**RBL**	**RLOS**
1 =	BVCR Saturation	ECR Saturation	Yellow Alarm Detected	Carrier Loss Detected	Frame Error Detected	B8ZS/COFA Detected	Blue Alarm Detected	Resync in progress

Figure 21. Receive Status Register (RSR)

Since the frame alignment is correct no OOF event or auto resync occurs. A forced resync will force the 2180B to synchronize to the frame and multiframe alignment.

T1DM Resync

Resync is based upon the 6-bit sync word in channel 24. Once the sync word is recognized, 6 consecutive frames with the correct sync word and F_S/F_T bits are required before declaring synchronization. RCR.2 must be set to "0". RCR.3 is ignored. When frame synchronization is declared, RLOS goes low and RFSYNC is output concurrent with the f-bits. However, the superframe output clocks (RMSYNC, RSIGFR and RSIGSEL) are held low for an additional short period of time until superframe synchronization is found.

Receive Status Register (RSR)

The CS2180A and CS2180B monitors the incoming T1 data for a number of error conditions. These alarms are recorded in the Receive Status Register (RSR), and output in real time on the status pins: RYEL, RCL, RBV, RFER, and RLOS. Three presettable counters are provided which count the number of occurrences of Bipolar Violations, Framing and CRC errors. The Receive Interrupt Mask Register, RIMR, can be set to specify which of the eight errors recorded in the RSR will generate a hardware interrupt on $\overline{INT}$. When operating in hardware mode, all these registers are cleared, and only the status pins provide real time alarm information.

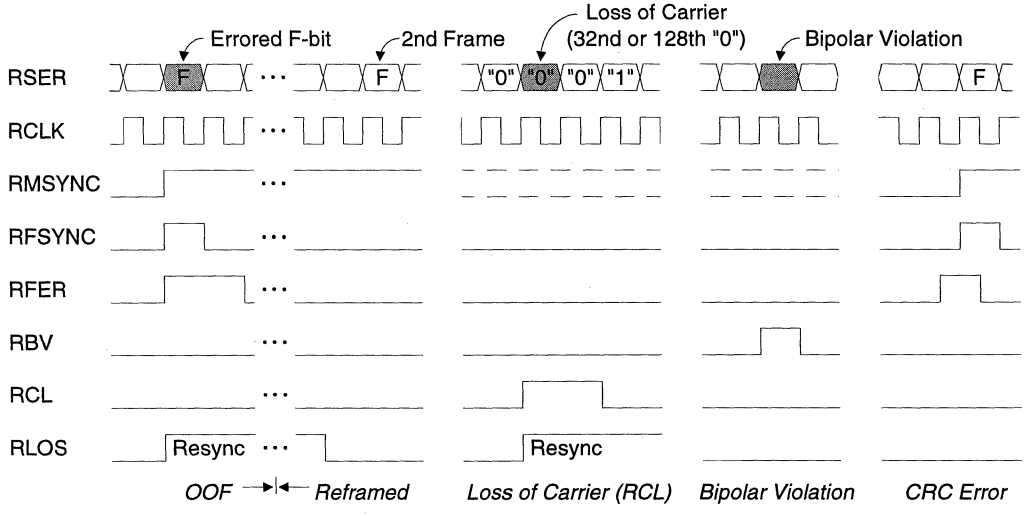


Figure 22. Receive Status Pin Timing

Each of the eight bits of the RSR (Figure 21) corresponds to an alarm condition. A bit in the RSR is set when the corresponding alarm is detected. It will be cleared when the RSR is directly read, unless the alarm condition persists (see Alarm Servicing, below). TCLK is used to clock the internal circuitry which clears RSR after RSR is directly read; therefore, a 1.544 MHz signal must always be input to TCLK, even for a "receiver-only" application. The status pins which correspond to many of the RSR bits operate in real time. They go high when the error is detected, and return low either immediately, or as soon as the error condition is cleared. Alarms are reported synchronously with the emergence of the offending bits on RSER. See Figure 22, and the corresponding alarm description below for further description of status pin timing.

Receive Loss of Sync
RSR.0: RLOS

RLOS (RSR.0) goes high when a receiver resync is in progress. When the receiver is set to auto resync (RCR.1 = 0), the receiver will commence resync when an OOF event or loss of carrier is detected. If in response to an OOF, RLOS transitions high synchronously with the output of the offending F-bit on RSER (see RCR.6).

CS2180A only: If in response to an RCL, RLOS goes high with the 32nd consecutive zero bit.

CS2180B only: If in response to an RCL, RLOS goes high with the 128th ±1 consecutive zero bit.

The RLOS pin will return low one bit period prior to the F-bit of the second frame after the new alignment has been declared (timing signals will reset at the start of the new superframe). Refer to *Receiver Synchronization*, above, for more information.

Receive Blue Alarm
RSR.1: RBL

RBL (RSR.1) will transition high when a blue alarm is detected, and is updated at the beginning of odd-numbered frames.

CS2180A only: A blue alarm is reported whenever less than 3 zeros are detected in the channel data of 2 consecutive frames (F-bit positions are not tested). There is no status pin corresponding to RBL.

CS2180B only: A blue alarm is reported whenever unframed all ones occurs, as per Bellcore TR-TSY-000191. The algorithm used is to simultaneously check for an out-of-frame (OOF) condition, and check for 14 or less zeros out of 13,895 bits. All bits, including frame bits, are tested. RBL goes high on a frame boundary. RBL goes low immediately (indicating the termination of the AIS condition) if OOF goes low, or if 15 or more zeros are counted and the number of bit periods is less than or equal to 13,895. RBL is reported on pin 3 of the 44-pin PLCC package. There is no status pin corresponding to RBL on the 40-pin DIP package.

B8ZS/COFA Detect
RSR.2: B8ZSD

B8ZSD (RSR.2) is a multifunction bit. It can be configured either to report the detection of B8ZS codes, or to indicate a change of framing alignment. This selection is performed through the setting of CCR.6 (see Common Control Register, above). There is no status pin corresponding to RSR.2.

If CCR.6 is clear, RSR.2 will go high every time a B8ZS code is detected in the incoming T1 data. This detector remains operational, whether or not B8ZS substitution has been enabled via CCR.2.

If CCR.6 is set to a "1", RSR.2 will go high in response to a Change of Frame Alignment (COFA). A COFA is reported when the last receiver resync resulted in a change of frame or multiframe alignment. RSR.2 will go high at the same time the timing signals are reset after a resync. (See *Receiver Synchronization*, above.)

Frame Bit Error
RSR.3: FERR

FERR (RSR.3) is set whenever a framing bit is in error.

193S Frame Bit Errors: The framing bits for the 193S is the F_T channel (odd F-bits). The RFER status pin (pin 38) signals the same F_T errors, but in addition, signals F_S errors as well. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for 2 bit periods.

193E Frame Bit Errors: The framing bits for the 193E mode are the FPS channel (F-bits of frames 4, 8, 12, 16, 20, and 24). The RFER status pin (pin 38) signals the same FPS errors, but in addition, signals CRC errors as well. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for 2 bit periods. When signaling a CRC error, RFER will transition high 1/2 bit before the new superframe to indicate a CRC error in the previous superframe. It goes high on the falling edge of RCLK, and is held for only one period, returning low on the next falling edge of RCLK.

SLC-96® Frame Bit Errors: The framing bits for the SLC-96® mode is the F_T channel (odd F-bits). The RFER status pin (pin 38) signals the same F_T errors, but in addition, signals F_S errors as well. The presence of DL bits in F_S bit positions will not be reported as frame bit errors on pin RFER, or in registers RSR.3 and ECR.0-3, and will not contribute to determining that an OOF condition exists. When signaling a frame bit error, RFER will go high simultaneously with the output of the offending F-bit on RSER, and hold for two bit periods.

T1DM Frame Bit Errors: The framing bits for the T1DM mode are the F_T and F_S bits, plus the channel 24 sync word. The RFER status pin (pin 38) signals errors in the frame bits. RFER will go high simultaneously with the F-bit of the frame following the frame in which the error(s) occured, and will remain high for two bit periods.

Receive Carrier Loss
RSR.4: RCL

CS2180A only: Carrier loss is declared when 32 consecutive zero's are detected at RPOS/RNEG. RCL (RSR.2) and the RCL pin (pin 36) transition high with the output of the 32^{nd} zero bit on RSER. The RCL pin will return low as soon as the next "1" is received at RPOS/RNEG.

CS2180B only: Carrier loss is declared when 128±1 consecutive zero's are detected at RPOS/RNEG. RCL (RSR.2) and the RCL pin (pin 36) transition high with the output of the 128^{th}±1 zero bit on RSER. The RCL pin will return low as soon as the next "1" is received at RPOS/RNEG.

Receive Yellow Alarm
RSR.5: RYEL

RYEL (RSR.5) transitions high when a yellow alarm is detected. The format of the alarm detected is determined by the settings of either CCR.3 or CCR.5, depending on the framing format being used. The RYEL pin (pin 21) will return low as soon as the alarm clears, that is, when the next expected alarm bit no longer indicates an alarm.

When using a bit 2 yellow alarm, in either 193S or 193E mode, a yellow alarm is defined as a

7 (MSB)	6	5	4 (LSB)	3 (MSB)	2	1	0 (LSB)
OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0
OOF Count		Presetable. Saturates at 15 (1111).		ESF Error Count		Presetable. Saturates at 15 (1111).	

Figure 23. Error Count Register (ECR)

"0" in bit 2 (2nd MSB) of every DS0 channel. RYEL will signal a bit 2 yellow alarm when 256 or more consecutive channels are detected with a "0" in bit 2. The alarm will clear at the next "1" detected in a bit 2 position.

When using an FDL yellow alarm in 193E mode, RYEL will declare a yellow alarm after 16 repetitions of "00FF" on the FDL. The alarm will clear at the next bit which is out of sequence.

When using an S-bit yellow alarm in 193S mode, RYEL will transition high whenever a "1" is detected in the F-bit of frame 12. The alarm is not cleared until a zero is detected in the F-bit of frame 12.

In T1DM mode , a yellow alarm is detected by checking the channel 24 sync word. In SLC-96® mode, the CS2180B does not recognize yellow alarms, rather, they are recognized by the user via the DL.

Error Count Saturation
RSR.6: ECS

ECS (RSR.6) monitors the status of the Error Count Register (ECR), as shown in Figure 23. The ECR provides two, separate, 4 bit counters at one register address: the ESF Error Count (D0 - D3), and the OOF Count (D4 - D7). RSR.6 will go high after either of these 4 bit counters becomes saturated (at 15), and new OOF or ESF event is detected (the 16^{th} or greater).

The OOF Counter (D4 - D7) records the number of out-of-frame events. An OOF event occurs when 2 out of either 4 or 5 consecutive framing bits are in error, as defined by RCR.6. In 193S mode, the F_T bits are monitored for OOF events, while in 193E mode, the FPS bits are used.

The ESF counter (D0 - D3) records the number of "Errored Superframes". An ESF event in 193E mode is defined as an OOF event, or a CRC error. The ESF counter will be advanced each time either event is detected. In 193S mode, the ESF counter records individual framing bit errors. If RCR.3 is set, requiring F_S bits to be qualified for synchronization, both F_T and F_S bit errors will advance the ESF counter. If RCR.3 is clear, only F_T bits will be monitored.

The OOF and ESF operate separately, each counting up from 0 (hex) and saturating at F (hex). The saturation threshold can be changed for each counter separately, by presetting the counter to some value higher than 0. Because they share the same register address, both counters must be read or written simultaneously. There is no status pin directly corresponding to the ECS bit, but FERR signals individual frame bit and CRC errors, and RLOS signals an OOF event. ECS counter increments are disabled when resync is in progress (RLOS high).

Bipolar Violation Count Saturation
RSR.7: BVCS

Individual Bipolar Violations are recorded in an 8 bit counter, the Bipolar Violation Count Register (BVCR), as show in Figure 24. The BVCR counts up from 0 (all "0's") to 255 (all "1's"). After reaching saturation at 255, every Bipolar Violation received will cause BVCS (RSR.7) to be set to a "1". The BVCR can be preset, to a value greater than 0, to lower the threshold at

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0
Counts individual Bipolar Violations. Sets RSR.7 high when overflows past 255 (11111111). Presetable to any starting value to limit the number of Bipolar Violations needed to overflow.							

Figure 24. Bipolar Violation Count Register (BVCR)

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS
0	Disables interrupts for the corresponding bit of the RSR.						
1	Enables an interrupt whenever the corresponding bit of the RSR goes high.						

Figure 25. Receive Interrupt Mask Register (RIMR)

which it saturates and signals an alarm in RSR.7. Bipolar Violations in valid B8ZS codes are never counted by the CS2180B, but will be counted by the CS2180A if B8ZS format is disabled via CCR.2. Note also that the Bipolar Violation monitoring circuit is disabled entirely when using NRZ input at RPOS/RNEG (selected by tying RPOS/RNEG together).

Individual Bipolar Violations are also reported in real time on RBV (pin 37). RBV will go high simultaneously with the output of the accused bit at RSER. It will only be held for that bit period, falling at the next bit, unless another violation is detected.

Interrupts

When operating in host mode, an interrupt pin, $\overline{\text{INT}}$ (pin 14), is provided to signal the host processor of alarm conditions. $\overline{\text{INT}}$ is an open drain output, and should be tied to the positive supply through a resistor. The $\overline{\text{INT}}$ pin can be programmed to respond whenever any bit of the Receive Status Register (RSR) goes high by setting the corresponding bit of the Receive Interrupt Mask Register (RIMR). Each bit of the RIMR is 'AND'ed with the corresponding bit of the RSR to determine the interrupt. Clearing any bit in the RIMR will disable the interrupt for that alarm condition. When an interrupt has been signaled, the CS2180A and CS2180B must be serviced by the host processor to clear the alarm, as described below. Figure 25 shows an overview of the RIMR.

Alarm Servicing

The CS2180A and CS2180B must be serviced by the host processor to clear the interrupt. Clearing the appropriate bit (or bits, if more than 1 alarm condition exists) in the Receive Interrupt Mask Register (RIMR) will clear any interrupt unconditionally. The interrupt for that alarm will remain disabled until the bit in the RIMR is set again.

Depending on the type of alarm condition, an interrupt may also be cleared without changing the RIMR. If the alarm is in response to a counter saturation (see *Bipolar Violation Count Saturation* and *Error Count Saturation*, above), then the counter must be reset to a value other than all "1's" to clear the alarm. If the interrupt is in response to a real time event, then it may be cleared by a *direct* read (a burst read will have no effect) of the RSR. Note that reading the RSR will only clear the interrupt if the alarm condition no longer persists. For real time events of long duration, clearing the appropriate bits in the RIMR is the only way to clear the interrupt.

PIN NUMBER DIP	PIN NUMBER PLCC	REGISTER MAPPING	DESCRIPTION	FUNCTION
14	16	TCR.2	193S: S-bit Insertion	0 = Internal 1 = External
15	17	CCR.4	Framing Mode Select	0 = 193S 1 = 193E
16	18	TCR.0	Transmit Yellow Alarm	0 = Disabled 1 = Enabled
17	19	CCR.1	B7 Zero Suppression	0 = Transparent 1 = B7 Stuffing
18	20	CCR.2	B8ZS Zero Suppression	0 = Disabled 1 = Enabled

Table 2. Hardware Mode Control Pins

HARDWARE MODE

For stand alone applications or prototyping in which the device is to operate without a host processor, the CS2180A and CS2180B can be configured to run in hardware mode by tying the Serial Port Select pin (SPS) to ground (VSS). This disables the serial port and redefines pins 14-18 (16-20, PLCC) as mode control pins. All registers are cleared, with the exception of the control bits which are mapped to the mode control pins, and TCR.4, which is set to "1", enabling robbed bit signaling. This means that, with the exception of robbed bit signaling, the configuration of the CS2180A and CS2180B in hardware mode is the same as if it were in host mode with all control bits cleared. Dynamic control of a few of the control bits is provided by mapping them directly to pins 14-18 (16-20, PLCC). Operation of these pins is described in *Hardware Mode Control Pins* and Table 2. Note that the SLC-96® and T1DM framing formats are not supported in the hardware mode.

When operating in hardware mode, bit-robbed signaling is enabled for all channels. Signaling data sampled from TABCD is inserted into the 8th bit position (LSB) of every DS0 channel during signaling frames (every 6th frame). There is no facility for programming individual channels clear, however; all channels may be made transparent by tying TABCD to TSER.

When pulling 193SI high for external S-bit insertion in 193S mode, data is sampled from TLINK and inserted into the F-bits of even frames. The 193SI pin has no effect when the device is in 193E mode. When using 193E format, TLINK is sampled for insertion into every odd F-bit (FDL). CRC data is internally generated and cannot be externally supplied.

The receiver will initiate a resync if 2 of the previous 4 framing bits were in error. It will declare synchronization after 10 consecutive F-bits are qualified. When in 193E mode, CRC errors will be reported on RFER, but not used to qualify synchronization. Receiver status can be monitored via the status outputs: RYEL, RCL, RBV, RFER, and RLOS. There is no support for generating blue alarms or idle code insertion when in hardware mode.

Hardware Mode Control Pins

Framing Format

The FM pin allows selection of the framing mode for both transmit and receive sides. Holding this pin low selects 193S framing mode. 193E framing may be selected by pulling the FM pin high.

Yellow Alarm

A yellow alarm may be generated on the transmit side by pulling TYEL high. In 193S mode, bit 2 yellow alarms are supported internally. In 193E mode, FDL yellow alarms are supported. These formats are also detected by the receiver and reported on RYEL. Blue alarms are not supported in hardware mode, except for the transmission of all "1's" on TPOS/TNEG during loopback.

If S-bit yellow alarm is desired while in 193S mode, it may be externally provided via S-bit insertion, enabled by pulling the 193SI pin high. There is, however, no way to generate a bit 2 yellow alarm while in 193E mode. Moreover, the device will not decode either of these formats, while in hardware mode. If they are required, external alarm detection must be provided.

Zero Suppression

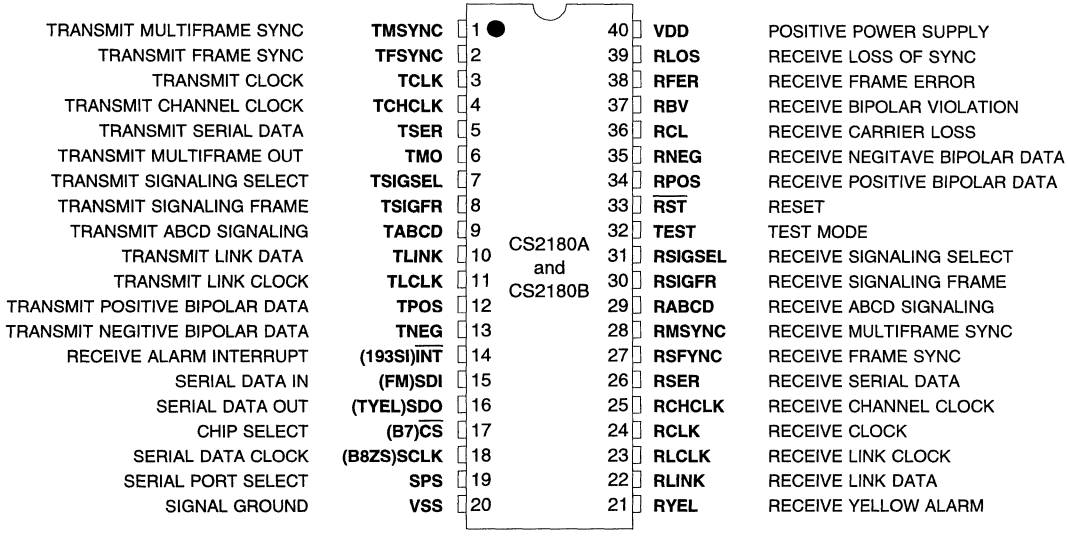
CS2180A only: B7 and B8ZS select the zero suppression format for both transmitter and receiver (B8ZS only). Pulling the B7 pin high enables bit 7 stuffing (B7), pulling the B8ZS pin high enables B8ZS. Transparent mode may be selected by holding both pins low.

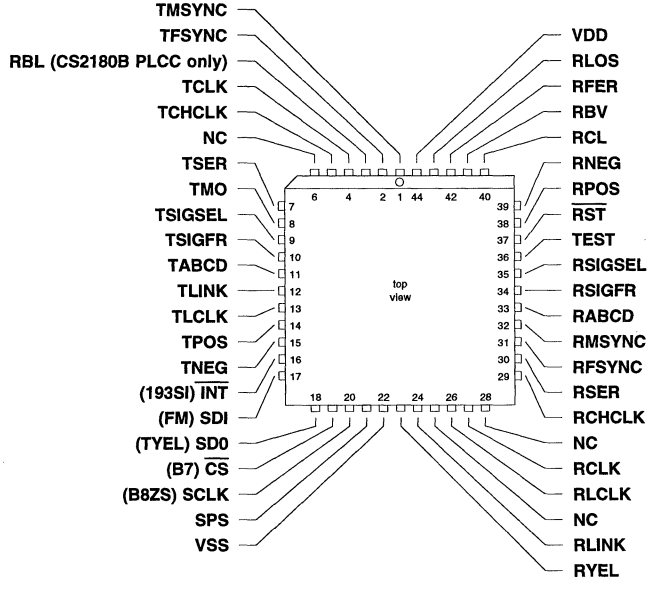
CS2180B only: B7 selects the B7 zero suppression format for the transmitter. Pulling the B7 pin high enables bit 7 stuffing. Pulling the B8ZS pin high enables B8ZS encoding on the transmitter. The receiver is always capable of decoding either B8ZS or AMI-encoded data. Transparent mode may be selected by holding both pins low.

Loopback

Loopback is also provided in the hardware mode by simultaneously driving the B7 and B8ZS pins high. The previous state of the pins is maintained, and the selected zero suppression mode remains effective during loopback. While in loopback, an unframed all "1's" signal (Blue alarm) is output on TPOS/TNEG.

PIN DESCRIPTION





Power Supply Connections

VDD - Positive Supply, Pin 40 (PLCC, Pin 44).

Positive digital power supply. Nominally +5.0 Volts.VDD current requirements increase if RCLK is static, and if $\overline{RST}$ is held high.

VSS - Signal Ground, Pin 20 (PLCC, Pin 22).

Power supply ground. Nominally 0 volts.

Host Mode Serial Interface

Pins 14 - 18 (PLCC, 16 - 20) are multifunctional. When in Host mode, they operate as serial interface pins. When in hardware mode, they are redefined as mode control pins. Their hardware mode operation is described separately under *Hardware Mode Control Pins*, below.

SPS - Serial Port Select, Pin 19 (PLCC, Pin 21).

Must be tied to VDD to select host mode, allowing operation of serial port. Tying SPS to VSS selects hardware mode. Selecting hardware mode clears all internal registers except the common control register (CCR) and transmitter control register (TCR), and redefines pins 14 through 18 (PLCC, 16 - 20) as mode control pins.

Inputs

SDI - Serial Data In, Pin 15 (PLCC, Pin 17).

Serial data input for addressing and writing to on-board control registers. Data is input LSB first. Input data is latched on the rising edge of SCLK. On the CS2180A only, the data must be valid during the SCLK low period to prevent momentary corruption of control registers.

$\overline{CS}$ - Chip Select, Pin 17 (PLCC, Pin 19).

$\overline{CS}$ low enables serial port for read or write. When $\overline{CS}$ transitions high, all data transfers are terminated, port control logic is disabled, and SDO is tri-stated to allow for multiprocessor interface.

SCLK - Serial Data Clock, Pin 18 (PLCC, Pin 20).

Used to read or write the serial port. Data at SDO is output on the falling edge of SCLK and held to the next falling edge. Input data on SDI is latched on the rising edge of SCLK. On the CS2180A only, data must be valid during the SCLK low period to prevent momentary corruption of control registers.

Outputs

$\overline{INT}$ - Receive Alarm Interrupt, Pin 14 (PLCC, Pin 16).

Pulled low to flag host controller when an alarm interrupt condition occurs. The user may select which alarm conditions will trigger an interrupt by appropriately setting the Receive Interrupt Mask Register (RIMR). $\overline{INT}$ is an open drain output, and should be tied to the positive supply (VDD) through a resistor.

SDO - Serial Data Out, Pin 16 (PLCC, Pin 18).

When reading the serial port, data is output LSB first. Data is updated on the falling edge of SCLK and held to the next falling edge. SDO goes to a high impedance state when $\overline{CS}$ is high or after the rising edge of SCLK corresponding to the output of the MSB (last bit output).

Hardware Mode Control Pins

Pins 14 - 18 (PLCC, 16 - 20) are multifunctional. When in Host mode, they operate as serial interface pins. When in hardware mode, they are redefined as mode control pins. Their host mode operation is described separately under *Host Mode Serial Interface*, above. SPS must be tied low to enable hardware mode.

193SI - 193S S-bit Insertion, Pin 14 (PLCC, Pin 16).

In hardware mode, this pin is redefined as a control pin and maps directly to TCR.2. Holding the pin low while in 193S framing format, configures the CS2180A and CS2180B to generate the F_S framing pattern internally for transmission. Pulling 193SI high allows external insertion of transmitted S-bits via TLINK.

FM - Frame Mode Select, Pin 15 (PLCC, Pin 17).

In hardware mode, this pin is redefined as a control pin and maps directly to CCR.4. Holding the FM pin low configures the CS2180A and CS2180B for 193S framing format, pulling it high selects 193E format.

TYEL - Transmit Yellow Alarm, Pin 16 (PLCC, Pin 18).

In hardware mode, this pin is redefined as a control pin and maps directly to TCR.0. Pulling the TYEL pin high enables transmission of a yellow alarm in the default format. In 193S mode yellow alarms default to a "0" in bit 2 (D6) of all DS0 channels. In 193E mode, yellow alarms are encoded/decoded as a repeating pattern of 00FF (hex) on the FDL.

B7 - Bit 7 Zero Suppression, Pin 17 (PLCC, Pin 19).

In hardware mode, this pin is redefined as a control pin and maps directly to CCR.1. Holding the B7 pin low disables bit 7 stuffing (B7) for transparent operation. Pulling the pin high enables B7 zero suppression. Pulling the B7 and B8ZS pins high simultaneously puts the CS2180A and CS2180B into loopback operation.

B8ZS - Bipolar Eight Zero Suppression, Pin 18 (PLCC, Pin 20).

In hardware mode, this pin is redefined as a control pin and maps directly to CCR.2. On the CS2180A, pulling the B8ZS pin high enables B8ZS zero suppression in both the transmitter and receiver. On the CS2180B, pulling the B8ZS pin high enables B8ZS zero suppression in just the transmitter, since the CS2180B receiver is always capable of receiving either B8ZS or AMI-encoded data. Pulling the B7 and B8ZS pins high simultaneously puts the CS2180A and CS2180B into loopback operation.

Transmitter

Inputs

TCLK - Transmit Clock, Pin 3 (PLCC, Pin 4).

1.544 MHz primary transmitter clock. Divided down internally to provide timing signals. TPOS and TNEG are updated on the rising edge of TCLK. Input transmission data (TSER, TABCD, and TLINK) is sampled on the falling edge of TCLK.

A 1.544 MHz signal must be input into TCLK even for those applications where the transmitter is not being used. TCLK is used by the circuitry which clears status registers after those registers have been directly read.

TMSYNC - Transmit Multiframe Sync, Pin 1 (PLCC, Pin 1).

A low to high transition of TMSYNC, occurring near the rising edge of TCLK, resets transmitter's frame and multiframe counters, identifying bit period (at TSER) concurrent with the next falling edge of TCLK as the F-bit of frame 1. If tied low, TFSYNC may be used to set frame alignment, and the CS2180A and CS2180B will arbitrarily choose multiframe alignment. Internal channel, frame, and multiframe counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK.

TFSYNC - Transmit Frame Sync, Pin 2 (PLCC, Pin 2).

A low to high transition of TFSYNC, occurring near the rising edge of TCLK, resets transmitter's frame counters, identifying bit period (at TSER) concurrent with the next falling edge of TCLK as the F-bit of a new frame. If tied low, TMSYNC may be used to set both frame and multiframe alignment. Without any sync input, the CS2180A and CS2180B will arbitrarily choose both frame and multiframe alignment. Internal channel, frame, and multiframe counters are output on TCHCLK, TMO, TSIGSEL, TSIGFR, and TLCLK.

TSER - Transmit Serial Data, Pin 5 (PLCC, Pin 7).

Input data (NRZ format), sampled on the falling edge of TCLK. TSER may also be used to provide externally supplied data for insertion into F_T, FPS, and CRC channels. Refer to *Transmit Control Register*, bits 5 and 6. Delay from TSER to TPOS/TNEG is 10 TCLK periods.

TABCD - Transmit ABCD Signaling, Pin 9 (PLCC, Pin 11).

When enabled, by setting bit 4 of the Transmit Control Register (TCR), data provided on TABCD is inserted into the 8th bit position (LSB) of every DS0 channel during signaling frames. Those are frames 6 and 12 in 193S format, and 6, 12, 18, and 24 in 193E. Signaling on individual DS0 channels may be suppressed by declaring those channels transparent in the Transmit Transparent Registers (TTR). Signaling in hardware mode is always enabled. Delay from TABCD to TPOS/TNEG is 10 TCLK periods.

TLINK - Transmit Link Data, Pin 10 (PLCC, Pin 12).

In 193S framing mode, setting bit 2 of the Transmission Control Register (TCR) enables data on TLINK to be inserted into the S-bit channel (F-bit of all even frames). In 193E mode, TLINK is sampled for data to be inserted into the F-bit of all odd frames for the 4 kHz facility data link (FDL). In the SLC-96® mode, TLINK is sampled for data to be inserted into the DL. In T1DM mode, TLINK is sampled for data to be inserted into the channel 24 "A" data link. Delay from TLINK to TPOS/TNEG is 10 TCLK periods. In hardware mode, external S-bit insertion on TLINK is enabled by setting pin 14 (193SI) high.

Outputs

TPOS, TNEG - Transmit Bipolar Data Outputs, Pins 12 and 13 (PLCC, Pins 14 and 15).

Coded data for transmission, updated on rising edge of TCLK. If TCR.7 is clear, or the CS2180A and CS2180B is in hardware mode, data is output in dual-unipolar format. If TCR.7 is set to a "1", data is output on TPOS in NRZ format, and TNEG is held low. Delay from input to TPOS/TNEG is 10 TCLK periods.

TCHCLK - Transmit Channel Clock, Pin 4 (PLCC, Pin 5).

192 kHz clock which identifies DS0 channel boundaries. TCHCLK rises to indicate that the next bit input on TSER is the first bit (MSB) of the DS0 channel. TCHCLK has a 50% duty cycle.

TMO - Transmit Multiframe Out, Pin 6 (PLCC, Pin 8).

Output of internal multiframe counter. Rising edge marks beginning of multiframe, with 50% duty cycle. Internal multiframe counter can be set on the rising edge of TMSYNC. In 193S mode, TMO is high for frames 1-6, and low for frames 7-12, allowing easy distinction of signaling channels A and B. In 193E mode, TMO is high for 1-12, and low for 13-24, and can be used together with TSIGSEL to distinguish channels A, B, C, and D.

TSIGSEL - Transmit Signaling Select, Pin 7 (PLCC, Pin 9).

In 193S, 193E and T1DM modes, TSIGSEL runs at 2x TMO with a 50% duty cycle. Together with TMO, TSIGSEL provides a way to distinguish signaling channels A, B, C, and D in 193E mode. TMO is high for channels A and B. TSIGSEL is high for channels A and C (frames 1-6 and 13-18). In SLC-96® mode, TSIGSEL provides a way to distinquish when the DL bits are to input.

TSIGFR - Transmit Signaling Frame, Pin 8 (PLCC, Pin 10).

TSIGFR goes high during signaling frames only, remaining low at all other times. Signaling frames are frames 6 and 12 in 193S, SLC-96® and T1DM modes, and 6, 12, 18, and 24 in 193E mode.

TLCLK - Transmit Line Clock, Pin 11 (PLCC, Pin 13).

In 193S, 193E and SLC-96® modes, TLCLK runs at 4 kHz with a 50% duty cycle. It's high during odd numbered frames, and is useful for marking F_S or FDL channel timing (input on TLINK), and F_T, FPS, and CRC channels (input on TSER). In T1DM, TLCLK runs at 8 kHz, with a duty cycle of one bit period high per frame.

Receiver

Inputs

RCLK - Receive Clock, Pin 24 (PLCC, Pin 27).

1.544 MHz primary receiver clock. Receiver data is output on the rising edge, and input on the falling edge of RCLK. If no signal is present on RCLK, $\overline{RST}$ should be held low to minimize power consumption.

RPOS, RNEG - Receive Bipolar Data Inputs, Pins 34 and 35 (PLCC, Pins 38 and 39).

Recovered data, sampled on falling edge of RCLK. Tie pins together to receive NRZ data and disable bipolar violation monitoring circuitry. Delay from RPOS/RNEG to output at RSER is 13 RCLK periods.

$\overline{RST}$ - Reset, Pin 33 (PLCC, Pin 37).

Falling edge of $\overline{RST}$ clears all internal registers and resets receiver error counters. A receiver resync is forced when $\overline{RST}$ returns high. This resync effects only the receiver synchronization, and has no effect on transmit timing, but transmit control modes are cleared. The host processor should restore all control modes following a reset by writing the appropriate control registers. NOTE: *On system power-up, $\overline{RST}$ must be held low to insure initialization of all on-board registers.*

Outputs

RYEL - Receive Yellow Alarm, Pin 21 (PLCC, Pin 23).

Transitions high when a yellow alarm is detected, returns low when yellow alarm is cleared. When in Host mode, Yellow alarm formats for both 193S and 193E modes can be selected via bits 3 and 5 of the Common Control Register. When in hardware mode, the 193S mode defaults to bit 2 Yellow alarms, and the 193E mode defaults to FDL yellow alarms. Refer to bit 5 of the Receive Status Register (RYEL) for a description of alarm detection conditions.

RCL - Receive Carrier Loss, Pin 36 (PLCC, Pin 40).

On the CS2180A, RCL transitions high if 32 consecutive "0's" are detected on RPOS and RNEG and returns low on next "1". On the CS2180B, RCL transitions high if 128±1 consecutive "0's" are detected on RPOS and RNEG and returns low on the next "1".

RBL - Receive Blue Alarm, (CS2180B PLCC only, Pin 3).

Transitions high on a frame boundary if an unframed-all ones and an out-of-frame condition simultaneously occur. Returns low when either out-of-frame ends or zeros are detected.

RBV - Receive Bipolar Violation, Pin 37 (PLCC, Pin 41).

If a bipolar violation is detected, RBV goes high simultaneous with output of accused bit on RSER, low otherwise.

RFER - Receive Frame Error, Pin 38 (PLCC, Pin 42).

Transitions high with the output of an errored framing bit, and is held for 2 bit periods. F_T and F_S bits are tested in 193S and SLC-96® modes, and FPS bits are tested in 193E. In T1DM mode, the F_S, F_T and channel 24 sync bits are tested. Also signals CRC errors in 193E mode, by going high 1/2 bit before the next extended superframe, and holding for 1 period (from falling edge of RCLK to next falling edge).

RLOS - Receive Loss of Sync, Pin 39 (PLCC, Pin 43).

Transitions high during receiver resync, low otherwise. Transitions high when receiver begins a resync, and falls low one frame after new timing is declared.

3

RSER - Receive Serial Data, Pin 26 (PLCC, Pin 30).

Received data, output in NRZ format. Data on RSER is valid and stable on the falling edges of RCLK. Delay from RPOS/RNEG to RSER is 13 RCLK periods.

RABCD - Receive ABCD Signaling, Pin 29 (PLCC, Pin 33).

Signaling data extracted from LSB of DS0 channels during signaling frames is valid on RABCD during corresponding channel output on RSER (LSB is available on RABCD seven bit periods before it appears at RSER). During non-signaling frames, RABCD continues to output LSB concurrently with word on RSER. After update, data on RABCD is valid and stable on the falling edge of RCLK.

RLINK - Receive Link Data, Pin 22 (PLCC, Pin 24).

In 193S mode, S-bit data is output on RLINK one RCLK prior to start of corresponding even frame, and held for 2 frames until next update. In 193E mode, FDL data is output on RLINK one RCLK prior to start of corresponding odd frame, and held for 2 frames until next update. After update, data on RLINK is valid and stable on the falling edge of RCLK.

In SLC-96® mode, all Fs and DL bits are output on RLINK using RLCLK. In T1DM mode, channel 24 "A" link data is output on RLINK, and is valid and stable on the falling edge of RFSYNC.

RLCLK - Receive Link Clock, Pin 23 (PLCC, Pin 26).

RLCLK runs at 4 kHz with a 50% duty cycle. It's high during odd numbered frames. RCLK is useful for marking S-bit, DL or FDL channel timing, output on RLINK. RLCLK is present, but serves no useful purpose in the T1DM mode.

RCHCLK - Receive Channel Clock, Pin 25 (PLCC, Pin 29).

192 kHz clock which identifies DS0 channel boundaries output on RSER. RCHCLK is useful for parallel to serial conversion of DS0 channel data.

RFSYNC - Receive Frame Sync, Pin 27 (PLCC, Pin 31).

Goes high for one RCLK period concurrent with the F-bit of each new frame output on RSER, low otherwise. In the T1DM mode, the falling edge of RFSYNC can be used to sample the "A" link channel on RLINK.

RMSYNC - Receive Multiframe Sync, Pin 28 (PLCC, Pin 32).

Rising edge signals the F-bit of 1st frame of multiframe. RMSYNC runs on 50% duty cycle, high for frames 1-6 in 193S mode, distinguishing signaling channels A and B. In 193E mode, it's high for frames 1-12, and can be used with RSIGSEL to distinguish channels A, B, C, and D.

RSIGFR - Receive Signaling Frame, Pin 30 (PLCC, Pin 34).

High during signaling frames, low at all other times, including resync. Serves no purpose in T1DM mode.

RSIGSEL - Receive Signaling Select, Pin 31 (PLCC, Pin 35).

In 193E mode, RSIGSEL goes high for frames 1-6 and 13-18, identifying signaling channels A and C. Used together with RMSYNC, which is high for channels A and B, it allows identification of all 4 signaling channels. In 193S mode, RSIGSEL goes high for frames 1-3 and 7-9. Serves no purpose in T1DM mode. In SLC-96® mode, RSIGSEL goes high in those frames where Fs bits (frames 59 to 11) and the last spolier bit (frame 58) are present; goes low in all other frames (frames 12 to 57).

Miscellaneous

TEST - Test Mode, Pin 32 (PLCC, Pin 36).

Tie to VSS for normal operation. Factory use only.

APPLICATIONS

System Connection Diagram

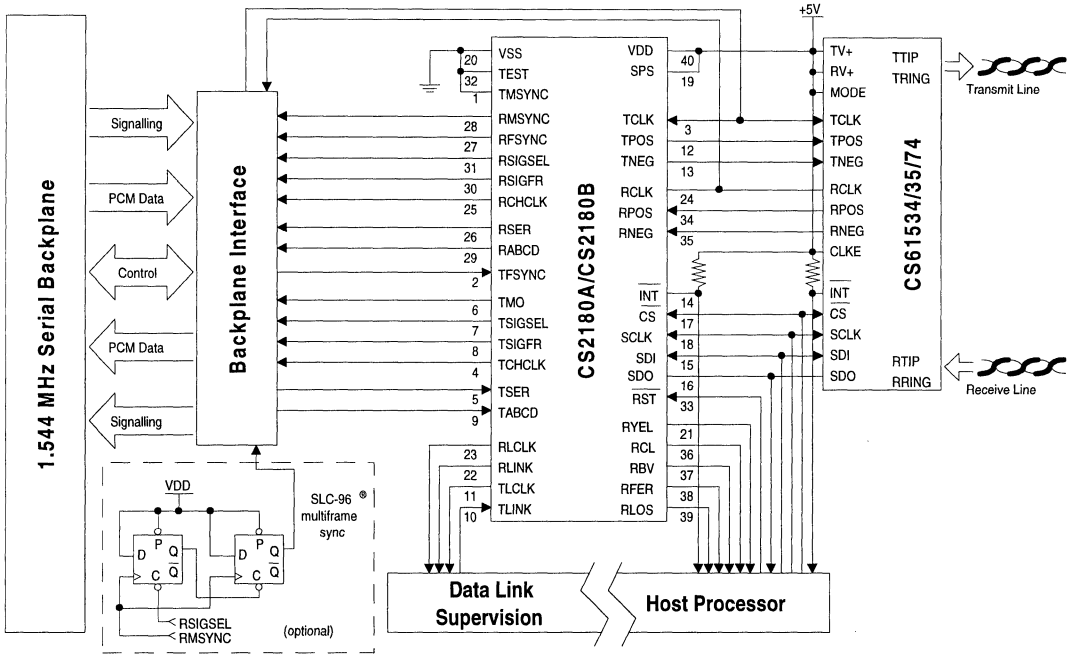


Figure A1. Typical System Connection

T1 Frame Formats

T1 is the basic format in the T-carrier PCM transmission system used in the United States. Detailed technical specifications can be found in ANSI T1.107-1988, ANSI T1.403-1993, ANSI T1.408-1990.

The T1 format time-division multiplexes 24 digitized voice (telephone) or data channels into a single, 1.544 Mbps data stream. This format is used primarily for transmission over dual twisted-pair cable with digital repeaters at 6000 ft. intervals. The T-carrier system also defines higher level formats for long-haul transmission via satellite or microwave relay. These higher level formats are constructed by multiplexing several T1 lines into higher and higher data rates. Figure A2 gives an overview of the T-carrier hierarchy.

Level	Number of voice channels	Bit Rate (Mbps)
T-1	24	1.544
T-1C	48	3.152
T-2	96	6.312
T-3	672	44.736
T-4	4032	274.176

Figure A2. T-carrier Hierarchy

The T1 format provides a 64 kbps channel for each individual voice or data line. These PCM voice channels consist of 8-bit samples which are sampled at 8 kHz for a data rate of 64 kbps. A T1 frame is constructed by multiplexing 24 of these DS-0 channels and inserting a framing bit at the beginning of the series. This results in 192 bits of channel data, plus an F-bit, for a total of 1.544 Mbps (193 bits/frame transmitted at 8 kHz). See Figure A3.

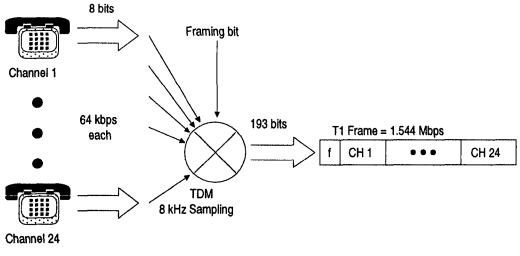


Figure A3. T1 Overveiw

Multiple T1 frames are then grouped into superframes of 12 or 24 frames to provide for framing and signaling synchronization. The older 193S or SF(D4®) format defines a superframe as 12 frames, with the F-bits carrying 2 channels of synchronization signals. The emerging 193E, or Extended Superframe Format (ESF) calls for 24 frames in a superframe. This allows the 24 F-bits to be divided into 3 separate channels for framing, CRC checks, and system messages.

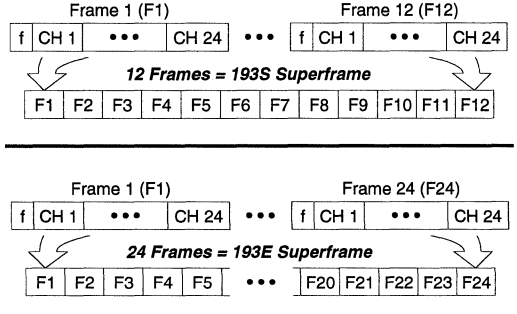


Figure A4. Framing Overveiw

Additional variations on T1 are used for Subscriber Loop Carrier (SLC-96®) and Digital Data Service (DDS®) T1DM.

193S Framing Format

Figure A5 shows the bit uses in the 193S framing format. The framing bits are divided into two channels. The odd F-bits are designated as the F_T (terminal framing) channel, which always carries a repeating pattern of "101010". This pattern allows synchronization to the frame boundaries, and distinguishes the even and odd frames. The even F-bits are designated as the F_S (signaling framing) channel. This channel carries a different synchronization code (001110) which identifies superframe alignment. The F_S channel can alternately be used as a message channel for system use, in which case there is no facility provided for multiframe synchronization.

Signaling information associated with each individual voice channel, such as on-hook/off-hook, call progress, dialing digits, etc., is transmitted within the voice channel itself. The signaling data is transmitted in the LSB of each channel

193S	F-bits		Channel bits		Signalling Options		
Frame	F_T	F_S	Data	Signalling	T	2	4
1	1						
2		0					
3	0		1-8				
4		0					
5	1						
6		1	1-7	Bit 8	-	A	A
7	0						
8		1					
9	1		1-8				
10		1					
11	0						
12		0	1-7	Bit 8	-	A	B

Figure A5. 193S Framing Format

during the 6th and 12th frames. The original LSB of the channel is actually replaced with the signaling data, hence this is known as "robbed-bit" signaling. The 6th and 12th frames can be treated as one, 2-state channel, allowing a 2-state signal to be updated twice every superframe. The two frames can also be treated as separate channels (A and B), yielding up to 4 separate codes for each channel every superframe. For voice grade applications, these signaling bits offer no noticeable degradation in the signal quality. When error-free data transmission is required however, robbed bit signaling can be disabled (transparent mode), and some other signaling facility must be provided by the host system.

193E	F-bits			Channel bits		Signaling Options			
Frame	FPS	FDL	CRC	Data	Signalling	T	2	4	16
1		m		1-8					
2			C1						
3		m							
4	0								
5		m							
6			C2	1-7	Bit 8	-	A	A	A
7		m		1-8					
8	0								
9		m							
10			C3						
11		m							
12	1			1-7	Bit 8	-	A	B	B
13		m		1-8					
14			C4						
15		m							
16	0								
17		m							
18			C5	1-7	Bit 8	-	A	A	C
19		m		1-8					
20	1								
21		m							
22			C6						
23		m							
24	1			1-7	Bit 8	-	A	B	D

Figure A6. 193E Framing Format

193E Framing Format

The 193E or Extended Superframe Format allows much greater flexibility in both the use of the framing bits, and the number of signaling channels provided. As shown in Figure A6, the framing bits are divided into 3 channels. The FPS, or Framing Pattern Sequence, provides a synchronization signal for determining frame and superframe alignment. The FDL, or 4 kHz Facility Data Link, provides a dedicated channel for system messages. The CRC (Cyclic Redundancy Check) channel allows CRC check sums to be transmitted with each superframe to monitor line quality. As with the 193S format, every 6th frame is designated as a signaling frame. The 4 signaling frames (6, 12, 18, and 24) can be multiplexed in different configurations to provide 2, 4, or 16-state signaling codes.

SLC-96® Framing Format

The SLC-96® T1 format is used between the Local Digital Switch (LDS) and a SLC-96® Remote Terminal (RT). The framing format is a SF(D4®) superframe format with specialized Data Link (DL) information bits. The DL bits consist of Concentrator (C), Spoiler (S), Maintenance (M), Alarm (A) and Protection Line Switch (PLS) bits as shown in Figure A7.

T1DM Framing Format

The T1DM T1 format is used for DDS® service among hub and local intermediate DDS® offices. As shown in Figure A8, the framing format is a SF(D4®) superframe format with a specialized channel 24 structure. The T1DM accepts up to 23 DS-0 signals and inserts one seven-bit byte from each signal into the first twenty-three 8-bit channel slots of the DS1 frame. The 24th channel slot contains a special synchronizing byte as shown in Figure A9. DDS® equipment insures that every DS0 channel contains at least one "1". Therefore, neither B8ZS nor bit-7 zero substitution should be selcted in the CS2180B.

SLC-96®	F-bits			Channel bits	
Frame	F_T	F_S	DL	Data	Signaling
1	1			1-8	
2		0			
3	0				
4		0			
5	1				
6		1		1-7	Bit 8 (A)
7	0			1-8	
8		1			
9	1				
10		1			
11	0				
12			C1	1-7	Bit 8 (B)
13	1			1-8	
14			C2		
15	0				
16			C3		
17	1				
18			C4	1-7	Bit 8 (A)
19	0			1-8	
20			C5		
21	1				
22			C6		
23	0				
24			C7	1-7	Bit 8 (B)
25	1			1-8	
26			C8		
27	0				
28			C9		
29	1				
30			C10	1-7	Bit 8 (A)
31	0			1-8	
32			C11		
33	1				
34			S=0		
35	0				
36			S=1	1-7	Bit 8 (B)

SLC-96®	F-bits			Channel bits	
Frame	F_T	F_S	DL	Data	Signaling
37	1			1-8	
38			S=0		
39	0				
40			M1		
41	1				
42			M2	1-7	Bit 8 (A)
43	0			1-8	
44			M3		
45	1				
46			A1		
47	0				
48			A2	1-7	Bit 8 (B)
49	1			1-8	
50			S1		
51	0				
52			S2		
53	1				
54			S3	1-7	Bit 8 (A)
55	0			1-8	
56			S4		
57	1				
58			S=1		
59	0				
60		0		1-7	Bit 8 (B)
61	1			1-8	
62		0			
63	0				
64		0			
65	1				
66		1		1-7	Bit 8 (A)
67	0			1-8	
68		1			
69	1				
70		1			
71	0				
72		0		1-7	Bit 8 (B)

Figure A7. SLC-96® Framing Format

T1DM	F-bits		Channel Bits
Frame	F_T	F_S	
1	1		1-7 (Bit 8 of user channels is reserved for network use)
2		0	
3	0		
4		0	
5	1		
6		1	
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	

Figure A8. T1DM Framing Format

Bit	Assignment
0	Synchronization Pattern = 1
1	Synchronization Pattern = 0
2	Synchronization Pattern = 1
3	Synchronization Pattern = 1
4	Synchronization Pattern = 1
5	Yellow Alarm: 0 = alarm; 1 = no alarm
6	8 kHz Data Link ("A" channel)
7	Synchronization Pattern = 0

Figure A9. T1DM Channel 24 Format

Alarms

Figure A10 shows a useful overview of the alarm operation in a PCM link. When an intermediate monitoring system (or central office repeater) detects a loss of signal, it transmits an all "1's" signal (Blue alarm, or Alarm Indication Signal) on the line to maintain clock recovery operation in the subsequent digital repeaters and the destination's receiver. The same Blue alarm may be used by the source transmitter if, for some reason, it cannot maintain normal functionality (such as during loopback).

When the loss of signal is detected at the intermediate monitor, an internal Red alarm (also known as a Service Alarm Indication, or Prompt Maintenance Alarm) is generated. While in a Red alarm mode, the monitor transmits a Yellow alarm back to the source's receiver, indicating a remote loss of alignment. This Yellow alarm informs the source that there's a problem farther down the line and it's transmission is not being received at the destination.

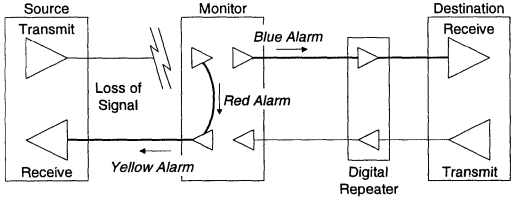


Figure A10. Alarm Operation

Zero Substitution

As was mentioned in the T1 overview, data is transmitted over dual twisted-pair cable with digital repeaters at 6000 ft. intervals. It is encoded in a bipolar AMI (Alternate Mark Inversion) format. Successive "1's" are encoded alternately as positive and negative voltage pulses. A zero is simply an absence of pulses. This means that a long stream of "0's" is indistinguishable from a dead line. Clock recovery circuits in the network maintain clock synchronization by syncing to the "1's" pulses in the transmission stream. Synchronization may be lost if there are too many consecutive zero's, hence there is a general requirement that there be at least 12.5 % "1's" density in the transmission stream. Furthermore, no more than 15 consecutive "0's" are allowable. Various zero substitution schemes have been developed to meet these requirements. The CS2180A and CS2180B supports B7 and B8ZS zero suppression formats.

3

B7 Zero Substitution

B7 zero substitution guarantees at least one "1" in all DS0 channels. This satasfies the 12.5 % ones density, and guarantees that more than 15 consecutive zeros will never occur. In B7 substitution systems, the 7^{th} bit (2^{nd} LSB) of an all zero channel is forced to a "1". This strategy maintains 1's density in voice grade transmission, with negligible audible interference. The drawback with the B7 format is that it's impossible for the receiving end to detect and remove the changed bits. This makes B7 zero suppression unacceptable for clear channel transmission, in which the integrity of the data must be maintained.

B8ZS Zero Substitution

B8ZS (Bipolar Eight Zero Substitution) satisfies the one's density requirement without corrupting transmission data. Instead of operating on individual channels, the B8ZS format looks at the entire transmission stream. Any eight consecutive zeros are replaced with an 8 bit code. This code uses specific bipolar violations of the AMI format to distinguish it from the ordinary data. If the last "1" transmitted before a string of zeros was encoded as a positive pulse, then the B8ZS code for the next eight bits will be 000+-0-+. Similarly, if the last "1" was a negative pulse, then the code will be 000-+0+-. In either case, bipolar violations occur in the fourth and seventh bits. These violations are decoded as a string of

zeros by the CS2180A and CS2180B if B8ZS is enabled. The received B8ZS code is replaced with eight zeros before any other processing is done on the incoming data. Note also that even if B8ZS is not enabled, the CS2180A and CS2180B monitors the incoming signal for B8ZS codes, and reports them on RSR.2 (if CCR.6 = 0).

A serious provisioning problem exists in the network regarding B8ZS. It is sometimes difficult to selectively turn-on B8ZS on all segments of an end-to-end path through the network, especially when some equipment types, such as M13s, sometimes require that all four lines on a line card be configured the same way. It is thereby highly desireable that all receivers in the network be able to receive B8ZS independent of the provisioning of B8ZS on the corresponding transmitter. Therefore, the CS2180B has its B8ZS receiver turned on all of the time, and bit CCR.2 controls only the B8ZS encoder in the transmitter. The CS2180B reports B8ZS occurrences on RSR.2. B8ZS substitutions will not increment the Bipolar Violation Count register.

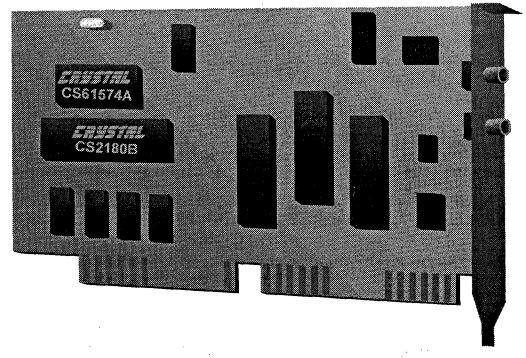
Digital Milliwatt Code

The Digital Milliwatt code is the digital representation of a 0 dBm0, 1 kHz signal. It's used as a test reference for calibrating channel bank equipment as specified in AT&T Publication 43801.

Evaluating the CS2180B

The CS2180B and the CS61574A can be easily evaluated using the GL Communications Super-T1 Card. Both parts are used on the card which plugs into an IBM PC-AT slot. The card connects to a T1 line through standard bantam jacks with signal levels that are DSX-1 compatible. Easy to use menu driven software allows configuration and monitoring of the CS2180B and CS61754A registers directly. Additional application software allows monitoring and test of a T1 line, including detailed error logging, oscilloscope-type display of incoming data, BER test capability, PCM DSP processing functions, user definable outputs, and T1 file transfer capability. Customized software applications can also be easily developed for the card.

For further information contact:
GL Communications
841-F Quince Orchard Blvd.
Gaithersburg, Md. 20878
Ph: 301-670-4784



GL Super T1 Card

Semiconductor Corporation

CS61304A

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Fully Compliant with AT&T 62411 Stratum 4, Type II Jitter Requirements
- Low Power Consumption
- B8ZS/HDB3/AMI Encoder/Decoder
- 50 mA Transmitter Short-Circuit Current Limiting

General Description

The CS61304A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61304A is a pin-compatible replacement for the LXT304A.

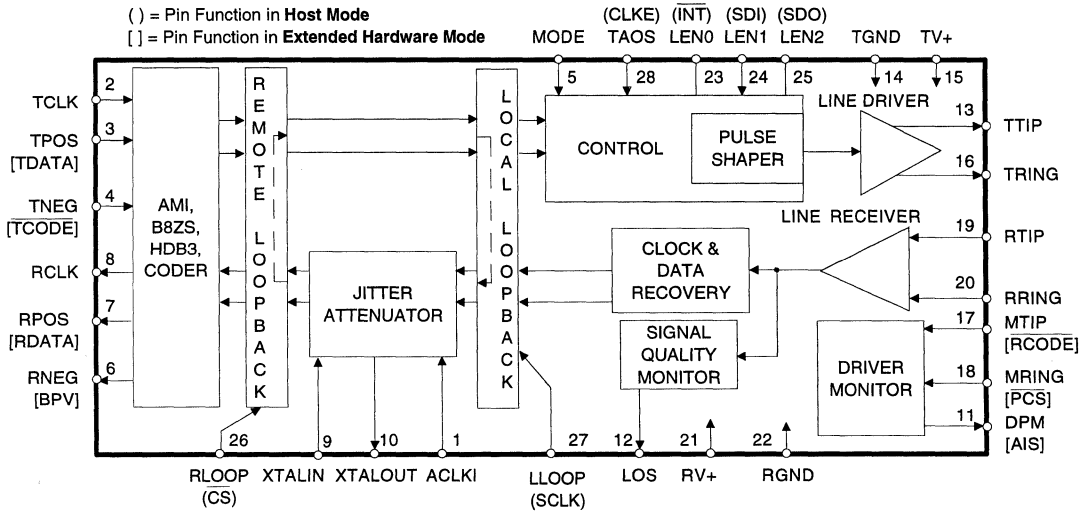
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The CS61304A has a receiver jitter attenuator optimized for T1 CPE applications subject to AT&T 62411 and E1 ISDN PRI applications. The transmitter features internal pulse shaping and a low impedance output stage allowing the use of external resistors for transmitter impedance matching.

Applications

- Primary Rate ISDN Network/Termination Equipment
- Channel Service Units

ORDERING INFORMATION

CS61304A-IP1	28 Pin Plastic DIP
CS61304A-IL1	28 Pin Plastic PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to RGND=TGND=0V)	RV+	-	6.0	V
	TV+	-	(RV+) + 0.3	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption (Notes 4,5)	P_C	-	-	350	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density, 5.25 V, LEN2/1/0=1/1/1, a 100 Ω load and a 1:1.15 transformer.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 6, 7) PINS 1-4, 17, 18, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 6, 7) PINS 1-4, 17, 18, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 6, 7, 8) I_{OUT} = -400 µA PINS 6-8, 11, 12, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 6, 7, 8) I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	µA
Low-Level Input Voltage, PIN 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5	V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5 (Note 9)	V_{IM}	2.3	-	2.7	V

Notes:
6. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate digital output.
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. Output drivers will drive CMOS logic levels into a CMOS load.
9. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 10)				
E1, 75 Ω	(Note 11)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 12)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 13)	2.7	3.0	3.3	V
T1, DSX-1	(Note 14)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
1:1 transformer and 75Ω load		-0.237	-	0.237	V
1:1.26 transformer and 120Ω load		-0.3	-	0.3	V
Load Presented To Transmitter Output	(Note 10)	-	75	-	Ω
Jitter Added by the Transmitter	(Note 15)				
10Hz - 8kHz		-	-	0.01	UI
8kHz - 40kHz		-	-	0.025	UI
10Hz - 40kHz		-	-	0.025	UI
Broad Band		-	-	0.05	UI
Power in 2kHz band about 772kHz	(Notes 10, 16)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 10, 16)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 10, 16)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
E1 Transmitter Return Loss	(Notes 10, 16, 17)				
51 kHz to 102 kHz		20	28	-	dB
102 kHz to 2.048 MHz		20	28	-	dB
2.048 MHz to 3.072 MHz		20	24	-	dB
E1 Transmitter Short Circuit Current	(Notes 10, 18)	-	-	50	mA RMS

Notes: 10. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.

11. Pulse amplitude measured at the output of a 1:1 transformer across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
12. Pulse amplitude measured at the output of a 1:1.26 transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0 or at the output of a 1:1 transformer across a 120 Ω load for LEN2/1/0=0/0/1.
13. Pulse amplitude measured at the output of a 1:1.15 transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
14. Pulse amplitude measured at the DSX-1 Cross-Connect across a 100 Ω load for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1 using a 1:1.5 transformer.
15. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
16. Not production tested. Parameters guaranteed by design and characterization.
17. Return loss = 20 $\log_{10}$ ABS($(z_1 + z_0)/(z_1 - z_0)$) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:2 transformer with two 9.4 Ω series resistors terminated by a 75Ω load, or for LEN2/1/0 = 0/0/1 with a 1:2 transformer and two 15 Ω series resistors terminated by a 120Ω load.
18. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0 or 0/0/1with a 1:2 transformer and the series resistors specified in Table A1.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6	-	-	dB
		500	-	-	mV
Data Decision Threshold					
T1, DSX-1	(Note 19)	60	65	70	% of peak
T1, DSX-1	(Note 20)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 21)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 22)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold	(Note 23)	0.25	0.30	0.50	V
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 16, 24)	-	3	-	Hz
Attenuation at 10kHz Jitter Frequency	(Notes 16, 24)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 16, 24)	138	-	-	UI

Notes:
19. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
20. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
21. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
22. Jitter tolerance increases at lower frequencies. See Figure 11.
23. The analog input squelch circuit shall operate when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V. Operation of the squelch results in the recovery of zeros. During receive LOS, the RPOS, RNEG or RDATA outputs are forced low.
24. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 12. Output jitter can increase significantly when more than 138 UI's are input to the attenuator. See discussion in the text section.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 25)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Note 26)	t_{pwh2}	150	-	500	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 27)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 28)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 29)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 29)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 30)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 31)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 32)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 30)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 31)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 32)	t_{h1}	150	274	-	ns

Notes: 25. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
26. The transmitted pulse width for LEN2/1/0 = 0/0/0 and 0/0/1 does not depend on the TCLK duty cycle.
27. ACLKI provided by an external source or TCLK.
28. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
29. At max load of 1.6 mA and 50 pF.
30. Host Mode (CLKE = 1).
31. Extended Hardware Mode.
32. Hardware Mode, or Host Mode (CLKE = 0).

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 25)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Note 26)	t_{pwh2}	150	-	340	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 27)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 28)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 29)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 29)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 30)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 31)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 32)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 30)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 31)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 32)	t_{h1}	100	194	-	ns

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 33)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

Notes: 33. Output load capacitance = 50pF.

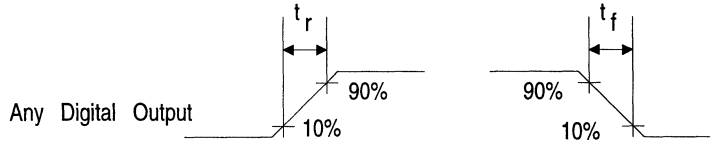


Figure 1. Signal Rise and Fall Characteristics

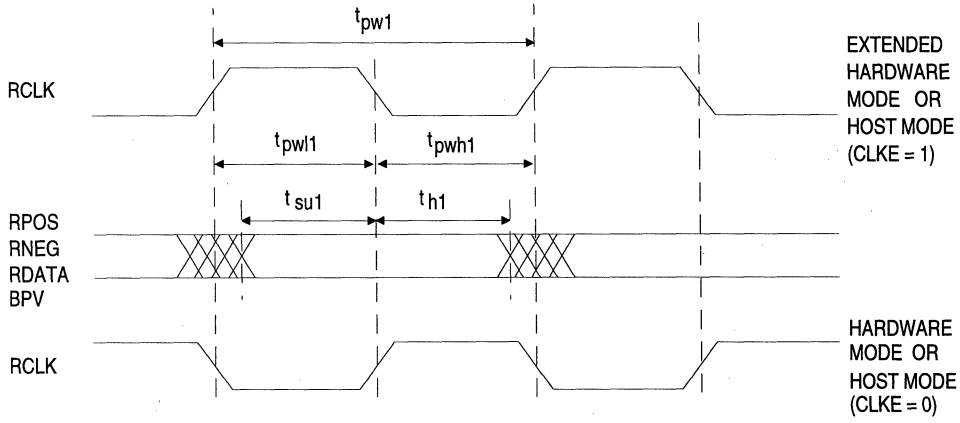


Figure 2. Recovered Clock and Data Switching Characteristics

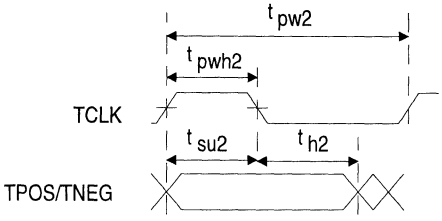


Figure 3a. Transmit Clock and Data Switching Characteristics

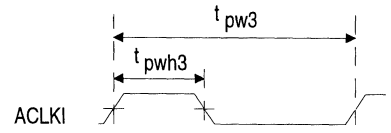


Figure 3b. Alternate External Clock Characteristics

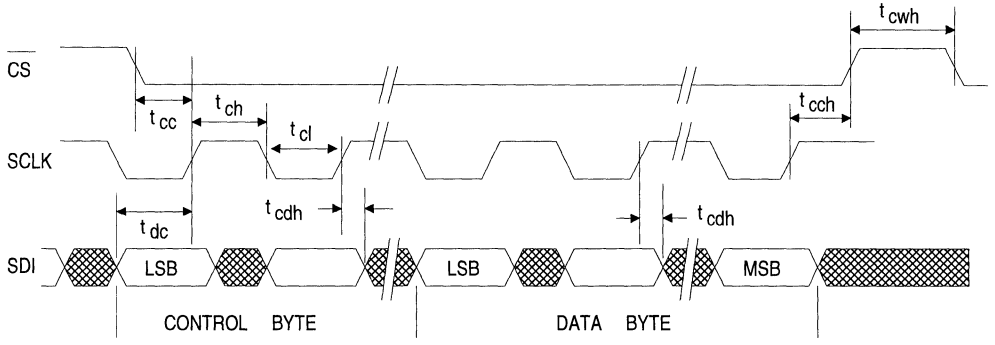


Figure 4. Serial Port Write Timing Diagram

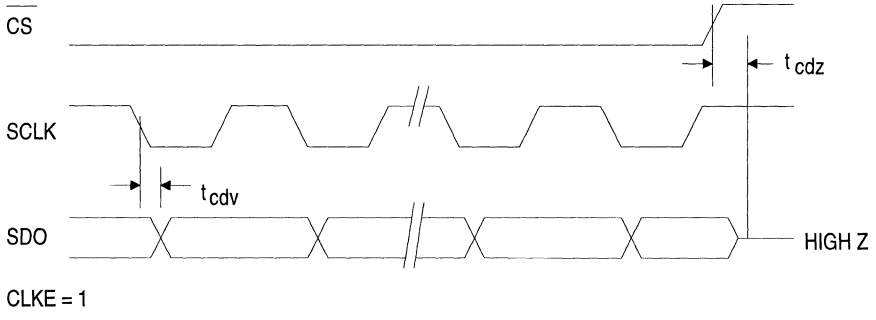


Figure 5. Serial Port Read Timing Diagram

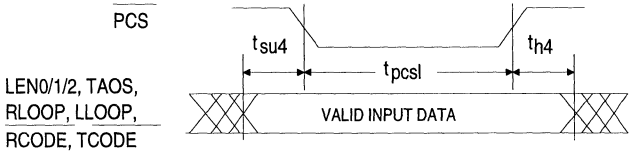


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Key Enhancements of the CS61304A Relative to the LXT304A

- 12.5% Lower Power Consumption,
- 50 mARMS transmitter short-circuit current limiting for E1 (per OFTEL OTR-001),
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- Improved receiver Loss of Signal handling (LOS set at power-up, reset upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros),
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,

Introduction to Operating Modes

The CS61304A supports three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2).

	Hardware Mode	**Extended Hardware Mode**	**Host Mode**
Control Method	Control Pins	Control Pins with Parallel Chip Select	Serial Interface
MODE Pin Level	<0.2 V	Floating or 2.5 V	>(RV+)-0.2 V
Line Coding	External	Internal-AMI, B8ZS, or HDB3	External
AIS Detection	No	Yes	No
Driver Performance Monitor	Yes	No	Yes

Table 1. Differences Between Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

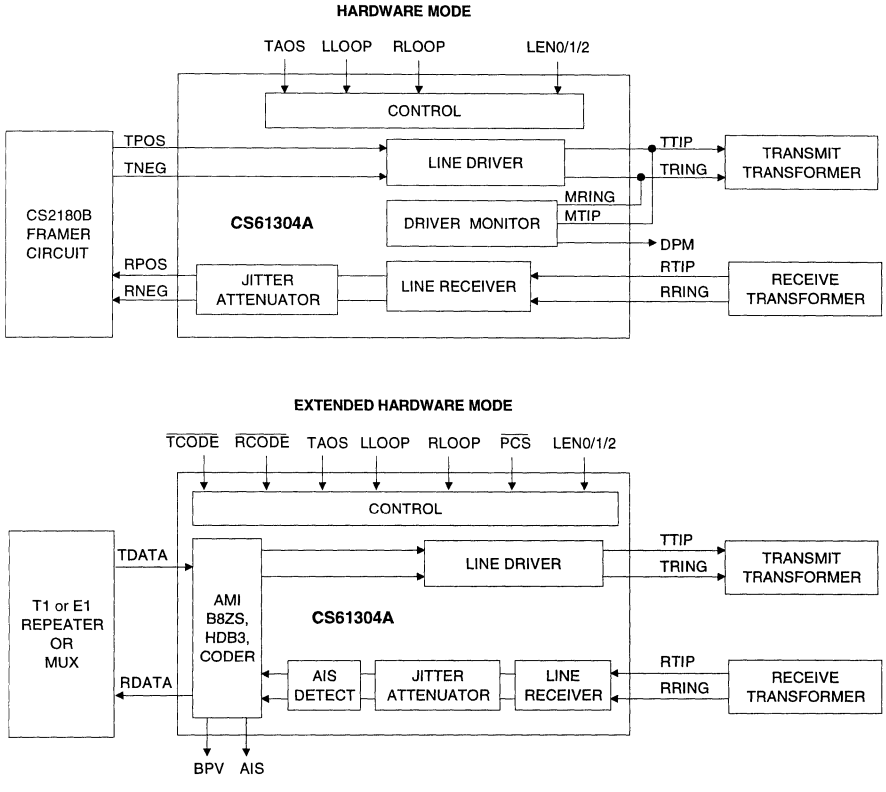


Figure 7. Overview of Operating Modes

Transmitter

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3. The output options in Table 3 are specified with a 1:1.15 transmitter transformer turns ratio for T1 and a 1:1 turns ratio for E1 without external series resistors. Other turns ratios may be used if approriate resistors are placed in series with the TTIP and TRING pins. Table A1 in the applications section lists other combinations which can be used to provide transmitter impedance matching.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61304A automatically adjusts the pulse width based upon the "line length" selection made.

The E1 G.703 pulse shape is supported with line length selections LEN2/1/0 = 0/0/0 and 0/0/1. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 ft	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 ft	
1	0	1	266-399 ft	
1	1	0	399-533 ft	
1	1	1	533-655 ft	
0	0	0	75Ω coax	E1 CCITT G.703
0	0	1	120Ω twisted-pair	
0	1	0	FCC PART 68, OPT. A	Network Interface
0	1	1	ECSAT1C1.2	

Table 3. Line Length Selection

The CS61304A transmitter provides short-circuit current limiting protection and meets OFTEL OTR-001 short-circuit current limiting requirements for E1 applications.

The CS61304A will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

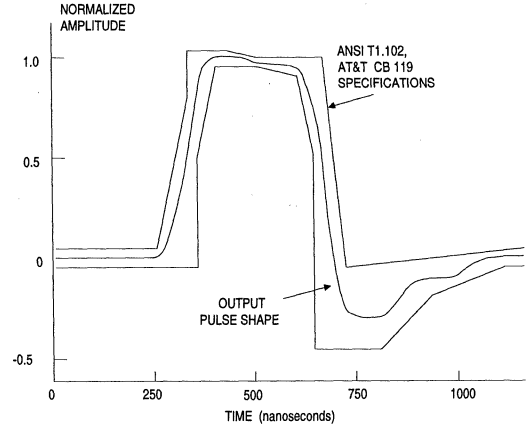


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

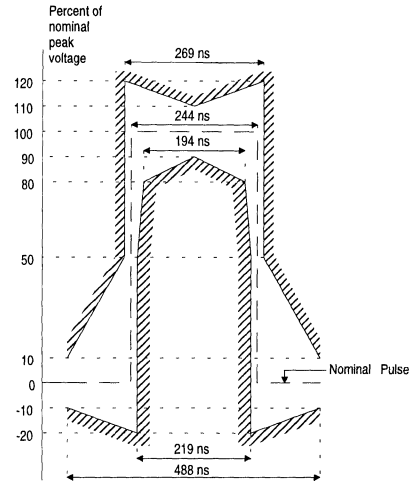


Figure 9. Mask of the Pulse at the 2048 kbps Interface

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, AT&T 62411, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 10. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The out-

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

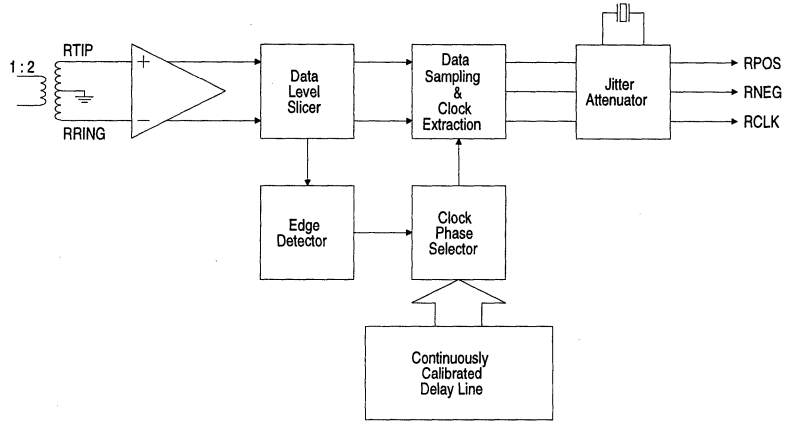


Figure 10. Receiver Block Diagram

put from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 11. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated using the crystal oscillator reference clock. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

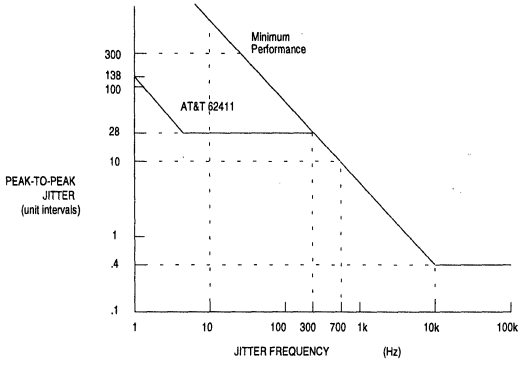


Figure 11. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

In the Hardware Mode, data at RPOS and RNEG should be sampled on the rising edge of RCLK, the recovered clock. In the Extended Hardware Mode, data at RDATA should be sampled on the falling edge of RCLK. In the Host Mode, CLKE determines the clock polarity for which output data should be sampled as shown in Table 5.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2v)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2 V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2 V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5v)	X	RDATA	RCLK	Falling

X= Don't care

Table 5. Data Output/Clock Relationship

Loss of Signal

The receiver will indicate loss of signal after power-up, reset or upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. A zero is received when the RTIP and RRING inputs are below the input comparator slicing threshold level established by the peak detector. After the signal is removed for a period of time the data slicing threshold level decays to approximately 300 mV_{peak}.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$ (unless disabled). LOS will return low (asserting the $\overline{INT}$ pin again in Host Mode) upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12. RPOS/RNEG or RDATA are forced low during LOS unless the jitter attenuator is disabled. (See "Jitter Attenuator")

If ACLKI is present during the LOS state, ACLKI is switched into the input of the jitter attenuator, resulting in RCLK matching the frequency of ACLKI. The jitter attenuator buffers any instantaneous changes in phase between the last recovered clock and the ACLKI reference clock. This means that RCLK will smoothly transition to the new frequency. If ACLKI is not present, then the crystal oscillator of the jitter attenuator is forced to its center frequency. Table 6 shows the status of RCLK upon LOS.

Crystal present?	ACLKI present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	ACLKI via the Jitter Attenuator

Table 6. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 12. The CS61304A fully meets AT&T 62411 jitter attenuation requirements.

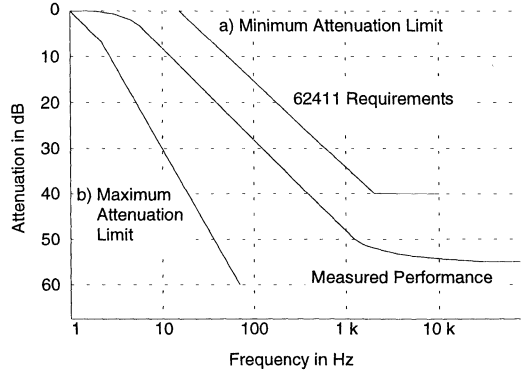


Figure 12. Typical Jitter Transfer Function

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG (or RDATA). The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to prevent overflow and underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent data loss from overflow or underflow.

The jitter attenuator may be bypassed by pulling XTALIN to RV+ through a 1 kΩ resistor and providing a 1.544 MHz (or 2.048 MHz) clock on ACLKI. RCLK may exhibit quantization jitter of approximately 1/13 UIpp and a duty cycle of approximately 30% (70%) when the attenuator is disabled.

Local Loopback

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG (or RDATA). If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

Remote Loopback

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 7). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{\text{RCODE}}$ is low.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from both the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance.

Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when less than 3 zeros are detected out of 2048 bit periods. AIS returns low when 4 or more zeros, out of 2048 bits, are detected.

Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

Parallel Chip Select

In the Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

An address/command byte, shown in Table 9, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 9. Address/Command Byte

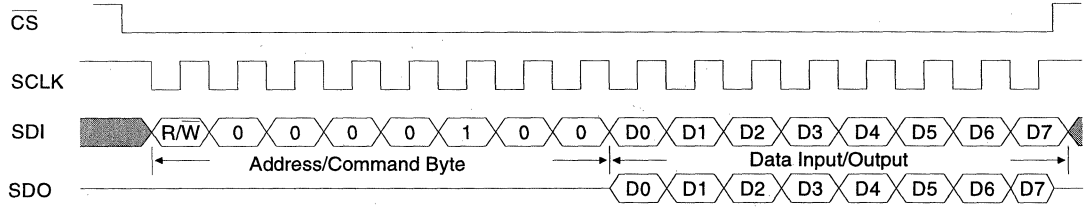


Figure 13. Input/Output Timing

The data register, shown in Table 10, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

Table 10. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 11 and 12. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermittent loss of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 11. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Coding for Serial Output bits 5,6,7

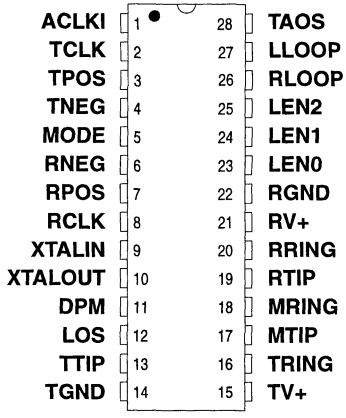
Power Supply

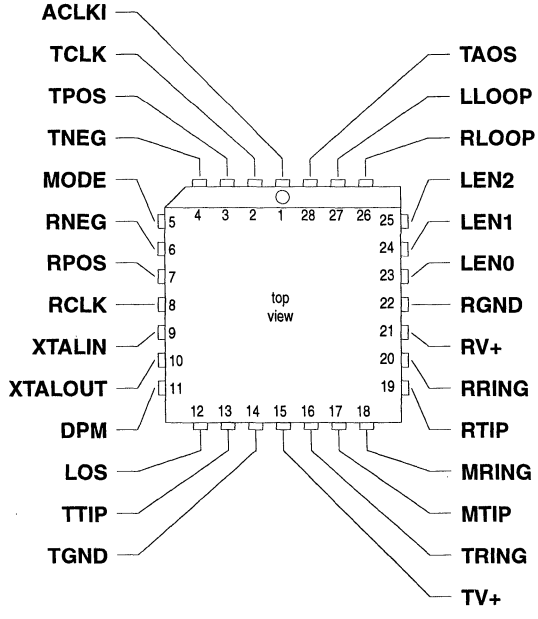
The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

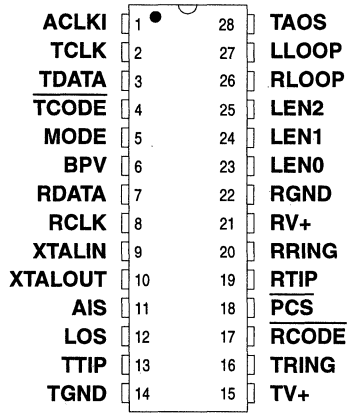
PIN DESCRIPTIONS

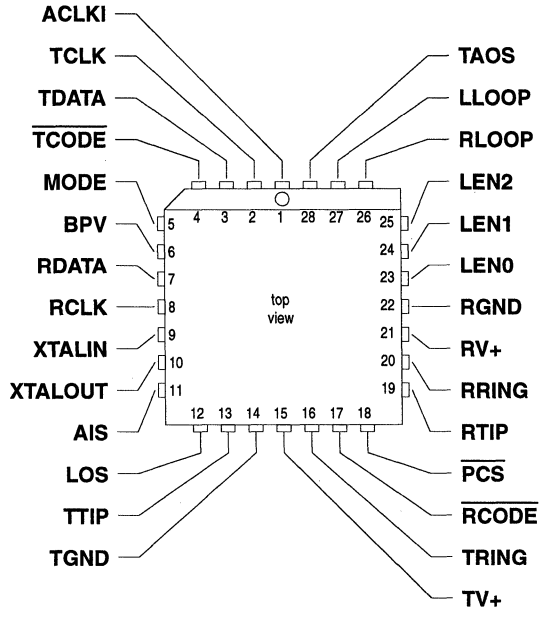
Hardware Mode



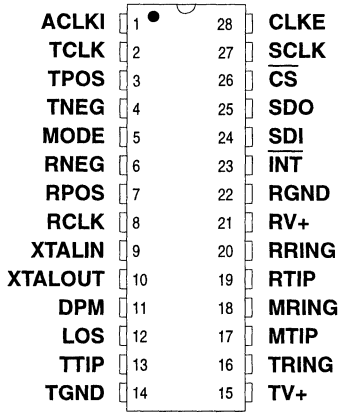


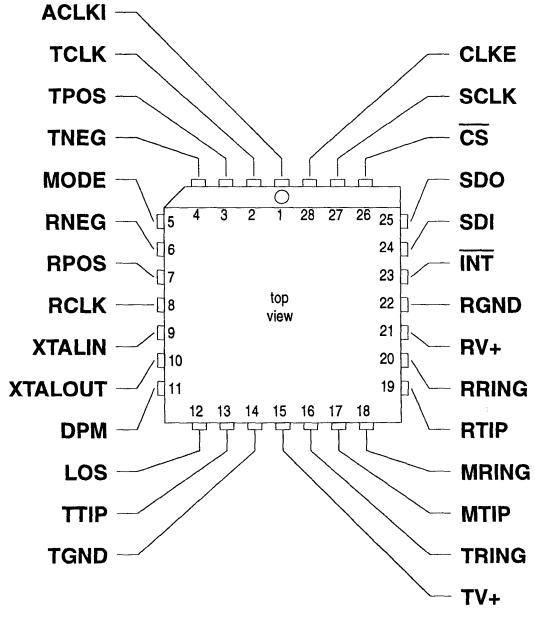
Extended Hardware Mode





Host Mode


ACLKI 1
TCLK 2
TPOS 3
TNEG 4
MODE 5
RNEG 6
RPOS 7
RCLK 8
XTALIN 9
XTALOUT 10
DPM 11
LOS 12
TTIP 13
TGND 14
28 CLKE
27 SCLK
26 CS
25 SDO
24 SDI
23 INT
22 RGND
21 RV+
20 RRING
19 RTIP
18 MRING
17 MTIP
16 TRING
15 TV+


ACLKI
TCLK
TPOS
TNEG
MODE
RNEG
RPOS
RCLK
XTALIN
XTALOUT
DPM
LOS
TTIP
TGND
CLKE
SCLK
CS
SDO
SDI
INT
RGND
RV+
RRING
RTIP
MRING
MTIP
TRING
TV+
top
view

Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Overdriving the oscillator with an external clock is not supported.

Control

ACLKI - Alternate External Clock Input, Pin 1.
A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground. During LOS, the ACLKI input signal, if present, is output on RCLK through the jitter attenuator.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

CS - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)
Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the line interface in the Host Mode. In the host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 V selects the Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ high causes the line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin.When in the loss of signal state ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator.

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. The transmitter output is designed to drive a 75 Ω load between TTIP and TRING. A transformer is required as shown in Table A1.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than three zeros out of 2048 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)

BPV goes high for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low when 3 ones are received within 32 bit periods with no more than 15 consecutive zeros. When in the loss of signal state RPOS/RNEG or RDATA are forced low, and ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the $\overline{\text{INT}}$ pin in the Host mode is used, and the monitor is not used, writing a 1 to the "clear DPM" bit will prevent an interrupt from the driver performance monitor.

APPLICATIONS

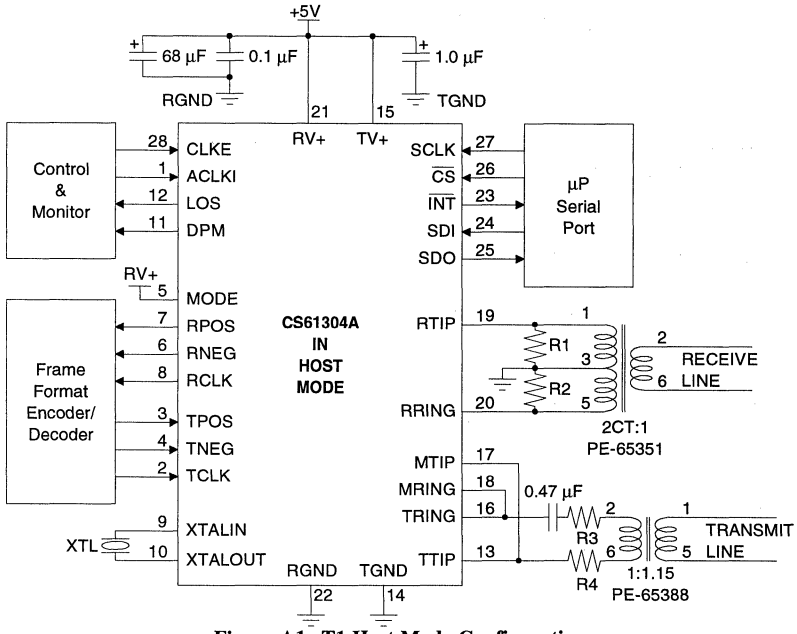


Figure A1. T1 Host Mode Configuration

Frequency MHz	Crystal XTL	Cable Ω	R1 and R2 Ω	LEN2/1/0	Transmit Transformer	R3 and R4 Ω	Typical TX Return Loss dB
1.544 (T1)	CXT6176	100	200	0/1/1 - 1/1/1	1:1.15	0	0.5
					1:2	9.4	20
					1:2.3	9.4	28
2.048 (E1)	CXT8192	120	240	0/0/0	1:1.26	0	0.5
				0/0/0	1:2	8.7	12
				0/0/1	1:1	0	0.5
				0/0/1	1:2	15	30
		75	150	0/0/0	1:1	0	0.5
				0/0/0	1:2	9.4	24
				0/0/1	1:1	10	5
				0/0/1	1:2	14.3	12

Table A1. External Component Values

Line Interface

Figures A1-A3 show typical T1 and E1 line interface application circuits. Table A1 shows the external components which are specific to each application. Figure A1 illustrates a T1 interface in the Host Mode. Figure A2 illustrates a 120 Ω E1 interface in the Hardware Mode. Figure A3 illustrates a 75 Ω E1 interface in the Extended Hardware Mode.

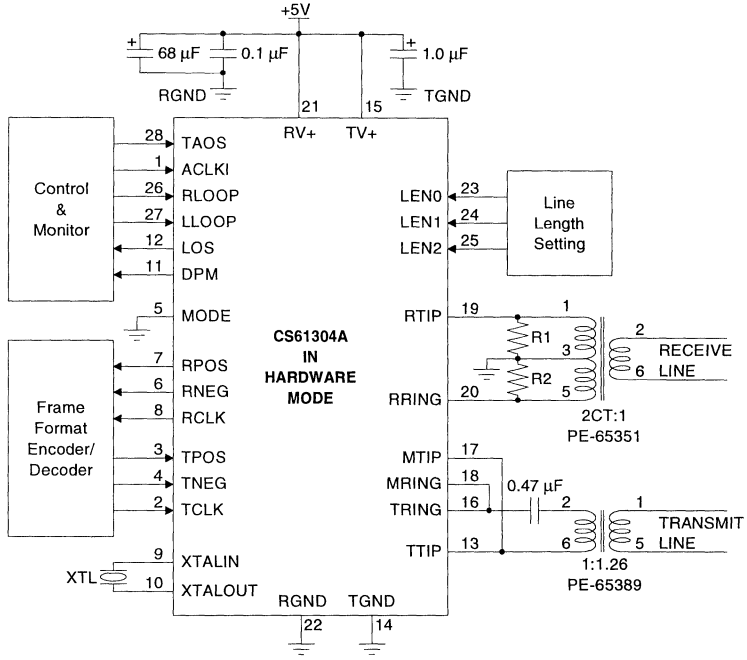


Figure A2. 120 Ω, E1 Hardware Mode Configuration

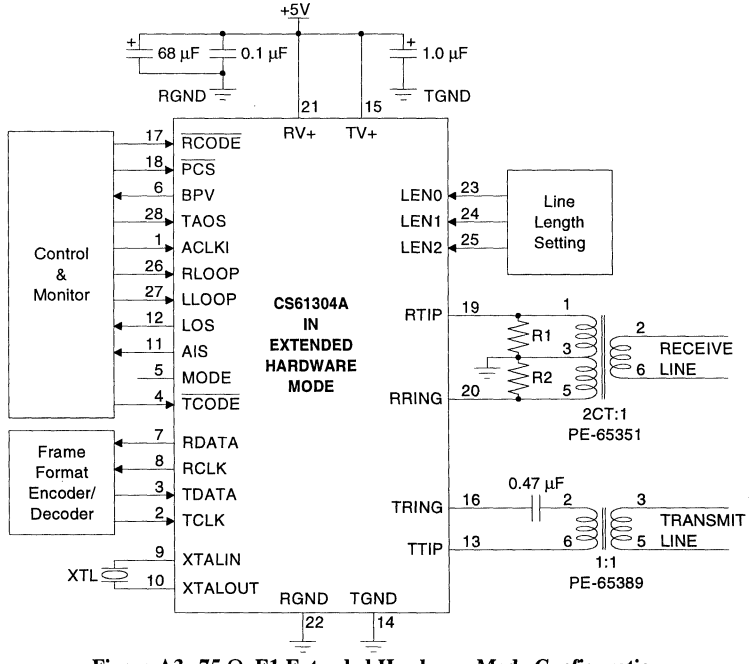


Figure A3. 75 Ω, E1 Extended Hardware Mode Configuration

Parameter	Receiver	Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 120 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 75 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

The receiver transformer has a grounded center tap on the IC side. Resistors between the RTIP and RRING pins to ground provide the termination for the receive line.

The transmitter transformer matches the 75 Ω transmitter output impedance to the line impedance. Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 are recommended for use with the CS61304A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Designing for AT&T 62411

For additional information on the requirements of AT&T 62411 and the design of an appropriate system synchronizer, please refer to the Crystal Semiconductor Application Notes: "AT&T 62411 Design Considerations – Jitter and Synchronization" and "Jitter Testing Procedures for Compliance with AT&T 62411".

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61304A in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the "Telecom Line Protection Application Note" for detailed information on the different electrical safety standards and specific application circuit recommendations.

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

Interfacing The CS61304A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A4. In this case, the line interface and CS2180B are in Host Mode controlled by a microprocessor serial interface. If the line interface is used in Hardware Mode, then the line interface RCLK output must be inverted before being input to the CS2180B. If the CS61304A is used in Extended Hardware Mode, the RCLK output does not have to be inverted before being input to the CS2180B.

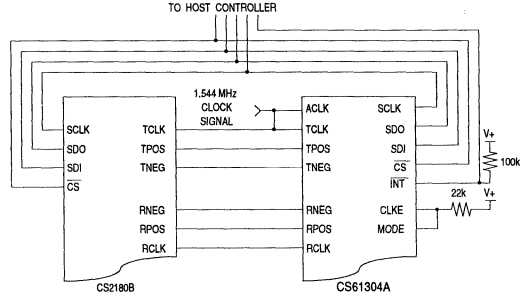


Figure A4. Interfacing the CS61304A with a CS2180B (Host Mode)

• *Notes* •

A Cirrus Logic Company

CS61305A

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 3 Hz, with > 300 UI of Jitter Tolerance
- B8ZS/HDB3/AMI Encoders/Decoders
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes
- 50 mA Transmitter Short-Circuit Current Limiting

General Description

The CS61305A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61305A is a pin-compatible replacement for the LXT305A in most applications.

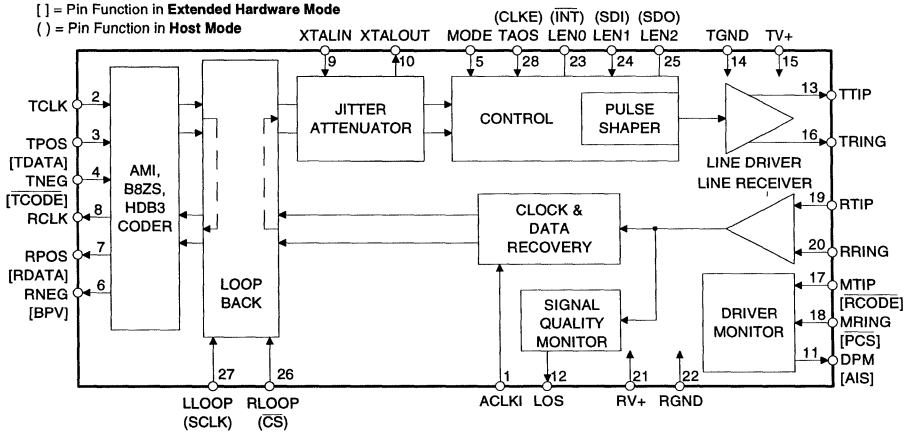
The CS61305A provides a transmitter jitter attenuator making it ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The transmitter features internal pulse shaping and a low impedance output stage allowing the use of external resistors for transmitter impedance matching. The receiver uses a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.

ORDERING INFORMATION

CS61305A-IP1	28 Pin Plastic DIP
CS61305A-IL1	28 Pin Plastic PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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(512) 445-7222 FAX:(512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to RGND=TGND=0V)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption (Notes 4,5)	P_C	-	-	350	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 6, 7) PINS 1-4, 17, 18, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 6, 7) PINS 1-4, 17, 18, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 6, 7, 8) I_{OUT} = -400 µA PINS 6-8, 11, 12, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 6, 7, 8) I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	µA
Low-Level Input Voltage, PIN 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5	V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5 (Note 9)	V_{IM}	2.3	-	2.7	V

Notes:
6. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate digital output.
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. Output drivers will drive CMOS logic levels into a CMOS load.
9. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 10)				
E1, 75 Ω	(Note 11)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 12)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 13)	2.7	3.0	3.3	V
T1, DSX-1	(Note 14)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 000)					
1:1 transformer and 75Ω load		-0.237	-	0.237	V
1:1.26 transformer and 120Ω load		-0.3	-	0.3	V
Load Presented To Transmitter Output	(Note 10)	-	75	-	Ω
Jitter Added by the Transmitter	(Note 15)				
10Hz - 8kHz		-	-	0.01	UI
8kHz - 40kHz		-	-	0.025	UI
10Hz - 40kHz		-	-	0.025	UI
Broad Band		-	-	0.05	UI
Power in 2kHz band about 772kHz	(Notes 10, 16)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 10, 16)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 10, 16)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
E1 Transmitter Return Loss	(Notes 10, 16, 17)				
51 kHz to 102 kHz		20	28	-	dB
102 kHz to 2.048 MHz		20	28	-	dB
2.048 MHz to 3.072 MHz		20	24	-	dB
E1 Transmitter Short Circuit Current	(Notes 10, 18)	-	-	50	mA RMS

Notes: 10. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.

11. Pulse amplitude measured at the output of a 1:1 transformer across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.

12. Pulse amplitude measured at the output of a 1:1.26 transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0 or at the output of a 1:1 transformer across a 120 Ω load for LEN2/1/0 = 001.

13. Pulse amplitude measured at the output of a 1:1.15 transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.

14. Pulse amplitude measured at the DSX-1 Cross-Connect across a 100 Ω load for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1 using a 1:1.5 transformer.

15. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.

16. Not production tested. Parameters guaranteed by design and characterization.

17. Return loss = 20 $\log_{10}$ ABS($(z_1 + z_0)/(z_1 - z_0)$) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:2 transformer with two 9.4 Ω series resistors terminated by a 75Ω load, or for LEN2/1/0 = 0/0/1 with a 1:2 transformer and two 15 Ω series resistors terminated by a 120Ω load.

18. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0 or 0/0/1with a 1:2 transformer and the series resistors specified in Table A1.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 16, 19)	-	3	-	Hz
Attenuation at 10kHz Jitter Frequency	(Notes 16, 19)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 16, 19)	12	23	-	UI
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6 500	- -	- -	dB mV
Data Decision Threshold					
T1, DSX-1	(Note 20)	53	65	77	% of peak
T1, (FCC Part 68) and E1	(Note 21)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 22)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold		-	0.30	-	V

Notes: 19. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 10. Output jitter can increase significantly when more than 12 UI's are input to the attenuator. See discussion in the text section.

20. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
21. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
22. Jitter tolerance increases at lower frequencies. See Figure 12.

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 23)	f_c	-	8.192000	-	MHz
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 24)	f_{aclki}	-	2.048	-	MHz
RCLK Cycle Width	(Note 25)	t_{pw1} t_{pwh1} t_{pwl1}	310 90 120	488 140 348	620 190 500	ns ns ns
Rise Time, All Digital Outputs	(Note 26)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 26)	t_f	-	-	85	ns
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Notes 27, 28) (Note 29)	t_{pwh2}	80 150	- -	- 340	ns ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 27)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 29)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 28)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 27)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 29)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 28)	t_{h1}	100	194	-	ns

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 23)	f_c	-	6.176000	-	MHz
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 24)	f_{aclki}	-	1.544	-	MHz
RCLK Cycle Width	(Note 25)	t_{pw1}	320	648	980	ns
		t_{pwh1}	130	190	240	ns
		t_{pwl1}	100	458	850	ns
Rise Time, All Digital Outputs	(Note 26)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 26)	t_f	-	-	85	ns
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Notes 27, 28)	t_{pwh2}	80	-	-	ns
	(Note 29)		150	-	500	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 27)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 29)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 28)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 27)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 29)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 28)	t_{h1}	150	274	-	ns

Notes: 23. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
24. ACLKI provided by an external source or TCLK but not RCLK.
25. RCLK duty cycle will vary with extent by which pulses are displaced by jitter. Specified under worst case jitter conditions: 0.4 UI AMI data displacement for T1 and 0.2 UI AMI data displacement for E1.
26. At max load of 1.6 mA and 50 pF.
27. Host Mode (CLKE = 1).
28. Hardware Mode, or Host Mode (CLKE = 0).
29. Extended Hardware Mode.

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 30)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

Notes: 30. Output load capacitance = 50pF.

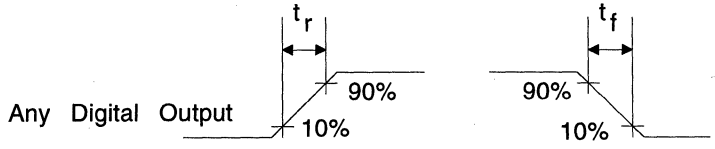


Figure 1. Signal Rise and Fall Characteristics

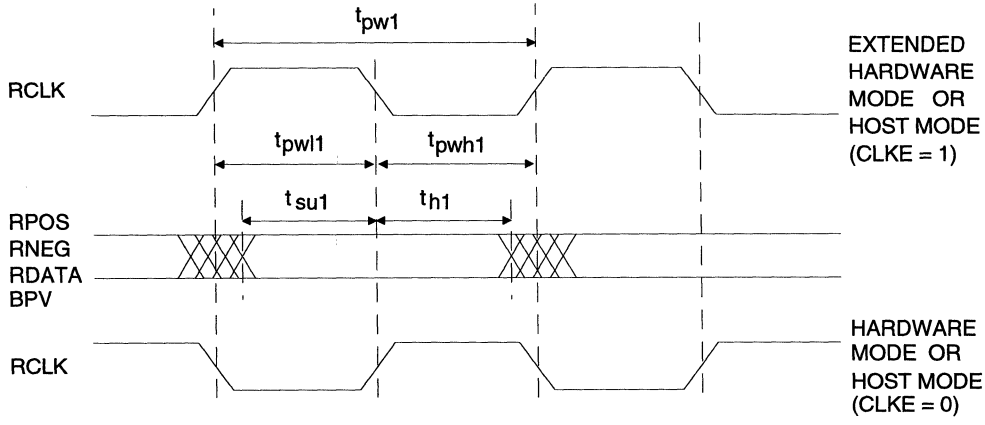


Figure 2. Recovered Clock and Data Switching Characteristics

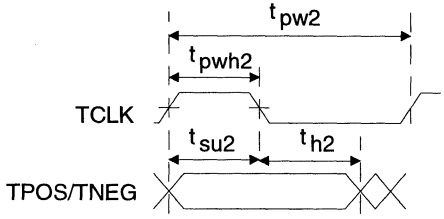


Figure 3a. Transmit Clock and Data Switching Characteristics

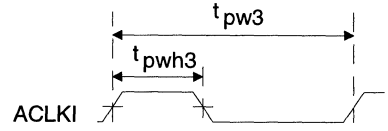


Figure 3b. Alternate External Clock Characteristics

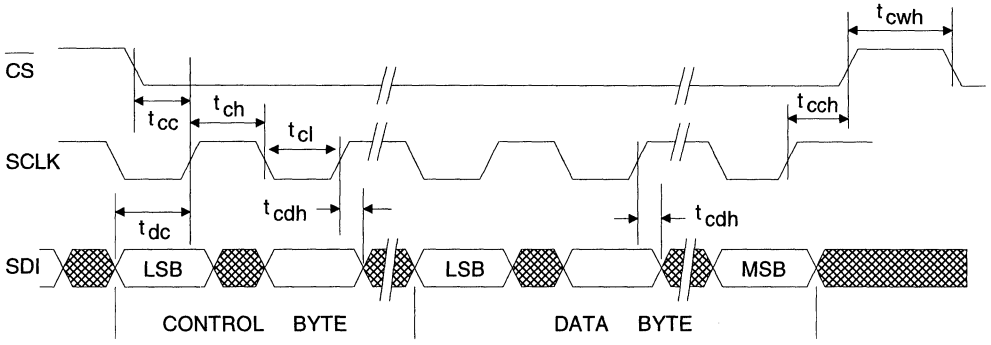


Figure 4. Serial Port Write Timing Diagram

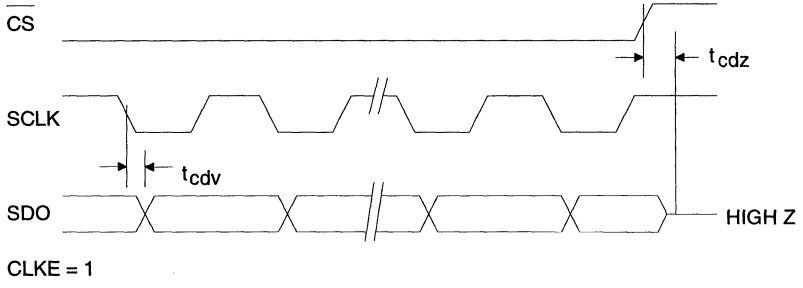


Figure 5. Serial Port Read Timing Diagram

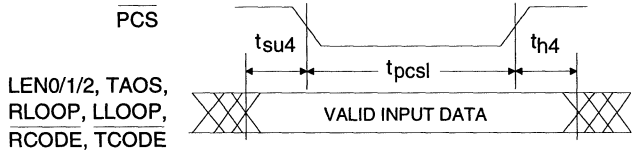


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Key Enhancements of the CS61305A Relative to the LXT305A

- 12.5% lower power consumption,
- 50 mA_{RMS} transmitter short-circuit current limiting for E1 (per OFTEL OTR-001),
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- Improved receiver Loss of Signal handling (LOS set at power-up, reset upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros),
- Transmitter TTIP and TRING outputs are forced low when TCLK is static.

Introduction to Operating Modes

The CS61305A supports three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2). The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface.

	Hardware Mode	**Extended Hardware Mode**	**Host Mode**
Control Method	Control Pins	Control Pins with Parallel Chip Select	Serial Interface
MODE Pin Level	<0.2 V	Floating or 2.5 V	>(RV+)-0.2 V
Line Coding	External	Internal-AMI, B8ZS, or HDB3	External
AIS Detection	No	Yes	No
Driver Performance Monitor	Yes	No	Yes

Table 1. Differences Between Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

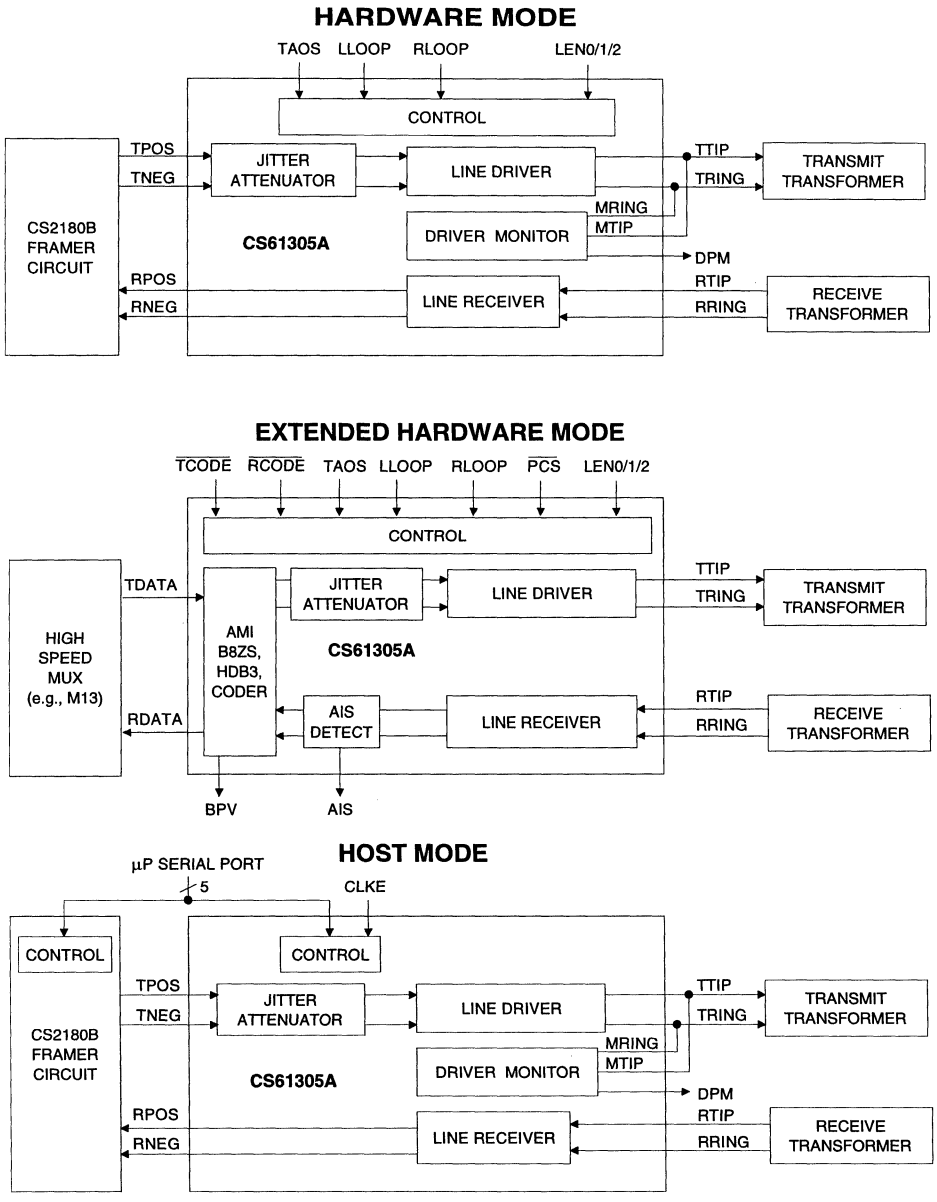


Figure 7. Overview of Operating Modes

Transmitter

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3. The output options in Table 3 are specified with a 1:1.15 transmitter transformer turns ratio for T1 and a 1:1 turns ratio for E1 without external series resistors. Other turns ratios may be used if approriate resistors are placed in series with the TTIP and TRING pins. Table A1 in the applications section lists other combinations which can be used to provide transmitter impedance matching.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102-1993 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61305A automatically adjusts the pulse width based upon the "line length" selection made.

The E1 G.703 pulse shape is supported with line length selections LEN2/1/0 = 0/0/0 and 0/0/1. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 ft	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 ft	
1	0	1	266-399 ft	
1	1	0	399-533 ft	
1	1	1	533-655 ft	
0	0	0	75Ω coax	E1 CCITT G.703
0	0	1	120Ω twisted-pair	
0	1	0	FCC PART 68, OPT. A	Network Interface
0	1	1	ECSAT1C1.2	

Table 3. Line Length Selection

The CS61305A transmitter provides short-circuit current limiting protection and meets OFTEL OTR-001 short-circuit current limiting requirements for E1 applications.

The CS61305A will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

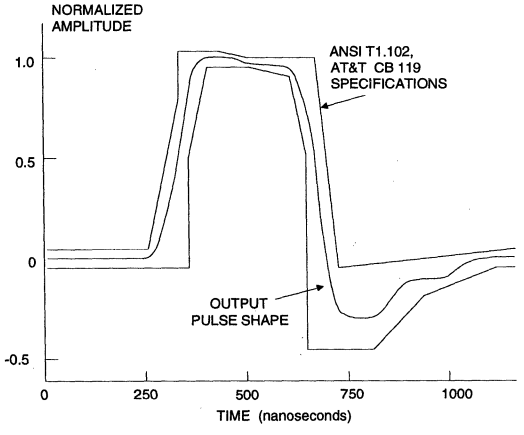


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

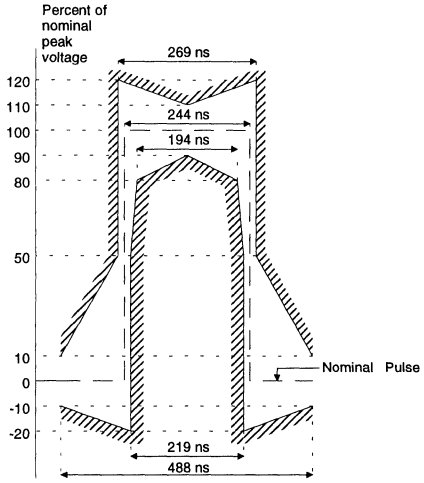


Figure 9. Mask of the Pulse at the 2048 kbps Interface

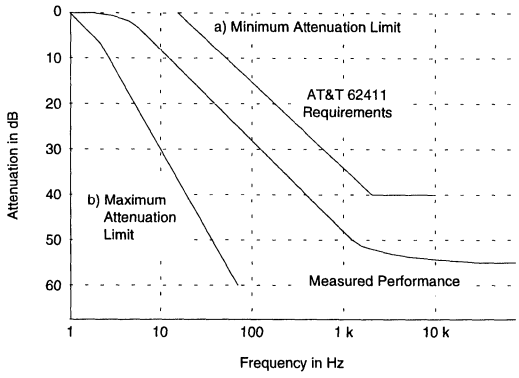


Figure 10. Typical Jitter Attenuation Curve

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of ACLKI. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. A TAOS request will be ignored if remote loopback is in effect. ACLKI jitter will be attenuated. TAOS is not available on the CS61305A when ACLKI is grounded.

Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the transmit clock signal. It consists of a 192 bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 10.

The jitter attenuator works in the following manner. Data on TPOS and TNEG (or TDATA) are

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

written into the jitter attenuator's FIFO by TCLK. The rate at which data is read out of the FIFO and transmitted is determined by the oscillator. Logic circuits adjust the capacitive loading on the crystal to set its oscillation frequency to the average of the TCLK frequency. Signal jitter is absorbed in the FIFO.

Jitter Tolerance of Jitter Attenuator

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should the pointers attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. When a divide by 3 1/2 or 4 1/2 occurs, the data bit will be driven on to the line either an eighth bit period early or an eighth bit period late.

The FIFO of the jitter attenuator in the transmit path is 192 bits deep. This FIFO will typically be near the half full point under normal operating conditions, buffering about 96 bits of data. The number of bits actually buffered depends on the relationship of the nominal TCLK frequency to the center frequency of the crystal oscillator. As these frequencies deviate, a few bits of FIFO depth will be lost.

TCLK can have gaps or bursts. As long as the gap or burst is less than the remaining FIFO depth, normal operation will continue. For example, if the nominal TCLK frequency was less than the oscillator's center frequency by 40 Hz. The FIFO will operate 3-4 bits off center or 92 bits full. A gap in TCLK of 80 cycles would empty the FIFO by 80 bits but would still not envoke the divide by 4 1/2 circuitry, as about 12 bits would remain in the FIFO.

The crystal frequency must be 4 times the nominal signal frequency: 6.176 MHz for 1.544 MHz operation; 8.192 MHz for 2.048 MHz applications. Internal capacitors load the crystal, controlling the oscillation frequency. The crystal must be designed so that over operating temperature, the oscillator frequency range exceeds the system frequency tolerance. Crystal Semiconductor offers the CXT6176 & CXT8192 crystals, which yield optimum performance with the CS61305A.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 11. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI or the jitter attenuator's oscillator, into 13 equal divisions or phases. Continuous calibration assures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The out-

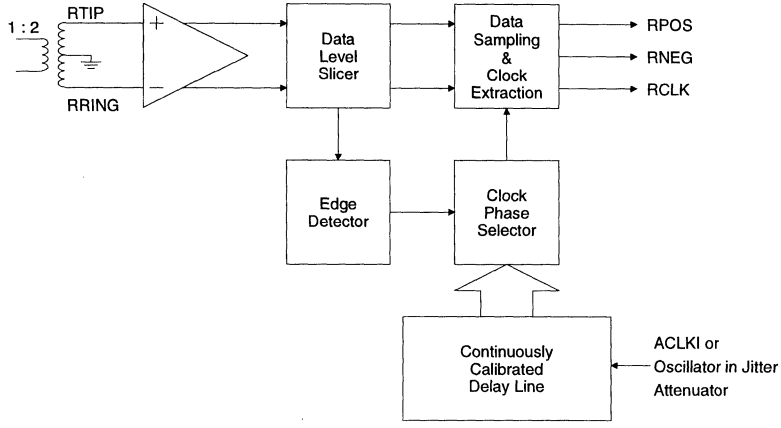


Figure 11. Receiver Block Diagram

put from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that shown in Figure 12.

The CS61305A outputs a clock immediately upon power-up and will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

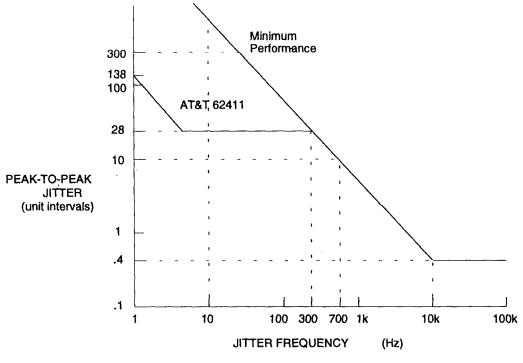


Figure 12. Minimum Input Jitter Tolerance of Receiver

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Extended Hardware Mode, data at RDATA is stable and may be sampled on the fallings edge of the recovered clock. In the Host Mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

Jitter and Recovered Clock

The CS61305A is designed for error free clock and data recovery from an AMI encoded data

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5V)	X	RDATA	RCLK	Falling

X = Don't care

Table 5. Data Output/Clock Relationship

stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until a data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UIpp. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation the instantaneous period can be 14/13 * 648 ns = 698 ns or 12/13 * 648 ns = 598 ns when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the E1 rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. The data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS61305A is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns. For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns.

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt issued on INT. LOS will go low (and flag the INT pin again if serial I/O is used) when a valid signal is detected. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12.

In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. LOS returns to logic zero when 3 ones are received out of 32 bit periods containing no more than 15 consecutive zeros. Also, a power-up or manual reset will set LOS high.

Local Loopback

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), and outputs it at RCLK, RPOS and RNEG (or RDATA). Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect. The jitter attenuator is not in the local loop back path.

Remote Loopback

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 7). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes: 1. X = Don't Care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{\text{RCODE}}$ is low.

Driver Performance Monitor

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from both the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when unframed all-ones condition (blue alarm) is detected using the criteria of less than 3 zeros out of 2048 bit periods.

Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

Parallel Chip Select

In the Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI, or the crystal oscillator. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function eliminates any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a

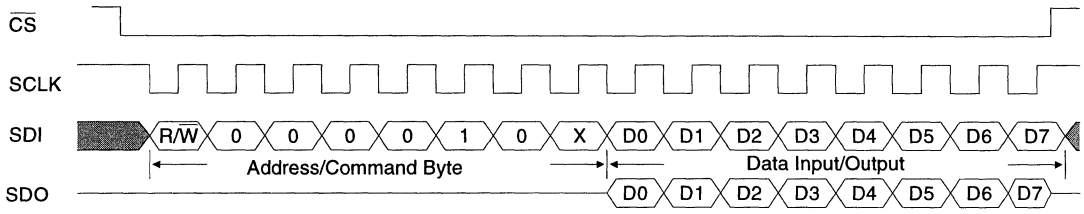


Figure 13. Input/Output Timing

host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes to the high impedance state when the serial port is being written ($R/\overline{W}$ = 0), or if $\overline{CS}$ goes high, or at the end of the hold period of data bit D7.

An address/command byte, shown in Table 9, precedes the data byte. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

Bit	Designation	Description
0	$R/\overline{W}$	Read/Write Select; 0 = write, 1 = read
1	ADD0	LSB of address, Must be 0
2	ADD1	Must be 0
3	ADD2	Must be 0
4	ADD3	Must be 0
5	ADD4	Must be 1
6	-	Reserved - Must be 0
7	X	Don't Care

Note: Bit 0 is the first bit input (LSB).

Table 9. Address/Command Byte

During a write cycle ($R/\overline{W}$ = 0), data is written to the input data register on the eight clock cycles immediately following the address/command byte. The input data format over SDI is shown in Table 10.

Bit	Designation	Description
D0	clr LOS	Clear Loss of Signal
D1	clr DPM	Clear Driver Performance Monitor
D2	LEN0	Bit 0 - Line Length Select
D3	LEN1	Bit 1 - Line Length Select
D4	LEN2	Bit 2 - Line Lenght Select
D5	RLOOP	Remote Loopback
D6	LLOOP	Local Loopback
D7	TAOS	Transmit All Ones Select

Note: Bit D0 is the first bit input (LSB).

Table 10. Input Data Register

Bits D0 and D1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits D5, D6 and D7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Bit	Designation	Description
D0	LOS	Loss of Signal
D1	DPM	Driver Performance Monitor
D2	LEN0	Bit 0 - Line Length Select
D3	LEN1	Bit 1 - Line Length Select
D4	LEN2	Bit 2 - Line Lenght Select

Note: Bit D0 is the first bit output (LSB)

Table 11. Output Data Register (bits D0-D4)

During a read cycle ($R/\overline{W}$ = 1), data is read from the output data register on the eight clock cycles immediately following the address/ command byte. The output data format over SDO is shown in Tables 11 and 12.

Bits D2, D3 and D4 can be read to verify line length selection. Bits D5, D6 and D7 must be decoded according to Table 12. Codes 101, 110 and 111 (Bits D5, D6 and D7) indicate intermittent losses of signal and/or driver problems.

The SDO pin goes to a high impedance state when not in use. The SDO and SDI pins may be tied together in applications where the host processor has a bi-directional I/O port.

Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit (TV+, TGND) and receive (RV+, RGND) supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Bits D5 D6 D7	Status
0 0 0	Reset has occurred or no program input.
0 0 1	TAOS in effect.
0 1 0	LLOOP in effect.
0 1 1	TAOS/LLOOP in effect.
1 0 0	RLOOP in effect
1 0 1	DPM changed state since last "clear DPM" occured.
1 1 0	LOS changed state since last "clear LOS" occured.
1 1 1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Output Data Register (bits D5-D7)

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

Extended Hardware	*Hardware/Host*		*Hardware*	*Extended Hardware*	*Host*
	ACLKI	1	TAOS		CLKE
	TCLK	2	LLOOP		SCLK
TDATA	TPOS	3	RLOOP		$\overline{CS}$
TCODE	TNEG	4	LEN2		SDO
	MODE	5	LEN1		SDI
BPV	RNEG	6	LEN0		$\overline{INT}$
RDATA	RPOS	7	RGND		
	RCLK	8	RV+		
	XTALIN	9	RRING		
	XTALOUT	10	RTIP		
AIS	DPM	11	MRING	$\overline{PCS}$	
	LOS	12	MTIP	$\overline{RCODE}$	
	TTIP	13	TRING		
	TGND	14	TV+		

DIP top view

Extended Hardware	*Hardware/Host*		*Hardware*	*Extended Hardware*	*Host*
	ACLKI	5	TAOS		CLKE
	TCLK	6	LLOOP		SCLK
TDATA	TPOS	7	RLOOP		$\overline{CS}$
TCODE	TNEG	8	LEN2		SDO
	MODE	9	LEN1		SDI
BPV	RNEG	10	LEN0		$\overline{INT}$
RDATA	RPOS	11	RGND		
	RCLK	12	RV+		
	XTALIN	13	RRING		
	XTALOUT	14	RTIP		
AIS	DPM	15	MRING	$\overline{PCS}$	
	LOS	16	MTIP	$\overline{RCODE}$	
	TTIP	17	TRING		
	TGND	18	TV+		

PLCC top view

Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (T1 operation) or 8.192 MHz (E1 operation) crystal should be connected across these pins. Overdriving the oscillator with an external clock is not supported.

Control

ACLKI - Alternate External Clock Input, Pin 1.
A 1.544 MHz or 2.048 MHz clock signal may be input on ACLKI to calibrate the clock recovery circuit and control the transmit clock during TAOS. If a clock is not provided on ACLKI, this input must be grounded, and the oscillator in the jitter attenuator is used to calibrate the clock recovery circuit and TAOS is not available. ACLKI may not be provided by RCLK.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

CS - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

INT - Receive Alarm Interrupt, Pin 23. (Host Mode)
Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor (47k - 100k).

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. These pins also control the receiver slicing level.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through to the receive clock and data pins. TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored during LLOOP. The jitter attenuator is bypassed.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

MODE - Mode Select, Pin 5.

Driving the MODE pin high places the line interface in the Host Mode. In the Host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin places the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 V places the device in Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

PCS - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ low causes the line interface to accept the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

RCODE - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Input for the input data register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control output from the output data register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written, or if $\overline{CS}$ is high, or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLKI.

TCODE - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{TCODE}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{TCODE}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock is output on this pin.

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output in NRZ format at this pin, after being decoded by the line code decoder. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data from RTIP and RRING is output on these pins. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse (with respect to ground) received on the RRING pin generates a logic 1 on RNEG. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid (see Table 5).

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input on these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 of the *Applications* section. Clock and data are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (T1 operation) or 2.048 MHz (E1 operation) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Data to be transmitted by the TTIP and TRING outputs is input in NRZ format at this pin, after being encoded by the line code encoder. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

The transmit NRZ digital data to TTIP and TRING is input on these pins. A logic 1 on TPOS causes a positive pulse (with respect to ground) to be transmitted on the TTIP pin, and a logic 1 on TNEG causes a negative pulse (with respect to ground) to be transmitted on the TRING pin. TPOS and TNEG are sampled on the falling edge of TCLK.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 75 Ω load. A transformer is required as shown in Figure A1 of the *Applications* section. Clock and data are sourced on TCLK and TPOS/ TNEG or TDATA.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than three zeros out of 2048 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)

BPV goes high for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low when 3 ones are received within 32 bit periods containing no more than 15 consecutive zeros.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

These pins are normally connected to TTIP and TRING and monitor the transmitter output. If the $\overline{\text{INT}}$ pin in the Host mode is used, and the monitor is not used, writing a "1" to the "clear DPM" bit will prevent an interrupt from the driver performance monitor.

APPLICATIONS

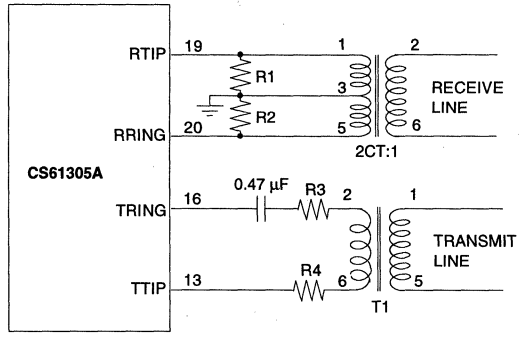


Figure A1. Line Interface Circuitry

Frequency MHz	Crystal XTL	Cable Ω	R1 and R2 Ω	LEN2/1/0	T1 turns ratio	R3 and R4 Ω	Typical TX Return Loss (dB)
1.544 (T1)	CXT6176	100	200	0/1/1 - 1/1/1	1:1.15	0	0.5
					1:2	9.4	20
					1:2.3	9.4	28
2.048 (E1)	CXT8192	120	240	0/0/0	1:1.26	0	0.5
				0/0/0	1:2	8.7	12
				0/0/1	1:1	0	0.5
				0/0/1	1:2	15	30
		75	150	0/0/0	1:1	0	0.5
				0/0/0	1:2	9.4	24
				0/0/1	1:1	10	5
				0/0/1	1:2	14.3	12

Note: Refer to Table A3 for specific transformer recommendations.

Table A1. External Component Values

Line Interface

Figure A1 illustrates the external components for the line interface circuitry and Table A1 shows the specific components for each application. Figures A2-A4 show typical T1 and E1 line interface application circuits. Figure A2 illustrates a T1 interface in the Host Mode. Figure A3 illustrates a 120 Ω E1 interface in the Hardware Mode. Figure A4 illustrates a 75 Ω E1 interface in the Extended Hardware Mode.

The receiver transformer has a grounded center tap on the IC side. Resistors between the RTIP and RRING pins to ground provide the termination for the receive line.

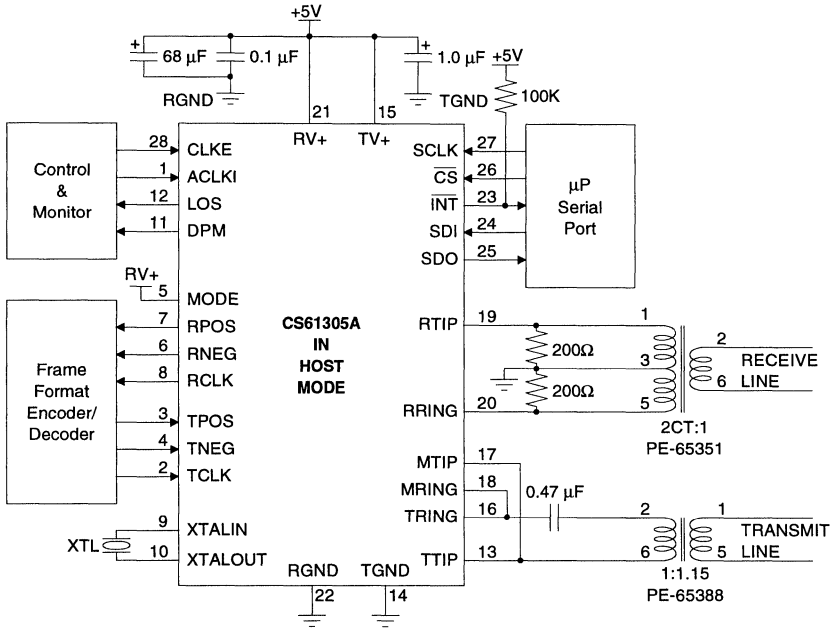


Figure A2. T1 Host Mode Configuration

Figures A2-A4 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 are recommended for use with the CS61305A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the Application Note "Secondary Line Protection for T1 and E1 Line Cards" for detailed information on the different electrical safety standards and specific application circuit recommendations.

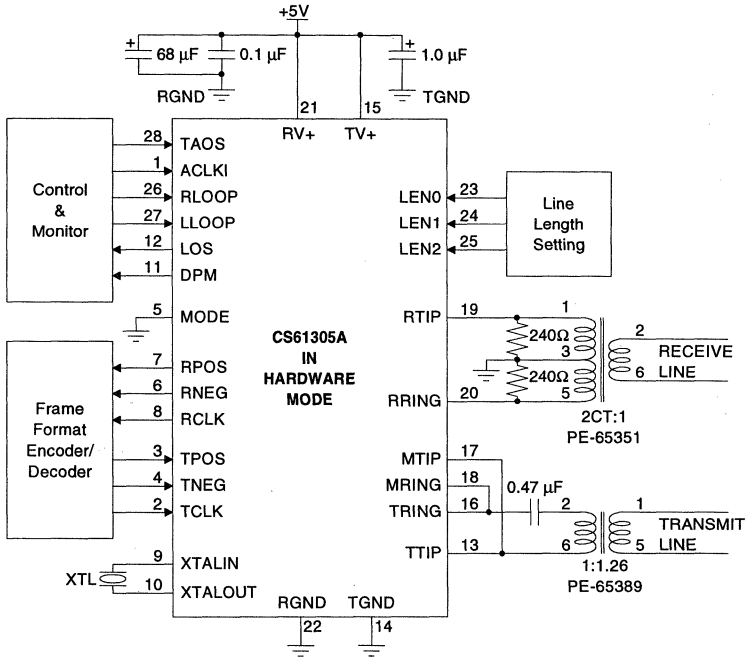


Figure A3. 120 Ω, E1 Hardware Mode Configuration

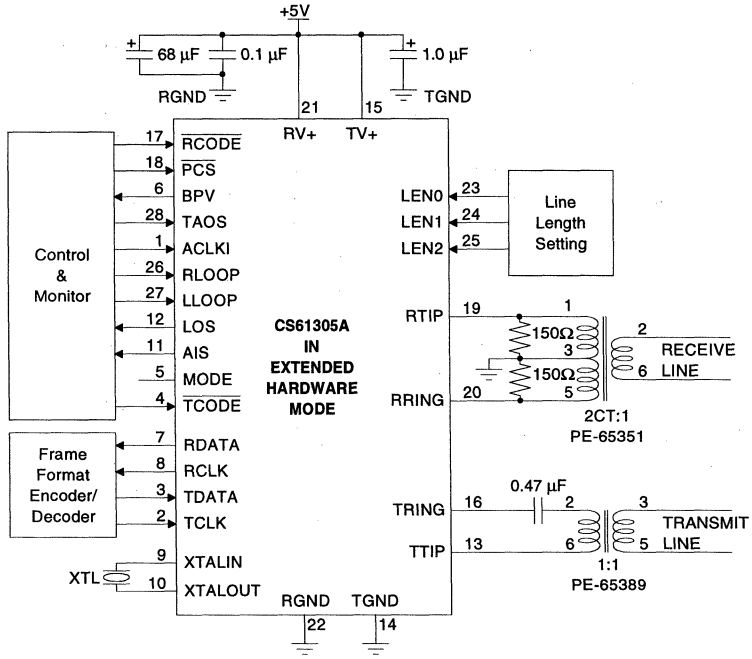


Figure A4. 75 Ω, E1 Extended Hardware Mode Configuration

Parameter	Receiver	Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 120 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 75 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Interfacing The CS61305A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A5. In this case, the line interface and CS2180B are in Host mode controlled by a microprocessor serial interface. If the line interface is used in Hardware mode, then the line interface RCLK output must be inverted before being input to the CS2180B. If the CS61305A is used in Extended Hardware Mode, the RCLK output does not have to be inverted before being input to the CS2180B.

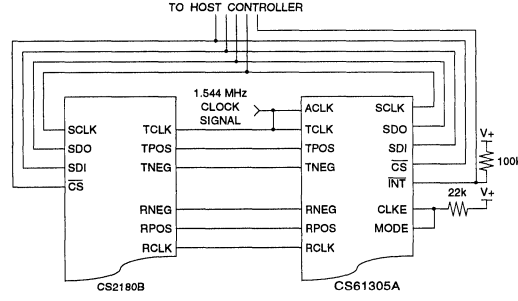


Figure A5. Interfacing the CS61305A with a CS2180B (Host Mode)

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

• Notes •

• Notes •

Semiconductor Corporation

CS6152

Low Power T1 Analog Interface

Features

- Provides Analog T1 Line Interface
- Low Power Consumption (normally 180 mW)
- SMART *Analog* ™ Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer Which Compliments Digital Gate Array Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components

General Description

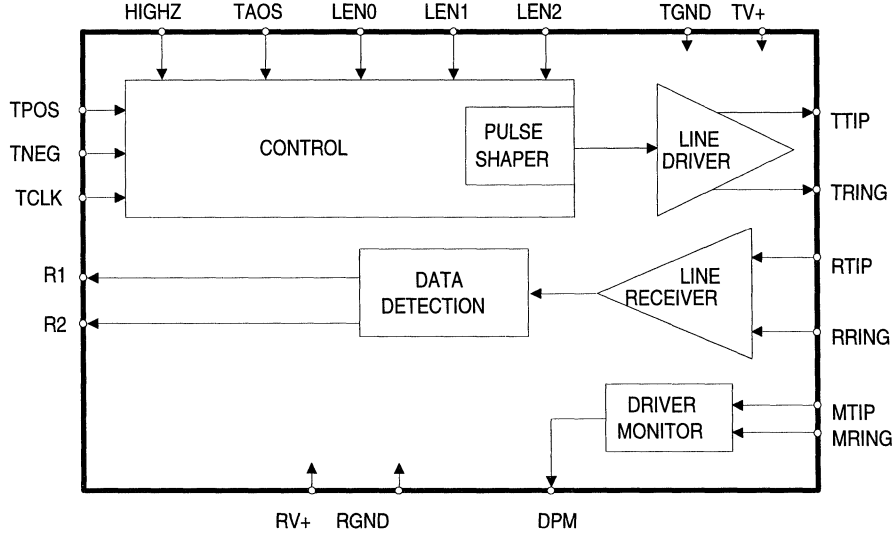
The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

Applications

- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexors, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152A-IP - 24 Pin Plastic, 300 mil DIP
CS6152-IL - 28 Pin J-lead PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	(RGND) - 0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, MTIP, and MRING, which must stay within a range of -6V to (RV+)+0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Notes 4 and 5) 100% ones density & max. line length @ 5.25V	P_D	-	-	350	mW
Normal Power Dissipation (Notes 4 and 5) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	180	-	mW
Normal Power Dissipation (Notes 5 and 6) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	145	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 54 Ω load over operating temperature range. Includes CS6152 and load.
5. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
6. Power dissipation internal to CS6152 while driving 54 Ω load over operating temperature range.

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS: TCLK, TPOS, TNEG, HIGHZ, LEN0/1/2, TAOS	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 7) I_{OUT} = ±4 mA; PINS: R1, R2, DPM	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 7) I_{OUT} = ±4 mA; PINS: R1, R2, DPM	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	µA
3-State Leakage Current PINS: R1, R2, DPM	I_{OZ}	-	-	±10	µA

Notes: 7. Output drivers are high speed CMOS compatible.

ANALOG SPECIFICATIONS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes Line Length Selections LEN2/1/0 = 0/0/0 (Measured at transformer output)		2.7	3.0	3.3	V
All line length settings except, LEN2/1/0 = 0/0/0; 0/0/1; 0/1/0 (Measured at the DSX; Nomalization factor for Figure 4)		2.4	3.0	3.6	V
Load Presented to Transmitter Output		-	54	-	Ω
Jitter Added by the Transmitter (Note 8)					
10Hz - 8kHz		-	0.005	-	UI
8kHz - 10kHz		-	0.008	-	UI
10HZ - 40kHz		-	0.010	-	UI
Broad Band		-	0.015	-	UI
Power in 2kHz band at 772kHz (Note 9)		12.6	15	17.9	dBm
Difference in power in 2kHz band at 1.544MHz to power in 2 kHz band at 772kHz (Note 9)		-29	-40	-	dB
Positive to Negative Pulse Imbalance (Note 9)		-	0.2	0.5	dB
Receiver					
Input Signal Squelch Level (Note 10)		-	0.5	-	mV
Data Decision Threshold Squelch Level < RTIP/RRING < 4.14 V		65	70	75	% of peak

Notes: 8. Input signal to TCLK is jitter free.
9. Measured with a nonpolarized 0.47 µF capacitor in series with the primary of the transmit transformer. Not production tested. Parameters guaranteed by design and characterization.
10. The squelch circuit operates when the DSX-1 receiver input signal amplitude falls below approximately 500 mVp, Operation of the squelch circuit causes R1 and R2 to remain low.

T1 SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Frequency	f_{in}	-	1.544	-	MHz
RTIP/RRING Rising to R1/R2 Rising (Note 11)	t_{dr}	20	45	150	ns
RTIP/RRING Falling to R1/R2 Falling (Note 11)	t_{df}	60	135	370	ns
Rise Time, All Digital Outputs (Note 12)	t_r	-	-	30	ns
Fall Time, All Digital Outputs (Note 12)	t_f	-	-	30	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_h	50	-	-	ns

Notes: 11. Both rising and falling delays will exhibit similiar tendencies, that is, for fast process, times will tend towards minimum delay times; slower process results in longer delays.
12. At max load of 4.0 mA and 50 pF.

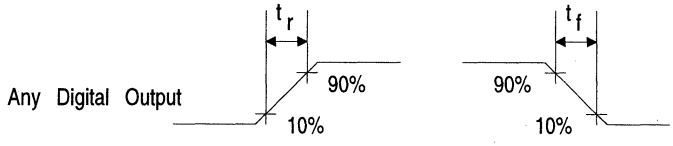


Figure 1. - Signal Rise and Fall Characteristics

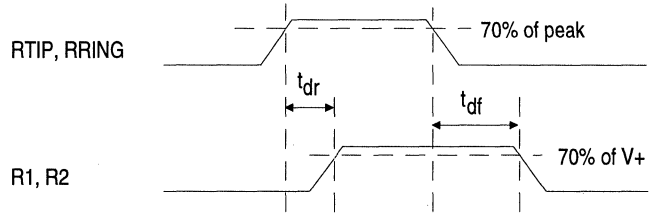


Figure 2. - Receiver Switching Characteristics

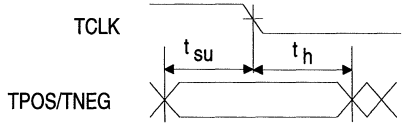


Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS6152 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 Volt supply, a 1:1.36, step-up transformer is required. The line driver is designed to drive a 54 Ω equivalent load.

When any transmit control pin (TAOS or LEN0/1/2) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter options are: HIGHZ which places TTIP, TRING, R1, and R2 in a high impedance state, and TAOS which transmits an AMI-encoded all ones on TTIP/TRING.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. These phases are then used to trigger different portions of the output waveform. The line length selection offers a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS6152 modifies the output pulse to meet the requirements of Compatibility Bulletin 119. The exact pulse shape achieved at the DSX-1 can be effected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	APPLICATION
0	1	1	0-133	DSX-1 ABAM (AT&T 600B Or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	1		Reserved
0	1	0		
0	0	0	Part 68, Option A	CSU
0	1	1	T1C1.2	

Table 1 - Line Length Selection

The T1 CSU pulse shapes meet FCC Part 68 for 0dB line build out and future ECSA T1C1.2 pulse shapes as shown in Table 1.

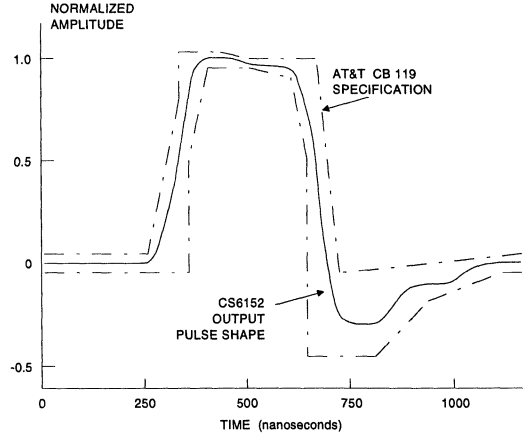


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6152 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will transition high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV within 64±2 TCLK cycles. If TCLK stops, DPM can not change state. The driver performance monitor is not designed to detect transmitted bipolar violations or broken printed circuit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING. DPM should be averaged externally in hardware or software for approximately 500 ms to filter short events caused by very low ones density.

Whenever more than one CS6152 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS6152 monitor performance of a neighboring CS6152 device, rather than having it monitor its own performance.

Receiver

The receiver converts AMI (Alternate Mark Inversion) coded signals to binary (dual unipolar) data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators detect pulses on RTIP and RRING. The comparators switching threshold is dynamically established to be approximately 70% of the peak signal level. The comparator outputs are output on R1 and R2 respectively. A positive pulse on RTIP results in a positive pulse on R1. A positive pulse on RRING results in a positive pulse on R2. The pulses are stretched by approximately 90 ns before being output on R1 and R2.

Squelch control in the receiver will force R1 and R2 low if the inputs on RTIP and RRING are below the squelch level of approximately 0.5 Volts.

Power On Reset

Upon power-up, the CS6152 is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this happens, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay line used in the transmit section commences. The delay line can be calibrated only if the transmit clock is present. The initial calibration should take less than 20 ms after TCLK is applied.

In operation, the delay line is continuously calibrated, making the performance of the device independent of power supply or temperature variations, and eliminating the need to reset a CS6152 when in operation.

Power Supply

The device operates from a single 5 Volt supply. Decoupling and filtering of the power supplies is crucial for proper operation of the analog circuits in the transmit and receive paths. Separate pins for transmit and receive supplies provide internal isolation. TV+ should be connected to RV+ externally and each power supply pin should be

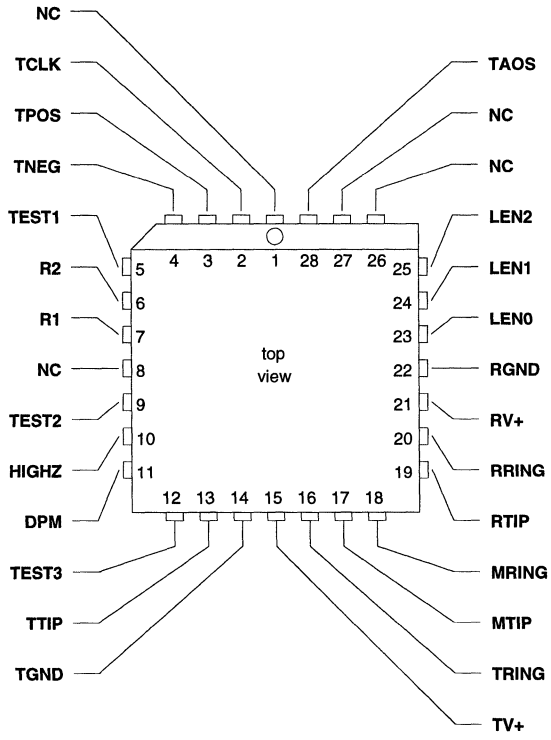
decoupled to its respective ground. TV+ must not exceed RV+ by more than 0.3V.

A 1µF capacitor should be connected between TV+ and TGND, and a 0.1µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire wrap bread-boarding of the CS6152 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

TRANSMIT CLOCK	**TCLK**	1	24	**TAOS**	TRANSMIT ALL ONES SELECT
TRANSMIT POSITIVE PULSE	**TPOS**	2	23	**LEN2**	BIT 2 OF LINE LENGTH SELECT
TRANSMIT NEGATIVE PULSE	**TNEG**	3	22	**LEN1**	BIT 1 OF LINE LENGTH SELECT
FACTORY TEST1	**TEST1**	4	21	**LEN0**	BIT 0 OF LINE LENGTH SELECT
RECEIVED SIGNAL 2	**R2**	5	20	**RGND**	RECEIVE GROUND
RECEIVED SIGNAL 1	**R1**	6	19	**RV+**	RECEIVE V+ (+5VDC)
FACTORY TEST2	**TEST2**	7	18	**RRING**	RECEIVE RING
HIGH IMPEDANCE	**HIGHZ**	8	17	**RTIP**	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	**DPM**	9	16	**MRING**	MONITORED RING
FACTORY TEST3	**TEST3**	10	15	**MTIP**	MONITORED TIP
TRANSMIT TIP	**TTIP**	11	14	**TRING**	TRANSMIT RING
TRANSMIT GROUND	**TGND**	12	13	**TV+**	TRANSMIT V+ (+5VDC)

24-Pin DIP



28-Pin PLCC

Power Supplies

TV+ - Positive Power Supply, Transmit Drivers.
Positive power supply for the transmit drivers; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers.
Power supply ground for the transmit drivers; typically 0 Volts.

RV+ - Positive Power Supply.
Positive power supply for the device, except transmit drivers; typically +5 Volts.

RGND - Ground.
Power supply ground for the device, except transmit drivers; typically 0 Volts.

Control

HIGHZ - High Impedance.
Setting HIGHZ to a logic 1 causes TTIP, TRING, DPM, R1, and R2 to enter a high impedance state. This pin is internally pulled down, so the device will be in normal operating mode if this pin is left floating.

TAOS - Transmit All Ones Select.
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

LEN0, LEN1, LEN2 - Line Length Selection.
Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TEST1, TEST2, TEST3 - Factory Test1, 2, 3.
Reserved for factory testing, TEST1 must be tied low for normal operation. TEST2 and TEST3 should be left floating.

Inputs

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data.
Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted. If the clock signal is removed from TCLK, then TPOS and TNEG should both be logic low during last falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring.
The AMI receive signal is input to these pins. A center-tapped, center-grounded, 1:2, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data is buffered and output on R1 and R2.

MTIP, MRING - Monitored Tip, Monitored Ring.
These pins are normally connected to TTIP and TRING and monitor the output of a CS6152. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

DPM - Driver Performance Monitor.

If no signal is present on MTIP and MRING for between 31 to 63 clock cycles, DPM goes to a logic 1 until the first detected signal. If TCLK is static, DPM cannot change state.

Outputs

TTIP, TRING - Transmit Tip, Transmit Ring.

The AMI signal is driven to the line through these pins. This output is designed to drive a 54 Ω load. A 1.36:1 step-up transformer is required as shown in Figure A1.

R1, R2 - Received Signal 1, Received Signal 2.

RTIP and RRING inputs are buffered and stretched before being output digitally on R1 and R2 respectively.

Miscellaneous

NC - No Connection (PLCC package only) Pins, 1, 8, 26, 27.

APPLICATIONS

Line Interface

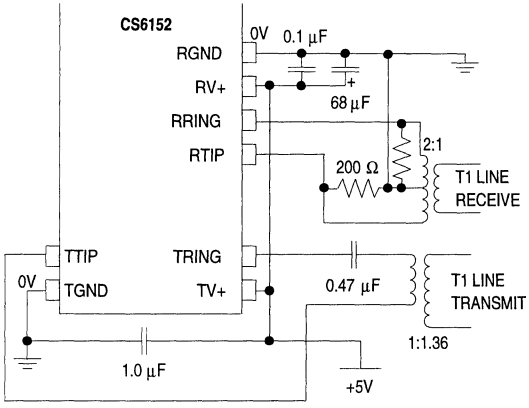


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS6152 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS6152 side. These resistors provide the 100 Ω termination for the T1 line.

To save on power consumption under normal operating conditions, the line driver outputs, TTIP and TRING, are forced into a high impedance state during the transmission of a space (zero) on to the line. Just prior to transmitting a mark (one), the driver outputs are enabled. The transformer interacting with the driver can cause a slight voltage difference (< 200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

Transformers

Transformers listed below have been found to be suitable for use with the CS6152. Receive transformer specifications are not as critical.

Manufacturer	Part#
Transmit + Receive	
Pulse Engineering	PE-64952
Bel Fuse	0553-0013-2J
Transmitter	
Schott	67130240
Midcom	671-5961
Pulse Engineering	PE-65586
Bel Fuse	0553-0013-YC
Receiver	
Pulse Engineering	PE-65351
Schott	67129300
Midcom	671-5832
Bel Fuse	0553-0013-HC

A 1:1.36 turns ratio transformer is required for the transmit side. The receiver side transformer is normally 1:2 turns ratio. However, the receiver side transformer can be 1:1.36 if it is necessary to have only 1 type of transformer, at the expense of a few dB of receive sensitivity. The input squelch level of the CS6152 is set at 0.5 V, with a 1:2 transformer. Using a 1:1.36 transformer will lower the effective squelch level.

Semiconductor Corporation

CDB6152

Evaluation Board for CS6152

Features

- Socketed CS6152 Line Interface IC
- All Required Components for Complete Line Interface Evaluation
- DIP Switch Configuration of all CS6152 Control Inputs
- LED Status Indicator for CS6152 Driver Performance Monitor Output

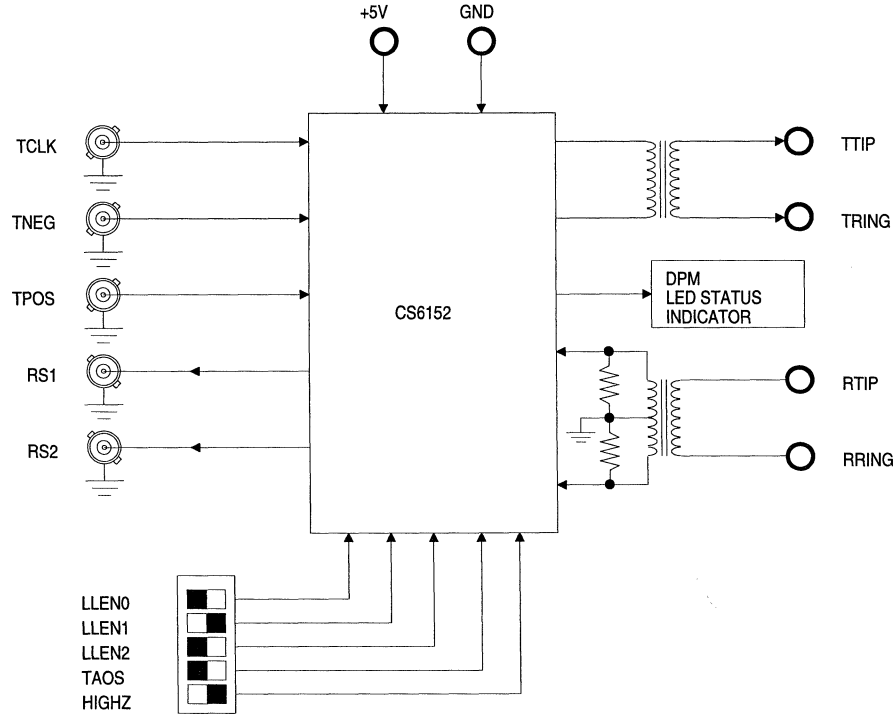
General Description

The evaluation board includes a CS6152 line interface IC and all support components required for evaluation. The board is powered by an external 5 Volt supply.

The board features four binding post connectors for connecting two 100Ω twisted pair T1 lines to the transformers on the board. BNC connectors allow easy access to the digital transmit clock and data inputs and the digital receiver data outputs.

An LED status indicator is provided for monitoring the CS6152's Driver Performance Monitor (DPM) output. A DIP switch is provided for configuring the CS6152's control input pins: LEN0, LEN1, LEN2, TAOS, and HIGHZ.

ORDERING INFORMATION: CDB6152



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CIRCUIT DESCRIPTION

Power Supply

As shown in the schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labled +5V and 0V. D1 is a transient suppressor which protects the components on the board from overvoltage damage and reversed supply connections. The supply decoupling recommended in the CS6152 data sheet is provided on the board by C1, C2 and C4. C2 is the 1.0µF decoupling capacitor which decouples TV+ to TGND. Similarly, the parallel combination of C1 (a 0.1µF ceramic capacitor) and C4 (a 68µF capacitor) is used to decouple RV+ to RGND. The CS6152 TV+ and RV+ leads are tied together at the IC.

Transmit Circuit

The CS6152's digital transmitter inputs are brought in through the BNC connectors labeled TCLK, TPOS and TNEG for the transmit clock and NRZ data respectively. The transmitter output is coupled onto a 100Ω twisted pair T1 line at the TTIP and TRING binding posts using a 1:1.36 step-up transformer (X1). C3 is the 0.47µF blocking capacitor recommended in the CS6152 data sheet.

Receive Circuit

The CS6152's receiver inputs are transformer coupled to the T1 twisted pair cable connected to the RTIP and RRING binding posts on the board. A center-tapped, center-grounded, 1:2 transformer, X1, is used to provide equal amplitude pulses of opposite polarity to the RTIP and RRING pins of the CS6152. R1 and R2 are 200Ω resistors which terminate the T1 line with 100Ω. The CS6152's digital receiver outputs are brought out to the BNC connectors labeled RS1 and RS2.

Control Circuit

The CS6152 digital control inputs are configured using the DIP switch SW1. Placing a switch in the "on" position grounds the corresponding pin of the same name placing it in the logic "0" or "off" state. LLEN0, LLEN1 and LLEN2 select the transmitter line length setting as described in the CS6152 data sheet. TAOS selects the transmission of all ones at the TCLK frequency. HIGHZ causes TTIP, TRING, R1 and R2 to enter a high impedance state.

Driver Performance Monitor

An LED status indicator is provided on the board for the Driver Performance Monitor (DPM) output of the CS6152. The LED is turned on to indicate that the CS6152 has transmitted somewhere between 31 to 63 or more consecutive zeros. Note that DPM can not change state if the TCLK signal is removed.

EVALUATION HINTS

1. Be sure to properly terminate TTIP and TRING when evaluating the transmitted signal. For more information on pulse shape evaluation refer to the Crystal application note AN-7 entitled, "Measurement and Evaluation of Pulse Shapes in T1/PCM-30 Transmission Systems".

2. Note that the SW1 position labeled "on" (the closed position) grounds the corresponds pin of the same name on the CS6152 and places the function in the logic "0" or "off" state.

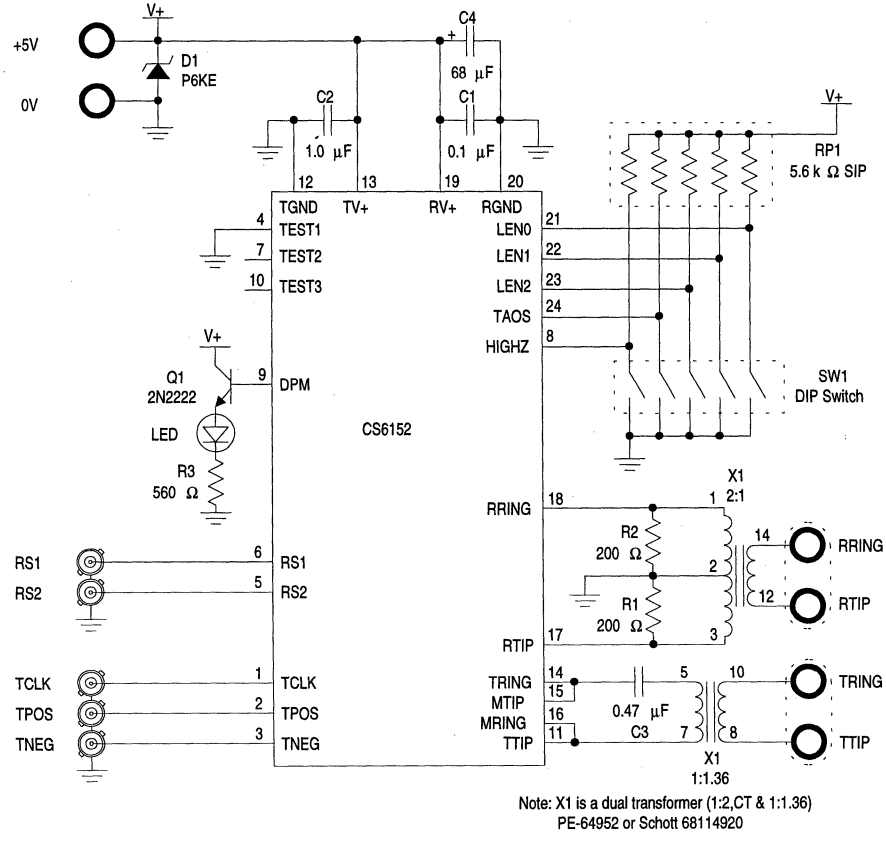


Figure 1. CDB6152 Schematic

Semiconductor Corporation

CS61534

T1/E1 Line Interface

Features

- Provides Analog PCM Line Interface for T1 and E1 Applications
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Transparent to AMI Polarity
- Diagnostic and Performance Monitoring Features
- Selectable Hardware or Host Processor Modes
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61534 combines the analog transmit and receive line interface functions for T1 or E1 applications in one 28-pin device. The line interface operates from a single 5 Volt supply, is transparent to the PCM framing format, and can work with ABAM and other cable types.

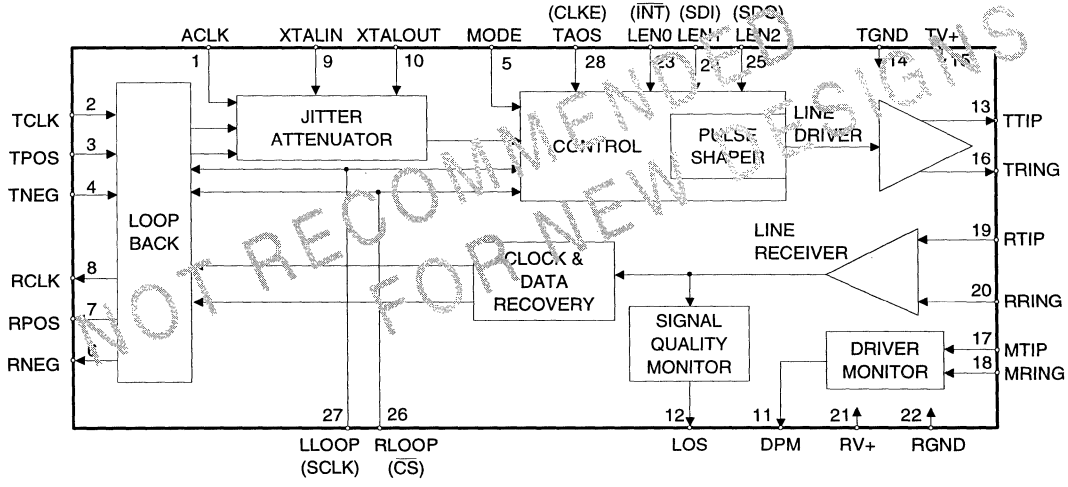
Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet in T1 applications. Maximum range is greater than 450 meters. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

Applications

- Interfacing Network Equipment to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexers, Data PBX's and LAN Gateways to a channel Service Unit or T1 Modem.

ORDERING INFORMATION

CS61534-IP	28 Pin Plastic DIP	(T1 only)
CS61534-IP1	28 Pin Plastic DIP	(T1 & E1)
CS61534-IL	28 Pin J-lead PLCC	(T1 only)
CS61534-IL1	28 Pin J-lead PLCC	(T1 & E1)
CS61534-ID	28 Pin CERDIP	(T1 only)
CS61534-ID1	28 Pin CERDIP	(T1 & E1)



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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	(RGND) - 0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, MTIP, and MRING, which must stay within a range of -6V to (RV+)+0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Total Power Dissipation 100% ones density & max. line length @ 5.25V	(Notes 4)	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS6152 and load.

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Notes 5 and 6) Pins 1-5, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	(Notes 5 and 6) Pins 1-5, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA; Pins 6-8, 11, 12, 23, 25	(Notes 5 and 6)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = -1.6 mA; Pins 6-8, 11, 12, 23, 25	(Notes 5 and 6)	V_{OL}	-	-	0.4	V
Input Leakage Current			-	-	±10	µA
High Impedance Leakage Current	(Note 5) Pin 25		-	-	±10	µA

Notes: 5. Functionality of pins 23 and 25 depends on the mode. See Host/Hardware mode description.
6. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter			Symbol	Min	Typ	Max	Units
Receiver Sensitivity Below DSX-1				-10	-	-	dB
Jitter Attenuation Curve	Corner Frequency	(Note 7)		-	-	50	Hz
Receiver Jitter Tolerance		(Note 8)					
	1.544 MHz	8kHz - 40kHz		0.1	-	-	UI
		10Hz - 500Hz		5	-	-	UI
	2.048 MHz	18kHz - 100kHz		0.2	-	-	UI
		20Hz - 2.4kHz		1.5	-	-	UI
Input Jitter Tolerance	Transmitter			7.0	-	-	UI
Loss of Signal Threshold				-	0.5	-	V
Transmitter Output Load		(Note 9)		-	25	-	Ω
AMI Output Pulse Amplitudes							
Line Length Selections LEN2/1/0 = 0/0/0 (Measured at transformer output; 0/0/0 see Figure 7)				2.7	3.0	3.3	V
All line length settings except, LEN2/1/0 = 0/0/0 (Measured at the DSX; Nomalization factor for Figure 6)				2.4	3.0	3.6	V
Power in 2kHz band about 772kHz		(Note 10)		12.6	15	17.9	dBm
Power in 2kHz band about 1.544 MHz (referenced to power at 772kHz)		(Note 10)		-29	-40	-	dB
Positive to Negative Pulse Imbalance		(Note 10)		-	0.2	0.5	dB

Notes:
7. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter.
8. For CERDIP ICs, assumes IC is operated within -70 ° to +70 °C of reset temperature. For plastic ICs, assumes IC is operated within -25 ° to +40 °C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1V of reset V+. Input data pattern is quasi-random. For 1.544 MHz: (2↑20)-1 with 1-in-15. For 2.048 MHz: (2↑15)-1 as defined in CCITT 0.151. For frequencies not specified above, the jitter tolerance will be better than the AT&T 43802 line or the CCITT G.823 line shown in Figure 10.
9. Transmitter is a low impedance voltage source. Transmitter performance is typical with a 25Ω load for T1 applications, which is determined by the 2:1 turns ratio of transformer and 100 Ω line impedance.
10. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.

T1 SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 11)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 12)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 13)	t_{pwl}	-	324	-	ns
Duty Cycle	(Note 14)		-	50	-	%
Rise Time, All Digital Outputs	(Note 15)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 15)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	274	-	ns
Reset Pulse Duration			0.2	-	2000	µs

Notes: 11. Crystal must meet specifications described in CXT6176 data sheet.
12. ACLK provided by an external source.
13. The sum of the pulse widths must always meet the frequency specifications.
14. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
15. At max load of 1.6 mA and 50 pF.

CCITT SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 16)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{in}	-	2.048	-	MHz
ACLK Frequency	(Note 12)	f_{out}	-	2.048	-	MHz
RCLK Pulse Width		t_{pwh}	-	244	-	ns
	(Note 13)	t_{pwl}	-	244	-	ns
Duty Cycle	(Note 14)		-	50	-	%
Rise Time, All Digital Outputs	(Note 15)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 15)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	194	-	ns
Reset Pulse Duration			0.2	-	2000	µs

Notes: 16. Crystal must meet specifications described in CXT8192 data sheet.

SWITCHING CHARACTERISTICS - HOST MODE (T_A = -40° to 85° C; V+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	250	-	-	ns
SCLK High Time	t_{ch}	250	-	-	ns
SCLK Rise and Fall Time	tr, tf	-	-	50	ns
CS to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to CS Hold Time	t_{cch}	50	-	-	ns
CS Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 17)	t_{cdv}	-	-	200	ns
CS to SDO High Z	t_{cdz}	-	100	-	ns

Notes: 17. Output load capacitance = 50 pF.

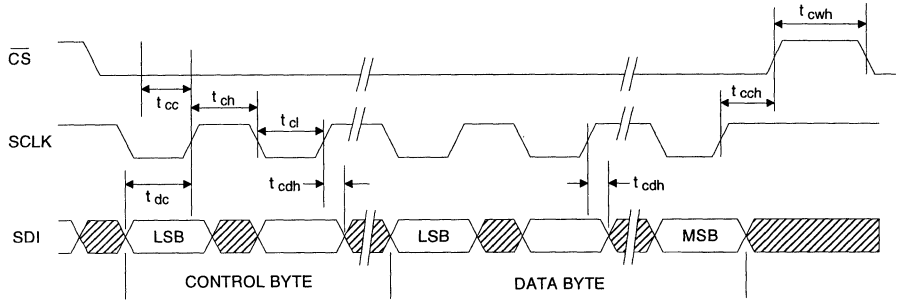


Figure 1. - Serial Port Write Timing Diagram

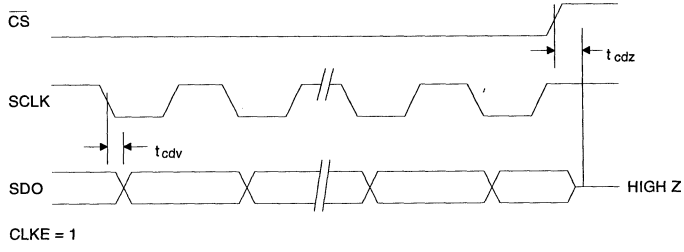


Figure 2. - Serial Port Read Timing Diagram

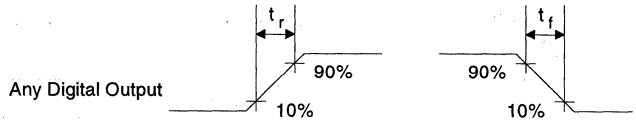


Figure 3. - Signal Rise and Fall Characteristics

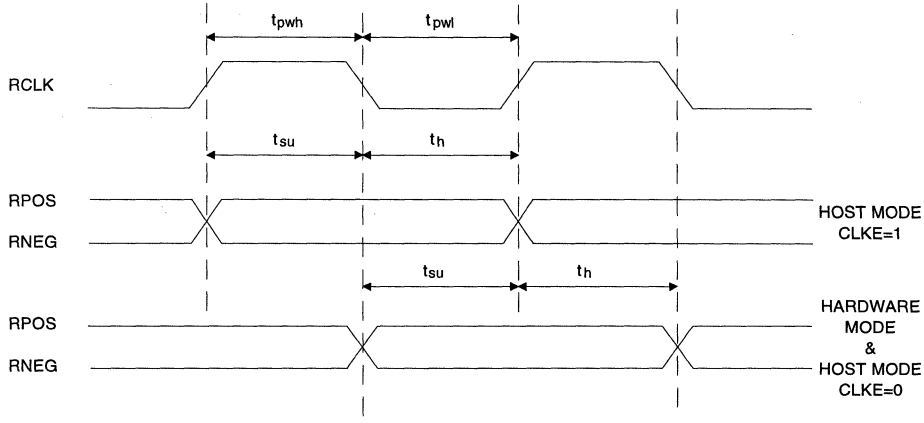


Figure 4. - Recovered Clock and Data Switching Characteristics

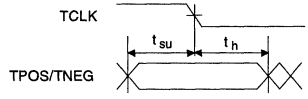


Figure 5. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a PCM transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

The CCITT pulse shape and T1 pulse shapes for line lengths from 0 to 655 feet (as measured from the CS61534 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is a low-impedance voltage source designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	1	1	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM (AT&T 600B or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	0	G.703	2.048 MHz CCITT

Table 1. Line Length Selection

Transmit Line Length Selection

For T1 applications, the line length selection supports both a three partition arrangement for ICOT and MAT cable, and a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61534 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 6.

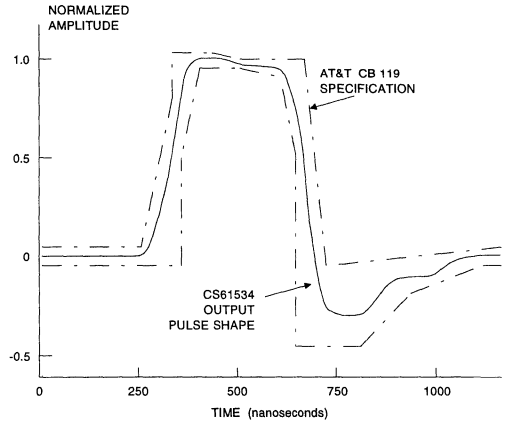


Figure 6. Typical Pulse Shape at DSX-1 Cross Connect

The remaining line length selection is for CCITT options. Transformer and resistor values depend on whether the coax or shielded cable is used, as shown in the *Applications* section at the back of this data sheet. The CCITT pulse shape meets the template shown in Figure 7, and the requirements of Table 2 for the given load conditions.

Transmit Jitter Attenuator

The CS61534 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a signal. Figure 8 shows a family of curves which show the jitter attenuation achieved by the CS61534 at T1 data rates. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input toler-

	For coaxial cable, 75 ohm load and transformer specified in Table A2.	For shielded twisted pair, 120 ohm load and transformer specified in Table A2.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

Table 2. CCITT G.703 Pulse Specifications

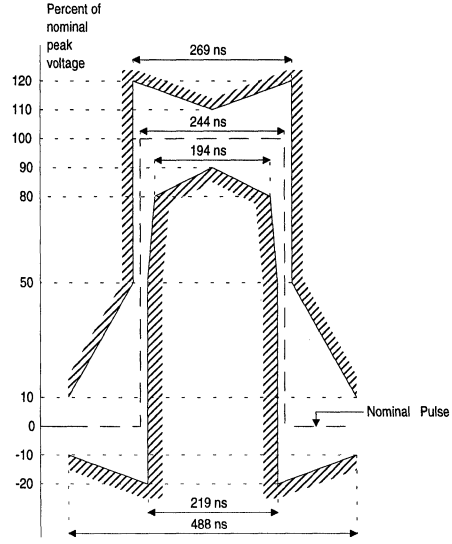


Figure 7. Mask of the Pulse at the 2048 kbps Interface

ance specifications of AT&T Publication 43802, as shown in Figures 9 and 10.

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, (8.192 MHz for PCM-30 rates), and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be

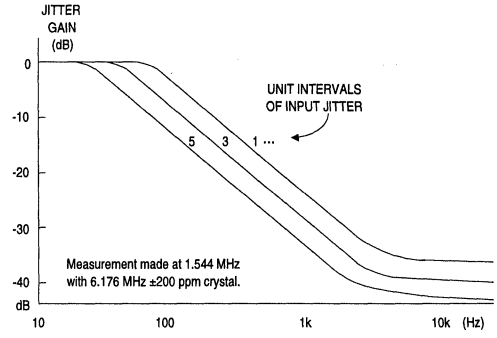


Figure 8. Jitter Attenuation Curves

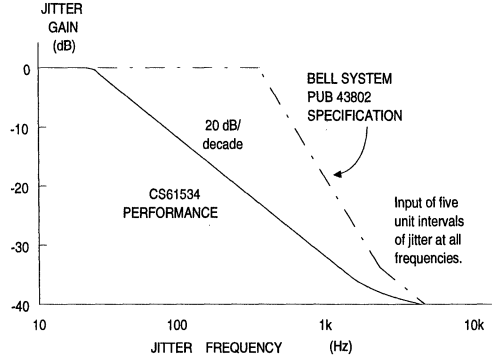


Figure 9. Jitter Attenuation Characteristics

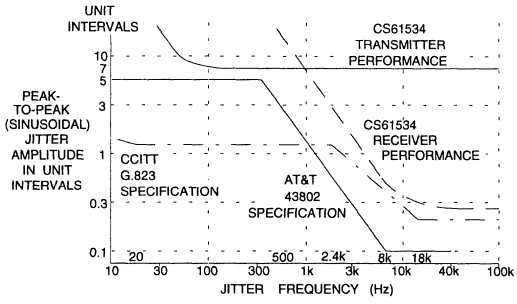


Figure 10. Typical Input Jitter Tolerance

disabled by driving XTALIN with a clock which is *exactly* four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock, ACLK. In this mode, the TPOS, TNEG and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of DSX-1/PCM-30 cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61534 side. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802 and CCITT G. 823, (see Figure 10).

The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61534, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO is near the reference frequency. This current is then held constant. The FPLL is controlled, small signal, by the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61534 will optimize receiver performance for the operating power supply and temperature.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	X	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
HIGH	LOW	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
		SDO	SCLK	Falling
HIGH	HIGH	RPOS	RCLK	Falling
		RNEG	RCLK	Falling
		SDO	SCLK	Rising

X= Don't care

Table 3. Data Output / Clock Relationship

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RPOS and RNEG are not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output but may drift up to 6% from the nominal frequency. Note that in the host mode, LOS is simultaneously available from pin 12 and the register.

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. The transmit data and clock signals (TPOS, TNEG and TCLK) are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case AMI-coded continuous ones are transmitted on the line at the rate determined by ACLK.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 4). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). Bipolar violations are passed unchanged through the CS61534 during remote loopback.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TPOS & TNEG	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 4. Interaction of RLOOP and TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV at least once within 32±2 cycles. In the host mode, DPM is available from both the register and pin 11. The driver performance monitor is not designed to detect broken printed ciruit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING.

DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by

having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61534 cannot be used to monitor the TTIP/TRING pins of a CS61574A, CS61535A, CS6158A, or CS61575.

Reset

The CS61534 initiates internal reset procedures either on power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training procedure for the FPLL. **It is strongly recommended that a hardware or software reset request be issued after the power supply has stabilized and signals have been applied to the device to insure that the FPLL is correctly trained.** Training the FPLL takes at most 43 ms, but typically requires less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The device will first clear its data registers then initiate the FPLL training procedure which will be complete within 53 ms.

During the reset procedure, the loss of signal indicator, LOS, is high. Once the reset procedures are completed, the loss of signal indicator goes low signifying that normal operation of the device has begun.

Mode of Operation

The CS61534 can be operated in two modes, the hardware mode and the host mode. In the hardware mode, discrete pins are used to interface the device's control functions and status information. In the host mode, the CS61534 is connected to a host processor and a serial data bus is used for input and output of control and status information. There are six dual function pins whose functionality is determined by the mode pin, MODE. Table 5 shows the pin definitions.

PIN #	MODE	
	HARDWARE	HOST
PIN 23	LEN0	$\overline{INT}$
PIN 24	LEN1	SDI
PIN 25	LEN2	SDO
PIN 26	RLOOP	$\overline{CS}$
PIN 27	LLOOP	SCLK
PIN 28	TAOS	CLKE

Table 5. Pin Definitions

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One onboard register can be written to the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the falling edge of the 16th SCLK cycle, and must go high before the rising edge of the 24th SCLK cycle.

Figure 11 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. Data bit D7 is held until the rising edge of the 17th clock cycle.

An address/command byte, shown in Table 6, precedes the register data. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61534 responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6. Address / Command Byte

The data byte, shown in Table 7, can be read/written by the serial port. Data is input/output on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are read only. During a write to the register, the CS61534 ignores the first two bits of the data byte. SDO goes to a high-impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

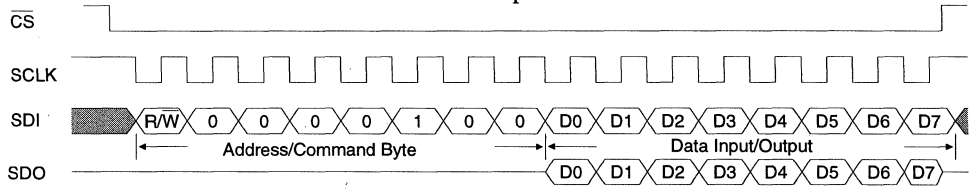
LSB: first bit in or out	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in or out	7	TAOS	Transmit All Ones Select

Table 7. Data Register

Power Supply

The device operates from a single 5 Volt supply. Separate pins for transmit (TV+) and receive (RV+) supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61534 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

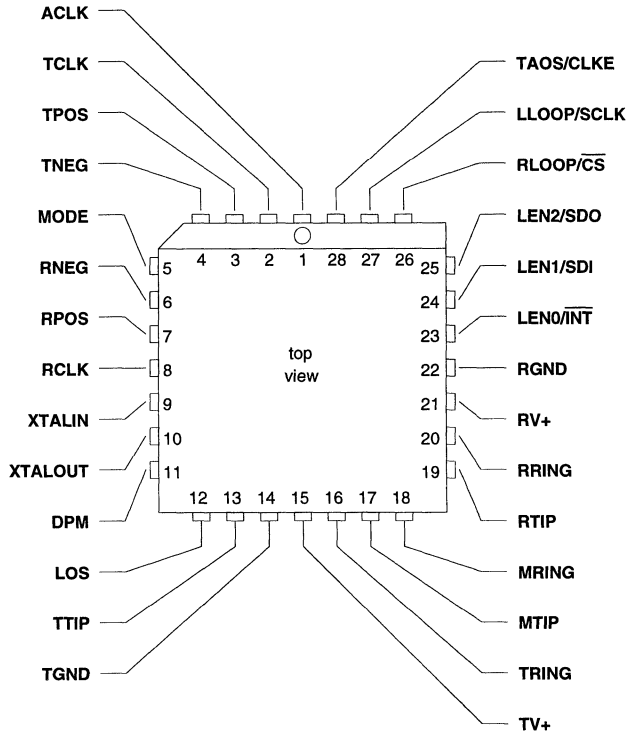


Note: SDI sampled on rising edge of SCLK; SDO updated on falling edge of SCLK (CLKE = 1).

Figure 11. Input / Output Timing

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	**ACLK**	1	28	**TAOS/CLKE**	TRANSMIT ALL ONES / CLOCK EDGE
TRANSMIT CLOCK	**TCLK**	2	27	**LLOOP/SCLK**	LOCAL LOOPBACK / SERIAL CLOCK
TRANSMIT POSITIVE PULSE	**TPOS**	3	26	**RLOOP/$\overline{CS}$**	REMOTE LOOPBACK / CHIP SELECT
TRANSMIT NEGATIVE PULSE	**TNEG**	4	25	**LEN2/SDO**	LINE / SERIAL DATA OUT
MODE SELECTION	**MODE**	5	24	**LEN1/$\overline{SDI}$**	LENGTH / SERIAL DATA OUT
RECEIVED NEGATIVE PULSE	**RNEG**	6	23	**LEN0/$\overline{INT}$**	SELECT / ALARM INTERUPT
RECEIVED POSITIVE PULSE	**RPOS**	7	22	**RGND**	RECEIVE GROUND
RECOVERED CLOCK	**RCLK**	8	21	**RV+**	RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	**XTALIN**	9	20	**RRING**	RECEIVE RING
CRYSTAL CONNECTION	**XTALOUT**	10	19	**RTIP**	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	**DPM**	11	18	**MRING**	MONITORED RING
LOSS OF SIGNAL	**LOS**	12	17	**MTIP**	MONITORED TIP
TRANSMIT TIP	**TTIP**	13	16	**TRING**	TRANSMIT RING
TRANSMIT GROUND	**TGND**	14	15	**TV+**	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (8.192 MHz for CCITT applications) crystal should be connected across these pins. If desired, an externally generated 6.176 MHz (8.192 MHz for CCITT) clock signal may be input to XTALIN, pin 9; XTALOUT, pin 10, should be left floating. Overdriving the oscillator with an external source disables the jitter attenuator. This externally generated clock must be *exactly* four times the frequency of the TCLK signal.

Control

MODE - Mode Select, Pin 5.
Setting MODE to logic 1 puts the CS61534 in the host mode. In the host mode, a serial control port is used to control the CS61534 and determine its status. Setting MODE to logic 0 puts the CS61534 in the hardware mode, where configuration and status are controlled by discrete pins. MODE defines the status of pins 23 through 28.

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored. If the oscillator is being driven with a 4x clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when received signal is lost (LOS is high), or the transmitter driver has failed (DPM is high), to flag the host processor. $\overline{\text{INT}}$ will stay low until the fault condition goes away. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.

Data for the on-chip registers and is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.

Status and control information from the on-chip registers. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or $\overline{\text{CS}}$ is high.

CLKE - Clock Edge, Pin 28.

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.

Clock used to read or write the serial port registers.

$\overline{\text{CS}}$ - Chip Select, Pin 26.

Pin must transition from high to low to read or write the serial ports.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 (or 2.048) MHz clock. The frequency of ACLK determines the rate at which TAOS is output.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1. Data and clock are recovered and output on RPOS/RNEG and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61534. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, input a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-voltage level. This clock frequency can range from 100 kHz to the TCLK frequency.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles without a detected one. LOS returns to logic 0 when signal returns.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, approximately 4.4 Ω of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

APPLICATIONS

Line Interface

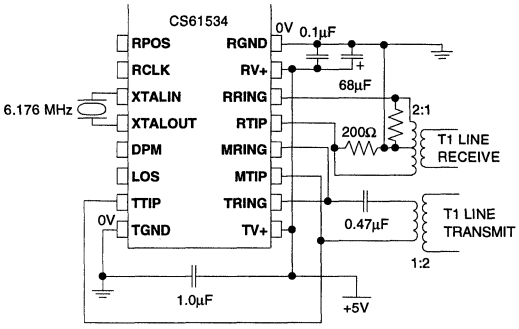


Figure A1. Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS61534 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS61534 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions. First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate

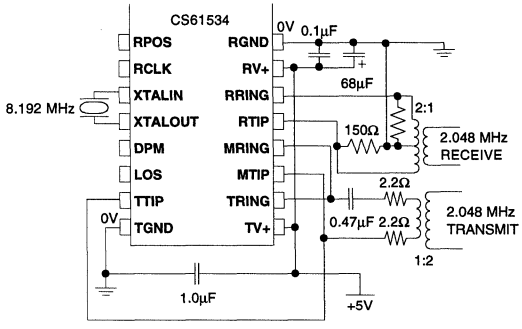


Figure A2. Configuration for Transmitting onto 75 Ω Coax

the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61534. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS61534.

Figure A3 shows the connections for some of the recommended transformers for the transmitter. Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,

Primary inductance: 600 µH min measured at 772 kHz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz

Interwinding capacitance: 23 pF max, primary to secondary

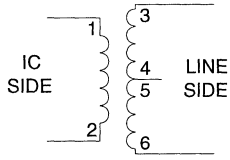
ET-Constant: 16 V-µs minimum for T1; 12 V-µs for CEPT

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A1. Suitable Transformers



Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

Figure A3.Some Recommended Transmitter/Transformer Connections

eliminated by inserting a 0.47uF non-polarized capacitor in series with the primary of the transmit transformer.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A4. In the host mode, the inverter is not needed if CLKE is high.

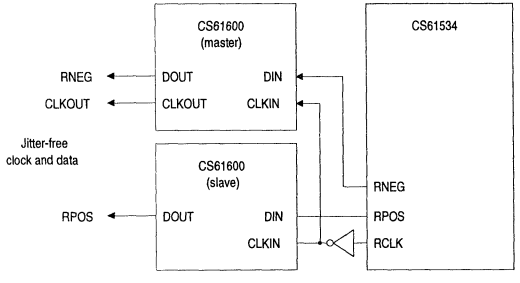


Figure A4. Receive Jitter Attenuation

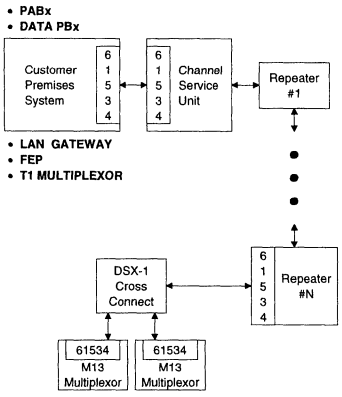


Figure A5. Application of CS61534

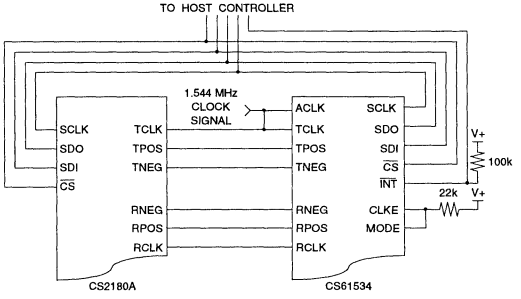


Figure A6. Interfacing the CS61534 with a CS2180A

Applicable Systems

Figure A5 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A5, the CS61534 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and in network equipment that connects to a DSX-1 cross connect.

Interfacing The CS61534 With T1 Digital Transceivers

To interface with the CS2180A, connect the devices as shown in Figure A6. In this case, the CS61534 and CS2180A are in host mode controlled by a microprocessor serial interface. If the CS61534 is used in hardware mode, then the CS61534 RCLK output must be inverted before being input to the CS2180A.

• Notes •

Semiconductor Corporation

CS61535A
CS61535

T1/E1 Line Interface

Features

- Provides Analog PCM Line Interface for T1 and E1 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

General Description

The CS61535A and CS61535 combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61535A provides additional features and higher performance than the CS61535.

Both devices feature a transmitter jitter attenuator making them ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The CS61535A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

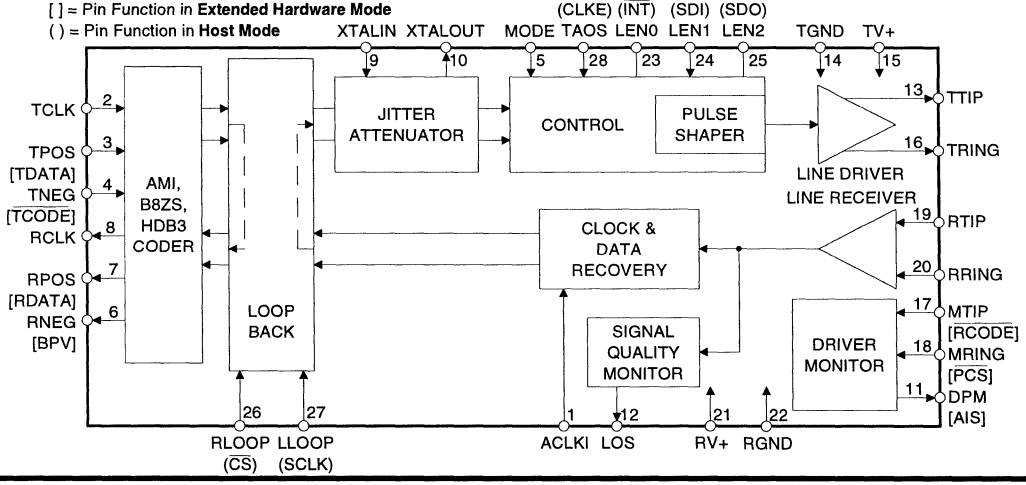
Both ICs use a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to E1 links.

Ordering Information

CS61535A-IP1	28 Pin Plastic DIP
CS61535A-IL1	28 Pin PLCC (j-leads)
CS61535-IP1	28 Pin Plastic DIP
CS61535-IL1	28 Pin PLCC (j-leads)



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to RGND,TGND=0V)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Min	Typ	Max	Units
DC Supply		(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature			T_A	-40	25	85	°C
Power Consumption	CS61535	(Notes 4,5)	P_C	-	620	760	mW
	CS61535A	(Notes 4,5)		-	290	350	mW
Power Consumption	CS61535	(Notes 4,6)	P_C	-	400	-	mW
	CS61535A	(Notes 4,6)		-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 7, 8)					
CS61535 Pins 1-5, 23-28	V_{IH}	2.0	-	-	V
CS61535A Pins 1-4, 17, 18, 23-28 (Note 9)		2.0	-	-	V
Low-Level Input Voltage (Notes 7, 8)					
CS61535 Pins 1-5, 23-28	V_{IL}	-	-	0.8	V
CS61535A Pins 1-4, 17, 18, 23-28 (Note 9)		-	-	0.8	V
High-Level Output Voltage (I_{OUT} = -40 µA) (Notes 7, 8, 10)					
CS61535 Pins 6-8, 11, 12, 25	V_{OH}	2.4	-	-	V
CS61535A Pins 6-8, 11, 12, 25		4.0	-	-	V
Low-Level Output Voltage (I_{OUT} = 1.6 mA) (Notes 7, 8, 10)					
CS61535 Pins 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
CS61535A Pins 6-8, 11, 12, 23, 25		-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	µA
CS61535A Low-Level Input Voltage, Pin 5	V_{IL}	-	-	0.2	V
CS61535A High-Level Input Voltage, Pin 5	V_{IH}	(RV+) - 0.2	-	-	V
CS61535A Mid-Level Input Voltage, Pin 5 (Note 11)	V_{IM}	2.3	-	2.7	V

Notes:
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate output.
9. Pins 17 and 18 of the CS61535A are digital inputs in the Extended Hardware Mode.
10. Output drivers will drive CMOS logic levels into a CMOS load.
11. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Min	Typ	Max	Units
Jitter Attenuator				
Jitter Attenuation Curve Corner Frequency (Notes 12)	-	6	-	Hz
T1 Jitter Attenuation in Remote Loopback (Note 13)				
Jitter Freq. [Hz] Amplitude [UIpp]				
10 10	3.0	6.0	-	dB
100 10	20	30	-	dB
500 10	35	35	-	dB
1k 5	40	50	-	dB
10k, 40k 0.3	40	50	-	dB
E1 Jitter Attenuation in Remote Loopback (Note 14)				
Jitter Freq. [Hz] Amplitude [UIpp]				
10 1.5	3.0	6.0	-	dB
100 1.5	20	32	-	dB
400 1.5	30	43	-	dB
1k 1.5	35	50	-	dB
10k, 100k 0.2	35	50	-	dB
Attenuator Input Jitter Tolerance (Note 15)	12	23	-	UI

Notes:
12. Not production tested. Parameters guaranteed by design and characterization.
13. Attenuation measured at the demodulator output of an HP3785B with input jitter equal to 3/4 of measured jitter tolerance using a measurement bandwidth of 1 Hz (10<f<100Hz), 4Hz (100<f<1000 Hz) and 10 Hz (f> 1kHz) centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern. Crystal must meet specifcations in CXT6176 datasheet.
14. Jitter measured at the demodulator output of an HP3785A using a measurement bandwidth not to exceed 20 Hz centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern. Crystal must meet specifications in CXT8192 datasheet.
15. Output jitter increases significantly when attenuator input jitter tolerance is exceeded.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 16)				
E1, 75 Ω	(Note 17)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 18)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 19)	2.7	3.0	3.3	V
T1, DSX-1	(Note 20)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
75Ω application	(Note 17)	-0.237	-	0.237	V
120Ω application	(Note 18)	-0.3	-	0.3	V
Recommended Output Load at TTIP and TRING					
CS61535		-	25	-	Ω
CS61535A		-	75	-	Ω
Jitter Added During Remote Loopback	(Note 21)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 12, 16)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 12, 16)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 12, 16)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
CS61535A Transmitter Return Loss	(Notes 12, 16, 22)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
CS61535A Transmitter Short Circuit Current	(Notes 12, 23)	-	-	50	mA RMS

Notes:
16. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.
17. Amplitude measured at the transformer (CS61535A-1:1 or 1:1.26, CS61535-1:2) output across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0. The CS61535 requires a 4.4 Ω resistor in series with the TTIP or TRING pin for this application.
18. Amplitude measured at the transformer (CS61535A-1:1.26, CS61535-1:2) output across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
19. Amplitude measured at the transformer (CS61535A-1:1.15, CS61535-1:2) output across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
20. Amplitude measured across a 100 Ω load at the DSX-1 cross-connect for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0 and 1/1/1 after the length of #22 AWG ABAM equivalent cable specified in Table 3. The CS61535A requires a 1:1.15 transformer and the CS61535 requires a 1:2.
21. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
22. Return loss = 20 $\log_{10}$ ABS($(z_1 + z_0)/(z_1 - z_0)$) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
23. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Driver Performance Monitor					
CS61535A MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.60	-	V
Receiver					
CS61535A RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)					
CS61535		-10	-	-	dB
CS61535A		-13.6	-	-	dB
CS61535A Data Decision Threshold					
T1, DSX-1	(Note 24)	60	65	70	% of peak
T1, DSX-1	(Note 25)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 26)	45	50	55	% of peak
CS61535 Data Decision Threshold	T1	-	65	-	% of peak
	E1	-	50	-	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 27)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold					
CS61535A	(Note 28)	0.25	0.30	0.50	V
CS61535		-	0.30	-	V

Notes: 24. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
25. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
26. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
27. Jitter tolerance increases at lower frequencies. See Figure 11.
28. LOS goes high after 160 to 190 consecutive zeros are received. A zero is output on RPOS and RNEG (or RDATA) for each bit period where the input signal amplitude remains below the data decision threshold. The analog input squelch circuit operates when the input signal amplitude above ground on the RTIP and RRING pins falls within the squelch range long enough for the internal slicing threshold to decay within this range. Operation of the squelch causes zeros to be output on RPOS and RNEG as long as the input amplitude remains below 0.25V. During receive LOS, pulses greater than 0.25V in amplitude may be output on RPOS and RNEG. LOS returns low after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency (Note 29)		f_C	-	6.176000	-	MHz
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency (Note 30)		f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle (Notes 31, 32)		t_{pwh1}/t_{pw1}	- -	78 29	- -	% %
CS61535A RCLK Cycle Width (Note 32)		t_{pw1} t_{pwh1} t_{pwl1}	320 130 100	648 190 458	980 240 850	ns ns ns
CS61535 RCLK Cycle Width (Note 32)		t_{pw1} t_{pwh1} t_{pwl1}	348 - 100	648 508 140	980 - -	ns ns ns
Rise Time, All Digital Outputs (Note 33)		t_r	-	-	85	ns
Fall Time, All Digital Outputs (Note 33)		t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling (Note 34)		t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling (Note 35)		t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising (Note 31)		t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling (Note 34)		t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling (Note 35)		t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising (Note 31)		t_{h1}	150	274	-	ns
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	CS61535	t_{pwh2}	150		500	
	CS61535A (Notes 31, 34)		80	-	500	ns
	CS61535A (Note 35)		150	-	500	ns

Notes: 29. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
30. ACLKI provided by an external source or TCLK, but *not* RCLK.
31. Hardware Mode, or Host Mode (CLKE = 0).
32. RCLK cycle width will vary with extent by which pulses displaced by jitter. Specified under worst case jitter conditions: 0.4 UI AMI data displacement for T1 and 0.2 UI AMI data displacement for E1.
33. At max load of 1.6 mA and 50 pF.
34. Host Mode (CLKE = 1).
35. Extended Hardware Mode.

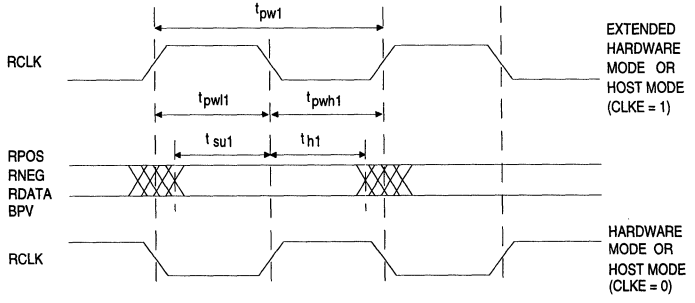


Figure 1. Recovered Clock and Data Switching Characteristics

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter			Symbol	Min	Typ	Max	Units
Crystal Frequency		(Note 29)	f_c	-	8.192000	-	MHz
ACLKI Duty Cycle			t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency		(Note 30)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	CS61535	(Notes 31, 32)	t_{pwh1}/t_{pw1}	-	71	-	%
	CS61535A	(Notes 31, 32)		-	29	-	%
CS61535A RCLK Cycle Width		(Note 32)	t_{pw1}	310	488	670	ns
			t_{pwh1}	90	140	190	ns
			t_{pwl1}	120	348	500	ns
CS61535 RCLK Cycle Width		(Note 32)	t_{pw1}	320	488	670	ns
			t_{pwh1}	-	348	-	ns
			t_{pwl1}	100	140	-	ns
Rise Time, All Digital Outputs		(Note 33)	t_r	-	-	85	ns
Fall Time, All Digital Outputs		(Note 33)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling		(Note 34)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling		(Note 35)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising		(Note 31)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling		(Note 34)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling		(Note 35)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising		(Note 31)	t_{h1}	100	194	-	ns
TCLK Frequency			f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	CS61535	(Note 36)	t_{pwh2}	215	-	258	ns
	CS61535A	(Notes 34, 31)		80	-	340	ns
	CS61535A	(Note 35)		150	-	340	ns

Notes: 36. The transmitted pulse width for LEN2/1/0 = 0/0/0 depends on the TCLK duty cycle for the CS61535.

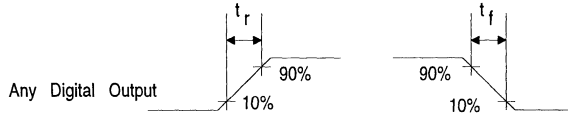


Figure 2. Signal Rise and Fall Characteristics

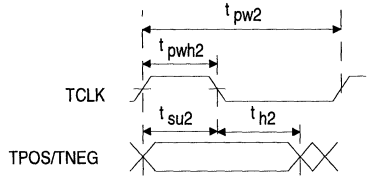


Figure 3a. Transmit Clock and Data Switching Characteristics

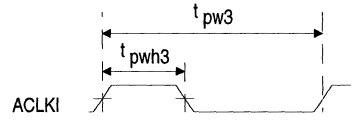


Figure 3b. Alternate External Clock Characteristics

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time		t_{dc}	50	-	-	ns
SCLK to SDI Hold Time		t_{cdh}	50	-	-	ns
SCLK Low Time		t_{cl}	240	-	-	ns
SCLK High Time		t_{ch}	240	-	-	ns
SCLK Rise and Fall Time		t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time		t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	(Note 37)	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time		t_{cwh}	250	-	-	ns
SCLK to SDO Valid	(Note 38)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z		t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	(Note 39)	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	(Note 39)	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	(Note 39)	t_{pcsl}	250	-	-	ns

Notes: 37. For CLKE = 0, $\overline{CS}$ must remain low at least 50 ns after the 16th falling edge of SCLK.
38. Output load capacitance = 50pF.
39. CS61535A only.

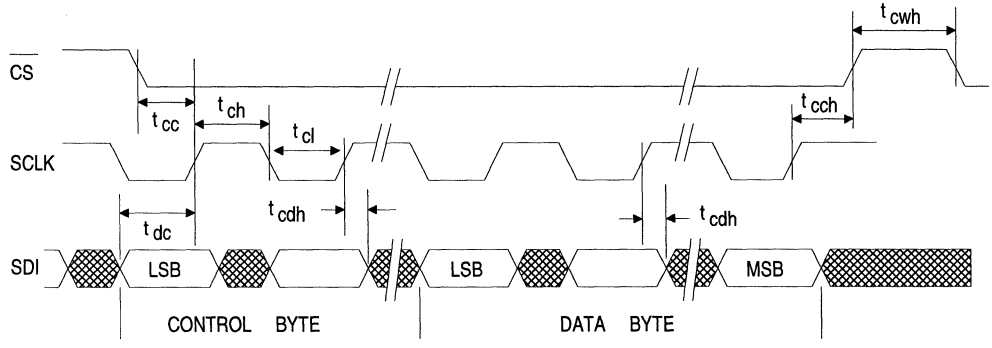


Figure 4. Serial Port Write Timing Diagram

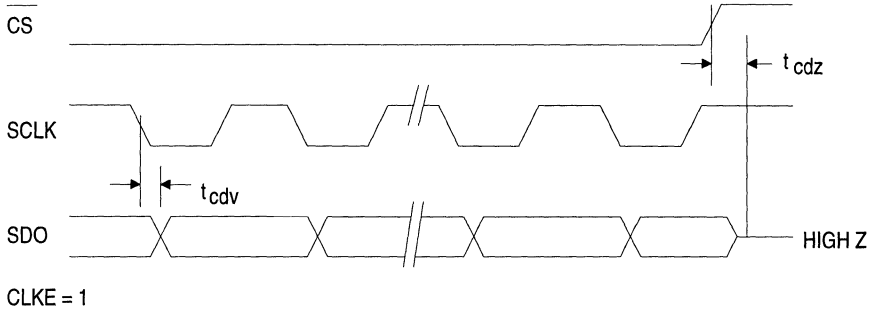


Figure 5. Serial Port Read Timing Diagram

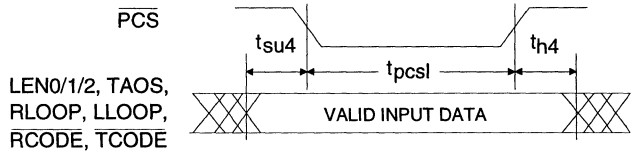


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Enhancements in CS61535A

The CS61535A provides higher performance and more features than the CS61535 including:

- 50% lower power consumption,
- Internally matched transmitter output impedance for improved signal quality,
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- ANSI T1.231-1993 compliant receiver Loss of Signal (LOS) handling,
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,
- The Driver Performance Monitor operates over a wider range of input signal levels.
- Elimination of the requirement that a reference clock be input on the ACLKI pin.

Existing designs using the CS61535 can be converted to the higher performance, pin-compatible CS61535A if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio.

Introduction to Operating Modes

The CS61535A supports three operating modes and the CS61535 supports two operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The CS61535A modes are Hardware Mode, Extended Hardware Mode, and Host Mode. The CS61535 supports the Host and Hardware Modes. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode (see Table 2).

	MODE		
	HARDWARE	EXTENDED HARDWARE*	HOST
SUPPORTED BY:	CS61535A CS61535	CS61535A	CS61535A CS61535
MODE-PIN INPUT LEVEL	<0.2V	FLOAT, or 2.5V	>(RV+) - 0.2V
CONTROL METHOD	INDIVIDUAL CONTROL LINES	INDIVIDUAL CONTROL LINES & PARALLEL CHIP SELECT	SERIAL µ-PROCESSOR PORT
LINE CODE ENCODER & DECODER	NONE	AMI, B8ZS, HDB3	NONE
AIS DETECTION	NO	YES	NO
DRIVER PERFORMANCE MONITOR	YES	NO	YES

*CS61535A only

Table 1. Differences in Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE*	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

* CS61535A only

Table 2. Pin Definitions

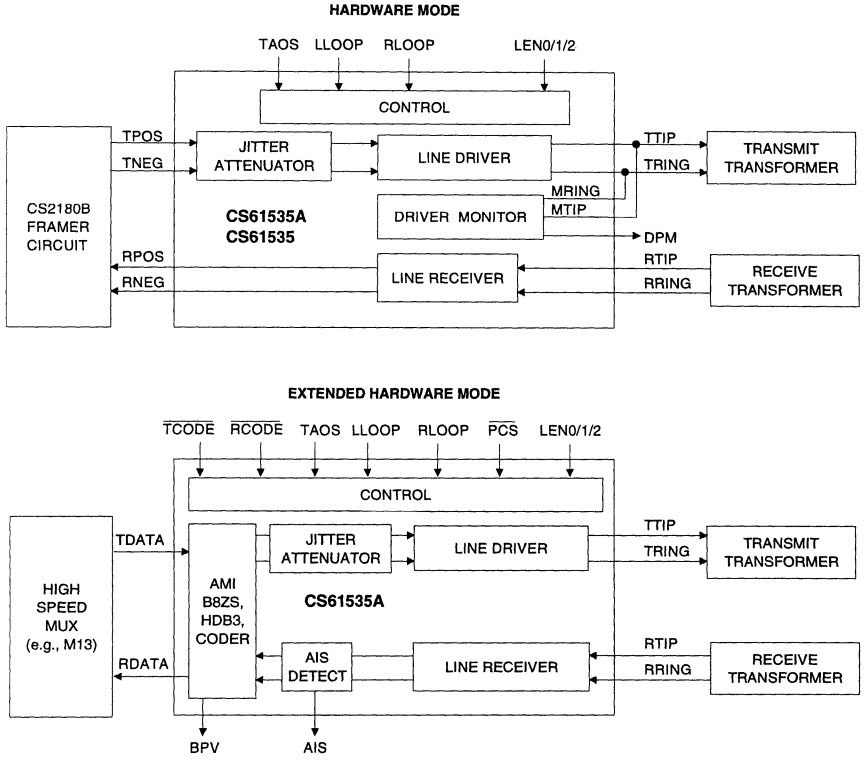


Figure 7. Overview of Operating Modes

Transmitter

The transmitter takes data from a T1 (or E1) terminal, attenuates jitter, and produces pulses of appropriate shape. The transmit clock, TCLK, and transmit data, TPOS & TNEG or TDATA, are supplied synchronously. Data is sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 3. The CS61535A line driver is designed to drive a 75 Ω equivalent load. The CS61535 drives a 25 Ω load.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets ANSI T1.102-1993 requirements when using ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61535 and CS61535A automatically adjust the pulse width based upon the "line length " selection made.

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1	AT&T CB113 (CS61535A only)	REPEATER
0	0	0	CCITT G.703	2.048 MHz E1
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

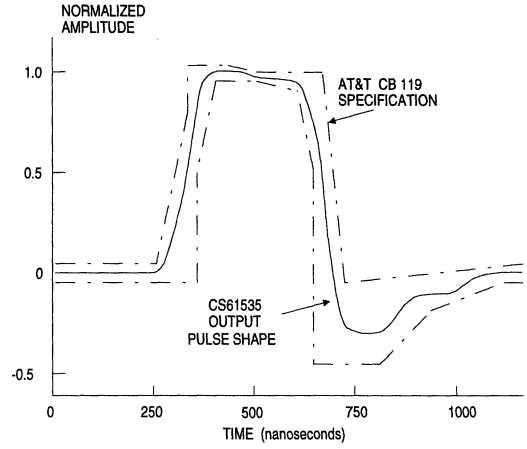


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

The E1 G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

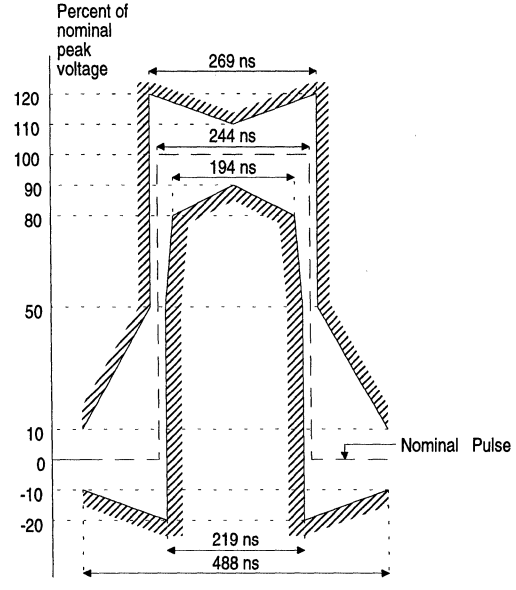


Figure 9 . Mask of the Pulse at the 2048 kbps Interface

For E1 applications, the CS61535A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

The CS61535A transmitter will detect a failed TCLK, and will force the TTIP and TRING outputs low. If the clock signal is removed from TCLK on the CS61535, TPOS and TNEG should both be low during the last falling edge of TCLK.

To place the CS61535 in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG (or TDATA) should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the transmit clock signal. It consists of a 32 bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 10.

The jitter attenuator works in the following manner. Data on TPOS and TNEG (or TDATA) are written into the jitter attenuator's FIFO by TCLK. The rate at which data is read out of the FIFO and transmitted is determined by the oscillator. Logic circuits adjust the capacitive loading on the crystal to set its oscillation frequency to the average of the TCLK frequency. Signal jitter is absorbed in the FIFO.

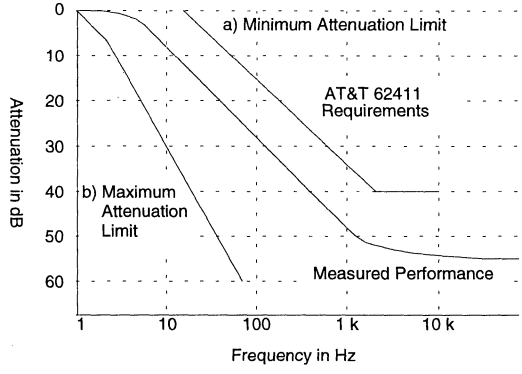


Figure 10. Typical Jitter Attenuation Curve

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

Jitter Tolerance of Jitter Attenuator

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should the pointers attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. When a divide by 3 1/2 or 4 1/2 occurs, the data bit will be driven on to the line either an eighth bit period early or an eighth bit period late.

When the TCLK frequency is close to the center frequency of the crystal oscillator, the high frequency jitter tolerance is 23 UI before the divide by 3 1/2 or 4 1/2 circuitry is activated. As the center frequency of the oscillator and the TCLK frequency deviate from one another, the jitter tolerance is reduced. As this frequency deviation becomes large, the maximum jitter tolerance at high frequencies is reduced to 12 UI before the underflow/overflow circuitry is activated. In application, it is unlikely that the oscillator center frequency will be precisely aligned with the TCLK frequency due to allowable TCLK tolerance, part to part variations, crystal to crystal variations, and crystal temperature drift. The oscillator tends to track low frequency jitter so jitter tolerance increases as jitter frequency decreases.

The crystal frequency must be 4 times the nominal signal frequency: 6.176 MHz for 1.544 MHz operation; 8.192 MHz for 2.048 MHz applications. Internal capacitors load the crystal, controlling the oscillation frequency. The crystal must be designed so that over operating temperature, the oscillator frequency range exceeds the system frequency tolerance. Crystal Semiconductor offers the CXT6176 & CXT8192 crystals, which yield optimum performance with the CS61535 and CS61535A.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of ACLKI. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. A TAOS request will be ignored if Remote loopback is in effect. ACLKI jitter will be attenuated. TAOS is not available on the CS61535A when ACLKI is grounded.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 11. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI or the jitter attenuator's oscillator, into 13 equal divisions or phases. Continuous calibration assures timing accuracy, even if temperature or power supply voltage fluctuate.

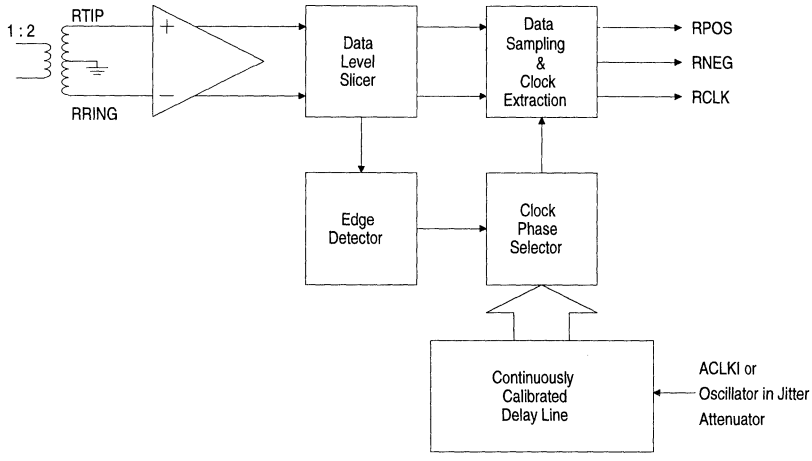


Figure 11. Receiver Block Diagram

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that shown in Figure 12.

The CS61535 device outputs a clock at RCLK after the first signal is input to RTIP/RRING. The CS61535A outputs a clock immediately upon power-up. In either case, the clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Extended Hardware Mode, data at RDATA is stable and may be sampled on the falling edge of the recovered clock. In the Host Mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

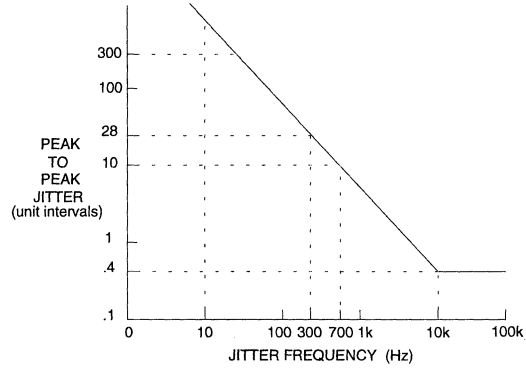


Figure 12. Input Jitter Tolerance of Receiver

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2v)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+)-0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+)-0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5v)	X	RDATA	RCLK	Falling

X= Don't care

Table 5. Data Output/Clock Relationship

Jitter and Recovered Clock

The CS61535 and CS61535A are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until a data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UIpp. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS61535 or CS61535A, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the E1 rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS61535 and CS61535A, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS61535 and CS61535A is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt issued on INT. LOS will go low (and flag the INT pin again if serial I/O is used) when a valid signal is detected. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12.

In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS and RNEG (or RDATA) regardless of LOS status. In the

CS61535, LOS returns to a logic zero upon receipt of the first bit at the RTIP and RRING inputs. In the CS61535A, LOS returns to logic zero when the ones density reaches 12.5% (based upon 175 bit periods staring with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993. Also, a power-up or manual reset will set LOS high on the CS61535A.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA) and outputs it at RCLK, RPOS and RNEG (or RDATA). Local loopback is selected by taking pin 27 high, or LLOOP may be selected using the serial interface. The data on the transmitter inputs is transmitted on the line unless TAOS is selected to cause the transmission of an all ones signal instead. Receiver inputs are ignored when local loopback is in effect. The jitter attenuator is not included in the local loopback data path. Selection of local loopback overrides the chip's loss of signal response.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). Remote loopback is selected by taking pin 26 high, or RLOOP may be selected using the serial interface. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In the CS61535A Extended Hardware Mode, remote loopback occurs before the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations. The recovered data will also be decoded and output on RDATA if $\overline{\text{RCODE}}$ is low.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the Hardware and Host Modes of the CS61535 and CS61535A are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure. In the Host Mode, DPM is available from both the register and pin 11.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring device, rather than having it monitor its own performance. Note that a CS61535 can not be used to monitor a CS61535A due to output stage differences.

For the CS61535 only, the DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Line Code Encoder/Decoder

In the CS61535A Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using pins LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ as shown in Table 6.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 6. Selection of Encoder/Decoder

Alarm Indication Signal

In the CS61535A Extended Hardware Mode, the receiver sets the output pin AIS high when less than 9 zeros are detected out of 8192 bit periods. AIS returns low when 9 or more zeros are detected out of 8192 bits.

Parallel Chip Select

In the CS61535A Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low. Changes in inputs will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the CS61535 and CS61535A are held in a static state until the supply crosses a threshold of approximately three Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI (or by the crystal oscillator if ACLKI is not present with the CS61535A). The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware modes, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0.

In the CS61535A, a reset will set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One eight-bit register can be written to via the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

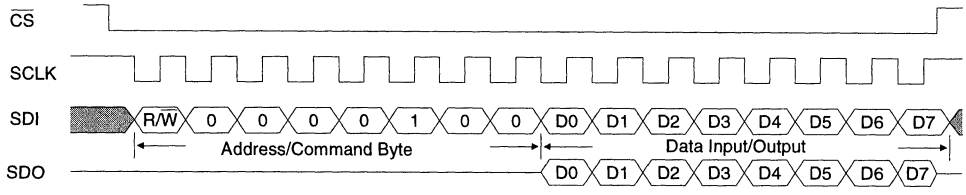


Figure 13. Input/Output Timing

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). SCLK may be either high or low when $\overline{CS}$ initially goes low. Address and input data bits are clocked in on the rising edge of SCLK. Data on SDO is valid and stable on the falling edge of SCLK when CLKE is low, and on the rising edge of SCLK when CLKE is high. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. For CLKE = 1, data bit D7 is held to the falling edge of the 16th clock cycle; for CLKE = 0, data bit D7 is held to the rising edge of the 17th clock cycle. SDO goes to a high impedance state either after bit D7 is output or at the end of the hold period of data bit D7.

An address/command byte, shown in Table 7, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61535 and CS61535A respond to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 7. Address/Command Byte

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61535 into a factory test mode.

Table 8. Input Data Register

The data register, shown in Table 8, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver. If bits 0 or 1 are true, the corresponding interrupt is suppressed. So if a loss of signal interrupt is cleared by writing a 1 to bit 0, the interrupt will be reenabled by writing a 0 to bit 0. This holds for DPM as well.

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) the current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt),

2) output data bits 5, 6 and 7 will be reset as appropriate,

3) future interrupts for the corresponding LOS or DPM will be prevented from occuring).

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 9 and 10. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (bits 5, 6 and 7) indicate LOS and DPM state changes. Writing a "1" to the "Clear LOS" and/or "Clear DPM" bits in the register also resets status bits 5, 6, and 7.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

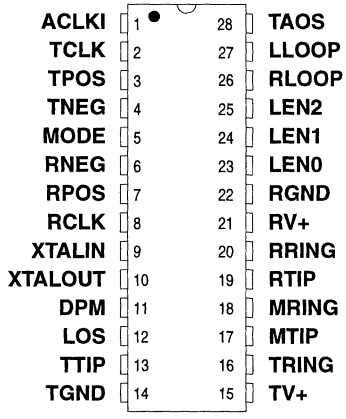
Table 9. Output Data Bits 0 - 4

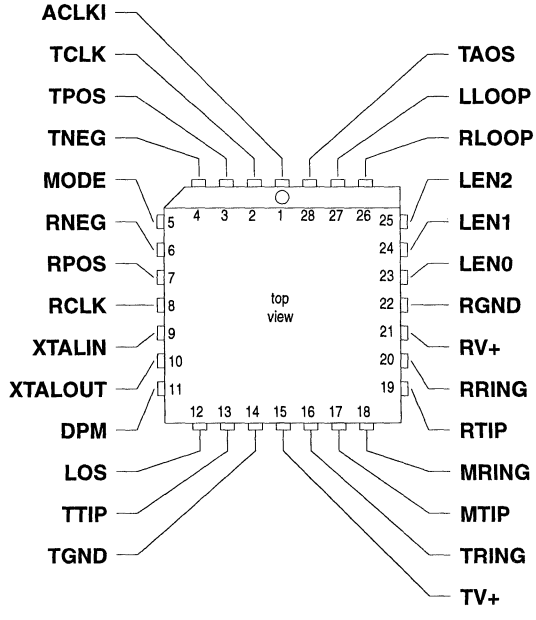
Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 10. Coding for Serial Output Bits 5, 6, 7

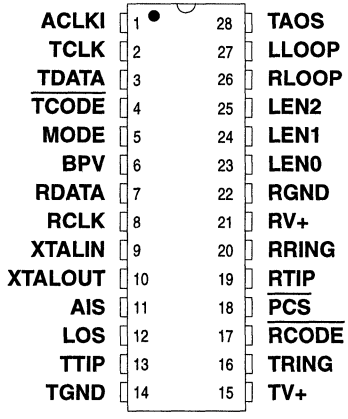
PIN DESCRIPTIONS

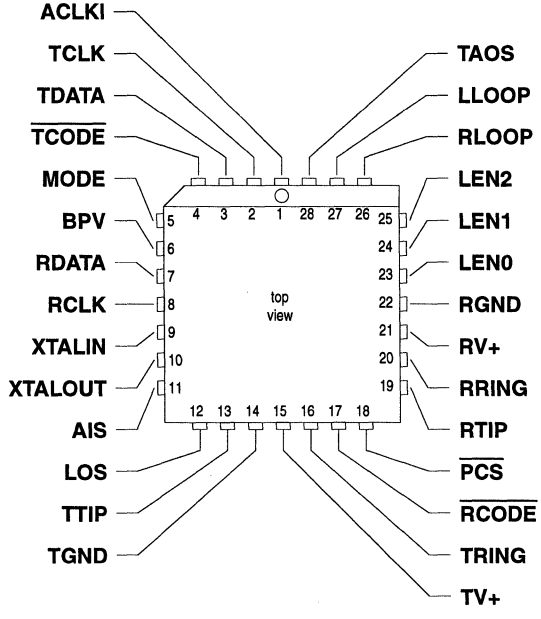
Hardware Mode



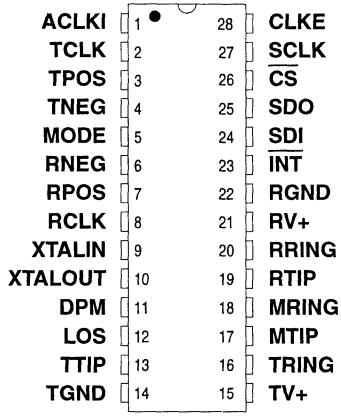


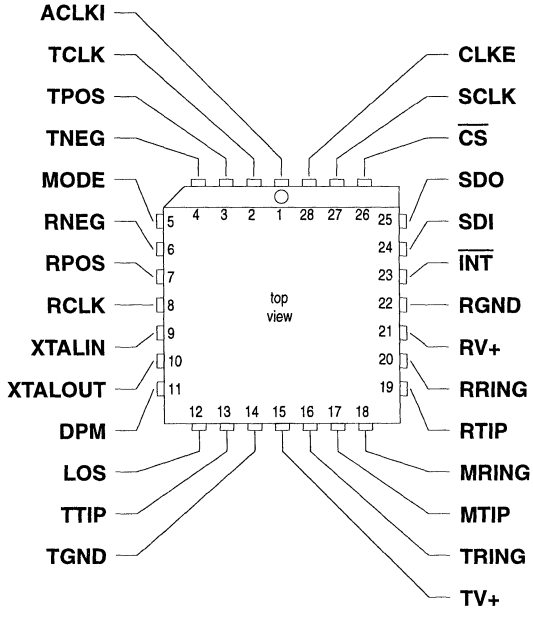
Extended Hardware Mode
(CS61535A only)





Host Mode


ACLKI 1
TCLK 2
TPOS 3
TNEG 4
MODE 5
RNEG 6
RPOS 7
RCLK 8
XTALIN 9
XTALOUT 10
DPM 11
LOS 12
TTIP 13
TGND 14
28 CLKE
27 SCLK
26 CS
25 SDO
24 SDI
23 INT
22 RGND
21 RV+
20 RRING
19 RTIP
18 MRING
17 MTIP
16 TRING
15 TV+


ACLKI
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12 13 14 15 16 17 18
24
23
22
21
20
19
top
view
CLKE
SCLK
CS
SDO
SDI
INT
RGND
RV+
RRING
RTIP
MRING
MTIP
TRING
TV+

Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Overdriving the oscillator with an external clock is not supported.

Control

ACLKI - Alternate External Clock Input, Pin 1.
For the CS61535 a 1.544 MHz (or 2.048 MHz for E1) clock must be input to ACLKI, which is used to calibrate the receiver clock recovery circuit. In a loss of signal state, the clock output, RCLK will equal the ACLKI frequency. Transmit All Ones Mode frequency is set by ACLKI. ACLKI may not be provided by RCLK.

The CS61535A does not require a clock signal to be input on ACLKI when a crystal is connected between pins 9 and 10. If a clock is not provided on ACLKI, this input must be grounded. If ACLKI is grounded, the oscillator in the jitter attenuator is used to calibrate the clock recovery circuit and TAOS is not available.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "Clear LOS" or "Clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes*)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode*.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes*)

Setting LLOOP to a logic 1 routes the transmit clock and data through to the receive clock and data pins. TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the CS61535A or CS61535 line interface in the Host Mode. In the host mode, a serial control port is used to control the CS61535A or CS61535 line interface and determine its status. Grounding the MODE pin puts the CS61535A or CS61535 line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 V puts the CS61535A in Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode*)

Setting $\overline{\text{PCS}}$ high causes the CS61535A line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode*)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes*)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored. In the Host Mode, simultaneous selection of RLOOP & TAOS enables a factory test mode for the CS61535.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

* Extended Hardware Mode available in CS61535A only.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes*)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLKI. In the Host Mode, simultaneous selection of RLOOP & TAOS enables a factory test mode for the CS61535.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode*)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock is output on this pin.

RDATA - Receive Data - Pin 7. (Extended Hardware Mode*)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

* Extended Hardware Mode available in CS61535A only.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode*)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK. Used only in the extended hardware mode of the CS61535A.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

3

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. In the CS61535A, this output is designed to drive a 75 Ω load. A 1:1, 1:1.15 or 1:1.26 transformer is required as shown in Figure A1.

In the CS61535, this output is designed to drive a 25 Ω load. A 1:2 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, a 4.4 Ω resistor should be added in series with the CS61535 transformer primary. The transmitter will drive twisted-pair cable, terminated with 100 Ω or 120 Ω, without additional components.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode*)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than 9 zeros out of 8192 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode*)

BPV goes high for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

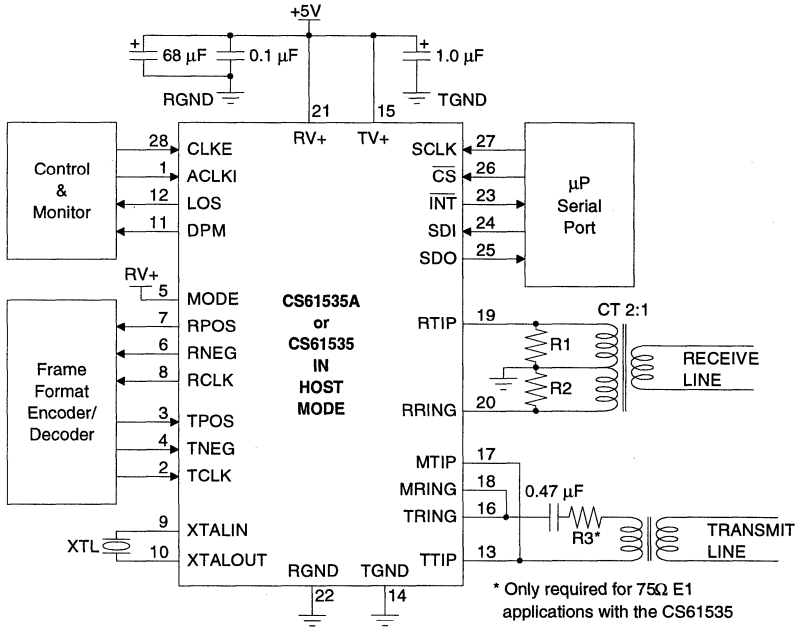
LOS goes high when 175 consecutive zeros have been received. For the CS61535A, LOS returns low when the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed by ANSI T1.231-1993. For the CS61535, LOS returns to low on the first bit received.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

These pins are normally connected to TTIP and TRING and monitor the output of a CS61535A or CS61535. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "Clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.

* Extended Hardware Mode available in CS61535A only.

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3 Ω	Transmit Transformer
CS61535	1.544	100	200	0	1:2
	2.048	120	240	0	1:2
	2.048	75	150	4.4	1:2
CS61535A	1.544	100	200	0	1:1.15
	2.048	120	240	0	1:1.26
	2.048	75	150	0	1:1

Figure A1. Host Mode Configuration

Line Interface

Figures A1-A3 show the typical configurations for interfacing the I.C. to a line through transmit and receive transformers. Note that the CS61535A transmitter transformer requirements have changed from those of the CS61535. This new transformer allows the CS61535A's lower power driver to be implemented.

The receiver transformer is center tapped and center grounded with resistors between the center tap and each leg on the I.C. side. These resistors provide the termination for the line.

Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer

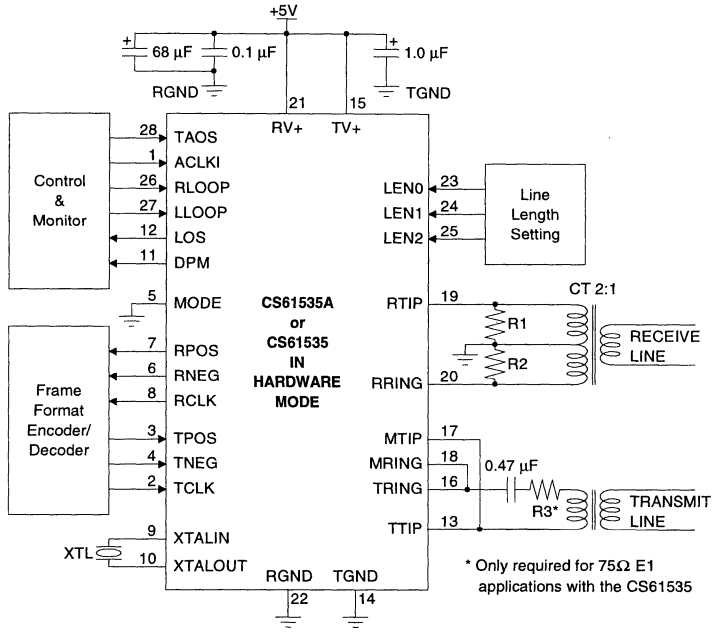


Figure A2. Hardware Mode Configuration

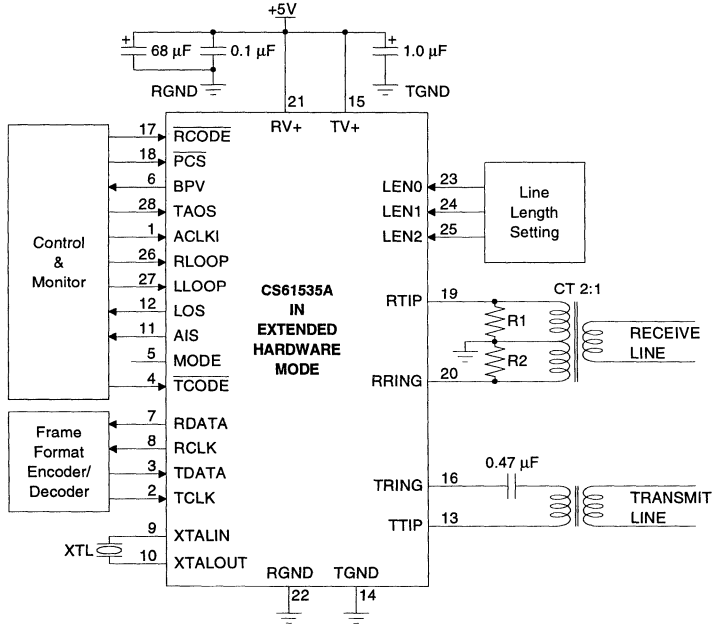


Figure A3. Extended Hardware Mode Configuration

tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61535A and CS61535. It is recommended that the CXT6176 from Crystal Semiconductor be used for T1 applications, and that the CXT8192 be used for E1 applications.

Interfacing The CS61535A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A4. In this case, the CS61535A and CS2180B are in Host Mode controlled by a microprocessor serial interface. If the CS61535A is used in Hardware Mode, then the CS61535A RCLK output must be inverted before being input to the CS2180B. If the CS61535A is used in Extended Hardware Mode, the CS61535A RCLK output does not need to be inverted before being input to the CS2180B.

CS61534 Compatibility

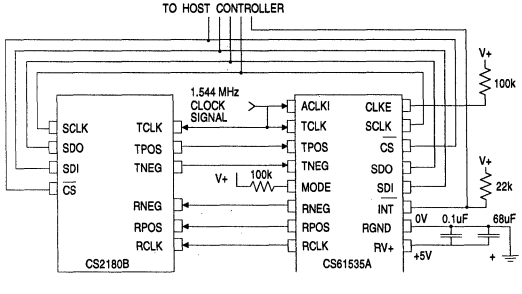


Figure A4. - Interfacing the CS61535A with the CS2180B (Host Mode)

The CS61535 and CS61535A are pin compatible with the CS61534. The CS61535 and CS61535A have greater jitter tolerance for both transmitter and receiver, and they provide more jitter attenuation starting at jitter frequencies of 6 Hz. The greater jitter tolerance and attenuation in the transmit path makes the CS61535 and CS61535A more suitable for CCITT demultiplexing applications where eight bits can be dropped from the clock/data stream at once. Similarly, these parts can be used in SONET applications with the addition of some external circuitry.

The main differences between the CS61535 and CS61535A relative to the CS61534 are:

1) On the CS61535 and CS61535A, selection of LEN 2/1/0 = 0/0/0 changes the voltage at which the receiver accepts an input as a pulse (slicing level) from 65% to 50% of the peak pulse amplitude. Lowering the data slicing level will improve receiver sensitivity at long cable lengths when the data is jittered. A 50% slicing level will also improve crosstalk sensitivity for channels where received pulses do not have undershoot.

2) There are differences in the functionality of the ACLKI (ACLK) input on the CS61534, CS61535 and CS61535A. ACKLI (ACLK) is used as the transmit clock in the transmit all ones (TAOS) mode. On the CS61535 and CS61535A, ACLKI is used as a calibration reference for the receiver clock recovery circuit and therefore may not be supplied by RCLK. On the CS61534, ACLK may be supplied by RCLK . If an external clock is not provide on the ACLKI input of the CS61535A, the crystal oscillator is used to calibrate the receiver clock recovery circuit. ACLKI on the CS61535 must be connected to an external timing reference.

3) On the CS61535 and CS61535A, the Host Mode status register bits 5, 6 and 7 are encoded so that state changes on LOS and DPM may be reported.

4) RCLK on the CS61534 has a 50% duty cycle, while RCLK on the CS61535 and CS61535A has a duty cycle which is typically 30% or 70%. Also, the CS61535 and CS61535A RCLK duty cycle and instantaneous frequency vary with received jitter and may exhibit 1/13 UIpp quantization jitter even when the incoming signal is jitter free.

5) The CS61535 and CS61535A require 25 ns of setup time on TPOS and TNEG before the falling edge of TCLK and 25 ns of hold time on these inputs after the falling edge of TCLK. The CS61534 requires 50 ns of hold time on TPOS and TNEG after the falling edge of TCL, and 0 ns of setup time.

6) LOS occurs after 31 consecutive zeros on the CS61534. For the CS61535A and CS61535 LOS occurs after 175 zeros.

7) Since the CS61535A and CS61535 receivers are continuously calibrated, there is no need to issue a reset to initialize the receiver timing as with the CS61534.

Using the CS61535A for SONET

The CS61535A can be applied to SONET VT1.5 and VT2.0 interface circuits as shown in Figure A5. The SONET data rate is 51.84 MHz, and has 6480 bits per frame (125 us per frame). An individual T1 frame (193 bits per frame) or PCM-30 frame (256 bits per frame) has its data mapped into the 6480 bit SONET frame. The mapping does not result in a uniform spacing between sucessive T1 (or E1) bits. Rather, for locked VT applications, gaps as large as 24 T1 bit periods or 32 E1 bit periods can exist between successive bits. With floating VTs, the gaps can be even larger.

The circuit in Figure A5 eliminates the demultiplexing jitter in a two-step approach. The first step uses a FIFO which is filled at a 51.84 MHz rate (when T1 or E1 bits are present), and which is emptied at a sub-multiple of the 51.84 rate. The FIFO is emptied only when it contains data. When the FIFO is empty the output clock is not pulsed.

The sub-multiple rate chosen should be slightly faster than the target rate (1.544 or 2.048 MHz), but as close to the target rate as possible. For locked VT operation, Table A1 shows potential sub-multiple data rates, and the impact on those rates on the maximum gap in the output clock of the FIFO, and depth of FIFO required. FIFO depth will have to be increased for floating VT

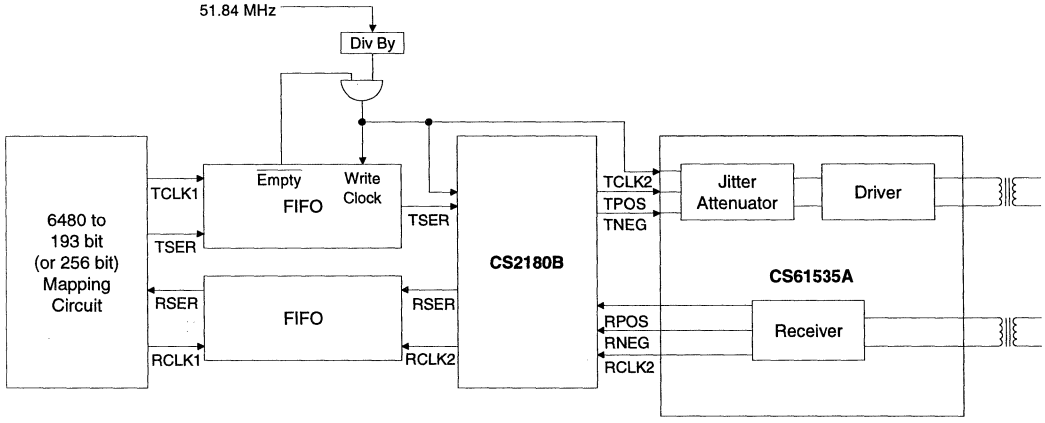


Figure A5.-SONET Application

operation, with 8 bits of FIFO depth being added for each pointer alignment change that can occur.

The objective that should be met in picking a FIFO depth and clock divider is keep the maximum gap on the output of the FIFO at 12 bits or less. Twelve bits is the maximum jitter which can be input to the CS61535A's jitter attenuator without causing the overflow/undeflow protection circuit to operate. The CS61535A then removes the remaining jitter from the signal.

The receive path also requires a bit mapping (from 193 or 256 bits to 6480 bits). This mapping requires an input buffer with the same depth as use on the transmit path. This buffer also absorbs the output jitter generated by the CS61535A's digital clock recovery.

Transformers

Recommended transmitter and receiver transformer specifications for the CS61535 and CS61535A are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61535. The transformers in Table A4 have been tested and recommended for use with the CS61535A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications with the CS61535A where it is advantageous to use a single transmitter transformer for both 75Ω and 120Ω E1 applications, a 1:1.26 transforer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct across a 75 Ω load.

Target Rate (MHz)	Clock Divider	Resultant Rate (MHz)	Maximum Gap		FIFO Depth Required
			(µs)	bits	
1.544	32	1.620	6.2	10	21
1.544	33	1.571	3.9	6	26
2.048	25	2.074	3.4	7	34

Table A1. Locked VT FIFO Analysis

Parameter	CS61535 Receiver & Transmitter CS61535A Receiver	CS61535A Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 120 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 75 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kVsurface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers For The CS61535

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A4. Recommended Transformers For The CS61535A

•Notes•

Semiconductor Corporation

CS61544

T1 Line Interface

Features

- Provides Analog T1 Line Interface
- Fully Compatible with CB119, Publication 43802, & TR-TSY-000009
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Implements ISDN Primary Rate and DMI Interface
- Diagnostic and Performance Monitoring Features
- Selectable B8ZS Encode/Decode
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61544 combines the analog transmit and receive line interface functions for a T1 system interface in one 28 pin device. The T1 line interface operates from a single 5V supply, is transparent to the T1 framing format, and can work with ABAM and other cable types.

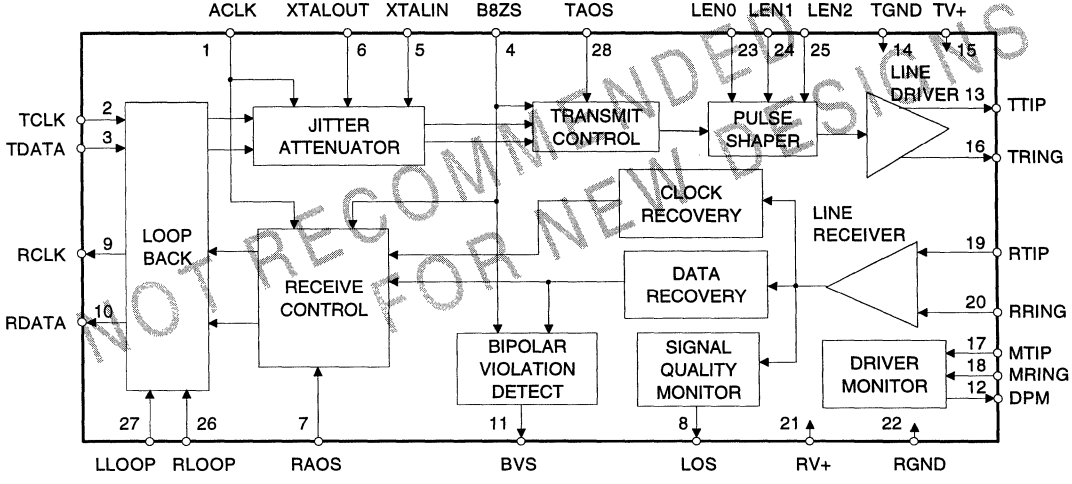
Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for the line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

Applications

- Interfacing Networking Equipment such as M13 Multiplexers to a DSX-1 Cross Connect.
- Interfacing fiber optic transmission equipment to T1 lines.

ORDERING INFORMATION

CS61544-IP	-	28 Pin Plastic DIP
CS61544-ID	-	28 Pin Cerdip
CS61544-IL	-	28 Pin PLCC (j-leads)



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to GND)	RV+ TV+	-	6.0	V
Input Voltage, Any Pin	(Note 1)	V_{in}	(RGND) - 0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 1 & 2)	I_{in}	-	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Excluding RTIP and RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Total Power Dissipation 100% ones density & max. line length @ 5.25V	(Note 4)	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25Ω load, over operating temperature range. Includes CS61544 and load.

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Pins 1-5, 7, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	'Pins 1-5, 7, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA	(Note 5) Pins 6, 8-12	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA	(Note 5) Pins 6, 8-12	V_{OL}	-	-	0.4	V
Input Leakage Current			-	-	±10	µA

Note: 5. Output drivers will output CMOS logic levels into a CMOS load.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = -40° to +85 °C; V+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
AMI Output Pulse Amplitudes	Measured at the DSX	2.4	3.0	3.6	V_{0-p}
Load Presented to Transmitter Output	(Note 6)	-	25	-	Ω
Power in 2kHz band at 772kHz	(Note 7)	12.6	15	17.9	dBm
Power in 2kHz band about 1.554MHz (referenced to power at 772kHz)	(Note 7)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 7)	-	0.2	0.5	dB
Input Jitter Tolerance-Transmitter		7.0	-	-	U.I.
Jitter Attenuation Curve Corner Frequency	(Note 8)	-	-	50	Hz
Loss of Signal Threshold		-	0.5	-	V
Receiver Sensitivity Below DSX-1	(2.4V)	-10	-	-	dB
Receiver Jitter Tolerance	(Note 9)				
8kHz - 40kHz		0.1	-	-	U.I.
10Hz - 500Hz		5	-	-	U.I.

Notes:
6. On the CS61544 side of the 2:1 transformer, with a 100Ω impedance line attached to the secondary.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter. Slope above corner frequency is -20dB/decade. See Figure 5.
9. For CERDIP ICs, assumes IC is operated within -70° to +70° C of reset temperature. For Plastic ICs, assumes IC is operated within -25° to +40° C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1 V of reset V+. Input data pattern is quasi-random: (2↑20) - 1 with 1-in-15. Between 500 Hz and 8 kHz the jitter tolerance will be better than the AT&T 43802 line shown in Figure 7.

SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5.0V ±5%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 10)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 11)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 12)	t_{pwl}	-	324	-	ns
Duty Cycle	(Note 13)		-	50	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	274	-	ns
Reset Pulse Duration			0.2	-	2000	µs

Notes: 10. Crystal must meet specifications described in CXT6176 data sheet.
11. ACLK provided by an external source.
12. The sum of the pulse widths must always meet the frequency specifications.
13. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
14. At max load of 1.6 mA and 50 pF.

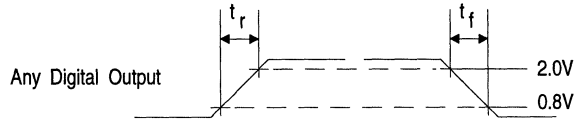


Figure 1 - Signal Rise and Fall Characteristics

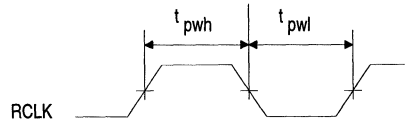


Figure 2 - Clock Signal Quality

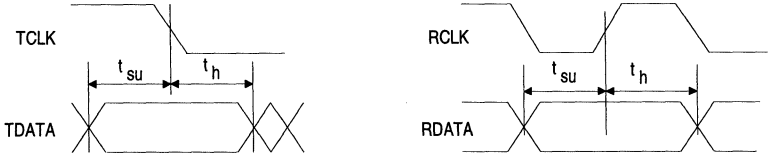


Figure 3 - Switching Characteristics

Note that when externally looping RCLK back into TCLK, RCLK must be inverted.

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS61544 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew-rate-controlled fast digital-to-analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver drives a 25Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the B8ZS and TDATA should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0, LEN1, LEN2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

B8ZS coding can be inserted into the data stream using the B8ZS select feature. This feature replaces every string of eight consecutive zeros with a pulse train containing bipolar violations. The violations can then be decoded at the receive end and the original data recovered.

Transmit Line Length Selection

Line length selection can be controlled by an intelligent controller or hard-wired with a switch which is set at the time of installation. The line length selection supports both a three-partition arrangement for ICOT and MAT cable, and a five-partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61544 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	0	0	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM (AT&T 600B & 600C series)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	

Table 1 - Line Length Selection

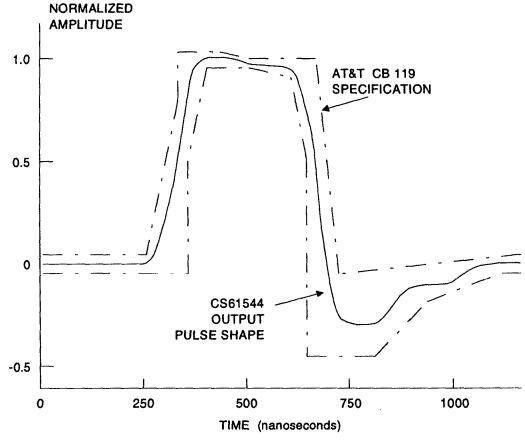


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Transmit Jitter Attenuator

The 61544 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a T1 signal. Figure 5 shows a family of curves which show the jitter attenuation achieved by the 61544. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 6 and 7.

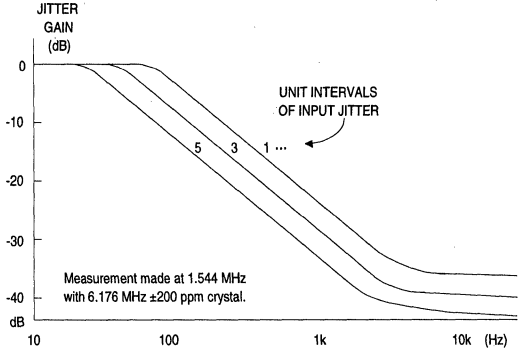


Figure 5 - CS61544 Jitter Attenuation Curves

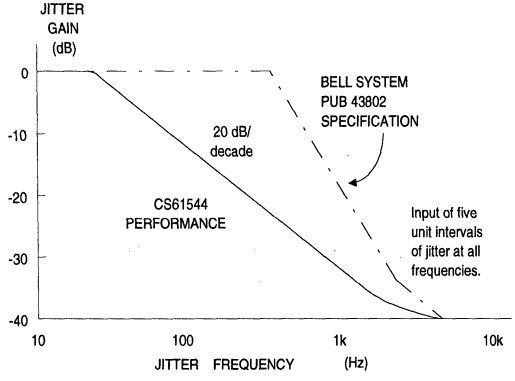


Figure 6 - Jitter Attenuation Characteristics

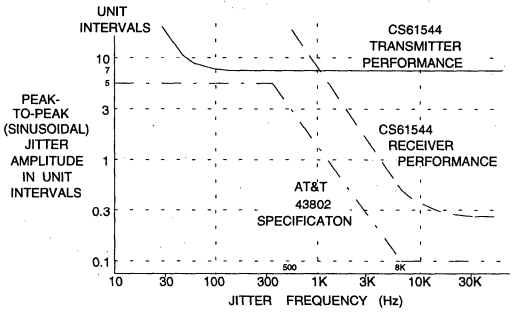


Figure 7 - Typical Input Jitter Tolerance of Transmitter and Receiver

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is exactly four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. (The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together). Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock. The TDATA and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61544 side. Data on RDATA is stable and may be sampled on the rising edge of the recovered clock, RCLK. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802.

The two leads of the receiver transformer have opposite polarity and drive the receiver inputs RTIP and RRING differentially. Comparators detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61544, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO frequency is near the reference frequency. This current is then held constant. The FPLL has small signal control from the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61544 will optimize receiver performance for the operating power supply and temperature.

The received signal is monitored to detect bipolar violations. If a bipolar violation is detected, a positive strobe (BVS) is output with a width of one half the clock period.

The receiver has the capability to decode signals which have been transmitted with B8ZS bipolar violations. This feature is enabled when B8ZS (pin 4) goes high. Recovered data is processed by B8ZS decode (if enabled) and sent to the output. The bipolar violation detection algorithm is also modified to not detect the B8ZS encoded violation as an error.

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RDATA is not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output, but may drift up to ± 6% from 1.544 MHz.

Receive All Ones Select

Receive all ones is selected when RAOS goes high. If receive all ones is selected when the local loopback is not in effect, continuous ones are sent to RDATA using the alternate clock, ACLK, for timing. The alternate clock, ACLK, is sent to RCLK. (The transmit clock, TCLK, can be used as the alternate clock by connecting pins 1 and 2 together.) If it is desirable to have all ones automatically replace recovered data (at RDATA) upon loss of signal, then RAOS and LOS should be tied together (pins 7 and 8).

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. Any RAOS request is overridden (see Table 2). The transmit clock and data signals, TCLK and TDATA are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case continuous ones are transmitted on the line at the rate determined by ACLK.

LLOOP Input Signal	RAOS Input Signal	Source of Data for RDATA	Source of Clock for RCLOCK
0	0	RTIP & RRING	RTIP & RRING
0	1	all 1s	ACLK
1	X	TDATA	TCLK

Table 2 - Interaction of LLOOP and RAOS

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 3). The recovered incoming signals are also sent to RCLK and RDATA unless receive all ones (RAOS) is selected, in which case continuous ones and an alternate clock are sent to RDATA and RCLK. Remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see *Reset*).

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV at least once within 32±2 cycles. The driver performance monitor is not designed to detect broken printed ciruit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING.

DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61544 cannot be used to monitor the TTIP/TRING pins of a CS61574A, CS61535A, CS6158A, or CS61575.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X - Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicated that Loopback or All Ones option is selected.

Table 3 - Interaction of RLOOP and TAOS

Reset

The CS61544 initiates internal reset procedures either upon power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training proceedure for the FPLL. **It is strongly recommended that a hardware reset request be issued after the power supply has stabilized and signals have been applied to the device to insure that the FPLL is correctly trained.** Training the FPLL takes at most 43 ms, but typically requirès less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

During the reset procedure, the loss of signal indicator is high. Once the reset procedures are completed, the loss of signal indicator goes low, signifying that normal operation of the device has begun.

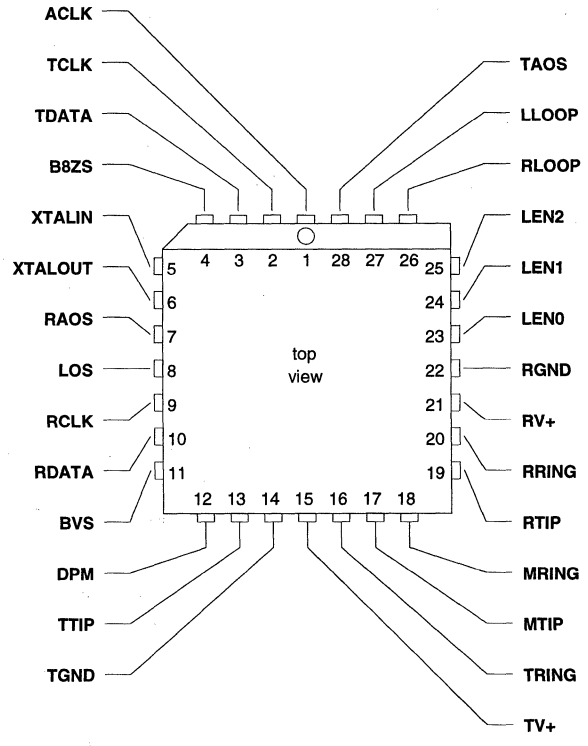
Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. These capacitors should be located physically close to the device. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61544 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	**ACLK**	1	28	**TAOS**	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	**TCLK**	2	27	**LLOOP**	LOCAL LOOPBACK
TRANSMIT DATA	**TDATA**	3	26	**RLOOP**	REMOTE LOOPBACK
B8ZS ENABLE	**B8ZS**	4	25	**LEN2**	BIT 2 OF LINE LENGTH SELECT
CRYSTAL INPUT 2	**XTALIN**	5	24	**LEN1**	BIT 1 OF LINE LENGTH SELECT
CRYSTAL INPUT 1	**XTALOUT**	6	23	**LEN0**	BIT 0 OF LINE LENGTH SELECT
RECEIVE ALL ONES SELECT	**RAOS**	7	22	**RGND**	RECEIVE GROUND
LOSS OF SIGNAL	**LOS**	8	21	**RV+**	RECEIVE V+ (+5V DC)
RECOVERED CLOCK	**RCLK**	9	20	**RRING**	RECEIVE RING
RECEIVE DATA	**RDATA**	10	19	**RTIP**	RECEIVE TIP
BIPOLAR VIOLATION STROBE	**BVS**	11	18	**MRING**	MONITORED RING
DRIVER PERFORMANCE MONITOR	**DPM**	12	17	**MTIP**	MONITORED TIP
TRANSMIT TIP	**TTIP**	13	16	**TRING**	TRANSMIT RING
TRANSMIT GROUND	**TGND**	14	15	**TV+**	TRANSMIT V+ (+5V DC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Inputs, Pins 5 and 6.
A 6.176 MHz crystal should be connected across these pins. An externally generated 6.176 MHz clock signal may be put into the XTALIN pin, disabling the jitter attenuator. This clock must be *exactly* four times the frequency at TCLK. See the CXT6176 data sheet for more information on crystals.

Control

B8ZS - B8ZS Encoding Enable, Pin 4.
Setting B8ZS to a logic 1 enables B8ZS encoding of the transmit data and B8ZS decoding of the receive data.

RAOS - Receive All Ones Select, Pin 7.
Setting RAOS to a logic 1 causes continuous ones to be sent to RDATA at the frequency determined by ACLK.

TAOS - Transmit All Ones Select, Pin 28.
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. Any RAOS request is ignored. TCLK and TDATA are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RDATA unless overridden by a RAOS request. Any TAOS request is ignored. If the oscillator is being driven with a 4X clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accomodate several cable types and lengths. See Table 1 for information on line length selection.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 MHz clock. The frequency of ACLK determines the rate at which TAOS and RAOS are output.

TCLK, TDATA - Transmit Clock, Transmit Data, Pins 2 and 3.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The receive AMI signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A3. Data and clock are recovered and output on RDATA and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61544. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Outputs

RCLK, RDATA - Recovered Clock, Receive Data, Pins 9 and 10.

Data and clock are recovered from the RTIP and RRING inputs and output at these pins. RDATA is valid on the rising edge of RCLK.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI, T1 signal is driven to the line through these pins. This output is designed to drive a 25Ω load. A 2:1 step-up transformer is required to drive the line as shown in Figure A1.

Status

LOS - Loss of Signal, Pin 8.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles with out a detected one. LOS returns to logic 0 when the signal returns.

BVS - Bipolar Violation Strobe, Pin 11.

BVS goes to a logic 1 when a bipolar violation is detected in the received signal. The strobe is approximatly 324 ns wide and aligned with the rising edge of RCLK. The strobe will occur concurrently with the RDATA output for which the violation was detected. The bipolar violation detection algorithm is modified when B8ZS is selected to accept B8ZS encoded data.

DPM - Driver Performance Monitor, Pin 12.

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

APPLICATIONS

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61544. It is recommended that the Crystal Semiconductor CXT6176 be used with the CS61544.

General Applications

Figure A1 shows the typical configuration for the CS61544, including transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200Ω resistors between the center tap and each leg on the CS61544 side. These resistors provide the 100Ω termination for the T1 line. Line Length Select pins are shown in a manual switching configuration. These inputs can be controlled by logic circuitry if desired.

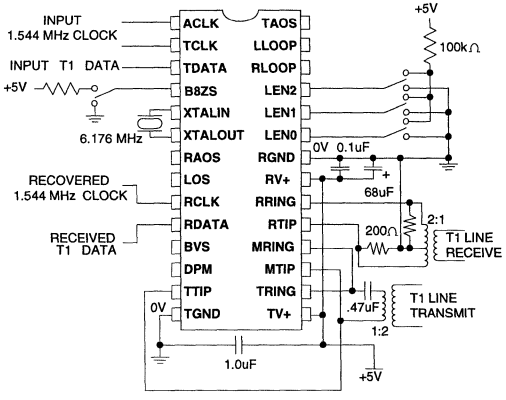


Figure A1. Typical Configuration Showing Line Interface

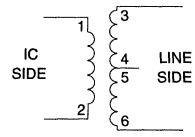
Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS61544. Figure A2 shows the connections for some of the transformers mentioned in the Table A1. The transformers should be placed physically close to the CS61544.

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A1. Suitable Transformers



Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

Figure A2. Transmitter Transformer Configuration

Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1)±5%

Primary inductance: 600 µH min measured at 772 khz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary

ET-Constant: 16 V-µs min for T1;

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect

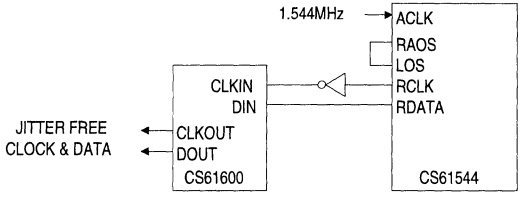


Figure A3. Receiver Jitter Attenuation

be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A3.

Maintaining Recovered Clock

Figure A3 also shows how the recovered clock, RCLK, can be maintained within desired specifications in the event that the received AMI signal is lost. This design requires a locally generated 1.544 MHz clock whose frequency is within the required system specifications. This clock is input to the ACLK input of the CS61544. The loss of signal output, LOS, is connected to the receive all ones select input, RAOS.

If the AMI signal is lost, the LOS signal goes high, taking RAOS high, directing the CS61544 to output all ones at RDATA at the frequency determined by ACLK (i.e. RCLK = ACLK). The CS61600 will buffer any instantaneous phase or frequency change at the RCLK and RDATA pins, retaining clock integrity. This type of circuit is necessary since the frequency/phase lock loop in the CS61544 may drift when the AMI signal is lost.

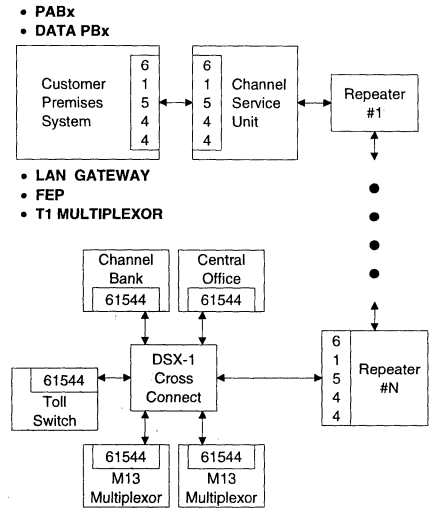


Figure A4. Applicable Types of Connection

If the receiver input returns, LOS goes low, deselecting RAOS, and returning the circuit to its normal operating status. It is important to note that LOS will go low as soon as a valid pulse is detected, which is before the receiver has locked onto the incoming signal. It is advisable to delay the transition from RAOS to the receiver output for a few milliseconds after LOS indicates receipt of signal.

Applicable Systems

Figure A4 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A4, the CS61544 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and is applicable in network equipment that connects to a DSX-1 cross connect.

Interfacing The CS61544 With T1 Digital Transceivers

To interface with the CS2180A, connect the devices as shown in Figure A5. When RPOS is tied to RNEG, B8ZS encoding/decoding and bipolar

violation detection functions are performed by the CS61544.

Test and Evaluation of the CS61544

When connecting the receive clock and data, RCLK and RDATA, to the transmit clock and data, TCLK and TDATA, of the CS16544, be sure to invert the clock signal.

Transmitter or Receiver Function Only

If the CS61544 is used for transmit only, tie RTIP and RRING high through a resistor, ground RAOS, RLOOP, and LLOOP, and float the outputs. To configure the device for receive only, float TTIP, TRING, TV+ and TGND, ground TAOS, TCLK, TDATA, RLOOP, LLOOP and LEN0/1/2 .

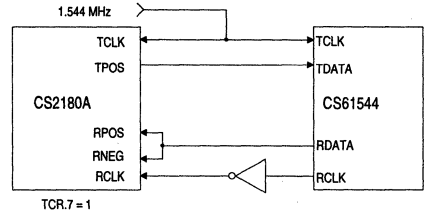


Figure A5. Interfacing CS61544 with CS2180A

Semiconductor Corporation

CDB61544

PCM Line Interface Demonstration Board

Features

- Socketed CS61544
- Complete Line Interface Function
- Slide Switch Control of Digital Inputs
- Reset Circuit

General Description

The board comes with a socketed CS61544 IC plus all the discretes so that the CS61544's performance can be verified in the lab without having to first build a breadboard.

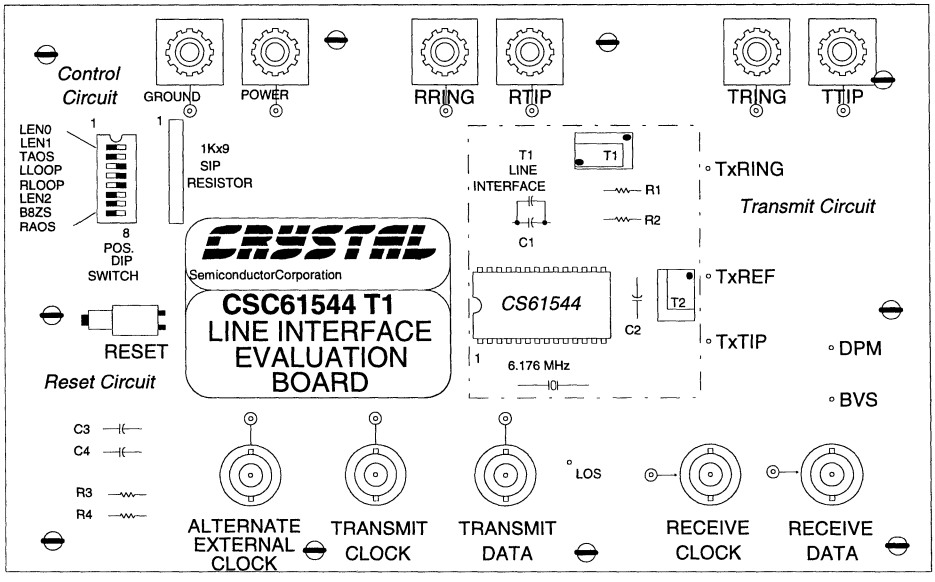
The board has four banana connectors for connecting two 100 ohm twisted pair cables to the line transformers present on the board. Two other banana connectors allow for easy connection of an external five volt power supply. Power supply decoupling capacitors are resident on the board. BNC connectors allow easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. Testing terminals provide access to the Serial Control Interface, DPM, MTIP, MRING, TTIP, TRING, LOS, and center tap of the transmit transformer.

Additional components provided on the board are a crystal, a reset circuit, and a DIP switch for controlling the input pins: LEN0, LEN1, LEN2, TAOS, RLOOP, LLOOP, B8ZS, and RAOS.

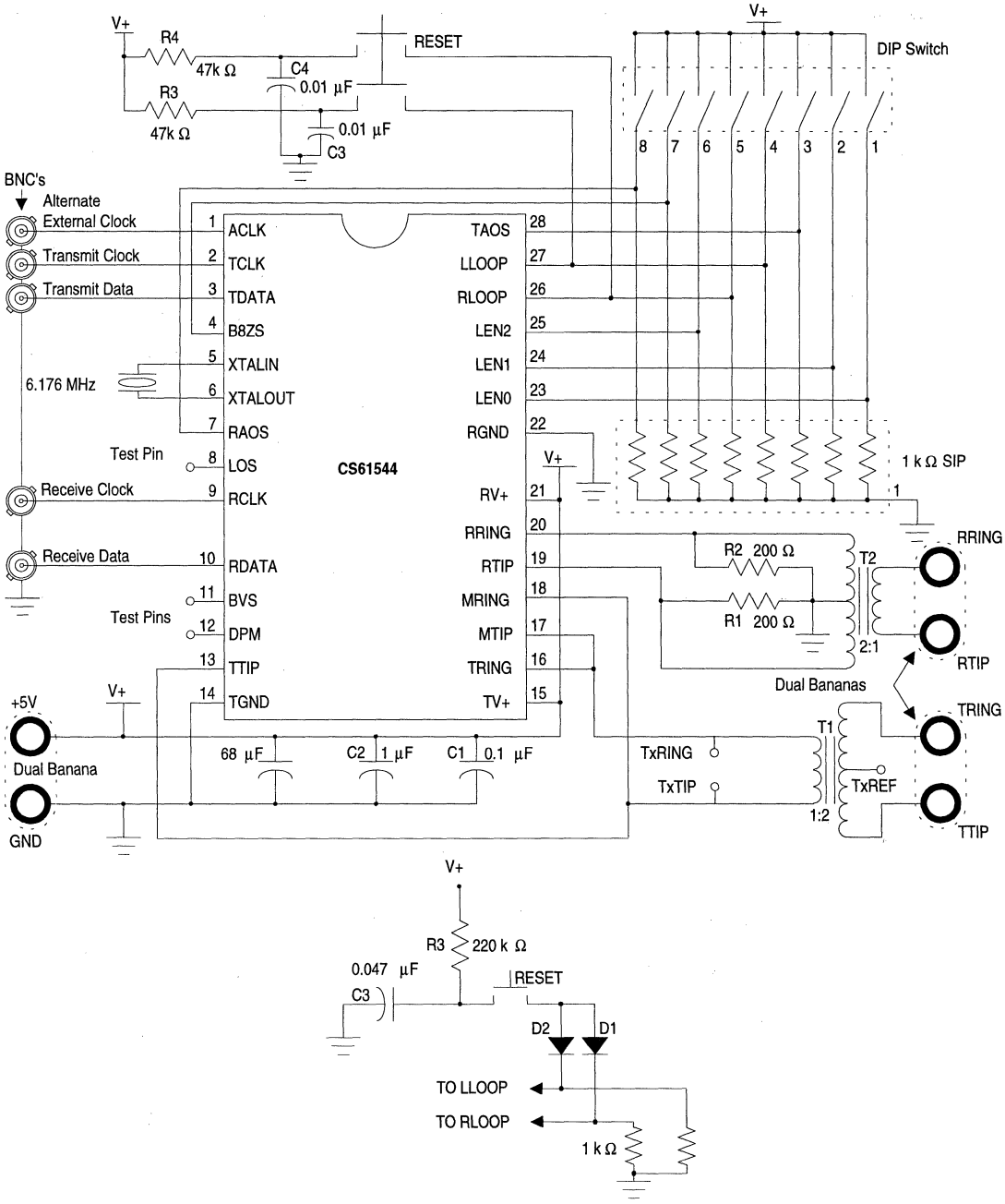
ORDERING INFORMATION: CBD61544

3

BOARD LAYOUT



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 TWX: 910-874-1352



NEW AND IMPROVED RESET CIRCUIT
(NOT PROVIDED, BUT RECOMMENDED FOR SIMILAR DESIGNS)

Semiconductor Corporation

CS61574

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Diagnostic Features
- Microprocessor Controllable
- Has the same pin-out and uses the same external components as the CS61577. The CS61577 has performance advantanges over the CS61574.

General Description

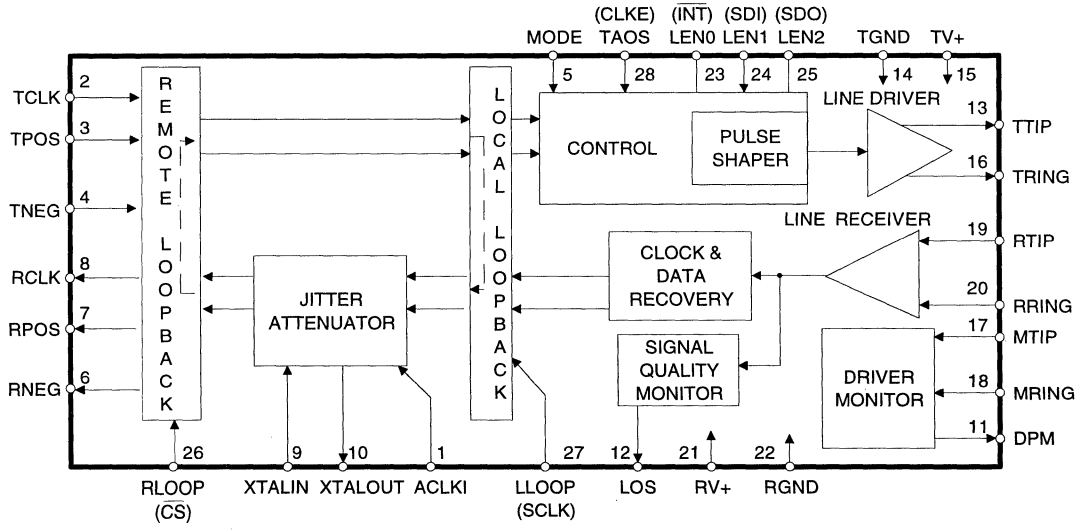
The CS61574 combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device. The CS61574 supports processor-based or stand-alone operation and interfaces with industry standard T1 and E1 framers.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The transmitter internally shapes output pulses according T1 DSX-1 and E1 template specifications.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION - See page 3-217.



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to GND	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4,5)	P_C	-	620	760	mW
Power Consumption	(Notes 4,6)	P_C	-	400	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (T_A = -40° to 85°C; TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA PINS 6-8, 11, 12, 23, 25	(Note 8)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	(Note 8)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)			-	-	±10	µA

Notes:
7. Functionality of pins 23 and 25 depends on the mode. See Operating Modes description.
8. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 9)				
E1, 75 Ω	(Note 10)	2.14	2.37	2.6	V
T1, Part 68; E1, 120 Ω	(Note 11)	2.7	3.0	3.3	V
T1, DSX-1	(Note 12)	2.4	3.0	3.6	V
Recommended Output Load at TTIP and TRING		-	25	-	Ω
Jitter Added During Remote Loopback	(Note 13)				
10Hz - 8kHz		-	0.005	-	UI
8kHz - 40kHz		-	0.008	-	UI
10Hz - 40kHz		-	0.010	-	UI
Broad Band		-	0.015	-	UI
Power in 2kHz band about 772kHz	(Notes 14, 15)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Note 14, 15)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 14, 15)	-	0.2	0.5	dB
Receiver					
Sensitivity Below DSX (0dB = 2.4V)		-13.6	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold T1 pulse settings		-	65	-	% of peak
E1, LEN2/1/0 = 000 or 010		-	50	-	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 16)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 15, 17)	-	6	-	Hz
Attenuation at 10kHz Jitter Frequency	(Notes 15, 17)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 15, 17)	12	23	-	UI

Notes:
9. Using transformer recommended in the Application Section.
10. This amplitude is measured at the output of the transformer for line length setting LEN2/1/0 = 000 (see Figure 8) with a 4.4 Ω resistor in series with TTIP.
11. These amplitudes, measured at the output of the transformer for line length setting LEN2/1/0 = 000 or LEN210 = 010.
12. These amplitudes, measured at the DSX-1 Cross-Connect, are for all line length settings from LEN2/1/0 = 011 to LEN2/1/0 = 111 (see Figure 7).
13. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
14. Typical performance with a 0.47µF capacitor in series with primary of transmitter output transformer.
15. Not production tested. Parameters guaranteed by design and characterization.
16. Jitter tolerance increases at lower frequencies. See Figure 10.
17. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 11.
    Output jitter can increase significantly when more than 12 UI's are input to the attenuator.
    See discussion in Wander and Jitter Attenuator section.

T1 SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 18)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 19)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	274	-	ns

PCM-30 SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 18)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 22)	t_{pwh2}/t_{pw2}	44	50	53	%
ACLKI Frequency	(Note 19)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	194	-	ns

Notes: 18. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
19. ACLKI provided by an external source or TCLK.
20. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
21. At max load of 1.6 mA and 50 pF.
22. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK.

SWITCHING CHARACTERISTICS (T_A = -40° to 85°C; TV+, RV+ = ±5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 23)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Notes: 23. Output load capacitance = 50pF.

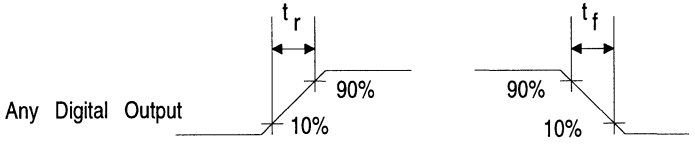


Figure 1. Signal Rise and Fall Characteristics

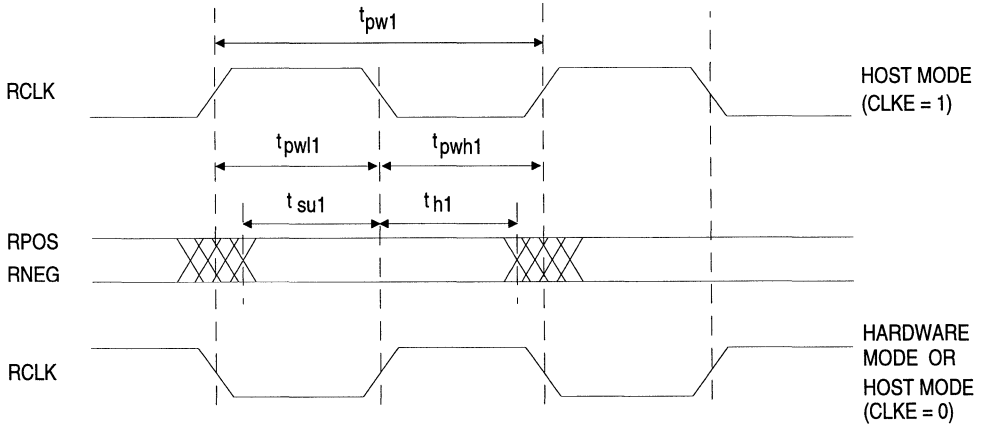


Figure 2. Recovered Clock and Data Switching Characteristics

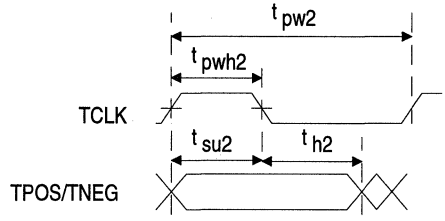


Figure 3. Transmit Clock and Data Switching Characteristics

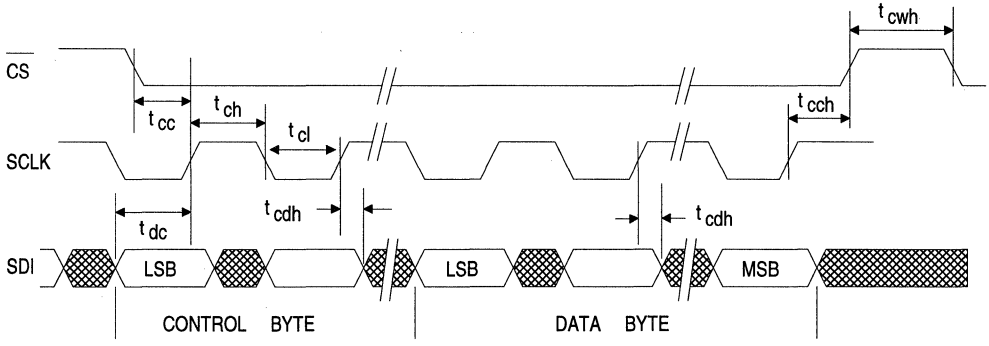


Figure 4. Serial Port Write Timing Diagram

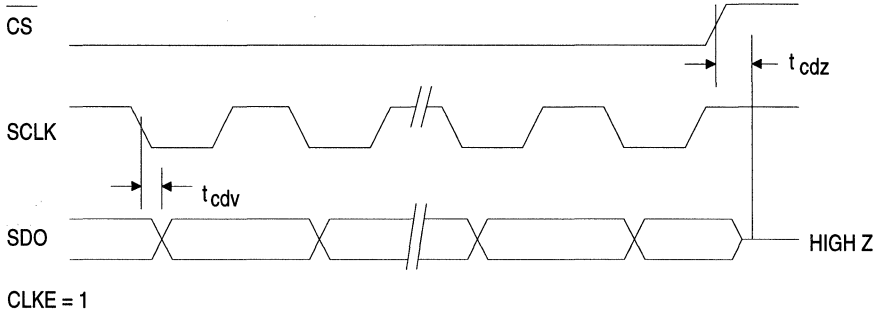


Figure 5. Serial Port Read Timing Diagram

THEORY OF OPERATION

Introduction to Operating Modes

The CS61574 supports two operating modes (as selected by pin MODE) as shown in Figure 6, and Figures A1 and A2 of the applications section.

The modes are Hardware Mode, and Host Mode. In Hardware Mode, discrete pins are used to interface the device's control functions and status information. In the Host Mode, the line interface is connected to a host processor and a serial data bus is used for input and output of control and status information

Transmitter

The transmitter takes data from a T1 (or E1) terminal, and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

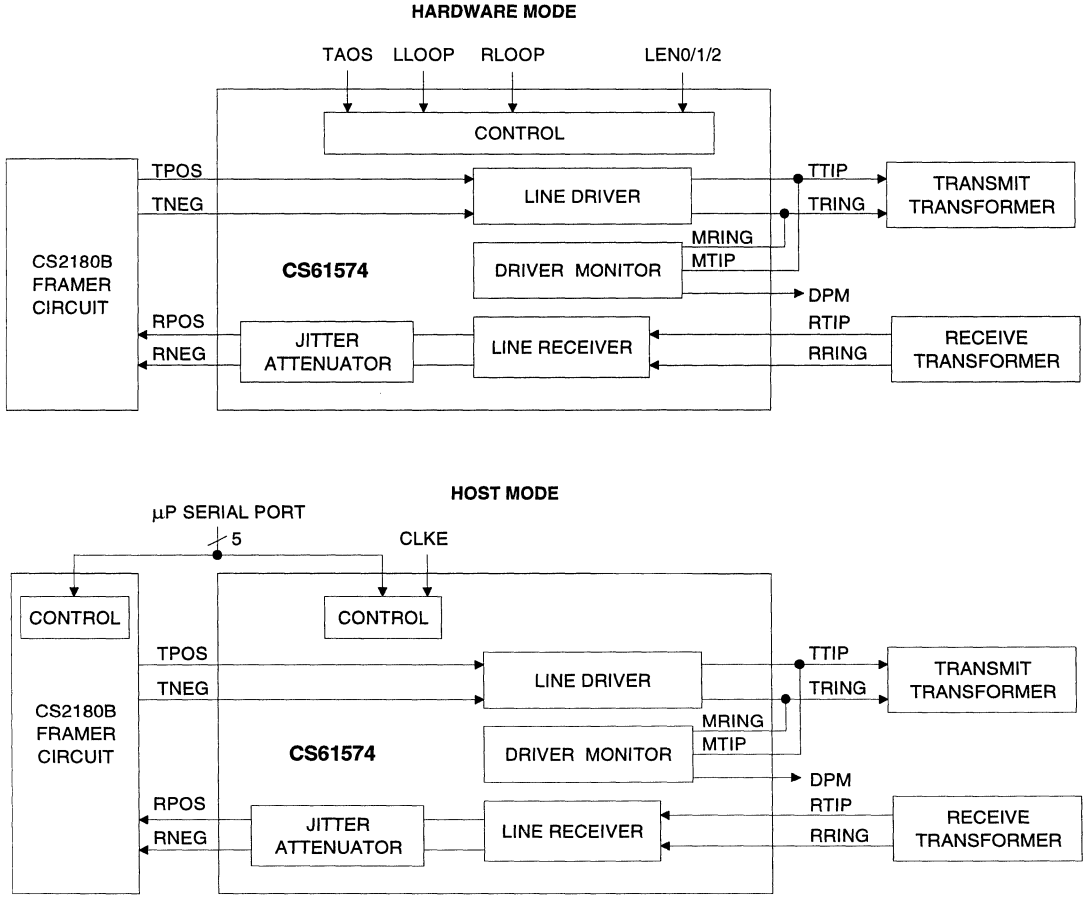


Figure 6. Overview of Operating Modes

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	0	75Ω (with 4.4Ω resistor) & 120 Ω	E1 CCITT G.703
0	0	1		RESERVED
0	1	0	FCC PART 68, OPT. A	NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1. Line Length Selection

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS61574 drives a 25 Ω load.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 7. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

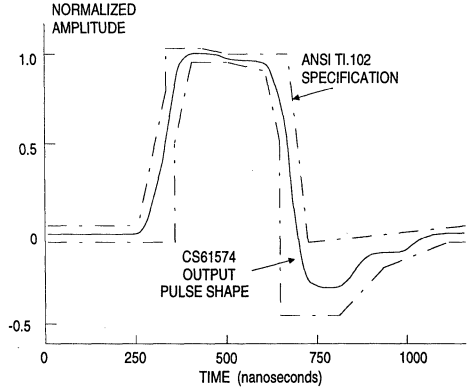


Figure 7. Typical Pulse Shape at DSX-1 Cross Connect

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns).

The CCITT G.703 E1 output pulse shapes supported with line length selection LEN2/1/0=0/0/0. For 75Ω E1 applications a 4.4Ω resistor is required in series with the TTIP or TRING pins as shown in Figure A1.

Note that for LEN2/1/0=000, the transmitter pulse width is determined by the high time of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 8, and specified in Table 2, assuming the TCLK duty cycle and frequency are appropriate.

If the clock signal is removed from TCLK on the CS61574, TPOS and TNEG should both be low during the last falling edge of TCLK.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter

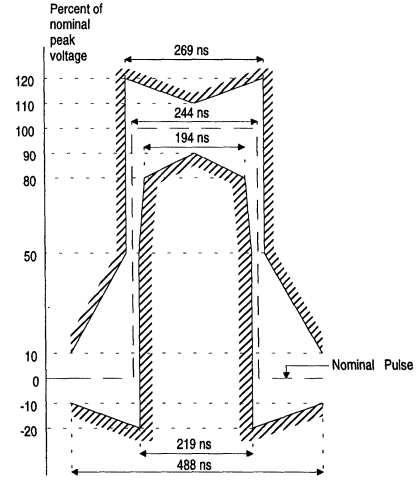


Figure 8. Mask of the Pulse at the 2048 kbps Interface

outputs may not meet all data sheet specifications for 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411-1990, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 9. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for PCM-30, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 10. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transfromer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, and A2

Table 2. CCITT G.703 Specifications

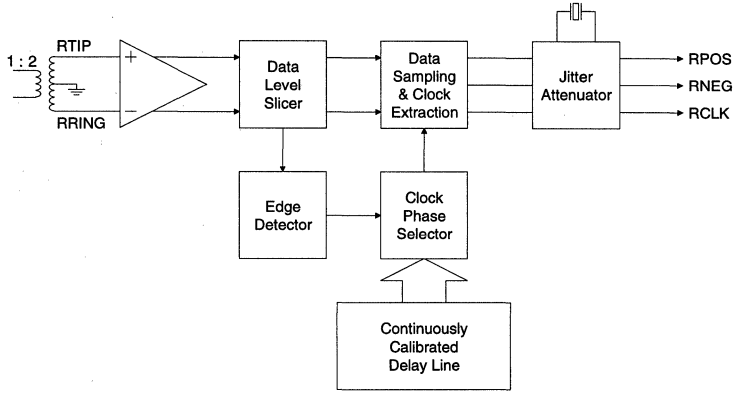


Figure 9. Receiver Block Diagram

its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated relative to a reference clock, which is provided by the crystal oscillator. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 3. Data Output/Clock Relationship

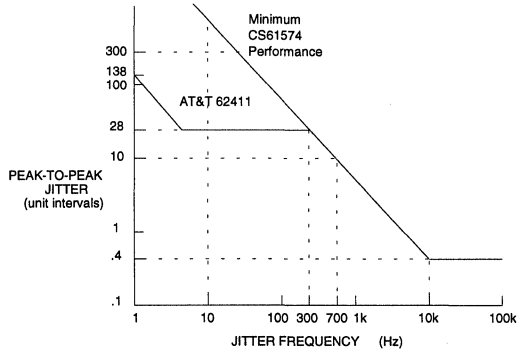


Figure 10. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

Loss of Signal

The receiver will indicate loss of signal upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. The zero input level is determined either when zeros are received, or when the received signal amplitude degrades below a $0.3V_{peak}$ threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$. LOS will go low (and flag the $\overline{INT}$ pin again if the serial I/O is used) when a valid signal is detected. Note that in the host mode, LOS is simultaneously available from both the register and pin 12. Table 4 shows

the status of RCLK upon LOS. Received data is output on RPOS/RNEG regardless of LOS status.

LOS returns to logic zero when the first one is received. ACLKI serves no significant purpose and should be grounded.

Crystal Present?	ACLKI Present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	RTIP/RRING via Jitter Attenuator

Table 4. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 11. The CS61574 will have a discontinuity in the jitter transfer function when the incoming jitter amplitude exceeds approximately 23 UIs.

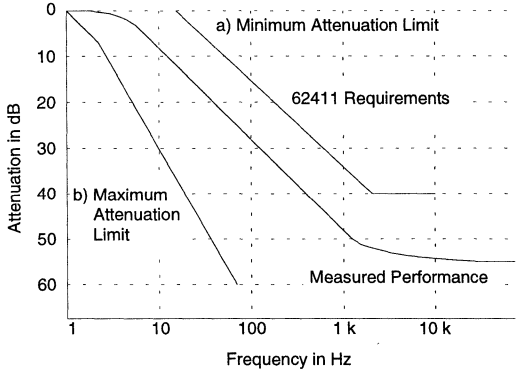


Figure 11. Typical Jitter Transfer Function

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG. The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG. If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on the line, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted to the line at the rate determined by TCLK. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high or LLOOP may be commanded via the serial interface.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the

jitter attenuator to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 5). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). A remote loopback bypasses the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 5. Interaction of RLOOP with TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV at least once within 64±2 cycles. In the Host Mode, DPM is available from both the register and pin 11. The driver performance monitor is not designed to detect broken printed ciruit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING.

DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61574 cannot be used to monitor the TTIP/TRING pins of a CS61574A, CS61535A, CS6158A or CS61575.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface

when in operation. However, a reset function is available which will clear all registers.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration.

Serial Interface

In the Host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 12 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle.When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

An address/command byte, shown in Table 6, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6. Address/Command Byte

The data register, shown in Table 7, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

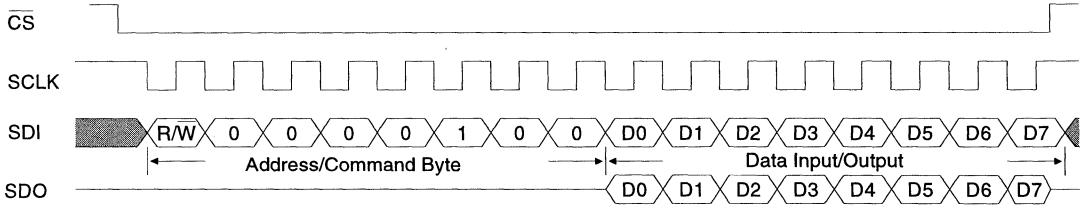


Figure 12. Input/Output Timing

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61574 into a factory test mode.

Table 7. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be suppressed (i.e., prevented from occurring).

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Input bits 5/6/7=111 and 5/6/7=101 are the same request, and cause the line interface to enter into the factory test mode. In other words, when RLOOP=1 (Bit 5) and TAOS=1 (Bit 7), LOOP (Bit 6) is a don't care. For normal operation, RLOOP and TAOS should not be simultaneously selected via the serial interface.

Output data from the serial interface is presented as shown in Tables 8 and 9. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermitent losses of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 8. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 9. Coding for Serial Output bits 5,6,7

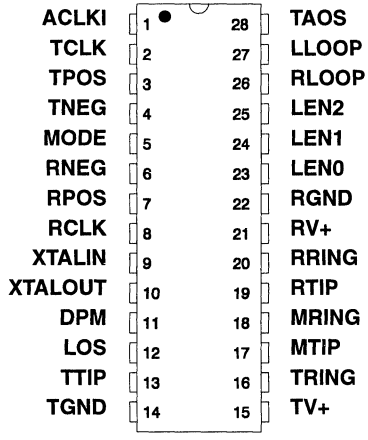
Power Supply

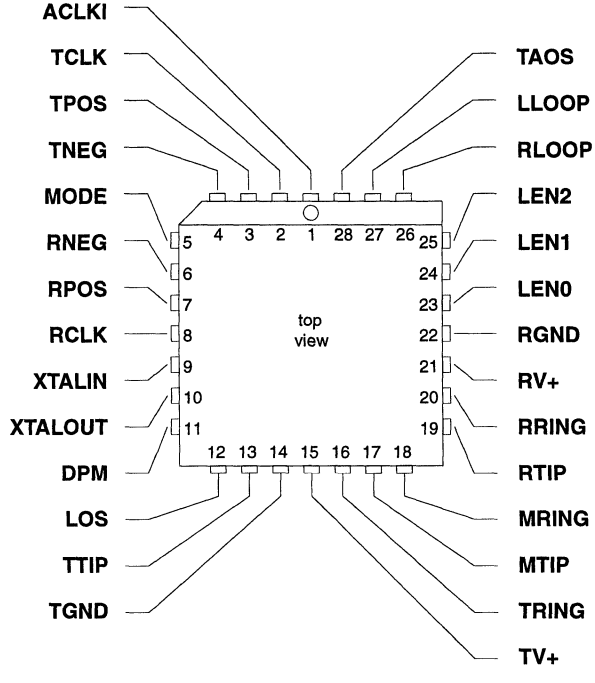
The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

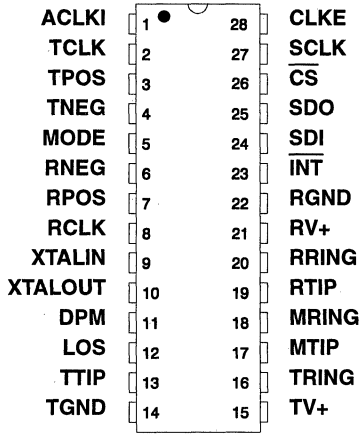
PIN DESCRIPTIONS

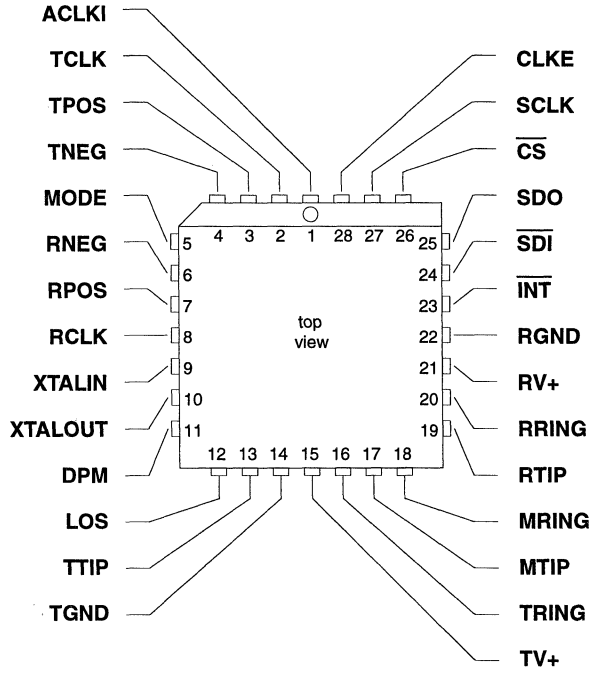
Hardware Mode





Host Mode


ACLKI 1
TCLK 2
TPOS 3
TNEG 4
MODE 5
RNEG 6
RPOS 7
RCLK 8
XTALIN 9
XTALOUT 10
DPM 11
LOS 12
TTIP 13
TGND 14
28 CLKE
27 SCLK
26 CS
25 SDO
24 SDI
23 INT
22 RGND
21 RV+
20 RRING
19 RTIP
18 MRING
17 MTIP
16 TRING
15 TV+


ACLKI
TCLK
TPOS
TNEG
MODE
RNEG
RPOS
RCLK
XTALIN
XTALOUT
DPM
LOS
TTIP
TGND
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6
7
8
9
10
11
12 13 14 15 16 17 18
25
24
23
22
21
20
19
top
view
CLKE
SCLK
CS
SDO
SDI
INT
RGND
RV+
RRING
RTIP
MRING
MTIP
TRING
TV+

Power Supplies

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Note: Overdriving the oscillator with an external clock is not supported.

Control

MODE - Mode Select, Pin 5.
Driving the MODE pin high puts the line interface in the Host Mode. In the Host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins.

TAOS - Transmit All Ones Select, Pin 28 (Hardware Mode).
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

LLOOP - Local Loopback, Pin 27 (Hardware Mode).
Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26. (Hardware Mode)
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored in the hardware mode. In the Host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode. Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware Mode)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection. Also controls the receiver slicing level.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

CLKE - Clock Edge, Pin 28. (Host Mode)

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)

Pin must transition from high to low to read or write the serial port.

ACLKI - Alternate External Clock Input, Pin 1.

A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground.

Data

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG.

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin. When in the loss of signal state RPOS/RNEG are forced low. If ACLKI is grounded, RCLK is forced to the center frequency of the crystal oscillator during loss of signal.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7 (Hardware and Host Modes).

The receiver recovered digital data is output on these pins. In the Hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. The transmitter output is designed to drive a 25 Ω load between TTIP and TRING.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG are sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4 (Hardware and Host Modes).

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

Status

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low after the next pulse is received. When in the loss of signal state RPOS/RNEG are forced low. If ACLKI is grounded, RCLK is forced to the center frequency of the crystal oscillator during loss of signal.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.

DPM - Driver Performance Monitor, Pin 11.

DPM goes high if no activity is detected on MTIP and MRING for 64±2 bit periods. DPM returns low when the first transition is detected on MTIP and MRING.

Ordering Guide

Model	Frequency	Package
CS61574-IP	T1 only	28-pin Plastic DIP
CS61574-IP1	T1 & E1	28-pin Plastic DIP
CS61574-IL	T1 only	28-pin PLCC
CS61574-IL1	T1 & E1	28-pin PLCC

APPLICATIONS

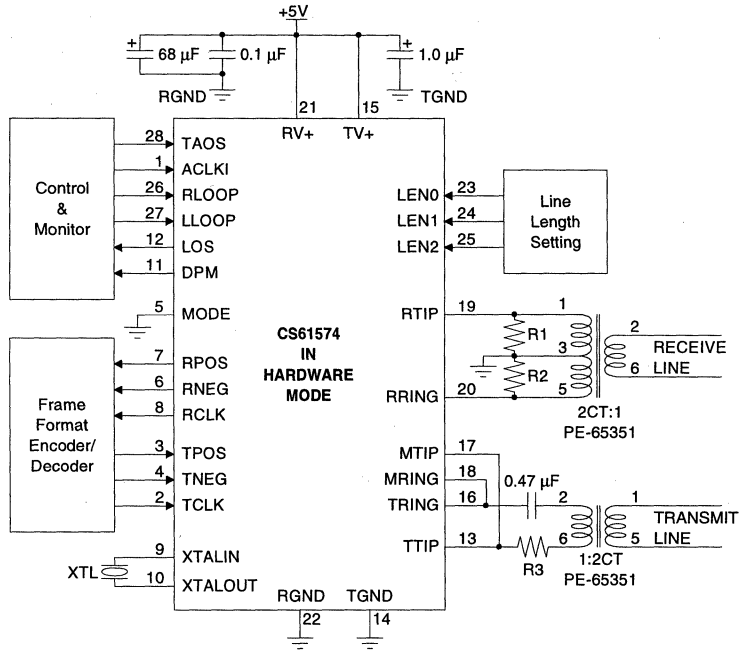


Figure A1. E1 Hardware Mode Configuration

Frequency MHz	Crystal XTL	Cable Ω	LEN2/1/0	R3 Ω	R1 and R2 Ω
1.544 (T1)	CXT6176	100	0/1/1 - 1/1/1	not used	200
2.048 (E1)	CXT8192	120	0/0/0	not used	240
		75	0/0/0	4.4	150

Table A1. External Component Values

Line Interface

Figures A1-A2 show typical T1 and E1 line interface application circuits. Table A1 shows the external components which are specific to each application. Figure A1 illustrates an E1 interface in the Host Mode. Figure A2 illustrates a T1 interface in the Hardware Mode.

The 1:2 receiver transformer has a grounded center tap on the IC side. Resistors R1 and R2 between the RTIP and RRING pins to ground provide the termination for the receive line. The transmitter also uses a 1:2 transformer. A 0.47 µF capacitor is required in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

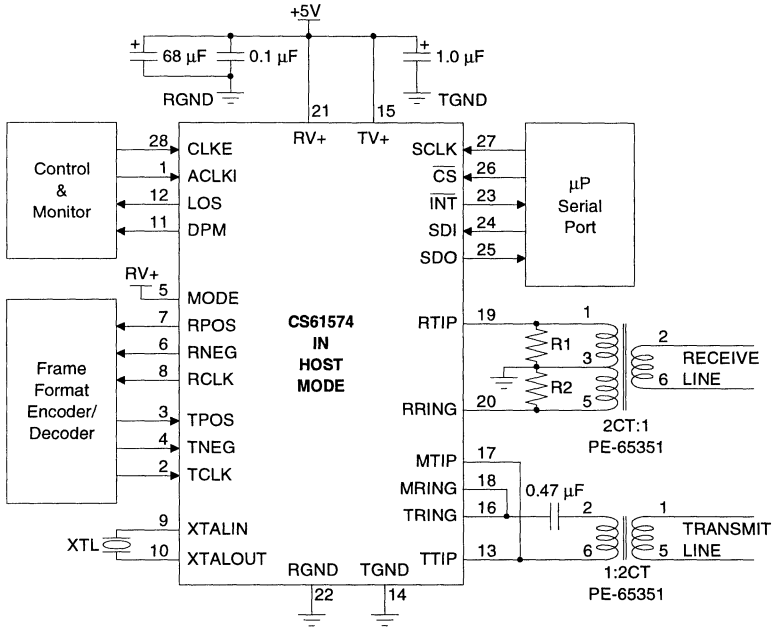


Figure A2. T1 Host Mode Configuration

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61574. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Turns Ratio	1:2 CT ± 5%
Primary Inductance	600 µH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kVsurface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61574 in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the application note "Secondary Line Protection for T1 and E1 Line Cards" for detailed information on the different electrical safety standards and specific application circuit recommendations.

Interfacing The CS61574 With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A3. In this case, the line interface and CS2180B are in host mode controlled by a microprocessor serial interface. If the line interface is used in Hardware Mode, then the line interface RCLK output must be inverted before being input to the CS2180B.

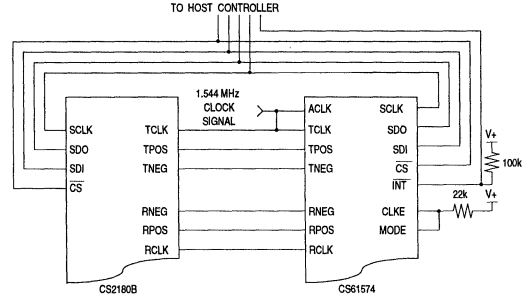


Figure A3. Interfacing the CS61574 with a CS2180B (Host Mode)

Semiconductor Corporation

CS61574A
CS61575

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Fully Compliant with AT&T 62411 Stratum 4 Jitter Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoder/Decoder
- 14 dB of Transmitter Return Loss

General Description

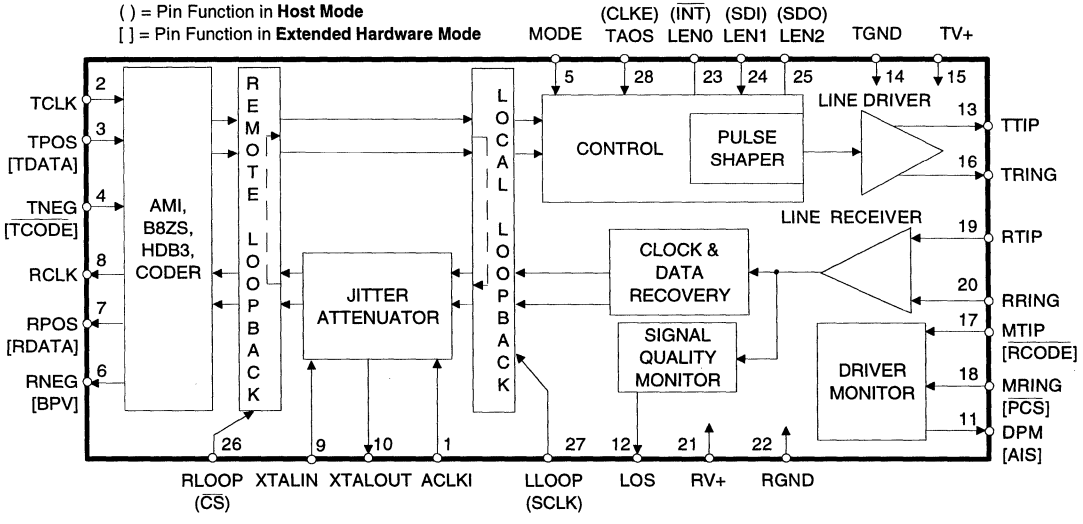
The CS61574A and CS61575 combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. Both devices support processor-based or stand-alone operation and interface with industry standard T1 and E1 framers.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The CS61574A has a receiver jitter attenuator optimized for minimum delay in switching and transmission applications, while the CS61575 attenuator is optimized for CPE applications subject to AT&T 62411 requirements. The transmitter features internal pulse shaping and a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION - See page 3-246.



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to RGND, TGND=0V)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Consumption (Notes 4,5)	P_C	-	290	350	mW
Power Consumption (Notes 4,6)	P_C	-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 7, 8) PINS 1-4, 17, 18, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 7, 8) PINS 1-4, 17, 18, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 7, 8, 9) I_{OUT} = -40 µA PINS 6-8, 11, 12, 25	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (Notes 7, 8, 9) I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	µA
Low-Level Input Voltage, PIN 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5	V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5 (Note 10)	V_{IM}	2.3	-	2.7	V

Notes:
7. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate output.
8. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
9. Output drivers will drive CMOS logic levels into a CMOS load.
10. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 11)				
E1, 75 Ω	(Note 12)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 13)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 14)	2.7	3.0	3.3	V
T1, DSX-1	(Note 15)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
1:1 transformer and 75Ω load		-0.237	-	0.237	V
1:1.26 transformer and 120Ω load		-0.3	-	0.3	V
Recommended Output Load at TTIP and TRING		-	75	-	Ω
Jitter Added During Remote Loopback	(Note 16)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 11, 17)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 11, 17)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 11, 17)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss	(Notes 11, 17, 18)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
Transmitter Short Circuit Current	(Notes 11, 19)	-	-	50	mA RMS
Driver Performance Monitor					
MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.6	-	V

Notes: 11. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications section.

12. Pulse amplitude measured at the output of a 1:1 or 1:1.26 transformer across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
13. Pulse amplitude measured at the output of a 1:1.26 transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
14. Pulse amplitude measured at the output of a 1:1.15 transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
15. Pulse amplitude measured at the DSX-1 cross-connect across a 100 Ω load for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0, or 1/1/1 using a 1:1.15 transformer and the length of #22 AWG, ABAM, or equivalent cable specified in Table 3.
16. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
17. Not production tested. Parameters guaranteed by design and characterization.
18. Return loss = 20 $\log_{10}$ ABS((z_1 +z_0)/(z_1-z_0)) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
19. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6	-	-	dB
		500	-	-	mV
Data Decision Threshold					
T1, DSX-1	(Note 20)	60	65	70	% of peak
T1, DSX-1	(Note 21)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 22)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 23)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold	(Note 24)	0.25	0.30	0.50	V

Notes: 20. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
21. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
22. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
23. Jitter tolerance increases at lower frequencies. See Figure 11.
24. The analog input squelch circuit shall operate when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V. Operation of the squelch results in the recovery of zeros. During receive LOS, the RPOS, RNEG or RDATA outputs are forced low.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 17, 25)				
CS61574A		-	6	-	Hz
CS61575		-	3	-	Hz
CS61574A T1 Receiver Jitter Transfer	(Notes 25, 26)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	10	3.0	6.0	-	dB
100	10	20	30	-	dB
500	10	35	40	-	dB
1k	5	40	50	-	dB
10k, 40k	0.3	40	50	-	dB
CS61575 T1 Receiver Jitter Transfer	(Notes 25, 26)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	10	6.0	9.0	-	dB
100	10	23	33	-	dB
500	10	38	43	-	dB
1k	5	40	50	-	dB
10k, 40k	0.3	40	50	-	dB
CS61574A E1 Receiver Jitter Transfer	(Notes 26, 27, 28)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	1.5	3.0	6.0	-	dB
20	1.5	6.0	12	-	dB
100	1.5	20	32	-	dB
400	1.5	30	40	-	dB
1k	1.5	35	45	-	dB
10k, 100k	0.2	35	45	-	dB
CS61575 E1 Receiver Jitter Transfer	(Notes 26, 27, 28)				
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	1.5	6.0	12	-	dB
20	1.5	12	18	-	dB
100	1.5	22	29	-	dB
400	1.5	30	39	-	dB
1k	1.5	35	45	-	dB
10k, 100k	0.2	35	45	-	dB
Attenuator Input Jitter Tolerance	(Notes 17, 28)				
(Before Onset of FIFO Overflow or Underflow Protection)					
CS61574A		12	23	-	UI
CS61575		138	-	-	UI

Notes: 25. Attenuation measured at the demodulator output of an HP3785B with input jitter equal to 3/4 of measured jitter tolerance using a measurement bandwidth of 1 Hz (10<f<100Hz), 4Hz (100<f<1000 Hz) and 10 Hz (f> 1kHz) centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern.

26. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.

27. Jitter measured at the demodulator output of an HP3785A (or equivalent) using a measurement bandwidth not to exceed 20 Hz centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern.

28. Jitter below 100 kHz and within the attenuator's input jitter tolerance is not translated or aliased to other frequencies. Output jitter increases significantly when attenuator input jitter tolerance is exceeded.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 26)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Note 29)	t_{pwh2}	150	-	500	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 31)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 32)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 32)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 33)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 34)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 35)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 33)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 34)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 35)	t_{h1}	150	274	-	ns

Notes: 29. The transmitted pulse width does not depend on the TCLK duty cycle.
30. ACLKI provided by an external source or TCLK.
31. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
32. At max load of 1.6 mA and 50 pF.
33. Host Mode (CLKE = 1).
34. Extended Hardware Mode.
35. Hardware Mode, or Host Mode (CLKE = 0).

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 26)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Note 29)	t_{pwh2}	150	-	340	ns
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 31)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 32)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 32)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 33)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 34)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 35)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 33)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 34)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 35)	t_{h1}	100	194	-	ns

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 36)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

Notes: 36. Output load capacitance = 50pF.

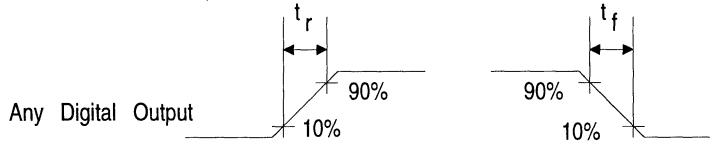


Figure 1. Signal Rise and Fall Characteristics

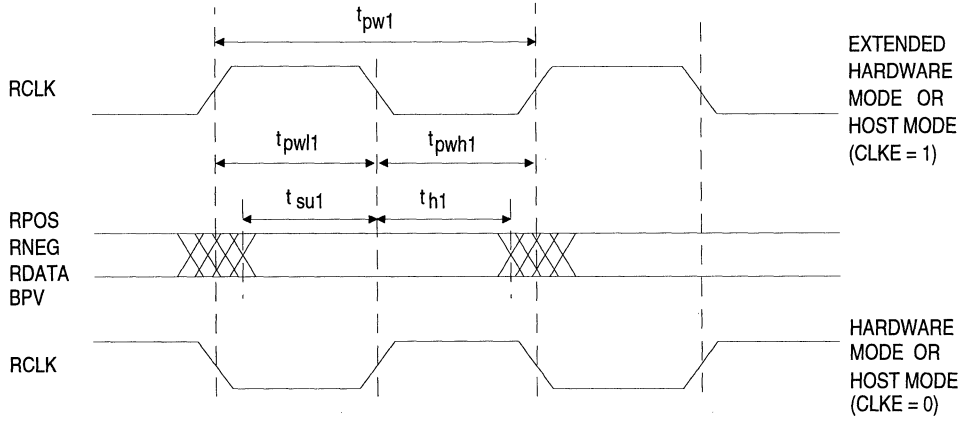


Figure 2. Recovered Clock and Data Switching Characteristics

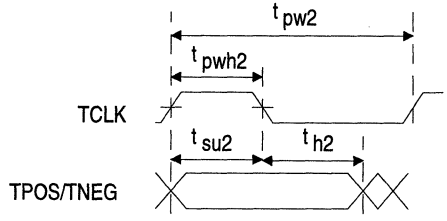


Figure 3a. Transmit Clock and Data Switching Characteristics

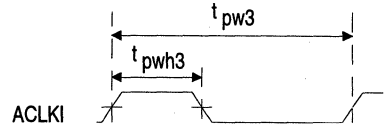


Figure 3b. Alternate External Clock Characteristics

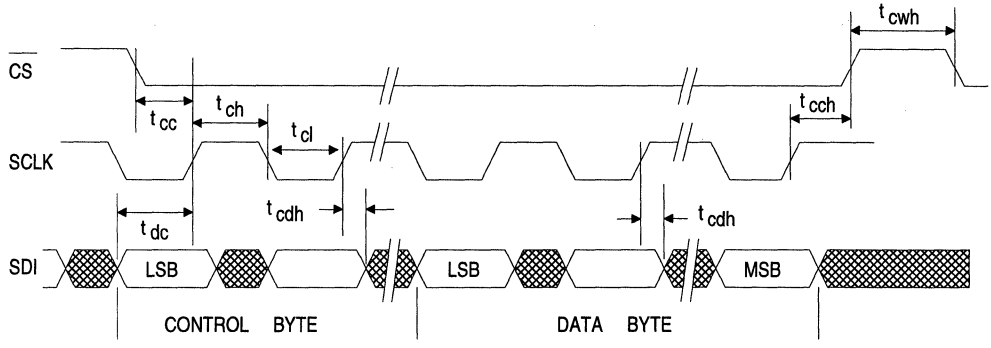


Figure 4. Serial Port Write Timing Diagram

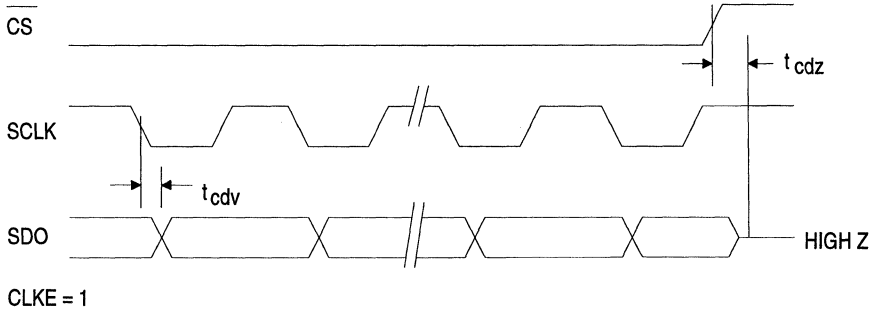


Figure 5. Serial Port Read Timing Diagram

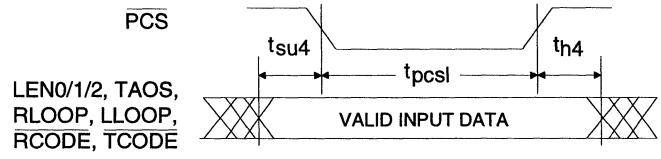


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Enhancements in CS61575 and CS61574A

The CS61574A and CS61575 provide higher performance and more features than the CS61574 including:

- AT&T 62411, Stratum 4 compliant jitter attenuation over the full range of operating frequency and jitter amplitude (CS61575),
- 50% lower power consumption,
- Internally matched transmitter output impedance for improved signal quality,
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- ANSI T1.231-1993 compliant receiver LOS (Loss of Signal) handling,
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,
- The Driver Performance Monitor operates over a wider range of input signal levels.

Existing designs using the CS61574 can be converted to the higher performance, pin-compatible CS61574A or CS61575 if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio.

Understanding the Difference Between the CS61575 and CS61574A

The CS61574A and CS61575 provide receiver jitter attenuation performance optimized for different applications. The CS61575 is optimized to attenuate large amplitude, low frequency jitter for T1 Customer Premises Equipment (CPE) applications as required by AT&T 62411. The CS61574A is optimized to minimize data delay in T1 and E1 switching or transmission applications. Refer to the "Jitter Attenuator" section for additional information.

Introduction to Operating Modes

The CS61574A and CS61575 support three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2).

	Hardware Mode	Extended Hardware Mode	Host Mode
Control Method	Control Pins	Control Pins with Parallel Chip Select	Serial Interface
MODE Pin Level	<0.2 V	Floating or 2.5 V	>(RV+)-0.2 V
Line Coding	External	Internal-AMI, B8ZS, or HDB3	External
AIS Detection	No	Yes	No
Driver Performance Monitor	Yes	No	Yes

Table 1. Differences Between Operating Modes

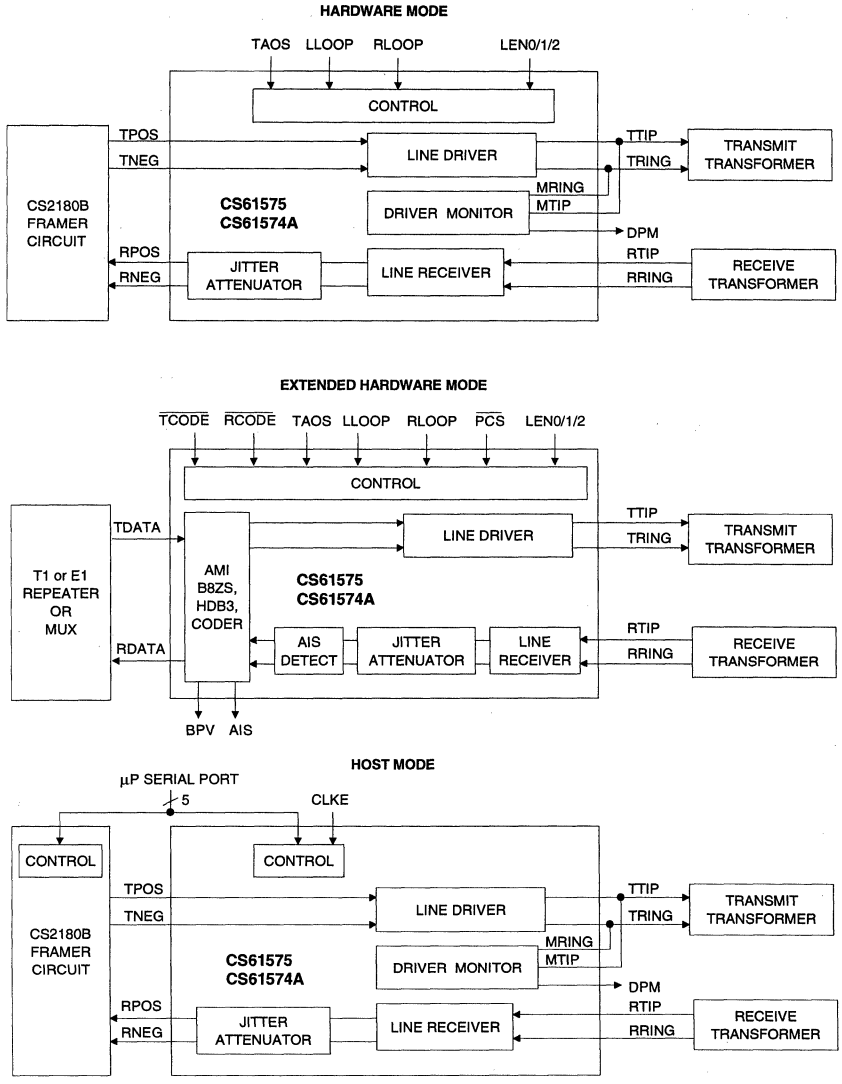


Figure 7. Overview of Operating Modes

FUNCTION	PIN	MODE HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

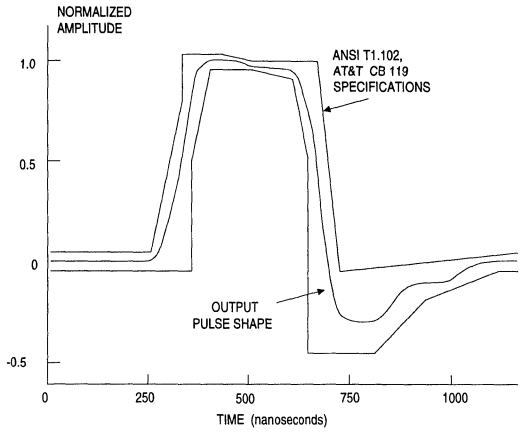


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

Transmitter

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	0	120Ω (1:1.26) 75Ω (1:1)	E1 CCITT G.703
0	0	1	AT&T CB113	Repeater
0	1	0	FCC PART 68, OPT. A	Network Interface
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

The CS61575 and CS61574A line drivers are designed to drive a 75 Ω equivalent load.

For E1 applications, the CS61574A and CS61575 drivers provide 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61575 and CS61574A automatically adjusts the pulse width based upon the "line length" selection made.

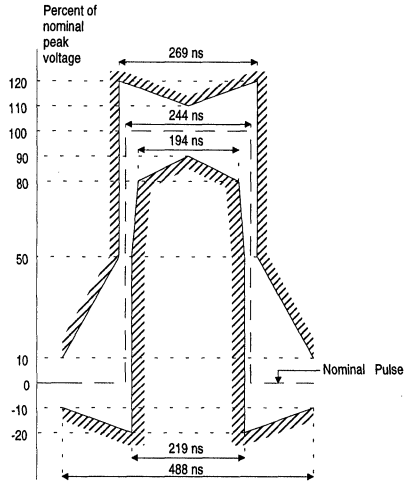


Figure 9. Mask of the Pulse at the 2048 kbps Interface

The E1 G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

The CS61574A and CS61575 will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, AT&T 62411, TR-TSY-000170, and CCITT REC. G.823.

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

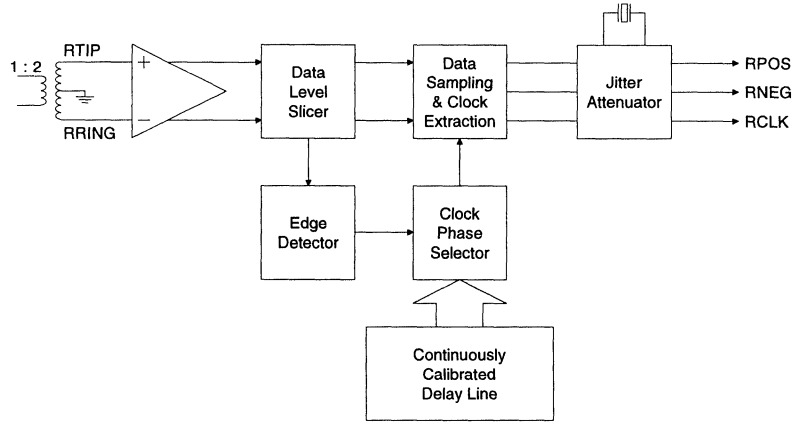


Figure 10. Receiver Block Diagram

A block diagram of the receiver is shown in Figure 10. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 11. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated using the crystal oscillator reference clock. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

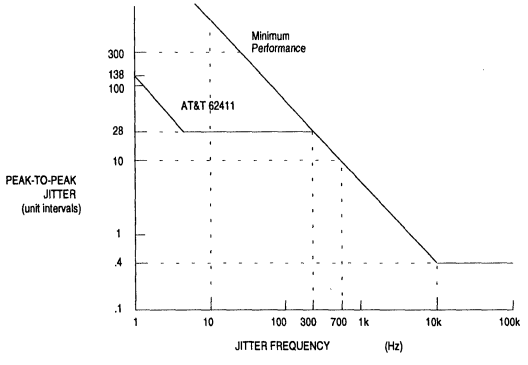


Figure 11. Minimum Input Jitter Tolerance of Receiver

In the Hardware Mode, data at RPOS and RNEG should be sampled on the rising edge of RCLK, the recovered clock. In the Extended Hardware Mode, data at RDATA should be sampled on the falling edge of RCLK. In the Host Mode, CLKE determines the clock polarity for which output data should be sampled as shown in Table 5.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5V)	X	RDATA	RCLK	Falling

X = Don't care

Table 5. Data Output/Clock Relationship

Loss of Signal

The receiver will indicate loss of signal after power-up, reset or upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. A zero is received when the RTIP and RRING inputs are below the input comparator slicing threshold level established by the peak detector. After the signal is removed for a period of time the data slicing threshold level decays to approximately 300 mV_{peak}.

If ACLKI is present during the LOS state, ACLKI is switched into the input of the jitter attenuator, resulting in RCLK matching the frequency of ACLKI. The jitter attenuator buffers any instantaneous changes in phase between the last recovered clock and the ACLKI reference clock. This means that RCLK will smoothly transition to the new frequency. If ACLKI is not present, then the crystal oscillator of the jitter attenuator is forced to its center frequency. Table 6 shows the status of RCLK upon LOS.

Crystal present?	ACLKI present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	ACLKI via the Jitter Attenuator

Table 6. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32 or 192-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 12. The CS61575 fully meets AT&T 62411 jitter attenuation requirements. The CS61574A will have a discontinuity in the jitter transfer function when the incoming jitter amplitude exceeds approximately 23 UIs.

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG (or RDATA). RCLK is equivalent to the oscillator's output. By changing the load capacitance that the IC presents to the crystal, the oscillatior frequency (and RCLK) is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Jitter is absorbed in the FIFO according to the jitter transfer characteristic shown in Figure 12.

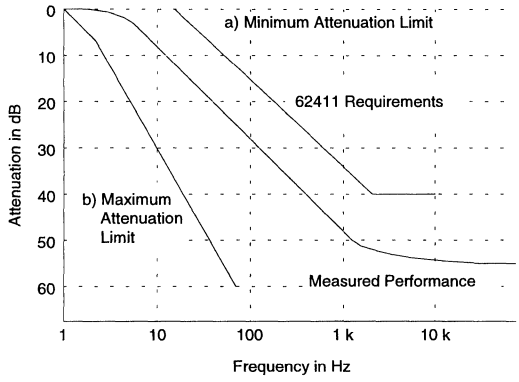


Figure 12. Typical Jitter Transfer Function

The FIFO in the jitter attenuator is designed to prevent overflow and underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

The difference between the CS61575 and CS61574A is the depth of the FIFO in the jitter attenuator. The CS61575 has a 192-bit FIFO which allows it to attenuate large amplitude, low frequency jitter as required by AT&T 62411 (e.g., 28 UIpp @ 300 Hz). This makes the CS61575 ideal for use in T1 Customer Premises Equipment which must be compatible with AT&T 62411 requirements. In single-line Stratum 4, Type II systems which are loop-timed, he CS61575 recovered clock can be used as the transmit clock eliminating the need for an external system clock synchronizer. In Stratum 4, Type I systems which transfer timing and require a clock synchronizer, the CS61575 simplifies the design of the synchronizer by absorbing large amplitude low frequency jitter before it reaches the synchronizer.

The CS61574A has a 32-bit FIFO which allows it to absorb jitter with minimum data delay in T1 and E1 switching or transmission applications. The CS61574A will tolerate large amplitude jitter by tracking rather than attenuating it, preventing data errors so that the jitter may be absorbed in external frame buffers. With large amplitude input jitter, the CS61574A jitter transfer function may exhibit some jitter peaking, but will offer performance comparable to the CS61574.

The jitter attenuator may be bypassed by pulling XTALIN to RV+ through a 1 kΩ resistor and providing a 1.544 MHz (or 2.048 MHz) clock on ACLKI. RCLK may exhibit quantization jitter of approximately 1/13 UIpp and a duty cycle of approximately 30% (70%) when the attenuator is disabled.

Local Loopback

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG (or RDATA). If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

Remote Loopback

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 7). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). Simultaneous selection of local and remote loopback modes is not valid (see Reset).

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{\text{RCODE}}$ is low.

Driver Performance Monitor

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from both the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61574A or CS61575 can not be used to monitor a CS61574 due to output stage differences.

Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when less than 9 zeros are detected out of 8192 bit periods. AIS returns low when 9 or more zeros are detected out of 8192 bit periods.

Parallel Chip Select

In the Extended Hardware Mode, $\overline{PCS}$ can be used to gate the digital control inputs: $\overline{TCODE}$, $\overline{RCODE}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{PCS}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{PCS}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{PCS}$ low period. The digital control inputs are ignored when $\overline{PCS}$ is high.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

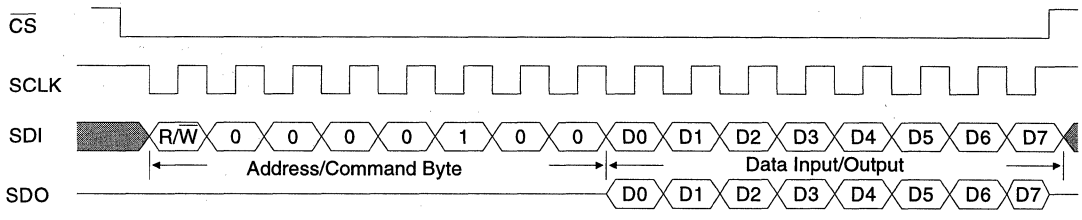


Figure 13. Input/Output Timing

An address/command byte, shown in Table 9, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 9. Address/Command Byte

The data register, shown in Table 10, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

Table 10. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 11 and 12. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermittent loss of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 11. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Coding for Serial Output bits 5,6,7

3

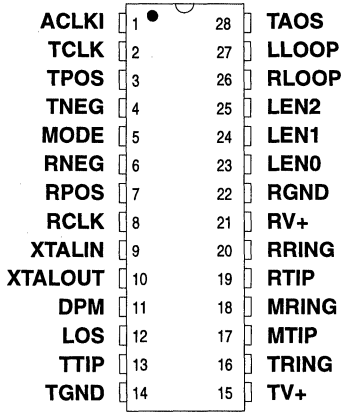
Power Supply

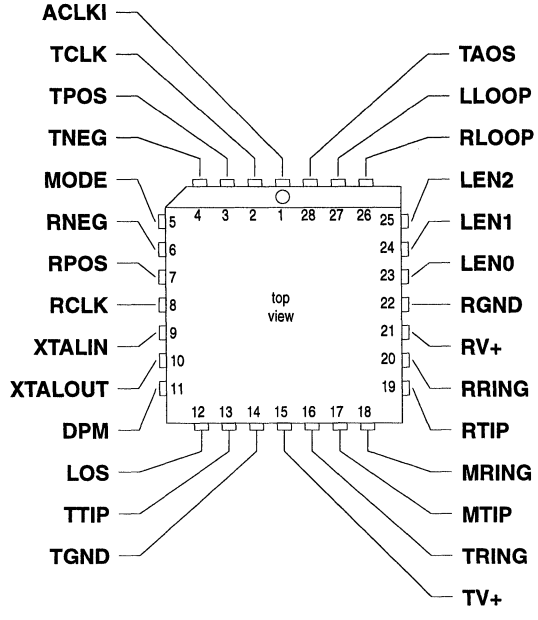
The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

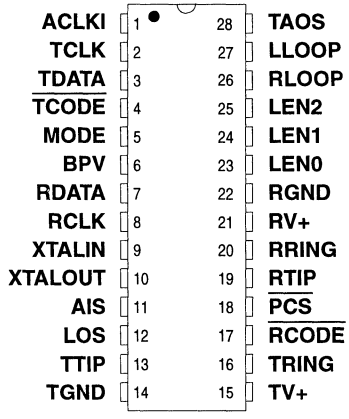
PIN DESCRIPTIONS

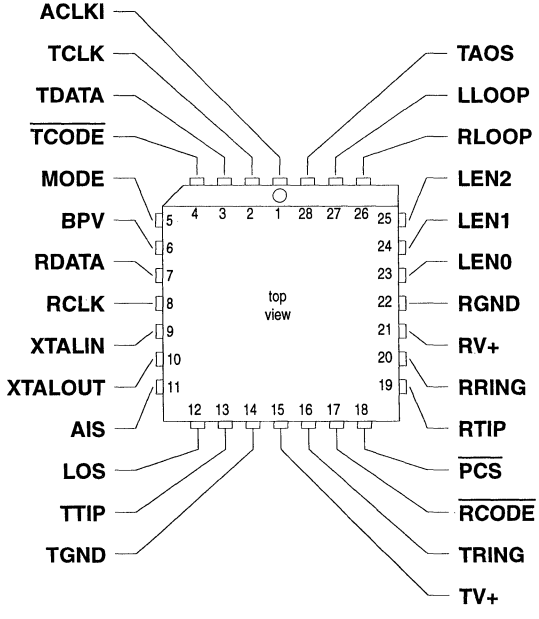
Hardware Mode



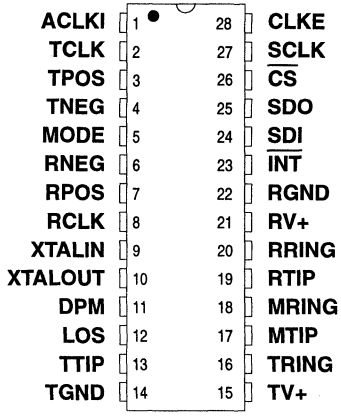


Extended Hardware Mode





Host Mode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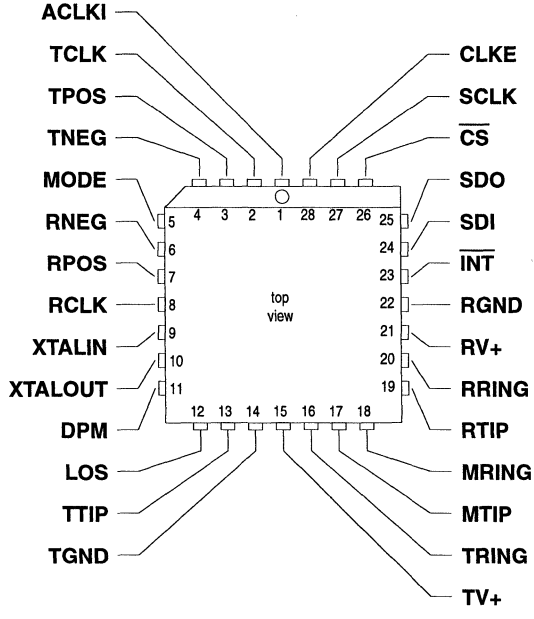
TCLK 2
TPOS 3
TNEG 4
MODE 5
RNEG 6
RPOS 7
RCLK 8
XTALIN 9
XTALOUT 10
DPM 11
LOS 12
TTIP 13
TGND 14
28 CLKE
27 SCLK
26 CS
25 SDO
24 SDI
23 INT
22 RGND
21 RV+
20 RRING
19 RTIP
18 MRING
17 MTIP
16 TRING
15 TV+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TNEG
MODE
RNEG
RPOS
RCLK
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DPM
LOS
TTIP
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6
7
8
9
10
11
12 13 14 15 16 17 18
24
23
22
21
20
19
top
view
CLKE
SCLK
CS
SDO
SDI
INT
RGND
RV+
RRING
RTIP
MRING
MTIP
TRING
TV+

Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Overdriving the oscillator with an external clock is not supported.

Control

ACLKI - Alternate External Clock Input, Pin 1.
A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground. During LOS, the ACLKI input signal, if present, is output on RCLK through the jitter attenuator.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

$\overline{CS}$ - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

$\overline{INT}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)
Goes low when LOS or DPM change state to flag the host processor. $\overline{INT}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{INT}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the line interface in the Host Mode. In the host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 Vselects the Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ high causes the line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin.When in the loss of signal state ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator..

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. The transmitter output is designed to drive a 75 Ω load between TTIP and TRING. A transformer is required as shown in Table A1.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than 9 zeros out of 8192 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)

BPV goes high for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low when the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consectutive zeros) as prescribed in ANSI T1.231-1993. When in the loss of signal state RPOS/RNEG or RDATA are forced low, and ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.

Ordering Guide

Model	Frequency	FIFO Depth (Bits)	Package
CS61575-IP1	T1 & E1	192	28-pin Plastic DIP
CS61575-IL1	T1 & E1	192	28-pin PLCC
CS61574A-IP1	T1 & E1	32	28-pin Plastic DIP
CS61574A-IL1	T1 & E1	32	28-pin PLCC

APPLICATIONS

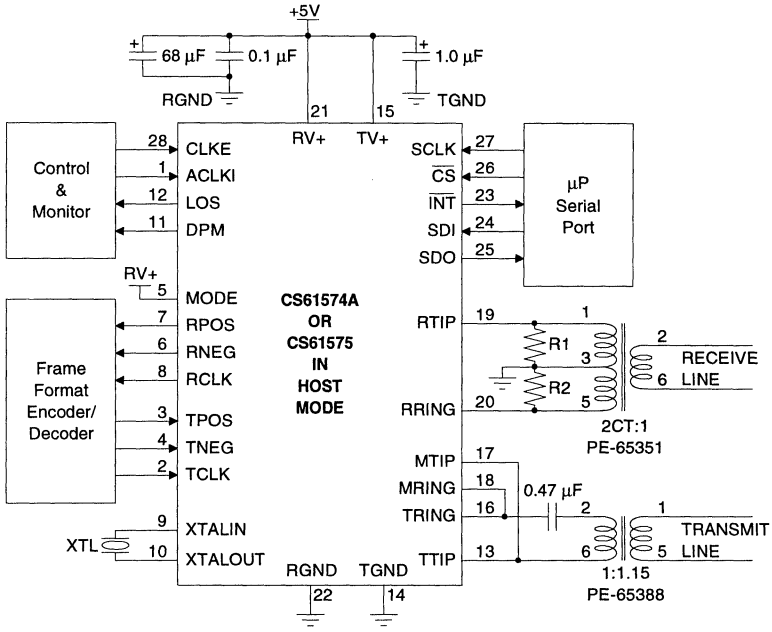


Figure A1. T1 Host Mode Configuration

Frequency MHz	Cable Ω	R1 and R2 Ω	Transmit Transformer	Crystal XTL
1.544 (T1)	100	200	1:1.15	CXT6176
2.048 (E1)	120	240	1:1.26	CXT8192
	75	150	1:1	

Table A1. External Component Values

Line Interface

Figures A1-A3 show typical T1 and E1 line interface application circuits. Table A1 shows the external components which are specific to each application. Figure A1 illustrates a T1 interface in the Host Mode. Figure A2 illustrates a 120 Ω E1 interface in the Hardware Mode. Figure A3 illustrates a 75 Ω E1 interface in the Extended Hardware Mode

The receiver transformer has a grounded center tap on the IC side. Resistors between the RTIP and RRING pins to ground provide the termination for the receive line.

The transmitter transformer matches the 75 Ω transmitter output impedance to the line impedance. Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

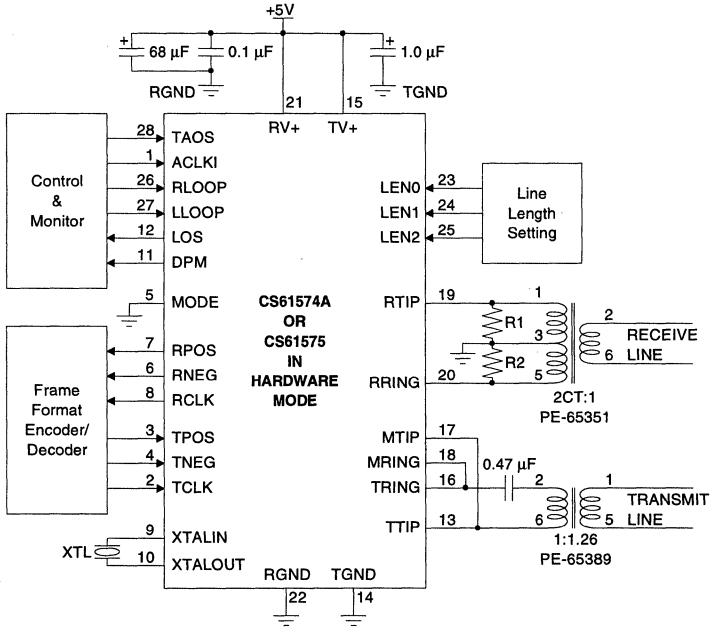


Figure A2. 120 Ω, E1 Hardware Mode Configuration

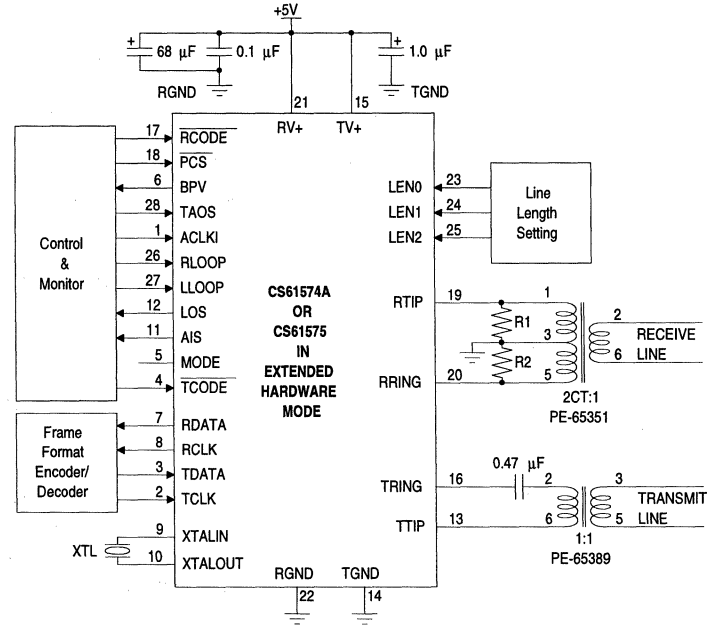


Figure A3. 75 Ω, E1 Extended Hardware Mode Configuration

Parameter	Receiver	Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 120 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 75 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61574A and CS61575. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications where it is advantageous to use a single transmitter transformer for 75Ω and 120Ω E1 applications, a 1:1.26 transformer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct across a 75Ω load.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Designing for AT&T 62411

For additional information on the requirements of AT&T 62411 and the design of an appropriate system synchronizer, please refer to the Crystal Semiconductor Application Notes: "AT&T 62411 Design Considerations – Jitter and Synchronization" and "Jitter Testing Procedures for Compliance with AT&T 62411".

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61575 in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the application note "Secondary Line Protection for T1 and E1 Line Cards" for detailed information on the different electrical safety standards and specific application circuit recommendations.

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

Interfacing The CS61575 and CS61574A With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A4. In this case, the line interface and CS2180B are in Host Mode controlled by a microprocessor serial interface. If the line interface is used in Hardware Mode, then the line interface RCLK output must be inverted before being input to the CS2180B. If the CS61575 or CS61574A is used in Extended Hardware Mode, the RCLK output does not have to be inverted before being input to the CS2180B.

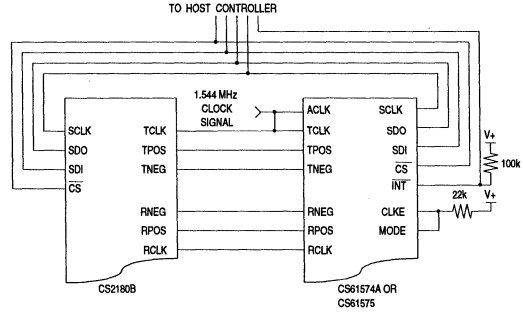


Figure A4. Interfacing the CS61574A or CS61575

Semiconductor Corporation

CS61577

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Drop-in Replacement for CS61574 with the Following Enhancements:
  - Lower Power Consumption
  - Transmitter Short-Circuit Current Limiting
  - Greater Transmitter Immunity to Line Reflections
  - Software Selection Between 75Ω and 120Ω E1 Output Options
  - Internally Controlled E1 Pulse Width
  - B8ZS/HDB3/AMI Encoder/Decoder

General Description

The CS61577 is a drop-in replacement for the CS61574, and combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61577 supports processor-based or stand-alone operation and interfaces with industry standard T1 and E1 framers.

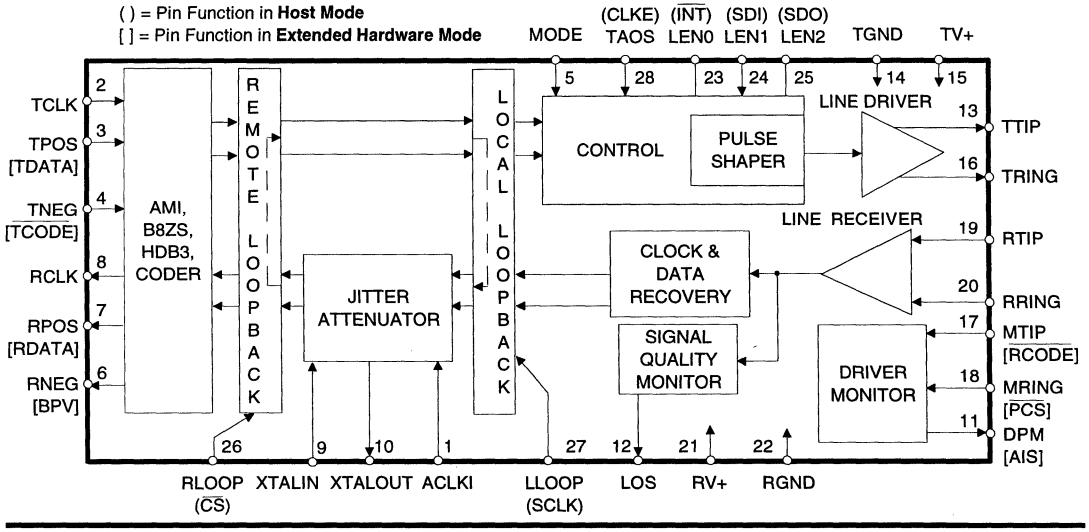
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The receiver includes a jitter attenuator optimized for minimum delay in switching and transmission applications. The transmitter provides internal pulse shaping to insure compliance with T1 and E1 pulse template specifications.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Building Channel Service Units

ORDERING INFORMATION

CS61577-IP1	28 Pin Plastic DIP
CS61577-IL1	28 Pin Plastic PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to RGND=TGND=0V)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4,5)	P_C	-	400	500	mW
Power Consumption	(Notes 4,6)	P_C	-	230	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-4, 17, 18, 23-28	(Notes 7, 8)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-4, 17, 18, 23-28	(Notes 7, 8)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA PINS 6-8, 11, 12, 25	(Notes 7, 8, 9)	V_{OH}	4.0	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	(Notes 7, 8, 9)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)			-	-	±10	µA
Low-Level Input Voltage, PIN 5		V_{IL}	-	-	0.2	V
High-Level Input Voltage, PIN 5		V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, PIN 5	(Note 10)	V_{IM}	2.3	-	2.7	V

Notes: 7. In Extended Hardware Mode, pins 17 and 18 are digital inputs. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate output.
8. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
9. Output drivers will drive CMOS logic levels into a CMOS load.
10. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 11)				
E1, 75 Ω	(Note 12)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 13)	2.7	3.0	3.3	V
T1, (FCC Part 68)	(Note 14)	2.7	3.0	3.3	V
T1, DSX-1	(Note 15)	2.4	3.0	3.6	V
Load Presented To Transmitter Output	(Note 11)	-	25	-	Ω
Jitter Added During Remote Loopback	(Note 16)				
10Hz - 8kHz		-	0.005	-	UI
8kHz - 40kHz		-	0.008	-	UI
10Hz - 40kHz		-	0.010	-	UI
Broad Band		-	0.015	-	UI
Power in 2kHz band about 772kHz	(Notes 11, 17)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 11, 17)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 11, 17)	-	0.2	0.5	dB
Transmitter Output Impedance	(Notes 17, 18)	-	-	10	Ω
Transmitter Short Circuit Current	(Notes 11, 19)	-	-	50	mA RMS

Notes: 11. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.

12. Pulse amplitude measured at the output of the transformer across a 75 Ω load for line length settings LEN2/1/0 = 0/0/1 and 0/0/0. For LEN2/1/0 = 0/0/0 only, a 4.4 Ω resistor is required in series with the transformer primary.
13. Pulse amplitude measured at the output of the transformer across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
14. Pulse amplitude measured at the output of the transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
15. Pulse amplitude measured at the DSX-1 Cross-Connect for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1.
16. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
17. Not production tested. Parameters guaranteed by design and characterization.
18. Measured between the TTIP and TRING pins at 772 kHz during marks and spaces.
19. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern with LEN2/1/0 = 0/0/0 or 0/0/1.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6 500	- -	- -	dB mV
Loss of Signal Threshold		-	0.30	-	V
Data Decision Threshold					
T1, DSX-1	(Note 20)	60	65	70	% of peak
T1, DSX-1	(Note 21)	53	65	77	% of peak
T1, (FCC Part 68) and E1	(Note 22)	45	50	55	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 23)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 17, 24)	-	6	-	Hz
Attenuation at 10kHz Jitter Frequency	(Notes 17, 24)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 17, 24)	12	23	-	UI

Notes: 20. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
21. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
22. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
23. Jitter tolerance increases at lower frequencies. See Figure 11.
24. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 12. Output jitter can increase significantly when more than 12 UI's are input to the attenuator. See discussion in the text section.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 25)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 26)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 27)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 28)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 28)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 29)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 30)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 31)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 29)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 30)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 31)	t_{h1}	150	274	-	ns

Notes: 25. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
26. ACLKI provided by an external source or TCLK.
27. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
28. At max load of 1.6 mA and 50 pF.
29. Host Mode (CLKE = 1).
30. Extended Hardware Mode.
31. Hardware Mode, or Host Mode (CLKE = 0)
32. The transmitted pulse width for LEN2/1/0 = 0/0/0 and 0/0/1 does not depend on the TCLK duty cycle.

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;

GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 25)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 32)	t_{pwh2}/t_{pw2}	40	50	60	%
ACLKI Frequency	(Note 26)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 27)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time, All Digital Outputs	(Note 28)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 28)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 29)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 30)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 31)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 29)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 30)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 31)	t_{h1}	100	194	-	ns

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;

Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 33)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns
Input Valid To $\overline{PCS}$ Falling Setup Time	t_{su4}	50	-	-	ns
$\overline{PCS}$ Rising to Input Invalid Hold Time	t_{h4}	50	-	-	ns
$\overline{PCS}$ Active Low Time	t_{pcsl}	250	-	-	ns

Notes: 33. Output load capacitance = 50pF

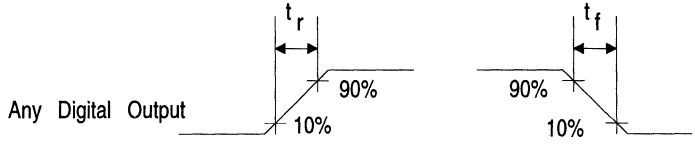


Figure 1. Signal Rise and Fall Characteristics

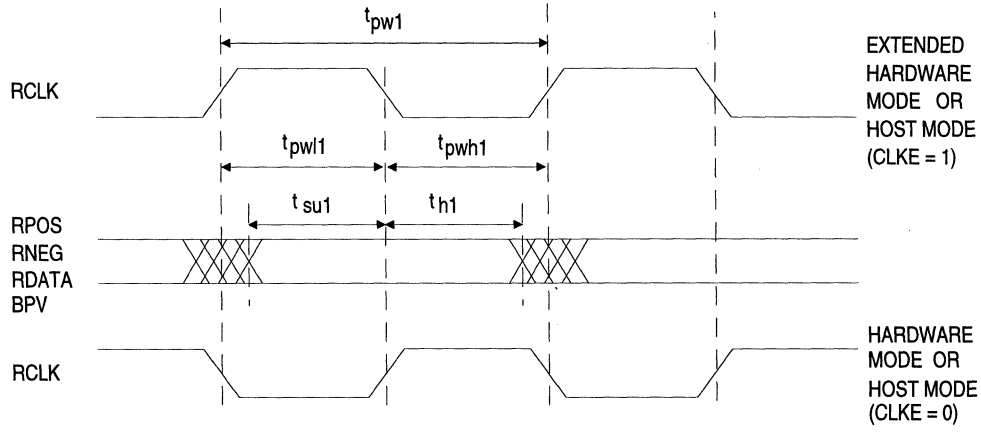


Figure 2. Recovered Clock and Data Switching Characteristics

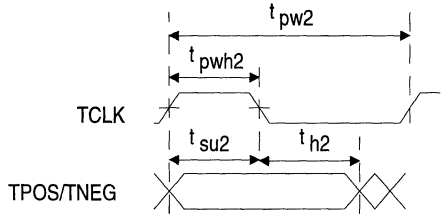


Figure 3. Transmit Clock and Data Switching Characteristics

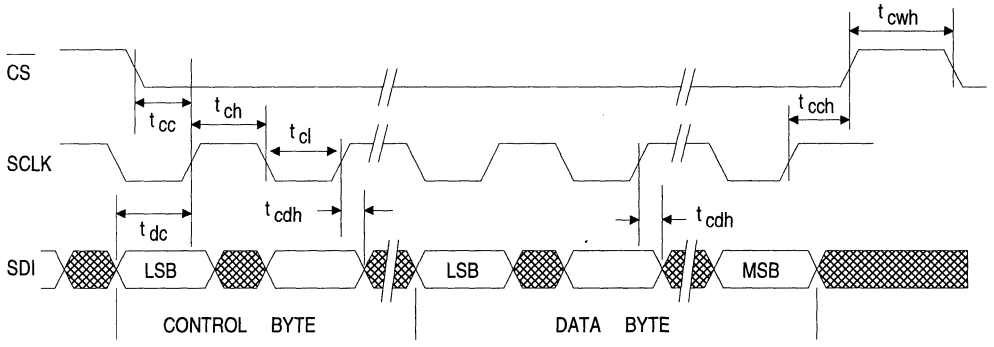


Figure 4. Serial Port Write Timing Diagram

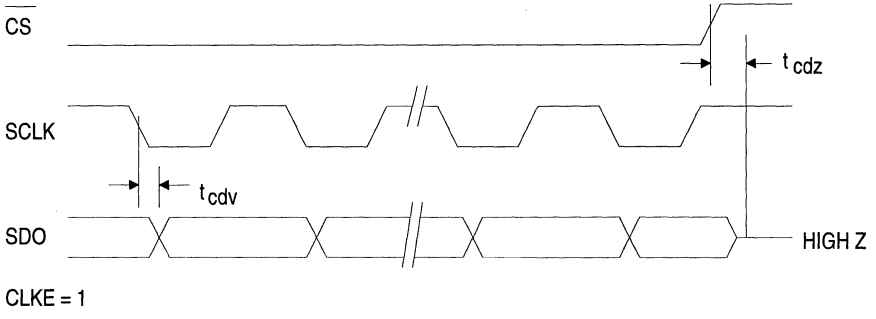


Figure 5. Serial Port Read Timing Diagram

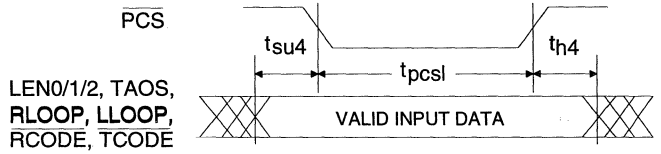


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

CS61577 Enhancements Relative to CS61574

Existing designs using the CS61574 can be converted to the higher performance, pin-compatible CS61577 with no changes to the PCB, external component or system software.

The CS61577 provides higher performance and more features than the CS61574 including:

- Selection of 75 Ω or 120 Ω E1 output options under *software* or hardware control,
- 50 mA_{RMS} transmitter short-circuit current limiting for E1 (per OFTEL OTR-001),
- internally controlled pulse width for E1 output options,
- 35% lower power consumption,
- Increased transmitter immunity to signal reflections for improved signal quality,
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- Improved receiver Loss of Signal handling (LOS set at power-up, reset upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros),
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,
- The Driver Performance Monitor operates over a wider range of input signal levels.

Introduction to Operating Modes

The CS61577 supports three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode. (see Table 2).

	Hardware Mode	**Extended Hardware Mode**	**Host Mode**
Control Method	Control Pins	Control Pins with Parallel Chip Select	Serial Interface
MODE Pin Level	<0.2 V	Floating or 2.5 V	>(RV+)-0.2 V
Line Coding	External	Internal-AMI, B8ZS, or HDB3	External
AIS Detection	No	Yes	No
Driver Performance Monitor	Yes	No	Yes

Table 1. Differences Between Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

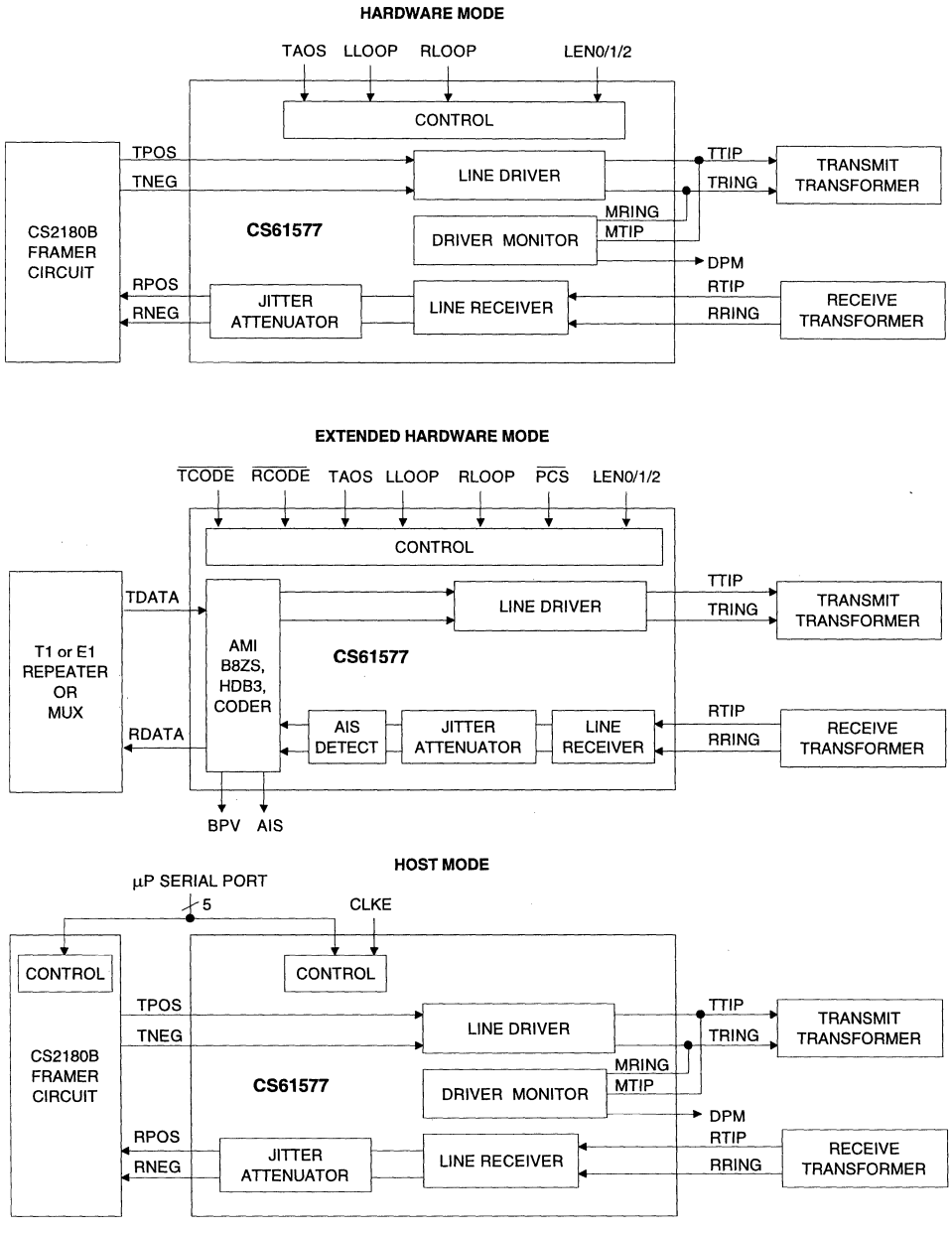


Figure 7. Overview of Operating Modes

Transmitter

The transmitter takes digital T1 or E1 input data and drives appropriately shaped bipolar pulses onto a transmission line through a 1:2 transformer. The transmit data (TPOS & TNEG or TDATA) is supplied synchronously and sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are controlled by "line length select" inputs as shown in Table 3.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) may be selected. The five partition arrangement in Table 3 meets ANSI T1.102 and AT&T CB-119 requirements when using #22 ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, two additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61577 automatically adjusts the pulse width based upon the "line length" selection made.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	0	75 Ω (with 4.4 Ω resistor) & 120 Ω	E1 CCITT G.703
0	0	1	75 Ω (without 4.4 Ω resistor)	
0	1	0	FCC PART 68, OPT. A	NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

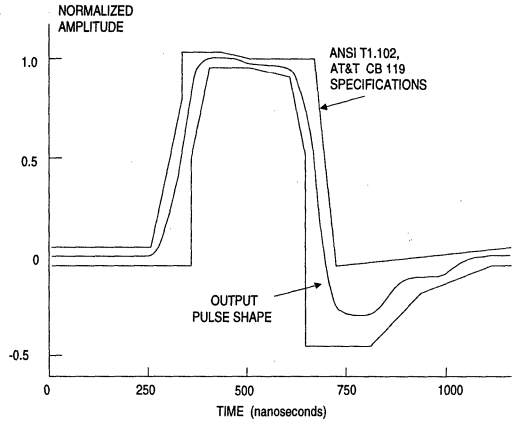


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

The E1 G.703 pulse shape is supported with line length selections LEN2/1/0=0/0/0 or LEN2/1/0=0/0/1. As with the CS61574, LEN2/1/0=0/0/0 supports the 120 Ω, 3 V output option without external series resistors, but will also support the 75 Ω, 2.37 V output option with an external 4.4 Ω resistor in series with TTIP or TRING. The new LEN2/1/0=0/0/1 code supports the 75 Ω, 2.37 V output option without external series resistors allowing for software selection between the two E1 output options. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

The CS61577 will detect a static TCLK, and will force TTIP and TRING low to prevent transmission when data is not present. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

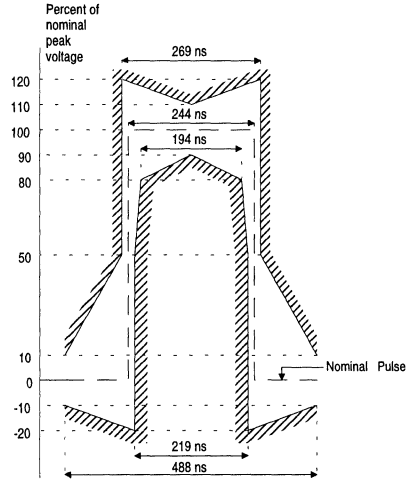


Figure 9. Mask of the Pulse at the 2048 kbps Interface

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, AT&T 62411, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 10. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The out-

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

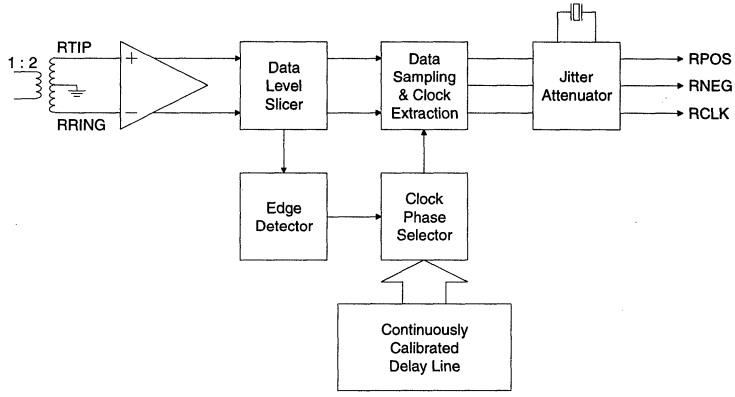


Figure 10. Receiver Block Diagram

put from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 11. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated using the crystal oscillator reference clock. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

In the Hardware Mode, data at RPOS and RNEG should be sampled on the rising edge of RCLK, the recovered clock. In the Extended Hardware Mode, data at RDATA should be sampled on the falling edge of RCLK. In the Host Mode, CLKE determines the clock polarity for which output data should be sampled as shown in Table 5.

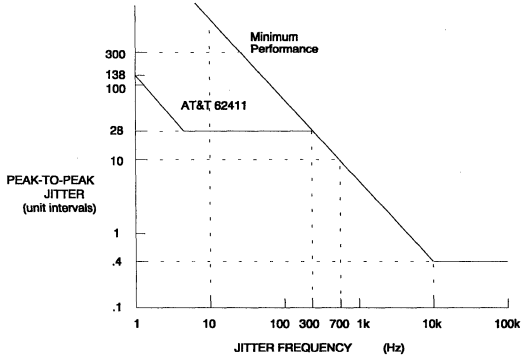


Figure 11. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5V)	X	RDATA	RCLK	Falling

X = Don't Care

Table 5. Data Output/Clock Relationship

Loss of Signal

The receiver will indicate loss of signal after power-up, reset or upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. A zero is received when the RTIP and RRING inputs are below the input comparator slicing threshold level established by the peak detector. After the signal is removed for a period of time the data slicing threshold level decays to approximately 300 mV_{peak}.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$ (unless disabled). LOS will return low (asserting the $\overline{INT}$ pin again in Host Mode) upon receipt of 3 ones in 32 bit periods with no more than 15 consecutive zeros. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12. RPOS/RNEG or RDATA are forced low during LOS unless the jitter attenuator is disabled. (See "Jitter Attenuator" section)

If ACLKI is present during the LOS state, ACLKI is switched into the input of the jitter attenuator, resulting in RCLK matching the frequency of ACLKI. The jitter attenuator buffers any instantaneous changes in phase between the last recovered clock and the ACLKI reference clock. This means that RCLK will smoothly transition to the new frequency. If ACLKI is not present, then the crystal oscillator of the jitter attenuator is forced to its center frequency. Table 6 shows the status of RCLK upon LOS.

Crystal present?	ACLKI present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	ACLKI via the Jitter Attenuator

Table 6. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742.

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG (or RDATA). The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Jitter is absorbed in the FIFO according to the jitter transfer characteristic shown in Figure 12.

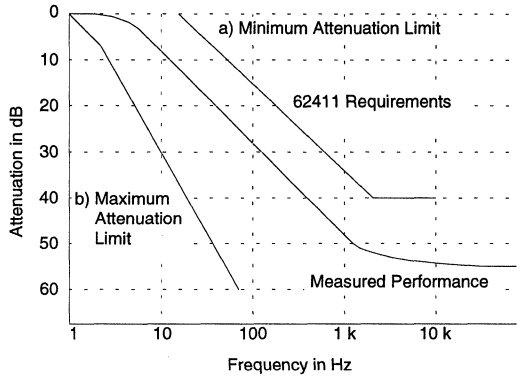


Figure 12. Typical Jitter Transfer Function

The FIFO in the jitter attenuator is designed to prevent overflow and underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

The 32-bit FIFO in the CS61577 attenuator allows it to absorb jitter with minimum data delay in T1 and E1 switching or transmission applications. Like the CS61574, the CS61577 will tolerate large amplitude jitter (>23 UIpp) by tracking rather than attenuating it, preventing data errors so that the jitter may be absorbed in external frame buffers.

The jitter attenuator may be bypassed by pulling XTALIN to RV+ through a 1 kΩ resistor and providing a 1.544 MHz (or 2.048 MHz) clock on ACLKI. RCLK may exhibit quantization jitter of approximately 1/13 UIpp and a duty cycle of approximately 30% (70%) when the attenuator is disabled.

Local Loopback

Local loopback is selected by taking LLOOP, pin 27, high or by setting the LLOOP register bit via the serial interface.

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA), sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG (or RDATA). If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

Remote Loopback

Remote loopback is selected by taking RLOOP, pin 26, high or by setting the RLOOP register bit via the serial interface.

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 6). The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or RDATA). A remote loopback occurs in response to RLOOP going high.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 7. Interaction of RLOOP with TAOS

Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In the Extended Hardware Mode the transmitted data is looped before the AMI/B8ZS/HDB3 encoder/decoder during remote loopback so that the transmitted signal matches the received signal, even in the presence of received bipolar violations. Data output on RDATA is decoded, however, if $\overline{\text{RCODE}}$ is low.

Alarm Indication Signal

In the Extended Hardware Mode, the receiver sets the output pin AIS high when less than 3 zeros are detected out of 2048 bit periods.

Line Code Encoder/Decoder

In the Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using the LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ pins as shown in Table 8.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 8. Encoder/Decoder Selection

Parallel Chip Select

In the Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low and will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The digital control inputs are ignored when $\overline{\text{PCS}}$ is high

Driver Performance Monitor

To aid in early detection and easy isolation of non-functioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally low, and goes high upon detecting a driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period. In the Host Mode, DPM is available from the register and pin 11.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61577 can not be used to monitor a CS61574 due to output stage differences.

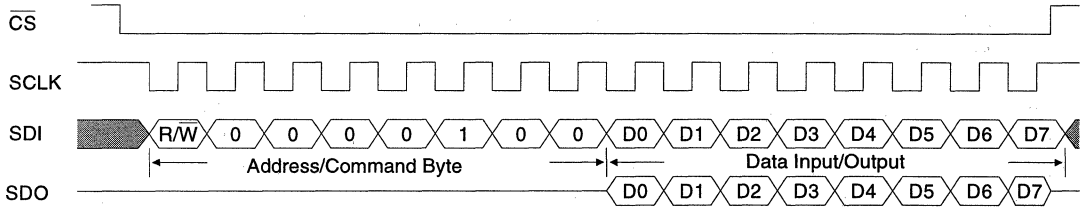


Figure 13. Input/Output Timing

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 5. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 9. Address/Command Byte

An address/command byte, shown in Table 9, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

The data register, shown in Table 10, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61574 into a factory test mode.

Table 10. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be prevented from occurring.

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Input bits 5/6/7=111 and 5/6/7=101 are the same request, and cause the line interface to enter into the factory test mode. In other words, when RLOOP=1 (Bit 5) and TAOS=1 (Bit 7), LOOP (Bit 6) is a don't care. For normal operation, RLOOP and TAOS should not be simultaneously selected via the serial interface.

Output data from the serial interface is presented as shown in Tables 11 and 12. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermittent losses of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 11. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 12. Coding for Serial Output bits 5,6,7

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware Modes, a reset request is made by simultaneously setting both the RLOOP and LLOOP pins high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to

the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration. A reset will also set LOS high.

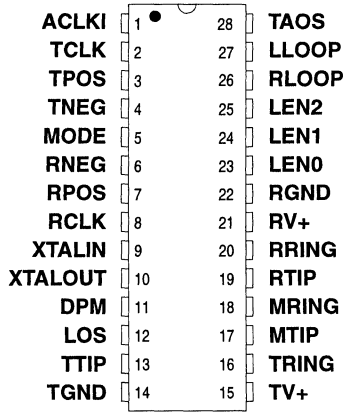
Power Supply

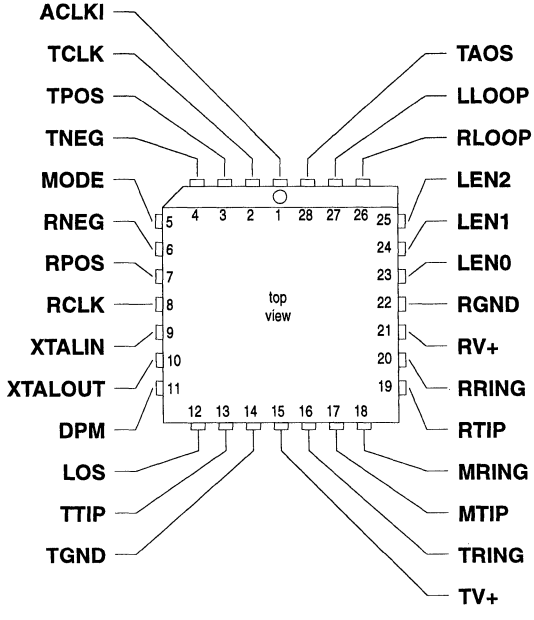
The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

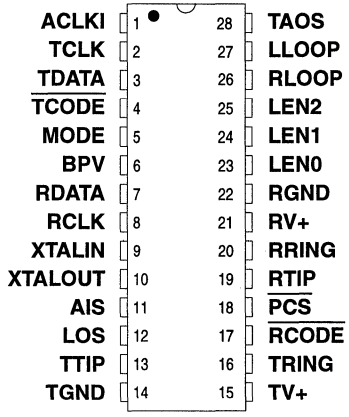
PIN DESCRIPTIONS

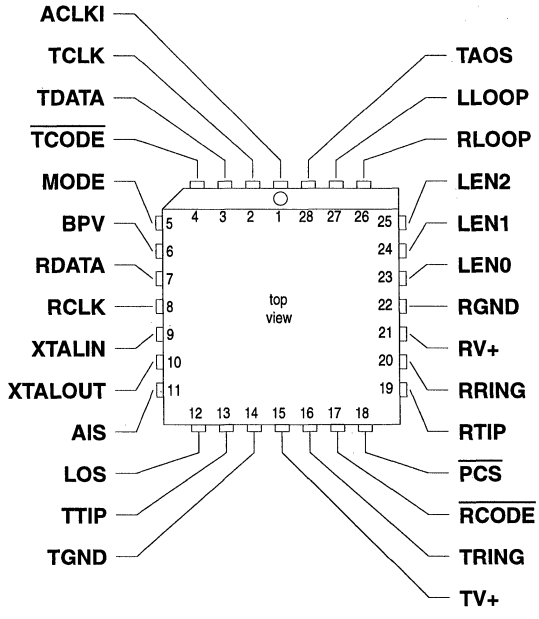
Hardware Mode



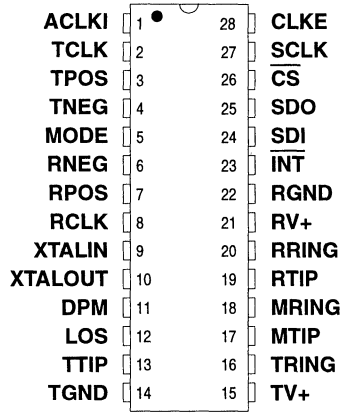


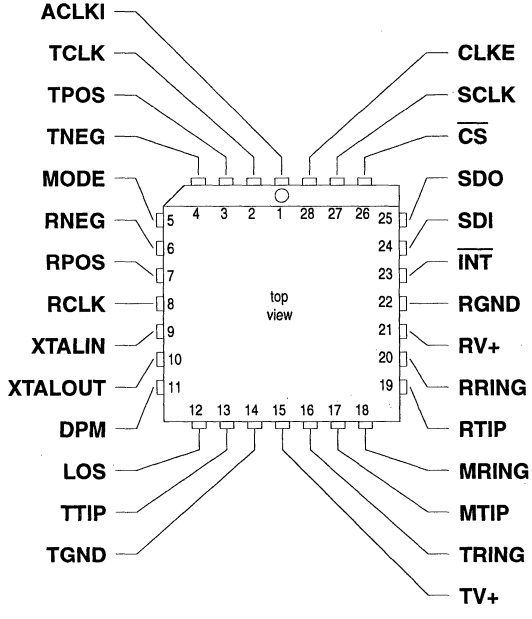
Extended Hardware Mode





Host Mode


ACLKI 1
TCLK 2
TPOS 3
TNEG 4
MODE 5
RNEG 6
RPOS 7
RCLK 8
XTALIN 9
XTALOUT 10
DPM 11
LOS 12
TTIP 13
TGND 14
28 CLKE
27 SCLK
26 CS
25 SDO
24 SDI
23 INT
22 RGND
21 RV+
20 RRING
19 RTIP
18 MRING
17 MTIP
16 TRING
15 TV+


ACLKI
TCLK
TPOS
TNEG
MODE
RNEG
RPOS
RCLK
XTALIN
XTALOUT
DPM
LOS
TTIP
TGND
CLKE
SCLK
CS
SDO
SDI
INT
RGND
RV+
RRING
RTIP
MRING
MTIP
TRING
TV+
top view

Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Overdriving the oscillator with an external clock is not supported.

Control

ACLKI - Alternate External Clock Input, Pin 1.
A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground. During LOS, the ACLKI input signal, if present, is output on RCLK through the jitter attenuator.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)
Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the line interface in the Host Mode. In the host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 Vselects the Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ high causes the line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored. In the Host Mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK. In the Host Mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin.When in the loss of signal state ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator..

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDTA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. The transmitter output is designed to drive a 25 Ω load between TTIP and TRING. A transformer is required as shown in Table A1.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than three zeros out of 2048 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)

BPV goes high for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low when 3 ones are received within 32 bit periods with no more than 15 consecutive zeros. When in the loss of signal state RPOS/RNEG or RDATA are forced low, and ACLKI (if present) is output on RCLK via the jitter attenuator. If ACLKI is not present during LOS, RCLK is forced to the center frequency of the crystal oscillator.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.

APPLICATIONS

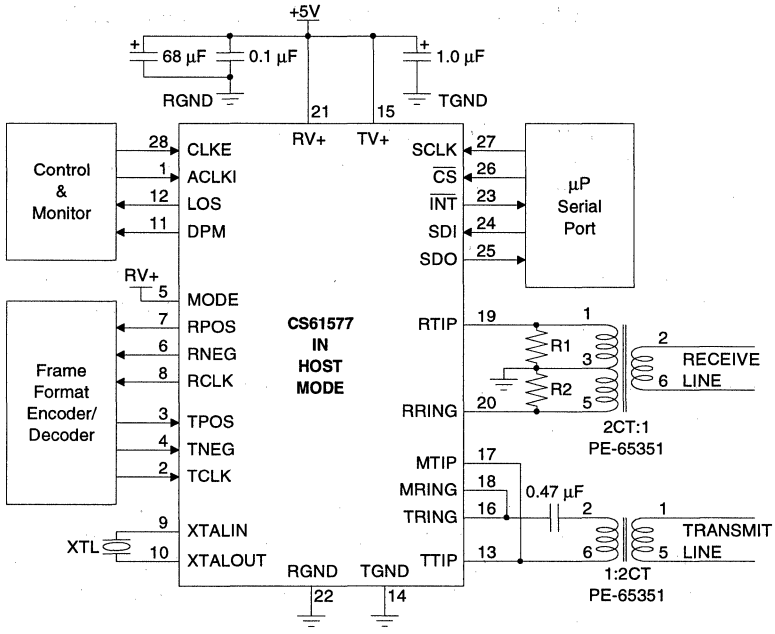


Figure A1. T1 Host Mode Configuration

Frequency MHz	Crystal XTL	Cable Ω	LEN2/1/0	R3 Ω	R1 and R2 Ω
1.544 (T1)	CXT6176	100	0/1/1 - 1/1/1	not used	200
2.048 (E1)	CXT8192	120	0/0/0	not used	240
		75	0/0/0	4.4	150
			0/0/1	not used	

Table A1. External Component Values

Line Interface

Figures A1-A3 show typical T1 and E1 line interface application circuits. Table A1 shows the external components which are specific to each application. Figure A1 illustrates a T1 interface in the Host Mode. Figure A2 illustrates a 120 Ω E1 interface in the Hardware Mode. Figure A3 illustrates a 75 Ω E1 interface in the Extended Hardware Mode.

The 1:2 receiver transformer has a grounded center tap on the IC side. Resistors R1 and R2 between the RTIP and RRING pins to ground provide the termination for the receive line. The transmitter also uses a 1:2 transformer. A 0.47 µF capacitor is required in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

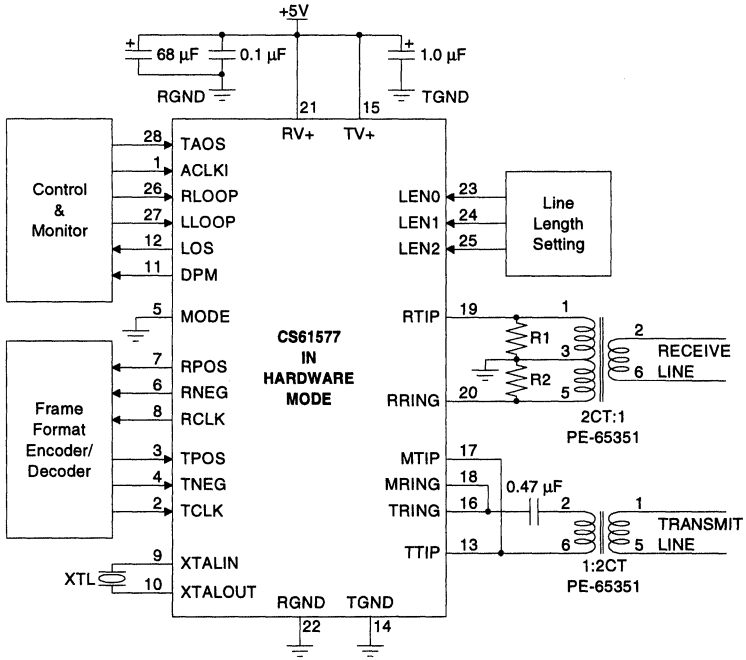


Figure A2. 120 Ω, E1 Hardware Mode Configuration

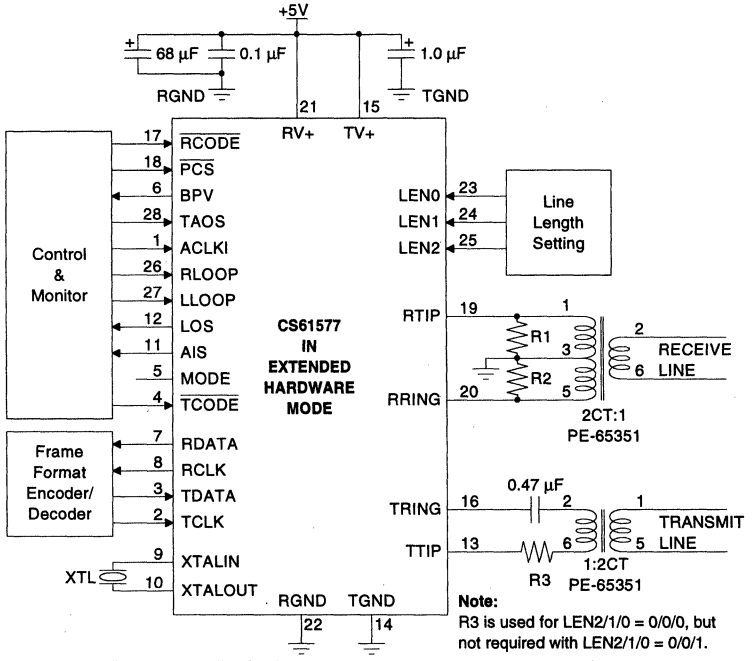


Figure A3. 75 Ω, E1 Extended Hardware Mode Configuration

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61577. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

Turns Ratio	1:2 CT ± 5%
Primary Inductance	600 µH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61577 in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the "Telecom Line Protection Application Note" for detailed information on the different electrical safety standards and specific application circuit recommendations.

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kVsurface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

Interfacing The CS61577 With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A5. In this case, the line interface and CS2180B are in host mode controlled by a microprocessor serial interface. If the line interface is used in Hardware Mode, then the line interface RCLK output must be inverted before being input to the CS2180B. If the CS61577 is used in Extended Hardware Mode, the RCLK output does not have to be inverted before being input to the CS2180B.

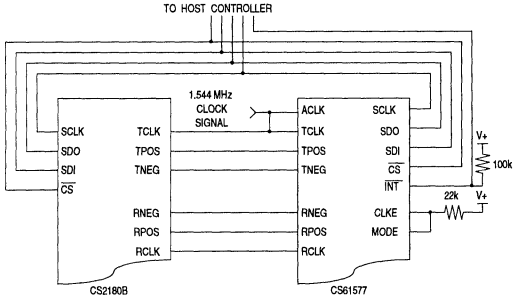


Figure A4. Interfacing the CS61577 with a CS2180B (Host Mode)

• Notes •

Semiconductor Corporation

CS6158A
CS6158

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, and Clock and Data Recovery Functions
- Internal Generation of Transmitted Pulse Width and Pulse Shape
- Low Power Consumption (typically 175 mW)
- Minimum External Components (no external crystal required)
- 14 dB of Transmitter Return Loss

General Description

The CS6158 and CS6158A combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply.

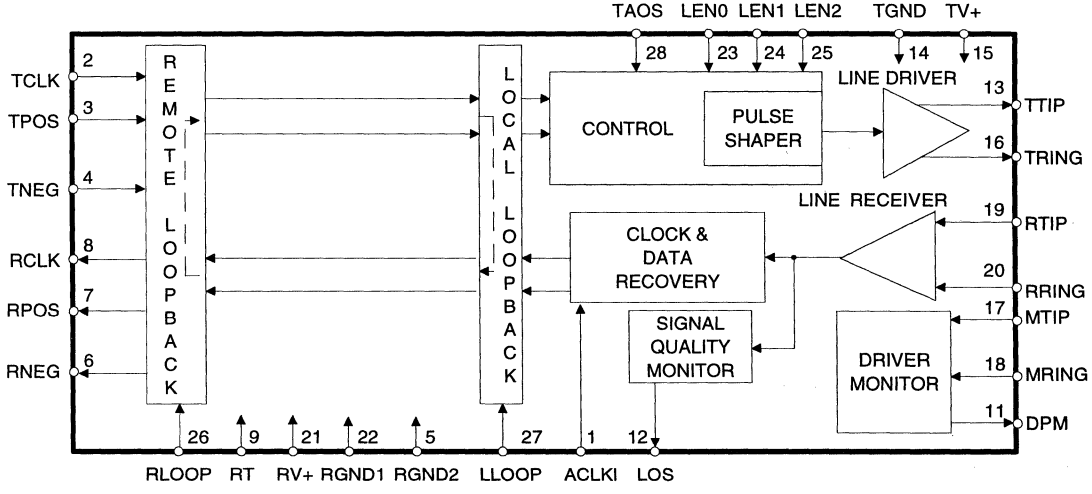
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from an external reference to provide excellent stability and jitter tolerance. The transmitter features internal pulse shaping. The CS6158A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Central Office Exchnges
- Digital Access and Cross Connect Systems
- Large PABX's

ORDERING INFORMATION

CS6158A-IP1	28 Pin Plastic DIP
CS6158A-IL1	28 Pin Plastic PLCC
CS6158-IP1	28 Pin Plastic DIP
CS6158-IL1	28 Pin Plastic PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (referenced to GND)		RV+	-	6.0	V
		TV+	-	(RV+) + 0.3	V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Min	Typ	Max	Units
DC Supply		(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature			T_A	-40	25	85	°C
Power Consumption	CS6158	(Notes 4, 5)	P_C	-	620	760	mW
	CS6158A	(Notes 4, 5)		-	290	350	mW
Power Consumption	CS6158	(Notes 4, 6)	P_C	-	400	-	mW
	CS6158A	(Notes 4, 6)		-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving the load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage		(Note 7) PINS 1-4, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage		(Note 7) PINS 1-4, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage		(Notes 7, 8)	V_{OH}				
CS6158	I_{OUT} = -40 µA	PINS 6-8, 11, 12		2.4	-	-	V
CS6158A	I_{OUT} = -40 µA	PINS 6-8, 11, 12		4.0	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA		(Notes 7, 8) PINS 6-8, 11, 12	V_{OL}	-	-	0.4	V
Input Leakage Current		Except Pin 5		-	-	±10	µA

Notes:
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 9)				
E1, 75 Ω	(Note 10)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 11)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 12)	2.7	3.0	3.3	V
T1, DSX-1	(Note 13)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
75Ω application	(Note 10)	-0.237	-	0.237	V
120Ω application	(Note 11)	-0.3	-	0.3	V
Load Presented To Transmitter Output	(Note 9)				
CS6158		-	25	-	Ω
CS6158A		-	75	-	Ω
Jitter Added by the Transmitter	(Note 14)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 9, 15)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 9, 15)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 9, 15)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
CS6158A Transmitter Return Loss	(Notes 9, 15, 16)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
CS6158A Transmitter Short Circuit Current	(Notes 9, 17)	-	-	50	mA RMS

Notes:
9. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.
10. Amplitude measured at the transformer (CS6158A-1:1 or 1:1.26, CS6158-1:2) output across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0. The CS6158 requires a 4.4Ω resistor in series with the TTIP or TRING pin for this application only.
11. Amplitude measured at the transformer (CS6158A-1:1.26, CS6158-1:2) output across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
12. Amplitude measured at the transformer (CS6158A-1:1.15, CS6158-1:2) output across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
13. Amplitude measured across a 100 Ω load at the DSX-1 Cross-Connect for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0 and 1/1/1 after the length of #22 AWG ABAM equivalent cable specified in Table 1. The CS6158A requires a 1:1.15 transformer and the CS6158 requires a 1:2.
14. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
15. Not production tested. Parameters guaranteed by design and characterization.
16. Return loss = 20 $\log_{10}$ ABS$((z_1 + z_0)/(z_1 - z_0))$ where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
17. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver					
CS6158A RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)					
CS6158		-10	-	-	dB
CS6158A		-13.6	-	-	dB
CS6158A Data Decision Threshold					
T1, DSX-1	(Note 18)	60	65	70	% of peak
T1, DSX-1	(Note 19)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 20)	45	50	55	% of peak
CS6158 Data Decision Threshold	T1	-	65	-	% of peak
	E1	-	50	-	% of peak
Allowable Consecutive Zeros before LOS	(Note 21)	160	175	190	bits
Receiver Input Jitter Tolerance	(Note 22)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold					
CS6158A	(Note 21)	0.25	0.30	0.50	V
CS6158		-	0.30	-	V
Driver Performance Monitor					
CS6158A MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.6	-	V

Notes:
18. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
19. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
20. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
21. LOS goes high after 160 to 190 consecutive zeros are received. A zero is output on RPOS and RNEG for each bit period where the input signal amplitude remains below the data decision threshold. The analog input squelch circuit operates when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V long enough for the internal slicing threshold to decay within this range. Operation of the squelch causes zeros to be output on RPOS and RNEG as long as the input amplitude remains below 0.25V. During receive LOS, pulses greater than 0.25V in amplitude may be output on RPOS and RNEG. LOS returns low after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.
22. Jitter tolerance increases at lower frequencies. See Figure 7.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency			f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width			t_{pwh2}	150	-	500	ns
ACLKI Duty Cycle			t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency		(Note 23)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	CS6158	(Notes 24, 25, 26)	t_{pwh1}/t_{pw1}	-	78	-	%
	CS6158A	(Notes 24, 25, 26)		-	29	-	%
RCLK Cycle Width		(Notes 24, 25, 26)	t_{pw1}	320	648	980	ns
RCLK High Time	CS6158	(Notes 24, 25, 26)	t_{pwh1}	-	508	-	ns
	CS6158A	(Notes 24, 25, 26)		130	190	240	ns
RCLK Low Time	CS6158	(Notes 24, 25, 26)	t_{pwl1}	100	140	-	ns
	CS6158A	(Notes 24, 25, 26)		100	458	850	ns
Rise Time, All Digital Outputs		(Note 27)	t_r	-	-	85	ns
Fall Time, All Digital Outputs		(Note 27)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising		(Notes 25, 26)	t_{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising		(Notes 25, 26)	t_{h1}	50	-	-	ns

Notes: 23. ACLKI may be provided by an external source or TCLK, but *not* RCLK.
24. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
25. Max and Min RCLK duty cycles and pulse widths are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for E1. See text section on *Jitter and Recovered Clock*.
26. Not production tested. Guaranteed by design and/or characterization.
27. At max load of 1.6 mA and 50 pF.

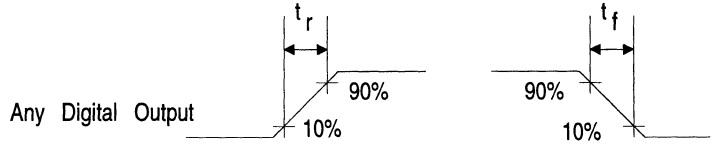


Figure 1. Signal Rise and Fall Characteristics

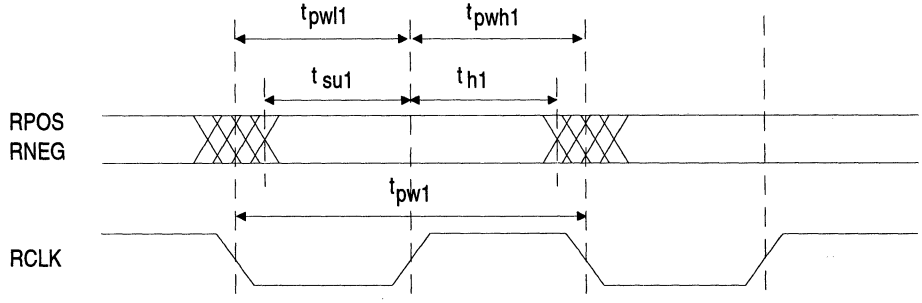


Figure 2. Recovered Clock and Data Switching Characteristics

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency			f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	CS6158	(Note 28)	t_{pwh2}	215	-	258	ns
	CS6158A			150		340	ns
ACLKI Duty Cycle			t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency		(Note 23)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	CS6158	(Notes 24, 25, 26)	t_{pwh1}/t_{pw1}	-	71	-	%
	CS6158A	(Notes 24, 25, 26)		-	29	-	%
RCLK Cycle Width	CS6158	(Notes 24, 25, 26)	t_{pw1}	320	488	670	ns
	CS6158A	(Notes 24, 25, 26)		310	488	670	ns
RCLK High Time	CS6158	(Notes 24, 25, 26)	t_{pwh1}	-	348	-	ns
	CS6158A	(Notes 24, 25, 26)		90	140	190	ns
RCLK Low Time	CS6158	(Notes 24, 25, 26)	t_{pwl1}	100	140	-	ns
	CS6158A	(Notes 24, 25, 26)		120	348	500	ns
Rise Time, All Digital Outputs		(Note 27)	t_r	-	-	85	ns
Fall Time, All Digital Outputs		(Note 27)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising		(Notes 25, 26)	t_{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising		(Notes 25, 26)	t_{h1}	50	-	-	ns

Notes: 28. The transmitted pulse width of LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK for the CS6158 only.

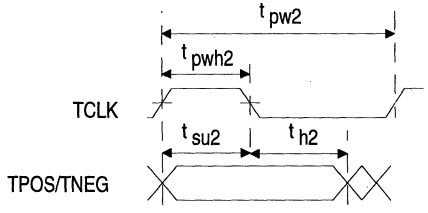


Figure 3a. Transmit Clock and Data Switching Characteristics

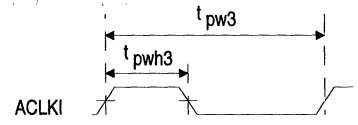


Figure 3b. Alternate External Clock Characteristics

THEORY OF OPERATION

Enhancements in CS6158A

The CS6158A provides higher performance and more features than the CS6158 including:

- 50% reduction in power consumption
- 14 dB of transmitter return loss (during marks and spaces) improves signal quality.
- The E1 transmitted pulse width is set internally by the CS6158A (and not by the TCLK input duty cycle).
- Upon power up, RCLK immediately starts and LOS (loss of signal) is set high.
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- ANSI T1.231-1993 compliant receiver LOS (Loss Of Signal) handling.
- The driver performance monitor operates over a wider range of input signal levels.

CS6158 designs can be converted to the higher performance, pin-compatible CS6158A if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio.

Transmitter

The transmitter takes data from a T1 (or E1) terminal and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 (DSX-1 or Network Interface) or CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS6158A line driver is designed to drive a 75 Ω equivalent load. The CS6158 drives a 25 Ω load.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1		RESERVED
0	0	0	75Ω and 120Ω	E1 CCITT G.703
0	1	0	FCC PART 68, OPT. A	T1 NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1. Line Length Selection

For E1 applications, the CS6158A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the IC to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 4. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

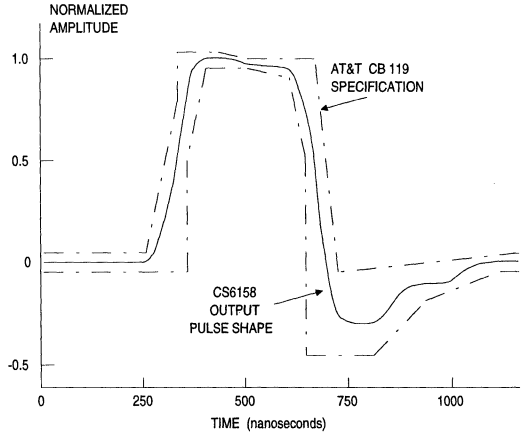


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figure A1.

Table 2. CCITT G.703 Specifications

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS6158A automatically adjusts the pulse width based upon the "line length " selection made.

The E1 CCITT G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 5, and specified in Table 2.

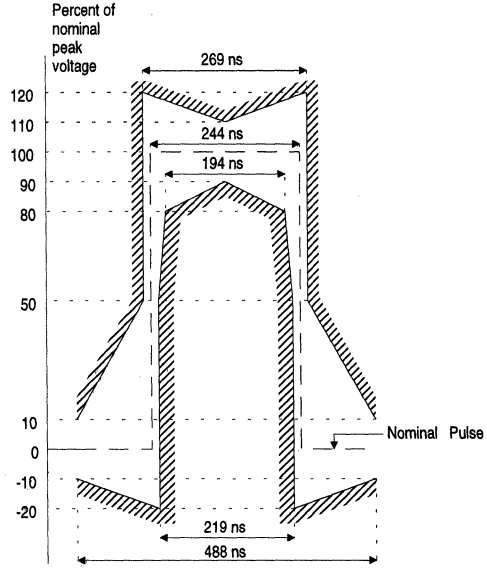


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

Only in the case of CS6158 and LEN2/1/0= 0/0/0, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5 assuming the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur.

The CS6158A transmitter will detect a failed TCLK, and will insure that neither TTIP nor TRING gets stuck high. If the clock signal is removed from TCLK on the CS6158, TPOS and TNEG should both be low during the last falling edge of TCLK. This places the CS6158 in a low-power dissipation mode.

When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes

continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals down to approximately 300 mV in amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS6158A or CS6158 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI, into 13 equal divisions of phases. Continuous calibration ensures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that plot shown in Figure 7.

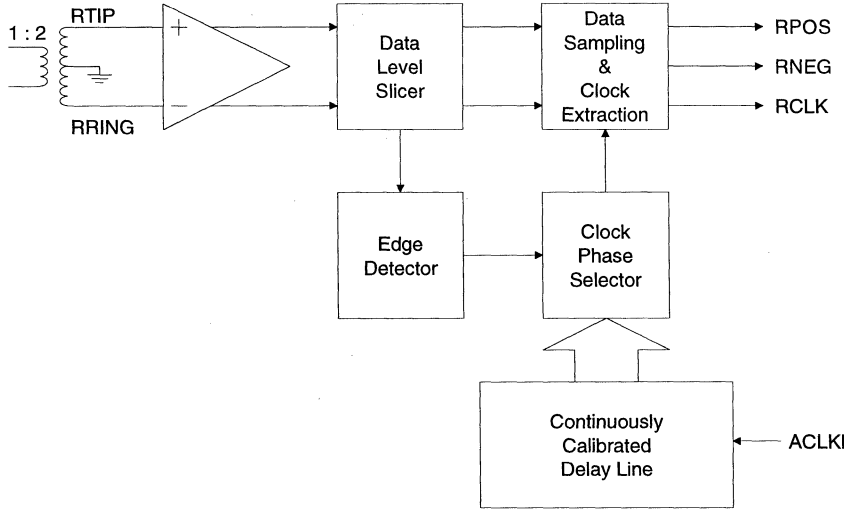


Figure 6. - Receiver Block Diagram

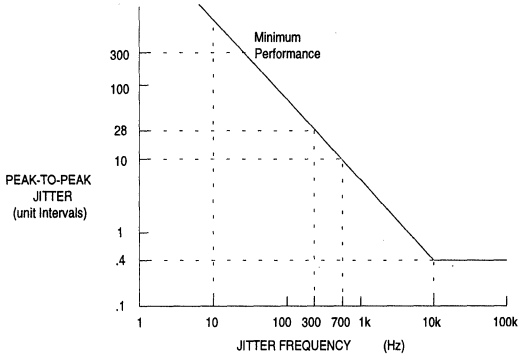


Figure 7. - Input Jitter Tolerance of Receiver

The CS6158 device outputs a clock at RCLK after the first signal is input to RTIP/RRING. The CS6158A outputs a clock on RCLK immediately upon power-up. In either case, the clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

Data on RPOS and RNEG is stable and may be sampled on the rising edge of RCLK, the recovered clock.

Jitter and Recovered Clock

The CS6158A and CS6158 are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS6158A and CS6158, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the 2.048 MHz rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS6158A and CS6158, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS6158A and CS6158 is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period

later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. In the CS6158, LOS returns to a logic zero upon receipt of the first bit at the RTIP/RRING inputs. In the CS6158A, LOS returns to logic zero after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

Also in the CS6158A, a power-up or manual reset will set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line. Because RCLK cycle times vary, selecting RLOOP will result in adding jitter to the transmitted data. *Therefore selection of the RLOOP function on a functioning link is not recommended.* Rather, it is recommended that remote loopbacks be implemented external to the CS6158A and CS6158, for example, by using a frame buffer in the data path between the CS6158A and CS6158 receiver and transmitter.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6158A and CS6158 are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS6158A can not be used to monitor a CS6158 due to output stage differences.

For the CS6158 only, DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Power On Reset / Reset

Upon power-up, the CS6158A and CS6158 are held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear the internal logic.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP or LLOOP).

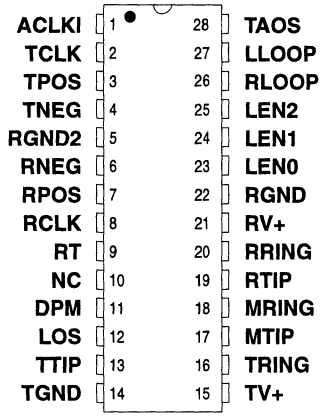
A reset will set LOS high on the CS6158A.

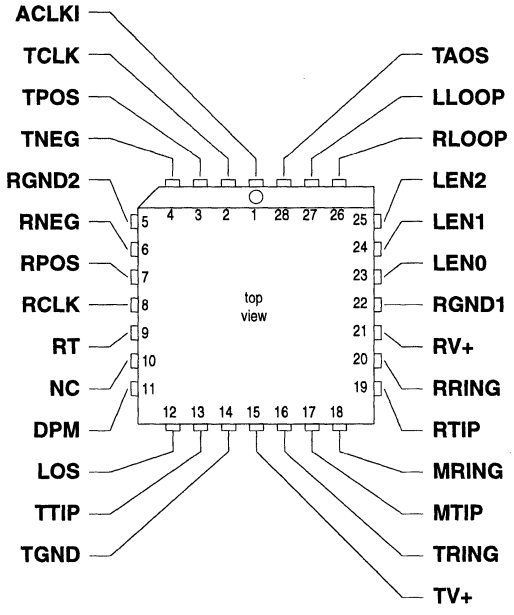
Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS





Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 Volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 Volts.

RGND1, RGND2 - Ground, Pins 22 and 5

Power supply grounds for the device, except transmit drivers; typically 0 Volts.

Control

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TAOS - Transmit All Ones select, Pin 28.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency selected by TCLK.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.

Either a 1.544 MHz (or 2.048 MHz for E1) clock must be input to ACLKI, which is used to calibrate the receiver delay line. Since ACLKI is used to calibrate the receiver, RCLK will equal ACLKI upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

RT - Resistor Termination, Pin 9.

This pin should be connected to the RV+ power supply through a 1kΩ resistor.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the transmitter output. If the monitor is not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. In the CS6158, LOS returns to logic 0 on the first bit received. When in the loss of signal state, received ones are output at RPOS/RNEG. In the CS6158A, LOS returns to a logic 0 after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING, DPM goes to a logic 1.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

The receiver recovered clock and NRZ digital data is output on these pins. RPOS and RNEG are stable and valid on the rising edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins.

For the CS6158A, this output is designed to drive a 75 Ω ohm load. A transformer is required as shown in Figure A1.

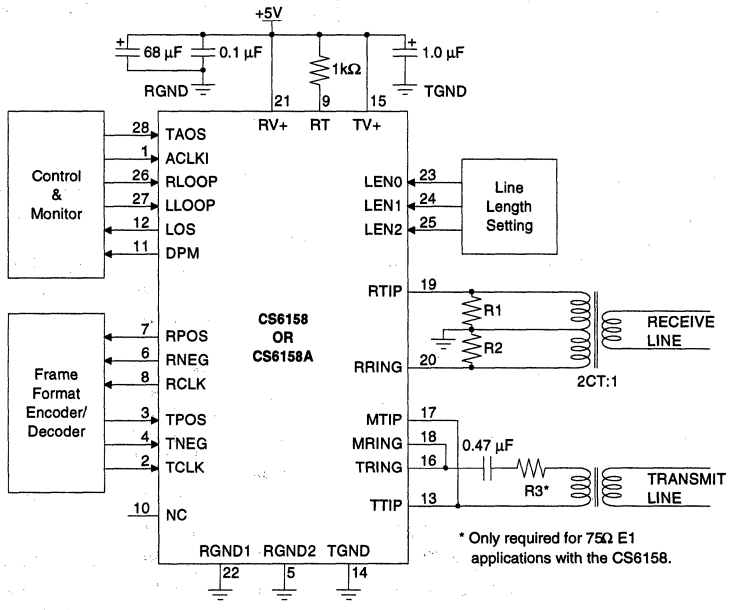
For the CS6158, this output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, 4.4 Ohms of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

Miscellaneous

NC - No Connect, Pin 10

Pin 10 may be left floating (recommended for new designs), or may be tied to ground.

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3 Ω	Transmit Transformer
CS6158	1.544	100	200	0	1:2
	2.048	120	240	0	1:2
	2.048	75	150	4.4	1:2
CS6158A	1.544	100	200	0	1:1.15
	2.048	120	240	0	1:1.26
	2.048	75	150	0	1:1

Figure A1. - Typical Connection Diagram

Line Interface

Figure A1 shows the typical configuration for the CS6158A and CS6158. Note that CS6158A transmitter transformer requirements have changed from those of the CS6158. This new transformer allows the CS6158A's lower power driver to be implemented.

For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω resistors between the center tap and each leg on the IC side. These resistors provide the 100 Ω termination for the T1 line. When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load. For transmitting data at 2.048 MHz onto a 75 Ω coax cable, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 µF capacitor in series

with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

Transformers

Recommended transmitter and receiver transformer specifications for the CS6158 and CS6158A are shown in Table A1. The transformers in Table A2 have been tested and recommended for use with the CS6158. The transformers in Table A3 have been tested and recommended for use with the CS6158A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications with the CS6158A where it is advantageous to use a single transmitter transformer for both 75Ω and 120Ω E1 applications, a 1:1.26 transformer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct.

Interfacing the CS6158A with CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A2.

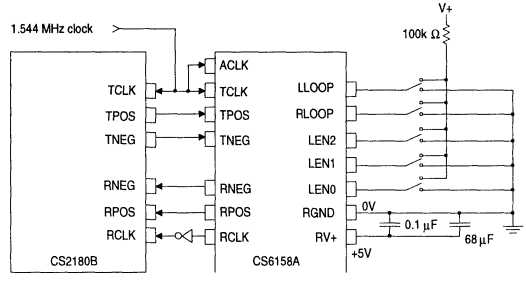


Figure A2. - Interfacing the CS6158A with a CS2180B

Parameter	CS6158 Receiver & Transmitter CS6158A Receiver	CS6158A Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 120 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 75 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A1. Transformer Specifications

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kVsurface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A2. Recommended Transformers For The CS6158

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers For The CS6158A

Semiconductor Corporation

CDB61534, CDB61535, CDB61535A, CDB61574, CDB61574A, CDB61575, CDB61577, CDB6158, & CDB6158A

PCM Line Interface Evaluation Board

Features

- Socketed Line Interface IC
- All Required Components for Complete Line Interface Evaluation
- DIP Switch or Serial Interface Configuration
- LED Status Indicators
- Support for Host, Hardware, and Extended Hardware Modes

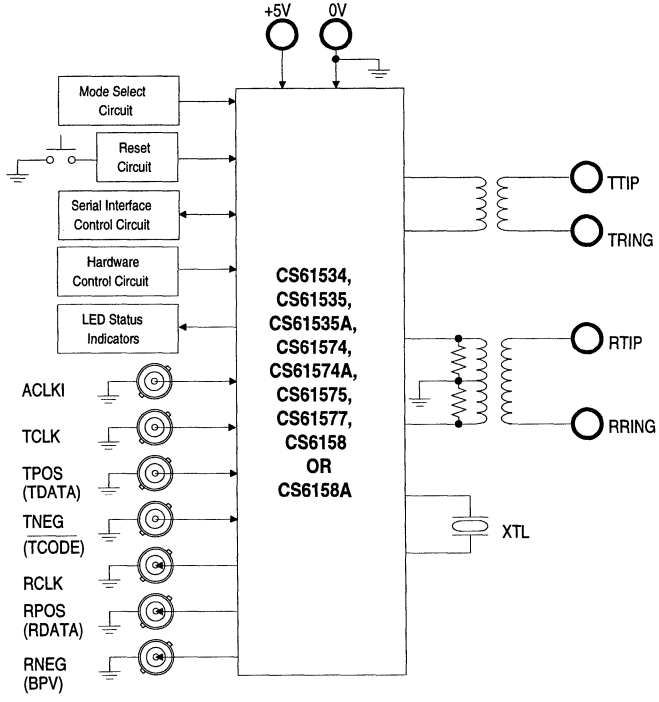
General Description

The evaluation board includes a socketed line interface IC and all support components required for evaluation. The board is powered by an external 5 Volt supply.

Four binding posts are provided for line connections. The board may be configured for use with 100 Ω twisted-pair T1 lines as well as 75 Ω coax or 120 Ω twisted-pair EI lines. BNC connectors are provided for all IC digital clock and data inputs and outputs. LED indicators are provided to monitor IC status outputs. The board supports all of the operating modes available in the supplied line interface.

ORDERING INFORMATION:

CDB61534, CDB61535, CDB61535A,
CDB61574, CDB61574A, CDB61575,
CDB61577, CDB6158, CDB6158A.



CIRCUIT DESCRIPTION

Power Supply

As shown on the schematic in Figure 1, power is supplied to the evaluation board from an external +5 Volt supply connected to the two binding posts labeled +5V and GND. D10 is a transient suppressor which protects the components on the board from over-voltage damage and reversed supply connections. The recommended supply decoupling is provided by C1, C2 and C3. C3 is the 1.0 µF capacitor which decouples TV+ to TGND. C2, a 0.1 µF ceramic capacitor, and C1, a 68 µF electrolytic or tantalum capacitor, are used to decouple RV+ to RGND. The TV+ and RV+ power supply traces are connected at the IC. The component side of the evaluation board is used as a ground plane insuring optimum performance.

Control Circuit

The evaluation board schematic is shown in Figure 1. Pins on the line interface IC, U1, with more than one pin name have different functions depending upon the operating mode selected. Pin names enclosed in parenthesis describe the pin's function only in the Extended Hardware mode, while pin names enclosed in square brackets describe the pin's function only in the Host mode.

The evaluation board may be configured to support all available operating modes in the supplied line interface IC. The CS61535A, CS61574A, CS61577 and CS61575 support the Host, Hardware and Extended Hardware operating modes. The CS61534, CS61535 and CS61574 support the Host and Hardware operating modes. The CS6158 and CS6158A only support the Hardware operating mode. Mode selection is accomplished with the slide switch SW1 and three jumpers, JP2, JP6 and JP7 (refer to Table 1). After the line interface operating mode is changed with SW1 note that JP2, JP6 and JP7 must be changed as well. Refer to Table 1 information on how to configure the evaluation board jumpers.

Hardware Mode

For Hardware mode operation the line interface is configured using the DIP switch S2. In this mode, the DIP switch sets the IC digital control inputs which select: transmit line length (LEN2,1,0), local loopback (LLOOP), remote loopback (RLOOP), and transmit all ones (TAOS). Closing a DIP switch (or placing it in the on position) sets the IC control pin of the same name to logic 1 (+5 Volts). Note that the $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ switch positions have no function in the Hardware mode. Also, JP1, the host processor interface connector, should be left open in the Hardware mode.

Two LED status indicators are provided in the Hardware mode. The LED labeled LOS illuminates to indicate that the line interface has detected the loss of the receive input signal. The LED labeled DPM(AIS) illuminates when the line interface asserts the Driver Performance Monitor alarm. (This LED reports the detection of AIS, receive blue alarm, in the Extended Hardware mode.)

Host Mode

For Host mode operation, the line interface is configured by a host processor connected to the serial interface port, JP1. In this mode, the S2 position labeled TAOS/CLKE is used to select the active edges of SCLK and RCLK. Closing (turning on) the TAOS/CLKE position of S2 selects SDO valid during the rising edge of SCLK and RPOS and RNEG valid during the falling edge of RCLK as required by the CS2180B T1 framer. All other DIP switch positions on S2 should be left open (off) to prevent shorting together any of the serial interface signals. R15 is a current limiting resistor which will prevent any of the serial interface signals from being shorted directly to the board's +5 Volt supply in the event that any S2 switches other than CLKE are accidentally closed. JP3 should be open to disconnect the pull-down resistor on $\overline{\text{INT}}$, pin 23 of the IC, so that

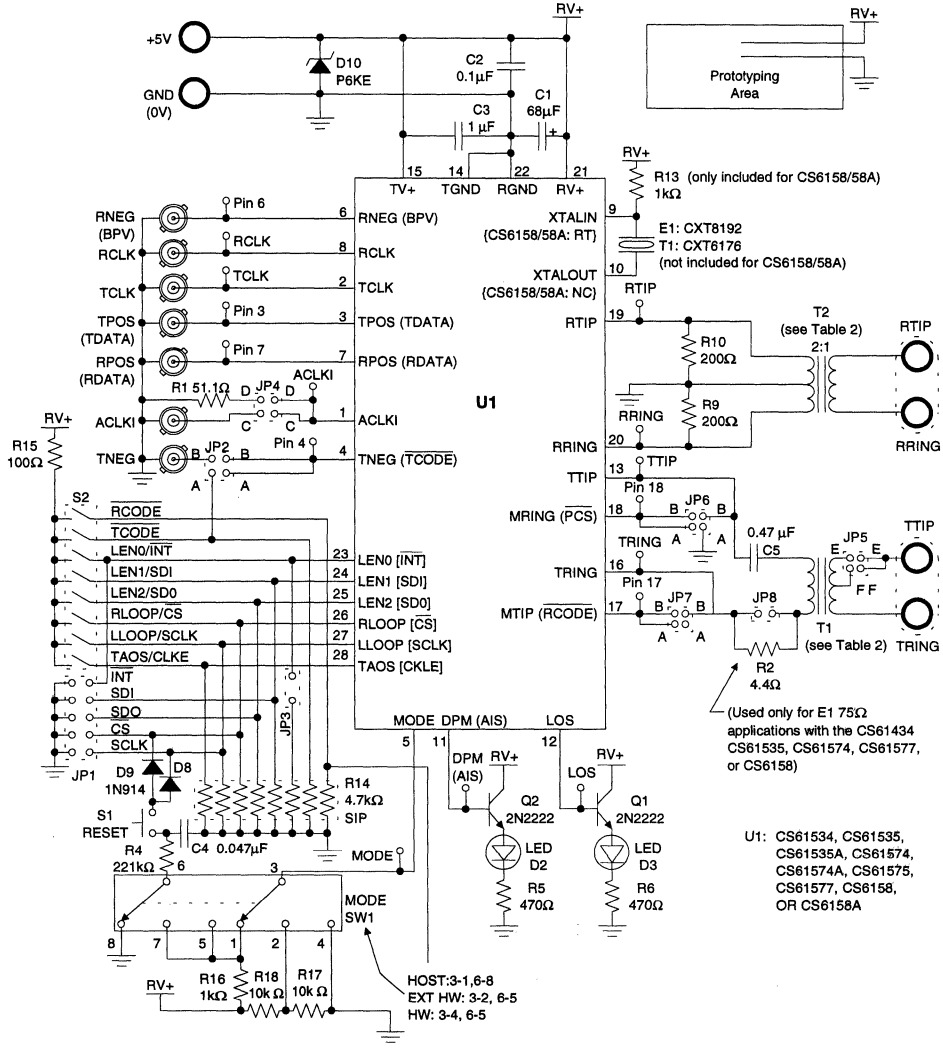


Figure 1. Evaluation Board Schematic

this pin may be externally pulled-up at the host processor interrupt pin.

In the Host mode, the LOS LED illuminates to indicate receiver Loss Of Signal, while the DPM LED illuminates to indicate a Driver Performance Monitor alarm.

Extended Hardware Mode

For Extended Hardware mode operation, the line interface is configured using the DIP switch S2. In this mode, the DIP switch sets the IC digital control inputs which select: transmit line length (LEN0,1,2), local loopback (LLOOP), remote loopback (RLOOP), transmit all ones (TAOS), receive line code ($\overline{\text{RCODE}}$), and transmit line code ($\overline{\text{TCODE}}$). Closing a DIP switch (placing it in the on position) sets the IC control pin of the same name to logic 1 (+5 Volts). Note that the IC's parallel chip select input, $\overline{\text{PCS}}$, is tied to ground so that the device will be reconfigured any time S2 is changed. JP1, the serial interface connector, should be left open in the Extended Hardware mode.

Two LED status indicators are provided in the Extended Hardware mode. The LED labeled LOS illuminates to indicate that the line interface has detected the loss of the receive input signal. The LED labeled DPM(AIS) illuminates when the line interface detects AIS, receive blue alarm. (This LED reports the Driver Performance Monitor alarm in the Hardware and Host modes.)

Crystal / Alternate Clock Input

A quartz crystal should be installed in the socket Y1 for all ICs except the CS6158 and CS6158A. A Crystal Semiconductor CXT6176 crystal is recommended for T1 operation, while a CXT8192 is recommended for PCM-30 operation. The evaluation board has a CXT6176 installed at the factory. A CXT8192 is also provided with the board.

For the CS6158 and CS6158A, R13 is installed instead of a crystal to tie the RT pin of the IC to the +5 Volt supply.

The ACLKI BNC is used to provide the alternate clock reference for the line interface ACLKI (ACLK for the CS61534) input pin when JP4 is jumpered across C-C. This clock is required for the CS61535, CS6158 and CS6158A, but is optional for other devices. When an external 1.544 MHz or 2.048 MHz clock is not provided on this connector JP4 should be jumpered across D-D to ground pin 1 of the IC through R1. Note that it may be desirable to connect C-C and D-D on JP4 to terminate the external clock source providing ACLKI with the 51 Ω resistor R1.

JUMPER	POSITION	FUNCTION SELECTED
JP1	-	Host Processor Connector
JP2, JP6, JP7	A-A	Extended Hardware Mode
	B-B	Host Mode or Hardware Mode
JP3	IN	pin 23 pulled down by R14 (normal for Hdw/Ext. Hdw Modes)
	OUT	pin 23 may be pulled up at host controller (normal for Host Mode)
JP4	C-C	connects ACLKI BNC to Pin 1
	D-D	grounds Pin 1 through R1
JP5	E-E	TX line connection for all applications except those on the next line
	F-F	for 75 Ohm applications with the Schott 12485/12532
JP8	IN	shorts R2 for all applications except those on the next line
	OUT	inserts R2 for 75 Ohm applications with the CS61534,35,74 or 58

Table 1. Evaluation Board Jumper Settings

Prototyping Area

A prototyping area with power supply and ground connections has been provided on the evaluation board. This area can be used to develop and test a variety of additional circuits like a data pattern generator, CS2180B framer IC, system synchronizer PLL, or specialized interface logic.

Reset Circut

A reset circuit is provided in the Hardware and Extended Hardware operating modes which generates both power-on and manual reset outputs. This circuit consists of R4, R5, D8, D9 and S1. Note that reset is only necessary for the CS61534 IC to insure the accurate calibration of its receiver clock recovery circuit center frequency. All other ICs use a continuously calibrated clock recovery circuit eliminating the need for a reset.

Transmit Circuit

The line interface IC digital transmitter clock and data input signals are supplied using the BNC connectors labeled TCLK, TPOS(TDATA) and TNEG. In the Hardware and Host operating modes, data is supplied on the TPOS(TDATA) and TNEG connectors in dual NRZ format. In the Extended Hardware operating mode, data is supplied in NRZ format on the TPOS(TDATA) connector and the TNEG connector is not used.

The transmitter output is coupled onto the line connected at the TTIP and TRING binding posts using a step-up transformer denoted T1 in Figure 1. C5 is the recommended 0.47 µF DC blocking capacitor. Table 2 lists the transformers and line interface ICs which may be used in T1 or PCM-30 applications. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the IC when the transformer is installed in the board with pin 1 positioned to match the letter shown on the drawing in Table 2. For example, the Schott 12498 may be used with the transmitter of the CS61574A for T1 (1.544 MHz) applications (as indicated by note 3) when installed as T1 (Transformer #1) with pin 1 at position B.

The evaluation board supports 100 Ω twisted-pair T1 lines, 75Ω coax PCM-30 lines and 120 Ω twisted-pair PCM-30 lines. The CDB61534, CDB61535, CDB61574, CDB61577 and CDB6158 are supplied from the factory with a 1:2 transmit transformer which may be used in both T1 and PCM-30 applications. The CDB61535A, CDB61574A, CDB61575 and CDB6158A are supplied with a 1:1.15 transmit transformer installed for T1 applications, and an additional transformer for PCM-30 applications is provided with the board. For all applications except the two described below, JP8 must be installed and JP5 must be connected across E-E.

For 75Ω coax applications using the CS61534, CS61535, CS61574, CS61577 or CS6158, JP5 should be connected across E-E and a 4.4Ω resistor must be installed at R2. JP8 must be removed. R2 is used to reduce the pulse amplitude to meet the 2.37 V nominal pulse amplitude required by CCITT G.703. In addition, R2 increases the equivalent load impedance across the IC TTIP and TRING pins.

For 75Ω coax applications using the CS61535A, CS61574A, CS61575 or CS6158A, JP8 must be installed. JP5 must be connected across F-F for use with the Schott 12485 or Schott 12532. JP5 must be connected across E-E for use with the PE-65400.

Receive Circuit

The IC receiver inputs are transformer coupled to the line connected to the RTIP and RRING binding posts on the board. A center-tapped, center-grounded 1:2 transformer, T2, is used to produce ground referenced pulses of equal amplitude and opposite polarity on the RTIP and RRING pins of the IC.

Table 2 lists the transformers and line interface ICs which may be used together in T1 or PCM-30 applications. A letter at the intersection of a row and column in Table 2 indicates that the selected transformer is supported for use with the IC when the transformer is installed in the board with pin 1 positioned to match the letter shown on the drawing in Table 2. For example, The PE-65351 is supported for use with the receiver of the CS61574 when installed as T2 with pin 1 at position A.

The receive line is terminated by the resistors R9 and R10. As supplied from the factory, R9 and R10 are 200Ω resistors for terminating a 100Ω T1 twisted-pair line. R5 and R6 should be replaced with 240Ω resistors for terminating a balanced 120Ω PCM-30 twisted-pair line. For a 75Ω unbalanced coax line, R5 and R6 should each be 150Ω.

Access to the IC digital receiver clock and data outputs is provided by the BNC connectors labeled RCLK, RPOS(RDATA) and RNEG(BPV). In the Hardware and Host modes data is output in dual NRZ format on RPOS(RDATA) and RNEG(BPV). In the Extended Hardware mode data is output in NRZ format on RPOS(RDATA) and bipolar violations are reported on RNEG(BPV).

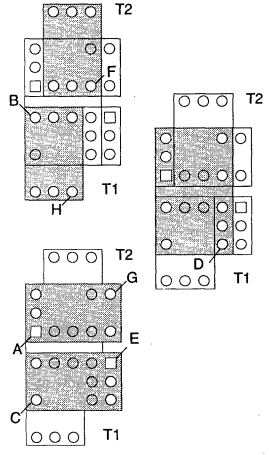
EVALUATION HINTS

1. Be sure to properly terminate TTIP/TRING when evaluating the transmitter output signal. For more information on pulse shape evaluation refer to the Crystal application note AN-7 entitled, "Measurement and Evaluation of Pulse Shapes in T1/PCM-30 Transmission Systems".

2. Note that the S2 position marked open or off grounds the corresponding pin of the same name on the IC.

3. To avoid damage to a host controller connected to JP1, all S2 positions except TAOS/CLKE should be open or off. In the Host mode, the TAOS/CLKE position of S2 selects the active edge of SCLK and the active edge of RCLK.

TRANSFORMER (and turns ratio)	LINE INTERFACE IC															
	'34		'35		'35A		'74, '77		'74A		'75		'58		'58A	
	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX
PE-64951 (dual 1:2CT)	D		D				D						D			
PE-65565 (dual 1:1.15 & 1:2CT)					D^3				D^3		D^3				D^3	
PE-65566 (dual 1:1:1.26 & 1:2CT)					D^5				D^5		D^5				D^5	
Schott 12531 (dual 1:1.15 & 1:2CT)					D^3				D^3		D^3				D^3	
Schott 12532 (dual 1:1:1.26 & 1:2 CT)					D^6				D^6		D^6				D^6	
Schott 11509 (dual 1:2CT)	D		D				D						D			
PE-64931 (1:2CT)	F	B	F	B	F		F	B	F		F		F	B	F	
PE-65351 (1:2CT)	A	E	A	E	A		A	E	A		A		A	E	A	
Schott 11510 (1:2CT)	F	B	F	B	F		F	B	F		F		F	B	F	
Schott 12467 (1:2CT)	G	C	G	C	G		G	C	G		G		G	C	G	
PE-65387 (1:1.15)						H^3				H^3		H^3				H^3
PE-65388 (1:1.15)						E^3				E^3		E^3				E^3
PE-65389 (1:1:1.26)						E^5				E^5		E^5				E^5
Schott 12484 (1:1.15)						C^3				C^3		C^3				C^3
Schott 12485 (1:1:1.26)						C^6				C^6		C^6				C^6
Schott 12498 (1:1.15)						B^3				B^3		B^3				B^3
PE-65400 (1:1)						H^4				H^4		H^4				H^4
PE-65401 (1:1.26)						H^5				H^5		H^5				H^5



NOTES:

1. A letter in the table indicates that the corresponding transformer and IC may be used together. The transformer is installed with pin 1 in the position given by the letter (see the figure at left).
2. RX (receive) transformer is denoted T2 on the PCB silkscreen. TX (transmit) transformer is denoted T1 on the PCB silkscreen.
3. For use in 100Ω T1 twisted-pair applications only.
4. For use in 75Ω PCM-30 coax applications only.
5. This transformer is supported for use in 120Ω PCM-30 twisted-pair applications only.
6. This transformer is supported for use in 75Ω and 120Ω PCM-30 applications.

Table 2. Transformer Applications

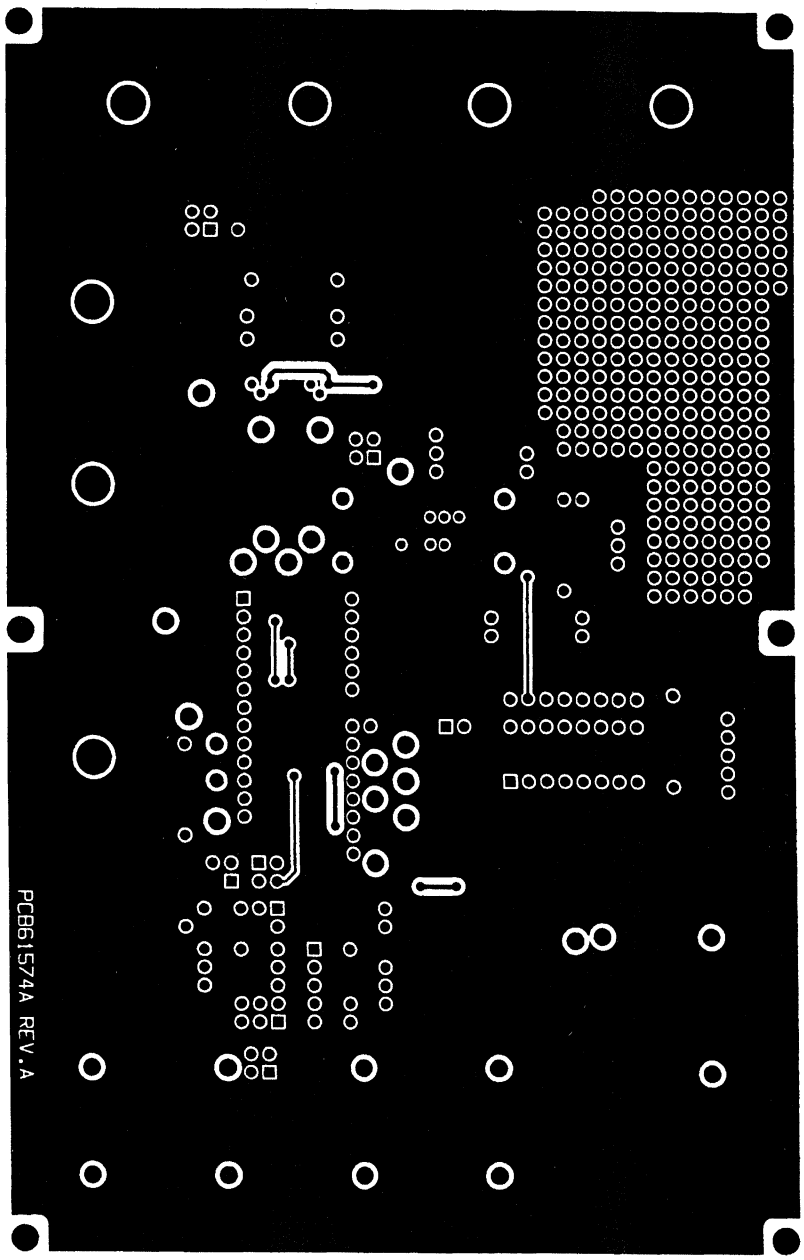


Figure 2. Top Ground Plane Layer (NOT TO SCALE)

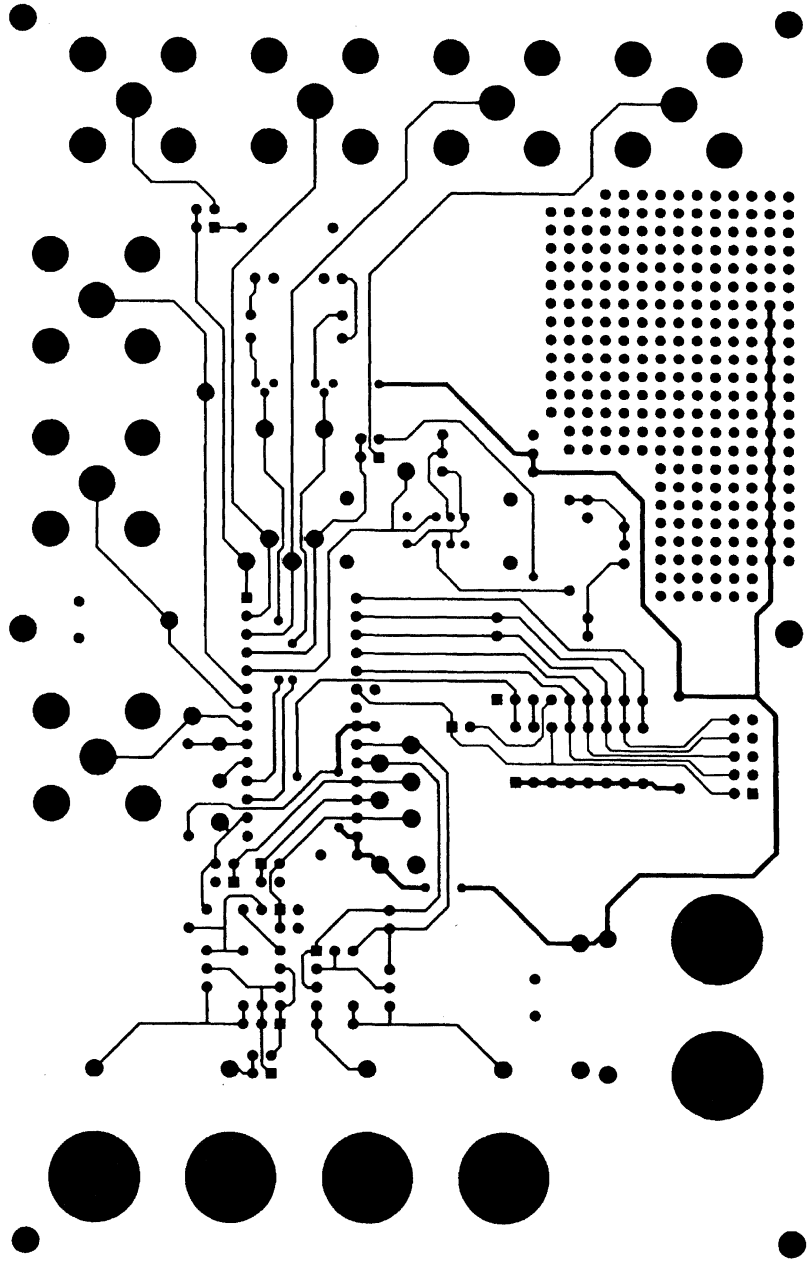


Figure 3. Bottom Trace Layer (NOT TO SCALE)

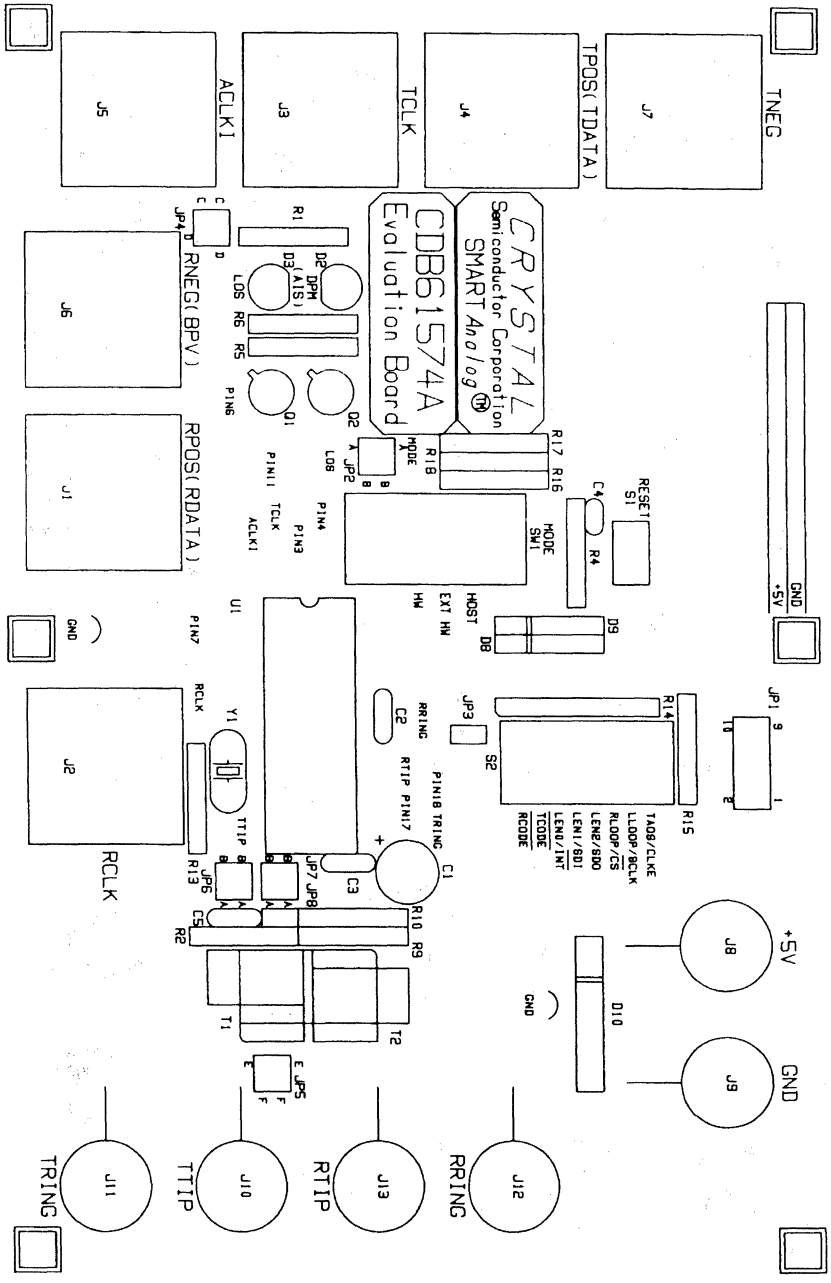


Figure 4. Silk Screen Layer (NOT TO SCALE)

CRYSTAL
A Cirrus Logic Company

CS61584

Dual Low Power T1/E1 Line Interface

Features

- Provides Dual Analog PCM Line Interface for short-haul, T1 and E1 applications
- 3.3 Volt and 5 Volt Versions
- Low Power Consumption (typically 160 mW per Line Interface)
- Operating mode fully software configurable; same external components can be used for all modes. No external quartz crystal is required.
- User-customizable pulse shapes
- Support of JTAG boundary scan

General Description

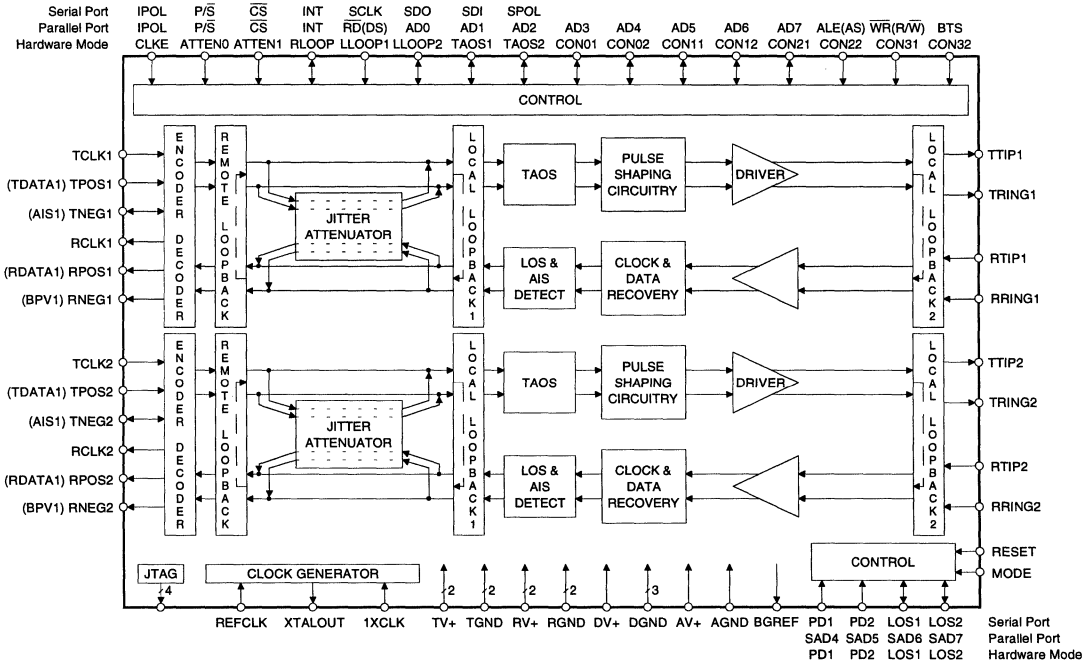
The CS61584 is a universal line interface for T1/E1 applications, designed for high-volume cards where low power, high density and universal operation is required. One board design can support all T1/E1 modes. Only the frequency of the reference clock input must change as software selects between T1 and E1.

The CS61584 is a low-power CMOS device available in 3.3 Volt and 5 Volt versions.

Transmitted pulse shapes are software-customizable, allowing non-standard line loads or protection circuits to be supported. Control is via either a serial port, parallel port or individual control lines.

ORDERING INFORMATION

CS61584-IQ3 3.3V, 64-pin TQFP, 10x10x1.4 mm
CS61584-IQ5 5V, 64-pin TQFP, 10x10x1.4 mm
CS61584-IL5 5V, 68-pin PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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Table of Contents

ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Min	Max	Units
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+)		(Note 1)		-	6.0	V
Input Voltage	Any Pin		V_{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current	Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature			T_A	-40	85	°C
Storage Temperature			T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Referenced to RGND1, RGND2, TGND1, TGND2, AGND, DGND at 0V.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter			Symbol	Min	Typ	Max	Units
DC Supply (TV+1, TV+2, RV+1, RV+2, AV+, DV+)		(Note 3)					
		-IQ3		3.135	3.3	3.465	V
		-IQ5		4.75	5.0	5.25	V
Ambient Operating Temperature			T_A	-40	25	85	°C
Power Consumption	T1	(Notes 4 and 5)	P_C	-	292	380	mW
(-IQ3, Each Channel)	T1	(Notes 4 and 6)		-	167	220	mW
	E1, 75Ω	(Notes 4 and 5)		-	193	250	mW
	E1, 120Ω	(Notes 4 and 5)		-	176	230	mW
REFCLK Frequency	T1	1XCLK = 1		1.544 - 100ppm	1.544	1.544 + 100ppm	MHz
	T1	1XCLK = 0		12.352 - 100ppm	12.352	12.352 + 100ppm	MHz
	E1	1XCLK = 1		2.048 - 100ppm	2.048	2.048 + 100ppm	MHz
	E1	1XCLK = 0		16.384 - 100ppm	16.384	16.384 + 100ppm	MHz

Notes: 3. TV+1, TV+2, AV+, DV+, RV+1, RV+2 should be connected together. TGND1, TGND2, RGND1, RGND2, DGND1, DGND2, DGND3 should be connected together.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 3.465V.
6. Assumes 50% ones density and 300ft. line length at 3.3V.

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 7)	V_{IH}	(DV+)-0.5	-	-	V
Low-Level Input Voltage	(Note 7)	V_{IL}	-	-	0.5	V
High-Level Output Voltage (Digital pins except parallel port)	(Note 8) I_{OUT} = -40 µA	V_{OH}	(DV+)-0.3	-	-	V
Low-Level Output Voltage (Digital pins except parallel port)	(Note 8) I_{OUT} = 1.6 mA	V_{OL}	-	-	0.3	V
Input Leakage Current (Digital pins except INT, J_TMS, and J_TDI)			-	-	±10	µA

Notes: 7. Digital inputs are designed for CMOS logic levels.
8. Digital outputs are TTL compatible and drive CMOS levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter			Min	Typ	Max	Units
Receiver						
RTIP/RRING Differential Input Impedance			-	20k	-	Ω
Sensitivity Below DSX-1 (0 dB = 2.4 V)			-13.6	-	-	dB
Loss of Signal Threshold, Short Haul			-	0.3	-	V
Data Decision Threshold	T1, DSX-1	(Note 9)	60	65	70	% of Peak
		(Note 10)	55	-	75	
	E1	(Note 11)	45	50	55	
		(Note 12)	40	-	60	
Allowable Consecutive Zeros before LOS			160	175	190	bits
Receiver Input Jitter Tolerance (DSX-1, E1)	10 Hz and below	(Note 13)	300	-	-	UI
	2 kHz		6.0	-	-	UI
	10 kHz - 100 kHz		0.4	-	-	UI
Jitter Attenuator						
Jitter Attenuation Curve Corner Frequency		(Notes 14 and 15)				
	T1		-	4	-	Hz
	E1		-	5.5	-	Hz
Attenuation at 10 kHz Jitter Frequency		(Notes 14 and 15)	-	60	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)		(Note 14)	28	43	-	UI_{pk-pk}

Notes: 9. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}
10. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk}, and 4.14 V_{pk} to 5.0 V_{pk}
11. For input amplitude of 1.07 V_{pk} to 4.14 V_{pk},
12. For input amplitude of 4.14 V_{pk} to 5.0 V_{pk},
13. Jitter tolerance increases at lower frequencies. See Figure 5.
14. Not production tested. Parameters guaranteed by design and characterization.
15. Attenuation measured with sinusoidal input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 12. Output jitter can increase significantly when more than 28 UI's are input to the attenuator. See discussion in Jitter Attenuator section.

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C; power supply pins within ±5% of nominal)

Parameter			Min	Typ	Max	Units
Transmitter						
AMI Output Pulse Amplitudes		(Note 16)				
	E1, 75Ω	(Note 17)	2.14	2.37	2.6	V
	E1, 120Ω	(Note 18)	2.7	3.0	3.3	V
	T1, DSX-1	(Note 19)	2.4	3.0	3.6	V
Recommended Transmitter Output Load (-IQ3)		(Note 16)				
	T1		-	25	-	Ω
	E1, 75Ω		-	18.75	-	Ω
	E1, 120Ω		-	30	-	Ω
Jitter Added During	10 Hz - 8 kHz		-	0.005	-	UI
Remote Loopback	8 kHz - 40 kHz		-	0.008	-	UI
	10 Hz - 40 kHz		-	0.010	-	UI
	Broad Band	(Note 20)	-	0.015	-	UI
Power in 2 kHz band about 772 kHz		(Notes 14 and 21) (DSX-1 only)	12.6	15	17.9	dBm
Power in 2 kHz band about 1.544 MHz (referenced to power in 2 kHz band at 772 kHz)		(Notes 14 and 21)) (DSX-1 only)	-29	-38	-	dB
Positive to Negative Pulse Imbalance		(Notes 14 and 21)				
	T1, DSX-1		-	0.2	0.5	dB
	E1, amplitude at center of pulse interval		-5	-	+5	%
	E1, width at 50% of nominal amplitude		-5	-	+5	%
Transmitter Return Loss		(Notes 14, 21, and 22)				
	51 kHz - 102 kHz		8	-	-	dB
	102 kHz - 2.048 MHz		14	-	-	dB
	2.048 MHz - 3.072 MHz		10	-	-	dB
E1 Short Circuit Current		(Note 23)	-	-	50	mA_{rms}
Arbitrary DSX-1	T1		-	45	-	mV/LSB
Pulse Amplitude	E1, Coaxial		-	26	-	mV/LSB
	E1, Shielded Twisted Pair		-	32	-	mV/LSB
E1 and DSX-1 Output Pulse Rise/Fall Times		(Note 24)	-	25	-	ns
E1 Pulse Width (at 50% of peak amplitude)			-	244	-	ns
E1 Pulse Amplitude	E1, 75Ω		-0.237	-	0.237	V
for a space	E1, 120Ω		-0.3	-	0.3	V

Notes: 16. Using a transformer that meets the specifications in Table 2.

17. Measured across 75 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/0.
18. Measured across 120 Ω at the output of the transmit transformer for CON3/2/1/0 = 0/0/0/1.
19. Measured at the DSX-1 Cross-Connect for line length settings CON3/2/1/0 = 0/0/1/0, 0/0/1/1, 0/1/0/0, 0/1/0/1, and 0/1/1/0 after the length of #22 ABAM cable specified in Table 1.
20. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
21. Typical performance with a 0.47 µF capacitor in series with primary of transmitter output transformer.
22. Return loss = 20 log $_{10}$ ABS($(z_1+z_0)/(z1-z_0)$) where z_1=impedance of the transmitter, and z_0=cable impedance.
23. Transformer secondaries shorted with 0.5 Ω resistor.
24. At transformer secondary. From 10% to 90% of amplitude.

SWITCHING CHARACTERISTICS - T1 CLOCK/DATA (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0V, Logic 1 = DV+) (See Figures 1, 2, and 3)

Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency		(Note 25)	f_{tclk}	-	1.544	8.192	MHz
TCLK Duty Cycle			t_{pwh2}/t_{pw2}	30	50	70	%
RCLK Duty Cycle		(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time	All Digital Outputs	(Note 27)	t_r	-	-	65	ns
Fall Time	All Digital Outputs	(Note 27)	t_f	-	-	65	ns
TPOS/TNEG to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time			t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time			t_{h1}	-	274	-	ns

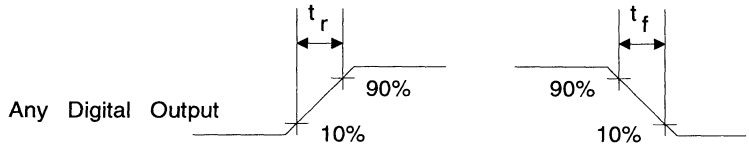
Notes: 25. Max value of 8.192 MHz describes the maximum burst rate of a gapped input clock (TCLK). For the gapped clock to be tolerated by the CS61584, the jitter attenuator must be switched to transmit path of the line interface. The maximum gap size is defined in the Analog Specification table.

26. RCLK duty cycle may be outside the spec limits when jitter attenuator is in the receive path, and when the jitter attenuator is employing the overflow/underflow protection mechanism.

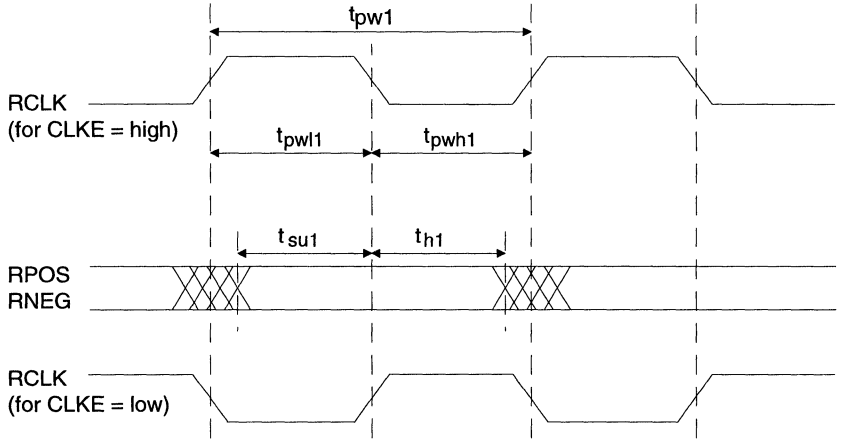
27. At max load of 50 pF.

SWITCHING CHARACTERISTICS - E1 CLOCK/DATA (T_A = -40 to 85 °C; power supply pins within ±5% of nominal; Inputs: Logic 0 = 0V, Logic 1 = DV+) (See Figures 1, 2, and 3)

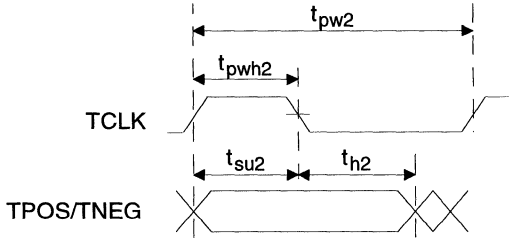
Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency		(Note 25)	f_{tclk}	-	2.048	8.192	MHz
TCLK Duty Cycle			t_{pwh2}/t_{pw2}	30	50	70	%
RCLK Duty Cycle		(Note 26)	t_{pwh1}/t_{pw1}	45	50	55	%
Rise Time	All Digital Outputs	(Note 27)	t_r	-	-	65	ns
Fall Time	All Digital Outputs	(Note 27)	t_f	-	-	65	ns
TPOS/TNEG to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time			t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time			t_{h1}	-	194	-	ns



Signal Rise and Fall Characteristics



Recovered Clock and Data Switching Characteristics

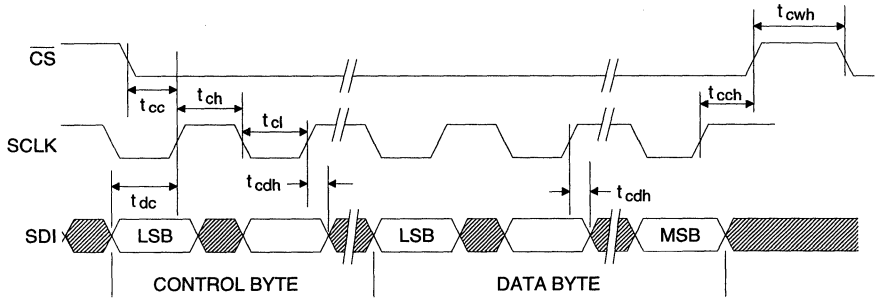


Transmit Clock and Data Switching Characteristics

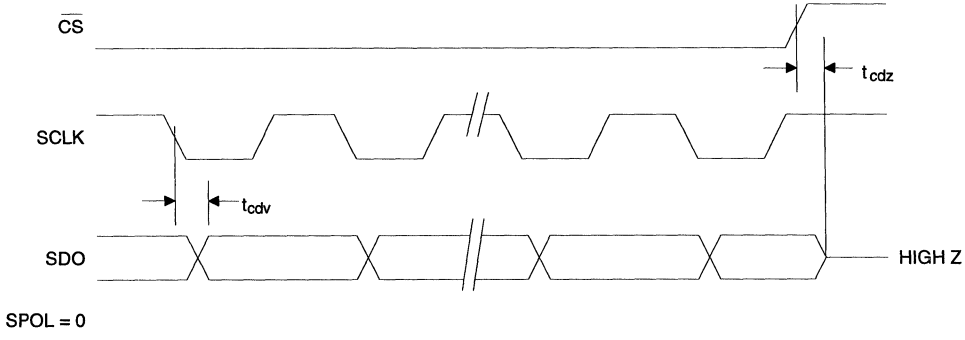
SWITCHING CHARACTERISTICS - SERIAL PORT (T_A = -40 to 85 °C;
DV+, TV+, RV+ = nominal ± 0.3V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	25	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	25	-	-	ns
SCLK Low Time	t_{cl}	50	-	-	ns
SCLK High Time	t_{ch}	50	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	15	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	20	-	-	ns
SCLK to $\overline{CS}$ Hold Time (Note 28)	t_{cch}	20	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	100	-	-	ns
SCLK to SDO Valid (Note 29)	t_{cdv}	-	-	50	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	50	-	ns

Notes: 28. If SPOL=0, then $\overline{CS}$ should return high no sooner than 20ns after the 16'th falling edge of SCLK during a serial port read.
29. Output load capacitance = 50 pF.



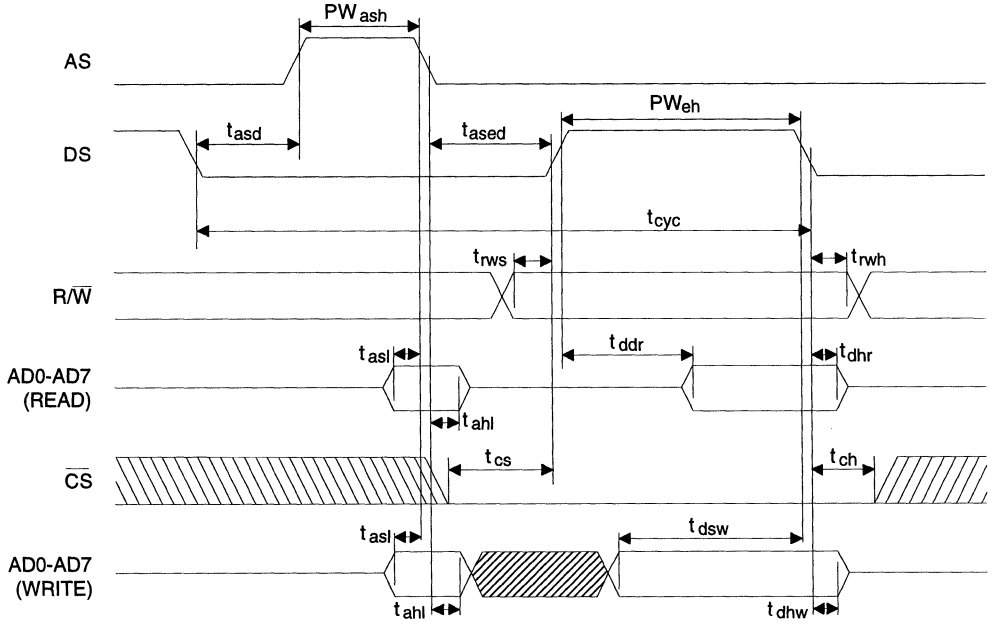
Serial Port Write Timing Diagram



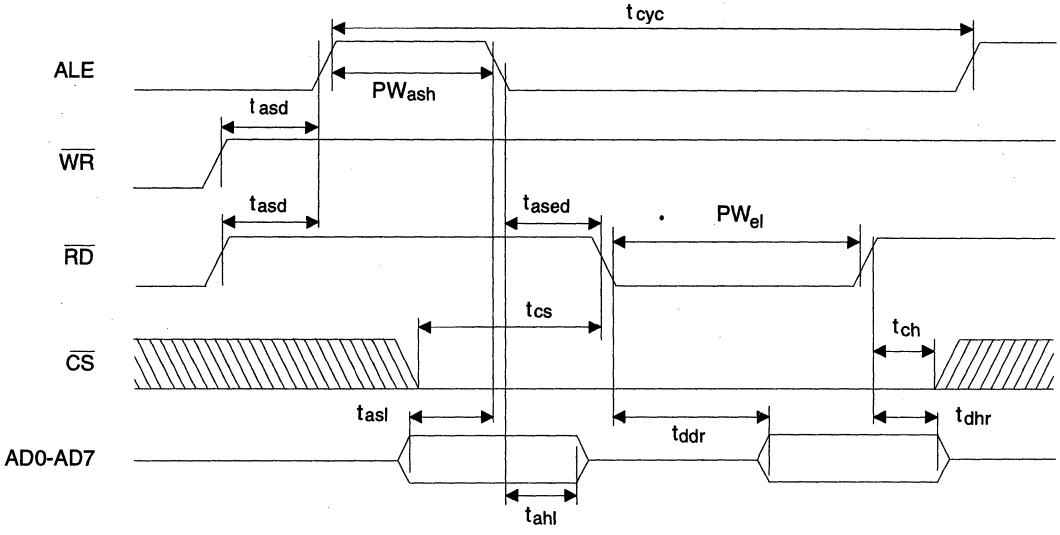
Serial Port Read Timing Diagram

SWITCHING CHARACTERISTICS - PARALLEL PORT (T_A = - 40 ° to 85 ° C;
TV+ ,RV+ = nominal ±0.3V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

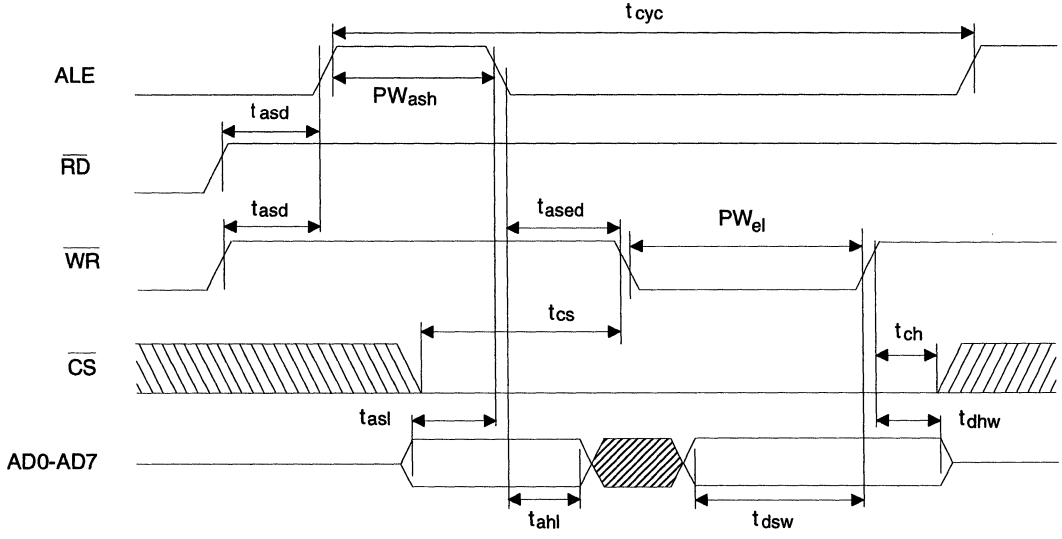
Parameter	Symbol	Min	Typ	Max	Units
Cycle Time	t_{cyc}	250	-	-	ns
Pulse Width, DS Low or $\overline{RD}$ High	PW_{el}	150	-	-	ns
Pulse Width, DS High or $\overline{RD}$ Low	PW_{eh}	150	-	-	ns
Input Rise/Fall Times	t_r, t_f	-	-	30	ns
R/$\overline{W}$ Hold Time	t_{rwh}	10	-	-	ns
R/$\overline{W}$ setup Time Before DS High	t_{rws}	50	-	-	ns
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$ or $\overline{RD}$ Active	t_{cs}	20	-	-	ns
$\overline{CS}$ Hold Time	t_{ch}	0	-	-	ns
Read Data Hold Time	t_{dhr}	10	-	80	ns
Write Data Hold Time	t_{dhw}	0	-	-	ns
Muxed Address Valid to AS or ALE Fall	t_{asl}	15	-	-	ns
Muxed Address Hold Time	t_{ahl}	10	-	-	ns
Delay Time DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{asd}	25	-	-	ns
Pulse Width AS or ALE High	PW_{ash}	40	-	-	ns
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ased}	20	-	-	ns
Output Data Delay Time from DS or $\overline{RD}$	t_{ddr}	20	-	120	ns
Data Setup Time	t_{dsw}	80	-	-	ns



Parallel Port Timing - Motorola Mode



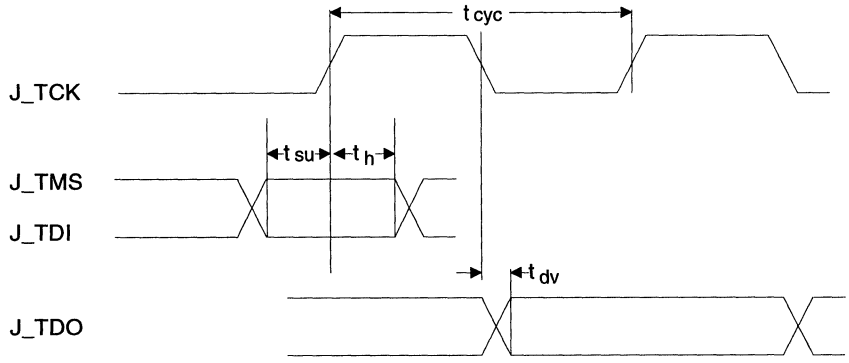
Parallel Port Timing - Intel Read Mode



Parallel Port Timing - Intel Write Mode

SWITCHING CHARACTERISTICS - JTAG (T_A = - 40 ° to 85 ° C;
TV+ ,RV+ = nominal ±0.3V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
Cycle Time	t_{cyc}	200	-	-	ns
J_TMS/J_TDI to J_TCK rising setup time	t_{su}	50	-	-	ns
J_CLK rising to J_TMS/J_TDI hold time	t_h	50	-	-	ns
J_TCLK falling to J_TDO valid	t_{dv}	-	-	50	ns



OVERVIEW

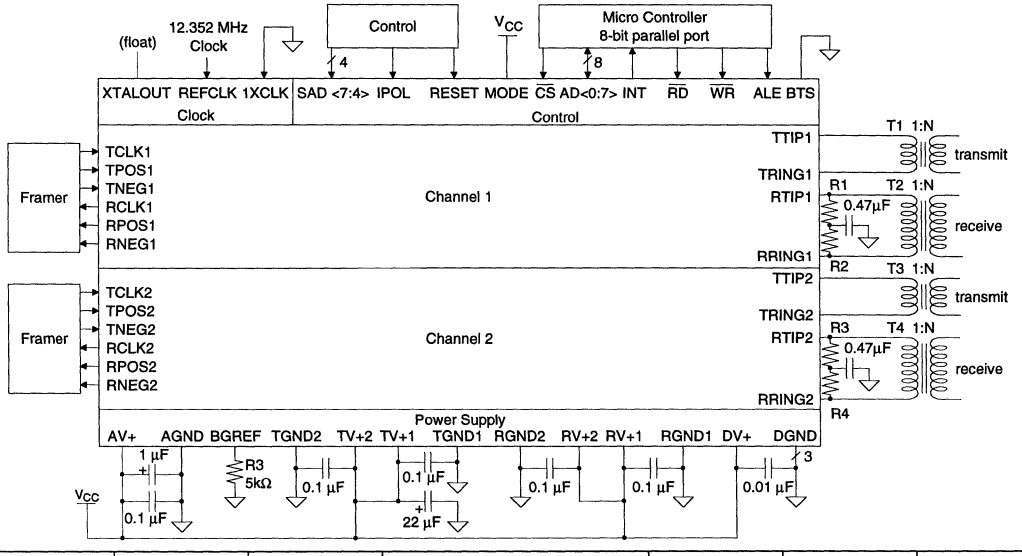
The CS61584 is a universal line interface for T1/E1 applications, designed for high-volume cards where low power, high density and universal operation is required. One board design can support all T1/E1 short-haul modes. The T1 and E1 modes can be selected entirely via software, without changing transformers or external oscillator (assuming REFCLK and TCLK are externally tied together).

As shown in Figure 1, the CS61584 provides all the functions needed for a line interface including a line driver, a receiver and jitter attenuator.

Under software control, the line driver generates waveforms compatible with E1 (CCITT G.703), T1 short haul (DSX-1) and T1 FCC Part 68 Option A (DS-1). A single transformer turns ratio is used for all waveform types. The driver internally matches the impedance of the load, providing excellent return loss. The benefit of the internal impedance matching is a 50 percent reduction in power consumption compared to implementing return loss with external resistors. With external resistors a driver has to drive the equivalent of two line loads.

The receiver contains clock and data recovery circuits.

The jitter attenuator meets AT&T 62411 requirements without the use of an external quartz crystal. The attenuator does require an external reference clock.



VCC Volts	Device Suffix	Data Rate MHz	REFCLK Frequency MHz		Cable Ω	R1 - R4 Ω	Transformers T1 - T4
			1XCLK = 1	1XCLK = 0			
3.3	-IQ3	1.544	1.544	12.352	100	12.5	1 : 2
		2.048	2.048	16.384	75	9.375	
					120	15	
5.0	-IQ5	1.544	1.544	12.352	100	37.5	1 : 1.15
		2.048	2.048	16.384	75	28.36	
					120	45.37	

Figure 1 - Typical Connection Diagram
(T1 Operation with Intel Parallel Host Mode)

OPERATING OPTIONS

The following are the major operating options which are supported by the CS61584:

Control

Control of the CS61584 is via either *host mode* (serial port, or 8-bit parallel port) or *hardware mode* (individual control lines). The parallel port is compatible with both Motorola and Intel 8-bit, multiplexed address/data buses. Hardware mode offers significantly fewer programability options than the serial and parallel port modes.

T1/E1

The CS61584 supports T1 short-haul (DSX-1), and E1 operation. Additionally, FCC Part 68 option A is supported (DS-1). The configuration pins (CON<0:3>) and register bits control transmitted pulse shapes, transmitter source impedance, and receiver slicing level. Both channels must be operated at the same rate (both T1 or both E1)

The pulse shapes are fully pre-defined by circuitry in the CS61584, and are fully compliant with appropriate standards when used with our application guidelines in standard installations. In addition, an option exists in host mode for the user to download into the CS61584 arbitrary waveforms, so that the board designer can compensate for the waveform degradation which can be caused by non-standard cables, transformers, or protection circuitry.

The transmitter impedance changes with the line length options in order to match the impedance of the load (75-Ω for E1 coax, 100-Ω for T1, 120-Ω for E1 Shielded twisted pair).

The receiver slicing level is set at 65% for DSX-1 short-haul, and at 50% for all other applications.

Line Codes

The CS61584 supports a *transparent mode* where the line code is encoded and decoded by an external T1/E1 framing device. Alternatively, in host mode, a *coder mode* can be selected. In coder mode, an internal B8ZS/AMI/HDB3 coder can be used on those systems which don't need T1/E1 framers (typically high-speed multiplexers). The choice of transmit encoder is independent of the choice of receiver decoder.

Reference Clock

The CS61584 requires a T1 or E1 reference clock. This clock can be either a 1-X clock (i.e., 1.544 MHz or 2.048 MHz), or can be a 8-X clock (i.e., 12.352 MHz or 16.384 MHz). In systems which want software selection of data rate, the 1-X clock option is typically chosen, and the reference clock is tied to the transmit clock. In systems with a jittered transmit clock, an external oscillator should drive the reference clock input, and a 8-X rate can be used to minimize the physical size of the oscillator. In either case, any jitter present on the reference clock will not be filtered by the jitter attenuator, and the reference clock should have 100 ppm or better frequency accuracy.

Power Down

Either one of the two line interfaces may be independently powered down.

Jitter Attenuator

The jitter attenuator may be placed in the receiver path, the transmit path or bypassed entirely.

OVERVIEW OF APPLICATIONS

This section summarizes a typical application of the CS61584 in various environments, and discusses what CS61584 options would normally be selected in that application. See Figure 2.

AT&T 62411 Customer Premises Application

AT&T 62411 applies at the T1 interface between the customer premises and the carrier, and must be implemented by the customer premises equipment.

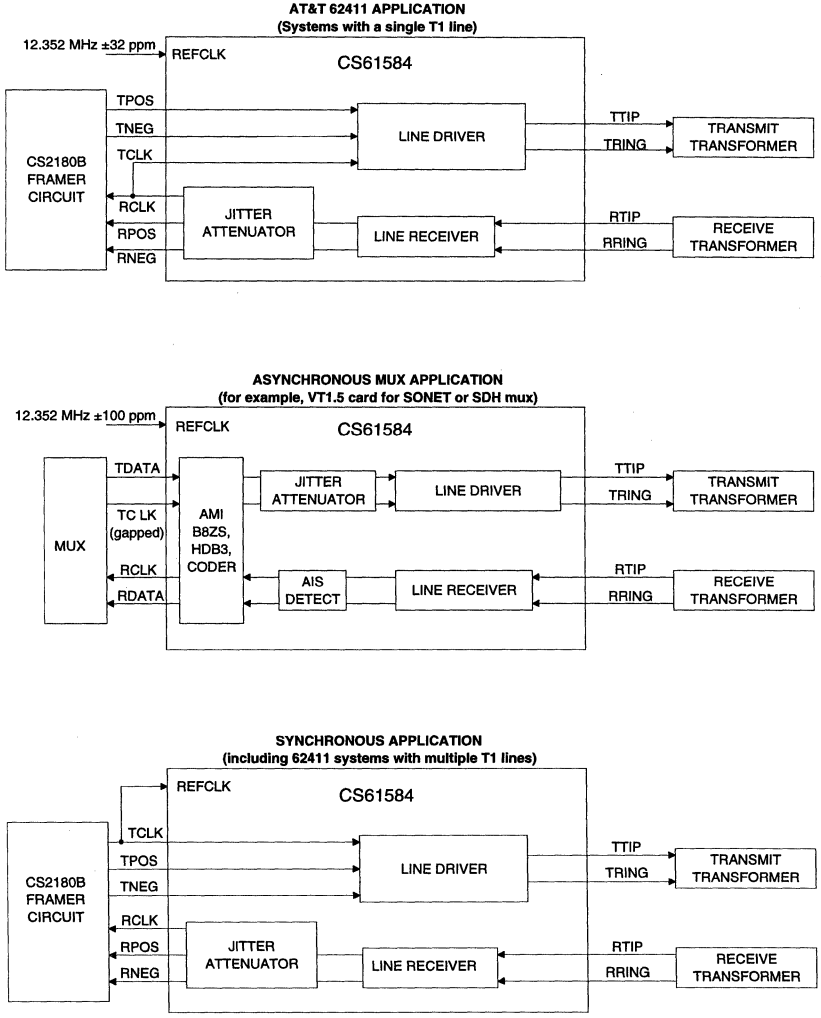


Figure 2. Configuration Examples for Various Applications

In 62411 applications, an overriding design consideration is management of jitter. Typically, the CS61584 will use it's jitter attenuator on the receive side to reduce the jitter seen by the system synchronizer. The transmit clock presented to the CS61584 by the system will be Stratum 4 quality or better, and is input to both the reference clock pin and transmit clock pin. If an independent clock source is used for the reference clock, the jitter on the reference clock must be well below the jitter allowed by 62411.

Category I Asynchronous Multiplexer Application

Asynchronous multiplexers take multiple T1/E1 lines (which are asynchronous to each other), and combine them into a higher speed transmission rate. Examples are M13 muxes, and SONET muxes. In these systems, the jitter attenuator is used on the transmit side of the CS61584 to remove the waiting time jitter caused by the multiplexer. Because the transmit clock is jittered, the reference clock to the CS61584 will be provided by an external quartz crystal, which operates at the 8-X data rate. T1/E1 framers are typically not required in asynchronous multiplexers, so the B8ZS/AMI/HDB3 coders in the CS61584 are activated.

Category II Synchronous Application

A typical example of a category II application is a T1 card of a central office switch or a 0/1 digital cross-connect system. These systems use receive side jitter attenuation to reduce the jitter presented to the system, and will use a Stratum 3 or better system clock to feed the CS61584 transmit and reference clocks. In these systems, a single hardware design can support T1 and/or E1 under software control since the rate of the transmit/reference clock rate will be varied by the system to match the line rate (T1 or E1).

TRANSMITTER

The transmitter takes data from a T1 or E1 terminal, and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG, or TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

3

Pulse shaping and signal level are determined by configuration inputs as shown in Table 1. Typical output pulses are shown in Figures 3 and 4. Note that the optimal pulse width for Part 68 Option A (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61584 automatically adjusts the pulse width based upon the configuration selection made. Arbitrary pulse shapes can also be created in host mode (see Control and Status Register section).

The line driver internally matches the impedance of the line load, providing 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Internal impedance matching reduces current consumption by a factor of nearly two compared to return loss achieved by external resistors.

The CS61584 driver will detect an inactive input clock (i.e., if no valid data is being clocked into the driver). Once this condition is detected, the driver prevents TTIP and TRING from getting stuck in a transmit-mark state.

The transmitter provides for all ones insertion at the frequency of REFCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG, or TDATA, inputs are ignored.

When any transmit control pin (TAOS, LLOOP, or CON<0-3>) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected

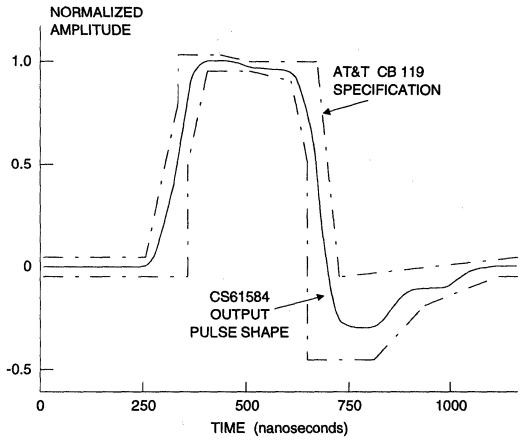


Figure 3. Typical Pulse Shape at DSX-1 Cross Connect

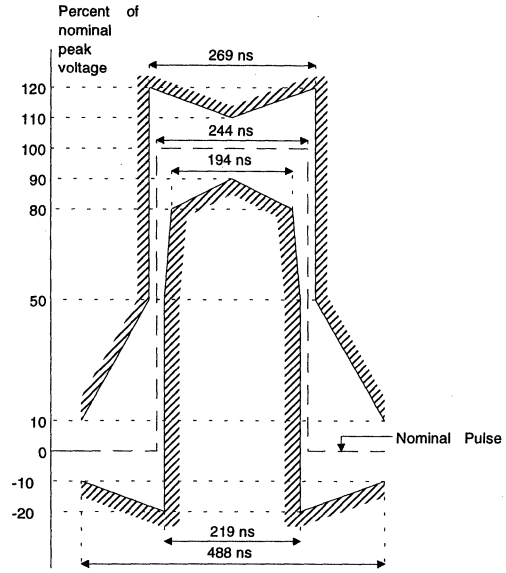


Figure 4. Mask of the Pulse at the 2048 kbps Interface

CON3	CON2	CON1	CON0	TRANSMITTER Pulse width at 50% amplitude	Pulse Shape	RECEIVER Slicing Level	Coder
0	0	0	0	244 ns (50%)	E1: square, 2.37 Volts into 75 Ω	50%	AMI/HDB3
1	0	0	0	244 ns (50%)	Arbitrary "E1" Wave into 75 Ω	50%	AMI/HDB3
0	0	0	1	244 ns (50%)	E1: square, 3.00 Volts into 120 Ω	50%	AMI/HDB3
1	0	0	1	244 ns (50%)	Arbitrary "E1" Wave into 120 Ω	50%	AMI/HDB3
0	0	1	0	350 ns (54%)	DSX-1: 0-133 ft.	65%	AMI/B8ZS
0	0	1	1	350 ns (54%)	DSX-1: 133-266 ft.	65%	AMI/B8ZS
0	1	0	0	350 ns (54%)	DSX-1: 266-399 ft.	65%	AMI/B8ZS
0	1	0	1	350 ns (54%)	DSX-1: 399-533 ft.	65%	AMI/B8ZS
0	1	1	0	350 ns (54%)	DSX-1: 533-655 ft.	65%	AMI/B8ZS
1	0	1	0	350 ns (54%)	Arbitrary "DSX-1" Waveform	65%	AMI/B8ZS
0	1	1	1	324 ns (50%)	DS1: FCC Part 68 Option A with undershoot	65%	AMI/B8ZS
1	1	0	0	324 ns (50%)	DS1: FCC Part 68 Option A, (0 dB)	65%	AMI/B8ZS
1	1	0	1	Reserved			
1	1	1	0	Reserved			
1	1	1	1	Reserved			
1	0	1	1	324 ns (50%)	Arbitrary "DS-1" Waveform	65%	AMI/B8ZS

Table 1. Configuration Selection

because the timing circuitry must adjust to the new frequency.

Recommended transmitter transformer specifications are shown below:

Turns ratio - IQ3	 1:2 step-up for transmit 1:2 step-down for receive
-IQ5	1:1.15 step-up for transmit 1:1.15 step-down for receive
Primary inductance	1.5 mH min measured at 772 kHz
Primary leakage inductance	0.3 µH max at 772 kHz with secondary shorted
Secondary leakage inductance	0.4 µH max at 772 kHz
Interwinding capacitance	18 pF max, primary to secondary
ET-constant	16 V-µs min

Table 2. Transformer Requirements

When the transmitter transformer secondaries are shorted via a 0.5 Ω resistor, the transmitter will output a maximum of 50 mA-rms, as required by the British OFTEL OTR-0001 specification.

RECEIVER

The receiver extracts data and clock from the T1/E1 signal and outputs clock and synchronized data. The receiver can receive signals over the entire range of short haul cable lengths.

The clock recovery circuit is a second-order phase lock loop, and can tolerate as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error (Figure 5). The clock and data recovery circuit is tolerant of long strings of consecutive zeros, and will successfully receive a 1-in-175, jitter-free input signal.

Data at RPOS and RNEG, is stable and may be sampled using the recovered clock. CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3. When CLKE is high, RPOS and RNEG are valid on the falling edge of RCLK. When CLKE is low, RPOS and RNEG are valid on the rising edge of RCLK. In Hardware mode, the CLKE selection is made via pin 33. In host mode, the CLKE selection is made via control register (Channel 1 Control A, bit 7).

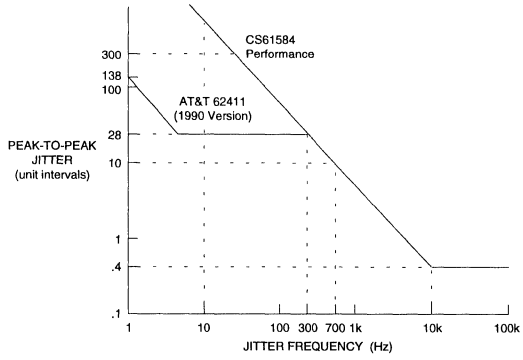


Figure 5. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

CLKE	DATA	CLOCK	Clock edge for valid data
LOW	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH	RPOS RNEG	RCLK RCLK	Falling Falling

Table 3. Data Output/Data Relationship

The signal is detected differentially across the receive transformer. Recommended receiver transformer specifications are identical to the transmit transfomer specifications.

Receiver Loss of Signal

The receiver will indicate loss of signal upon receiving 175±15 consecutive zeros. A digital counter counts received zeros, based on recov-

ered clock cycles. The receiver reports loss of signal by setting the appropriate Loss of Signal pin, LOS, high. The LOS condition is exited using the ANSI T1.231-1993 criteria, namely 12.5% ones density for 175±75 bit periods with no more than 100 zeros in a row.

If a loss of signal condition occurs when the host mode is being used, the LOS and LOS-latched bits will be set and an interrupt will be issued. LOS will go low (and flag the interrupt pin again, if the serial or parallel I/O is used) when a valid signal is detected. The LOS-latched bit will stay high until read, and then will remain low until the next loss of signal event occurs. See Figure 6. Note that in the hosts mode, LOS is simultaneously available from both the register and pin LOSx.

When the jitter attenuator is in the receive path, upon loss of signal, the frequency of the last recovered signal is held over. When the jitter attenuator is not in the receive path, the last recovered frequency is not held over. Rather, the output frequency will become the frequency of the reference clock.

Any time a channel is reset or powered down, (for example by RESET, PD1, PD2 or power-on reset), the loss of signal indicator on that channel is set high. The loss of signal indicator remains high until data is recovered by the receiver.

Receiver AIS Detection

The receiver detects AIS upon observation of 99.9% ones density for 5.3 ms. More specifically, the AIS detection criteria is less than 9 zeros out of 8192 bits. When AIS is detected, the CS61584 sets the control register bits AIS and Latched-AIS, high. In the coder mode, the receiver also sets output pin AIS high. The end of the AIS condition occurs when ≥9 zeros are detected out of 8192 bits. The AIS bits in the status register operate the same as the LOS bits (see Table 6) upon detecting AIS. When a channel is powered down, all AIS indications are forced low.

JITTER ATTENUATOR

The jitter attenuator can be switched into either the receive or transmit paths. Alternatively it can be removed from both paths (thereby decreasing propagation delay).

Atten0x	Atten1x	Location of Jitter Attenuator
0	0	Receiver
0	1	Transmitter
1	0	Neither
1	1	Reserved

Table 4. Jitter Attenuation Control

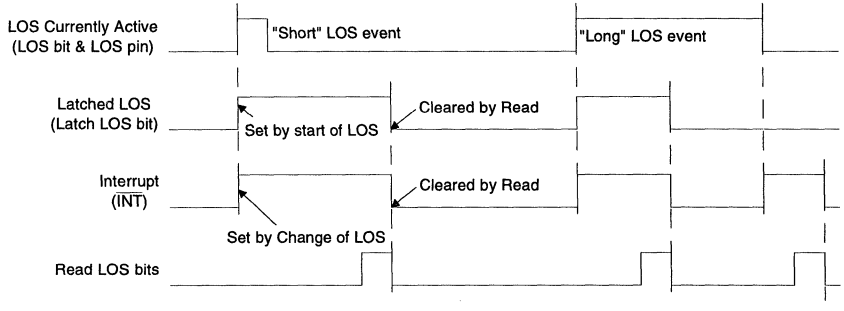


Figure 6. Loss of Signal Event Relationships

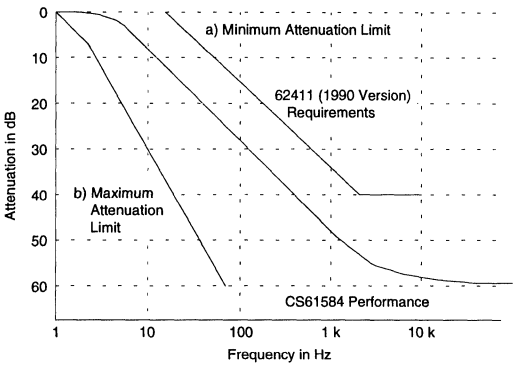


Figure 7. Typical Jitter Transfer Function

In hardware mode, the location of the attenuators is the same for channels 1 and 2, and is controlled by pins ATTEN0 and ATTEN1. See Table 4. In host modes, the location of the attenuators is programmable on a per-channel basis, using bits ATTEN01 and ATTEN11 for channel 1, and bits ATTEN02 and ATTEN12 for channel 2. The control bits also conform to Table 4.

A typical jitter attenuation curve is shown in Figure 7.

The attenuator consists of a 64-bit FIFO, a narrow-band monolithic PLL, and control logic. Signal jitter is absorbed in the FIFO. The FIFO is designed to neither overflow nor underflow. If overflow or underflow is imminent, the jitter transfer function is altered to insure that no bit-errors occur. Under this circumstance, jitter gain may occur, and jitter should be attenuated externally in a frame buffer. The jitter attenuator will typically tolerate 43 UIs before the overflow/underflow mechanism takes effect. Before the jitter attenuator has had time to "lock" to the average incoming frequency, for example, after a chip reset, the attenuator will tolerate a minimum of 22 UIs before the overflow/underflow mechanism takes effect.

For T1/E1 line cards employed in high-speed mutiplexers (e.g., SONET and SDH), the jitter attenuator is typically used in the transmit path. The attenuator can be fed a gapped transmit clock, with gaps ≤ 22 UIs, and transmit clock burst rate ≤ 8 MHz.

CODER MODE

In the coder Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using control register bits CODER (1 = coder active, 0 = transparent mode, coder disabled) and AMI-T/AMI-R(1 = AMI, 0 = B8ZS or HDB3) where the transmitter and receiver can be independently controlled. The selection of B8ZS versus HDB3 is made by the control bits: CON<0:3>.

In the coder mode, the receiver sets output pins AIS1 and AIS2 high, when AIS is detected, respectively on channels 1 and 2.

In the coder mode, pin BPV goes to a logic 1 for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled. A latched-BPV indication is also available in the status register.

REFERENCE CLOCK

The CS61584 requires a T1 or E1 reference clock. This clock is input on pin REFCLK, and can be either a 1-X clock (i.e., 1.544 MHz or 2.048 MHz), or a 8-X clock (i.e., 12.352 MHz or 16.384 MHz). Pin 1XCLK determines which option is used (active high for 1-X, and low for 8-X).

Any jitter present on the reference clock will not be filtered by the jitter attenuator, and will be present on the output of the jitter attenuator. The reference clock should have a minimum accuracy of 100 ppm.

If a reference clock signal is not available, a quartz crystal can be connected across pin REFCLK and XTALOUT. When a quartz crystal is used, the 8-X clock rate crystal must be used.

The crystal should be AT-cut and fundamental mode. Specifications are given below:

Parameter	Min	Typ	Max	Unit
T1 Parallel resonant frequency	-	12.352	-	MHz
E1 Parallel resonant frequency	-	16.384	-	MHz
Resonant frequency error (for CL=20 pF, and 25°C)	-50	-	+50	ppm
Temperature drift (over required temperature range)	-100	-	+100	ppm
Drive level	-	-	2	mW
Series resistance	-	-	50	Ohms
Aging	-5	-	+5	ppm/year

Table 5. Quartz Crystal Requirements

LOOPBACKS

Local Loopbacks

The two local loopbacks take clock and data presented on TCLK, TPOS, and TNEG, or TDATA and outputs it at RCLK, RPOS and RNEG, or RDATA. As shown in the block diagram on the first page of the data sheet, loopback 1 includes the jitter attenuator. Loopback 2 includes the line driver and the receiver.

For both local loopbacks, inputs to the transmitter are still transmitted on the line, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted to the line at the rate determined by TCLK. Receiver inputs are ignored when local loopback is in effect. Local loopback 1 is selected by a control pin, or a control bit. Loopback 2 is selected only via a control bit.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING as shown in the block diagram on the front page of this data sheet. The recovered incoming signals are also sent to RCLK, RPOS and RNEG, or RDATA. A remote loopback may be selected in both the hardware and host modes. However, in hardware mode, the RLOOP pin controls operation of the remote loopback in both channels (i.e., either both channels are looped back, or neither channel is looped back). Simultaneous selection of local and remote loopback modes is not valid.

POWER DOWN

The PD1 and PD2 pins reset, respectively, the transmitter, receiver and jitter attenuator of channels 1 and 2. Whenever PD1 or PD2 is selected, the selected channel remains powered down, and the outputs (pins RCLK, RPOS, RNEG, RDATA, BPV, AIS, TTIP and TRING) associated with that channel are put into a high-impedance state, and pin LOS is set high. Additionally, the status register bits are reset. The control, mask, and arbitrary waveform registers are unchanged. The non-selected channel operates normally. Selecting PD1 or PD2 does not reset the CS61584 control registers, or parallel or serial control ports. Simultaneously selecting PD1 and PD2 will power down some additional analog circuitry that is shared by both channels. After exiting the power down state, the channel will be fully operational in less than 20 ms.

RESET

In operation, the CS61584 is continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation.

The RESET pin resets the entire device, including the control logic, and clears all control and mask registers. A reset event results in the Latched-reset bit being set in the Status register. A reset request can be made by setting RESET high for at least 200 ns. Reset will initiate on the falling edge of RESET. The reset operation takes less than 20 ms to complete. Upon exiting RESET, both channels are powered up.

POWER ON RESET

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 60% of the power supply voltage. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the transmit and receive sections commences. The calibration can take place only if REFCLK and TCLK are present. The initial calibration takes less than 20 ms. The power-on reset has the same effect as the RESET. A power-on reset event results in the Latched-reset bit being set in the Status register.

CONTROL

Control of the CS61584 is via either host mode (register read/write via serial control port or parallel control port), or hardware mode (individual control pin). The parallel port is compatible with both Motorola and Intel 8-bit, multiplexed address/data buses. Hardware mode offers significantly fewer programability options than the serial and parallel port modes.

The following pins are used to select the mode. The MODE pin active low selects Hardware mode. The MODE pin active high enables host mode. Once host mode is invoked, the P/$\overline{S}$ pin selects parallel-port (logic high) or serial-port (logic low). The definition of the pins in each mode is shown in the block diagram of the first page of the data sheet.

3

Hardware Mode

The following control options are available in Hardware mode on a per channel basis: power down, remote loopback, local loopback #1, transmit all ones, line length selection and location of jitter attenuator.

Host Modes

Host mode allows a microcontroller to read/write ten CS61584 control and status registers. The registers are defined in Table 6, and discussed in a later section. Two host mode interface ports are available, serial and parallel.

In serial port operation, the CS61584 registers occupies a six-bit address space, where those six bits select a register in the range h10 to h19.

In parallel operation, the CS61584 registers occupies an eight-bit address space where the four most significant bits can select one of 16 CS61584s on a board, and the four least significant bits select one of ten registers in that IC. The IC address is set for each CS61584 by hardwiring pins SAD7, SAD6, SAD5 and SAD4 to ground or power supply, as appropriate. This architecture allows up to 16 CS61584 devices to share the same chip select signal and parallel bus.

The CS61584 generates an interrupt on pin INT whenever a status register changes. The polarity

of the INT pin is programmable. When the IPOL pin is high, INT goes high to generate a processor interrupt. When the IPOL pin is low, INT goes low to generate a processor interrupt.

REGISTERS

The control and status registers are defined in Table 6, and are accessible in host mode. Each channel has its own set of Status, Mask, Control and Arbitrary Waveform registers. The status register is read-only. Writing to the status register has no impact on its contents. Interrupts are generated on the INT pin every time a status register changes. Reading a status register resets all bits in that status register to 0. The mask register allows the user to mask interrupts on a status register on a per-bit basis. The control registers select features/functionality. The Arbitrary Waveform register is written to multiple times in succession to define a custom waveform. See a later section for a description of how to use this register.

Parallel Register Address	Serial Register Address	bit	Name	Definition 1	Definition 0	Reset Value
h0 b0000	h10 b010000		Channel 1 Status			
		7	LOS1	LOS currently detected	no LOS	1
		6	Latched-LOS1	LOS event since last read	no LOS	1
		5	AIS1	AIS currently detected	no AIS	0
		4	Latched-AIS1	AIS event since last read	no AIS	0
		3	Latched-BPV1	BPV event since last read	no BPV	0
		2	Latched-Overflow1	Pulse overflow since last read	no overflow	0
		1	Latched-reset	Reset event since last read	no reset	1
		0	Interrupt1	Interrupt event since last read	no interrupt	0
h1 b0001	h11 b010001		Channel 2 Status			
		7	LOS2	LOS currently detected	no LOS	1
		6	Latched-LOS2	LOS event since last read	no LOS	1
		5	AIS2	AIS currently detected	no AIS	0
		4	Latched-AIS2	AIS event since last read	no AIS	0
		3	Latched-BPV2	BPV event since last read	no BPV	0
		2	Latched-Overflow2	Pulse overflow since last read	no overflow	0
		1	reserved			0
		0	Interrupt2	Interrupt event since last read	no interrupt	0

Table 6(a). Status Registers

Parallel Register Address	Serial Register Address	bit	Name	Definition		Reset Value
				1	0	
h2 b0010	h12 b010010		Channel 1 Mask			
		7	Mask LOS1	Mask status bit 7	enable status bit 7	0
		6	Mask Latched LOS1	Mask status bit 6	enable status bit 6	0
		5	Mask AIS1	Mask status bit 5	enable status bit 5	0
		4	Mask Latched-AIS1	Mask status bit 4	enable status bit 4	0
		3	Mask Latched-BPV1	Mask status bit 3	enable status bit 3	0
		2	Mask Latch-Ovrflw1	Mask status bit 2	enable status bit 2	0
		1	reserved			0
		0	Mask Interrupt1	Mask status bit 0 & interrupt pin	enable status bit 0 & interrupt pin	0
h3 b0011	h13 b010011		Channel 2 Mask			
		7	Mask LOS2	Mask status bit 7	enable status bit 7	0
		6	Mask Latched-LOS2	Mask status bit 6	enable status bit 6	0
		5	Mask AIS2	Mask status bit 5	enable status bit 5	0
		4	Mask Latched-AIS2	Mask status bit 4	enable status bit 4	0
		3	Mask Latched-BPV2	Mask status bit 3	enable status bit 3	0
		2	Mask Latch-Ovrflw2	Mask status bit 2	enable status bit 2	0
		1	reserved			0
		0	Mask interrupt2	Mask status bit0 & interrupt pin	enable status bit 0 & interrupt pin	0

Table 6(b). Mask Registers

Status Registers Description

Each bit in the status register is defined below.

AIS and Latched-AIS: Indicates an all-ones condition. AIS is set high while AIS condition is currently detected. Latched-AIS indicates that a AIS condition has occurred since the last read of the status register.

Interrupt: Indicates that the status register has changed sometime since the last read of the status register.

Latched-BPV: Indicates a bipolar violation event has been detected in the receiver sometime since the last read of the status register. This bit is set only when the line-code decoder is enabled.

Latched-Overflow: Indicates that a waveform generated using the Arbitrary Waveforms has exceeded full scale sometime since the last read of the status register.

LOS and Latched-LOS: Indicates loss of signal condition. LOS is set high while LOS condition is currently detected. Latched-LOS indicates that

Parallel Register Address	Serial Register Address	bit	Name	Definition 1	Definition 0	Reset Value
h4 b0100	h14 b010100		Channel 1 Control A			
		7	CLKE	RPOS/RNEG valid on falling RCLK	RPOS/RNEG valid on rising RCLK	0
		6	PD1	Power Down Channel 1	Power up Channel 1	0
		5	ATTEN01	ATTEN01 ATTEN11		0
		4	ATTEN11	0 0 0 1 1 0	Attenuator 1 in receiver path Attenuator 1 in transmit path Attenuator 1 inactive	0
		3	CODER1	Coder/Mode enabled	Transparent mode enabled	0
		2	AMI-T1	AMI encoder enabled	B8ZS/HDB3 encoder enabled	0
		1	AMI-R1	AMI decoder enabled	B8ZS/HDB3 decoder enabled	0
		0	Factory Test 1	Test	Normal operation	0
h5 b0101	h15 b010101		Channel 2 Control A			
		7	Reserved	Must be set to 0		0
		6	PD2	Power Down Channel 2	Power Up Channel 2	0
		5	ATTEN02	ATTEN02 ATTEN12		0
		4	ATTEN12	0 0 0 1 1 0	Attenuator 2 in receiver path Attenuator 2 in transmit path Attenuator 2 inactive	0
		3	CODER2	Coder/Mode enabled	Transparent mode enabled	0
		2	AMI-T2	AMI encoder enabled	B8ZS/HDB3 encoder enabled	0
		1	AMI-R2	AMI decoder enabled	B8ZS/HDB3 decoder enabled	0
		0	Factory Test	Test	Normal Operation	0

Table 6(c). Control A Registers

a LOS condition has occurred since the last read of the status register.

Latched-reset: Indicates that a reset event (power-up or manual) has occurred since the last read of the status register. This status bit is not maskable.

Mask Registers Description

Writing a "1" to a bit of the mask register forces the corresponding bit of the status register to stay fixed at "0".

Control A Registers Description

Each bit in the control register is defined below.

AMI-R: Writing a "0" enables the B8ZS or HDB3 decoder in the receive path. B8ZS vs. HDB3 selection is determined by the CON<0:3> bits. Writing a "1" enables the AMI decoder.

AMI-T: Writing a "0" enables the B8ZS or HDB3 encoder in the transmit path. B8ZS vs. HDB3 selection is determined by the CON<0:3> bits. Writing a "1" enables the AMI encoder.

ATTEN0 and ATTEN1: Controls the location of the jitter attenuator, as defined in Table 4.

CLKE: When CLKE is set to "1", RPOS and RNEG are valid on the falling edge of RCLK. When CLKE is set to "0", RPOS and RNEG are valid on the rising edge of RCLK. This bit controls the RPOS/RNEG polarity for both host

Parallel Register Address	Serial Register Address	bit	Name	Definition 1	Definition 0	Reset Value
h6 b0110	h16 b010110		Channel 1 Control B			
		7	TAOS1	enable transmit all ones	disable transmit all ones	0
		6	RLOOP1	enable remote loopback	disable remote loopback	0
		5	LLOOP11	enable local loopback #1	disable loopback # 1	0
		4	LLOOP21	enable local loopback #2	disable loopback # 2	0
		3	CON31	See Table 1		0
		2	CON21	See Table 1		0
		1	CON11	See Table 1		0
		0	CON01	See Table 1		0
h7 b0111	h17 b010111		Channel 2 Control B			
		7	TAOS2	enable transmit all ones	disable transmit all ones	0
		6	RLOOP2	enable remote loopback	disable remote loopback	0
		5	LLOOP12	enable local loopback #1	disable loopback # 1	0
		4	LLOOP22	enable local loopback #2	disable loopback # 2	0
		3	CON32	See Table 1		0
		2	CON22	See Table 1		0
		1	CON12	See Table 1		0
		0	CON02	See Table 1		0

Table 6(c). Control B Registers

modes. The CLKE pin provides the same functionality for the hardware mode.

CODER: Writing a "1" enables a coder (AMI, B8ZS or HDB3), and enables pins TDATA, RDATA, AIS and BPV. Writing a "0" disables the coder, placing the channel in transparent mode, and enables pins TPOS, TNEG, RPOS and RNEG.

Factory Test: Must be set to "0" for normal operation.

PD: Writing a "1" powers down the channel.

Control B Registers Description

Each bit in the control register is defined below.

CON<0:3>: Controls the configuration of the transmitter, receiver and coder as shown in Table 1. Both channels must operate at the same rate (both T1 or both E1). Specifications are not guaranteed with the channels operating at different rates. After a manual or power-on reset, the CON bits are reset to the E1 rate. If a single channel T1 mode is desired (i.e., second channel is not used), it is recommended that both channels be set to the T1 rate.

LLOOP1: Writing a "1" enables local loopback #1, as shown in the block diagram on the front page of the data sheet.

LLOOP2: Writing a "1" enables local loopback #2, as shown in the block diagram on the front page of the data sheet.

RLOOP: Writing a "1" enables remote loopback for this channel.

TAOS: Writing a "1" enables transmit all ones.

Parallel Register Address	Serial Register Address	bit	Name	Definition	Reset Value
h8 b1000	h18 b011000		Channel 1 Arbitrary Pulse Shape		
		7	MSB	See Section on Arbitrary	undefined
		6		Waveform Generation	undefined
		5			undefined
		4			undefined
		3			undefined
		2			undefined
		1			undefined
		0	LSB		undefined
h9 b1001	h19 b011001		Channel 2 Arbitrary Pulse Shape		
		7	MSB	See section on Arbitrary	undefined
		6		Waveform Generation	undefined
		5			undefined
		4			undefined
		3			undefined
		2			undefined
		1			undefined
		0	LSB		undefined

Table 6(e). Arbitrary Waveform Registers

Arbitrary Waveform Registers

These registers are written multiple times to enter an arbitrary waveform. See discussion in later section.

HOST-MODE REGISTER ACCESS

The serial-port and parallel-port have different procedures for register access.

Host-Mode Serial-Port Operation

This mode is selected by setting pin MODE to logic high, and pin P/$\overline{S}$ to logic low. In the serial-port host mode, the on-board registers can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through these registers, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Any read or write to the serial port is initiated by by setting Chip Select ($\overline{CS}$) low and writing an 8-bit address/command byte (ACB). The ACB consists of three separate fields including a 6-bit register address (see Figure 8). The ACB is followed by a data word.

In the ACB, D0 (LSB) is the R/$\overline{W}$ field, and specifies whether the current operation is to be a read or a write: 1 = read, 0 = write. The next 5 bits (D1 - D5) contain the address field. They specify which of the registers to access. D6 is reserved, and must be set to 0 for normal operation. Setting bit D7 to 1 selects burst mode (described below).

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BM	**ADD5**	**ADD4**	**ADD3**	**ADD2**	**ADD1**	**ADD0**	**R/W**
0 Individual 1 Burst	(MSB)	Register Address Field				(LSB)	0 Write 1 Read

Figure 8. Address Command Byte (ACB)

Registers h10 to h17 are read and written as described above. Registers h18 and h19 are used to access multiple bytes of the CS61584's Arbitrary Waveform RAM, and use additional addressing. Reading or writing arbitrary waveform data requires two consecutive address bytes per data bytes. The first address byte is an ACB as shown in Figure 8, and contains register address of either h18 or h19. The second address byte is an eight bit, unsigned binary number, which identifies one of 42 RAM byte locations (numbered h00 to h29). Register h18 allows access to one bank of 42 bytes; register h19 allows access to a second bank of 42 bytes. When communicating over the port, the third byte, which follows the ACB, and RAM address, is the data byte.

Another communication option, burst mode, is available. Burst mode is specified by setting bit D7 (MSB) of the ACB to 1. Burst mode allows multiple registers to be consecutively read or written. Writing all registers allows fast initialization at power-up or system reset. When using burst mode, the address field of the ACB command word must be h00. The registers are read or written in address order h10 to h11, followed by 42 byte reads or writes to register h18, followed by 42 bytes reads or writes to register h19. Burst mode ends on the first rising edge of $\overline{CS}$, and may be ended at any time. If a burst write ends before writing 92 bytes, the remaining, unwritten bytes are unchanged.

Figure 9 shows the timing relationships for data transfers. When the SPOL pin is high, data on SDO is valid on the rising edge of SCLK. When the SPOL pin is low, data on SDO is valid on the falling edge of SCLK.

All data is written to and read from the port LSB first. When writing to the port, SDI input data is sampled on the rising edge of SCLK.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

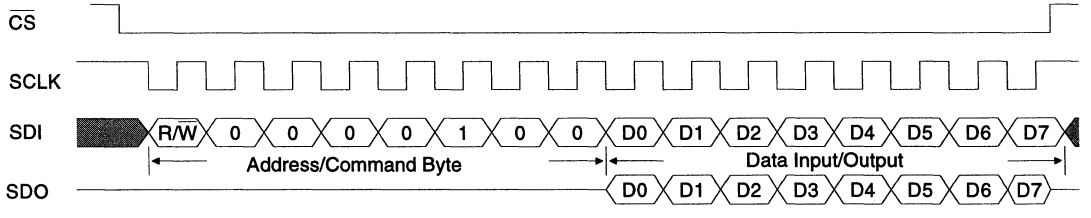


Figure 9. Serial Read/Write Timing

Host-Mode Parallel-Port Operation

This mode is selected by setting pins MODE and P/$\overline{S}$ to logic high. In parallel-port host mode, the CS61584 is controlled via a multiplexed bi-directional address/data bus.

Any read or write to the serial port is initiated by first writing an 8-bit address byte. The address byte consists of two nibbles. The four most significant bits can select one of 16 CS61584s on a board, and the four least significant bits select one of ten registers in that IC. The IC address is set for each CS61584 by hard wiring pins SAD7, SAD6, SAD5 and SAD4 to ground or power supply as appropriate. The CS61584 will compare the value of pins SAD7-SAD4 to the value of address bits AD7-AD4. When all four pins/bits match, the next four address bits are used to access a register. This architecture allows up to 16 CS61584 devices to share the same chip select signal and parallel bus.

Registers h0 to h7 are read and written as described above. Registers h8 and h9 are used to access multiple bytes of the CS61584's Arbitrary Waveform RAM, and use additional addressing. Reading or writing arbitrary waveform data requires two consecutive address bytes per data bytes. The first address byte is a standard IC/register byte, and contains register address of either h8 or h9. The second address byte is an eight bit, unsigned binary number, which identifies one of 42 RAM byte locations (numbered h00 to h29). Register h8 allows access to one bank of 42 bytes; register h9 allows access to a second bank of 42 bytes. When communicating over the port, the third byte, which follows the address, and RAM address, is the data byte.

The CS61584 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the Switching Characteristics for more details. The multiplexed bus on the CS61584 saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the CS61584 latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or $\overline{WR}$ pulses. In a read cycle, the CS61584 outputs a byte of data during the latter portion of the DS or $\overline{RD}$ pulses. the read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or as DS transitions low in Motorola timing.

ARBITRARY WAVEFORM GENERATION

In addition to the predefined pulse shapes, the user can create arbitrary pulse shapes using the host mode. This flexibility allows the board designer to accommodate non-standard cables, EMI filters, protection circuitry, etc.

The arbitrary pulse shape of mark (a transmitted "1") is specified by describing it's pulse shape across three Unit Intervals (UIs). This allows, for example, the long DSX-1 return-to-zero tail to extend into the next UI, as is required for isolated DSX-1 pulses. As another example, for T1 long-haul waveforms, the pulse shape can smear across three UIs.

Each UI is divided into multiple phases, and the users defines the amplitude of each phase. The waveform of a space (a transmitted "0") is fixed at zero volts. Examples of the phases are shown in Figure 10. In all cases, to define an arbitrary waveform, the user writes to the Waveform Register 42 times (14 phases per UI for three UIs). The phases are written in the order: UI1/phase1, UI1/phase2, ... , UI1/phase14, UI2/phase1, ... , UI2/phase14, UI3/phase1, ... , UI3/phase14.

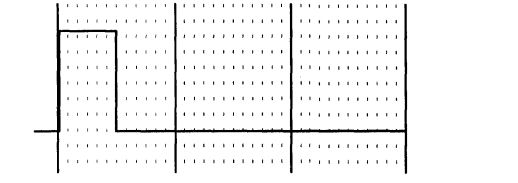
For E1 applications, as selected by the CON<0:3> bits or pins, the CS61584 divides the 488 ns UI into 12 uniform phases (40.7 ns each), and will ignore the phase amplitude information written for phases 13 and 14 of each UI.

For DSX-1 applications, the CS61584 divides the 648 ns UI into 13 uniform phases (49.8 ns each), and will ignore the phase amplitude information written for phase 14 of each UI.

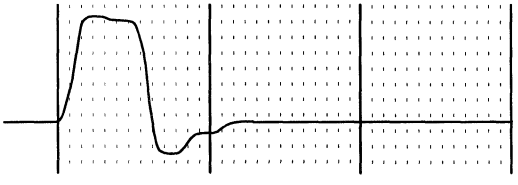
For DS-1 applications, the CS61584 divides the 648 ns UI into 14 uniform phases (46.3 ns each), and uses the phase information written for all 14 phases of each UI.

When transmitting pulses, the CS61584 will add the amplitude information from the prior two symbols with the amplitude of the first UI of the current symbol before outputting a signal on TTIP/TRING. Therefore, a mark preceded by two spaces will be output exactly as the mark is programmed. However, when one mark is preceded by marks, the first portion of the last mark may be modified. With AMI data, where successive pulses have opposite polarity, the undershoot tail of one pulse will cause the rising edge of the next mark to rise more quickly, as shown in Figure 11. If the sum of the amplitudes exceed the full scale values defined below, the sum is replaced by the full scale value, and an error indication is made by setting bit Latched_OVERFLOW in the status register.

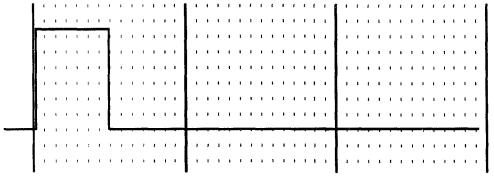
The amplitude of each phase is described by a 7-bit, 2's compliment number, where a positive value describes pulse amplitude, and a negative value describes pulse undershoot. The positive full value is hex 3F. The negative full value is hex 41. For T1, the typical output voltage is 38 mV/LSB. For E1 coax, the typical output voltage



E1 Arbitrary Waveform Example



DSX-1 (54% duty cycle) Arbitrary Waveform Example



DS-1 (50% duty cycle) Arbitrary Waveform Example

Figure 10. Phase definition of Arbitrary Pulses

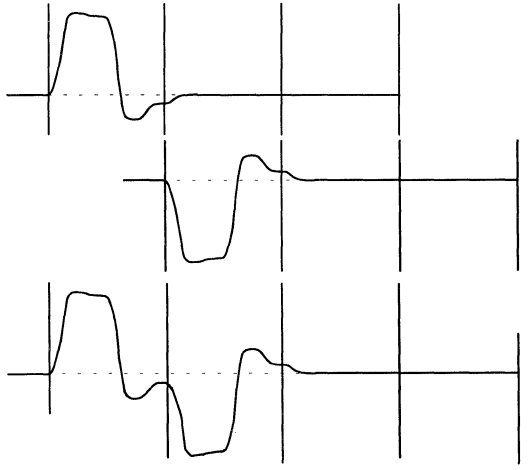


Figure 11. Example of Summing of Waveforms

is 22 mV/LSB. For E1 shielded twisted pair, the typical output voltage is 27 mV/LSB. All voltages are peak voltages across the TTIP and TRING outputs. On the secondary of a 1:2 step-up transformer, the mV/LSB is twice the values stated above. Note that although the full scale digital input is 3F, it is recommended that full scale output voltage on the transformer primary be limited to 2.4 Vpk. At higher output voltages, the driver may not drive the requested output voltage.

The amplitude information for all phases is written via either the parallel-port or serial-port to Arbitrary Pulse Shape registers as described in an earlier section. Each phase amplitude is written as an eight-bit byte, where the first phase of the symbol is written first. If a burst write terminates before all phases are written, the unwritten phases retain their previous value. If too many bytes are written into Channel 1 Arbitrary Pulse Shape Register during burst mode, the extra bytes are written into the Channel 2 Arbitrary Pulse Shape Register. If too many bytes are written into Channel 2 Arbitrary Pulse Shape Register during burst mode, the extra bytes are ignored.

In serial-port host mode, the amplitude bytes are written LSB first.

The contents of the Arbitrary Waveform register can be verified by performing a read.

POWER SUPPLY

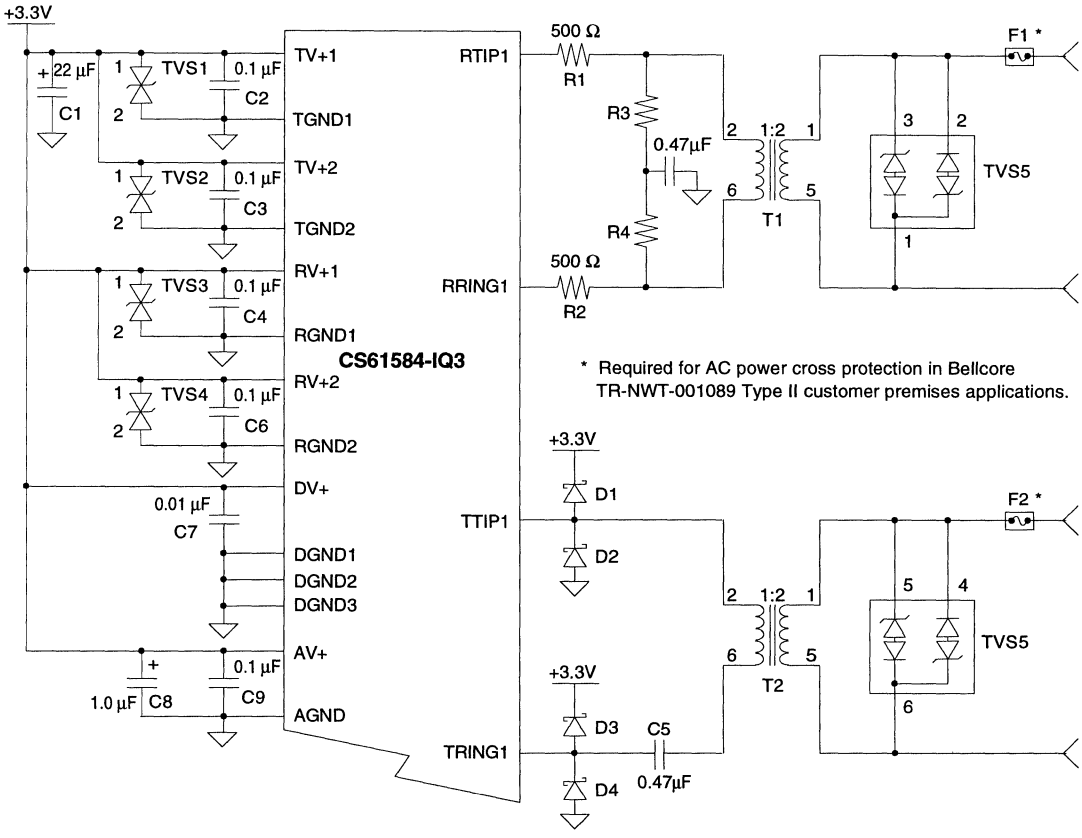
The device operates from a single 3.3 Volt or 5 Volt supply. Separate pins for the various supplies provide internal isolation. However, these pins should be connected externally with the power supply pins de-coupled to their respective grounds. The various ground pins must not be more negative than AGND.

De-coupling and filtering of the power supplies is crucial for the proper operation of the analog circuits. The best way to configure the power supplies is to tie all of the supply pins together at the chip. As shown in Figure 1, a capacitor should be connected between each supply and its respective ground. For the 1 µF and smaller capacitors, use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. Wire-wrap bread boarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the de-coupling capacitors. A 5k Ω, 1%, resistor should connect BGREF to ground.

SURGE PROTECTION

This section presents guidelines on the selection and use of external components for secondary transmission line surge protection. Several transient immunity and electrical safety standards define requirements for different T1 and E1 interfaces. For T1 applications these requirements are contained in Bellcore TR-NWT-001089, FCC Part 68 and UL1459. TR-1089 defines the intra-building lightning surge and AC power cross requirements for DSX-1 interface applications for which these recommendations are based. Requirements for E1 applications have not been harmonized and must be satisfied in each country individually. CCITT K.20 and IEC 801-5 define requirements typical of those in many countries. Refer to the Crystal application note, "Secondary Line Protection for T1 and E1 Line Cards" for more information on these standards.

Figure 12 shows the recommended secondary line protection components. These components provide current and voltage limiting for metallic TIP/RING surges and take advantage of the isolation provided by the line transformers to prevent damage from longitudinal (common mode) surges to ground.



Component	Description	Part #	Manufacturer
TVS1-TVS4	6.0V, 300W, bi-directional TVS	SM05	Semtech Corporation
TVS5	12V, 600W, low capacitance, bi-directional TVS array	VSB06P12LC	Protek Devices
D1-D4	Schottky diode	1N5711	BKC International
F1, F2	1.0A, time delay fuse	TR-8T	Wickman U.S.A.
R3,R4	1%, metal-film resistor 12.5Ω - 100Ω, T1 15Ω - 120Ω, E1 9.37Ω - 75Ω, E1		
T1, T2	1:2, 1500V pulse transformer	PE-65351 67129300 0553-0013-HC	Pulse Engineering Schott Corporation Bel Fuse

Figure 12. Application Circuit with Line Protection

Since the line side of each transformer is floating relative to chassis ground, it is not necessary to provide common-mode clamping for longitudinal surges as long as the high potential isolation rating of the transformers is not exceeded. The TR-1089 intra-building lightning surge standard requires immunity from longitudinal surges of 1500 Vpk. The transformers T1 and T2 specified here will withstand these surges since they are rated for high potential isolation in excess of 1500 VRMS (at 60 Hz). Transformers with additional isolation are required in some European countries.

TVS5 contains low capacitance avalanche diodes which provide voltage limiting protection for the transformers and the CS61584 during metallic (differential mode) surges. Each protector in TVS5 has a maximum clamping voltage of approximately 16V and are rated to handle the 800V-100A, 2/10µs intra-building lightning surge required by TR-1089 and the 10/700µs surges required by CCITT K.20 and IEC 801-5.

The 1.0A time delay fuses, F1 and F2, provide series current limiting protection in the event of a sustained fault condition such as contact with an AC power line or an analog subscriber line carrying battery or ringing voltages. The time delay fusing characteristic allows the fuses to survive the peak surge currents of lightning surges and still fuse quickly during sustained fault currents before the ignition of building wiring or other components on the line card. TR-1089 requires that all DSX-1 customer premises equipment safely handle a 120 V AC power cross fault. (Equipment on outside lines is subject to a more comprehensive series of power cross requirements). During a power cross fault, the equipment must not present a fire or electrical safety hazard, but may become non-functional and blow fuses.

The receive line is coupled to the CS61584 by the 1:2 step-down transformer T1. R3 and R4 terminate the receive line. On the IC side of the transformer, R1 and R2 provide protection for the receiver RTIP and RRING input pins. These series resistors limit surge currents when the CS61584's internal protection diodes become forward biased. During normal operation when the internal protection diodes on RTIP and RRING are reversed biased, these inputs are high impedance, and R1 and R2 will not reduce input sensitivity.

The CS61584 transmitter is coupled to the line by the 1:2 step-up transformer, T2. Although the transformer and TVS5 will limit longitudinal and metallic surges, additional protection on the TTIP and TRING output pins is required. D1-D4 are Schottky diodes which clamp the transmitter output pins within the power supply rails preventing SCR latch-up and damage to the internal ESD protection diodes. These diodes will only be required to handle a small portion of the surge energy which is coupled across the transformer inter-winding capacitance during a longitudinal surge. During a metallic surge they will provide protection for the IC until TVS5 enters avalanche breakdown.

TVS1 - TSV4 provides ESD and over voltage protection for the CS61584 power supply pins. These devices also limit surges coupled from the transmission lines onto the power supply by the CS61584's internal clamp diodes or the external Schottky diodes to prevent damage to other components.

While these recommendations provide practical guidelines on how to satisfy common transient immunity and electrical safety requirements, they should not replace careful design verification and testing. The effectiveness of line protection will depend upon the specific components chosen and how they are implemented in a particular system. The following guidelines should be followed to insure optimum protection without impacting signal quality.

1. T1 and E1 line connections should be *physically isolated* from other components on the same circuit board. Provide adequate component spacing between line side components and chassis ground contact points to prevent arcing.

2. T1 and E1 line connections should be *electrically isolated* from other components on the same circuit board. Careful attention to board layout should insure that no signal traces cross the transformer isolation barrier on any layer of the board.

3. Printed circuit board traces must be of appropriate size and length. The length of T1 or E1 analog signal connections should be minimized and trace width should be at least 20-25 mils to limit trace inductance. Short, wide traces preserve the bandwidth of the signal path to insure compliance with transmitter pulse template specifications. Voltage limiting components should be placed close to the device they are protecting because trace impedance results in increased peak surge voltages. D1-D4 and TVS1-TVS4 should be placed directly beside the CS61584.

JTAG BOUNDARY SCAN

JTAG boundary scan supports board testing. Using boundary scan, the integrity of the digital paths between ICs on a board can be verified. This verification is supported by the ability to externally set the signals on the CS61584's digital output pins, and to externally read the signals present on the CS61584's input pins. Additionally, the manufacturer ID, part number and revision of the CS61584 can be read during board test.

As shown in Figure 13, the JTAG hardware consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the Test Mode Select (J_TMS) and Test Clock (J_TCK) input pins. Data is shifted into the registers via the Test Data Input (J_TDI) pin, and shifted out of the registers via the Test Data Output (J_TDO) pin, again using J_TCK. The Instruction register defines which data register is included in the shift operation. Note that if J_TDI is left floating, an internal pull-up resistor forces the pin high.

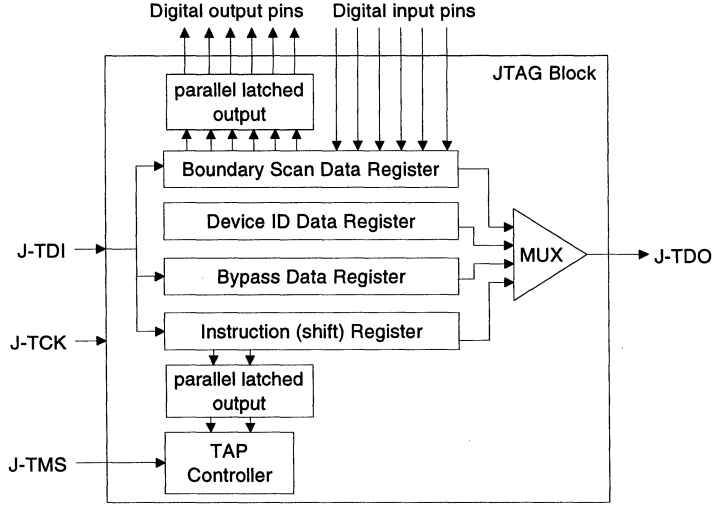


Figure 13. JTAG Circuitry Block Diagram

JTAG Data Registers (DR)

The test data registers are: the Boundary-Scan Register (BSR), the Device Identification Register (DIR), and the Bypass Register (BR).

Boundary Scan Register: The BSR can be connected in parallel to all the digital I-O pins, and provides the mechanism for applying/reading test patterns to/from the board traces. The BSR is initialized and read using the instruction SAMPLE/PRELOAD. The bit ordering for the BSR is the same as the top-view packaged pin out, counter-clockwise beginning with PD1 (pin 15) and ending with LOS1 (pin 7), as shown in Table 7. The analog, oscillator, power, ground, CLKE/IPOL and MODE pins are not included as part of the boundary-scan register. CLKE/IPOL and MODEare not included because they are typically hard-wired to power or ground on a board.

All output pins are 3-state pins (logic high, logic low or high impedance); their value can be set via the PRELOAD/EXTEST instructions. Since outputs are all 3-state, 2 bits are required to specify the states of each output pin in the BSR. The first bit (which is shifted in first) contains the testing data which may be output on the pin. The second bit ,which is shifted in following the first bit, selects between an output-enabled state (bit set to 1) or high-impedance state (bit set to 0). Thus, two J_TCK cycles are required to load testing data for each output pin.

Each input pin requires only 1 bit in the BSR.

The bi-directional pins, TNEG1/AIS1, TNEG2/AIS2, INT/RLOOP, LOS1/SAD6, LOS2,/SAD7 and the AD<0:7> pins have three bits in the BSR. The first bit shifted into the BSR captures the value of the pin. This pin may have its value set externally (if the third bit is 0) or set internally (if the third bit is 1). The second bit shifted into the BSR sets the output value. This value is output on the pin when the third bit is 1. The third bit configures the output driver as high-impedance (bit set to 0) or active (bit set to 1).

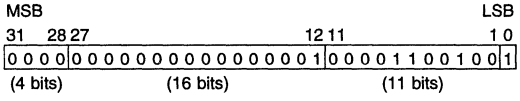
Thus, the entire BSR is 62 bits long.

BSR bits	Pin Name	Pin #	Pad Type
1	PD1, SAD4	15	input
2	PD2, SAD5	34	input
3	BTS, CON32	41	input
4-6	LOS2, SAD7	42	bi-directional
7-9	TNEG2, AIS2	43	bi-directional
10	TPOS2, TDATA2	44	input
11	TCLK2	45	input
12-13	RNEG2, BPV2	46	output
14-15	RPOS2, RDATA2	47	output
16-17	RCLK2	48	output
18	WR(R/W), CON31	49	input
19	ALE(AS), CON22	50	input
20-22	AD7, CON21	51	bi-directional
23-25	AD6, CON12	52	bi-directional
26-28	AD5, CON11	53	bi-directional
29-31	AD4, CON02	54	bi-directional
32-34	AD3, CON01	58	bi-directional
35-37	AD2, TAOS2	59	bi-directional
38-40	AD1, SDI, TAOS1	60	bi-directional
41-43	AD0, SDO, LLOOP1	61	bi-directional
44	RD(DS), SCLK, LLOOP2	62	input
45-47	INT, RLOOP	63	bi-directional
48	CS, ATTEN1	64	input
49-50	RCLK1	1	output
51-52	RPOS1, RDATA1	2	output
53-54	RNEG1, BPV1	3	output
55	TCLK1	4	input
56	TPOS1, TDATA1	5	input
57-59	TNEG1, AIS1	6	bi-directional
60-62	LOS1, SAD6	7	bi-directional

Table 7. Boundary Scan Register Contents

Note that the interrupt pin on the CS61584 has the ability of being a active high or active low signal. In host mode, the IPOL pin controls this functionality. During JTAG testing in host mode, the polarity of the INT pin will be determined by the state of the IPOL pin. The INT pin on the CS61584 should not be configured as an output by the JTAG BSR if the device is in hardware mode. Likewise, the INT pin should not be configured as an input by the JTAG BSR if the device is in host mode.

Device Identification Register: The DIR provides the manufacturer, part number, and version of the CS61584. This information can be used to verify that the proper version or revision number has been inserted into the system under test. The DIR is 32 bits long and is partitioned as follows (31=MSB):



BIT #(s)	FUNCTION	Total Bits
31-28	Version number	4
27-12	Part Number	16
11-1	Manufacturer Number	11
0	Constant Logic '1'	1

Data from the DIR is shifted out to J_TDO LSB first.

Bypass Register: The Bypass register consists of a single bit, and provides a serial path between J_TDI and J_TDO, bypassing the BSR. The provision of this register allows the bypassing of those segments of the board-level serial test register which are not required for a specific test. This also reduces test access times, by reducing the total number of shifts required from J_TDI to J_TDO.

JTAG Instructions and Instruction Register (IR)

The instruction register (2 bits) allows the instruction to be shifted into the circuit. The instruction is used to select the test to be performed or the data register to be accessed or both. The valid instructions are (LSB shifted in first):

IR CODE	INSTRUCTION
00	EXTEST
01	SAMPLE/PRELOAD
10	IDCODE
11	BYPASS

EXTEST Instruction: The EXTEST instruction allows testing of off-chip circuitry and board-level interconnect. EXTEST connects the BSR to J_TDI and J_TDO. The normal path between the CS61584 logic and it's IO pins is broken; the signals on the output pins are loaded from the BSR; the signals on the input pins are loaded into the BSR.

SAMPLE/PRELOAD Instruction: The SAMPLE/PRELOAD instructions allows scanning of the boundary-scan register without interfering with the operation of the CS61584. This instruction connects the BSR to J_TDI and J_TDO. The normal path between the CS61584 logic and its IO pins is maintained; the signals on those IO pins are loaded into the BSR. Additionally, this instruction can be used to latch values into the digital output pins.

IDCODE Instruction: The IDCODE instruction connects the device identification register to J_TDO. The IDCODE instruction (10) is forced into the instruction register during the Test-Logic-Reset controller state. Also, after the reset of the chip, the default instruction is IDCODE.

BYPASS Instruction: The BYPASS instruction connects the minimum length, Bypass register between J_TDI and J_TDO, and allows data to be shifted in the Shift-DR controller state.

Internal Testing Considerations

Note that the INTEST instruction is not supported because of the difficulty of performing significant internal tests using JTAG. The most complete internal test would involve inputting digital data on pins TCLK, TPOS, TNEG, activating local loopback#2, and reading that same data out on pins RCLK, RPOS and RNEG. This test would include the full transmit path, the full receive path, and optionally, the jitter attenuator, and provides excellent test coverage of the functional blocks. However, this test is difficult to implement for two reasons.

First, TCLK and REFCLK must be clocked at specific frequencies, e.g., T1/E1±200 ppm for TCLK. If these frequency requirements are not met, the performance of the transmitter, clock recovery circuit and jitter attenuator is not guaranteed. It would be difficult with JTAG to toggle the TCLK input at the required rate.

Second, the loopback path includes two asynchronous blocks, clock recovery and jitter attenuator. Therefore, the exact time delay for a TPOS-input appearing on RPOS-output is variable, making output signature correlation difficult.

The one test that could be easily performed using an arbitrary clock rate on TCLK and REFCLK is local loopback#1, with jitter attenuator disabled. However, that test provides such limited fault coverage, that is only useful in determining if the device had been catastrophically destroyed. Alternatively, catastrophic destruction of the IC and/or surrounding board traces can be detected using EXTEST. Therefore, the INTEST instruction was viewed as providing little significant incremental testing capability, while adding to product complexity, and was not included in the CS61584.

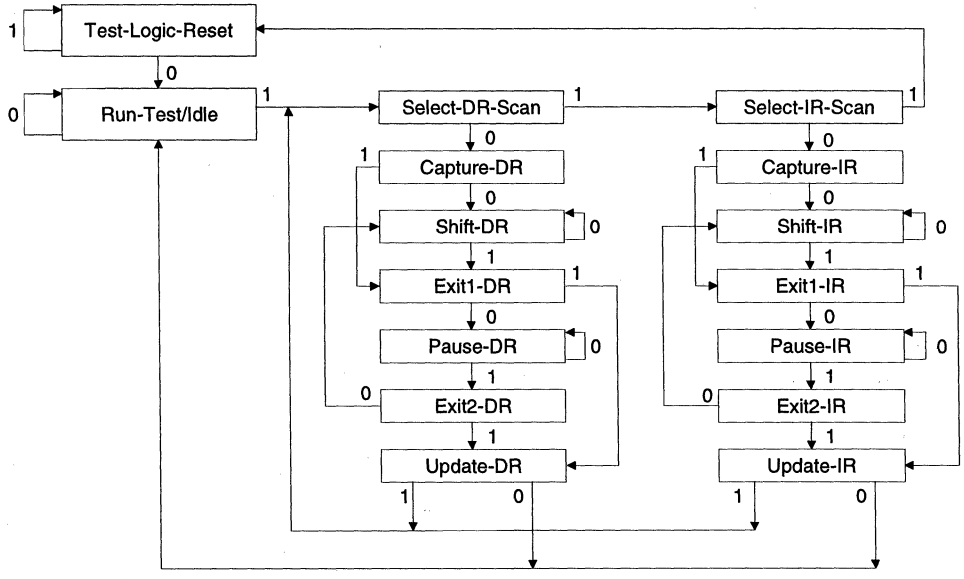


Figure 14. TAP controller State Diagram

JTAG TAP Controller

Figure 14 shows the state diagram for the TAP state machine. A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure is the value present at J_TMS at each rising edge of J_TCK.

Test-Logic-Reset State

In this state, the test logic is disabled so that normal operation of the device can continue unhindered. During initialization, the CS61584 initializes the instruction register such that the IDCODE instruction is loaded.

No matter what the original state of the controller, the controller enters Test-Logic-Reset state when the J_TMS input is held high (logic 1) for at least five rising edges of J_TCK. The controller remains in this state while J_TMS is high. The CS61584 processor automatically enters this state at power-up.

Run-Test/Idle State

This is a controller state between scan operations. Once in this state, the controller remains in this state as long as J_TMS is held low. The instruction register and all test data registers retain their previous state. When J_TMS is high and a rising edge is applied to J_TCK, the controller moves to the Select-DR state.

Select-DR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If J_TMS is held low and a rising edge is applied to J_TCK when in this state, the controller moves into the Capture-DR state, and a scan sequence for the selected test data register is initiated. If J_TMS is held high and a rising edge applied to J_TCK, the controller moves to the Select-IR-Scan state.

The instruction does not change in this state.

Capture-DR State

In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The other test data registers, which do not have parallel input, are not changed.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to J_TCK, the controller enters the Exit1-DR state if J_TMS is high or the Shift-DR state if J_TMS is low.

Shift-DR State

In this controller state, the test data register connected between J_TDI and J_TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of J_TCK.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to J_TCK, the controller enters the Exit1-DR state if J_TMS is high or remains in the Shift-DR state if J_TMS is low.

Exit1-DR State

This is a temporary state. While in this state, if J_TMS is held high, a rising edge applied to J_TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J_TMS is held low and a rising edge is applied to J_TCK, the controller enters the Pause-DR state.

The test data register selected by the current instruction retains its previous value during this

state. The instruction does not change in this state.

Pause-DR State

The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between J_TDI and J_TDO. An example use of this state could be to allow tester to reload its pin memory from disk during application of a long test sequence.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as J_TMS is low. When J_TMS goes high and a rising edge is applied to J_TCK, the controller moves to the Exit2-DR state.

Exit2-DR State

This is a temporary state. While in this state, if J_TMS is held high, a rising edge applied to J_TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If J_TMS is held low and a rising edge is applied to J_TCK, the controller enters the Shift-DR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Update-DR State

The Boundary Scan Register is provided with a latched parallel output to prevent changes at the parallel output while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched onto the parallel output of this register from the shift-register path on the falling edge of J_TCK. The data held at the latched parallel output does not change other than in this state.

All shift-register stages in the test data register selected by the current instruction retains their previous value during this state. The instructions does not change in this state.

Select-IR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If J_TMS is held low and a rising edge is applied to J_TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If J_TMS is held high and a rising edge is applied to J_TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change in this state.

Capture-IR State

In this controller state, the shift register contained in the instruction register loads a fixed value of "01" on the rising edge of J_TCK. This supports fault-isolation of the board-level serial test data path.

Data registers selected by the current instruction retain their value during this state. The instructions does not change in this state.

When the controller is in this state and a rising edge is applied to J_TCK, the controller enters the Exit1-IR state if J_TMS is held high, or the Shift-IR state if J_TMS is held low.

Shift-IR State

In this state the shift register contained in the instruction register is connected between J_TDI and J_TDO and shifts data one stage towards its serial output on each rising edge of J_TCK.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

When the controller is in this state and a rising edge is applied to J_TCK, the controller enters the Exit1-IR state if J_TMS is held high, or remains in the Shift-IR state if J_TMS is held low.

Exit1-IR State

This is a temporary state. While in this state, if J_TMS is held high, a rising edge applied to J_TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If J_TMS is held low and a rising edge is applied to J_TCK, the controller enters the Pause-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Pause-IR State

The pause state allow the test controller to temporarily halt the shifting of data through the instruction register.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as J_TMS is low. When J_TMS goes high and a rising edge is applied to J_TCK, the controller moves to the Exit2-IR state.

Exit2-IR State

This is a temporary state. While in this state, if J_TMS is held high, a rising edge applied to J_TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If J_TMS is held low and a rising edge is applied to J_TCK, the controller enters the Shift-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

Update-IR State

The instruction shifted into the instruction register is latched onto the parallel output from the shift-register path on the falling edge of J_TCK. Once the new instruction has been latched, it becomes the current instruction.

Test data registers selected by the current instruction retain their previous value.

JTAG Application Examples

Figures 15 and 16 show examples of updating the instruction register and data registers.

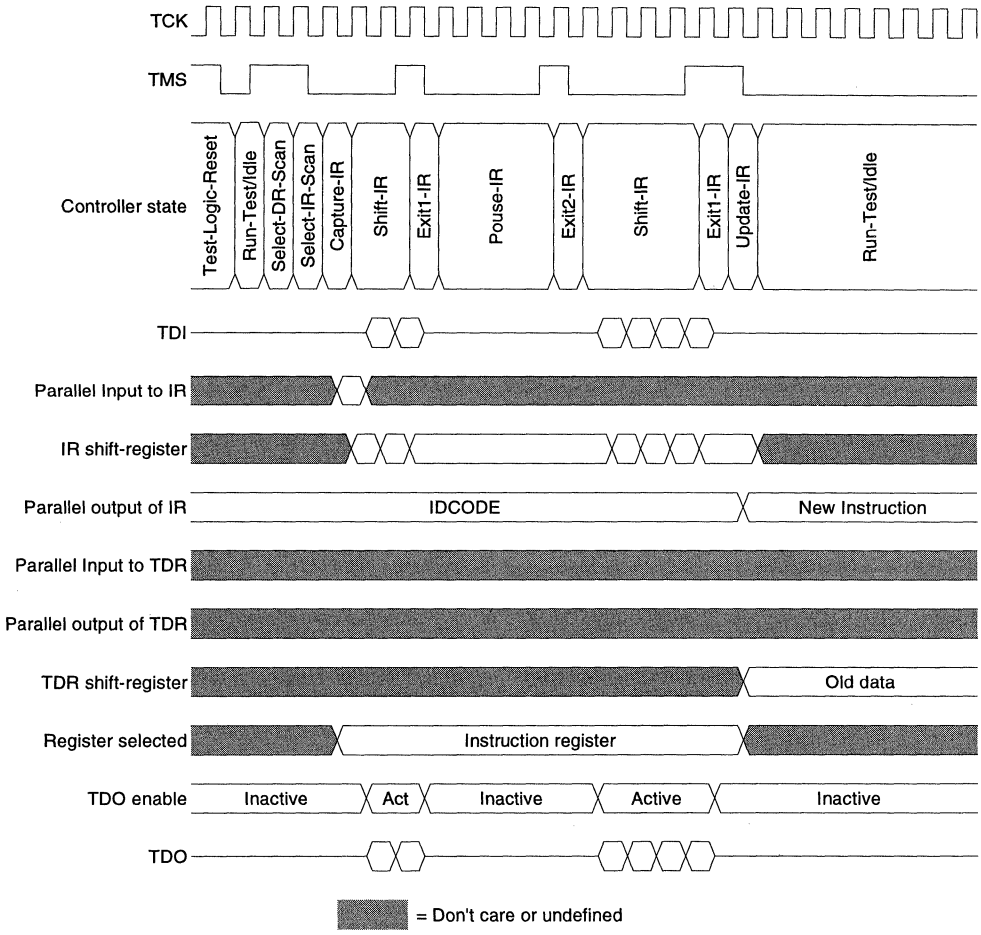


Figure 15. Test Logic Operation: Instruction Scan

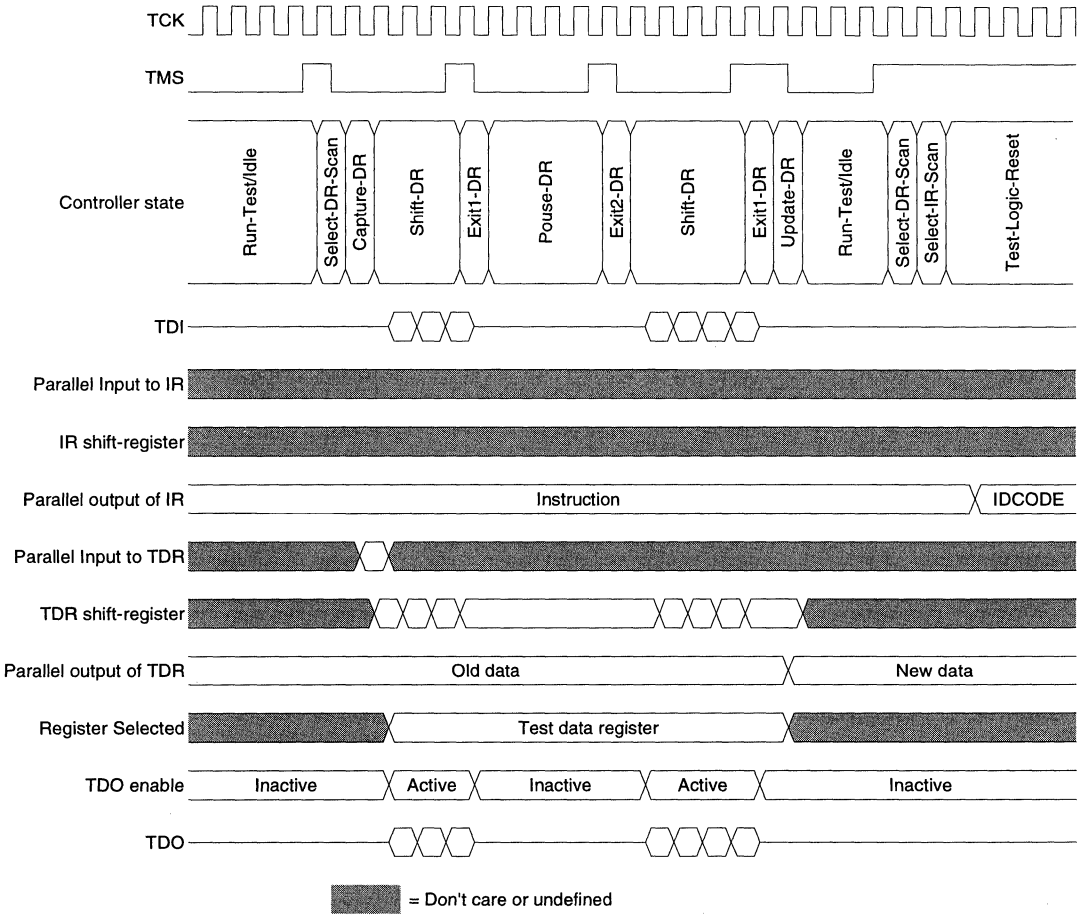
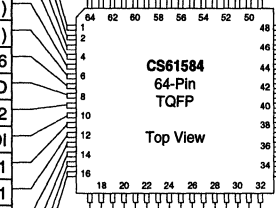


Figure 16. Test Logic Operation: Data Scan

PIN DESCRIPTIONS

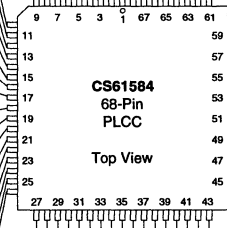
Hard-ware Mode	Host Mode Serial Port	Host Mode Parallel Port
DGND1	DGND1	DGND1
CON01	not used*	AD3
TAOS2	SPOL	AD2
TAOS1	SDI	AD1
LLOOP2	SDO	AD0
LLOOP1	SCLK	$\overline{RD}$ (DS)
RLOOP	INT	INT
ATTEN1	$\overline{CS}$	$\overline{CS}$
RCLK1	RCLK1	RCLK1
RPOS1	RPOS1(RDATA1)	RPOS1(RDATA1)
RNEG1	RNEG1(BPV1)	RNEG1(BPV1)
TCLK1	TCLK1	TCLK1
TPOS1	TPOS1(TDATA1)	TPOS1(TDATA1)
TNEG1	TNEG1 (AIS1)	TNEG1(AIS1)
LOS1	LOS1	SAD6
J-TDO	J-TDO	J-TDO
DGND2	DGND2	DGND2
J-TDI	J-TDI	J-TDI
TTIP1	TTIP1	TTIP1
TV+1	TV+1	TV+1
TGND1	TGND1	TGND1
TRING1	TRING1	TRING1
PD1	PD1	SAD4
ATTEN0	P/$\overline{S}$	P/$\overline{S}$
RTIP1	RTIP1	RTIP1
RRING1	RRING1	RRING1
RV+1	RV+1	RV+1
RGND1	RGND1	RGND1
MODE	MODE	MODE
BGREF	BGREF	BGREF
AGND	AGND	AGREF
AV+	AV+	AV+



Hard-ware Mode	Host Mode Serial Port	Host Mode Parallel Port
DV+	DV+	DV+
DGND3	DGND3	DGND3
CON02	not used*	AD4
CON11	not used*	AD5
CON12	not used*	AD6
CON21	not used*	AD7
CON22	not used*	ALE(AS)
CON31	not used*	$\overline{WR}$(R/$\overline{W}$)
RCLK2	RCLK2	RCLK2
RPOS2	RPOS2 (RDATA2)	RPOS2(RDATA2)
RNEG2	RNEG2(BPV2)	RNEG2(BPV2)
TCLK2	TCLK2	TCLK2
TPOS2	TPOS2(TDATA2)	TPOS2(TDATA2)
TNEG2	TNEG2(AIS2)	TNEG2(AIS2)
LOS2	LOS2	SAD7
CON32	not used*	BTS
J-TCK	J-TCK	J-TCK
J-TMS	J-TMS	J-TMS
TTIP2	TTIP2	TTIP2
TV+2	TV+2	TV+2
TGND2	TGND2	TGND2
TRING2	TRING2	TRING2
PD2	PD2	SAD5
CLKE	IPOL	IPOL
RTIP2	RTIP2	RTIP2
RRING2	RRING2	RRING2
RV+2	RV+2	RV+2
RGND2	RGND2	RGND2
1XCLK	1XCLK	1XCLK
XTALOUT	XTALOUT	XTALOUT
REFCLK	REFCLK	REFCLK
RESET	RESET	RESET

Note: ***not used*** pins should be tied to ground.

Hard-ware Mode	Host Mode Serial Port	Host Mode Parallel Port
DGND1	DGND1	DGND1
CON01	not used*	AD3
TAOS2	SPOL	AD2
TAOS1	SDI	AD1
LLOOP2	SDO	AD0
LLOOP1	SCLK	$\overline{RD}$ (DS)
RLOOP	INT	INT
ATTEN1	$\overline{CS}$	$\overline{CS}$
not used*	not used*	not used*
RCLK1	RCLK1	RCLK1
RPOS1	RPOS1(RDATA1)	RPOS1(RDATA1)
RNEG1	RNEG1(BPV1)	RNEG1(BPV1)
TCLK1	TCLK1	TCLK1
TPOS1	TPOS1(TDATA1)	TPOS1(TDATA1)
TNEG1	TNEG1(AIS1)	TNEG1(AIS1)
LOS1	LOS1	SAD6
J-TDO	J-TDO	J-TDO
DGND2	DGND2	DGND2
J-TDI	J-TDI	J-TDI
TTIP1	TTIP1	TTIP1
TV+1	TV+1	TV+1
TGND1	TGND1	TGND1
TRING1	TRING1	TRING1
PD1	PD1	SAD4
ATTEN0	P/$\overline{S}$	P/$\overline{S}$
not used*	not used*	not used*
RTIP1	RTIP1	RTIP1
RRING1	RRING1	RRING1
RV+1	RV+1	RV+1
RGND1	RGND1	RGND1
MODE	MODE	MODE
BGREF	BGREF	BGREF
AGND	AGND	AGND
AV+	AV+	AV+



Hard-ware Mode	Host Mode Serial Port	Host Mode Parallel Port
DV+	DV+	DV+
DGND3	DGND3	DGND3
CON02	not used*	AD4
CON11	not used*	AD5
CON12	not used*	AD6
CON21	not used*	AD7
CON22	not used*	ALE (AS)
CON31	not used*	$\overline{WR}$ (R/$\overline{W}$)
not used*	not used*	not used*
RCLK2	RCLK2	RCLK2
RPOS2	RPOS2(RDATA2)	RPOS2(RDATA2)
RNEG2	RNEG2(BPV2)	RNEG2(BPV2)
TCLK2	TCLK2	TCLK2
TPOS2	TPOS2(TDATA2)	TPOS2(TDATA2)
TNEG2	TNEG2(AIS2)	TNEG2(AIS2)
LOS2	LOS2	SAD7
CON32	not used*	BTS
J-TCK	J-TCK	J-TCK
J-TMS	J-TMS	J-TMS
TTIP2	TTIP2	TTIP2
TV+2	TV+2	TV+2
TGND2	TGND2	TGND2
TRING2	TRING2	TRING2
PD2	PD2	SAD5
CLKE	IPOL	IPOL
not used*	not used*	not used*
RTIP2	RTIP2	RTIP2
RRING2	RRING2	RRING2
RV+2	RV+2	RV+2
RGND2	RGND2	RGND2
1XCLK	1XCLK	1XCLK
XTALOUT	XTALOUT	XTALOUT
REFCLK	REFCLK	REFCLK
RESET	RESET	RESET

Note: ***not used** pins should be tied to ground.

Power Supplies

AGND - Ground, Analog, Pin 23.
Analog supply ground pin.

AV+ - Power Supply, Analog, Pin 24.
Analog supply ground pin for internal bandgap reference, oscillator and internal clock multipliers

BGREF - Bandgap Reference, Pin 22.
Used by the internal bandgap reference. This pin should be connected to ground by a 5k ohm resistor.

DGND1, DGND2, DGND3 - Ground, Pins 57, 9 ,55.
Power supply ground pin for the digital circuitry in both channels.

DV+ - Power Supply, Pin 56.
Power supply pin for the digital circuitry in both channels.; typically +3.3 Volts referenced to DGND.

RGND1, RGND2 - Ground, Receiver, Pins 20, 29.
Power supply ground pins for the receivers.

RV+1, RV+2 - Power Supply, Receiver, Pins 19, 30.
Power supply pins for the analog circuitry in the receivers; typically +3.3 Volts referenced to RGND1 and RGND2.

TGND1, TGND2 - Ground, Transmit Drivers, Pins 13, 36.
Power supply ground pins for the transmitters.

TV+1, TV+2 - Power Supply, Transmit Drivers, Pins 12, 37.
Power supply pins for the transmitter analog circuitry; typically +3.3 Volts referenced to TGND1 and TGND2.

Control Pins and Control Buses

AD0-AD7 - Address/Data Bus, Pins 61, 60, 59, 58, 54, 53, 52, 51. (Host mode - parallel port)
The 8-bit multiplexed address/data bus.

ALE(AS) - Address Latch Enable (Address Strobe), Pin 50. (Host mode - parallel port)
A positive-going edge serves to demultiplex the bus.

ATTEN0 ATTEN1 - Jitter Attenuator Select, Pins 16, 64. (Hardware Mode)
Selects, for both channels, which path has jitter attenuation (transmit/receive/neither). See Table 4.

BTS - Bus Type Select, Pin 41. (Host mode - parallel port)

Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD(DS), ALE(AS), and WR(R/W) pins. If BTS=1, then these pins assume the function listed in parenthesis ().

CLKE - Clock Edge, Pin 33. (Hardware mode)

CLKE controls RCLK polarity. Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK.

CON01, CON11, CON21, CON31,
CON02, CON12, CON22, CON32 - Configuration Selection, Pins 58, 53, 51, 49, 54, 52, 50, 40. (Hardware Mode)

Configures the transmitter (pulse shape, pulse width, pulse amplitude and driver impedance), receiver (slicing level), and coder (HDB3 vs B8ZS) as shown in Table 1. The CONx1 pins control channel 1. The CONx2 pins control channel 2. Both channels must operate at the same rate (both T1 or both E1). The Arbitrary Waveform option is not available in the hardware mode using these pins.

$\overline{CS}$ - Chip Select, Pin 64. (Host modes)

Pin must transition from high to low to read or write the parallel or serial port.

INT - Receive Alarm Interrupt, Pin 63. (Host modes)

An interrupt is generated when a status register changes state to flag the host processor. INT is cleared by reading the status registers. The logic level for an active interrupt alarm is controlled by pin IPOL. INT is an open drain output and should be tied to the appropriate supply through a resistor.

IPOL - Interrupt Polarity, Pin 33. (Host mode)

IPOL controls INT polarity. Setting IPOL to logic 1 causes interrupts to be indicated by INT equal high. Setting IPOL to logic 0 causes interrupts to be indicated by INT equal to low.

LLOOP1, LLOOP2 - Local Loopback, Pin 61. (Hardware Mode)

Setting LLOOP to a logic 1 activates Local Loopback #1. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 21.

Setting MODE to logic 1 puts the line interface in the host mode. In the host mode, either a serial or parallel interface is used to control the line interface and monitor its status. Setting MODE to logic 0 puts the line interface in the hardware mode, where it is configured and monitored using discrete pins. MODE defines the function of pins shown across the top of the block diagram on the front page of the data sheet. Setting MODE to AV+/2 volts will cause unpredictable results.

PD1, PD2 - Power Down, Pins 15, 34. (Hardware mode, and Host mode-serial port)

Setting PD1 or PD2 to logic 1 puts the channel 1 or channel 2 line interface, respectively, in a low power, inactive state. Setting PD1 or PD2 to logic 0 returns the selected channel to normal operation.

P/$\overline{S}$ - Parallel/$\overline{Serial}$ Port selection, Pin 16. (Host modes)
Setting P/$\overline{S}$ to a logic 1 selects parallel port. Setting P/$\overline{S}$ to a logic 0 selects serial port.

$\overline{RD}$(DS) - Read Input (Data Strobe), Pin 62. (Host mode - parallel port)
When using the Intel bus interface, a low pulse selects a read operation when the CS61584 is selected by the $\overline{CS}$ pin. When using the Motorola bus interface, a high pulse performs a read/write operation if the CS61584 is selected by the $\overline{CS}$ pin.

RESET - Reset, Pin 25.
Setting RESET to logic 1 resets the CS61584, clears the host-mode control registers, and then sets LOS high.

RLOOP - Remote Loopback, Pin 63. (Hardware Mode)
Setting RLOOP to a logic 1 causes the recovered clock and data on both channels to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

SAD7 - SAD4 - Set Chip Address, Pins 42, 7, 35, 15. (Host mode - parallel port)
These pins are used to hard wire a chip address. The CS61584 will compare the value of pins SAD7 - SAD4 with the value of address bits AD7 - AD4, as part of its address decode procedures.

SCLK - Serial Clock, Pin 62. (Host mode - serial port)
Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{CS}$ pin.

SDI - Serial Data Input, Pin 60. (Host mode - serial port)
Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 61. (Host mode - serial port)
Status and control information from the on-chip register. If SPOL is high SDO is valid on the rising edge of SCLK. If SPOL is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS1,2 - Transmit All Ones Select, Pin 60, 59. (Hardware Mode)
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by REFCLK.

$\overline{WR}$(R/$\overline{W}$) - Write Input (Read/Write), Pin 49. (Host mode - parallel port)
When using the Intel bus interface, a low pulse selects a write operation when the CS61584 is selected by the $\overline{CS}$ pin. When using the Motorola bus interface, a logic 1 selects a read operation and a logic 0 selects a write operation.

Status

AIS1, AIS2 - All Ones Signal Detection, Pins 6, 43. (Host mode)
AIS goes high when an all-ones condition is detected using the detection criteria of less than nine zeros out of 8192 bit periods.

BPV1, BPV2 - Bipolar Violation Detection, Pins 3, 46. (Host mode)

BPV goes to a logic 1 for one bit period when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

LOS1, LOS2 - Loss of Signal, Pins 7, 42. (Hardware mode, and Host mode - serial port)

LOS goes to a logic 1 when 175 consecutive zeros have been detected. LOS returns to logic 0 when a 12.5% ones density signal returns.

SPOL - SDO Polarity Control, Pin 59. (host mode - serial port)

Setting SPOL to logic 1, causes SDO to be valid on the rising edge of SCLK. Setting SPOL to logic 0 causes SDO to be valid on the falling edge of SCLK.

Oscillator

1XCLK - One-times Clock Frequency Select, Pin 28.

When 1XCLK is set to logic 1, REFCLK should be a 1.544 MHz for T1 or 2.048 MHz for E1 applications. When 1XCLK is set to logic 0, REFCLK should be an 8x clock, i.e., 12.352 MHz for T1 or 16.384 MHz for E1 applications.

REFCLK - External Reference Clock Input, Pin 26.

A reference clock for the receiver and jitter attenuator circuits of both channels. When 1XCLK is set to logic 1, REFCLK should be 1.544 MHz for T1 or 2.048 MHz for E1 applications. When 1XCLK is set to logic 0, REFCLK should be 12.352 MHz for T1 or 16.384 MHz for E1 applications.

XTALOUT - Crystal Oscillator Output, Pin 27.

A quartz crystal calibrated at 12.352 MHz for T1 or 16.384 MHz for E1 may be connected across XTALOUT and REFCLK instead of a CMOS compatible clock source.

T1/E1 Data Inputs and Outputs

RCLK1, RCLK2 - Receive Clock, Pins 1, 48.
RPOS1/RDATA1, RPOS2/RDATA2 - Receive Positive Data, Pins 2, 47.
RNEG1, RNEG2 - Receive Negative Data, - Pins 3, 46.

The receiver recovered clock and NRZ digital data is output on these pins. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG. In coder mode, the decoded digital data stream is output on RDATA.

RTIP1, RRING1, RTIP2, RRING2 - Receive Tip, Receive Ring, Pins 17, 18, 32, 31.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs. Data and clock are recovered and output on RPOS/RNEG and RCLK.

TCLK1, TCLK2 - Transmit Clock, Pins 4, 45.
TPOS1/TDATA1, TPOS2/TDATA2 - Transmit Positive Data, Pins 5, 44.
TNEG1, TNEG2 - Transmit Negative Data, - Pins 6, 43.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted. In coder mode, the un-encoded digital data stream is input on TDATA.

TTIP1, TRING1, TTIP2, TRING2 - Transmit Tip, Transmit Ring, Pins 11, 14, 38, 35.

The AMI signal is driven to the line through these pins. This output is designed to drive the primary of the recommended transformer. In transparent mode, TPOS drives TTIP, and TNEG drives TRING.

Test

J_TCLK - JTAG Test Clock, Pin 40.

Data on pins J-TDI and J-TDO is valid on the rising edge of J-TCK. When J-TCK is stopped low, all JTAG registers remain unchanged.

J_TMS - JTAG Test Mode Select, Pin 39.

An active high signal on this pin enables the JTAG serial port. Connected to an internal pull-up resistor.

J_TDI - JTAG Test Data In, Pin 10.

JTAG data is shifted into the CS61584 via this pin. Connected to an internal pull-up resistor. Data should be stable on the rising edge of J-CLK.

J_TDO - JTAG Test Data Out, Pin 8.

JTAG data is shifted out of the CS61584 via this pin. This pin is active except when JTAG testing is in progress. J-TDO will be updated on the falling edge of J-TCK.

• Notes •

• Notes •

Semiconductor Corporation

CXT6176
CXT8192

Pullable Quartz Crystals

Features

- Complements CS61534, CS61535, CS61535A, CS61544, CS61574, CS61574A, and CS61575 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.

Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

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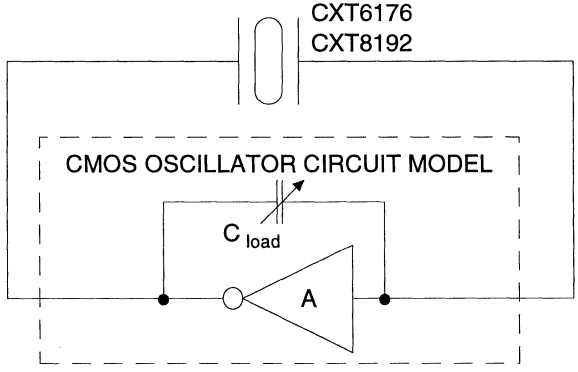
Ordering Information

CXT6176	Crystal for T1 Applications
CXT8192	Crystal for PCM-30 Applications



Crystal Line Interface or Jitter Attenuator I.C.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

CXT6176 Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 1)	-	370	390	ppm
Operating Frequency	C_{load} = 11.6 pF	(Note 2)	6.176803	-	-	MHz
	C_{load} = 19.0 pF	(Note 3)	6.175846	6.176000	6.176154	MHz
	C_{load} = 37.0 pF	(Note 2)	-	-	6.175197	MHZ

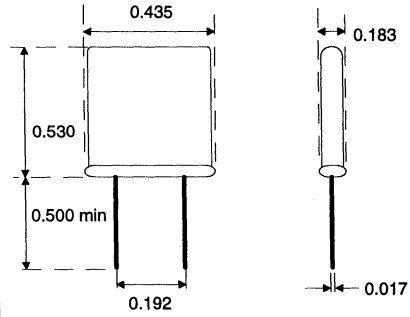
CXT8192 Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 1)	-	210	245	ppm
Operating Frequency	C_{load} = 11.6 pF	(Note 2)	8.192410	-	-	MHz
	C_{load} = 19.0 pF	(Note 3)	8.191795	8.192000	8.192205	MHz
	C_{load} = 37.0 pF	(Note 2)	-	-	8.191590	MHZ

Notes: 1. With C_{load} varying from 11.6 to 37.0 pF at a given temperature.
2. Measured at -40 to 85 °C.
3. Measured with Saunders 150D meter at 25 °C.

General Specifications & Package Dimensions

Mode	Fundamental
Drive Level	2 mW (max)
Aging	5 ppm/yr. (max)
Shock	10 G's, 6 ms, 6 planes
Vibration	5 G's, 10 Hz to 500 Hz
Seal Leaks	10^{-8} cc/sec in Helium
Solderability	per Mil. std. 202, method 208 (no preconditioning, RMA flux)
Thermal Shock	5 cycles, -55 to 125 °C, 1/2 cycle/hr. in air
Series Resistance	40 Ω (max) at 50 µW power



All measurements are in inches
Package identifier: HC-49

INTRODUCTION

Crystal offers two jitter attenuator circuits. The CS61600 PCM jitter attenuator uses a 16-bit FIFO and a variable oscillator to provide up to 40 dB of jitter reduction in a 1.544 to 2.048 MHz data stream. Also offered is the CS80600, a general purpose high speed (4.5 to 8.5 MHz) jitter attenuator. This part may be used in conjunction with the TMS380 device family to double the number of stations connected to 4 MHz IEEE 802.5 token ring local area network. The CS80600 slows the accumulation of data-dependent jitter, allowing more stations and repeaters to be inserted on the ring without overflowing the elastic buffer of the active system monitor. The input to the CS80600 is clock and data which have been recovered by the TMS38051/52. Jitter is removed by the CS80600 using an 8-Manchester symbol FIFO and a variable oscillator. The dejittered clock and data are then input to the TMS38020.

USER'S GUIDE

Device:	CS61600	CS80600
Data Rates	1.544 MHz or 2.048 MHz	4.5-8.5 MHz
Size of FIFO	16	8
Package	14 pin DIP	14 pin DIP

CONTENTS

Semiconductor Corporation

CS61600

PCM Jitter Attenuator

Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 and PCM-30 Applications
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

The jitter attenuation function can be determined by appropriate specification of the external crystal.

The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

ORDERING INFORMATION
CS61600-IP1 - 14 Pin Plastic DIP; T1 and 2.048 MHz

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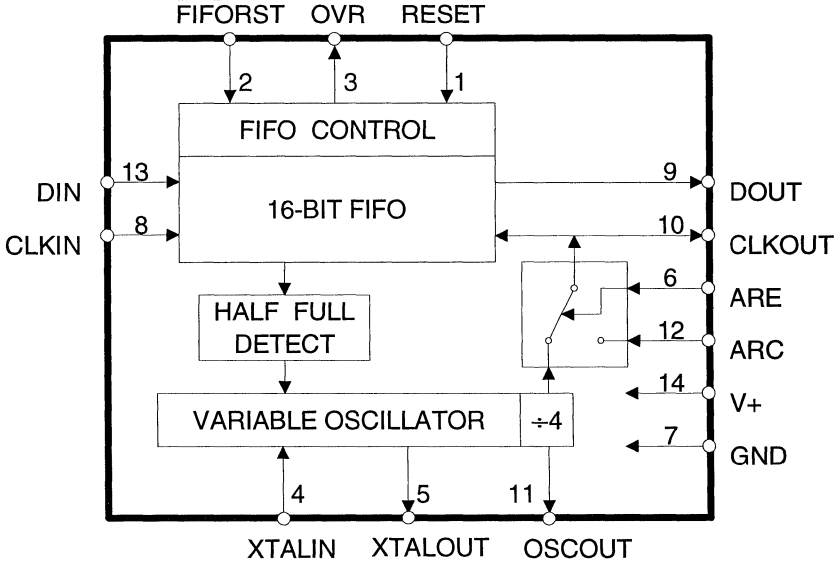


Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	(V+)-GND	-0.3	7.0	V
Input Voltage	V_{in}	GND - 0.3	(V+) + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	(V+)-GND	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	-40	25	85	°C

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5V ±10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 2 and 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 2 and 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10.0	µA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

DIGITAL CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5V ±10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation	P_D	-	50	85	mW
Input Jitter Tolerance		7	-	14*	U.I.

* Depends on accuracy of crystal with respect to CLKIN frequency. See *Applications* section.

SWITCHING CHARACTERISTICS (T_A = -40° to 85° C; V+ = 5V ±10%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter			Symbol	Min	Typ	Max	Units
Crystal Frequency	T1		f_c	-	6.176000	-	MHz
	CCITT	(Note 5)		-	8.192000	-	
CLKIN Frequency	T1		f_{in}	-	1.544	-	MHz
	CCITT	(Note 6)		-	2.048	-	
CLKOUT Frequency	T1		f_{out}	-	1.544	-	MHz
	CCITT	(Note 6)		-	2.048	-	
Clock Pulse Width	T1		t_{pwh}	-	324	-	ns
			t_{pwl}	-	324	-	
	CCITT		t_{pwh}	-	244	-	ns
		(Note 7)	t_{pwl}	-	244	-	
Acceptable CLKIN range		(Note 8)		-	±130	-	ppm
Duty Cycle		(Note 9)		-	50	-	%
Rise Time, All Digital Outputs		(Note 10)	t_r	-	36	100	ns
Fall Time, All Digital Outputs		(Note 10)	t_f	-	17	100	ns
DIN to CLKIN Falling Setup Time			t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time			t_h	50	-	-	ns
CLKOUT Falling to DOUT Propogation Delay			t_{phl}	-	-	200	ns

Note:
5. Crystal should have sufficient pull range when in the oscillator circuit, to meet the system's frequency tolerance requirement over the operating temperature range. See *Applications* section for more information on crystals.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter) over time, CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Crystal must have at least ±130ppm pull range over operating temperature range.
9. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
10. At C_L = 50pF.

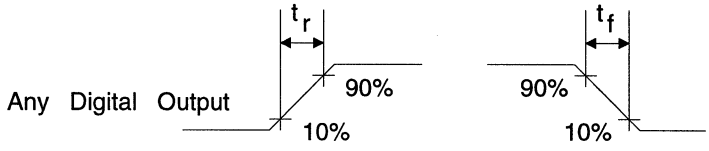


Figure 1. Signal Rise and Fall Characteristics

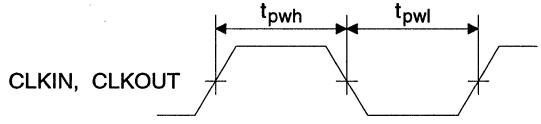


Figure 2. Clock Signal Quality

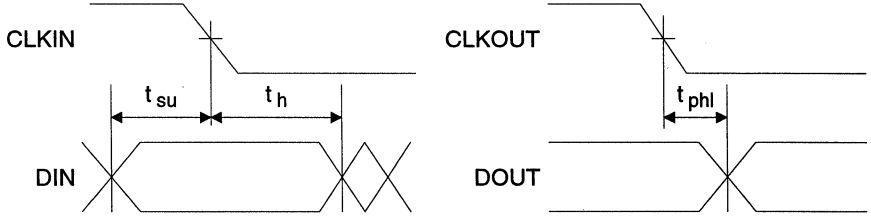


Figure 3. Switching Characteristics

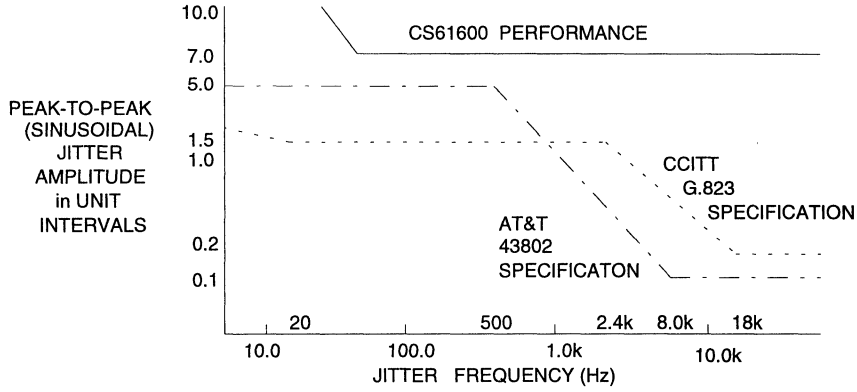


Figure 4. Input Jitter Tolerance

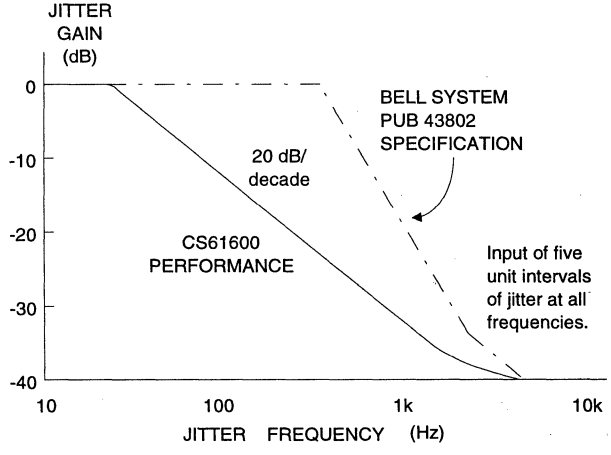


Figure 5. Jitter Attenuation Characteristic

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter from clock and data signals of 1.544 MHz and 2.048 MHz. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS61600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter receives little attenuation. This performance characteristic is shown graphically in Figure 6.

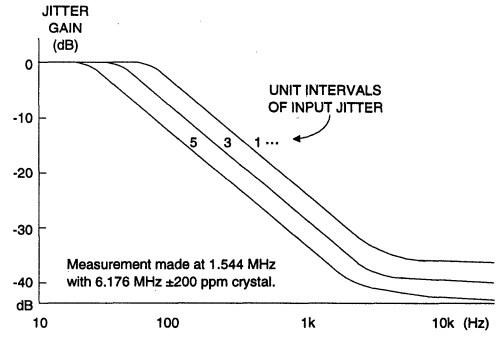


Figure 6. Jitter Attenuation Characteristics

Using the CS61600 in a Slave Configuration

It is possible to use an externally generated clock signal to clock data out of the CS61600. When an external clock is used, a crystal is not necessary. The external clock is input to the Alternate Read Clock input, ARC (pin 12). Holding the Alternate Read Enable pin, ARE (pin 6), high directs the CS61600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS61600 will be prone to underflow or overflow, and data will be lost. See the *Applications* section of this data sheet for more information on the use of an alternate clock.

Oscillator and Crystal

The CS61600 requires an external 6.176000 MHz (8.192000 MHz for CCITT) crystal be connected to pins XTALOUT and XTALIN. The oscillator circuit divides the crystal frequency by four, and switches various capacitive loads to provide a clock that swings in five steps from at least 1.544 MHz - 130 ppm to at least 1.544 MHz + 130 ppm (2.048 MHz - 50 ppm to

2.048 MHz + 50 ppm for CCITT). The crystal oscillator must be able to reach these signal frequency tolerances over the system's operating temperature range. The oscillator adjusts to and holds the average frequency of the signal input to CLKIN.

Some applications specify a narrower frequency tolerance. In these cases, it is possible to improve jitter attenuation performance by specifying a crystal with less pull range. A narrow pull range crystal has the effect of shifting the curves shown in Figure 6 to the left. Care must be taken to ensure that the crystal/oscillator will reach the signal's frequency extremes over the operating temperature range of the system. More information on specifying and testing crystals is provided in the *Applications* section at the back of this data sheet.

FIFO Overflow/Underflow

Because the oscillator clock, which is used to empty the FIFO, has a wider frequency range than the standard T1 input signal, the FIFO should never underflow or overflow. However, if underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an overflow occurs, the 16 bits of data in the FIFO are lost. An underflow condition causes the next 16 bits read from the FIFO to be invalid. In either case, the CS61600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the overflow flag, OVR.

FIFO Reset

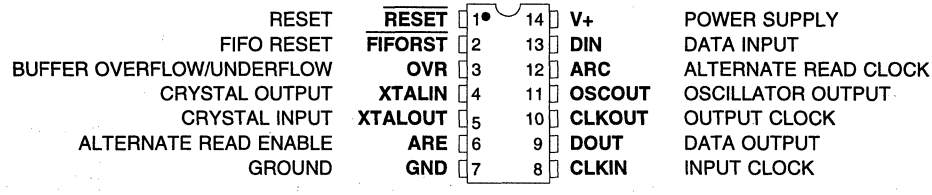
Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS61600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. ***However, the outputs of the CS61600 are undefined if $\overline{\text{FIFORST}}$ is held low for more than 500 ms.*** The FIFO reset function will set the FIFO write and read pointers to the first and eighth locations respectively. The oscillator will continue to run and CLKOUT will be held low.

Power-Up Reset

Upon power up, the CS61600 goes through an initialization procedure which requires approximately 3 ms. During this initialization procedure, OVR is held high. After initialization is complete, OVR goes low. When the clock signal is input to CLKIN, the CS61600 will immediately try to lock onto the clock signal on CLKIN. At this point, the FIFO may overflow, and the $\overline{\text{RESET}}$ pin should be toggled to clear the overflow/underflow flag, OVR.

4

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALIN, XTALOUT - Crystal Input 1, 2; PINS 4, 5.
6.176 MHz or 8.192 MHz crystal inputs. A 200 kohm resistor should be connected across these pins. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss. When $\overline{\text{FIFORST}}$ is low, the OSCOUT output is disabled.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.

Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.

Input data is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.

When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.

Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.

Output data with jitter attenuated. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.

Jitter reduced clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.

Output of on-chip oscillator, divided by four. This pin should be left floating for normal operation.

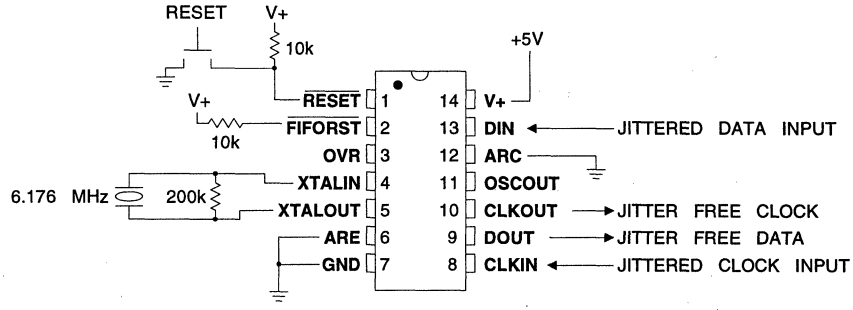


Figure A1. Typical Application Circuit

APPLICATIONS

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61600. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

General Applications

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS61600 will tolerate more jitter; up to 14 unit intervals will be tolerated under optimal conditions.

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 1.544 MHz - 130 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 1.544 MHz + 130 ppm.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS61600. If the center frequency of the oscillator is precisely four times the CLKIN frequency, and the crystal has at least the specified pull range, the CS61600 will tolerate 14 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some T1 applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS61600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A2 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS61600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied to-

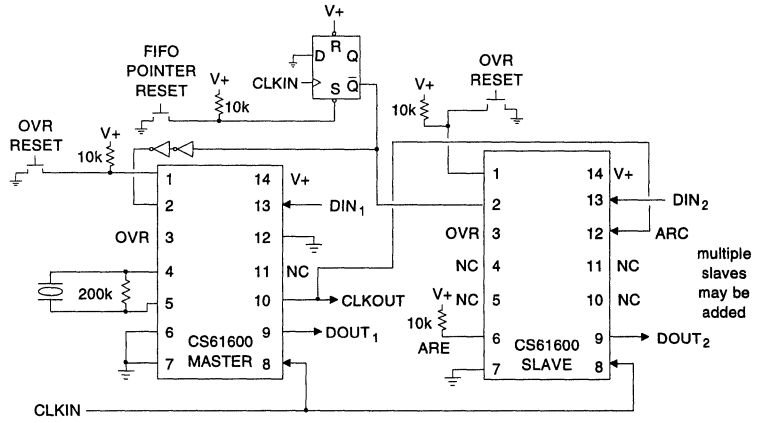


Figure A2. Master / Slave configuration

gether. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS61600 to drive the subsequent CS61600 will induce some propagation delay. These potential timing problems should be considered when cascading CS61600s.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T1 signal clock) goes away. Figure A3 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

Jitter Attenuation at Different Clock Rates

The CS61600 can be used to attenuate jitter at frequencies below 2.048 MHz. For signal frequencies above about 900 kHz, selection of the appropriate crystal will suffice. For jitter attenu-

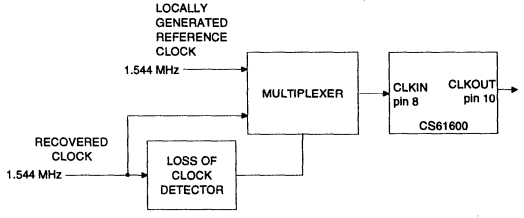


Figure A3. Maintaining Clock Integrity

ation of lower frequency signals, an external divider is required. Figure A4 shows how the CS61600 can be configured for low frequency jitter attenuation.

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 32, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

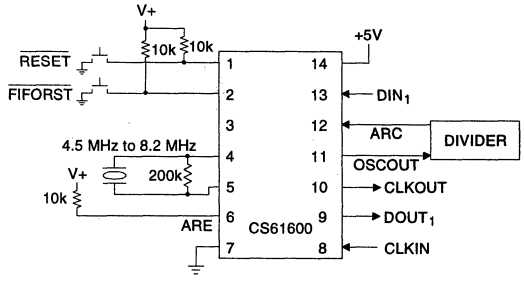


Figure A4. Low Clock Frequency Jitter Attenuation

Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to ±3 data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

Applications

- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators, and in repeators.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexors.

ORDERING INFORMATION

CS80600-CP - 14 Pin Plastic DIP

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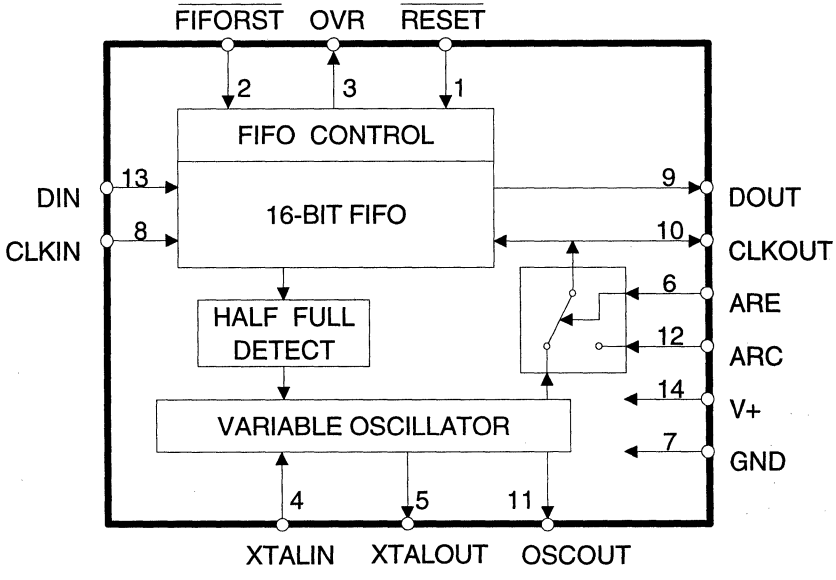

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	(V+)-GND	-	7.0	V
Input Voltage	V_{in}	GND - 0.3	(V+) + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-100	100	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	125	°C

Note: 1. Device can tolerate transients of up to 100mA without latching up.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	0	25	70	°C
Power Dissipation	P_D	20	50	85	mW
Input Jitter Tolerance		3	-	7	U.I.

DIGITAL CHARACTERISTICS (T_A = 0° to 70° C; V+ = 5V ±10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 2 and 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 2 and 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10.0	µA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 0° to 70° C; V+ = 5V ±10%; GND = 0V;

Inputs: Logic 0 = 0V, Logic 1 = V+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 5)	f_c	4.500	-	8.500	MHz
CLKIN Frequency	(Note 6)	f_{in}	-	f_c	-	MHz
CLKOUT Frequency	(Note 6)	f_{out}	-	f_c	-	MHz
Clock Pulse Width	(Note 7)	t_{pwh} t_{pwl}	- -	$1/(2f_c)$ $1/(2f_c)$	- -	ns
Duty Cycle	(Note 8)		-	50	-	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	36	-	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	17	-	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Falling to DOUT Propogation Delay		t_{phl}	-	-	60	ns
$\overline{\text{RESET}}$ Pulse Width			100	-	-	ns
$\overline{\text{FIFOREST}}$ Pulse Width			100	-	-	ns

Note:
5. Crystal must meet specifications described in *Applications* Section of this data sheet.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter), over time CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
9. At maximum load of 1.6mA and 50pF.

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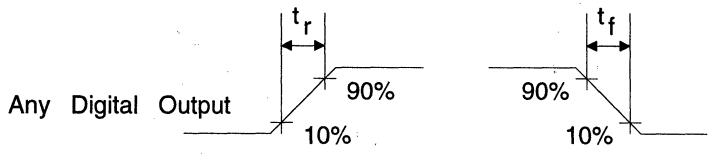


Figure 1. Signal Rise and Fall Characteristics

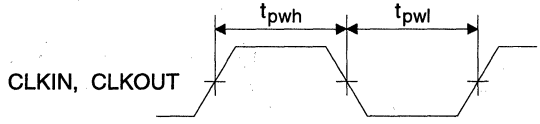


Figure 2. Clock Signal Quality

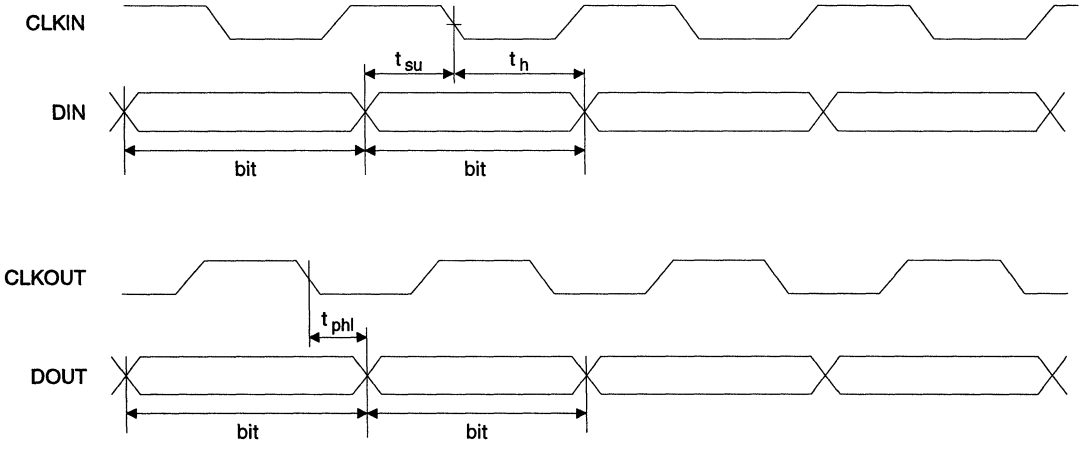


Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS80600 will tolerate and attenuate at least three unit intervals of jitter from a 4.5MHz to 8.5MHz data and clock signal. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS80600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter recieves little attenuation. This performance characteristic is shown graphically in Figure 4.

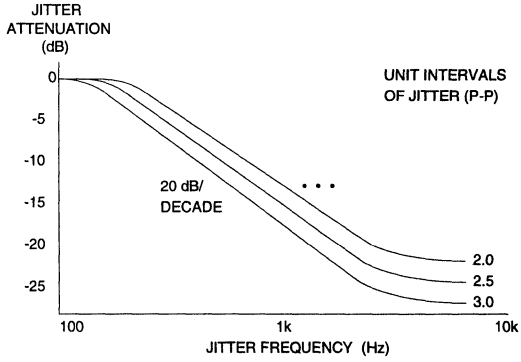


Figure 4 - Jitter Attenuation Characteristics for 8MHz Nominal Frequency

Clock Operation

The CS80600 requires an external crystal. Exacting crystal specifications must be met to ensure proper operation of the curcuit. Information on specifying crystals for the CS80600 is provided in the *Applications* section which appends this data sheet.

It is possible to use an externally generated clock signal to clock data out of the CS80600. The external clock is input to the Alternate Read Clock input, (ARC, pin 12). Holding the Alternate Read Enable pin high (ARE, pin 6), directs the CS80600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS80600 will be prone to underflow or overflow and data will be lost.

FIFO Overflow/Underflow

If underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an

overflow occurs, the eight bits of data in the FIFO are lost. An underflow condition causes the next eight bits read from the FIFO to be invalid. In either case, the CS80600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the OVR flag.

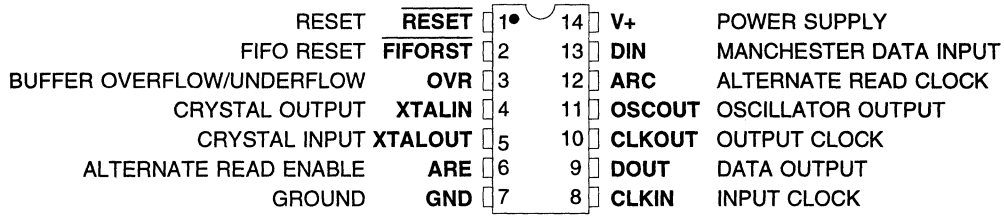
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS80600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. ***However, the outputs of the CS80600 are undefined if FIFORST is held low for more than 500 ms.*** The FIFO reset function will set the FIFO write and read pointers to the first and fourth locations respectively. The oscillator will continue to run and CLKOUT will continue to be output.

Power-Up Reset

Upon power up, the CS80600 goes through an initialization procedure which requires approximately 3 ms. During power-up reset, the overflow pin, OVR, is held high. When initialization is complete, the OVR pin goes low and the CS80600 is ready to lock on to an input clock signal on CLKIN.

PIN DESCRIPTIONS



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Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALIN; XTALOUT - Crystal Input; Crystal Output; PINS 4, 5.
A 20 kΩ resistor should be connected across these pins parallel with the crystal. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.
Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.
Data input is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.
When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.
Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.
Data output with jitter removed. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.
Jitter free clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.
Output of the crystal oscillator.

APPLICATIONS

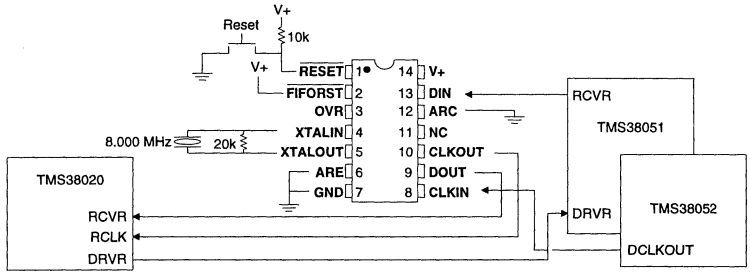

Figure A1. Basic LAN Application suggested for TMS380 Chip Set

Token Ring Operation

The CS80600 can be used, as shown in Figure A1 with the TMS380 Token Ring adaptor chipset in station adaptors, active wiring concentrators and/or repeaters to attenuate jitter that accumulates in a ring. Figure A1 has the effect of masking frequency deviations from the TMS38020 and preventing the "Hardware Error Process" from triggering. In this case, error recovery occurs as the result of higher level procedures.

Figure A2 allows the "Hardware Error Process" to occur. When the CS80600 overflows or underflows, a MUX is used to pass the out-of-frequency clock data around the CS80600 for a fixed number of bits. After those number of bits are passed, the CS80600 is switched back into the circuit. This allows the TMS38020 to observe a wide frequency variation.

Figure A3 shows how the CS80600 can be used to generate a FRAQ signal, thereby allowing the TMS38051/52 PLL to be controlled in a repeater without the use of the TMS38020.

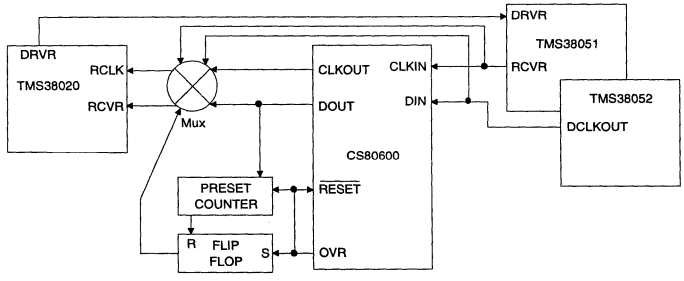

Figure A2. Passing of Frequency Errors

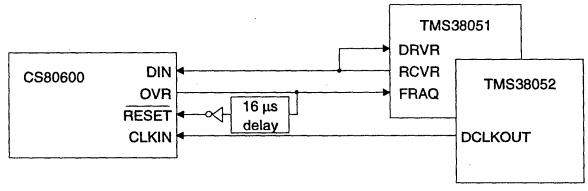

Figure A3. Eliminating TMS38010/20/30 in Repeaters

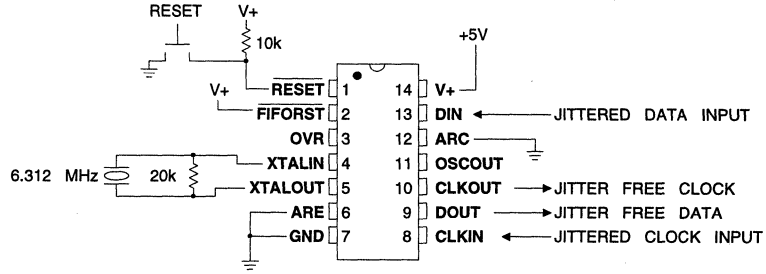

Figure A4. Typical Jitter Attenuation Curcuit

T2 Operation

The CS80600 may be connected as shown in Figure A4 for jitter attenuation in T2 applications.

Selecting an Oscillator Crystal

Figure A5 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS80600. The value of this capacitor is controlled by logic internal to the CS80600. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

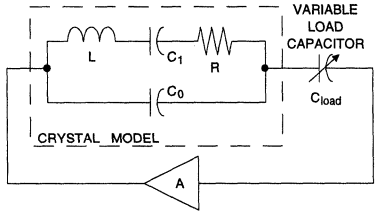

Figure A5. Equivalent Circuit of Oscillator

The important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_0 and C_1. C_1 can be used to control the series resonant frequency of the crystal. The minimum values of C_{load} and C_0 set the parallel resonant frequency. Together, C_1, C_0 and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application.
2) The frequency drift of the crystal over the operating temperature range.
3) The variability in load capacitance from IC to IC.
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_1. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_1 (greater series resonant frequency) results in less pull range, while the larger the C_1 (lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L - C_H)} (C_L + C_H + 2C_0) \quad (C\text{'s in pF}) \qquad (1)$$

f_S = series resonant frequency of crystal
f_N = Nominal Signal Frequency
- should be 8.000000 MHz for LAN
- should be 6.312000 MHz for T2
- should be 8.448000 MHz for CEPT2

Δf = required pull range of crystal in Hz (Δppm x f_N)
C_L = load capacitance for low frequency oscillation (average is ~44.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~9.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1 + C_{load} + C_0}{C_{load} + C_0}\right)^{1/2}$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_0 and C_1 can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

The setup shown in Figure A6 can be used to test crystals. When no CLKIN signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

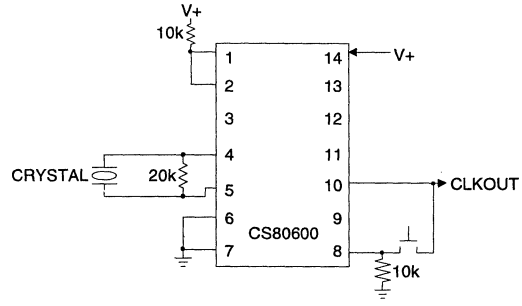

Figure A6. Crystal Pull Range Test

General Applications

The CS80600 will tolerate and attenuate at least three unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS80600 will tolerate more jitter; up to seven unit intervals will be tolerated under optimal conditions.

NOMINAL INPUT SIGNAL FREQUENCY
8.000000 MHz

CRYSTAL FREQUENCY FOR CORRESPONDING LOAD CAPACITANCE

C_L in pf	FREQUENCY TOLERANCE OF INPUT SIGNAL ±100 ppm		
$C_{low\ freq}$ min 41.0	-170 ppm 7998640	$C_{high\ freq}$ max 10.7	+170 ppm 8001360
ASSUMING ±50 ppm TEMPERATURE DRIFT FROM 0° - 70° C			
MAXIMUM ALLOWABLE PULL RANGE: 400 ppm			

Table A1. LAN Crystal Requirements

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 8.000 MHz - 100 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 8.000 MHz + 100 ppm. In either case, the CS80600 will tolerate at least 3 unit intervals of jitter.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS80600. If the center frequency of the oscillator is precisely the CLKIN frequency, and the crystal has at least the specified pull range, the CS80600 will tolerate 7 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS80600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A7 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS80600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO the read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

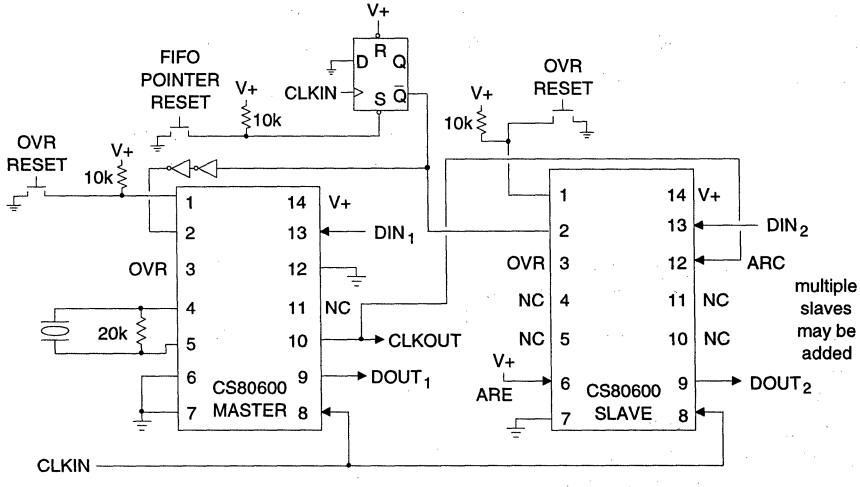

Figure A7. Master/Slave Configuration

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS80600 to drive the subsequent CS80600 will induce some propagation delay. These potential timing problems should be considered when cascading CS80600s.

Creating Phase Coherent Clocks From Two Clock/Data Streams

The master/slave configuration can be used to align two independent clock/data streams as long as the clocks of both signals are at exactly the same average frequency. The schematic shown in Figure A7 is used to implement this application, but CLKIN signals are independent, not tied together. This application will attenuate jitter as long as the jitter input to either device plus the difference in unit intervals between the clock signals does not exceed seven unit intervals. Note that more jitter can be tolerated if the guidelines described at the beginning of this section are followed.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T2 or CEPT2 signal clock) goes away. Figure A8 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

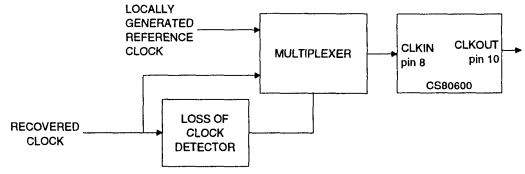

Figure A8. Maintaining Clock Integrity

Jitter Attenuation at Different Clock Rates

The CS80600 can be used to attenuate jitter at frequencies below 4.5 MHz. For signal frequencies above about 4.5 MHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A9 shows how the CS80600 can be configured for low frequency jitter attenuation.

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 128, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

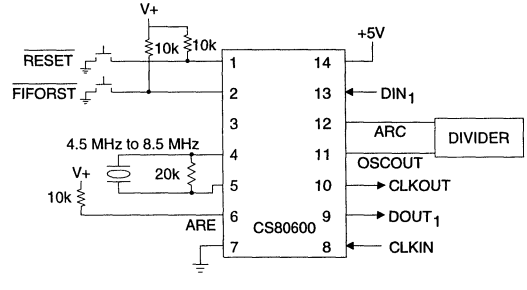

Figure A9. Low Frequency Jitter Attenuation

• Notes •

INTRODUCTION

Crystal's industry-standard CS8870 DTMF receiver exhibits performance which exceeds that of competitive devices. The receiver incorporates filters to guarantee the best possible signal-to-noise ratio. This allows highly accurate decoding of telephone tones into digital outputs.

USER'S GUIDE

Device:	CS8870 DTMF Reciever
Package Size (# pins)	18
Signal Sensitivity	-29 dBm
Dial Tone Tolerance	22 dB
Acceptable Twist	10 dB
Typical Power Consumption	6 mA
Tone pairs Detected	16
Output Format	Hex
Package	18 pin DIP

CONTENTS

Semiconductor Corporation

CS8870

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitvity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870B

General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION
CS8870-IP - 18 Pin Plastic DIP

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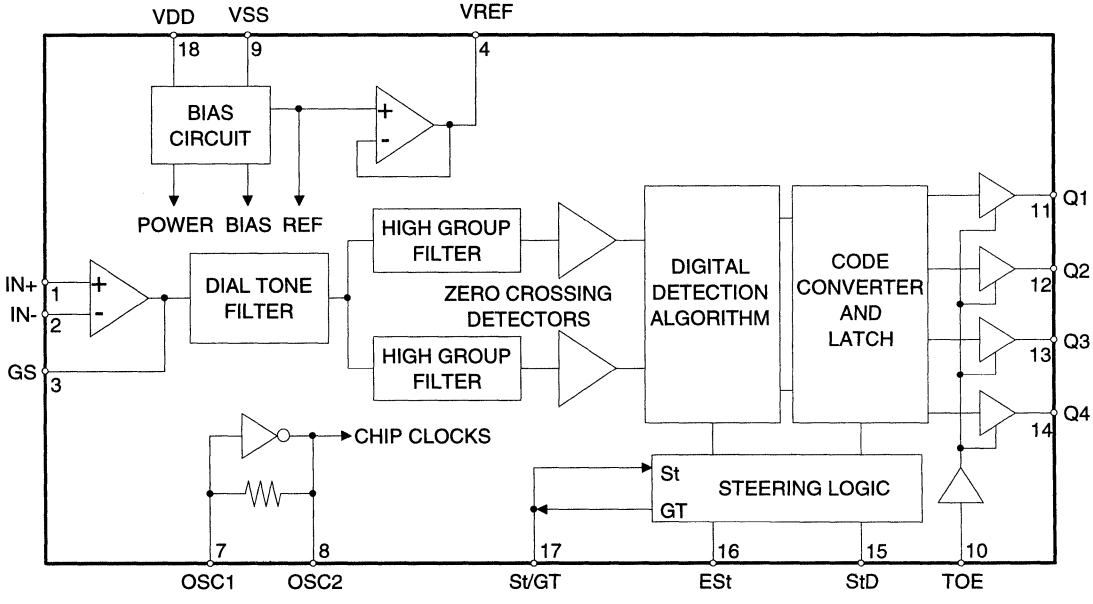

NOT RECOMMENDED FOR NEW DESIGNS

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply		V_{DD}-V_{SS}	-	6.0	V
Input Voltage		V_{in}	V_{SS} - 0.3	V_{DD} + 0.3	V
Input Current, Any Pin	(Note 1)	I_{in}	-	10	mA
Power Dissipation	(Note 2)	P_D	-	1000	mW
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100mA will not cause latch-up.
2. Derate above 75°C at 16 mW/°C; all leads soldered to board.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_{DD}-V_{SS}	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	0	25	70	°C
Crystal Frequency	f_C	3.5759	3.5795	3.5831	MHz

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I_{DD}	-	6.0	10.0	mA
Power Consumption		-	30	45	mW
Input Impedance, pins 1 & 2 (Note 3)	R_{IN}	-	10	-	MΩ
Steering Threshold Voltage	V_{TSt}	2.2	-	2.5	V
Signal Levels for Valid Input (Notes 4, 5, 6, 7, 8, and 9) (each tone of composite signal)		-29 27.5	- -	+1 883	dBm mV_{rms}
Twist (Notes 5, 6, 8, 9, and 10)		-	±10	-	dB
Frequency Detect Bandwidth (Notes 5, 6, 7, and 9)		±1.5%±2Hz	-	±3.5%	
Third Tone Tolerance (Notes 5, 6, 7, 9, 11, and 12)		-	-16	-	dB
Noise Tolerance (Notes 5, 6, 7, 9, 11, 12, and 13)		-	-12	-	dB
Dial Tone Tolerance (Notes 5, 6, 7, 9, 11, 14, and 15)		-	+22	-	dB
Clock Output (OSC 2, pin 8) Capacitive Load		-	-	30	pF
V_{REF} Output Voltage No Load	V_{REF}	2.4	-	2.8	V
V_{REF} Output Resistance	R_{OR}	-	10	-	kΩ

Parameters measured using test circuit shown in Figure 4.

Notes:
3. Input frequency of 1kHz.
4. dBm referenced to power of 1mW into 600Ω load.
5. Digit sequence consists of all 16 DTMF tones.
6. Tone duration of 40ms, tone pause of 40ms.
7. Both tones of the composite signal have equal amplitudes.
8. Tone pair is deviated by ±1.5%±2Hz.
9. For error rate of better than 1 in 10,000.
10. Twist = high tone/low tone.
11. Nominal DTMF frequencies are used.
12. Referenced to lowest frequency component of DTMF signal.
13. Bandwidth limited to 3kHz Gaussian noise.
14. Precise dial tone frequencies of 350Hz±2% and 440Hz±2%.
15. Referenced to minimum valid accept level.

5

ANALOG CHARACTERISTICS - Gain Setting Amplifier

(T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter		Symbol	Min	Typ	Max	Units
Input Leakage Current	(Note 16)	I_{IN}	-	100	-	nA
Input Resistance		R_{IN}	-	10	-	MΩ
Input Offset Voltage		V_{OS}	-	25	-	mV
Common Mode Rejection	(Note 17)	CMRR	-	60	-	dB
Power Supply Rejection	(Note 18)	PSRR	-	60	-	dB
DC Open Loop Voltage Gain		A_{VOL}	-	65	-	dB
Open Loop Unity Gain Bandwidth		f_C	-	1.5	-	MHz
Output Voltage Swing	(Note 19)	V_O	-	4.5	-	V_{p-p}
Tolerable Capacitive Load, GS pin		C_L	-	100	-	pF
Tolerable Resistive Load, GS pin		R_L	-	50	-	kΩ
Common Mode Range	(Note 20)	V_{CM}	-	3.0	-	V_{p-p}

Notes: 16. $V_{SS} \le V_{IN} \le V_{DD}$
17. $-3.0V \le V_{IN} \le +3.0V$
18. At 1kHz
19. $R_L \ge 100k\Omega$ to V_{SS}
20. Unloaded

SWITCHING CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter			Symbol	Min	Typ	Max	Units
Tone Present Detection Time			t_{DP}	5	11	14	ms
Tone Absent Detection Time			t_{DA}	0.5	4	8.5	ms
Tone Duration Accept		(Note 21)	t_{REC}	-	-	40	ms
Tone Duration Reject		(Note 21)	$\overline{t_{REC}}$	20	-	-	ms
Interdigit Pause Accept		(Note 21)	t_{ID}	-	-	40	ms
Interdigit Pause Reject		(Note 21)	t_{DO}	20	-	-	ms
Propagation Delay (St to Q)		(Note 22)	t_{PQ}	-	8	11	µs
Propagation Delay (St to StD)		(Note 22)	t_{PStD}	-	12	-	µs
Output Data Set Up (Q to StD)		(Note 22)	t_{QStD}	-	3.4	-	µs
Propagation Delay (TOE to Q)	ENABLE	(Note 23)	t_{PTE}	-	50	-	ns
	DISABLE	(Note 23)	t_{PTD}	-	300	-	ns
Clock Input Rise Time			t_{LHCL}	-	-	110	ns
Clock Input Fall Time			t_{HLCL}	-	-	110	ns
Clock Input Duty Cycle			DC_{CL}	40	50	60	%

Parameters measured using test circuit shown in Figure 4.

Notes: 21. User adjustable; see *General Description* on page 5-9.
22. TOE = V_{DD}
23. R_L = 10kΩ, C_L = 50pF

DIGITAL CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter			Symbol	Min	Typ	Max	Units
Digital Inputs	"0" level		V_{IL}	-	-	1.5	V
	"1" level		V_{IH}	3.5	-	-	V
Digital Outputs	"0" level	(Note 24)	V_{OL}	-	-	0.03	V
	"1" level	(Note 24)	V_{OH}	4.97	-	-	V
Output Low (Sink) Current		(Note 25)	I_{OL}	1	2.5	-	mA
Output High (Source) Current		(Note 26)	I_{OH}	0.4	0.8	-	mA
Input Leakage Current		(Note 27)	I_{IH}, I_{IL}	-	0.1	-	µA
Pull Up Source Current		(Note 28)	I_{SO}	-	7.5	15	µA

Notes: 24. No Load
25. V_{OUT} = 0.4V
26. V_{OUT} = 4.6V
27. V_{IN} = V_{SS} or V_{DD}
28. TOE (pin 10) = 0V

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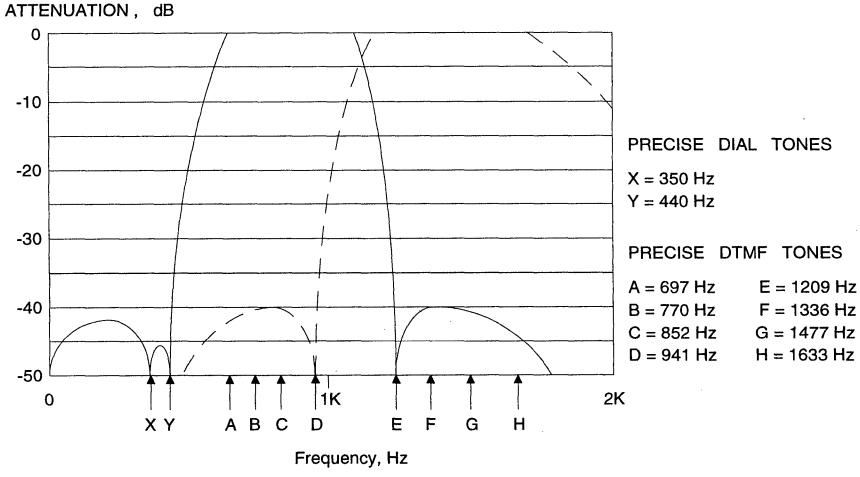
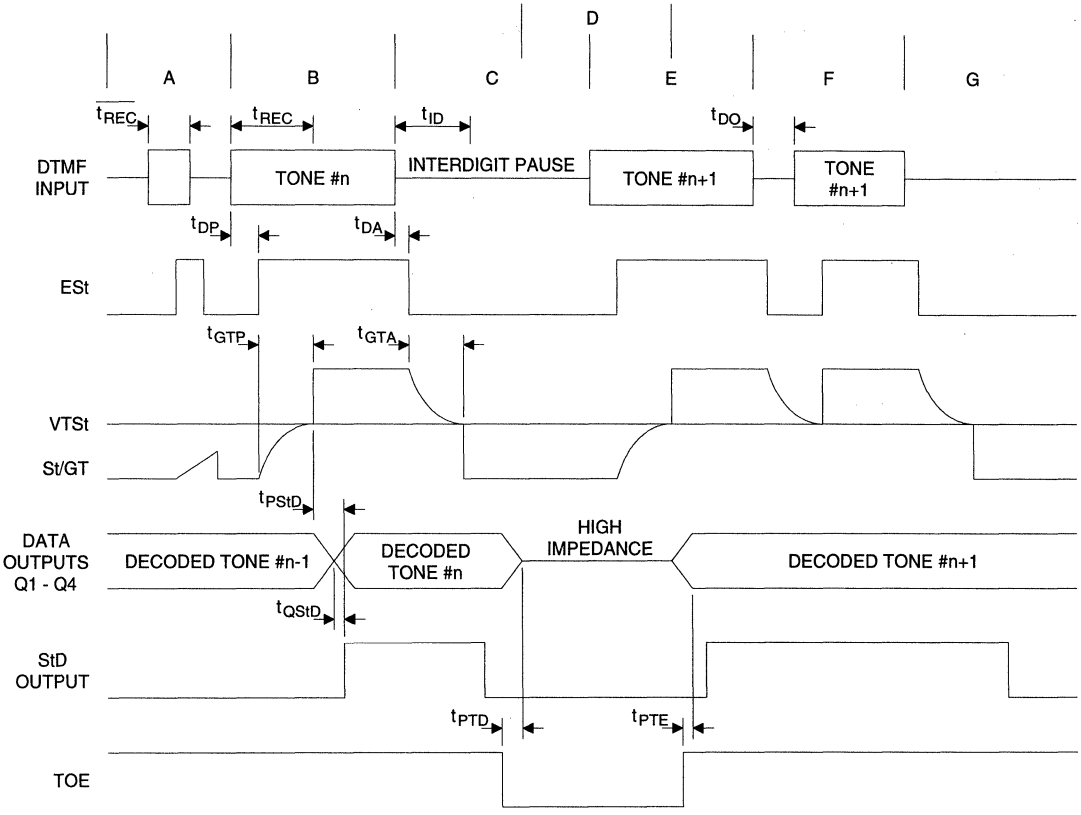


Figure 1. Filter Characteristics



EXPLANATION OF EVENTS

A. Short tone burst is detected, but duration is invalid.
B. Tone #n is detected, and duration is valid. Decoded to outputs.
C. End of tone #n detected and duration is valid. Outputs remain latched until next valid tone.
D. Three state outputs are disabled (high impedance).
E. Tone #n+1 is detected and validated. Decoded to outputs.
F. Three state outputs are enabled. Momentary dropout of tone #n+1 does not register at outputs.
G. End of tone #n+1 detected and validated. Outputs remain latched until next valid tone.

DEFINITION OF SYMBOLS

ESt - EARLY STEERING OUTPUT - Indicates detection of valid DTMF signal.
St/GT - STEERING INPUT/GUARD TIME OUTPUT - Drives external timing circuit.
Q1 - Q4 - DATA OUTPUTS - Gives code corresponding to decoded tone pair.
StD - DELAYED STEERING OUTPUT - Indicates that valid signals have been present (or absent) for the required time.
TOE - TONE OUTPUT ENABLE (Input) - Holding TOE low causes Q1 - Q4 to go to high impedance state.

$\overline{t_{REC}}$ - DTMF singal duration too short to be detected as valid.
t_{REC} - Minimum signal duration required for valid recognition.
t_{ID} - Minimum acceptable time between valid signals.
t_{DO} - Maximum allowable dropout of DTMF signal.
t_{PTD} - Propagation Delay, Disable
t_{PTE} - Propagation Delay, Enable
t_{DP} - Time to detect presence of valid signal.
t_{DA} - Time to detect absence of valid signal.
t_{GTP} - Tone Present Guard Time
t_{GTA} - Tone Absent Guard Time
t_{QStD} - Output Data Setup (Q to StD)
t_{PStD} - Propagation Delay (St to StD)

GENERAL DESCRIPTION

The CS8870 is a complete Dual Tone Multifrequency (DTMF) receiver designed to detect all 16 tone pairs and output a corresponding four bit binary code. This device provides all necessary filtering and requires a minimum of external components. Low power CMOS technology provides the highest performance for the lowest cost.

Filter Section

The CS8870's on chip filtering provides excellent signal-to-noise performance. The DTMF signal is separated into high and low groups using two six pole, bandpass switched capacitor filters. The bandpass filters are elliptical designs with notches placed at 350 Hz and 440 Hz for exceptional dial tone rejection. The output of each bandpass filter contains frequency components from only one DTMF tone group. The filter outputs are smoothed and then limited by high gain comparators, which have hysteresis to reduce sensitivity to unwanted low level signals, jitter, and noise. The comparators' outputs swing from rail to rail at the frequencies of the incoming tones.

Decoder Section

The decoder uses a digital detection algorithm to determine the frequencies of the two tones. The decoder measures the period of the square wave output of the comparators. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four possible tones in either band. This averaging prevents DTMF simulation by extraneous signals such as voice, while allowing small frequency deviations in the signal. The averaging algorithm has been optimized to provide excellent immunity to "talk-off" and tolerance to the presence of interfering frequencies (third tones) and noise. When both bands simultaneously decode a valid tone, the Early Steering (ESt) output goes high. Should the DTMF signal be lost, the ESt pin will go low.

Steering Circuit

The receiver verifies that the duration of a valid signal is sufficient before registering a decoded tone pair. Tone detection timing is controlled by an external resistor and capacitor (see Figure 2). After a valid tone is present for t_{DP} (Tone Present Detection Time), ESt goes high, and the capacitor discharges through resistor R. The voltage on the St/GT pin changes as a function of the RC time constant, providing the DTMF signal remains valid. When the capacitor voltage (and the voltage on St/GT) reaches the Steering Threshold Voltage, V_{TSt}, the GT output drives the capacitor voltage to VDD. At this point, the four bit code corresponding to the DTMF signal is latched to the outputs. GT remains high as long as ESt remains high. After the output latches settle, the Delayed Steering Output, StD, goes high, indicating that a valid tone pair has been registered. The code is made available at outputs Q1 - Q4 by pulling the three state control input, TOE, to a logic high.

The steering circuit works in reverse to sense the interdigit pause between signals. When the DTMF signal is removed, the capacitor charges. When the Steering Threshold Voltage is reached, GT is pulled to V_{SS}. This circuit also enables the receiver to tolerate signal dropouts too short to be considered a valid pause.

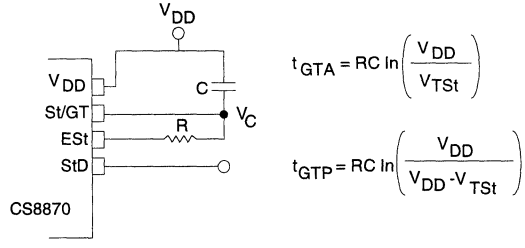


Figure 2 - Basic Steering Circuit

Guard Time Adjustment

The external timing circuitry shown in Figures 2 and 3, enables the user to adjust the timing to meet specific needs. The following formulas, along with the formulas given in Figure 2, are used to determine the resistor and capacitor values.

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

t_{REC} is the minimum signal duration accepted by the receiver. t_{DP} is the Tone Present Detection Time (the time a valid tone must be present before ESt goes high). t_{ID} is the Interdigit Pause Time. t_{DA} is the Tone Absent Detection Time. Values for t_{DP} and t_{DA} are given in the Switching Characteristics Table. Using the configuration shown in Figure 2, and the recommended capacitor value of 0.1µF, a t_{REC} of 40ms is achieved by using a 390kΩ resistor.

Different circuit configurations may be used to independently select Tone Present Guard Time, t_{GTP}, and Tone Absent Guard Time, t_{GTA}, durations. Using the equations and circuits shown in Figure 3, the designer can meet system specifications which place limits on accept and reject times for tone and pause durations, and tailor system parameters such as "talk-off" and noise immunity. For example, increasing recognition time improves talk-off performance (speech immunity) since it reduces the probability that tones simulated by speech remain valid long enough to register.

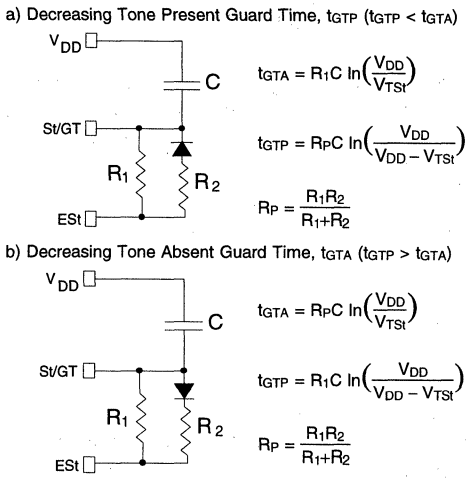


Figure 3 - Steering Circuits for Guard Time Adjustment

Input Configuration

Input signals to the CS8870 pass through an on-chip operational amplifier. A voltage reference, VREF, is provided to bias the input near mid-supply. Figure 4 shows a single ended input configuration with the inputs biased at VREF, and for unity gain. A differential input configuration is shown in Figure 5. The feedback resistor, R5, connected to the op-amp output, GS, can be used to control the gain.

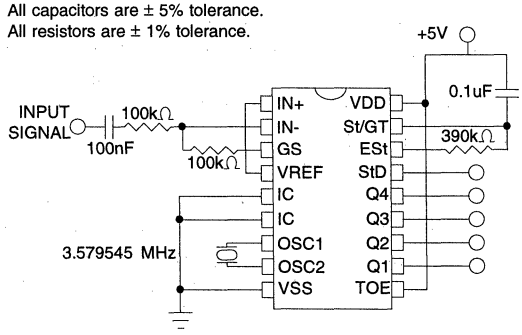
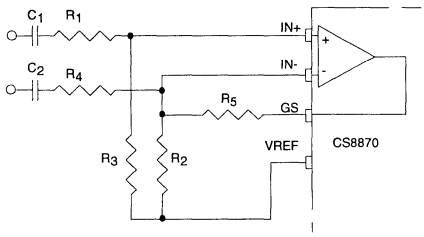


Figure 4 - Single Ended Input Configuration



$C_1 = C_2 = 0\ .01\mu F$
$R_1 = R_4 = R_5 = 100k\Omega$
$R_2 = 60k\Omega$
$R_3 = 37.5k\Omega$

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{Voltage Gain (Av diff)} = \frac{R_5}{R_1}$$

$$\text{Input Impedance } (Z_{IN} \text{ diff}) = 2\sqrt{R_1 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 5 - Differential Input Configuration

F_{LOW}	F_{HIGH}	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L - LOGIC LOW H - LOGIC HIGH
Z - HIGH IMPEDANCE

Table 1 - Functional Decoding

Crystal Oscillator

An external 3.579545 MHz (TV colorburst) crystal must be connected across pins OSC1 and OSC2 to complete the internal clock circuit. Up to ten CS8870s may be driven by one crystal by connecting the oscillator output, OSC2, with the oscillator input, OSC1, of another device through a 30pf capacitor. Refer to Figure 6.

Logic high on TOE enables the data output pins to output code for the last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See the Functional Decode table, Table 1.

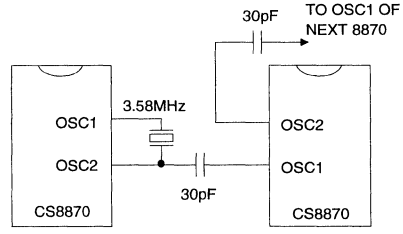


Figure 6 - Oscillator Interconnection

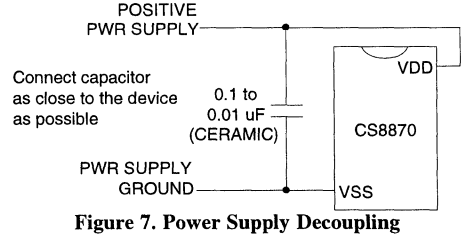
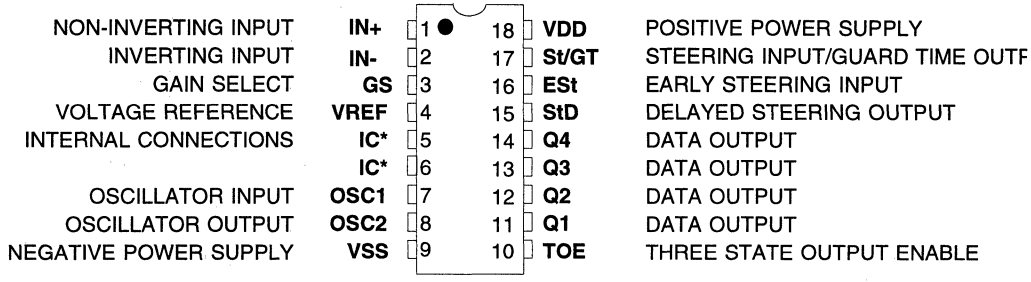


Figure 7. Power Supply Decoupling

PIN DESCRIPTIONS



*Connect to V_{SS}

Power Supplies

VDD - Positive Power Supply Input, PIN 18.

Normally connected to +5 volts. A 0.01µF to 0.1µF ceramic capacitor should be connected as close to the device as possible across V_{DD} and V_{SS}. (See Figure 7).

VSS - Negative Power Supply Input, PIN 9.

Normally connected to 0 volts.

Oscillator

OSC1; OSC2 - Oscillator Input, PIN 7; Oscillator Output, PIN 8.

A 3.579545 MHz crystal connected across these pins completes the internal clock circuit.

Inputs

St/GT - Steering Input/Guard Time Output, PIN 17.

When the voltage on this pin rises past the Steering Threshold Voltage, V_{TSt}, the device registers the detected tone pair, updates the output latch, and drives this pin to a logic high. When the voltage on this pin falls below V_{TSt}, this pin goes to a logic low, freeing the device to accept a new tone pair. The Guard Time Output's function is to reset the external steering time constant. The state of GT is a function of ESt and St.

IN+ - Non-Inverting Input, PIN 1.

Non-inverting input to the front end operational amplifier.

IN- - Inverting Input, PIN 2.

Inverting input to the front end operational amplifier.

TOE - Three State Output Enable, PIN 10.
Logic high on this pin enables outputs Q1 - Q4. Internal pull up.

Outputs

GS - Gain Select, PIN 3.
Connected to the output of the front end operational amplifier. Gain applied to the input can be controlled by a feedback resistor at this pin.

VREF - Voltage Reference, PIN 4.
Voltage on this pin is nominally 2.5 VDC independent of power supply, and may be used to bias inputs at mid supply.

Q1, Q2, Q3, Q4 - Data Outputs, PINS 11, 12, 13, 14.
Logic high on TOE enables pins to output code for last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See Functional Decode Table.

StD - Delayed Steering Output, PIN 15.
Outputs a logic high when voltage on St/GT exceeds V_{TSt} and the output latch has been updated with code from the received tone pair. StD goes to a logic low when voltage on St/GT falls below V_{TSt}.

ESt - Early Steering Output, PIN 16.
Goes to a logic high whenever the detection algorithm detects a valid tone pair. Any loss of a valid DTMF signal causes the output to go to a logic low

IC, IC - Internal Connection, PINS 5, 6.
Both pins must be tied to V_{SS}.

• Notes •

CS6400 Echo Canceling Codec

The CS6400 is a low-cost voiceband echo cancellation product with integrated codec and program ROM. The CS6400 which can be used in full-duplex speakerphones, cellular phones, base stations, personal digital assistants, video-teleconferening and long-distance telephone lines. This circuit contains an embedded, low-cost, application-specific DSP, and can cancel up to 64 ms of acoustic or network echo.

CS6401 Programmable Echo Canceller

The CS6401 is a general-purpose voiceband echo cancellation product. This circuit contains an embedded, low-cost, application-specific DSP, and can cancel up to 64 ms of acoustic or network echo. The program code is loaded from an external ROM, allowing Crystal to tailor functionality for specific applications.

CWECAXB Executable code for the CS6401

Contains the program code which is loaded into the CS6401 at CS6401 power-up.

Introduction: Custom Communication Codecs

Crystal Semiconductor offers a broad variety of technology for processing voiceband and radio baseband signals. The CS645x series of products are representative of Crystal's ability to apply its delta-sigma converter technology to specific communication applications. Crystal will develop custom codec circuits for high-volume applications.

CS6450 I&Q Baseband Codec for IS-54

The CS6450 supports CDPD and TDMA cellular phones, and provides a baseband interface between a DSP and a radio module.

CS6453 Alternate Voice/data Codec

The CS6453 supports high-performance modems, and provides a voiceband interface between a DSP and a direct access arrangement.

CONTENTS

Semiconductor Corporation

CS6400

Echo-Cancelling Codec

Features

- Applicable in:
  - Digital-Cellular Hands-Free Phones
  - Analog-Cellular Hands-Free Phones
  - Office Speaker Phones
  - Desktop & Video Teleconferencing
  - Network/Base Stations
- Echo Cancellation
  - Up to 60 dB ERLE
  - 512 Tap (64 ms at 8 kHz Fs)
  - Split Mode For Two ECs
  - Cascadable For Longer Response
- Zero-Glue Serial Data/Control Interface
- On-Chip Codec
  - < 1% THD, 8Ω Load On Output
  - > 70 dB S/(N+D) on Input
  - 0-3600 Hz Bandwidth at 8 kHz Fs
  - 0-7200 Hz Bandwidth at 16 kHz Fs

General Description

The CS6400 is an application-specific digital signal processor optimized for acoustic echo and noise cancellation applications. A high-quality codec is integrated with the processor to provide a complete, low-cost echo-cancellation solution.

The CS6400 is a fully independent processor that requires no signal processing support to implement its cancellation functions. Volume control, mute, and sleep functions are also provided.

The on-chip A/D and D/A converters employ over-sampling technology, which eliminates the need for complex external anti-aliasing and reconstruction filters, further reducing system cost.

The CS6400 has a zero glue-logic serial interface that is compatible with most DSPs. Clock and sync lines control the transfer of serial data via the separate serial data-in and data-out pins. Both 15-bit audio data and control/status information may be multiplexed on this serial channel using a steering bit.

ORDERING INFORMATION

CS6400-IQ	-40 to +85 °C	44-pin TQFP
CDB6400	Evaluation Board	

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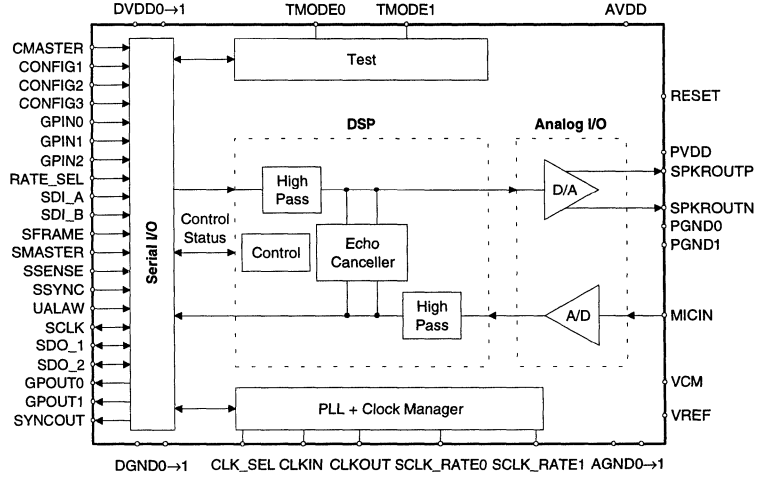

Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ADC CHARACTERISTICS (T_A = 25 °C; All DVDD, AVDD, and PVDD = 5.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = DVDD; Signal test frequency 1kHz, word rate (Fs) = 8kHz, audio signal measurement bandwidth is 20Hz to 20kHz; Microphone amp gain = 0dB; SPRKOUT outputs connected to 8Ω load; CLKIN frequency = 2.048MHz; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
ADC Resolution With No Missing Codes		12			bits
Instantaneous Dynamic Range	IDR	70	72		dB
Total Harmonic Distortion at -0.5dBFS signal level	THD	0.03			%
Gain Drift			150		ppm/°C
Offset Error			25	50	LSB
Full Scale Input Voltage (Note 1)		0.9	1.0	1.1	V_p
Input Resistance (at MICIN)		25			kΩ
Input Capacitance (at MICIN)			15		pF
Inter-Section Isolation, DAC to ADC			75		dB
Sample Rate	Fs			16	kHz
Microphone Amp Gain (switchable on/off)			+26		dB
Anti-aliasing Rejection			30		dB
Power Supply Rejection (1kHz)	PSR		40		dB
Frequency Response		-0.6		0.6	dB
Transition Band		0.45		0.6	Fs
Stop Band Rejection		70			dB
VREF Reference Voltage Output			2.0		V
VCM Voltage Output constant load only, >100 kΩ			1.0		V
Group Delay (Note 2)			8/Fs		s
Group Delay Variations vs. Frequency (Note 2)			0.0		µs

Notes:
1. This is the peak input voltage (in volts) with the mic amp gain set to 0 dB. Peak-to-peak voltage is 2x peak. Input signals will be properly clipped if the peak signal is greater than full scale, but less than 2x full scale.
2. This group-delay specification is for the ADC only; additional group delay may be introduced by the high-pass filter that is implemented on the CS6400 in software.

DAC CHARACTERISTICS (T_A = 25 °C; All DVDD, AVDD, and PVDD = 5.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = DVDD; Signal test frequency 1kHz, word rate (Fs) = 8kHz, audio signal measurement bandwidth is 20Hz to 20kHz; Microphone amp gain = 0dB; SPRKOUT outputs connected to 8Ω load; CLKIN frequency = 2.048MHz; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
DAC Resolution		12			bits
DAC step size error				±0.5	LSB
Instantaneous Dynamic Range	IDR	70	72		dB
Frequency Response		-0.8		+0.6	dB
Programmable Output Level Attenuator Range (Note 3)		-92.2		0	dB
Gain Step Size			2.49		dB
Gain Drift			150		ppm/°C
VREF Reference Output Voltage			2.0		V
VCM Output Voltage constant load only, >100kΩ			1.0		V
Offset Error			25	50	mV
Full Scale Output Voltage (SPKROUT pins) (Note 4)		1.58	1.75	1.93	V_p
Common Mode Output Voltage (SPKROUT pins)			1.35		V
Total Harmonic Distortion at -0.5dBFS level, SPKROUT	THD			0.8	%
Output Impedance SPKROUT pins			0.1		Ω
Load Impedance SPKROUT pins		8			Ω
Short Circuit Current Limit SPKROUT pins (Note 5)				500	mA
Output Capacitance			15		pF
Audible Stop Band Attenuation (<20kHz)		68			dB
Integrated Inaudible Energy (>20kHz) (Note 6)				30	mVrms
Audible Noise with Fs = 8kHz (<20kHz)			-70		dB
Power Supply Rejection (1kHz)	PSR		40		dB
Inter-Section Isolation, ADC to DAC			75		dB
Filter Transition Band		0.45		0.6	Fs
Group Delay (Note 7)			8/Fs		s

Notes:
3. Attenuation settings greater than 92.2 dB will cause a full scale input signal to be completely attenuated to zero signal level.
4. This is the peak differential output voltage. The peak-to-peak signal level on each output pin is equal to the peak differential value.
5. SPKROUTP or SPKROUTN shorted to ground.
6. Assuming an external 43.2 kHz RC output filter.
7. This group-delay specification is for the DAC only; additional group delay may be introduced by the high-pass filter that is implemented on the CS6400 in software.

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PHASE-LOCKED LOOP CHARACTERISTICS (T_A = 25°C; AVDD, DVDD, and PVDD = +5V; Input Levels: Logic 0 = 0V, Logic 1 = DVDD)

Parameter	Symbol	Min	Typ	Max	Units
PLL acquisition time				1	ms
PLL frequency range		22.12	24.58	27.03	MHz
PLL jitter			200		ps rms
Input ref frequency		1.84	2.048	2.25	MHz

DIGITAL CHARACTERISTICS (T_A = 25°C; AVDD, DVDD, and PVDD = 5V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	VD - 1.0			V
Low-level Input Voltage	V_{IL}			1.0	V
High-level Output Voltage at I_O = -2.0 mA	V_{OH}	VD - 0.3			V
Low-level Output Voltage at I_O = +2.0 mA	V_{OL}			0.1	V
Input Leakage Current (Digital Inputs)				10	µA
Output Leakage Current (High-Z Digital Outputs)				10	µA
Output Capacitance	C_{OUT}			15	pF
Input Capacitance	C_{IN}			15	pF

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies		-0.3		6.0	V
Input Current Except Supply Pins & Driver Pins		-		±10.0	mA
Analog Input Voltage		-0.3		VA + 0.3	V
Digital Input Voltage		-0.3		VD + 0.3	V
Ambient Temperature (Power Applied)		-55		125	°C
Storage Temperature		-65		150	°C
ESD using human body model (100pF with series 1.5kΩ)		2000		-	V

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

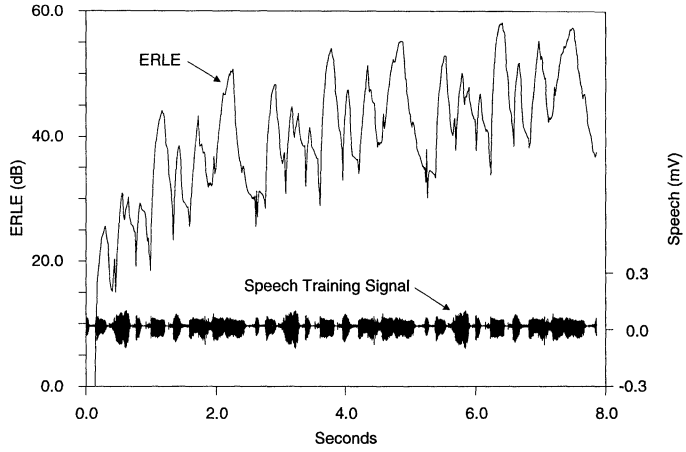


Figure 1. Typical ERLE Convergence Characteristics

Echo Canceller Characteristics

The typical Echo Return-Loss Enhancement (ERLE) convergence characteristics for the CS6400 are illustrated in the above diagram under the following conditions:

- Echo-canceller length: 512 taps
- Echo-canceller initial conditions: zeroed filter taps, updates disabled until t=0.125s
- Sampling rate: 8 kHz
- Echo path (including microphone, speaker, and amplifiers):
  - spectrally flat
  - linear
  - duration < 64 ms
  - noise free
  - time invariant
- Near-end high-pass filter: enabled
- Pre-emphasis filter: enabled
- Graded-beta profile: 64 echo-canceller filter taps processed per 2x reduction in update gain
- Training signal: speech, full scale
- Unlimited S/(N+D) on linear A/D

Note: Many of these conditions may be significantly different in real applications, resulting in significantly different measured ERLE performance.

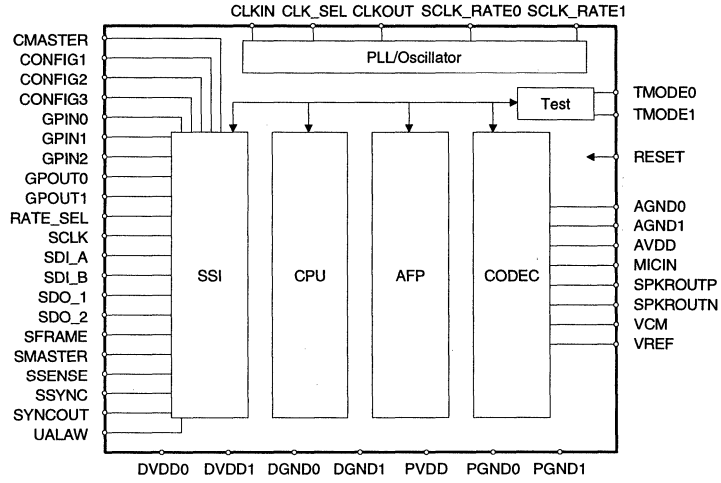


Figure 2. CS6400 Internal Block Diagram

OVERVIEW

In hands-free speakerphones, the signal from the far end may echo about the near-end environment and then be received at the near-end microphone. When heard at the far end, this echo signal can be very annoying, particularly if the signal is delayed by transmission or signal-processing delays.

Voice switching is a particularly simple technique for eliminating this echo, but since it requires half-duplex communication, it seriously compromises conversation quality.

Echo cancellation can provide high-quality, full-duplex communication, but typically must be implemented using expensive digital signal-processing hardware.

Echo Cancellation in the CS6400

The CS6400 provides high-quality echo cancellation at low cost. This breakthrough in cost/performance is made possible on the CS6400 by custom, application-optimized processing blocks, which are integrated on a single die, as shown in Figure 2.

One of these processing blocks is the AFP (Adaptive Filter Processor). This block implements a 512-tap AFIR (Adaptive Finite Impulse-Response) filter which is updated using an enhanced least-mean squared (LMS) algorithm. At a sampling rate of 8 kHz, it can cancel up to 64 ms of echo. In some operating modes, some of the available 64 ms may be allocated to a network canceller (NEC), or the available 64 ms may be split to provide two independent echo-cancellation channels.

Another processing block is the CPU. This block facilitates other processing, like update control. This processing has a critical influence on overall echo-cancellation performance. Double-talk detection is a particularly important part of this processing. Double-talk detection and other algorithms were carefully developed and validated at Crystal under real-world conditions.

To increase the CS6400's echo return-loss enhancement (ERLE), optional echo suppression may be enabled to supplement echo cancellation. To assure the highest-quality conversation, a sophisticated voice-detection algorithm is used to provide graduated, soft-switching echo suppression.

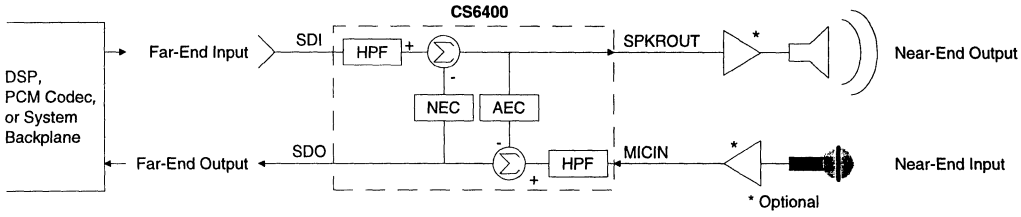


Figure 3. Functional Diagram

As shown in Figure 3, a high-pass filter is provided at the far-end and near-end inputs to remove low-frequency noise that is typically present, for example, in a car environment.

Analog Interface

Another processing block is the codec block. This block provides an A/D and a D/A converter that can be connected directly to a microphone and a speaker, respectively.

The output of the microphone is low-pass filtered, then AC-coupled to the audio input, MICIN. A 26 dB gain stage is included in the CS6400 at the A/D input to amplify the microphone signal. However, this gain stage is bypassed in modes in which a line-level source is connected to the CS6400 instead of a microphone. The CS6400 also includes a speaker driver, which can drive an 8Ω speaker directly, or alternatively, it can drive a high-impedance differential input on an external amplifier.

Both the D/A and A/D paths are bandlimited as a function of sampling rate. At a sampling rate of 8 kHz, the paths are limited to 0-3600 Hz. S/(N+D) is greater than 70 dB for a 20 kHz and 4 kHz bandwidth for the D/A and A/D converter, respectively. For applications that require higher-quality audio, the sampling rate for the codec can be doubled to 16 kHz, increasing the codec bandwidth to 0-7200 Hz. At a 16 kHz sampling rate, however, a CS6400 can compensate for only 32 ms of echo. To extend the echo response back to 64 ms, two CS6400s can be cascaded.

Synchronous Serial Interface

Another processing block is the Synchronous Serial Interface (SSI). This block provides a data and control interface to the CS6400. The SSI can connect to an external codec, DSP, to backplane network, or to another CS6400.

The SSI can be connected to an external network codec (like the MC145503) for applications like speakerphones. The SSI can be connected to a DSP for high-end applications like video teleconferencing. For network applications, the SSI can connect to a network backplane and a TSAC (Time-Slot Assigner Chip).

The CS6400 can operate as either a system-timing master, or as a system-timing slave. When the CS6400 is a system-timing master, timing is generated by a crystal oscillator on the CS6400. When the CS6400 is a system-timing slave (i.e., when the CS6400 is connected to a DSP), timing is generated by an internal PLL (Phase-Locked Loop) on the CS6400, using the SCLK input as a timing reference.

The crystal oscillator will operate only at 2.048 MHz, but the PLL can operate at 256 kHz, 384 kHz, 1.024 MHz, or 2.048 MHz. As a result, when the CS6400 is a timing master, the SCLK will operate only at 2.048 MHz, but can operate at any of the above frequencies when it is a timing slave.

Configuration			CMASTER	SFRAME	SMASTER	CONFIG3	CONFIG2	CONFIG1
Mode 1:	Interface to CODEC (CODEC⇔CS6400)							
Application:	Low-cost speaker phone							
1.1:	Short-Frame Mode		0	0	1	0	0	1
1.2:	Long-Frame Mode		0	1	1	0	0	1
Mode 2:	Interface to DSP (DSP⇔CS6400)		0	0	0	0	1	1
Application:	Digital cellular							
Mode 3:	Cascade Mode (CS6400(m)⇔CS6400(s))	master:	1	0	1	0	1	0
Application:	Teleconferencing	slave:	1	0	0	0	1	1
Mode 4:	Interface to DSP (DSP⇔CS6400(m)⇔CS6400(s))	slave:	1	0	0	0	1	1
Application:	Teleconferencing							
4.1:	Master's Codec is Bypassed	master:	0	0	0	0	1	0
4.2:	Master's Codec is Used	master:	1	0	0	0	1	0
Mode 5:	Interface to Network: Single Serial Port							
5.1:	1ch data: codec-8bit		0	1	0	0	0	1
5.2:	2ch data: codec-8bit		0	1	0	0	0	0
5.3:	1ch data: dsp-16bit		0	1	0	0	1	1
5.4:	2ch data: dsp-16bit		0	1	0	0	1	0
Mode 6:	Interface to Network: Dual Serial Port							
6.1:	1ch data: codec-8bit		0	1	0	1	0	1
6.2:	2ch data: codec-8bit		0	1	0	1	0	0
6.3:	1ch data: dsp-16bit		0	1	0	1	1	1
6.4:	2ch data: dsp-16bit		0	1	0	1	1	0

Table 1. CS6400 Configurations

The behavior of the CS6400 is controlled by configuration-control input pins. The behavior of the CS6400 for each possible state of these control signals is illustrated in Table 1.

As indicated in Table 1, the CS6400 has six operating modes. These operating modes are illustrated in Figure 4.

The simplest operating mode is Mode 1. This operating mode is useful in applications where the data link to the far end is analog, as in analog cellular hands free, or in analog speaker phones.

Mode 2 is useful in applications where the data link to the far end is digital, as in digital cellular hands free, or in digital (ISDN) speaker phones.

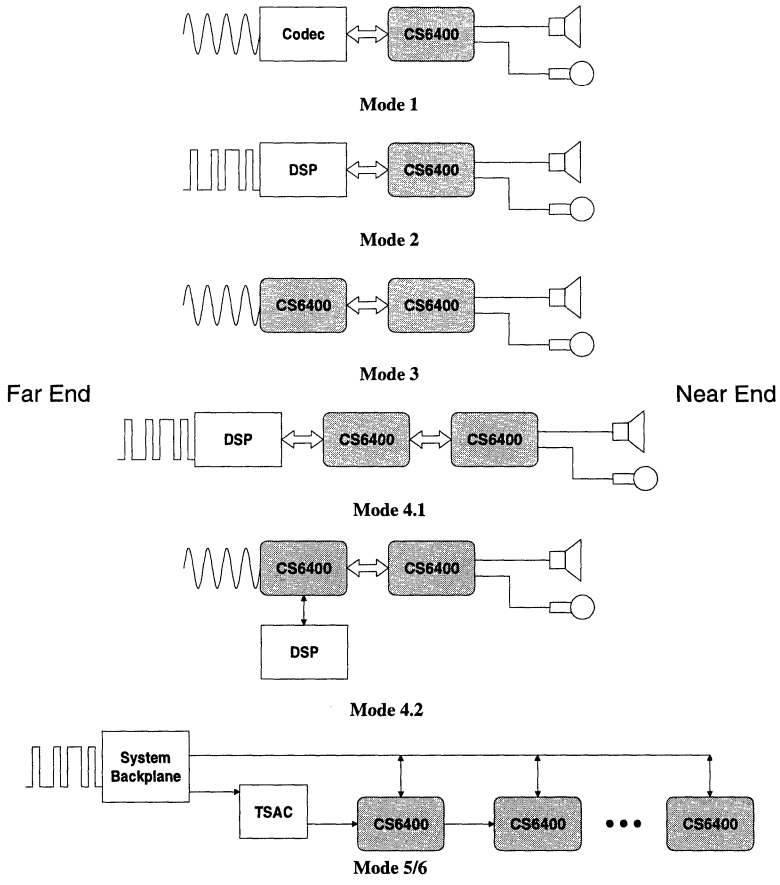


Figure 4. Operating Modes

Mode 3 is similar to Mode 1, except that a second CS6400 is used as the codec. In this configuration, the echo cancellers on the two CS6400s are cascaded, allowing the CS6400 to be used in environments with longer echo response. This mode would be useful in teleconferencing applications.

Mode 4 is similar to Mode 3, except that in Mode 4, the CS6400 is connected to a DSP. Also, in Mode 4, the data link to the far-end may be digital or analog. For example, the codec on the master CS6400 may be used as the far-end interface, and the serial interface to the DSP may be used for control. Alternatively, the master codec may be bypassed, with the far-end data being passed digitally from the DSP to the master CS6400.

Mode 5 and 6 are for network and base-station applications. In these cases, CS6400s are connected together on a PCM highway; access to the PCM highway is controlled by an external TSAC (Time-Slot Assigner Chip).

In Modes 5 and 6, the taps in the CS6400 may be split to provide two independent 32 ms channels. In Mode 5, these channels are time multiplexed onto a single serial bus. In Mode 6, each channel is assigned to a separate serial bus.

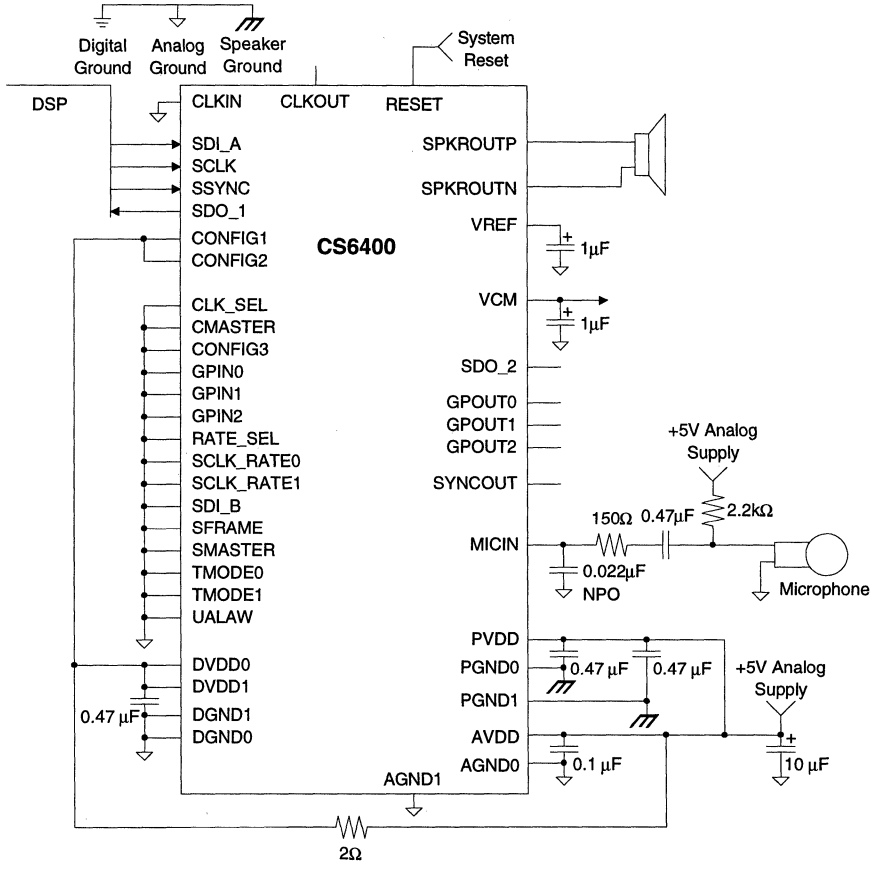


Figure 5. DSP Connection Diagram (Mode 2)

Interfacing to an external DSP

When interfacing to an external DSP (Mode 2), the CS6400 is configured as a serial-bus slave; i.e., SCLK, and SSYNC signals are provided to the CS6400 by the DSP. The recommended interface circuitry for this case is shown in Figure 5.

In this case, the DSP sends a single start-of-frame pulse to the SSYNC input one SCLK period before the start of a data frame. Since there is only one SSYNC input, every data frame includes both a data read from the CS6400 and a data write to the CS6400.

The CS6400's SSI is compatible with industry-standard DSPs. For Motorola, TI, and other popular DSPs, the start-of-frame sync pulse is positive logic. The SSI can be configured to accept a positive start-of-frame pulse by setting SSENSE=0. For AT&T DSPs, the start-of-frame sync pulse is negative logic. In this case, SSENSE=1. The behavior of the serial interface in these cases is illustrated in Figure 6. Note that the sense of SCLK also changes.

When a DSP is connected to a CS6400, the DSP can reconfigure the CS6400 by writing to the CS6400's control registers via the SSI.

To multiplex both data and control on one serial interface, a steering bit is used. The first bit sent (MSB) by the DSP determines whether the data is control or data, as shown in Figure 7.

If the Steering Bit (b15) is zero, then the data transferred on the Serial Interface is audio data. Note that since a transfer consists of 16 bits, this allows 15-bit precision for audio data.

If STR is one, the data transferred on the Serial Interface is control information. If the RNW bit is a zero, the data written by the external DSP is stored by the CS6400 in the indicated destination register, and simultaneously, the state of the destination register before the write is read back into the DSP. If RNW is one, the data written by the external DSP is ignored.

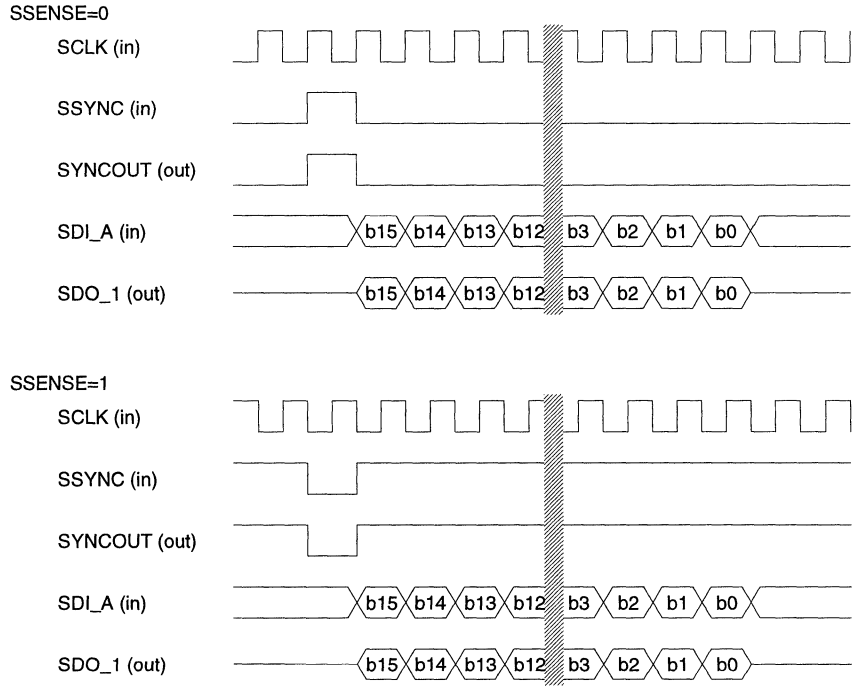


Figure 6. Serial Port Timing for Pulsed Sync Mode (Modes 2 and 4)

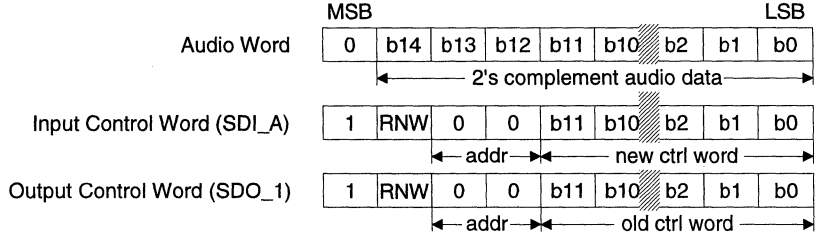


Figure 7. Audio and Control Transfer for 16-bit Data Modes

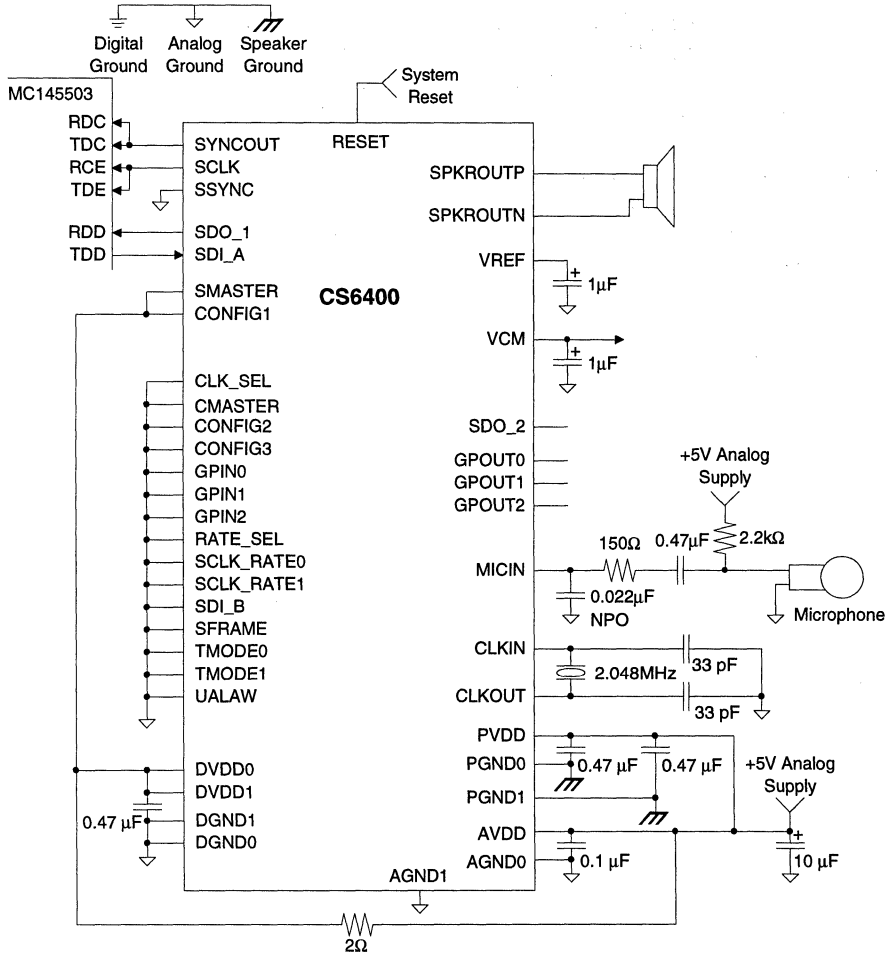


Figure 8. External Codec Connection Diagram

Note that only one control word or one data word may be transferred in a sample time, meaning that no audio data is transferred in sample times where control information is transferred. In such sample times, the CS6400 will reuse (double-sample) the audio data from the previous sample time. As a result, to minimize distortion of the audio signal, control transactions should be made infrequently.

Interfacing to an external codec

In applications like speakerphones, a DSP is normally not present. In such cases, it is possible to connect the CS6400 directly to an external network codec (like the Motorola MC145503). The interface circuit in this case is shown in Figure 8.

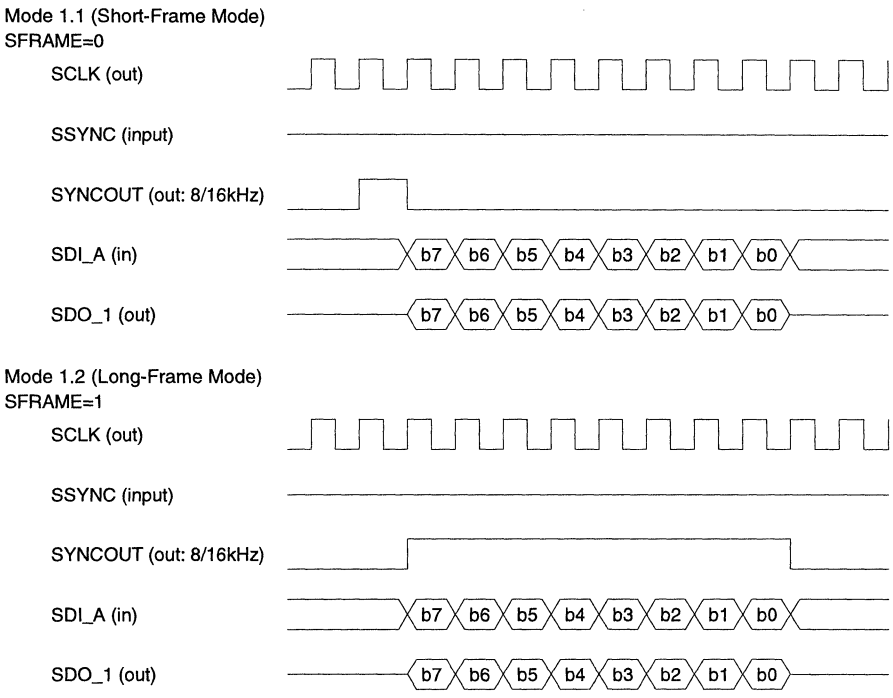


Figure 9. External-Codec Mode Timing (Mode 1)

Interfacing the CS6400 to an external codec (Mode1) is like interfacing to an external DSP (Mode2), except that SSYNC and SCLK are sourced by the CS6400 (i.e., SMASTER=1), and CLKIN is generated locally by connecting a crystal between CLKOUT and CLKIN. The timing for these signals is illustrated in Figure 9.

Unlike audio-data samples in Mode 2, audio-data samples in Mode 1 are 8 bits (μ–law or A-law companded). No control information can be transferred in Mode 1, so there is no control/data steering bit. Also note that since control information cannot be transferred, the default settings of the control registers are used.

Another difference between Mode 1 and Mode 2 is that in Mode 1, 160 echo-canceller taps (out of the available 512) are allocated to network-echo cancellation ("NEC" in Figure 3).

Interfacing to a network backplane

Interfacing the CS6400 to a network backplane is similar to interfacing the CS6400 to DSPs and external codecs. Like an external codec, a network backplane normally does not transfer control data over the SSI to the CS6400; instead, it uses the default control settings. Like an external DSP, the backplane sources SSYNC and SCLK (i.e., SMASTER=0).

In network (TSAC) applications, up to 16 CS6400s may be connected to a single backplane serial interface, providing up to 16 independent 64 ms channels, or 32 independent 32 ms channels.

The hardware connection to the CS6400 depends on the operating mode. For Mode 5 applications (i.e., a single serial port), the hardware connection is as shown in Figure 10. For Mode 6 applications (i.e., a dual serial port), the hardware connection is as shown in Figure 11.

Signal timing for Mode 5 applications is shown in Figures 12-15. As shown in these figures, the transactions for a particular sample time are initiated by a framing pulse from the TSAC. During the framing pulse, the CS6400 connected to the TSAC will make at least two transactions on the serial bus. This CS6400 will then send a similar framing pulse (via SYNCOUT) to the next CS6400 in the chain, which will also make at least two transactions. This CS6400 will send a framing pulse to the next CS6400, and so forth.

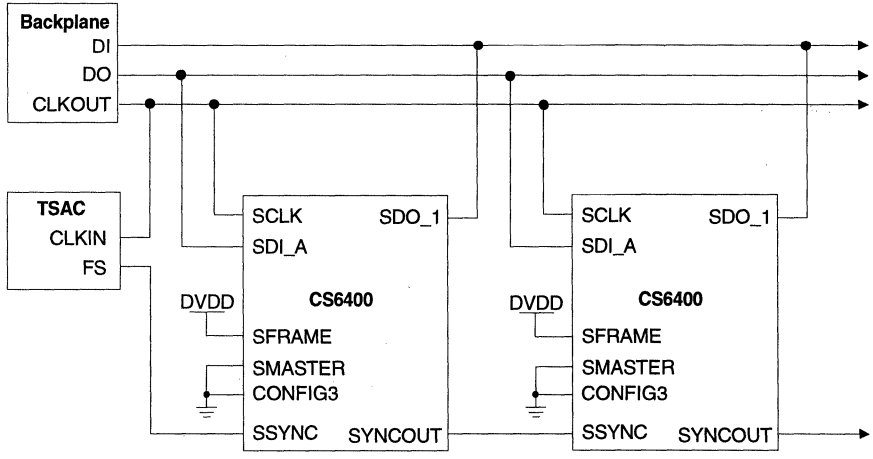


Figure 10. Network Connection Diagram (Mode 5)

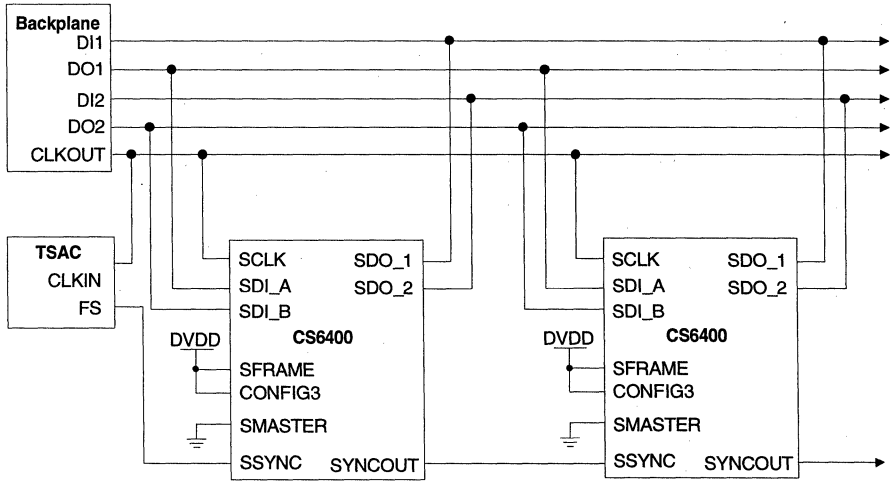


Figure 11. Network Connection Diagram (Mode 6)

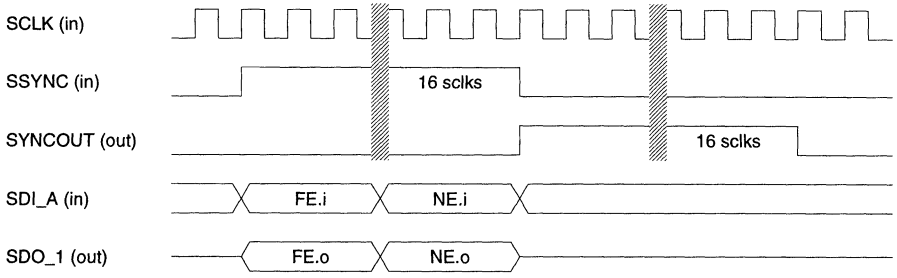


Figure 12. Network mode with 1 channel, 8-bit data (Mode 5.1)

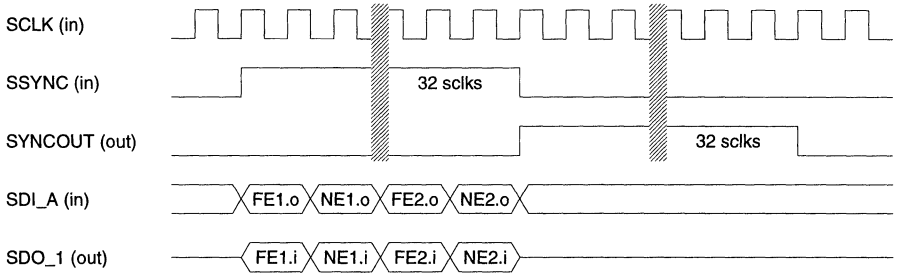


Figure 13. Network mode with 2 channels, 8-bit data (Mode 5.2)

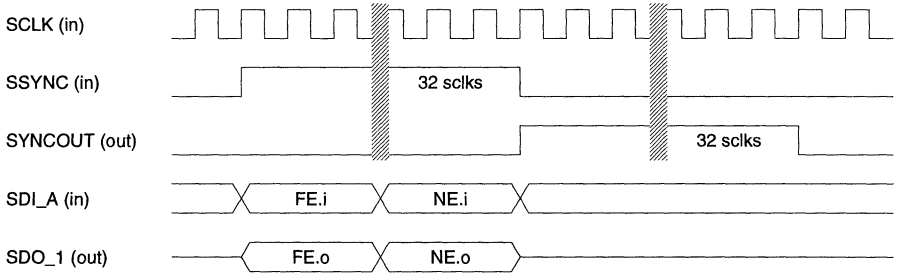


Figure 14. Network mode with 1 channel, 16-bit data (Mode 5.3)

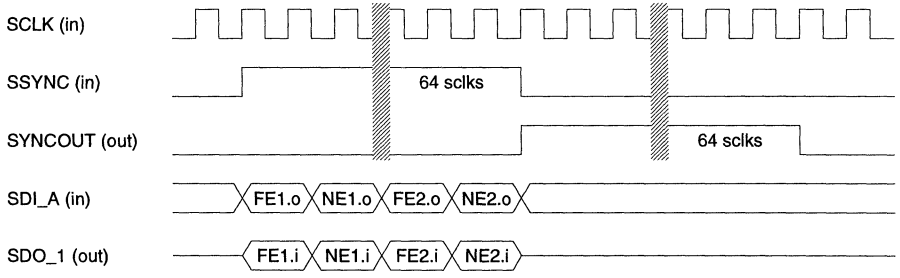


Figure 15. Network mode with 2 channels, 16-bit data (Mode 5.4)

For Mode 6 applications, the hardware connections are shown in Figure 11. In this case, two serial parts are used, doubling the data rate between the backplane and the CS6400. Signal timing for Mode 6 is shown in Figure 16-19.

In Modes 5 and 6, serial-data transactions may be 8 bits or 16 bits. Eight-bit data is always μ–law or A-law companded, and contains no control information.

Operating Modes

Reset Mode

Reset may be asserted either by setting the RESET pin high, or by setting the RST bit in control register SSI_CR0. The only functional difference between these two operations is that setting the RESET pin clears the RST bit. During Reset, all chip functions are halted except for the Serial Interface, though writes to any control bit except RST are ignored. Power down is not enabled.

Upon exiting Reset, control registers and RAMs are cleared, and then control constants are loaded into Data RAM.

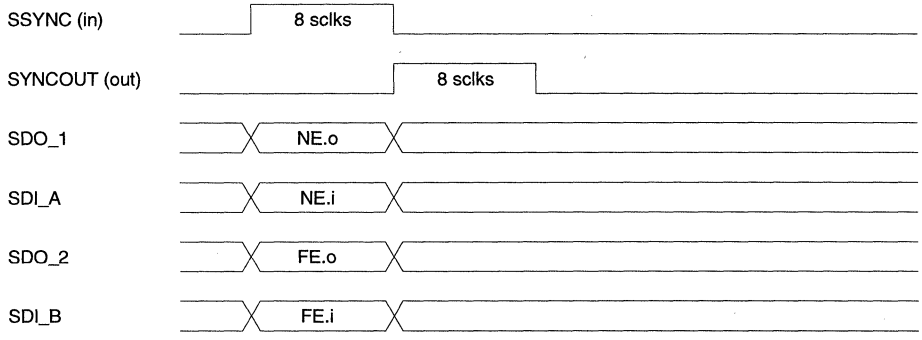


Figure 16. Network mode with 1 channel, 8-bit data (Mode 6.1)

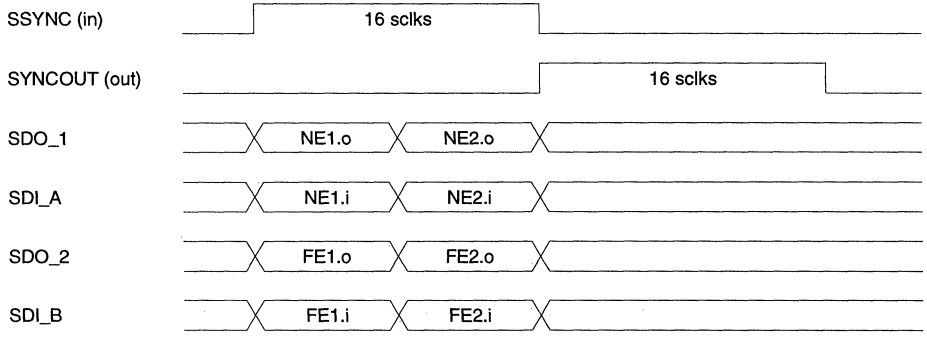


Figure 17. Network mode with 2 channels, 8-bit data (Mode 6.2)

Power-Down Mode

Power Down is initiated by setting the "SLP" bit in register SSI_CR0. In Power Down, the CPU and the AFP are powered down, but the SSI and the Codec are still operational.

Since the SSI and the Codec are active during Power Down, it is possible to serially transfer audio and control data while SLP is asserted, bypassing the CPU and AFP. Note, however, that since the CPU is powered down, no scaling is performed on the ADC input, no echo is cancelled, and audio data is not companded. Note also that audio data transfers during power down are possible only in Mode 2.

Isolated Modes

Modes 1 and 2 are the "Isolated" modes for the CS6400. In the Isolated modes, a single CS6400 is connected either to an external codec or to an external DSP. In the Isolated modes, only one data or control transaction may occur in any particular sample time.

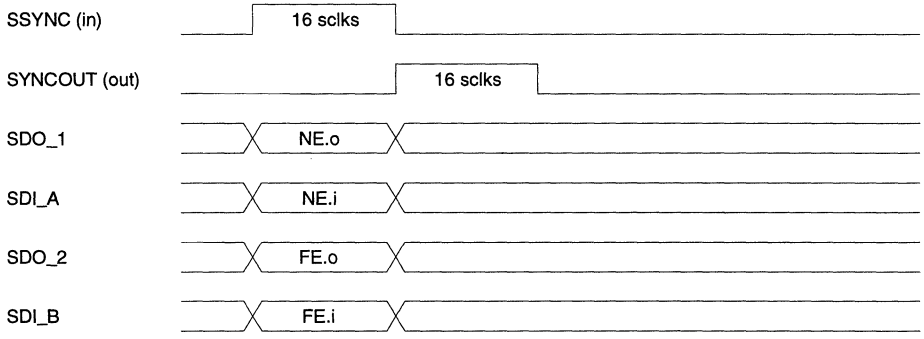


Figure 18. Network mode with 1 channel, 16-bit data (Mode 6.3)

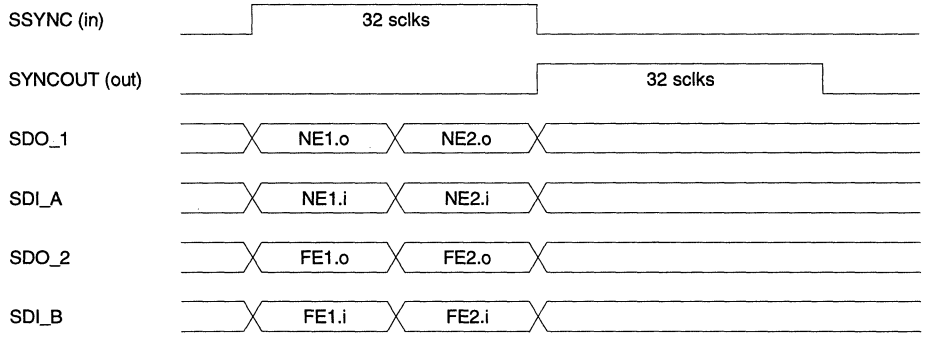


Figure 19. Network mode with 2 channels, 16-bit data (Mode 6.4)

Cascaded Modes

Modes 3 and 4 are the "Cascaded" modes for the CS6400. In the Cascaded modes, two CS6400s are connected together to double the effective adaptive-filter length, and to potentially provide a second codec. With two CS6400's, up to 128 ms of echo can be cancelled at an 8 kHz sample rate, and up to 64 ms can be cancelled at a 16 kHz sample rate.

Mode 3 is used when the interface to the far end is analog. In this case, the codecs in both the master CS6400 and the Slave CS6400 are used: the codec in the Master CS6400 is used for the far-end acoustic interface, and the codec in the slave is used as the near-end interface. The serial-port connections for the Mode 3 are shown in Figure 20. Note that in Mode 3, the 26 dB microphone gain stage in the Master CS6400 is bypassed.

In Mode 3, 20 ms of the available 64 ms are allocated to network echo cancellation when the 8 kHz sampling rate is selected. The network canceller is disabled when the 16 kHz sampling rate is selected.

Mode 4 is used when an external DSP is present. In mode 4, the codec on the Master CS6400 is typically bypassed, meaning that the audio data from the far end is passed to the CS6400 digitally. Alternatively, the codec on the Master CS6400 may be used as the far-end acoustic interface, with control information being provided by the DSP. In this case, acoustic data from the external DSP is ignored. As in Mode 3, the 26 dB microphone gain stage in the Master CS6400 is bypassed. The serial-port connections for the Mode 4 are shown in Figure 21.

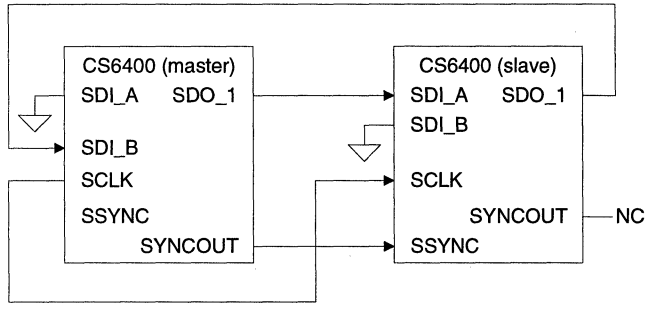


Figure 20. Cascaded Mode (Mode 3)

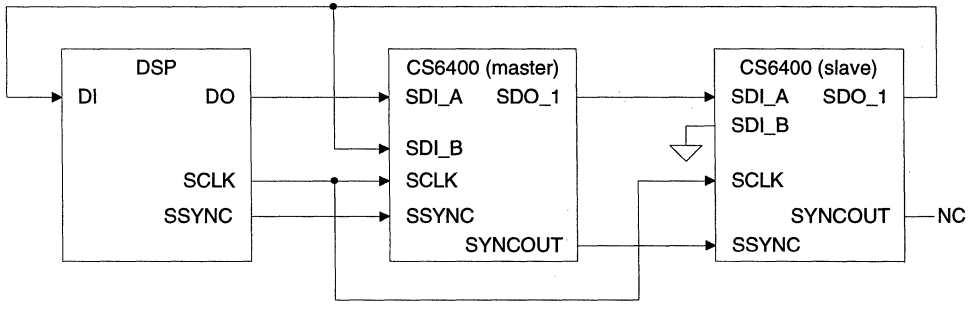


Figure 21. Cascaded Mode (Mode 4)

	Time Slot	Host DSP		Master		Slave	
		DI	DO	SDI	SDO_1	SDI	SDO_1
	1	Conv		Conv	Conv	Conv	Conv
	2	NE In		NE In			NE In
	3	Ctrl, R1		Ctrl, R1	Ctrl, R1	Ctrl, R1	Ctrl, R1
1/Fs seconds	. . .	. . .	. . .	. . .	. . .	. . .	. . .
	2/6/14						
	3/7/15						
	4/8/16	FE Out	FE In	FE In	Last M	Last M	FE Out

Table 2. Serial-Interface Transactions in Cascaded Mode (Mode 4)

In Mode 4, 20 ms of the available 64 ms are allocated to network echo cancellation when both the 8 kHz sampling rate is selected and the codec on the Master CS6400 is used. The network canceller is disabled when the 16 kHz sampling rate is selected.

In Mode 3 and Mode 4, a sample time is started when the 16-bit far-end data sample is transferred by the DSP to the Master CS6400. In the ensuing sample time, the two CS6400s exchange convolution results, transparent to the DSP (see Table 2). In the next time slot, the Slave passes the near-end data sample to the Master. To end the transactions for a sample time, the Master sends control information to the Slave, again transparent to the DSP, as illustrated in Figures 22 and 23.

Data must be exchanged quickly between the Master and the Slave to allow time for processing in the CS6400s. In particular, the serial bit rate must be at least 1.024 MHz in Cascaded Mode. Note that the number of time slots present in a sample time is a function of the sampling rate and the serial data rate (see Table 2). For example, with an 8 kHz sampling rate and a 2.048 MHz serial data rate, 16 time slots are present in a sample time. With a 16 kHz sample rate and a 1.024 MHz serial data rate, four time slots are present in a sample time.

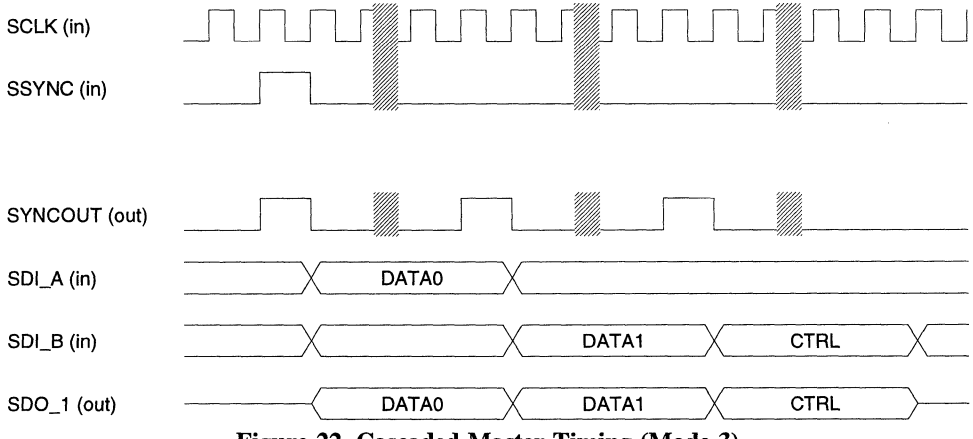


Figure 22. Cascaded Master Timing (Mode 3)

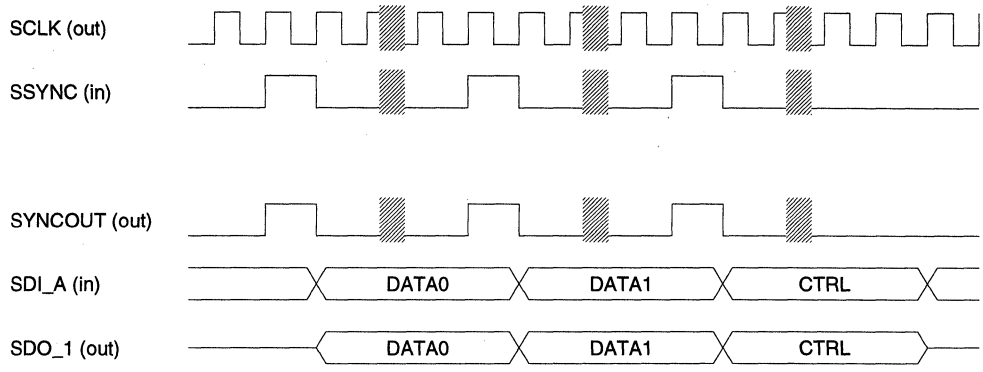


Figure 23. Cascaded Slave Timing (Mode 3)

Control Register Definitions

The CS6400 has four control registers that are accessible via the SSI, which allow a user to monitor and control the behavior of the CS6400. Note that these registers are accessible only when an external DSP is connected to the SSI. Even without a DSP, however, some visibility and control is provided by the GPIN/OUT pins (see PIN DESCRIPTIONS).

The following tables explain the four registers accessible by the serial interface in 16-bit modes. These registers are accessed by setting b15 high. The state of b14 indicates whether the register access operation is a read (high) or a write (low). Bits b13 and b12 together address the register as follows:

b13 : b12	Register
00	SSI_CR0
01	SSI_CR1
10	SSI_CR2
11	SSI_CR3

In the following tables describing each bit of the control registers, the bit names of each 12-bit register are at the top of the page. The Reset state of these registers is immediately below that. The Reset state is also noted by an "R" beside the appropriate value in the "value" column.

Register SSI_CR0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RST	**SLP**	**SETS**	**NECD**	**FHPD**	**NHPD**	**CE**	**NECS**	**GBC1**	**GBC0**	**AECB1**	**AECB0**
0	0	0	0	0	0	0	0	1	0	1	0

This register is read from the SSI by the CPU only upon exit from Reset and Sleep. This register is cleared at reset except for D3-D0 (see below).

BIT	NAME	VALUE		FUNCTION
RST	Reset	0	*R*	Normal operation.
		1		Control registers and RAMs are cleared, and then control constants are loaded into Data RAM. SSI is still operational, though writes to any control bit except RST are ignored.
SLP	Sleep	0	*R*	Normal operation.
		1		The CPU and AFP on the CS6400 are powered down. Control registers and RAMs are unaffected. Serial Data transactions that occur during power down are transferred directly between the SSI and the codec, bypassing the CPU. As a result, echo is passed uncancelled.
SETS	Saved-ERL Threshold Select			After reset, the CS6400 will operate in half duplex until the echo canceller(s) have adequately converged. Saved-ERL Threshold Select (SETS) determines the ERLE level required before the CS6400 will transition from half duplex to full duplex.
		0	*R*	TBD
		1		TBD
NECD	NEC Disable	0	*R*	In Modes 1 & 3, 20 ms of the available 64 ms of EC taps are allocated by default to network echo cancellation.
		1		No taps are allocated to network echo cancellation.
FHPD	FE_IN High-Pass Disable	0	*R*	A high-pass filter ((1-D)/(1-0.75D)) is inserted in the far-end input signal path.
		1		This filter is bypassed.
NHPD	NE_IN High-Pass Disable	0	*R*	A high-pass filter ((1-D)/(1-0.75D)) is inserted in the near-end input signal path.
		1		This filter is bypassed.
CE	Companding Enable	0	*R*	Data in 16-bit data modes is linear (i.e., not companded).
		1		b15 is still used as the steering bit, but if b15=0, the next 8 bits are companded.
NECS	NEC-Size Select	0	*R*	The NEC filter covers 20 ms and the AEC covers 44 ms when the NEC is enabled.
		1		The NEC size is reduced to 10 ms, and the AEC is extended to 54 ms.

6

Register SSI_CR0 (cont.)

BIT	NAME	VALUE	FUNCTION
GBC1 GBC0-	Graded-Beta Count		Graded-Beta Count - These bits control the rate at which the update gain decays in the AEC as the adaptive-filter taps are updated in a particular sample time. For each setting below, some number of taps are processed, after which the update gain is divided by two. The possible settings are given below: Taps Processed — Equivalent path-decay rate
		00	512 — 0 dB/ms
		01	64 — 0.75 dB/ms
		10 *R*	128 — 0.38 dB/ms
		11	256 — 0.19 dB/ms
AECB1 AECB0	AEC Beta		These bits scale the adaptive filter update gain that is present at the start of each sample time. Update Gain
		00	0.25
		01	0.5
		10 *R*	1.0
		11	2.0

Recommended settings for D3-D0:

Not Cascaded	Cascaded	
0001	0000	--No graded beta
0111	0111	--"dead" room/car; 0.75 dB/ms path decay
1010	1010	--medium room; (default) 0.28 dB/ms path decay
1100	1100	--large (or "live") room; 0.19 dB/ms decay

Register SSI_CR1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CSR	**CSS**	**NACD**	**NDCD**	**FACD**	**FDCD**	**NSD**	**FSD**	**NCC**	**HDD**	**SD**	**ACC**
0	0	0	0	0	0	0	0	0	0	0	0

This register is read/written by the CPU every sample time. This register is cleared at Reset by the SSI.

BIT	NAME	VALUE		FUNCTION
CSR	Cascade-Slave Reset	0 1	*R*	Normal operation. Reset the cascade slave in Modes 3 & 4. Note that for control data to propagate from the master CS6400 to the slave, control information must be written twice.
CSS	Cascade-Slave Sleep	0 1	*R*	Normal operation. This bit will power down the CPU and the AFP in the cascade slave in Modes 3 & 4. Note that for control data to propagate from the master CS6400 to the slave, control information must be written twice.
NACD	NE ADC Clipping Detect	0 1	*R*	Near-end ADC clipping not detected. Near-end ADC clipping detected. (Modes 1-4 only)
NDCD	NE DAC Clipping Detect	0 1	*R*	Near-end DAC clipping not detected. Near-end DAC clipping detected. (Modes 1-4 only)
FACD	FE ADC Clipping Detect	0 1	*R*	Far-end ADC clipping not detected. Far-end ADC clipping detected. (Modes 3 & 4 only)
FDCD	FE DAC Clipping Detect	0 1	*R*	Far-end DAC clipping not detected. Far-end DAC clipping detected. (Modes 3 & 4 only)
NSD	NE Speech Detect	0 1	*R*	Near-end speech not detected Near-end speech detected.
FSD	FE Speech Detect	0 1	*R*	Far-end speech not detected. Far-end speech detected.
NCC	NEC Coefficient Clear	0 1	*R*	Normal operation. (or if GPIN0 is asserted) The network canceller (or channel 2 in Modes 5/6) coefficients are cleared.
HDD	Half-Duplex Disable	0 1	*R*	Normal operation. (or if GPIN2 is asserted) Half-duplex mode, which is normally used during convergence, is disabled.
SD	Suppression Disable	0 1	*R*	Normal operation. (or if GPIN1 is asserted) Supplementary suppression, which normally operates in conjunction with the echo cancellers, is disabled.
ACC	AEC Coefficient Clear	0 1	*R*	Normal operation. (or if GPIN0 is asserted) The acoustic canceller (or channel 1 in Modes 5/6) coefficients are cleared.

Register SSI_CR2

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PDC	**PDSD**	**MGD**	**DV4**	**DV3**	**DV2**	**DV1**	**DV0**	**AV3**	**AV2**	**AV1**	**AV0**
0	0	0	0	0	0	0	0	0	0	0	0

This register is cleared at Reset by the SSI. This register is read/written by the CPU every sample time.

BIT	NAME	VALUE		FUNCTION
PDC	Power Down Codec	0 1	*R*	Normal operation. The entire codec is powered down.
PDSD	Power Down Speaker Driver	0 1	*R*	Normal operation. Only the speaker driver in the codec is powered down.
MGD	Microphone 26 dB Gain Disable	0 1	*R*	Normal operation. The 26 dB microphone preamp is bypassed.
DV4-DV0	DAC Volume	00000 · · 11111	*R*	DAC volume control is implemented in the Codec, with the attenuation being -2.5 dB times the DAC-volume value.
AV3-AV0	ADC Volume	0000 · · 1111	*R*	ADC volume control is implemented in the CPU, with the attenuation being -3 dB times the ADC-volume value.

Register SSI_CR3 (Test Register)

This register allows real-time access to the CPU data RAM.

To read a particular location, the external DSP will write the address of the desired RAM location into SSI_CR3. The CPU data RAM is only 128 words, so only the seven least-significant bits of the 12-bit word are used for address. The most-significant bit indicates if the access is for the 12 most-significant data bits, or for the 12 least-significant bits. The next most-significant bit indicates write or read.

If the access is a read, the requested CPU-RAM data item is placed in the control register so that it can be read by the external DSP in the next sample time from SSI_CR3.

If the access is a write, the DSP will write the address in one sample time, and then it will write the data that it wishes to write into CPU data RAM in the next sample time. Only 12 bits of the 16-bit data item are affected; the other four bits are unchanged.

If two DCECs are connected in cascade mode, b9 indicates whether a read/write request is for the master or the slave DCEC. In cascade mode, all commands should be sent twice to allow them to propagate to the slave. Read data is read by the DSP two transactions after the second time a command is transmitted.

If bit 8 is set on a read, the revision code is returned instead of RAM data (b11 and b7-0 are ignored). For first silicon, the revision code is "0x101". The first nibble is incremented when an all-layer change is made; the lower byte is incremented on a metal revision.

This register is cleared at reset by the SSI.

	Address written by DSP	Data Written by DSP	Data Read by DSP
D11	top12/!bottom12	data, b15/b11	data, b15/b11
D10	write/!read	data, b14/b10	data, b14/b10
D9	master/!slave	data, b13/b9	data, b13/b9
D8	rev code/!rc	data, b12/b8	data, b12/b8
D7	must be 0	data, b11/b7	data, b11/b7
D6	addr, b6	data, b10/b6	data, b10/b6
D5	addr, b5	data, b9/b5	data, b9/b5
D4	addr, b4	data, b8/b4	data, b8/b4
D3	addr, b3	data, b7/b3	data, b7/b3
D2	addr, b2	data, b6/b2	data, b6/b2
D1	addr, b1	data, b5/b1	data, b5/b1
D0	addr, b0	data, b4/b0	data, b4/b0

Detailed Power Supply Connections

Figure 24 shows the detailed power supply connections. The CS6400 requires a clean analog quality +5V supply. The digital supply for the CS6400 should be derived from the system clean analog supply, and should not be connected directly to the board-level digital 5V supply.

Grounding and Layout

The CS6400 requires very careful attention to layout, power supplies, and decoupling to achieve rated performance. Extensive use of ground planes and ground-plane fill is recommended. The system circuit board should be partitioned into a digital region and an analog region, each with its own, non-overlapping, ground plane. The CS6400 should be completely over the analog ground plane, close to the digital region. The package should be oriented so that the digital pins face toward the digital region of the board. Figure 25 shows the general guidelines for proper layout.

The power and ground connections for the speaker (PVDD and PGND) should be routed separately from the analog power and ground planes to prevent the high speaker currents from flowing in the same ground plane as the microphone signal.

Note: In applications where the codec is not used no separate ground plane is required. The CS6400 may reside on the digital ground plane in this case.

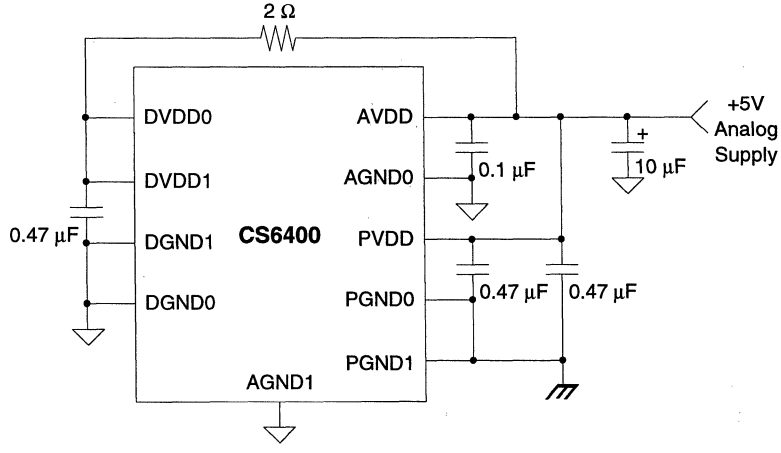
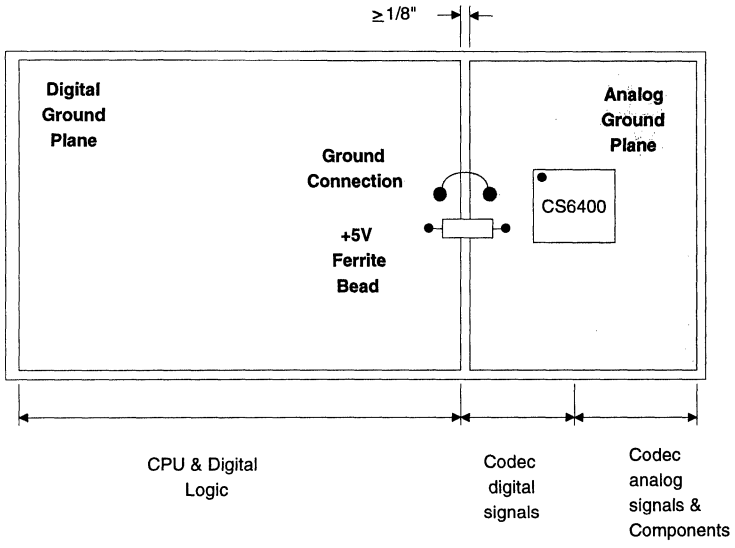


Figure 24. Power Supply Connections

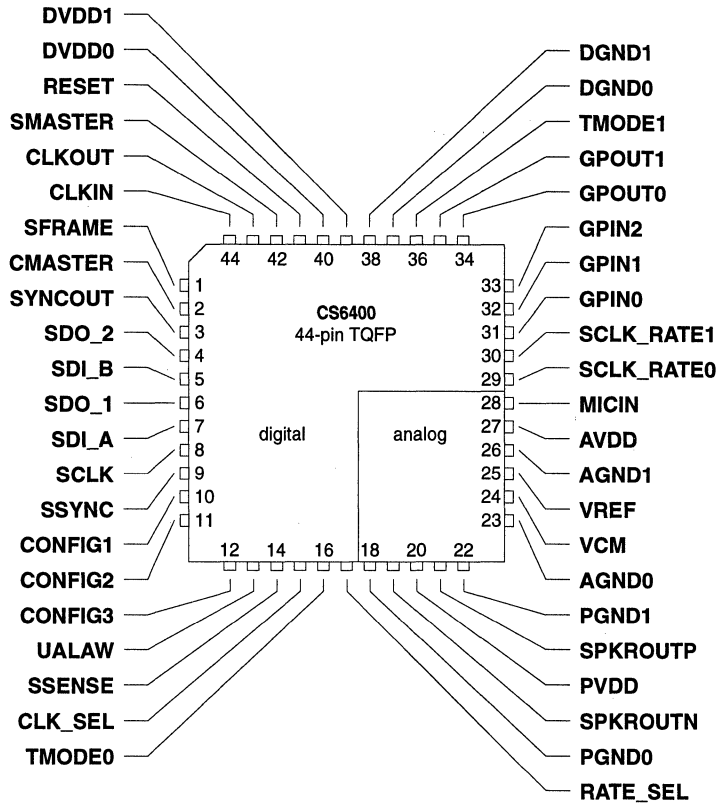


Note that the CS6400 is oriented with its digital pins towards the digital end of the board.

Figure 25. Suggested Layout Guideline

6

PIN DESCRIPTIONS



Power Supply

AGND0 - Analog ground, PIN 23
Analog ground.

AGND1 - Analog ground, PIN 26
Analog ground.

AVDD - Analog supply, PIN 27
+5V Analog supply.

DGND0 - Digital ground, PIN 37
Digital ground.

DGND1 - Digital ground, PIN 38
Digital ground.

DVDD0 - Digital supply, PIN 40
Digital +5V supply.

DVDD1 - Digital supply, PIN 39
Digital +5V supply.

PGND0 - Speaker-driver ground, PIN 18
Speaker driver ground.

PGND1 - Speaker-driver ground, PIN 22
Speaker driver ground.

PVDD - Speaker-driver supply, PIN 20
Speaker-driver +5V supply.

Analog I/O

MICIN - A/D input, PIN 28
Audio analog input.

SPKROUTN - D/A minus output, PIN 19
Negative differential speaker-driver output. The voltage on SPKROUTN will decrease if the DAC value is increased.

SPKROUTP - D/A plus output, PIN 21
Positive differential speaker-driver output. The voltage on SPKROUTP will increase if the DAC value is increased.

VCM - Voltage reference common out, PIN 24
A stable output voltage for setting the bias level for external analog circuits. No time-varying loads should be attached to VCM. Output voltage is about 1V into a load of not less than 100kΩ.

VREF - Voltage reference bypass out, PIN 25
Voltage reference used internal to the CS6400. Must be connected to AGND0 via a 1 µF capacitor. Connections should be made with short, fat traces.

Test

TMODE0 - Test-mode select pin, PIN 16
TMODE0 is used in conjunction with TMODE1 to set the test mode. TMODE0 should be grounded in nomal operation.

TMODE1 - Test-mode select pin, PIN 36
TMODE1 is used in conjunction with TMODE0 to set the test mode. TMODE1 should be grounded in normal operation.

Serial Digital I/O

RATE_SEL - Test input, PIN 17

If RATE_SEL is low, the Codec sampling rate and the SSYNC pulse frequency are 8 kHz; if RATE_SEL is high, they are 16 kHz.

SCLK - Serial clock, PIN 8

SCLK is the bit clock for the serial interface. It may be an output or an input, depending on the state of SMASTER, and may operate at 256 kHz, 384 kHz, 1.024 MHz, or 2.048 MHz depending on the states of SCLK_RATE0, SCLK_RATE1 and SMASTER.

SCLK_RATE0 - SCLK frequency control, PIN 29

Used in conjunction with SCLK_RATE1 to set the SCLK frequency when the CS6400 is a timing slave. Possible frequencies are 2.048 MHz, 1.024 MHz, 384 kHz, and 256 kHz, for SCLK_RATE1:SCLK_RATE0 being 11, 10, 01, and 00, respectively. However, if the CS6400 is a timing master (i.e., SMASTER is high), the SCLK frequency may only be 2.048 MHz, so in this case, SCLK_RATE0 must be high.

SCLK_RATE1 - SCLK frequency control, PIN 30

Used in conjunction with SCLK_RATE0 to set the SCLK frequency when the CS6400 is a timing slave. Possible frequencies are 2.048 MHz, 1.024 MHz, 384 kHz, and 256 kHz, for SCLK_RATE1:SCLK_RATE0 being 11, 10, 01, and 00, respectively. However, if the CS6400 is a timing master (i.e., SMASTER is high), the SCLK frequency may only be 2.048 MHz, so in this case, SCLK_RATE1 must be high.

SDI_A - Serial data in, PIN 7

SDI_A is the primary serial-data input to the CS6400.

SDI_B - Serial data in, PIN 5

SDI_B is the secondary serial-data input to the CS6400. This input is used only in cascaded and network modes.

SDO_1 - Serial data out, PIN 6

Primary serial output.

SDO_2 - Serial data out, PIN 4

Secondary serial output. Used only in two-channel network modes.

SFRAME - SSYNC frame/pulse control, PIN 1

If SFRAME is high, SSYNC is high during serial data transactions. If SFRAME is low, SSYNC is pulsed before the start of a serial-data transaction.

SMASTER - SSYNC direction control, PIN 42

SMASTER is used in conjunction with other configuration-control pins to control operating mode (see Table 1). If SMASTER is high, the CS6400 is a timing master, meaning that SCLK is an output, and the SCLK rate is set by the on-board crystal oscillator (nominally 2.048 MHz). If SMASTER is low, the CS6400 is a timing slave, meaning that the SCLK is an input, and the SCLK rate is set by the external DSP, but SCLK_RATE0 and SCLK_RATE1 must be set to reflect the nominal SCLK rate.

SSENSE - SSYNC Sense control, PIN 14

SSENSE controls the sense of SCLK, SSYNC, and SYNCOUT. If SSENSE is high, SSYNC and SYNCOUT are negative logic, and SCLK samples on the rising edge. If SSENSE is low, SSYNC and SYNCOUT are positive logic, and SCLK samples on the falling edge.

SSYNC - Sync signal for serial port, PIN 9

SSYNC is the serial-data sync strobe used when the CS6400 is a system-timing slave.

SYNCOUT - SSYNC cascade out for TSAC applications, PIN 3

SSYNC is the serial-data sync strobe used when the CS6400 is a system-timing master. It is also used when the CS6400 is a system-timing master in network modes and in cascaded modes.

UALAW - PIN 13

When UALAW is high, 8-bit serial data is μ-law; when UALAW is low, 8-bit serial data is A-law.

CONFIG1 - Configuration-control input, PIN 10

CONFIG1 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CONFIG2 - Configuration-control input, PIN 11

CONFIG2 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CONFIG3 - Configuration-control input, PIN 12

CONFIG3 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CMASTER - Cascade Master Configuration Control, PIN 2

CMASTER is used in conjuction with other configuration-control pins to control operating mode (see Table 1).

Miscellaneous

CLK_SEL - PIN 15

If CLK_SEL is high, the CS6400 PLL is bypassed, and the CS6400 24.576 MHz internal system clock is supplied via CLKIN. This mode is intended to facilitate production test.

CLKIN - System input clock from external master, PIN 44

If the CS6400 is a system-timing master, a 2.048 MHz clock-crystal circuit is connected between CLKIN and CLKOUT. If the CS6400 is a system-timing slave, CLKIN must be grounded.

CLKOUT - System output clock, PIN 43

If the CS6400 is a system-timing master, a 2.048 MHz clock-crystal circuit is connected between CLKIN and CLKOUT. Otherwise, CLKOUT is unconnected.

GPIN0 - General-purpose input, PIN 31

When GPIN0 is high, all echo canceller coefficients are cleared.

GPIN1 - General-purpose input, PIN 32

When GPIN1 is high, supplementary suppression is disabled.

GPIN2 - General-purpose input, PIN 33

When GPIN2 is high, half-duplex mode (which is used during convergence) is disabled.

GPOUT0 - General-purpose outputs, PIN 34

GPOUT0 is high while clipping is detected on the ADC input.

GPOUT1 - General-purpose outputs, PIN 35

GPOUT1 is high while the CS6400 is in half-duplex mode during initial convergence.

RESET - System reset, PIN 41

RESET must be asserted high for at least two SCLK periods after powerup to place the CS6400 in a known state.

PARAMETER DEFINITION

Anti-Alias Rejection

The rejection of input frequencies in the frequency range ±Fs/2 of all multiples of the input sample rate (64 x Fs). This rejection is almost solely dependent on the external input RC.

Audible (<20kHz) Noise

The DAC audible noise floor. Measured by applying a -60dB, 1kHz sine wave. S/(N+D) is then measured (over a 20Hz to 20kHz bandwidth). Then add 60dB to the answer, to compensate for the -60dB signal level.

Convergence

The process by which an echo canceller improves its path estimate, thereby improving its echo return-loss enhancement. Convergence is complete once the echo return-loss enhancement reaches its best value for a given environment.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

ERLE

Echo signal-power reduction (Echo Return-Loss Enhancement) provided by an echo canceller. Maximum ERLE for an echo canceller is dependent on training-signal statistics and echo-path attributes. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over the passband (20Hz to 0.45Fs), referenced to the level at 1kHz. Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Integrated Inaudible (>20kHz) Energy

The integrated signal level on the analog output pin after a 20kHz hi-pass filter. Zero digital input into the DAC. Units in mVrms.

Inter-Section Isolation

For an ADC, the amount of 1 kHz signal present on the output of the grounded input ADC, with 1 kHz 0 dB signal present on each other ADC/DAC. For a DAC, the amount of 1 kHz signal present on the output of a zero input DAC, with 1kHz 0dB signal present on each other ADC/DAC. Units in dB.

Offset Error

For the ADC, the deviation of the output code from the mid-scale with the selected input at VCM. For the DAC, the deviation of the output from VCM with mid-scale input code. Units in LSB's for the ADC and millivolts for the DAC.

Resolution

The number of bits in the input words to the DAC, and in the output words from the ADC.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e., attenuation bits for the DAC at full attenuation). Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms amplitude of the test signal to the rms sum of all the harmonic components. 1 kHz is used for testing. Units in dB.

Semiconductor Corporation

CS6401

Programmable Echo Canceller

Features

- For All Echo Canceller Applications
  - Digital Cellular Network Equipment
  - Analog Cellular Hands Free
  - Digital Cellular Hands Free
  - Office Speaker Phones
  - Desktop Teleconferencing
  - Long Distance Network Equipment
- Echo Cancellation
  - 8 kHz Sampling Rate
  - 512 tap (64 ms)
  - Split Mode for Two ECs (total taps = 512)

General Description

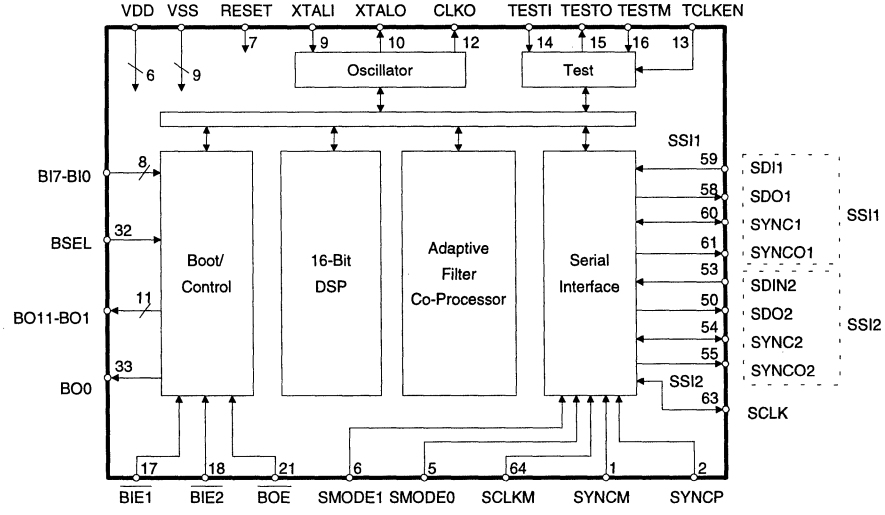
The CS6401 is a digital signal processor optimized for acoustic and/or network echo cancellation algorithms. The CS6401 implements all the adaptive filtering and control algorithms needed for high quality echo cancellation for a variety of applications. Crystal has developed the echo cancellation algorithms, and provides the DSP object code with the evaluation board. Custom algorithm development services are available from Crystal.

The CS6401 contains four main blocks:

- 16 MIPS, 16-Bit Programmable DSP
- 512-tap Adaptive FIR Filter Hardware Accelerator
- Data I-O Serial Interface
- Boot/Control Interface

ORDERING INFORMATION

CS6401-CQ	0 to 70 °C	64-pin Plastic QFP
CDB6401	Evaluation Board with object code	



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS (VSS = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VDD	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	(VDD)+0.4	V
Ambient Operating Temperature (power applied)	T_{Amax}	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS = 0V; all voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VDD	4.50	5.0	5.50	V
Ambient Operating Temperature	T_A	0	-	70	°C

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VDD = 5V ± 10%; measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-		V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -2.0mA	V_{OH}	2.4	-	-	V
Low-Level Output Voltage at I_o = 2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	1.0	µA.

Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Crystal Oscillator Frequency	fCLK	-	32.768	-	MHz

Serial Mode A (SMODE1=L, SMODE0=L, SCLKM=H, SYNCM=H, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	fSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	200	-	-	ns
SCLK Pulse Width High	tSCKH	200	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	3906	-	ns
SCLK rising to SDO1, 2 Valid	tCD	-	-	60	ns
SCLK2 rising to SDO1, 2 Valid	tSYD	-	-	40	ns
SCLK rising to SYNC2 edge	tCSD	-	-	20	ns
SDI1, 2 data setup time	tSU	40	-	-	ns
SDI1, 2 data hold time	tHD	40	-	-	ns

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Serial Mode B (SMODE1=L, SMODE0=L, SCLKM=L, SYNCM=H, SYNCP=H)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	fSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	120	-	-	ns
SCLK Pulse Width High	tSCKH	120	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	488	-	ns
SCLK rising to SDO1, 2 Valid	tCD	-	-	120	ns
SCLK2 rising to SDO1, 2 Valid	tSYD	-	-	60	ns
SCLK rising to SYNC2 edge	tCSD	-	-	60	ns
SDI1, 2 data setup time	tSU	20	-	-	ns
SDI1, 2 data hold time	tHD	20	-	-	ns

Serial Mode C CS4216 Application (SMODE1=L, SMODE0=H, SCLKM=H, SYNCM=H, SYNCP=H)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	220	-	-	ns
SCLK Pulse Width High	tSCKH	220	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	488	-	ns
SCLK rising to SDO 2 Valid	tCD	-	-	70	ns
SYNC2 falling to SDO 2 Valid	tSYD	-	-	50	ns
SCLK rising to SYNC2 edge	tCSD	-	-	20	ns
SDI2 data setup time	tSU	30	-	-	ns
SDI2 data hold time	tHD	30	-	-	ns

Serial Mode D (SMODE1=H, SMODE0=L, SCLKM=H, SYNCM=H, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	512	-	kHz
SCLK Pulse Width Low	tSCKL	960	-	-	ns
SCLK Pulse Width High	tSCKH	960	-	-	ns
SYNC1 Frequency	fSYN1	-	2.048	-	MHz
SYNC1 Pulse Width Low	tSY1L	-	244	-	ns
SYNC1 Pulse Width High	tSY1H	-	244	-	ns
SYNC2 Frequency	fSYN2	-	8	-	kHz
SYNC2 Pulse Width Low	tSY2L	-	62.5	-	us
SYNC2 Pulse Width High	tSY2H	-	62.5	-	us
SCLK falling to SDO2 Valid	tCD	-	-	60	ns
SCLK falling to SYNC2 edge	tCSD	-	-	30	ns
SYNC rising to SCLK edge	tSYSD	-	-	10	ns
SDI2, data setup time	tSU	40	-	-	ns
SDI2, data hold time	tHD	40	-	-	ns

Serial Mode E Network Application (SMODE1=H, SMODE0=H, SCLKM=L, SYNCM=L, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	120	-	-	ns
SCLK Pulse Width High	tSCKH	120	-	-	ns
SYNC1, 2 Frequency	fSYNC	-	8	-	kHz
SYNC1, 2 Pulse Width High	tSYNH	-	3906	-	ns
SYNCO1, 2 Frequency	fSYO	-	8	-	kHz
SYNCO1, 2 Pulse Width High	tSYOH	-	3906	-	us
SCLK rising to SDO1, 2 Valid	tCD	-	-	120	ns
SCLK rising to SYNC1, 2 edge	tCSD	-	-	60	ns
SYNC rising to SYNCOUT1, 2 edge	tCSOD	-	-	60	ns
SDI1, 2 data setup time	tSU	20	-	-	ns
SDI1, 2 data hold time	tHD	20	-	-	ns

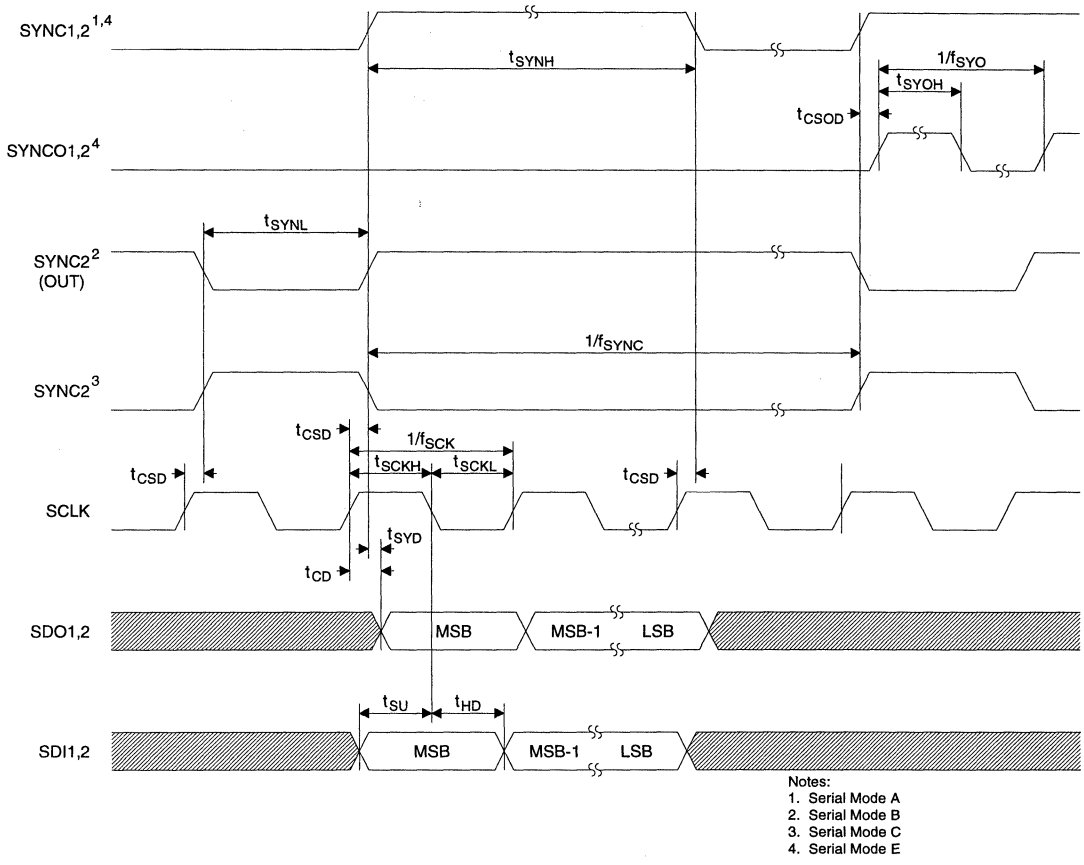

Figure 1. Serial Mode A, B, C, and E Timing.

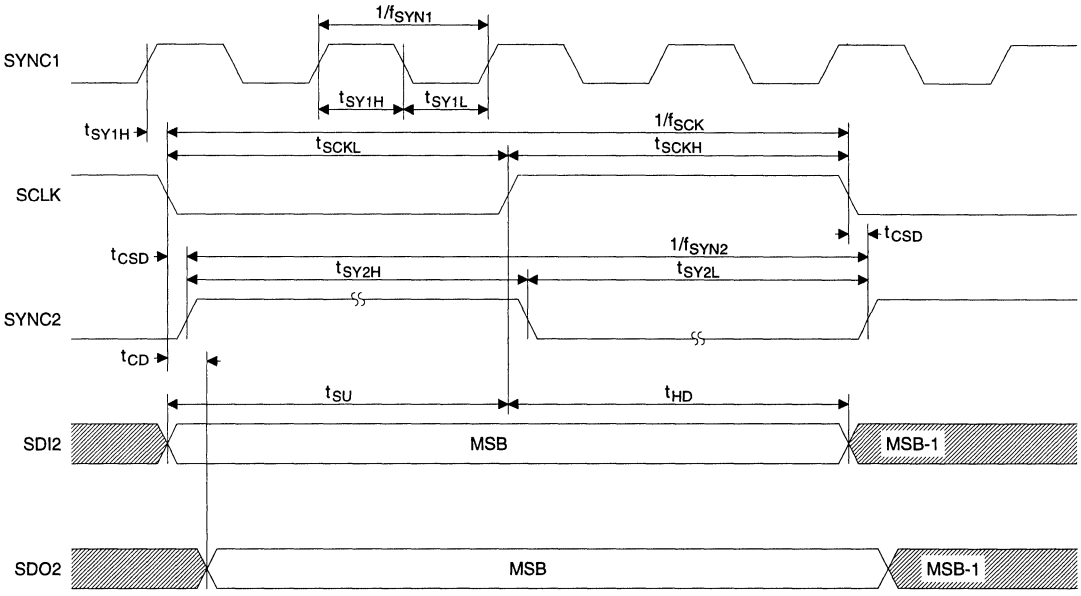

Figure 2. Serial Mode D Timing

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Boot Mode 1: Boot with Parallel EPROM (CS6401 is boot master. BSEL=L, $\overline{BIE1}$=L, $\overline{BIE2}$=L, $\overline{BOE}$=L)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	80/fCLK	-	s
RESET Falling to BO [11:0] become [000]	tRBO	-	130/fCLK	-	s
BO0 Pulse width Low (for upper byte)	tBOTL1	-	112/fCLK	-	s
BO0 Pulse Width High (for upper byte)	tBOTH1	-	68/fCLK	-	s
BO0 Pulse width Low (for lower byte)	tBOL2	-	106/fCLK	-	s
BO0 Pulse Width High (for lower byte)	tBOTH2	-	86/fCLK	-	s
BO0 Falling to BIN [7:0] Latch	tBOBI	-	30/fCLK	-	s
BI [7:0] setup time	tBISU	60		-	ns
BI [7:0] hold time	tBIHD	60		-	ns
Boot Procedure Period	tBOOT	-	285084/ fCLK	-	s

Boot Mode 2: Boot with Serial PROM (CS6401 is boot master. BSEL=H, $\overline{BIE1}$=L, $\overline{BIE2}$=L, $\overline{BOE}$=L)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	80/fCLK	-	s
RESET Falling to BO0 Falling	tRBO	-	100/fCLK	-	s
BO0 Pulse width Low	tBOTL1	-	36/fCLK	-	s
BO0 Pulse Width High (for bit15 bit1)	tBOTH1	-	32/fCLK	-	s
BO0 Pulse Width High (for bit0)	tBOTH2	-	60/fCLK	-	s
BO0 Falling to BI7 Latch	tBOBI	-	24/fCLK	-	s
BI7 setup time	tBISU	60	-	-	ns
BI7 hold time	tBIHD	60	-	-	ns
Boot Procedure Period	tBOOT	-	854958/ fCLK	-	s

Boot Mode 3: Boot with Parallel uP or DSP (CS6401 is boot slave. BSEL=L, BIEX=H at RESET, Controlled by Boot Master)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	78/fCLK	-	s
RESET Falling to $\overline{BIEX}$ Falling	tRBI2	132/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low (for upper byte)	tBINEL1	106/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for upper byte)	tBINEH1	62/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low (for lower byte)	tBINEL2	100/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for lower byte)	tBINEH2	80/fCLK	-	-	s
$\overline{BIEX}$ Falling to BI [7:0] Latch	tBINB	-	10/fCLK	-	s
BI [7:0] setup time	tBISU	200	-	-	ns
BI [7:0] hold time	tBIHD	200	-	-	ns

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Boot Mode 4: Boot with Serial uP or DSP (CS6401 is boot slave. BSEL=H, BIEX=H at RESET, Controlled by Boot Master)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	78/fCLK	-	s
RESET Falling to $\overline{BIEX}$ Falling	tRBI2	100/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low	tBINEL	30/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for bit15 bit1)	tBINEH1	32/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for bit0)	tBINEH2	54/fCLK	-	-	s
$\overline{BIEX}$ Falling to BI7 Latch	tBINEB	-	10/fCLK	-	s
BI7 setup time	tBISU	200	-	-	ns
BI7 hold time	tBIHD	200	-	-	ns

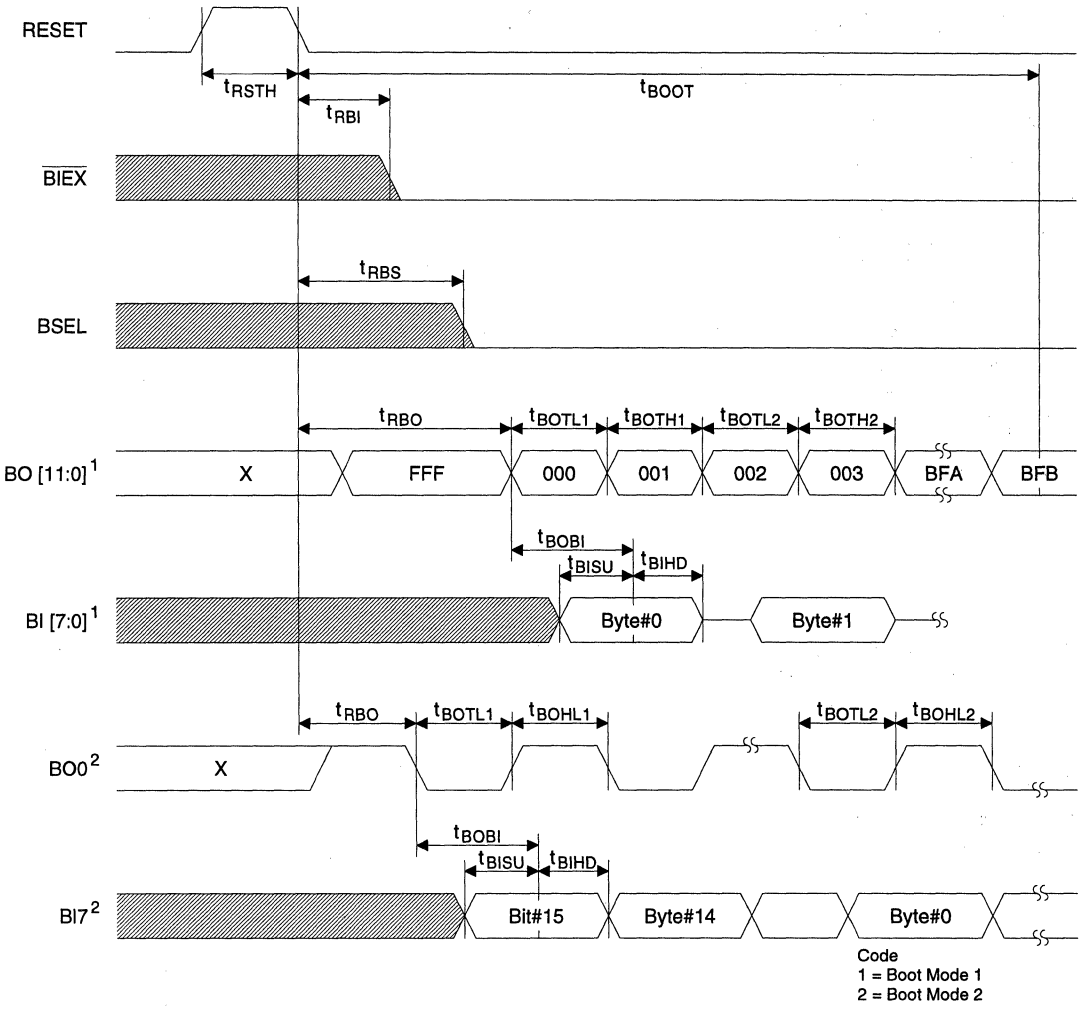


Figure 3. Boot Mode 1 and Mode 2

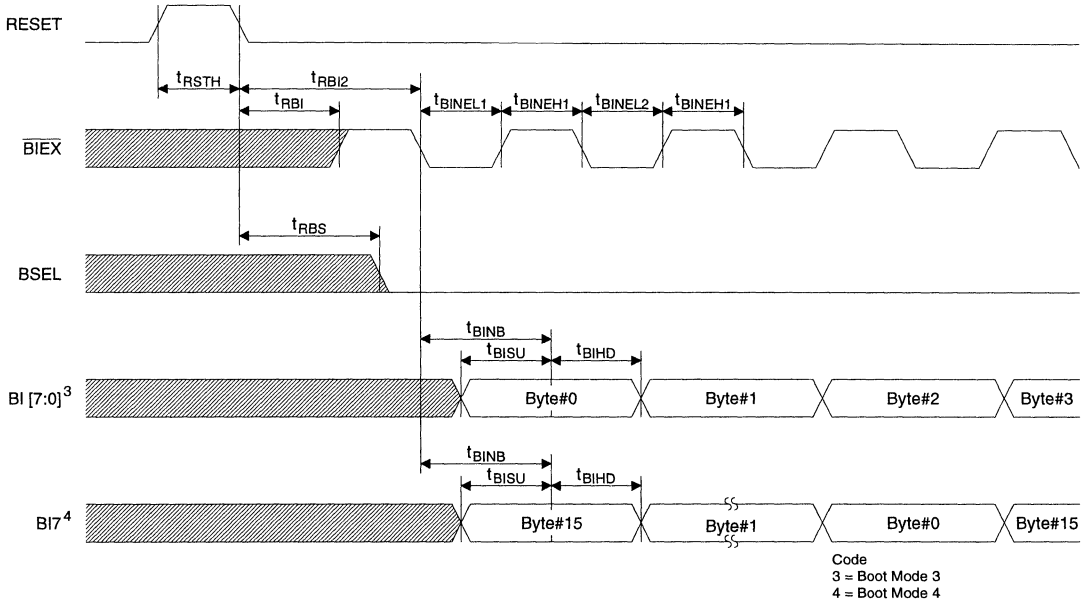


Figure 4. Boot Mode 3 and Mode 4

6

GENERAL DESCRIPTION

OVERVIEW

The CS6401 is a programmable custom DSP optimized for echo cancellation in telephony applications.

Internally, the CS6401 is divided into a programmable DSP section and an adaptive filter coprocessor (AFP) unit. Boot interface and two serial ports are provided. Because the CS6401 is an application specific DSP designed to perform the echo-cancellation function, many of the features found in general purpose DSPs are not implemented in favor of performing the desired function as efficiently as possible. This efficiency is the reason that the CS6401 can provide high quality echo-cancellation at a much lower price than comparable general-purpose DSPs.

In the CS6401, digital audio data received via the serial port is processed by the AFP using the Normalized Least Mean Squared (NLMS) update algorithm to produce an echo estimate which is digitally subtracted by the DSP. This echo-cancelled data is sent back through the serial port back to a codec or supervisory DSP.

The programmable DSP executes 16.384 million instruction cycles every second when using a 32.768 MHz clock source. The DSP features 128 words of 16-bit Data RAM, 256 words of 16-bit Program ROM, and 768 words of 16-bit Program RAM. The Program ROM contains code for Linear/μ-Law conversions, multiply, divide, multiply/accumulates, and software initiated booting. The DSP usually runs the update control algorithms as well as supplementary suppression and other code.

The AFP implements 512 taps of adaptive FIR filtering using the NLMS algorithm, which provides 64 ms of echo cancellation at an 8 kHz sample rate. The AFP features 512 taps of 18-bit Coefficient RAM, 512 taps of 14-bit Buffer RAM, and the NLMS update and convolution engine. The AFP can also implement a split mode to create two distinct echo chancellors. This is especially useful in speakerphone applications that need both acoustic echo-cancellation and network echo-cancellation.

The Program RAM in the DSP is loaded with program code via the boot interface. The program code is provided by Crystal Semiconductor. For more details, see the CWECAXB data sheet. The boot interface loads the CS6401 program into the Program RAM from an external code source such as an EPROM, DSP, or microcontroller. The boot interface is capable of booting either serially or in parallel and can be either master of the boot process or slave. After the boot is complete, the boot interface is available as general purpose inputs and outputs to the CS6401. There are eight inputs and twelve outputs in the boot interface.

The serial interface provides two channels of data for the CS6401. The serial interface has four modes with master/slave options. It can directly interface to popular single-channel or dual channel codecs, as well as most general-purpose DSPs.

Echo Cancellation Overview

A block diagram of a situation that requires an echo-canceller is shown below in Figure 5. A training signal is applied at FE_IN and the desired signal at FE_OUT is S(t). With no echo-canceller in the system, the signal at FE_OUT is S(t)+H*FE_IN, which has the unwanted component of FE_IN. The echo canceller filter must adapt itself to appear equivalent to the path response, H. Then, when the echo canceller is active, the signal at FE_OUT will be S(t) + H*FE_IN - H*FE_IN, or just S(t).

A hands-free phone is a good practical example of a situation that would benefit from an echo-canceller. H would represent the room response from speaker to microphone and S(t) would be the talker on the hands-free phone. The talker at FE_IN does not want to hear his own voice at FE_OUT, he should only hear S(t). When converged, or fully adapted, the echo canceller's path estimate EC should be the same as the path response between the microphone and speaker, H. Ideally, none of FE_IN will be perceived at FE_OUT, and so full-duplex hands-free communication is possible.

SYSTEM OVERVIEW

The CS6401 is meant to be used as part of a larger audio-processing system. There are several possible permutations of system configurations that depend to a large degree on the application. Typical applications include: network echo-cancellation of time-division multiplexed PCM data, analog speakerphone, digital speakerphone, and audio for video-conferencing.

A typical connection diagram for the majority of applications is shown in Figure 6. Note that the system requirements will dictate what is connected to the serial ports and boot interface. For example, a telephone network echo-canceller would typically connect the serial port to a network backplane. An analog speakerphone would likely connect the serial port to either two single-channel codecs or one dual-channel codec and it would boot from a ROM. The video-conferencing application may have one serial port connected to a single channel codec, the other serial port connected to a host processor, and boot from the host processor. The configuration depends on the application.

CS6401 SERIAL INTERFACE OVERVIEW

The CS6401 has two serial ports, Synchronous Serial Interface #1 (SSI1) and Synchronous Serial Interface #2 (SSI2), which can be used to interface to a variety of peripherals including popular codecs and DSPs. Each serial port has its own Serial Data Output (SDO), Serial Data Input (SDI), Synchronize Signal (SYNC), and Delayed Synchronize Signal (SYNCO), but both share the common serial bit clock SCLK.

SDO is changed on the rising edge of SCLK while SDI is sampled on the falling edge of SCLK. The SYNC signal may be either a pulse or a frame type depending on the state of the SYNCP pin. This will be explained in greater detail in the discussion of serial modes below. The SYNCO pins are provided for use in Time-Slot Allocation Circuit (TSAC) applications (see serial mode E for details). The SYNCO pin outputs a copy of the SYNC signal received by the CS6401 delayed by 8 SCLK periods. The CS6401 can thus be daisy chained for subsequent time slots on the serial bus given only one external SYNC.

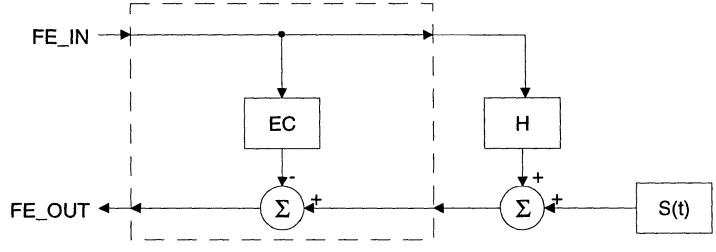


Figure 5. Echo Canceller Path

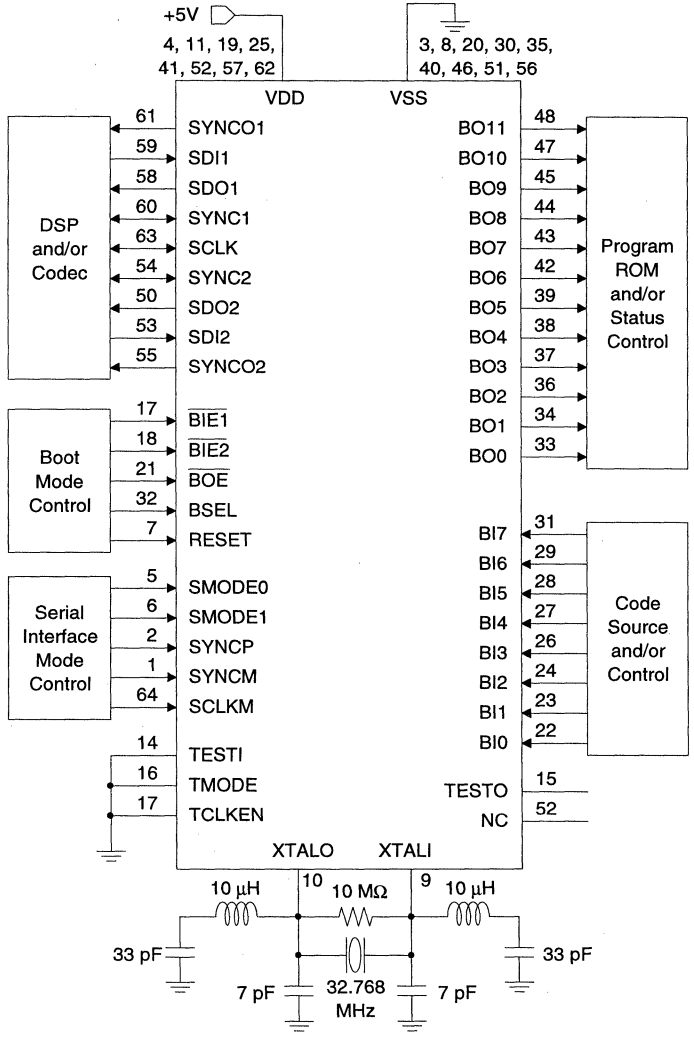


Figure 6. Typical Connection Diagram

The SCLKM pin determines whether or not the CS6401 is the SCLK source. If SCLKM is high, the CS6401 is the SCLK master. Similarly, if SYNCM is high, the CS6401 is the SYNC master. SYNCP determines whether the SYNC signal is a frame-type or a pulse type. If SYNCP is low, the SYNC signal will be a frame-type, high for the valid data bits and low for the remaining bits. If SYNCP is high, the SYNC signal will be a pulse-type. The serial mode determines the polarity of the pulse: SYNC is pulsed low in SM0 and high in SM1. The pulse duration is one SCLK period and the pulse occurs just prior to the start of a frame of serial data (depends on the serial mode, see below).

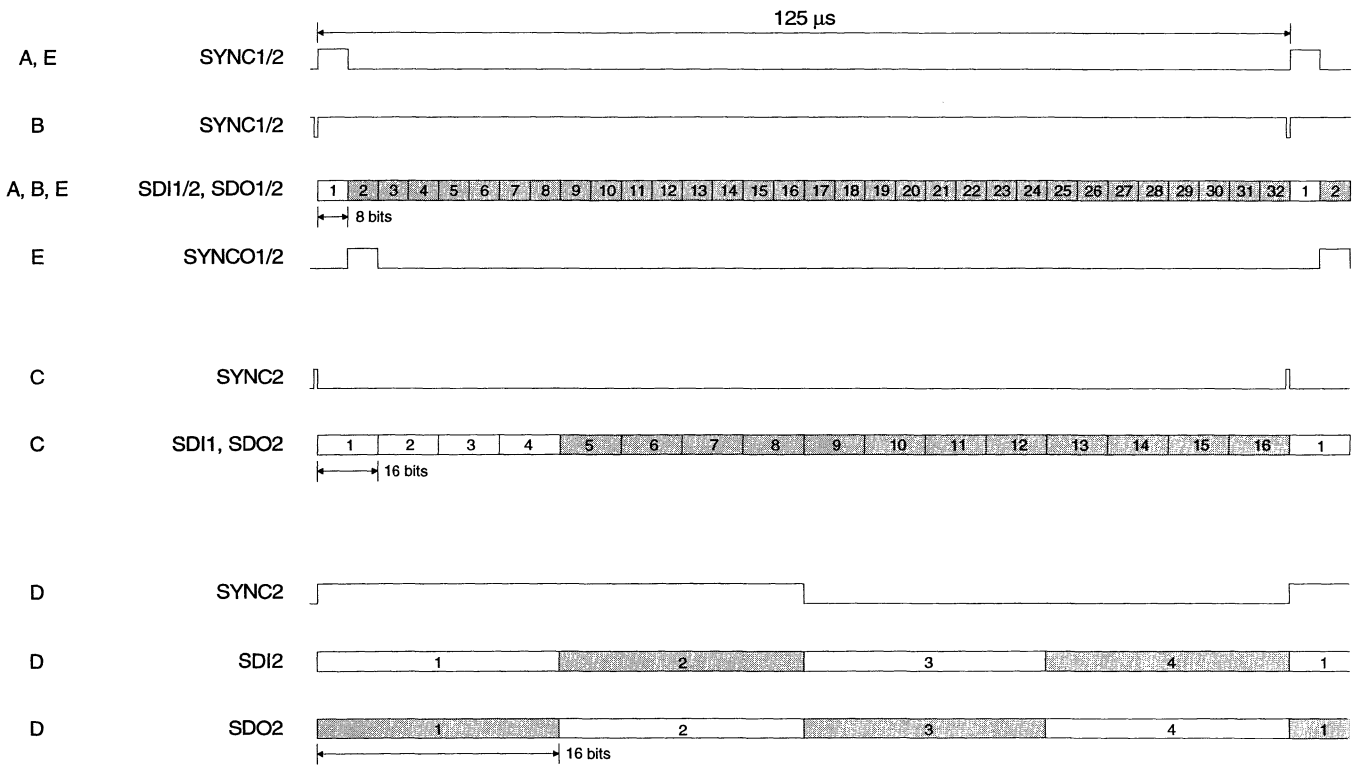


Figure 7. Serial Modes Overview

CS6401 SERIAL INTERFACE MODES

The CS6401 supports 5 serial port modes. The different serial modes allow connectivity to many popular codecs and DSPs. Serial mode A and serial mode B are 8-bit modes which interface to popular codecs and DSPs. Serial mode C uses SSI2 to interface to Crystal's popular CS4216 dual-channel codec. Serial mode D interfaces to a 16-bit dual-channel codec. Serial mode E is used for 8-bit TSAC interfaces.

Serial Mode:	A	B	C	D	E
SMODE0	0	0	1	0	1
SMODE1	0	0	0	1	1
SCLKM	1	0	1	1	0
SYNCM	1	1/0	1	1	0
SYNCP	0	1	1	0	0
Bits	8	8	16	16	8
Ports	1,2	1,2	2	2	1,2
SYNCO	no	no	no	no	yes

In Serial Mode A, both SSI1 and SSI2 are active. SCLK outputs at 2.048 MHz and SYNC1 and SYNC2 are frame-type synchronization signals (high while the 8-bit data is valid (8 SCLK periods)). The timing relationships for this mode are shown in Figure 8.

Serial Mode B is detailed in Figure 9. SCLK is an input at 2.048 MHz and SYNC1 and SYNC2 are either both inputs or both outputs. The synchronization signals in this mode are the pulse-type: they are always high except for the SCLK period just prior to the 8-bit data being valid.

Serial Mode C, whose timings are shown in Figure 10, is meant to connect to a CS4216 in SM3 in slave mode with 256 bits per frame, sampling at 8 kHz through SSI2. SCLK again outputs a 2.048 MHz clock and can be used as the master clock of the codec. SYNC2 goes high for one SCLK period just prior to the 16-bit stereo data being valid. Note that there is status and control

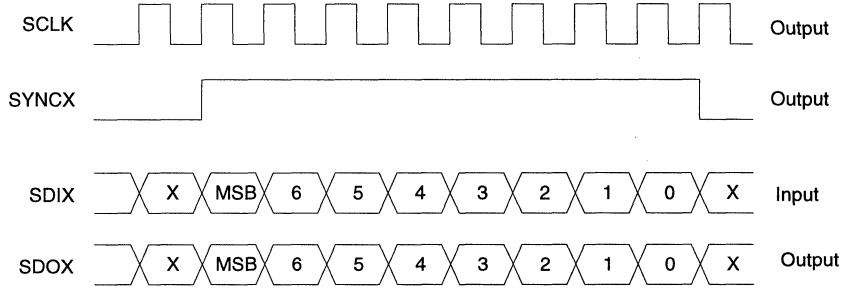


Figure 8. Serial Mode A

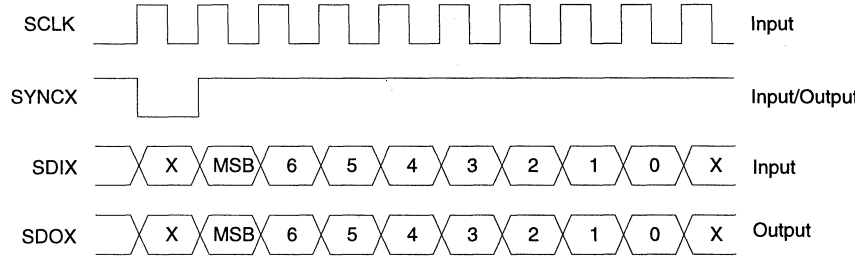


Figure 9. Serial Mode B

data for the CS4216 passed through the serial port as well in this mode. For more information on this Serial Mode, consult the CS4216 data sheet. This mode can be used to implement 64 bit data transfers as long as the timing relationships are maintained (so the CS6401 can communicate with the CS4215 as well).

Figure 11 gives timing relationships for Serial Mode D where SCLK now changes to 512 kHz. SYNC1 provides a 2.048 MHz output that may be used as a master clock. SDI1 and SDO1 are inactive. SYNC2 is an 8 kHz, 50% duty cycle square wave that is high for 16-bit data valid on one channel of a stereo ADC and DAC, and low for the other channel. Note that the first 16 bits of data (after a SYNC2 edge) at SDI2 are valid and the next 16 are ignored. Similarly the first 16 bits of SDO2 should be ignored while the later 16 bits are valid. This mode can be used to interface the CS6401 to the CS5336 ADC and CS4328 DAC.

Serial Mode E is to be used for TSAC applications. In this mode, SCLK and SYNC1 and SYNC2 are all inputs. SCLK should receive a 2.048 MHz clock and SYNC1 and SYNC2 should be frame-type synchronization signals that are high while the data is valid. SYNCO1 and SYNCO2 output the framing signal for the next 8-bit timeslot. This mode is very similar to serial mode A, with the exception of the SYNCO signals and the directions of SCLK and the SYNC signals. The operation of this mode can be seen in Figure 12.

Currently the CS6401 only supports the five modes with SMODE0, SMODE1, SCLKM,

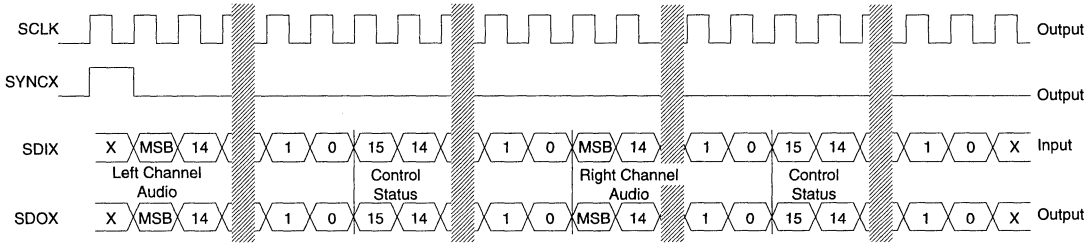


Figure 10. Serial Mode C: CS4216 SM3 Interface

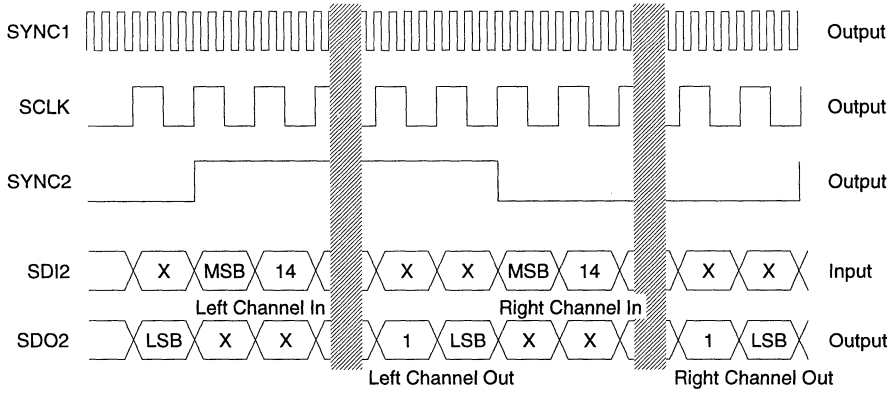


Figure 11. Serial Mode D: 16-bit codec interface

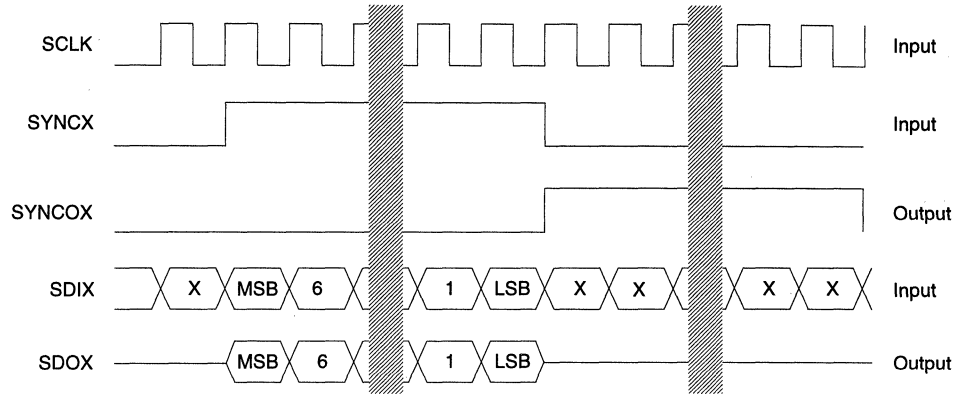


Figure 12. Serial Mode E: 8 bit codec interface

SYNCM, and SYNCP set as indicated. Note that since the CS6401 is programmable, the way it interprets what it reads from or writes to the serial ports is also programmable. If further flexibility is desired, please contact Crystal.

CS6401 BOOT INTERFACE OVERVIEW

The CS6401 has a very flexible boot interface which loads user code into its Program RAM. The CS6401 may be booted in either parallel mode, with 8 bits of instruction presented to BI0-7, or serial mode with serial data presented to BI7. The boot interface is configured using the BSEL, $\overline{\text{BIE1}}$, $\overline{\text{BIE2}}$, and $\overline{\text{BOE}}$ pins. The state of the BIE pins determine whether or not the CS6401 is master of the boot process. If either $\overline{\text{BIE1}}$ and $\overline{\text{BIE2}}$ are high after reset, the CS6401 boot interface is slaved to an external memory source such as a DSP or microcontroller. In this case, the data presented to the BI0-7 pins (parallel boot) or BI7 (serial boot) is latched on the falling edge of $\overline{\text{BIE1}}$ or $\overline{\text{BIE2}}$.

In the stand alone parallel boot mode (chosen when BSEL, $\overline{\text{BIE1}}$, and $\overline{\text{BIE2}}$ are low), the CS6401 clears all the BO pins after reset. The BO pins register the address in the parallel EPROM that the CS6401 is to boot from. The outputs from the EPROM should present their data to BI0-7. It is recommended that BO0 be used as an active-low chip select for the EPROM. In this manner the CS6401 can load 766 words of 16-bit instructions into its Program RAM one byte at a time by incrementing the address presented at BO1-11 and sampling the data at BI0-7 on the falling edge of BO0.

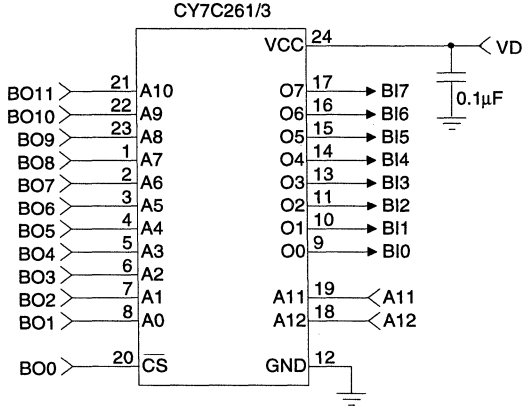


Figure 13. Standalone parallel boot from 8k EPROM

In the stand alone serial boot mode (differentiated from the previous mode by setting BSEL high), the CS6401 latches the data presented at BI7 on the falling edge of BO0. BO0 is connected to the clock input of the serial EPROM and BI7 is connected to the data output. The reset signal for the serial EPROM should be common with the CS6401 reset signal. The first rising edge of BO0 causes the first bit from the EPROM to be present at BI7. This bit is latched on the falling edge of BO0 and becomes the most significant bit of the first 16-bit word. After 16 bits are loaded, that word is loaded into the Program RAM, and the next 16 bits are loaded.

The boot modes where the CS6401 is the slave are very similar to the standalone modes except that the data is latched on the falling edge of either $\overline{\text{BIE}}$ pin. The BOx pins still drive out the addresses for a ROM, but these are generally ignored by the boot master. It is important to make sure that a ROM is not selected at this time, though, in order to avoid bus-contention problems. Note that the CS6401 begins executing as soon as it receives 1532 bytes of instructions.

Two $\overline{\text{BIE}}$ pins are provided to allow simultaneous booting of multiple CS6401s. In this case, one CS6401 is selected as the boot master and the rest as boot slaves. The BO0 of the master is fed to the $\overline{\text{BIE2}}$ of the slaves and the BIs are all ganged together. The master controls the EPROM accesses and all data is accessed at the same time via BO0/$\overline{\text{BIE2}}$. Simultaneous booting is possible in both serial and parallel modes. If the code source is a DSP or microcontroller, there will only be slave CS6401s.

Setting the $\overline{\text{BOE}}$ pin causes the BO pins to become high impedance. This pin can be used to

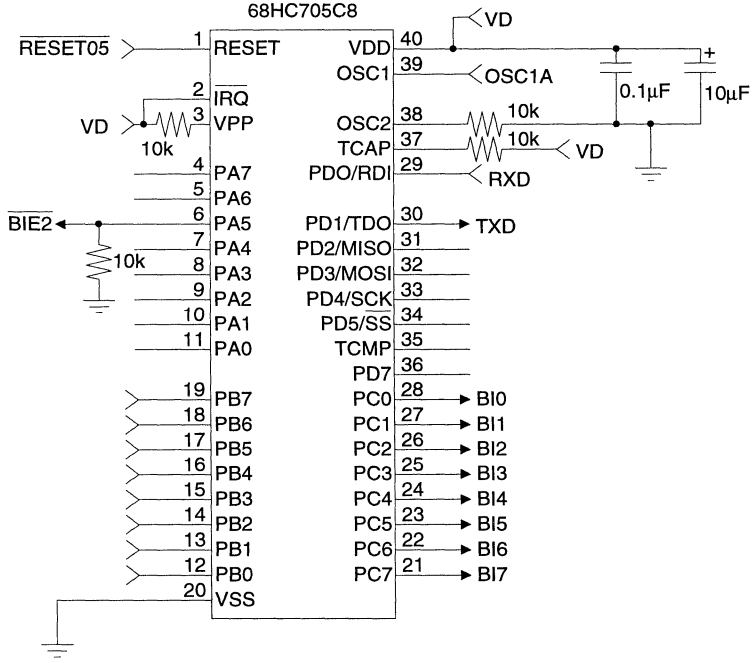
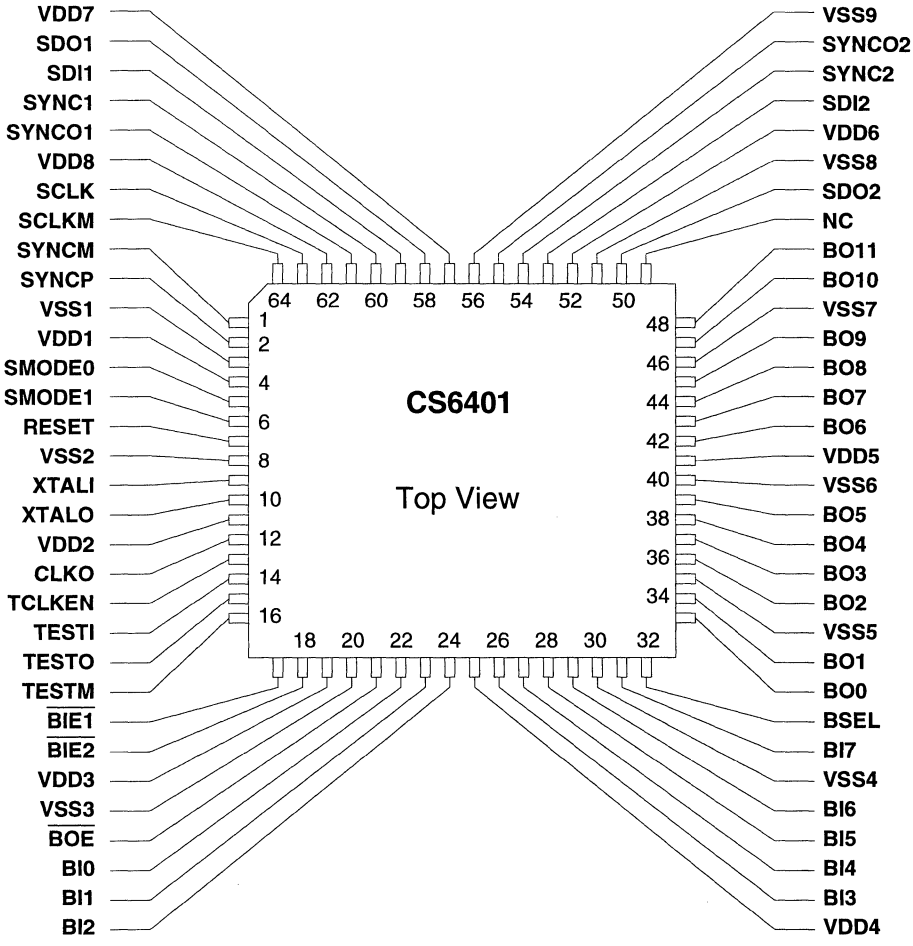


Figure 14. Microcontroller mastered parallel boot (See CDB6401 for more details).

allow a CS6401 to share a bus with another chip. When $\overline{BOE}$ is low, the BO pins are enabled and will act as outputs.

The boot sequence can be initiated either by re-setting the CS6401 or by a software call. The software call option is useful if the user wishes to boot different sets of code.

PIN DESCRIPTIONS



Power Supply Connections

VDD1 - VDD8 – Pins 4, 11, 19, 25, 41, 52, 57 and 62
+5V power supply pins

VSS1 - VSS9 – Pins 3, 8, 20, 30, 35, 40, 46, 51 and 56
0V ground pins

RESET - Active High Reset Input, Pin 7
Resets the AFP and serial ports when high. All RAM is unaffected. Fall of RESET initiates the boot process.

XTALI, XTALO - Crystal Input and Output, Pins 9 and 10

Input and output connections for 32.768 MHz crystal. Alternately, an external clock fed into XTALI may clock the CS6401.

CLKO - Master Clock Output, Pin 12

CLKO is Master Clock output, whose freqency is half that of the signal at XTALI. CLKO is always active while the chip is powered and clocked.

Serial Interface Pins

SDO1, SDO2 - Port 1 and Port 2 Serial Data Output, Pins 58 and 50

Data is output from serial port 1 and serial port 2 of the CS6401 via these pins.

SDI1, SDI2 - Port 1 and Port 2 Serial Data Input, Pins 59 and 53

Data is input to serial port 1 and serial port 2 of the CS6401 via these pins.

SYNC1, SYNC2 - Port 1 and Port 2 Synchronization Signal, Pins 60 and 54

Used to indicate the start of a word of serial data on serial port 1 and serial port 2.

SYNCO1, SYNCO2 - Port 1 and Port 2 Delayed Synchronization Output, Pins 61 and 55

Provides a SYNC signal delayed by 8 SCLK periods for TSAC applications. Active in serial mode 3.

SCLK - Serial Port Bit Clock, Pin 63

SCLK controls the digital data on SDO1 and SDO2 and latches the data on SDI1 and SDI2. SCLK is low while RESET is high.

SCLKM - Serial Clock Mode Select, Pin 64

SCLKM high makes the CS6401 output SCLK. SCLKM low makes the CS6401 slave to a supplied SCLK.

SYNCM - Synchronization Mode Select, Pin 1

SYNCM high makes the CS6401 output SYNC1 and SYNC2. SYNCM low makes the CS6401 accept external SYNC signals as inputs.

SYNCP - Synchronization Pulse Mode Select, Pin 2

SYNCP high makes the CS6401 produce a SYNC pulse of one SCLK period duration just prior to the start of a new word of data. SYNCP low makes the CS6401 frame each word with SYNC high while data is valid.

SMODE0, SMODE1 - Serial Mode Selects, Pins 5 and 6

Select the serial mode format of the data input to and output from the serial ports.

Boot/Control/Status Interface Pins

$\overline{\text{BIE1}}$, $\overline{\text{BIE2}}$ - Boot Interface Enables, Pins 17 and 18
After reset if either $\overline{\text{BIEx}}$ pin is low the Boot Interface is self-clocking, else it is slaved (to $\overline{\text{BIE1}}$ or $\overline{\text{BIE2}}$).

$\overline{\text{BOE}}$ - Boot Output Enable, Pin 21
Boot outputs are low impedance when low.

BI0-BI7 - Boot Inputs, Pins 22, 23, 24, 26, 27, 28, 29 and 31
Parallel or serial boot data input from EPROM and general purpose input after boot.

BO0-BO11 - Boot Outputs, Pins 33, 34, 36, 37, 38, 39, 42, 43, 44, 45, 47 and 48
Parallel boot address word for parallel EPROM, serial boot clock or output enable, and general purpose output after boot.

BSEL - Boot Mode Select, Pin 32
When BSEL is high, a serial boot is selected. When BSEL is low, a parallel boot is selected.

Test Interface Pins

TESTI - Scan Test Input, Pin 14
Keep grounded.

TESTO - Scan Test Output, Pin 15
Keep unconnected.

TESTM - Test Mode Select, Pin 16
Keep grounded.

TCLKEN - Test Clock Enable, Pin 13
Keep grounded.

Semiconductor Corporation

CDB6401

CS6401 Evaluation Board

Features

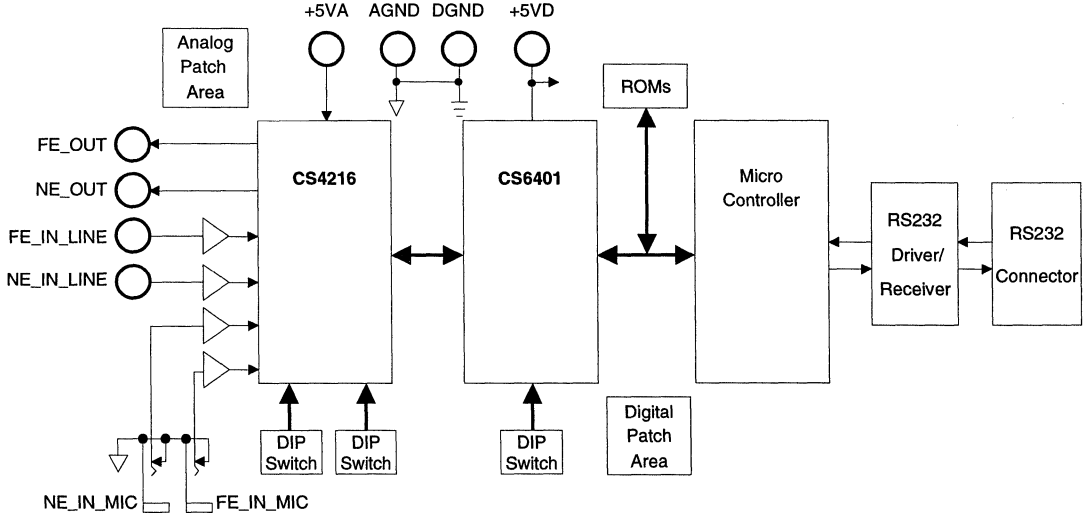
- On Board Microcontroller
- RS232 Serial Communications with Host PC
- High Quality Stereo Codec
- Microphone Pre-amplifiers
- Line Input Buffers
- Analog and Digital Patch Area

General Description

The CDB6401 allows an end-user to quickly integrate the CS6401 echo-canceller into a system and evaluate its performance. The board comes with a microcontroller and software to enable flexible setup and evaluation. Evaluation requires a +5V power supply and a Windows-capable personal computer with an available RS232 serial port. Connections for analog audio sources are provided on the board.

Also included is the CS4216 stereo audio codec which performs the data acquisition for the echo-canceller and which has such features as programmable gain and attenuation, clipping detectors, and a wide range of selectable sample rates.

ORDERING INFORMATION CDB6401



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

HARDWARE

Power Supply Circuitry

The CDB6401 power supply circuitry is shown in Figure 1. The evaluation board supports various power supply arrangements. The factory configuration powers the analog portion of the CS4216, along with input buffers, from the +5VA binding post, which needs a clean +5V supply. The digital portion of the CS4216 is factory configured to obtain power through a 2Ω resistor from the VA+ supply. The CS6401, microcontroller, and other logic obtain power from the +5VD binding post, which also needs +5V. Although binding posts exist for both analog and digital grounds, only one need be connected if a single power supply is used for both +5VA and +5VD. Note that the CS4216 resides entirely on the analog ground plane and close to the ground plane split, as recommended by the CS4216 Data Sheet. Also note that the two ground planes are connected near the two ground binding posts.

Space for a ferrite bead, L1, is provided so that the board may be modified to power the CS4216 from the digital supply. Selection of L1 will depend on the noise characteristics of the digital supply used.

Analog Inputs

There are two line-level analog inputs and two 1/4" microphone inputs on the CDB6401. The labels "FE" and "NE" stand for "near-end" and "far-end." In a typical acoustic echo-canceller application, there will be a speaker and microphone at the near-end. The CS6401 assumes the left channel to be the near-end and the right channel to be the far-end.

As shown in Figure 2, the line-level inputs go through a buffer which attenuates the input by 6 dB allowing a maximum input signal of $2V_{rms}$ to the evaluation board.

The microphone inputs are single-ended and are designed to work with both condenser and dynamic microphones. Figure 3 shows the microphone input buffer, which has a gain of 32 dB. Another 22 dB of programmable gain is available on the CS4216 should more gain be necessary.

An analog patch area is provided, complete with power and ground areas, for any additional analog circuitry that may be required. Thus, the customer can implement any custom input or output circuitry directly on the evaluation board.

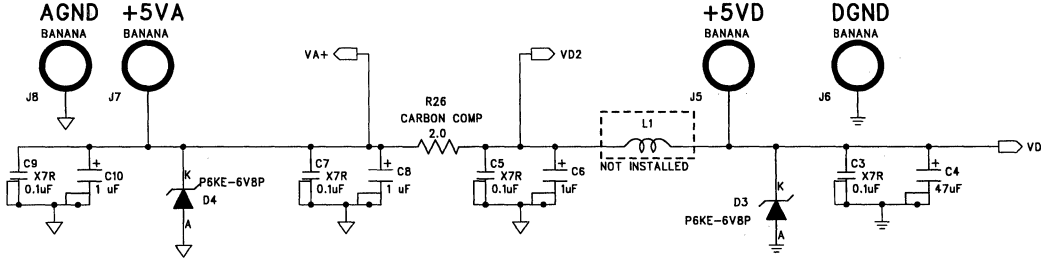


Figure 1. Power supply circuitry.

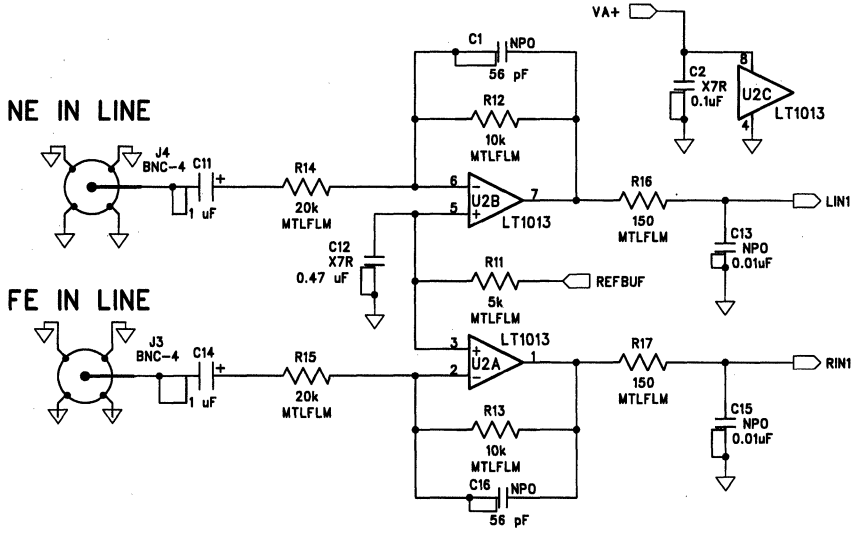


Figure 2. Line input buffers.

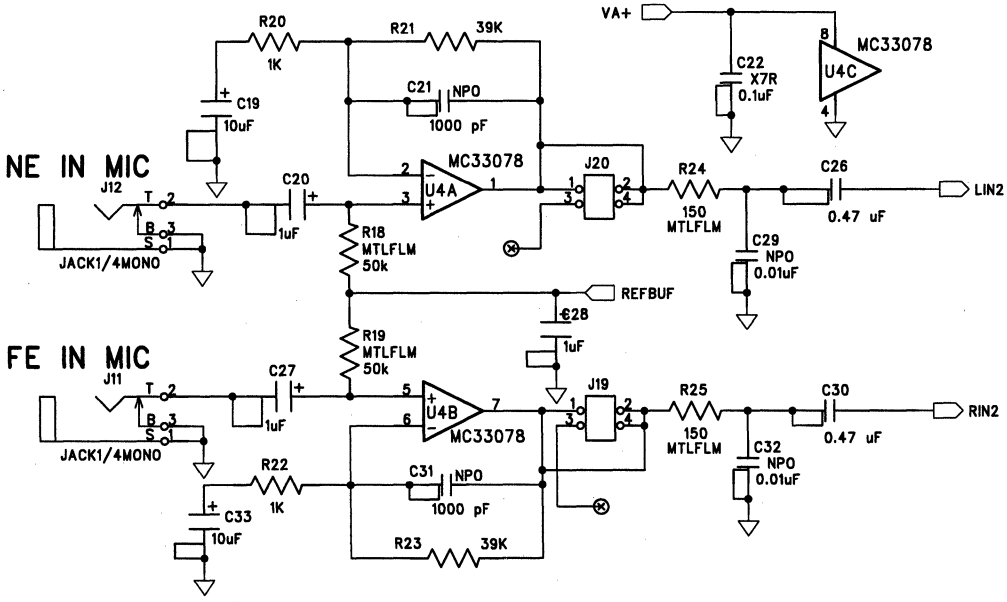


Figure 3. Microphone input buffers

Analog Outputs

The BNC's FE_OUT and NE_OUT are the filtered outputs of the CS4216. The line outputs can drive an impedance of 10kΩ or more, which is the typical input impedance of most audio equipment. Note that the outputs cannot drive a speaker directly and must have an amplifier if a speaker is required. Also note that the full-scale output from the CDB6401 will be $1V_{rms}$. These outputs are shown in Figure 4.

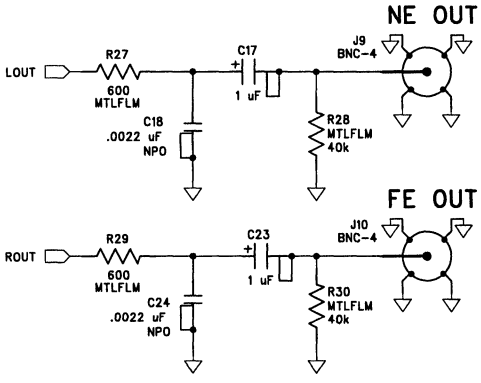


Figure 4. Line outputs.

Stereo Audio Codec

The schematic for the CS4216 stereo audio codec is shown in Figure 6. This codec handles the data conversion for the CS6401. It features 22.5 dB of programmable gain and 46.5 dB of programmable attenuation on each channel. In addition, status information is encoded in the serial data stream to indicate clipping and logic levels present at pins DI1 and DI2. These pins connect to DIP switches as do various mode setting switches to allow the program executing in the CS6401 to interact with the user. Note that the LED on the board is controlled by the CS4216 output pin DO1.

Echo Canceller

Figure 7 shows the CS6401 and all its associated circuitry. Note that the crystal oscillator circuitry which forces the crystal into a third-overtone mode of operation. The decoupling capacitors for the CS6401 are shown in Figure 8. Each power pin has its own decoupling capacitor. These are located as close as possible to the pins to ensure reliable operation.

The Boot Interface pins of the CS6401 connect both to the on-board microcontroller and to the ROM sockets. Every pin of the Serial Interface and Boot Interface has a test point for easy monitoring by oscilloscope or logic analyzer.

Clock Divider

The clock divider in Figure 5 takes the 16.384 MHz output from the CS6401 CLKO pin and divides it by four in order to generate the 4.096 MHz microcontroller clock. This is done to ensure that all the clocks in the system have similar phase relationships in order to minimize noise.

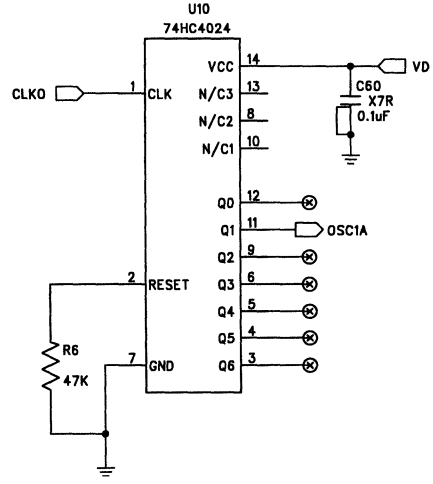


Figure 5. Clock divider.

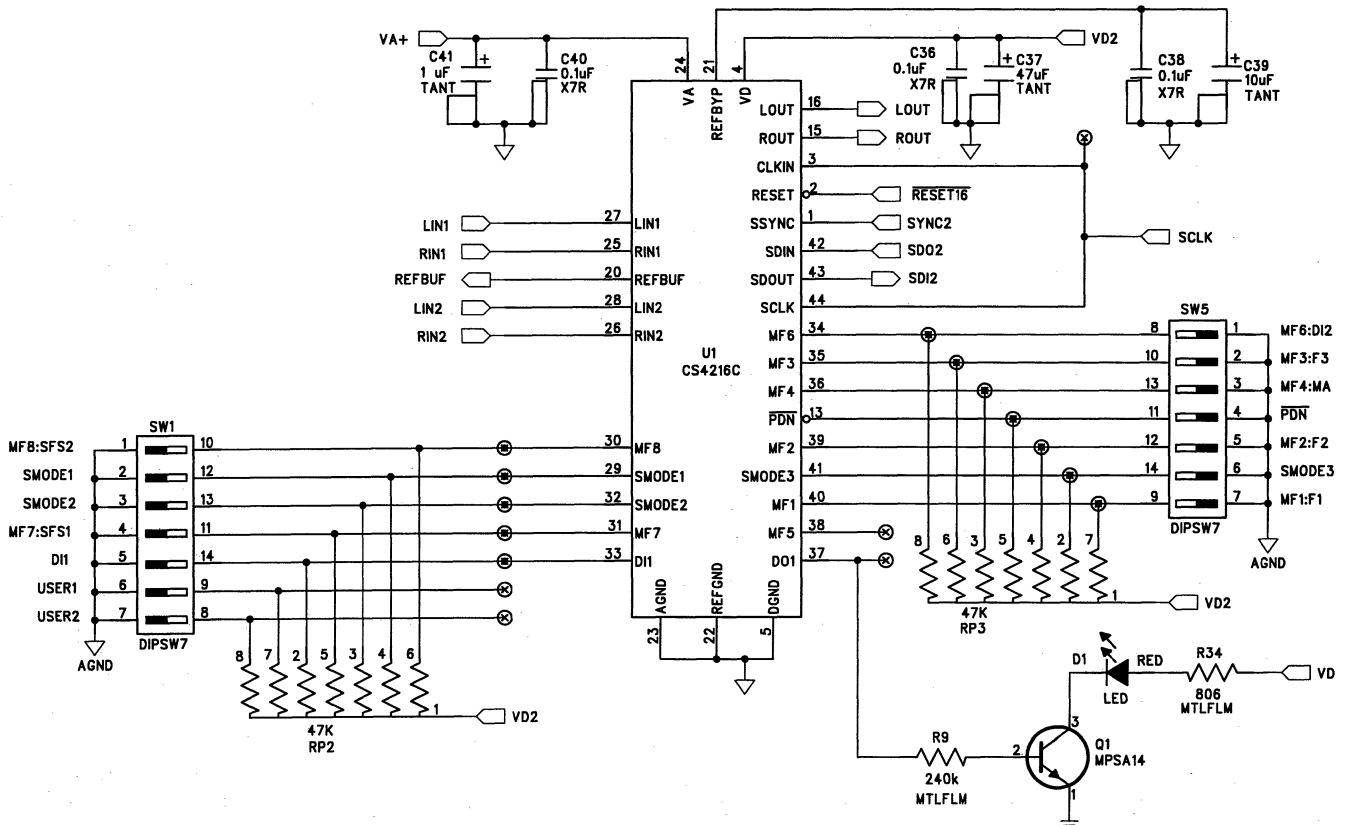


Figure 6. CS4216 connection diagram.

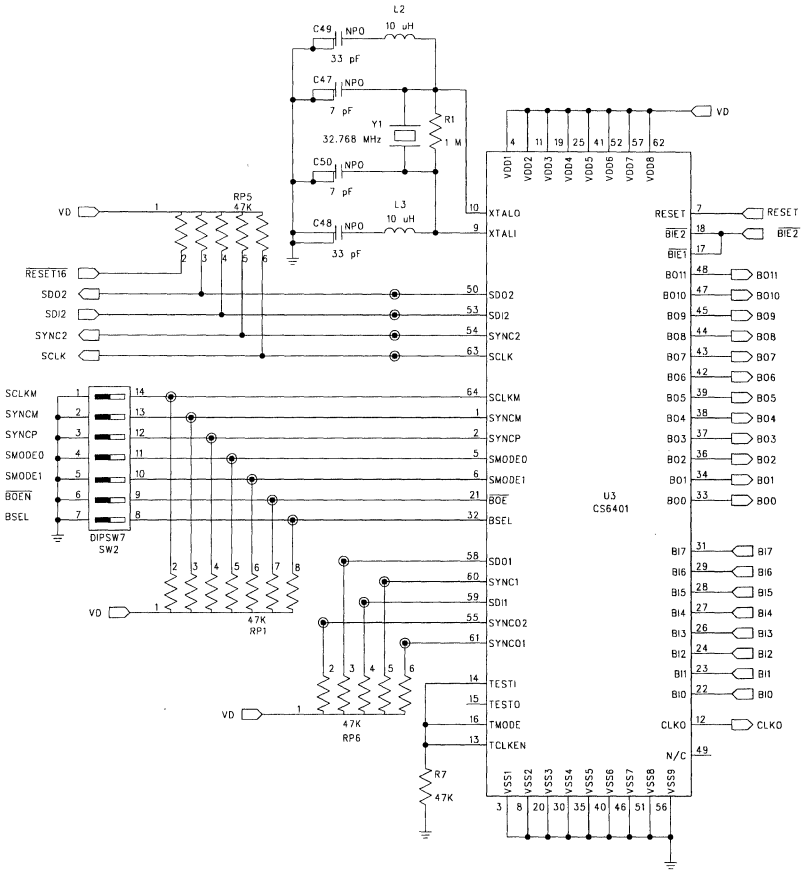


Figure 7. CS6401 connection diagram.

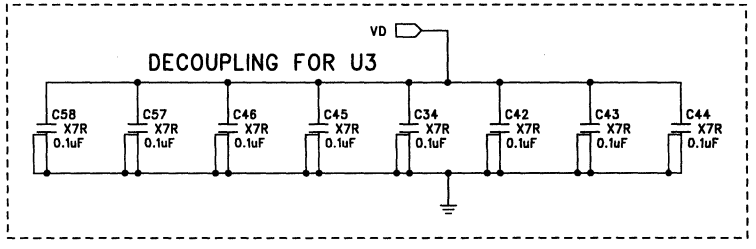


Figure 8. Decoupling capacitors for the CS6401.

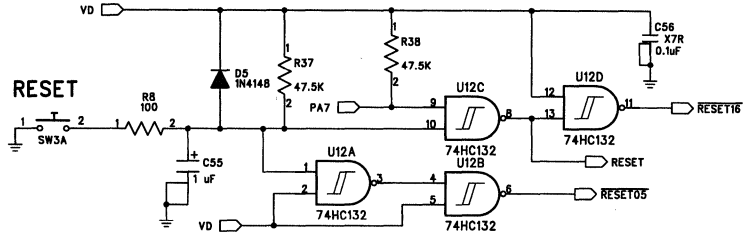


Figure 9. Reset circuitry.

Reset Circuitry

The reset circuit for the CDB6401 consists of four Schmitt-triggered NAND gates. The push-button will reset the microcontroller, the CS4216, and the CS6401. Alternatively, when the microcontroller is controlling the boot process, it needs to be able to reset the CS4216 and CS6401 only. The circuit in Figure 9 implements these functions.

RS232 Serial Communication Port

The CDB6401 is equipped with an RS232 port (see Figure 10) and a microcontroller (detailed in Figure 11) to allow the CS6401 to be controlled externally. The communication protocol is discussed in a later section entitled "Communication Protocol." Should the users desire to use their own microcontroller for the task, the microcontroller source code is provided in the section "Microcontroller Source Code." The transfers are set for 9600 baud with eight data bits, no parity, and one stop bit.

The microcontroller code allows a user to boot a program into the CS6401, echo a byte for connection validation, and read or write any data memory location on the CS6401 in real-time.

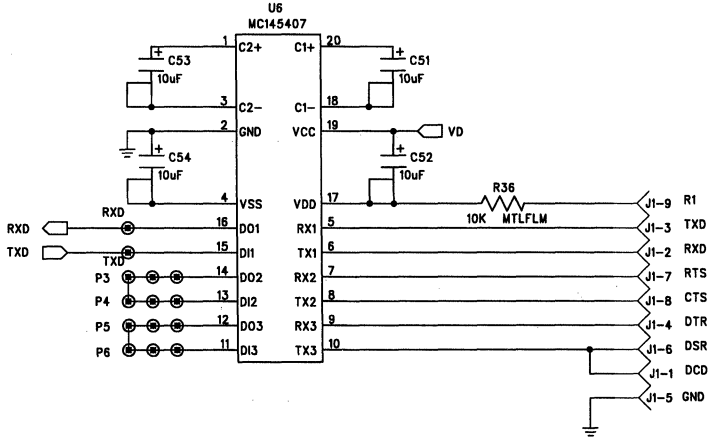


Figure 10. RS232 level shifter circuitry.

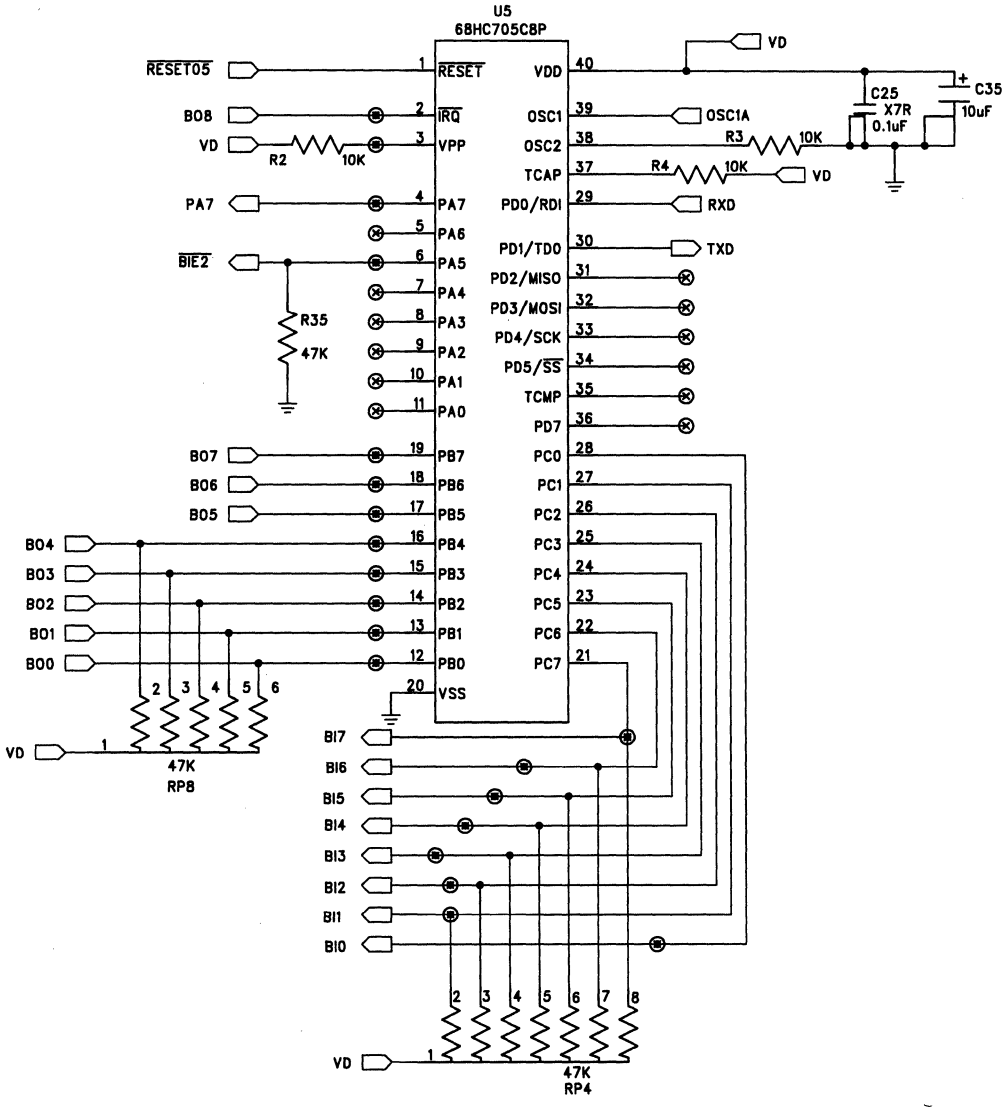


Figure 11. Microcontroller connection diagram.

SW2 - CS6401		OFF	ON	Description
BSEL	ON	Serial	Parallel	Selects boot type
$\overline{\text{BOEN}}$	ON	Disabled	Enabled	Enable BO pins
SMODE1	ON	Change serial mode of CS6401 if interfacing to a codec other than the CS4216 or to an external DSP		
SMODE0	OFF			
SYNCP	OFF	Pulse	Frame	SYNC type
SYNCM	OFF	Output	Input	SYNC direction
SCLKM	OFF	Output	Input	SCLK direction

SW5 - CS4216		OFF	ON	Description
MF1:F1	OFF	Together with MF2:F2 determines the number of bits per serial frame		
SMODE3	ON	Together with SMODE1 and SMODE2 set the CS4216 serial mode		
MF2:F2	ON	Together with MF1:F1 determines the number of bits per serial frame		
$\overline{\text{PDN}}$	OFF	Active	Sleep	Power down the CS4216
MF4:MA	ON	Master	Slave	Master/slave the codec
MF3:F3	XX	XX	XX	Algorithm control switch 3 in CS4216 SM3 slave
MF6:DI2	XX	XX	XX	Algorithm control switch 2

SW1 - CS4216		OFF	ON	Description
USER2	XX	XX	XX	Not connected
USER1	XX	XX	XX	Not connected
DI1	XX	XX	XX	Algorithm control switch 1
MF7:SFS1	ON	Together with MF8:SFS2 determines the active sub-frame		
SMODE2	OFF	Together with SMODE3 set the CS4216 serial mode. See CS4216 data sheet for more details		
SMODE1	ON			
MF8:SFS2	ON	Together with MF7:SFS1 determines the active sub-frame		

Table 1. DIP switch descriptions.

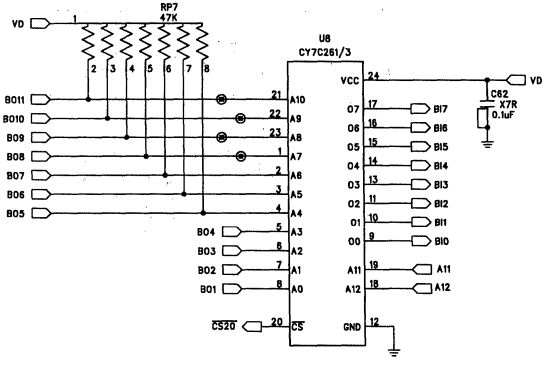


Figure 12. Parallel EPROM connection diagram.

DIP Switches

The DIP switches on the CDB6401 allow the users to configure the CS6401 and CS4216 in any manner desired. Each of the switches is labeled according to the pin name in the appropriate data sheet. Note that the CS4216 DIP switches (SW1 and SW5) have names which assume Serial Mode 3. Table 1 summarizes of what each of the switches controls.

Factory defaults are shown immediately to the right of the switch name in Table 1. "XX" represents a "don't care" case. The ON position of the switch yields a voltage of zero volts at the corresponding test point.

Note that DI1 and DI2 are used for real-time algorithm control by the CDB6401 echo-canceller code. Their functions will be detailed in code-specific addenda to this document. The DIP switch labeled MF7:SFS2 should be MF8:SFS2.

ROM Sockets

The evaluation board can also be operated in stand-alone mode provided that there is an external ROM on the board. The board does not ship with a ROM, since the microcontroller provides greater flexibility for evaluation.

U8 and U9 are sockets provided for ROMs connected as shown in Figures 12 and 13. U8 is meant to accommodate an 8K by 8 parallel ROM, specifically, the CY7C261/3 from Cypress Semiconductor. U9 is for a serial ROM, the XC1736 from Xylinx. These ROMs allow for stand-alone operation of the CDB6401. The microcontroller should be removed if a ROM is socketed to avoid contention problems that could damage both parts.

Headers P7 and P8 control the enable logic for the serial ROM and parallel ROM, respectively. The "EPROM ACCESS SEQ" header J13 allows

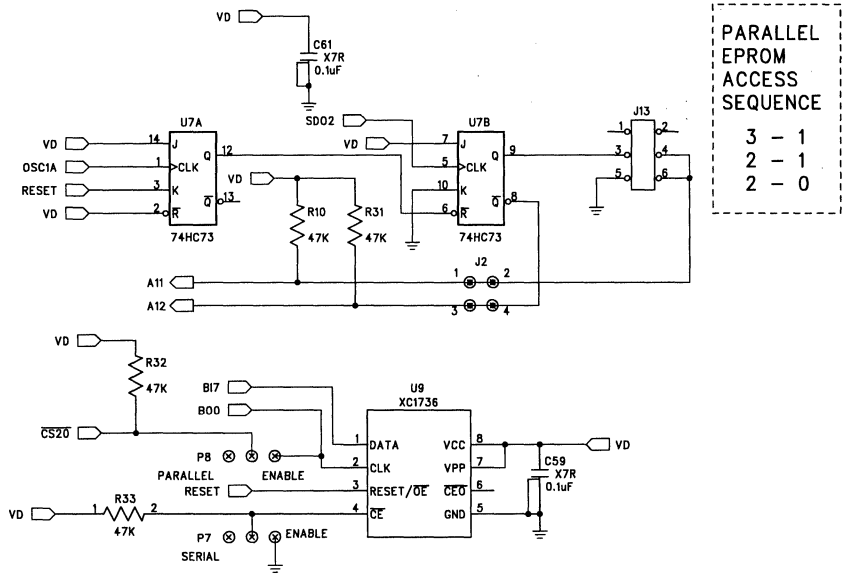


Figure 13. J-K flip flop circuit and serial EPROM connection diagram.

the booting of multiple programs from the parallel ROM, such as Boot1 and Boot2, using the J-K flip-flop circuit in Figure 13. Since the program memory space in the CS6401 is 1532 bytes, an 8K by 8 ROM can be segmented to contain four programs. The segments are defined as: 0 (0 to 2K), 1 (2K to 4K), 2 (4K to 6K), and 3 (6K to 8K). The placement of the header defines the sequence of the segment access upon boot. The multi-program boot is initiated by pressing the RESET button.

Note that ROM code varies slightly from the standard ".hex" files that are shipped with the evaluation board. For ROM versions of the ".hex" files, please contact the factory.

Minimum Components

The bold white line on the evaluation board denotes the minimum component set necessary to implement an echo-cancellation system. The CS6401, CS4216, and the parallel EPROM socket should be the only required components other than a handful of resistors and capacitors, as well as the crystal and associated circuitry. Using surface mount components with no sockets can result in a very tiny footprint for an echo-canceller.

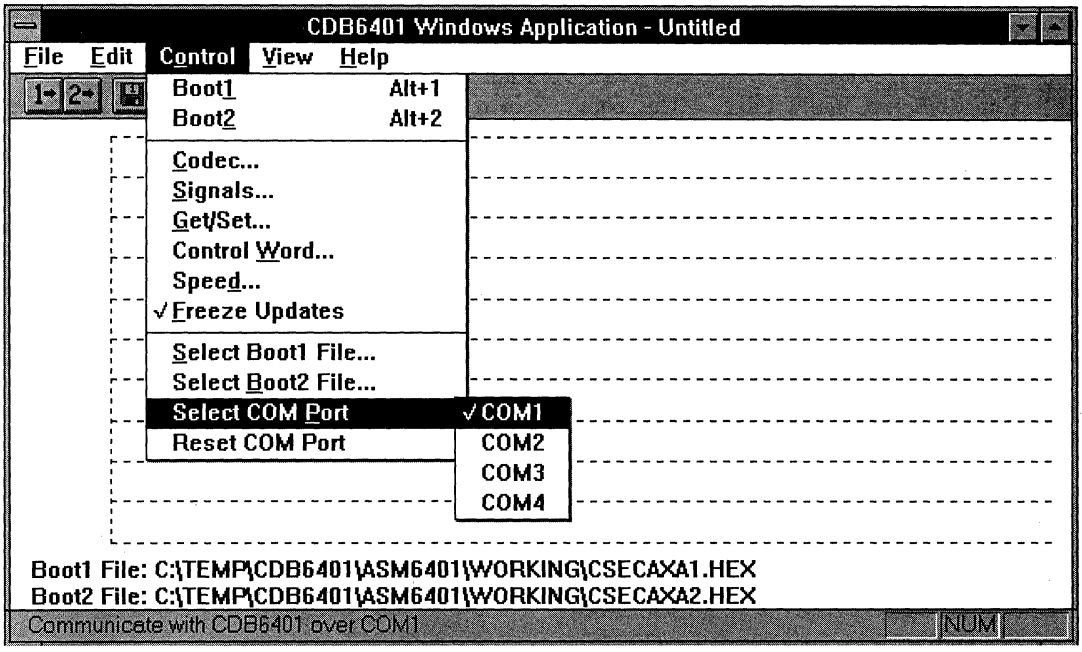


Figure 14. The CDB6401 Windows Application display.

SOFTWARE

Windows Code

Minimum system requirements:

Windows-capable PC
1 MB free hard drive space,
Tested on 486DX33 with 8MB RAM
Tested on 386DX25 with 4MB RAM

The Windows application, CDB6401.EXE, was created specifically to provide an easy-to-use interface to the CDB6401. This software allows an evaluator to boot echo-canceller code through the RS232 port of a PC and gather performance data while the echo-canceller is running. This allows for real-time measurement of echo-return loss enhancement and convergence time of the canceller.

In addition the control registers of the CS4216 are accessible through a dialog box. Thus, gain and attenuation levels for both the near and far-ends can be independently adjusted in real-time.

A menu by menu explanation of the software follows.

File Menu - This menu is not fully implemented and is therefore not supported. Future versions of the software may enable these functions reliably.

Edit Menu - This menu is not implemented. It exists only for coherence with standards set by Windows.

Control/Boot1 - This command causes the file labeled Boot1, initially selected by the **Control/Select Boot1 File...** menu item to be booted into the CDB6401. If no Boot1 file is selected, the **Control/Select Boot1 File...** dialog is brought up.

Control/Boot2 - Same as above except for the file that is booted: Boot2.

Control/Select Boot1 File... - This command brings up the standard Windows "File Open" dialog box. Its purpose is to select the Boot1 file.

Control/Select Boot2 File... - Same as above for Boot2 file.

Control/Codec... - This command brings up the **Codec Parameters** dialog box if a valid RS232 connection has already been established, and boot 1 and boot 2 are executing. The command causes the codec control registers on the CS6401 to be read in order to present the current state of the codec upon initialization of the dialog box. Once the dialog box is up, the user can make any desired changes to the settings. Clicking "Cancel" will cause the dialog to close without sending the changes to the CS6401. Clicking "OK" will update the registers in the CS6401, if necessary. Note that this means that no changes in gain, attenuation, input, or other will take place until the dialog box is closed.

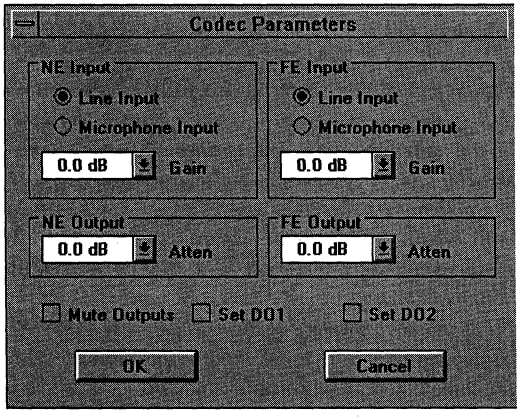


Figure 15. The Codec Parameters dialog box.

Control/Signals... - This command is the most useful to the evaluator. It allows the evaluator to look at signals gathered from the CS6401 in real-time. There are four lines: black, red, blue, and green which can be set to represent any variable in the list box. The lines can also be independently represented on linear signed, linear unsigned, or decibel scales. Also, the values retrieved can be independently scaled by an integer amount between one and one thousand. This command assumes a boot file has already been selected, and boot 1 and boot 2 are executing. If a line is to be omitted from the display, be sure that it's list box entry is "-NONE-", the default.

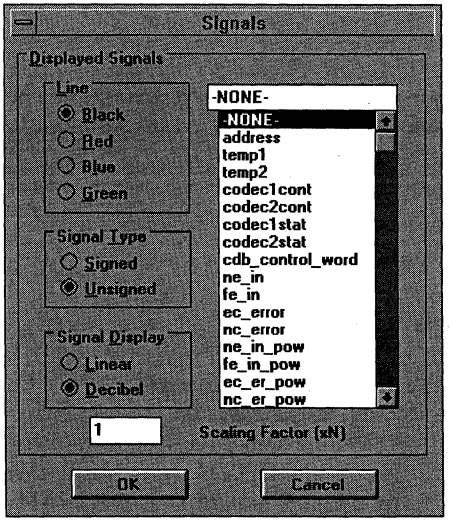


Figure 16. The Signals dialog box.

Control/Get/Set... - This command brings up the **Get/Set EC Parameters** dialog box. This allows the user to scroll through any of the listed variables (boot 1 and boot 2 must be downloaded prior to calling this function) and **Get** the hexadecimal value or **Set** the variable to

a particular value. This is mainly of use to the factory in code debugging.

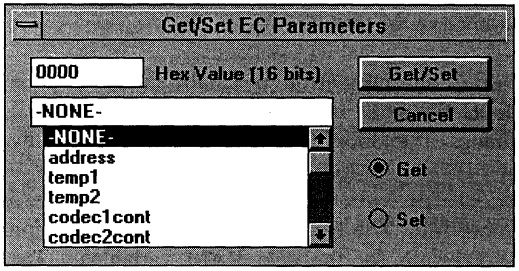


Figure 17. The Get/Set EC Parameters dialog box.

Control/Control Word... - This dialog box gives the user some control of algorithmic functions in order to tailor them more appropriately to a specific application. The text will vary.

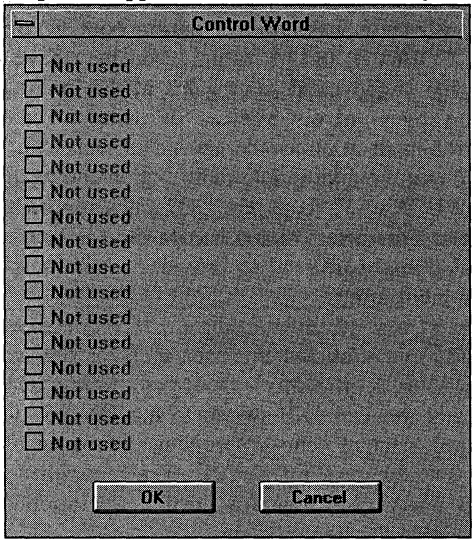


Figure 18. The Control Word dialog box.

Control/Speed... - This command allows the evaluator to change three parameters about the display: the total number of samples displayed, the number of samples collected before a screen update, and the parameter sample rate in milliseconds of the PC. Extending the total number of samples displayed allows for a higher resolution display, at the expense of memory. Extending the number of samples collected before a screen update allows even higher resolution, at the expense of jerkiness of the strip chart display. This improvement in resolution is important on slower computers that take a long time to update the screen. Reducing the sample rate will have no effect beyond a certain point. The update rate will be defined by the speed of the evaluating PC.

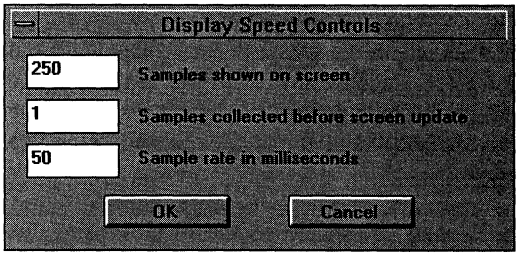


Figure 19. The Display Speed Controls dialog box.

Control/Freeze Updates - This command will halt the screen update and data acquisition from the evaluation board. This state is entered every time the CDB6401 is booted in order to prevent communication errors from locking up the computer. Updates should not be unfrozen until the Boot2 program is executing.

Control/Select COM Port - Leads to a submenu with a list of COM ports 1-4. The current selection is checked. To change the current selection, highlight it. If a connection was not established, a message box will tell you. Possible causes include case, the power to the evaluation board may not be on, or the microcontroller might need to be reset.

Control/Reset COM Port - This command will reset the currently selected RS232 port and send the echo flag to the CDB6401. If the flag is not received at host PC, an error condition exists that must be fixed before evaluation can continue.

6

View Menu - This menu is not supported and is included to conform to Windows standards.

Help/About CDB6401... - This menu item calls an **About** dialog box.

Help/Support... - Displays a dialog box containing customer support information.

The Display

The CDB6401 display window consists of a set of axes where the y-axis denotes magnitude and the x-axis denotes time, with t=0 at the extreme left. Also included in the default display is the current Boot1 and Boot2 files named below the graph.

As signals are added to the display using the **Control/Signals...** mechanism, the variable being viewed, as well as the range of values is displayed vertically to the left of the graph in the color of the line. The y-axis is divided into ten divisions to facilitate estimation of values. The x-axis scale depends on factors set in the **Control/Speed...** menu and system hardware and, therefore, is not numerically demarcated.

Note that the display will continue to be updated continuously except in the case when **Control/Get/Set...** is called in which case, the display is halted until the dialog box is closed or **Control/Freeze Updates** is invoked.

USING THE CDB6401 EVALUATION SYSTEM

Setup

Install the software onto the PC by following the included instructions. Connect the CDB6401 to a +5V power supply. Connect the PC to the CDB6401 with the supplied serial port cable. Power up the evaluation board. Start the CDB6401.EXE application. If there is an error message when the application starts up, try changing the COM port. If the COM port is correct, then try "Control/Reset COM Port." If this also fails, try connecting the CDB6401 to another COM port.

Once communication is established, select a Boot1 file using the **Control/Select Boot1 File...** dialog. The Boot1 file will be a filename ending in "1," for example "CWECAXA1.hex" is a Boot1 file, whereas "CWECAXA2.hex" is a Boot2 file. The Boot1 file contains initialization information for the data RAM variables. The Boot2 file is the actual executable of the echo-canceller.

Next, select a Boot2 file and boot them both by selecting **Control/Boot1** followed by **Control/Boot2**. At this point the program will have been booted into the CS6401 and will be executing. If there was an error during boot, RESET the CDB6401 and try again. You may have to set the codec inputs and gains at this point by choosing **Control/Codec...**. If using a microphone input at either the far-end or near-end, be sure that the appropriate radio button shows this. "CWECAXA2" maps the DO1 click-box in the Codec Parameters dialog box to the LED on the evaluation board, and so provides a good test of communications.

CWECAXA allows the user to clear the echo canceller coefficients (thereby disabling it) by setting the DI1 DIP switch to the ON position. Supplementary echo-suppression can be enabled by switching MF6:DI2 ON. The recommended DIP switch settings for normal operation are shown in the figure below.

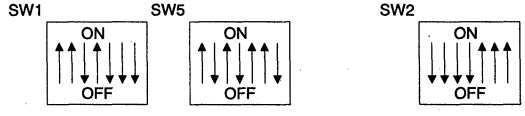


Figure 20. Recommended DIP Switch Settings.

Setting the Gains

The drop down list of decibel values will select the gain for the appropriate end, but the balance must be correct for the echo-canceller to work properly. The echo-canceller must not overrange or it will not work. The Normalized Least-Mean-Squares (NLMS) algorithm is linear in nature and any nonlinearity in the system (including distortion and clipping) will limit the performance of the echo-canceller. However, at the other extreme, since the CS6401 is a fixed-point machine, as the signal level decreases, the quantization error relative to that signal increases, which leads to a loss in performance. The goal of setting the gains is to maximize dynamic range while maintaining acceptable signal levels.

Try to set the gains as follows:

1) Turn the echo-canceller off by setting DI1 on SW1 to ON.

2) Connect a sine-wave generator to NE_IN_LINE (with near-end input gain set to 0dB). Set the near-end input source to be Line Input. Send 2Vrms out of the sine-wave generator (after the input buffer, this should be full scale for the CS4216).

3) Using the **Control/Signals...** menu, select "ne_in_pow" as the black line in "Decibel" format. Signed or unsigned is irrelevant for decibel format. After clicking "OK," the signal should be displayed. Record the level of ne_in_pow.

4) Disconnect from NE_IN_LINE and attach the full scale sine-wave to FE_IN_LINE. Set the far-end input source to Line Input and the near-end input source to whatever your microphone is connected to. Again, far-end gain should be 0dB. Connect your speaker amplifier to NE_OUT.

5) Adjust the speaker amplifier gain so that the volume at the speaker is the loudest that you would ever want it to be.

6) Using the **Control/Signals...** menu, select "ne_in_pow" as the black line in "Decibel" format. Signed or unsigned is irrelevant for decibel format. Select "fe_in_pow" as the red line, also in "Decibel" format. After clicking "OK," the two signals should be displayed.

7) Adjust the near-end input gain so that the current ne_in_pow line is at about the same level or a little lower than the line recorded in step 3.

8) Adjust the output gain of the far-end output amplifier so that it is at the maximum comfortable listening level.

9) Replace the sine-wave generator with the desired far-end source. Adjust the far-end gain so that the volume at the near-end is acceptable.

10) The gains should now be correctly set.

Note: After this process, any volume changes should be made using the Codec Parameters dialog box, not with the external amplifiers. If further volume control is required, change the gain at FE_IN to maintain good echo-canceller performance.

Measuring Performance

The two parameters, "ne_in_pow" and "ec_er_pow" will give most performance information. Set the black line to display ne_in_pow and the red line to display ec_er_pow, both in Decibel. ne_in_pow is the power measured at the near-end input. ec_er_pow is the error power from the echo-canceller that is sent to the far-end. With the echo-canceller off, these values should track each other closely. When the

echo-canceller is on (DI1 set to OFF), however, a speech signal introduced at the far-end input should be heard at the near-end output speaker, but not at the far-end output. This manifests itself graphically by the black and red lines diverging. The difference between the two should be a reasonable approximation of echo-return loss enhancement (ERLE).

Note that since ne_in_pow and ec_er_pow are calculated by

$$\sum_{N} \frac{abs(x)}{N}$$

rather than a true power calculation

$$\sqrt{\sum_{N} \frac{x^2}{N}},$$

the ERLE observed on the screen is not exact. Later versions of the code may address this problem. Convergence time can be observed by increasing the number of samples taken between screen updates and beginning far-end speech immediately after a screen update. With a bit of calculation, and a reasonable sample rate, convergence time can be calculated by observing ne_in_pow and ec_er_pow.

OTHER INTERESTING INFORMATION

Code Naming Convention

Code versions will be named as follows: AAecBCDE.hex

The lower case represents constants. AA will be either "RM" or "CW" to differentiate PC booted versions from ROM versions of the same code. B will be either "A" to indicate the existence of an acoustic echo canceller, or "X" to indicate no acoustic echo canceller. C will be either "N" to indicate the existence of a network echo canceller, or "X" to indicate no network echo canceller. D will be the version character, starting from "A". E will be "1" for a Boot1 program or "2" for a Boot2 program.

So, CWECAXA1.hex is the microcontroller loaded version of the revision A Boot1 program ("A1") of the acoustic canceller only ("AX") application.

Note that the PC booted versions also have a ".drm" file associated with them. This file contains all the variable names of the data ram variables that the user has access to in the **Control/Get/Set...** and **Control/Signals...** dialogs. These dialogs cannot be used if this file does not exist.

Communication Protocol

The CDB6401 communicates with the PC through a serial port communications protocol that requires a command byte.

If the command byte is 0x00 (hexidecimal), then the command byte is echoed back through the RS232 link and the value of 0x00 is presented to the BI pins of the CS6401.

If the command byte is 0x80, then the boot subroutine on the microcontroller is called. The boot subroutine sets $\overline{BIE}$ inactive to indicate that the CS6401 is the boot slave, forces the CS6401 and CS4216 into RESET, and releases that RESET when the first boot byte is received from the serial port. This allows time for the voltage reference of the CS4216 to settle for accurate calibration. The boot protocol involves the PC sending a byte and waiting until the byte is echoed before sending another. The byte received at the microcontroller is presented to the BI pins and $\overline{BIE}$ is toggled to latch the data into the CS6401 on the falling edge. This process is repeated for all 1532 bytes. Once all 1532 bytes are loaded, the CS6401 begins executing. Note that the data file is 2048 bytes. The last 516 bytes are not transmitted.

Any other number as a command byte indicates a data RAM read or write from the CS6401. The microcontroller will then expect two data

bytes from the PC. A write is signified if the most significant bit is high (0x80 or higher). The address of data RAM to be read or written is contained in the lower seven bits. On a read, the two data bytes from the PC are zeroes. When all three bytes are received by the microcontroller, the microcontroller presents the data to the BI pins of the CS6401. When the CS6401 reads the command byte at the BI pins, it outputs to the lower eight BO pins the high byte of the requested data (on a read) or zero on a write and toggles the microcontroller's interrupt pin. This tells the microcontroller to output the first data byte, which when read causes another interrupt with the low byte of the requested data (or zero). This interrupt causes the microcontroller to output the last data byte, which causes the last interrupt in the communication cycle, with 0x00 on the lower eight BO pins. At this third interrupt, the microcontroller should present 0x00 to the BI pins and send the bytes received from the CS6401 to the PC in the order in which they were received. The interrupts should occur once per sample time, or approximately 125µs apart. The interrupts synchronize the microcontroller with the CS6401 since the devices operate at such different speeds.

Microcontroller Source Code

This microcontroller source code was written for the Motorola 68HC705C8 8-bit microcontroller. It assumes the existence of a Serial Communications Interface port (or other UART) and at least one 8-bit parallel output port, one 8-bit parallel input port, and two more output pins, as well as external interrupts. This code is provided so that a system designer can use another microcontroller to implement the same functions.

```
*** CDB6401 Rev 1.0
*******Internal equates*******
PORTA       equ     $00
PORTB       equ     $01
PORTC       equ     $02
PORTD       equ     $03
PADDR       equ     $04
PBDDR       equ     $05
PCDDR       equ     $06
PDDDR       equ     $07
SPICR       equ     $0A
SPISR       equ     $0B
SPIDR       equ     $0C
SCIBR       equ     $0D
SCIR1       equ     $0E
SCIR2       equ     $0F
SCISR       equ     $10
SCIDR       equ     $11
TCR         equ     $12
TSR         equ     $13
ICHIR       equ     $14
ICLOR       equ     $15
OCHIR       equ     $16
OCLOR       equ     $17
CHIR        equ     $18
CLOR        equ     $19
ACHIR       equ     $1A
ACLOR       equ     $1B
PROGR       equ     $1C
COPRR       equ     $1D
COPCR       equ     $1E
BOOTCODE    equ     %10000000
ECHOCODE    equ     %00000000

******* Internal variables *******
            org     $50
COMDATA     rmb     1
I           rmb     1
COUNT       rmb     1
FLAG        rmb     1
RXDATA      rmb     3
TXDATA      rmb     3
            org     $180
MAIN        rsp
            lda     #%11000000
            sta     $1fdf
            sei
            lda     #$A0
            sta     PORTA
            lda     #$FF
            sta     PADDR
            lda     #$00
            sta     PORTB
            lda     #$00
            sta     PBDDR
            lda     #$00
            sta     PORTC
            lda     #$FF
            sta     PCDDR
            clr     FLAG
            lda     #$30
            sta     SCIBR
```

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```
        lda     #$00
        sta     SCIR1
        lda     #$0C
        sta     SCIR2
DO1     equ     *
        brset   5,SCISR,IF1
        jmp     EE1
IF1     equ     *
        jsr     INCOM
        sta     COMDATA
S10     equ     *
        lda     COMDATA
        cmp     #BOOTCODE
        beq     S10A
        jmp     S11
S10A    equ     *
        jsr     BOOT
        jmp     ES1
S11     equ     *
        cmp     #ECHOCODE
        beq     S11A
        jmp     S12
S11A    equ     *
        lda     COMDATA
        jsr     OUTCOM
        lda     COMDATA
        sta     PORTC
        jmp     ES1
S12     equ     *
        jsr     COMMEC
S13     equ     *
ES1     equ     *
EE1     equ     *
        jmp     DO1
LP1     equ     *

SUB1    equ     *
BOOT    equ     *
        lda     #0
        sta     PORTC
        bset    5,PORTA
        bset    7,PORTA
        bclr    7,PORTA
BOOTLOOP equ    *
        brset   5,SCISR,IF2
        jmp     EE2
IF2     equ     *
        jmp     EDIF2
EE2     equ     *
        jmp     BOOTLOOP
EDIF2   equ     *
        bset    7,PORTA
        lda     #0
        sta     I
FOR1    cmp     #94
        bls     FOR1A
        jmp     NEXT1
FOR1A   equ     *
        lda     #0
        sta     COUNT
FOR2    cmp     #15
        bls     FOR2A
        jmp     NEXT2
FOR2A   equ     *
        jsr     INCOM
        sta     COMDATA
        lda     COMDATA
        sta     PORTC
        bclr    5,PORTA
        lda     COMDATA
        jsr     OUTCOM
WAITLOOP equ    *
        brset   7,SCISR,IF3
        jmp     EE3
IF3     equ     *
        jmp     EDIF3
EE3     equ     *
        jmp     WAITLOOP
EDIF3   equ     *
        bset    5,PORTA
        inc     COUNT
        lda     COUNT
        jmp     FOR2
NEXT2   equ     *
        inc     I
        lda     I
        jmp     FOR1
NEXT1   equ     *
        lda     #0
        sta     COUNT
FOR3    cmp     #11
        bls     FOR3A
        jmp     NEXT3
FOR3A   equ     *
        jsr     INCOM
        sta     COMDATA
        lda     COMDATA
        sta     PORTC
        bclr    5,PORTA
        lda     COMDATA
        jsr     OUTCOM
WAITLP  equ     *
        brset   7,SCISR,IF4
        jmp     EE4
IF4     equ     *
        jmp     EDIF4
EE4     equ     *
        jmp     WAITLP
EDIF4   equ     *
        bset    5,PORTA
```

```
        inc     COUNT
        lda     COUNT
        jmp     FOR3
NEXT3   equ     *
        lda     #0
        sta     PORTC
        bclr    5,PORTA
        lda     #1
        sta     FLAG
        rts

SUB2    equ     *
COMMEC  equ     *
        jsr     INCOM
        ldx     #0
        sta     RXDATA,x
        jsr     INCOM
        ldx     #1
        sta     RXDATA,x
        ldx     #2
        clr     RXDATA,x
        clr     COUNT
        cli
        lda     COMDATA
        sta     PORTC
DO2     equ     *
        lda     COUNT
        cmp     #3
        bhs     LP2
        jmp     DO2
LP2     equ     *
        sei
        ldx     #0
        lda     TXDATA,x
        jsr     OUTCOM
        ldx     #1
        lda     TXDATA,x
        jsr     OUTCOM
        ldx     #2
        lda     TXDATA,x
        jsr     OUTCOM
        rts

INTIRQ  equ     *
        tst     FLAG
        beq     IF5
        bra     EE5
IF5     equ     *
        ldx     COUNT
        lda     RXDATA,x
        sta     PORTC
        lda     PORTB
        ldx     COUNT
        sta     TXDATA,x
        inc     COUNT
        jmp     EDIF5
EE5     equ     *
        clr     FLAG
EDIF5   equ     *
        rti

SUB3    equ     *
 ****** INCOM (SCI input) Subroutine *
INCOM   brclr   5,SCISR,INCOM
        lda     SCIDR
        rts

SUB4    equ     *
****** OUTCOM (SCI output) Subroutine *
OUTCOM  brclr   7,SCISR,OUTCOM
        sta     SCIDR
        rts

****** Reset and Interrupt Vectors *
*
        org     $1ffe
        fdb     MAIN
        org     $1ffa
        fdb     INTIRQ *
****** End of Reset and Interrupt Vectors *
```

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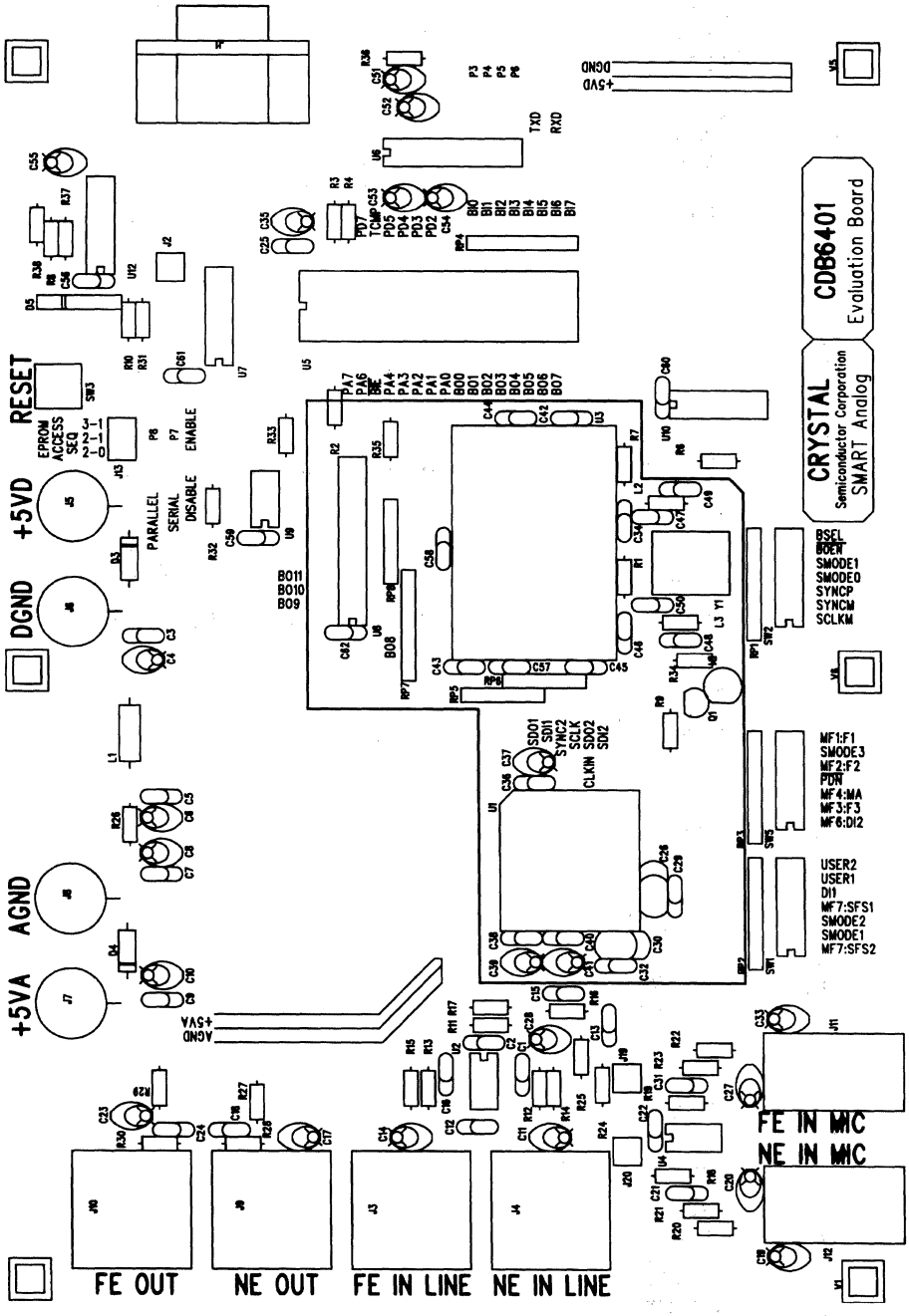


Figure 20. CDB6401 Silkscreen.

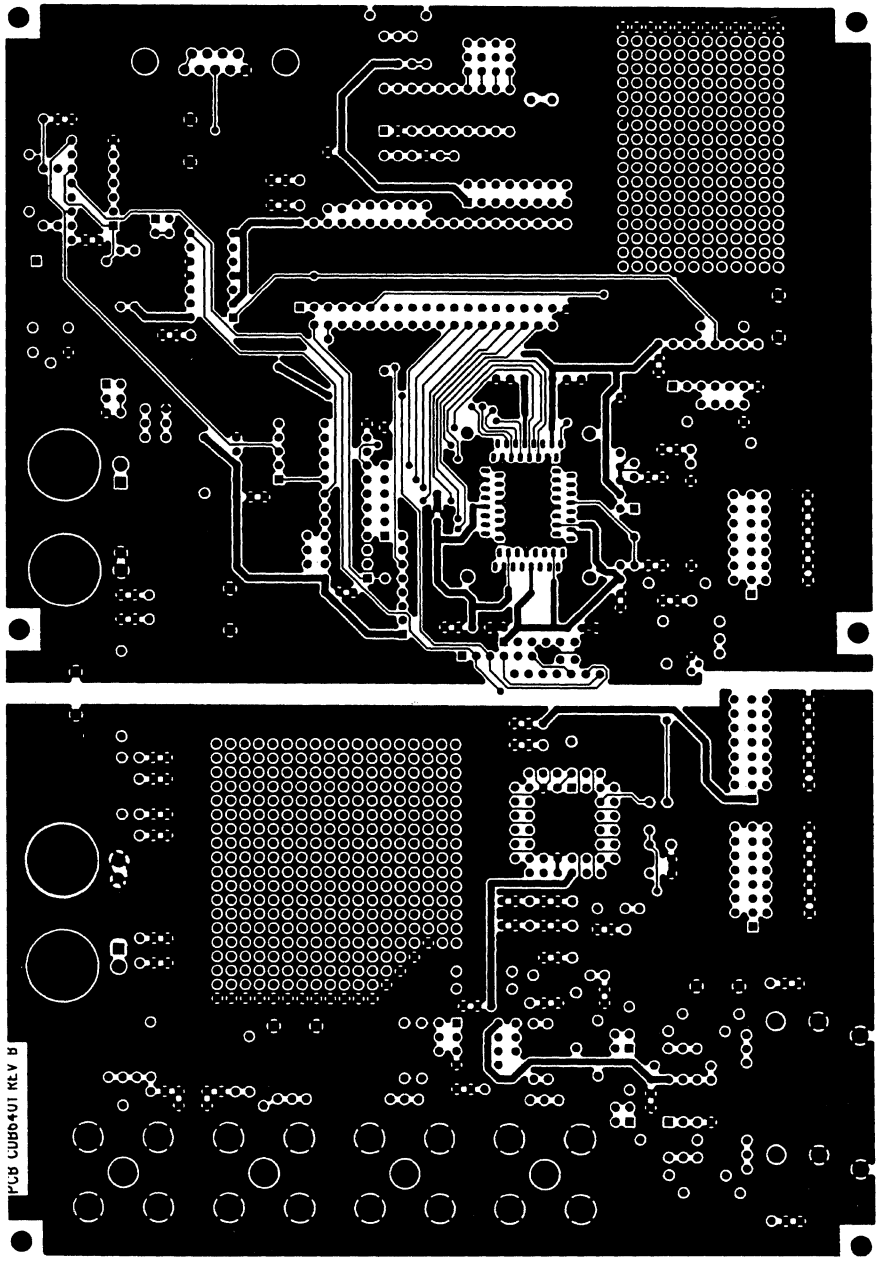


Figure 21. CDB6401 Component-side Layer.

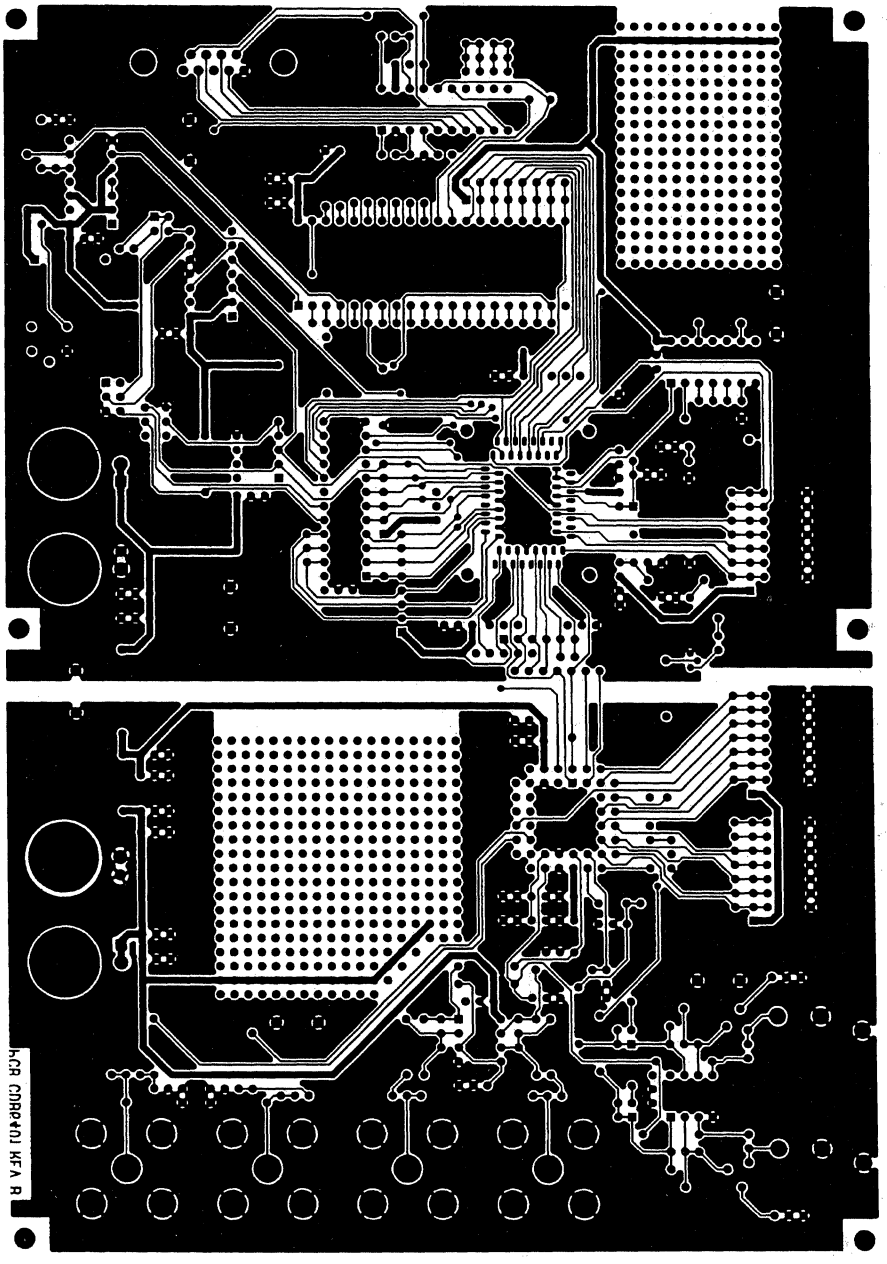


Figure 22. CDB6401 Solder-side Layer.

Semiconductor Corporation

CWECAXB

CS6401 Echo-Canceller Code

FEATURES

- 30dB of ERLE
- Input high pass filters (HPF) (-3dB@300Hz) for noise reduction and offset removal
- Pre-emphasis (PE) filter for convergence speed and ERLE improvement
- Half-duplex mode on startup and for fall-back in adverse conditions
- Customizability

OVERVIEW

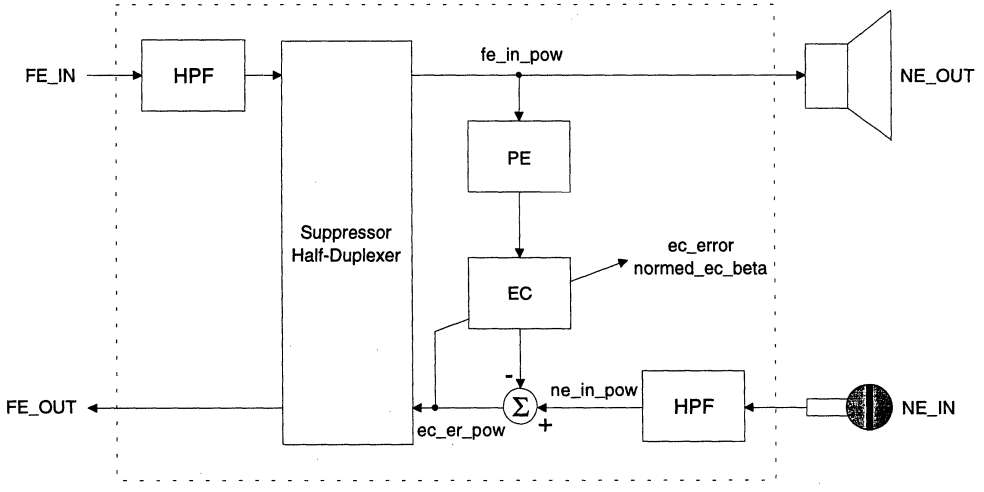
The CWECAXB version of application code for the CS6401 Programmable Echo-Canceller is optimized for acoustic echo-cancellation applications in noisy environments.

Version CWECAXB of the echo-canceller code contains advanced features:

- Support of hands-free audio at both ends of a communication link
- Support of a half-duplex fall-back mode
- Greater immunity to near-end noise

Version CWECAXB also provides the user some measure of customizability with modifiable threshold constants.

ORDERING INFORMATION
CW6401EAA3



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Crystal Semiconductor Corporation
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OVERVIEW

The CWECAXB application code for the CS6401 is optimized for echo-cancellation in noisy environments. At power up, the CWECAXB application will enter half-duplex mode, allowing only the near-end user or the far-end user to speak at a time. If the noise level in the near-end environment is low enough, the echo-canceller will train (i.e., estimate the near-end path response) while the far-end speaker is talking. Once the echo-canceller has created an adequate near-end path estimate, the CWECAXB application will automatically switch to full-duplex operation.

CONTROLS

Once booted into the CS6401, CWECAXB allows the user to control and monitor the performance of the software in many ways. The DIP switches on the CDB6401 allow control of some of the algorithms, as does the **Control/Control Word...** dialog box in the Windows Application. The **Control/Signals...** dialog box provides a way to monitor the performance of the algorithm. The **Control/Get/Set...** dialog box allows the user to customize various constants.

DIP Switches

DIP switch DI1 will clear the echo-canceller coefficients when ON (GND). This effectively turns off the echo-canceller. Note that the half-duplex mode will come on at this point unless half-duplex mode is disabled (see **Control/Control Word...** below). DIP switch MF6:DI2 will enable the Supplementary Echo-Suppression (SES) when ON (GND). SES helps remove residual echo that the canceller lets through. The recommended settings of the DIP switches is DI1 OFF and MF6:DI2 ON.

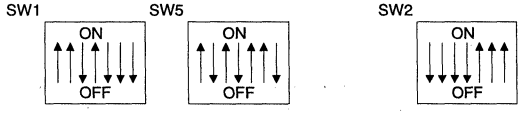

Figure 1. Recommended DIP Switch Settings.

Control/Signals...

Choosing **Signals...** under the **Control** menu of the CDB6401 Windows Application will bring up a dialog box that allows the user to choose what variables to monitor. Select a color (Black, Red, Blue, or Green) and choose a variable and the appropriate view option (unsigned/signed, linear/dB) in order to display it on the screen. The variables will be displayed as if on a strip chart with the newest values appearing on the left side of the screen. See the section on *Relevant Variables* at the end of this document for specific variables and view options.

Control/Get/Set...

The **Control/Get/Set...** dialog box is invoked by choosing **Get/Set...** under the **Control** menu of the CDB6401 Windows application. This dialog box allows the user to view and/or change any of the variables and constants in the Data RAM of the CS6401. As most variables get changed during every cycle, a list of *Threshold Constants* that can influence algorithm performance is included at the end of this document. To change a constant, merely select it into the List Box, enter the hexadecimal value to change it to in the Edit Box, select the Set button, and click on the Get/Set button. To view a constant, select it into the List Box, select the Get button, and click on the Get/Set button. The retrieved value will appear in the Edit Box. Note that changes are valid only for the current session. A reboot will reset the defaults.

Control/Control Word...

The **Control Word...** dialog box, which is invoked from the **Control** menu in the CDB6401 Windows Application, is included to extend algorithm control beyond the two DIP switches that are on the evaluation board. Currently, the only enabled option is the ability to disable the half-duplex mode of CWECAXB.

CUSTOMIZING SUPPRESSION

The SES works by attenuating the output by an amount specified by *ne_in_code* and *fe_in_code*. These variables are indices into a table beginning with the constant *V1*. Currently, the table is 4 dB per step, but the user can change this by changing the table values.

NETWORK APPLICATIONS

Although CWECAXB is intended primarily for acoustic echo-cancellation, it should also be able to cancel electrical network echo.

SCALING

It is extremely important to make sure that the signals entering the echo-canceller are scaled properly in order to get maximum performance from the part. See the section *Setting the Gains* in the CDB6401 data sheet for the procedure to ensure proper scaling of signal levels. The echo-canceller will not work properly unless the signals are scaled properly.

CHANGES FROM VERSION CWECAXA:

Half-Duplex Mode

From boot-up, half-duplex mode will be on until *decision_delay_timer* becomes equal to *fd_en_cnt*. This ensures that the echo-canceller does not enter full-duplex until it has converged sufficiently to reduce loop gain to prevent acoustic howling. This has the added benefit of ensuring that the residual echo is very low, as well. The LED on the evaluation board will be lit when full-duplex mode is achieved.

The canceller will revert to half-duplex mode if a major path change occurs which reduces the *saved_erl* to below *saved_erl_thld* or when the echo-canceller performance is very poor.

Half-duplex mode may be disabled by setting the *Disable half-duplex mode* button in the **Control/Control Word...** dialog box. This will allow evaluation of convergence time.

Near-End Noise Tolerance

If the noise level is too high for the echo-canceller to create a reasonable path estimate when the echo-canceller is first booted, then it will remain in half-duplex mode until the noise has dropped (until *best_noise* is less than *ec_noise_thld*). If the noise drops enough to allow the echo-canceller to accurately estimate the path response, then the half-duplex mode is turned off. If the noise subsequently becomes high after the canceller has converged, then the updates of the coefficients are disabled, but the echo-canceller is still active, so full-duplex mode should be retained.

Minor path changes, such as people moving about in an acoustic echo-cancellation environment, should not unduly affect the performance of the canceller. Moving the microphone or speaker would be a major path change that would require several seconds of far-end speech in order to recover.

Note that the recovery time after a path change can be significantly longer than the initial convergence time.

Variable Suppression

Suppression is disabled when the noise is "high" (determined by comparing *sup_noise_thld* to *ne_noise_level*) to prevent noise modulation caused by suppression from becoming objectionable. A high noise level at the near-end can mask echo, so suppression is not needed under such conditions.

0 dB Attenuation

This version will have 0 dB of signal attenuation from FE_IN to NE_OUT and NE_IN to FE_OUT during single-talk conditions.

Doubletalk Detector

The doubletalk detector in this version is greatly revised.

RELEVANT VARIABLES

(Use **Control/Signals...** to add these to the strip chart.)

Variable	View Option	Description
ne_in_pow	unsigned dB	near-end input power
fe_in_pow	unsigned dB	far-end input power
ec_er_pow	unsigned dB	echo-canceller error power residual echo power (includes near end input power)
normed_ec_beta	unsigned dB	update gain: will be -96dB (0) when coefficients are frozen
saved_erl	unsigned linear x1000	saved echo return loss enhancement: estimated peak performance
decision_delay_timer	unsigned linear x1000	number of utterances after *saved_erl* is greater than *saved_erl_thld* before full-duplex is allowed
fe_speech_detected	unsigned linear	non-zero when far-end speech detected
ne_speech_detected	unsigned linear	non-zero when near-end speech detected
channel_status	signed linear	half-duplex channel: 32767 when far-end speaker has the channel, -32768 when near-end speaker has the channel
channel_indicator	signed linear	three-state channel: *channel_status* above, but 0 for idle channel

THRESHOLD CONSTANTS

(Use **Control/Get/Set...** to view or change these constants.)

Constant	Description
saved_erl_thld	half-duplex is enabled so long as *saved_erl* is less than this number
max_vox	this constant determines how quickly the noise-power estimator can react to changes in the background noise power. Time in negative samples
up_noise_thld	if *ne_noise_level* is above this threshold, suppression is disabled
ec_noise_thld	noise threshold for half-duplex (relative to *best_noise*)
fd_en_cnt	number of utterances after good *saved_erl* obtained before full-duplex mode is enabled. Should always be at least one. Duplex adjusts discrimination of speech-detector for half-duplex. Increase duplex for less sensitivity to impulsive noise.

• Notes •

Semiconductor Corporation

CS6450

TDMA/AMPS I&Q Baseband Codec

Features

- Transmit I&Q Interface
  Two D/A converters: 10-bit, 194.4 kHz sample rate
- Receive I&Q Interface
  Two range-scaling A/D converters: 18-bit resolution, 97.2 kHz sample rate, 10-bit outputs
- Single +5V power supply; optional 3V digital I-O pins
- Three 8-bit auxiliary D/A converters for control
- Receive I & Q offset error correction

General Description

The CS6450 is a monolithic 15 kHz bandwidth I&Q baseband codec designed for use in AMPS and TDMA applications. The baseband codec provides the interfaces between a digital baseband subsystem and an analog radio subsystem. On the digital side, the codec interfaces to a digital sub-system through a parallel port. The codec includes 10-bit Delta-Sigma DAC's and ADC's for the I and Q signals. Three low speed 8-bit D/A converters can be used to control, for example, for frequency and gain of the radio sub-system. The baseband codec has efficient power management features, including the ability to power down individual transmit, receive and control channels.

ORDERING INFORMATION
CS6450-IQ 44-pin TQFP

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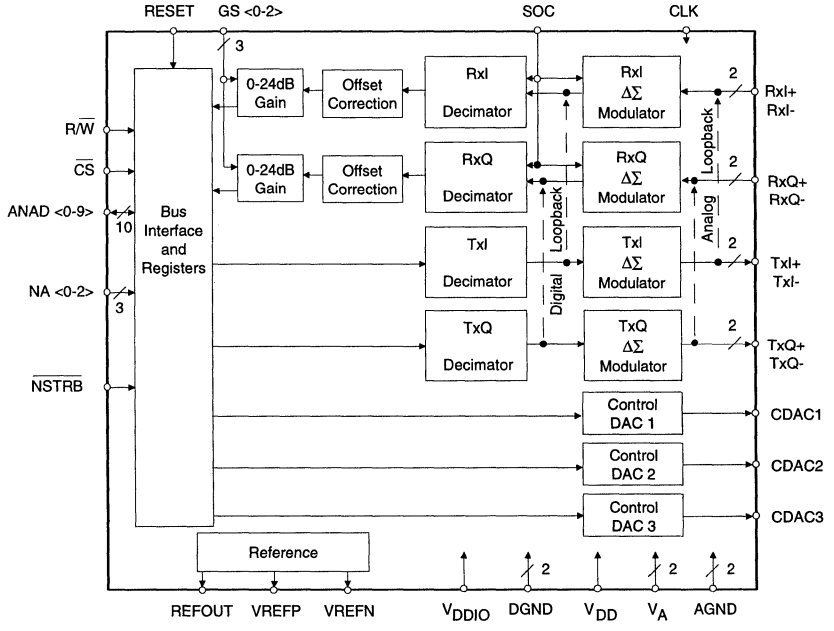

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 Fax: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V)

Parameter	Symbol	Min	Max	Units
DC Supply Voltage	V_{DD},V_A	-	6.0	V
Digital I-O Supply Voltage	V_{DDIO}	- 0.3	V_{DD}+0.3	V
Input Voltage, Analog Pins	V_I	- 0.3	V_A + 0.3	V
Input Voltage, Digital IO Pins	V_I	- 0.3	V_{DDIO}+0.3	V
Input Current (except supplies)		-	±10.0	mA
Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature	T_{stg}	-55	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V, V_{INH} = V_{DD}, V_{INL}= 0V)

Parameter	Symbol	Min	Typ	Max	Units
Digital Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature	T_A	-40	-	85	°C
Digital I-O Supply Voltage	V_{DDIO}	3.0	-	VDD	V
Analog Supply Voltage	V_A	-	V_{DD}	-	V
Power Dissipation					
All sections powered up, V_{DD}=5V, T_A=25°C		-	105	144	mW
All sections powered up, V_{DD}=5.5V, T_A=85°C		-	-	177	mV
All sections powered down, and CLK active		-	-	10	mW
All sections powered down, and CLK inactive		-	0.1	0.4	mW
TxQ and TxI DAC Code Update Rate		180	-	194.4	kHz
RxQ and RxI ADC Code Update Rate		90	-	97.2	kHz
RxQ and RxI Signal Bandwidth		-	-	15	kHz
CDAC<1:3> Input Signal Bandwidth		0	-	3.0	kHz
CDAC<1:3> Code Update Rate		-	-	24.3	kHz
CDAC<1:3>, TxI± and TxQ± load impedance (Note 1)		10	-	-	kΩ
REFOUT load impedance (Note 2)		5	-	-	kΩ
RxI± and RxQ± Common Mode Voltage		1.15	-	V_A-1.3	V

Notes: 1. Resistive in parallel with ≤20 pF capacitor.
2. Resistive in parallel with ≤50 pF capacitor.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS (V_{DDIO} = 5V ±10% or 3.3V ±10%, DGND = 0V, Notes 1, 3 and 4)

Parameter		Symbol	Min	Typ	Max	Units
High-level Output Voltage	(Iout = 600 µA)	V_{OH}	V_{DDIO}-0.5	-	-	V
Low-level Output Voltage	(Iout = -800 µA)	V_{OL}	-	-	0.4	V
High-level Input Voltage		V_{IH}	V_{DDIO}-1.0	-	V_{DDIO}+0.3	V
Low-level Input Voltage		V_{IL}	-0.3	-	0.8	V
Input Leakage Current	(V_{IL} = DGND)	I_{IL}	-10	0.01	+10	µA
High-impedance Output Leakage Current		I_{OZ}	-10	-	10	µA
Input Pin Capacitance		C_i	-	10	-	pF
Output Pin Capacitance		C_o	-	12	-	pF

Notes: 3. Performance over recommended operating temperature is guaranteed by design and characterization.
4. Digital pins are $\overline{\text{RESET}}$, GS<0:2>, SOC, CLK, R/$\overline{W}$, $\overline{CS}$, ANAD<0:9>, NA<0:2> and $\overline{\text{NSTRB}}$.

REFERENCE ANALOG SPECIFICATION (V_A = 5V ±10%, AGND = 0V, Note 3, load impedance of 5 kΩ resistive with ≤ 50 pF capacitive)

Parameter	Min	Typ	Max	Units
REFOUT Voltage	2.1	2.2	2.3	V
Differential Reference Voltage (VREFP-VREFN)	2.4	2.5	2.6	V

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I AND Q TRANSMITTER ANALOG SPECIFICATIONS

(V_A = 5V ±10%, AGND = 0V, DAC code update rate of 180 kHz, 1 kHz digital sinewave with peak amplitude equal to 90% of full scale, load impedance of 10 kΩ resistive with ≤ 20 pF capacitive, 14.58 MHz CLK, Notes 3 and 5, V_{IH} = V_{DD}, V_{IL} = 0V)

Parameter		Min	Typ	Max	Units
Delay Mismatch between I and Q channels	(Note 6)	-	-	50	nsec
Amplitude Mismatch between I and Q channels	(Note 7)	-	-	0.5	%
Differential Output Range	(VoutMAX - VoutMIN)	2.09	2.2	2.31	Vp-p
Differential Output Voltage (TX+ - TX-)					
with (00 0000 0000) input	VoutMIN	-	-1.1	-	V
with (10 0000 0000) input	VoutBIAS (Note 8)	-50	0	50	mV
with (11 1111 1111) input	VoutMAX	-	1.1	-	V
Common Mode Output Voltage		2.0	2.2	2.4	V
Signal to (Noise + Distortion) ratio		48	-	-	dB
Integral Non Linearity	(Note 6)	-	-	±0.5	LSB_{10}
Differential Linearity Error	(Note 6)	-	-	±1	LSB_{10}
THD					
	(with 1 kHz digital sinewave)	-	-70	-	dB
	(Note 9)	-	-	-85	dB
Pass band	(Note 6)	0	-	15	kHz
Pass band Gain Droop		-	-	0.7	dB
Pass band Differential Group Delay	(Note 6)	-	-	3	µs
Beginning Stop band Frequency (Analog Mode)	(Note 6)	-	-	165	kHz
Beginning Stop band Frequency (Digital Mode)	(Note 6)	-	-	180	kHz
Stop band Attenuation	(Note 6)	60	-	-	dB
Group Delay	(Note 6)	20.8	21.3	21.8	µs

Notes:
5. Operation at 194.4 kHz sample rate guaranteed by design and characterization.
6. Guaranteed by design and characterization.
7. With same code on each channel.
8. The Min and Max values specify the maximum DC offset.
9. This test is performed with a special input wave form. The wave form is created by digitizing a 1 kHz sinewave, and then filtering the harmonics. This signal is exclusive of input quantization noise.

I AND Q RECEIVER ANALOG SPECIFICATIONS (V_A = 5V ±10%, AGND = 0V, Start-Of-Conversion rate of 97.2 kHz, 1 kHz sinewave with 350 mVp-p amplitude, 2.2V DC bias, with external 81 kHz single-pole anti-aliasing filter, receiver common mode voltage of V_A-1.3V, Gain Block set to 0 dB, 14.58 MHz CLK, Notes 3 and 10, V_{IH} = V_{DD}, V_{IL}= 0V)

Parameter		Min	Typ	Max	Units
Delay Mismatch between I and Q channels	(Note 6)	-	-	50	nsec
Amplitude Mismatch between I and Q channels		-	-	0.5	%
Differential Full Scale Input Level (RX+ - RX-)		0.475	0.5	0.525	Vp-p
Differential Input Impedance (resistive)		20	-	-	kΩ
Gain-block Step Size		-	6	-	dB
Gain-block Range		0	-	24	dB
Offset Error					
	Before calibration	-	-	±20	LSB_{10}
	After calibration	-	-	±1	LSB_{10}
Signal to Noise Ratio (inband, with a gain of 24 dB, 35 mVp-p input signal)		56	-	-	dB
Signal to Noise Ratio (inband, with a gain of <24 dB)		58	-	-	dB
Differential Linearity Error	(Note 6)	-	-	±0.5	LSB_{10}
Aperture Jitter	(Note 6)	-	-	50	ns
Integral Non Linearity	(Note 6)	-	-	0.5	LSB_{10}
THD (at 1 kHz)	(Note 6)	-	-	-85	dB
Pass Band (Analog Mode)		0	-	45	kHz
Pass Band (Digital Mode)		0	-	48.6	kHz
Pass Band Gain Droop		-	-	0.4	dB
Pass Band Differential Group Delay	(Note 6)	-	-	3	µs
Stop Band Attenuation (Notes 6 and 11)	at 81 kHz	35	40	-	dB
	at 180 kHz	-	69	-	dB
	at 500 kHz	-	85	-	dB
Group Delay	(Note 6)	52.5	53	53.5	µs

Notes: 10. Operation with SOC rate of 90 kHz guaranteed by design and characterization.
11. Stop Band defined as 75 kHz to 4.785 MHz for analog mode, and 81 kHz to 4.785 MHz for digital mode.

6

CONTROL DACs ANALOG SPECIFICATIONS (V_A = 5V ±10%, AGND = 0V,

Note 3, 1 kHz digital sinewave sampled at 24.3 kHz, external 10 kHz single-pole anti-imaging filter, load impedance of 10 kΩ, CLK = 14.58 MHz, $V_{IH} = V_{DD}$, V_{IL} = 0V)

Parameter		Min	Typ	Max	Units
Output Range	(VoutMAX - VoutMIN)	3.135	3.30	3.465	Vp-p
Output Voltage					
for 11 1111 11xx input	VoutMAX	-	3.85	-	V
for 10 0000 00xx input	VoutBIAS (Note 8)	2.15	2.20	2.25	V
for 00 0000 00xx input	VoutMIN	-	0.55	-	V
Signal to Noise Ratio	(Note 6)	48	-	-	dB
THD	(Note 6)	-	-44	-	dB
Integral Non Linearity (Linearity Error)		-	-	±1	LSB_8
Crosstalk isolation (between control DACs)		+49	-	-	dB
Differential Linearity Error	(Notes 6)	-	-	±1	LSB_8
Static AC Noise Power	(Notes 6)	-	-	-70	dB

SWITCHING CHARACTERISTICS (V_{DD} = 5V ±10%, DGND=0V, Note 3, V_{IL} = 0V, V_{IH} = V_{DD})

Parameter	Symbol	Min	Typ	Max	Units
$\overline{NSTRB}$, $\overline{CS}$, R/$\overline{W}$, NA<2:0> Setup Time	t_1	10	-	-	ns
$\overline{NSTRB}$, $\overline{CS}$, R/$\overline{W}$, NA<2:0> Hold Time	t_2	1.4	-	-	ns
$\overline{RESET}$ Setup Time	t_6	10	-	-	ns
$\overline{RESET}$ Hold Time	t_7	10	-	-	ns
ANAD<9:0> Output Delay after CLK rising	t_{15}	-	-	35	ns
ANAD<9:0> Output Valid before $\overline{NSTRB}$ rising	t_{16}	80	-	192	ns
ANAD<9:0> Output Valid after $\overline{NSTRB}$ rising	t_{17}	1	-	31	ns
ANAD<9:0> Input Setup Time	t_{11}	25	-	-	ns
ANAD<9:0> Input Hold Time	t_{12}	25	-	-	ns
$\overline{CS}$, R/$\overline{W}$, $\overline{NSTRB}$ to ANAD<9:0> Input Hold Time	t_{14}	0	-	-	ns
$\overline{RESET}$ Pulse Width	t_{20}	73.2	-	-	ns
CLK Frequency	f_{CLK}	14.58 - 15 ppm	14.58	14.58 + 15 ppm	MHz
CLK Period	t_9	-	68.6	-	ns
CLK Duty Cycle	t_8/t_9	30	-	70	%
SOC Pulse Width	t_{10}	t_9 * 3	-	-	ns
$\overline{NSTRB}$ Pulse Width Read Cycle	t_{23}	t_9 * 2 +t_1+t_2	-	-	ns
$\overline{NSTRB}$ Pulse Width Write Cycle	t_{22}	t_9 * 3 +t_1+t_2	-	-	ns

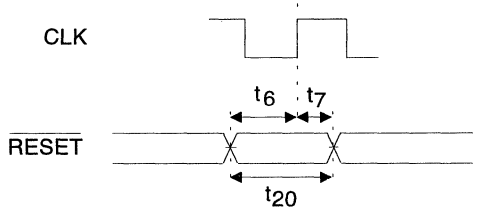


Figure 1a. Reset Cycle

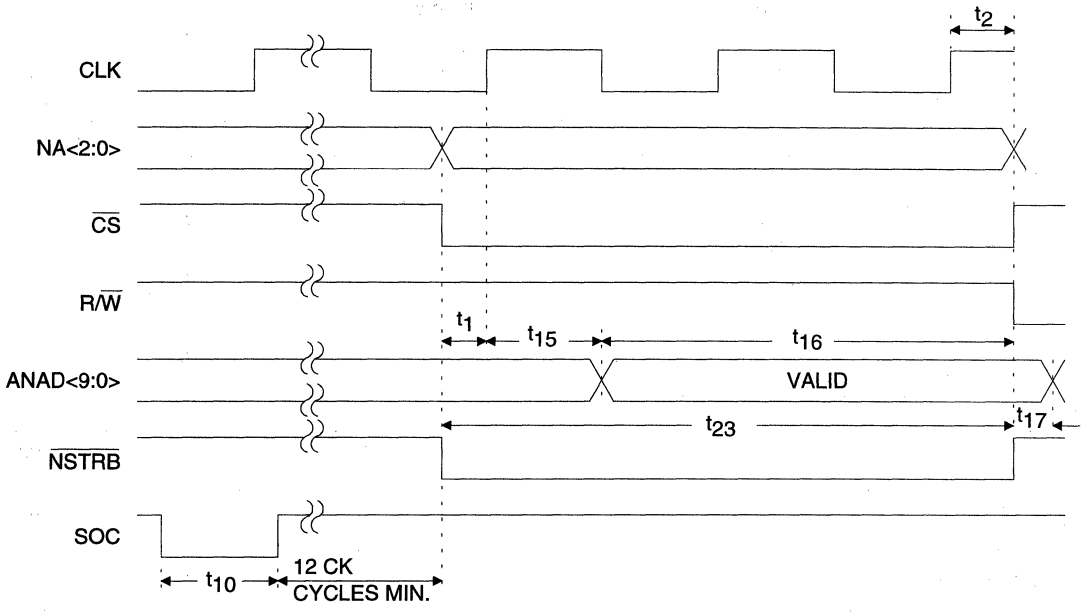


Figure 1b. Receive Switching Characteristics (CS6450 writes onto parallel bus)

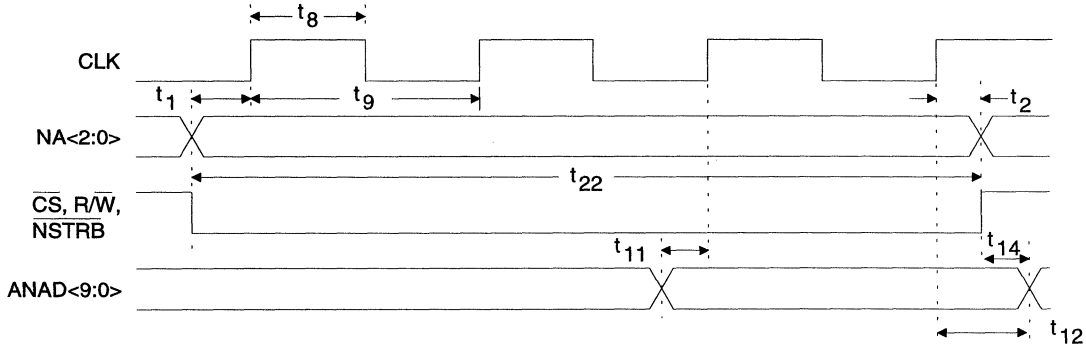


Figure 1c. Transmit Switching Characteristics (CS6450 reads from parallel bus)

GENERAL DESCRIPTION

The CS6450 is a monolithic, dual channel (I&Q) baseband codec designed for use in AMPS and TDMA applications The baseband codec provides the interfaces between a digital baseband subsystem and an analog radio subsystem. On the digital side, the codec interfaces to a DSP through a 10-bit data bus, a three-bit address bus and eight control signals.

On the analog side, the codec interfaces to the radio subsystem, and provides the signal conversion functions and associated filtering. This includes two 10-bit, 15 kHz bandwidth DACs for the differential I and Q transmit signals, and two 18-bit, 45 kHz bandwidth, ADCs for the differential I and Q receive signals. The ADCs include support for system calibration of ADC offset.

The rate at which samples are transferred between the digital sub-system and the CS6450 are approximately 100 kHz for ADC inputs, and approximately 200 kHz for the DAC outputs. Receive ADC conversions start at a time determined by the SOC input pin.

The receiver has selectable gain control, with gain options of 0, 6, 12, 18, and 24 dB. An analog reference signal, REFOUT, is output to the RF subsystem, allowing the radio to DC couple the transmit and receive I and Q signals.

Three low speed 8-bit D/A converters are provided for control signals, and can be used, for setting AGC and AFC levels in the RF circuits.

The baseband codec has efficient power management features, including the ability to power down individual transmit, receive and control channels, and operates from a 5 volt power supply. Optionally, the digital IO pins can be operated with a 3V power supply.

A typical connection diagram is shown in Figure 2. In the RF subsystem, the TxQ and TxI signals are modulated and up-converted to the appropriate carrier frequency, amplified and output to the antenna. On the receive side, the RF subsystem amplifies, converts and demodulates the received RF signal, and inputs the signal as differential analog signals RxI and RxQ to the CS6450.

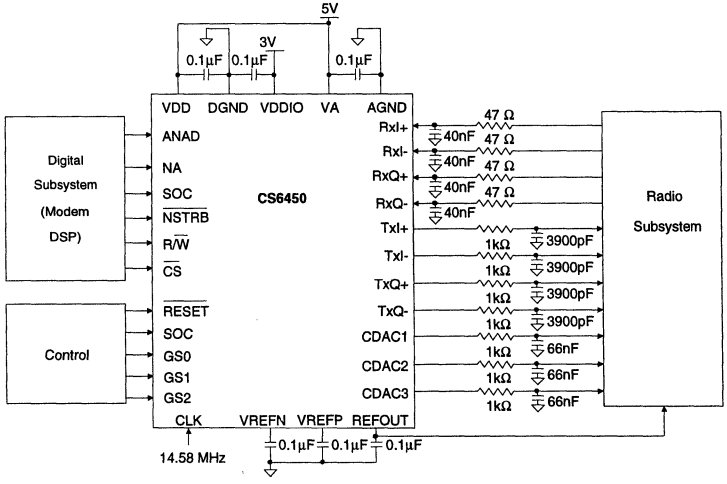


Figure 2. Typical Connection Diagram

The modem DSP encodes and modulates the transmit data creating digital I and Q signals, which are input to the CS6450 over the parallel data bus. The modem DSP inputs the received modulated, digital data samples over the same bus. In TDMA mode, these samples are then demodulated, de-interleaved and FEC decoded.

Digital I-O Overview

Digital I-O to the DSP subsystem is via a 13-bit parallel port, with ten data lines and three address lines. Data is written to 8 transmit registers. Data is read from 3 receive registers. Pin R/$\overline{W}$ selects between the read and write operations. The registers are defined in Table 1. In addition, five individual input lines control reset, start of receive conversion and receive gain.

The digital input/output pins can be operated with a logic high voltage of either 3V or 5V. The voltage level is set by the voltage supplied to the V_{DDIO} power supply pin. The digital input/output pins are: CLK, SOC, GS<2:0>, $\overline{RESET}$, R/$\overline{W}$, $\overline{CS}$, ANAD<9:0>, NA<2:0> and $\overline{NSTRB}$.

Operating Modes

The CS6450 has several operating mode options. These options are selected by writing to register 101. First, the CS6450 is commanded to either the analog AMPS mode or the digital TDMA mode. With the exception of the conversion and code update rates, there is no difference in operation between these two modes. In addition to the AMPS and the digital TDMA modes, the CS6450 is capable of powering down individual sections of the chip. These modes and configurations are controlled by writing the MODE command (address 5) onto the NA<2:0> address bus and writing a control word on ANAD<9:0>. The operational modes are shown is Tables 2, 3, and 4.

In power-down mode, individual sections of the CS6450 can be powered down for minimum power consumption. This includes the transmit channels (TxI, TxQ), receive channels (RxI, RxQ) and the control channels (CDAC1, CDAC2 and CDAC3).

When in a power-down configuration, those channels not powered down are capable of normal operation. To wake up the sections in power-down mode, associated control bits are set to a logic "1" (see Table 3). While in power-

ANAD Bus		Mode
B9	B8	
0	0	Analog: Loop backs and System Cal
0	1	Analog: Power-down Options
1	0	Digital: Power-down Options
1	1	Digital: Loop backs and System Cal

Table 2. Mode Selection

Address			Read from Bus Mode: (R/$\overline{W}$ = 0)	Write to Bus Mode: (R/$\overline{W}$ = 1)
NA2	NA1	NA0		
0	0	0	TxI Channel Data	RxI Channel Data
0	0	1	TxQ Channel Data	RxQ Channel Data
0	1	0	Control 1 DAC Data	Reserved
0	1	1	Control 2 DAC Data	Reserved
1	0	0	Control 3 DAC Data	Reserved
1	0	1	Mode Control	Mode Control
1	1	0	RxI± DC Offset	Reserved
1	1	1	RxQ± DC Offset	Reserved

Table 1. Register Definitions

Bit which is set to '0'	Block which is Powered Down
B0	RX I
B1	RX Q
B2	TX I
B3	TX Q
B4	CDAC1
B5	CDAC2
B6	CDAC3
B7	REF

Table 3. Power-down Options

ANAD Bus								Mode
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	0	0	0	1	I channel analog loop back
0	0	0	0	0	0	1	0	Q channel analog loop back
0	0	0	0	0	0	1	1	Unused
0	0	0	0	0	1	0	0	Unused
0	0	0	0	0	1	0	1	Unused
0	0	0	0	0	1	1	0	I and Q channel analog loop back
0	0	0	0	0	1	1	1	digital loop back
0	0	0	0	1	0	0	0	Reserved for factory test
0	0	0	0	1	0	0	1	Reserved for factory test
0	0	0	0	1	0	1	0	Reserved for factory test
0	0	0	0	1	0	1	1	Reserved for factory test
0	0	0	0	1	1	0	0	Reserved for factory test
0	0	0	0	1	1	0	1	short Rx analog differential inputs

Table 4. Loop back and System Calibration Options

down mode, the CS6450 retains the integrity of the information contained in its mode control registers. When normal operation is re-established, the data contained in the CS6450 registers reverts to the state prior to power down. Also, in the power-down mode, the transmit analog outputs are floating. If the voltage reference is powered down, all analog outputs are floating. The CDAC<1:3> analog outputs are held to the output voltage present just prior to being powered down. After RESET, all channels are in a power-down mode.

Transmit I and Q Data Channel

A pair of I and Q data signals are typically transferred from the digital subsystem to the CS6450 once per sample time (5.144 µsec for TDMA mode, 5.556 µsec for AMPS mode).

The transmitter has a band width of 15 kHz, and data can be input to the DAC as slow as 114 kHz (or CLK÷128). In any case, the sample rate and master clock rate, f_{CLK}, must be related by an integer multiple of 3. However, to insure TDMA/AMPS systems performance and minimal out-of-band power, samples should be input to the DAC at 194.4 kHz for TDMA and 180 kHz for AMPS. With the 194.4 kHz sample rate, the lowest frequency image of a pass band signal occurs at 194.4 kHz - 15 kHz = 179.4 kHz. The result is better control of out-of-band energy versus a 30 kHz sample rate.

DAC input samples can be transferred first I then Q, or Q then I. A control signal, $\overline{\text{NSTRB}}$, generated by the digital subsystem, is used to latch the data into the DAC. The data samples provided by the digital subsystem are 10 bits wide and interface to the CS6450 via the bi-directional data bus ANAD<9:0>. The format of the samples is unsigned binary number, where minimum output signal is described by h000, and full scale output is described as 3FFH.

On the radio side, the TxI and TxQ baseband analog signals should pass through an external 15 kHz low-pass filter before entering the radio subsystem, as shown in Figure 2.

Transmit Timing

Figures 1c and 3 show the functional timing requirements for the transmit timing, as shown in Table 1. Register addresses zero through four correspond to the TxI Channel Data, TxQ

Channel Data, Control 1 Data, Control 2 Data, and Control 3 Data, respectively.

Several key concepts govern transmit timing:

1) I and Q transmit samples may be input to the CS6450 at any arbitrary point in time, and need not have any relationship to SOC or receive timing.
2) I and Q input samples must be input on a regular, periodic basis in order to avoid distortion in the internal filters.
3) I samples can be input (without inputting any Q samples) if the CS6450 is being used in a single channel mode.
4) If both I and Q samples are being input, then the two samples must be input with the second sample being written immediately after the first sample (as shown in Figure 3). Six clock cycles after the rising edge of $\overline{\text{NSTRB}}$ associated with the first sample, the latest two I and Q samples are simultaneously shifted into the DAC.
5) The control and CDAC registers can be written at any point of point, and asynchronously to any I and Q data.

Time Period	Number of 14.58 MHz Clock Periods
T1	3
T2	3
T3	1
T4	3
T5	2
T6	2
T7	1
T8	3
T9	4

During transmit, all signals on the bus interface are inputs. When $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ are low, the address appearing on the address bus (NA<2:0>) must be valid on the falling edge of $\overline{\text{NSTRB}}$. The address on the NA<2:0> bus may vary in length from 5 to 8 master clock cycles. The corresponding data for the DACs must be valid on the first rising edge of CLK occurring after the falling edge of $\overline{\text{NSTRB}}$ (Figure 1c).

Receive I & Q Data Channel

During receive, the baseband signal output by the RF subsystem should be passed through an external 81 kHz lowpass anti-aliasing filter before entering the CS6450, as shown in Figure 2.

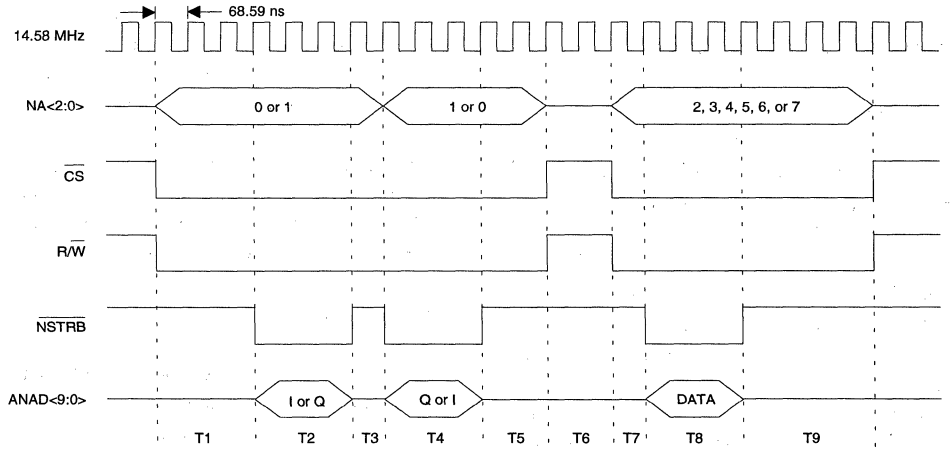


Figure 3. Transmit Timing

Inside the CS6450, the received signals pass through range-scaling channels, one channel for I and one channel for Q. Each channel consists of an 18-bit ADC, followed by an offset correction block and a digital gain block. The output of the channel is 10 bits. The gain block allows the external DSP system to determine which 10-bits of the internal 18 bits should be output. Each channel has 81 kHz bandwidth, and a group delay of 53 µs.

As discussed in the later section on system calibration, the external DSP system can write offset error correction values into the offset correction blocks. The digital gain blocks have 0 to 24 dB of gain in 6 dB steps. The gain is set by pins GS0, GS1 and GS2, as shown in Table 5.

GS2	GS1	GS0	Gain
0	0	0	Reserved
0	0	1	24
0	1	0	18
0	1	1	12
1	0	0	6
1	0	1	0
0	1	0	Reserved
1	1	1	Reserved

Table 5. Receiver Gain Control

The data conversion starts at the beginning of each sample time, as provided by the SOC signal. SOC is an asynchronous signal, and may be input at any time. Typically, the DSP digital subsystem will generate SOC using a clock recovery algorithm. In the AMPS mode of operation, the receive conversion rate is 90 kHz. In the digital TDMA mode, the receive conversion rate is 97.2 kHz. More generally, the CS6450 ADC may be sampled at any arbitrary rate from 30 kHz to 110 kHz. However, the ADC analog performance varies significantly as a function of sample rate.

The format of receiver data outputs is an unsigned binary number, where minimum input signal (-0.25 V differential) is typically converted to h000, and full scale input (0.25 V differential) is typically converted to 3FFH.

System Calibration of RxI and RxQ Offset

The ADC receiver differential inputs can be internally shorted, allowing the digital subsystem to determine the ADC offset errors, as shown in Table 4. The digital subsystem can then write the ADC offset correction values to registers 7 and 8, and the CS6450 will add an offset correction sample to all ADC outputs, before those outputs pass through the programmable gain block. The format of the offset value is 2's compliment, with the same voltage/LSB as the I and Q data samples.

Note that the offset correction is applied digitally to the output of the ADC, and will have no impact on the input range of the ADC. For example, if the ADC is clipping an overranged input signal before calibration, the ADC will still clip that same input signal after calibration.

Receive Timing

Figures 1b and 4 show the functional timing requirements for the receive timing. All signals are inputs except for ANAD<9:0> which is an output of the CS6450. The sequence of events is as follows:

1) The analog data appearing at the input to the ADC converter is sampled when the associated Start Of Conversion (SOC) signal goes low. SOC can be applied asynchronously, and is sampled on the rising edge of CLK. SOC must be low for two CLK periods.

2) Twelve master clock cycles after SOC rises, a read cycle can begin. The read read cycle has the following requirements. When Chip Select ($\overline{CS}$) goes low, the address appearing on NA<2:0> must be valid, the ReadWrite line (R/$\overline{W}$) must be high, and $\overline{NSTRB}$ must be low. Any of three ad-

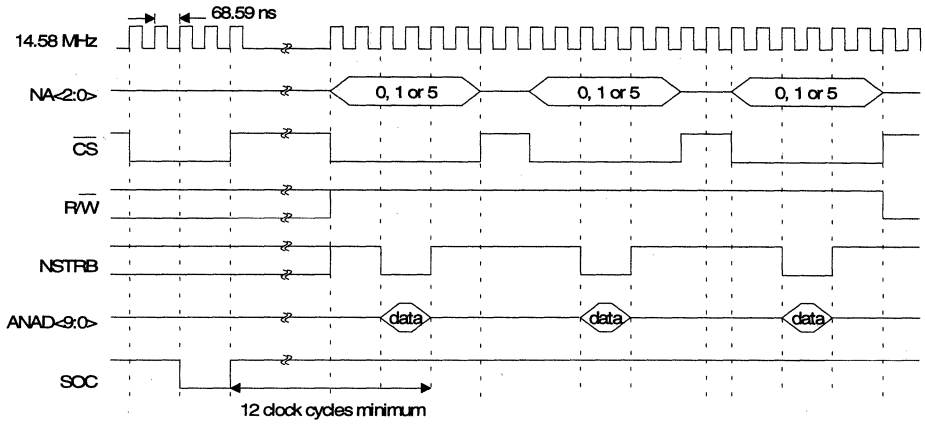


Figure 4. Receive Timing

desses may be on NA<2:0>: address 0 for reading I-channel data, address 1 for reading Q-channel data, or address 5 for reading the control register.

3) On the falling edge of $\overline{\text{NSTRB}}$, the CS6450 will make the data available on the 10-bit ANAD <9:0> data bus. This data will be valid for as long as $\overline{\text{NSTRB}}$ is low. The data becomes invalid on the falling edge of SOC, and remains invalid for 12 CLK cycles.

Typically, two read cycles will follow SOC (to read I and Q samples), although in some cases three read cycles will be used (to additionally read the control register).

Voltage References

An analog reference signal, REFOUT (nominally at 2.20V), is provided by the CS6450 to the radio to DC couple the I and Q analog signals to the corresponding RF signals. Alternately, a differential reference is provided between VREFP and VREFN. REFOUT, VREFP and VREFN should be de-coupled to ground with a 0.1 µF capacitor as shown in Figure 2, regardless of whether the outputs are used or not.

If the voltage reference is powered down via the control register, all analog output voltages become undefined.

Auxiliary Control Interfaces

The control interface consists of three 8-bit DACs where the voltage outputs can be used, for example, as automatic frequency control, automatic gain control and auxiliary signal control. The code update rate for the control channels can be up to 24.3 kHz. When a conversion is made on the digital input, the analog output will be held at a value until the next conversion.

The input data for the converters is input to the CS6450 over the parallel data bus. The output signals should be passed through external, first-order, low-pass, anti-imaging filters, as shown in Figure 2. The Figure 2 filter has a 2.4 kHz band width. Production testing is performed with a 2.5 kHz code update rate.

The range of the control DAC outputs are from 0.55V to 3.85V, and are divided into 256 steps.

If a control DAC is powered down via the control register, the output voltage becomes undefined, but the register value (DAC input

code) remains valid. When powered back up, the control DAC output returns to the register value.

Clock Input

The CS6450 operates from a single master clock having a nominal frequency of 14.58 MHz, 15 ppm, with a 70%-30% or better duty cycle.

Master Reset

An asynchronous master reset is provided to clear all registers, putting the CS6450 in a known state. $\overline{\text{RESET}}$ is active low and will override all other modes. The pulse width will be a minimum of 73.2 nsec wide, with no upper limit specified.

Loop Backs

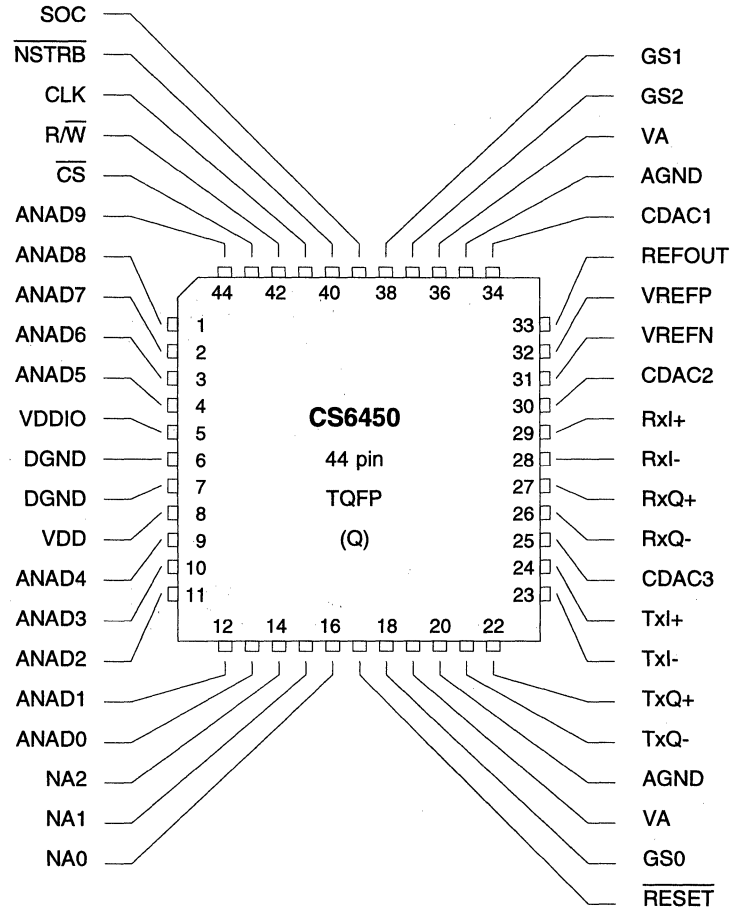
The test mode configuration consists of internal loop back paths which allow validation of the functionality of the CS6450. These loop backs are shown in the block diagram on the front page of the data sheet. When the MODE command has been issued (address 5 on the NA<2:0> bus), and the b8 and b9 register bits on the ANAD<9:0> bus are equal, the remaining bits (b0 through b7) identify which loops are activated according to Table 4.

Power Supply and Board layout Considerations

The power supply and ground pins should be de coupled with 0.1 µF capacitors as shown in Figure 2. There are no power supply sequencing requirements.

For layout guidelines, refer to the Crystal application note, "Layout and Design Rules for Data Converters".

PIN DESCRIPTIONS



Pin Descriptions

Analog I-O Pins

TxQ+, TxQ- - Q Channel, Analog Transmit Data Outputs, PINs 22 and 21.
Differential output of Q-channel signal.

TxI+, TxI- - I Channel, Analog Transmit Data Outputs, PINs 24 and 23.
Differential output of I-channel signal.

RxQ+, RxQ- - Q Channel, Analog Receive Data Inputs, PINs 27 and 26.
Differential input of Q-channel signal.

RxI+, RxI- - I Channel Analog Receive Data Inputs, PINs 29 and 28.
Differential input of I-channel signal.

CDAC1 - Control DAC 1 Analog Output, PIN 34.
Single-ended control DAC output.

CDAC2 - Control DAC 2 Analog Output, PIN 30.
Single-ended control DAC output.

CADC3 - Control DAC 3 Analog Output, PIN 25.
Single-ended control DAC output.

Parallel Bus Interface

NA2, NA1, NA0 - Address Bus Inputs , PINs 14, 15 and 16.
These pins identify the CS6450 register which is the source or sink for the data on ANAD<9:0>. NA2 is the most-significant bit, and NA0 is the least-significant bit (Table 1). These inputs should be stable on the rising edge of CLK.

ANAD9, ANAD8, ANAD7, ANAD6, ANAD5, ANAD4, ANAD3, ANAD2, ANAD1, ANAD0 - Bi-Directional Data Bus, PINs 44, 1, 2, 3, 4, 9, 10, 11, 12, and 13.
These pins contain the data being written to, or read from, the CS6450 registers. ANAD9 is the most-significant bit. ANAD0 is the least-significant bit. See Tables 2, 3 and 4. Input signals on these pins should be stable on the rising edge of CLK. Output signals are also stable on the rising edge of CLK.

R/$\overline{W}$ - Read / Write Control, PIN 42.
When high, register data is output via the parallel port. When low, data is written into the registers via the parallel port.

$\overline{CS}$ - Chip Select, PIN 43.
$\overline{CS}$ must be low during all reads and write operations via the parallel port.

$\overline{NSTRB}$ - Bus Strobe Input, PIN 40.
During parallel port inputs (register writes), NA<2:0> and ANAD<9:0> must be valid on the falling edge of $\overline{NSTRB}$, and must remain valid while $\overline{NSTRB}$ remains low. During parallel port outputs (register reads), AND<9:0> will be valid on the falling edge of $\overline{NSTRB}$, and will remain valid while $\overline{NSTRB}$ remains low.

Control Inputs

$\overline{RESET}$ - Master Reset Clears All Registers, PIN 17.
This active low signal clears all registers. $\overline{RESET}$ is asynchronous, and can be asserted at any time. $\overline{RESET}$ is sampled on the rising edge of CLK, and should be active low for a minimum of 73.2 ns.

GS0, GS1, GS2 - Receiver Gain Select, PINS 18, 37, 38.

These pins select the I and Q receiver gain level as defined in Table 5.

Clocks

SOC - Start Of Conversion for RxI and RxQ ADC's, PIN 39.

This active low signal control input causes the receiver ADCs to sample the input signals on pins RxQ± and RxI±. SOC is asynchronous, and is sampled on the rising edge of CLK.

CLK - Master Clock, PIN 41.

The master clock input should have a frequency of 14.58 MHz ± 15 ppm.

Power Supply

V_{DD} - Digital Supply Voltage, PIN 8.

Connected to 5V supply.

V_{DDIO} - Digital Supply Voltage for Digital IO, PIN 5.

Connected to 5V or 3V supply. This pin sets the logic high voltage for all digital pins (CLK, SOC, GS<2:0>, ANAD<9:0>, NA<2:0>, $\overline{\text{RESET}}$, $\overline{\text{NSTRB}}$, R/$\overline{\text{W}}$, and $\overline{\text{CS}}$).

D_{GND} - Digital Ground, PINS 6 and 7.

Connected to ground. Should be decoupled from each of V_{DD} and V_{DDIO} by 0.1 µF capacitors.

V_A - Analog Supply Voltage, PINS 19 and 36.

Connected to 5V supply.

A_{GND} - Analog Ground, PINS 20 and 35.

Connected to ground. Should be decoupled from V_A by a 0.1 µF capacitor.

Voltage References

REFOUT - Reference Voltage Output, PIN 33.

Nominally 2.2V. REFOUT can be used to provide a DC reference to the RF sub-system for the I&Q signals. REFOUT should be decoupled from ground by a 0.1 µF capacitor.

VREFP, VREFN - Differential Reference Voltage, PINs 32 and 31.

Differentially provide a nominal 2.5V. These signals can be used to provide a differential DC reference to the RF sub-system for the I&Q DAC signals. VREFP and VREFN should each be decoupled from ground by a 0.1 µF capacitor.

PARAMETER DEFINITIONS

DAC Output Range

$V_{OUT}MAX - V_{OUT}MIN$

ADC Offset Error

Measured with 0V differential input. Stated in LSB_N.

Static AC Noise Power

Noise at output of DAC with fixed DC digital input value.

LSB_N

Least Significant bit for N-bit converter. Defined as Typical Output or Input Range divided by resolution of converter. For I/Q ADC, LSB_{10} = 0.49mVp-p. For I/Q DAC, LSB_{10} = 2.1mVp-p. For control DAC, LSB_8 = 12.9 mVp-p.

• Notes •

Semiconductor Corporation

CS6453

Modem and Audio Analog Front End

Features

- Complete Voiceband DSP Front-End
  - 24-Bit A/D Converter
  - 18-Bit D/A Converter
- Minimum 84 dB Dynamic Range and 80 dB Signal-to-Distortion (at full scale)
- Supports telephone emulation
- Supports business audio
- On-chip speaker driver for modem monitoring
- Supports PCMCIA digital speaker signal
- 3.0 to 5.5V power supply range

General Description

The CS6453 is a high-resolution analog-to-digital and digital-to-analog converter for V.fast, V.32bis, V.32 and other high performance modems.

The CS6453 also supports telephone emulation. In telephone emulation, the CS6453 and external DSP collectively implement both modem and telephone set capabilities. This allows an end-user to connect a handset to the "modem" card, and alternatively use the telephone connection for voice and data.

The CS6453 has 5 kHz bandwidth for modem and telephone applications, and 10 kHz bandwidth for business audio applications. The business audio capability allows the modem to playback and input audio files.

The CS6453 also supports the digital speaker signal of the PCMCIA interface standard. The modem can transfer the modem monitor signal via PCMCIA to the system speaker.

ORDERING INFORMATION:

CS6453-CQ 44-Pin TQFP package

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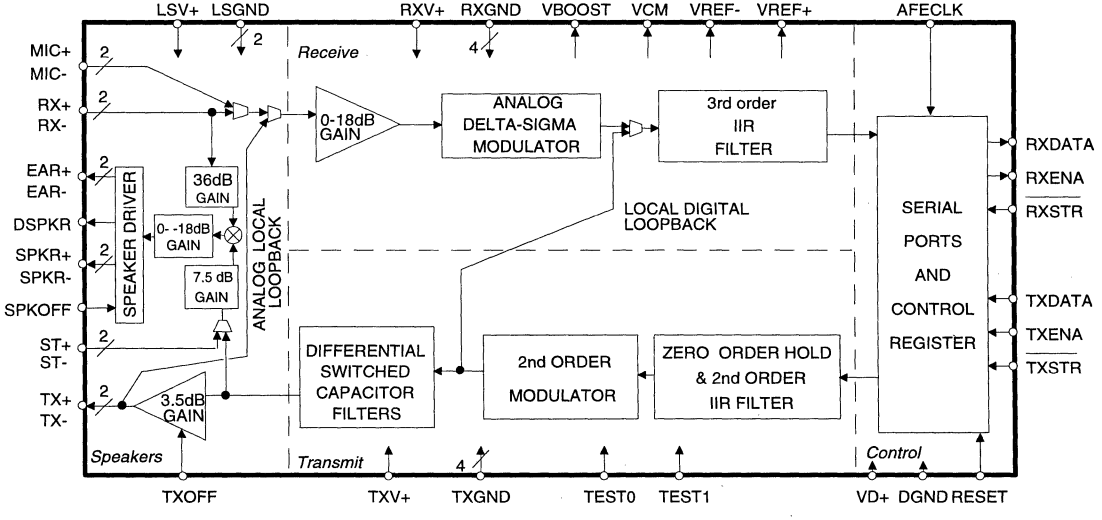

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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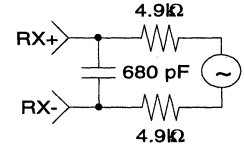
(512) 445-7222 FAX: (512) 445-7581

ANALOG RECEIVER CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input sine wave at 3.0 Vp-p; Gain = 0dB; Output sampling rate of 19.2 kHz; Speaker drivers off; RX± inputs selected; with Test Circuit (antialiasing filter) as shown below; Note 1.)

Parameter		Min	Typ	Max	Units
Resolution		24	-	-	Bits
Dynamic Performance	(Note 2)				
Dynamic Range (300 Hz to 3.3 kHz)					
gain=0dB;	- with full scale input	84	91	-	dB
	- with input 20dB below full scale	87	91	-	dB
	- BAudio=1, Low_Power=0, with full scale input	-	80	-	dB
gain=6dB;	- with full scale input	-	88	-	dB
gain=12dB;	- with full scale input	-	85	-	dB
gain=18dB;	- with full scale input	-	82	-	dB
Signal-to-Total Harmonic Distortion (300 Hz to 3.3 kHz)					
gain=0dB;	- with full scale input	80	90	-	dB
	- with input 20dB below full scale	83	90	-	dB
gain=6dB;	- with full scale input	-	90	-	dB
gain=12dB;	- with full scale input	-	90	-	dB
gain=18dB;	- with full scale input	-	90	-	dB
Idle Channel Noise	- with input at differential ground	-75	-90	-	dB
Total Absolute Gain Accuracy (300 Hz - 3.3 kHz)		-5	-	+5	%
Power Supply rejection: Passband	(Note 3)	-	60	-	dB
dc Performance					
Offset Error		-	100	-	mV
Filter Characteristics					
Passband BAudio=0, Low_Power=1	(Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0		dc	-	5	kHz
BAudio=1, Low_Power=0		dc	-	10	kHz
Passband variation from ideal (ripple) (300 Hz - 3.3 kHz)		-0.125	-	+0.125	dB
Input Characteristics					
AC Input Impedance at 1 kHz		-	27	-	kΩ
Analog Input Full Scale Signal Level (RX+ to RX-)		-	±1.5	-	V
Gain Stage Performance					
Nominal step size		5.5	-	6.5	dB

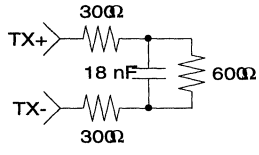
Notes:
1. 5V operation is guaranteed by design
2. Unless stated otherwise, dynamic performance is relative to 0.707x of full scale. Receiver full scale defined as $2^{21}+2^{19}+2^{18}$ (hex 2C0000). Transmitter full scale defined as $(2^{17})/1.5$ (decimal 87831).
3. With 300 mVp-p, 1 kHz ripple applied to supply.
4. Passband bandwidth specifications for BAudio=0 and Low_Power=0 are tested. All other combinations of BAudio and Low-Power are guaranteed by characterization and design.



Test Circuit

ANALOG TRANSMITTER CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input Digital sine wave with full scale 2^{17}/1.5 input; Input sampling rate of 19.2 kHz; Speaker drivers off; with Analog Load as shown below; Note 1.)

Parameter	Min	Typ	Max	Units
Resolution	18	-	-	Bits
Dynamic Performance (Note 2)				
Dynamic Range (300 Hz - 3.3 kHz)				
- with full scale input	84	90	-	dB
- with input 12dB below full scale	87	90	-	dB
- BAudio=1, Low_Power=0, with full scale input	-	80	-	dB
Signal-to-Total Harmonic Distortion (300 Hz - 3.3 kHz)				
- with full scale input	80	90	-	dB
- with input 12dB below full scale	83	90	-	dB
Idle Channel Noise - with input code of 0	-75	-	-	dB
Total Absolute Gain Accuracy (300 Hz - 3.3 kHz)	-20	-	+20	%
Power Supply rejection: Passband (Note 3)	-	60	-	dB
dc Performance				
Monotonicity	-	16	-	Bits
Filter Characteristics				
Passband BAudio=0, Low_Power=1 (Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0	dc	-	5	kHz
BAudio=1, Low_Power=0	dc	-	10	kHz
Passband variation from ideal (ripple) (300 Hz - 3.3 kHz)	-0.125	-	+0.125	dB
Output Characteristics				
Maximum output swing (TX+ to TX-)	±2.5	-	-	V
AC Output Impedance at 1 kHz	-	0.3	-	Ω
Output Current	±4	-	-	mA



Analog Load

8-ohm SPEAKER CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; Analog receiver input of 50 mVp-p, 1 kHz sine wave; Digital transmitter input of 1 kHz sine wave with peak amplitude of 35132; Speaker driver load of 8Ω; Volume gain setting = high; 8-ohm Speaker selected [Ephone=0], Note 1.)

Parameter		Min	Typ	Max	Units
Smode1=0 and Smode0=0	TX-to-SPKR gain	-	off	-	-
	RX-to-SPKR gain	-	off	-	-
Smode1=0 and Smode0=1	TX-to-SPKR gain	-	+4	-	dB
	RX-to-SPKR gain	-	off	-	-
Smode1=1 and Smode0=0	TX-to-SPKR gain	-	off	-	-
	RX-to-SPKR gain	-	+36	-	dB
Smode1=1 and Smode0=1	TX-to-SPKR gain	-	+4	-	dB
	RX-to-SPKR gain	-	+36	-	dB
Signal-to-Noise plus Distortion		30	45	-	dB
Maximum differential Output voltage		±1.6	-	-	V
Passband BAudio=0, Low_Power=1 (Note 4)		dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0		dc	-	5	kHz
BAudio=1, Low_Power=0		dc	-	10	kHz

EARPHONE CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; Analog receiver input of 40 mVp-p, 1 kHz sine wave; Digital transmitter input of 1 kHz sine wave with peak amplitude of 27447; Earphone driver load of 125Ω; Volume gain setting = high; Earphone selected [Ephone=1], Note 1.)

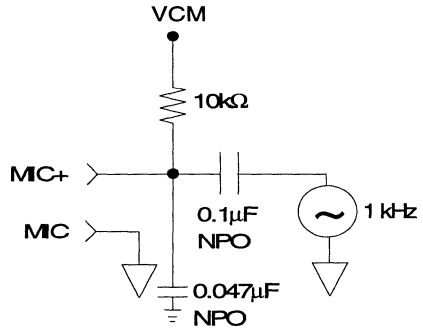
Parameter		Min	Typ	Max	Units
Smode1=0 and Smode0=0	TX-to-Ear gain	-	off	-	-
	RX-to-Ear gain	-	off	-	-
	ST-to-Ear (Note 5)		off		-
Smode1=0 and Smode0=1	TX-to-Ear gain	-	+4	-	dB
	RX-to-Ear gain	-	off	-	-
	ST-to-Ear (Note 5)		+7.5		dB
Smode1=1 and Smode0=0	TX-to-Ear gain	-	off	-	-
	RX-to-Ear gain	-	+36	-	dB
	ST-to-Ear (Note 5)		off		-
Smode1=1 and Smode0=1	TX-to-Ear gain	-	+4	-	dB
	RX-to-Ear gain	-	+36	-	dB
	ST-to-Ear (Note 5)		+7.5		dB
Signal-to-Noise plus Distortion		30	45	-	dB
Maximum differential Output voltage		±1.25	-	-	V
Passband BAudio=0, Low_Power=1 (Note 4)		dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0		dc	-	5	kHz
BAudio=1, Low_Power=0		dc	-	10	kHz

Notes: 5. When the earphone output and microphone input are both enabled and TX± enabled (TXOFF=0), the sidetone path is selected instead of the transmit path.

MICROPHONE CHARACTERISTICS (T_A = 25 °C; LSV+, TXV+, RXV+, VD+ = 3.3V; AFECLK = 5.5296 MHz; 1 kHz Input sine wave at 187.5 mVp-p; Gain = 18dB; Output sampling rate of 19.2 kHz; Speaker drivers off; with Test Circuit as shown below.)

Parameter		Min	Typ	Max	Units
Signal-to-Noise plus Distortion					
BAudio=0, Low_Power=0		-	82	-	dB
BAudio=1, Low_Power=0		-	80	-	dB
Passband BAudio=0, Low_Power=1	(Note 4)	dc	-	2.5	kHz
BAudio=1, Low_Power=1 or BAudio=0, Low_Power=0		dc	-	5	kHz
BAudio=1, Low_Power=0		dc	-	10	kHz
Analog Input Maximum Swing		-	0.75	-	V

Test Circuit



DIGITAL CHARACTERISTICS (T_A = 25 °C; TXV+, RXV+, VD+ = 3.3V; All measurements performed under static conditions, Note 1.)

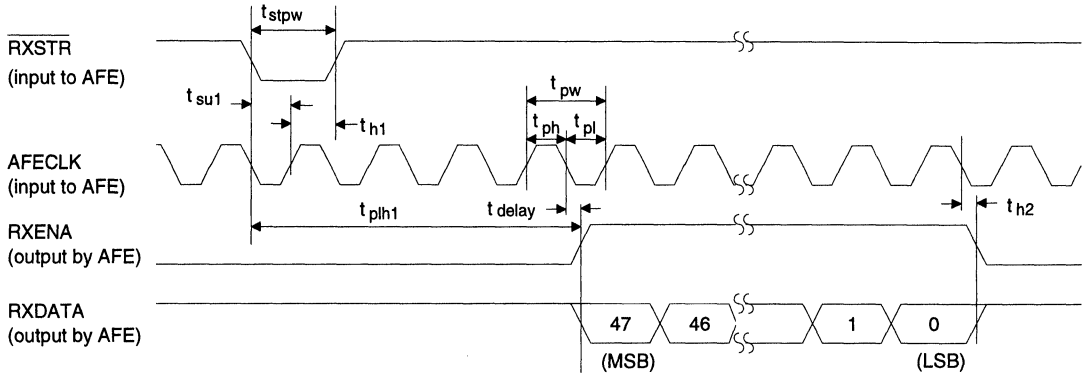
Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	(VD+)-0.5V	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.5	V
High-Level Output Voltage (Iout = -600 µA)	(Note 6)	V_{OH}	(VD+)-0.3V	-	-	V
Low-Level Output Voltage (Iout = 800 µA)	(Note 6)	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{IN}	-	-	±10	µA
Digital Output Pin Capacitance		C_{OUT}	-	9	-	pF

Note: 6. The device is designed for low current drive. Only CMOS inputs may be connected to digital outputs.

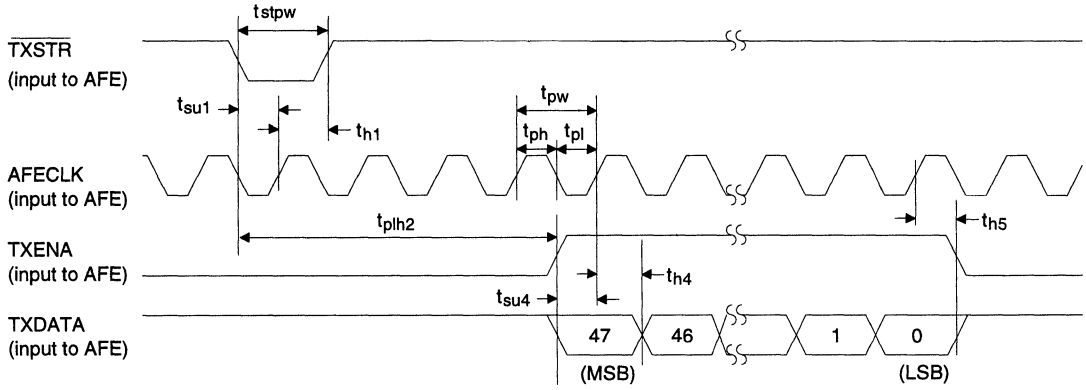
SWITCHING CHARACTERISTICS (T_A = 25 °C; CL = 50 pF; TXV+, RXV+, VD+ = 3.3V; All timing measurements performed at 50% level unless otherwise noted; Note 1.)

Parameter		Symbol	Min	Typ	Max	Units
AFECLK Clock Rate		f_{AFECLK}	1.0	5.5296	5.8	MHz
AFECLK Duty Cycle	Pulse Width	t_{pw}	172	180.85	-	ns
	Pulse Width High	t_{ph}/t_{pw}	40	-	60	%
	Pulse Width Low	t_{pl}/t_{pw}	40	-	60	%
Strobe Pulse Width		t_{stpw}	t_{pw}	-	-	ns
$\overline{RXSTR}$ and $\overline{TXSTR}$ setup to AFECLK rising		t_{su1}	25	-	-	ns
$\overline{RXSTR}$ and $\overline{TXSTR}$ hold after AFECLK rising		t_{h1}	65	-	-	ns
Receiver Delay: $\overline{RXSTR}$ low to RXENA high		t_{plh1}	-	t_{pw} * 4	-	ns
RXDATA, RXENA delay from AFECLK falling	(Note 7)	t_{delay}	-	-	60	ns
RXENA and RXDATA hold from 52nd AFECLK falling		t_{h2}	10	-	-	ns
Transmitter Delay: $\overline{TXSTR}$ low to TXENA high	(Note 8)	t_{plh2}	t_{pw} * 4	-	-	ns
TXENA andTXDATA setup to AFECLK rising	(Note 8)	t_{su4}	25	-	-	ns
TXENA and TXDATA hold after AFECLK rising	(Note 8)	t_{h4}	65	-	-	ns
TXENA and TXDATA hold from AFECLK rising on LSB	(Note 9)	t_{h5}	65	-	-	ns
RESET deasserted to $\overline{TXSTR}$ or $\overline{RXSTR}$ falling	(Note 10)	t_{delay1}	t_{pw} * 2	-	-	ns
RESET low to AFECLK rising		t_{su6}	20	-	-	ns
RESET pulse width		t_{rspw}	t_{pw}	-	-	ns
Sleep delay: last AFECLK to start of sleep mode	(Note 11)	t_{delay4}	0.001	-	1	ms
Rise Times: (see figure) Any Digital Input		t_{risein}	-	20	-	ns
Any Digital Output		$t_{riseout}$	-	15	-	ns
Fall Times: (see figure) Any Digital Input		t_{fallin}	-	20	-	ns
Any Digital Output		$t_{fallout}$	-	15	-	ns
VBOOST Settling Time	(Note 12)	t_{vboost}	-	15	-	ms
VCM Settling Time	(Note 12)	t_{vcm}	-	5	-	ms
VREF Settling Time	(Note 12)	t_{vref}	-	5	-	ms

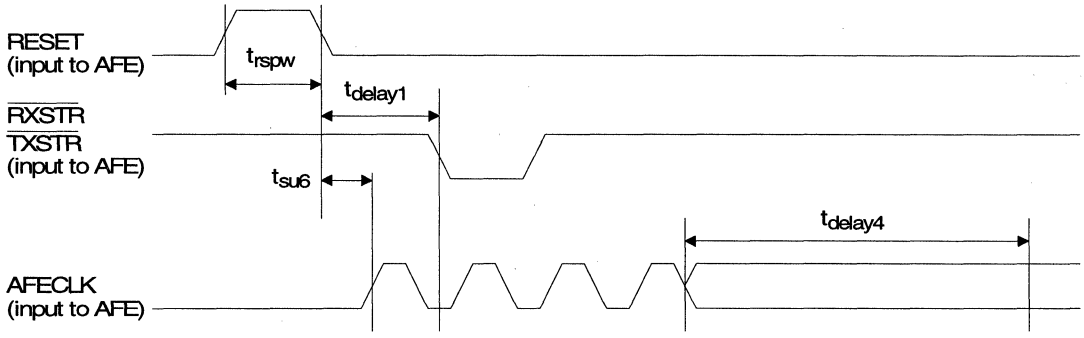
Note:
7. RXENA asserts on 4th falling edge of AFECLK after $\overline{RXSTR}$ is latched.
8. TXENA and TXDATA are ignored until the 4th AFECLK rising edge after $\overline{TXSTR}$ is latched.
9. If more than 48 bits are input, shift data into the CS6453.
10. Assert before t_{pw} * 2 after RESET is deasserted.
11. The device enters sleep mode 1 ms from the last AFECLK edge. AFECLK can idle either high or low.
12. This is the time required for the analog bias voltage to settle to its final value after power is applied, reset falls, or the clock is restored. Operation of the device before this time may yield incorrect results. The control bit FReset (see Table 2) may be asserted after the settling time for 1 sample to ensure a consistent starting state. All zero input data should be written on bits 6-23 and 30-47 when removing FRESET (falling) to avoid a race condition between the new data and reset being removed. The control bits 0-5 and 24-29 may be high or low as needed.



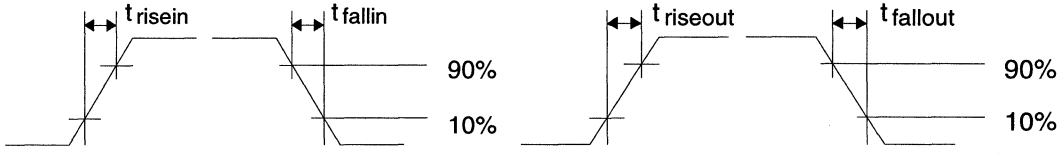
Serial Data Output Timing



Serial Data Input Timing



Reset and Power-down Timing



Rise and Fall Times

RECOMMENDED OPERATING CONDITIONS

(TXGND, RXGND, DGND, LSGND = 0V, Note1.)

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 13)	TXV+, RXV+, VD+, LSV+	3.0	3.3	5.5	V
Analog Current Consumption (TXV+ plus RXV+) (Note 14)					
Low_Power = 0, TXOFF = 0		-	20	TBD	mA
Low_Power = 0, TXOFF = 1		-	11	TBD	mA
Low_Power = 1, TXOFF = 0		-	12	TBD	mA
Low_Power = 1, TXOFF = 1		-	7	TBD	mA
(power-down mode)		-	25	150	µA
Digital Current (VD+) Power = 0	I_d	-	1.5	-	mA
Speaker driver current (no load)					
8-ohm Speaker selected		-	6.5	-	mA
Earphone selected		-	2.5	-	mA
RX+/RX- Source impedance		-	-	5	kΩ
8-ohm Speaker current (SPKR+, SPKR-)	I_{lds}	-	-	250	mA
Earphone current (Ear+, Ear-)	I_{ear}	-	-	10	mA

Note: 13. All voltages with respect to ground.
14. Speaker drivers off; current consumption applies to 3 and 5V operation.

6

ABSOLUTE MAXIMUM RATINGS

(TXGND, RXGND, DGND, LSGND = 0V; all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supply	TXV+, RXV+, VD+, LSV+	-0.3	6.0	V
Input Current (Note 14) Any pin except supplies and SPKR±	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	0.3 + RXV+	V
Digital Input Voltage	V_{IND}	-0.3	0.3 + VD+	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	-65	150	°C

Note: 15. Transient currents up to 200 mA will not cause SCR latch-up.

WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS6453 functions as an analog front end to a DSP, allowing the DSP to send and receive modem, telephone and business audio signals. The CS6453 provides a complete data conversion subsystem for voice band signal processing. The A/D converter (including sample/hold and much of the antialiasing filtering), D/A converter, and voltage reference are on-chip.

As shown in Figure 1, for modem applications, the TX± and RX± pins connect to the modem Data Access Arrangement. To support the monitoring of modem call progress, the CS6453 can drive a 8-ohm loud speaker via pins SPKR±, and drive a personal computer speaker via pin DSPKR. For telephone and business audio applications, the EAR± output pins connect to the earphone speaker, and the MIC± input pins connect to the microphone.

The CS6453 is a single channel device, and supports modem and voice communications on an non-simultaneous basis. Either the RX± inputs or the MIC± signals may be multiplexed into the A/D channel.

A 5.5296 MHz clock must be supplied to the CS6453 pin AFECLK. The CS6453 divides AFECLK input signal by two or four to generate an oversampling clock.

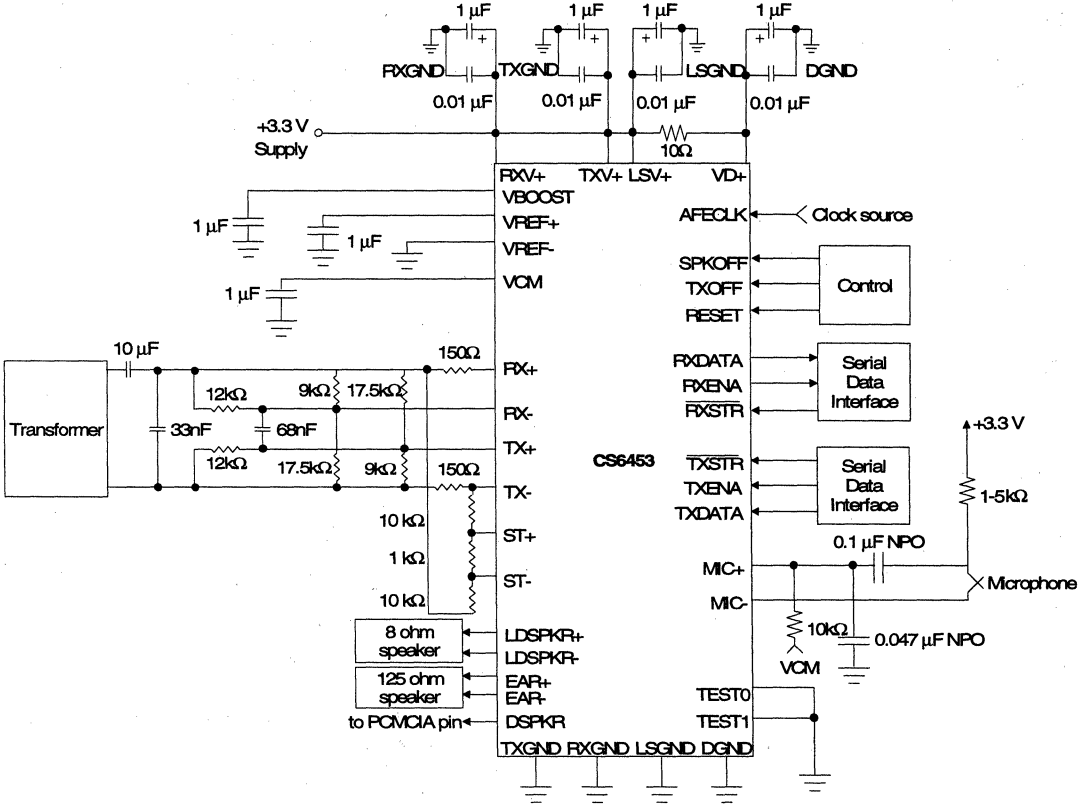


Figure 1. Recommended Connection Diagram

SUPPORT OF MODEM STANDARDS

The CS6453 dynamic range is designed for V.32 and higher-performance standards. For V.22 and lower performance standards, the CS6453 has better analog performance than is required. For these lower performance modems, the CS6453's power requirements can be reduced by approximately 50%. The power reduction will result in reduced analog specifications, as shown in the specification tables.

To place the CS6453 in the low-power V.22 mode, set control bits Low_Power and BAudio to 1. With bit Low_Power enabled (low-power mode), the internal sampling clock is reduced by one-half, cutting the filter bandwidth in half. This allows certain analog sections to be throttled back in power. The selection of business audio doubles the digital filter bandwidth. The net effect is retaining the 5 kHz bandwidth. Note that in this V.22 mode, the filter update rate is $f_{AFECLK}/4$ instead of $f_{AFECLK}/2$. The serial port operation is unchanged in this mode.

RECEIVER

The full scale input range of the CS6453 is nominally ±1.5 V differential. The CS6453 is production tested with a 50 ohm source impedance. However, the receiver can be used with higher source impedances. When the source impedance exceeds 5k ohms, the linearity of the ADC may be degraded.

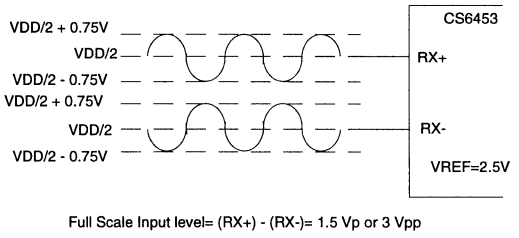


Figure 2. Full Signal Input Voltage

A programmable gain block precedes the ADC. Four gain options (0 dB, 6 dB, 12 dB, 18 dB) are selectable via the control register.

The 3rd-order modulator has an oscillation detection circuit. When oscillation is detected, the modulator is collapsed to a 1st-order modulator for 32 AFECLK clock cycles. After that interval, the modulator returns to third order. It is expected that certain input signals, such as busy tones, will cause the reduction to 1st order. While operating as a 1st-order loop, noise performance is degraded.

The converter's serial output appears MSB-first in 2's complement format (see Table 1). A digital 24-bit output of $2^{21} + 2^{19} + 2^{18}$ (hex "2C0000") corresponds to a full scale, 3.0 V peak-to-peak differential, input (see Figure 2).

The receiver creates 24-bit samples, which are available at a 2.7648 MHz rate (1.3824 MHz for Power = 1). The DSP will request samples at a rate of approximately 19.2 kHz. Each request results in the two most-recent samples being transferred to the DSP.

	Bits	Mnemonic	Function
(MSB)	47-24	RXSAMP1	RX Sample #1, MSB first
(LSB)	23-0	RXSAMP2	RX Sample #2, MSB first

Table 1. Receive Serial Data Output Word

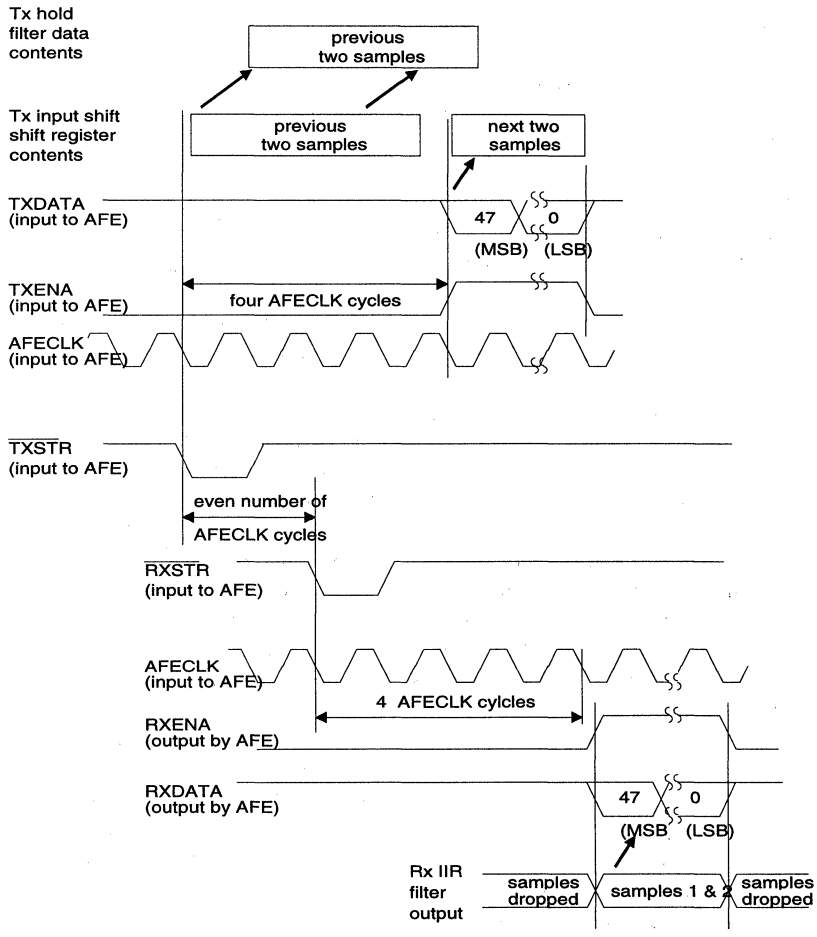


Figure 3. Receive and Transmit Signal Timing (Power=0)

Serial Data Out: AFE to DSP

The serial output port is used to output data words from the receiver. Output consists of 48 bits, written MSB first, on pin RXDATA. The DSP requests to receive 48 bits from the CS6453 by strobing $\overline{\text{RXSTR}}$ low (see Figure 3). The falling edge of $\overline{\text{RXSTR}}$ must be synchronous with the falling edge of AFECLK. $\overline{\text{RXSTR}}$ signal must also be properly phased with the $\overline{\text{TXSTR}}$ signal. If not, the $\overline{\text{RXSTR}}$ will be ignored, that is to say, $\overline{\text{RXSTR}}$ is sampled internally with the sampling clock whose phase is determined by $\overline{\text{TXSTR}}$. A properly phased $\overline{\text{RXSTR}}$ signal is a multiple of 2 or 4 AFECLK cycles from the latest $\overline{\text{TXSTR}}$ signal. When the CS6453 senses that $\overline{\text{RXSTR}}$ is low, then four AFECLK cycles later, the CS6453 sets RXENA high, and transfers 48 bits to the DSP using AFECLK. RXDATA is valid, and may be sampled, on the rising edge of AFECLK.

Receiver Filtering Considerations

The digital filtering is located after the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself).

In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS6453's analog modulator and digital filter reserve headroom such that the device can process signals with amplitude approaching ±2 V, and still output accurately converted and filtered data.

In applying the CS6453, aliasing occurs during both the initial sampling of the analog input at $f_{s_{in}}$ (2.7648 MHz for Low_Power=0, 1.3824 MHz for Low_Power = 1), and during the digital decimation process. Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate, $f_{s_{in}}$. That is, any noise within ± 5 kHz bands around $f_{s_{in}}$, 2 $f_{s_{in}}$, 3 $f_{s_{in}}$, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled.*

Since the signal is heavily oversampled (144:1), a single-pole passive RC filter can typically be used as shown in Figure 1. Any nonlinearities contributed by this filter will be encoded as distortion by the CS6453. Therefore low distortion, high frequency capacitors such as NPO (or COG) ceramic are recommended.

TRANSMITTER

The CS6453 utilizes the delta-sigma technique of executing low-cost, high-resolution D/A conversions. A delta-sigma D/A converter consists of three basic blocks: an interpolator, a 2nd-order digital modulator and an analog filter.

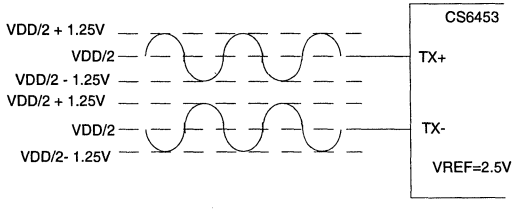
The analog output is driven differentially from TX+/TX-. An analog output amplitude of ± 2.5 V corresponds to a full scale input (87381 decimal which equals $(2^{17})/1.5$, after analog loopback calibration. Refer to Figure 4 and the System Calibration section. The transmitter driver can be powered down using pin TXOFF.

Serial Data In: DSP to AFE

The converter's serial input appears MSB-first in 2's complement format (Table 2). Upon each strobe to the CS6453 from the DSP, two events occur. (Figure 3). First, the old data words, received following the previous strobe, are input to the filter. The first of the old words is input to the DAC for one clock cycle (2.7648 MHz for Low_Power = 0, 1.3824 MHz for Low_Power = 1).
The second of the old words is input to the DAC continuously until the next strobe occurs.

The second event is that two new words are received by the CS6453, and are stored in a shift register until the next strobe occurs.

Data is transferred using four input pins: TXSTR, AFECLK, TXENA and TXDATA. Input consists of 48 bits, written MSB first, on pin TXDATA. The DSP indicates that it desires to transfer 48 bits to the CS6453 by strobing TXSTR low.



Full Scale Output level= (TX+) - (TX-)= 2.5 Vp or 5 Vpp

Figure 4. Full Scale Output Signal Level

	Bits	Mnemonic	Function
(MSB)	47-30	TXSamp1	TX Sample #1, MSB first
	29	Smode1	Speaker source control.
	28	Smode0	

Smode1	Smode0	Mode
0	0	speaker off
0	1	TX/ST only (Note 1)
1	0	RX only
1	1	TX/ST and RX (Note 1)

27	Sp1	Speaker level control.
26	Sp0	

Sp1	Sp0	Level
0	0	Mute
0	1	Low (-18 dB)
1	0	Medium (-6 dB)
1	1	High (0 dB)

25	RXGain1	Receiver Modulator Gain control
24	RXGain0	

RXGain1	RXGain0	Gain
0	0	0 dB
0	1	+6 dB
1	0	+12 dB
1	1	+18 dB

23-6	TXSamp2	TX Sample #2, MSB first
5	BAudio	Enable Business Audio filters (1=filter bandwidth of 10 kHz; adjusts filter coefficients).
4	FReset	Filter reset enable (1=clear the filter contents).
3	Cntl1	Source for ADC Channel
2	Cntl0	

Cntl1	Cntl0	Function
0	0	RX±
0	1	Digital Local Loopback
1	0	Analog Local Loopback
1	1	Microphone

1	Low_Power	Power control. (0=full power & performance; 1= reduce power & performance; adjusts bias currents).
0	Speaker Selection	

EPHONE	Output Selected
0	8-ohm Speaker (SPKR±) & Digital speaker (DSPKR)
1	Earphone (EAR±)

Notes: 1. The sidetone path is selected over the transmit path when the earphone output, microphone input, and TX± output (TXOFF=0) are all enabled.

Table 2. Transmit Serial Data Input Word

The falling edge of $\overline{\text{TXSTR}}$ should be synchronous with the falling edge of AFECLK. The $\overline{\text{TXSTR}}$ determines the phase of the AFE's internal sampling clock (AFECLK divided by 2 for POWER=0, and AFECLK divided by 4 for POWER=1). If the $\overline{\text{TXSTR}}$'s phase is inconsistent, noise/distortion is introduced into the converters.

Four AFECLK cycles after $\overline{\text{TXSTR}}$ goes low, the CS6453 is prepared to receive data on TXDATA under control of TXENA. During these first four clock cycles, the previous data samples are being shifted into a zero order hold. Therefore, if TXENA goes high prior to four clock cycles, the new input samples are ignored until the completion of the first four clock cycles.

When TXENA goes high, 48 bits are transferred to the CS6453 using AFECLK. TXDATA is sampled on the rising edge of AFECLK.

SPEAKER DRIVERS

Three speaker outputs are provided: an 8-ohm speaker driver, a 125-ohm earphone driver, and a 1-bit digital speaker out. The 8-ohm speaker output pins allow end-users to monitor the progress of modem call set-up. The CS6453 can drive an 8-ohm speaker directly, via pins SPKR±. The digital speaker signal, output on pin DSPKR, can be connected to an external speaker driver, as might be supported in a PCMCIA application. The DSPKR signal has hysteresis to avoid chatter.

Speaker Output Enable

The desired speaker output signal is selected via bit EPHONE of the control register, and pin SPKOFF. Four configurations are available as shown in Table 3. Non-selected analog outputs are high impedance.

Selection		Output Status		
Speaker Selection bit (EPHONE)	SPKOFF Pin	Speaker	Ear-phone	Digital Speaker
0	0	on	off	on
0	1	off	off	on
1	0	off	on	off
1	1	off	off	off

Table 3. Speaker Output Enable

Speaker Output Level Control

The speaker driver outputs are controlled via the control register. The volume levels can be set with the Sp1 and Sp0 control bits (see Table 2). The relative volume levels are 0 dB (High), -6 dB (Medium), -18 dB (Low), and mute. Note that all of the speakers can be turned off by either setting Sp0 and Sp1 to 0, or by setting pin SPKOFF to logic high and bit EPHONE to 1. Using the former approach is recommended since it achieves the lowest power consumption.

Speaker Source Selection

The signal source for the speaker drivers is selected via the Smode1 and Smode0 control bits. The speaker can be driven with the transmit signal only (Smode1=0, Smode0=1), the receive signal only (Smode1=1,Smode0=0) or a combination of the transmit and receive signals (Smode1=1, Smode0=1). Typically, the "RX only" 8-ohm speaker configuration is used to monitor the modem call in progress. For applications where the hybrid completely cancels the transmit signal, the "TX and RX" configuration can be used.

For telephone emulation applications, the sidetone inputs are selected instead of the transmit outputs when the earphone output, TX± output, and microphone input are all enabled.

MICROPHONE INPUT

The microphone input is selected via the control register (bits Cntl0 & Cntl1). When selected, the MIC± pins are multiplexed into the analog receiver. The MIC+ pin must be AC coupled as shown in Figure 1. The MIC- pin provides the ground for the electret microphone. The RXgain control bits can also be used to select the microphone gain. If the microphone input is not selected then the MIC± pins are high impedance, and the external microphone circuitry is powered down.

LOOPBACKS

Two local loopbacks are provided as shown in the block diagram on the data sheet cover.

The *analog local loopback* connects the output of the transmitter to the input of the receiver's delta-sigma modulator. During analog loopback, the TX± outputs are still active.

The *digital local loopback* connects the 1-bit output of the transmitter's 2nd-order modulator to the input of the receiver's decimation filter. During digital loopback, the TX± outputs are still active.

CONTROL REGISTER

The control register is updated, once per strobe, via the TXDATA input pin. Just as is the case with the input data words, the control words are buffered for one $\overline{\text{TXSTR}}$ period. Therefore the sequence of events is the following: upon the falling edge of TXENA, the contents of the control register is updated with the "old" control bits which were input to the CS6453 following the previous strobe. Several clock periods after the $\overline{\text{TXSTR}}$ transition, "new" control bits are input on TXDATA using AFECLK and TXENA. These new bits are held temporarily in a shift register until the next strobe occurs. The control information input to the CS6453 is shown in Table 2.

The FReset control bit clears all registers in the digital modulator and filters without affecting the control bits. An asserted FReset will cause the transmitter analog outputs to tend toward the supply rails.

RESET

Taking the RESET pin high will reset the internal logic of the CS6453 and set all contents of the control register to 0. Although the rising edge of RESET asynchronously resets all internal logic, the internal reset state is not exited until the first rising edge of AFECLK after RESET is de-asserted. Analog bias voltage settling time must be allowed to elapse before full device operation is ensured (see Switching Characteristics).

The power-up reset also clears the control register. It is recommended however, that the RESET pin be brought high, then low, at least 1 ms after power is applied.

The digital filter's contents can be reset to zero via the FReset bit, located in the control register. The input data should be all zero when removing the FReset condition (FRESET falling to 0) to avoid race conditions between the data and the removal of reset. The control bits may be any value as needed.

POWER DOWN MODE

The CS6453 can be placed in a power-down standby mode by holding AFECLK static for 1 ms. The CS6453 senses the idle AFECLK and stops A/D and D/A conversions, and shuts down the serial I/O ports. Toggling the AFECLK will wake up the CS6453. Analog bias voltage settling must be allowed to elapse before full de-

vice operation is ensured (see Switching Characteristics).

SYSTEM CALIBRATION

This section describes how system calibration of receiver gain can be performed. The receiver absolute gain accuracy, before system calibration, is ±5% for the 0 dB gain setting. During calibration, the DSP uses analog loopback to send a signal from the DSP through the transmitter, and then the receiver, and back to the DSP. The transmit gain accuracy is measured. Once the transmit gain is known, the other receiver gains can be calibrated.

More specifically, a transmit gain system calibration can be performed as follows. Select the 0 dB receiver gain setting. Select analog local loopback. While in analog loopback, the DSP transmits a reference signal. The DSP measures the transmit gain by comparing the loopback receive signal to the transmitted reference signal. Once the transmit gain is known, the receive gain for the +6 dB, + 12 dB, and +18 dB gain setting can be measured in a similar manner.

APPLICATION NOTES

Table 4 summarizes the operating modes.

Telephone Emulation

The CS6453 can connect the DSP to both a telephone handset and a telephone line. In this application, the DSP can emulate the functions of a telephone set, including generating DTMF tones, and recognizing telephony signaling and supervision.

The telephone line is connected via TX±, ST±, and RX± to the Data Access Arrangement. See Figure 5. The handset earphone is connected to EAR±. The handset mouthpiece is connected to MIC±.

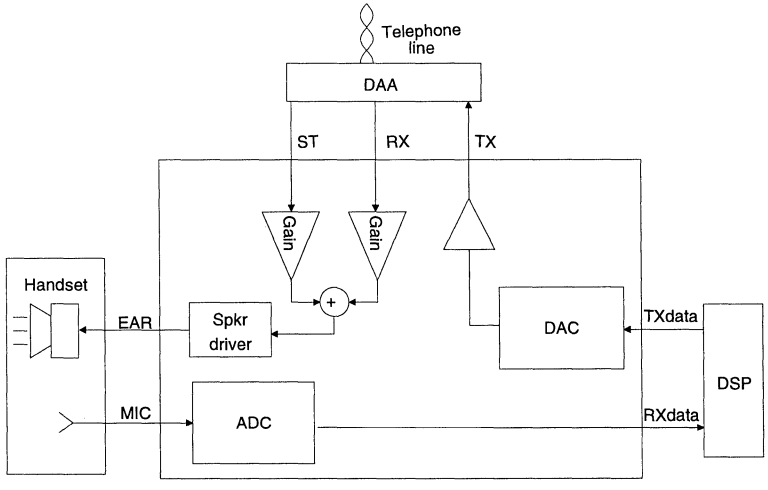


Figure 5. Telephone Emulation

Mode	Active External Interfaces	Control Selections					Input Status		Output Status				
		ADC Source (Cntl1, Cntl0)	Speaker Source (Smode1, Smode0)	Transmitter off (TXOFF)	Speaker off (SPKOFF)	Speaker Selection (EPHONE)	Microphone (MIC±)	Receiver (RX±)	Speaker (SPK±)	Earphone (EAR±)	Digital Speaker (DSKPR)	Transmitter (TX±)	Source of Handset Sidetone
Modem	DSP DAA	RX: 0,0	off: 0,0	0	1	1	off	to DAA	off	off	off	to DAA	NA
Modem with call Monitor	DSP DAA Speaker	RX: 0,0	RX only or TX & RX 1,0/1	0	0	0	off	to DAA	on; to 8-ohm speaker	off	on; not used	to DAA	NA
PCMCIA Modem	DSP DAA DSPKR	RX: 0,0	RX only or TX & RX 1,0/1	0	1	0	off	to DAA	off	off	on: to PCMCIA pin	to DAA	NA
Telephone Emulation	DSP DAA Handset	MIC: 1,1	ST & RX: 1,1	0	0	1	to handset microphone	to DAA	off	on: to 125-ohm earphone	off	to DAA	ST±, RX±
Speaker-phone	DSP DAA Speaker	MIC: 1,1	RX only: 1,0	0	0	0	to microphone	to DAA	on to 8-ohm speaker	off	on; not used	to DAA	NA
Mobile Handset	DSP Handset	MIC: 1,1	TX only: 0,1	1	0	1	to microphone	off	off	on: to 125-ohm earphone	off	off	TX±
Answer. Machine: Record	DSP DAA	RX: 0,0	off: 0,0	1	1	1	off	to DAA	off	off	off	off	NA
Answer. Machine: Playback	DSP Speaker	DC: ignored by DSP	TX only 0,1	1	0	0	DC	DC	on; to 8-ohm speaker	off	on; not used	off	NA
Business Audio	DSP Speaker Microphone	MIC: 1,1	TX only: 0,1	1	0	0	to microphone	off	on; to 8-ohm speaker	off	on; not used	off	NA

Table 4. Application Suggestions (NA=not applicable; DC=don't care)

The following control options are selected via the control register. The microphone input is enabled (Cntrl=1, Cntl0=1). The earphone drive is enabled (EPHONE=1). Side tone is provided by the speaker configuration of "ST and RX" (Smode1=1 and Smode0=1).

The sidetone signal is derived from the transmit signal via an external resistor divider. The resistor divider is external so that the sidetone signal strength can be adjusted to a particular level.

Handset Support

When the DSP needs to connect to the handset and not to a DAA (for example, in a portable radio), the transmit driver can be powered down by setting TXOFF high, cutting power dissipation by 50% (see Figure 6).

Answering Machine Application

The CS6453 can be used to playback recorded messages or screen incoming telephone calls. The audio output is provided over the 8 Ω speaker pins (SPKR±). For the answering machine playback mode, the "TX only" (Smode1=0, Smode0=1) 8 Ω speaker configuration is used. For the call screening option the "TX and RX" (Smode1=1, Smode0=1) configuration is used.

Business Audio Application

The CS6453 supports business audio application. Because of the bandwidth requirements of business audio, it is necessary to change the filter bandwidths to 10 kHz (set control bit BAudio=1), and use input/output sample rates of 38.4 kHz (which is twice the normal sample rate) on pins $\overline{\text{TXSTR}}$ and $\overline{\text{RXSTR}}$.

Typically, the audio input is received on MIC±, and the audio is output via pins SPKR± or EAR±.

POWER SUPPLY AND GROUNDING

The CS6453 can operate over the entire 3V to 5.5V power supply range.

The CS6453, along with associated analog circuitry, should be positioned in an isolated section of the circuit board, and have its own, separate, ground plane. The best solution is to place the

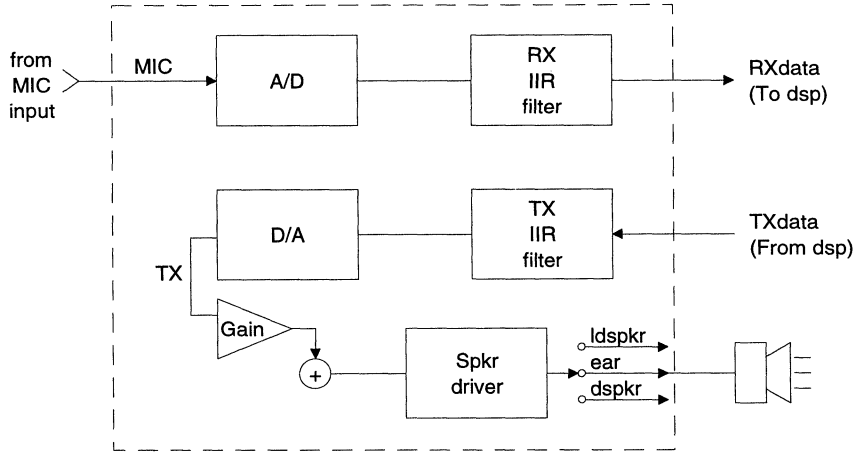


Figure 6. Mobile Handset

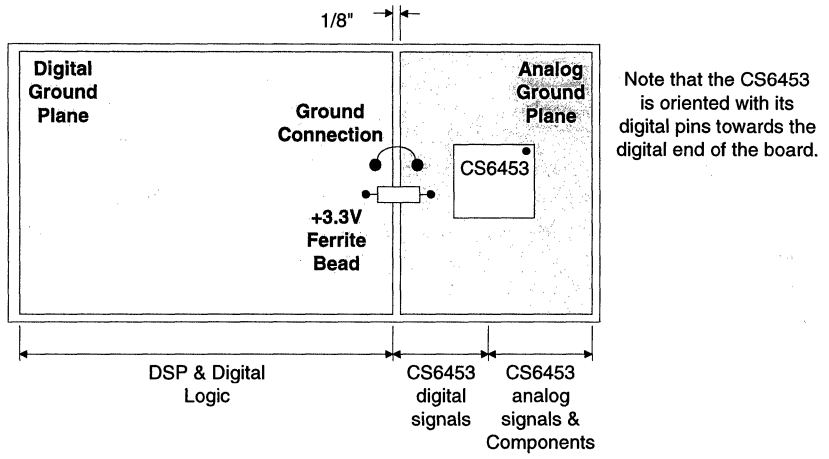


Figure 7. Suggested Layout Guidelines

entire chip on a solid ground plane as shown in Figure 7. A single connection between the CS6453 analog ground and the board digital ground should be positioned as shown in Figure 7. The TXGND, RXGND, LSGND and DGND pins must be externally connected with zero impedance between them.

Preferably, the CS6453 should also have its own power plane, isolated from the power plane for the rest of the board by a ferrite bead, as shown in Figure 7. The VD+ power supply can be derived from the TXV+, RXV+ and LSV+ supplies using the 10 ohm resistor shown in Figure 1. However, the VD+, TXV+, RXV+ and LSV+ supplies must stay within a diode drop of each other, or the chip could be permanently damaged.

Alternatively, a separate +3.3V analog supply may be used for TXV+, RXV+, LSV+.

The supply pins should be decoupled to their respective grounds as shown in Figure 1. Decoupling should be accomplished with 0.01 µF ceramic and 1.0 µF capacitors.

There are no power supply sequencing requirements.

Layout of through-hole boards

This section assumes: a surface-mount socket, leaded decoupling capacitors, and a fairly solid ground plane in either the bottom or inter-layer.

There should be a solid ground plane under the CS6453 on the same layer as the CS6453 and it should connect all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors should be placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor should be placed closest to the CS6453. Vias should be placed near the TXGND, RXGND, LSGND and DGND pins, under the IC, and should attach to the solid ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces and vias bringing power to the CS6453 should be large, which minimizes the impedance.

The trace layer (top layer) should have ground plane fill in-between the traces to minimize coupling into the analog section.

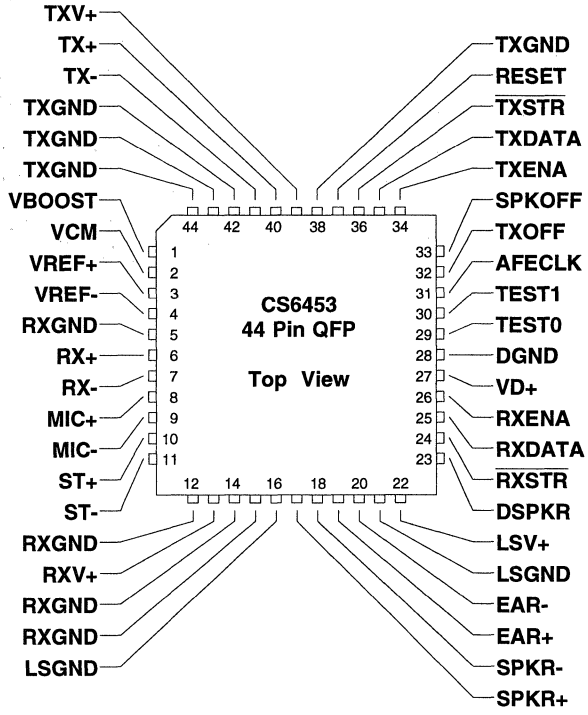
If using a through-hole socket, effort should be made to find a socket with minimum height, which will minimize the socket impedance.

Layout of surface-mount boards

If using all surface-mount components, the decoupling capacitors should be placed on the same layer as the CS6453. The vias should attach to the appropriate power and ground layers. Traces and vias bringing power to the CS6453 should be as large as possible to minimize the impedance.

Crystal publishes an Application Note entitled "Layout Rules for Analog-to-Digital and Digital-to-Analog Converters It is reprinted in the application note section of this book.

PIN DESCRIPTIONS



Power Supplies

VD+ - Digital Power, PIN 27.
Digital supply voltage. Nominally 3.3 volts.

DGND - Digital Ground, PIN 28.
Digital ground reference.

TXV+ - Transmitter Power, PIN 39.
Transmitter analog supply voltage. Nominally 3.3 volts.

TXGND - Transmitter Ground, PINS 38, 42, 43 and 44.
Transmitter analog ground reference.

RXV+ - Receiver Power, PIN 13.
Receiver analog supply voltage. Nominally 3.3 volts.

RXGND - Receiver Ground, PINS 5, 12, 14 and 15.
Receiver analog ground reference.

LSV+ - 8 Ω Speaker Power, PIN 22.
8 Ω Speaker supply voltage. Nominally 3.3 volts.

LSGND - 8 Ω Speaker Ground, PINS 16 and 21.
8 Ω speaker ground reference.

Clock

AFECLK - AFE Clock Input, PIN 31.
Must be driven by a 5.5296 MHz CMOS clock signal.

Inputs

ST+, ST- - Sidetone Inputs, PINS 10 and 11.
Sidetone differential inputs. Used by the CS6453 when earphone outputs, microphone inputs, and transmitter outputs are all enabled.

RX+, RX- - Analog Inputs, PINS 6 and 7.
Analog receiver differential inputs.

MIC+, MIC- - Microphone Inputs, PINS 8 and 9.
Microphone differential inputs.

$\overline{\text{TXSTR}}$ - Transmitter Data Input Strobe, PIN 36.
Control for transmitter serial input interface. A transition to low is a request for the CS6453 to receive two 24-bit words on TXDATA.

TXDATA - Transmitter Data Input, PIN 35.
Serial data input pin. Data is sampled on the rising edge of AFECLK. Includes two's complement format data to be transmitted plus update for the control register. See Table 1 for the format of this data.

TXENA - Transmitter Data Input Enable, PIN 34.
The rising edge indicates the start of serial data input on the TXDATA pin. The falling edge indicates the end of serial data input.

$\overline{\text{RXSTR}}$ - Receiver Data Input Strobe, PIN 24.
Control for receiver serial output interface. A transition to low is a request for the CS6453 to output two 24-bit words on RXDATA.

RESET - Reset, PIN 37.
Resets the CS6453, and clears of the control register.

TXOFF -Transmitter Off Select, PIN 32.

If set to logic high, the CS6453 powers down the TX± transmit driver.

TEST0, TEST1 - Factory Test Select, PIN 29, 30.

These pins must be held low for normal operation.

SPKOFF-SPEAKER DRIVER OFF, PIN 33.

If set to logic high, the CS6453 powers down the speaker driver.

Outputs

TX+, TX- - Transmitter Analog Outputs, PINS 40 and 41.

Analog transmitter differential outputs.

RXENA - Receiver Digital Output Enable, PIN 26.

The rising edge indicates the start of serial data output on the RXDATA pin. The falling edge indicates the end of serial data output.

RXDATA - Data Output, PIN 25.

Receiver serial data output pin. Converted data is clocked out on this pin by the falling edge of AFECLK. Data is sent MSB first in two's complement format.

SPKR+, SPKR- - 8-ohm Speaker Outputs, PINS 17 and 18.

Differential output driver pins for external 8-ohm speaker.

EAR+, EAR- - Earpiece Outputs, PINS 19 and 20.

Differential output driver pins for external 125-ohm telephone handset speaker.

DSPKR - Digital Speaker Drive Output, PIN 23.

This pin is a quantized (1-bit) representation of the speaker drive first stage output.

VREF+, VREF- - Voltage Reference Buffer, PINS 3 and 4.

The voltage references provide an internal reference. VREF+ allows the reference to be bypassed using an external 1.0 µF capacitor. VREF- should be connected to ground.

VCM - Voltage Common Mode, PIN 2.

The common mode voltage provides an external mid-scale reference for the external differential analog circuitry, and should be used, for example, as a reference for the external microphone.

VBOOST - Voltage Boost, PIN 1.

This pin is part of the internal 3V-to-5V charge pump circuit, and should be bypassed to ground with an external 1 µF cap. The nominal voltage on this pin is two times VREF. This pin should be connected only to the specified capacitor.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words from the ADCs.

Dynamic Range

Dynamic Range is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the noise floor with grounded inputs. Units in dB.

Total Harmonic Distortion

THD is the ratio of a rms full-scale signal to the rms sum of the first five harmonic components. 1 kHz is used for testing. Units in dB.

Offset Error

For the ADC, the deviation from the zero-voltage differential input voltage needed to produce an ideal mid-scale output code. For the DAC, the deviation of the output from differential zero with mid-scale input code. Units in volts for the DAC and the ADC.

Monoticity

The DAC is monotonic if every increasing input code produces a continuously increasing analog output (i.e, a differential linearity error < ±1LSB).

• Notes •

Personal Communication Technology

Crystal Semiconductor is a leading supplier of mixed-signal technology to the new and emerging Personal Digital Assistant and personal communications marketplaces, offering both standard off-the-shelf, and custom/customer specific integrated circuits.

Crystal's technology portfolio includes all of the building blocks required for PDA mixed-signal controllers. These technologies include audio codecs, radio baseband codecs, screen digitizers and DC-measurement ADCs. Crystal will design custom PDA controllers for high-volume opportunities.

CS8130 IrDA Transceiver

Crystal's first standard personal communication product is the CS8130 Multi-Standard Infrared Transceiver. The CS8130 adds an IR port to a standard UART, and implements the IrDA physical-layer. Other standards supported are HP-SIR, ASK and TV remote. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud. The CS8130 uses an external PIN diode and transmit LED.

CONTENTS

Semiconductor Corporation

CS8130

Multi-Standard Infrared Transceiver

Features

- Adds IR port to standard UART
- IrDA, HPSIR, ASK (CW) & TV remote compatible
- 1200bps to 115kbps data rate
- Programmable Tx LED power
- Programmable Rx threshold level
- Power down modes
- Direct, no modulation, mode
- Tiny 5x7mm 20 pin SSOP package
- +2.7V to +5.5V supply

General Description

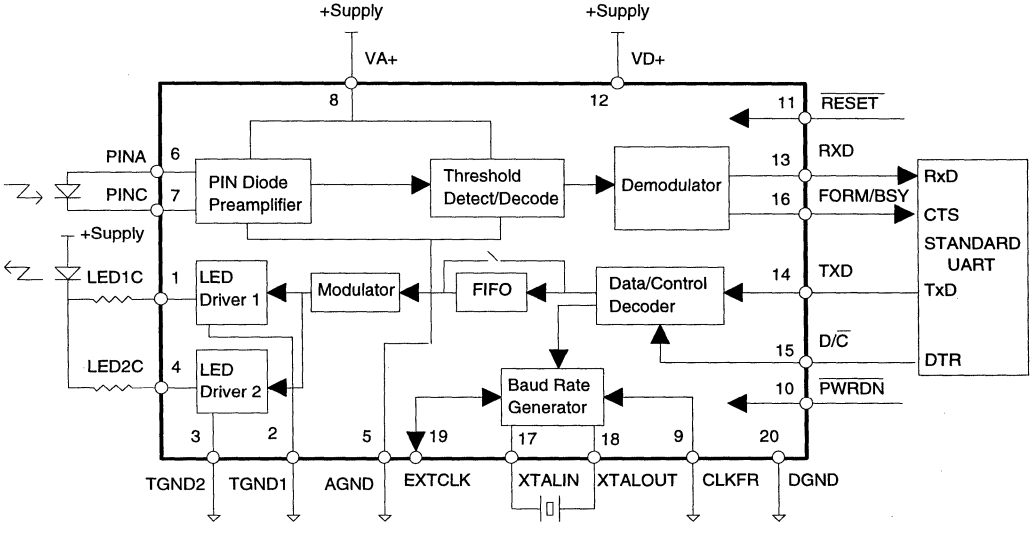
The CS8130 is an infrared transceiver integrated circuit. The receive channel includes on-chip high gain PIN diode amplifier, IrDA, HPSIR, ASK & TV remote compatible decoder, and data pulse stretcher. The transmit path includes IrDA, HPSIR, ASK & TV remote compatible encoder, and LED driver. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud.

External PIN diode and transmit LED are required. A control mode is provided to allow easy UART programming of different modes.

The CS8130 operates from power supplies of +2.7V to +5.5V.

Ordering Information:

CS8130-CS	0° to 70°C	20-pin SSOP
CDB8130 Evaluation kit		



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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TRANSMITTER DRIVER CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
Output capacitance (Note 1)			10	TBD	pF
Output rise time (10% to 90%)	tr	-	20	50	ns
Output fall time (90% to 10%)	tf	-	20	50	ns
Overshoot over final current		-	-	25	%
On resistance		-	-	0.5	Ω
Off leakage current		-	-	20	µA
Output current (each driver) (Note 2)		-	-	250	mA
Output jitter relative a jitter free input clock		-	-	200	ns

Notes: 1. Typical LED junction capacitance is 20pF.
2. 50% duty cycle, max pulse width 165 µs (3/16 of (1/1200 bps + 5%)).

RECEIVER CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Units
Input capacitance (Note 3)			-	10	TBD	pF
Input noise current			-	-	11	pA/rtHz
Maximum signal input current from detector			-	-	2	mA
Maximum DC input current (typically sunlight)			-	-	200	µA
Input current detection thresholds	RS4-0=00000:		-	7.8	-	nA
(Programmable with a 5 bit value)	RS4-0=00001:		-	15.6	-	nA
(Min, Max = Typical ±30%)	RS4-0=00010:		16.4	23.4	30.4	nA
(Note 4)	↓		↓	↓	↓	"
	RS4-0=11110:		169.5	242.2	314.9	nA
	RS4-0=11111:		175	250	325	nA
Bandpass filter response	High Pass -3dB:		-	35	-	kHz
	Low Pass -3dB:		-	700	-	kHz
Receiver power up time	With high (200µA) dc ambient		-	5	10	ms
	With normal (2µA) dc ambient		-	0.3	1	ms
Turn-around time, with receiver on continuously (Note 5)			-	5	10	ms
EMI rejection of system (0.5MHz to 100MHz). (Note 6)			3	-	-	V/m

Notes: 3. Typical PIN diode junction capacitance is 50pF.
4. The ±30% tolerance covers chip-to-chip variation. The temperature coefficient of the receiver threshold setting is low. Current detection thresholds are above the DC ambient condition. Settings of RS4-0 of less than 00010 are not practical because of noise.
5. Turn-around time is the time taken for the PIN diode receiver to recover from the IR energy from the transmitter. The remote end of the link must wait for this time after receiving data before transmitting a reply. This time may be reduced to <1 ms by good IR shielding from the transmit LED to the PIN diode.
6. This is a system specification. A metal shield over the PIN diode and CS8130 is recommended to ensure system compliance.

Specifications are subject to change without notice.

POWER SUPPLY SPECIFICATIONS (TA = 25°C; V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+, Note 7)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage		2.7	3.0	5.5	V
Power Supply Current - All functions enabled (Note 8)		-	-	2.5	mA
Power Supply Current - All functions disabled (Note 9)		-	-	1	µA
Power Supply Current - Receiver only enabled (Note 8)		-	-	2.5	mA
Power Supply Current - Transmit only enabled (Note 10)		-	-	0.5	mA
Oscillator Power Supply Current low power mode:		-	-	0.5	mA
normal power mode:		-	-	1.5	mA
Data & State Retention Supply Voltage		2	-	-	V

Notes:
7. Power supply current specifications are with the supply at 3.0V. For approximate consumption at +5.0V, multiply the above currents by 1.667.
8. Oscillator in low power mode, does not include LED current. Subtract oscillator current if using an external clock to run the CS8130.
9. Floating digital inputs will not cause the power supply to increase beyond the specification.
10. Does not include LED current, does include oscillator current in low power mode.

RECOMMENDED OPERATING CONDITIONS (All voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Units
Operating Ambient Temperature	T_A	0	25	70	°C
Data and State Retention Temperature (In Power Down)		-40	-	85	°C

DIGITAL PIN CHARACTERISTICS (TA = 25°C, Supply = 3.0V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	2.0	-	-	V
Low-level Input Voltage	V_{IL}	-	-	0.8	V
High-level Output Voltage at I_O = -2.0mA	V_{OH}	VD-0.3	-	-	V
Low-level Output Voltage at I_O = 2.0mA	V_{OL}	-	-	0.3	V
Output Leakage Current in Hi-Z state				0.2	µA
Input Leakage Current (Digital Inputs)		-	-	0.2	µA
Output Capacitance	C_{OUT}	-	5	-	pF
Input Capacitance	C_{IN}	-	5	-	pF

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ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V)

Parameter		Symbol	Min	Max	Units
Power Supplies			-0.3	6.0	V
Input Current	Except Supply Pins & Driver Pins		-	±10	mA
Input Voltage			-0.3	VD+0.3	V
Ambient temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C
ESD using human body model	(100pF with series 1.5kΩ)		2000	-	V

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Units
XTALIN frequencies	CLKFR pin low:		-	3.6864	-	MHz
(Note 11)	CLKFR pin high:		-	1.8432	-	MHz
XTALIN duty cycle			45	50	55	%
Crystal Oscillator start up time			-	-	25	ms

Notes: 11. In normal oscillator mode, the crystal is internally loaded with 20 pF, which is the standard loading at which the crystal frequency is tuned. In low power oscillator mode, the internal loading on the crystal is reduced to approximately 5pF. The crystal frequency will therefore increase by about 0.03% in low power mode.

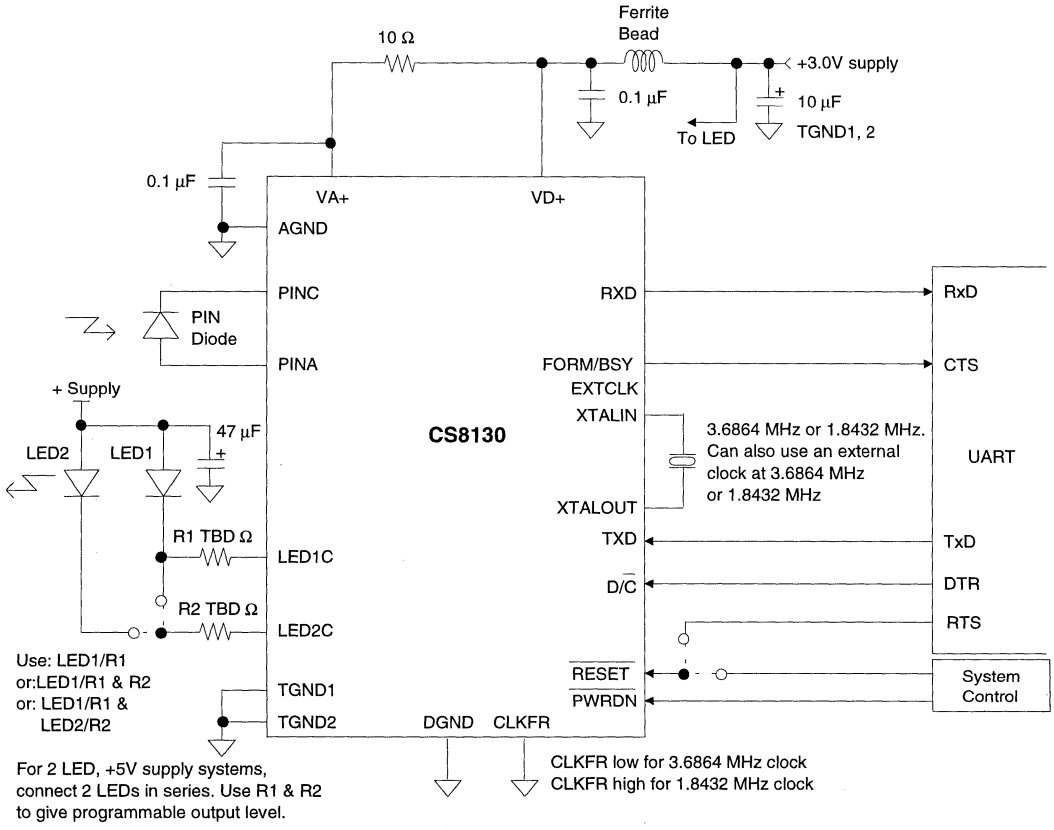

Figure 1. Recommended Connection Diagram

OVERVIEW

The CS8130 is an infrared transceiver I.C. The receive channel includes on-chip high gain PIN diode amplifier, IrDA, HP-SIR, 500 kHz Amplitude Shift Keying (ASK) & TV remote compatible decoder, and data pulse stretcher. The transmit path includes IrDA, HPSIR, 500 kHz ASK & TV remote compatible encoder, and LED drivers. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud. An on-chip baud rate generator is provided.

External PIN diode and transmit LED(s) are required. A control mode is provided to allow easy UART programming of different modes.

The CS8130 operates from power supplies of +2.7 V to +5.5 V. The device is supplied in a 20-pin SSOP package

FUNCTIONAL DESCRIPTION

The following pages describe the detailed operation of the CS8130.

IR Data Formats

The CS8130 supports three infrared data transmission formats: IrDA/HPSIR, 500kHz ASK and 38kHz ASK (TV Remote). There is also a direct access mode, which bypasses the CS8130 encoder and decoders, and gives direct access to the IR raw data. This mode is for situations where the encoding and/or decoding is done externally.

Modes may be set independently for transmit and receive, although this would be unusual.

Mode 1 IrDA/HP-SIR

The CS8130 is designed to allow easy realization of an IrDA compatible IR port (see IrDA Serial Infrared (SIR) Physical Layer Link Specification, Version 1.0, April 27 1994). Figure 2 shows the format of Mode 1. A pulse of IR energy indicates a logic '0'. No IR indicates a logic '1'. The pulse can be from 3/16 of a bit cell time at 115200 (~1.6 µs), to 3/16 of a bit cell time at 2400 bps (~78 µs). The width of the pulse may be fixed at 1.6µs for all baud rates, or may scale with the baud rate. The initial baud rate for IrDA is 9600 bps, with a negotiated baud rate possibility of 2400 to 115200 bps.

Mode 2 500 kHz ASK

Figure 3 shows the infrared data format for Mode 2. This is a Carrier Wave (CW) type system, where the presence of a 500kHz carrier is treated as a '0', and absence of a carrier is treated as a '1'. Normally used baud rates are 9600 bps, 19.2 kbps and 38.4 kbps.

Mode 3 38 kHz ASK (TV remote mode)

Figure 4 shows the infrared data format for Mode 3, the TV remote control mode. This is similar to Mode 2, except that the modulation frequency is ~38kHz. The IR bit rate is approximately 2400 bps. Both modulation frequency and bit rate vary significantly for different manufacturer and model remote controls.

Mode 4 Direct Access Mode

In Mode 4, the IR transmission tracks directly what is present on the TXD pin. A logic '1' means that the LED is off, a logic '0' means that the LED is on. Care must be taken to ensure that the LED is not 'on' continuously, otherwise the LED may be damaged.

In Mode 4, received IR is compared against the programmed threshold. The resulting logic output is routed directly to the RXD pin. A logic '1' means no IR is detected, a logic '0' means IR is being detected. If a IR carrier is being received,

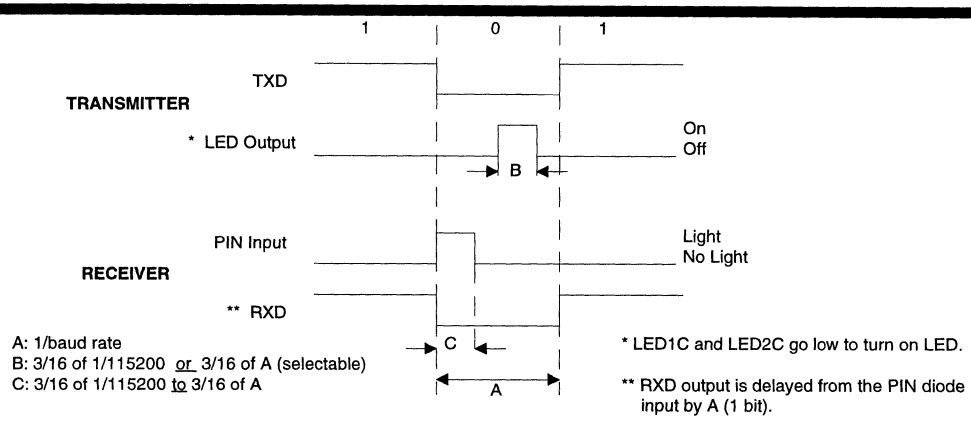

Figure 2. Infra Red Data Format Mode 1 (IRDA/HPSIR)

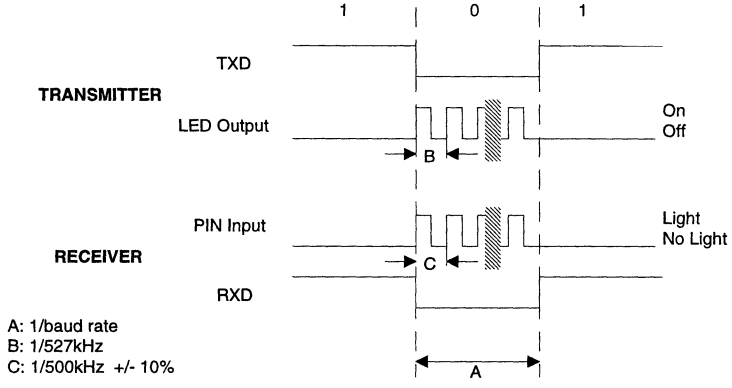

Figure 3. Infra Red Data Format Mode 2 (500kHz ASK)

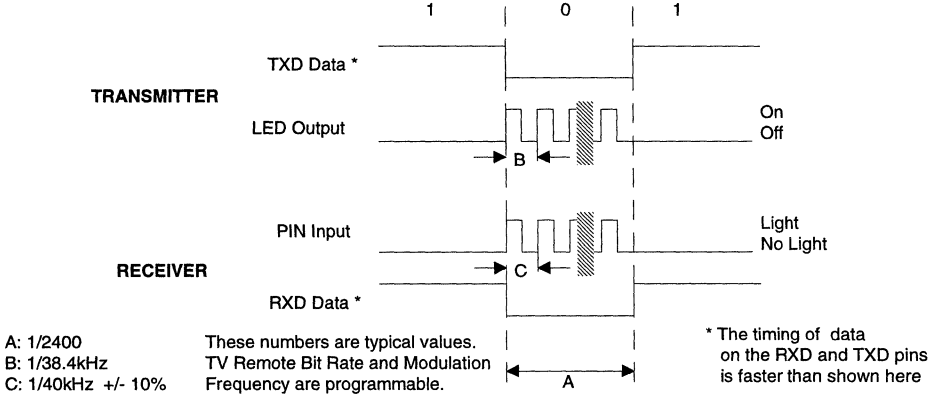

Figure 4. Infra Red Data Format 3 (TV Remote, 38kHz ASK)

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then the RXD pin will oscillate at the carrier frequency.

Transmit Path

Data for transmission is input to the CS8130 on the TXD pin. The selected modulation scheme is then applied to the data, and the resulting signals are used to drive the LED. There are 2 LED output pins: LED1C and LED2C. They are open drain outputs, which pull down to TGND or float. The LED is connected via resistors to both LED1C and LED2C. The current level flowing through the LED is determined by the external resistors. Normally, LED1C is used to drive the LED. If additional current is needed, (for example for TV remote operation), then the second driver may be enabled. The amount of 'boost' current is determined by the external resistor connected to the LED2C pin.

For larger amounts of IR output, it may be preferable to use two LEDs, rather than drive a large current through one LED. For a +3V supply system using two LEDs, each one is connected, via a resistor, to each driver output. For a +5V supply system, 2 LEDS may be connected in series, and then routed to each driver via 2 resistors, one for each driver. This minimizes the power dissipation in the resistors.

Mode 1 Transmit Choices

In Mode 1 (IrDA), the pulse width may be fixed at 1.6 µs, or set to 3/16 of the bit period. Either of these settings will meet the IrDA standard, but fixed 1.6 µs pulses will save power at lower baud rates.

In addition, there is a choice which affects the output pulse jitter. The default state causes the CS8130 to look for the start bit on TXD. All subsequent LED transitions for that character are timed relative to the internal baud rate clock. Therefore there will be no jitter in the LED output pulse timing. However, the CS8130 now has to be programmed with the desired number of bits per character, which for IrDA compliance, is 8.

Alternatively, the CS8130 can generate output pulses based entirely on individual transitions on TXD, with no knowledge of which bit is the start bit. Thus a 1 to 0 transition will generate a pulse based on that transition edge. If TXD is low for multiple successive bits, then the CS8130 will generate pulses based on its internal clock. Therefore there is the possibility of jitter in the output pulses of N*271 ns. N can be 0, 1 2....., depending on the difference in frequency between the UART baud rate clock and the CS8130 clock. Clearly, if the CS8130 and its associated UART are running from the same clock, the possibility of jitter is eliminated.

Mode 2 (ASK) Transmit Choices

The modulation frequency is determined by the modulator divider registers. For nominal 500 kHz, use a divide value of 6, which yields a modulation frequency of 527 kHz.

Mode 3 (TV Remote) Transmit Choices

During transmission of IR, the start and stop bits present in the incoming data from the UART are stripped off (see Figure 5). The remaining data bits are then sent out at ~2400 bps. Since there should be no gaps in the transmitted data, the input data is buffered in a 22-character location FIFO. Characters can be received on the TXD pin while the previous characters are being transmitted. To prevent overflow, a hardware handshake mechanism is provided. If the FIFO is one character away from being full, the FORM/BSY pin is brought high, indicating that the UART should not send any more data. Once another character has been transmitted, FORM/BSY pin is brought low, indicating to the UART that it is OK to send another character.

The modulation frequency is determined by the modulator divider registers. The transmit bit rate is determined by the TV Remote transmit bit rate divider. The UART to CS8130 baud rate must be set to at least 20% faster than the transmit bit rate.

Receive Path

A PIN diode is attached to the PINA and PINC pins. Compensation for the DC ambient light is applied to the photocurrent from the diode. The change in photocurrent from ambient is amplified and compared to a threshold value. If the photocurrent is greater than the set threshold, the output is set to 'light'. If the photocurrent is less than the set threshold, the output is set to 'no light'. The threshold current is programmable. This allows users to make the tradeoff between noise immunity and the reliable transmission distance of the link. The PIN diode amplifier has a bandpass filter characteristic, to limit the effects of IR interference. The resulting logic signal is further qualified, depending on the IR format selected.

An autodetect feature is provided. If autodetect mode is enabled, and transmit TV remote mode is disabled, the FORM/BSY output pin indicates the format of incoming data. If high, then the incoming data is in IrDA/HPSIR format. If low, the data is in ASK format which matches the programmed modulation frequency.

Mode 1 (IrDA) Receive Choices

For Mode 1a, a logic circuit is set to only look for pulse widths of 1.6µs. For Mode 1b, a logic circuit looks for pulses of 3/16 of the set baud rate bit period. For Mode 1c, a logic circuit looks for pulse widths of ≥1.6 µs, but ≤3/16 of the set baud rate bit period.

Mode 2 (ASK) Receive Choices

For Mode 2, a logic circuit looks for sequences of 'light' and 'no light' which matches the expected 500kHz carrier. The modulator divider registers must be set to 6. The ASK receive timing sensitivity register should be set to 0, yielding a valid incoming frequency range of 461 kHz to 614 kHz.

The RXD data transitions will lag behind the infrared activity by 3 modulation cycles. This allows the modulation detect circuit time to verify the correct modulation frequency.

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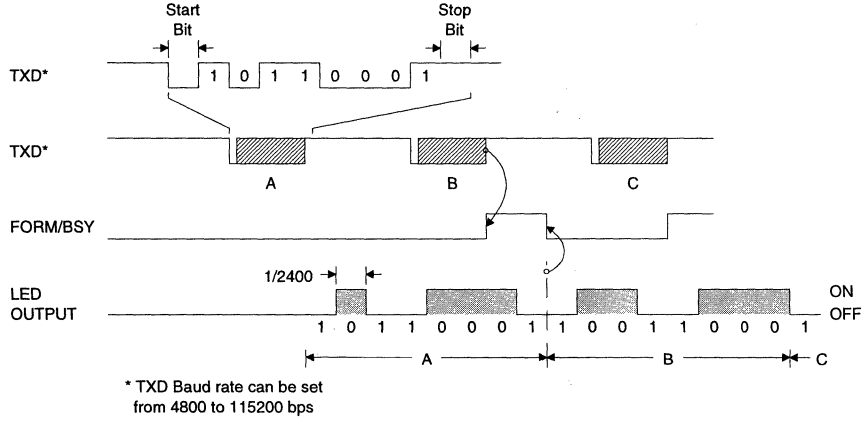

Figure 5. Mode 3 (TV Remote) Transmit Data Format

Mode 3 (TV remote) Receive Choices

The modulation frequency must be set into the modulator divider registers. The tolerance on the expected frequency must be programmed into the Receive ASK Timing Sensitivity (RATS) register. The RATS register sets the time window that the demodulator will accept for the period of valid data. Since the RATS register specifies time windows which are negative (e.g. 1000b (8) = +0.27 µs to -4.61 µs), then the modulation frequency must be set to lower than the desired nominal setting. For example, with RATS set to 1000 (8), and the desired nominal frequency being 38 kHz, then set the modulation divider registers to 35.10 kHz. With these settings, the demodulator will accept any frequency from 34.78 kHz to 41.88 kHz as valid. Smaller RATS register settings will result in tighter tolerance on the accepted receive modulation frequency. Changes in the RATS register settings must be accompanied by changes in the modulation frequency register to keep the nominal desired frequency in the center of the valid frequency band.

There are two TV remote receive data modes: "oversampled" mode and "programmed T period" mode. For "oversampled" mode, first choose the UART to CS8130 baud rate, typically 115.2 kbps. Then set the TV remote receive timing register to a rate which is less than 80% of the UART baud rate. The CS8130 will now start sampling the demodulated infrared data at the TV remote receive sample rate. The stream of samples will be assembled into characters, with a start bit and a stop bit, and will be transmitted to the UART via RXD at the UART baud rate. The system software can then concatenate successive characters and reconstruct the incoming bit stream.

"Programmed T period" mode requires that the bit period of the bursts of modulated carrier be known. This period is programmed into the TV remote receive timing registers. The UART to CS8130 baud rate must be set to at least 20% greater than 1/T. The CS8130 will now use the edges of the demodulated incoming infrared data to indicate each bit state. For continuous periods of low or high, the CS8130 will sample the level in the center of each incoming bit period (using T as the bit period). Any transition will reset the timer that is used for the sampling process, thereby eliminating errors caused by the sample timing being different to the incoming bit period. Characters are assembled and sent to the UART every 8 bits (see Figure 6).

If the T period is not known, it is possible to measure T by using "oversampled" mode, and

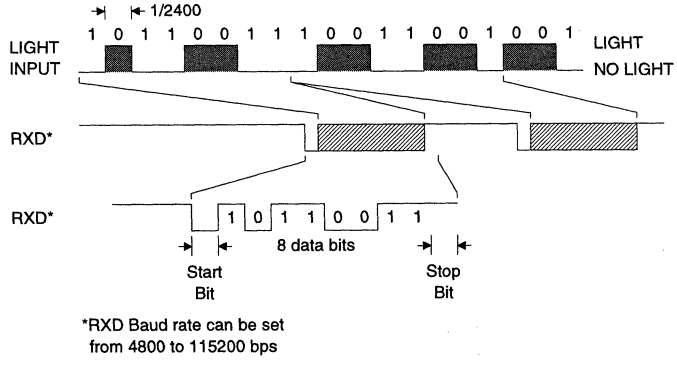

Figure 6. Mode 3 (TV remote) Receive Data Format

then switch to "programmed T period" mode to reduce processing overhead in the host CPU.

Clock Generation

The primary clock required is 3.6864 MHz. This may be generated by attaching a 3.6864 MHz crystal to the XTALIN and XTALOUT pins. In this case, the EXTCLK pin becomes an output, and may be used to drive external devices. If this is not required, power may be saved by disabling the EXTCLK output. The CLKFR pin should be connected to DGND, which causes the clock circuits to be configured for 3.6864 MHz operation.

The oscillator has a low power mode. This reduces the internal crystal loading capacitance on XTALOUT and XTALIN. The selection of this mode is via a bit in Control Register #4. Since the loading capacitance is reduced, then the crystal frequency will increase by approximately 0.03%.

Alternatively, a 3.6864 MHz clock may be input into the EXTCLK pin, in which case XTALIN must be grounded, and XTALOUT is left floating. The CLKFR pin must be connected to DGND.

If only a 1.8432 MHz clock is available, then it may be input into the EXTCLK pin and the CLKFR pin connected to VD+. This causes the CS8130 to double the incoming 1.8432 MHz clock to 3.6864 MHz for internal use. XTALIN must be grounded, and the XTALOUT pin is left floating.

The CS8130 automatically sets the direction of the EXTCLK pin. If the crystal oscillator is running when $\overline{\text{RESET}}$ goes high, then EXTCLK becomes an output. Since the crystal oscillator can take up to 25 ms to start, then it follows that $\overline{\text{RESET}}$ must be held low, with $\overline{\text{PWRDN}}$ high and power applied, for at least 25 ms. If using an external clock, then $\overline{\text{RESET}}$ low can be short (>1 µs).

Power Down

When the $\overline{\text{PWRDN}}$ pin is brought low, all internal logic is stopped, including the crystal oscillator. The power consumption in power down mode is very low (<1 µA). When the $\overline{\text{PWRDN}}$ pin is brought high, the crystal oscillator will start. If using the crystal oscillator, allow 25 ms for oscillator start up after bringing $\overline{\text{PWRDN}}$ high, before trying to use the CS8130. The control register status will not be changed by toggling $\overline{\text{PWRDN}}$.

Control Register #1 allows for individual disabling and enabling of the transmit and receive sections of the CS8130.

The CS8130 also goes into power down if both transmit enable and receive enable bits are false, and the D/$\overline{\text{C}}$ pin is brought high. This allows control of power down in a pod environment, where access to the $\overline{\text{PWRDN}}$ pin is difficult. In this mode, it is possible to select, via a control register bit, whether the crystal oscillator remains running, or is powered off. If the oscillator remains running, then it consumes power, but offers instant wake up. If the oscillator is powered off, then it consumes no power, but will take 25 ms to start up.

The $\overline{\text{PWRDN}}$ pin must always be 'high' or 'low'. If this pin is allowed to float, excessive power consumption may occur. All other digital inputs may be allowed to float without causing excessive power consumption in the CS8130 in power down mode.

The RXD and FORM/BSY output pins may be programmed to be high, low or float in power down. This allows maximum flexibility in different applications.

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Reset

Bringing the $\overline{\text{RESET}}$ pin low will force the internal logic, including the control registers, into a known state, provided the $\overline{\text{PWRDN}}$ pin is high. $\overline{\text{RESET}}$ is disabled if the $\overline{\text{PWRDN}}$ pin is low. The reset state is given in each register definition table. $\overline{\text{RESET}}$ must be low for >25 ms if using the crystal oscillator (see Clock Generation above).

Control Register Definitions

The various control registers within the CS8130 may be written by setting the D/$\overline{\text{C}}$ pin to low, and sending characters from the UART to the TXD pin. The characters are interpreted as a 4-bit address field and a 4-bit data field, as shown in Figure 7. After the control character is received and written into the control register, it is optionally echoed back out the RXD pin. The baud rate used for this control mode is whatever is currently set in the baud rate register. If the "load baud rate" bit is written to, then the new baud rate takes effect after the character has been echoed back, if echo is enabled. Otherwise, the new baud rate is effective immediately.

One of the control registers contains a shadow register set enable bit, which effectively becomes the MSB of the 5-bit register address. Hence there are 31 4-bit registers. The shadow bit must be written to a 1 to allow access to the registers with addresses 16 through 31. The shadow bit register is always accessible, independent of the state of the shadow bit. The shadow bit must be written to 0 to enable access to registers 0 through 15.

The following tables define the detailed function of all the registers inside the CS8130.

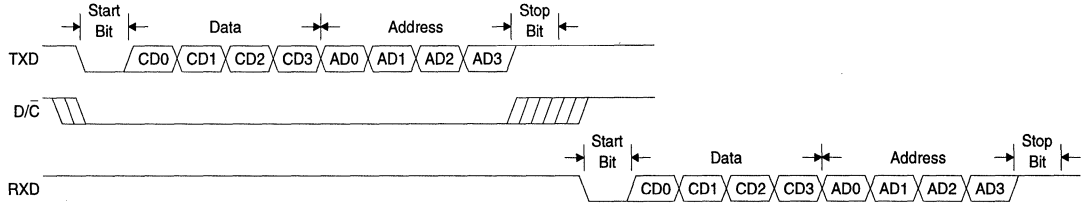


Figure 7. Control Mode Timing

Control Data Byte Format

D7	D6	D5	D4	D3	D2	D1	D0
AD3	**AD2**	**AD1**	**AD0**	**CD3**	**CD2**	**CD1**	**CD0**

BIT	NAME	VALUE		FUNCTION
AD3-0	Register Address (4 bits of transmitted address + MSB, which is the shadow (SHDW) bit state [Control Reg #3]. All registers have 4 data bits).	0_0000	0	Control register #1
		0_0001	1	Control register #2
		0_0010	2	Transmit Mode Register #1
		0_0011	3	Transmit Mode Register #2
		0_0100	4	Output Power register
		0_0101	5	Receive Mode register
		0_0110	6	Receive Sensitivity register #1
		0_0111	7	Receive Sensitivity register #2
		0_1000	8	Baud Rate Divider register #1
		0_1001	9	Baud Rate Divider register #2
		0_1010	10	Modulator Divider register #1
		0_1011	11	Modulator Divider register #2
		0_1100	12	Digital Output Pin Control register
		0_1101	13	Control Register #3
		0_1110	14	Reserved
		0_1111	15	Status register (read only)
		1_0000	16	TV Remote Receive Sample Rate & T Period Divider
		1_0001	17	TV Remote Receive Sample Rate & T Period Divider
		1_0010	18	TV Remote Receive Sample Rate & T Period Divider
		1_0011	19	TV Remote Transmit Bit Rate Divider #1
		1_0100	20	TV Remote Transmit Bit Rate Divider #2
		1_0101	21	Control Register #4
		1_0110	22	Reserved
		1_0111	23	Reserved
		1_1000	24	ASK Receive Timing Sensitivity register
		1_1001	25	Reserved
		1_1010	26	Reserved
		1_1011	27	Reserved
		1_1100	28	CS8130 Revision Level register (Read Only)
		1_1101	29	Reserved
		1_1110	30	Reserved (Resets to 1111; must not be changed)
		1_1111	31	Reserved (Resets to 1111; must not be changed)
CD3-0	Control Data			Contains control register data.

It is essential that all reserved registers and bits are not changed from their reset state. If reserved bits are changed, then internal test modes may be invoked, which may change some input pins to output pins, and may completely change the definition of some functions and signals. Reserved bits in registers, and reserved registers, may not return a known state when read, and should be ignored. Registers 28 and 15 are read only. Other non-reserved registers are write only. The CS8130 can be set to echo back register write commands to verify correct reception of the control settings.

Register 0, Control Register #1

	D3	D2	D1	D0
Register	ECHO	0	RXEN	TXEN
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
ECHO	Echo Control Characters	0 1	R	Do not echo control characters Echo control characters.
RXEN	Receiver Enable	0 1	R	Receiver disabled Receiver enabled
TXEN	Transmitter Enable	0 1	R	Transmitter disbabled Transmitter enabled

Register 1, Control Register #2

	D3	D2	D1	D0
Register	0	0	AUTD	LODB
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
AUTD	Receiver auto detect mode enable	0 1	R	Auto detect receive format disabled Auto detect receive format enabled
LODB	Load Baud Rate Counter	0 1	R	Do not load new baud rate count value Load new baud rate count value

The LODB bit resets to 0 automatically.

Register 2, Transmit Mode Register #1

	D3	D2	D1	D0
Register	DIR	TVR	PWID	MODU
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DIR	Direct Mode Enable	0 1	R	Mode 4 Direct access mode disabled Mode 4 Direct access mode enabled
TVR	TV Remote Mode Enable	0 1	R	Mode 3 TV remote mode disabled Mode 3 TV remote mode enabled
PWID	Select Pulse Width	0 1	R	Set pulse width to 1.6 µS Set pulse width to 3/16 of the bit period
MODU	Select Modulation Method	0 1	R	Mode 1 IrDA pulse modulation enabled Mode 2 Amplitude modulated carrier modulation

Register 3, Transmit Mode Register #2

	D3	D2	D1	D0
Register	0	CHSY	BC1	BC0
Reset (R)	0	1	1	0

BIT	NAME	VALUE			FUNCTION
CHSY	Character/bit synchronized	0 1		R	Bits are transmitted based on TXD bit transitions Bits are transmitted timed from the start bit
BC1-0	Number of bits per character (only needed if CHSY = 1)	00 01 10 11	0 1 2 3	R	6 data bits per character 7 data bits per character 8 data bits per character 9 data bits (8 data, 1 parity) per character

Register 4, Output Power Register

	D3	D2	D1	D0
Register	0	0	OP1	OP0
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
OP1-0	Output Power Level	00 01 10 11	0 1 2 3	R	No LED output enabled LED1C output only enabled LED2C output only enabled Both LED1C and LED2C outputs enabled

Register 5, Receive Mode Register

	D3	D2	D1	D0
Register	RTVR	RMOD	RWIDS	RWIDL
Reset (R)	0	0	1	1

BIT	NAME	VALUE			FUNCTION
RTVR, RMOD, RWIDS, RWIDL	Receive Mode	0000	0		Mode 2 Amplitude modulated carrier mode
		0001	1		Mode 1a IRDA - fixed 1.6µs pulse
		0010	2		Mode 1b IRDA - variable 3/16 bit cell time pulse
		0011	3	R	Mode 1c IRDA - Any width pulse from 1.6µs to 3/16 bit cell time
		0100	4		Mode 4 Direct access mode
		1000	8		Mode 3 TV remote mode, oversampling receive
		1100	12		Mode 3 TV remote mode, timed bit cell receive
		All other combinations are reserved			

Register 6, Receive Sensitivity Register #1

	D3	D2	D1	D0
Register	RS3	RS2	RS1	RS0
Reset (R)	0	1	1	1

Register 7, Receive Sensitivity Register #2

	D3	D2	D1	D0
Register	0	0	0	RS4
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
RS4-0	Receive threshold setting.	00000	0		7.8 nA nominal receive threshold
		00001	1		15.6 nA nominal receive threshold
		"	"		"
		00111	7	R	62.5 nA nominal receive threshold
		"	"		"
		11110	30		242.2 nA nominal receive threshold
		11111	31		250 nA nominal receive threshold

Threshold settings of less than 20nA should not be used because background noise will cause the apparent occurrence of constant signal.

Register 8, Baud Rate Divider Register #1

	D3	D2	D1	D0
Register	BR3	BR2	BR1	BR0
Reset (R)	0	1	1	1

Register 9, Baud Rate Divider Register #2

	D3	D2	D1	D0
Register	BR7	BR6	BR5	BR4
Reset (R)	0	0	0	1

BIT	NAME	VALUE			FUNCTION
BR7-0	Baud Rate Divider Value (BRD). BRD=(3.6864E6/ (16*BR))-1, where BRD = divider value and BR = desired baud rate.	01011111	95		2400 bps
		00101111	47		4800 bps
		00010111	23	R	9600 bps
		00001011	11		19.2 kbps
		00001001	5		38.4 kbps
		00000010	2		76.8 kbps
		00000001	1		115.2 kbps

Register 10, Modulator Divider Register #1

	D3	D2	D1	D0
Register	MD3	MD2	MD1	MD0
Reset (R)	0	1	1	0

Register 11, Modulator Divider Register #2

	D3	D2	D1	D0
Register	MD7	MD6	MD5	MD4
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
MD7-0	Modulator Divider Value (MD). MD=(3.6864E6/FR)-1, where MD = divider value and FR = desired modulation frequency.	01100000	96		38 kHz
		00000110	6	R	527kHz

The transmitted modulation frequency will be exact. The receive carrier detection frequency can be slightly different from the programmed frequency (see Receive ASK Carrier Timing Register).

Register 12, Output Pin Control Register

	D3	D2	D1	D0
Register	RXDT	RXDH	FORT	FORH
Reset (R)	0	1	0	1

BIT	NAME	VALUE		FUNCTION
RXDT	RXD output pin three-state enable	0 1	R	In power down, RXD will go high or low. In power down, RXD will float.
RXDH	RXD output pin high/low enable	0 1	 R	In power down, RXD will go low, if RXDT = 0 In power down, RXD will go high, if RXDT = 0
FORT	FORM/BSY output pin three-state enable	0 1	R	In power down, FORM/BSY will go high or low. In power down, FORM/BSY will float.
FORH	FORM/BSY output pin high/low enable	0 1	 R	In power down, FORM/BSY will go low, if FORT = 0 In power down, FORM/BSY will go high, if FORT = 0

Register 13, Control Register #3

	D3	D2	D1	D0
Register	0	0	0	SHDW
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
SHDW	Shadow register set enable	0 1	R	Enable access to registers 0 though 15 Enable access to shadow registers (16 through 31)

Register 15, Status Register

	D3	D2	D1	D0
Register	0	OSCR	ERR	DMOD
Reset (R)	0		0	0

BIT	NAME	VALUE		FUNCTION
OSCR	Oscillator running flag	0 1		Oscillator not running, using external clock input, oscillator circuit is powered down. Oscillator running, EXTCLK is an output, if enabled.
ERR	Framing error flag	0 1	R	No error A framing error has occurred since the last read of this bit. Resets after read
DMOD	Detected Modulation Type	0 1	R	IrDA pulse style data format detected Amplitude modulated carrier style data format detected

To read this register, write 0000 to address 15. Independent of the setting of the ECHO bit, the CS8130 will transmit the above contents, with an address field of 1111.

Register 16, TV Remote Receive Timing Register #1

	D3	D2	D1	D0
Register	TVR3	TVR2	TVR1	TVR0
Reset (R)	1	1	1	1

Register 17, TV Remote Receive Timing Register #2

	D3	D2	D1	D0
Register	TVR7	TVR6	TVR5	TVR4
Reset (R)	1	1	1	1

Register 18, TV Remote Receive Timing Register #3

	D3	D2	D1	D0
Register	TVR11	TVR10	TVR9	TVR8
Reset (R)	0	1	1	1

BIT	NAME	VALUE	FUNCTION
TVR11-0	TV remote mode receiver timing register TVR = (3.6864E6 * T) -1 where T = the incoming bit period, and TVR = this register value.	000000000000 0 000000000001 1 ↓ ↓ 011111111111 2047R ↓ ↓ 111111111111 4095	T = 271 ns T = 542 ns ↓ T = 555 µs (1800 bps) ↓ T = 1.11 ms

For TV remote receive "oversampled" mode, this register value determines the input data sample rate. The sample rate is 3.6864 MHz divided by this register value. The sample rate should be set to as fast as possible, to give the best resolution on the incoming data edges, but should be less than 80% of the main UART communication baud rate.

For TV remote receive "programmed T period" mode, this register sets the expected incoming bit cell time (T). The main UART communications rate must be set to at least 20% greater than 1/T.

Register 19, TV Remote Transmit Bit Rate Divider Register #1

	D3	D2	D1	D0
Register	TBR3	TBR2	TBR1	TBR0
Reset (R)	1	1	1	1

Register 20, TV Remote Transmit Bit Rate Divider Register #2

	D3	D2	D1	D0
Register	TBR7	TBR6	TBR5	TBR4
Reset (R)	0	1	1	1

BIT	NAME	VALUE	FUNCTION
TBR7-0	TV remote mode transmit bit rate register TBR= (3.6864E6/(16*RATE)) -1 where TBR is this register value & RATE is the desired transmit bit rate.	01111111 127 R	RATE = 1800 bps

Register 21, Control Register #4

	D3	D2	D1	D0
Register	OSCE	OSCL	EXCK	SRES
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
OSCE	Disable crystal oscillator in D/$\overline{C}$ controlled power down state	0 1	R	In D/$\overline{C}$ controlled power down state, crystal oscillator stays running. In D/$\overline{C}$ controlled power down state, crystal oscillator stops.
OSCL	Set oscillator in low power mode	0 1	R	Oscillator in normal power, high accuracy, mode. Oscillator in low power, medium accuracy mode.
EXCK	Disable external clock output driver	0 1	R	If crystal is used, enable clock output driver If crystal is used, disable clock output driver (Hi-Z)
SRES	Software Reset	0 1	R	Normal operation Causes a software reset, which forces all registers into their reset state. If ECHO is true, then the echo will occur at the current baud rate, before the baud rate changes to the default value.

Register 24, Receive ASK Timing Sensitivity Register

	D3	D2	D1	D0
Register	RAT3	RAT2	RAT1	RAT0
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
RAT3-0	Receiver ASK Timing Sensitivity. Timing window = +0.27 µs to -RAT(2/3.6864E06) - 0.27 µs	0000 0001 0010 ↓ 1111	0 1 2 ↓ 15	R	+0.27 µs to -0.27 µs window (500 kHz ASK mode) +0.27 µs to -0.54 - 0.27 µs window +0.27 µs to -1.08 - 0.27 µs window ↓ +0.27 µs to -8.14 - 0.27 µs window

The timing window is relative to the modulation divider register nominal setting.

Register 28, CS8130 Silicon Revision Register

	D3	D2	D1	D0
Register	REV3	REV2	REV1	REV0

BIT	NAME	VALUE	FUNCTION
REV3-0	CS8130 silicon revision level	0000	1st silicon, designed to meet DS134PP2 data sheet, dated June 1994

This register should be read by the CS8130 driver to allow CS8130 future enhancements to be recognized, and incorporated into future versions of the driver.

Grounding & Layout

Grounding and layout for the CS8130 are critical, because of the sensitive nature of the PIN diode amplifier. The CS8130 should be over its own dedicated ground plane. The PIN diode should be very close to the PINA and PINC pins. The PIN diode traces should be very short (< 5 mm), and should be surrounded by ground plane. There should be holes in the ground plane provided for mounting a metal shield over the CS8130 and the PIN diode for EMI shielding. The PIN diode and transmit LEDs should be positioned so as to line up the front optical surfaces of the packages. The optical surface of the PIN diode and transmit LED(s) should be positioned 1cm back from the daylight IR filter window inside the case of the equipment. This ensures that direct sunlight does not fall upon the top surface of the PIN diode.

An evaluation kit, CDB8130, is available from Crystal. This may be used as an example of the correct layout for the CS8130 and the optical components.

Optical Components

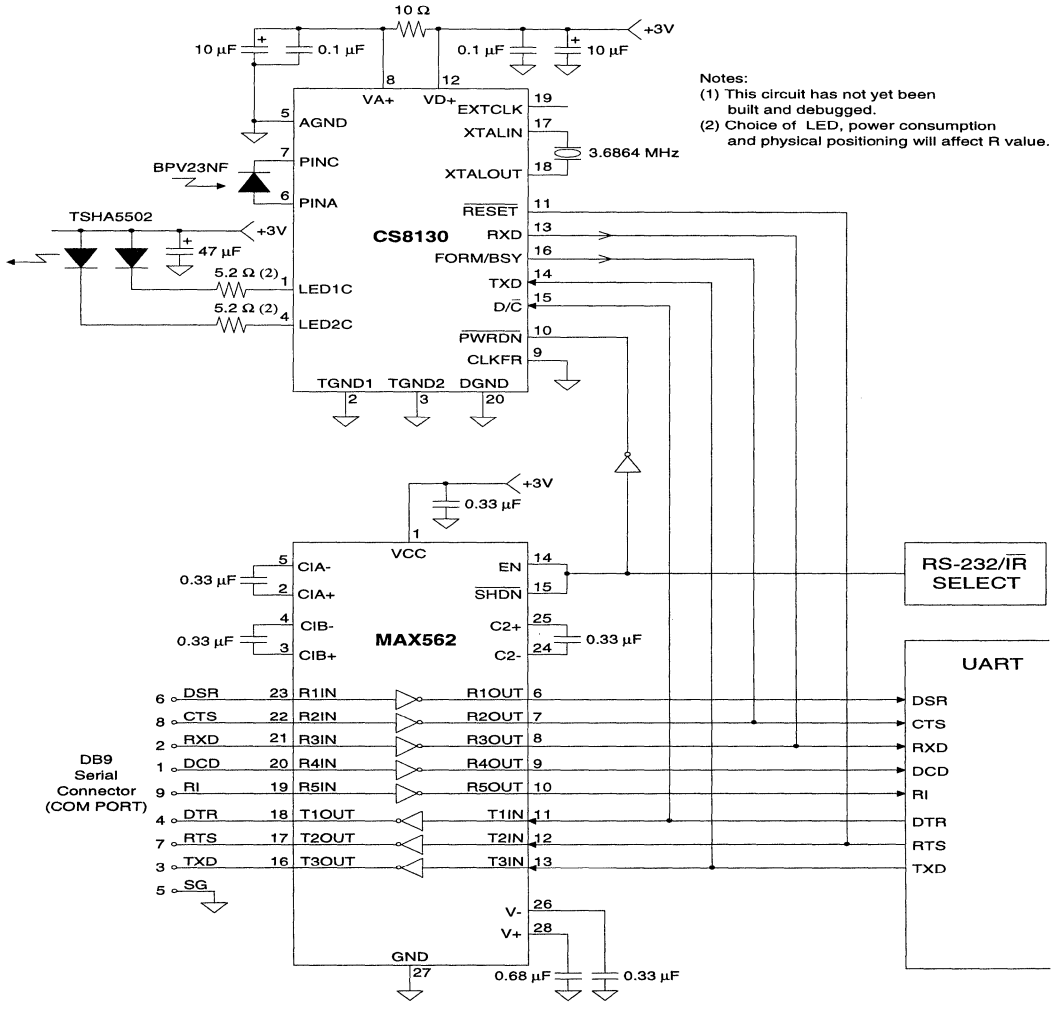
TEMIC (Tel: 408 970 5684) provides Telefunken infrared LEDs and PIN diodes which are compatible with the CS8130. Contact Crystal for details of additional qualified LED and PIN diode sources.

Example Application Schematics

Crystal has prepared some example schematics which demonstrate possible uses for the CS8130.

Figure 8 shows a computer or PDA motherboard example, where one UART is used to drive both a wired RS232 COM port and an IR port.

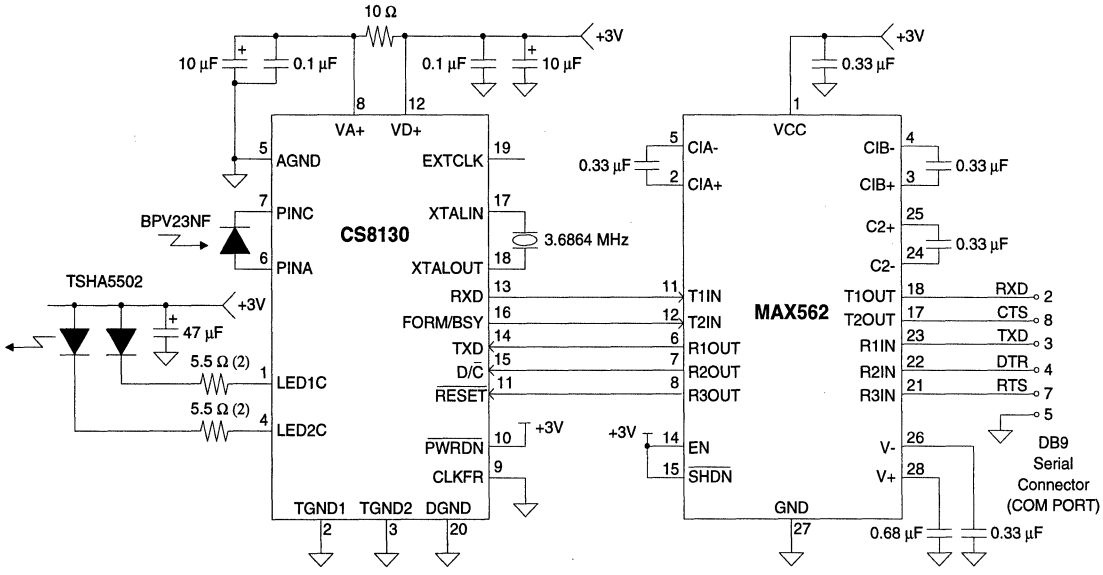
Figure 9 shows a pod schematic. This is an external unit which can be plugged into any existing COM port to create an IR port.



UART to both RS232 and IR Port Interface
Motherboard Example Schematic

Steven Harris
Crystal Semiconductor
5/26/94

Figure 8. IR and RS232 from 1 UART



Notes:
(1) This circuit has not yet been built and debugged.
(2) Choice of LED, power consumption and physical positioning will affect R value.
(3) The creation of +3V or +5V supply is not included here.

RS232 COM PORT to Infra Red Interface
Pod Schematic

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Crystal Semiconductor
5/26/94

Figure 9. Example Pod Schematic

LED1 CATHODE	**LED1C**	1	20	**DGND**	DIGITAL GROUND
TRANSMIT GROUND 1	**TGND1**	2	19	**EXTCLK**	EXTERNAL CLOCK
TRANSMIT GROUND 2	**TGND2**	3	18	**XTALOUT**	CRYSTAL OUTPUT
LED2 CATHODE	**LED2C**	4	17	**XTALIN**	CRYSTAL INPUT
ANALOG GROUND	**AGND**	5	16	**FORM/BSY**	FORMAT/BUSY
PIN DIODE ANODE	**PINA**	6	15	**D/$\overline{C}$**	DATA/CONTROL
PIN DIODE CATHODE	**PINC**	7	14	**TXD**	TRANSMIT DATA
ANALOG SUPPLY	**VA+**	8	13	**RXD**	RECEIVE DATA
CLOCK FREQUENCY	**CLKFR**	9	12	**VD+**	DIGITAL SUPPLY
POWER DOWN	**$\overline{PWRDN}$**	10	11	**$\overline{RESET}$**	RESET

Power Supplies

VD+ - Digital Positive Supply.
Digital positive supply voltage. Nominally +3V

VA+ - Analog Positive Supply.
Analog positive supply voltage. Nominally +3V.

DGND - Digital Ground.
Digital ground, 0V, connection.

AGND - Analog Ground.
Analog ground, 0V, connection.

TGND1, TGND2 - Transmitter Grounds.
LED Transmitter grounds, 0V, connections.

Analog Pins

LED1C, LED2C - Transmit LED Cathode.
These pins are connected to the transmit LED cathode via resistors. Appropriate resistor choice allows user setting of LED current options. The anode of the LED is connected to the positive supply.

PINC - Receiver PIN Diode Cathode
Receiver PIN diode cathode.

PINA - Receiver PIN Diode Anode.
Receiver PIN diode anode.

Digital Pins

RXD - Receiver Data Output

Receiver output data. Normally connected to RxD on the UART.

TXD - Transmit Data Input

Transmitter input data. Normally connected to TxD on the UART.

D/$\overline{C}$ - Data/Control Mode Input

The D/$\overline{C}$ pin determines whether the input data on TXD is treated as data to be transmitted via the LED, or as control information to set up the CS8130 internal registers. The D/$\overline{C}$ pin also can act as a power down control.

FORM/BSY - Received Data Format Output/Busy Signal Output

If auto format detect mode is enabled, this pin indicates the format of the incoming data. FORM is low for ASK format data, and high for IRDA/HPSIR format data.

In TV remote data mode (Mode 3), this pin becomes a handshake signal to the UART. FORM/BSY low means OK to send a character. FORM/BSY high means "I am busy, do not send another character".

PWRDN - Power Down Control Input

PWRDN low places the CS8130 into a very low power consumption "off" state.

RESET - Reset Input

RESET low places all the internal logic into a known state. All the control register bits are forced high or low, as defined in the register definition section. If the crystal oscillator is in use, then $\overline{\text{RESET}}$ must be held low for >25 ms, with PWRDN high and power applied. If an external clock is used, then the $\overline{\text{RESET}}$ pulse can be short (>1 µs).

XTALIN, XTALOUT - Crystal Connections

To use the internal oscillator, connect either a 3.6864 MHz or a 1.8432 MHz crystal between XTALOUT and XTALIN. If using an external clock, connect XTALIN to DGND.

EXTCLK - External Clock Input or Output

If no crystal is present on XTALIN and XTALOUT, EXTCLK becomes an input. A 3.6864 MHz or 1.8432 MHz clock should be connected to EXTCLK. XTALIN should be connected to DGND.

If a crystal is present on XTALIN and XTALOUT, EXTCLK becomes an output. EXTCLK will output the same frequency as the crystal. The EXTCLK output driver may be disabled to conserve power.

CLKFR - Clock Frequency Select Input

Tie CLKFR to ground to select a 3.6864 MHz clock. Connect CLKFR to the VD+ pin to select a 1.8432 MHz clock.

INTRODUCTION

Crystal Semiconductor pioneered and brought delta-sigma conversion technology to production in a variety of digital audio A/D and D/A converter products. These products address both high-end, performance-driven audio systems (see CS5389 and CS4303) and low cost, high integration applications (see CS5336/8/9 and CS4328/30).

CS3310 Volume Control

The CS3310 is a stereo analog volume control, allowing volume level adjustment from -95.5dB to +31.5dB in 0.5dB steps. The volume level is changed via a simple serial digital control bus, which is cascadeable for multiple parts. Low glitch circuit design ensures no "zipper" noise during volume changes. Exceptionally low THD and noise allow use in consumer and professional applications.

CS4225 Two ADC, Four DAC Codec

Intended for automotive and surround sound applications, the CS4225 includes two 16-bit ADCs and four 16-bit DACs. The analog inputs have level adjustment and the analog outputs include an output level attenuator. The device has many clocking modes, including using the on-chip PLL for locking onto an audio sample rate clock. The CS4225 runs from +5V and has a low power standby mode.

CS4303 Digital to Analog Converter

The CS4303 is an all digital I.C. containing an 8X interpolation filter and overall 64X oversampling delta-sigma modulator. Addition of an external analog reconstruction filter yields 107 dB dynamic range with superb low level linearity.

CS4328 Digital to Analog Converter

The CS4328 is the industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X delta-sigma modulator, 1-bit D/A converter and a 124 dB signal-to-noise ratio analog anti-imaging filter, all in one packaged, tested, solution. The device features patented delta-sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This approach is particularly insensitive to clock jitter and allows the benefit of scaling the bandwidth proportionally to the system master clock. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface makes with CD player circuitry, DAT recorders and DSP's.

CS4330/1/3 Digital to Analog converter

Packaged in an 8 pin SOIC, the CS4330 is the world's smallest stereo audio DAC. This 18-bit complete digital-to-analog output system contains interpolation filters, 128X oversampling delta-sigma modulators, 1-bit D/A converters, and analog filtering. De-emphasis is also included for CD applications.

CS5330 Low Power A/D Converter

The CS5330 is a single chip, 18-bit, stereo A/D converter requiring only 100mW of power from a single +5V supply. The part features two 128x oversampling delta-sigma modulators, two digital decimation filters and a voltage reference in an 8 pin SOIC package.

CS5336/8/9 Delta-Sigma Audio A/D Converters

This new class of device features 64X oversampling, using a Delta-Sigma architecture with resolutions of 16 or 18-bits. Output word rates can be from 1 kHz to 50 kHz. These stereo parts have 2 sample and holds, dual Delta-Sigma modulators, two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measurements include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

CS5349 Single Supply, Stereo A/D Converter for Digital Audio.

The CS5349 is a complete, 16-bit analog-to-digital converter for stereo digital audio systems that require a single +5V supply. Similar to the CS5339, the CS5349 features 64X oversampling Delta Sigma conversion with on-chip sample and hold, filtering and voltage reference in a 28-pin package.

CS5389 & CS5390 Professional Audio Analog to Digital Converters

The CS5389 is Crystal's newest audio A/D converter aimed at the professional audio market. Dual differential inputs, with special modulator design, yield a dynamic range of 107 dB. Excellent noise rejection and low idle tones yield a superbly performing A/D Converter.

The CS5390 is pin compatible with the CS5389, and offers increased dynamic range and 20-bit output data words.

CS8401A, CS8402A AES/EBU & S/PDIF Transmitters

The CS8401A & CS8402A accept digital audio in many standard formats and generate an AES/EBU or S/PDIF compatible data stream. The CS8401A is software programmable for mode and for channel status and user data. The CS8402A is pin programmable.

Audio A/D Converter Comparison Table

Device	CS5330/1	CS5336	CS5338	CS5339	CS5349	CS5389	CS5390
Number of Bits	18	16	16	16	16	18	20
Dynamic Range (dB)	96	95	95	95	90	107	110
SOIC Package	✓	✓	✓	✓	✓	-	-
Filter Passband (kHz)	0-21.7	0-20	0-22	0-22	0-22	0-22	0-22
Filter Transition Band (kHz)	21.7-28	20-26	22-28	22-28	22-28	22-28	22-28
Stop Band Attenuation (dB)	-80	-80	-80	-80	-80	-80	-100
Overrange Tag Bits	-	✓	✓	✓	✓	-	-
Left/Right Tag Bits	-	✓	✓	✓	✓	-	-
Master Clocking Mode	✓	✓	✓	✓	✓	✓	✓
SCLK active edge	↓	↑	↑	↓	↓	↓	↓
Master Clock Frequency (CFs)	256/384/512	256/384	256/384	256/384	256/384	256/384	256/384
Power Supply Voltages (V)	+5	±5	±5	±5	+5	±5	±5
Operation < 30 kHz without TEST Mode	✓	✓	✓	✓	✓	✓	✓
Power Consumption mW	100	400	400	400	325	550	550

All frequencies are with an output word rate of 48 kHz

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CS8411, CS8412 AES/EBU and S/PDIF Receivers

The CS8411 and CS8412 digital audio receivers accept AES/EBU or S/PDIF signals and generate digital audio in many standard formats. A low jitter PLL recovers a clean clock for system use. The CS8411 is software readable for channel status and user data. The CS8412 is pin programmable

CS8425 A-LAN - Audio Local Area Network Transceiver

The CS8425 is an S/PDIF transceiver with on-chip low jitter PLL. A ring of CS8425 devices forms an Audio Local Area Network, where user data bits may be used for system messages between nodes. Intended for automotive applications, the device finds use wherever audio and some additional low bandwidth information needs to be communicated between multiple devices.

CONTENTS

Semiconductor Corporation

CS3310

Stereo Digital Volume Control

Features

- Complete Digital Volume Control
  - 2 Independent Channels
  - Serial Control
  - 0.5 dB Step Size
- Wide Adjustable Range
  - -95.5 dB Attenuation
  - +31.5 dB Gain
- Low Distortion & Noise
  - 0.001% THD+N
  - 116 dB Dynamic Range
- Noise Free Level Transitions
- Channel-to-Channel Crosstalk Better Than 110 dB

General Description

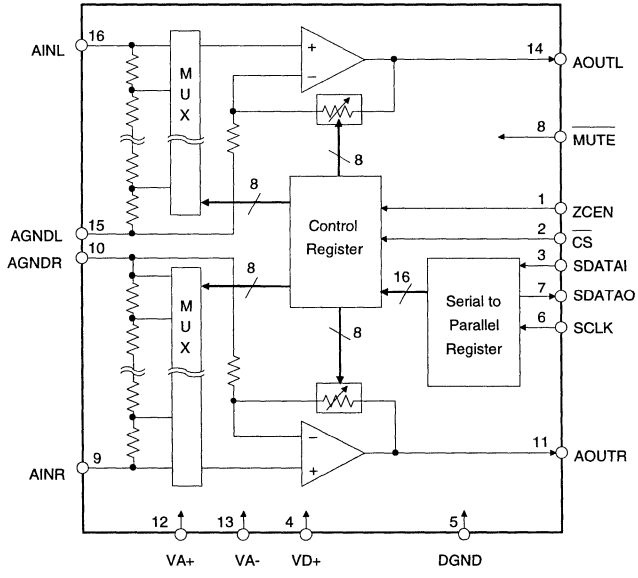
The CS3310 is a complete stereo digital volume control designed specifically for audio systems. It features a 16-bit serial interface that controls two independent, low distortion audio channels.

The CS3310 includes an array of well-matched resistors and a low noise active output stage that is capable of driving a 600 Ω load. A total adjustable range of 127 dB, in 0.5 dB steps, is achieved through 95.5 dB of attenuation and 31.5 dB of gain.

The simple 3-wire interface provides daisy-chaining of multiple CS3310's for multi-channel audio systems.

The device operates from ±5V supplies and has an input/output voltage range of ±3.75V.

For more information call (512)445-7222 and ask for the Audio Databook.



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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS4225

Digital Audio Conversion System

Features

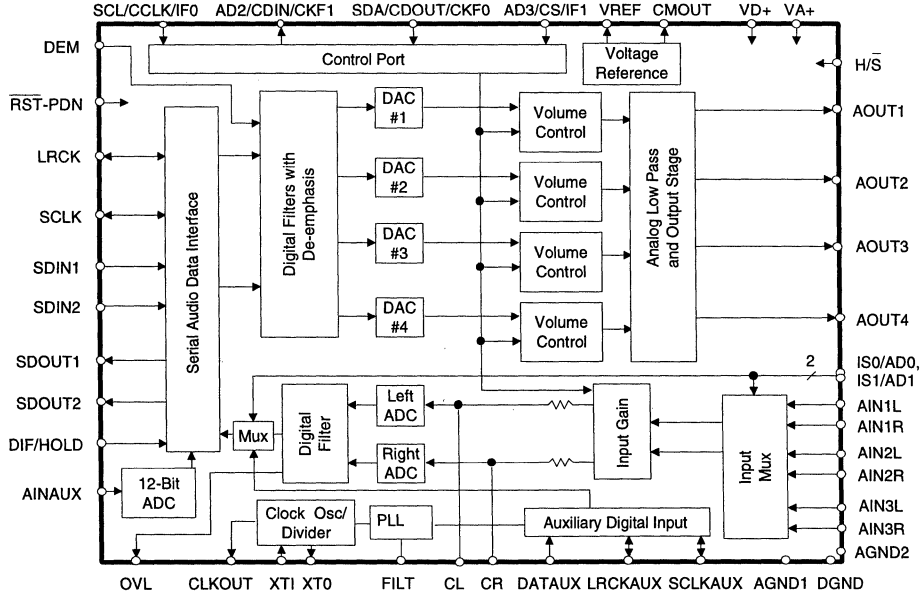
- Stereo 16-bit A/D Converters
- Quad 16-bit D/A Converters
- Sample Rates From 4kHz to 50kHz
- >100 dB DAC Signal-to-Noise Ratio
- Variable Bandwidth Auxiliary 12-bit A/D
- Programmable Input Gain & Output Attenuation
- +5V Power Supply
- On-chip Anti-aliasing and Output Smoothing Filters
- Error Correction and De-Emphasis

Description

The CS4225 is a single-chip, stereo analog-to-digital and quad digital-to-analog converter using delta-sigma conversion techniques. Applications include CD-quality music, FM radio quality music, telephone-quality speech. Four D/A converters make the CS4225 ideal for surround sound and automotive applications.

The CS4225 is supplied in a 44-pin plastic package with J-leads (PLCC) or as a die.

For more information call (512)445-7222 and ask for the Audio Databook.



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS4303

107 dB, D/A Converter for Digital Audio

Features

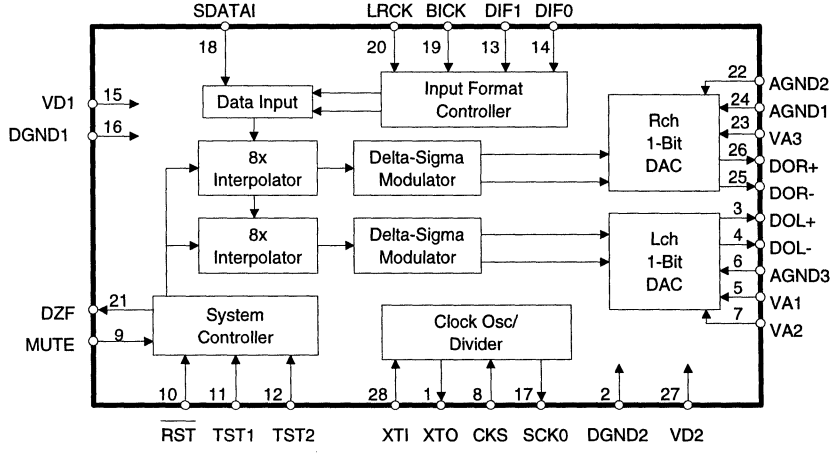
- Stereo Delta-Sigma D/A converter
  8× Interpolation Filter
  64× Delta-Sigma DAC
- Single +5V Operation
- Adjustable System sampling Rates including 32 kHz, 44.1 kHz and 48 kHz
- 107 dB Dynamic Range Over the Audio Bandwidth
- ±0.0002 dB Passband Ripple
- Flexible Serial Input Port
  Supports Multiple Input Formats
  16 or 18 Bit Input Words

General Description

The CS4303 is a high performance delta-sigma D/A converter for digital audio systems which require wide dynamic range. The CS4303 includes 8× interpolation and a 64× oversampled delta-sigma modulator that outputs a 1-bit signal to an external analog low pass filter. The 1's density of the 1-bit signal is proportional to the digital input.

The CS4303 has a configurable input serial port that provides four interface formats. The master clock rate can be either 256 or 384 times the input word rate, supporting various audio environments.

For more information call (512)445-7222 and ask for the Audio Databook.



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Crystal Semiconductor Corporation
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Semiconductor Corporation

CS4328

18-Bit, Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System
  - 8× Interpolation Filter
  - 64× Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- 120 dB Signal-to-Noise Ratio
- Low Clock Jitter Sensitivity
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- Flexible Serial Interface for Either 16 or 18 bit Input Data

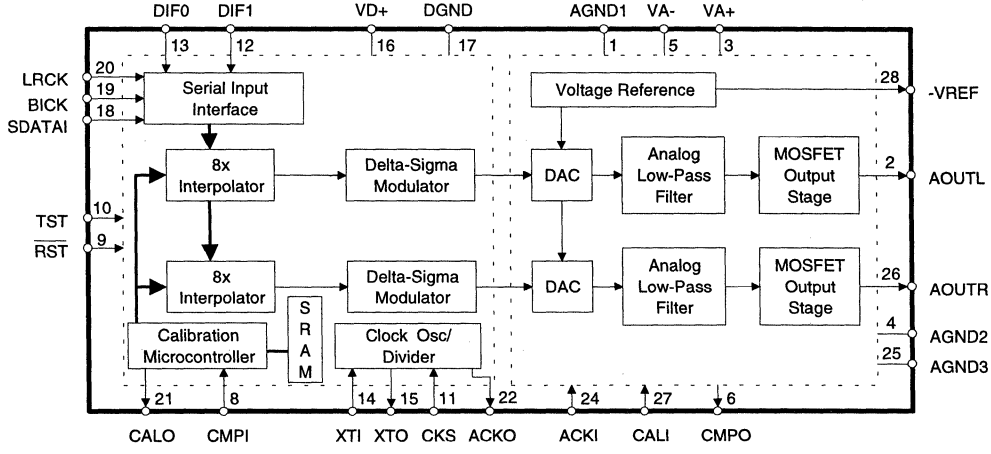
General Description

The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 256 or 384 times the input word rate, supporting various audio environments.

For more information call (512)445-7222 and ask for the Audio Databook.



Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS4330 CS4331 CS4333

8-Pin Stereo D/A Converter for Digital Audio

Features

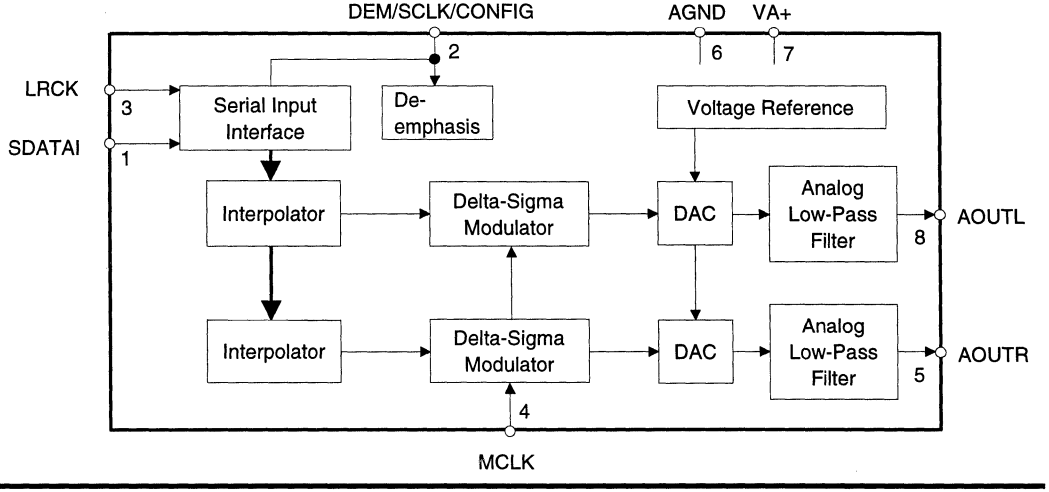
- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 18-Bit Resolution
- 96 dB Dynamic Range
- 0.003% THD
- Low Clock Jitter Sensitivity
- Single +3V or +5V Power Supply
- Completely Filtered Line Level Outputs Linear Phase Filtering
- On-Chip Digital De-emphasis

General Description

The CS4330, CS4331 and CS4333 are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. These devices differ in the serial interface format used to input audio data. The CS4330, CS4331 and CS4333 are based on delta-sigma modulation where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4330, CS4331 and CS4333 contain on-chip digital de-emphasis, operate from a single +3V or +5V power supply and consume only 50 mW of power with a 3V power supply. These features make them ideal for portable CD players and other portable playback systems.

For more information call (512)445-7222 and ask for the Audio Databook.



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CS5330 CS5331

8-Pin, Stereo A/D Converter for Digital Audio

Features

- Single +3 V or +5 V Power Supply
- 18 Bit Resolution
- 96 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  0.05dB Passband Ripple
  80dB Stopband Rejection
- Low Power Dissipation: 50 mW
  Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz

General Description

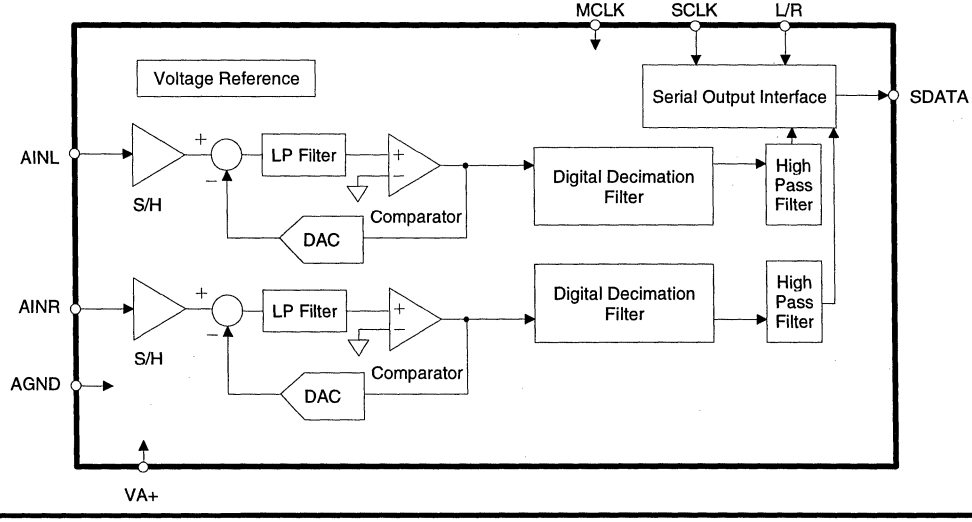
The CS5330 is a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and analog-to-digital conversion generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5330 operates from a single +3V or +5V supply and requires only 100 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 128X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband to 21.7 kHz, 0.05 dB passband ripple and >90 dB stopband rejection. The device also contains a high pass filter to remove DC offsets.

The device is available in a 0.208" wide 8-pin SOIC surface mount package.

For more information call Crystal Semicondutor at (512)445-7222



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16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion
  >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  0.01dB Passband Ripple
  80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

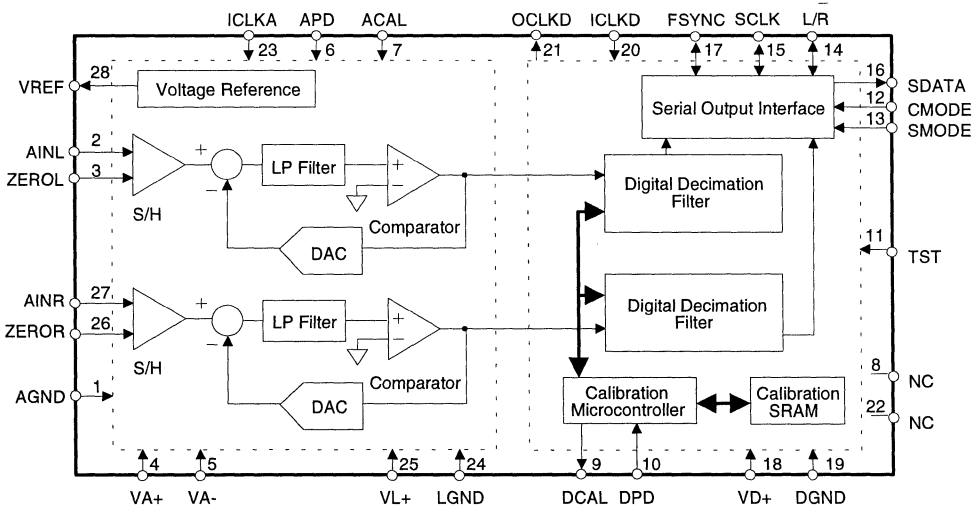
The ADCs use delta-sigma modulation with 64X over-sampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5339 has an SCLK which clocks out data on falling edges.

The CS5336 has a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package. Extended temperature range versions of the CS5336 are also available.

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS5349

Single Supply, Stereo A/D Converter for Digital Audio

Features

- Single +5 V Power Supply
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 90 dB Dynamic Range
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 300 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

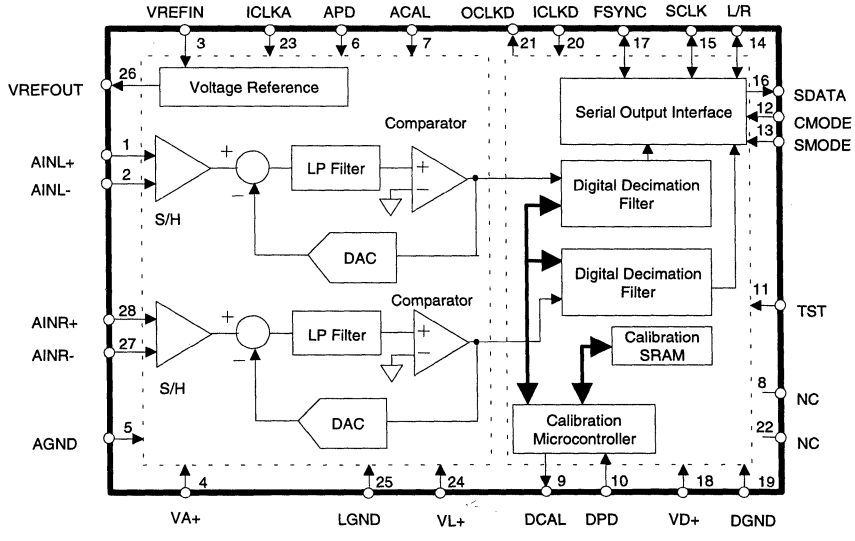
The CS5349 is a complete analog-to-digital converter which operates from a single +5V supply. It performs sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5349 has an SCLK which clocks out data on falling edges and a filter passband of dc to 24 kHz. The filter has linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The device is available housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS5389

18-Bit, Stereo A/D Converter for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 107 dB Dynamic Range (A-Weighted)
- Low Noise and Distortion
  - 100 dB THD + N
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
- Low Power Dissipation: 550 mW
  - Power-Down Mode
- Evaluation Board Available

General Description

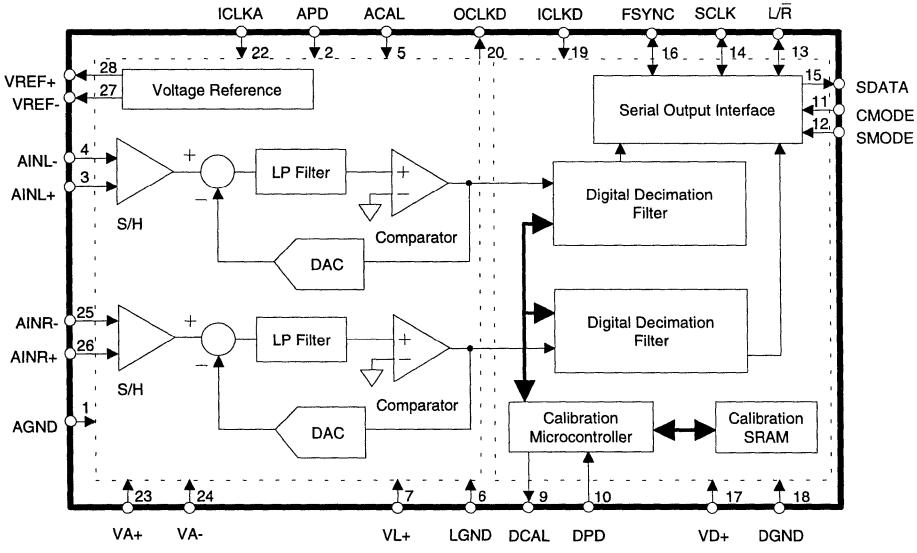
The CS5389 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5389 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5389 has a filter passband of dc to 24kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The CS5389 is targeted for the most demanding professional audio systems requiring wide dynamic range and low noise and distortion.

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS5390

20-Bit, Stereo A/D Converter for Digital Audio

Features

- 110 dB Dynamic Range (A-Weighted)
- THD + N better than -100dB
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - >100dB StopBand Attenuation
  - 0.005dB Passband Ripple
- Low Power Dissipation: 550 mW
  - Power-Down Mode
- Pin Compatible with CS5389
- Evaluation Board Available

General Description

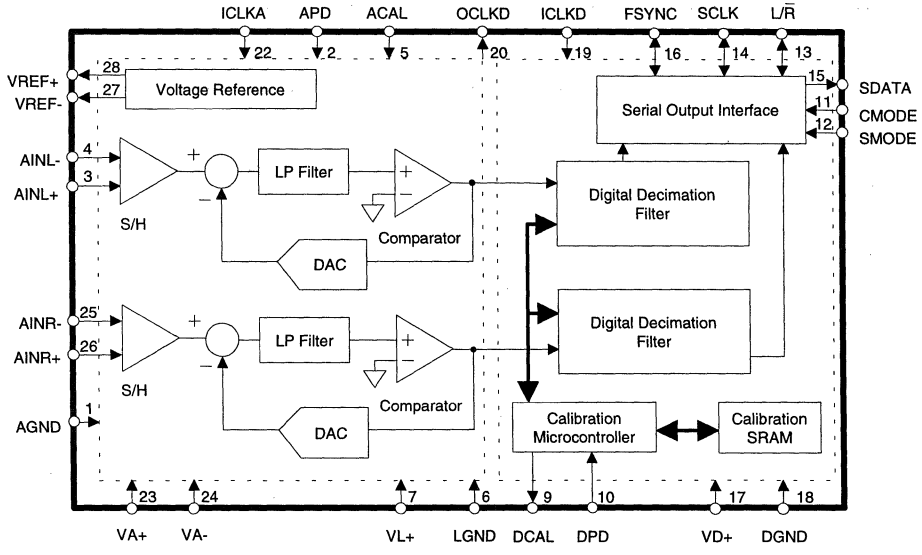
The CS5390 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5390 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5390 has a filter passband of dc to 21.7kHz. The filters have linear phase, 0.005 dB passband ripple, and >100 dB stopband rejection.

The CS5390 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise. Pin compatibility with the CS5389 allows a simple upgrade path without hardware changes.

For more information call (512)445-7222 and ask for the Audio Databook.



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CS8401A CS8402A

Digital Audio Interface Transmitter

Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401A)
- Transparent Mode Allows Direct Connection of CS8402A and CS8412 or CS8401A and CS8411A

General Description

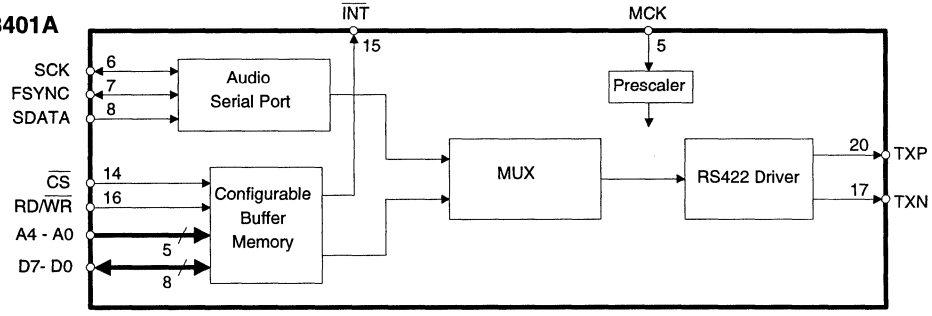
The CS8401/2A are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8401A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

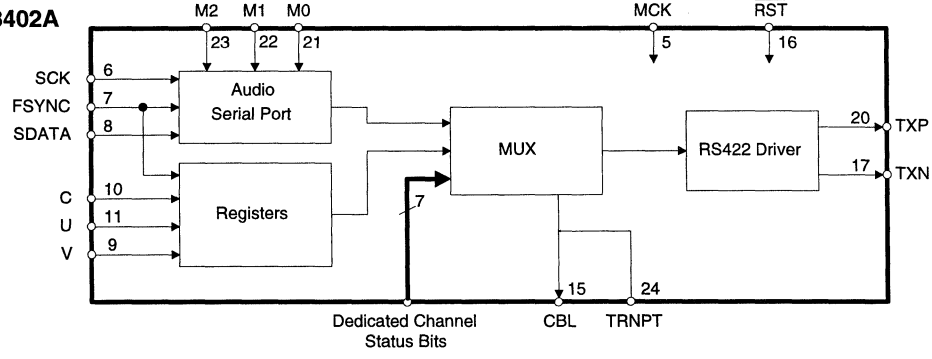
The CS8402A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

For more information call (512)445-7222 and ask for the Audio Databook.

CS8401A



CS8402A



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Semiconductor Corporation

CS8411 CS8412

Digital Audio Interface Receiver

Features

- Monolithic CMOS Receiver
- Low-Jitter, On-Chip Clock Recovery
  256×Fs Output Clock Provided
- Supports: AES/EBU, IEC 958,
  S/PDIF, & EIAJ CP-340
  Professional and Consumer Formats
- Extensive Error Reporting
  Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8411)

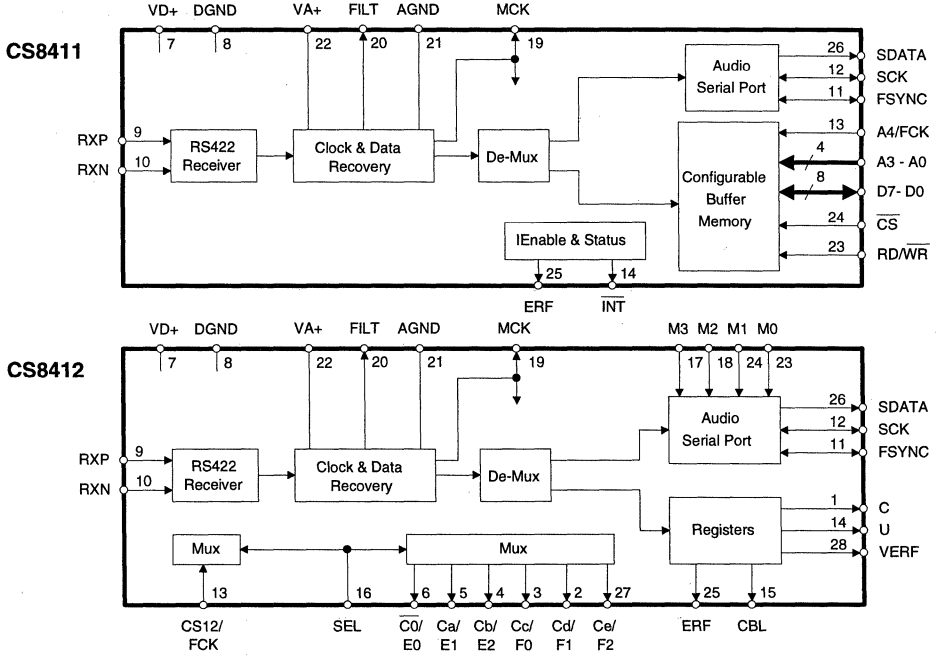
General Description:

The CS8411/12 are monolithic CMOS devices which receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8411/12 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

The CS8411 has a configurable internal buffer memory, read via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8412 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS8425

A-LAN - Audio Local Area Network Transceiver

Features

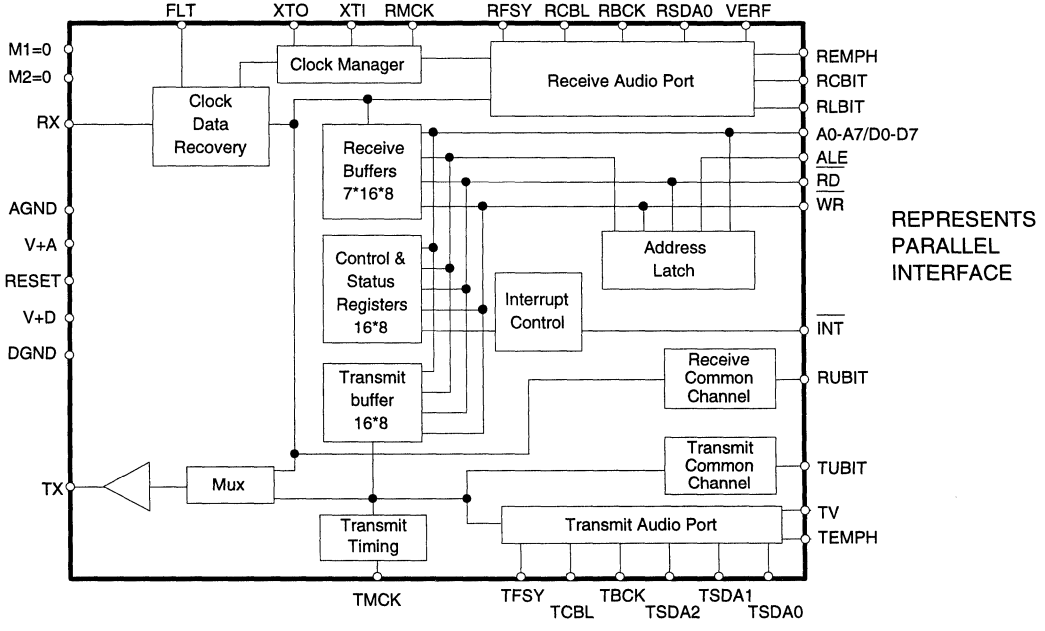
- Monolithic Digital Audio Transceiver for Point-to-Point Transmission of Audio Data
- Supports D2B OPTICAL
- User Channel Used for Communication of System Messages Between Nodes
- Configurable Interface Port Supports SPI, I²C Bus®, Parallel Interface, or the CS8425 Operates as Stand-alone Unit
- Supports Large Number of Nodes per Network
- Also Applicable as General Purpose IEC-958 Digital Audio Transceiver

General Description

The A-LAN chip is a monolithic CMOS circuit that implements the physical layer of an Audio Local Area Network. The A-LAN allows numerous pieces of audio equipment such as CD players, digital equalizers, digital tape decks, DACs, amps, etc. to be connected in a ring topology, sharing audio data from a designated source. Control and configuration messages are passed between nodes via a unique application of the user channel.

Audio data is transmitted using the format specified by IEC-958, and can be generated by any one of multiple nodes on the A-LAN. External drivers and receivers are required for interface to the transmission media.

For more information call (512)445-7222 and ask for the Audio Databook.



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• Notes •

INTRODUCTION

Using SMART Analog technology, Crystal Semiconductor has created a family of CMOS A/D Converters which feature patented on-chip, self-calibrating architectures to maintain accuracy and linearity over their full temperature range and device lifetime. Each of our A/D Converters features an on-chip sample and hold, and is manufactured in low-power CMOS. Most devices include a power-down sleep mode.

For complete data sheets on the products in this chapter, see the Crystal Semiconductor Data Acquisition Databook, or contact Crystal.

CS5012A, CS5014, CS5016 SAR Family

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution respectively, with conversion times of 7 µs to 16 µs. On-chip self-calibration ensures that linearity, offset and full-scale errors remain with specification, with no missing codes.

CS5030, CS5031, CS5032 12-bit 500kHz ADCs

The CS5030/1 feature a 1 ppm/°C on-chip reference. This yields a 12-bit ADC which has a total unadjusted error (including reference error) of <±0.5 LSB over the military temperature range. The CS5032 is a low cost version with a 60 ppm/°C reference.

CS5101A, CS5126 16-bit 100 kHz ADC

The CS5101A is a 16-bit ADC capable of converting in 8 µs, yielding sample rates of 100 kHz. A 2-channel analog input mux is included. The CS5126 is a low-cost version of the CS5101A, intended for signal processing applications.

CS5102A 16-bit 20 kHz Low Power ADC

The CS5102A is a low power version of the CS5101A. Requiring only 44 mW from ±5 V supplies, along with a 1 mW power down mode, the CS5102A is ideal for battery powered applications.

CS5317 16-bit Voice Band ADC

The CS5317 is well suited for a wide range of voiceband applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz band width, 84 dB dynamic range and 80 dB THD.

CS5321, CS5322, CS5323, CS5324, 24-bit Variable Band width ADC

The CS5323 or CS5321 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 1500 Hz frequency band. Seven different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing users to implement their own final filter stage.

CS5412 12-bit 1 MHz ADC

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at a 1 MHz sample rate. Self calibration insures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

CS5480, CS5490 10/12-bit 40/20 MHz ADC

The CS5480 is a monolithic CMOS 10-bit sampling ADC capable of 40 Msps conversion rates. The CS5490 is a 12-bit sampling ADC capable of 20 Msps conversion rates. Digital inputs are CMOS and TTL compatible, and the digital outputs are CMOS compatible. Output data is available in offset binary format.

CS5501, CS5503 16/20-bit DC Measurement ADC

The CS5501 and CS5503 feature an on-chip, 6-pole, low-pass filter, with adjustable corner frequencies from 0.1 Hz to 10 Hz. The ADC's achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications.

Specifications	CS5012A CS5014 CS5016	CS5030 CS5031 CS5032	CS5101A CS5102A CS5126	CS5317	CS5321 CS5322 CS5323 CS5324	CS5412	CS5480	CS5490	CS5501 CS5503	CS5504 CS5505 CS5506 CS5507 CS5508 CS5509	CS5516 CS5520	CS7870 CS7875
Application	GP	GP	GP	Modem	Seismic	GP Fast	High Speed		DC Measurement			GP
Resolution (bits)	12/14/16	12	16	16	24	12	10	12	16/20	16/20	16/20	12
Conversion Time (µs)	7/14/16	2	8/40	-	-	1.25	-	-	-	-	-	10
Throughput (kHz)	100/56/50	500	100/20	20	-	1 MHz	40	20	4	60/100Hz	60Hz	100
Number of Inputs	1	1	2	1	1	1	1	1	1	1/2/4	1	1
Input Bandwidth	-	-	-	10 kHz	500 Hz	4 MHz	200 MHz	200 MHz	10 Hz	10 Hz	12 Hz	-
Integral Non-Linearity	.006/.002/ .001%	.25 LSB	.0015%	-	-	.01%	1 LSB	1 LSB	.0007%	.0015%	.0007%	0.25 LSB
Differential (±LSB) Non-Linearity	0.25/0.25/ NMC	0.5	NMC	NMC	NMC	0.9	0.5	0.5	0.125/ NMC	0.125	0.5	0.5
No Missing Codes	12/14/16	12	16	16	20	12	10	12	16/20	16/18	16/20	12
Total Harmonic Distortion (%)	.008/.003/ .001	-80 dB	.001	.007	.0003	.02	-54 dB	-63 dB	-	-	-	-80 dB
Signal-to-Noise plus Distortion (dB)	73/83/92	72	92	80	-	70	-	-	-	-	-	73
Dynamic Range (dB)	73/83/92	72	92	84	120	70	62	70	-	-	-	72
Power Needed (mW)	150	50	280/44	220	150	750	375	225	25	3	30	95
Conversion Method	Succ. Approx.	Succ. Approx.	Succ. Approx.	Delta Sigma	Delta Sigma	2-Step Flash	Pipeline	Pipeline	Delta Sigma	Delta Sigma	Delta Sigma	Succ. Approx.
Power Down Mode	-	-	✓	-	✓	-	-	-	✓	✓	✓	-
On-Chip Sample and Hold	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
On-Chip V. Ref	-	✓	-	✓	-	-	✓	✓	-	✓	✓	✓
On-Chip Filtering	-	-	-	✓	✓	-	-	-	✓	✓	✓	-
Statically Tested	✓	✓	✓	-	-	✓	✓	✓	✓	✓	✓	✓
Dynamically Tested	✓	✓	✓	✓	✓	✓	✓	✓	-	-	-	✓
Temperature Range	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind Mil	Com Ind	Com Ind Mil	Ind	Ind	Com Ind Mil	Ind Mil	Ind Mil	Ind Mil
Number of Pins (DIP)	40	24	28	18	28	40	28	44	20	20/24	24	24
Packages	DIP PLCC LCC	DIP SOIC	DIP PLCC LCC	DIP SOIC	PLCC	DIP JLCC	PLCC	PLCC	DIP SOIC	DIP SOIC	DIP SOIC	DIP SOIC PLCC

NMC = No Missing Codes GP = General Purpose

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CS5504/5/6/7/8/9 1,2 & 4-channel, 16/20-bit DC Measurement ADC

Very low power consumption of 1.5 mW, along with an optional 1, 2, or 4-channel input mux, make this part ideal for process control and hand held meter applications. These ADC's are available in 16 or 20 bit versions.

CS5516, CS5520 16/20-bit Bridge Transducer ADC

The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells and pressure transducers. The devices offer an on-chip software programmable instrumentation amplifier, choice of AC or DC bridge excitation, software selectable reference and signal demodulation.

CS7870, CS7875 12-bit 100 kHz Sampling ADC

The CS7870 and CS7875 are complete monolithic CMOS ADCs providing 100 kHz throughput. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data. The CS7870 has a ±3V analog input range while the CS7875 accepts input signals from 0V to +5V.

CDBCAPTURE Data Capture and Interface Board for a PC

The CAPTURE interface board is a development tool that can be easily interface to Crystal Semiconductor Evaluation boards. Application software, developed with Lab Windows, adjusts the CAPTURE interface board for the appropriate signal timing and polarity, coding format and number of bits.

CONTENTS

16, 14 & 12-Bit, Self-Calibrating A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12, 14 and 16-Bit Precision
- Conversion Times:

CS5016	16.25 µs
CS5014	14.25 µs
CS5012A	7.2 µs

- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Low Distortion

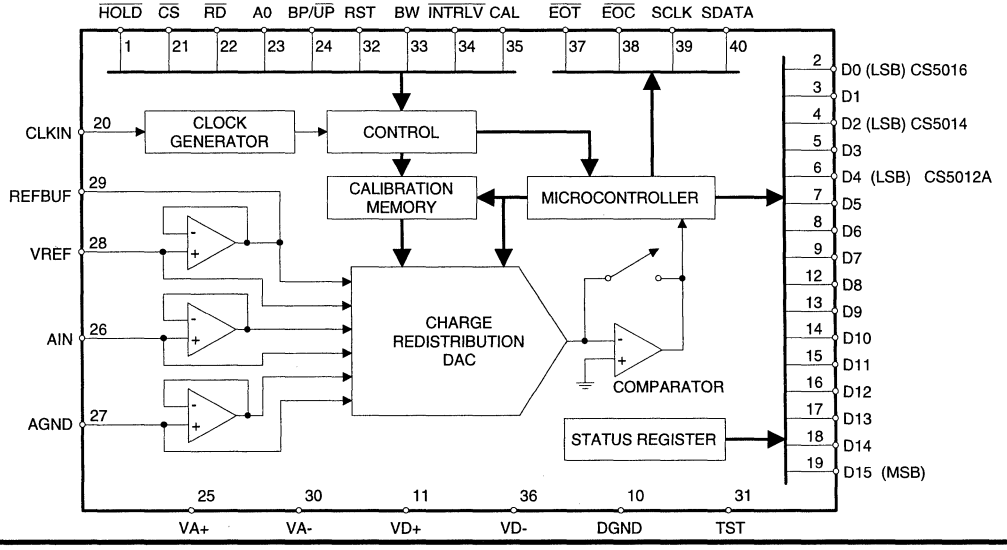
General Description

The CS5012A/14/16 are 12, 14 and 16-bit monolithic analog to digital converters with conversion times of 7.2µs, 14.25µs and 16.25µs. Unique self-calibration circuitry insures excellent linearity and differential non-linearity, with no missing codes. Offset and full scale errors are kept within 1/2 LSB (CS5012A/14) and 1 LSB (CS5016), eliminating the need for calibration. Unipolar and bipolar input ranges are digitally selectable.

The pin compatible CS5012A/14/16 consist of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the devices' sampling architecture, acquires the input signal after each conversion using a fast slewing on-chip buffer amplifier. This allows throughput rates up to 100 kHz (CS5012A), 56 kHz (CS5014) and 50 kHz (CS5016).

An evaluation board (CDB5012/14/16) is available which allows fast evaluation of ADC performance.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



9

Semiconductor Corporation

CS5030 CS5031

12-Bit, 400 kHz, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 0.5µs Track/Hold Amplifier
  - 2µs A/D Converter
  - 2.5V Voltage Reference
  - Flexible Parallel, Serial and Byte interface
- 12-Bit ADC and Reference Accuracy
  - Total Unadjusted Error: ±1/2 LSB
  - Ref Tempco: 1ppm/°C
- Low Distortion
  - Signal-to-Noise Ratio: 72 dB
  - Total Harmonic Distortion: 0.01%
  - Peak Harmonic or Noise: 0.01%
- Low Power: 50mW

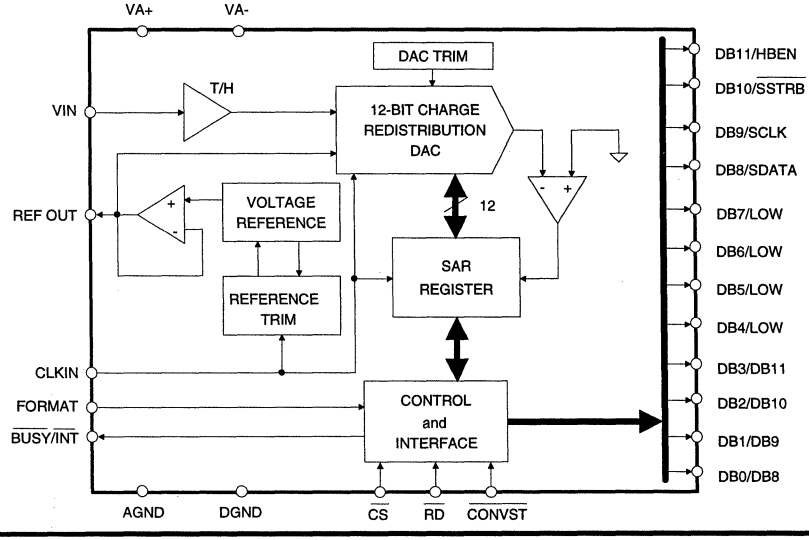
General Description

The CS5030, and CS5031 are complete monolithic CMOS analog-to-digital converters capable of 400 kHz throughput. On-chip calibration circuitry achieves true 12-bit accuracy for the ADC and on-chip reference over the full operating temperature range without external adjustments.

The CS5030/CS5031 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS5030/CS5031 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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CRYSTAL
Semiconductor Corporation

CS5032

12-Bit, 500 kHz, Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - 0.5µs Track/Hold Amplifier
  - 2µs A/D Converter
  - 2.5V Voltage Reference
  - Flexible Parallel, Serial and Byte Interface.
- 12-Bit ADC Linearity Error: ±1/2 LSB
- Low Distortion
  - Signal-to-Noise Ratio: 72 dB
  - Total Harmonic Distortion: 0.01%
  - Peak Harmonic or Noise: 0.01%
- Low Power: 50mW

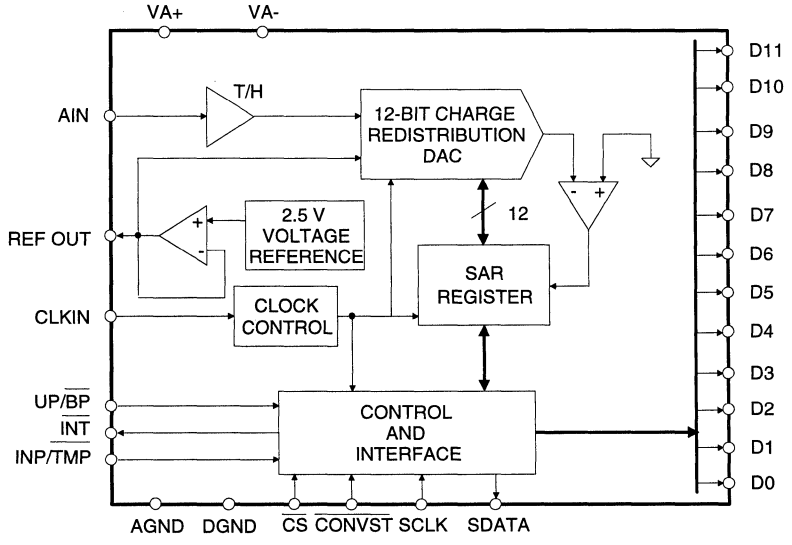
General Description

The CS5032 is a complete monolithic CMOS analog-to-digital converter capable of 500 kHz throughput. The part has an internal sample and hold, voltage reference and can operate with an internal or external clock.

The CS5032 has a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, 8 + 4 byte or serial formats.

The CS5032 is available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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CRYSTAL
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CS5101A
CS5102A

16-Bit, 100 kHz/20 kHz A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 92 dB
  - THD: 0.001%
- Conversion Time
  - CS5101A: 8 µs
  - CS5102A: 40 µs
- Linearity Error: ± 0.001% FS
  - Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption
  - CS5101A: 320 mW
  - CS5102A: 44 mW
  - Power-down Mode: < 1 mW
- Evaluation Board Available

General Description

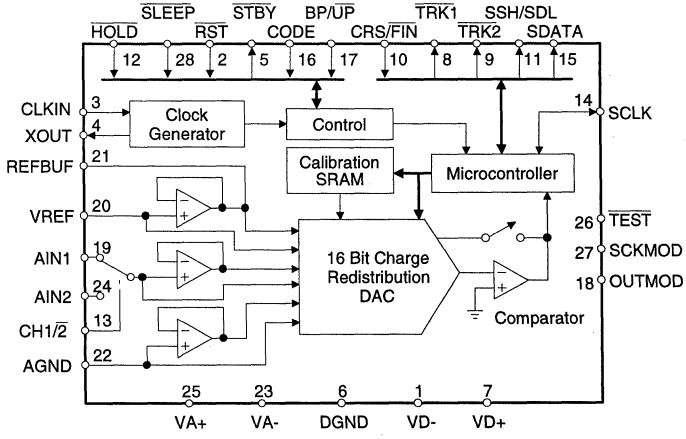
The CS5101A and CS5102A are 16-bit monolithic CMOS analog-to-digital converters capable of 100 kHz (5101A) and 20 kHz (5102A) throughput. The CS5102A's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The CS5101A and CS5102A each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

The converters' 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5317

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

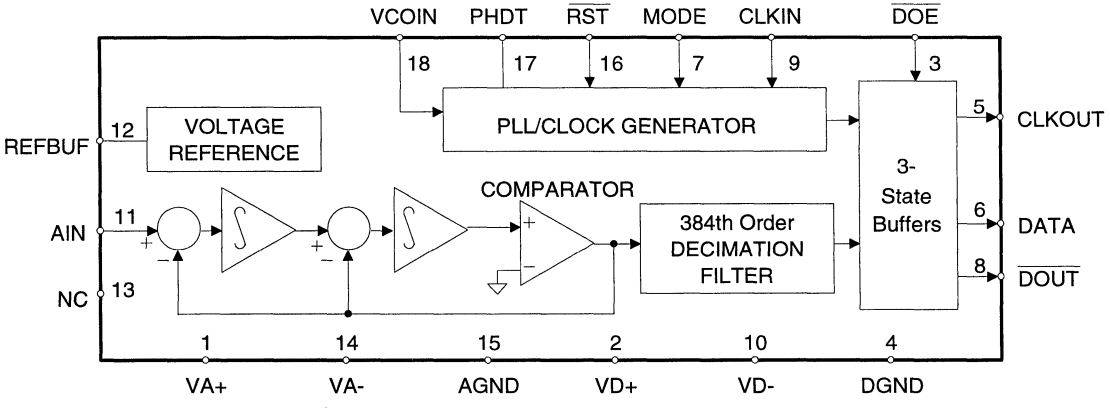
The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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CRYSTAL
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CS5321

High Dynamic Range Delta-Sigma Modulator

FEATURES

- Delta-Sigma Architecture
  - Fourth-Order Modulator
  - Variable Sample Rate
  - Internal Track-and-Hold Amplifier
- Clock Jitter Tolerant Architecture
- Dynamic Range
  - 121 dB @ 411 Hz Bandwidth
  - 118 dB @ 822 Hz Bandwidth
- Signal-to-Distortion: 115 dB
- Input Range: ± 4.5V
- Improved offset drift, gain drift, and clock jitter immunity over CS5323

DESCRIPTION

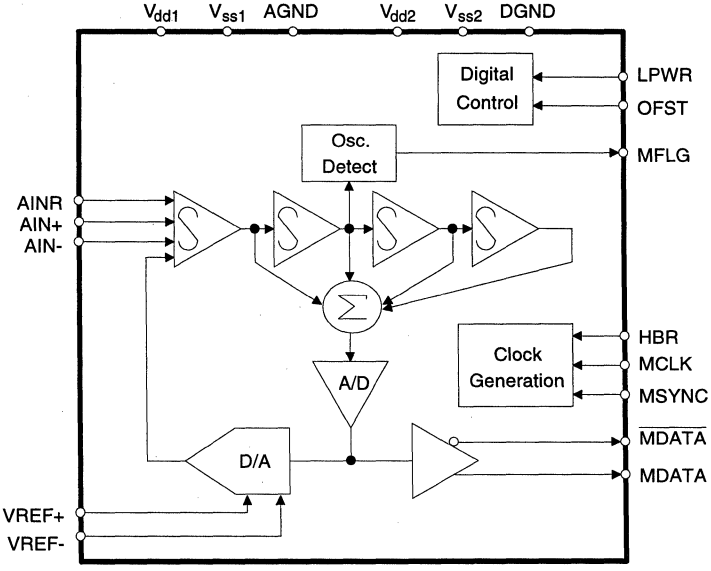
The CS5321 is a high dynamic range, fourth-order delta-sigma modulator intended for geophysical and sonar applications. Used in combination with the CS5322 digital FIR filter, a unique high resolution A/D system results.

The CS5321 provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz.

The monolithic CMOS design of the CS5321 insures high reliability while minimizing power dissipation.

The CS5321 can be operated in two power modes. In Normal mode (LPWR=0) power dissipation is 55 mW. In Low Power mode (LPWR=1) power dissipation is 30 mW.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5322/CS5323

24-Bit Variable Bandwidth A/D Converter

Features

- Monolithic CMOS A/D Converter
- Dynamic Range
  - 130dB @ 25 Hz Bandwidth
  - 120dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corner (-3dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: < 100mW

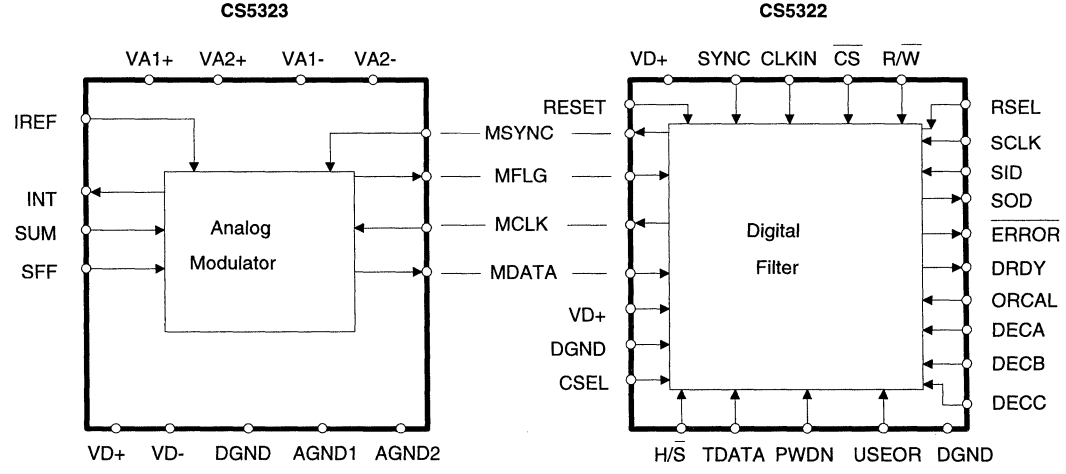
General Description

The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - —256X Oversampling
  - —Linear Phase Digital Filter
  - —Output Word Rate 32 kHz
- Low Power Dissipation: 150 mW
- Evaluation Board Available

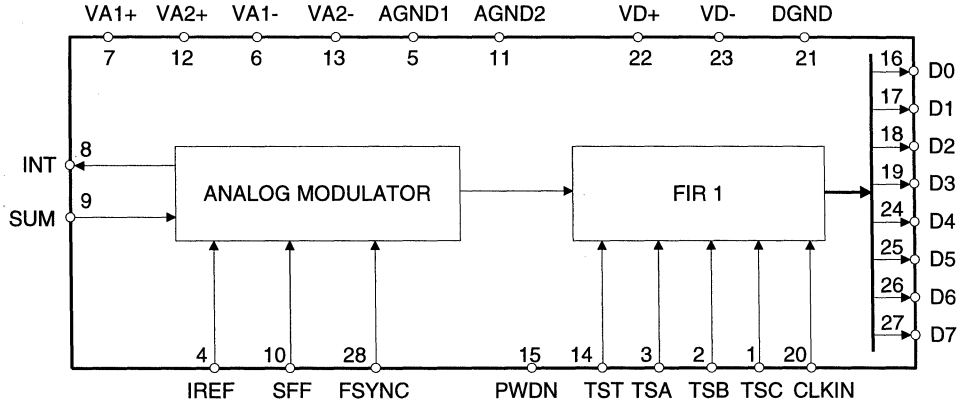
General Description

The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5412

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Typical Nonlinearity: 3/4 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

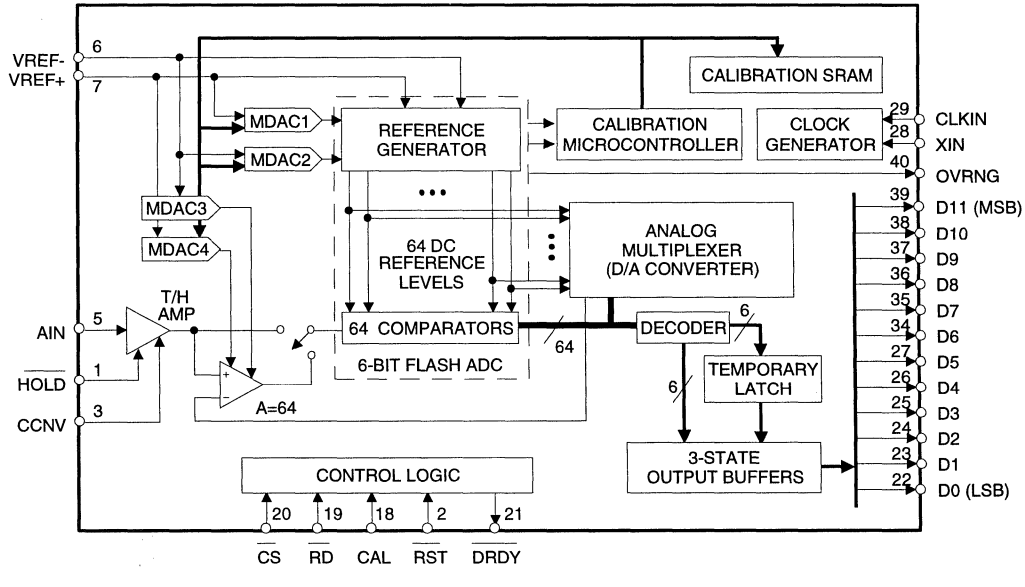
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acqusition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

For more information call (512)445-7222 and ask for the Data Acqusition Databook.



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Semiconductor Corporation

CS5480

10-Bit, 40 MHz A/D Converter

Features

- Monolithic CMOS ADC
  Sample Rate: 40 MSPS
  On-chip Track/Hold

- Signal-to-Noise Ratio:
  f_{in}= 1 MHz: 58 dB
  f_{in}= 10 MHz: 54 dB
  f_{in}= 20 MHz: 50 dB

- Analog Input Range:
  Single-ended Input: $1.2V_{p-p}$
  Differential Input: $2.4V_{p-p}$

- Low Power: 375 mW

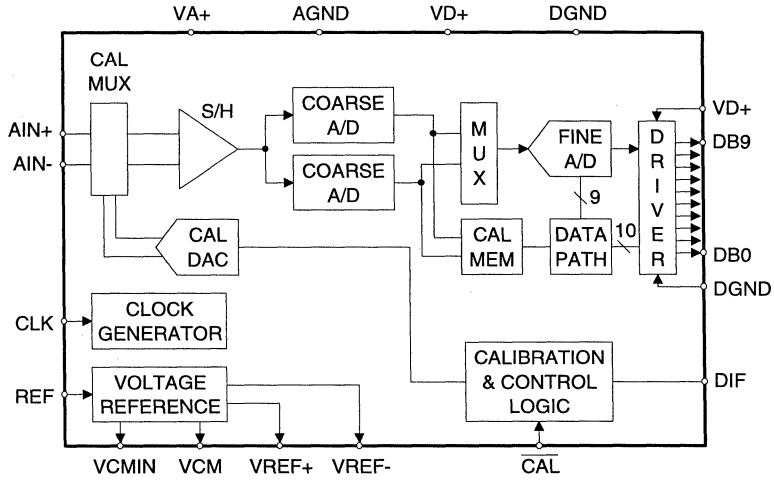
General Description

The CS5480 is a monolithic 10-bit sampling analog-to-digital converter capable of 40 MSPS conversion rate. To achieve high throughput, the CS5480 uses a fully pipelined architecture. Unique self-calibration circuitry insures excellent linearity with no missing codes over the entrire operating temperature range.

Digital inputs are CMOS and TTL compatible and the outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5480 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



Product Preview

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Semiconductor Corporation

CS5490

12-Bit, 20 MHz A/D Converter

Features

- Monolithic CMOS ADC
  Sample Rate: 40 MSPS
  On-chip Track/Hold
- Signal-to-Noise Ratio:
  f_{in}= 1 MHz: 62 dB
  f_{in}= 10 MHz: 58 dB
- Analog Input Range:
  Single-ended Input: $1.2V_{p-p}$
  Differential Input: $2.4V_{p-p}$
- Low Power: 225 mW

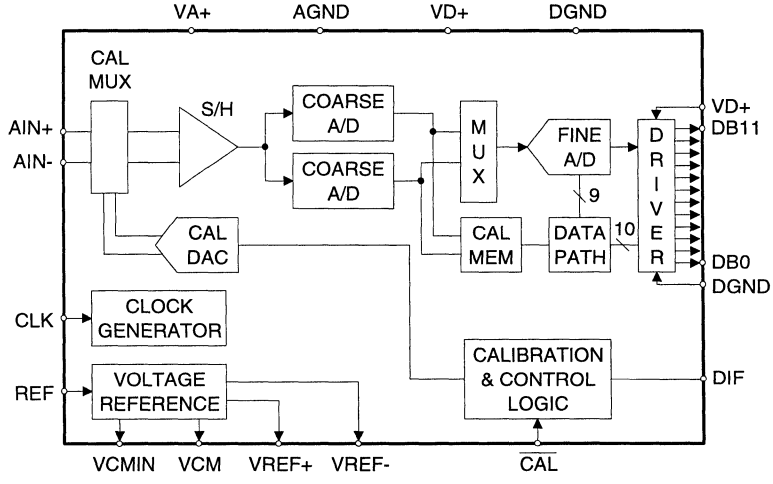
General Description

The CS5490 is a monolithic 12-bit sampling analog-to-digital converter capable of 20 MSPS conversion rate. To achieve high throughput, the CS5490 uses a fully pipelined architecture. Unique self-calibration circuitry insures excellent linearity with no missing codes over the entrire operating temperature range.

Digital inputs are CMOS and TTL compatible and the outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5490 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Product Preview

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Semiconductor Corporation

CS5501
CS5503

Low-Cost, 16 & 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering 6-Pole, Low-Pass Gaussian Filter
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  - Linearity Error: ±0.0003%
  - Differential Nonlinearity:
    CS5501: 16-Bit No Missing Codes (DNL ±1/8LSB)
    CS5503: 20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  - µC-Compatible Formats
  - 3-State Data and Clock Outputs
  - UART Format (CS5501 only)
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  - 10µW Sleep Mode for Portable Applications
- Evaluation Boards Available

General Description

The CS5501 and CS5503 are low-cost CMOS A/D converters ideal for measuring low-frequency signals representing physical, chemical, and biological processes. They utilize charge-balance techniques to achieve 16-bit (CS5501) and 20-bit (CS5503) performance with up to 4kHz word rates at very low cost.

The converters continuously sample at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The converters' low-pass, 6-pole Gaussian response filter is designed to allow corner frequency settings from .1Hz to 10Hz in the CS5501 and .5Hz to 10Hz in the CS5503. Thus, each converter rejects 50Hz and 60Hz line frequencies as well as any noise at spurious frequencies.

The CS5501 and CS5503 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB for the CS5501 and less than 4LSB for the CS5503. The devices can also be applied in system calibration schemes to null offset and gain errors in the input channel.

Each device's serial port offers two general purpose modes of operation for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. In addition, the CS5501's serial port offers a third, UART-compatible mode of asynchronous communication.

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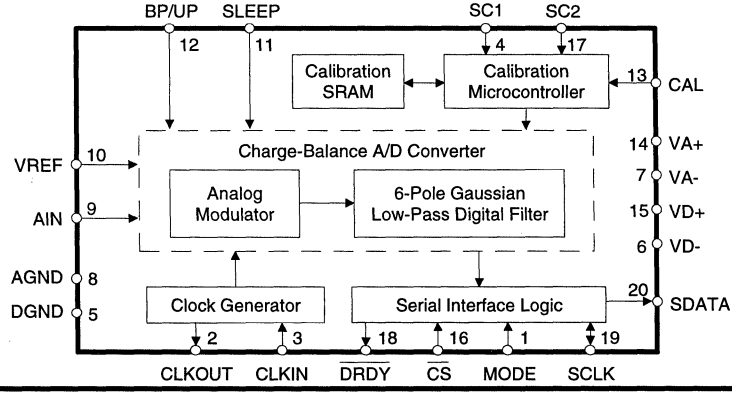

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Semiconductor Corporation

CS5504

Low Power, 20-Bit A/D Converter

Features

- Delta-Sigma A/D Converter
  - 20-bit No Missing Codes
  - Linearity Error: ±0.0015%FS
- 2 Differential Inputs
  - Pin Selectable Unipolar/Bipolar Ranges
  - Common Mode Rejection
    - 105 dB @ dc
    - 120 dB @ 50, 60 Hz
- On-chip Self-Calibration Circuitry
- Output Update Rates up to 200/second
- Low Power Consumption: 4 mW

General Description

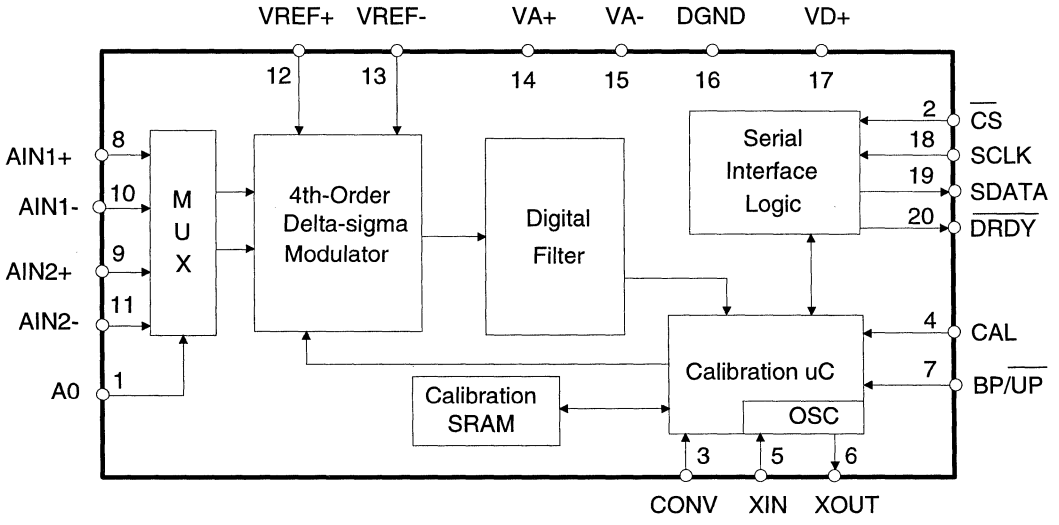
The CS5504 is a 2-channel, fully differential 20-bit, serial-output CMOS A/D converter. The CS5504 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 200 samples per second.

The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5504 has on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5504 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery-powered instruments.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5505	CS5506
CS5507	CS5508

Very Low Power, 16-Bit and 20-Bit A/D Converters

Features

- Very Low Power Consumption
  Single supply +5V operation: 1.5 mW
  Dual supply ±5V operation: 3.0 mW
- Offers superior performance to VFCs and multi-slope integrating ADCs
- Differential Inputs
  Single Channel and Four-Channel pseudo-differential versions
- On Chip Self-Calibration Circuitry
- Linearity Error: ±0.0015% FS
- Output update rates up to 100/second
- Flexible Serial Port
- Pin-Selectable Unipolar/Bipolar Ranges

General Description

The CS5505/6/7/8 are a family of low power CMOS A/D converters which are ideal for measuring low-frequency signals representing physical, chemical, and biological processes.

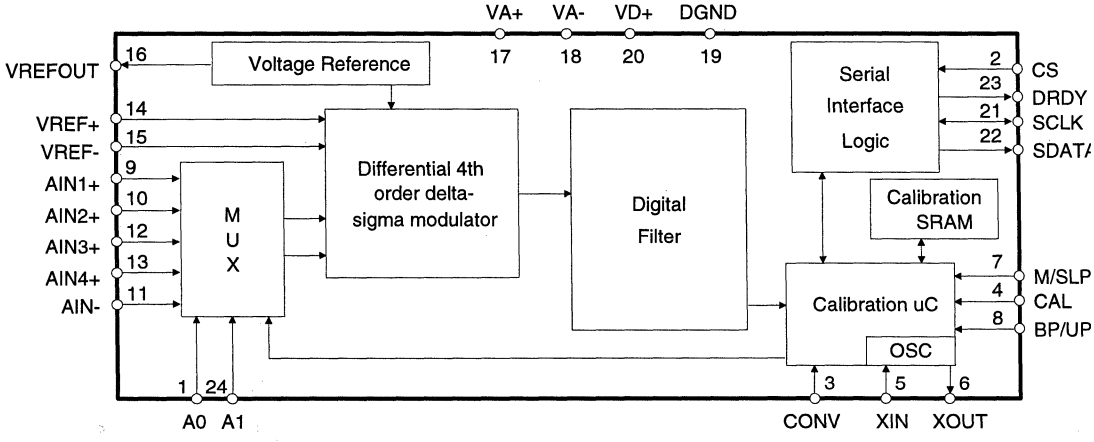
The CS5507/8 have single-channel differential analog and reference inputs while the CS5505/6 have four pseudo-differential analog input channels. The CS5505/7 have a 16-bit output word. The CS5506/8 have a 20-bit output word. The CS5505/7 sample upon command up to 100 output updates per second. The CS5506/8 sample up to 60 updates per second.

The on chip digital filter offers superior line rejection at 50 and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5505/6/7/8 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

The CS5505/6/7/8 serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS5509

Single Supply, 16-Bit A/D Converter

Features

- Delta-Sigma A/D Converter
  - 16-bit No Missing Codes
  - Linearity Error: ±0.0015%FS
- Differential Input
  - Pin Selectable Unipolar/Bipolar Ranges
  - Common Mode Rejection
    - 105 dB @ dc
    - 120 dB @ 50, 60 Hz
- On-chip Self-Calibration Circuitry
- Output Update Rates up to 200/second
- Ultra Low Power: 1.5 mW

General Description

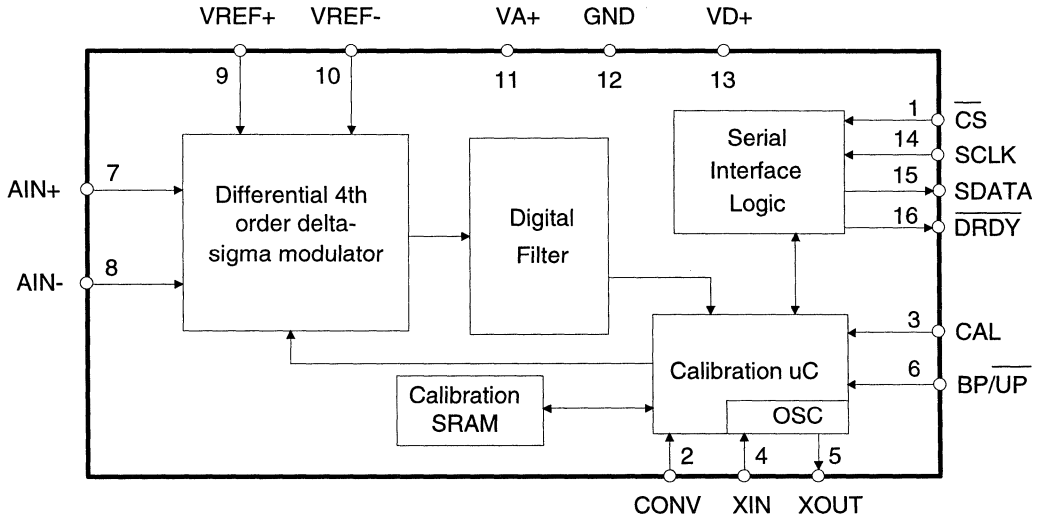
The CS5509 is a single supply, 16-bit, serial-output CMOS A/D converter. The CS5509 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 200 samples per second.

The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate=20 Hz.).

The CS5509 has on-chip self-calibration circuitry which can be initiated at any time or temperature to insure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5509 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery powered instruments.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CS5516
CS5520

16-Bit/20-Bit Bridge Transducer A/D Converters

Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error: ±0.0015% FS Max 20-Bit No Missing Codes
- CMRR at 50 / 60Hz >200dB
- System Calibration Capability with calibration read/write option
- 3, 4 or 5 wire Serial Communications Port
- Low Power Consumption: under 40mW 10µW Standby Mode for Portable applications

General Description

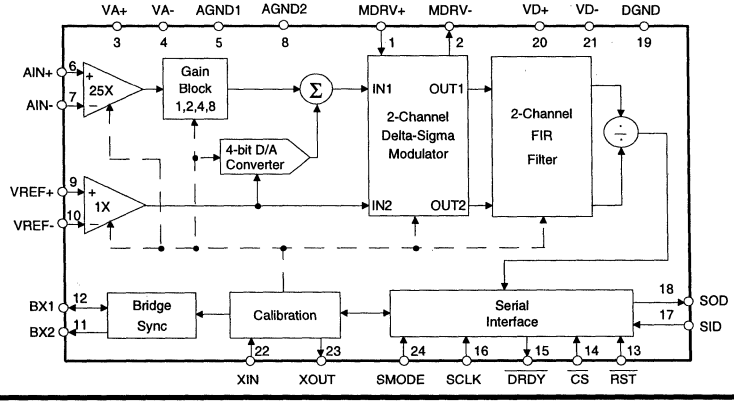
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60Hz. The CS5520 achieves 20-bit resolution at word rates up to 60Hz.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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CRYSTAL
Semiconductor Corporation

CS7870 CS7875

12-Bit, 100 kHz, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 2µs Track/Hold Amplifier
  - 8µs A/D Converter
  - 3V Voltage Reference
  - Internal Clock
  - Parallel, Serial and Byte Outputs
- 12-Bit ADC and Reference Accuracy
  - Linearity: ±1/2 LSB
  - SNR: 72 dB
- Input Ranges
  - ±3V for CS7870
  - 0 to +5V for CS7875
- Low Power: 55mW

General Description

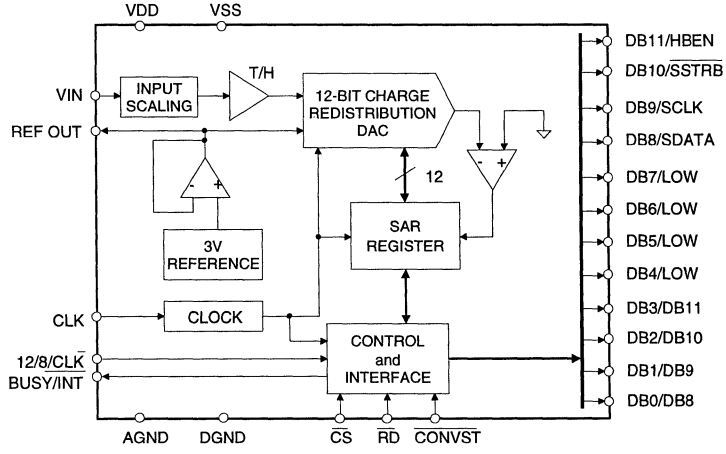
The CS7870 and CS7875 are complete monolithic CMOS analog-to-digital converters providing 100 kHz throughput. The capacitive DAC has been calibrated at the factory to ensure 12-bit performance.

The CS7870/CS7875 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS7870/CS7875 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP) or Cerdip. The CS7870 and CS7875 are also available in a 28-pin PLCC package.

The CS7870/CS7875 are pin compatible replacements for the AD7870/7875 with equal or better performance.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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Semiconductor Corporation

CDBCAPTURE

Data Capture and Interface Board for a PC

Features

- Measurement Tool used for the evaluation of Crystal Semiconductor Analog to Digital Converters.
- Easy interface to a PC Compatible computer.
- LabWindows® evaluation software for data analysis.
- Includes time domain, FFT and noise distribution histograms.
- Can be used to evaluate the ADC in your equipment.

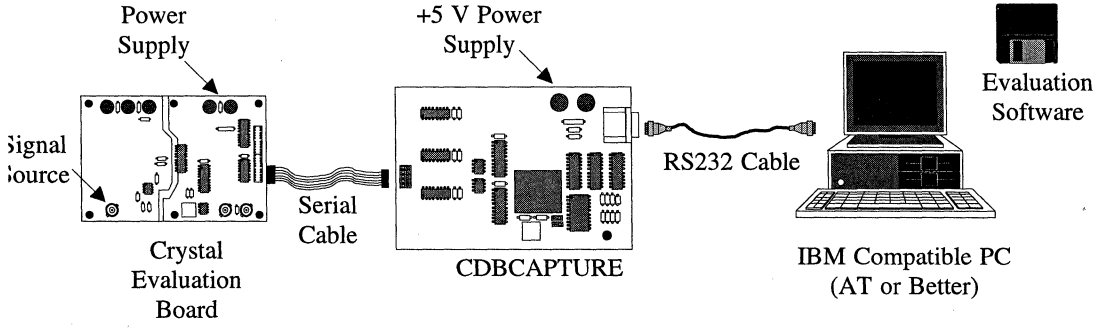
General Description

The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor analog to digital converter to a PC compatible computer. Digital data is collected in a high speed digital FIFO, then transferred to the PC over a serial COM port. Evaluation software is included to analyze the data and demonstrate the analog to digital converter's performance.

The CAPTURE interface board is designed to be easily interfaced to Crystal Semiconductor Evaluation boards. Application software is loaded via the PC's serial COM port. The software adjusts the CAPTURE interface board for the appropriate signal timing and polarity, coding format and number of bits, thus allowing the same hardware to be used with a variety of Crystal Semiconductor ADCs.

Evaluation software is included with the CAPTURE interface board. The software is developed with LabWindows, a software development system for instrument control, data acquisition, and analysis applications. The evaluation software permits time domain, frequency domain and histogram analysis.

For more information call (512)445-7222 and ask for the Data Acquisition Databook.



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INTRODUCTION

CS4215 Serial Interface Audio Codec

The CS4215 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is a microphone preamplifier, stereo headphone driver, crystal oscillators and a mono monitoring output. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4216 Serial Interface Audio Codec

The CS4216 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4231 and CS4231A PC ISA Bus Multimedia Audio Codec

The CS4231 and CS4231A are single chips with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is ADPCM compression and decompression, MPC compatible mixer, timer register for audio/visual synchronization and 16 samples deep FIFOs for record and playback. The devices require only a +5V supply, and have a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

CS4248 PC ISA Bus Multimedia Audio Codec

The CS4248 is a single chip with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

Software

To support the multimedia codec family, a wide range of software is available. Windows and NT drivers are available for the CS4231 and CS4248 multimedia codecs. A comprehensive diagnostics package assists in the debug of boards. In addition, voice recognition and text-to-speech synthesis software demonstrates some of the capabilities of an audio equipped PC.

CS4920 Multi-Standard Audio Decoder/DAC

The CS4920 combines a 16.5MIPS DSP with a stereo 16-bit Digital to Analog converter. In addition, a decompressed linear PCM coded digital output is available in industry standard S/PDIF format. An on-chip PLL allows very flexible clocking. DSP code for MPEG Layers 1 and 2, and Dolby AC2 decompression algorithms is provided. Targetted at TV set top audio decoder applications, this device is useful in any application where low-cost audio decompression is required.

CS8905 and CS9203 Audio Wave Table Synthesizers

The CS9203 is a wave table synthesizer which uses a set of sampled real sounds, stored in a ROM, to construct very realistic musical sounds. When teamed with a 8051 type microcontroller, a General Midi compliant synthesizer may be easily realized. Crystal can supply the CS9203, the wave table ROM information and code for the microcontroller.

The CS8905 is a programmable effects DSP which may be used to add various sound effects to the output of the CS9203 wave table synthesizer.

CONTENTS

Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

General Description

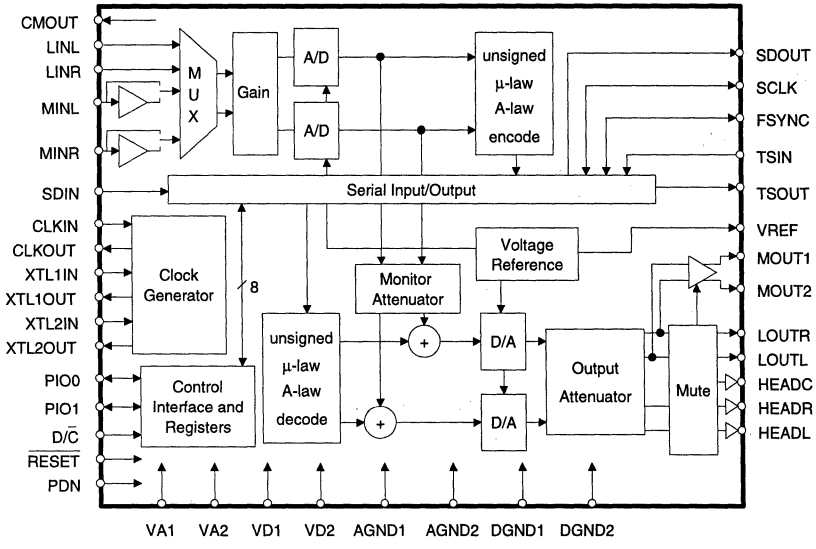
The CS4215 is an Mwave™ audio codec.

The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64×oversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

For more information call (512)445-7222 and ask for the Audio Databook.



This data sheet was written for Revision E CS4215 codecs and later. For differences between Revision E and previous versions, see *Appendix A.*

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CS4216

16-Bit Stereo Audio Codec

Features

- CMOS Stereo Audio Input/Output System
  - Delta-Sigma A/D Converters
  - Delta-Sigma D/A Converters
  - Input Anti-Aliasing and Output Smoothing Filters
  - Programmable Input Gain and Output Attenuation
- Sample Frequencies of 4 kHz to 50 kHz
- CD Quality Noise and Distortion < 0.01 %THD
- Internal 64X Oversampling
- Low Power Dissipation: 80 mA
  1 mA Power-Down Mode

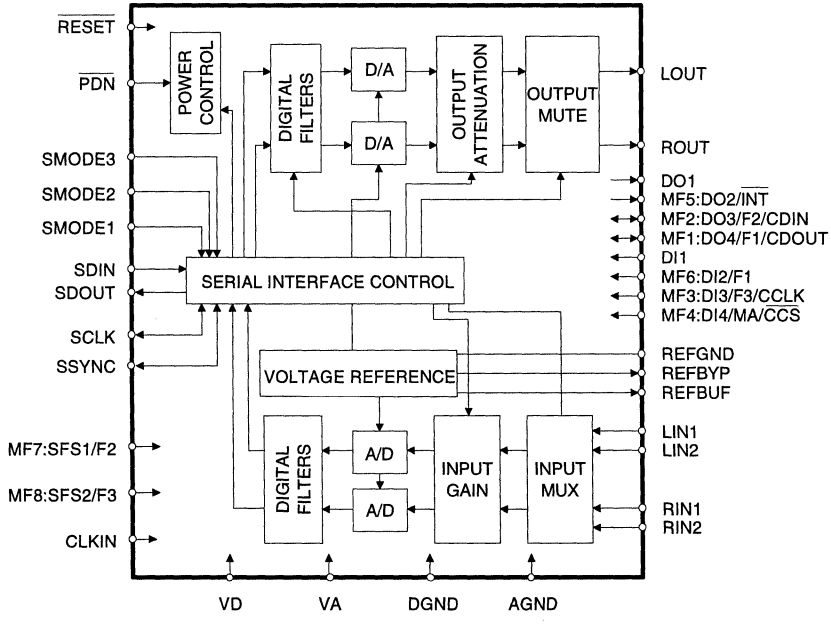
General Description

mwave The CS4216 is an Mwave™ audio codec.

The CS4216 Stereo Audio Codec is a monolithic CMOS device for computer multimedia, automotive, and portable audio applications. It performs A/D and D/A conversion, filtering, and level setting, creating 4 audio inputs and 2 audio outputs for a digital computer system. The digital interfaces of left and right channels are multiplexed into a single serial data bus with word rates up to 50 kHz per channel. Up to 4 CS4216 devices can be attached to a single hardware bus.

Both the ADCs and the DACs use delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter which eliminates the need for external anti-aliasing filters. The DACs include output smoothing filters on-chip.

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS4231

Parallel Interface, Multimedia Audio Codec

Features

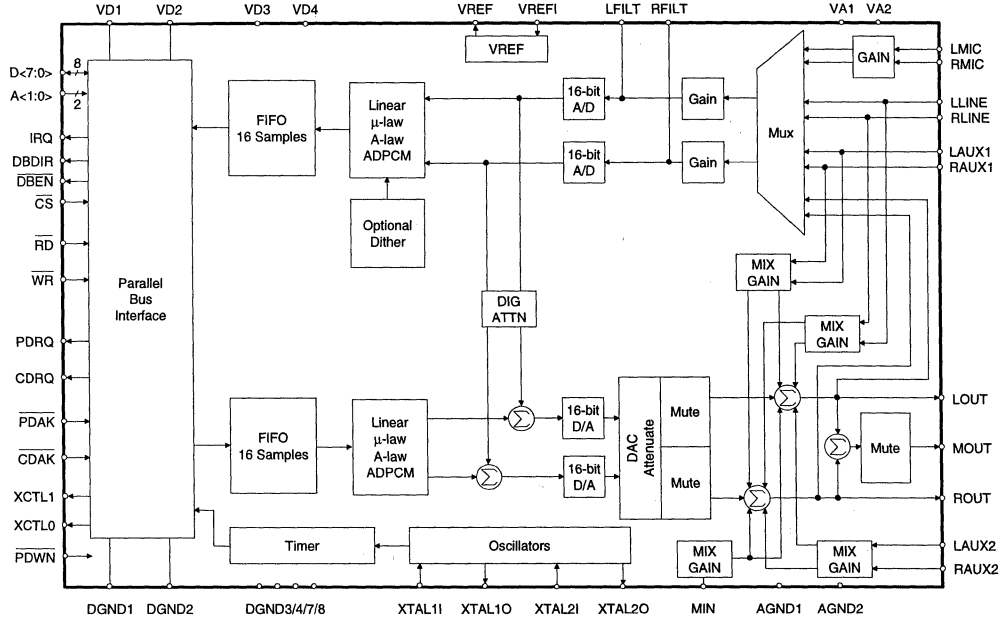
- ADPCM Compression/Decompression
- Free Windows™ Software Drivers
- MPC Compatible Mixer
- Dual DMA Count Registers for Full Duplex Operation
- DMA Transfers with On-chip FIFOs.
- Timer for Audio/Visual Synchronization
- 16 mA Bus Drive Capability
- Digital 3.3/5V Operation
- Pin Compatible with CS4248/AD1848

General Description

mwave The CS4231 is an Mwave™ audio codec.

The CS4231 provides 16-bit audio for computer multimedia systems. The CS4231 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data, plus analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. Free high-performance Windows software drivers are available that support all the CS4231 features including full duplex transfers. The CS4231 is a pin compatible upgrade to the CS4248 and AD1848 (PLCC Version).

For more information call (512)445-7222 and ask for the Audio Databook.



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Semiconductor Corporation

CS4231A

Parallel Interface, Multimedia Audio Codec

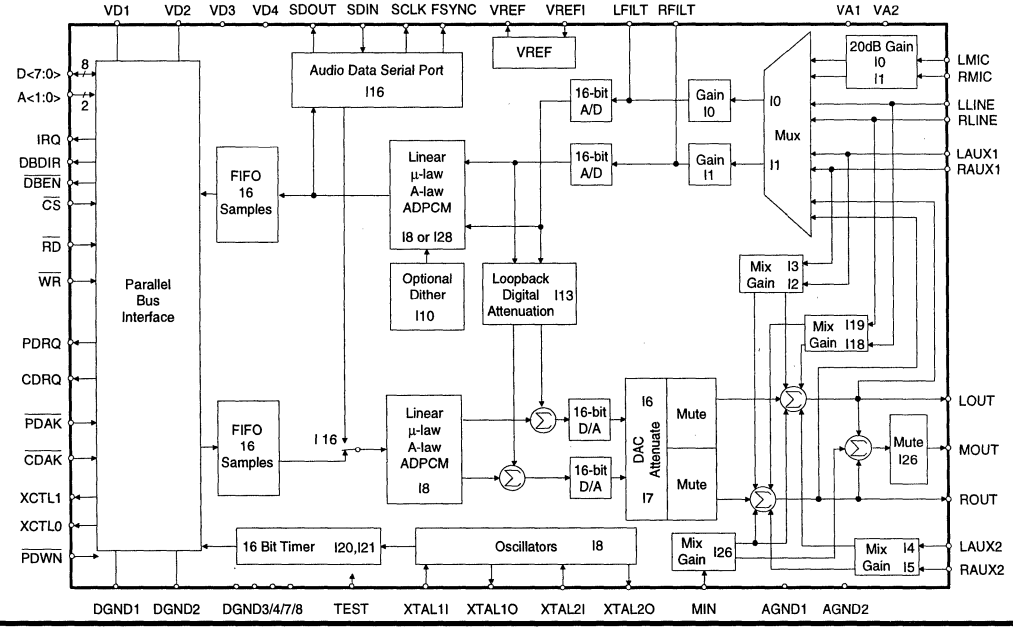
Features

- Windows Sound System™ Compatible Codec
- ADPCM Compression/Decompression
- Extensive Software Support
- MPC Level 2 Compatible Mixer
- Dual DMA Registers support Full Duplex Operation
- On-Chip FIFOs for higher performance
- Selectable Serial Audio Data Port
- Pin Compatible with CS4231/CS4248

General Description

The CS4231A includes stereo 16-bit audio converters and complete on-chip filtering for record and playback of 16-bit audio data. In addition, analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. A selectable serial port can pass audio data to and from DSPs or ASICs. High-performance software drivers for various operating systems are available that support all the CS4231A features including full duplex transfers. The CS4231A is a pin compatible upgrade to the CS4231 and CS4248.

For more information call Crystal Semicondutor at (512)445-7222



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Semiconductor Corporation

CRD4231

CRD4231 16-bit Audio Adapter Reference Design

Features

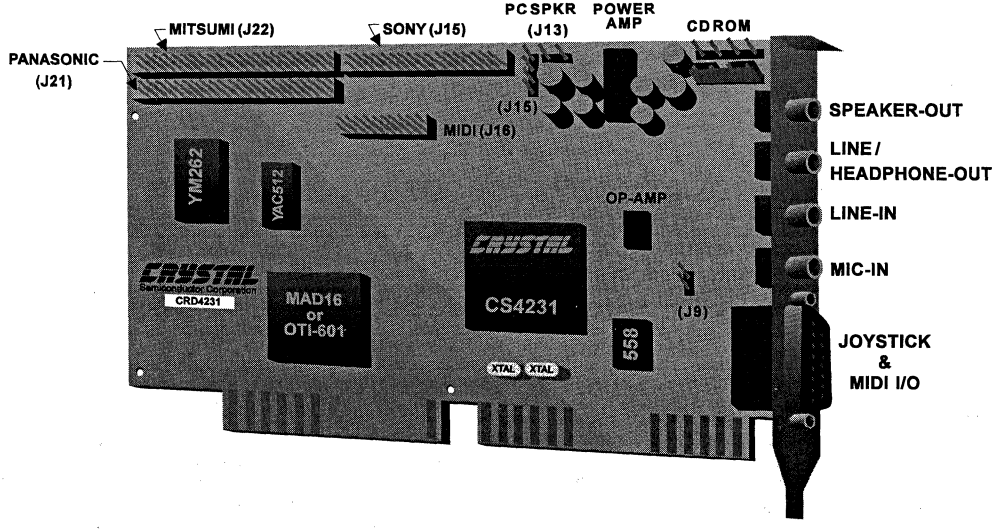
- MPC2 compliant (with enhancements), Windows Sound System™, DOS Games* and AdLib™ compatible
- 16-bit, 48kHz audio capture/playback
- WaveBlaster™ compatible MIDI interface & external Joystick/MIDI Interface
- Microphone and Line Level Inputs, Mono In / Mono Out Support, Line Out / Headphone Driver
- Multiple CD-ROM connectors: Sony, Panasonic & Mitsumi

General Description

The CD-quality CRD4231 reference design is fully MPC2 compliant, Ad Lib, DOS Games* and Windows Sound System compatible. The design is a half size ISA-bus PC adapter board, based on the CS4231 Multimedia Audio Codec, OPTi/Media Chip's 82C928/MAD16 or Oak Technologies' OTI-601, and Yamaha's YM262 FM based music synthesizer (OPL3). Optionally the CRD9203 Wavetable Music Synthesizer Daughtercard may be installed on the design. The CRD4231 supports Sony, Panasonic, and Mitsumi CD-ROM drives. Maximum SMT and DFM was used throughout.

The manufacturing kit includes: complete schematics and board layouts; bill of materials with supplier list; user's and technical manuals; DOS software support; Windows 3.1 & NT driver object code (supports all MPC2 & WSS 2.0 functions); Windows 3.1/NT volume & mixing control, waveform capture/playback; MIDI drivers; and CD-ROM drivers.

For more information call Crystal Semicondutor at (512)445-7222



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Semiconductor Corporation

CS4248

Parallel Interface, Multimedia Audio Codec

Features

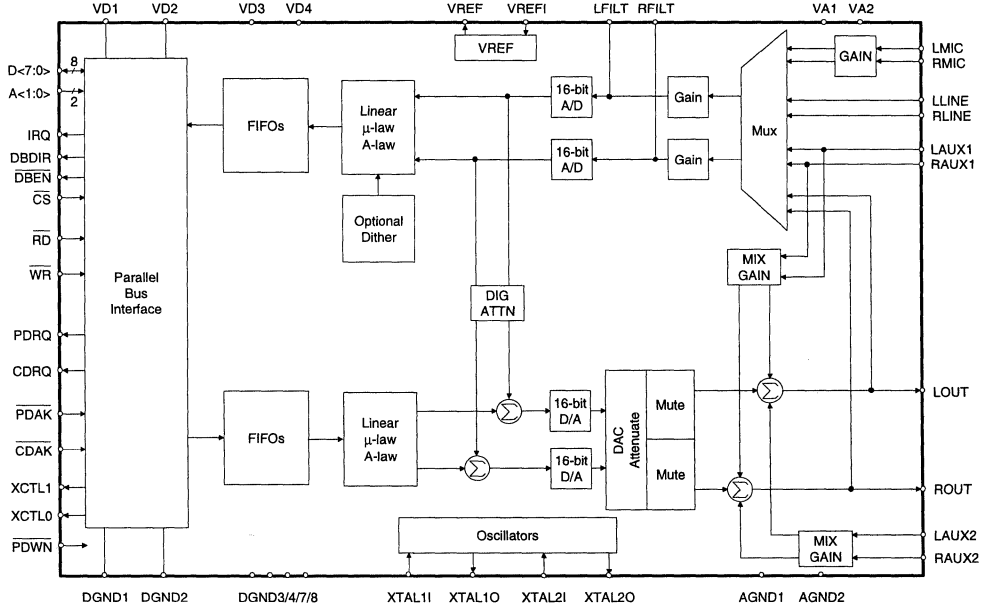
- Integrated parallel interface to ISA and EISA buses
- Stereo Digital Audio at sample rates from 4 kHz to 50 kHz with 16-bit resolution.
- DMA Transfers with on-chip FIFOs
- Free Window™ Software Drivers
- Linear, μ-law, and A-law coding
- Pin compatible with the AD1848 (PLCC)

General Description

mwave The CS4248 is an Mwave™ audio codec.

The CS4248 is a mixed signal integrated circuit that provides 16-bit audio for computer multimedia systems. The CS4248 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data. The CS4248 combines conversion, analog mixing, and programmable gain and attenuation to provide a complete audio subsystem in a single 68-pin PLCC or 100-pin TQFP package. The CS4248 includes an 8-bit parallel interface to the industry standard ISA bus.

For more information call (512)445-7222 and ask for the Audio Databook.



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DRIVERS

CS4231 and CS4248 Device Drivers

Features

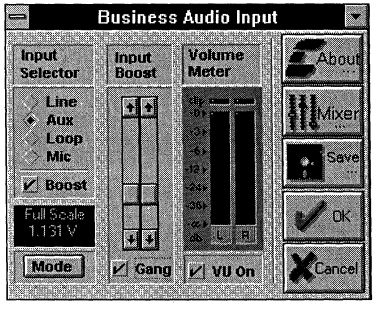
- Support wave audio capture, playback under Windows 3.1 & NT
- Highly optimized code for maximum throughput, minimum CPU utilization
- Input & Output volume/mixing control
- Support ADPCM compression & decompression
- Full Duplex audio capture & playback
- Complete with installation routines, documentation, etc.

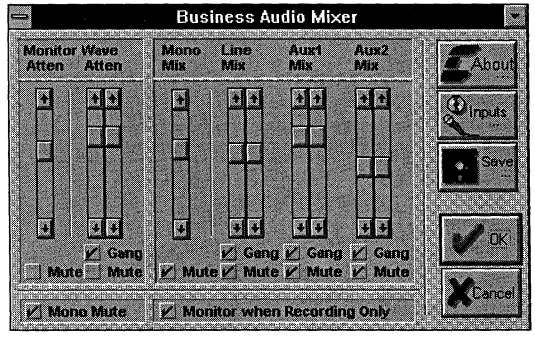
General Description

Crystal offers complete wave driver support for the Microsoft Windows 3.1 & NT environments. CS4231 drivers supports full duplex operation -- i.e. simultaneous capture and playback. Full duplex permits voice recognition to control multimedia playback. Control panel applets are provided supporting all features of the CS4248 and CS4231 devices. Functions include: 1) Input control panel used to select audio source and individually set the gain level, turn dither on/off, and visually monitor recording levels with a VU meter; 2) Output control panel used to control volume, mixer levels and loopback monitoring; 3) Recorder applet used to capture and playback .WAV files, at various sample frequencies, with compression & de-compression (ADPCM, ULaw & ALaw). The recorder is an OLE server.

All source code was developed in-house. Object code is provided without licensing fees directly by Crystal. Sample copies are available.

For more information call (512)445-7222 and ask for the Audio Databook.





Product Preview

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Multimedia Audio Codec Diagnostic Software

Features

- Development and manufacturing test support for the CS4248 & CS4231
- Control over every feature & function - automated board test features
- Measure Codec performance without need of an external signal source
- Record and playback .WAV files in the DOS environment
- Real-time FFT, time and frequency-response plots

General Description

The diagnostics program for the CS4231 and CS4248 assists in every phase of PC audio sub-system design. From initial board bring-up and functional testing to factory test and field service, the diagnostics provide in-depth information to the engineer regarding audio performance and function.

Detailed reporting capabilities aid in both burn-in and board debug. The diagnostics support communication through input and output files, as well as DOS exit codes, allowing it to be spawned by another program and return meaningful results. A system-level diagnostics/factory test system could thus use the program while retaining its' own user interface routines.

The diagnostics run under DOS, and are controlled by a command line interface optimized for minimum keystrokes. Sample 'C' source code is available detailing how to call the routines from inside a host program.

All source code was developed in-house by Crystal. Object code is provided to OEMs without charge. Sample copies are available.

For more information call (512)445-7222 and ask for the Audio Databook.

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CWDRGNTT

Talk→To Voice Recognition from Dragon Systems

Features

- World's foremost voice recognition
- Supports popular Windows apps.
- Hands free command & control in the Windows 3.1 environment
- Reduces typing for data entry
- Speaker independent - also supports regional dialects through training
- Supports 64 active commands; context sensitive for unlimited recognition

General Description

Talk→To is a powerful and flexible voice recognition package for the Microsoft Windows 3.1 environment. Voice recognition enhances productivity by allowing users to enter simple voice commands, instead of complicated keystrokes or multiple mouse movements, to choose menu and control options. Voice recognition redefines the human/computer interface, making it truly intuitive. Talk→To is highly speaker independent, yet may be quickly trained to support an individual's speaking style, thus handling regional or foreign accents.

Crystal Semiconductor has a strategic relationship with Dragon Systems to allow OEMs to integrate voice recognition capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

For more information call (512)445-7222 and ask for the Audio Databook.

Product Preview

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Semiconductor Corporation

CWMNLG

First Byte's Monologue for Windows

Features

- Monologue Text-To-Speech synthesis software from First Byte.
- Industry leading text-to-speech
- Allows Windows applications to speak
- Permits efficient proof-reading of text and numerical data
- Multilingual: French, German, Spanish and American available now; Italian, British and Japanese in development
- Transfer data through clipboard or direct DLL/DDE link

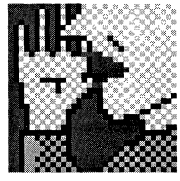
General Description

Monologue increases productivity in the business environment, allowing users to add speech capabilities to any Windows (or DOS) application. Any pronounceable combination of letters and numbers will be spoken clearly. No voice recording or speech training is necessary. Customizable speech parameters permit control of volume, pitch and speed. An exception dictionary allows the user to save preffered pronounciations of words and abbreviations.

Crystal Semiconductor has a strategic relationship with First Byte to allow OEMs to integrate speech capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

For more information call (512)445-7222 and ask for the Audio Databook.



Monologue
16-bit

10

Product Preview

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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

CRYSTAL
Semiconductor Corporation

CS4920

Multi-Standard Audio Decoder - DAC

Features

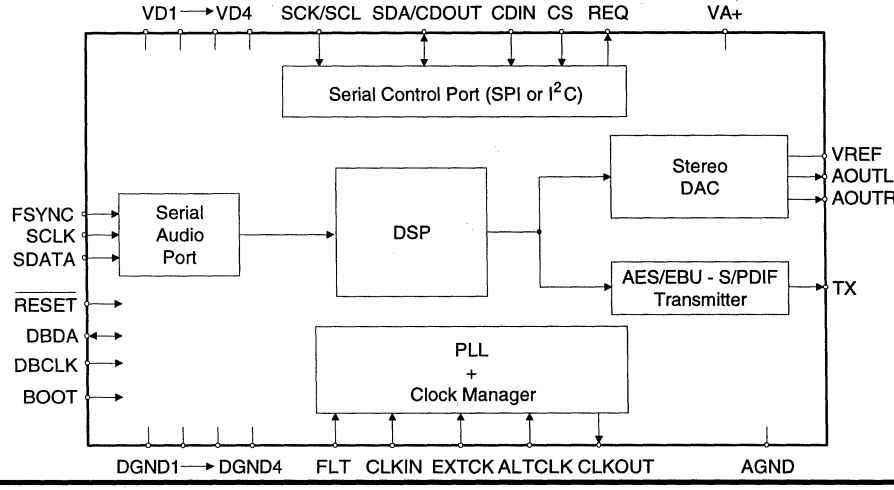
- General Purpose Digital Signal Processor Optimized for Audio
  - 24 Bit Fixed Point
  - 48 Bit Accumulator
  - 16.9 MIPS @ 44.1 kHz Sample Rate
- On-Chip Functional Blocks Include:
  - -CD Quality D/A Converter
  - -Programmable PLL Clock Multiplier
  - -AES/EBU - S/PDIF Compatible Digital AudioTransmitter
  - -Audio Serial Input Port
  - -Serial Control Port
- Applications Include:
  - -Audio Decompression
  - -MPEG Layers 1 and 2
  - -Dolby AC-2
- Standard 44 pin PLCC Package

General Description

The CS4920 is a complete audio subsystem on a chip. This device contains a general purpose DSP, a CD quality stereo Digital-to-Analog Converter, a programmable PLL clock multiplier, an AES-EBU - S/PDIF compatible digital audio transmitter, an audio serial input port, and a serial control port. The CS4920 is based on a programmable DSP core and is intended to support a wide variety of digital signal processing applications which include decoding compressed digital audio. Serial audio data broadcast on networks such as cable TV, direct broadcast satellite TV, or the telephone system can be decompressed and converted to standard analog or digital signals.

Both industry standard and proprietary DSP algorithms can be supported. Software which performs industry standard MPEG layers 1 and 2 and Dolby AC-2 is available. A complete set of software development tools are available. These include an assembler, simulator, and debugger.

For more information call (512)445-7222 and ask for the Audio Databook.



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CS8905

Programmable Music Processor

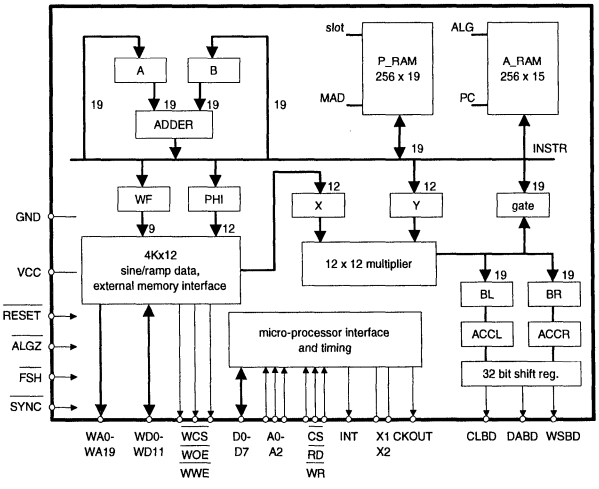
Features

- Polyphonic up to 16 notes
- Multi-timbral up to 16 simultaneous timbres
- Oscillator frequencies to 48 MHz (46.875 kHz sampling rate)
- Stereo 16 bit digital audio output
- On-chip 256x15 Algorithm RAM, and 256x19 Parameter RAM
- Built-in sine and ramp data
- Addresses up to 1Mx12 sample ROM directly, 64Mx12 using paging
- Single +5V supply CMOS, 50 mW typical power dissipation
- 68 pin PLCC package

General Description

The CS8905 is a high performance programmable signal processor which is specially designed for music and sound generation applications such as music synthesis and digital effects processing. This device features 19-bit internal data paths, a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register. As a music synthesizer, the CS8905 is capable of generating 16 notes of polyphony with a high quality 16-bit stereo digital audio output at a 44.1 kHz sampling rate. For wave table synthesis applications, up to 64 Msamples of external sample memory may be addressed, and the CS8905 can generate linear envelope segments under external microprocessor control. The micro-programmable architecture of the CS8905 also makes this device well suited for use as a digital effects processing engine.

For more information call (512)445-7222 and ask for the Audio Databook.



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CS9203

Advanced Music Synthesizer

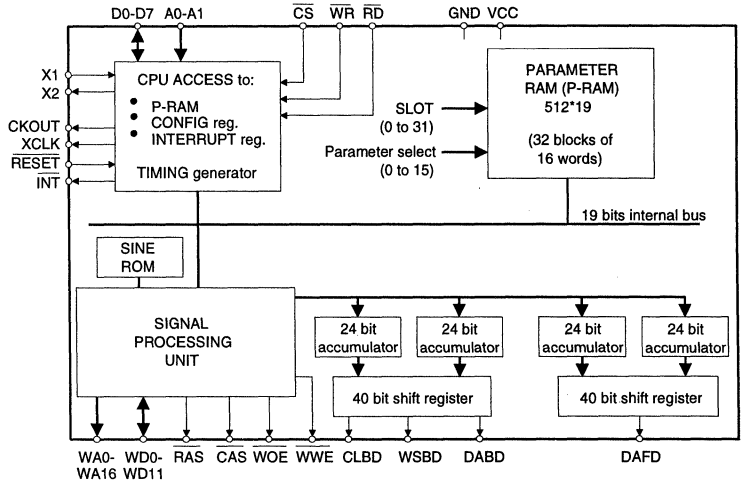
Features

- Polyphonic up to 32 notes
- Multi-timbral up to 32 simultaneous timbres
- 15 built-in synthesis algorithms
- On-chip high speed adder, multiplier, and 24 bit accumulators with overflow protection
- Built-in sine wave data
- Addresses up to 8Mx12 external sampling memory (ROM, SRAM, or DRAM)
- Two stereo 16 - 20 bit digital audio outputs (four audio outputs)
- Independent pan and volume mix assignable for each voice
- +5V supply CMOS, 50 mW power
- 68 pin PLCC package

General Description

The CS9203 is a high performance signal processor which is specially designed for high-quality music synthesis applications. Fifteen built-in music synthesis algorithms make the CS9203 extremely flexible, and the advanced features associated with it's PCM sampling algorithms, such as linear interpolation between samples, linear segment envelope generator, and 12 dB variable Q filtering, make the CS9203 a superb wave table synthesis engine. Dual stereo digital audio outputs are provided to allow the addition of an external effects processor, such as the CS8905. The 32 note polyphony and 32 part multi-timbral capabilities of the CS9203 make it an ideal choice for General MIDI (GM) synthesis applications, including musical instruments, MIDI sound modules, Karaoke machines, and high quality Personal Computer sound cards.

For more information call (512)445-7222 and ask for the Audio Databook.



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(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CRD9203

General MIDI Music Synthesizer Daughtercard

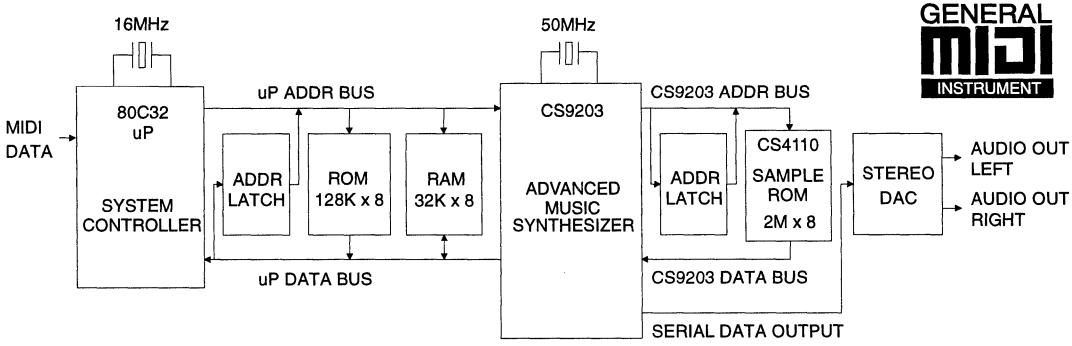
- Professional quality music synthesis for the Multimedia PC
- Low-cost Daughtercard implementation with Wave Blaster™-compatible pin-out
- 24-, 28- or 32-note polyphony, 16-part multitimbral
- Supports Roland GS bank select and GS envelope and filter controls
- Nearly 300 quality instrument sounds, including GS variations and drum kits
- Complete manufacturing kit available

General Description

The CRD9203 is a reference design wavetable synthesizer based on the CS9203 Advanced Music Synthesizer IC. This General MIDI synthesizer is implemented as a daughter card subsystem for a Personal Computer audio adapter (sound card). The host interface connector and pin-out is compatible with the Creative Labs Sound Blaster 16™ and Wave Blaster™ products. The CRD9203 plugs directly onto a host sound card, such as the Sound Blaster 16; Sound Galaxy NX Pro 16, AudioWave Platinum 16, or the CRD4231 reference design, to provide professional quality MIDI music synthesis in the PC environment. The exceptional sound quality of this design makes it an ideal choice for business multimedia, education, entertainment, computer games, or music composition applications.

The CRD9203 is available stand-alone or in combination with the CRD4231 16-bit audio adapter reference design.

For more information call Crystal Semicondutor at (512)445-7222



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Semiconductor Corporation

CRD9203R

GM/GS Music Synthesizer Daughtercard

- Professional quality music synthesis with digital reverb & chorus effects.
- General MIDI (GM), General Synthesizer (GS), Sound Canvas™ MKII, and MT32 compatible
- 24- or 32-note polyphony, 16-part multitimbral
- Four MBytes of ROM store a total of 393 sounds: 225 instruments, 120 drum sounds, & 48 special effects
- Wave Blaster™ compatible pinout

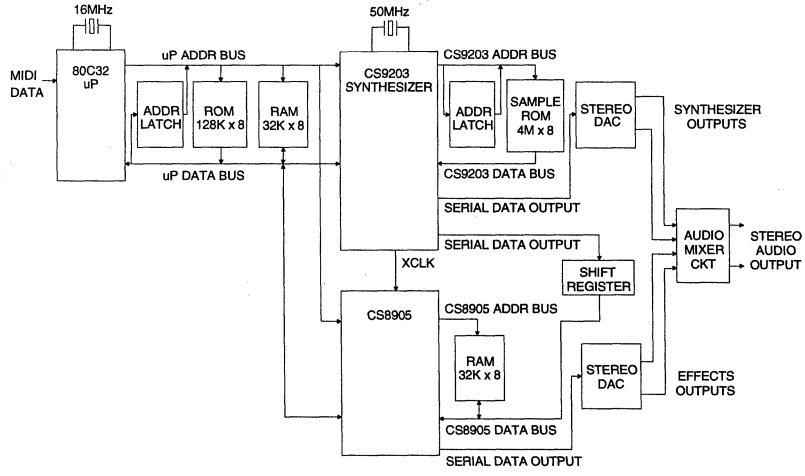
General Description

The CRD9203R is a high-polyphony multi-timbral wavetable synthesizer daughtercard, implemented using the CS9203 Music Synthesizer and the CS8905 Effects Processor. The CRD9203R daughtercard attaches to a host PC audio adapter (sound card), such as the CRD4231 reference design, through the 26-pin host interface connector. The connector pin-out is Wave Blaster compatible, allowing compatibility with a number of existing PC audio adapter cards.

The CRD9203R synthesizer features four Megabytes of pcm instrument samples which have been developed for the highest level of compatibility with General MIDI and General Synthesizer standards, and with the industry-standard Roland Sound Canvas products. The synthesizer features resonant filters for each voice, and reverb and chorus levels are adjustable on a per-channel basis.

The synthesizer can also be integrated onto the audio adapter card, or adapted for stand-alone applications.

For more information call Crystal Semicondutor at (512)445-7222



GENERAL MIDI INSTRUMENT

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CONTENTS

Application Note

Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems

By Roger Taylor

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Introduction

The T1 (1.544 Mbps) transmission system is widely used in North American public and private telephone networks. An analogous system, PCM-30 (2.048 Mbps), is used outside North America. Both of these primary rate transmission systems must meet exacting pulse shapes as described in Bellcore TR-NWT-000499, ANSI T1.102-1993, AT&T CB-119 and CCITT G.703. Crystal Semiconductor T1 and PCM-30 line interface devices have pulse shaping line drivers whose output pulses are designed to meet the pulse-shape requirements of the specifications stated above. Measuring these pulses to ensure they comply with the specifications is not as straightforward as it may seem. This paper covers pulse shape measurement techniques to allow accurate assessment of T1 and PCM-30 pulse shapes.

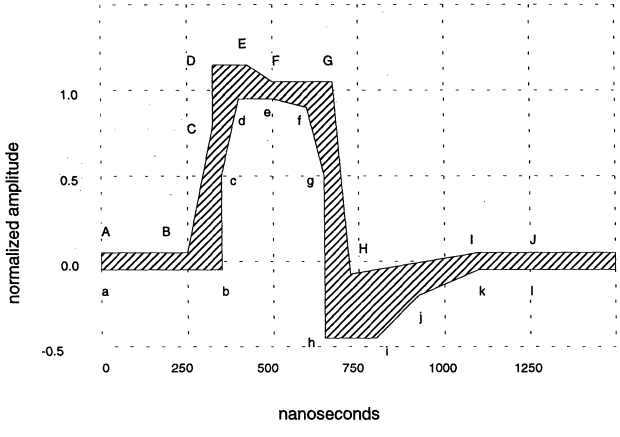
Pulse Shape Requirements

T1 equipment designed for central office use must interface with a DSX-1 cross connect. For most applications, the transmitter is located within 655 feet of the cross connect. All T1 pulses arriving at the cross connect must meet the pulse amplitude and template requirements at the cross connect as shown in Figure 1, whether the originating transmitter is a few feet away or 655 feet away. The line is terminated with a 100 Ω load. The pulse amplitude is measured at the center of the pulse and must be within 20% of 3.0 volts according to CB-119. (Other specs differ slightly; be sure to consult the applicable spec.) If the amplitude requirement is met, the pulse may be linearly scaled to fit within the template.

PCM-30 pulse shapes are specified in Rec. G.703. In this case, the pulses are measured at the output of the line driver only, and *not* required to meet the pulse template over a variety of cable lengths. The pulse must fit the template without scaling.

For 2.048 MHz operation, there are two amplitudes specified depending on the type of cable used. For 75 Ω coax, the pulse height is 2.37 volts ±10%. For 120 Ω symmetrical (shielded-twisted) pair, the specified pulse amplitude is 3.0 volts ±10%. The CCITT G.703 template for 2.048 MHz operation is shown in Figure 2.

CCITT also specifies a template for operation at 1.544 MHz which is shown in Figure 3. This



Maximum Curve		
A	(0,	0.05)
B	(250,	0.05)
C	(325,	0.80)
D	(325,	1.15)
E	(425,	1.15)
F	(500,	1.05)
G	(675,	1.05)
H	(725,	-0.07)
I	(1100,	0.05)
J	(1250,	0.05)

Minimum Curve		
a	(0,	-0.05)
b	(350,	-0.05)
c	(350,	0.50)
d	(400,	0.95)
e	(500,	0.95)
f	(600,	0.90)
g	(650,	0.50)
h	(650,	-0.45)
i	(800,	-0.45)
j	(925,	-0.20)
k	(1100,	-0.05)
l	(1250,	-0.05)

Figure 1. ANSI T1.102 - 1993 T1 pulse template

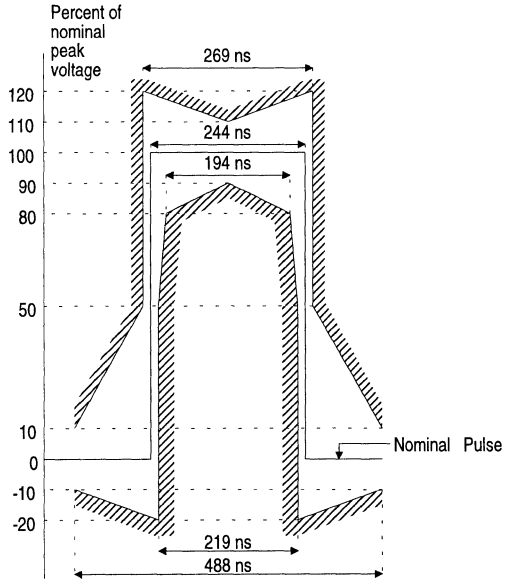


Figure 2. CCITT Rec. G.703 pulse template for 2.048 MHz operation

pulse shape is very similar to the pulse shape shown in Figure 1. As in T1 applications, the pulse is required to meet the template at the digital distribution frame. In this case however, the pulse must meet the mask without scaling. The peak undershoot is specified not to exceed 40% of the peak pulse amplitude.

The remainder of this paper discusses procedures which should be used to accurately measure pulse shapes. There is also a section on measuring pulse imbalance and power transmitted levels.

Reflections

When transmitting a high frequency pulse down a transmission line, a portion of the pulse will reflect wherever it encounters an impedance mismatch. The amount of reflection is proportional to the impedance mismatch; the greater the mismatch, the greater the reflection of the pulse. Even hooking two pieces of wire with different characteristic impedances together will cause re-

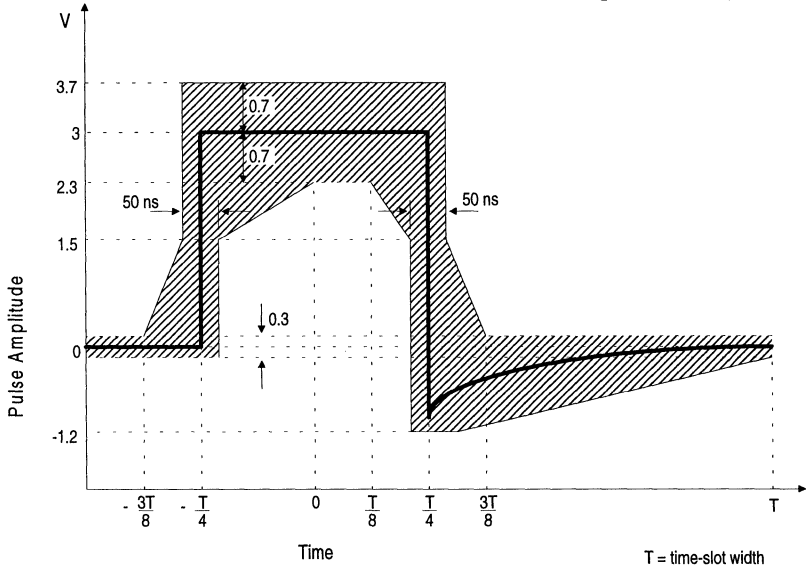


Figure 3 - CCITT Rec. G.703 pulse shape for 1.544 MHz operaton.

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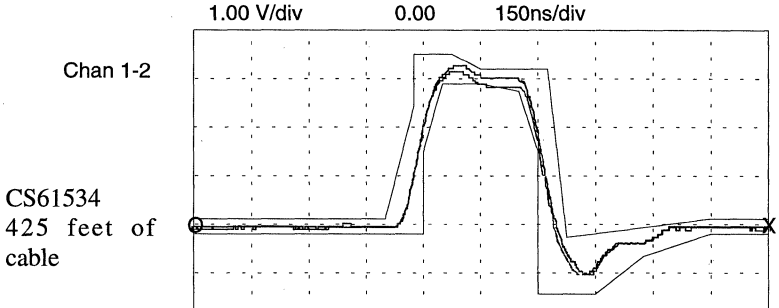


Figure 4 - The smaller pulse's amplitude was reduced by combination with a reflection from a previously transmitted pulse in a repeating 1 out of 2 pattern. The larger pulse is

flections. In order to avoid reflections in a transmission line, impedance mismatches should be avoided, and the line should be terminated with a load that is equal to the characteristic impedance of the line. Proper terminations are every bit as important when measuring pulses in the lab as they are in connecting up the network.

Remember that the load specified for T1 pulse shape measurement is 100 Ω. A commonly used cable in T1 applications is Western Electric ABAM cable which has a characteristic impedance in the neighborhood of 110 Ω. This means that even an otherwise optimal test setup will have a reflection at the load. When this reflection returns to the source, it is likely to experience an even greater impedance mismatch at the driver outputs and therefore have a relatively large reflection component at the source.

One way to reduce reflections at the load is to terminate the desired length of cable with a comparatively long piece of the same type of cable which is then terminated with the load resistor. Such a setup begins to approximate an infinite amount of cable which should provide an optimal impedance match for the test length. In addition, any reflection from the load resistor will be attenuated by the resistive loss of the cable and should be insignificant by the time it returns to the measurement point. *However*, for Central Office equipment, the standard test method is as follows: the cable will be disconnected at the DSX-1, terminated with a 100 Ω load resistor, and measured for compliance with the template. This approach should be used in your lab as well.

Reflections in a lab setup can be minimized by eliminating impedance mismatches wherever possible. The best way to eliminate mismatches is to use the same type of test cable everywhere; that is, from the output of the driver to the input to the oscilloscope. Impedance mismatches due to coax test cables, probes, test leads, or any other leads connected to the line will cause reflections.

Data Pattern

The first step in measuring pulse shapes is to notice that the T1 specifications call for an *isolated* pulse. Unless the pulse is sufficiently isolated, reflections on the line can badly corrupt the measured pulse shape. However transmitting a repeating pattern is necessary to trigger the oscilloscope. A repeating one out of 16 pattern (repeating a 1000 0000 0000 0000 AMI data pattern) is recommended to isolate the pulses to allow reflections to die.

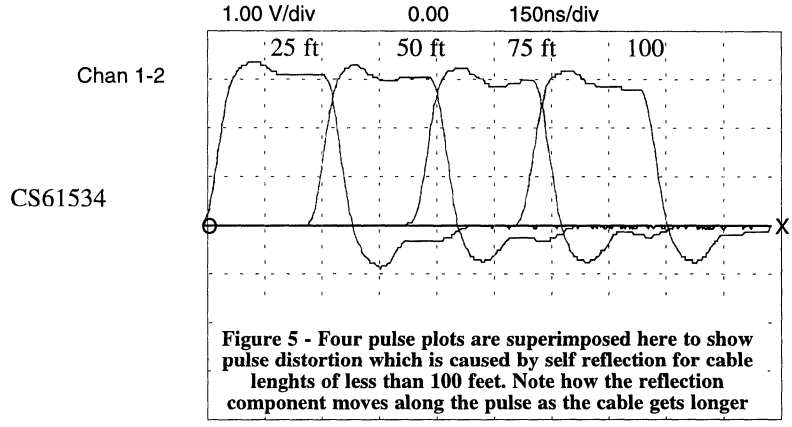


Figure 5 - Four pulse plots are superimposed here to show pulse distortion which is caused by self reflection for cable lenghts of less than 100 feet. Note how the reflection component moves along the pulse as the cable gets longer

Why is the isolated pulse important? Let's assume that a portion of the pulses will be reflected at both ends of the line. As a pulse travels down the line at about 0.66 ft/ns, it will reflect from the termination, reflect from the source, and return to the termination of a 425 ft cable about 1932 ns after it was transmitted, just in time to combine with a pulse transmitted 1296 ns later when it arrives at the load. Depending on the sign of the reflections, this reflected pulse can be either added to or subtracted from the pulse arriving two bit periods later. This is the situation one would observe when transmitting a one out of two pattern as shown in Figure 4. A one out of 16 pattern allows plenty of time between each pulse for reflections to die out of a properly terminated line, allowing accurate measurement of the transmitted pulse.

CCITT specifications for 1.544 MHz operation are very similar to North American T1 specifications in that an isolated pulse is specified and pulses are measured at the distribution frame. There are two significant differences for 2.048 MHz operation. First, G.703 specifies that all pulses must meet the template, not just an isolated pulse, implying that any data pattern is acceptable. Thankfully, the second difference is that pulses are measured at transmitter output rather than after some length of cable, so reflection interaction due to different cable lengths is not a consideration.

Self Reflections

When making pulse shape measurements on short line lengths (generally less than 100 feet), pulses can reflect upon themselves, distorting the pulse shapes of isolated pulses as shown in Figure 5. Nonisolated pulses will likely suffer even greater distortion. Self reflection is unavoidable as long as impedance mismatches exist. Proper termination is crucial when measuring pulse shapes for CCITT G.703 compliance at 2.048 MHz.

Equipment

It is important to understand and identify the sources of error in measurement equipment and choose equipment to minimize any error sources. Since pulses are transformer-coupled to the line, they are differential in nature, so pulse shape measurement should be made in a truly differential manner. Grounding one wire for single ended measurement can introduce uncertainties due to transformer nonidealities, and cable characteristics such as distributed capacitance to a ground, which may be different from the oscillo-

scope ground. Consider that in making a single ended measurement, one wire is referenced to ground while the other wire is unbalanced.

The exception is transmission over 75Ω coaxial cable at 2.048 MHz. CCITT G.703 states that the outer conductor shall be connected to ground at the output port. Accordingly, measurements of pulse shape should be made with the outer conductor grounded at the oscilloscope input. A single oscilloscope channel is sufficient.

Probes and oscilloscope amplifiers with good balance and high CMRR should be used. Probes, if used, should have low capacitance so pulse distortion is minimized. Unmatched 10X probes may cause significant measurement error due to relative inaccuracies in the 10X attenuation and poor CMRR. Also, the CMRR between two channels of an oscilloscope is rarely specified and is generally very low.

Eliminating the probes altogether is generally preferable. In this case, the same type of cable should be used from the output of the line driver to the input of the oscilloscope. Ideally the load for the cable should be placed at the inputs to the oscilloscope. Some oscilloscopes can be set for internal 50 Ω termination at the inputs. Alternatively, a 50 Ω termination can be connected to both oscilloscope inputs. Providing 50 Ω termination from each wire to ground is analogous to connecting 100 Ω across the two wires, but has the distinct advantage of providing both oscilloscope inputs with signals referenced to the same point rather than having the inputs floating with respect to one another. The 50 Ω resistors should be equal in resistance. Fifty ohm terminating plugs work well and are readily available.

For compliance with CCITT G.703, use 60Ω terminations from both channels to ground when evaluating equipment designed for 120Ω shielded twisted pair, and a 75Ω termination resistor from oscilloscope input to oscilloscope ground for equipment using 75Ω coax. With a little imagination, these terminations can be easily created and attached to the oscilloscope inputs.

Some specifications such as AT&T Publication 43801 call for a 100 Ω resistor connected across TIP and RING. If this setup must be rigidly followed, use either matched differential probes, or the shortest leads possible between the load and the oscilloscope. It may be necessary to use two 50 Ω resistors in series so the oscilloscope can be grounded to a reference point relative to the line so it can trigger. (This is the same as 50 Ω terminators.) These resistors must be accurately matched.

Digital oscilloscopes offer some features such as plotting, amplitude scaling and time and amplitude measurement which makes their use desirable when evaluating pulse shapes. However, be advised that digital oscilloscopes have inherent inaccuracies in the analog to digital conversion and in the sampling process. Most high frequency digital oscilloscopes use either 6-bit or 8-bit A-to-D converters. A six-bit ADC divides a full scale input into only 64 parts, so the quantization error is significant. Any gain error or offset error in the converter, in either channel or between the two channels, will result in amplitude error and distortion of the actual pulse shape. Calibration of a digital oscilloscope is essential to making accurate measurements. Any noise present on the signal or within the converter during the conversion process will result in an error in the conversion. Averaging a fairly large number of samples will help reduce uncertainties caused by noise (quantization or external). Such averaging cannot compensate for ADC nonlinearity errors however.

Sampling uncertainty of digital oscilloscopes must also be considered. If the oscilloscope is sampling at 150 MHz, the sample period is 6.7 ns. For pulse width measurements, the worst

case time quantization error is 13.4 ns which can be significant when measuring 244 ns or 324 ns wide pulses. Once again, averaging several samples effectively eliminates any error due to sampling uncertainty.

Digital oscilloscopes are very useful in evaluating pulse shapes. However, the averaging process will tend to mask pulse-to-pulse variations that are undesirable. It is advisable to check the results on an analog oscilloscope which is in calibration.

A oscilloscope with a delayed triggering feature is essential. Delayed triggering allows precise positioning of the isolated pulse on the screen, and also allows the user to amplify and observe a small portion of the pulse which may require greater scrutiny. Delayed triggering also allows for fairly easy comparison of positive and negative pulses for verifying that pulse imbalance requirements are met.

No matter which instruments you have available, a proper test setup is essential. Three good measurement techniques are as follows:

1) An active differential probe such as the Tektronix P6046 allows differential signal processing at the probe tip with very high CMRR. Only a single channel on the oscilloscope is required thus removing CMRR considerations at that point. This probe offers distinct advantage when using a digital oscilloscope in that the addition of the quantization errors of the two channels is avoided. For both analog and digital oscilloscopes channel-to-channel inaccuracy and imbalance are no longer an issue and CMRR is much better.

2) Use a true differential amplifier with good common mode rejection such as the Tektronix 7A13. Run the test wire all the way to the diff amp's input (avoid using test leads for interconnection) and terminate the line at the inputs with 50Ω (60Ω for CCITT 120Ω shielded twisted pair). The only probes that should be considered for use in such measurements are matched probes with high CMRR like the Tektronix P6055. When using probes, make sure they are calibrated.

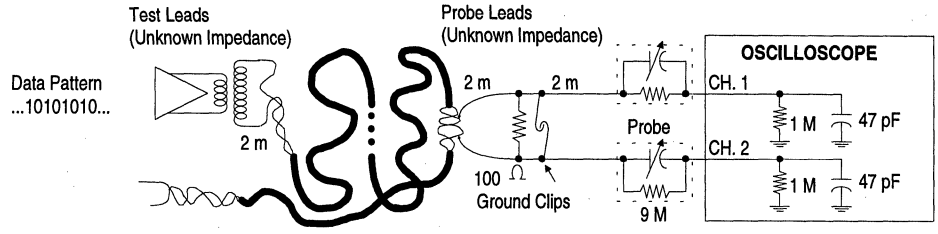
3) As previously discussed, using a standard two channel oscilloscope has some disadvantages, but may be the only method available for pulse shape measurement. Once again, it is best to run the test wire all the way to the oscilloscope inputs and terminate the line at the oscilloscope inputs. (If probes are necessary, use matched and calibrated probes.) TIP should be connected to one channel and RING to the other channel. Invert channel 2 and add it to channel 1. Always set the oscilloscope inputs for DC coupling to keep the internal oscilloscope capacitors out of the circuit. The amplifiers should always be in the calibrated configuration.

The following figures illustrate pulse measurement techniques and show an example of the error that can be caused by poor techniques. Figures 6 and 7 show some DOs and DON'Ts for measuring pulse shapes. Figure 8 shows the effects of terminating the line with a floating 100 Ω resistor and measuring the signal across the resistor with unmatched probes.

Pulse Shape Evaluation

The pulse displayed on the oscilloscope must be checked for amplitude and conformance to the pulse template. The pulse amplitude is measured at midpulse. The method for checking for conformance with the template depends on the specification. For CCITT specifications, the pulse must fit the template with no scaling allowed. DSX-1 specifications allow the pulse to be scaled by a linear factor to fit within the template. Figure 9 shows a pulse which has been aligned, scaled and plotted from a digital oscilloscope onto a template.

What's Wrong With This Picture?

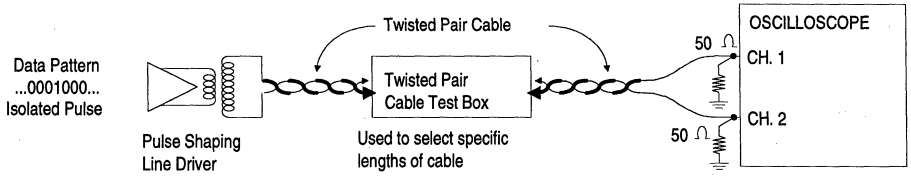


- Numerous impedance mismatches - reflections galore
- Data pattern does not provide an isolated pulse.
- Floating termination - no ground reference for measurement
  (but required by 43801)
- Undetermined tail on cable - improper termination
- Are probes precisely 10:1?
  Have they been calibrated correctly?

Figure 6 - How NOT to measure pulses.

PULSE MEASUREMENT USING TWO CHANNEL OSCILLOSCOPE

- Avoid reflections due to impedance mismatches
  - Despite taking precautions, neither end of the cable will be ideally terminated so watch for reflections from previous or current pulse
  - Use the same type of cable where ever possible



- Oscilloscope should be DC coupled
- High-resolution, digital oscilloscopes are nice because pulses can be precisely scaled and plotted making evaluation easier
- Test cable terminated at oscilloscope input

Figure 7 - Recommended pulse shape measurement test configuration and guidelines.

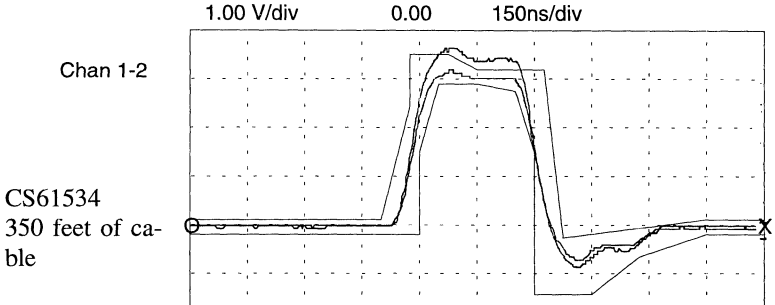


Figure 8 - Mistermination and gain error can have significant effect on pulse amplitude. The larger pulse results from the use of probes which are not well matched,

When evaluating pulse amplitude and template conformance, be sure to test over the line driver's specified operating voltage and temperature ranges. For amplitude measurements, setting the oscilloscope for 0.5 V/div is best, while 1.0 V/div is convenient for template matching.

Creation of the pulse template against which the displayed pulse is to be evaluated is worthy of consideration. It is important that the template have the correct proportions so that the pulse may be accurately evaluated. In some cases, the template must be created to an absolute scale so it can overlay the pulse or have the pulse plotted over it. Reproduction of the pulse template is very tricky since copiers tend to distort the original. A first generation photocopy can have enough distortion to render the copied template useless. Only through painstaking effort can a useful copy be produced (and if this method is used, make an abundant number of copies once the copied template is accurate).

To evaluate a pulse displayed on the oscilloscope's CRT, create a template which is scaled to the oscilloscope grid on a transparency, align the template to the grid and affix the template to the CRT. Center the pulse in the template. Scaling the pulse by adjusting the amplifier gain is only possible when using a single channel oscilloscope, a differential amplifier, or a digital oscilloscope. When using a two channel oscilloscope, method three, do not use the amplifier's gain adjustment (uncalibrated) to adjust the pulse

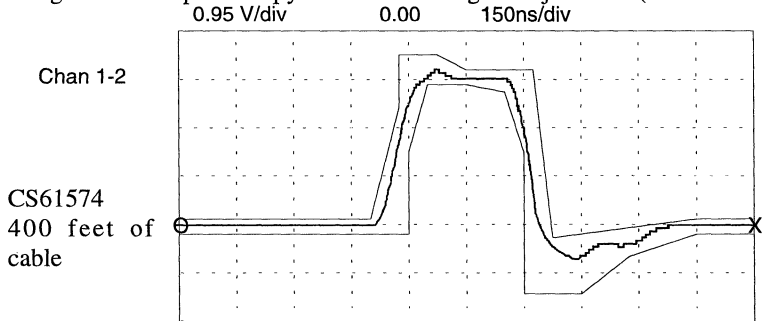


Figure 9 - Plot of a properly terminated, isolated pulse from a CS61574. Note that the amplitude scaling feature of the digital 'scope was used to boost the pulse amplitude

amplitude to match the template. Adjusting one channel only results in a nonlinear change in the pulse. Additional templates scaled to larger and smaller amplitudes are required.

Once everything is satisfactorily aligned, take a picture. It is much easier to describe, complain about or compare pulse shapes on hard copies. A hard copy also provides a permanent record for future reference.

Most digital oscilloscopes have the capability to transfer the image displayed on their screen to a plotter. There are three basic methods of plotting available. The most sophisticated method allows entry of the template parameters to the system so the template is plotted to the appropriate scale along with the pulse.

A second method offered by some systems, allows the operator to align the oscilloscopes plot dimensions to an independently created grid. This method allows the user to create the template to a convenient scale. Using the plotter, the corner points of the oscilloscope's grid are physically aligned with the corner points of the grid on the plotter paper. The plotter then scales the plot of the oscilloscope's grid to fit the grid on to plotter paper. This technique is especially good when using photo copies of an original grid and template. Since the plot is scaled to fit, copier distortion is irrelevant.

The third method involves generating a template for a plotter without a scaling feature. The template must be created to exactly the same size as the plotter's rendition of the oscilloscope grid, and positioned on the plotter paper at precisely the point at which the oscilloscope's display is plotted. The biggest problem here is creating a sufficiently large number of blank templates which are the right size and in the right place so they will line up with the plot. The alternative is to generate a single template on a transparency to overlay the plots, but this approach makes it difficult to evaluate a large number of plots.

An especially nice feature of digital oscilloscopes is the gain scaling which allows the user to linearly scale the pulse either up or down to fit a fixed template. For instance, if the pulse is a little short, the gain may be set for 0.95 V/div, thereby making the pulse a little taller. The horizontal and vertical settings are usually plotted along with the trace, so these settings are recorded as well. Take care to maintain the time scale to a fixed value which corresponds with the template. Pulse width scaling is not allowed.

A note about the DSX-1 pulse template: the minimum pulse width allowed is 300 ns, the maximum is 400 ns. If the pulse width is based on a 50% duty cycle of a 1.544 MHz clock, the pulse width will be 324 ns. This allows only 12 ns of margin to either side of the template's minimum curve. When compared to the template, the pulse will look narrow, but it is really all right. (Presumably, the minimum allowable pulse width is kept wide to help maximize receiver jitter tolerance.) The opposite situation exists for CCITT G.703 pulse width specifications which range from 194 ns to 269 ns. A 50% duty cycle pulse, 244 ns, is a little on the wide side.

Positive/Negative Imbalance and Power Levels

Pulse imbalance and signal power level measurement are both intended to ensure that there is no significant DC offset at the termination of the line. Since positive to negative pulse imbalance can result in more power at 1.544 MHz relative to the power at 772 kHz of an all ones signal, meeting the power level specifications also means pulse imbalance is satisfied.

An oscilloscope can be used for checking pulse imbalance between the positive and negative pulses. CB-119 calls for less than 0.5 dB difference between the power of positive and negative pulses. Power is roughly the product of the square of the pulse height and pulse width, so both must be investigated. There should be less

than 200 mV difference in amplitude of otherwise identical positive and negative pulses. Variation in the widths of positive and negative pulses of only a few nanoseconds will also result in some pulse imbalance. One good method for comparing positive and negative pulses is through the use of a digital oscilloscope which is capable of integrating the area of a pulse; this makes for straightforward comparison of the positive and negative pulses.

Measurement of power levels in an all ones pattern is best accomplished with a specialized instrument such as the Hewlett Packard 3586B (HP 3586A for CCITT). This instrument can measure the power in a 2 kHz band at both 772 kHz and 1.544 MHz as required by CB-119. The power in the 2 kHz band at 772 kHz must be between 12.4 dBm and 18.0 dBm, and at least 29 dBm greater than the power in a 2 kHz band at 1.544 MHz . CCITT 1.544MHz specs require the power in a 3 kHz band at 772 kHz be between 12.0 dBm and 19.0 dBm and at least 25 dBm greater than the power in a 3 kHz band at 1.544 MHz. CCITT PCM-30 specs allow ±5% variation in the heights and widths of positive and negative pulses. When using this instrument, take care to terminate the line driver properly. The input impedance of the HP 3586 is selectable but 100 Ω input impedance is not offered. A HP 15508B converter will provide a 110 Ω balanced termination for the line and 75 Ω unbalanced impedance for the input of the instrument.

Alternatively, power levels can be measured using a spectrum analyzer. An estimation of the power at 772 kHz can be made by selection of the appropriate resolution bandwidth of the spectrum analyzer. As long as the power at 772 kHz meets the specification with reasonable guardband, and the difference in amplitudes of the power at 772 kHz and 1.544 MHz is several dB in excess of the spec, precision measurements are probably unnecessary.

• Notes •

Application Note

Jitter Testing Procedures

for Compliance with AT&T 62411

By Roger Taylor, Greg Stearman and Bob Bridge

Introduction

This application note presents guidelines for measuring whether a design is compliant with AT&T 62411 jitter tolerance, jitter generation and jitter attenuation requirements. 62411 compliance is a necessary requirement for *CPE* (Customer Premises Equipment) which is connected to T1 lines provided by AT&T. These T1 lines may be either private-line or central-office access lines. 62411 may not apply to equipment sold to telephone companies, equipment used within a campus environment or equipment used to access an alternative long-distance carrier.

AT&T 62411 jitter testing can be performed using the test equipment listed in Table 1. Other equipment with jitter generation and measurement capability is available from a number of vendors, but these systems commonly lack the performance required for 62411 in two areas. First, many do not have the ability to generate and measure the large amplitude (>28 UIpp) jitter below 300 Hz which is required by AT&T 62411. Also, many do not have the dynamic range to make the narrow-bandwidth, low amplitude jitter measurements required for measuring 62411 high frequency jitter transfer beyond 40 dB. The equipment and procedures shown here are based upon those used during AT&T conformance testing.

The HP 3785B is a powerful and flexible jitter test set which provides sinusoidal jitter generation and demodulation. The HP 3785B receiver features a front-panel meter which can display the broadband input jitter amplitude as well as the amplitude in the passband of one of its three internal filters. The HP 3785B also provides a demodulator output signal which can be input to a spectrum analyzer to make accurate narrow-bandwidth, high frequency jitter transfer measurements. However, the HP 3785B cannot generate or measure jitter larger than 10 UIpp.

Characterizing large amplitude jitter performance requires an RF signal generator with FM modulation capability. The HP 8656B accepts an externally generated modulating signal (from an audio oscillator) while the HP 8644A provides an internal modulation synthesizer. The RF generator's output is connected to a 50 Ω buffer which produces a logic level clock suitable for the pattern generator external clock input.

HP 3785B	Jitter Generator/Receiver
Phoenix 5500 or HP 3780A	QRTS Pattern Generator and Error Detector
HP 3585A	Spectrum Analyzer
HP8656B and Khron-Hite 5500A or HP 8644A	RF Signal Generator Audio Oscillator RF Signal Generator with Modulation Synthesizer
HP 5372A	Time Interval Analyzer

Table 1. Equipment Used for Jitter Testing

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Jitter Tolerance Measurements

The basic test setup is shown in Figure 1. The RF generator creates a 1.544 MHz jittered clock which clocks the Pattern Generator producing the AMI-encoded QRTS data. The Pattern Generator output connects to the T1 trunk card under test using a twisted pair cable. The signal is routed through the T1 trunk card and synchronizer and back through the trunk card to the data input of the Pattern Receiver. The Pattern Receiver is then used to measure bit errors. The jitter tolerance of a receiver will vary with the width of the AMI pulses. It is very important that the pattern generators used have consistent pulse widths. (The pulses should meet DSX-1 type pulse requirements as identified in CB-119.)

The jitter frequencies typically checked are: 3, 10, 30, 100, 1k, 2k, 4k, 8k, 16k, 32k, 64k and 100k Hz. The normal procedure is to select a jitter frequency, and then increase the jitter amplitude until the onset of bit-errors (for DTE testing) or synchronization loss (for synchronizer testing). The jitter frequency is set with the audio oscillator connected to the HP 8656B modulation input.

The jitter amplitude is set by entering the peak frequency deviation (in kHz) on the front panel of the HP 8656B. Given the frequency deviation, the jitter amplitude in UIpp can be calculated using Equation 1 below.

$$UIpp = \frac{\Delta f}{\pi F_j} \qquad (1)$$

where,

Δf is the frequency deviation in Hz, and
F_j is the jitter frequency in Hz.

It is important to determine how much the system exceeds the minimum 62411 jitter tolerance requirements since the later attenuation tests are made with three-quarters of the observed tolerance of the system. Larger tolerance levels have the benefit of raising the floor on the acceptable output jitter level during the attenuation tests.

AT&T 62411 testing calls for measuring jitter tolerance using a QRTS data pattern, which is representative of live traffic on the network. But the key to guaranteeing jitter tolerance is to test

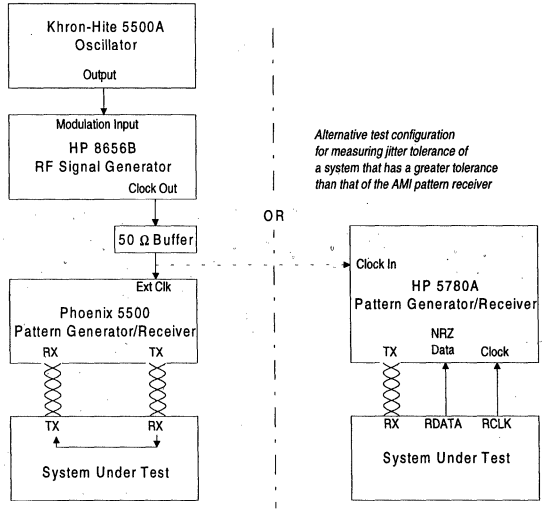


Figure 1 - Test Setup for Jitter Tolerance Measurements

receiver performance using a data pattern which is representative of the worst case conditions within the QRTS pattern. The most stressful jitter case for a receiver occurs when the maximum deviation from the ideal arrival time occurs between two ones which are separated by a string of zeros. For example, two ones separated by seven zeros can have maximum deviation from ideal arrival time at a jitter frequency of 96,500Hz. (Maximum phase deviation occurs in 1/2 of a jitter period; eight bit periods take 5181.4ns.) Still, this maximum jitter hit is dependant on the relationship of the phase of the jitter with respect to the occurence of the string of zeros.

To truely measure jitter tolerance, one must guarantee that the maximum phase deviation between two consecutive ones separated by zeros will occur (assuming that the maximum allowable consecutive zeros is not exceeded). When using a quasi-random data pattern, it is unlikely that the jittered clock and the zero string in the data pattern will align to produce a maximum phase hit between successive ones unless the condition is tested for a long time. To guarantee 0.4 UI of jitter tolerance at jitter frequencies above 50 kHz, it is best to use a short pattern with repeating strings of 7 to 14 zeros to significantly increase the likelihood of a maximum jitter hit. Tests at Crystal Semiconductor have shown that repeating a data pattern similiar to:

AA AA AA AA 33 33 33 33 33 33 33 03 00 03 00 03 hex

gives good correlation to the QRTS pattern. This pattern is considerably shorter than QRTS (which is 2^{20} - 1 bits long) so the strings of fourteen zeros occur often enough for a robust test of jitter tolerance at 51.4 kHz (the worst case jitter frequency for ones separated by 14 zeros). In addition, this pattern has sections of 50% ones, to avoid placing undue strain on the clock recovery circuit. This pattern can be modified or extended for testing different zero strings at different frequencies.

The maximum jitter frequency at which the HP 3785B operates is 77kHz, however 62411 specifies jitter performance to 100kHz. Generally, the jitter tolerance performance of a receiver will have flattened out by 77kHz, so one can assume that if the jitter tolerance curve has flattened out, and if it passes a difficult data pattern such as 2 in 16 at 77kHz, that it will also pass at 100kHz. Hewlett Packard does make a CCITT version of the HP 3785B, the HP 3785A, which can produce jitter to beyond 100kHz and is available with a T1 option.

A word of caution: not all jitter (and pattern) generators have enough jitter tolerance to recover jitter amplitudes as large as they can generate. A pattern generator's receiver which is looking for bit errors in a retransmitted (looped back) signal which has not been jitter attenuated may itself make errors in data recovery leading the tester to falsely believe that the equipment being tested is making errors. Many pattern generators (like the HP 3780A) have a provision for accepting recovered clock and NRZ data. A test configuration such as shown on the right hand side of Figure 1 is highly recommended for measuring jitter tolerance of equipment which does not provide jitter attenuation.

Output Jitter Measurements

The basic test setup is shown in Figure 2. The measurement looks at jitter in specific frequency bands:

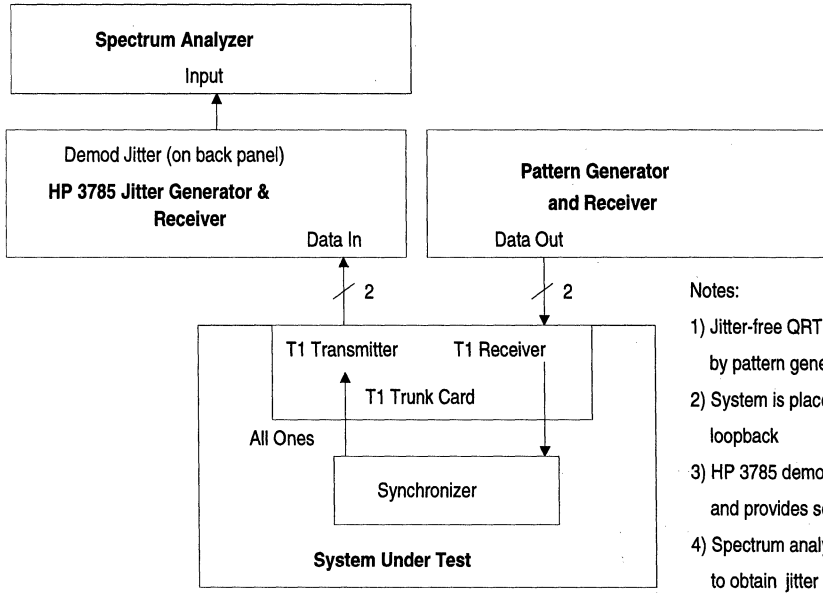
1) broadband; 0.05 UI,
2) using 10 Hz to 40 kHz filter; 0.025 UI,
3) using 8 kHz to 40 kHz filter; 0.025 UI, and
4) using 10 Hz to 8 kHz filter; 0.020 UI.

The first three of the frequency bands are selected using the filters available on the front panel of the HP 3785B. The output jitter levels are measured using the Received Jitter meter on the HP 3785B. For these measurements, the HP 3785B should be set to its "1" range which is its most sensitive scale. It is important to note that the HP 3785B's published accuracy is ±4% + (≤0.035 UI) for input data patterns, and ±4% + (≤0.025 UI) for input clocks.

Because the published accuracy of the instrument is not sufficient to measure to the small jitter levels required, it is advisable to do some sanity checks. Have the jitter receiver measure the jitter from the jitter free pattern generator. This will provide a "feel" for the HP 3785's measurement floor. It may be appropriate to subtract this result from subsequent measurements.

Furthermore, using an all ones data pattern will improve the instruments accuracy slightly (approaching that for input clocks). If the system under test has a transmit all ones capability, select this function for testing transmitted jitter. The transmit clock used in this case should be same as for normal operation or remote loopback.

Observing the DEMOD JITTER output (available from the back of the HP 3785) on a spectrum analyzer may also prove enlightening. While the sum of the jitter over a frequency band is not readily available, one can observe the jitter spectrum of the demodulated signal, look for jitter spikes ris-



Note: Measurement is much more accurate if All Ones are transmitted to the HP 3785 using the recovered clock.

Figure 2 - Test Setup for Output (Added) Jitter Measurements

ing out of the noise floor, and most importantly, compare the spectrum of the jitter free pattern's source to the transmitter's output, watching for artifacts that may be present in the source or created by the HP 3785 itself.

The HP 3785 does not have internal filters for measuring jitter from 10 Hz to 8 kHz, so measuring jitter in this band requires additional work. Obviously, if the jitter from 10 Hz to 40 kHz is less than 0.020 UI, so is the jitter from 10 Hz to 8 kHz. Jitter in the 10 Hz to 8 kHz band can be mathematically approximated by measuring the jitter in the band from 10 Hz to 40 kHz and jitter and the band from 8 kHz to 40 kHz by using Equation 2.

$$b=\sqrt{c^2-a^2} \qquad (2)$$

where

b = jitter from 10 Hz to 8 kHz
c = jitter from 10 Hz to 40 kHz, and
a = jitter from 8 kHz to 40 kHz.

Jitter in different bands will add as the sum of the squares. The most rigorous method is to build a band-pass filter which rolls off at 6dB / octave below 10 Hz and above 8 kHz. This filter is placed between the Demodulated Jitter Output and Measurement Input (both on the rear panel) of the HP 3785.

Jitter Transfer Measurements

The basic test setup is shown in Figure 3. The HP 3785B generates jitter at selected frequencies (the same frequencies at which jitter tolerance was measured, up to 32 kHz). The jitter amplitude that is input to the system should be 75% of the system's measured jitter tolerance.

Jitter attenuation is determined by comparing the amount of jitter in the signal output from the pattern generator (configuration "a") to the amount of jitter contained in the looped-back signal from the system under test (configuration "b"). The amount of jitter output from the jitter generator at each frequency should be 75% of the receiver's jitter tolerance at that frequency. The range scale used on the HP 3785 jitter receiver should be the same for both measurements.

When the input jitter is large (> 1 UI) *and* the output jitter from the system under test is greater than about 0.1 UI, the value shown on the Received Jitter display is sufficiently accurate. When the received jitter gets small (< 0.1 UI), it becomes necessary to use a spectrum analyzer to determine the jitter attenuation.

A spectrum analyzer must be used for two reasons. First, the accuracy of the jitter receiver is only ± 4% + (≤ 0.035 UI). Second, the value displayed by the jitter receiver is representative of the jitter over the selected bandwidth, not the jitter at the frequency being tested. Figure 4 shows a spectrum analysis display representing jitter attenuation. The upper curve shows the demodulated jitter present in the AMI data pattern output from the pattern generator. The lower curve shows the demodulated jitter present in the signal from the system under test. The attenuation is the difference in the amplitude of the two curves at the frequency of interest (shown at the top/center of the display).

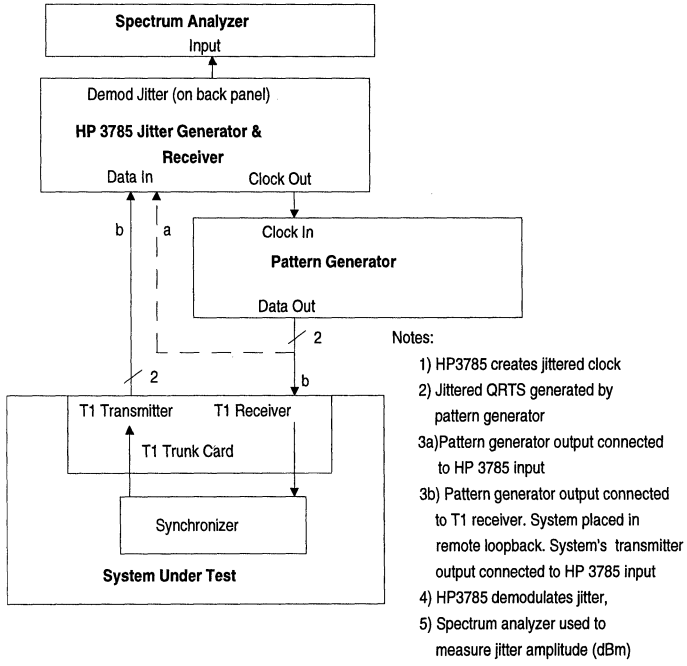


Figure 3 - Measuring Input and Output Jitter Amplitudes

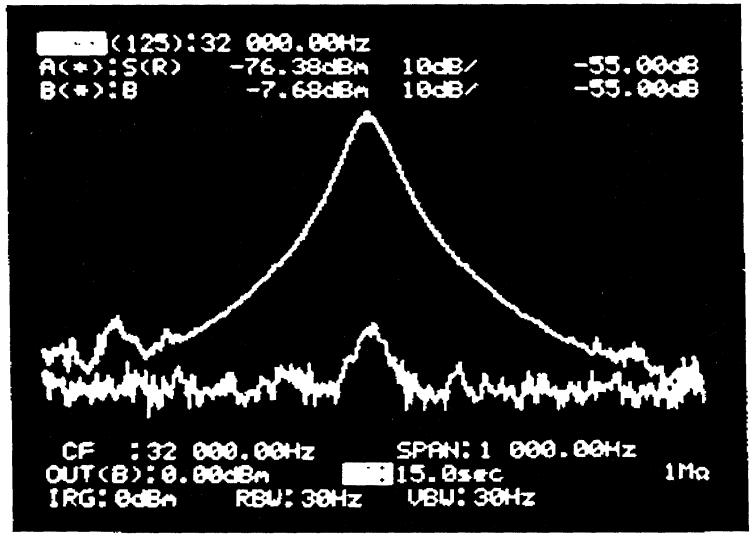


Figure 4 - Spectrum analyzer photograph showing 68.7dB of jitter attenuation at 32kHz.

Additional Considerations

When testing for compliance to 62411 it is often a good idea to expand the scope of some of the tests slightly to look for anomalous behavior of the system under test, and evaluate the robustness of the system's design. Here are some suggestions: Evaluate the system's performance as power supply and temperature are varied. ICs using external components (inductors, capacitors, and quartz crystals) may be particularly susceptable to temperature or supply variations.

It is prudent to check performance over the T1 frequency range allowed by the system. AT&T 62411 specifies a frequency tolerance of ±75Hz (±50 ppm). Some circuits will have sensitivity to frequency, and that sensitivity might be amplified by variations in temperature or supply. Verify that the frequency tolerance of the receiver exceeds ±50 ppm, and check for anomalous behavior of the jitter attenuator as the T1 frequency is varied.

Testing for frequency dependance generally requires a frequency source which can be set to within a few Hertz of a desired frequency. The HP 3780A Pattern Generator / Error Detector has an option which allows the user to adjust the output clock frequency with great accuracy to frequencies within 50ppm of 1.544MHz. This clock can be used to externally clock a jitter generator, another pattern generator, or to simply vary the frequency at which the HP 3780A outputs a data pattern.

Verify that the receiver will readily acquire lock on to a data stream which is presented while the receiver is in a "loss of signal" state. This test will show how well the receiver locks on to a T1 signal when it is first input, or recovers from momentary interruption in the signal. Also see if the receiver will false lock when initially presented with a data pattern with low ones density such as a 1 of 8 or 1 of 16 pattern. A good design should immediately lock on to any valid input signal, even one with low ones density.

When characterizing jitter transfer and generated jitter performance, it is wise to observe the output clock of the jitter attenuator in the time domain using an oscilloscope or a Frequency and Time Interval Analyzer like the HP 5372A. With a fast analog oscilloscope, this can be done by triggering the oscilloscope with the jitter free clock source, and observing edges of the jitter attenuated clock in the 1 ns to 5 ns time domain. Observations on a spectrum analyzer focus only on a narrow bandwidth. Anomalies created by the jitter attenuator that may appear at other frequencies would go unnoticed on the spectrum analyzer but the oscilloscope might indicate that more jitter is present. For example if input jitter of 0.3 UI is attenuated by 60dB, the output jitter should be 0.003 UI, which corresponds to about 2ns of time domain jitter. If the oscilloscope indicates something different, further investigation is warranted.

For loop-timed applications, it may also be important to evaluate the receiver's loss-of-signal, LOS, response. Check the receive circuit's LOS criteria: how many consecutive zeros, or how much pulse amplitude decay before LOS is declared? More importantly, test the circuit's recovered clock output. The recovered clock should smoothly transition to a reference clock when LOS is declared to ensure that no anomalies propagate to the system's backplane timing.

• Notes •

Application Note

AT&T 62411 Design Considerations - Jitter and Synchronization

By Bob Bridge and Greg Stearman

INTRODUCTION

This application note outlines the technical requirements which must be considered when designing a system to meet the AT&T 62411 synchronization and jitter requirements. The first section discusses how the digital network is synchronized. This section is followed by a discussion of the jitter/synchronization requirements for trunk cards and system clocks.

AT&T 62411 is the network interface specification which should be adhered to at the point of demarcation between the AT&T network and the customer premises location. It applies when connecting *CPE* (Customer Premises Equipment) to an AT&T 1.544 MHz access line or private line. Note that 62411 does not usually apply to equipment sold to telephone companies, equipment used internally to a campus environment or equipment used to access an alternative long-distance carrier (e.g., MCI, US Sprint, etc.).

AT&T 62411 has gone through numerous revisions (1983, 1985 and 1988) with the most recent version published in December, 1990.

SYNCHRONIZATION OF DIGITAL NETWORKS

The digital telephone network is synchronous. "Synchronous" implies that all T1 systems in the network are designed to operate at exactly the same average frequency (1.544 MHz ± 0 ppm). Synchronous operation is required so bits of information are not dropped as data is transfered between the various sinks and sources in the network. Imagine the problem that would occur in the codec of a digital telephone set if the codec were required to perform its A/D conversions and D/A conversions at different clock rates.

Synchronization is achieved via the hierarchical distribution of a Stratum 1 clock (Figure 1). Each carrier has one or more Stratum 1 clocks. The frequency of this master clock is distributed via various transmission media (optical cable, microwave radio and satellite) through a hierarchy of switching systems (toll, tandem and central-office switches) until it finally reaches the CPE. The CPE typically recovers the frequency of the incoming T1 line, and uses that frequency as the basis for its system clock and for retransmitting back toward the network. Typically, the network switching systems have Stratum 2 and 3

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clocks, and the customer system has Stratum 3 or 4 clocks. This overall timing plan is defined in ANSI T1.101-1987, Synchronization Interface Standard for Digital Networks.

The engineering of a network needs to ensure that the network will remain locked to a Stratum 1 frequency even upon the failure of one or more trunks that relay the timing information.

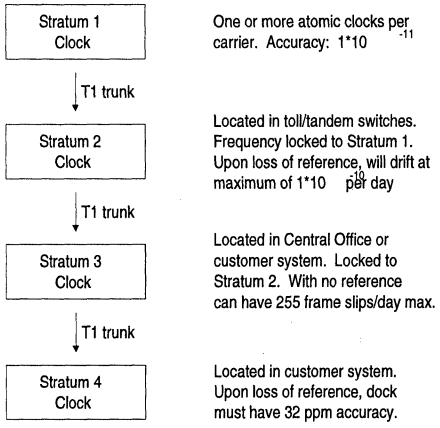


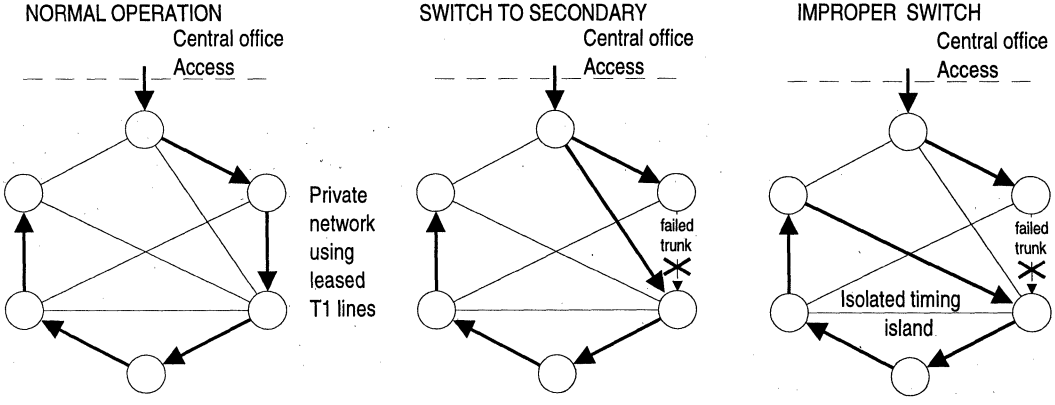
Figure 1 - Digital Timing Hierarchy

Figure 2 shows how a Stratum 1 traceable timing reference is passed through the T1 trunks of a private network. Upon failure of a trunk, a secondary path is used. Upon selection of an inappropriate secondary reference, an isolated timing island (with no master clock source) is created.

Figure 3 shows a typical system configuration where more than one trunk is used to input a traceable timing source into the system. Upon the failure of the primary timing source, a switch is made to a backup timing source. In the rare event that all timing sources fail, the system depends upon the ability of the synchronizer to free-run near the desired frequency.

To prevent chatter, it is important that there be hysteresis in the switch between reference sources. A switch should not be repeated any sooner than 10 seconds after the last switch, and only if one of the following conditions exists:

1) Phase hit of 1000 ns with phase slope $\leq 6.1 \times 10^{-5}$
2) Loss of signal (all zeros) for 0.10 seconds
3) 10^{-3} BER for ≥ 2.5 seconds
4) Excessive Input Jitter amplitude (Figure 8).



Stratum 1 tracable timing reference is transfered on trunks shown with bold lines.

Figure 2 - Multiple Paths to Stratum 1 Clock

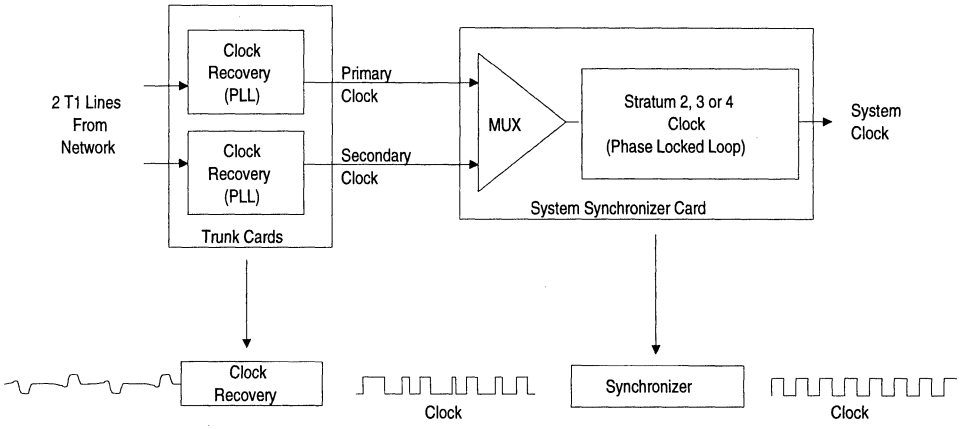


Figure 3 - Multiple Timing Sources Feeding a System Synchronizer

Synchronization plans for private networks can become, in practice, quite complicated. Figure 4 shows a multi-state private network with connections to multiple inter-exchange carriers, multiple local-exchange carriers and an international carrier. Also note that Bell South has trunks to three inter-exchange carriers. In this example, the PBX in Atlanta can be the timing source for the private lines to Long Beach. The Atlanta PBX gets its Stratum 1 traceable source from AT&T via Bell South. The PBX in Long Beach uses this AT&T timing to talk to Europe and to GTE of California.

CPE falls into one of two categories from a synchronization point of view. The CPE can either relay incoming timing to another downstream system, or it can terminate the timing chain. When a system terminates timing, failure of the system does not affect the timing of any downstream systems. This situation is refered to as *loop timing*.

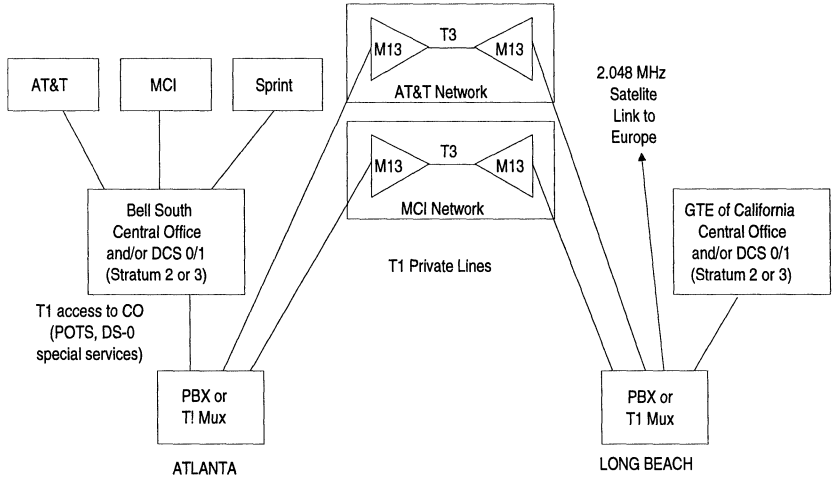


Figure 4 - Example of Private Network

A system synchronizer must meet a variety of requirements, including selecting a timing reference source to use, maintaining lock to that reference clock, tolerating impairments on the timing reference, attenuating jitter, and free-running at a specified frequency accuracy when all references are lost.

These requirements differ between systems that relay (or transfer) timing (Stratum 4 Type I, Stratum 3 or Stratum 2) and loop-timed systems (Stratum 4 Type II) that don't relay timing. In particular, in systems which relay timing, the maximum rate of change of the system synchronizer frequency must be limited (see definition of Maximum Time Interval Error in ANSI T1.101). Controlling the rate of change is important because if the synchronizer oscillates (i.e., overshoots then undershoots the target frequency) while acquiring lock or during degraded timing reference conditions, that frequency deviation can be relayed through all successive downstream systems.

An overview of Stratum requirements are given below:

Stratum 2: This is the highest performance level available to CPE, and is rarely used (except in very sophisticated CPE). The clock must have a free-running accuracy of 1,544,000 ± 0.025 Hz. Also a Stratum 2 clock must provide holdover to limit drift to no more than 0.0001 ppm from the last known reference frequency within 24 hours of the time the reference becomes unavailable. Redundancy is required so the synchronizer must be duplicated. The external reference clock must be Stratum 1 or 2 since the pull-in range of the synchronizer is only ± 0.05 Hz.

Stratum 3: Stratum three clocks must also be duplicated, and are required to have free-running accuracy of 1,544,000 ± 7.1 Hz. Stratum 3 requirements limit frequency drift during holdover to allow ≤255 DS1 frame slips in the first 24 hours. The external reference clock must be a Stratum 3 or better clock, since the pull in range is only ± 15 Hz.

Stratum 4 (Type I): This is normally the stratum level chosen for multi-T1 line CPE. Free-running frequency requirements are 1,544,000 ± 50 Hz, and the pull-in range is ± 100 Hz Additional pull-in range is recommended, since older equipment in the telephone company buildings are allowed to have output frequency variations of T1 ± 130 ppm (± 200 Hz). Type I does not require redundant clock hardware. However, just like Stratum 2 and 3 clocks, the Type I clock must gracefully handle rearrangements. "Gracefully" means that the rearrangements must not result in abrupt phase discontinuities in the output clock. Examples of rearrangements are:

1) a switching of timing reference (for example from T1 card "n" to card "n+1"),
2) automatic protection switch to a redundant synchronizer card, or
3) any change in clock mode

Stratum 4 (Type II): This is the lowest grade clock available, and normally would be used only in small systems (such as a single-T1 line system). Type II synchronizers cannot be used if the system transfers timing to a downstream system. The synchronizer clock output is required only during successful loop-timing. When loop-timing fails, the system no longer is required to transmit toward the network. There is no requirement on the synchronizer's free-running frequency. Nor is there any requirement to handle rearrangements. During loop-timing the frequency of the clock must be 1,544,000 ± 50 Hz. The pull-in range is 1,544,000 ± 100 Hz.

JITTER IN SYNCHRONOUS NETWORKS

Although the frequency of the T1 signal is well controlled (32 ppm), the signal itself can contain significant amount of jitter. *Jitter* is defined as a short-term variations in the position in time of a signal (or bit) from its ideal position. In other words, the bit could arrive at a receiver slightly sooner or later than expected. Jitter can cause bit errors or other impairments to occur. When jitter occurs at a 10 Hz or lower rate, it is arbitrarily defined as *wander*. Jitter and wander can be simultaneously present. Figure 5 shows high-frequency jitter superimposed upon low-frequency wander.

Due to the characteristics of the phase-lock loop technology used in trunk cards and system synchronizers, jitter can be more readily filtered than can wander (Figure 6). Normally, most wander which is input on a timing reference source will be relayed to all downstream systems.

A primary source of wander is frequency instability in a system synchronizer during a switch between timing reference sources. Why does the synchronizer need to switch between timing sources? One major source of errors is upstream clock rearrangement (typically two per day will reach Stratum 4 nodes). While acquiring lock to the new source, wander can be created and sent to all the downstream timing sources. Stratum 2 clocks can take hours/minutes to reacquire lock

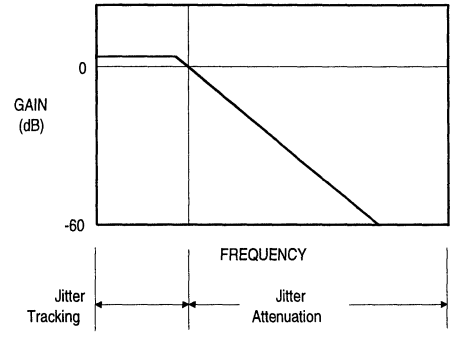


Figure 6 - Jitter Transfer of PLLs

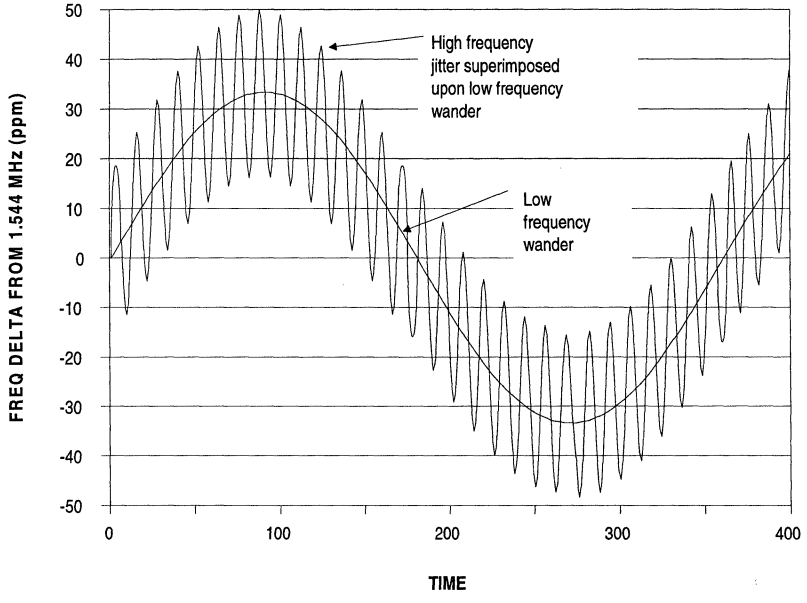


Figure 5 - Jitter Superimposed Upon Wander

after a switch. Stratum 4 clocks take seconds to reacquire lock. This wander can be amplified by each of the downstream synchronizers, causing an ever-larger wave-of-wander to spread out through the network.

The sources of jitter include data-dependent jitter introduced by line repeaters, jitter created by asynchronous multiplexors (such as M13 muxes) and jitter (phase) hits attributed to transient behavior of clock sources or other sudden changes in transmission facilities. Jitter is not a significant problem for equipment as long the trunk card and system synchronizer meets specificed jitter tolerance requirements.

62411 JITTER REQUIREMENTS

The motivation behind 62411 jitter specifications is to ensure robust operation of CPE and the network despite the presence of jitter. The CPE is at the end of a local loop (whose line repeaters can create jitter) and is far removed from the network's Stratum 1 clock. To work robustly, CPE must be extremely jitter tolerant, and must remove significant amounts of the jitter received over the local loop before re-transmitting back toward the network.

Before one can understand 62411 jitter requirements, it is necessary to understand some basic terminology (Figure 7). 62411 measurements are made at the NI (Network Interface) which is the demarcation line between CPE and the AT&T line. The *CSU* (Channel Service Unit) can be either a stand-alone unit (purchased from a CSU manufacturer), or may be integrated into the T1 trunk cards of the system. AT&T views the CSU and system as one entity for 62411 testing. Jitter generated or attenuated by either the CSU or the system will impact jitter testing at the NI.

From 62411's point of view, the system has two critical components, the *digital line termination of the DTE* (more commonly referred to as a T1 trunk card), and a *synchronizer (or clock recovery circuit)* (more commonly referred to as a

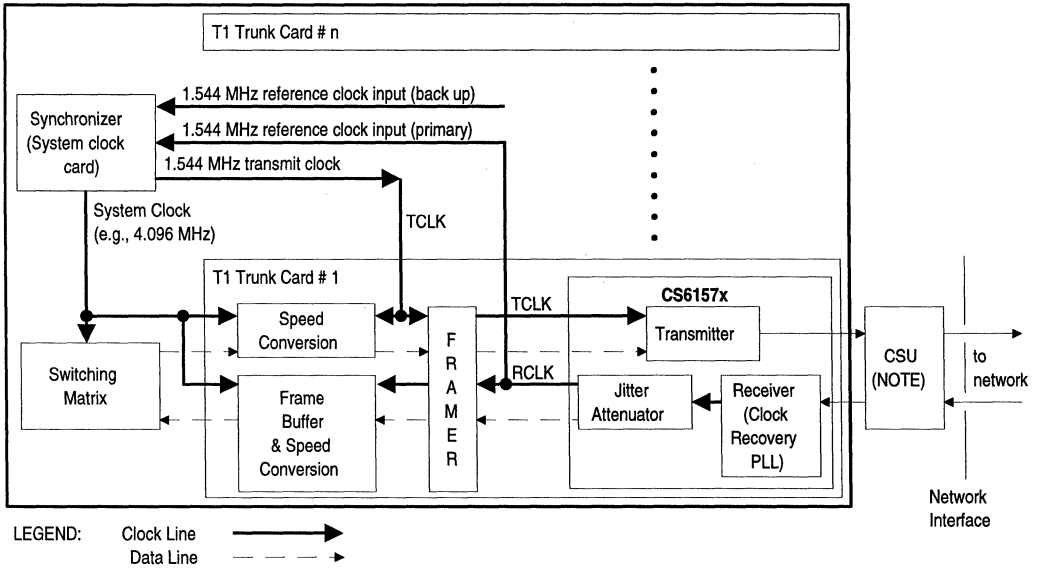


Figure 7 - Basic Terminology of 62411

system clock). 62411's use of the term "clock recovery circuit" should not cause the designer to think that 62411 is referring to a clock recovery circuit in a T1 trunk card. Rather the clock recovery circuit refers to the clock which drives the system and backplane. Typically the synchronizer outputs a system clock at 4.096 or 8.192 MHz and is phase locked to one of the incoming T1 lines. The assumption behind 62411 is that the synchronizer is the source of jitter attenuation. This assumption is generally appropriate unless the system has a 1.544 MHz backplane or only one T1 line. In this case the synchronizer may in fact not exist as a independent sub-circuit in the system, but rather may be imbedded in the T1 trunk card.

62411 has three types of jitter specifications: input jitter tolerance (also known as jitter accommodation), output jitter generation (also known as intrinsic jitter or additive jitter), and jitter transfer function (also known as jitter attenuation). The requirements for each specification are discussed below.

All 62411 jitter tests are made with a 2^{20}-1 QRTS (Quasi-Random Test Signal) modified to ensure that no more than 14 consecutive zeros are output. The Application Note, "Jitter Testing Procedures for compliance with AT&T 62411" gives a tutorial on test procedures.

Input Jitter Tolerance: Jitter tolerance is specified for both the T1 trunk card and for the synchronizer. In fact, the tolerance requirements are more stringent for the synchronizer than the line card. The more stringent specifications ensure that the synchronizer, which is a critical system element, is extremely robust. The tolerance curves are shown in Figure 8.

Tolerance is specified for jitter frequencies from DC to 100 kHz, and is normally measured at spot frequencies. At a given frequency, the jitter amplitude is increased until bit errors are observed.

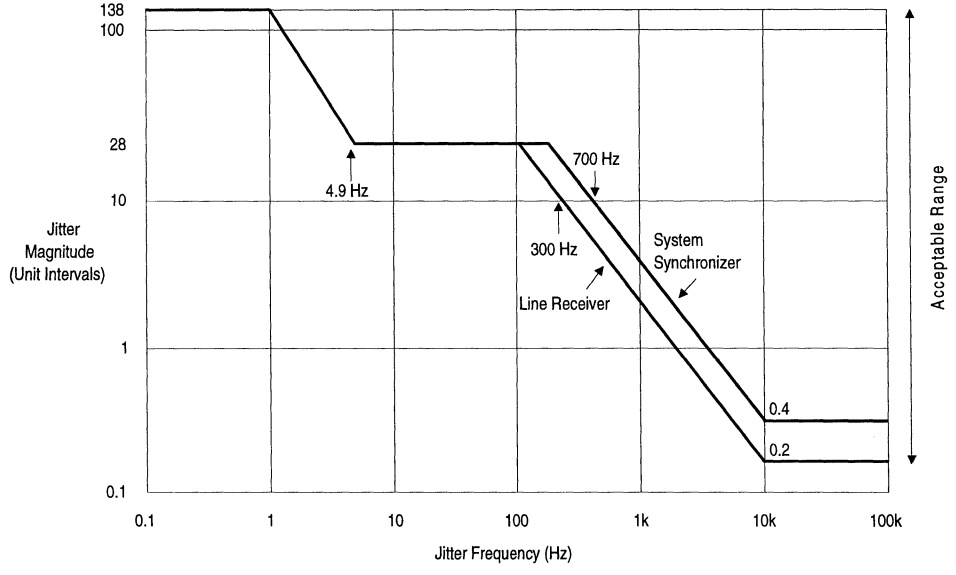


Figure 8 - 1990 AT&T 62411 Jitter Tolerance Requirement

The jitter tolerance of the synchronizer is relevant for all loop-timed systems. However, testing of the synchronizer is indirect since the synchronizer is not directly observable at the NI, and since the trunk card is not required to tolerate as much jitter amplitude as the synchronizer. Rather, the synchronizer is said to fail if loss of synchronization at the NI is observed, or if the system is observed to permanently switch to a back-up (internally-generated) clock. The switch to a back-up clock becomes apparent because of a shift to a new frequency (which may differ from the old frequency by only a few Hz).

62411 states that jitter (wander) tolerance at low frequencies can be limited by the size of a buffer. The required tolerance is one T1 frame (193 bits) plus hysteresis (138 bits). This model assumes that a frame buffer is being employed. Frame buffers allow a system to synchronize multiple, incoming, asynchronous T1 lines at the bit, channel and frame levels. Each incoming T1 line is fed into its own frame buffer (Figure 7). All of the frame buffers are emptied into the switching matrix with all frame bits aligned. If two incoming T1 lines have frequency offsets, one frame buffer will periodically output a frame twice (to compensate for a low input frequency) or will drop a frame (never outputing it to compensate for a high input frequency). This buffer adjustment is referred to as a *controlled frame slip*.

The 193 + 138 = 331 bit-length requirement applies to frame buffers making controlled frame slips. The goal is to have frame slips occur only as a result of long term frequency offsets, not due to jitter (wander). *However, only 138 bits are required in a jitter (hysteresis) buffer that does not perform frame slips.* In this case, the clock used to take data out of the buffer tracks the long term average input frequency so that the Jitter produced by modulating a QRTS with white noise bandlimited between 10Hz and 300Hz must be attenuated by 25dB when measured using an 8kHz to 40kHz filter. This performance is important. FIFO depth requirements are defined by the buffer length necessary to tolerate the jitter (wander) without overflow/underflow. The exact length needed to meet the requirements of Figure 8 depends upon the jitter transfer function of the PLL (Figure 6). The PLL will track jitter or wander at low frequencies, and only requires a FIFO long enough to contain the maximum input jitter amplitude possible in the jitter attenuation range.

Output Jitter Generation: Output jitter generation is a measurement of how much jitter is output by the system when no jitter is input to the system (using a QRTS). The requirements are measured using band-pass filters to measure jitter in various frequency bands, as shown below:

Filter applied	Maximum output jitter
None (Broadband)	0.05 UI peak-peak
10 Hz to 40 kHz	0.025 UI peak-peak
8 kHz to 40 kHz	0.025 UI peak-peak
10 Hz to 8 kHz	0.02 UI peak-peak

Jitter Transfer Function: Jitter transfer describes the ratio of input jitter and output jitter at a given jitter frequency using the following equation:

Jitter Transfer(dB) =
20 log (jitter output/jitter input)

The jitter input and output are measured in peak-to-peak UIs.

If a system contains a Stratum 4 clock, the jitter transfer function must meet the requirements of Figure 9. Figure 9 is irrelevant for systems with Stratum 2 or 3 clocks. Those clocks will attenuate jitter to the "output jitter generation" levels defined in the preceding section.

Since the system synchronizer has its basic frequency locked to the T1 rate of one particular

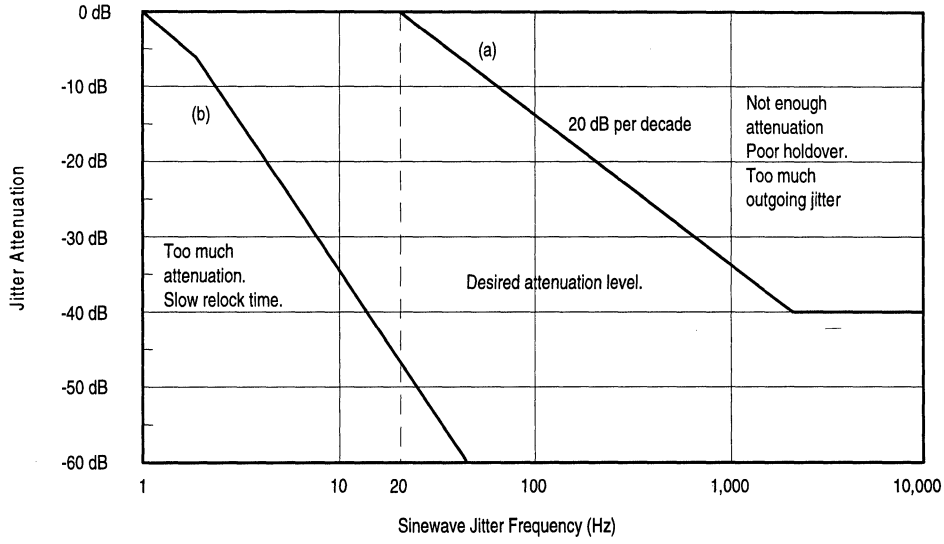


Figure 9 - 1990 AT&T 62411 Jitter Transfer Requirement

line card, the attenuation test is at the NI associated with that particular line card. QRTS input jitter is applied at spot frequencies in the band 10 Hz to 40 kHz. The input jitter level is three-quarters of the system's jitter tolerance. Output jitter is measured using narrow frequency windows (1 Hz in 10-100 Hz range, 4 Hz in 100-1000 Hz range and 10 Hz above 1kHz). Jitter Transfer must be between the two limits, (a) and (b), shown in Figure 9. In the vicinity of 10 kHz, the output jitter level, after attenuation, must typically be in the range of 0.001 to 0.002 UIs (or 0.65 to 1.3 ns).

The curve (b) indicates an attenuation level which must not be exceeded. Too much attenuation can be harmful. The negative effects can include increasing the number of frame slips that occur in the central office, and increasing the time needed to reacquire lock after a loss of signal condition.

Jitter peaking is not allowed above 10 Hz. Peaking is defined as a higher amplitude of output jitter than input jitter (at any frequency, not just at the frequency under test). Peaking is especially undesirable at low frequencies which lie within the tracking range (and not the attenuation range) of downstream PLLs. Analog PLLs can easily have peaking at the "knee" of the jitter transfer curve (just before attenuation starts).

In digitally controlled PLLs, another phenomenon, jitter aliasing, can often be observed. With jitter aliasing, jitter which appears at one frequency is attenuated and shifted to another frequency. Jitter aliasing is especially undesirable when the frequency is shifted down to the tracking range of the downstream PLLs. The 1990 version of 62411 has added language to address aliasing.

T1 TRUNK CARD DESIGN CONSIDERATIONS

A number of architectural choices face the trunk card designer. One is whether to integrate the CSU onto the trunk card.

Another design choice is whether to use a Line Interface IC that provides jitter attenuation. For Stratum 4 Type II systems that don't relay timing and utilize a 1.544 MHz backplane clock, the answer is simple. By using a CS61574, CS61574A, or CS61575 on the trunk card, the Type II clock is provided on the trunk card by the line interface RCLK output, and no separate synchronizer card needs to be designed. If the Type II system has multiple T1 lines, then the line interface IC's may be connected as shown in Figure 10. In this configuration, the master 1.544 MHz system clock is provided by the top CS61574A or CS61575 in the figure. The system clock will normally be recovered from the T1 line connected to the top line interface until the line interface enters the Loss of Signal state. Upon Loss of Signal (175 ±75 zeros), the CS61574A and CS61575 will substitute ACLKI (if present) for the recovered clock at the input of the jitter attenuator. The jitter attenuator filters any phase hits resulting from the switch before the clock is output on RCLK. In this configuration the RCLK output of the top line interface will always remain locked to one of the T1 recovered clocks. Each line interface that experiences Loss of Signal will pass on the recovered clock from the line interface preceeding it in the chain. When the master experiences Loss of Signal, the line interface nearest the master that is not in the Loss of Signal State will provide the 1.544 MHz system clock. If all line interfaces experience Loss of Signal, the reference clock is used instead. This configuration is advantageous for multi-line loop timed applications because it provides a jitter-free 1.544 MHz line recovered timing reference (ideally traceable to Stratum 1) even if there is only one functioning T1 line reference available. This capability helps to maximize the system's ability to successfully maintain loop timing on as many T1 lines possible.

However, for three reasons, the configuration shown in Figure 10 is not appropriate for systems which transfer timing (i.e., Stratum 4 Type I or Stratum 2 or 3). First, the CS61574A and CS61575 switch to a secondary reference clock upon Loss of Signal and not upon the conditions outlined in 62411 (summarized previously in the "Synchronization of Digital Networks" section) for systems that transfer timing. Furthermore, the CS61574A and CS61575 may not meet the maximum time interval error (MTIE ≤1µs) and phase change slope (81 ns in any 1.326 ms) requirements which apply during rearrangements. Systems which transfer timing must utilize a system synchronizer and the control circuitry requried to judiciously switch between reference sources, and the synchronizer's 1.544 MHz PLL is responsible for insuring the MTIE and phase slope requirements are met. Finally, the configuration in Figure 10 does not necessarily enforce a well defined network synchronization plan. Such a plan is essential in a network throughout which timing is transferred. A synchronization plan defines an appropriate manner in which timing rearrangements may be made without creating network timing problems such as self-locked timing islands (refer back to Figure 2). The configuration in Figure 10 will not necessarily prevent the fallback to an inappropriate timing reference (eg., a line already loop timed to

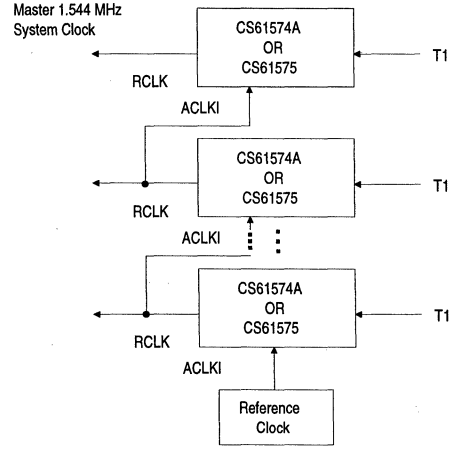


Figure 10 - Cross Coupling of Recovered Clocks (Stratum 4 Type II)

this node). Therefore, when using the configuration shown in Figure 10, it is important that there be a field-installable definition of how the chain is configured.

The use of a Line Interface IC with jitter attenuation also provides advantages for Stratum 4 Type I systems and Stratum 2 or 3 systems. By using a CS61574, CS61574A or CS61575 on the trunk card, the synchronizer becomes easier to design. Since the CS61574 exceeds jitter tolerance requirements and outputs an essentialy jitter-free recovered-clock, the synchronizer has reduced jitter tolerance requirements, and will see phase hits only when the switch is made between primary and secondary references. This frees the synchronizer designer to concentrate on meeting the holdover frequency, MTIE and reference switching criteria requirements.

SYSTEM CLOCK CARD DESIGN CONSIDERATIONS

As shown in Figure 7, the synchronizer provides the master clock for the system. It typically runs at a multiple of 8 kHz (the PCM frame rate), and generates a backplane clock at the rate of 2.048 MHz, 4.096 or 8.192 MHz.

A block diagram of a synchronizer is shown in Figure 11. This diagram shows multiple T1 lines being available as reference clocks for the synchronizer. A MUX is used to select one of the lines. The output of the MUX is fed through a CS61574 used only as jitter attenuator (accomplished by placing the CS61574 in local loop back mode). This jitter attenuation stage shields the 1.544 MHz Phase Locked Loop (PLL) from significant phase and frequency discontinuities

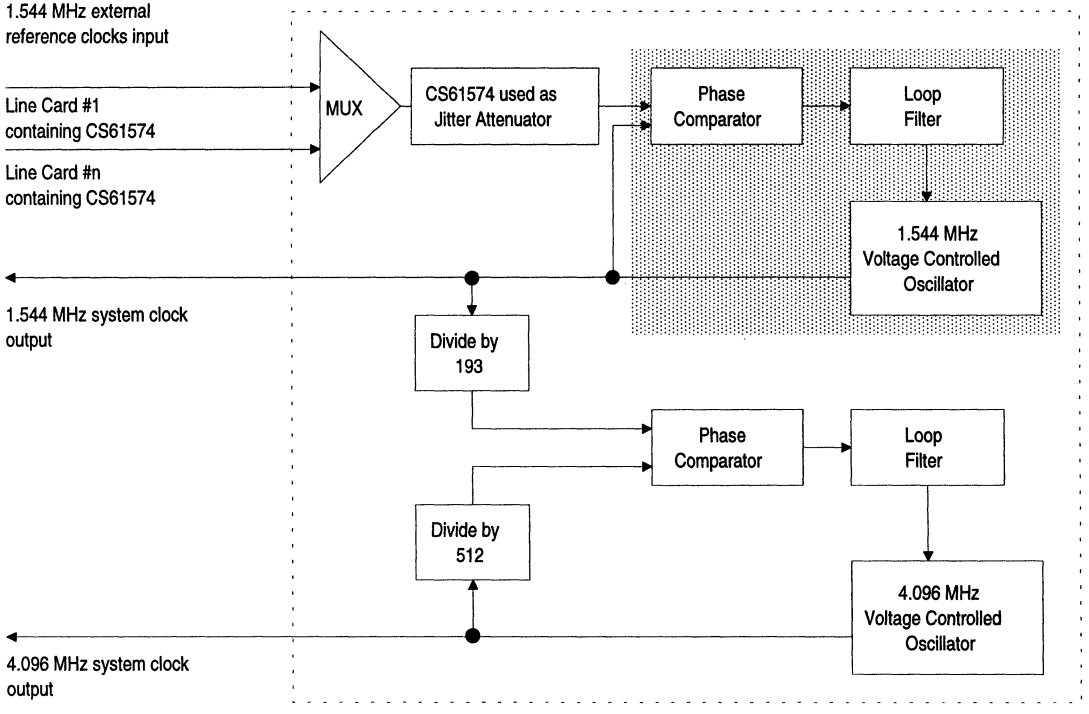


Figure 11 - Block Diagram of System Synchronizer

which can result from either the loss of signal on the active reference clock input, or the switching of the MUX. The 1.544 MHz PLL provides a clean 1.544 MHz output clock for transmitting back toward the network. The system backplane clock is also locked to the 1.544 MHz clock using a second PLL. This system backplane clock does not need to meet 62411 jitter transfer specifications, since it is not used to clock data back to the network (Figure 7).

The system synchronizer clock card design is greatly simplified in systems which employ CS61574's, CS61574A's or CS61575's on the T1 trunk cards. In such a system, jitter performance requirements (jitter transfer, jitter tolerance and intrinsic jitter) are met by the line interface IC. The 1.544 MHz PLL does not need to be designed with the narrow closed loop bandwidth required for 62411 (i.e., jitter attenuation starting at 6 Hz). Wider closed loop bandwidth simplifies the design of the PLL and promotes stability. For example, VCO (Voltage Controlled Oscillator) phase noise is suppressed in a system which has wider closed loop bandwidth. The fact that VCO stability is improved by wider closed loop bandwidth (feedback) means that it is often possible to use a VCO instead of a more expensive VCXO (Voltage Controlled Crystal Oscillator) in the 1.544 MHz synchronizer PLL of a Stratum 4 (Type I) system. VCXO based designs offer excellent stability even in low bandwidth applications and are recommended for use in Stratum 3 systems. Although the synchronizer does not need to be the primary source of jitter attenuation in a system utilizing line interface IC's with jitter attenuation, the synchronizer PLL should not exhibit jitter peaking (jitter gain). It is easier to design a PLL which does not exhibit jitter peaking when a significant amount of jitter attenuation is not required.

Not only does the use of a CS61575 based trunk card design relax the jitter performance constraints imposed on the synchronizer's 1.544 MHz PLL, but it also eliminates the holdover (free-running) frequency accuracy requirement. Because the CS61574A and CS61575 will gracefully transition from the line recovered clock to a reference clock upon Loss of Signal, the 1.544 MHz PLL will always have an appropriate timing reference to stay phase locked to and will never need to free-run. The holdover frequency accuracy of the system will be that of the 1.544 MHz reference clock supplied to the line interface IC's.

With the other design constraints greatly relaxed, the PLL may be designed specifically to meet the dynamic performance required by 62411. To do this, the PLL must be designed with adequate damping to meet the Maximum Time Interval Error (MTIE) and phase change slope requirements discussed earlier.

There are several types of components from which the synchronizer PLL's may be constructed. Monolithic PLL IC's like the 74HC4046A offer excellent performance and minimal circuit board space requirements. For more information on PLL design using the 74HC4046A, refer to (2) - (4). The free design program (3) offered by Signetics is an excellent tool for evaluating and optimizing a 74HC4046A PLL Design.

Recommended References on PLL design are:

1. Gerdner, Floyd M: Phaselock Techniques, John Wiley & Sons, New York, 1979. (ISBN: 0-471-04294-3)

2. Volgers, B.: "Phase-Locked Loop Circuits: 74HC/HCT4046A & 74HC/HCTR7046A HCMOS Designer's Guide", Signetics/Phillips Components. (Ordering Code: 98-2908-350)

3. Signetics/Phillips Components: HCMOS Phase-Locked-Loop Design Program . (For IBM compatible computers)

4. Austin, W. M.: "CMOS Phase-Locked-Loop Applications Using the CD54/74HC/HCT 7046A", ICAN - 8823, Harris Semiconductor.

• Notes •

Application Note

Secondary Line Protection for T1 and E1 Line Cards

Greg Stearman, Larry Stillings, & Roger Taylor

The lower cost of high speed digital T1 and E1 trunk lines has resulted in the increasing deployment of this technology in place of traditional analog lines. In the past, T1/E1 trunks were used primarily in protected telephone company central office transmission applications, but now they are used outside the central office to bring higher capacity service directly to customers. The broader application of this technology makes it important for line card designers to include secondary protection circuitry in their designs.

Line cards are exposed to a wide variety of electrical hazards through the transmission lines which connect them to the network. Even line cards installed on inside lines in a protected central office or customer premises environment are subject to line induced hazards capable of damaging line interface ICs. Line cards connected to outside lines are especially subject to the hazards of lightning surges and contact with AC power distribution facilities. The use of appropriate board-level secondary protection devices can dramatically improve the reliability and robustness of line cards in all applications.

This application note is organized into four major sections. The first is a description of the hazards line cards are exposed to through transmission lines. This section establishes the practical importance of protection circuitry. Presented next, is an overview of the major transient immunity and electrical safety standards which establish realistic immunity levels against these threats. Then, a comprehensive survey of the many transient protection devices now available helps explain which components are best suited to T1/E1 applications. Finally, three application circuits with line protection are presented along with explanation of how each responds to various faults.

LINE CARD THREATS

There are three general types of threats to which line cards are exposed: lightning surges, AC power faults, and improper installation or maintenance practices.

Lightning Surges

T1/E1 Line cards are exposed to lightning induced damage through surges coupled either through their transmission lines or through the AC power system. Although power supplies are often designed with excellent surge immunity, many line card designs do not provide adequate board level protection to prevent damage during lightning surges through transmission line connections. The type of line protection a card requires depends upon the nature of the lines it is connected to.

For outside lines, spark gap or gas tube primary protectors are installed at the network interface. Unfortunately, these devices will not limit voltages and currents to levels safe for semiconductor ICs on line cards. Primary protectors are only designed to limit voltages and currents below levels where premises wiring might ignite. Because of the way they are connected, primary protectors often compound the

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danger of surges on outside T1 lines. Typically, gas tubes or carbon block arrestors are installed on outside T1 lines between TIP to ground and RING to ground. A lightning surge will generate a longitudinal, or common-mode, transient on both TIP and RING conductors. Ideally, the longitudinal surge should not damage components on the card because the line coupling transformers will not pass a common mode signal. Unfortunately, the line coupling transformer's interwinding capacitance does couple fast transients across the transformer potentially damaging sensitive components. Also, the primary protection components will convert some of the longitudinal transient energy to a metallic transient because the two protectors on each TIP/RING pair breakdown asymmetrically. [2] When one of the primary protectors fails or limits at different potential than the other, a smaller metallic TIP to RING transient results. This smaller metallic transient will be coupled across the line transformers and may also damage sensitive components on the line card.

The primary protectors with the highest let-through energy are 3-mil carbon blocks. These devices have a maximum 3-sigma limiting voltage of 1 kV peak under transient conditions and 600 VRMS at 60 Hz. [17] In the event that one primary protector fails completely and the other does not, equipment on outside lines may be exposed to voltages within these limits and should provide adequate secondary protection to withstand them.

Intra-building T1 lines do not have primary protectors so they will not see metallic surges created by primary protector asymmetry. However, they may still be damaged by longitudinal surges coupled through the line transformer interwinding capacitance. (Note that Bellcore network equipment standards still require equipment on inside lines have immunity from low energy, metallic lightning surges so that secondary metallic protection is still necessary.)

AC Power Faults

AC power cross faults can occur because of the close proximity of telephone lines to AC power distribution lines on utility poles and in building wiring. Power cross faults result from direct contact between a T1 line and an AC power line. This type of fault can result in as much as 600 VAC across a T1 line. Unfortunately, in the past many designers of telecommunications equipment designed only for worst case power cross faults and overlooked the danger from low voltage power cross faults. Such designs typically used a large fuse (e.g., 1 Amp) in conjunction with a 200 V to 300 V voltage limiting device such as a Metal Oxide Varistor (MOV). [12] This type of interface will open the fuse providing protection for faults above the MOV breakdown voltage. However, during sustained faults below the MOV breakdown voltage, this design will allow steady state fault currents which result in component heating and a fire hazard. Adequate series current limiting protection should be provided to prevent fire and electrical safety hazards resulting from *all* power cross faults. Most electrical safety standards have been revised to include additional testing below the breakdown voltage of secondary shunt protectors.

Although AC power cross faults pose a more serious threat to telecom lines, AC power induction can impair performance also. Through electromagnetic coupling, currents in nearby AC power lines can induce long-term, common mode interference on telephone lines. [17] While digital T1 lines are less sensitive to this type of interference than analog subscriber lines, proper longitudinal balance is important in both applications. Secondary protection circuitry must be designed to maintain longitudinal balance.

Bellcore TR-EOP-000001 contains additional information and statistics on disturbances at the Network Interface (NI) due to lightning, AC power or RF transmission systems. [16]

Maintenance Related Hazards

Although line cards connected to inside lines may not be directly subjected to worst case lightning surge and power cross faults, they are susceptible to hazards associated with installation and general handling. Electrostatic discharge (ESD) can damage CMOS components on line cards, although most CMOS ICs now have internal protection which insures good ESD immunity. ESD damage can be prevented during maintenance or installation if grounded wrist straps and work surfaces are used. Also, twisted-pair cables should be discharged before they are connected to T1 equipment. Cables may become charged as they are "pulled" through building walls during installation. T1 equipment which uses a current source to provide span power can be damaged by the start-up transient which can result when a cable is connected to the port and current starts to flow.

Care should also be used to avoid the installation of a line card into the backplane of an operating system unless the card has been designed to allow this. Some line cards have an edge connector with long power and ground traces which will insure power is applied before other signals when the card is inserted into a live backplane. Cards which are not designed this way may present signals to CMOS ICs before power is established triggering SCR latchup. Crystal Semiconductor uses design and layout techniques to reduce susceptibility to SCR latch-up.

T1/E1 line cards can be damaged if they are incorrectly connected to analog telephone lines which carry ringing and battery voltages. Damage may also occur if line card output ports are shorted to each other or to ground. Crystal Semiconductor's newest generation of T1/E1 line interface ICs have transmitter short-circuit current limiting to help prevent damage during output shorts.

TRANSIENT IMMUNITY AND ELECTRICAL SAFETY STANDARDS

Transient immunity and electrical safety requirements for T1 equipment are defined in standards published by the United States Federal Communications Commission (FCC), Underwriters Laboratories (UL) and Bell Communications Research (Bellcore). In addition, standards bodies such as The American National Standards Institute (ANSI) and the Telecommunications Industry Association (TIA) play an active role in shaping revisions to these standards.

International standards published by the CCITT, ETSI and IEC together with country-specific standards establish the requirements for systems which are marketed in other countries. CCITT K.20, IEC-801-5 and ETS 300-046-1 outline some of these requirements for E1 systems.

The major surge immunity and electrical safety standards which apply to T1 equipment are FCC Part 68, UL 1459 and Bellcore TR-NWT-001089. Article 800-4 of the 1993 National Electric Code requires that telecommunications equipment be listed by a Nationally Recognized Testing Laboratory. [12] UL 1459, Second Edition, establishes the mandated electrical safety requirements for telecommunications equipment. This equipment must also be FCC Part 68 registered before it may be connected to the public network. [1] Part 68 establishes requirements to insure that equipment will not harm the network. Bellcore TR-NWT-001089 presents new guidelines that Regional Bell Operating Companies (RBOCs) *may* require for equipment they purchase or allow customers to connect to their networks. The requirements in TR-NWT-001089 are similar to but not identical to those in UL 1459 and Part 68. The following sections summarize the key requirements applicable to T1 equipment in each of these standards.

Bellcore TR-NWT-001089

Bellcore Technical Reference TR-NWT-001089, entitled "Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment", contains requirements for both inside and outside plant network equipment and customer premises equipment which will be used in a Regional Bell Operating Company (RBOC) network. This document consolidates Electromagnetic Compatibility (EMC) and safety requirements found in TR-NWT-000063, FR-NWT-000064 and TR-TSY-000499. In all future issues of these standards, EMC and safety criteria will be replaced by references to TR-NWT-001089.

Section	TR-NWT-001089 Requirement	Type:	Teleco Premises Outside Lines 1	Teleco Premises Inside Lines 2	Customer Premises Outside Lines 3	Customer Premises Inside Lines 4
2.4	ESD Immunity		X	X	X	X
3.2	EMI		X	X	X	X
4.5.3	NRTL Listing		X	X	X	X
4.5.4	Short-Circuit Test (Telecom Ports)		X		X	
4.5.6	First-Level Lightning Surge) Test (Telecom Ports)		X		X	
4.5.7	Second-Level Lightning Surge Test (Telecom Ports)		X		X	
4.5.8	Intra-Building Lightning Surge Test (Telecom Ports)		X	X	X	X
4.5.9	AC Lightning Surge Test (AC power Port)		X	X	X	X
4.5.10	Current Limiting Protector Test (Telecom Ports)		X		X	X
4.5.11	First-Level AC Power Fault Test (Telecom Ports)		X		X	
4.5.12	Second-Level AC Power Fault Test (Telecom Ports)		X			
4.5.13	Second-Level AC Power Fault Test Series Equipment (Telecom Ports)		X			
4.5.14	Second-Level AC Power Fault Test CPE (Telecom Ports)		X		X	
4.5.15	Second-Level Intra-Building AC Power Fault Test (Telecom Ports)					X
5	Steady State Power Induction		X		X	
6	DC Potential Difference		X		X	
7	Electrical Safety		X	X	X	X
8	Corrosion		X		X	
9	Bonding and Grounding		X	X	X	X

Table 1. TR-NWT-001089 Requirements vs. Equipment Type

Under TR-NWT-001089 telecommunications equipment is classified into one of four type categories based upon the nature of its connection to the network and intended operating environment. Table 1 summarizes the major requirements in TR-NWT-001089 which apply to each equipment type. The following sections summarize the lightning surge, AC power fault, current limiting protector, and short-circuit tests for telecommunications ports.

Lightning Immunity

TR-NWT-001089 has lightning immunity tests for equipment installed on inside lines only (type 2 or 4 systems) and tests for equipment installed on outside lines (type 1 or 3 systems). These tests use the standard double exponential surge waveform shown in Figure 1.

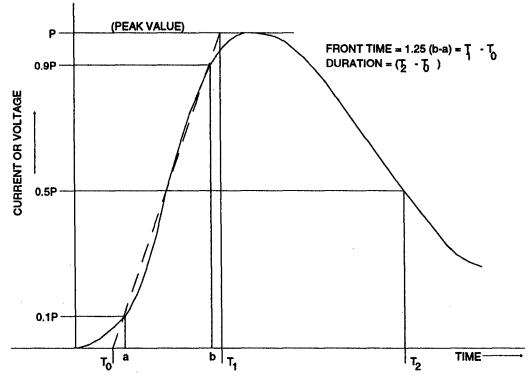


Figure 1. Double Exponential Surge Waveform

Equipment designed to connect to outside lines is subject to the first level longitudinal and metallic surge tests summarized in Table 2. After these tests the equipment must function correctly.

Surge	Min. Voltage[3] [Vpk]	Rise/ Decay Time [µs]	Min. Current [A]	Repetitions Each Polarity
1. L,M	±600	10/1000	100	25
2. L,M	±1000	10/360	100	25
3. L,M	±1000	10/1000	100	25
4. L	±2500	2/10	500	10
5. L	±1000	10/360	25	5

Notes:
1. L = Longitudinal Mode, M = Metallic Mode
2. Surge 3 is optional in place of Surges 1 and 2.
3. These tests are repeated at a voltage just below the operating threshold of any secondary protectors.
4. Primary protectors removed.

Table 2. TR-NWT-001089 First Level Lightning Surges

Upon completion of the first level test, the second level longitudinal surge test in Table 3 is conducted. After this test, the equipment may be damaged but must not pose a fire, fragmentation or electrical safety hazard.

Surge	Min. Voltage[3] [Vpk]	Rise/ Decay Time [µs]	Min. Current [A]	Repetitions Each Polarity
1. L	±5000	2/10	500	1

Notes:
1. L = Longitudinal Mode
2. Primary protectors removed.
3. Repeated at a voltage just below the operating threshold of any secondary voltage limiting device.

Table 3. TR-NWT-001089 Second Level Lightning Surges

Customer Premises Equipment (CPE) designed for use only on inside lines (i.e., type 4 equipment) is tested to the intra-building lightning immunity requirements in Table 4. To pass the intra-building lightning surge testing, the equipment must not be damaged. This test consists of a TIP/RING metallic surge of each polarity and a longitudinal surge of each polarity from TIP and RING to chassis ground.

Surge	Min. Voltage[3] [Vpk]	Rise/ Decay Time [µs]	Min. Current [A]	Repetitions Each Polarity
1. L,M	±800	2/10	100	1
2. L	±1500	2/10	100	1

Notes:
1. L = Longitudinal Mode, M = Metallic Mode
2. Primary protectors removed.
3. Repeated at a voltage just below the operating threshold of any secondary voltage limiting device.

Table 4. TR-NWT-001089 Intra-Building Lightning Surges

Current Limiting Protector Test

The current limiting protector test applies to equipment connected to outside lines (type 1 and 3 systems), and it is designed to verify that the equipment has a time vs. current fusing characteristic which will limit fault current enough to prevent it from becoming a fire hazard or igniting the building wiring. Fuse links are provided on outside lines which might come in contact with AC power lines, but these links are only designed to meet the current handling limitation of the carbon block primary protectors and not those of downstream network equipment and wiring.

A Bussman MDQ 1.6 Ampere fuse is used in the test to simulate the fusing characteristics of premises wiring. During the test a 60 Hz, 600 VAC source is applied differentially to the telecommunication ports for 15 minutes. If the 1.6 A fuse breaks or the equipment under test becomes a fire hazard, then it must be specified for use only with external current-limiting protectors. This protection is typically provided by a 350 mA heating coil installed between the equipment and the primary voltage-limiting protector.

Short Circuit Immunity

The equipment under test must not be damaged or require any manual intervention after 30 minutes of operation with: 1) TIP shorted to RING, 2) TIP shorted to ground with RING floating, 3) RING shorted to ground with TIP floating, or 4)

TIP and RING both grounded. Also, the equipment under test must not become a fire or electrical safety hazard as a result of this test.

AC Power Fault Immunity

TR-NWT-001089 includes telecom port AC power fault immunity tests for type 1, 3 and 4 equipment. Equipment which will interface to an outside line (types 1 and 3) is subject to the first and second level AC power fault tests, while CPE intended for use on inside lines (type 4 equipment) is subject to the second-level intra-building AC power fault test only. These tests demonstrate the safety of the equipment under power cross and power induction fault conditions.

The first level AC power fault tests (for telecom ports) are shown in Table 5. The equipment under test should not be damaged after these tests. Note that tests 1 - 3 are performed first at the indicated voltage then repeated at a lower voltage just below the operating threshold of any secondary voltage or current limiting protectors. This additional testing insure that the equipment under test will not become a fire hazard during sustained fault current at levels below the operating threshold of secondary protectors.

Test Config.[4]	Voltage[1] [VRMS]	Resistance [Ω]	Primary Protectors	Duration
1. L,M	50	150	Removed	15 min.
2. L,M	100	600	Removed	15 min.
3. L,M	200 400 600	600	Removed	60 times @ 1 sec. ea. Volt.
4. L[2]	1000	1000	Connected	60 times @ 1 sec.
5. L[3]	600	N/A	Removed	60 times @ 5 sec.

Notes:
1. All sources are 60 Hz sinusoidal. Tests 1-3 are repeated at a voltage just below the operating threshold of secondary protectors.
2. This test insures compatibility with the primary protection device when it operates.
3. This test simulates a high impedance induction fault.
4. M = Metallic Mode, L = Longitudinal Mode

Table 5. TR-NWT-001089 First Level AC Power Fault

The second level AC power fault tests for telecom ports on type 1 equipment are shown in Table 6. The equipment under test may be damaged after these tests, but must not become a fire, fragmentation or electrical safety hazard. Cheesecloth is applied to the unit to serve as a fire hazard indicator. For series (i.e. non-terminating) type 1 equipment, these test are applied to network-side connections with customer-side connections open-circuited and then short-circuited. Successful completion of UL1459 testing can establish conformance with all requirements except test 1 which must still be performed.

Test Config.[8]	Voltage[1] [VRMS]	Current[9] [A]	Duration
1. L,M	120 277	25	15 min.
2. L,M	600	60	5 sec.
3. L,M	600	7	5 sec.
4. L,M	100-600	2.2	15 min.
5. L	600	N/A	15 min.

Notes:
1. All sources are 60 Hz sinusoidal. Tests are repeated at a voltage just below the operating threshold of secondary protectors.
2. This test insures compatibility with the primary protection device when it operates.
3. Test 1 simulates secondary contact.
4. Test 2 simulates primary contact.
5. Test 3 simulates short-term fault induction.
6. Test 4 simulates long-term fault induction.
7. Test 5 simulates a high impedance induction fault.
8. M = Metallic Mode, L = Longitudinal Mode
9. Tests are repeated at a current just below the operating threshold of any current limiting protectors. Fuses are bypassed and current is set to 135% of the fuse rating.

Table 6. TR-NWT-001089 Second Level AC Power Fault Tests

The second level AC power fault tests for telecom ports on type 3 equipment are somewhat different. Fist a 300 VRMS, 60 Hz source is applied between all exposed conductive surfaces of the equipment and ground. To pass this part of the test current must remain below 20 A. Next, the 60 Hz sinusoidal source is applied in both longitudinal then metallic configurations to the telecom ports through a 20 Ω resistor (on each conductor) and a wiring simulator fuse (Bussman

MDQ 1.6 A or equivalent). The voltage is swept slowly from 30 VRMS (or lower if necessary to bring the current below 100 mA) to 600 VRMS. The equipment under test may not become a fire or electrical safety hazard during this test, and the wiring simulator fuse must not open (indicating ignition of premises wiring occurred). The equipment may fail open circuit. After an open circuit failure another identical unit is tested at 600 VRMS for 15 minutes and must satisfy the same set of requirements.

For series type 3 equipment, these test are applied to network-side connections with customer-side connections open-circuited and then short-circuited. The wiring simulator fuse is not used during the test with customer-side connections short-circuited.

For type 4 equipment, the second level intrabuilding power fault test consists of test 1, at 120 V only, in Table 6. The equipment must complete this test without become a fire or electrical safety hazard, but it may fail open-circuited.

FCC Part 68

FCC Part 68 registration is required for all customer premises telecommunications equipment which connects to the public network. The requirements in Part 68 are designed to protect the network from damage caused by poorly designed equipment. Unlike Bellcore TR-NWT-001089 and UL1459, Part 68 requirements do not focus on insuring that the equipment itself will not become a fire or electrical safety hazard. Part 68 requirements establish test guidelines on hazardous voltages and currents, signal power levels, line balance, and billing protection. [6] In addition, these requirements must be meet before and after environmental stress tests.

The tests for hazardous voltages and currents consist of a leakage test and a hazardous voltage test. The leakage test places a 60 Hz AC voltage from the TIP and RING connections of each T1 ports to exposed conductive surfaces, nonregistered equipment interfaces. This voltage is increased from 0 to 1000 VRMS in 30 seconds and sustained for 1 minute. At no time during the test is the current allowed to exceed 10 mA. This test is repeated with voltage increasing from 0 to 1500 VRMS between power supply primary leads and exposed conductive surfaces, power supply secondary leads, and nonregistered equipment interface ports. Leakage must again remain below 10 mA. Since these tests are intended to verify the dielectric strength of the T1 line and power supply isolation transformers, any secondary protectors which would operate during the tests should be removed.

The tests for hazardous voltages is designed to insure that the equipment will not expose the network to dangerous voltages. During this test, a 60 Hz, 120 VAC signal is applied to exposed conductive surfaces and nonregistered interface ground connections, and the voltage on TIP or RING must is not allowed to exceed 70 V for more than 1 second.

Table 7 summarizes the Part 68.302 lightning surge immunity requirements applicable to T1 equipment designed to interface to outside lines. The first surge is an 800 V 10/560 µs pulse applied between TIP and RING (i.e., in the metallic configuration). The second surge is a 1500 V 10/160 µs pulse applied from TIP and RING together then individually to ground (i.e., in the longitudinal configuration). For AC powered equipment, additional surges are specified between line and neutral connections of the AC

Surge	Min. Voltage3 [Vpk]	Rise/ Decay Time [µs]	Min. Current [A]	Repetitions Each Polarity
1., M	±800	10/560	100	2
2., L	±1500	10/160	200	2

Notes:
1. L = Longitudinal Mode, M = Metallic Mode
2. Primary protectors removed.

Table 7. FCC Part 68 Lightning Surges

line. Although Part 68 allows open-circuit failures (such as broken line fuses), the equipment should be designed to withstand these surges to insure reliable operation in all environments.

UL1459

UL 1459, Second Edition, establishes the safety requirements for telecommunications equipment mandated by the National Electrical Code. This standard is focused primarily upon fire and electrical shock hazards and includes guidelines on equipment enclosures, printed circuit board flammability, and user accessable voltages and currents. (Refer to [12] for an in depth overview of the requirements in UL 1459 - Second Edition.)

The overvoltage tests for telecommunication ports on outside lines are summarized in Table 8. These tests are applied in longitudinal and metallic configurations through a resistor and a fuse used to simulate premises wiring. As in the TR-NWT-001089 AC power fault tests, the equipment is allowed to fail open circuit as long as it does not become a fire or safety hazard.

For series type equipment (such as a CSU/DSU), longitudinal testing is conducted on the network port with the terminal equipment port open. Metallic testing is conducted on the network port with the terminal equipment port short circuited.

Test	Min. Voltage [VRMS]	Min. Current [A]	Duration
M-1, L-1	600	40	1.5 sec.
M-2, L-2	600	7	5 sec.
M-3, L-3	600[3]	2.2	30 min.
M-4, L-4	200[4]	2.2	30 min.
L-5	120	25	30 min.

Notes:
1. L = Longitudinal Mode, M = Metallic Mode
2. Primary protectors removed.
3. Test repeated with current set just below the interrupting current of any secondary current limiting devices.
4. Applicable to equipment with Voltage limiting devices operating between 200 - 600 V. Voltage adjusted below the operating threshold of the secondary Voltage limiting devices.

Table 8. UL1459 Overvoltage Tests

PROTECTION COMPONENTS

This section provides an overview of the wide variety of components typically used to provide line protection for communications equipment. A brief explanation of the operating principles, advantages and disadvantages of each component is provided in order to point out the devices best suited for T1/E1 line protection applications.

Metal Oxide Varistors

Metal oxide varistors, or MOVs, are devices made from a zinc oxide material whose resistance varies with terminal voltage. MOVs provide bipolar over-voltage clamping protection and are placed in parallel with the circuitry they are protecting. An MOV is selected by specifying its maximum operating voltage and breakdown voltage. [13] At and below the operating voltage, the MOV presents a very high impedance. However, when its terminal voltage reaches the positive (or negative) breakdown voltage, the MOV's impedance decreases dramatically limiting the voltage near the breakdown voltage.

MOVs are designed to handle large surge currents, and are commonly manufactured in a disk form factor with large cross-sectional area to reduce point current density. Its large cross-sectional area unfortunately gives the MOV a large parasitic capacitance of as much as 10 nF in some models. [11] The parasitic capacitance of an MOV is inversely proportional to clamping voltage. [11] These devices are fast acting (with response times of a few nanoseconds), but they have a finite lifetime and will gradually degrade (with a reduction in clamping voltage and increased leakage) when subjected to a number of transients. [11] MOVs must be derated when specified for operation with repetitive transients. [13]

MOVs are not designed for continuous currents because they exhibit a negative temperature coef-

ficient. The negative temperature coefficient can cause thermal runaway because as current flow heats the device its resistance decreases thereby increasing the current and further heating the device. Thermal runaway ultimately results in a short circuit failure of the device. For this reason, MOVs used to provide the low clamping voltages for board level secondary protection must be protected from the continuous current possible during an AC power cross fault. A fuse or PTC resistor can provide this overcurrent protection.

Although MOVs are commonly used in analog subscriber line applications because of their low cost and high surge handling capability, they are not suitable for use on digital T1 line cards because of their high parasitic capacitance.

Spark Gaps

The spark gap is another shunt (or parallel) protector which provides over-voltage limiting.

The spark gap consists of two movable electrodes separated by an air gap. A spark gap is specified by its breakdown voltage which is the potential difference between the plates just large enough to breakdown the air gap and trigger a spark across the gap. [11] The gap size is adjusted to control the breakdown voltage of the device which is typically several hundred Volts. When the voltage across the gap is below the breakdown voltage the device presents a high impedance between its terminals. Once the terminal voltage exceeds the breakdown voltage the arc which results across the terminals creates a low impedance path for current which persists until the current falls below the minimum extinguishing current level. During operation in the arc regime, the voltage across the spark gap is limited at just above the breakdown voltage.

The carbon block arrestor is inexpensive and has fast response time, but also has significant disadvantages. It must be replaced after handling a high energy transient because of electrode erosion which widens the gap and significantly increases the firing voltage leaving downstream circuitry unprotected. [11] Also, the accumulation of carbon dust between the electrodes after conduction eventually leads to erratic operation.

Because spark gaps provide clamping at high voltages and handle high currents, they are used as primary protection devices rather than board level secondary protectors.

Gas Filled Surge Arrestors

Gas filled arrestors, commonly called gas tubes, are devices which incorporate electrodes inside a sealed glass or ceramic package filled with a noble gas. Gas filled arrestors are parallel over-voltage protectors based on the same principle as the spark gap without the mechanical instability and contamination problems common in air gap devices. Since these arrestors can fail as an open circuit, some gas tube devices also include a parallel air gap for backup protection.

Gas filled protectors are specified by: DC firing voltage, surge firing voltage, arc extinguishing voltage, max. terminal voltage (during an arc), and max. surge current. [13]

The DC firing voltage is the voltage required to trigger an arc in response to a slowly increasing gap voltage (typically 75 V to 300 V specified at dv/dt = 500 V/s). Since the gas in the gap requires time to ionize, the breakdown voltage increases for signals with faster rise times. [13] Often, the surge firing voltage (typically specified at dv/dt = 1000 V/µS) is several times higher than the DC firing voltage. However the response time also decreases for signals with faster rise times. Both of these factors determine how much transient energy is allowed to pass through a gas tube. For signals with slow rise times the tube will conduct within microseconds after the DC firing voltage is reached. For sig-

nals with fast rise times the tube will conduct within nanoseconds after the DC firing voltage is reached, however the fast rise time can allow the signal to reach several times the DC firing voltage in a few nanoseconds. [11] To specify a gas tube that will provide effective transient protection it is necessary to know the magnitude and rise time of the transients it must suppress.

Once a gas tube begins conduction in the arc regime, the voltage drop across the device is typically between 10 V to 30 V. Conduction will continue until the voltage falls below the minimum extinguishing voltage (typically 60% to 70% of the DC firing voltage). [13] If sufficient current (as little as 10 µA for some devices) is available the gas tube can continue to operate in the glow regime with between 50 V to 100 V across its terminals. [11] It is important that the signal fall below this voltage after a transient to extinguish this follow current. In T1/E1 applications the 3 V AMI encoded signal will not sustain follow current, although follow current is a problem in AC power line protection applications.

Gas tube arrestors have high surge current handling capability (e.g., 15 kA for an 8/20 µS waveform), but the large current increase that occurs when the device goes from the insulating to the conducting state can produce a great deal of radiated energy potentially upsetting other system components. [11]

Gas tube arrestors have the lowest capacitance of the common shunt type protection devices which makes them ideal for use as primary protectors in T1 and higher rate digital communications applications. These devices are often used as primary protectors because of their high breakdown voltages (at least 60 to 100 V) and large surge handling capability, but some models are suitable for use as board level secondary protectors.

Like MOVs, gas tubes require current limiting protection in communications applications which are exposed to AC power cross faults. When subjected to a power cross fault, the gas arrestor can get very hot and become permanently damaged. The hot expanding gas inside can break the package seal letting the gas escape and dramatically increasing the firing voltage. In some cases, the hot gas can even shatter the case.

Fuses

Fuses have traditionally been used for inexpensive, non-resettable series overcurrent protection in telecom applications. A fuse consists of a conductive element of precise length, diameter and composition designed to melt when subjected to a specified current flow for a specified period of time. [3] For North American T1 applications, UL listed/CSA certified fuses (commonly in a 1/4" x 1/4" cylindrical glass tube package) are used. For European applications, VDE and/or SEMKO certified fuses (commonly in a 5mm x 20mm package) are required. However, both types of fuses are available in other packages. For example, the TR5 and TE5 fuses from Wickmann USA use a small, sealed plastic package making them suitable for automated wave soldering and cleaning procedures. Because the parts are pin-compatible, one PCB layout can support the UL/CSA approved TR5 and the VDE/SEMKO certified TE5.

Fuses are specified by: an operating current rating, breaking capacity rating, maximum voltage rating, and a fusing time characteristic. [3]

The operating current rating defines the maximum current at which the fuse element is stable over time. Operating current must be derated for operation at high ambient temperatures. The fuse element has a small finite resistance (less than 0.1 Ω) below its rated current and exhibits a positive temperature coefficient. A current larger than the rated current causes the element tem-

perature to increase in turn causing the resistance to increase and thereby increasing the temperature until the element melts. Once the element melts, an arc forms between the broken ends of the element dissipating power and melting back the element ends further. Ultimately the arc is extinguished when the broken ends melt apart and the voltage can no longer breakdown the air gap to sustain the arc. The breaking capacity or interrupting rating is the maximum short-circuit current which causes the fuse to break without sustaining conduction through an arc. [3] High breaking capacity fuses often use an internal arc extinguishing medium which has a higher breakdown voltage than an air gap. Low breaking capacity fuses are filled with air and rely on the air gap formed when the element melts to extinguish the arc.

The maximum voltage rating defines the maximum voltage drop across the fuse once the element is broken that will not cause an arc to form allowing a high fault current to flow. [3]

The maximum voltage and breaking current ratings define the maximum thermal energy that a fuse can safely dissipate without becoming a fire or fragmentation hazard. [3] It is important to insure that the maximum energy rating (which is the product of maximum voltage rating, maximum current and maximum time) will not be exceeded in the intended application to insure that the fuse fails safely.

The fusing characteristic defines the energy required to melt the fuse element and extinguish the resulting arc. This relationship is often presented graphically as a time vs. current characteristic curve. The fusing time is also expressed in data sheets at a multiple of the rated operating current for a specified time (e.g., 200% of the rated current for 1 second). UL 198G classifies fusing time characteristics into two categories: time delay and non time delay. Time delay, or slow-acting, fuses are designed for applications where the fuse must remain intact during power-on inrush current surges or short duration transients.

In telecommunications applications, a fuse must be selected based upon both its ability to withstand lightning surges and its ability to open circuit quickly during an AC power cross fault before other components fail and create a fire or electrical safety hazard. Time delay fuses are often required to satisfy these two conflicting requirements. Series resistors are often used with fuses to provide additional current limiting to protect the fuse during surges.

Hybrid Resistor/Fuse Devices

The LFR-2 manufactured by IRC, Inc. is a combination series resistor and thermal fuse in one package that offers a unique solution to achieve the conflicting requirements to withstand lightning surges and still open quickly during AC power faults.

The resistor/thermal fuse is specified by: the resistance value, fusing time characteristic, and maximum surge voltage rating.

This device combines a precision resistor with a thermal fuse in an inorganic flameproof package. The internal series resistor provides surge current limiting giving the device the ability to withstand a lightning surge, and it melts quickly and safely under worst case 600 VAC power cross faults like a fuse element. The thermal fuse provides protection during sustained, low current power cross faults by opening as soon as the resistor temperature reaches 184 °C. It is this unique ability to provide protection during sustained low current faults and still tolerate lightning surges that makes the thermal fuse and resistor combination especially attractive in telecommunications applications. In order to provide this level of low voltage power cross protection using a conventional fuse, the fuse current rating would have to be so low that it couldn't withstand lightning surges. Unfortu-

nately, the LFR-2 is non-resettable and more expensive than conventional fuses, but it provides the kind of protection which is required for telecom equipment connected to outside lines and subject to both lightning and AC power cross.

PTC Resistors

PTCs are positive temperature coefficient resistors which are also used as series current limiting protectors. In normal operation, the PTC exhibits a low resistance, but when the current dramatically increases the PTC heats up and its resistance increases sharply, limiting the fault current. When the fault is removed the device cools and resets allowing the protected circuit to operate normally. Conductive polymer PTCs which can safely handle both lightning surges and AC power cross faults are available from companies such as Raychem, but these devices will typically be stressed beyond resettability by worst case UL1459 power cross tests. [9] PTCs are well suited to use on 600 Ω lines to provide current limiting under power cross fault conditions, but their series resistance (typically 10 to 15 Ω) results in significant signal attenuation especially at high temperatures in 100 Ω T1 systems. These devices also exhibit increased resistance after they reset.

Transformers

T1/E1 systems uses transformer coupling to provide isolation on the transmision line connections. Transformers pass differential AC signals and reject common mode signals. In additional to signal coupling, transformers also provide both metallic and common mode transient protection.

The transformers commonly used in T1/E1 applications provide between 1500 V to 3000 V of primary to secondary high potential isolation. These transformers also have limited bandwidth and energy handling characteristics which prevents them from coupling fast metallic transients. The transformer's bandwidth is limited by the primary & secondary coil inductances which are typically about 1 mH. Also the characteristics of the magnetic core determine how much energy the device can couple without saturating. The ET constant or Volt-microsecond rating defines the onset of core saturation. A transformer will no longer effectively couple energy at approximately 1.5 to 2 times this rating. ET constants of 15 V-µs are typical of T1/E1 line transformers. Once saturated, the transformer presents a low differential impedance on the line. The dominant mechanism available for coupling fast transients is the winding to winding capacitance (typically 30 pF) from primary to secondary.

Schottky Diodes

Schottky diodes provide very low forward clamping voltages making them ideal for use in clamping line I/O pins on CMOS ICs. A Schottky diode is formed by creating a junction between a metal like Aluminum and an n-type semiconductor material. The resulting junction exhibits rectification like a p-n junction but with only half the voltage drop. In addition, the Schottky diode is capable of faster switching because there are no minority carriers which must recombine as in a p-n junction.

The low forward voltage and fast switching time enable external Schottky diodes to clamp IC pins before the IC's internal silicon protection diode structures turn on and sustain damage. Since Schottky diodes have low junction capacitances, they are well suited to protect T1/E1 and higher bandwidth signals. These devices have limited power handling capacity but are well suited to absorb the potentially damaging let-through energy from other secondary protectors such transformers and silicon transient suppressors.

Avalanche and Zener Diodes

Silicon diodes optimized for surge current handling rather than voltage regulation make very effective transient suppressors. These devices use avalanche and/or zener reverse breakdown mechanisms to provide parallel overvoltage limiting protection. Although both mechanisms may be used in some of the lower breakdown voltage devices, these parts are commonly called avalanche transient voltage suppressors (TVS). [11] Avalanche diodes are designed with large cross-sectional area and internal heat sinks to increase surge current handling capability. [13] Avalanche suppressors provide low clamping voltages (as low as 5 V) and have excellent reliability when operated within specifications.

Avalanche diodes are specified by: reverse breakdown voltage, reverse stand-off voltage, max. clamping voltage, reverse leakage current, shunt capacitance, peak pulse current and power, and response time. [13]

For bipolar overvoltage clamping, two of these devices may be connected anode to anode in series across the circuit they are to protect. For applications like T1/E1 line protection which are sensitive to shunt capacitance, an avalanche diode (e.g., Semtech SMBJ6.5) can be connected anode to anode in series with a low-capacitance diode (e.g., Semtech SS8198) to minimize the total capacitance. This configuration only provides unipolar clamping so another pair connected in parallel with opposite polarity across the line is required for bipolar protection. Low capacitance avalanche protectors like the Semtech LC01 and Protek Devices use this technique to achieve capacitances of 50 pF.

Low breakdown voltage avalanche suppressors with low capacitance and low leakage are commonly used as secondary board level protectors in T1/E1 line card applications.

Thyristor Crowbar Devices

The self triggered triac, or sidac, is another highly effective type of bidirectional parallel overvoltage protector. These devices are constructed with a triac whose gate is controlled by back-to-back avalanche diodes. A voltage transient is initially limited by the avalanche breakdown characteristic of the diodes until the device current becomes large enough to turn on the triac. Once the triac is turned on, it is able to sink very large transient currents while clamping the voltage across the device typically within 2 or 3 V. The triac's low clamping voltage allows it to sink large currents while minimizing power dissipation. As the transient subsides, the current decreases below the minimum holding current and the device returns to the high impedance blocking state. Unlike a gas tube protector, the breakover voltage of a sidac does not vary with the surge current magnitude and rise time (dv/dt) of the voltage transient. [4] These devices are available with breakdown voltages ranging from 30 to 600 V. The Sidactor manufactured by Teccor Electronics and the Surgector manufactured by Harris offer excellent power handling capability, fast response time and low off-state capacitance which makes them attractive for T1/E1 applications.

T1/E1 LINE PROTECTION CIRCUITS

This section illustrates how to implement transmission line protection for both inside and outside line applications with Crystal Semiconductor T1/E1 line interface ICs. These circuits are designed to limit voltages and currents on the transmission line input and output pins of the line interface IC within data sheet absolute maximum ratings.

T1, Outside Line Protection Circuit

The schematic in Figure 2 shows a T1 applications circuit for use on outside lines. This type of line protection may be used in customer premises equipment (such as a Channel Service Unit) or telephone company equipment on ports which connect directly to metallic, outside plant lines. (Note that the CS61577 requires additional receiver equalization and transmitter line build-out components not shown here for ANSI T1.403 network interface applications with carrier provided T1 lines.)

This circuit is designed to provide the lightning surge and power cross immunity required by UL 1459 - Second Edition, FCC Part 68 and Bellcore TR-NWT-001089.

During the metallic lightning surges required by Part 68 and TR-NWT-001089, this circuit provides current and voltage limiting. TVS2 and TVS3 are LC01 low capacitance, bi-directional avalanche TVS devices from Semtech. These devices were chosen because of their 1500 W (10 x 1000 µs) peak pulse power rating and maximum clamping voltage of 16 V.

To protect the line interface IC from the energy which is coupled through the transformer, additional current or voltage limiting is provided on the line input and output pins of the IC. On the receiver RTIP and RRING pins, the 470 Ω series resistors R1 and R2 are used for surge current limiting. The use of series resistors will not reduce the receiver input signal amplitude in normal operation because the RTIP and RRING pins are high impedance inputs (> 20 kΩ). During an overvoltage on these inputs, the internal protection diodes will clamp the input a diode drop above the + 5 V supply rail and the 470 Ω resistor will limit current at a safe level. R3 and R4 are 200 Ω resistors which provide the line side termination of 100 Ω.

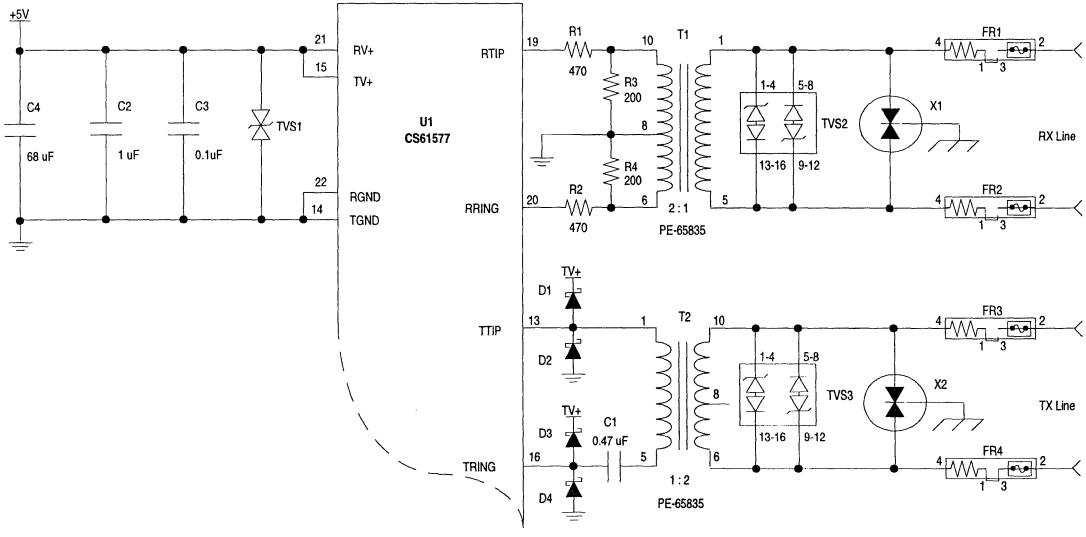
On the transmitter output pins another approach is required since a large series resistor will attenuate the signal too much to meet the output pulse template specifications. On the TTIP and TRING output pins, Schottky diode clamps composed of D1 - D4 are used to limit these pins within approximately 300 mV of the +5 V supply and ground. Schottky diodes were chosen because their fast response time and low forward voltage will enable them to protect before the line interface ICs internal protection diodes breakdown. The 11DQ04 Schottky diodes specified will easily handle the surge currents and voltages passed through TVS2 or TVS3 and the transformers. These diodes also have low shunt capacitance which insures that they will not distort the transmitter output pulse shape.

During longitudinal (common mode) lightning surges to ground below 2500 V, this circuit takes advantage of the isolation provided by the line transformers to prevent damage without clamping. Since the line side of each transformers is floating relative to chassis ground, it is not necessary to provide common-mode clamping protection for longitudinal surges below the high potential isolation rating of the line transformers. In practice, longitudinal surges should be limited to 1000 Vpk by the primary protectors which are installed on outside lines. However, the TR-NWT-001089 second level lightning surge tests require the system under test safely handle longitudinal surges of 5000 Vpk, although they do allow it to stop functioning. The transformers

specified here are rated for high potential isolation of 3000 VRMS (at 60 Hz). The gas tubes X1 and X2 are provided to insure the transformer isolation rating is not exceeded during the 5000 Vpk second level lightning surge test in TR-NWT-001089. X1 and X2 have a surge firing voltage above 2500 V and below 3000 V so that they will not fire during the first level surge tests, but will fire during the second level test. When X1 and X2 fire, the resulting surge current will quickly open the fuse/resistors FR1 and FR2 and the circuit will fail safely.

FR1 and FR2 are 5.6 Ω LFR-2 integrated thermal fuse/resistor devices from IRC, Inc. which provide series current limiting protection during AC power cross faults. These devices are rated to handle the metallic surges in FCC Part 68 and TR-NWT-001089 without fusing. Their series resistance provides transient current limiting to protect the fuses during a lightning surge and increases the impedance TVS2 and TVS3 place across the primary protectors allowing the primary protectors to shunt most of the surge current.

TVS1 is an SM05 bi-directional, 5 V transient voltage suppressor from Semtech which is used to clamp surges coupled onto the power supply by the Schottky diodes D1-D4.



Component	Description	Part #	Manufacturer
TVS1	5 V, bi-directional TVS	SM05	Semtech
TVS2, TVS3	6 V, bi-directional, low capacitance TVS	LC01	Semtech
X1, X2	2800 V gas discharge tube		
FR1 - FR4	5.6 Ω thermal fuse/resistor	LFR-2-5.6-1	IRC, Inc.
D1 - D4	Schottky diode	11DQ04	International Rectifier

Figure 2. T1, Outside Line Protection Circuit.

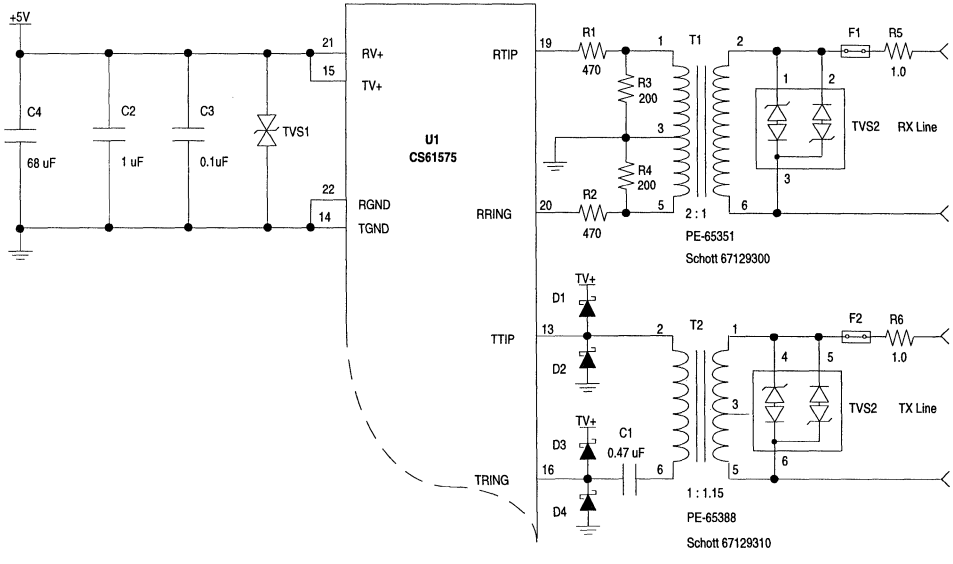
T1, Inside Line Protection Circuit

The schematic in Figure 3 shows a T1, DSX-1 applications circuit for inside lines. This type of line protection may be used in customer premises equipment or telephone company equipment on ports which connect only to intra-building, metallic lines.

This circuit is designed to provide the intra-building lightning surge and 120 VAC power cross immunity required by Bellcore TR-NWT-001089.

This circuit provides current and voltage limiting for the TR-NWT-001089 metallic lightning surges. TVS2 is a low capacitance, avalanche TVS array from Protek Devices. This device contains two 12 V, bi-directional protectors rated to handle the 2 x 10 µs, 100A peak surge current required.

On both transmit and receive lines, time delay fuses, F1 and F2 provide the 120 V intra-building AC power cross protection required for customer premises equipment. The 1 Ω series resistors R5 and R6 provide surge current limiting to protect the fuses during a lightning surge.



Component	Description	Part #	Manufacturer
TVS1	5 V, bi-directional TVS	SM05	Semtech
TVS2	12 V, bi-directional, low capacitance TVS	VSB06P12LC	Protek Devices
R5, R6	1.0 Ω, 2 W resistor		
F1 - F2	1.0 A time delay fuse	1.0A TR5-T	Wickmann USA
D1 - D4	Schottky diode	11DQ04	International Rectifier

Figure 3. T1, Inside Line Protection Circuit.

Since there is no chassis ground reference on the secondary (line side) of either the transmit or receive lines, all fault current flows from TIP to RING and only one fuse and series resistor is required for each line.

The 470 Ω series resistors R1 and R2 provide surge current limiting to protect the high impedance receiver RTIP and RRING input pins of the IC. R3 and R4 are 200 Ω resistors which provide the line side termination of 100 Ω.

On the transmitter output pins, the Schottky diodes D1 - D4 provide clamping within approximately 300 mV of the +5 V supply and ground without distorting the output pulse shape.

This circuit does not provide clamping during longitudinal (common mode) lightning surges to ground because the line transformers T1 and T2 are rated to withstand the 1500 Vpk surges required by TR-NWT-001089.

TVS1 is an SM05 bi-directional, 5 V transient voltage suppressor from Semtech which is used to clamp surges coupled onto the power supply by the Schottky diodes D1-D4.

E1 Protection Circuit

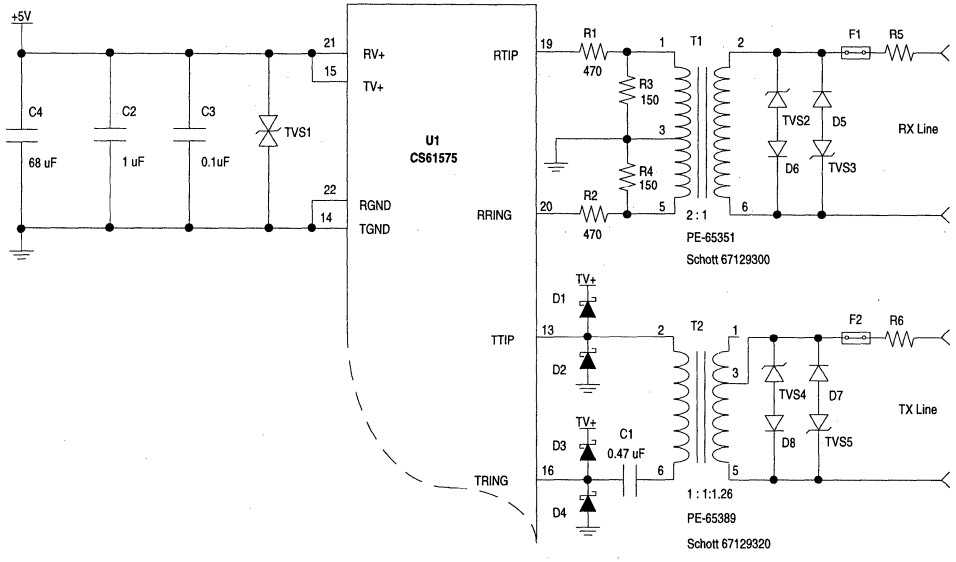
The schematic in Figure 4 shows a 75 Ω unbalanced E1 application circuit with line protection. Because no harmonized European standard has been formally adopted for E1 terminal equipment it is still necessary to consult the requirements imposed by specific countries. CCITT K.20, IEC-801-5 and ETS 300-046-1 provide requirments which are similar to those imposed by many European countries. This circuit provides a general illustration which may readily adapted to other requirements.

This circuit uses the avalanche diodes TVS2 - TVS5 together with the ultra-fast recovery diodes D5-D8 to provide low capacitance, bi-directional voltage limiting protection.

On both transmit and receive lines, time delay fuses, F1 and F2 provide current limiting protection for AC power cross or other steady-state faults. Some countries requirethe use of indicating fuses while others do not allow the use of fuses at all. In countries that do not allow fuses PTC resistors can be used to provide resettable protection. The 1 Ω series resistors R5 and R6 provide transient current limiting to protect the fuses during a lightning surge. Since the line connectios are unbalanced, all fault current flows from TIP to RING and only one fuse and series resistor is required for each line.

The 470 Ω series resistors R1 and R2 provide surge current limiting to protect the high impedance receiver RTIP and RRING input pins of the IC. R3 and R4 are 150 Ω resistors which provide the line side termination of 75 Ω.

On the transmitter output pins, the Schottky diodes D1 - D4 provide clamping within approximately 300 mV of the +5 V supply and ground without distorting the output pulse shape.



Component	Description	Part #	Manufacturer
TVS1	5 V, bi-directional TVS	SM05	Semtech
TVS2 - TVS5	6.5 V TVS	SMBJ6.5	Semtech
D5-D8	Ultra-fast recovery diode	SS8198	Semtech
R5, R6	1.0 Ω, 2 W resistor		
F1 - F2	1.0 A time delay fuse	TE5-T	Wickmann USA
D1 - D4	Schottky diode	11DQ04	International Rectifier

Figure 4. E1, 75 Ω Line Protection Circuit.

TVS1 is an SM05 bi-directional, 5 V transient voltage suppressor from Semtech which is used to clamp surges coupled onto the power supply by the Schottky diodes D1-D4.

CONCLUSIONS

This application note has illustrated how to combine protection devices to realize practical secondary protection for the sensitive ICs on a T1/E1 line card. While these recommendations are intended to provide practical recommendations on how to satisfy FCC Part 68, UL1459, Bellcore TR-NWT-001089, CCITT K.20 and IEC 801-5 requirements, they should not replace careful design verification and testing to insure compliance with the appropriate specifications. The effectiveness of line protection will depend upon its specific implementation in a particular system. The following guidelines should be followed to insure optimum implementation.

1. T1/E1 line connections should be physically isolated from other components on the same circuit board. Provide adequate component spacing between line side components and chassis ground contact points to prevent arcing.

2. T1/E1 line connections should be electrically isolated from other components on the same circuit board. Careful attention to board layout should insure that no signal traces cross the transformer isolation barrier on any layer of the PCB. To insure this isolation, board area for line interface connections should be excluded from auto-routing and layout should be done by hand. No internal power or ground planes or signal traces should cross the isolation zone. The dielectric breakdown voltage between adjacent layers of a multi-layer PCB is much lower than that of a line coupling transformer.

3. Use appropriate size PCB traces for line side traces. Traces should be large enough to handle peak fault currents. Also keep in mind the thermal dissipation limits of the PCB and any connectors or cables in the signal path.

4. Board-level secondary protection should be designed to handle the energy that primary protectors let through and should allow most of the fault energy to be diverted by higher capacity primary protectors. Primary protection devices should not generally be used in line cards because of the limited energy handling capacity of printed circuit boards. It is more appropriate to shunt fault currents through large low impedance grounding links in distribution frames than to do so through line cards.

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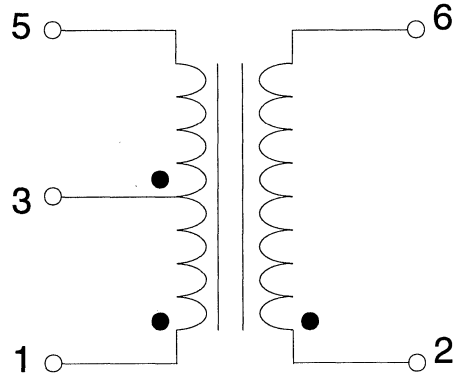
Application Note

Telecom Transformer Selection Guide

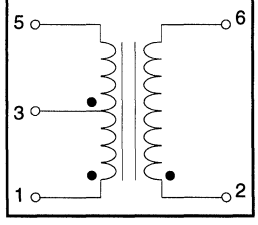


Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 462-2723

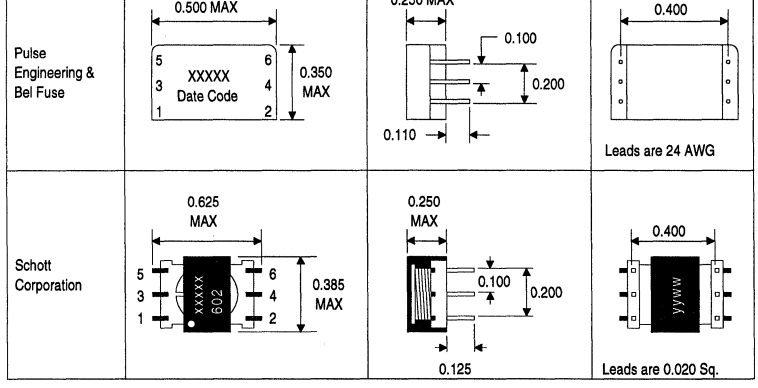
Transformer	CS61534 CS61544 CS61577 Rx	CS61535 CS61574 CS6158 Tx	CS61535A CS61575 Rx	CS61574A CS6158A Tx
PE-65351 Schott 67129300 Bel Fuse 0553-0013-HC	•[1]	•[2]	•[1]	
PE-65388 Schott 67129310 Bel Fuse 0553-0013-RC				•[3]
PE-65389 Schott 67129320 Bel Fuse 0553-0013-SC				•[4]

Notes:
1. Refer to Figure 1 for receiver application circuit.
2. Refer to Figure 2 for 100 Ohm T1 and 120 Ohm E1 transmitter application circuit.
   Refer to Figure 3 for 75 Ohm E1 transmitter application circuit.
3. Refer to Figure 4 for 100 Ohm T1 transmitter application circuit.
4. Refer to Figure 5 for 75 Ohm E1 transmitter application circuit.
   Refer to Figure 6 for 120 Ohm E1 transmitter applications circuit.

Schematic



Mechanical Specifications



Notes:
1. The first two digits and final digit of Schott part numbers are suppressed on the package mark.
2. Schott drawings use a different pin numbering convention than that shown here but Schott and Pulse Engineering devices are interchangeable.
3. Surface-mount, dual, low temperature, or 3 kV Isolation transformers are also available.

To request information or samples contact:

Pulse Engineering
P.O. Box 12235
San Diego, CA 92112
TEL: (619) 674-8100
FAX: (619) 674-8262

Schott Corporation
1000 Parkers Lake Rd.
Wayzata, MN 55391
TEL: (612) 475-1173
FAX: (612) 475-1786

Bel Fuse
198 Van Vorst Street
Jersey City, NJ 07302
TEL: (201) 432-0463
FAX: (201) 432-9542

Applications With Crystal PCM Line Interface IC's

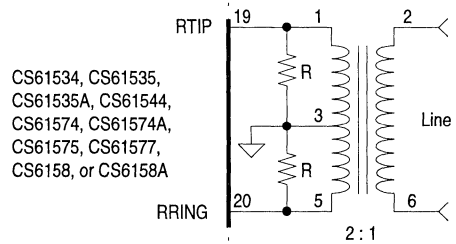


Figure 1. Receiver Application for T1 and E1

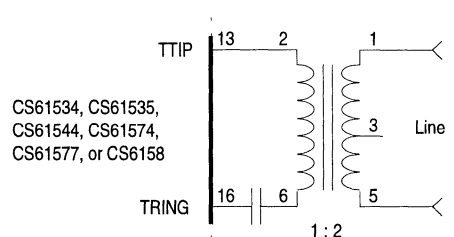


Figure 2. Transmitter Application for 100 Ohm T1 and 120 Ohm E1

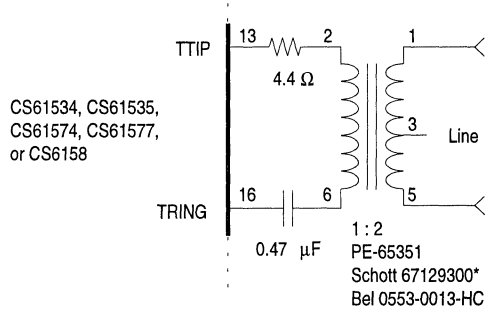


Figure 3. Transmitter Application for 75 Ohm E1

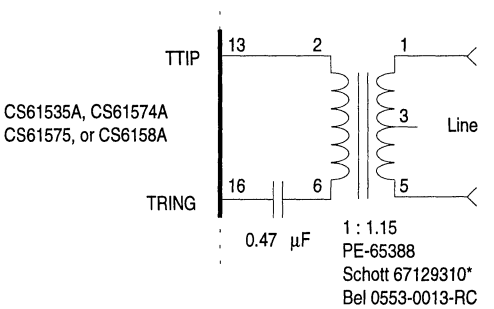


Figure 4. Transmitter Application for 100 Ohm T1

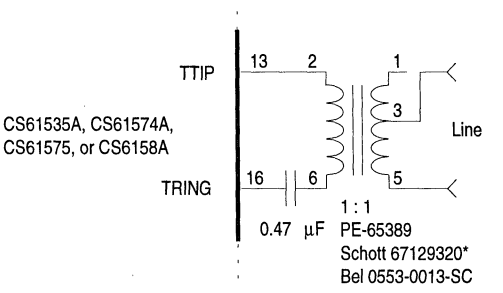


Figure 5. Transmitter Application for 75 Ohm E1

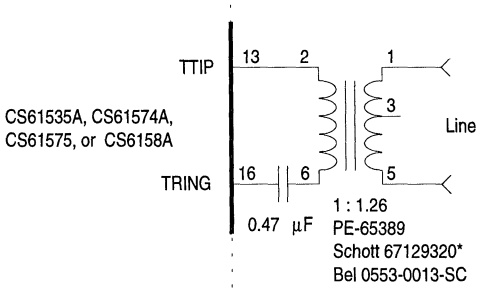


Figure 6. Transmitter Application for 120 Ohm E1

* Schott drawings use a different pin numbering convention than that shown here. These schematics follow the pin numbering convention used in this document.

11

• Notes •

Jitter Attenuation Performance of the CS61575 and CS61574A PCM Line Interface Circuits

By Bob Bridge

SUMMARY

This application note helps customers choose between the CS61575 and CS61574A. Both the CS61575 and CS61574A are pin-compatible, higher performance alternatives to the CS61574. Performance improvements include a reduction in power requirements by 50%, a guarantee of 14 dB of transmitter return loss, and an optional B8ZS/AMI/HDB3 coder. Both the CS61575 and CS61574A provide all these advantages, and differ only in the areas of receiver jitter transfer function and receiver propagation delay.

In summary, the CS61575 is designed for systems needing to meet AT&T 62411 jitter transfer requirements. The CS61574A is the logical choice for all other systems (i.e., those systems not requiring AT&T 62411 certification). The CS61575 has improved jitter transfer relative to the CS61574A and CS61574 when the input jitter amplitude exceeds 23 Unit Intervals (UIs) at a frequency in the attenuation range. This improved transfer comes at the expense of longer propagation delay through the receiver; typically a 96-bit delay for the CS61575 versus 16-bits for the CS61574A and CS61574. Also, attenuation begins at a jitter frequency of 3 Hz for the CS61575 compared to 6 Hz for the CS61574A.

However, the summary statement that the CS61575 should be used for 62411 applications is qualified as follows: If a system employing the CS61574 has previously been certified as compliant with 62411, a system upgraded to the CS61574A will continue to pass the same certification procedure. (The CS61575 would also pass the same certification tests). This qualification is elaborated upon in a later section.

JITTER ATTENUATOR CIRCUIT DESCRIPTION

This section describes the jitter attenuator circuitry of the CS61575 and CS61574A. This provides a basis for more detailed discussion of the performance differences of the two ICs.

Figure 1 shows the attenuator circuitry. The jitter attenuator reduces jitter in the recovered clock signal. It consists of a FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted in fine steps

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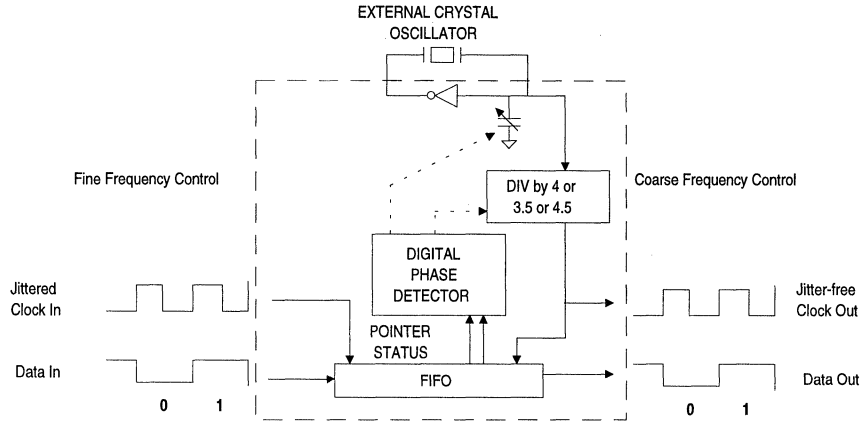


Figure 1 - Jitter Attenuator Block Diagram

to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3.5 or divide by 4.5 to prevent the FIFO overflow or underflow. This is a coarse adjustment of the outgoing clock. During this activity, data will never be lost, but jitter gain occurs.

The jitter attenuator of the CS61575 contains a 192-bit FIFO, and will tolerate 138 UIs at 1 Hz and 28 UIs at 300 Hz as required by 62411 (Figure 2), while attenuating the jitter. The jitter attenuators of the CS61574A and CS61574 contain a 32-bit FIFO, and will typically tolerate 23 UIs (at a frequency in the attenuation range) before the overflow or underflow mechanism takes effect increasing output jitter to prevent data loss.

PERFORMANCE IMPLICATIONS OF ATTENUATOR DESIGN

As shown in Figure 2, the CS61575, CS61574A and CS61574 all tolerate the input jitter defined by AT&T 62411. (Note that all other recent standards require a maximum tolerance of 10 UIs). However, when the input amplitude exceeds 23 UIs, the CS61575 continues to provide a continuous jitter transfer function. As shown in Figure 2, when more than 23 UIs are input to the CS61574A, CS61574 or similar devices (such as the LXT300), the divide by 3.5 or 4.5 mechanism produces jitter gain.

If the CS61574 has discontinuities in the transfer function, then how can it be that systems using the CS61574 have routinely passed 62411?

One answer is that most sophisticated systems contain a system synchronizer (PLL) and one frame buffer (FIFO) per trunk (Figure 3). In fact, all systems which meet Stratum 4 (Type 1), Stratum 3 or Stratum 2 requirements will have a synchronizer. The synchronizer/FIFO can provide attenuation which is incremental to that provided by the CS61574A or CS61574 on the trunk card.

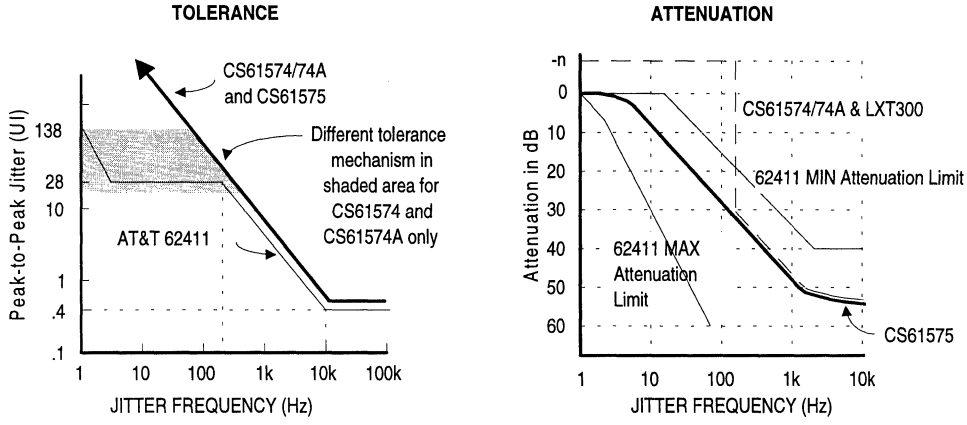


Figure 2 - Jitter Performance Differences of CS61575 and CS61574A/CS61574

Note that smaller systems (typically systems with a single T1 trunk attached) are often Stratum 4 (Type 2) systems. See Figure 4. These systems lack a system synchronizer, and should always use the CS61575.

Another answer to the question "how can systems using the CS61574 pass 62441" is that many test laboratories have historically not been equipped to generate and receive more than 10 UIs of jitter. These labs would be unable to distinguish the performance difference of the CS61575 and CS61574A. Newer test equipment (often custom equipment designed by a lab) is capable of generating/receiving more than 10 UIs of jitter. For example, the AT&T labs now have the capability to measure the length of frame buffers located inside a system. With that sophisticated test capability, jitter gain by a divide by 3.5 or 4.5 is detectable.

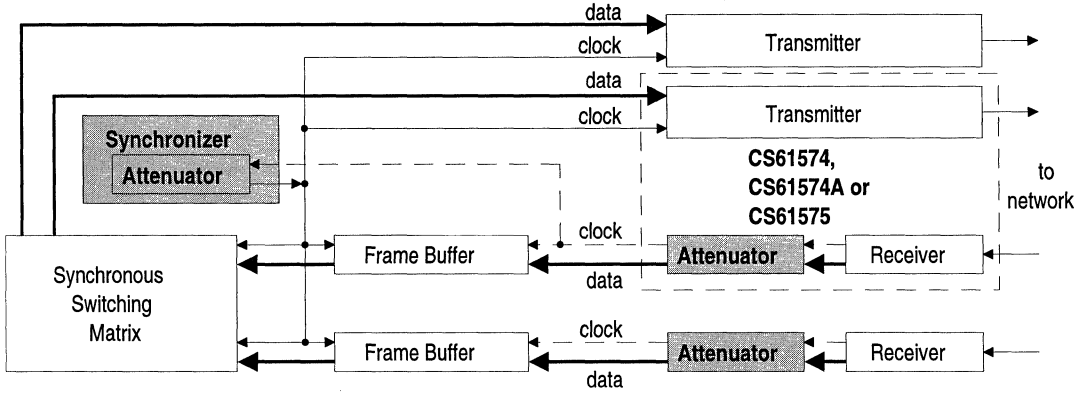


Figure 3 - Using the CS615x4 in AT&T 62411 Stratum 2,3 or 4(Type 1) Systems

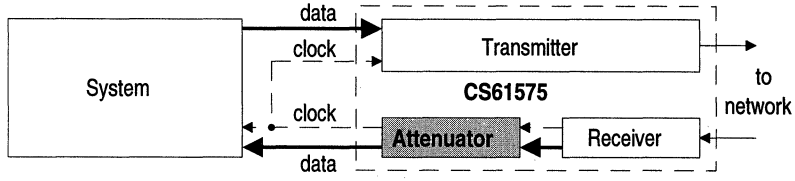


Figure 4 - Using the CS61575 in AT&T Stratum 4 (Type 2) Systems

CHANGES IN AT&T 62411 REQUIREMENTS

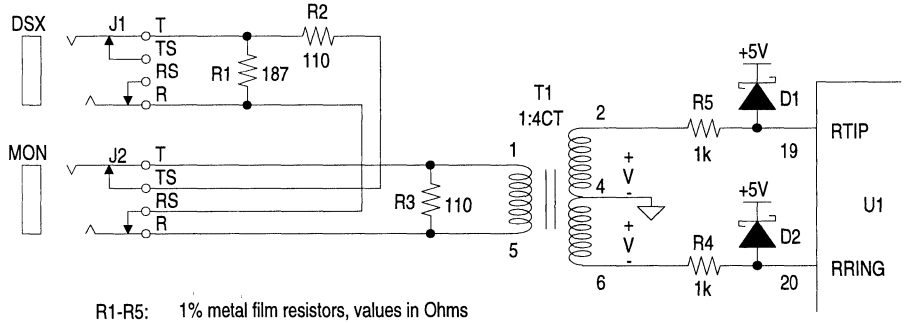
In December 1990, AT&T changed the high-frequency jitter transfer test procedures used at 62411 certification labs. Whereas 62411 formally required 60 dB of attenuation (a performance level not achieved under all operating conditions by any line interface IC from any vendor), the latest 62411 spec requires only 40 dB of attenuation.

AT&T made this change at the request of equipment manufacturers who demonstrated that the attenuation performance of the CS61574 was consistent with the requirements for robust and reliable network performance. Note that 60 dB of attenuation implies 0.0002 UI of output jitter at spot frequencies. This amplitude is so small as to be barely measureable. 40 dB of attenuation implies 0.002 UI of output jitter at spot frequencies.

Application Note

FlexibleT1 Receiver Interface Supports Line Monitoring

by
Greg Stearman



R1-R5: 1% metal film resistors, values in Ohms
D1,D2: 1N5711, Schottky Diode (BKC)
T1: PE-65363, 1:4CT transformer (Pulse Engineering)
U1: CS61535A, CS61574A, CS61575, or CS6158A
J1, J2: RTT34B-02, minature telephone jack, (Switchcraft)

Figure 1. T1 Receiver Interface

The application circuit, shown in Figure 1 above, allows the CS61535A, CS61574A, CS61575 or CS6158A to terminate or monitor a DSX-1 line.

To use this circuit to terminate a DSX-1 line, connect the input signal to the "DSX" connector and leave the "MON" connector open. In this configuration, the line is terminated by the parallel combination of R1 and (R2+R3) which is approximately 100 Ω. Also, R2 forms a voltage divider with R3 so that only half of the input signal amplitude is coupled across the transformer. The 1:4 transformer provides a gain of 2 since the IC receiver inputs process only positive pulses relative to ground. Since the center tap is grounded only half the voltage across the secondary is above ground. With a pulse of the polarity TIP > RING as shown in Figure 1, the RTIP pin detects the pulse of amplitude +V and the RRING input ignores the pulse of -V. The transformer gain therefore cancels the voltage divider attenuation.

The line interface receiver peak detector automatically adjust the data decision threshold to 65% of the peak input level to provide excellent noise and cross-talk immunity for nominal signal levels between 500 mV and 3.6 V.

This cicuit also supports high impedance monitoring through a DSX-1 monitor port. Figure 2 shows the internal 432 Ω resistors in series with the TIP and RING connections in a cross-connect monitor jack. These resistors isolate the line which is being monitored from the 100 Ω termination in the test equipment receiver. The resistors also form a voltage divider with the test set termination resistance. When terminated into

11

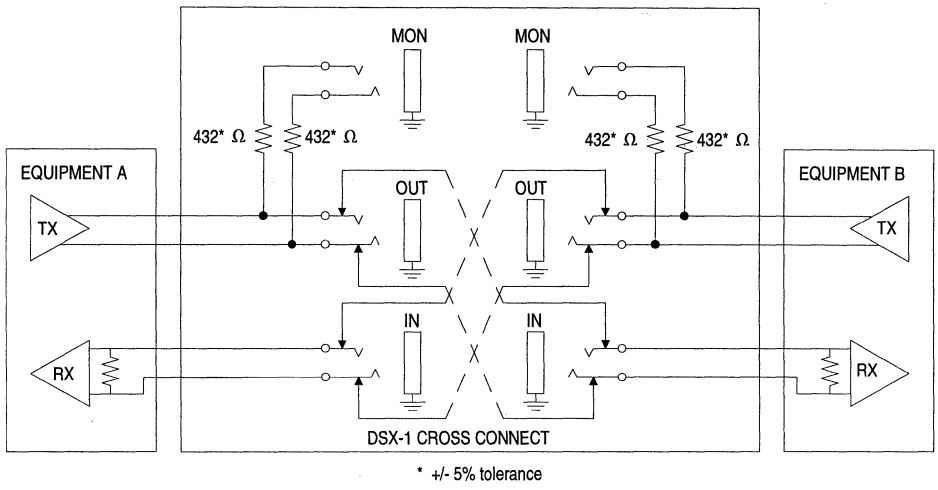


Figure 2. DSX Cross Connect

100 Ω, the monitor jack output level is approximately 19.7 dB below the DSX-1 signal level.

To monitor a line through a DSX-1 monitor jack using the circuit in Figure 1, connect the signal from the cross-connect monitor port to the "MON" connector and leave the "DSX" connector open. Note that the DSX jack is completely removed from the circuit when a signal is connected to the "MON" jack so no damage results from connections to both jacks simultaneously. The input impedance of the "MON" jack is set by R3 which is 110 Ω. This value reduces the nominal signal attenuation by approximately 0.76 dB (compared to a 100 Ω termination) and still matches the line impedance. All of the input signal amplitude is coupled across the transformer, and the 1:4 transformer provides an effective signal gain of 2 (or +6 dB). The signal level, V, at the RTIP and RRING input pins of U1 is approximately 12.9 dB lower that the signal level at the input of the DSX-1 monitor jack. With a 2.4 V signal at the monitor jack input, the signal level at each input pin of U1 will be at least 514 mV with respect to ground (based upon worst case resistor tolerances).

To insure that U1 is not damaged by excessive signal levels in the event a full amplitude DSX signal is connected to the "MON" jack, input protection is provided by R4, R5, D1 and D2. R4 and R5 provide input current limiting protection for D1 and D2 as well as the internal protection structures in the line interface IC input pins. R4 and R5 do not introduce significant signal attenuation because the RTIP and RRING pins have a typical input impedance of 50 kΩ. D1 and D2 are Schottky diodes which clamp the RTIP and RRING pins at approximately 0.3 V above the supply voltage.

It is also possible to monitor a line without using a DSX-1 monitor port by adding a series resistor. This configuration may be used to directly monitor across a line at any point along it. For this type of line monitoring, insert an 800 Ω resistor in series with the cable which is connecting the "MON" jack in parallel with the line being monitored. This resistor may be placed in series with either TIP or RING since the circuit in Figure 1 does not reference ground on the line side of the transformer.

INFRARED DATA LINKS: THE NEXT PORTABLE INTERFACE STANDARD

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ABSTRACT

Computing devices are becoming more mobile. Connectivity to office equipment and other computers is mandatory. Infrared data transfer allows the mobile user to communicate easily without cables. This paper discusses the technical details of a new infrared data transfer standard: IrDA (Infrared Data Association). Both the physical layer and software protocols are discussed. Example circuits are included.

INTRODUCTION

Pioneering computing devices have established the benefits of infrared (IR) data transfer. Good examples are the Hewlett Packard Omnibook sub-notebook PC, the Sharp Wizard organizer and the Apple Newton PDA. The IR-based TV and VCR remote control unit is now a familiar household item. However, these units use incompatible physical and software interfaces.

In the summer of 1993, an industry-wide meeting was called by Hewlett Packard to discuss the future of IR data transfer. The specter of multiple, incompatible standards was very real, with everybody suffering if different manufacturers' units were incompatible. The goal of the meeting was to discuss how the industry could achieve a common standard that would allow interoperability between all units with an IR port. The result of the meeting was the formation of a consortium of all the major computing companies. This consortium is called the Infrared Data Association (IrDA).

Extensive use of email and phone conferences, plus a lot of hard work from key individuals, has resulted in the June 1994 publication of both the physical layer and software protocol IrDA standard documents.

IrDA LINK CHARACTERISTICS

An IrDA port allows a short distance (0 to 1 meter is required for IrDA compliance), point-to-point link to be established. This follows from a "walk up and transfer" user model. IrDA deliberately did not try to create an IR based local area network. Such interfaces are very complex and require a lot of power. IrDA goals included low power consumption and low cost. The IrDA interface uses a narrow field of IR at low power which results in inexpensive hardware and does not require Federal Communications Commission (FCC) qualification.

An IrDA port is based on the architecture of the communications (COM) port of a Personal Computer (PC), see Figure 1. The port uses a Universal Asynchronous Receiver Transmitter (UART) and operates at bit rates from 2400 bps to 115200 bps. The data are transmitted as 10-bit characters, with 8 data bits, 1 start bit added to the beginning of the data and 1 stop bit added to the end of the data.

The link is half-duplex, since the transmitted IR swamps the adjacent PIN diode amplifier. The air space between units can only have IR energy from one source at a time.

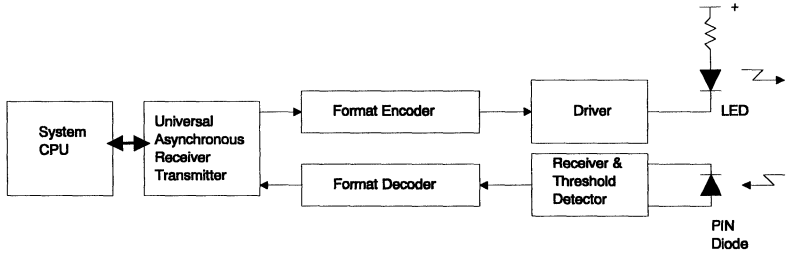


Figure 1. IrDA Infrared Link Port Architecture

PHYSICAL LAYER DETAILS

Transmit Path

The byte to be transmitted is sent to the UART from the system CPU usually as an output write instruction. The UART adds the start and stop bit, and transmits the character in a bit serial fashion, LSB first. The IrDA standard [1] requires that each serial bit be coded as follows: a logic 0 bit is transmitted as a single pulse of IR, which can be anywhere from 1.6 µs to 3/16 of the bit cell period; a logic 1 bit is transmitted as no IR (see Figure 2). The benefit of a fixed 1.6 µs pulse is that the power consumption is minimized.

After the bits are encoded, one or more IR LEDs must be driven with the appropriate current level to generate the required intensity of IR pulse. The IrDA standard [1] calls for a 40 mW/Sr to 500 mW/Sr intensity inside an angular range of ±30°. For a good explanation of radiant intensity, receive sensitivity and the length of a link see reference [2]. The wavelength of the IR LED should be 880 nm.

Receive Path

The incoming IR pulses are presented to a PIN diode. The PIN diode converts the light pulses into current pulses. The current pulses are amplified, filtered and compared against a threshold level to generate logic levels. A pulse of IR generates a logic 0; no light generates a logic 1. The IrDA standard [1] requires that the receiver correctly detect IR pulses of 4 $\mu W/cm^2$ to 500 mW/cm^2, over an angular range of 15° .

Two sources of interference are present. Sunlight is a major source of IR, but fortunately is predominantly DC. Well designed receivers will compensate for large DC ambient currents from the PIN diode. The second source is high frequency fluorescent lights, particularly common in desk lamps and in modern, energy saving offices. Well designed receivers will incorporate a bandpass filter to limit the effect of these noise sources. Ultimately, the link Bit Error Rate (BER) will depend on the correct choice of transmit power and receive sensitivity. The IrDA specification values were chosen to make sure that sunlight and fluorescent lights will not degrade a compliant link.

After conversion of the pulses from light to logic levels, the short pulses representing zeros must be stretched in time to equal the bit cell time for the current bit rate. The data stream is then presented to the UART RxD terminal. The UART strips off the start and stop bits, and converts the byte to parallel. The data byte is then read by the system CPU via an I/O read instruction to the UART.

SOFTWARE PROTOCOL

The IrDA software protocol, shown in Figure 3, includes a Link Access Protocol (IRLAP) which handles dividing the data into blocks, error checking and other low level functions. Also provided is a Link Management protocol, which allows multiple applications to exchange data over a single link. Finally, an optional transport layer protocol is included, which allows application to application flow control for multiple applications running over a single physical link. Three interfaces are provided to the different layers. At the LM-SVC layer, service primitives enable one IrDA device to find out what services and protocols are registered on another device. The M-SVC access primitives control the link mode, the opening and closing of indepedent connections between clients, and the sending and receiving of data, The L-SVC interface provides access to the IrLAP functions.

IRLAP - Serial Infrared Link Access Protocol

IRLAP is a derivative of existing standard asynchronous HDLC and SDLC half-duplex protocols, as used on multi-drop links. These use a Master/Slave relationship between a primary station (Master) and one or more secondary stations (Slaves). Some special modifications to the standard protocol have been made to take into account the interference prone nature of the IR interface, and the very mobile nature of the connecting stations.

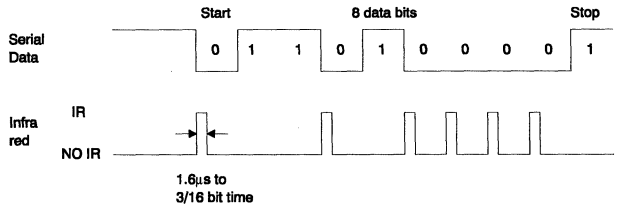


Figure 2. IrDA Data Format

Sniff before establishing a link. Before starting to transmit, IrDA compliant units must first attempt to read the nearby IR activity to establish if an existing transfer is occurring in the vicinity of the unit. If such activity is detected, an appropriate message is passed back to the calling software. The unit will not start to transmit IR. This results in a more robust perception of IR links, particularly as IrDA equipped units become more common.

Any station can be the primary. Since the two units communicating may both be computers (rather than a computer and a printer), then either unit can be the primary. The choice depends on which unit initiated the transfer.

Address extension to allow for mobile users. Each unit has a 32-bit address which is generated at random when the link is established. Each frame within the link has a 7-bit connection address, which is assigned by the master unit at the start of a connection.

Dynamic address conflict resolution. In the unlikely event of two devices having the same address, there is a mechanism for the master unit to command all slave units to change their device address.

Bit Rate Negotiation During the establishment of the link, the two units involved negotiate for the fastest bit rate that both units can handle. In most cases, this will be 115200 bps, but could be as low as 2400 bps. All initial transfers, prior to the bit rate negotiation phase, are done at 9600 bps.

Turn Round Time Settings. The Maximum Turn Around Time can be 100 ms, 250 ms or 500 ms, and is the maximum length of time that a unit can transmit before turning round to listen for an acknowledge. This is related to the bit rate and the buffer capacity of the receiving unit. The Minimum Turn Around Time results from the inability of the transmitting unit to receive data immediately after the last bit has been transmitted. The transmitting unit's PIN diode amplifier will be saturated from its own transmissions. The receiver takes a variable amount of time to recover (anywhere from 0.01ms to 10ms). These parameters should be known for a given unit, and are negotiated during the link start up phase.

Extended Recovery Procedures. These include a reset function, which returns an active, but interrupted, link to the default connection parameters state.

IRLAP uses three kinds of frame, as defined by HDLC. Un-numbered, or U frames, are used for establishing a link. Information, or I frames, are used to transfer information. Supervisory, or S frames, are used for handshaking functions.

IrDA Link Management Protocol

The IrDA is currently finalizing the Link Management Protocol standard. This involves discovery, where each IrDA device keeps a table of services and protocols that it currently has available. This information can be queried from another device.

A link manager multiplexer, and its associated control, enables multiple applications to exchange data over a single physical link. Reference [4] provides a complete description of the link management protocol.

IrDA Transport Protocol

Currently in the proposal stage, IrDA is working on using ISO 8073 as a transport protocol. This allows multiple streams of data to flow across an IrDA link, each one with its own flow control. Use of this protocol is optional. Reference [5] provides a complete description of the transport protocol.

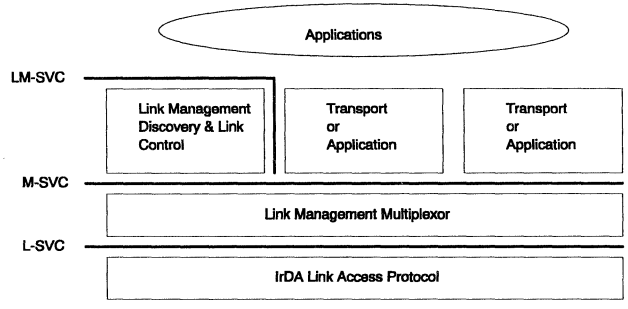


Figure 3. IrDA Software Structure

CERTIFICATION

The IrDA is currently involved in implementing a certification procedure. Companies may submit units for compliance testing to independent certification laboratories, or may become certified for self certification. Only after passing the certification tests can a unit carry the "IrDA data certified" logo, indicating that the unit is compliant with the IrDA standard

The certification procedure involves checking the software protocol handling for the correct responses to errors and interruption of the link. Certification also involves measuring the physical layer specifications, including IR output power and receive sensitivity.

EXAMPLE HARDWARE SCHEMATICS

Crystal Semiconductor manufactures an IR transceiver device, the CS8130 (Figure 4). This device interfaces a standard UART to the transmit LED and receive PIN diode. It handles IrDA, ASK and TV remote formats and includes programmable transmit power and receive threshold. It is packaged in a very small 5 mm x 7 mm SSOP package. Reference [6] contains full details of applying and programming the CS8130.

An example application is the addition of an IrDA port onto an existing notebook PC motherboard design (Figure 5). An existing UART can be used to both drive a wired RS232 COM port, using a Maxim MAX562 RS232 level translator device, and an IrDA compatible IR port using the CS8130. The $\overline{\text{PWRDN}}$ pin of the CS8130 is used to three-state the RXD and FORM/BSY lines, allowing the MAX562 to use the UART. Alternatively, the EN and $\overline{\text{SHDN}}$ pins will three-state the R2OUT and R3OUT pins on the MAX562, allowing the CS8130 to use the UART.

A second example application is a schematic for an external pod, which can connect to any existing standard COM port on any computer (Figure 6). This circuit could be made very small, for example as a 1 inch cube on the end of 1 yard of cable, allowing for easy optimum positioning of the port.

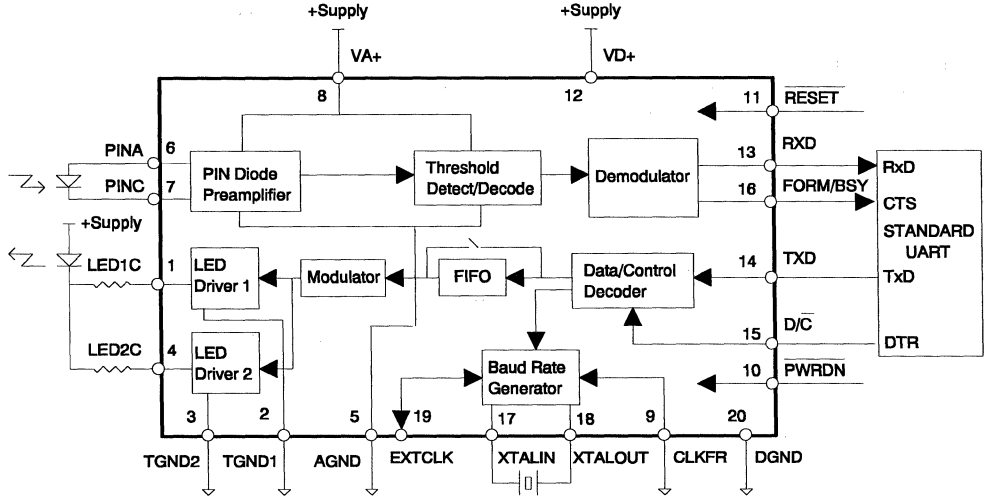


Figure 4. An Example IrDA Interface Device - CS8130

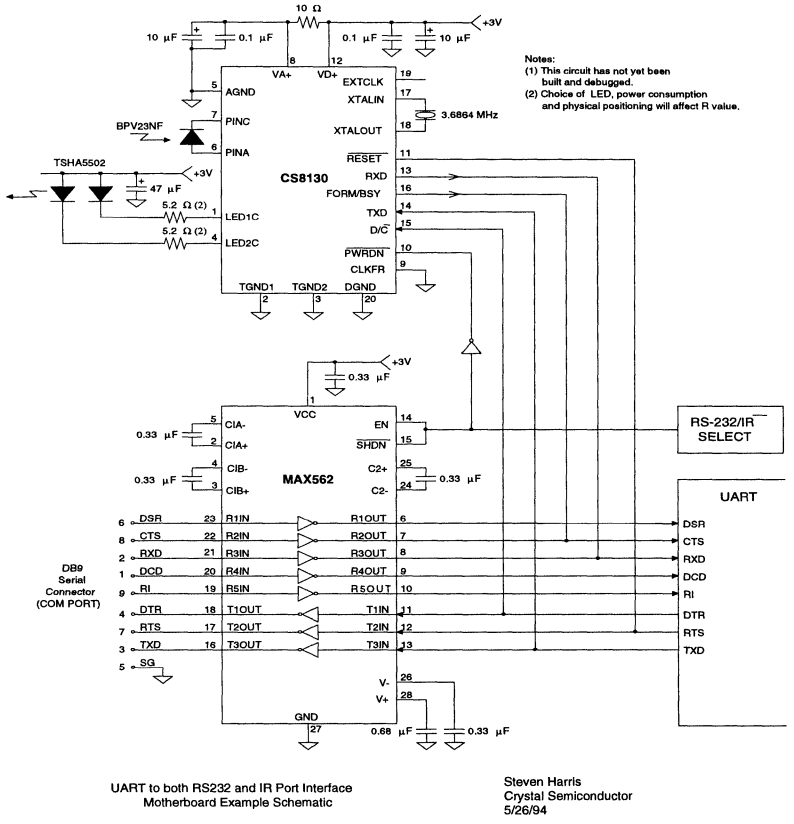


Figure 5. Example IrDA port schematic

SUMMARY

This paper has summarized the key features of an IrDA infrared data link. The combination of low cost, ease of implementation and the promise of inter unit compatibility will quickly result in the widespread use of IrDA links.

REFERENCES

[1] Infrared Data Association Serial Infrared (SIR) Physical Layer Link Specification, IrDA.

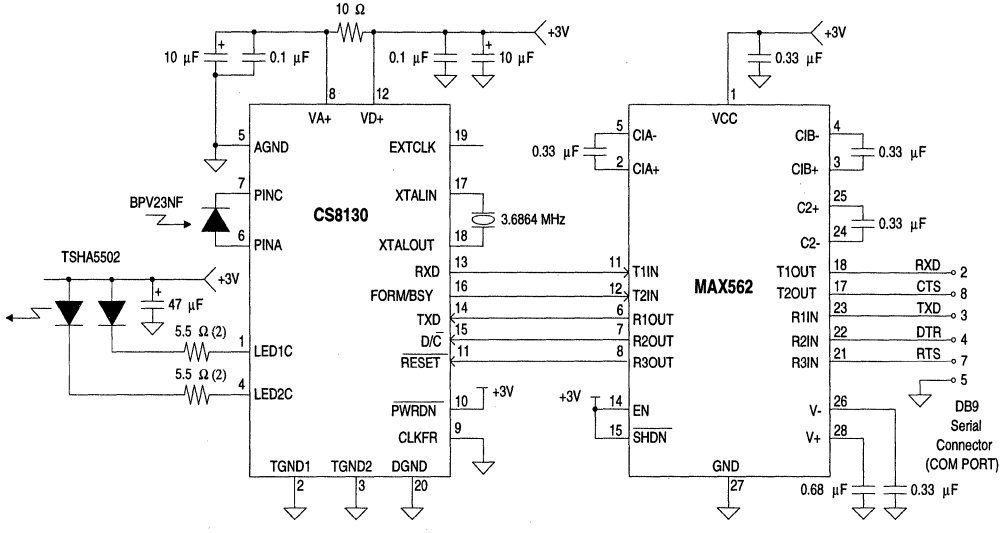
[2] Long-range Infrared Communications by Larry Foltzer, The Computer Applications Journal, June 1993, Issue #35

[3] Infrared Data Association Serial Infrared Link Access Protocol (IRLAP), IrDA

[4] Infrared Data Association Link Management Protocol, IrDA

[5] Infrared Data Association Proposal for the use of ISO 8073 as an IrDA Transport Protocol

[6] CS8130 Multi-Standard Infrared Transceiver Data Sheet, Crystal Semiconductor Corporation.



Notes:
(1) This circuit has not yet been built and debugged.
(2) Choice of LED, power consumption and physical positioning will affect R value.
(3) The creation of +3V or +5V supply is not included here.

RS232 COM PORT to Infra Red Interface
Pod Schematic

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Crystal Semiconductor
5/26/94

Figure 6. Example COM port to IR Pod Schematic

Common Abbreviations Used in the Communications Industry

	1Base5	1MHz, 500m over coax (CSMA/CD)
	10Base2	10MHz, 185m over thin coax (CSMA/CD) - Cheapernet
	10Base5	10MHz, 500m over coax (CSMA/CD)
	10BaseT	10MHz, 100m over twisted pair (CSMA/CD)
	10Broad36	10MHz over Broadband coax
	2B1Q	2 Binary to 1 Quaternary (Coding / Decoding)
	2B+D	2 Bearer + Data
	4B3T	4 Binary to 3 Ternary (Coding / Decoding)
A	**ABATS**	Automatic Bit Access Test System
	ACCS	Automatic Calling Card Services
	ACD	Automatic Call Distribution
	ACF	Automatic Call Forwarding
	ADM	Add/Drop Multiplex
	ADPCM	Adaptive Differential Pulse Code Modulation
	ADSL	Asymmetric Digital Subscriber Line
	AES	Audio Engineering Society
	AIS	Alarm Indication Signal (Blue Alarm)
	ALBO	Automatic Line Build Out
	AMI	Alternate Mark Inversion
	ANI	Automatic Number Identification
	ANSI	American National Standards Institute
	APPC	Advanced Program to Program Communication
	APS	Automatic Protection Switching
	ARCNET	Attached Resource Computer NETwork
	ARQ	Automatic Repeat reQuest
	ATIS	Alliance for Telecommunication Industry Solutions (formerly ECSA)
	ATM	Asynchronous Transfer Mode
	AUI	Attachment Unit Interface

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B	**B8ZS**	Bipolar, 8-Zero Substituition
	BATS	(Manual) Bit Access Test System
	Bellcore	Bell Communications Research
	BER	Bit Error Rate
	BERT	Bit Error Rate Tester
	BIP	Bit Interleaved Parity
	BIPCV	BIP Code Violation
	BISDN	Broadband ISDN
	BOC	Bell Operating Company
	bps	bits per second
	BPV	BiPolar Violation
	BRA	Basic Rate Access
	BRI	Basic Rate Interface
C	**CA**	Customer Access
	CAS	Channel Associated Signaling
	CCIS	Common Channel Interoffice Signaling
	CCITT	Consultative Committee on International Telegraphy & Telephony (see ITU)
	CCS	Common Channel Signaling
	CCS	Common Computation Services
	CD	Compact Disc
	CEPT	European Postal & Telegraph Committee
	CFA	Carrier Fault Alarm
	CI	Customer Installation
	CIU	Craft Interface Unit
	CLASS	Custom, Local Area Signaling Services
	CLEI	Common Language Equipment Indentifier
	CLIP	Calling Line Identification Presentation
	CMIP	Common Management Interface Protocol
	CMOL	CMIP Over LLC
	CMOT	Common Management Over TCP/IP
	CO	Central Office
	CODEC	COder / DECoder
	COFA	Change Of Frame Alignment
	COT	Centrol Office Terminal
	CPE	Customer Premises Equipment
	CPI	Common Programming Interface
	CPLID	Calling Party Line IDentification
	CPU	Central Processing Unit
	CRC	Cyclic Redundancy Check
	CRC-CV	Cyclic Redundancy Check - Code Violation
	CRV	Call Reference Value
	CS	Controller Slip
	CSD	Circuit Switched Data
	CSMA/CD	Carrier Sense Multiple Access with Collision Detection

	CSU	Channel Service Unit
	CSES	Consecutive Severely Errored Seconds
	CSMA/CD	Carrier Sense Multiple Access/Collision Detect
	CSS	Controlled Slip Seconds
	CUA	Common User Access
	CUT	Control Unit Terminal
	CV	Code Violation
D	**DA**	Destination Address
	DACS	Digital Access and Cross-connect System
	DAS	Dual Attached Station
	DAT	Digital Audio Tape
	DCC	Data Communication Channel
	DCC	Digital Compact Cassette
	DCE	Data Circuit terminating Equipment
	DCS	Digital Cross-connect System
	DCTE	Data Circuit Termination Equipment
	DDS	Dataphone Digital Service® (AT&T)
	DFT	Distributed Function Terminal
	DIA	Document Interface Architecture
	DIS	Draft International Standard
	DIT	Directory Information Tree
	DL	Data Link
	DLC	Digital Loop Carrier
	DLCI	Data Link Control Identifier
	DLS	Data Link Service
	DM	Degraded Minutes
	DMA	Direct Memory Access
	DMI	Digital Multiplexed Interface
	DP	Draft Proposal
	DPA	Demand Protocol Architecture
	DQDB	Distributed Queue Dual Bus
	DS0	Digital Signal level 0 (64 kbps)
	DS1	Digital Signal level 1 (1.544 Mpbs)
	DS1C	Digital Signal level 1C
	DSL	Digital Subscriber Line
	DSn	Digital Signal level n - (n=1, 1C, 2, 3, 4)
	DSS-1	Digital Subscriber Signaling - system 1
	DSU	Data Service Unit
	DSX	Digital Signal Cross-connect
	DTAU	Digital Test Access Unit
	DTE	Data Terminal Equipment
	DTMF	Dual Tone / Multi-Frequency
	DUA	Directory User Agent
	DUP	Data User Part

E	**EBU**	European Broadcast Union
	ECH	Echo Canceller with Hybrid
	ECMA	European Computer Manufacturers Association
	ECSA	Exchange Carrier Standards Association (see ATIS)
	EDSL	Extended Digital Subscriber Line
	EEPROM	Electrically Erasable Programmable ROM
	EIAJ	Engineering Industry Association Japan
	EMA	Enterprise Management Architecture
	EMS	Element Management System
	EOC	Embedded Operations Channel
	EOF	End Of Frame
	ES	Errored Second
	ESA	Errored Seconds, type A
	ESB	Errored Seconds, type F
	ESF	Extended Superframe Format
	ET	Exchange Termination equipment
F	**FAS**	Frame Alignment Sequence
	FCC	Federal Communications Commission
	FCS	Frame Check Sequence
	FDDI	Fiber Distributed Data Interface (100 MHz)
	FDM	Frequency Division Multiplexing
	FDX	Full DupleX
	FE	Framing (or frame synchronization) Error
	FEBE	Far End Block Error
	FEP	Front End processor
	FLS	Frame Loss Second
	FPS	Framing Pattern Sequence
	FR	Frame Relay
	FT1	Fractional T1 service
	FTAM	File Transfer, Access & Management
	FTP	File Transfer Protocol
G	**GNS**	Global Network Service
	GOSIP	Government OSI Profile
H	**H0**	384 kbps
	H10	1.472 Mbps
	H11	1.536 Mbps
	HDB3	High-Density, Bipolar - 3 zeroes
	HDLC	High level Data Link Control
	HDSL	High-bit-rate Digital Subscriber Line
	HLM	Heterogeneous LAN Management

I	**IA**	Individual Address
	IAC	International Communications Architecture
	IAN	Integrated Analog Network
	IC	Inter-exchange Carrier
	IDLC	Integrated Digital Loop Carrier
	IDN	Integrated Digital Network
	IEC	Inter Exchange Carrier
	IEEE	Institution of Electrical & Electronic Engineers
	IEEE802.3	IEEE Standard for CSMA/CD bus network
	IEEE802.4	IEEE Standard for non-contention network
	IEEE802.5	IEEE Standard for Token ring networks
	IETF	Internet Exchange Task Force
	IFG	Inter-Frame Gap
	IN	Intelligent newtork
	IP	Internet Protocol
	IPG	Inter-Packet Gap
	IPX	International Protocol eXchange
	IS	International Standard
	ISA	Industry Standard Architecture
	ISDN	Integrated Services Digital Network
	ISO	International Standards Organization
	ISPBX	Integrated Services Private Branch eXchange
	ISUP	ISDN User Part
	ITC	Independent Telephone Company
	ITU	International Telecommunications Union
	IVDT	Integrated Voice/Data Terminal
K	**kbps**	kilobits per second
L	**LA**	Latchable Address bus
	LAN	Local Area Network
	LAP-B	Link Access Procedures - Balanced
	LAP-D	Link Access Procedures on D channel
	LAP-DFR	LAP-D Frame Relay
	LAP-D*	LAP-D protocol for non-D-channel applications
	LATA	Local Access Transport Area
	LBO	Line Build Out
	LCV	Line Code Violation
	LEC	Local Exchange Company / Carrier
	LIDB	Line Information Data Base
	LLB	Line Loop Back
	LLC	Logical Link Control
	LLC	Lower Layer Compatibility
	LOF	Loss Of Frame
	LOP	Loss Of Pointer
	LOS	Loss Of Signal

	LT	Line Termination
	LTE	Line Termination Equipment
	LU	Logical Unit
M	**MAC**	Media Access Control
	MAN	Metropolitan Area Network
	MAP	Manufacturing Automation Protocol
	MAU	Media Access Unit
	MAU	Medium Attachment Unit
	MAU	Multistation Access Unit
	Mbps	Megabits per second
	MCA	Micro-Channel Architecture
	MCB	Message Control Block
	MHS	Message Handler System
	MIB	Management Information Base
	MODEM	MOdulator / DEModulator
	MTA	Message Transfer Agent
	MTP	Message Transfer Part
	MTS	Message Transfer System
	MUX	Multiplexer
N	**NANP**	North American Numbering Plan
	NAU	Network Addressable Unit
	NCP	Network Control Processor / Program
	NCTE	Network Channel Terminating Equipment, same as CSU
	NDIS	Network Driver Interface Specifications
	NE	Network Element
	NEBE	Near End Block Error
	NFS	Network File System
	NI	Network Interface
	NIST	National Institute of Standards and Technology
	NIUF	North Amercan ISDN Users Forum
	NLM	Network Loadable Module
	NMS	Network Management System
	NMVT	Network Management Vector Transport
	NNE	Non-SONET Network Element
	NRZ	Non Return to Zero
	NT	Network Termination
	NTn	Network Termination n (n=1, 2)
O	**OAM&P**	Operations, Administrations, Maintenance, & Provisioning
	OCU	Office Channel Unit
	OC-1	Optical Carrier - level 1
	OC-n	Optical Carrier - level n
	OOF	Out Of Frame
	OOS	Out Of Service

	OS	Operations System
	OSI	Open Systems Interconnect
	OSME	Open Systems Message Exhange
	OSPF	Open Shortest Path First
	OTF	Open Token Foundation
P	**PAD**	Packet Assembler/Disassembler
	PANS	Pretty Amazing New Stuff
	PBX	Private Branch eXchange
	PCM	Pulse Code Modulation
	PCTA	Personal Computer Terminal Adapter
	PDS	Premises Distribution System
	PDU	Protocol Data Unit
	PH	Packet Handler / Handling
	PIN	Type of light sensitive diode
	PJ	Pointer Justification
	PJC	Pointer Justification Count
	PLP	Packet Layer Protocol
	PMF	Path Monitoring Function
	POH	Path OverHead
	POP	Point Of Presence
	POTS	Plain Old Telephone System
	PPP	Point to Point Protocol
	PRBS	Pseudo Random Bit Sequence
	PRI	Primary Rate Interface
	PRM	Performance Report Message
	PS	Protection Switching
	PSAP	Public Safety Answering Point
	PSD	Protection Switching Duration
	PSPDN	Public Switched Packet Data Network
	PT	Path Termination
	PTE	Path Terminating Equipment
	PTT	Postal, Telegraph & Telephone administration
	PU	Physical Unit
	PVN	Private Virtual Network
	P-Bit CV	Parity-Bit Code Violation
Q	**QRS**	Quasi Random Signal
R	**RAI**	Remote Alarm Indication
	RBOC	Regional Bell Operating Company
	RDI	Remote Deficit Indication
	RHC	Regional Holding Company
	RTMP	Routine Table Maintenance Protocol
	RZ	Return to Zero

S

SA	Source Address
SA	ISA System Address bus (SA0 - SA19)
SAA	Systems Applications Architecture
SAPI	Service Access Point Identifier
SARTS	Switched Access Remote Test System
SAS	Single Attached Station
SCCP	Signaling Connection Control Part
SCO	Serving Central Office
SDH	Sychronous Digital Hierarchy
SDLC	Systems Data Link Control (protocol, IBM HDLC)
SEF	Severly Errored Frame
SEF	Source Explicit Forwarding
SEFE	Severly Errored Framing Event
SEFES	Severly Errored Framing Event Seconds
SEFS	Severly Errored Framing Seconds
SES	Severly Errored Seconds
SF	Superframe Format
SFD	Start of Frame Delimiter
SLAC	Subscriber Line Access Circuit / Card
SLIC	Subscriber Line Interface Circuit / Card
SLIP	Serial Line Internet Protocol
SMAS	Switched Management Access System
SMB	Server Message Block
SMDI	Simplified Message Desk Interface
SMDS	Switched Multimegabit Data Service
SMS	SONET Management Subnetwork
SMTP	Simple Mail Transfer Protocol
SNA	Systems Network Architecture
SNADS	SNA Distribution Services
SNMP	Simple Network Management Protocol
SOF	Start Of Frame
SONET	Sychronous Optical NETwork
SP	Signaling Point
SPE	Synchronous Payload Envelope
SPP	Sequenced Packet Protocol
SQE	Signal Quality Error (Heartbeat)
SS6	Signaling System 6
SS7	Signaling System 7
SSCP	System Service Control Point
STA	Spanning Tree Algorithm
STDM	Statistical Time Division Multiplexing
STE	Section Termination Equipment
STM	Synchronous Transfer Mode
STP	Screened, Twisted Pair (cable)
STP	Shielded Twisted Pair
STP	Signal Transfer Point

	STS	Synchronous Transport Signal
	STS-1	Synchronous Transport Signal - level 1
	STS-n	Synchronous Transport Signal - level n
T	**TA**	Technical Advisory
	TA	Terminal Adapter
	TCAP	Transaction Capabilities Application Part
	TCM	Time Compression Multiplexing
	TCP/IP	Transmission Control Protocol/Internet Protocol
	TDM	Time Division Multiplexing
	TDR	Time Domain Reflectometer (AUI only)
	TE-1	ISDN compatible Terminal Equipment
	TE-2	Non ISDN compatible Terminal Equipment
	TEI	Terminal Endpoint Identifier
	TIA	Telecommunications Industry Association
	TIC	Token ring Interface Coupler
	TL1	Transaction Language 1
	TLB	Test Loop Back
	TMN	Telecommunications Management Network
	TOP	Technical & Office Protocol
	TR	Technical Reference
	TSR	Terminate and Stay Resident
	TUP	Telephone User Part
U	**U bits**	User bits
	UA	User Agent
	UAS	UnAvailable Seconds
	UAT	UnAvailable Time
	UDI	Unrestricted Digital Information
	UDLC	Universal Digital Loop Carrier
	UI	Unit Interval
	UNMP	Unified Network Management Architecture
	UTP	Unshielded Twisted Pair
	UTP	Un-screened, Twisted Pair (cable)
V	**V bit**	Validity bit
	VAS	Value Added Service
	VT	Virtual Terminal
	VT	Virtual Tributary
	VTAM	Virtual Terminal Access Method
	VTn	VT of size n (Currently n = 1.5, 2, 3, 6)
W	**WAN**	Wide Area Network
	WATS	Wide Area Telecommunications Service
	WP	Working Paper

X	**XNS**	Xerox Network Systems
Z	**ZBTSI**	Zero Byte Time Slot Interchange

CONTENTS

PRODUCT CATEGORY LEVELS

Crystal's integrated circuit (IC) products are fabricated, assembled and tested either in-house or through one or more subcontractors. Qualification and manufacturability criteria are defined for each of four product category levels achievable during the product life cycle of an IC. Products are classified by the most stringent category level requirements met. Crystal's goal is to achieve Level I (World-Class) status for the majority of its product families. The product category levels are:

Level IV:	Engineering Prototype (EP) Release
Level III:	Production Level III
Level II:	Production Level II
Level I:	World Class

Level IV -- Engineering Prototype Qualification (EP)

Level IV is the first qualification level for IC products. It is used for early sampling and risk production builds. Qualification tests to achieve Level III begin shortly after the receipt of first functional devices. Level IV packaged devices are marked with an additional "EP".

Level III -- Production Level III

Level III is the second qualification level for IC products. This level is applicable to devices which are on track to achieving a Production Level II qualification and provides an interim reduction in the risk of substandard product shipments to customers. Comprehensive production test programs (with guardbands) are used for testing Level III products. Characterization of initial products is complete. Qualification tests have been completed per the criteria shown in the Qualification Criteria Table at the front of this databook.

Level II -- Production Level II

Level II is the high volume production qualification level for IC products. Level II products have met the goals for sustainable manufacturability and reliability by passing a comprehensive series of qualification tests, completing product documentation, and demonstrating product performance through detailed characterization.

Level I -- World Class Products

Level I is the highest level attainable for any product family. Qualification tests for Level I involve routine monitoring of ramped product families over a period of time to measure increasingly stringent reliability and quality levels that require a substantial number of devices and device-hours. Additionally, sources of variation throughout the manufacturing process (fab, assembly and test) are monitored and reduced over time following industry standard learning curves. This provides a statistical, pro-active approach to direct improvements in reliability performance and outgoing quality. It is the goal of every product family to achieve Level I status.

DEFINITION OF DATA SHEET TYPES

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

I. Product Preview

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

II. Preliminary Product Information

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pinout diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

III. Final Data Sheet

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.

RADIATION RESISTANCE PERFORMANCE

Crystal products are manufactured using various CMOS technologies. While not able to withstand large doses of radiation, our products are suitable for operation in low dose applications. Indeed, the self calibrating architecture of many of the A/D Converters is able to compensate for the effects of radiation.

Crystal will assist customers to test parts for radiation resistance by supplying free, data-logged parts. In exchange, we would like the parts returned to us, so that we can measure their post-radiation performance. In addition, we would like a copy of any report that is generated, along with permission to publish the report for other customer's information.

Several customer's have already undertaken radiation testing of our A/D Converters. Please contact the factory for the latest information and copies of the radiation performance reports.

RELIABILITY METHODS

I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

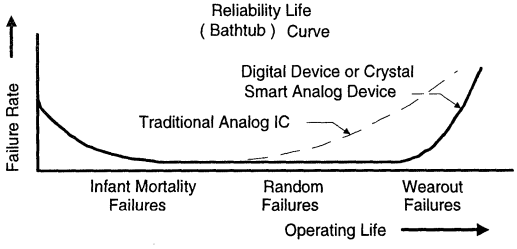

Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to- digital converter's linearity error stability is specified at ± .00075 % per 1000 hours at 25 °C. Stability degradation at 70 °C is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. Some of Crystal's acceptance criteria and goals are as described in the Qualification Criterion Table in section 1 of this data book.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or prescreening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Infant mortality (48 hrs at 125 °C), early operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported . Infant mortality life simulates approximately 3-4 months in the field at 55 °C and is reported as a percent. Early and Long term life simulate the total failures seen in the field and are expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of early and long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

Autoclave

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition B (-55 °C to +125 °C) or C (-65 °C to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a fluorocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with fluorocarbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

Electrostatic Discharge

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of 200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/µs and a 0 to 5 V risetime of less than 15 ns. Ground, V_{ss}, and the pin under test are connected to ground. The supply current is monitored for excessive current.

III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other temperatures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$F.R. = \frac{N}{D \bullet H} \quad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by 10^9 we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$FITS = (F.R.)(10^9) \quad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor, F_a. One hour of device operation at temperature T_1 is equivalent to F_a hours of operation at temperature T_2. The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{-\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \quad (3)$$

where k = Boltzman's Constant (8.63×10^{-5} eV/°K) and T_1 is the accelerated stress junction temperature and T_2 is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures, T_1 and T_2, should be used in determining acceleration factors. This temperature can be obtained from the equation below.

$$T_j = T_a + \theta_{ja}P_d \quad (4)$$

where T_a is the operating ambient temperature

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and θ_{ja} is the package thermal dissipation (°C/ W) and P_d is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15 °C, whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160 °C to 60 °C and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10 °C higher than the ambient which results in a junction temperature change from 135 °C to 35 °C. This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

TEMPERATURE CHANGE	TYPICAL ACCELERATION FACTOR (.7 E.A.)
125 → 70 °C	26.3
125 → 55 °C	77.5
125 → 25 °C	933.0
135 → 35 °C	636
160 → 60 °C	277

TABLE 2
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES (E.A. = .7 eV)

E.A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGIES (125 °C → 70 °C)

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by some other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$\text{FITS} = \frac{10^9 N}{DHF_a} \qquad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25°C can be calculated by substituting in equation (5) above:

N = 108
D•H = 28,475,272
Fa = 641 (Assuming .7 eV and stress temperature of 125°C, using junction temperature derating)

D•H is the summation of the devices stressed at each readpoint multiplied by that number of stress hours.

Substituting we get:

$$\text{FITS } 25°C = \frac{(10^9)(108)}{(28{,}475{,}272)(641)} = 5.9 \text{ FITS}$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull distribution has both a shape parameter, β, and a scaling parameter, α. This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make

this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF) f(t) is the probability of failure between time t and t + dt.

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function, R(t), and the instantaneous failure rate function, h(t), therefore:

$$f(t) = h(t)R(t) \qquad (7)$$

The Reliability function is found by integrating the Weibull PDF from t to ∞. This function is the probability that a device will survive to time t.

$$R(t) = \int_{t}^{\infty} f(t')dt' = e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time t and t+dt:

$$h(t) = -\frac{1}{R}\frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \qquad (9)$$

The Reliability function is used to calculate the shape parameter, β, and the time scale parameter, α. The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A β of 1 indicates a uniform failure rate, β > 1 indicates wearout and β < 1 indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of R(t). Failure times and R(t) values can be combined to estimate α and β. We first take the natural logarithm of both sides of equation (8).

$$\ln\left(\frac{1}{R(t)}\right) = \frac{t^{\beta}}{\alpha}$$

We again take the natural logarithm and obtain:

$$\ln\left[\ln\frac{1}{R(t)}\right] = \beta \ln(t) - \ln(\alpha) \qquad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Some semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining α and β.

Once the parameters α and β for the Weibull distribution are known we utilize R(t) to calculate FITS. Crystal uses a 10 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

t_{10} = 10 yrs = 87,600 hours
t_1 = 48 hours

The number of devices that will fail in the ten year lifetime following burn-in is given by:

$$N = D\,[R(t_1) - R(t_1 + t_{10})] \qquad (11)$$

where D is the total number of devices stressed. The number of device-hours accumulated in 10 years can be estimated by counting the devices surviving after 10 years.

$$DH \geq D \bullet R(t_1+t_{10}) \bullet t_{10} \qquad (12)$$

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Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$FITS \leq 10^9 \frac{D\,[\,R(t_1) - R(t_1 + t_{10})]}{D \bullet R(t_1 + t_{10}) \bullet (t_{10})}$$

$$= \frac{10^9\,[\,R(t_1) - R\,(t_1+t_{10})]}{R(t_1+ t_{10}) \bullet (t_{10})} \qquad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors, F_a, from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace $R(t_1 + t_{10})$ by $R(t_1 + t_{10}/Fa)$. Note that the device lifetime t_{10} is still 10 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the second quarter of 1993, yields a failure rate at 25 °C of 8.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 60% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85°C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These stresses are experiments in which a given device will either pass or fail. Test results can be expressed as a simple failure rate - the number of failing devices divided by the total number of devices. However, the true failure rate is usually very small, so often there will be no failures observed. Instead of reporting an observed failure rate of zero, a confidence bound on the true failure rate is determined. Crystal uses a 90% confidence level in a standard formula to determine the test results for environmental stresses.

$$FR = \frac{\chi^2\,(2f+2)}{2n} \qquad (14)$$

The failure rate, FR, is computed by finding an upper bound confidence interval from a standard chi-squared table and dividing it by 2n, where n is the number of parts in the test, and f is the number of failures observed. $\chi^2(2f+2)$ is the right endpoint of the interval starting at zero which spans 90% of the area under the chi-squared curve with $2f+2$ degrees of freedom. This formula results from a Poisson approximation to the Binomial distribution, which is appropriate when the Binomial distribution is heavily skewed towards zero. A chi-squared value arises as an easy way to compute Poisson probabilities. This calculation agrees with the widely accepted lot

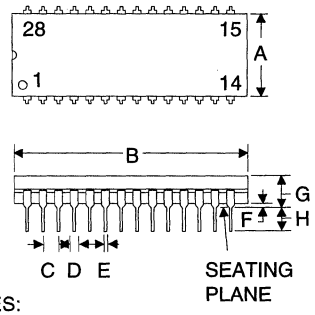
tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

MECHANICAL DATA

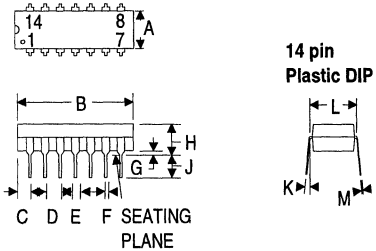


28 pin
CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

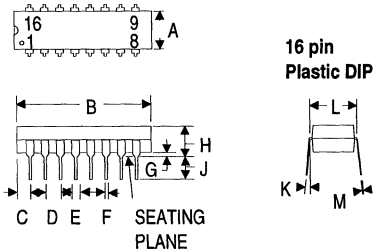


14 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.12	1.78	0.044	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	7.37	8.12	0.290	0.320
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

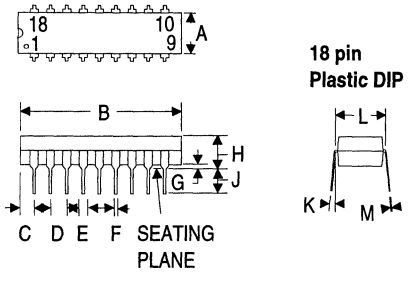


16 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.93	19.93	0.745	0.785
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	0.89	1.65	0.035	0.065
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	7.62	8.25	0.300	0.325
M	0.20	0.38	0.008	0.015

NOTES:

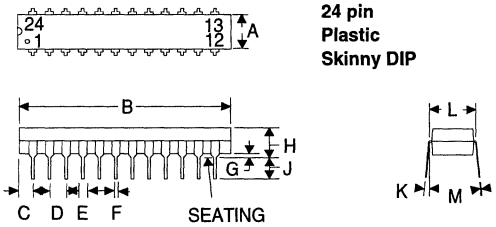
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



18 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	0.76	1.65	0.030	0.065
D	2.54 BSC		0.100 BSC	
E	1.27	1.65	0.050	0.065
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	7.62	8.25	0.300	0.325
M	0.20	0.38	0.008	0.015

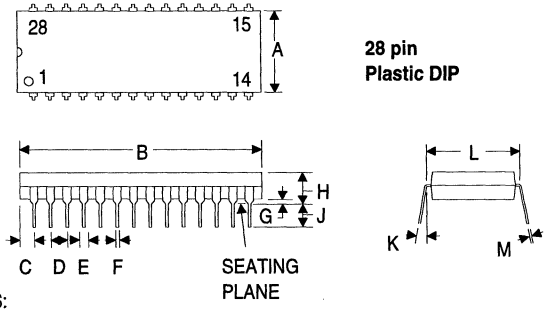
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.29	0.065	0.090
D	2.54 BSC		0.100 BSC	
E	1.02	1.65	0.040	0.065
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	7.62	8.25	0.300	0.325
M	0.20	0.38	0.008	0.015

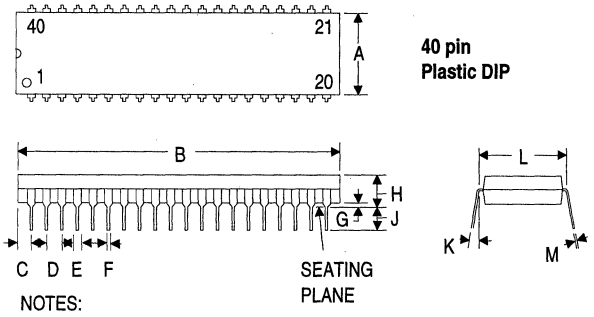
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.29	0.065	0.090
D	2.54 BSC		0.100 BSC	
E	1.02	1.65	0.040	0.065
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	15.24	15.87	0.600	0.625
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



40 pin
Plastic DIP

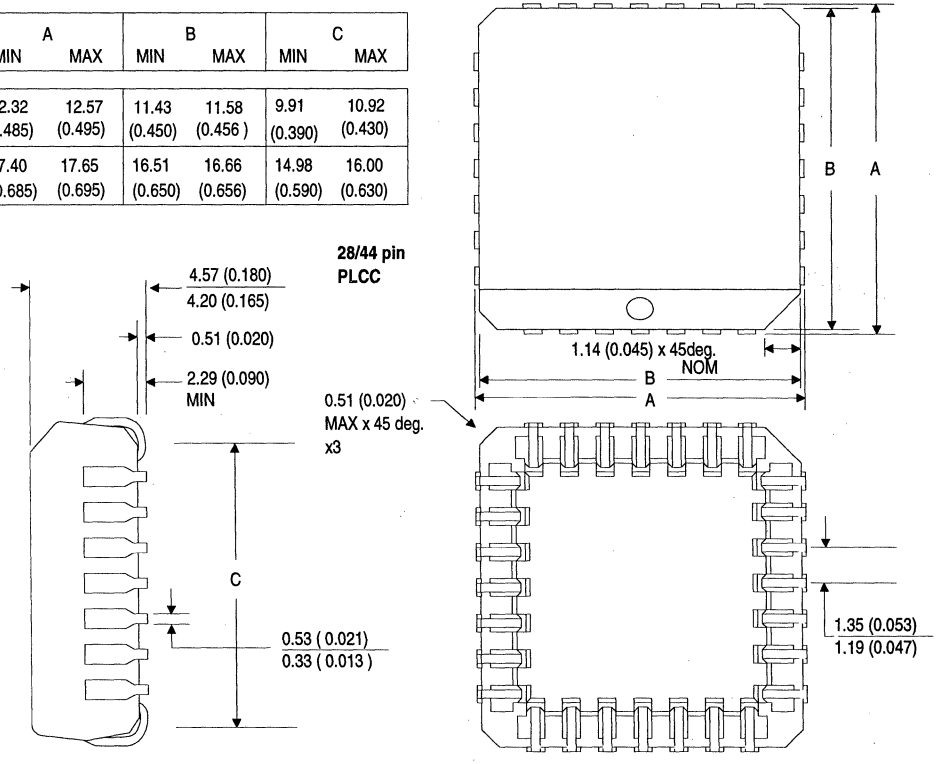
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.71	2.035	2.075
C	1.65	2.41	0.065	0.095
D	2.54 BSC		0.100 BSC	
E	1.02	1.65	0.040	0.065
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	3.18	3.81	0.125	0.150
K	0°	15°	0°	15°
L	15.24	15.87	0.600	0.625
M	0.20	0.38	0.008	0.015

NOTES:

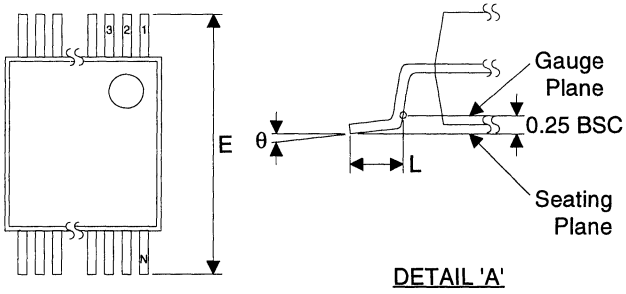
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)

28/44 pin
PLCC

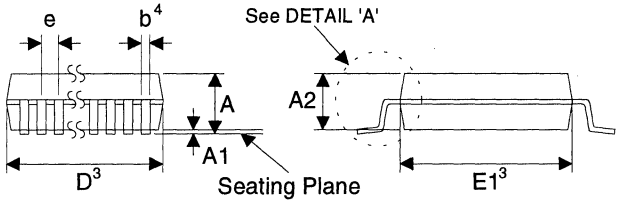


ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.



DETAIL 'A'

TOP VIEW



SIDE VIEW

END VIEW

Notes:

1. Dimensioning and tolerance per ANSI.Y14.5M-1982.
2. Symbols are defined in the "MO Series Symbol List" in section 2.2 of JEDEC Publication 95.
3. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20mm per side.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from lead tips.

	MILLIMETERS			
DIM	MIN	NOM	MAX	Note
A	-	-	2.13	
A1	0.05	-	0.25	
A2	1.62	1.75	1.88	
b	0.22	-	0.38	4, 5
D	see other table			3
E	7.40	7.80	8.20	
E1	5.00	5.30	5.60	3
e	0.65 BSC			
L	0.63	0.90	1.03	
N	see other table			
θ	0°	4°	8°	

	D			
N	MIN	NOM	MAX	Note
8	2.70	3.00	3.30	3
14	5.90	6.20	6.50	3
16	5.90	6.20	6.50	3
18	6.90	7.20	7.50	3
20	6.90	7.20	7.50	3
22	7.90	8.20	8.50	3
24	7.90	8.20	8.50	3
28	9.90	10.20	10.50	3
30	9.90	10.20	10.50	3

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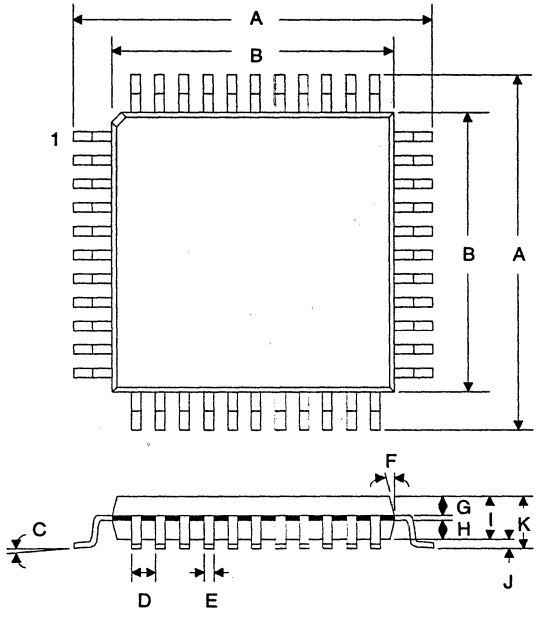
SSOP Package Dimensions

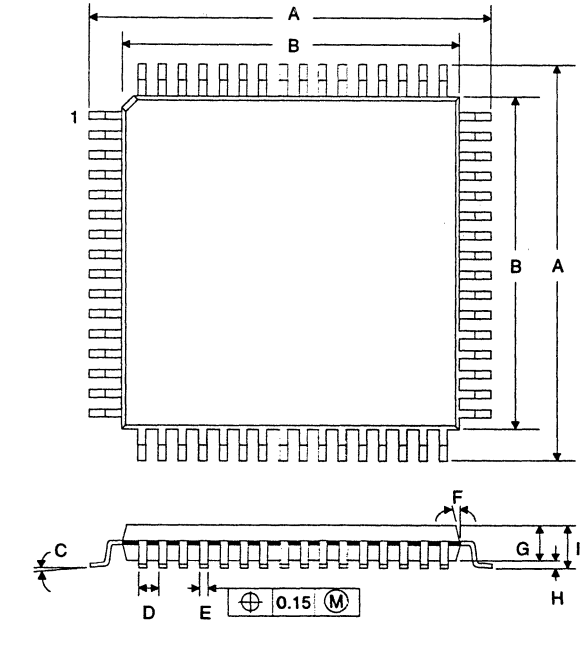
44 PIN QUAD FLATPACK



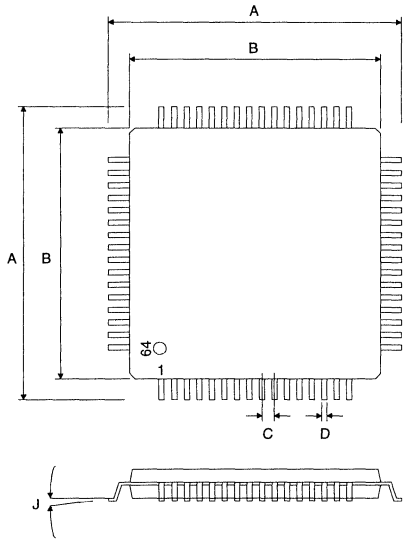
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026

0.102 MAX
Lead Coplanarity

QUAD FLATPACK

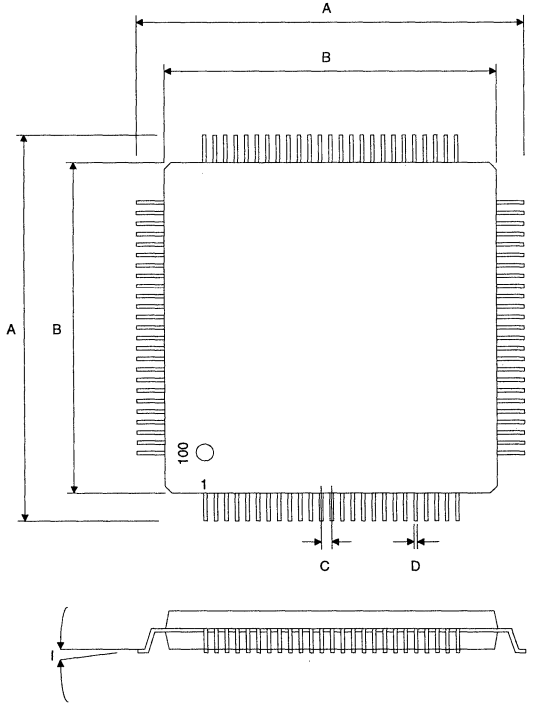


	64 Pin Dimensions			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.9	17.5	0.66	0.69
B		14		0.55
C	0°	5°	0°	5°
D	0.80 BSC		0.031 BSC	
E	0.25	0.45	0.010	0.018
F		12°		12°
G	2.54	2.90	0.100	0.114
H		0.1		0.004
I		3.05		0.120
J		1.6		0.063
K	0.5	0.11	0.020	0.004
L	0.12	0.22	0.005	0.009



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.70	12.30	0.461	0.484
B	10.00	10.00	0.394	0.394
C	0.40	0.60	0.016	0.024
D	0.14	0.26	0.006	0.010
E	-	1.66	-	0.068
F	0.00	-	0.00	-
G	0.35	0.70	0.014	0.028
H	0.077	0.177	0.003	0.007
J	0°	12°	0°	12°

64 pin
TQFP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.70	16.30	0.618	0.642
B	13.90	14.10	0.547	0.555
C	0.40	0.60	0.016	0.024
D	0.14	0.26	0.006	0.010
E		1.66		0.065
F	0.00		0.000	
G	0.30	0.70	0.012	0.028
H	0.077	0.177	0.003	0.007
I	0°	12°	0°	12°

100 pin
TQFP

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• Notes •

CONTENTS

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