VIC64
CY7C964

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VIC64 Design Notes

Introduction

Cypress Semiconductor has supplemented its Bus Interface product family with the VIC64, a member of the industry-standard VIC family of VMEbus interface products. The VIC64 implements 64-bit wide block transfers, in addition to 32- and 16-bit block transfers and 32-, 16-, and 8-bit single-cycle transfers, all using the same backplane hardware. VIC64 is software and hardware compatible with the VIC068A VMEbus Interface Circuit.

This document provides the designer with the information needed to evaluate and develop VIC64-based boards. You should have already read the User's Guide for the VIC068A. This document provides information on the enhancements found within the VIC64. Another recent addition to Cypress's Bus Interface Products portfolio, the CY7C964 Bus Interface Logic Chip, is described later in this book.

Like the Cypress VIC068A, the VIC64 contains all the circuitry necessary to manage VMEbus transfers, either as a slave or a master. It can also be programmed as the VMEbus system controller. The VIC64 contains circuitry intended to minimize the problems associated with the development of a VMEbus interface such as an interrupt controller, a DMA controller, a DRAM refresh controller, and many other features normally found on VMEbus boards. The VIC64 is a logical extension to the capabilities of the VIC068A, the industry-standard VMEbus Interface Controller chip, and it is fully compatible with the VIC068A.

The primary benefit of using the VIC64 is that you can perform 64-bit VMEbus transfers. The VIC64 also contains some enhancements to the VIC068A, including some performance improvements and additional features.

A board that has been designed to use the VIC068A is not likely to implement D64 VMEbus transfers, but there are several reasons why a user may choose to replace the VIC068A with a VIC64. For example, to take advantage of the enhancements of the VIC64, or to evaluate the device and use an existing board to speed the evaluation.

Compatibility

All pin assignments and register assignments are the same as those of the VIC068A, therefore the VIC64 will work flawlessly when used to replace a VIC068A. In fact, several of the VIC068's functions have been enhanced in the VIC64, allowing VIC068A applications to run faster in some cases. Naturally, some attention must be paid to the additional controls for the improved functionality to ensure that the original hardware and software supports the improvements. Therefore, several bits have been added to the VIC068A registers to control the enhancements. They map into the unused bits within the VIC068A register space; assuming that the VIC068A developer has not inadvertently set the bits, VIC068A code will run on the VIC64 without modification.

To add 64-bit functionality to the VIC family and still retain plug compatibility, the SCON* pin has been modified in the VIC64. Whereas previously it performed only the input function of selecting VIC068A to be the system controller, in VIC64 the pin is sensed and latched during reset to determine whether the system controller function is enabled. After reset the pin becomes an output to control external circuitry during 64-bit transfers. The new name for the pin is SCON*/D64. If you simply replace the VIC068A with the VIC64, the VIC64 will function in an identical manner to the VIC068A, whether it is the system controller or not. It is recommended that the VIC64 SCON*/D64 pin be connected via a resistive pull-down/up of greater than 4.7kΩ to enable/disable the system controller function.

64-Bit Operation

VMEbus Specification

The primary reason for the development of the VIC64 was to provide users with the capability to perform 64-bit-wide data transfers in a manner consistent with the goals of the proposed 64-bit VMEbus specification, more commonly known as the VME64 specification. Although at the date of this publication the specification was not finalized, the protocol for 64-bit MBLT (Multiplexed Block Transfer) is well known and stable. The VIC64 implements this protocol.

Address Modifier Codes

VIC64 responds as a slave to the address modifier (AM) codes associated with MBLT transfers as follows:

3C, 38, 0C, 08; Performs D64 operation as implied by the actual AM code, and the contents of the Slave Configuration Registers $C3 and $CB, and Block Transfer Definition Register $AB.

00 - 07; No response: these codes are associated with 64 bit address operations, and the VIC64 does not support 64-bit address operations.

As a master, VIC64 will use the MBLT protocol to transfer data if the appropriate conditions occur:

AM codes 3C, 38, 0C, 08 are selected, and the appropriate bits of the configuration registers are set (see later for exact details).

In summary, VIC64 performs A32/D64 operations in addition to the D8/16/32 single cycles and A16/24/32..D16/32 block transfers performed by VIC068A.

Boundary Crossing

There are several implications of the 64-bit VMEbus protocol and the requirement for compatibility that you should consider. The VIC64, being a 144-pin device, can connect to only the lower byte of the VMEbus address. For block transfers other than D64 transfers, the VMEbus specification requires that the VMEbus address be rebroadcast at 256-byte boundary crossings; this quantity maps neatly into the byte of address that the VIC64 can monitor. MBLT transfers, however, are required to rebroadcast the address only at 2-Kbyte boundaries. VIC64 has no means of determining how the starting address of a master block transfer relates to the 2K boundary (it has access to only the lower 8 address bits), and therefore VIC64 rebroadcasts the address at every 256-byte boundary. This is still compatible with the specification, but has a small impact on the sustained transfer rate. If you wish to take advantage of the increased performance of 2-Kbyte boundaries, then VIC64 can be programmed to rebroadcast the address every 2048 bytes, and the starting address must then be aligned on a 2-Kbyte boundary.

External Circuit Complexity

The VIC64 is a flexible building block that can be used in many different configurations. The VMEbus specification is written to allow many levels of circuit complexity to conform to the specification. Such circuitry may include slave address decode circuitry, local DMA transfer, slave read modify cycles, and more. The VIC64 and the VIC068A provide dual-path operation, a mechanism whereby the local bus master can perform single-cycle VMEbus operations during the time that the VMEbus is between block transfer bursts (interleave period). They also provide a mechanism allowing master write-posting, and slave read modify cycles to occur concurrently without harming the posted data. All this circuitry must be duplicated externally for the higher-order data bytes if you want these features.

You may choose to implement only those features that your system requires, thereby simplifying the necessary external circuitry. Alternatively, the user may decide to use the companion device, the CY7C964, and gain access to all the features using only three small devices. The CY7C964 is described in the second half of this publication.

VIC068A User's Guide: Additional Information

The following sections are related to the *VIC068A User's Guide*. The chapter numbers are those sections of the *VIC068A User's Guide* that require clarification or modification for the VIC64. All other information in the *VIC068A User's Guide* is applicable to the VIC64.

VIC64 Signal Description (Chapter 2)

All pins are identical to those of the VIC068A with the following exception:

SCON*/D64

Input:	Yes
Output:	Yes
Drive:	16mA

This is the dual-function signal by which the VIC64 determines whether system controller functions are required, and by which the VIC64 controls external logic during 64-bit VMEbus transfers. During the time that IRESET* is asserted, this pin is the SCON* input whose state is latched internally when IRESET* goes inactive. A Low state causes VIC64 to become the VMEbus system controller. During the time that IRESET* is inactive, this pin becomes the D64 output whose state is normally Low, becoming High only during the Data Phase of D64 transactions.

System Controller Operations (Chapter 4)

The VIC64 functions identically to VIC068A as a system controller, except that the SCON* pin of the VIC068A has been renamed to be SCON*/D64 on the VIC64. During the period that IRESET* is asserted (Low), VIC64 assumes that the pin is an input whose state is latched on the rising edge of IRESET*. The latched state is then used to determine whether the VIC64 is the system controller: if the state is Low, then the VIC64 is the system controller.

SCON*/D64 becomes an output after the rising edge of IRESET*; the state of the output is used to enable 64-bit data transfers (Chapter 10, Block Transfer Functions contains information on this operation).

VMEbus Master Operations (Chapter 5)

There is no provision for single-cycle D64 transfers in the VMEbus specification. The VIC64 does not perform single-cycle 64-bit transfers.

The VIC64 uses the same pins and register bits as the VIC068A to configure and select 64-bit block transfers. The release modes are identical, and the address broadcast phase is identical to the VIC068A, except that the AM code reflects the D64 transaction (see Table 1).

Table 1. Master Transfer AM Code Control Map for D64 Operations

VIC64 Master Access Inputs				VIC64 AM Code Output	
ASIZ1/0	Address Size	Blk	FC2	Operation Type	AM[5:0]
01	A32 addressing	Yes	0X	User block	$08
			1X	Supervisory block	$0C
11	A24 addressing	Yes	0X	User block	$38
			1X	Supervisory block	$3C

As the VIC64 has an identical local bus interface to that of the VIC068A, some mention must be made of the protocol used to transfer the 64-bit VMEbus data to the 32-bit local bus. First, it should be noted that data byte D0 is transferred on VMEbus address [A31:A24], and byte D7 is transferred on VMEbus data [D7:D0]. Two local transactions are required for each VMEbus transaction. For maximization of performance a pipelined architecture is used. The VIC64 provides the appropriate timing for latch controls to implement the pipe externally for those bytes that the VIC64 itself does not connect to.

D64 Master Write Cycles

In the case of master write cycles, the first local cycle fetches the first [D0−D3] longword and the VIC64 places it into a two-stage pipe: the next local cycle fetches the next longword and presents it to the VMEbus data bus, while the piped data is presented to the VMEbus address bus. Then the next local cycle can commence without waiting for the completion of the VMEbus cycle, as the first stage of the pipe is now free. See the timing diagrams for full details of this operation.

D64 Master Read Cycles

In the case of Master Read Cycles, 64 bits of VMEbus data are latched under the control of VIC64. The [D4−D7] long-word is placed into a two-stage pipe, while the [D0−D3] long-word is presented to the local bus. After the local bus write cycle, the piped data is then presented to the local bus, and the next VMEbus cycle can commence as the first stage of the pipe is now free. See the timing diagrams for full details of this operation.

VMEbus Slave Operations (Chapter 6)

Upon detecting SLSEL0* or SLSEL1* asserted, the VIC64 behaves in an identical manner to the VIC068A except that if the AM code for the slave transaction is $08, $0C, $38, or $3C, the VIC64 configures itself for a D64 slave block transfer (see Table 2).

Table 2. Slave Transfer AM Code Control Map for D64 Operations

VIC64 AM Code Inputs		VIC64 Slave Access Outputs		
Operation Type	AM[5:0]	Address Size	Block Transfer	FC2/1
User block	$08	A32 addressing	Yes	00
Supervisory block	$0C			
User block	$38	A24 addressing	Yes	00
Supervisory block	$3C			

D64 Slave Read Cycles

As in the case of master write cycles, the first local cycle fetches the first [D0−D3] longword and the VIC64 places it into a two-stage pipe. The next local cycle fetches the next longword and presents it to the VMEbus data bus, while the piped data is presented to the VMEbus address bus. Then the next local cycle can commence without waiting for the completion of the VMEbus cycle, as the first stage of the pipe is now free.

D64 Slave Write Cycles

As in the case of Master Read Cycles, 64 bits of VMEbus data are latched under the control of VIC64. The [D4−D7] long-word is placed into a two-stage pipe, while the [D0−D3] longword is presented to the local bus. After the local bus write cycle, the piped data is then presented to the local bus, and the next VMEbus cycle can commence because the first stage of the pipe is now free.

Interrupts (Chapter 9)

The VIC64 can be programmed to perform either D8, D16, or D32 interrupt acknowledge cycles. The method by which this is performed is simply to drive the values on SIZ1/0, in a similar fashion to a master read or write operation. The SIZ1/0 lines are sensed by the VIC64 following the assertion of FCIACK* by the local processor. Note that no provision is made for non-aligned status/ID vector: The VIC64 enables the appropriate local bus drivers for either 8, 16, or 32 bit Status/ID.

Table 3. VIC64 Interrupt Acknowledge Cycle Selection

SIZ1/0	VMEbus Data Width
00	32
01	8
10	16
11	32

VIC64 Block Transfer Functions (Chapter 10)

As the VIC64 is a superset of the VIC068A, all the VIC068A block transfer functionality is reproduced in the VIC64. The additional features provided by the VIC64 are D64 transfers and performance enhancements.

D64 Transfers, VMEbus Boundary Crossing

The VME64 specification allows D64 block transfers to exceed the 256-byte boundary-crossing limitation that the original VMEbus specification contains. The new specification allows for 2-Kbyte boundaries. As the VIC64 can only discern 8 bits of address, it has no means of determining which 256-byte boundary is the 2048-byte boundary, and therefore the VIC64 rebroadcasts the address every 256 bytes unless BTDR[7] is set: this bit causes the address to be rebroadcast on 2-Kbyte boundaries, but the VIC64 then assumes that the transfer starts on the 2-Kbyte boundary.

Miscellaneous Features (Chapter 12)

Selection of System Controller Functionality

The VIC068A is configured to be system controller by strapping SCON* Low. In VIC64, the SCON*/D64 pin performs this function: the state of the pin is latched during any of the possible Reset operations, and this state determines whether VIC64 is system controller. Following the Reset operation, the SCON*/D64 pin becomes an output whose state controls the external circuitry (such as the CY7C964) used during the data phase of D64 transfers. The detailed timing of this operation depends upon internal states such as DRAM refresh timing, in addition to the external stimuli such as SYSRESET*, IRESET*, and IPL0*. Use of an external pull-up/pull-down resistor to determine the state of the SCON* pin during the Reset operation is all that is required to ensure correct operation.

Enhanced Turbo Mode

In addition to the use of ICR[1] another performance enhancement is possible in the VIC64. Setting BTDR[5] reduces the DSACK*-to-DTACK* time defined in the slave select control registers by 0.5 clock period for both master and slave block transfers. The reduced times are 0, 1.5, 2, 2.5,...,8.5 clock periods. See the AC Timing Parameters section for details on which times are affected by this bit.

Register Map and Descriptions (Chapter 13)

There are some differences between the VIC068A and the VIC64 register assignments and contents.

Interprocessor Communications Register 5

Name: ICR5

Address: $77

Description: This register provides the VIC64 revision number.

Block Transfer Definition Register

Name: BTDR

Address: $AB

Description: Configures master block transfers for boundary crossing, dual-path and user defined address modifiers. There are four additional bits defined for VIC64:

Bit 4
(0/0/0)

Enables D64 Master Operations when BTCR[6] is set

Bit 5
(0/0/0)

Enables Accelerated Block Transfer Operations as discussed above.

Bit 6
(0/0/0)

Enables D64 Slave Operations

Bit 7

Enables 2-k-byte boundary crossing for D64 Master Operations. If this bit is set, VIC64

(0/0/0)

assumes that the transfer is aligned to a 2-k-byte boundary.

Release Control Register

Name: RCR

Address: $D3

Description: This register configures the VMEbus release mode, and the burst length for
             block transfers with local DMA.

Bits 5-0   For MBLT operations (D64 transfers), the burst length is 4 times the actual field contents.
(0/0/0)   A value of 0 is interpreted to mean 4 x 64.

For non-MBLT operations, the burst length is simply the field contents. A value of 0 in this field is interpreted to mean 64.

Block Transfer Length Register 2

Name: BTLR2

Address: $E7

Description: This register provides the most significant byte of the 24-bit value used to determine the
             byte count for block transfers with local DMA.

Bits 7-0   Bits 23:16 of the block transfer length.
(0/0/0)

AC Performance Specifications (Chapter 15)

AC Timings for D64 Operations (Commercial)[1]

Operation		Min.	Max.
Master D64 Block Transfer with Local DMA (Initiation Cycle)[2]			
A1	MWB*[0] & PAS*[0] & DS*(0) to BRi*[L]	T+7	2T+32
A2	MWB*[0] & PAS*[0] & DS*(0) to LADO[H]	T+9	2T+31
A3	MWB*[0] & PAS*[0] & DS*(0) to BLT*[L]	T+9	2T+26
A4	MWB*[0] & PAS*[0] & DS*(0) to DSACK1*[L]	T+11	2T+46
A5	MWB*[0] & PAS*[0] & DS*(0) to DSACK0*[L]	T+11	2T+46
Master D64 Block Transfer Address Broadcast Cycle[2]			
B1	DTACK*[0] to LBR*[L]	24	65
B2	DTACK*[0] to DSi*[H]	8	24
B3	DTACK*[0] to SCON*/D64[H]	16	59
Master D64 Block Transfer with Local DMA (Write)			
First Longword Fetch			
C1	DSACKi*[0] and DS*[L] to DS*[H][2, 3, 4]	MBAT0+8	MBAT0+T+36
C2	DSACKi*[0] and DS*[L] to LEDO[H] [2, 3, 4]	MBAT0+7	MBAT0+T+33
C3	DSACKi*[0] and DS*[L] to LA(7:0)[2, 3, 4]	MBAT0+.5T+9	MBAT0+2T+30
C4	DS*(H) to DS*[L][2, 3, 4, 5]	T+8	3T+31
Second Longword Fetch			
C5	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	MBAT1+14	MBAT1+T+46
C6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	MBAT1+11	MBAT1+T+37
C7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	MBAT1+.5T+9	MBAT1+2T+31
C8	DSACKi*[0] and DS*[L] to DSi*[L] [6]	MBAT1+3T+12	MBAT1+4T+32
C9	DSACKi*[0] and DS*[L] to LEDO[L] [4]	MBAT1+16	MBAT1+T+56
C10	DS*(H) to DS*[L] [2, 4, 5]	T+8	3T+31
C11	DTACK*[0] to DSi*[H]	7	22
C12	DTACK*[0] to DENO*[H] [2]	8	24
Master Block Transfer with Local DMA (Read)			
First Longword Write			
D1	LBG*[0] to LWDENIN*[L] [2]	2T+11	3T+41
D2	DTACK*[0] to LEDI[H] [7]	2T+6	3T+23
D3	DTACK*[0] to DSi*[H] [2, 7]	2T+9	3T+28
D4	DTACK*[0] to DS*[L] [7]	2T+13	3T+36
D5	DSACKi*[0] and DS*[L] to DS*[H] [2, 3, 4]	MBAT0+8	MBAT0+T+37

AC Timings for D64 Operations (Commercial)

	Operation	Min.	Max.
D6	DSACKi*[0] and DS*[L] to LEDI[L] [3, 4]	MBAT0+13	MBAT0+T+52
D7	DSACKi*[0] and DS*[L] to UWDENIN*[L] [3, 4]	MBAT0+8	MBAT0+T+35
D8	DSACKi*[0] and DS*[L] to LA(7:0) [2, 3, 4]	MBAT0+.5T+9	MBAT0+2T+29
D9	DSACKi*[0] and DS*[L] to DSi*[L] [3, 4]	MBAT0+22	MBAT0+T+56
D10	DS*[H] to DS*[L] [2, 4, 5]	T+8	3T+29
Second Longword Write			
D12	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	MBAT1+8	MBAT1+T+36
D13	DSACKi*[0] and DS*[L] to UWDENIN*[H] [2, 4]	MBAT1+16	MBAT1+T+56
D14	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	MBAT1+.5T+9	MBAT1+2T+29
D15	DSACKi*[0] and DS*[L] to LD(7:0) [2, 4]	MBAT1+.5T+12	MBAT1+2T+39
Master D64 Block Transfer with Local DMA (Boundary Crossing) [2]			
E1	DS*[0] to BLT*[H]	3	28
E2	DS*[1] to BLT*[L]	3	19
E3	DSi*[0] to LADO first transition	3	19
E4	DSi*[1] to LADO second transition	3	19
Slave D64 Block Transfer Address Broadcast Cycle [2]			
F1	DSi*[1] to LBR*[L]	11	36
F2	DSi*[0] to DTACK*[L]	2T+9	3T+28
F3	DSi*[1] to DTACK*[H]	9	28
F4	DSi*[1] to SCON*/D64[H]	10	33
F5	DSi*[0] and AS*[0] and SLSELi[0] to LADI[H]	1.5T+5	2T+25
Slave D64 Block Transfer (Write)			
First Longword Cycle			
G1	DSi*[0] to DS*[L] [2, 4]	3T+11	4T+38
G2	DSi*[0] to DTACK*[L] [7]	2T+9	3T+23
G3	DSi*[0] to LEDI[H] [2, 4]	T+11	2T+37
G4	DSACKi*[0] and DS*[L] to DS*[H] [2, 4, 8]	SBAT0+8	SBAT0+T+36
G5	DSACKi*[0] and DS*[L] to LEDI[L] [2, 4, 8]	SBAT0+13	SBAT0+T+52
G6	DSACKi*[0] and DS*[L] to UWDENIN*[L] [2, 4, 8]	SBAT0+8	SBAT0+T+31
G7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+9	SBAT0+2T+29
G8	DS*[H] to DS*[L] [2, 4, 5]	T+8	3T+31

AC Timings for D64 Operations (Commercial)

Operation		Min.	Max.
Second Longword Cycle [2, 4]			
G9	DSACKi*[0] and DS*[L] to UWDENIN*[H]	SBAT1+20	SBAT1+T+64
G10	DSACKi*[0] and DS*[L] to DS*[H]	SBAT1+11	SBAT1+T+34
G11	DSACKi*[0] and DS*[L] to LA(7:0)	SBAT1+.5T+9	SBAT1+2T+29
G12	DSACKi*[0] and DS*[L] to LD(7:0)	SBAT1+.5T+11	SBAT1+2T+40
Slave D64 Block Transfer (Read)			
First Longword Cycle			
H1	DSACKi*[0] and DS*[L] to LEDO[H] [4, 8]	SBAT0+7	SBAT0+T+36
H2	DSACKi*[0] and DS*[L] to DS*[H] [4, 8]	SBAT0+8	SBAT0+T+39
H3	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+9	SBAT0+T+29
H4	DS*[H] to DS*[L] [2, 4, 5]	T+8	3T+30
Second Longword Cycle			
H5	DSACKi*[0] and DS*[L] to LEDO[L] [4]	SBAT1+19	SBAT1+T+64
H6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	SBAT1+11	SBAT1+T+37
H7	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	SBAT1+24	SBAT1+T+72
H8	DSACKi*[0] & DS*[L] & DSi*[0] to DTACK*[L] [4]	SBAT1+13	SBAT1+T+33
H9	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	SBAT1+.5T+9	SBAT1+2T+29
H10	DS1/0*[1] to DENO*[H] [2]	6	21
Slave D64 Block Transfer (Boundary Crossing)			
H11	DS*[0] to LADI[L] [2]	11	26
H12	DS*[1] to LADI[H] [2]	6	13

AC Timings for D64 Operations (Industrial)

Operation		Min.	Max.
Master D64 Block Transfer with Local DMA (Initiation Cycle) [2]			
A1	MWB*[0] & PAS*[0] & DS*(0) to BRi*[L]	T+7	2T+33
A2	MWB*[0] & PAS*[0] & DS*(0) to LADO[H]	T+8	2T+32
A3	MWB*[0] & PAS*[0] & DS*(0) to BLT*[L]	T+8	2T+27
A4	MWB*[0] & PAS*[0] & DS*(0) to DSACK1*[L]	T+10	2T+48
A5	MWB*[0] & PAS*[0] & DS*(0) to DSACK0*[L]	T+10	2T+48
Master D64 Block Transfer Address Broadcast Cycle [2]			
B1	DTACK*[0] to LBR*[L]	20	69
B2	DTACK*[0] to DSi*[H]	7	26
B3	DTACK*[0] to SCON*/D64[H]	15	62

AC Timings for D64 Operations (Industrial)

Operation		Min.	Max.
Master D64 Block Transfer with Local DMA (Write)			
First Longword Fetch			
C1	DSACKi*[0] and DS*[L] to DS*[H] [2, 3, 4]	MBAT0+7	MBAT0+T+38
C2	DSACKi*[0] and DS*[L] to LEDO[H] [2, 3, 4]	MBAT0+6	MBAT0+T+35
C3	DSACKi*[0] and DS*[L] to LA(7:0) [2, 3, 4]	MBAT0+.5T+8	MBAT0+2T+32
C4	DS*(H) to DS*[L] [2, 3, 4, 5]	T+7	3T+32
Second Longword Fetch			
C5	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	MBAT1+13	MBAT1+T+48
C6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	MBAT1+10	MBAT1+T+39
C7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	MBAT1+.5T+8	MBAT1+2T+32
C8	DSACKi*[0] and DS*[L] to DSi*[L] [6]	MBAT1+3T+10	MBAT1+4T+33
C9	DSACKi*[0] and DS*[L] to LEDO[L] [4]	MBAT1+15	MBAT1+T+57
C10	DS*(H) to DS*[L] [2, 4, 5]	T+7	3T+32
C11	DTACK*[0] to DSi*[H]	6	23
C12	DTACK*[0] to DENO*[H] [2]	7	26
Master Block Transfer with Local DMA (Read)			
First Longword Write			
D1	LBG*[0] to LWDENIN*[L] [2]	2T+10	3T+43
D2	DTACK*[0] to LEDI[H] [7]	2T+5	3T+24
D3	DTACK*[0] to DSi*[H] [2, 7]	2T+8	3T+29
D4	DTACK*[0] to DS*[L] [7]	2T+12	3T+37
D5	DSACKi*[0] and DS*[L] to DS*[H] [2, 3, 4]	MBAT0+7	MBAT0+T+38
D6	DSACKi*[0] and DS*[L] to LEDI[L] [3, 4]	MBAT0+12	MBAT0+T+53
D7	DSACKi*[0] and DS*[L] to UWDENIN*[L] [3, 4]	MBAT0+7	MBAT0+T+36
D8	DSACKi*[0] and DS*[L] to LA(7:0) [2, 3, 4]	MBAT0+.5T+8	MBAT0+2T+31
D9	DSACKi*[0] and DS*[L] to DSi*[L] [3, 4]	MBAT0+20	MBAT0+T+58
D10	DS*[H] to DS*[L] [2, 4, 5]	T+7	3T+31
Second Longword Write [2, 4]			
D12	DSACKi*[0] and DS*[L] to DS*[H]	MBAT1+7	MBAT1+T+38
D13	DSACKi*[0] and DS*[L] to UWDENIN*[H]	MBAT1+15	MBAT1+T+59
D14	DSACKi*[0] and DS*[L] to LA(7:0)	MBAT1+.5T+8	MBAT1+2T+31
D15	DSACKi*[0] and DS*[L] to LD(7:0)	MBAT1+.5T+10	MBAT1+2T+42
Master D64 Block Transfer with Local DMA (Boundary Crossing) [2]			
E1	DS*[0] to BLT*[H]	2	30
E2	DS*[1] to BLT*[L]	2	20

AC Timings for D64 Operations (Industrial)

	Operation	Min.	Max.
E3	DSi*[0] to LADO first transition	3	20
E4	DSi*[1] to LADO second transition	3	20
Slave D64 Block Transfer Address Broadcast Cycle [2]			
F1	DSi*[1] to LBR*[L]	10	39
F2	DSi*[0] to DTACK*[L]	2T+8	3T+29
F3	DSi*[1] to DTACK*[H]	8	35
F4	DSi*[1] to SCON*/D64[H]	9	35
F5	DSi*[0] and AS*[0] and SLSELi[0] to LADI[H]	1.5T+4	2T+26
Slave D64 Block Transfer (Write)			
First Longword Cycle			
G1	DSi*[0] to DS*[L] [2, 4]	3T+10	4T+40
G2	DSi*[0] to DTACK*[L] [7]	2T+8	3T+24
G3	DSi*[0] to LEDI[H] [2, 4]	T+10	2T+39
G4	DSACKi*[0] and DS*[L] to DS*[H] [2, 4, 8]	SBAT0+7	SBAT0+T+38
G5	DSACKi*[0] and DS*[L] to LEDI[L] [2, 4, 8]	SBAT0+12	SBAT0+T+54
G6	DSACKi*[0] and DS*[L] to UWDENIN*[L] [2, 4, 8]	SBAT0+7	SBAT0+T+33
G7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+8	SBAT0+2T+31
G8	DS*[H] to DS*[L] [2, 4, 5]	T+7	3T+32
Second Longword Cycle [2, 4]			
G9	DSACKi*[0] and DS*[L] to UWDENIN*[H]	SBAT1+19	SBAT1+T+67
G10	DSACKi*[0] and DS*[L] to DS*[H]	SBAT1+10	SBAT1+T+36
G11	DSACKi*[0] and DS*[L] to LA(7:0)	SBAT1+.5T+8	SBAT1+2T+31
G12	DSACKi*[0] and DS*[L] to LD(7:0)	SBAT1+.5T+10	SBAT1+2T+42
Slave D64 Block Transfer (Read)			
First Longword Cycle [4, 8]			
H1	DSACKi*[0] and DS*[L] to LEDO[H]	SBAT0+6	SBAT0+T+37
H2	DSACKi*[0] and DS*[L] to DS*[H] [4, 8]	SBAT0+7	SBAT0+T+41
H3	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+8	SBAT0+T+31
H4	DS*[H] to DS*[L] [2, 4, 5]	T+7	3T+32
Second Longword Cycle			
H5	DSACKi*[0] and DS*[L] to LEDO[L] [4]	SBAT1+18	SBAT1+T+67
H6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	SBAT1+10	SBAT1+T+39
H7	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	SBAT1+23	SBAT1+T+75
H8	DSACKi*[0] & DS*[L] & DSi*[0] to DTACK*[L] [4]	SBAT1+12	SBAT1+T+34

AC Timings for D64 Operations (Industrial)

	Operation	Min.	Max.
H9	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	SBAT1+.5T+8	SBAT1+2T+31
H10	DS1/0*[1] to DENO*[H] [2]	5	22
Slave D64 Block Transfer (Boundary Crossing) [2]			
H11	DS*[0] to LADI[L]	10	28
H12	DS*[1] to LADI[H]	5	14

AC Timings for D64 Operations (Military)

	Operation	Min.	Max.
Master D64 Block Transfer with Local DMA (Initiation Cycle) [2]			
A1	MWB*[0] & PAS*[0] & DS*(0) to BRi*[L]	4T+5	5T+38
A2	MWB*[0] & PAS*[0] & DS*(0) to LADO[H]	T+8	2T+38
A3	MWB*[0] & PAS*[0] & DS*(0) to BLT*[L]	T+8	2T+30
A4	MWB*[0] & PAS*[0] & DS*(0) to DSACK1*[L]	T+10	2T+54
A5	MWB*[0] & PAS*[0] & DS*(0) to DSACK0*[L]	T+10	2T+54
Master D64 Block Transfer Address Broadcast Cycle [2]			
B1	DTACK*[0] to LBR*[L]	20	75
B2	DTACK*[0] to DSi*[H]	7	30
B3	DTACK*[0] to SCON*/D64[H]	15	70
Master D64 Block Transfer with Local DMA (Write)			
First Longword Fetch			
C1	DSACKi*[0] and DS*[L] to DS*[H] [2, 3, 4]	MBAT0+7	MBAT0+T+42
C2	DSACKi*[0] and DS*[L] to LEDO[H] [2, 3, 4]	MBAT0+6	MBAT0+T+36
C3	DSACKi*[0] and DS*[L] to LA(7:0) [2, 3, 4]	MBAT0+.5T+8	MBAT0+2T+35
C4	DS*(H) to DS*[L] [2, 3, 4, 5]	T+7	3T+35
Second Longword Fetch			
C5	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	MBAT1+13	MBAT1+T+52
C6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	MBAT1+10	MBAT1+T+42
C7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	MBAT1+.5T+8	MBAT1+2T+35
C8	DSACKi*[0] and DS*[L] to DSi*[L] [6]	MBAT1+3T+10	MBAT1+4T+36
C9	DSACKi*[0] and DS*[L] to LEDO[L] [4]	MBAT1+15	MBAT1+T+64
C10	DS*(H) to DS*[L] [2, 4, 5]	T+7	3T+35
C11	DTACK*[0] to DSi*[H]	6	25
C12	DTACK*[0] to DENO*[H] [2]	7	30

AC Timings for D64 Operations (Military)

Operation		Min.	Max.
Master Block Transfer with Local DMA (Read)			
First Longword Write			
D1	LBG*[0] to LWDENIN*[L] [2]	2T+10	3T+48
D2	DTACK*[0] to LEDI[H] [7]	2T+5	3T+27
D3	DTACK*[0] to DSi*[H] [2, 7]	2T+8	3T+32
D4	DTACK*[0] to DS*[L] [7]	2T+12	3T+41
D5	DSACKi*[0] and DS*[L] to DS*[H] [2, 3, 4]	MBAT0+7	MBAT0+T+42
D6	DSACKi*[0] and DS*[L] to LEDI[L] [3, 4]	MBAT0+12	MBAT0+T+60
D7	DSACKi*[0] and DS*[L] to UWDENIN*[L] [3, 4]	MBAT0+7	MBAT0+T+41
D8	DSACKi*[0] and DS*[L] to LA(7:0) [2, 3, 4]	MBAT0+.5T+8	MBAT0+2T+35
D9	DSACKi*[0] and DS*[L] to DSi*[L] [3, 4]	MBAT0+20	MBAT0+T+64
D10	DS*[H] to DS*[L] [2, 4, 5]	T+7	3T+35
Second Longword Write [2, 4]			
D12	DSACKi*[0] and DS*[L] to DS*[H]	MBAT1+7	MBAT1+T+42
D13	DSACKi*[0] and DS*[L] to UWDENIN*[H]	MBAT1+15	MBAT1+T+66
D14	DSACKi*[0] and DS*[L] to LA(7:0)	MBAT1+.5T+8	MBAT1+2T+35
D15	DSACKi*[0] and DS*[L] to LD(7:0)	MBAT1+.5T+10	MBAT1+2T+48
Master D64 Block Transfer with Local DMA (Boundary Crossing) [2]			
E1	DS*[0] to BLT*[H]	2	33
E2	DS*[1] to BLT*[L]	2	21
E3	DSi*[0] to LADO first transition	2	21
E4	DSi*[1] to LADO second transition	2	21
Slave D64 Block Transfer Address Broadcast Cycle [2]			
F1	DSi*[1] to LBR*[L]	10	42
F2	DSi*[0] to DTACK*[L]	2T+8	3T+32
F3	DSi*[1] to DTACK*[H]	8	39
F4	DSi*[1] to SCON*/D64[H]	9	39
F5	DSi*[0] and AS*[0] and SLSELi[0] to LADI[H]	1.5T+4	2T+29
Slave D64 Block Transfer (Write)			
First Longword Cycle			
G1	DSi*[0] to DS*[L] [2, 4]	3T+10	4T+44
G2	DSi*[0] to DTACK*[L] [7]	2T+8	3T+26
G3	DSi*[0] to LEDI[H] [2, 4]	T+10	2T+42
G4	DSACKi*[0] and DS*[L] to DS*[H] [2, 4, 8]	SBAT0+7	SBAT0+T+42
G5	DSACKi*[0] and DS*[L] to LEDI[L] [2, 4, 8]	SBAT0+12	SBAT0+T+60

AC Timings for D64 Operations (Military)

	Operation	Min.	Max.
G6	DSACKi*[0] and DS*[L] to UWDENIN*[L] [2, 4, 8]	SBAT0+7	SBAT0+T+37
G7	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+8	SBAT0+2T+35
G8	DS*[H] to DS*[L]	T+7	3T+35
Second Longword Cycle [2, 4]			
G9	DSACKi*[0] and DS*[L] to UWDENIN*[H]	SBAT1+19	SBAT1+T+74
G10	DSACKi*[0] and DS*[L] to DS*[H]	SBAT1+10	SBAT1+T+42
G11	DSACKi*[0] and DS*[L] to LA(7:0)	SBAT1+.5T+8	SBAT1+2T+35
G12	DSACKi*[0] and DS*[L] to LD(7:0)	SBAT1+.5T+10	SBAT1+2T+48
Slave D64 Block Transfer (Read)			
First Longword Cycle			
H1	DSACKi*[0] and DS*[L] to LEDO[H] [4, 8]	SBAT0+6	SBAT0+T+41
H2	DSACKi*[0] and DS*[L] to DS*[H] [4, 8]	SBAT0+7	SBAT0+T+45
H3	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4, 8]	SBAT0+.5T+8	SBAT0+T+35
H4	DS*[H] to DS*[L] [2, 4, 5]	T+7	3T+35
Second Longword Cycle			
H5	DSACKi*[0] and DS*[L] to LEDO[L] [4]	SBAT1+18	SBAT1+T+74
H6	DSACKi*[0] and DS*[L] to DENO*[L] [4]	SBAT1+10	SBAT1+T+42
H7	DSACKi*[0] and DS*[L] to DS*[H] [2, 4]	SBAT1+23	SBAT1+T+85
H8	DSACKi*[0] & DS*[L] & DSi*[0] to DTACK*[L] [4]	SBAT1+12	SBAT1+T+38
H9	DSACKi*[0] and DS*[L] to LA(7:0) [2, 4]	SBAT1+.5T+8	SBAT1+2T+35
H10	DS1/0*[1] to DENO*[H] [2]	5	25
Slave D64 Block Transfer (Boundary Crossing) [2]			
H11	DS*[0] to LADI[L]	10	32
H12	DS*[1] to LADI[H]	5	15

Notes:

1. All minimum times are guaranteed, not tested.

2. These timings are specified for information, but not tested.

3. For second and all subsequent longword fetches, MBAT1 is used in the timing equations.

4. When the Enhanced Turbo Bit is set, all these times are reduced by 0.5T.

5. Min and Max Times are programmable: see Register Descriptions.

6. When the Enhanced Turbo Bit is set, these times become MBAT1+.5T+D min., MBAT1+1.5T +D max.

7. When the Enhanced Turbo Bit is set, all these items are reduced to 0.5T min., 1.0T max, plus appropriate asynchronous delay from the table. Minimum times reflect unloaded device pins. Actual in-system delays will be in accordance with the VMEbus specification.

8. For second and all subsequent longword fetches, SBAT1 is used in the timing equations.

DC Performance Specifications

VMEbus Signals (AS*, DS1*, DS0*, BCLR*, SYSCLK)

Parameter	Description	Test Conditions		Comm.	Industrial	Military	Units
V_{IH}	Minimum high-level input voltage			2.0	2.0	2.0	V
V_{IL}	Maximum low-level input voltage			0.8	0.8	0.8	V
V_{OH}	Minimum high-level output voltage	V_{CC} = Min., I_{OH} = −3 mA		2.4	2.4	2.4	V
V_{OL}	Minimum low-level output voltage	V_{CC} = Min., I_{OL} = 64 mA (com'l), 56 mA (Ind.), 48 mA (Mil.)		0.6	0.6	0.6	V
I_L	Maximum input leakage current	V_{CC} = Max., V_{IN} = 0.6−2.4		±5	±5	±5	µA
V_{IK}	Input clamp voltage	V_{CC} = Min.	I_{IN} = −18 mA	−1.2	−1.2	−1.2	V
			I_{IN} = 18 mA	V_{CC}+1.2	V_{CC}+1.2	V_{CC}+1.2	V
I_{OZ}	Maximum output leakage current	V_{CC} = Max., GND ≤ V_{OUT} ≤ V_{CC}, all outputs disabled		±10	±10	±10	µA
V_{IK}	Input clamp voltage	V_{CC} = Min.	I_{IN} = −18 mA	−1.2	−1.2	−1.2	V
			I_{IN} = 18 mA	V_{CC}+1.2	V_{CC}+1.2	V_{CC}+1.2	V
I_{OZ}	Maximum output leakage current	V_{CC} = Max., V_{OUT} = 0.6/2.4V, all outputs disabled		±5	±5	±10	µA

VMEbus Signals (Low Drive. All VMEbus, Daisy-Chain Signals.)

Parameter	Description	Test Conditions		Comm.	Industrial	Military	Units
V_{IH}	Maximum high-level input voltage			2.0	2.0	2.0	V
V_{IL}	Maximum low-level input voltage			0.8	0.8	0.8	V
V_{OH}	Minimum high-level output voltage	V_{CC} = Min., $I_{OH} = -8$ mA		2.4	2.4	2.4	V
V_{OL}	Minimum low-level output voltage	V_{CC} = Min., $I_{OL} = 8$ mA		0.6	0.6	0.6	V
I_L	Maximum input leakage current	V_{CC} = Max., $V_{IN} = 0.6-2.4$		±5	±5	±5	µA
V_{IK}	Input clamp voltage	V_{CC} = Min.	$I_{IN} = -18$ mA	−1.2	−1.2	−1.2	V
			$I_{IN} = 18$ mA	$V_{CC}+1.2$	$V_{CC}+1.2$	$V_{CC}+1.2$	V
I_{OZ}	Maximum output leakage current	V_{CC} = Max., $V_{OUT} = 0.6/2.4$V, all outputs disabled		±5	±5	±10	µA

VMEbus Signals (Medium Drive. All Non-High, Non-Low Drive Signals, All VAC068A VMEbus Signals.)

Parameter	Description	Test Conditions	Comm.	Industrial	Military	Units
V_{IH}	Maximum high-level input voltage		2.0	2.0	2.0	V
V_{IL}	Maximum low-level input voltage		0.8	0.8	0.8	V

VMEbus Signals (Medium Drive. All Non-High, Non-Low Drive Signals, All VAC068A VMEbus Signals.) (continued)

Parameter	Description	Test Conditions		Comm.	Industrial	Military	Units
V_{OH}	Minimum high-level output voltage	V_{CC} = Min., I_{OH} = -3 mA		2.4	2.4	2.4	V
V_{OL}	Minimum low-level output voltage	V_{CC} = Min., I_{OL} = 48 mA		0.6	0.6	0.6	V
I_L	Maximum input leakage current	V_{CC} = Max., V_{IN} = 0.6$-$2.4		±5	±5	±5	μA
V_{IK}	Input clamp voltage	V_{CC} = Min.	I_{IN} = -18 mA	-1.2	-1.2	-1.2	V
			I_{IN} = 18 mA	V_{CC}+1.2	V_{CC}+1.2	V_{CC}+1.2	V
I_{OZ}	Maximum output leakage current	V_{CC} = Max., V_{OUT} = 0.6/2.4V, all outputs disabled		±5	±5	±10	μA

Non-VMEbus Signals

Parameter	Description	Test Conditions	Comm.	Industrial	Military	Units
V_{IH}	Maximum High-Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{CC} = Min., I_{OH} = -8 mA	2.4	2.4	2.4	V
V_{OL}	Minimum Low-Level Output Voltage	V_{CC} = Min., I_{OL} = 8 mA	0.6	0.6	0.6	V

Non-VMEbus Signals (Continued)

Parameter	Description	Test Conditions		Comm.	Industrial	Military	Units
I_L	Maximum Input Leakage Current	V_{CC} = Max., V_{IN} = 0.00/V_{CC}		±5	±5	±5	μA
V_{IK}	Input Clamp Voltage	V_{CC} = Min.	$I_{IN} = -18$ mA	−1.2	−1.2	−1.2	V
			$I_{IN} = 18$ mA	V_{CC}+1.2	V_{CC}+1.2	V_{CC}+1.2	V
I_{OZ}	Maximum Output Leakage Current	V_{CC} = Max. GND $\leq V_{OUT} \leq V_{CC}$ All Outputs Disabled		±5		±10	μA

Capacitance

C_{IN}	Input Capacitance	$T_A = 25°C$, f = 64 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Figure 1. Master Address Broadcast Cycle
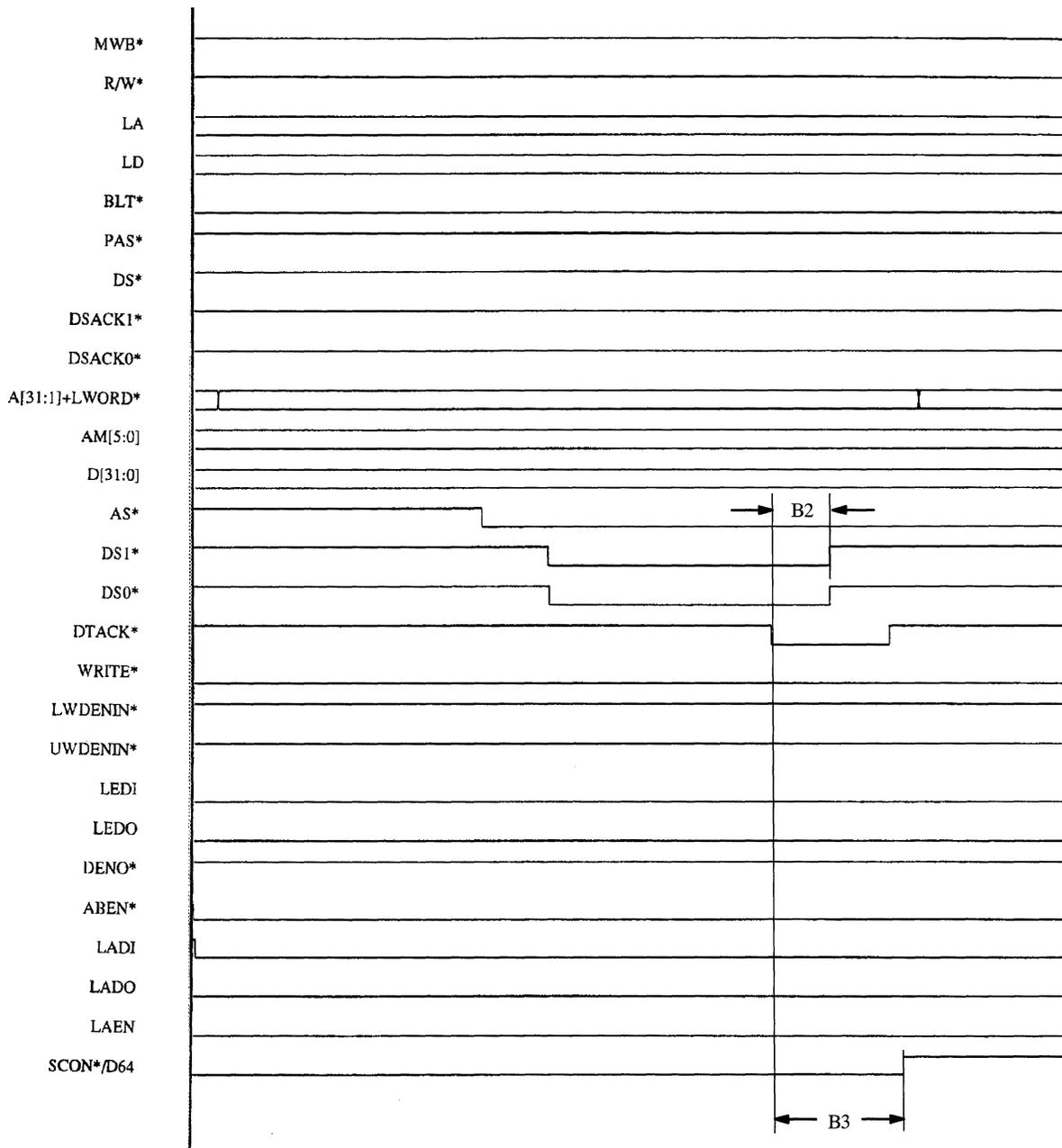
VIC64/7C964-1

Figure 2. Master D64 Write Operation: Detail
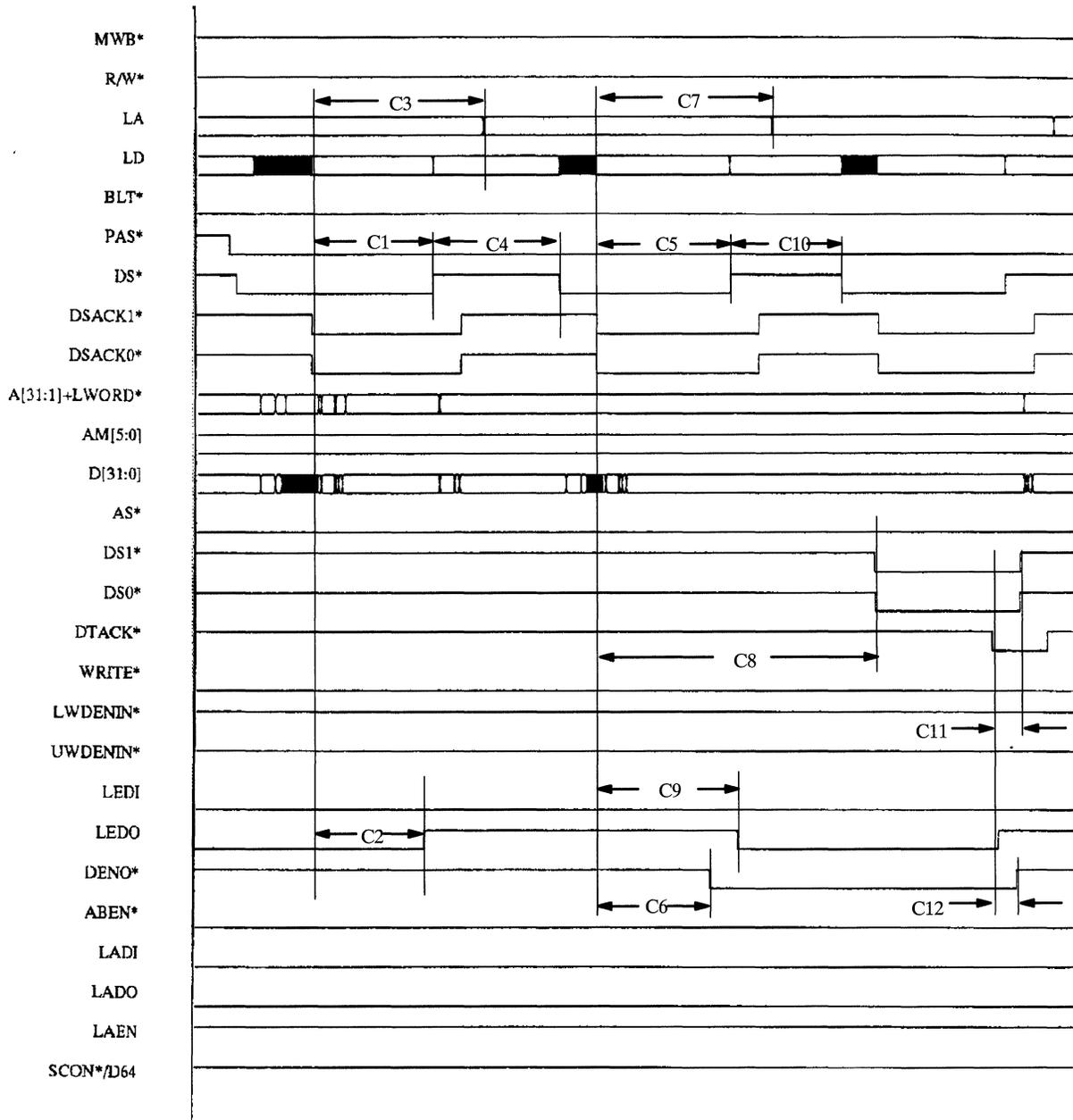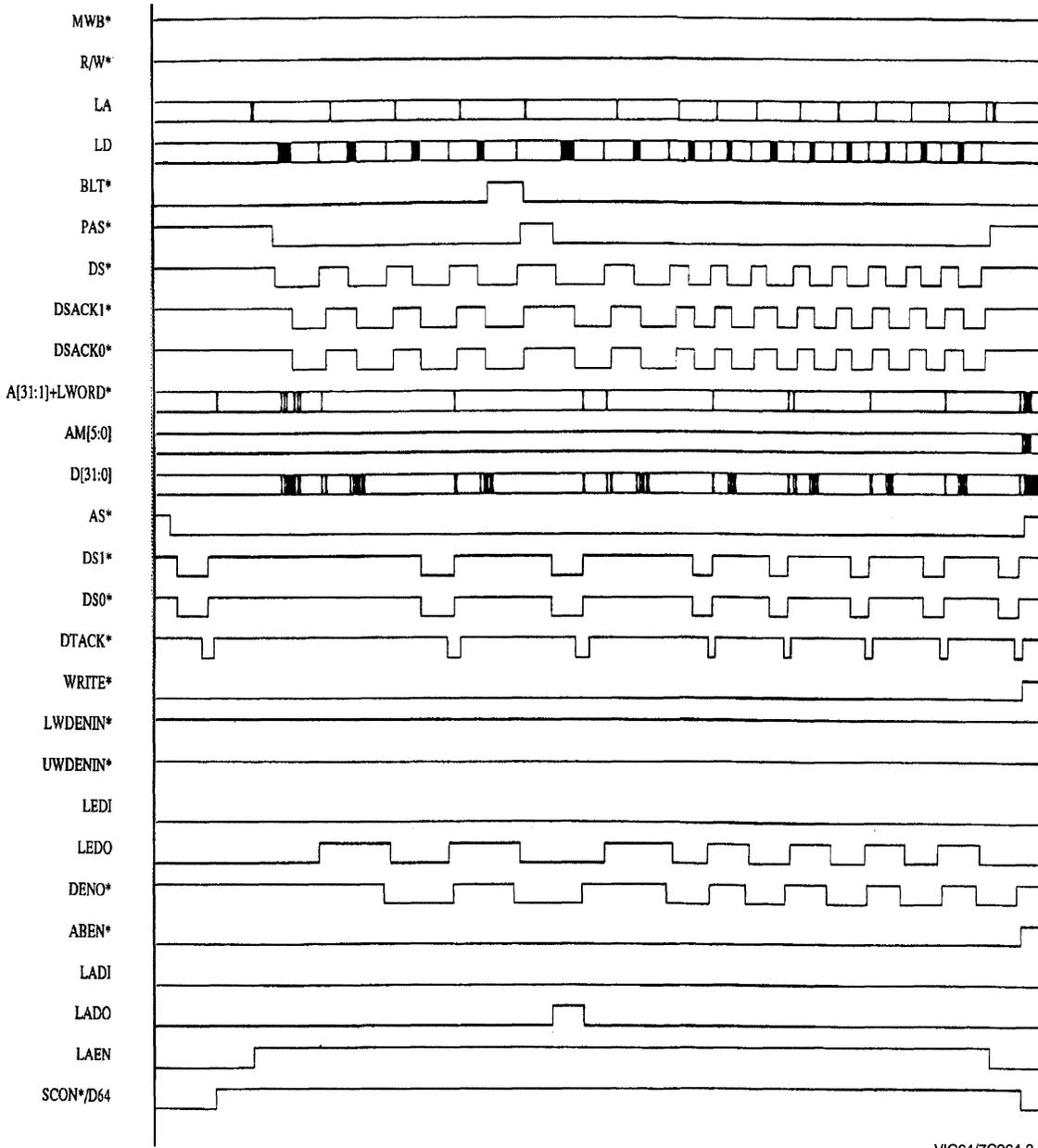
VIC64/7C964-2

Figure 3. Master D64 Write Operation: Block Transfer

Figure 4. Master D64 Read Operation: Detail
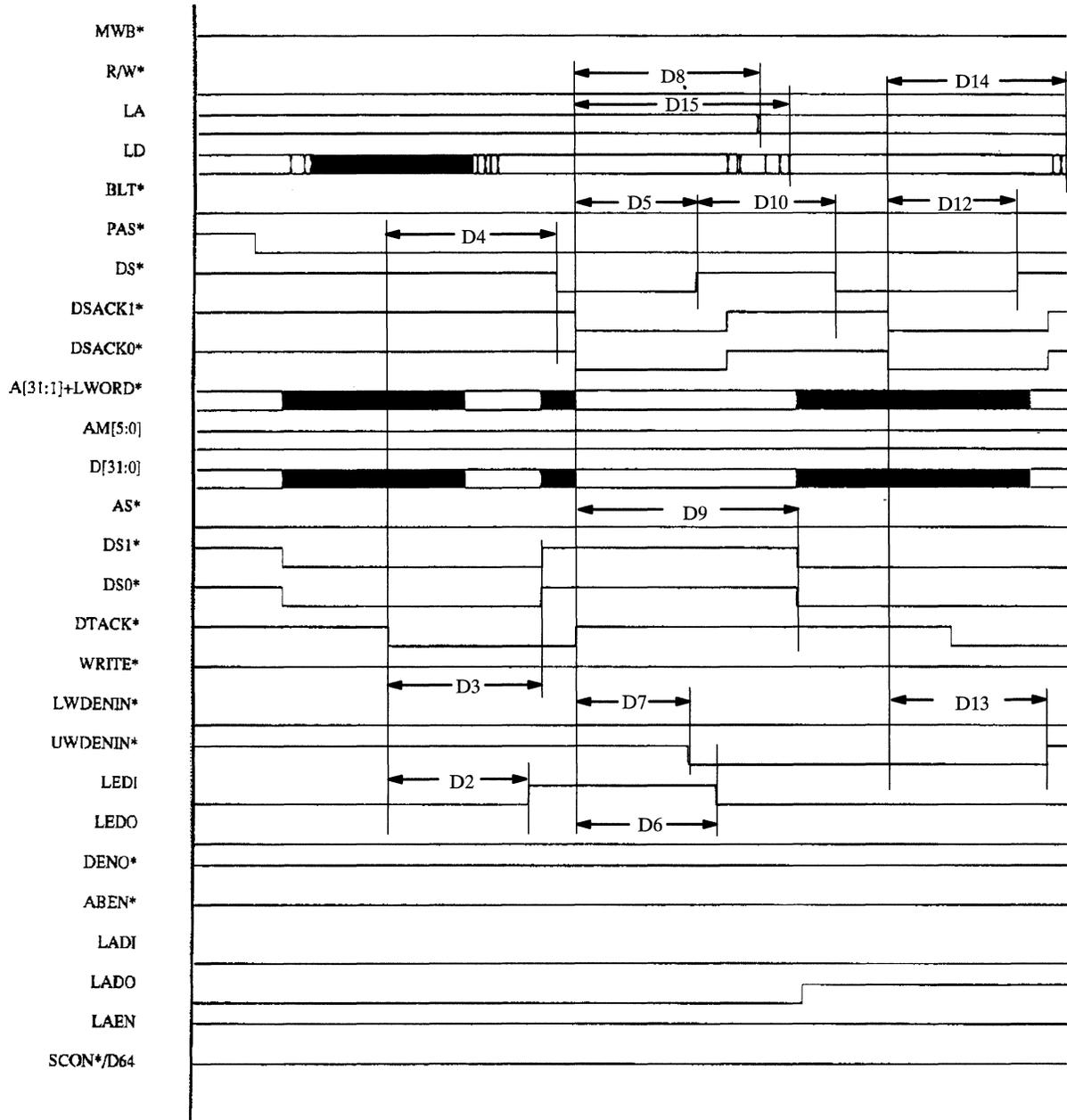
VIC64/7C964-4

Figure 5. Master D64 Read Operation: Block Transfer
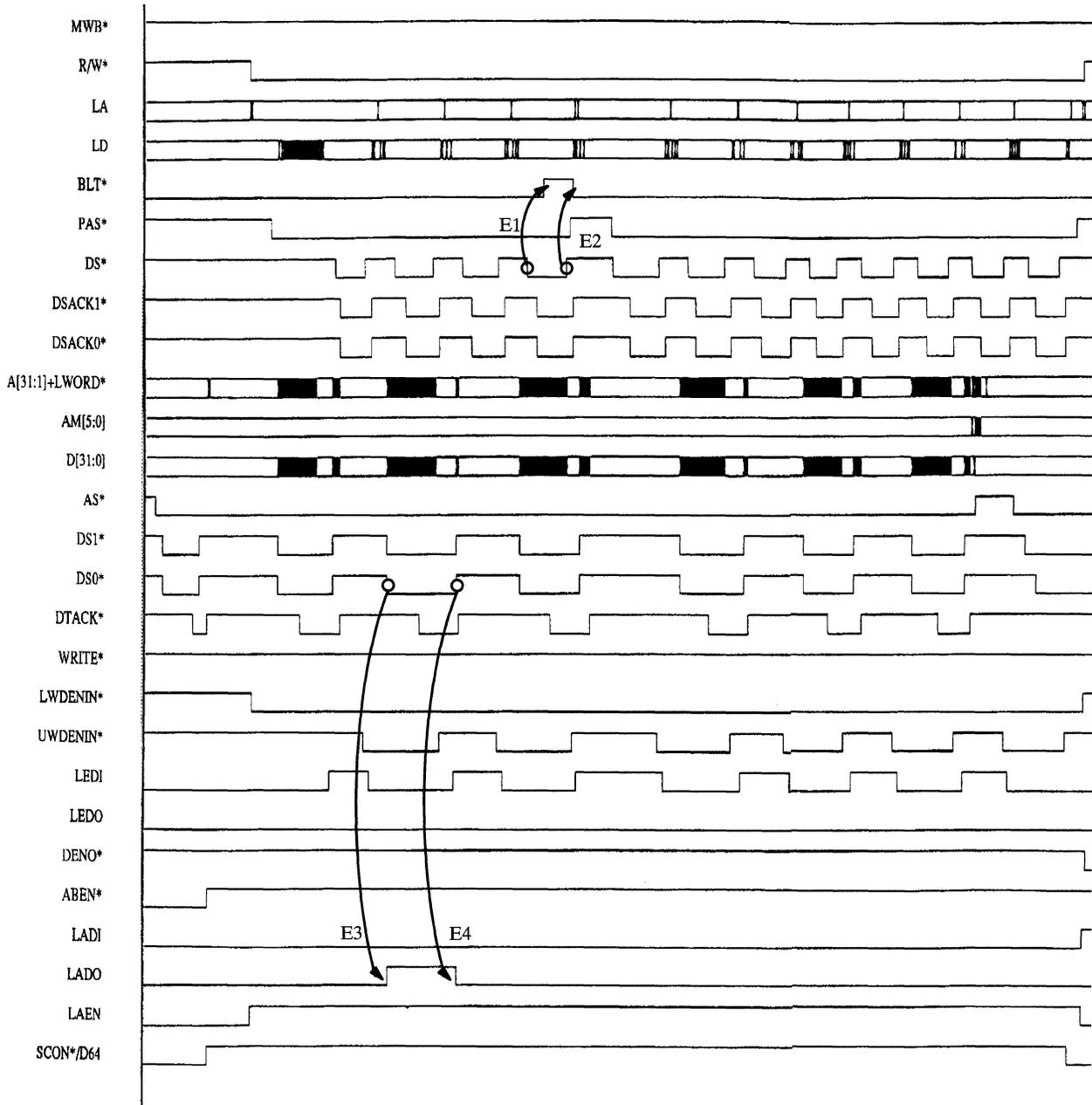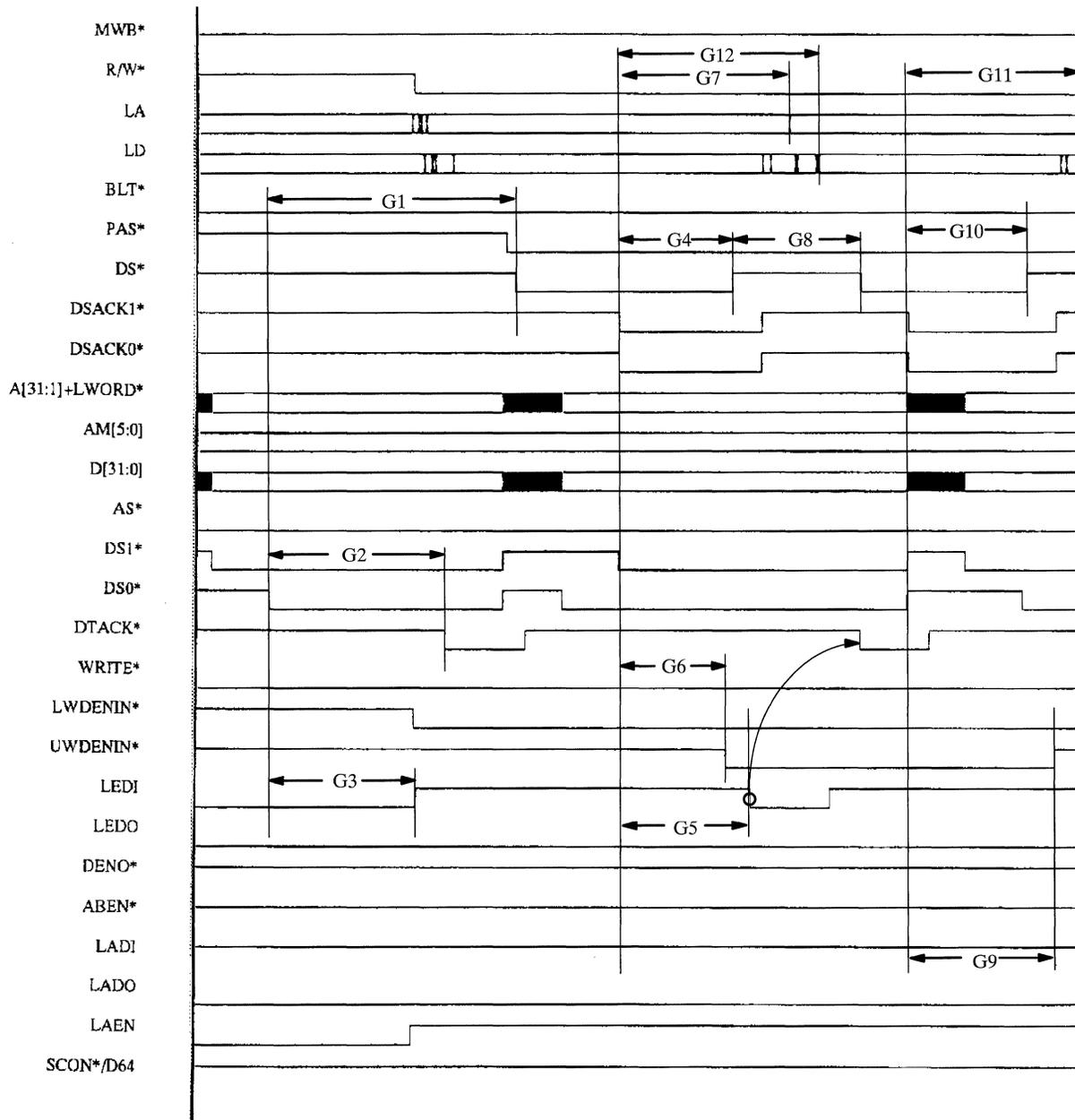
VIC64/7C964-5

Figure 6. Slave D64 Write Operation: Detail
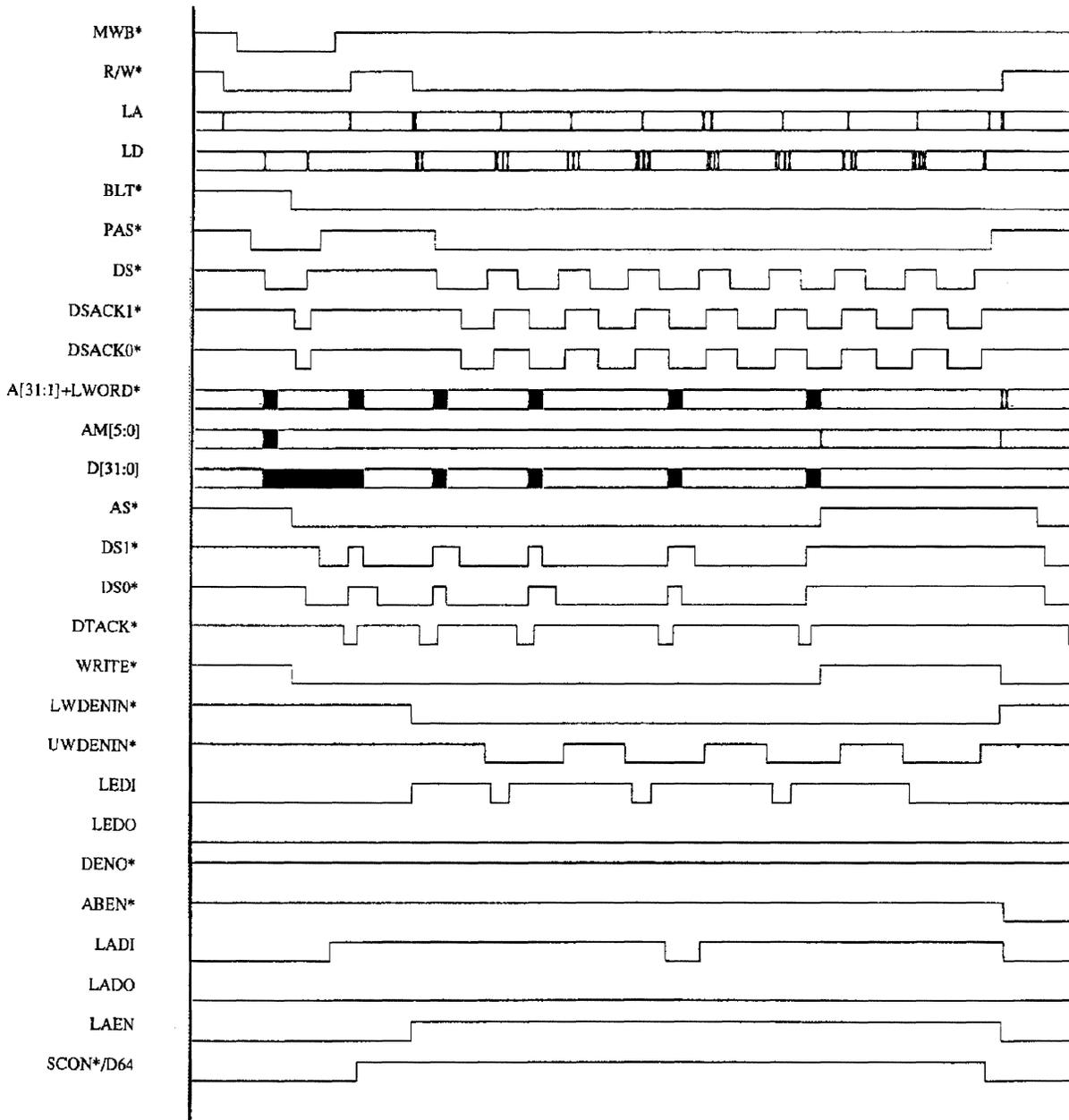
VIC64/7C964-6

VIC64/7C964-7

Figure 7. Slave D64 Write Operation: Block Transfer

CYPRESS
SEMICONDUCTOR
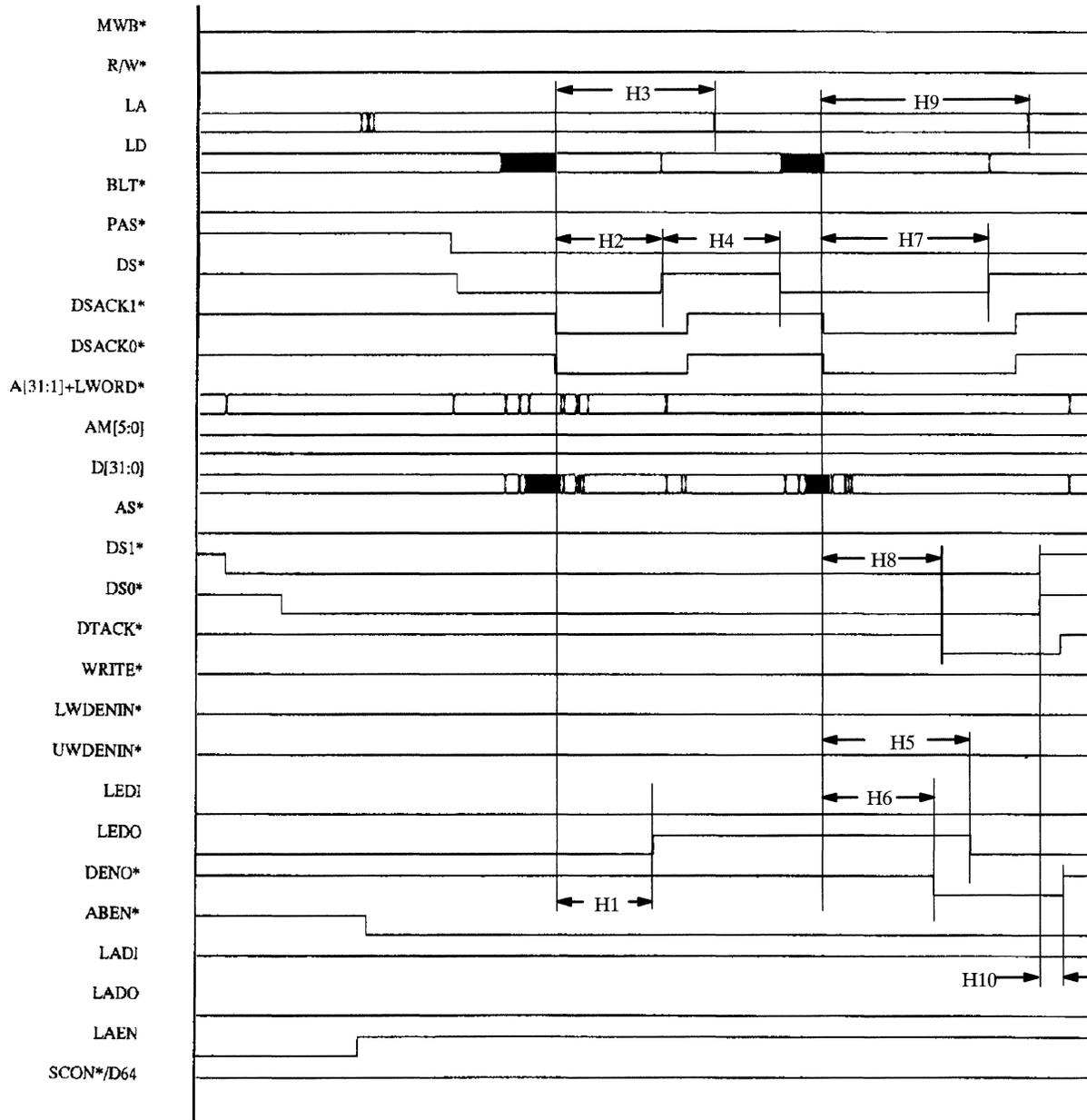
Figure 8. Slave D64 Read Operation: Detail

VIC64/7C964-8

27
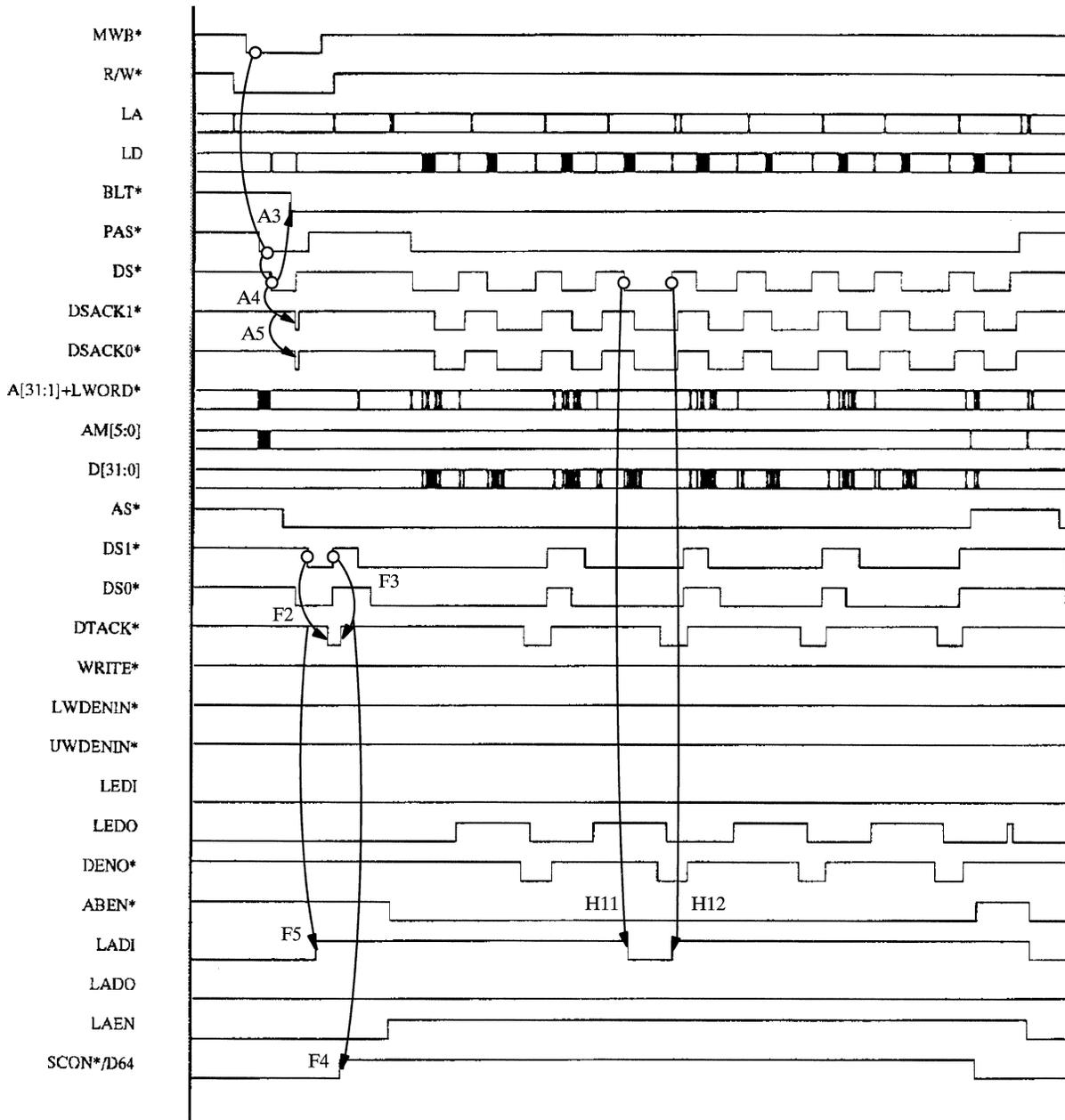
VIC64/7C964-9

Figure 9. Slave D64 Read Operation: Block Transfer

Pin Configurations

Bottom View
PGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	VSS	IPL2*	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1*	ASIZ0*	SLSEL1*	WORD	FIACK*	A02	A04	VDD	VSS	IRQ4*	1
2	LD6	BLT*	IPL1*	VDD	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
3	LD2	LD5	DEDLK*	IPL0*	LAEN	LIRQ3*	LIRQ7*	VSS	SLSEL0*	VSS	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
4	LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VDD	IACKOUT*	4
5	LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
6	LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
7	LA2	LA4	VSS										VSS	AS*	AM1	7
8	LA1	LA0	VCC7										VSS	AM2	AM3	8
9	CS*	DSACK1*	$\overline{\text{DS}}$										VDD	LWORD*	AM4	9
10	PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
11	DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
12	HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
13	FC2	SIZ0	SCON*/D64	CLK64M	LADI	VSS	VDD	VSS8	VCC5	D00	BG1OUT*	BG2IN*	BG0IN*	$\overline{\text{BR3}}$	VSS	13
14	SIZ1	IRESET*	LADO	LEDI*	DDIR*	LWDENIN*	DENO*	D06	D03	D01	VSS7	BG0OUT*	BG3IN*	BG1IN*	BCLR*	14
15	LBG*	ABEN*	VDD	LEDO	UWDENIN*	SWDEN*	ISOBE*	D07	D05	D04	D02	BG3OUT*	BG2OUT*	SYSCLK	VSS	15

VIC64/7C964-10

CYPRESS SEMICONDUCTOR

**Top View
PQFP/CQFP**

Pin diagram — VIC64

Top (pins 1–40, left to right):

Pin	Signal	Pin	Signal
1	VSS	21	SLSEL0*
2	VSS	22	WORD*
3	IPL0*	23	FCIACK*
4	IPL1*	24	MWB*
5	IPL2*	25	A1
6	VDD	26	A2
7	LAEN	27	VSS
8	LIAKO*	28	A3
9	LIRQ0*	29	A4
10	LIRQ1*	30	VDD
11	LIRQ2*	31	A5
12	LIRQ3*	32	A6
13	LIRQ4*	33	A7
14	LIRQ5*	34	VSS
15	LIRQ6*	35	IRQ1*
16	LIRQ7*	36	IRQ2*
17	ASIZ0*	37	IRQ3*
18	ASIZ1*	38	IRQ4*
19	ICFSEL*	39	VSS
20	SLSEL1*	40	VSS

Left (pins 41–80):

Pin	Signal
41	VDD
42	VDD
43	IRQ5*
44	IRQ6*
45	IRQ7*
46	VDD
47	SYSFAIL*
48	ACFAIL*
49	SYSRESET*
50	IACKOUT*
51	IACKIN*
52	IACK*
53	DTACK*
54	AS*
55	VSS
56	AM0
57	AM1
58	AM2
59	AM3
60	VSS
61	VDD
62	AM4
63	AM5
64	LWORD*
65	WRITE*
66	BERR*
67	DS0*
68	DS1*
69	BR0*
70	VSS
71	BR1*
72	BR2*
73	BR3*
74	BCLR*
75	BBSY*
76	BGIN0*
77	BGIN1*
78	VSS
79	VDD
80	VDD

Bottom (pins 81–120):

Pin	Signal	Pin	Signal
81	VSS	101	VDD
82	VSS	102	ISOBE*
83	BGIN2*	103	DENO*
84	BGIN3*	104	SWDEN*
85	SYSCLK	105	LWDENIN*
86	BGOUT0*	106	VSS
87	BGOUT1*	107	UWDENIN*
88	BGOUT2*	108	DDIR*
89	VSS	109	LEDO
90	BGOUT3*	110	VDD
91	D00	111	LADI
92	D01	112	LEDI
93	D02	113	LADO
94	D03	114	ABEN*
95	VDD	115	CLK64M
96	D04	116	SCON*/D64
97	D05	117	IRESET*
98	D06	118	LBG*
99	D07	119	VSS
100	VSS	120	VSS

Right (pins 121–160):

Pin	Signal
121	VDD
122	VDD
123	LBR*
124	SIZ0
125	SIZ1
126	RMC*
127	FC1
128	FC2
129	R/W*
130	HALT*
131	RESET*
132	LBERR*
133	DSACK0*
134	DSACK1*
135	DS*
136	PAS*
137	CS*
138	LA0
139	LA1
140	VDD
141	VSS
142	LA2
143	LA3
144	LA4
145	LA5
146	LA6
147	LA7
148	LD0
149	LD1
150	LD2
151	LD3
152	LD4
153	LD5
154	LD6
155	LD7
156	DEDLK*
157	BLT*
158	VSS
159	VDD
160	VDD

Top View
TQFP

Top pins (left to right), pins 144–109:
VSS, BLT*, DEDLK*, LD7, LD6, LD5, LD4, LD3, LD2, LD1, LD0, LA7, LA6, LA5, LA4, LA3, LA2, VSS, VDD, LA1, LA0, CS*, PAS*, DS*, DSACK1*, DSACK0*, LBERR*, RESET*, HALT*, R/W*, FC2, FC1, RMC*, SIZ1, SIZ0, LBR*

Left pins (top to bottom), pins 1–36:

Pin	Signal
1	IPL0*
2	IPL1*
3	IPL2*
4	VDD
5	LAEN
6	LIAKO*
7	LIRQ1*
8	LIRQ2*
9	LIRQ3*
10	LIRQ4*
11	LIRQ5*
12	LIRQ6*
13	LIRQ7*
14	ASIZ1*
15	ASIZ0*
16	ICFSEL*
17	SLSEL1*
18	VSS
19	SLSELO*
20	WORD*
21	FCIACK*
22	MWB*
23	A1
24	VSS
25	A2
26	A3
27	A4
28	VDD
29	A5
30	A6
31	A7
32	VSS
33	IRQ1*
34	IRQ2*
35	IRQ3*
36	IRQ4*

Right pins (top to bottom), pins 108–73:

Pin	Signal
108	LBG*
107	IRESET*
106	SCON*/D64
105	CLK64M
104	ABEN*
103	LADO
102	LADI
101	LEDI
100	VDD
99	LEDO
98	DDIR*
97	UWDENIN*
96	VSS
95	LWDENIN*
94	DENO*
93	SWDEN*
92	ISOBE*
91	VDD
90	VSS
89	D07
88	D06
87	D05
86	D04
85	VDD
84	D03
83	D02
82	D01
81	D00
80	BGOUT3*
79	VSS
78	BGOUT2*
77	BGOUT1*
76	BGOUT0*
75	SYSCLK
74	BGIN3*
73	BGIN2*

Bottom pins (left to right), pins 37–72:
IRQ5*, IRQ6*, IRQ7*, VDD, SYSFAIL*, ACFAIL*, SYSRESET*, IACKOUT*, IACKIN*, IACK*, DTACK*, AS*, VSS, AM0, AM1, AM2, AM3, VSS, VDD, AM4, AM5, LWORD*, WRITE*, BERR*, DS0*, DS1*, BR0*, VSS, BR1*, BR2*, BR3*, BCLR*, BBSY*, BGIN0*, BGIN1*, VSS

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Package Diagrams

144-Pin Thin Quad Flat Pack A144

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

145-Plastic Pin Grid Array (Cavity Up) B144

TOP VIEW

PIN 1 INDICATOR
.040 X 45°

1.521
1.537

1.521
1.537

SEATING
PLANE

.062
.078

.120
.150

.120
.140

.050 DIA.
4 X

.185
.209

DIA. .016
.020
145 X

BOTTOM VIEW

1.400 BSC.

.100
BSC.

EXTRA
PIN

1.400
BSC.

.100
BSC.

DIMENSIONS IN INCHES
MIN.
MAX.

145-Ceramic Pin Grid Array (Cavity Up) G145

DIMENSIONS IN INCHES
MIN.
MAX.

1.565
1.590
SQ.

1.383
1.415
SQ.

PIN 1
INDEX
MARK

EXTRA
PIN

.100
TYP.

.100
TYP.

145 X .070 MAX. DIA.

.105
.145

.165
.195

145 X
.016
.020 DIA.

4 X
.050 DIA.

.040
.060

.125
.135

SEATING
PLANE

33

160-Lead Plastic Quad Flatpack N160

PIN #1

.300 [.012]
TYP.

.650 [.0256]
TYP.

DIMENSION IN mm [INCHES as reference only]

28.00±.10 SQ
[1.102±.004]

31.20±.25 SQ
[1.228±.010]

.127±.02
[.005±.001]

SEATING PLANE

MIN. 3.59
MAX. 3.99
[.141]
[.157]

MIN. .050
MAX. .500
[.002]
[.020]

.800±.15
[.031±.006]

160-Lead Ceramic Quad Flatpack U162

PIN 1

0.650 (.0256)
TYP.

0.300 (.012)
TYP.

DIMENSION IN MM (INCH)
MIN.
MAX.

28.00 ±0.10
(1.102 ±.004)
SQ.

31.20 ±0.25
(1.228 ±.010)
SQ.

SEATING PLANE
2.03 (.080)
2.79 (.110)

0.15 ±0.02
(.006 ±.001)

0.050 (.002)
0.500 (.020)

0.51 ±0.20
(.020 ±.008)

CY7C964 Design Notes

Introduction

The CY7C964 is a flexible collection of byte (8-bit) wide transceivers, latches, counters, multiplexers, and comparators that provide bus interface designs with a low-cost alternative to PLDs, ASICs, or discrete logic devices. It is based on a standard cell design that incorporates patented line drivers for reduced ground bounce and high noise immunity. The CY7C964 is a companion part to Cypress's VIC068A and VIC64 VMEbus interface controller devices. It is completely compatible with all operating modes of either device, such as dual-address path, block transfer boundary crossing conditions, block transfer initialization cycle, local DMA control, and D64 VMEbus block transfers, (the latter when used in conjunction with the VIC64). Signal-naming conventions correspond directly to the VIC068A/VIC64 buffer control signals, and the CY7C964 can be directly connected to these corresponding signals.

The CY7C964 can also be used as a generic-interface building block. Some examples include low-cost slave VMEbus controllers, VSB interfaces, or other interface applications. CY7C964s are cascadable allowing easy interfacing to buses of any width. By combining multiple logic functions into one discrete part, the CY7C964 saves board space and reduces power consumption, which is becoming increasingly important to designers. The CY7C964 has two operating modes, Byte Width and Word Width. The Byte Width configuration of the device has 8 local address, 8 local data signals, 8 VMEbus address and 8 VMEbus data signals. The Word Width mode changes the local and VMEbus data signals into 16-bit extended address or data paths.

Features

- Directly connects to VIC068A or VIC64 for seamless VME bus interface
- Has internal counters for block transfer and local DMA address control
- Has internal multiplexers for D64 64-bit VMEbus block transfers
- Has internal comparators for address decoding
- Supports VIC068A/VIC64 dual-address-path option
- Has cascadable operation
- Directly drives VMEbus address and data bus signals
- Directly drives local address and data bus signals
- Reduces components for a compact board design
- Has low power requirements
- Is available in a 64-pin QFP or 68-pin PGA
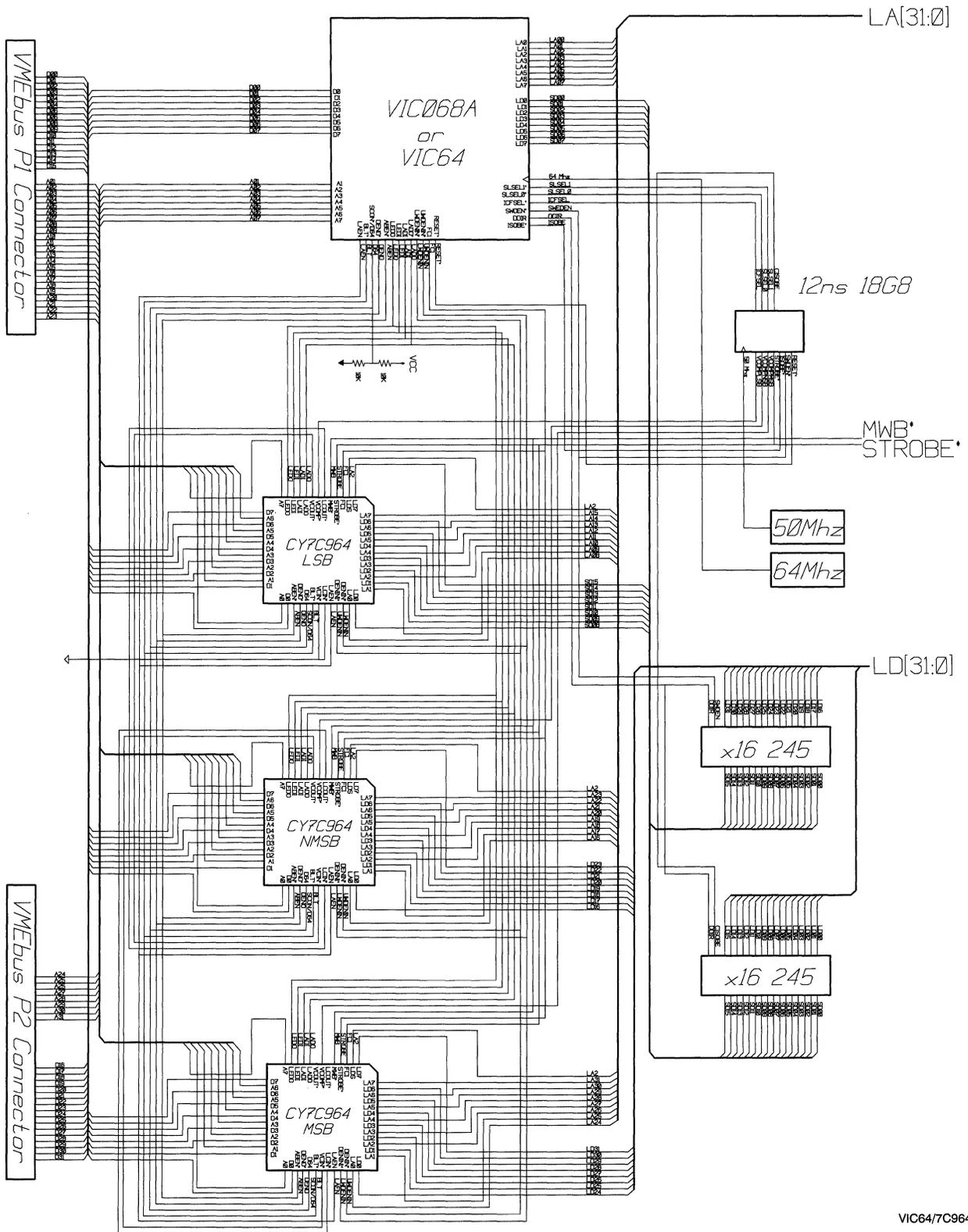
Figure 10. Full Function D64 VMEbus Interface

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Interfacing to the VIC64 and VIC068A

Previously, interfacing the VIC068A to the VMEbus required a significant amount of LSI and MSI devices. With the advent of 64-bit VMEbus block transfers and the VIC64, the external discrete device count for a full functional interface has expanded. The CY7C964 has been developed to combat this problem by incorporating the functions of much of this external logic into a single package. Using the CY7C964 shortens system design, debug, and manufacturing cycle times. Design engineers are relieved from the burden of performing critical or worst-case timing analysis on the VMEbus and VIC buffer control signals. Local control signals other than those directly interfaceable to the VIC64 or VIC068A have been kept to a minimum.

Figure 10 shows a full function D64 VMEbus interface implemented using the CY7C964, VIC64, and all VMEbus interface local support logic. This interface features:

- Block transfer support for D16, D32, and D64 VMEbus transfers
- Dual-path address operation (allowing single-cycle transfers during master block transfer interleave periods)
- Slave block transfers during master block transfer interleave periods
- Fully programmable slave VMEbus address decoding
- Write posting
- The VIC mail box interrupt message support

The interface can be broken into six functional sections for the purpose of discussion. These sections are:

- VMEbus signal group
- VIC buffer control signal group
- CY7C964 local signal group
- CY7C964 address comparator and local signal group
- Local data swap buffer logic
- VIC local control signal group

The focus of this section is the CY7C964. Each of the interface functional blocks are examined from this perspective. The CY7C964s will be referred to as the LSB, NMSB, and MSB device depending on the segment of the VMEbus that they control. The LSB controls VMEbus address and data signals [15:8], NMSB [23:16], and MSB [31:24]. This interface uses the CY7C964s in the Byte Width mode as address and data controllers. All of the information contained within this section is pertinent to this mode of operation. Refer to the Operation section of this document for information on the Word Width (16-bit address control) mode of the device. For additional information on the signals described within this section, consult the VMEbus Specification (IEEE 1014) and/or Cypress Semiconductor's *VIC068A/VAC068A User's Guide*.

Table 4. VMEbus Signals

Signal	Description	Interface Comments
D[7:0]	VMEbus compatible data signals	Directly connect to VMEbus P1 and P2 connectors
A[7:0]	VMEbus compatible address signals	Directly connect to VMEbus P1 and P2 connectors

VMEbus Signal Group

This group includes the VMEbus address and data signals. Each CY7C964 provides support for 8 bits of VMEbus address and data. Three CY7C964s are necessary for 32-bit interface applications when used

with the VIC068A or VIC64. The A[7:0] and D[7:0] transceivers on the CY7C964 furnish a high drive strength, allowing direct connection to the respective address and data signals on the VMEbus backplane. With the VIC068A or VIC64 generating the control information, the CY7C964s meet VMEbus worst-case timing and drive-strength requirements for all forms of data transfers.

VIC Buffer Control Signal Group

This group includes all of the VIC buffer control signals. A major design time savings is realized using the CY7C964s as all of these signals directly connect to the VIC or are hard-wired to a steady state value. The buffer control interface is simple and straight forward with the minor exception that the connection of UWDENIN* and LWDENIN* control signals from the VIC are swapped to the DENIN* and DENIN1* on the LSB CY7C964. See Table 5 for further information on the connection of these signals.

Table 5. Buffer Control Signals

Signal	Description	Interface Comments
LADO	Latch address out	Directly connect to VIC LADO on all CY7C964s.
LADI	Latch address in	Directly connect to VIC LADI on all CY7C964s.
LEDO	Latch enable data out	Directly connect to VIC LEDO on all CY7C964s.
LEDI	Latch enable data in	Directly connect to VIC LEDI on all CY7C964s.
ABEN*	VMEbus address bus enable	Directly connect to VIC ABEN* on all CY7C964s.
DENO*	Data enable output	Directly connect to VIC DENO* on all CY7C964s.
D64	D64 block transfer mode enable	Directly connect to VIC64 SCON/D64 pin on all CY7C964s. Tie this input LOW on all CY7C964s when using VIC068A.
BLT*	Block transfer enable	Directly connect to VIC BLT* on all CY7C964s.
LAEN	Local address enable	Directly connect to VIC LAEN on all CY7C964s.
DENIN*	Primary data enable in signal	Directly connect to VIC UWDENIN* on NMSB and MSB CY7C964s, directly connect to VIC LWDENIN* on LSB CY7C964.
DENIN1*	Companion data enable in signal	Directly connect to VIC LWDENIN* on NMSB and MSB CY7C964s, directly connect to VIC UWDENIN* on LSB CY7C964.

CY7C964 Local Signal Group

The CY7C964 local signal group consists of the VMEbus and local block-transfer counter count-enable daisy-chains. These signals enable the local and VMEbus higher-order address counters; two local address counters (a master block transfer and a slave block transfer) and a single VMEbus address counter. The local address counters share the LCIN*/LCOUT* count-enable daisy-chain. These signals are multiplexed within the CY7C964 and enable counting for the proper counter depending on the current state of the interface. The VCIN*/VCOUT* daisy-chain is dedicated to the VMEbus address counter on the device. When the VCIN* or LCIN* inputs are held Low, counting is enabled for the appropriate counters within the device. The VCIN* and LCIN* signals do not advance the counters, they just enable counting. The counters increment when these signals are active and the proper increment count control logic sequence

occurs. The VIC advances the address counters at the proper time during VMEbus and local DMA block transfer operations. For further information on the counter advance control sequence, refer to the CY7C964 Operation section of this document.

Table 6. CY7C964 Local Signals

Signal	Description	Interface Comments
LCIN*	Local address counter count enable	On LSB CY7C964 tie this input LOW. On the NMSB device directly connect to the LCOUT* of the LSB device. For the MSB CY7C964 connect to the LCOUT* of the NMSB device.
LCOUT*	Local address counter carry out	On LSB CY7C964 connect this output to the LCIN* input. On the NMSB CY7C964 connect this output to the MSB LCIN* input. For the MSB device do not connect this output.
VCIN*	VMEbus address counter count enable	On LSB CY7C964 tie this input LOW. On the NMSB device directly connect to the VCOUT* of the LSB device. For the MSB CY7C964 connect to the VCOUT* of the NMSB device.
VCOUT*	VMEbus address counter carry out	On LSB CY7C964 connect this output to the VCIN* input. On the NMSB CY7C964 connect this output to the MSB VCIN* input. For the MSB device do not connect this output.

CY7C964 Address Comparison and Local Signal Group

The implementation of this group of CY7C964 signals is application specific. The MWB* signal and FC1 signal have been included in this section because they are locally generated signals required by the VIC. These two signals differ slightly on the VIC; MWB* is an input only, while FC1 is a bidirectional signal that can be driven by the VIC. On the CY7C964 the MWB* and FC1 signals are inputs. These signals should be directly connected to the respective local signals on VIC.

Table 7. CY7C964 Address Comparison and Local Signals

Signal	Description	Interface Comments
FC1	Function code 1 signal	Directly connect on all CY7C964s to the same local signal that drives the FC1 signal on the VIC.
MWB*	Module wants VMEbus	Directly connect on all CY7C964s to the same local signal that drives the MWB* signal on the VIC.
LDS	Load register select signal	Should be directly connected to LA2 for systems with 32-bit local bus. Refer to text below for further information.
STROBE*	Latch register control signal	Chip select−like signal for CY7C964 internal comparator mask and comparison registers. See text below for further information.
VCOMP*	VMEbus address comparator output	Needs a small amount of external glue logic to validate and combine signals in a parallel high-performance fashion.
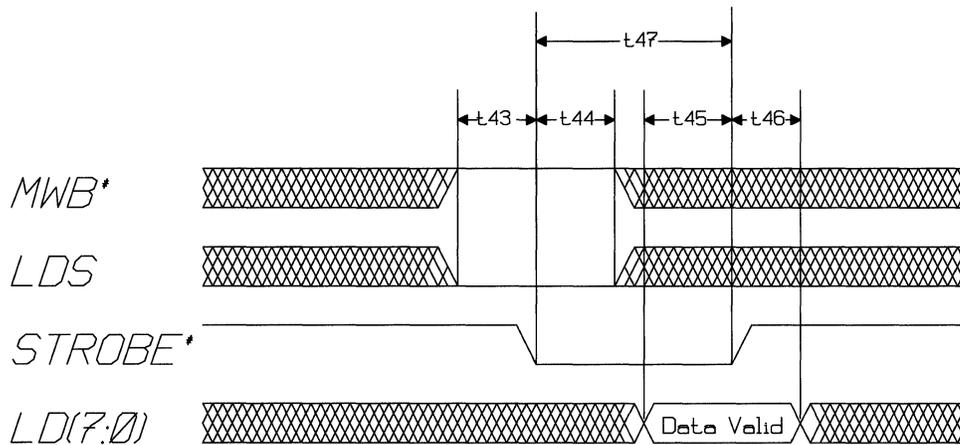
Load CY7C964 Mask Register
Byte Width Mode

VIC64/7C964-14

Figure 11. Mask Register Load Timing in Byte Width Mode

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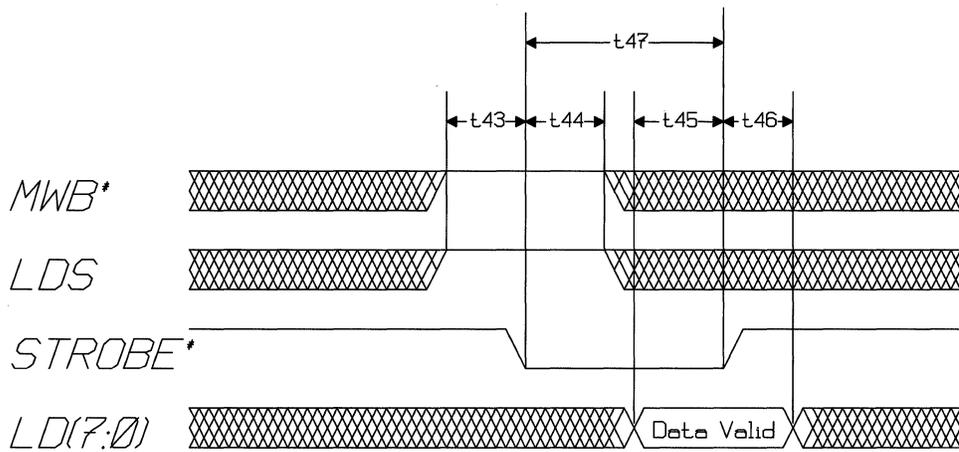
Load CY7C964 Compare Register
Byte Width Mode

VIC64/7C964-15

Figure 12. Compare Register Load Timing in Byte Width Mode

The CY7C964s contain a high-performance programmable VMEbus address equality comparator. The comparator is controlled by two internal, write-only registers, a mask, and a compare register. The mask register enables and disables bits of the comparator, and the compare register stores the data pattern that inputs are compared against. VCOMP* is the active-Low comparator match output signal. VCOMP* is driven Low by the CY7C964 when the bit pattern on pins A[7:0] match enabled bits of the compare register. Setting mask register bits to 0 enables the corresponding bits of the compare register. Loading bits of the mask register with 1's places bits of the compare register in don't care or match anything state. Loading the mask register with all 0's forces the compare register to match all bits of the pattern on A[7:0]. Setting the mask register to all 1's effectively disables the on-board comparator. VCOMP* will always be Low.

These registers are loaded by supplying the proper data on LD[7:0] and the register address on MWB* and LDS signals. The STROBE* input is used to qualify the address and latch the data into the proper internal register. *Figure 11* and *Figure 12* show the waveforms needed to load the compare and mask registers.

This load cycle operates as follows:

1. The state of LDS and MWB* are latched on the falling edge of STROBE*.

2. The data is loaded into the selected register on the rising edge of the STROBE* signal.

3. MWB* must be held inactive (High): the state of LDS selects the register to load.

4. If LDS is High at the falling edge of STROBE*, the compare register will be loaded; if LDS is Low the data is written to the mask register.

This load cycle can be generated by decoding a separate address region or chip select signal for the CY7C964 comparator registers. In applications with a 32-bit local data bus, it is desirable to load all three CY7C964s in parallel by having the host processor perform a 32-bit write cycle to the address region that will activate STROBE*. The select signal for the address region is connected to the STROBE* input on all three CY7C964s. The 8 bits of data on the lowest-order section of the data bus does not matter to the VIC, as long as the VIC CS signal remains inactive during this write cycle. Boards that use this style of interface should connect LDS to LA2, thereby decoding the mask register at the *base address* of the address region and the compare register at the *base address +4*. LDS also controls the operation of the D64 block transfer data multiplexer/demultiplexer. If it is not connected to LA2, this logic will not operate properly.

```
C18G8;
{ VMEbus address decode CY7C964 support logic PLD Cypress Semiconductor 12ns
18G8 PLD }
CONFIGURE;
{ 32 MHz Clock }
CLK_32(node=1),
{ LSB CY7C964 VCOMP* output signal }
LSB_VCOMP*(node=2),
{ NMSB CY7C964 VCOMP* output signal }
NMSB_VCOMP*(node=3),
{ MSB CY7C964 VCOMP* output signal }
MSB_VCOMP*(node=4),
{ CY7C964 STROBE* register load signal }
STROBE*(node=5),
{ System resent signal }
SYSTEM_RESET(node=6),

{ Node Declaration }
{ Signal used to ENABLE to the SLESEL0, SLSEL1, and ICFSEL to the VIC }
ENABLE(node=12, noreg, iop),
{ Delay ICFSEL signal used  to filter ICFSEL output to VIC }
DICFSEL(node=13),
{ Delay SLSEL1 signals used to filter SLSEL1 output to VIC }
DSLSEL1(node=14),
{ Delay SLSEL0 signals used to filter SLSEL0 output to VIC }
DSLSEL0(node=15),
{ Filtered SLSEL1 output to VIC }
SLSEL1(node=17),
{ Filtered SLSEL0 output to VIC }
SLSEL0(node=18),
{ Filtered ICFSEL output to VIC }
ICFSEL(node=19),

EQUATIONS;
{ Enable term built to disable VIC slave select signal generation until the
first register access has occurred to the CY7C964 }
/ENABLE=SYSTEM_RESET * /STROBE*
       +SYSTEM_RESET * /ENABLE;
{ Generate DICFSEL when ENABLE has been activated and LSB_VCOMP* is active}
/DICFSEL=/LSB_VCOMP* * /ENABLE * SYSTEM_RESET;
{ Filter ICFSEL output by ANDing the DICFSEL and the LSB_VCOMP* signal this
method forces the output to remain stable for two clock cycles. }
/ICFSEL=/DICFSEL * LSB_VCOMP* * /ENABLE * SYSTEM_RESET;
{Generate DSLSEL0 when ENABLE has been activated and NMSB_VCOMP* is active }
/DSLSEL0=/NMSB_VCOMP* * /ENABLE * SYSTEM_RESET;
{ Filter SLSEL0 output by ANDing the DSLSEL0 and the NMSB_VCOMP* signal this
method forces the output to remain stable for two clock cycles }
/SLSEL0=/DSLSEL0 * /NMSB_VCOMP* * /ENABLE * SYSTEM_RESET;
{ Generate DSLSEL1 when ENABLE has been activated and both MSB VCOMP* and
NMSB_VCOMP* are active }
/DSLSEL1=/MSB_VCOMP* * /NMSB_VCOMP* * /ENABLE * SYSTEM_RESET;
{ Filter SLSEL1 output by ANDing the DSLSEL1 and the MSB_VCOMP* and NMSB_VCOMP*
signals allows greater than 8 bits of VMEbus address decoding }
/SLSEL1=/MSB_VCOMP* * /NMSB_VCOMP* * /DSLSEL1 * /ENABLE * SYSTEM_RESET;
```

Figure 13. PLD Toolkit™ Design File

The mask and compare registers can be set to select any contiguous address region on the VMEbus. These registers do not preload and can power up in any state. It is advisable to initialize these registers as soon as possible in the system boot sequence. Note that the act of writing the compare register clears the mask register.

The CY7C964 comparator output signal VCOMP* supplies the result from the equality compare logic. VCOMP* drives Low when the input matches the loaded conditions. The CY7C964 VCOMP* signals are not directly compatible with the VIC SLSEL0* and SLSEL1* slave select signals. The short (10 ns) address set up time to AS* active for VMEbus slave boards, does not meet the worst case compare out delay of the CY7C964 VCOMP* signal. Combining this with the potential output glitching that can occur with an asynchronous comparator can cause problems for the VIC. It is recommended that the VCOMP* signal be externally filtered prior to being used with the VIC SLSEL0* or SLSEL1* signal. Most applications will require some external comparison logic to combine VCOMP* signals from the NMSB and MSB device, furnishing finer grained VMEbus decoding: this logic can also be used to filter the CY7C964 VCOMP* signals.

The interface in *Figure 10* uses a 12-ns 18G8 to perform these functions and disable the VMEbus slave select signals to the VIC until the first CY7C964 comparator register access has been performed. Using the PLD allows the interface to decode VMEbus addresses in three different regions:

*   VMEbus A32 (for local access VIC SLSEL0)
*   VMEbus A24 (for local access VIC SLSEL1)
*   VMEbus A16 (for VIC mailbox interrupt and message VIC ICFSEL)

Figure 13 shows the PLD Toolkit design file for this device. The two VIC slave select signals, SLSEL0* and SLSEL1*, can be used to conveniently decode two VMEbus address regions. SLSEL0* will select if the NMSB CY7C964 becomes True. SLSEL1* requires both NMSB and MSB comparators to evaluate True.

A 32-MHz clock and the D registers within the 18G8 are used to build a simple digital filter which removes any glitches that may occur on the CY7C964 VCOMP* signals.

As mentioned previously, the comparators within the CY7C964s are always active, and power up in an unknown state. The PLD includes an Enable signal that disables the SLSEL0*, SLSEL1* and ICFSEL* signals to the VIC until the first access is made to one of the comparator control registers. Adding the Enable function to this PLD guarantees that the VIC slave select signals can not become active until one of the comparator control registers has been initialized.

Local Data Swap Buffer Logic

Local Data Swap Buffer logic is a requirement for all 32-bit local bus designs that perform 8- or 16-bit transfers. The swap buffer moves data to and from the lower section of the VMEbus, D[15:0], to the upper segments of the local bus, D[31:16]. VMEbus requires that all 8- and 16-bit data transfers be performed on the D[15:0] section of the bus. The CY7C964s work properly with the VIC-controlled swap buffer. If an isolation buffer is implemented, care should be taken to ensure that the local data bus is driven to the least-significant CY7C964 during address/mask register programming cycles. One way to ensure this is to assert the $\overline{CS}$ and $\overline{PAS}$ signals to the VIC068/VIC64, thus causing VIC to assert the $\overline{ISOBE}$ signal to the isolation buffer.

VIC Local Control Signal Group

All VIC local interface signals that have not been discussed are not impacted when using the CY7C964s. For further information on the local VIC interface refer to the *VIC068A/VAC068A User's Guide.*

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CYPRESS
SEMICONDUCTOR

Signal Descriptions

VMEbus Signals

A[7:0]

Input: Yes
Output: Yes, three-state
Drive (I_{OL}):   48 mA

These are VMEbus-compatible address signal transceivers that can be directly connected to the VMEbus. A0 is the least significant address bit. In flow-through modes of operation, these signals correspond one for one with local interface signals LA[7:0].

In VMEbus interface applications including those using the VIC068A or VIC64, these signals should be connected to the VMEbus address bus sequentially.

D[7:0]

Input: Yes
Output: Yes, three-state
Drive (I_{OL}):   48 mA

These are VMEbus compatible data signal transceivers that can be directly connected to the VMEbus. D0 is the least data signals. In flow-through modes of operation, these signals correspond one for one with local interface signals LD[7:0].

In VMEbus interface applications, including those using the VIC068A or VIC64, these signals should be connected to the VMEbus address bus sequentially.

Local Signals

LA[7:0]

Input: Yes
Output: Yes, three-state
Drive (I_{OL}):   8 mA

These are medium drive-strength local address transceivers that allow direct connection to memory, micro-processors and/or peripheral controllers. LA0 is the least-significant local address signal. In flow-through operating modes these signals correspond one for one with the VMEbus signals A[7:0].

When implementing conventional VMEbus interfaces or using the CY7C964 with the VIC068A or VIC64, these signals should be connected to the local bus sequentially.

LD[7:0]

Input: Yes
Output: Yes, three-state
Drive (I_{OL}):   8 mA

These are medium drive-strength local address transaceivers that allow direct connection to memory, mi-croprocessors, and/or peripheral controllers. LD0 is the least-significant local address signal. In flow-through operating modes these signals correspond one for one with the VMEbus signals D[7:0].

In VMEbus interface applications, including those using the VIC068A or VIC64, these signals should be connected to the local data bus sequentially.

ABEN*

Input: Yes
Output: No
Drive: None

This is the VMEbus Address Bus ENable control signal. This signal controls the state of the VMEbus address transceivers A[7:0]. When asserted (driven Low) the transceivers are configured as outputs and are enabled.

When using the CY7C964 with the VIC068A or VIC64 to implement VMEbus interfaces, this input should be connected to the ABEN* output of the VIC.

BLT*

Input: Yes
Output: No
Drive: None

This signal controls the VIC-compatible block transfer operations that require local Direct Memory Access (DMA). If this input is driven Low, the CY7C964 will operate in the appropriate VIC-compatible block transfer mode (dependent on the states of the other buffer control logic).

When using the CY7C964 with the VIC068A or VIC64, this signal can be directly connected to the VIC BLT* pin. A rising edge on BLT* increments the local address counters if LCIN* is Low. Refer to the LCIN* signal description and the CY7C964 Operation section of this document for further information on the local address counter function.

D64

Input: Yes
Output: No
Drive: None

This signal is used to indicate to the CY7C964 that a VMEbus D64 block transfer is in progress. When High, the CY7C964 is instructed to use the high-performance two-state pipeline and multiplex or demultiplex 64-bit data to and from the VMEbus address bus.

When used in conjunction with the VIC64, this pin can be directly connected to the SCON*/D64 signal. For applications that only support 32-bit block transfers, as is the case with the VIC068A, this input should be tied Low.

DENIN*

Input: Yes
Output: No
Drive: None

The Data ENable IN signal is used to control the three-state data transceivers LD[7:0]. If a logic Low level is presented to this input, LD[7:0] transceivers will be enabled. In conventional VMEbus designs, this signal would need to be driven during master read or slave write operations.

When used in conjunction with the VIC068A or VIC64, this input is typically connected to UWDENIN* for CY7C964's controlling bus data lines D16 through D31, and to LWDENIN* for the CY7C964's controlling bus data lines D8 through D15.

DENIN1*

Input: Yes
Output: No
Drive: None

The Data ENable IN 1 signal is used in conjunction with DENIN* to latch data from the VMEbus and provide a second enable control of the LD[7:0] transceivers for D64 transactions.

When used in conjunction with VIC64, this input is typically connected to LWDENIN* for CY7C964's controlling data bus signals D16 through D31 and to UWDENIN* for the CY7C964 controlling data bus signals D8 through D15.

DENO*

Input: Yes
Output: No
Drive: None

The Data ENable Out signal is used to control the three-state transceivers D[7:0]. If a logic-Low level is presented to this input, the D[7:0] transceivers will be enabled. In conventional VMEbus design, the D[7:0] signals will be directly connected to the VMEbus. Used in this manner, this input must be asserted during master writes and slave read operations.

When used in conjunction with the VIC068A or VIC64, this signal should be connected to the DENO* output on the VIC.

FC1

Input: Yes
Output: No
Drive: None

The Function Code 1 input is used by the CY7C964 during block transfer operations to determine the source for the local address signals LA[7:0]. If the input is driven High the internal Local DMA counter is selected as the source for LA[7:0]. If this input is Low, the Slave Block Transfer counter is the source for LA[7:0].

When used with the VIC068A or VIC64, this signal can be directly connect to the FC1 bidirectional pin on VIC. VIC will drive this pin to the proper level for slave or block transfer operations when it is master of the local system bus.

LCOUT*

Input: No
Output: Yes
Drive: 8 mA

The Local Carry Out signal is used by the CY7C964 for cascading the local address counter chains. This signal will drive Low when the local address counter has reached the maximum count (255). The signal

generates a synchronous count enable for the next-most-significant CY7C964 in the cascade chain. This signal alone does not cause the local address counter to increment.

When cascading the CY7C964s, this signal should be connected to the LCIN* input pin of the next most significant device. Refer to the description of the LCIN* pin for further information on the operation of the local address counters.

LDS

Input: Yes
Output: No
Drive: None

The Local Data Select input has two main functions: (1) as a control input for the data to address bus multiplexer during D64 VMEbus block transfers, (2) as a select bit for configuring the CY7C964 address comparison and mask registers. Refer to the operation section of this document for further information about how data is steered to and from the VMEbus address bus during block transfers. Typically this input will be connected to LA2. It must be connected to LA2 for proper operation when using the VIC068A or VIC64.

When configuring the CY7C964 internal address mask and address compare registers, this pin in conjunction with MWB* selects which registers to load. During a comparator register load cycle, LDS High will select the Address Compare register; otherwise the Address Mask register will be selected. Refer to the section called Interfacing to the VIC64 and VIC068A for further information on loading the address comparator control registers.

LADI

Input: Yes
Output: No
Drive: None

The Latch ADdress In signal controls a transparent VMEbus to local address latch within the CY7C964. When this input is High, the device will latch the data present on A[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus address during a slave access. If LADI is Low, the internal address latch will be in a flow-through mode. LADI* is also used to incremennt the slave block transfer local address counter. LADI is used in conjunction with LAEN to control the operation of the address VMEbus to local address section of the CY7C964. For more information, refer to the description of LAEN.

When using the CY7C964 to implement VMEbus interfaces, this signal is used to maintain the local address during slave read and write cycles. For VMEbus designs that use the VIC068A or VIC64, this input should be connected to the LADI output of the VIC.

LAEN

Input: Yes
Output: No
Drive: None

The Local Address ENable signal controls the three-state enable for signals LA[7:0]. When this signal is High, LA[7:0] drive the address local bus. Driving the signal Low places LA[7:0] in the high-impedance/input state.

When using the CY7C964 to implement VMEbus interfaces, this signal is driven High to maintain the local address VMEbus during slave cycles. For VMEbus interfaces using the VIC068A or VIC64, this pin should be connected to the LAEN output on the VIC.

LEDI

Input: Yes
Output: No
Drive: None

The Latch Enable Data In signal controls a transparent VMEbus-to-local-data-bus latch within the CY7C964. When this input is High, the device will latch the data present on D[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus data during a master or slave access. If LEDI is Low, the internal address latch will be in a flow-through mode.

LEDI is used in conjunction with DENIN* and DENIN1* to control the operation of the address VMEbus-to-local data section of the CY7C964. For additional information, refer to the description of DENIN* and DENIN1*.

When implementing VMEbus interfaces with the CY7C964, LEDI can be used to maintain the local data during VMEbus master read and slave write cycles. For VMEbus designs that use the VIC068A or VIC64, this input should be connectd to the LEDI output of the VIC.

LEDO

Input: Yes
Output: No
Drive: None

The Latch Enable Data Out signal controls a transparent local-data-to-VMEbus-data latch within the CY7C964. When this input is High, the device will latch the data present on LD[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus data during a master or slave access. If LEDO is Low the internal address latch will be in a flow-through mode.

LEDO is used in conjunction with DENO* to control the operation of the local-to-VMEbus data section of the CY7C964. For further information, refer to the description of DENO*.

When implementing VMEbus interfaces with the CY7C964, LEDO can be used to maintain the VMEbus data during VMEbus master write or slave read cycles. For VMEbus designs that use the VIC068A or VIC64, this input should be connected to the LEDO output of the VIC.

LADO

Input: Yes
Output: No
Drive: None

The Latch Address Out signal controls a transparent local-to-VMEbus address latch within the CY7C964. When this input is High, the device will latch the data present on LA[7:0]. This function is useful when building VMEbus interfaces for latching the local address during a master transfers. If LADO is Low the internal address latch will be in a flow-through mode.

LADO is used in conjunction with ABEN* to control the operation of the local-to-VMEbus address section of the CY7C964. For further information, refer to the description of ABEN*.

When using the CY7C964 to implement a VMEbus interface, this signal can be used to maintain the local address during slave read and write cycles. For VMEbus designs that use the VIC068A or VIC64, this input should be connected to the LADO output of the VIC.

LCIN*

Input: Yes
Output: No
Drive: None

Local Carry IN is a synchronous count enable for both the local master block transfer and slave block transfer local address counters. LCIN* is multiplexed within the CY7C964 and can be routed to either local block transfer address counter. When connected to the master block transfer local address counter, if LCIN* is driven Low, a falling edge on the BLT* signal will increment the address count. When this input is connected to the slave block transfer counter and driven Low, a rising edge of LADI will increment the address count.

When cascading CY7C964s, this signal should be connected to the LCOUT* signal of the next-least-significant device.

MWB*

Input: Yes
Output: No
Drive: None

The Module Wants Bus is a decoding/control signal for the CY7C964 that allows the device to discern the cycle type. When MWB* is active (Low), the CY7C964 assumes that a block transfer initiation cycle of a single-cycle VMEbus transfer is pending. Subsequent assertion of BLT* allows the CY7C964 to enter block transfer mode.

MWB* is also used to decode accesses to the CY7C964 address Mask and Compare registers. To load these registers MWB* must be inactive (High).

Refer to the Interfacing to the VIC64 and VIC068A section for further information on the use of MWB* to load the Address Mask and Compare registers.

STROBE*

Input: Yes
Output: No
Drive: None

The STROBE* signal controls the loading of the internal Address Mask and Compare registers. This signal operates in the same manner as an active-Low chip select for these registers. When STROBE* is Low and MWB* is High, data present on LD[7:0] will be loaded into either the Address Mask or Compare registers.

Refer to the CY7C964 Operation section for further information on the use of MWB* to load the Address Mask and Compare registers.

VCOMP*

Input: No
Output: Yes
Drive: 8 mA

The VMEbus COMPare signal indicates whether the address presented on A[7:0] matches the significant bit of the internal Address Compare register. If the two values are determined to match, VCOMP* will drive Low. (Note: The Address Mask register can mask compare bits, causing these bits match anything.)

Refer to the section called 3 Interfacing to the VIC64 or VIC068A for further information on the use of MWB* to load the Address Mask and Compare registers.

This signal is the output of an asynchronous comparator and is therefore susceptible to glitching during address transitions on A[7:0]. When used in conjunction with theVIC64 or VIC068A for conventional VMEbus implementations, these signals should be de-glitched externally. External logic is required to cascade VCOMP* comparison outputs.

VCIN*

Input: Yes
Output: No
Drive: None

The VMEbus Carry IN is a synchronous count enable for the local address counters. When VCIN* is Low and the device is not operating in the Dual-Address-Path mode, a rising edge on the LADO signal will increment the VMEbus address counter.

When cascading CY7C964s, this signal should be connected to the VCOUT* signal of the next-least-significant device.

For more information on the Dual-Address-Path mode, refer to the CY7C964 Operations sections.

VCOUT*

Input: No
Output: Yes
Drive: 8 mA

The VMEbus Carry Out signal is used by the CY7C964 for cascading the VMEbus address counter chains. This signal will drive Low when the VMEbus address counter has reach the maximum count (255). The signal generates a synchronous count enable for the next-most-significant CY7C964 in the cascade chain. This signal alone does not cause the VMEbus address counter to increment.

When cascading CY7C964s, this signal should be connected to the VCIN* input pin of the next-most-significant device. Refer to the description of the VCIN* pin for further information on the operation of the VMEbus address counters.
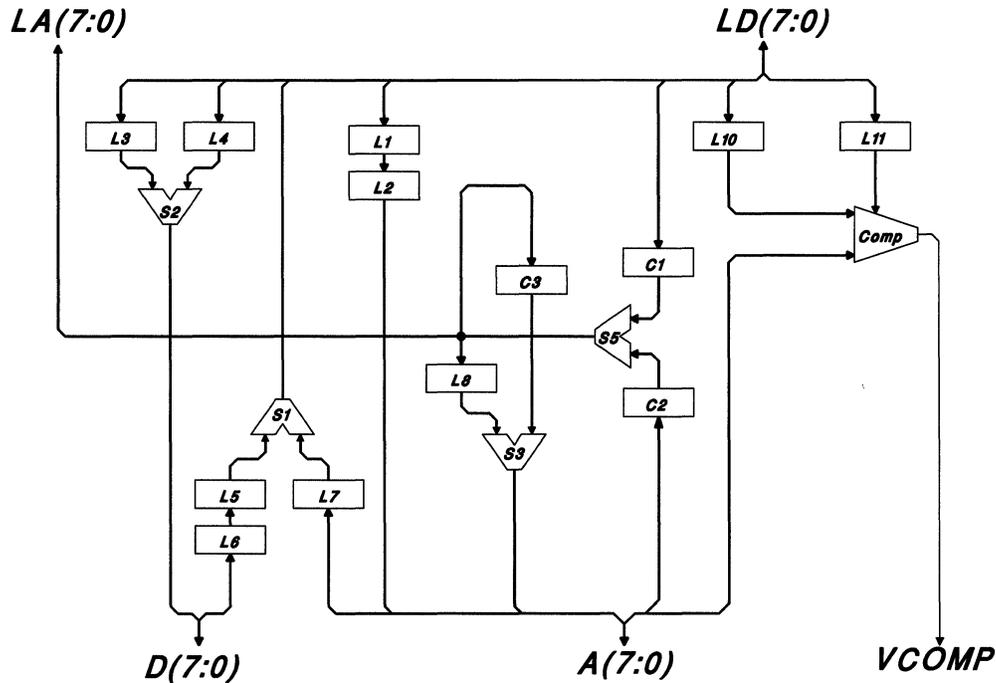
VIC64/7C964-16

Figure 14. CY7C964 Block Diagram

CY7C964 Byte Width Mode Operation

Overview

The CY7C964 is a general-purpose bus interface device that provides seamless support for the VIC64/VIC068A family VMEbus interface controllers. The part is also suitable for many other general-purpose bus interface applications. *Figure 14* is the block diagram of the device, showing the array of latches, multiplexers, and counters.

This section of the document dissects the high-level block diagram into lower-level functional blocks. General operational and timing information is presented on a block-by-block basis. This information is provided for designers who wish to implement non-VIC-controlled interfaces. The tables show the control signal logic sequence needed to operate or communicate with each of the functions. Timing parameters are included, which reference the switching characteristics listed later in this document.

The CY7C964 operation is controlled by the combination of external control signals and internal state logic. Three internal asynchronous state bits control the operating mode of the device. These bits are referred

to as BLT_STATE, BLT_INIT, and DUAL_PATH. The BLT_STATE bit is set during VIC block transfer operations. The VIC block transfer initiation cycle generates a rising edge on the BLT_INIT signal. The DUAL_PATH signal is the output of a transparent latch within the device that latches the state of LADO. These internal state bits must be in the proper state to use and communicate with the internal logic of the device. The functional tables include references to these signals when their state is required for the operation. The designer must perform the appropriate cycle to the device to set or clear these latches as needed prior to the desired functional cycle. The internal latch signals and all other control signals that are not called out within the tables for a specific operation can be considered don't cares.

Table 8. Examples of References to Control Signals Within Functional Tables

Note 1: BLT_STATE=(/BLT* * /MWB*) + (BLT_STATE * (/BLT* + /MWB* + LAEN))
Note 2: BLT_INIT=(/BLT*_STATE * /BLT* * /MWB*) + (BLT_INIT * /BLT* * /MWB*)
Note 3: DUAL_PATH=(LADO * BLT_INIT) + (DUAL_PATH * /BLT_INIT)
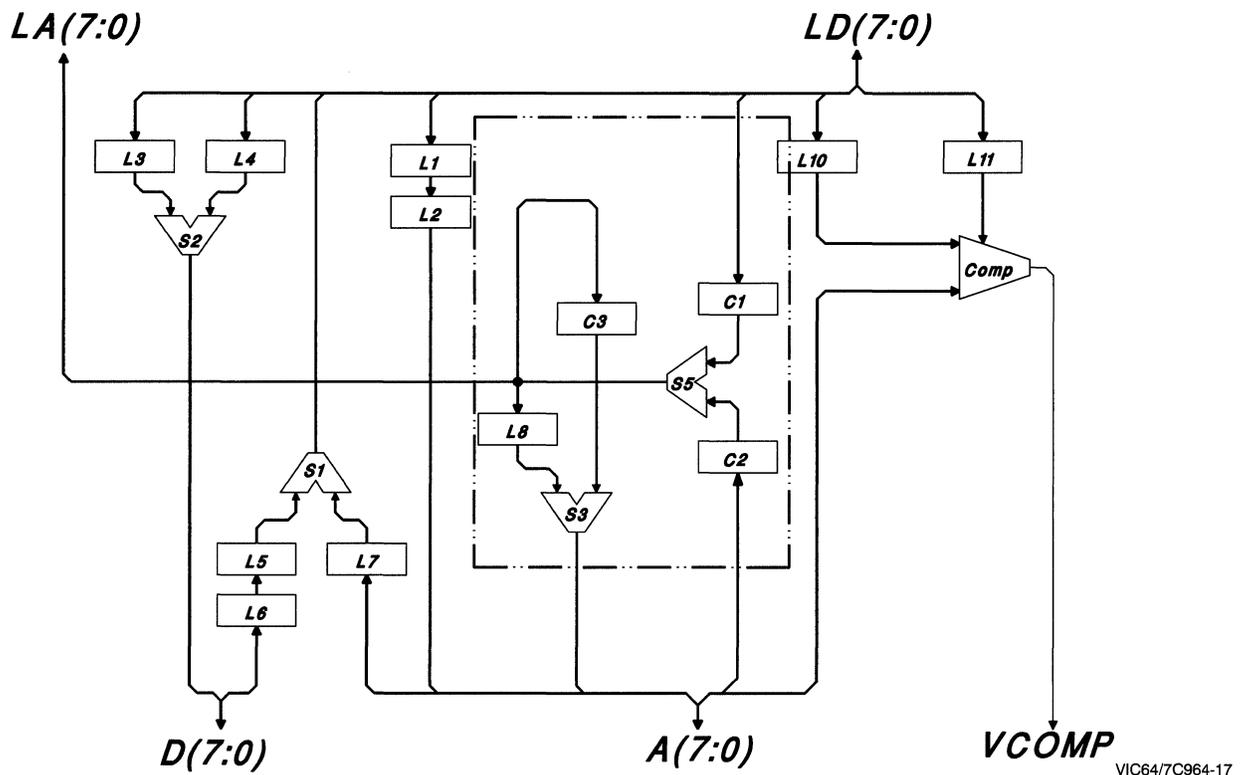
Figure 15. CY7C964 Block Diagram: Address Counters and Address Multiplexers

Master Block Transfer Local Address Counter (C1)

The Master Block Transfer Local Address Counter supplies the local address to LA[7:0] during master block transfer operations. This 8-bit synchronous counter is cascadable using the LCIN*/LCOUT* daisy-chain. The counter powers up in an uninitialized state and must be initialized for predictable operation. The counter loads from LD[7:0] when both MWB* and BLT* control signals are active (Low). To enable

the counter onto LA[7:0], an internal asynchronous latch (BLT_STATE) must be set and Local Address Multiplexer S5 must select counter C1. A falling edge on MWB* or BLT* increments C1. FC1 controls S5. If it is High, as shown in Table 10., C1 is selected. The internal latch and S5 multiplexer must also be in the proper state to increment the counter. For further information on the S5 Local Address Multiplexer, see the next section.

Table 9. Master Block Transfer Local Address Counter Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C1	Load counter	LD[7:0] valid to falling edge of MWB*	BLT*=0, LAEN=0	Set-up t48
				Hold t49
		LD[7:0] valid to falling edge of BLT*	MWB*=0, LAEN=0	Set-up t50
				Hold t51
	Increment counter	MWB* falling edge to LA[7:0] valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t54
		BLT* falling edge to LA[7:0] valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t54
		LCIN* valid to MWB* falling edge	LAEN=1, FC1=1, BLT_STATE=1[1]	Set-up t52
				Hold t53
		LCIN* valid to BLT* falling edge	LAEN=1, FC1=1, BLT_STATE=1[1]	Set-up t52
				Hold t133
	Counter carry out at terminal count	MWB* falling edge to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t55
		BLT* falling edge to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t55
		LCIN* valid to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t56
	Minimum pulse widths	BLT*	LAEN=1, FC1=1, BLT_STATE=1[1]	t57
		MWB*		t57

Local Address Multiplexer (S5)

The Local Address Multiplexer S5 routes the outputs of counters C1 or C2 to signals LA [7:0]. The local address counter carry chain LCIN*/LCOUT* is also controlled by this multiplexer. If FC1 is High counter C1 drives LA[7:0] and LCIN*/LCOUT* are visible/driven by C1, respectively. When FC1 is Low, C2 drives LA [7:0] and is attached to the LCIN*/LCOUT* daisy-chain.

Table 10. Local Address Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
S5	Select C1 counter	FC1 rising edge to LA [7:0] valid		Prop t85
	Select C2 counter	FC1 falling edge to LA [7:0] valid		Prop t86
	Select C1 carry chain	FC1 rising edge to LCOUT* valid		Prop t88
	Select C2 carry chain	FC1 falling edge to LCOUT* valid		Prop t87

Slave Block Transfer Local Address Counter/Latch (C2)

The Slave Block Transfer Local address counter provides two functions: a counter for slave block transfer operations and a transparent address latch for VMEbus slave operations. When the latch control signal LADI is held Low the counter is in a transparent mode: Logic levels present will flow through the device to the inputs of the local address multiplexer S5. FC1 controls the S5 multiplexer and must be Low to select counter C2 as the source for LA[7:0]. Driving either LADI or D64 High exclusively latches the data present on A[7:0]. The counter increments if LCIN* is Low, D64 is High, and a rising edge occurs on LADI. The contents of the counter/latch are enabled onto the local data bus when LADI and FC1 are Low and D64 is High. Counter C2 is not initialized at power-up; for predictable operation the counter should be loaded prior to use.

Table 11. Slave Block Transfer Local Address Counter/Latch Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C2	Load counter	A[7:0] valid to D64 rising edge	LADI=0	Set-up t58
				Hold t59
		A[7:0] valid to LADI rising edge	D64=0	Set-up t60
				Hold t61
	Increment counter	LADI rising edge to LA[7:0]	D64=1, FC1=0	Prop t64
		LCIN* active to LADI rising edge	D64=1	Set-up t62
				Hold t63
	Counter carry out at terminal count	LADI rising edge to LCOUT*	D64=1, FC1=0	Prop t65
	Minimum pulse width	LADI		t66

Master Block Transfer VMEbus Address Counter (C3)

The VMEbus Master Block Transfer Address stores and increments the VMEbus address during master block transfer operations. The counter loads from LA[7:0] on the rising edge of MWB* provided that the internal asynchronous latch BLT_STATE is set. The contents of the counter are enabled onto the A[7:0] pins if the internal asynchronous latch bits BLT_STATE and multiplexer S3 are in the appropriate state. Depending on the state of DUAL_PATH, either the rising or the falling edge of LADO increments C3. Counter C3 uses the VCIN*/VCOUT* counter daisy-chain. This counter is uninitialized at power-up and should be initialized prior to use for predictable operation.

Table 12. Master Block Transfer VMEbus Address Counter Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C3	Load counter	LA[7:0] valid to rising edge of MWB*	BLT_STATE=1[1] BLT_INIT=1	Set-up t67
				Hold t68
	Increment counter	LADO falling edge to A[7:0]	BLT_STATE=1[1], DUAL_PATH=1[3], BLT_INIT=0	Prop t69
		LADO rising edge to A[7:0]	BLT_STATE=1[1], DUAL_PATH=0, BLT_INIT=0	Prop t70
		VCIN* valid to LADO rising/falling edge		Set-up t134
				Hold t135
	Counter carry out	LADO falling edge to VCOUT* valid	BLT_STATE=1[1], DUAL_PATH=1[3], BLT_INIT=0	Prop t71
		LADO rising edge to VCOUT* valid	BLT_STATE=1[1], DUAL_PATH=0, BLT_INIT=0	Prop t72
	Minimum pulse width	LADO (High)		t73
		LADO (Low)		t73

VMEbus Address Latch (L8) and Multiplexer (S3)

The VMEbus Address Latch and Multiplexer selects the source for the VMEbus address signals A[7:0]. The information supplied to A[7:0] originates at one of three sources: the D64 block transfer data pipeline latch L2, the VMEbus master block transfer counter C3, or the VMEbus address latch L8. Table 13 shows how to latch information into the VMEbus address latch L8 and control the selection of the source for signals A[7:0]. Latch L8 is uninitialized at power-up and for predictable operation should be loaded prior to use.

Table 13. VMEbus Address Latch and Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
S3	Select L8	D64 falling edge to A[7:0] valid	BLT_STATE=1[1]	Prop t83
		ABEN* falling edge to A[7:0] valid	BLT_STATE=1[1]	Prop t84
		D64 falling edge to A[7:0] valid	BLT_STATE=0	Prop t81
L8	Load L8	LA[7:0] valid to LADO rising edge		Set-up t40
				Hold t41
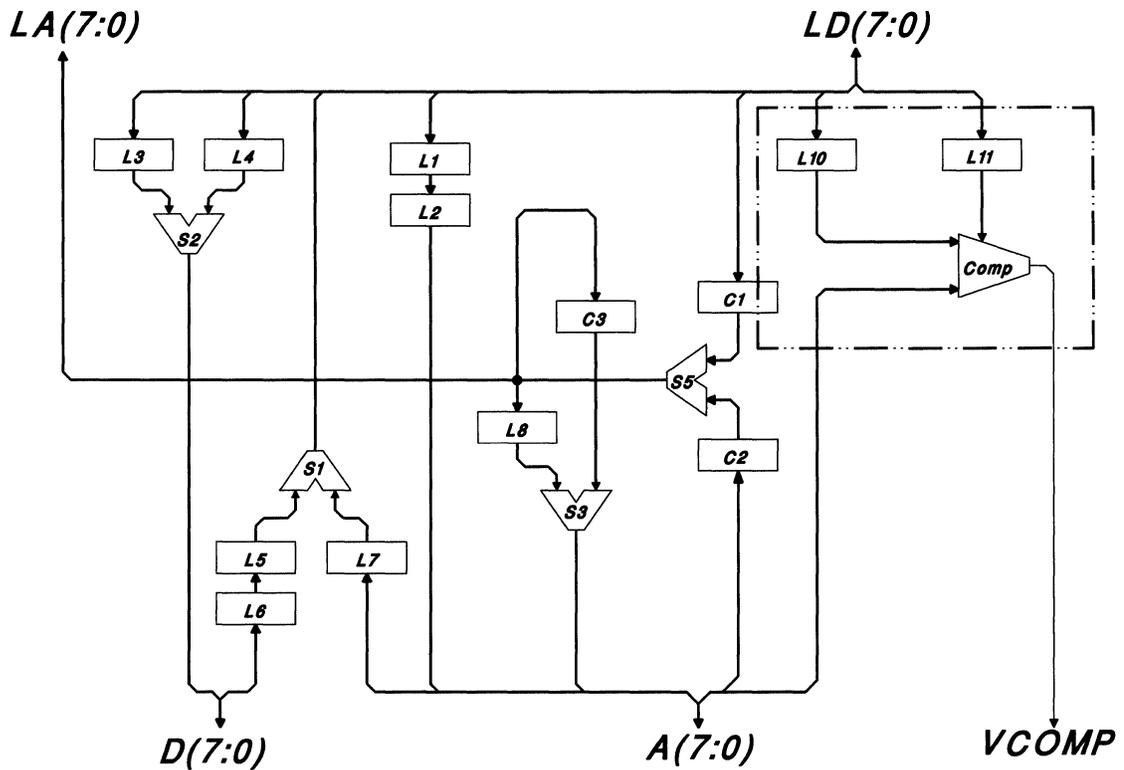
VIC64/7C964-18

Figure 16. CY7C964 Block Diagram: VMEbus Address Comparator

VMEbus Address Comparator

The VMEbus Address Comparator is made up of three logic elements: an address mask register, address compare register, and a high-performance, 8-bit, equality comparator. The compare and mask registers control the compare logic. The mask register contains an 8-bit value that enables or disables bits of the comparator. The compare register contains an 8-bit pattern. The enabled bits of the compare register are matched against the value on A[7:0]. If a match is detected (all active bits equal), the VCOMP* output pin is driven Low. Neither the compare register nor the mask register are preset at power-up and must be initialized for predictable operation. The act of writing the compare register clears the mask register. This prevents any inadvertant address compares during the configuration process. See the Interfacing to the VIC64 and VIC068A section for further information on the VMEbus address comparator.

Table 14. VMEbus Address Comparator Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L10	Select compare register	LDS, MWB* valid to STROBE* falling edge	LDS=1, MWB*=1	Set-up t43
				Hold t44
	Load compare register	LD[7:0] valid to STROBE* rising edge		Set-up t46
				Hold t47
L11	Select mask register	LDS, MWB* valid to STROBE* falling edge	LDS=0, MWB*=1	Set-up t43
				Hold t44
	Load compare register	LD[7:0] valid to STROBE* rising edge		Set-up t46
				Hold t47
	Compare out	A[7:0] valid to VCOMP* valid		Prop t23
		A[7:0] valid to VCOMP* invalid		Prop t24
	Minimum pulse width	STROBE* minimum pulse width		t47

VMEbus D64 Block Transfer Data Pipeline and Multiplexer

Latches L1 and L2 form a two-stage high-performance data pipeline for D64 block transfer operations. These latches load from the local signals LD[7:0], but drive VMEbus address signals A[7:0]. Latches L3 and L4 load from the local data signals LD[7:0] and in combination with multiplexer S2 drive D[7:0]. On the first cycle of a D64 block transfer data on LD[7:0] is written to latch L1. During the second local data fetch of a D64 block transfer operation (D64 = 1), data from LD[7:0] is written to latch L3 and the data within latch L1 moves to L2. Two fetches must be performed to form the 64-bit block transfer data word. During non-D64 modes of operation (D64=0) data from LD[7:0] is written to latch L4. This is the normal data path from LD[7:0] to D[7:0] for all non-D64 operation. Because all the latches are implemented on transparent latches, L2 may be loaded from LD[7:0] when L1 is transparent (LEDO=0). None of the latches are initialized at power-up. Therefore for predictable operation these latches should be written prior to their use.

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Figure 17. CY7C964 Block Diagram: D64 Block Transfer Data Pipeline and Multiplexer

Table 15. VMEbus D64 Block Transfer Data Pipeline and Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L1	Load register	LD[7:0] valid to LEDO rising edge		Set-up t25
				Hold t26
L2	Load register	LD[7:0] valid to DENO* falling edge	LEDO=0	Set-up t28
				Hold t29
	Drive A[7:0]	D64 rising edge to A[7:0] valid	BLT_STATE=1	Prop t82
L3	Load register	LD[7:0] valid to DENO* rising edge		Set-up t25
				Hold t26
L4	Load register	LD[7:0] valid to LEDO* rising edge		Set-up t131
				Hold t132
S2	Multiplexer selects L3 drive D[7:0]	D64 rising edge to D[7:0] valid		Prop t78
	Multiplexer selects L4 drive D[7:0]	D64 falling edge to D[7:0] valid		Prop t79
	Minimum pulse width	DENO*		t30
		LEDO		t27

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Figure 18. CY7C964 Block Diagram: D64 Block Transfer Data Demultiplexer

VMEbus D64 Block Transfer Data Demultiplexer

The VMEbus D64 block transfer data demultiplexer moves data from D[7:0]/A[7:0] to LD[7:0]. The demultiplexer consists of three latches-L5, L6, and L7-and an output multiplexer, S1. During D64 block transfer operations (D64=1), data is written to latches L6 and L7 simultaneously on the rising edge of LEDI. Multiplexer S1 then selects either latch L6 or L7, depending on the state of LDS as a source for LD[7:0]. In most applications, LDS should be connected to LA2, showing that L7 contains even 32-bit words (addresses 0, 8, $10_{16}...$) and L6 contains odd 32-bit words (addresses 4, C, $14_{16}...$). Latch L6 is also used for non-D64 operating modes. None of these latches are initialized at power-up and for predictable operation should be initialized prior to use.

Table 16. VMEbus D64 Block Transfer Data Demultiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameters
L5	Load register	D[7:0] valid to DENIN* falling edge	DENIN1*=0, LEDI=0	Set-up t31
				Hold t32
	Load register	D[7:0] valid to DENIN1* falling edge	DENIN*=0, LEDI=0	Set-up t34
				Hold t35
L6	Load register	D[7:0] valid to LEDI rising edge	LEDO=0	Set-up t37
				Hold t38
L7	Load register	A[7:0] valid to LEDI rising edge	LEDO=0	Set-up t37
				Hold t38

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Table 17. VMEbus D64 Block Transfer Data Demultiplexer Operation (Continued)

Logic	Functional Description	Operational Description	Required Condition	Parameter
S1	Select L5	LDS rising edge to LD[7:0] valid	D64=1	Prop t74
		D64 rising edge to LD[7:0] valid	LDS=1	Prop t76
	Select L7	LDS falling edge to LD[7:0] valid	D64=1	Prop t75
	Select L6	D64 falling edge to LD[7:0] valid		Prop t77
	Minimum pulse width	DENIN*		t33
		DENIN1*		t36
		LEDI		t39

CY7C964 Byte Width Mode Alternate BLT Initiation Operation

Another method of loading the VMEbus block transfer address counters exists within the CY7C964. This method has been placed within its own section of the document because it is not completely compatible with the VIC block transfer initiation cycle.

The CY7C964 determines the source for loading the VMEbus master block transfer counter C3 by monitoring the arrival sequence of the MWB* and BLT* signals. For typical block transfers initiation cycles the assertion of MWB* occurs prior to the assertion of the BLT*. The VMEbus master block transfer counter C3 loads from the local address pins, LA[7:0], as described within a previous section of this document.

Reversing the arrival order of these two signals changes the operation of the device. This is done at system design time by swapping the BLT* and MWB* inputs to the CY7C964. For proper operation, these signals must continue to operate in the same manner as they do on the VIC, even though they are no longer connected to the associated input pins on the CY7C964 which have the same name. Swapping these signals on the device changes the way that the VMEbus master block transfer counter C3 is loaded. In this mode it loads from the local data bus via latch L9. All other functions within the device operate in the same manner as described within the previous section.

Loading C3 is accomplished with a local cycle similar to the cycles needed to load the mask and compare registers. This cycle operates as follows: LDS is driven high, (most likely this signal is connected to LA2), the MWB* input pin of the CY7C964 is driven Low, (this pin is actually connected to the open collector BLT* output of the VIC), and STROBE* is asserted. The local data bus should be driven to the appropriate value for the address to load into the C3 counters. STROBE* is deasserted and the data is latched into L9 within the CY7C964. The local address decode signal used to assert MWB* on the CY7C964, (BLT* on the VIC), must be a three-state or an open-collector output. This signal must not be driven high or the VIC will be unable to perform block transfers.

A normal master block transfer initiation cycle is then performed, with one minor exception. The lower 8 bits of address LA[7:0] which are controlled by the VIC, must contain the desired lower address. This is needed because the VIC operates in the typical block transfer initiation mode. The upper address LA[31:8] will be ignored by the CY7C964s during the initiation cycle.
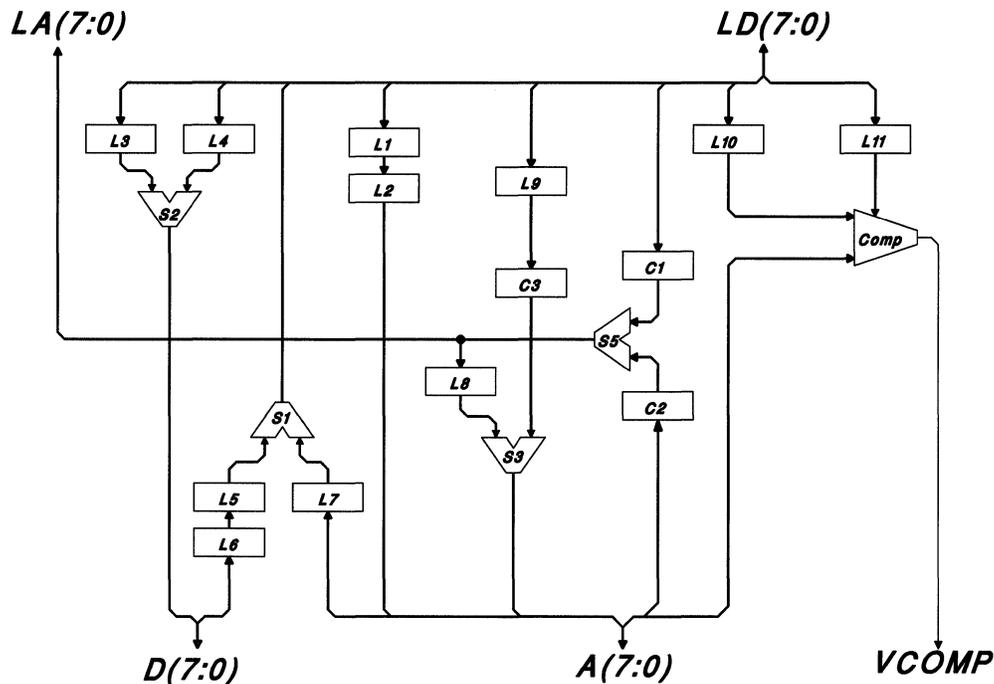
VIC64/7C964-21

Figure 19. CY7C964 Byte Width Mode Alternate BLT Operation Block Diagram

This mode of operation allows the VMEbus master block transfer address counters to be loaded independent of the VMEbus address. This has advantages in some designs, but C3 cannot be used to source single cycle transfer addresses. This limitation should be considered while performing the design analysis to use this mode.

Table 17. Byte Width Mode Alternate BLT Initiation Operation

Logic	Functional Description	Operational Description	Required Condition	Parameters
L9	Select register	LDS, MWB* valid to STROBE* falling edge	LDS=1, MWB*=0	Set-up t43
				Hold t44
	Load register	LD[7:0] valid to STROBE* rising edge		Set-up t45
				Hold t46
	Minimum pulse width	STROBE*		t46

CY7C964 Word Width Mode Operation

The second operating personality of the CY7C964 is a 16-bit wide address or data-only controller. The device is more suited to be an address controller for conventional VMEbus interfaces because the block transfer counters C1, C2, and C3 and the comparator operate in the same manner as described in the previous section, but they expand to 16 bits wide. Data-related functions such as the data multiplexer and data demultiplexer are not available in this mode of operation.
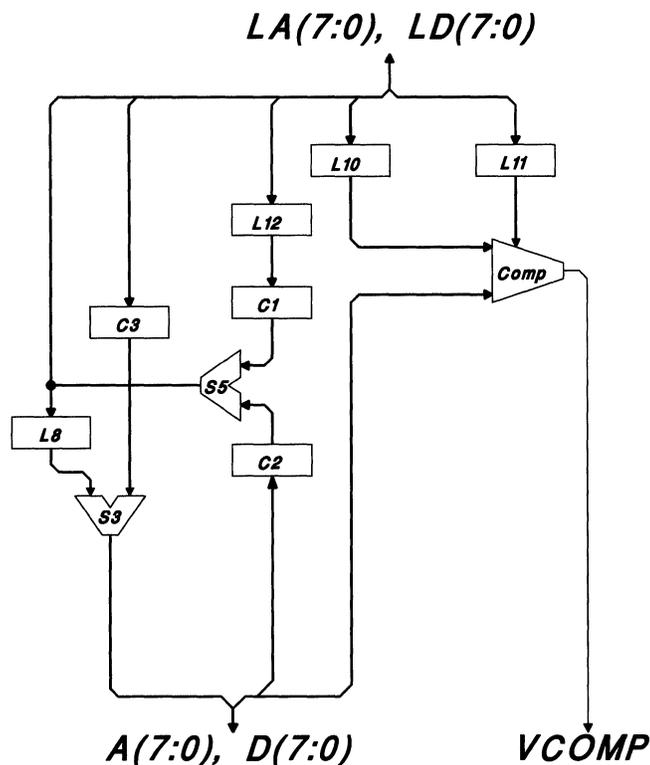
Figure 20. CY7C964 Block Diagram for Word Width Mode of Operation

The address and data signals A[7:0], D[7:0], LA[7:0], and LD[7:0] are combined to form two 16-bit buses. A high drive-strength, 16-bit bus-A[7:0], D[7:0]-and a medium drive-strength bus-LA[7:0], LD[7:0], D[7:0], and LD[7:0]-are the least-significant bytes of these buses.

The word width mode of operation has a rich set of features for use as a 16-bit VMEbus address controller. Because of this, the local bus-LA[7:0], LD[7:0] and A[7:0], D[7:0]-are being referred to as the local and VMEbus address buses within this section of the document.

In word width mode, one additional latch, L12, is located between the local address bus and local master block transfer counter C1. This latch allows the local master block transfer counter to be loaded from the local address bus prior to loading the VMEbus master block transfer counter C3. This is necessary since both VMEbus master block transfer counter C3 and the local master block transfer counter C1 are loaded from the same local address bus. When the VMEbus master block counter C3 loads during the block transfer initiation cycle, the contents of latch L12 are moved to counter C1. To write L12, LDS and DENIN* must both be Low. In the same manner as the byte width mode, C3 is normally loaded directly from LA[7:0], LD[7:0]. If the arrival order of MWB* and BLT* is reversed, the device operates in a similar manner to the byte width mode, using L9 to hold the information destined for C3. This operation is described on page 61 of this book.

To place the device in word width mode of operation, input signals LEDO and LEDI should be tied High. The address compare and mask registers load in a similar manner to the byte width mode, except DENIN* replaces MWB* as a control input for register decoding. Mask and compare register load waveforms are shown in *Figure 21* and *Figure 22*.

Load CY7C964 Mask Register
Word Width Mode
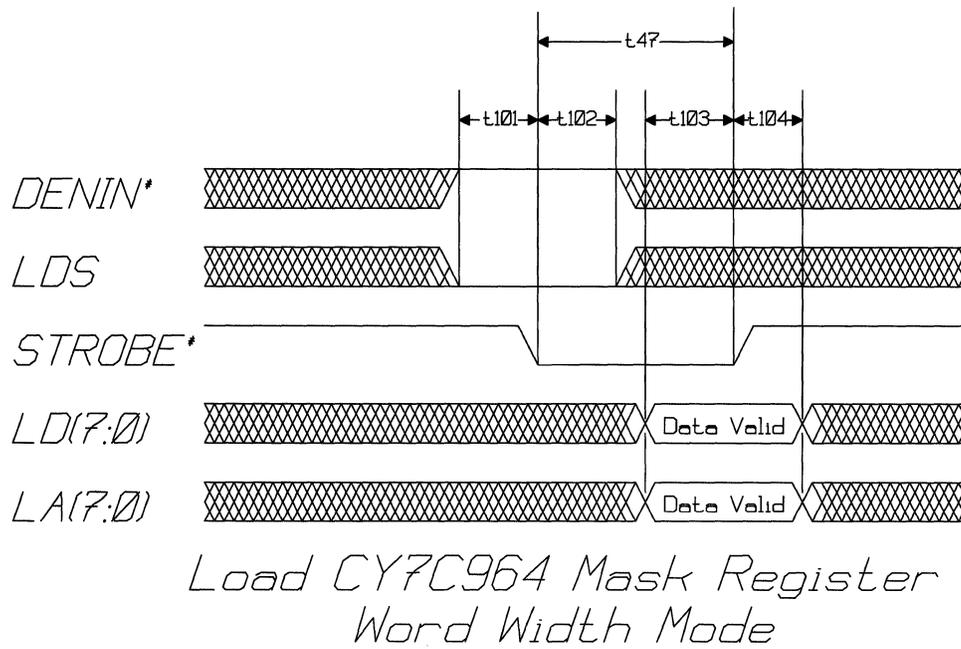
VIC64/7C964-23

Figure 21. Mask Register Load Timing in Word Width Mode

Load CY7C964 Compare Register
Word Width Mode
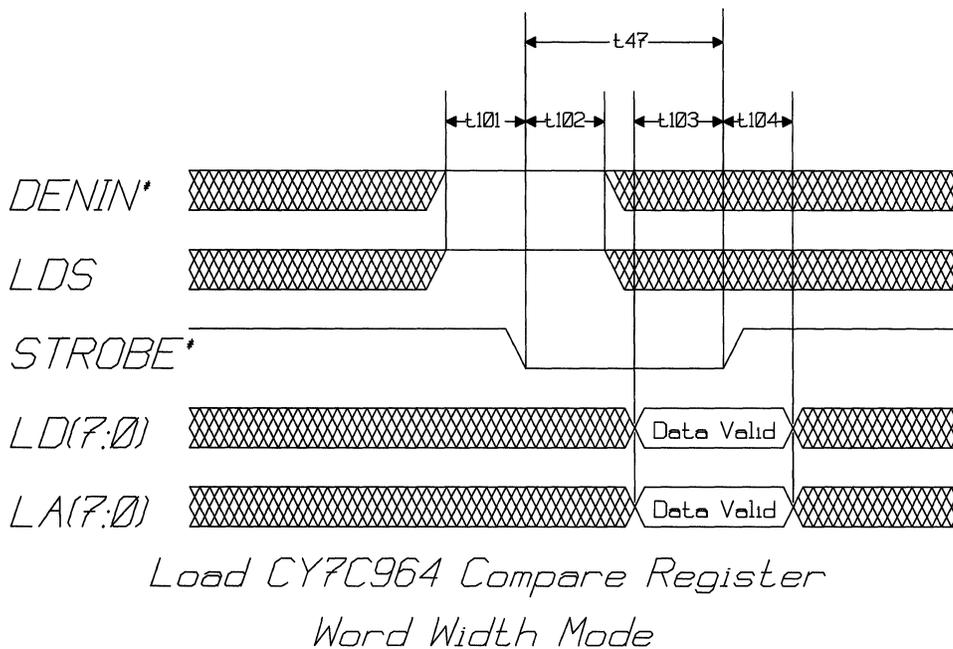
VIC64/7C964-24

Figure 22. Compare Register Load Timing in Word Width Mode

Load CY7C964 Local Block Transfer Address
Word Width Mode

VIC64/7C964-25
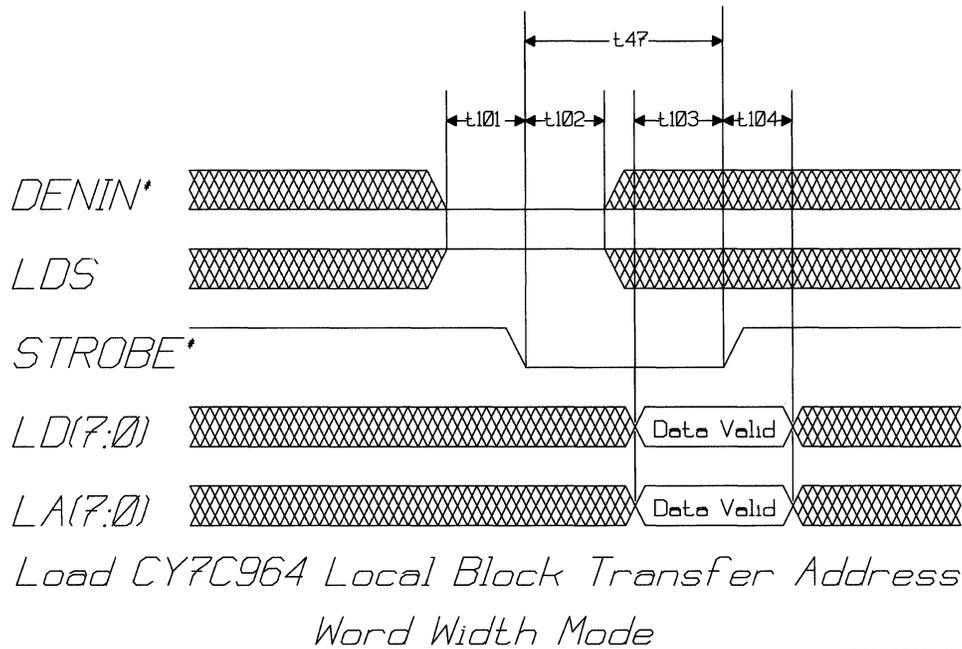
Figure 23. Local Block Transfer Address in Word Width Mode

The block transfer initiation cycle shanges slightly in the word width mode. The typical block transfer initiation cycle loads the local DMA address into the local DMA counter C1 from the data bus. This is not possible in the word width mode because the part is strictly an address controller and does not have a data bus.

Two cycles are required to initiate a block transfer in word width mode. The first cycle is used to set up the local DMA counter C1. This cycle is similar to the mask and compare register cycles. *Figure 23* shows the timing waveform for this cycle. The VMEbus block transfer address counter C3 is loaded using the usual VIC block transfer initiation cycle with the local address bus containing the large VMEbus address. It is important to note that the local DMA address must be loaded first, because the typical VIC block transfer cycle will begin the block transfer using the contents of the local DMA block transfer C3.

Table 18. Word Width Mode Operation

Logic	Functional Description	Operational Description	Required Condition	Parameters
L12	Select register	LDS, DENIN* valid to STROBE* falling edge	LDS=1, DENIN*=0	Set-up t43
				Hold t44
	Load register	LD[7:0] valid to STROBE* rising edge		Set-up t45
				Hold t46
	Minimum pulse width	STROBE*		t46

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DC Performance Specifications

VMEbus Signals (A[7:0], D[7:0])

Parameter	Description	Test Condition	Military/Industrial/Commercial	Unit
V_{IH}	Minimum high-level input voltage		2.0	V
V_{IL}	Maximum high-level input voltage		0.8	V
V_{OH}	Minimum high-level output voltage	V_{CC}=minimum I_{OH} = -3 mA	2.4	V
V_{OL}	Minimum low-level output voltage	V_{CC}=minimum I_{OL} = 48 mA	0.6	V
I_L	Maximum input leakage current	V_{CC}=maximum V_{IN}=0.6 - 2.4	± 5	uA
V_{IK}	Input clamp voltage	V_{CC}=min I_{IN}= -18 mA V_{CC}=min I_{IN}= 18 mA	-1.2 V_{CC} +1.2	V V
I_{OZ}	Maximum output leakage current	V_{CC}=maximum GND$\leq V_{OUT}$ $\leq V_{CC}$ all outputs disabled	± 10	uA

Non-VMEbus Signals

Parameter	Description	Test Condition	Military/Industrial/Commercial	Unit
V_{IH}	Minimum high-level input voltage		2.0	V
V_{IL}	Maximum high-level input voltage		0.8	V
V_{OH}	Minimum high-level output voltage	V_{CC}=minimum I_{OH} = -8 mA	2.4	V
V_{OL}	Maximum input leakage current	V_{CC}=maximum I_{OL} = 8 mA	0.6	V
I_L	Maximum input leakage current	V_{CC}=maximum V_{IN}=0 $- V_{CC}$	± 5	uA
V_{IK}	Input clamp voltage	V_{CC}=min I_{IN}= -18 mA V_{CC}=min I_{IN}= 18 mA	-1.2 V_{CC} +1.2	V V

Non-VMEbus Signals

Parameter	Description	Test Condition	Military/Industrial/Commercial	Unit
I_{OZ}	Maximum output leakage current	V_{CC}=maximum GND$\leq V_{OUT}$ $\leq V_{CC}$ all outputs disabled	$\pm$ 5	uA
I_{CC}	V_{CC} maximum operating supply current	V_{CC}=maximum all outputs disabled	25	mA

AC Performance Specifications

Byte Width Mode

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t1	LA[7:0] to A[7:0] propagation delay[2]		15	16	18	ns	
t2	LD[7:0] to D[7:0] propagation delay		16	17	19	ns	
t3	A[7:0] to LA[7:0] propagation delay		17	18	20	ns	
t4	D[7:0] to LD[7:0] propagation delay[2]		19	20	22	ns	
t5	LD[7:0] to A[7:0] propagation delay[2]		19	20	22	ns	D64 = 1
t6	A[7:0] to LD[7:0] propagation delay[2]		19	20	22	ns	D64 = 1
t7	ABEN* active to A[7:0] output enable delay[2]		11	11	12	ns	
t8	DENO* active to D[7:0] output enable delay[2]		14	15	16	ns	
t9	ABEN* active to D[7:0] output enable delay		14	15	17	ns	D64 = 1
t10	D64 active to D[7:0] output enable delay[2]		13	14	15	ns	ABEN* = 0
t11	LAEN active to LA[7:0] output enable delay[2]		10	11	12	ns	
t12	DENIN* active to LD[7:0] output enable delay		15	16	18	ns	
t13	DENIN1* active to LD[7:0] output enable delay[2]		18	19	21	ns	D64 = 1
t14	D64 active to LD[7:0] output enable delay[2]		18	19	21	ns	DENIN1* = 0

Byte Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t15	ABEN* inactive to A[7:0] High-Z outputdisable delay[2]		8	10	12	ns	
t16	DENO* inactive to D[7:0] High-Z output disable delay[2]		12	14	15	ns	
t17	ABEN* inactive to D[7:0] High-Z output disable delay[2]		12	14	15	ns	D64 = 1
t18	D64 inactive to D[7:0] High-Z output disable delay[2]		14	15	16	ns	ABEN* = 0
t19	LAEN Inactive to LA[7:0] High-Z output disable delay[2]		13	14	15	ns	
t20	DENIN* inactive to LD[7:0] High-Z output disable delay[2]		14	16	18	ns	
t21	DENIN1* Inactive to LD[7:0] High-Z output disable delay[2]		14	16	18	ns	D64 = 1
t22	D64 inactive to LD[7:0] High-Z output disable delay[2]		19	21	24	ns	DENIN1* = 0
t23	A[7:0] to VCOMP* High-to-Low propagation delay		18	19	21	ns	
t24	A[7:0] to VCOMP* Low-to-High propagation delay		16	17	19	ns	
t25	LD[7:0] set-up time to DENO* rising edge[1]	7				ns	
t26	LD[7:0] hold time after DENO* rising edge[1]	0				ns	
t27	LEDO minimum pulse width[1]	7				ns	
t28	LD[7:0] set-up time to DENO* falling edge[1]	0				ns	LEDO* = 0
t29	LD[7:0] hold time after DENO* falling edge[1]	7				ns	LEDO* = 0
t30	DENO* minimum pulse width[1]	10				ns	
t31	D[7:0] set-up time to DENIN* falling edge[1]	5				ns	DENIN1*=0, LEDI=0
t32	D[7:0] hold time after DENIN* falling edge[1]	5				ns	DENIN1*=0, LEDI=0
t33	DENIN* minimum pulse width[1]	10				ns	
t34	D[7:0] set-up time to DENIN1* falling edge[1]	5				ns	
t35	D[7:0] hold time after DENIN1* falling edge[1]	5				ns	
t36	DENIN1* minimum pulse width[1]	10				ns	

Byte Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t37	D[7:0], A[7:0] set-up time to LEDI rising edge[1]	7				ns	
t38	D[7:0], A[7:0] hold time after LEDI rising edge[1]	0				ns	
t39	LEDI minimum pulse width[1]	10				ns	
t40	LA[7:0] set-up time to LADO rising edge[1]	5				ns	
t41	LA[7:0] hold time after LADO rising edge[1]	5				ns	
t42	LADO minimum pulse width[1]	10				ns	
t43	MWB*, LDS setup time to STROBE* falling edge[1]	0				ns	
t44	MWB*, LDS hold time after STROBE* falling edge[1]	5				ns	
t45	LD[7:0] set-up time to STROBE* rising edge[1]	5				ns	
t46	LD[7:0] hold time after STROBE* rising edge[1]	5				ns	
t47	STROBE* minimum pulse width[1]	10				ns	
t48	Local master block transfer address counter C1 LD[7:0] set-up time before MWB* falling edge[1]	0				ns	BLT*, LAEN=0
t49	Local master block transfer address counter C1 LD[7:0] hold time after MWB* falling edge[1]	5				ns	BLT*, LAEN=0
t50	Master block transfer local address counter C1 LD[7:0] set-up time to BLT* falling edge[1]	0				ns	MWB*, LAEN=0
t51	Master block transfer local address counter C1 LD[7:0] hold time after BLT* falling edge[1]	5				ns	MWB*, LAEN=0
t52	LCIN* set-up time to MWB* falling edge[1]	5				ns	BLT_STATE, LAEN, FC1 = 1
t53	LCIN* hold time after MWB* or BLT* falling edge[1]	0				ns	BLT_STATE, LAEN, FC1 = 1
t54	MWB*, BLT* falling edge to LA[7:0]propagation delay		21	22	25	ns	BLT_STATE, LAEN, FC1 = 1
t55	MWB*, BLT* falling edge to LCOUT* propagation delay		24	25	28	ns	BLT_STATE, LAEN, FC1 = 1

Byte Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t56	LCIN* to LCOUT* propagation delay[2]		17	18	20	ns	BLT_STATE, LAEN, FC1 = 1
t57	BLT*, MWB* minimum pulse width[1]	10				ns	
t58	Slave block transfer local address counter C2, A[7:0] set-up time to D64 rising edge[1]	5				ns	LADI = 0
t59	Slave block transfer local address counter C2, A[7:0] hold time after D64 rising edge[1]	5				ns	LADI = 0
t60	Slave block transfer local address counter C2, A[7:0] set-up time to LADI rising edge[1]	5				ns	D64 = 0
t61	Slave block transfer local address counter C2, A[7:0] hold time after LADI rising edge[1]	5				ns	D64 = 0
t62	LCIN* set-up time to LADI rising edge[1]	8				ns	D64 = 1
t63	LCIN* hold time after LADI rising edge[1]	0				ns	D64 = 1
t64	LADI rising edge to LA[7:0] valid propagation delay		15	16	18	ns	D64 = 1, FC1=0
t65	LADI rising edge to LCOUT* valid propagation delay		20	21	24	ns	D64 = 1, FC1=0
t66	LADI minimum pulse width[1]	10				ns	
t67	Master block transfer VMEbus address counter LA[7:0] set-up time to MWB* rising edge[1]	5				ns	BLT_STATE=1 BLT_INIT=1
t68	Master block transfer VMEbus address counter LA[7:0] hold time after MWB* rising edge[1]	5				ns	BLT_STATE=1 BLT_INIT=1
t69	LADO falling edge to A[7:0] valid propagation delay		23	24	27	ns	BLT_STATE, DUAL PATH=1, BLT_INIT=0
t70	LADO rising edge to A[7:0] valid propagation delay[2]		24	25	28	ns	BLT_STATE,=1, DUAL PATH=0, BLT_INIT=0
t71	LADO falling edge to VCOUT* valid propagation delay		26	27	30	ns	BLT_STATE, DUAL PATH=1, BLT_INIT=0

Byte Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t72	LADO rising edge to VCOUT* valid propagation delay[2]		30	33	36	ns	BLT_STATE, DUAL PATH=0, BLT_INIT=0
t73	LADO minimum High or Low pulse width[1]	10				ns	
t74	LDS rising edge to LD[7:0] valid propagation delay[2]		20	21	24	ns	D64 = 1
t75	LDS falling edge to LD[7:0] valid propagation delay		20	21	24	ns	D64 = 1
t76	D64 rising edge to LD[7:0] valid propagation delay[2]		21	22	24	ns	
t77	D64 falling edge to LD[7:0] valid propagation delay		21	22	25	ns	
t78	D64 rising edge to D[7:0] valid propagation delay[2]		16	16	18	ns	
t79	D64 falling edge to D[7:0] valid propagation delay[2]		19	19	21	ns	
t80	D64 rising edge to A[7:0] valid propagation delay[2]		15	16	18	ns	
t81	D64 falling edge to A[7:0] valid propagation delay[2]		16	17	19	ns	BLT_STATE=0
t82	D64 rising edge to A[7:0] valid propagation delay[2]		19	19	22	ns	BLT_STATE=1
t83	D64 falling edge to A[7:0] valid propagation delay		20	21	23	ns	BLT_STATE=1
t84	ABEN* falling edge to A[7:0] valid propagation delay[2]		11	11	12	ns	BLT_STATE=1
t85	FC1 rising edge to LA[7:0] valid propagation delay[2]		14	15	17	ns	
t86	FC1 falling edge to LA[7:0] valid propagation delay		17	18	20	ns	
t87	FC1 falling edge to LCOUT* valid propagation delay[2]		17	18	20	ns	
t88	FC1 rising edge to LCOUT* valid propagation delay		17	18	20	ns	
t89	LADO set-up time to MWB*, BLT* rising edge[1]	0				ns	BLT_STATE=1
t136	LADO hold time after MWB*, BLT* rising edge[1]	7				ns	BLT_STATE=1
t137	BLT* set-up time to MWB* falling edge[1]	5				ns	

Byte Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t90	BLT* hold time after MWB* falling edge[1]	5				ns	
t131	LD[7:0] to DENO* falling edge set-up[1]	5				ns	
t132	LD[7:0] after DENO* falling edge[1]	5				ns	
t133	LCIN* hold time after BLT* falling edge[1]	5				ns	

Word Width Mode

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t91	LA[7:0], LD[7:0] to A[7:0], D[7:0] propagation delay[2]		16	17	19	ns	
t92	A[7:0], D[7:0] to LA[7:0], D[7:0] propagation delay[2]		16	17	19	ns	
t93	LAEN rising edge to LA[7:0], LD[7:0] valid[2]		16	17	19	ns	
t94	ABEN* falling edge to A[7:0], D[7:0] valid[2]		14	15	17	ns	
t95	LAEN falling edge to LA[7:0], LD[7:0] high impedance[2]		13	14	15	ns	
t96	ABEN* rising edge to A[7:0], D[7:0] high impedance[2]		12	14	15	ns	
t97	A[7:0], D[7:0] valid to VCOMP* active (Low)[2]		18	21	23	ns	
t98	A[7:0], D[7:0] valid to VCOMP* inactive (High)[2]		18	21	23	ns	
t99	LA[7:0], LD[7:0] set-up time to LADO rising edge[1]	7				ns	
t100	LA[7:0], LD[7:0] hold time after LADO rising edge[1]	0				ns	
t101	DENIN* set-up time to STROBE* falling edge[1]	0				ns	
t102	DENIN* hold time after STROBE* falling edge[1]	5				ns	
t103	LA[7:0], LD[7:0] set-up time to STROBE* rising edge[1]	5				ns	

Word Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t104	LA[7:0], LD[7:0] hold time after STROBE* rising edge[1]	5				ns	
t105	LA[7:0], LD[7:0] set-up time to MWB* falling edge[1]	0				ns	BLT*, LAEN=0
t106	LA[7:0], LD[7:0] hold time after MWB* falling edge[1]	5				ns	BLT*, LAEN=0
t107	LA[7:0], LD[7:0] set-up time to BLT* falling edge[1]	0				ns	MWB*, LAEN=0
t108	LA[7:0], LD[7:0] hold time after BLT* falling edge[1]	5				ns	MWB*, LAEN=0
t109	MWB* falling edge to LCOUT* valid propagation delay[2]		33	35	38	ns	BLT_STATE, LAEN, FC1=1
t110	BLT* falling edge to LCOUT* valid propagation delay[2]		33	34	38	ns	BLT_STATE, LAEN, FC1=1
t111	A[7:0], D[7:0] set-up time to D64 rising edge[1]	5				ns	LADI=0
t112	A[7:0], D[7:0] hold time after D64 rising edge[1]	5				ns	LADI=0
t113	A[7:0], D[7:0] set-up time to LADI rising edge[1]	5				ns	D64=0
t114	A[7:0], D[7:0] hold time after LADI rising edge[1]	5				ns	D64=0
t115	LADI rising edge to LA[7:0], LD[7:0] valid[2]		20	21	24	ns	D64=1, FC1=0
t116	LADI rising edge to LCOUT* valid		20	21	24	ns	D64=1, FC1=0
t117	LADI minimum pulse width[1]	10				ns	
t118	LA[7:0], LD[7:0] set-up time to MWB* rising edge[1]	5				ns	BLT_STATE=1
t119	LA[7:0], LD[7:0] hold time after MWB* rising edge[1]	5				ns	BLT_STATE=1
t120	LADO falling edge to A[7:0], D[7:0] valid[2]		27	28	31	ns	BLT_STATE, DUAL PATH, LAEN, FC1=1
t121	LADO rising edge to A[7:0], D[7:0] valid[2]		24	25	28	ns	BLT_STATE, LAEN, FC1=1, DUAL PATH=0
t122	LADO falling edge to VCOUT* valid[2]		30	33	36	ns	BLT_STATE, DUAL PATH, LAEN, FC1=1

Word Width Mode (continued)

Parameter	Description	Min. All Grades	Max. Com'l	Max. Ind	Max. Mil	Unit	Comment
t123	LADO rising edge to VCOUT* valid[2]		30	33	36	ns	BLT_STATE, LAEN, FC1=1, DUAL PATH=0
t124	D64 falling edge to A[7:0], D[7:0] valid[2]		23	24	27	ns	
t125	D64 rising edge to A[7:0], D[7:0] valid[2]		22	23	26	ns	BLT_STATE=1
t126	ABEN* falling edge to A[7:0], D[7:0] valid[2]		15	15	17	ns	BLT_STATE=1
t127	FC1 rising edge to LA[7:0], LD[7:0] valid[2]		18	19	21	ns	
t128	FC1 falling edge to LA[7:0], LD[7:0] valid[2]		20	21	23	ns	
t129	FC1 falling edge to LCOUT*[2]		25	26	29	ns	
t130	FC1 rising edge to LCOUT*[2]		21	22	24	ns	
t134	VCIN* set-up time to LADO rising edge[1]	8				ns	
t135	VCIN* hold time after LADO rising edge[1]	0				ns	

Notes:

1. All minimum times guaranteed by design, not tested.
2. Guaranteed, not tested.

Pin Definitions (Pin numbers refer to PQFP/CQFP package.)

Pin No.	Signal Name	Type	Description
1	GND	Power	Ground
2	LD7	Three-state I/O	Local data transceiver 7
3	LDS	Input	Register select bit
4	FC1	Input	Function code 1 control signal
5	STROBE*	Input	Comparator register load control signal
6	MWB*	Input	Module wants VMEbus control signal
7	LCOUT*	Output	Local address counters carry out signal
8	GND	Power	Ground
9	VCOMP*	Output	VMEbus address comparator out signal
10	VCOUT*	Output	VMEbus address counter carry out signal
11	LADO	Input	Latch address out control signal
12	LADI	Input	Latch address in control signal
13	LEDI	Input	Latch enable data in control signal
14	LEDO	Input	Latch enable data out control signal
15	A7	Three-state I/O	High drive address transceiver 7
16	GND	Power	Ground
17	V_{CC}	Power	V_{CC}
18	D7	Three-state I/O	High drive data transceiver 7
19	A6	Three-state I/O	High drive address transceiver 6
20	D6	Three-state I/O	High drive data transceiver 6
21	A5	Three-state I/O	High drive address transceiver 5
22	D5	Three-state I/O	High drive data transceiver 5
23	A4	Three-state I/O	High drive address transceiver 4
24	D4	Three-state I/O	High drive data transceiver 4
25	GND	Power	Ground
26	A3	Three-state I/O	High drive address transceiver 3
27	D3	Three-state I/O	High drive data transceiver 3
28	A2	Three-state I/O	High drive address transceiver 2
29	D2	Three-state I/O	High drive data transceiver 2
30	A1	Three-state I/O	High drive address transceiver 1
31	D1	Three-state I/O	High drive data transceiver 1
32	V_{CC}	Power	V_{CC}
33	GND	Power	Ground
34	A0	Three-state I/O	High drive address transceiver 0
35	D0	Three-state I/O	High drive data transceiver 0

Pin No.	Signal Name	Type	Description
36	ABEN*	Input	High drive address bus enable signal
37	DENO*	Input	High drive data bus enable signal
38	D64	Input	D64 mode enable control signal
39	BLT*	Input	Block transfer control signal
40	V_{CC}	Power	V_{CC}
41	VCIN*	Input	VMEbus address counter count enable signal
42	LCIN*	Input	Local address counter count enable signal
43	LAEN	Input	Local address enable control signal
44	DENIN1*	Input	Data enable in 1 control signal
45	DENIN*	Input	Data enable in control signal
46	LA0	Three-state I/O	Local address transceiver 0
47	LD0	Three-state I/O	Local data transceiver 0
48	GND	Power	Ground
49	V_{CC}	Power	V_{CC}
50	LA1	Three-state I/O	Local address transceiver 1
51	LD1	Three-state I/O	Local data transceiver 1
52	LA2	Three-state I/O	Local address transceiver 2
53	LD2	Three-state I/O	Local data transceiver 2
54	LA3	Three-state I/O	Local address transceiver 3
55	LD3	Three-state I/O	Local data transceiver 3
56	GND	Power	Ground
57	LA4	Three-state I/O	Local address transceiver 4
58	LD4	Three-state I/O	Local data transceiver 4
59	LA5	Three-state I/O	Local address transceiver 5
60	LD5	Three-state I/O	Local data transceiver 5
61	LA6	Three-state I/O	Local address transceiver 6
62	LD6	Three-state I/O	Local data transceiver 6
63	LA7	Three-state I/O	Local address transceiver 7
64	V_{CC}	Power	V_{CC}

Pin Configuration

Top View
PQFP/CQFP

Left pins		Right pins
GND	1	48 GND
LD7	2	47 LD0
LDS	3	46 LA0
FC1	4	45 DENIN
STROBE	5	44 DENIN1
MWB	6	43 LAEN
LCOUT	7	42 LCIN
GND	8	41 VCIN
VCOMP	9	40 VCC
VCOUT	10	39 BLT
LADO	11	38 D64
LADI	12	37 DENO
LEDI	13	36 ABEN
LEDO	14	35 D0
A7	15	34 A0
GND	16	33 GND

Top pins (64–49): VCC, LA7, LD6, LA6, LD5, LA5, LD4, LA4, GND, LD3, LA3, LD2, LA2, LD1, LA1, VCC

Bottom pins (17–32): VCC, D7, A6, D6, A5, D5, A4, D4, GND, A3, D3, A2, D2, A1, D1, VCC
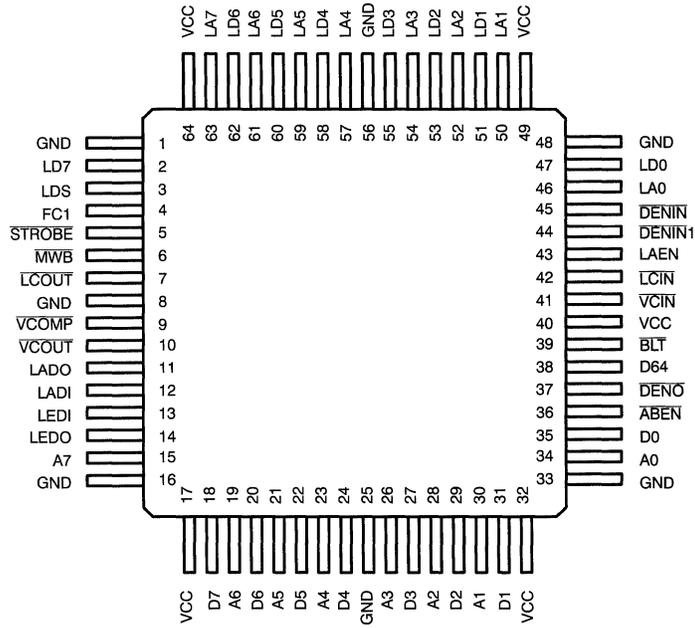
VIC64/7C964-2627

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Package Diagrams

64-Pin Thin Quad Flat Pack A64
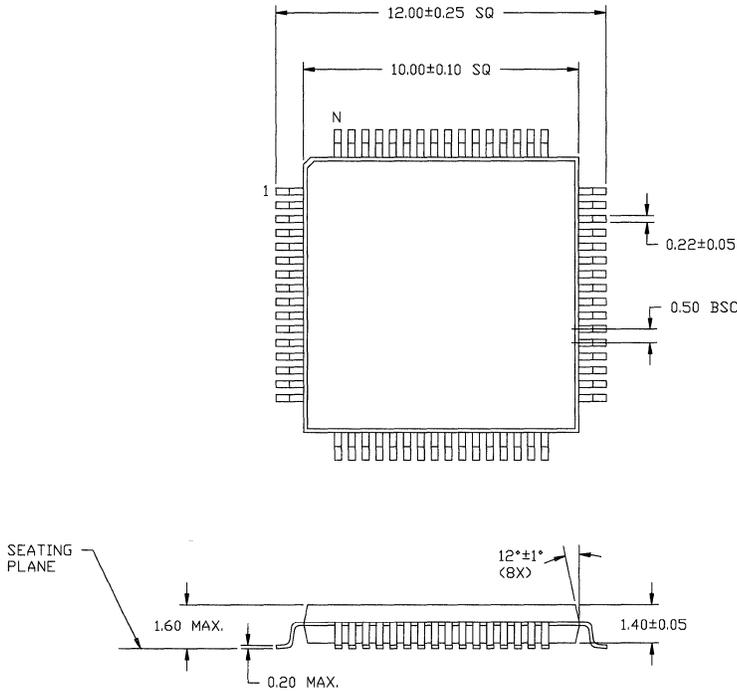
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.
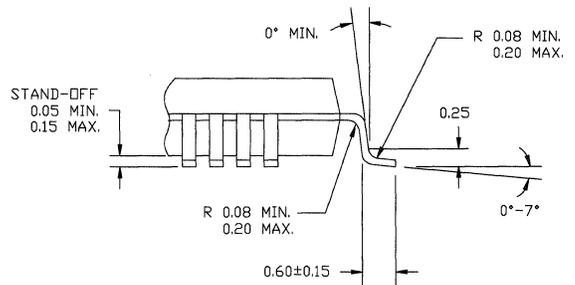
68-Pin Grid Array (Cavity Up) G68
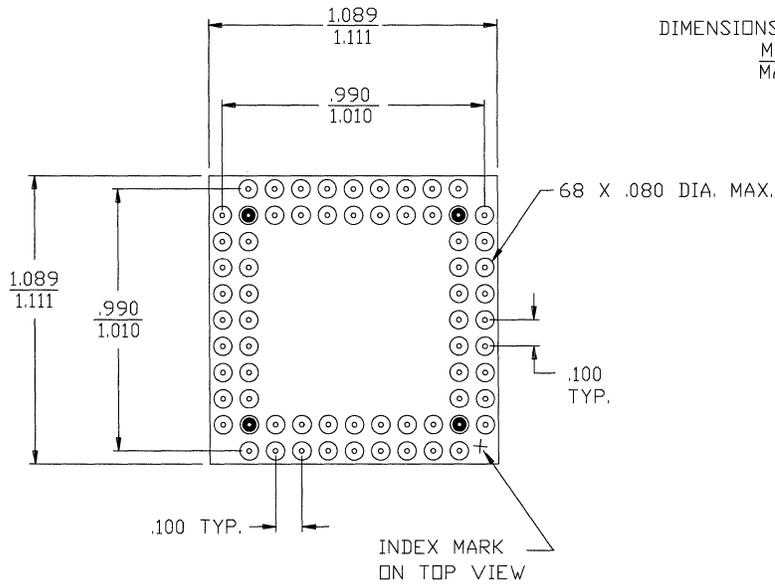
DIMENSIONS IN INCHES
$\frac{MIN.}{MAX.}$
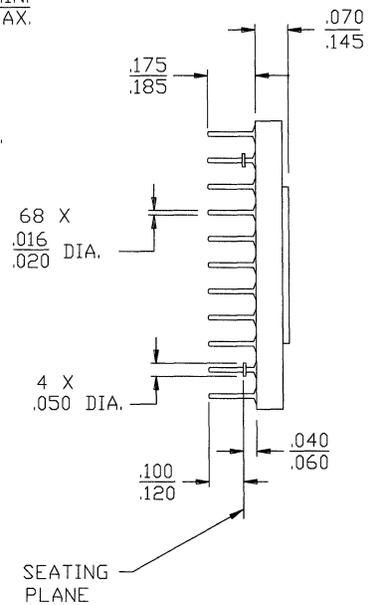
Package Diagrams (continued)

64-Lead Plastic Thin Quad Flatpack N65
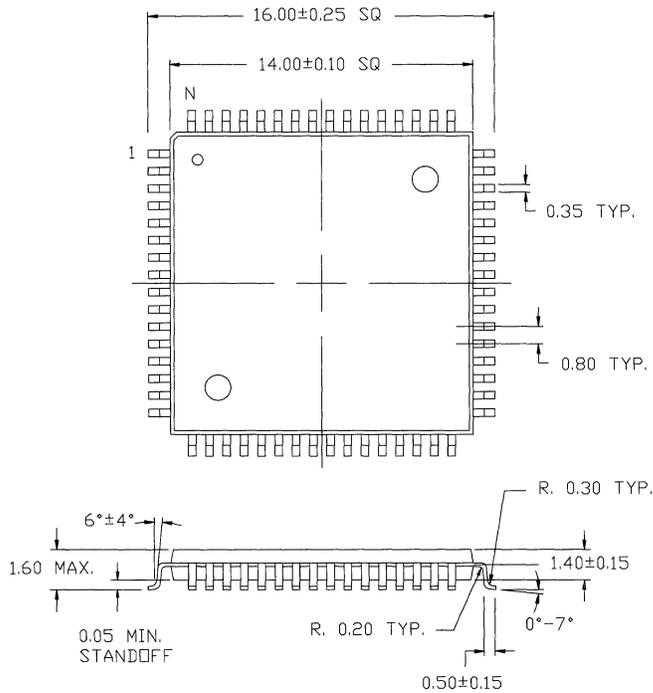
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

64-Lead Ceramic Quad Flatpack (Cavity Up) U65
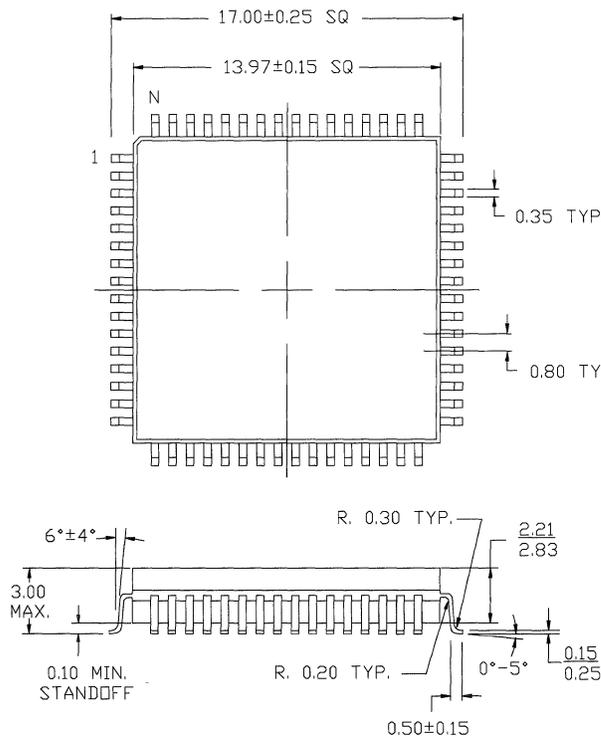
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.
DIMENSION   MIN.
            MAX.

Addendum to VIC068A/VAC068A User's Guide

VIC068A AC Performance Specification *(Chapter 14)*

Clock Input

Num.	Characteristic	Min.	Max.
	Frequency of Operation (MHz)	1	64
1	Cycle Time (ns)	15.6	1000
2, 3	Clock Pulse Width (Measured from 1.5V to 1.5V)	Note 1	Note 1
4, 5	Rise and Fall Time (ns)	—	5
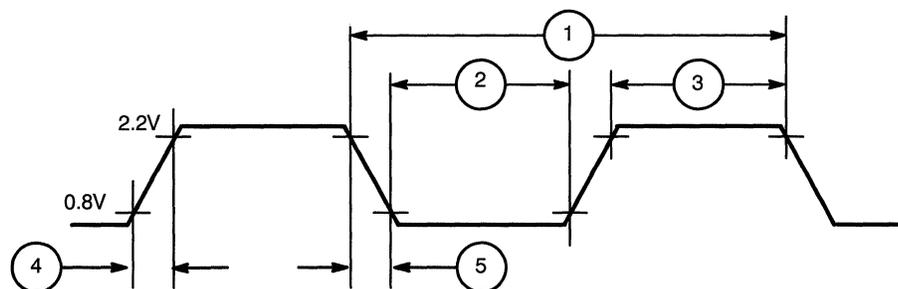
Note:
1. A 60/40 to 40/60 duty cycle must be maintained.

AC Specifications[2, 3]

			Commercial		Industrial		Military	
Operation		Notes	Min.	Max.	Min.	Max.	Min.	Max.
ARBITRATION								
A1	BRi*[0] to BBSY*[H]	4, 5	2½T+5	3T+25	2½T+4	3T+26	2½T+4	3T+31½
A2	BRi*[0] to BBSY*[L]	5, 6	3T+8	3½T+28	3T+7	3½T+34	3T+7	3½T+35
A3	BRi*[0] to BGiOUT*[L]	5, 6	3T+4	4T+25	3T+4	4T+26	3T+3	4T+28
A4	BRi*[0] to BCLR*[L]	5	2	16	2	16	2	19
A5	BGiIN*[0] to BGiOUT*[L]	5	2	18	2	18	2	20
A6	BGiIN*[0] to BBSY*[L]	7	4	23	4	24	3	25
A7	BGiIN*[0] to BRi*[H]	5, 7	5	3T+26	4	3T+27	4	3T+31
A8	BGiIN*[1] to BGiOUT*[H]	5	3	20	2	21	2	23
A9	BBSY*[0] to BGiOUT[H]	5, 6	4	21	3	22	3	24

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
A10	BBSY*[1] to BGiOUT*[L]	5	3T+5	4T+25	3T+4	4T+26	3T+3	4T+29
A11	BBSY*[1] to BCLR*[H]	5	1T+4	2T+24	1T+4	2T+25	1T+3	2T+27
MASTER ACCESSES								
B1	BGiIN*[0] to DENO*[L]	5, 7, 8	8	3T+36	7	3T+37	6	3T+42
B2	BGiIN*[0] to LADO[H]	5, 7	14	3T+59	13	3T+61	12	3T+67
B3	BGiIN*[0] to AS*[L]	5, 7	3T+5	6T+28	3T+5	6T+29	3T+4	6T+31
B4	BGiIN*[0] to A[7:1] Valid	5, 7	6	3T+31	6	3T+32	5	3T+37
B5	BGiIN*[0] to LWORD*[H/L]	5, 7	6	3T+31	6	3T+32	5	3T+37
B6	BGiIN*[0] to WRITE*[H/L]	5, 7	6	3T+31	6	3T+32	5	3T+37
B7	BGiIN*[0] to ABEN*[L]	5, 7	7	3T+34	6	3T+36	6	3T+38
B8	PAS*[0] & MWB*[0] to BRi*[L]	5	4	22	3	22	3	24
B9	PAS*[0] & MWB*[0] to ISOBE*[L]	5	4	22	3	23	3	25
B10	PAS*[0] & MWB*[0] to LADO[H]	5	15	60	13	62	12	68
B11	PAS*[0] & MWB*[0] to BBSY*[L]	5, 9	7	32	5	33	5	36
B12	PAS*[0] & MWB*[0] to ABEN*[L]	5, 9	1½T+8	2½T+36	1½T+7	2½T+37	1½T+6	2½T+41
B13	PAS*[0] & MWB*[0] to A[7:1]	5, 9	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B14	PAS*[0] & MWB*[0] to LWORD*[H/L]	5, 9	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B15	PAS*[0] & MWB*[0] to WRITE*[H/L]	5, 9	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B16	PAS*[0] & MWB*[0] & DS*[0] to DS1/0*[L]	5, 9	4½T+10	5½T+46	4½T+9	5½T+47	4½T+9	5½T+57
B17	PAS*[0] & MWB*[0] to SWDEN*[L]	5	1½T+7	2½T+36		12	3	14
B18	PAS*[0] & MWB*[0] to LWDENIN*[L]	5, 10	3	20	3	20	2	22
B19	PAS*[0] & MWB*[0] to UWDENIN*[L]	5, 10	3	20	3	21	3	23
B20	PAS*[0] & MWB*[0] & DS*[0] to AS*[L]	5, 9	4½T+6	5½T+28	4½T+5	5½T+29	4½T+5	5½T+32
B21	R/W*[0] to DDIR*[H]	5, 8	4	22	3	23	2	25
B22	R/W*[1] to DDIR*[L]	5, 8	2	14	1	14	1	15
B23	D[7:0] to LD[7:0] Valid	5, 10	3	18	2	18	2	22
B24	DTACK*[0] to LEDI[H]	5, 10	3T+6	4T+28	3T+4	4T+29	3T+4	4T+32
B25	DTACK*[0] to DSACKi*[L]	5	4	30	3	31	3	36

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
B26	PAS*[1] & DS*[1] to DSACKi*[H]	5	2	19	2	20	2	27
B27	PAS*[1] to AS*[H]	5	6	30	5	31	5	41
B28	DS*[1] to ISOBE*[H]	5	4	23	3	24	3	26
B29	DS*[1] to SWDEN*[H]	5	4	10	3	10	2	13
B30	DS*[1] to UWDENIN*[H]	5, 10	3	19	3	20	2	22
B31	DS*[1] to LWDENIN*[H]	5, 10	3	19	3	20	2	22
B32	DS*[1] to LD[7:0] Invalid	5, 10	3	20	2	22	2	28
B33	DS*[1] to LD[7:0] Hi-Z	5, 10	3	20	2	22	2	28
B34	DS*[0] to DSACKi*[L]	5, 11	6	T+30	5	T+32	5	T+35
B35	DS*[0] to LADO[H]	5, 11	8	38	7	39	7	43
B36	DS*[0] to LEDO[H]	5, 11	4	T+16	3	T+18	3	T+20
LOCAL BUS TIMING (VIC068A AS LOCAL BUS MASTER)								
C1	LBG*[0] to PAS*[L]	5	5T+6	6T+31	5T+5	6T+33	5T+5	6T+44
C2	LBG*[0] to LA[7:0] Valid	5	3T+8	4T+36	3T+7	4T+37	3T+6	4T+46
C3	LBG*[0] to SIZ[1:0] Valid	5	1T+3	2T+20	1T+3	2T+21	1T+2	2T+28
C4	LBG*[0] to FC[2:1] Valid	5	1T+3	2T+20	1T+3	2T+21	1T+2	2T+27
C5	LBG*[0] to LD[7:0] Driven	8	3T+8	4T+38	3T+7	4T+39	3T+7	4T+48
C6	LBG*[0] to LAEN[H]	5	3T+10	4T+43	3T+9	4T+44	3T+8	4T+48
C7	LBG*[0] to ISOBE*[L]	5	3T+8	4T+37	3T+7	4T+39	3T+7	4T+42
C8	LBG*[0] to SWDEN*[L]	5	3T+9	4T+39	3T+8	4T+41	3T+7	4T+45
C9	LBG*[0] to DDIR*[H]	5, 8	3T+8	4T+37	3T+7	4T+39	3T+7	4T+42
C10	LBG*[0] to UWDENIN*[L]	5, 8	3T+7	4T+36	3T+6	4T+38	3T+6	4T+42
C11	LBG*[0] to LWDENIN*[L]	5, 8	3T+7	4T+32	3T+6	4T+35	3T+5	4T+38
C12	LBG*[0] & DS1/0*[0] & WRITE[0] to R/W*[L]	5, 8	3T+8	4T+38	3T+7	4T+40	3T+7	4T+47
C13	LBG*[0] & DS1/0*[0] to DS*[L]	5	5T+8	6T+39	5T+7	6T+42	5T+7	6T+56
C14	PAS*[0] to DS*[L]	5, 12	0	12	0	15	0	15
C15	LBR*[H] to LBG*[1]	5, 13		T		T		T
SLAVE ACCESSES								
D1	SLSELi*[0] & AS*[0] to LBR*[L]	5	7	35	6	36	6	40
D2	SLSELi*[0] & AS*[0] & DS1/0*[1] to LADI[H]	5	5	25	4	26	4	29
D3	LD[7:0] to D[7:0]	5, 10	2	16	2	16	2	18
D4	DSACKI*[0] to LEDO*[H]	5, 10	SAT+8	SAT+½T+35	SAT+7	SAT+½T+36	SAT+6	SAT+½T+39

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
D5	DSACKi*[0] to DTACK*[L]	5	SAT+10	SAT+½T+45	SAT+9	SAT+½T+47	SAT+9	SAT+½T+53
D6	DS1/0*[0] to DTACK*[L]	5, 14	2T+5	3½T+28	2T+5	3½T+29	2T+4	3½T+33
D7	DS1/0*[0] to LEDI[H]	5, 14	9	41	8	43	8	47
D8	AS*[1] to LA[7:0], R/W* Invalid	5	5	38	4	42	4	55
D9	AS*[1] to LA[7:0], R/W* Hi−Z	5	5	38	4	42	4	55
D10	AS*[1] to FC2/1, Invalid	5	10	42	8	44	8	56
D11	AS*[1] & DSACKi*[1] to FC2/1, Hi-Z	5	10	42	8	44	8	56
D12	AS*[1] to SIZ1/0, Invalid	5	7	32	6	34	6	37
D13	AS*[1] & DSACKi*[1] to SIZ1/0, Hi-Z	5	3	1T+17	2	1T+19	2	1T+24
D14	AS*[1] to ISOBE*[H]	5	6	30	5	31	5	34
D15	AS*[1] to SWDEN*[H]	5	4	24	4	25	3	27
D16	AS*[1] to UWDENIN*[H]	5, 8	5	27	4	28	4	30
D17	AS*[1] to LWDENIN*[H]	5, 8	5	27	4	28	4	30
D18	AS*[1] & DSACKi*[1] to LBR*[H]	5	5	26	4	27	4	30
D19	AS*[1] to LAEN[L]	5	9	40	8	43	7	56
D20	DS*1/0[1] to LD[7:0] Invalid	5, 8	2	27	2	30	2	39
D21	DS*1/0[1] to LD[7:0] Hi-Z	5, 8	2	27	2	30	2	39
D22	DSACKi*[0] to PAS*[H]	5	SAT+10	SAT+½T+44	SAT+9	SAT+½T+46	SAT+8	SAT+½T+56
D23	DSACKi*[0] to DS*[H]	5	SAT+9	SAT+½T+40	SAT+8	SAT+½T+41	SAT+7	SAT+½T+48
D24	DSi*[1] to DTACK*[H]	5	3	27	3	28	3	35
INTERRUPT								
E1	IACKIN*[0] to IACKOUT*[L]	5	2	16	2	17	2	18
E2	IACKIN*[1] to IACKOUT*[H]	5	3	18	2	19	2	20
E3	FCIACK*[0] & PAS*[0] to BRi*[L]	5	5T+9	6T+41	5T+8	6T+42	5T+7	6T+48
E4	FCIACK*[0] & PAS*[0] to IACK*[L]	5, 9	7½T+7	8½T+34	7½T+6	8½T+35	7½T+6	8½T+39
E5	FCIACK*[0] & PAS*[0] to LD[7:0] Driven	5, 15	5T+12	6T+50	5T+10	6T+52	5T+10	6T+57
E6	FCIACK*[0] & PAS*[0] to LD[7:0] valid	5, 16	9T+5	10T+29	9T+5	10T+33	9T+4	10T+37

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
E7	FCIACK*[0] & PAS*[0] to LIACK0*[L]	5, 17	5T+7	6T+32	5T+6	6T+33	5T+5	6T+36
E8	IRQi*[0] to IPL*	5	5	33	5	34	4	37
E9	BGiIN*[0] to BBSY*[L]	5	7	32	5	33	5	36
E10	BGiIN*[0] to AS*[L]	5	3T+5	4T+27	3T+4	4T+28	3T+4	4T+31
E11	BGiIN*[0] to DS1/0*[L]	5	3T+10	4T+45	3T+9	4T+46	3T+8	4T+55
E12	BGiIN*[0] to IACK*[L]	5, 16	39	7	40	7	44	
E13	PAS*[0] to ISOBE*[L]	5	5T+9	6T+39	5T+7	6T+40	5T+7	6T+44
E14	PAS*[0] to SWDEN*[L]	5	5T+8	6T+37	5T+7	6T+38	5T+6	6T+42
E15	IPLi* to IPLi*	5, 12		10		12		12
MASTER BLOCK TRANSFER WITH LOCAL DMA (INITIATION CYCLE)								
F1	MWB*[0] & PAS*[0] & DS*[0] to BRi*[L]	5	T+7	2T+32	T+6	2T+33	T+5	2T+38
F2	BGiIN*[0] to LBR*[L]	5	4T+10	5T+42	4T+8	5T+44	4T+8	5T+50
F3	MWB*[0] & PAS*[0] & DS*[0] to LBR*[L]	5, 9	5T+10	6T+42	5T+8	6T+44	5T+8	6T+50
F4	MWB*[0] & PAS*[0] & DS*[0] to LADO[H]	5	T+7	2T+35	T+6	2T+36	T+6	2T+39
F5	MWB*[0] & PAS*[0] & DS*[0] to BLT*[L]	5	T+6	2T+28	T+5	2T+29	T+4	2T+37
MASTER BLOCK TRANSFER WITH LOCAL DMA (WRITE)								
** First cycle **								
G1	DSACKi*[0] and DS*[0] to DS*[H]	5	MBAT0+9	MBAT0+½T+41	MBAT0+8	MBAT0+½T+43	MBAT0+7	MBAT0+½T+52
G2	DSACKi*[0] and DS*[L] to LEDO[H]	5	MBAT0+8	MBAT0+½T+36	MBAT0+7	MBAT0+½T+37	MBAT0+6	MBAT0+½T+40
G3	DSACKi*[0] and DS*[L] to LA[7:0] valid	5	MBAT0+T+11	MBAT0+1½T+32	MBAT0+T+9	MBAT0+1½T+36	MBAT0+T+9	MBAT0+1½T+40
G4	DSACKi*[0] and DS*[L] to DSi*[L]		MBAT0+3T+6	MBAT0+3½T+37	MBAT0+3T+5	MBAT0+3½T+39	MBAT0+3T+5	MBAT0+3½T+42
G5	DTACK*[0] to LEDO[L]	5	7	32	6	33	6	38
G6	DTACK*[0] to DSi*[H]		10	49	9	51	9	56
G7	DTACK*[0] to A[7:0] Valid	5	11	46	10	48	9	64
G8	DS*[H] to DS*[L]	5	DST+1½T−13	DST+1½T−6	DST+1½T−14	DST−1½T−5	DST+1½T−15	DST+1½T−4
** Second and subsequent cycles **								
G9	DSACKi*[0] and DS*[L] to DS*[H]	5	MBAT1+9	MBAT1+½T+41	MBAT1+8	MBAT1+½T+43	MBAT1+7	MBAT1+½T+52
G10	DSACKi*[0] and DS*[L] to LEDO[H]	5	MBAT1+8	MBAT1+½T+36	MBAT1+7	MBAT1+½T+37	MBAT1+6	MBAT1+½T+40
G11	DSACKi*[0] and DS*[L] to LA[7:0] Valid	5	MBAT1+T+11	MBAT1+1½T+32	MBAT1+T+9	MBAT1+1½T+36	MBAT1+T+9	MBAT1+1½T+40

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
G12	DSACKi*[0] and DS*[L] to DSi*[L]	5	MBAT1+3T+6	MBAT1+3½T+29	MBAT1+3T+5	MBAT1+3½T+30	MBAT1+3T+5	MBAT1+3½T+38
G13	DTACK*[0] to LEDO[L]	5	7	32	6	33	6	38
G14	DTACK*[0] to DSi*[H]	5	10	45	9	46	9	59
G15	DTACK*[0] to A[7:0] Valid	5	11	46	10	48	9	64
G16	DTACK*[0] to DS*[H]	5,18	T + 15	1½T + 45	1½T + 14	1½T + 46	T + 13	1½T + 47
G17	LEDO[L] to LEDO[H]	5,18	T + 11	1½T + 25	1½T + 10	1½T + 26	T + 9	1½T + 27
MASTER BLOCK TRANSFER WITH LOCAL DMA (READ)								
** First Cycle **								
H1	DTACK*[0] to LEDI[H]		2T+6	3T+23	2T+4	3T+25	2T+4	3T+27
H2	DTACK*[0] to DSi*[H]		2T+9	3T+28	2T+8	3T+30	2T+7	3T+32
H3	DTACK*[0] to A[7:0] Valid	5	1½T+10	2½T+44	1½T+9	2½T+45	1½T+8	2½T+53
H4	DTACK*[0] to DS*[L]	5	1½T+8	2½T+38	1½T+7	2½T+40	1½T+7	2½T+47
H5	DSACKi*[0] and DS*[L] to DS*[H]		MBAT0+9	MBAT0+½T+38	MBAT0+8	MBAT0+½T+40	MBAT0+7	MBAT0+½T+45
H6	DSACKi*[0] and DS*[L] to LEDI[L]		MBAT0+9	MBAT0+½T+48	MBAT0+8	MBAT0+½T+50	MBAT0+7	MBAT0+½T+55
H7	DSACKi*[0] and DS*[L] to LA[7:0] Valid	5	MBAT0+T+11	MBAT0+1½T+30	MBAT0+T+9	MBAT0+1½T+32	MBAT0+T+9	MBAT0+1½T+35
H8	DSACKi*[0] and DS*[L] to DSi*[L]	5	MBAT0+11	MBAT0+½T+74	MBAT0+10	MBAT0+½T+76	MBAT0+10	MBAT0+½T+83
** Second and subsequent cycles **								
H9	DTACK*[0] to LEDI[H]	5	2T+6	3T+23	2T+4	3T+25	2T+4	3T+27
H10	DTACK*[0] to DSi*[H]	5	2T+9	3T+28	2T+8	3T+30	2T+7	3T+32
H11	DTACK*[0] to A[7:0] Valid	5	10	44	9	45	8	53
H12	DTACK*[0] to DS*[L]	5	8	38	7	40	7	47
H13	DSACKi*[0] and DS*[0] to DS*[H]	5	MBAT1+9	MBAT1+½T+36	MBAT1+8	MBAT1+½T+38	MBAT1+7	MBAT1+½T+45
H14	DSACKi*[0] and DS*[0] to LEDI[L]	5	MBAT1+9	MBAT1+½T+44	MBAT1+8	MBAT1+½T+46	MBAT1+7	MBAT1+½T+55
H15	DSACKi*[0] and DS*[0] to LA[7:0] Valid	5	MBAT1+T+11	MBAT1+1½T+31	MBAT1+T+9	MBAT1+1½T+33	MBAT1+T+9	MBAT1+1½T+35
H16	DSACKi*[0] and DS*[0] to DSi*[L]	5	MBAT1+11	MBAT1+½T+72	MBAT1+10	MBAT1+½T+76	MBAT1+10	MBAT1+½T+83
MASTER BLOCK TRANSFER WITH LOCAL DMA (BOUNDARY CROSSING)								
J1	DS*[L] to BLT*[H]		2	30	2	32	2	35
J2	DS*[H] to BLT[L]		2	17	2	19	2	21
J3	DSi*[L] to LEDO[H/L]		2	21	2	23	2	25
J4	DSi*[H] to LADO*[L/H]	5	1	16	2	18	2	20
SLAVE BLOCK TRANSFER (WRITE)								

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
** First Cycle **								
See: Local Bus Timing (VIC068A as local bus master)								
** Second and subsequent cycles **								
K1	DSi*[0] to LEDI*[H]	5	4	20	4	22	4	24
K2	DSi*[0] to DS*[L]		6	35	5	36	5	39
K3	DSACKi*[0] and DS*[L] to DS*[H]	5	SBAT+9	SBAT+½T+41	SBAT+8	SBAT+½T+42	SBAT+7	SBAT+½T+52
K4	DSACKi*[0] and DS*[L] to DTACK*[L]	5	SBAT+12	SBAT+½T+51	SBAT+11	SBAT+½T+53	SBAT+10	SBAT+½T+67
K5	DSACKi*[0] and DS*[L] to ISOBE*[H]	5	SBAT+13	SBAT+½T+54	SBAT+11	SBAT+½T+56	SBAT+11	SBAT+½T+62
K6	DSACKi*[0] and DS*[L] to SWDEN*[H]	5	SBAT+12	SBAT+½T+50	SBAT+10	SBAT+½T+52	SBAT+10	SBAT+½T+61
K7	DSACKi*[0] and DS*[L] to LA[7:0] Valid	5	SBAT+T+10	SBAT+1½T+34	SBAT+T+8	SBAT+1½T+36	SBAT+T+8	SBAT+1½T+40
K8	DSACKi*[0] and DS*[L] to LEDI*[L]	5	SBAT+8	SBAT+½T+46	SBAT+7	SBAT+½T+48	SBAT+6	SBAT+½T+53
K9	DS1/0*[1] to DTACK*[H]	5	5	27	5	28	4	35
SLAVE BLOCK TRANSFER (READ)								
** First Cycle **								
See: Local Bus Timing (VIC068A as local bus master)								
** Second and subsequent cycles **								
L1	DS1/0*[1] to LEDO*[L]		4	23	3	24	3	30
L2	DS*[H] to DS*[L]	5	DST+1½T−13	DST+1½T−2	DST+1½T−14	DST+1½T−3	DST+1½T−15	DST+1½T−4
L3	DS1/0*[0] to DENO*[L]	5	3	20	3	22	3	24
L4	DSACKi*[0] and DS*[0] to LEDO*[H]	5	SBAT+8	SBAT+½T+36	SBAT+7	SBAT+½T+37	SBAT+6	SBAT+½T+41
L5	DSACKi*[0] and DS*[0] to DS*[H]	5	SBAT+9	SBAT+½T+41	SBAT+8	SBAT+½T+43	SBAT+7	SBAT+½T+52
L6	DSACKi*[0] and DS*[0] to DTACK*[L]		SBAT+11	SBAT+½T+47	SBAT+9	SBAT+½T+48	SBAT+9	SBAT+½T+53
L7	DSACKi*[0] and DS*[0] to LA[7:0] Valid	5	SBAT+T+9	SBAT+1½T+34	SBAT+T+8	SBAT+1½T+36	SBAT+T+8	SBAT+½T+40
L8	DS1/0*[1] to DENO*[H]	5	3	19	3	20	2	22
L9	DS1/0*[1] to DTACK*[H]	5	3	20	3	21	3	24
L10	LEDO[L] to LEDO[H]	5,19	T + 11	1½ + 25	T + 10	1½ + 26	1½ + 9	1½ + 27
L11	DTACK*[0] to DS*[H]	5,19	T + 15	1½ + 45	1½ + 14	1½ + 46	1½ + 13	1½ + 47
REGISTER ACCESS								
M1	PAS*[0] & DS*[0] & CS*[0] to DSACKi[L]	5	4T+5	5T+34	4T+5	5T+35	4T+4	5T+38
M2	PAS*[0] & DS*[0] & CS*[0] to LD[7:0] Valid	5, 10	3T+5	4T+28	3T+5	4T+29	3T+4	4T+37

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
M3	AS*[0] & ICFSEL*[0] to DTACK*[L]	5	4T+6	4T+30	4T+5	4T+31	4T+5	4T+34
RESET								
N1	LBG*[0] to HALT*[L], RESET*[L]	5	8	36	7	37	6	48
N2	IRESET*[0] to LBR*[L]	5	6	29	5	30	5	33
N3	IRESET*[0] to IPL0[Z]	5	2	16	2	16	2	20
SET-UP TIMES								
P1	LA, ASIZ[1:0] Valid to PAS*[0]	5	−2T		−2T		−2T	
P2	SIZ[1:0], WORD*, FC[2:1] Valid to PAS*[0]	5	−2T		−2T		−2T	
P3	LD[7:0] Valid to DS*[0]	5	0		0		0	
HOLD TIMES								
Q1	PAS*[1] to LA, ASIZ[1:0] Invalid	5	0		0		0	
Q2	PAS*[1] to SIZ[1:0], WORD*, FC[2:1] Invalid	5	0		0		0	
Q3	DS*[1] to LD[7:0] Invalid	5	0		0		0	
Q4	DS1/0*[1] to DTACK*[H]	5	0		0		0	

Notes:

2. T = CLK64M clock period
   SAT = Slave Access Timing
   MBAT0 = Master Block Transfer Timing 0
   MBAT1 = Master Block Transfer Timing 1
   SBAT = Slave Block Transfer Timing
   DST = Data Strobe Timing

3. All minimum times are guaranteed, not tested.

4. ROR mode.

5. Timing specified but not tested.

6. While VMEbus system controller.

7. Synchronous delay depends on speed in which BGiIN is returned.
   If BGiIN is returned in zero time after request, synchronous delay will be maximum.

8. Write operation only.

9. While VMEbus master.

10. Read operation only.

11. Master write post only.

12. Skew.

13. Input requirement.

14. Slave write post only.

15. VMEbus interrupt only.

16. Local interrupt (LICR[4] = 1) only.

17. Local interrupt (LICR[4] = 0) only.

18. "Slow" Slave.

19. "Slow" Master.
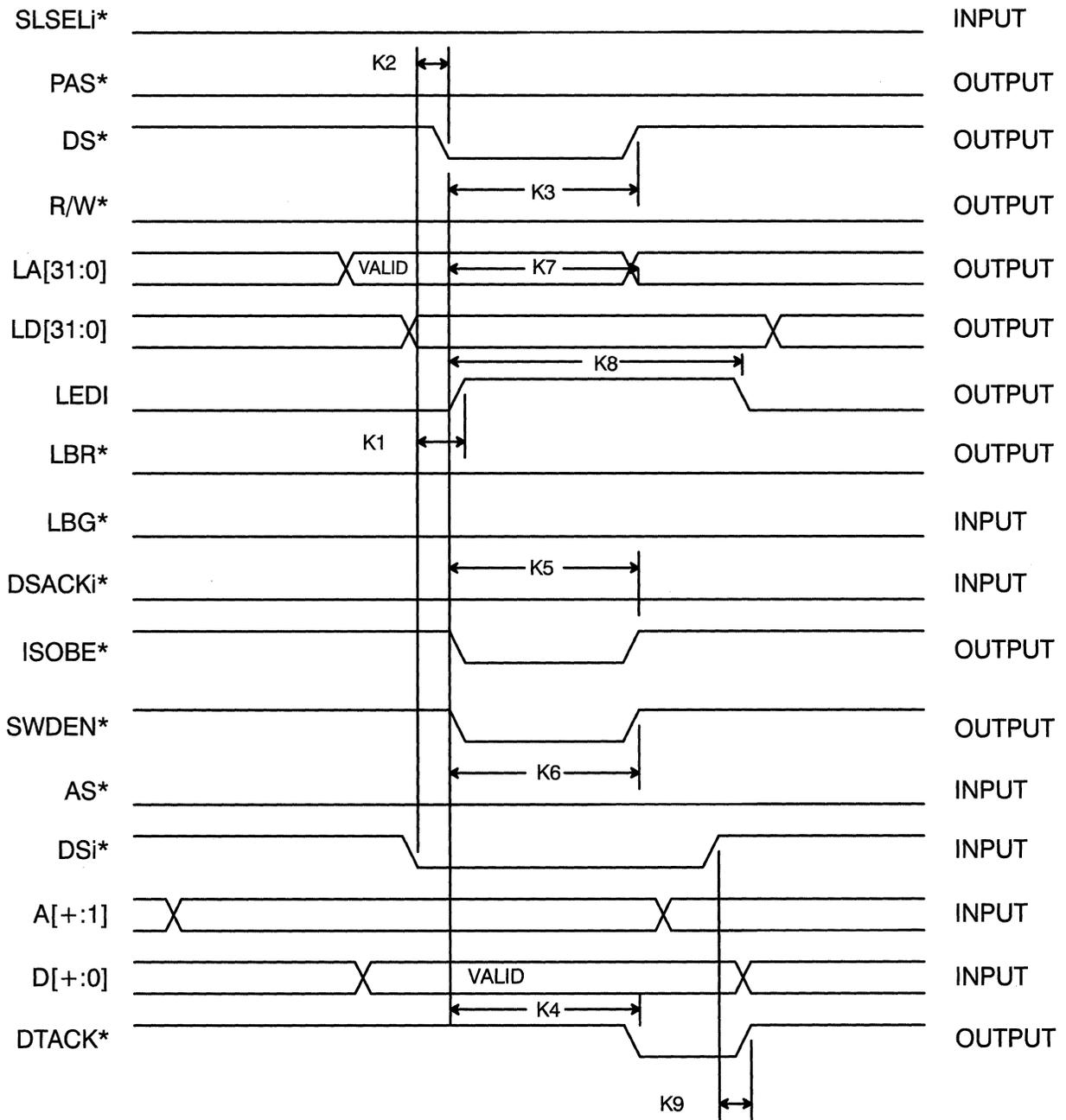
Figure 14−24. Slave Write BLT

VAC068A AC Performance Specification *(Chapter 22)*

Clock Input

Num.	Characteristic	Commercial		Military	
		Min.	Max.	Min.	Max.
	Frequency of Operation (MHz)	1	50	1	40
1	Cycle Time (ns)	20	1000	2.5	1000
2, 3	Clock Pulse Width (Measured from 1.5V to 1.5V)			11.25	
4, 5	Rise and Fall Time (ns)		5		5
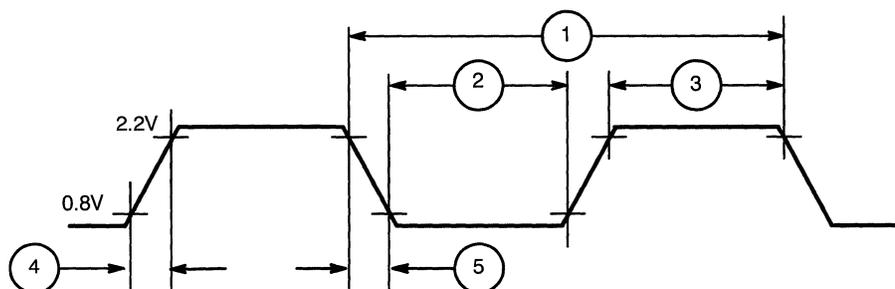
AC Specifications

Operation	Notes	Commercial		Industrial		Military	
		Min.	Max.	Min.	Max.	Min.	Max.
GLOBAL RESET							
1 RESET*[0] to WORD*[L]	1	5T		5T		5T	
2 WORD*[0] to RESET* High, WORD*[H]	1	10T		10T		10T	
REGISTER WRITE							
1 LA[31:8], FCi, R/W* Valid to PAS*[L] (Set-Up Time)	1	10		10		10	
2 LD[31:16] Valid to DSACKi*[L] (Set-Up Time)	1	5		5		5	
3 PAS*[0] to DSACKi*[L]		6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
4 PAS*[1] to DSACKi*[H]		5	29	4	30	4	33
5 PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
REGISTER READ							
1 LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
2	PAS*[0] to DSACKi*[L]		6	35 + 1T	5	36 + 1T	5	40 +1T
3	PAS*[0] to LD[31:16] Valid		9	51 + 1T	8	53 + 1T	7	58 +1T
4	PAS*[1] to DSACKi*[H]		5	17	4	17	5	18
5	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
6	PAS*[0] to LD[31:16] Invalid	2	6 + 3T	44 + 35T	5 + 3T	44 + 3.5T	5 + 3T	45 + 3.5T

LOCAL ACCESS VIA LOCAL BUS

	Operation	Notes	Min.	Max.	Min.	Max.	Min.	Max.
1	LA[31:8], FCi, R/W* to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to Chip Select[L]	3, 4	6	33	5	34	5	38
4	PAS*[0] to DSACKi*[L]	5	PI1 + 6	PI1+24+1T	PI1 + 5	PI1+25+1T	PI1 + 5	PI1+28+1T
5	PAS*[0] to IORD*/IOWR*[L]	6	PI3 + 6	PI3+47+1T	PI3 + 6	PI3+48+1T	PI3 + 5	PI3+53+1T
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to ASIZ1/0 WORD* Invalid		7	37	7	38	6	42
8	PAS*[1] to Chip Select*[H]	3	4	34	3	35	3	39
9	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18
10	PAS*[1] to IORD*[H] /IOWR*[H]	6	PI3 + 4	PI3+21+1T	PI3 + 3	PI3+22+1T	PI3 + 3	PI3+25+1T

LOCAL ACCESS VIA VMEbus

	Operation	Notes	Min.	Max.	Min.	Max.	Min.	Max.
1	PAS*[0] to ASIZ1/0, WORD Valid		7	33	6	34	6	37
2	PAS*[0] to Chip Select[L]	7	6	33	5	34	5	38
3	PAS*[0] to DSACKi*[L]	8	PI2 + 6	PI2+29+1T	PI2 + 5	PI2+30+1T	PI2 + 5	PI2+33+1T
4	PAS*[0] to IORD*[L], IOWR*[L]	6	PI3 + 6	PI3 + 47+1T	PI3 + 6	PI3+48+1T	PI3 + 5	PI3+53+1T
5	PAS*[1] to ASIZ1/0, WORD* Invalid		7	37	7	38	6	42
6	PAS*[1] to Chip Select[H]	6	4	34	3	35	3	39
7	PAS*[1] to DSACKi*[H]	9	5	17	4	17	4	18
8	PAS*[1] to IORD*[H], IOWR*[H]	6	PI3 + 4	PI3 +21+1T	PI3 + 3	PI3+22+1T	PI3 + 3	PI3+25+1T

VMEbus SLAVE/SLAVE BLOCK ACCESS

	Operation	Notes	Min.	Max.	Min.	Max.	Min.	Max.
1	AS*[0] to SLSELi*[L] or ICFSEL[L]		3	24	3	25	2	27
2	LAEN[1] to LA[31:8] Valid		4	24	3	25	3	27
3	AS*[1] to SLSELi*[H] or ICFSEL[L]		6	20	5	21	5	23

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
4	LAEN[0] to LA[31:0] Invalid		12	30	10	31	10	33
VMEbus MASTER ACCESS								
1	LA[31:8], FCi, R/W* to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to MWB*[L]		11	30	10	32	10	35
4	ABEN*[0] to A[31:8] Valid		3	17	2	18	2	20
5	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
6	PAS*[1] to ASIZ1/0, WORD* Invalid		7	37	7	38	6	42
7	PAS*[1] to MWB*[L]		3	31	2	32	2	36
8	ABEN*[1] to A[31:8] Invalid		2	10	1	10	1	11
MASTER BLOCK TRANSFER INITIATION CYCLE								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PAS*[0] to ASIZ1/0, WORD* Valid		7	33	6	34	6	37
3	PAS*[0] to DSACKi[L]		6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
4	PAS*[0] to MWB*[L]		11	30	10	32	10	35
5	PAS*[1] to ASIZ1/0, WORD* (Hold Time)		7	37	7	38	6	42
6	PAS*[1] to DSACKi*[H]		5	17	4	17	4	18
7	PAS*[1] to MWB*[H]		3	31	2	32	2	36
8	ABEN*[0] to A[31:8] Valid		3	17	2	18	2	20
9	LAEN[1], FCi Valid to LA[31:8] Valid		4	24	3	25	3	27
10	PAS*[0] to LDMACK*[1]		1	27	1	28	1	31
BOUNDARY CROSSING								
1	BLT*[1] to LA[31:8] Incremented		1	27	1	28	1	33
2	LADO[0] to A[31:8] Incremented		7	28	5	29	4	33
PIO OUTPUT								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	
2	LD[31:16] to PAS*[0] (Set-Up Time)	1	5		5		5	
3	PAS*[0] to PIO[13:0] Valid		4 + 1T	54 + 2T	3 + 1T	56 + 2T	3 + 1T	63 + 2T
4	PAS*[0] to DSACKi*[L]		6 + 1T	35 + 2T	5 + 1T	36 + 2T	5 + 1T	40 + 2T
5	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18

	Operation	Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to LD[31:16] Invalid		6	44	5	44	5	45
PIO INPUT								
1	LA[31:8], FCi, R/W* Valid to PAS*[0] (Set-Up Time)	1	10		10		10	
2	PIO[13:0] to PAS*[0] (Set-Up Time)	1	5		5		5	
3	PAS*[0] to DSACKi*[L]		6	35 + 1T	5	36 + 1T	5	40 + 1T
4	PAS*[0] to LD[31:16] Valid		9	51 +1T	8	53 + 1T	7	58 + 1T
5	PAS*[1] to DSACKi*[H]		4	16	4	17	4	18
6	PAS*[1] to LA[31:8], FCi, R/W* (Hold Time)	1	5		5		5	
7	PAS*[1] to LD[31:16] Invalid		6	44	5	44	5	45

Notes:

1. Guaranteed, but not tested.

2. Maximum time to LD[31:16] invalid is PAS[0] + 3.5T or PAS[1], whichever occurs first.

3. Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, VSBSEL*, FPUCS*, CS*, or IOSELi*.

4. The Decode Control register provides facilities to condition DRAMCS* or boundary decodes with the assertion of PAS*.

5. PI1 is the programmable interval for EPROMCS*, SHRCS*, and IOSELi* in the DSACKi* Control register.

6. PI3 is the programmable interval for IORD and IOWR in the Decode Control register.

7. Chip select can be any of DRAMCS*, EPROMCS*, SHRCS*, or VSBSEL*.

8. PI2 is the programmable interval for EPROMCS*, SHRCS*, DRAMCS*, or VSBSEL* in the Decode Control register.

9. SLSELi* redirection is enabled in the Decode Control register.

Errata for
VIC068A/VAC068A User's Guide

Chapter 2

Pages 1−6   Only the VMEbus output signals AS*, DS0*, DS1*, BCLR*, and SYSCLK are high drive-signals (64mA). Remaining output signals listed as high drive should be standard drive (48mA). Refer to section 24 for correct drive capabilities.

Page 1   The reference to 4 ms should be 6μ.

Page 6   The reference to the IRQ7* − IRQ0* signals should be IRQ7* − IRQ1*. There is no IRQ0* signal.

Page 6   The reference to LAEN* in the description for the LA(7:0) signals should be LAEN (active HIGH).

Page 15   The pin description for the RMC* pin is missing. It should be listed as follows:

RMC*
Input: Yes
Output: No
Drive: None

This is the Read-Modify-Write control signal. This signal may be used to control indivisible cycles on the VMEbus. Its operation is controlled with the interface configuration register, bits 5 − 7. RMC operations are described in section 5.6.

Figure 2.2   The OEBA* connection of the upper data '543 should be connected to the VIC signal UWDENIN*.

Chapter 6

Page 3   The *Standard Slave Access and Block Transfer with Local DMA* function codes are reversed on the FC table. The corrected table should be:

FC2	FC1	Description
0	0	Slave Block Transfer
0	1	Block Transfer with Local DMA
1	0	Standard Slave Access
1	1	DRAM Refresh

The correct table is also listed on page 2–10.

Chapter 9

Table 9–2   The reference to VICRi in Step 2 should be LICRi.

Chapter 10

Page 7   The 68 K assembler instruction,

         move.I(A0), (A1)

should be

         move.IA0, (A1)

Figure 10–2   The LE pin of the '373 should simply be connected to BLT*.

Chapter 13

Page 17   In the description for bit 7, the references to bits 1 and 2 should instead reference bits 5 and 6.

Page 21   The DMA complete bit (bit 0) is cleared at the completion of a local DMA operation automatically by the VIC068. It does not need to be manually cleared as specified.

Chapter 14

Page 3   The maximum for time C15 has been increased to 2T.

Page 5 — Only the minimum timings for reference G8 is applicable. Maximum timings will depend on acknowledge timing from the VMEbus slave.

Page 6 — The minimum parameters for items H1, H2, H3, and H4 should be 2T, not 1 1/2 T.

The maximum parameters for items H1, H2, H3, and H4 should be 3T, not 2 1/2 T.

The minimum parameters for items H9, H10, H11, and H12 should be prepended by a 2T.

The maximum parameters for items H9, H10, H11, and H12 should be prepended by a 3T.

Page 7 — Only the minimum timings for reference L2 is applicable. Maximum timings will depend on acknowledge timing from the VMEbus master.

Pages 11 – 12 — Item Q3 (LD to DS* hold time) is not applicable in these figures.

Page 13 — The state of the DDIR signal should be Low, not High as shown.

Page 14 — The state of the DDIR signal should be High, not Low as shown.

Pages 13 – 14 — The left leader from reference designator D24 should reference DSi*, not DSACKi*.

Page 16 — Reference designators D8 – D17 are not applicable for slave write posts.

Chapter 15

Table 15 – 2 — The QFP pin number for DS* should be 135, not 137 as specified.

The QFP pin number for LIRQ1* should be 9, not 40 as specified.

Table 15 – 2, 5 — The reference to ASIZ1* and ASIZ0* should be ASIZ1 and ASIZ0.

Chapter 19

Page 16 — The UART receive buffers are quad buffered, not quint buffered.

Figure 19 – 1 — The address for the IOSEL2* region should be FFF4 XXXX, not FFF1 XXXX as shown.

Chapter 20

Page 9   The designator ID(31:8) in item 4 should be LD(31:8).

Chapter 21

Page 5   Bits 19 − 22 are new bits for the VAC068A. They are not present on the VAC068F5.

Page 7   Bits 28 and 27 of the Decode Control Register enable/disable DSACKi* for all accesses, not just the slave accesses as described.

Page 15   Bit 31 fo the UART Channel A and B Mode Register should indicate that parity generation and checking is enabled when this bit is set, not diabled. Parity checking/generation is disabled when this bit is clear.

Page 16   The UART transmitter must be enabled (bit 24 os the UART Channel A and B Mode Register) before loading the UART Channel A and B Data Register.

Table 21−1   Address FFFD 02xx is the SLSEL0* Address Mask Register, not hte Base Address Register as specified.

                                Address FFFD 03xx is the SLSEL0* Base Address Register, not the Address Mask Register as specified.

Chapter 23

Page 7   Pin 116 should be labled as PIO7, not V_{DD}.

Chapter 24

Tables 24−2,
24−3 & 24−4 V_{OL} value is a maximum, not minimum.
                               V_{IH} value is a minimum, not a maximum.

Page 4 I_{CC} (Max.) for the VIC068 and the VAC068 is 150 mA for all temperature ranges.

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