DALLAS SEMICONDUCTOR

1992-1993 PRODUCT DATA BOOK

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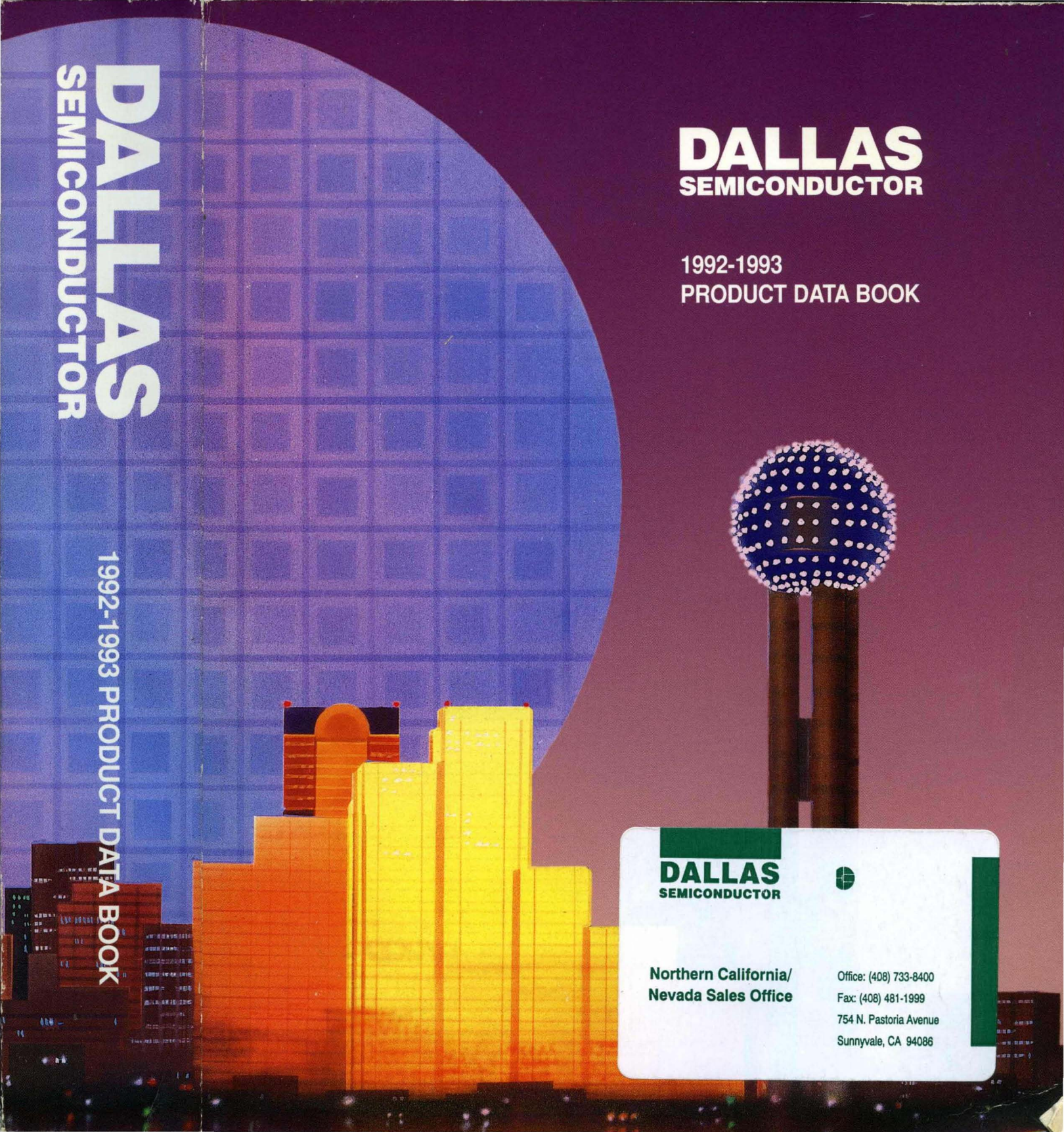

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DALLAS
SEMICONDUCTOR

1992-1993
PRODUCT DATA BOOK

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1991/1992
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General Information

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DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS0065	SOFTWARE	N/A	DS0065	
DS1000	14–Pin DIP	–40 to +85	DS1000–xxx	xxx = 025 to 500ns
	14–Pin DIP Sheared NC	–40 to +85	DS1000K–xxx	xxx = 025 to 500ns
	8–Pin DIP	–40 to +85	DS1000M–xxx	xxx = 025 to 500ns
	14–Pin GULLWING	–40 to +85	DS1000G–xxx	xxx = 025 to 500ns
	8–Pin GULLWING	–40 to +85	DS1000H–xxx	xxx = 025 to 500ns
	16–Pin SOIC	–40 to +85	DS1000S–xxx	xxx = 025 to 500ns
	8–Pin SOIC	–40 to +85	DS1000Z–xxx	xxx = 025 to 500ns
DS1003	8-Pin DIP	–40 to +85	DS1003M–16	
	8–Pin DIP	–40 to +85	DS1003M–20	
	8–Pin DIP	–40 to +85	DS1003M–25	
	8–Pin DIP	–40 to +85	DS1003M–33	
	8–Pin DIP	–40 to +85	DS1003M–40	
	8–Pin GULLWING	–40 to +85	DS1003H–16	
	8–Pin GULLWING	–40 to +85	DS1003H–20	
	8–Pin GULLWING	–40 to +85	DS1003H–25	
	8–Pin GULLWING	–40 to +85	DS1003H–33	
	8–Pin GULLWING	–40 to +85	DS1003H–40	
	14–Pin DIP	–40 to +85	DS1003–16	
	14–Pin DIP	–40 to +85	DS1003–20	
	14–Pin DIP	–40 to +85	DS1003–25	
	14–Pin DIP	–40 to +85	DS1003–33	
	14–Pin DIP	–40 to +85	DS1003–40	
	14–Pin GULLWING	–40 ot +85	DS1003G–16	
	14–Pin GULLWING	–40 to +85	DS1003G–20	
	14–Pin GULLWING	–40 to +85	DS1003G–25	
	14–Pin GULLWING	–40 to +85	DS1003G–33	
	14–Pin GULLWING	–40 to +85	DS1003G–40	
DS1005	14–Pin DIP	–40 to +85	DS1005–xxx	xxx = 060 to 250ns
	14–Pin DIP Sheared NC	–40 to +85	DS1005K–xxx	xxx = 060 to 250ns
	8–Pin DIP	–40 to +85	DS1005M–xxx	xxx = 060 to 250ns
	14–Pin GULLWING	–40 to +85	DS1005G–xxx	xxx = 060 to 250ns
	8–Pin GULLWING	–40 to +85	DS1005H–xxx	xxx = 060 to 250ns
	16–Pin SOIC	–40 to +85	DS1005S–xxx	xxx = 060 to 250ns
DS1007	16–Pin DIP	–40 to +85	DS1007–xxx	xxx = 001 to 999ns
	16–Pin SOIC	–40 to +85	DS1007S–xxx	xxx = 001 to 999ns
DS1010	14–Pin DIP	–40 to +85	DS1010–xxx	xxx = 050 to 500ns
	14–Pin GULLWING	–40 to +85	DS1010G–xxx	xxx = 050 to 500ns
	16–Pin SOIC	–40 to +85	DS1010S–xxx	xxx = 050 to 500ns
DS1012	8–Pin DIP	–40 to +85	DS1012M–xxx	xxx = 001 to 999ns
	8–Pin GULLWING	–40 to +85	DS1012H–xxx	xxx = 001 to 999ns
	8–Pin SOIC	–40 to +85	DS1012Z–xxx	xxx = 001 to 999ns
DS1013	14–Pin DIP	–40 to +85	DS1013–xxx	xxx = 010 to 150ns
	8–Pin DIP	–40 to +85	DS1013M–xxx	xxx = 010 to 150ns
	14–Pin GULLWING	–40 to +85	DS1013G–xxx	xxx = 010 to 150ns
	8–Pin GULLWING	–40 to +85	DS1013H–xxx	xxx = 010 to 150ns
	14–Pin Sheared	–40 to +85	DS1013K–xxx	xxx = 010 to 150ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	16–Pin SOIC	–40 to +85	DS1013S–xxx	xxx = 010 to 150ns
DS1020	16–Pin DIP	0 to +85	DS1020–25	0.25ns Steps
	16–Pin DIP	0 to +85	DS1020–500	.50ns Steps
	16–Pin DIP	0 to +85	DS1020–100	1.00ns Steps
	16–Pin DIP	0 to +85	DS1020–200	2.00ns Steps
	16–Pin SOIC	0 to +85	DS1020S–250	.25ns Steps
	16–Pin SOIC	0 to +85	DS1020S–500	.50ns Steps
	16–Pin SOIC	0 to +85	DS1020S–100	1.00ns Steps
	16–Pin SOIC	0 to +85	DS1020S–200	2.00ns Steps
DS1040	8–Pin DIP	–40 to +85	DS1040M–75	75ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–100	100ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–150	150ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–200	200ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–250	250ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–500	500ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–B50	50ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–D60	60ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–A15	15nx max pulse width
	8–Pin DIP	–40 to +85	DS1040M–A20	20ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–A32	32.5ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–B40	40ns max pulse width
	8–Pin DIP	–40 to +85	DS1040M–D70	70ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–75	75ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–100	100ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–150	150ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–200	200ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–250	250ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–500	500ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–B50	50ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–D60	60ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–A15	15ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–A20	20ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–A32	32.5ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–B40	40ns max pulse width
	8–Pin GULLWING	–40 to +85	DS1040H–D70	70ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–75	75ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–100	100ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–150	150ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–200	200ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–250	250ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–500	500ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–B50	50ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–D60	60ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–A15	15ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–A20	20ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–A32	32.5ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–B40	40ns max pulse width
	8–Pin SOIC	–40 to +85	DS1040Z–d70	70ns max pulse width

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1200	10–Pin DIP	0 to + 70	DS1200	
	10–Pin DIP	–40 to +85	DS1200N	
	16–Pin SOIC	0 to +70	DS1200S	
	16–Pin SOIC	–40 to +85	DS1200SN	
DS1201	Electronic Key/Tag	0 to +70	DS1201	
DS1202	8–Pin DIP	0 to +70	DS1202	24 x 8 RAM
	8–Pin DIP	–40 to +85	DS1202N	24 x 8 RAM
	16–Pin SOIC	0 to +70	DS1202S	24 x 8 RAM
	16–Pin SOIC	–40 to +85	DS1202SN	24 x 8 RAM
DS1203S–B1	8–Pin SOIC	0 to +70	DS1203S–B1	
	8–Pin SOIC	–40 to +85	DS1203SN–B1	
DS1204U	Electronic Key/Tag	0 to +70	DS1204U–G01	Generic Code #1
		0 to +70	DS1204U–G02	Generic Code #2
		0 to +70	DS1204U–G03	Generic Code #3
		0 to +70	DS1204U–G04	Generic Code #4
		0 to +70	DS1204U–G05	Generic Code #5
		0 to +70	DS1204U–xxx	xxx = 011 to 999
		0 to +70	DS1204U–G1C	Generic Code #1 w/cap
		0 to +70	DS1204U–G2C	Generic Code #2 w/cap
		0 to +70	DS1204U–G3C	Generic Code #3 w/cap
		0 to +70	DS1204U–G4C	Generic Code #4 w/cap
		0 to +70	DS1204U–G5C	Generic Code #5 w/cap
DS1205S	16–Pin SOIC	0 to +70	DS1205S	
	16–Pin SOIC	–40 to +85	DS1205SN	
DS1205U	Electronic Key/Tag	0 to +70	DS1205U	
DS1206	14–Pin DIP	0 to +70	DS1206	
	14–Pin DIP	–40 to +85	DS1206N	
	16–Pin SOIC	0 to +70	DS1206S	
	16–Pin SOIC	–40 to +85	DS1206SN	
DS1207	Electronic Key/Tag	0 to +70	DS1207–G01	Generic Code #1
		0 to +70	DS1207–G02	Generic Code #2
		0 to +70	DS1207–G03	Generic Code #3
		0 to +70	DS1207–G04	Generic Code #4
		0 to +70	DS1207–G05	Generic Code #5
		0 to +70	DS1207–xxx	xxx = 001 to 999
		0 to +70	DS1207–G1C	Generic Code #1 w/cap
		0 to +70	DS1207–G2C	Generic Code #2 w/cap
		0 to +70	DS1207–G3C	Generic Code #3 w/cap
		0 to +70	DS1207–G4C	Generic Code #4 w/cap
		0 to +70	DS1207–G5C	Generic Code #5 w/cap
DS1209S–B1	16–Pin SOIC	0 to +70	DS1209S–B1	
	16–Pin SOIC	–40 to +85	DS1209SN–B1	
DS1210	8–Pin DIP	0 to +70	DS1210	
	8–Pin DIP	–40 to +85	DS1210N	
	16–Pin SOIC	0 to +70	DS1210S	
	16–Pin SOIC	–40 to +85	DS1210SN	
DS1211	20–Pin DIP	0 to +70	DS1211	
	20–Pin DIP	–40 to +85	DS1211N	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20–Pin SOIC	0 to +70	DS1211S	
	20–Pin SOIC	–40 to +85	DS1211SN	
DS1212	28–Pin DIP	0 to +70	DS1212	
	28–Pin DIP	–40 to +85	DS1212N	
	28–Pin PLCC	0 to +70	DS1212Q	
	28–Pin PLCC	–40 to +85	DS1212QN	
DS1213B	Socket	0 to +70	DS1213B	
DS1213C	Socket	0 to +70	DS1213C	
DS1213D	Socket	0 to +70	DS1213D	
DS1215	16–Pin DIP	0 to +70	DS1215	
	16–Pin DIP	–40 to +85	DS1215N	
	16–Pin SOIC	0 to +70	DS1215S	
DS1216B	Socket	0 to +70	DS1216B	16/64K RAM Socket
DS1216C	Socket	0 to +70	DS1216C	64/256K RAM Socket
DS1216D	Socket	0 to +70	DS1216D	256K/1M RAM Socket
DS1216E	Socket	0 to +70	DS1216E	64/256K ROM Socket
DS1216F	Socket	0 to +70	DS1216F	64/256K/1M ROM Socket
DS1217A		0 to +70	DS1217A 16K–25	16K Bit Density
		0 to +70	DS1217A 64K–25	64K Bit Density
		0 to +70	DS1217A 128K–25	128K Bit Density
		0 to +70	DS1217A 192K–25	192K Bit Density
		0 to +70	DS1217A 256K–25	256K Bit Density
DS1217M		0 to +70	DS1217M 1/2–25	1/2 Megabit Density
		0 to +70	DS1217M 1–15	1 Megabit Density
		0 to +70	DS1217M 2–25	2 Megabit Density
		0 to +70	DS1217M 3–25	3 Megabit Density
		0 to +70	DS1217M 4–25	4 Megabit Density
DS1218	8–Pin DIP	0 to +70	DS1218	
	16–Pin SOIC	0 to +70	DS1218S	
DS1220AB/AD		0 to +70	DS1220AB	200ns
		0 to +70	DS1220AB–150	150ns
		0 to +70	DS1220AB–120	120ns
		0 to +70	DS1220AB–100	100ns
		–40 to +85	DS1220AB–IND	200ns
		–40 to +85	DS1220AB–100–IND	100ns
		0 to +70	DS1220AD	200ns
		0 to +70	DS1220AD–150	150ns
		0 to +70	DS1220AD–120	120ns
		0 to +70	DS1220AD–100	100ns
		–40 to +85	DS1220AD–IND	200ns
		–40 to +85	DS1220AD–100–IND	100ns
DS1220Y		0 to +70	DS1220Y	200ns
		0 to +70	DS1220Y–150	150ns
		0 to +70	DS1220Y–120	120ns
		0 to +70	DS1220Y–100	100ns
		–40 to +85	DS1220Y–IND	200ns
		–40 to +85	DS1220Y–100–IND	100ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1221	16–Pin DIP	0 to +70	DS1221	
	16–Pin DIP	–40 to +85	DS1221N	
	16–Pin SOIC	0 to +70	DS1221S	
	16–Pin SOIC	–40 to +85	DS1221SN	
DS1222	14–Pin DIP	0 to +70	DS1222	
	14–Pin DIP	–40 to +85	DS1222N	
	16–Pin SOIC	0 to +70	DS1222S	
	16–Pin SOIC	–40 to +85	DS1222SN	
DS1225AB/AD		0 to +70	DS1225AB	200ns
		0 to +70	DS1225AB–170	170ns
		0 to +70	DS1225AB–150	150ns
		–40 to +85	DS1225AB–IND	200ns
		–40 to +85	DS1225AB–150–IND	150ns
		0 to +70	DS1225AD	200ns
		0 to +70	DS1225AD–170	170ns
		0 to +70	DS1225AD–150	150ns
		–40 to +85	DS1225AD–IND	200ns
		–40 to +85	DS1225AD–150–IND	150ns
DS1225D/E		0 to +70	DS1225D–120	120ns
		0 to +70	DS1225D–100	100ns
		0 to +70	DS1225D–85	85ns
		0 to +70	DS1225D–70	70ns
		–40 to +85	DS1225D–120–IND	120ns
		–40 to +85	DS1225D–70–IND	70ns
		0 to +70	DS1225E–120	120ns
		0 to +70	DS1225E–100	100ns
		0 to +70	DS1225E–85	85ns
		0 to +70	DS1225E–70	70ns
		–40 to +85	DS1225E–120–IND	120ns
		–40 to +85	DS1225E–70–IND	70ns
DS1225Y		0 to +70	DS1225Y	200ns
		0 to +70	DS1225Y–150	150ns
		0 ot +70	DS1225Y–170	170ns
		–40 to +85	DS1225Y–IND	200ns
		–40 to +85	DS1225Y–150–IND	150ns
DS1227	20–Pin DIP	0 to +70	DS1227	
	20–Pin DIP	–40 to +85	DS1227N	
	20–Pin SOIC	0 to +70	DS1227S	
	20–Pin SOIC	–40 to +85	DS1227SN	
DS1228	16–Pin DIP	0 to +70	DS1228	
	16–Pin SOIC	0 to +70	DS1228S	
DS1229	20–Pin DIP	0 to +70	DS1229	
	20–Pin SOIC	0 to +70	DS1229S	
DS1230Y/AB		0 to +70	DS1230AB	200ns
		0 to +70	DS1230AB–150	150ns
		0 to +70	DS1230AB–120	120ns
		0 to +70	DS1230AB–100	100ns
		0 to +70	DS1230AB–85	85ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
		0 to +70	DS1230AB–70	70ns
		–40 to +85	DS1230AB–IND	200ns
		–40 to +85	DS1230AB–120–IND	120ns
		–40 to +85	DS1230AB–85–IND	85ns
		–40 to +85	DS1230AB–70–IND	70ns
		0 to +70	DS1230Y	200ns
		0 to +70	DS1230Y–150	150ns
		0 to +70	DS1230Y–120	120ns
		0 to +70	DS1230Y–100	100ns
		0 to +70	DS1230Y–85	85ns
		0 to +70	DS1230Y–70	70ns
		–40 to +85	DS1230Y–IND	200ns
		–40 to +85	DS1230Y–120–IND	120ns
		–40 to +85	DS1230Y–85–IND	85ns
		–40 to +85	DS1230Y–70–IND	70ns
DS1231	8–Pin DIP	0 to +70	DS1231–20	20
	8–Pin DIP	0 to +70	DS1231–35	35
	8–Pin DIP	0 to +70	DS1231–50	50
	8–Pin DIP	–40 to +85	DS1231N–20	20
	8–Pin DIP	–40 to +85	DS1231N–35	35
	8–Pin DIP	–40 to +85	DS1231N–50	50
	8–Pin GULLWING	0 to +70	DS1231G–20	20
	8–Pin GULLWING	0 to +70	DS1231G–35	35
	8–Pin GULLWING	0 to +70	DS1231G–50	50
	8–Pin GULLWING	–40 to +85	DS1231GN–20	20
	8–Pin GULLWING	–40 to +85	DS1231GN–35	35
	8–Pin GULLWING	–40 to +85	DS1231GN–50	50
	16–Pin SOIC	0 to +70	DS1231S–20	20
	16–Pin SOIC	0 to +70	DS1231S–35	35
	16–Pin SOIC	0 to +70	DS1231S–50	50
	16–Pin SOIC	–40 to +85	DS1231SN–20	20
	16–Pin SOIC	–40 to +85	DS1231SN–35	35
	16–Pin SOIC	–40 to +85	DS1231SN–50	50
DS1232	8–Pin DIP	0 to +70	DS1232	
	8–Pin DIP	–40 to +85	DS1232N	
	8–Pin GULLWING	0 to +70	DS1232G	
	8–Pin GULLWING	–40 to +85	DS1232GN	
	16–Pin SOIC	0 to +70	DS1232S	
	16–Pin SOIC	–40 to +85	DS1232SN	
DS1232LP	8–Pin DIP	0 to +70	DS1232LP	
	8–Pin DIP	–40 to +85	DS1232LPN	
	8–Pin SOIC	–40 to +85	DS1232LPS–2	
	16–Pin SOIC	0 to +70	DS1232LPS	
	16–Pin SOIC	–40 to +85	DS1232LPSN	
DS1233 5V	TO–92	0 to +70	DS1233–10	10% MONITOR
	TO–92	0 to +70	DS1233–15	15% MONITOR
	TO–92	–40 to +85	DS1233–10N	10% MONITOR
	TO–92	–40 to +85	DS1233–15N	15% MONITOR

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	SOT–223	0 to +70	DS1233Z–10	10% MONITOR
	SOT–223	0 to +70	DS1233Z–15	15% MONITOR
	SOT–223	–40 to +85	DS1233Z–10N	10% MONITOR
	SOT–223	–40 to +85	DS1233Z–15N	15% MONITOR
DS1233A 3.3V	TO–92	0 to +70	DS1233B–10	10% MONITOR
	TO–92	0 to +70	DS1233B–15	15% MONITOR
	TO–92	–40 to +85	DS1233B–10N	10% MONITOR
	TO–92	–40 to +85	DS1233B–15N	15% MONITOR
	SOT–223	0 to +70	DS1233BZ–10	10% MONITOR
	SOT–223	0 to +70	DS1233BZ–15	15% MONITOR
	SOT–223	–40 to +85	DS1233BZ–10N	10% MONITOR
	SOT–223	–40 to +85	DS1233BZ–15N	15% MONITOR
DS1234	14–Pin DIP	0 to +70	DS1234	
	16–Pin SOIC	0 to +70	DS1234S	
DS1236	16–Pin DIP	0 to +70	DS1236	10% MONITOR
	16–Pin DIP	0 to +70	DS1236–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236N–5	5% MONITOR
	16–Pin SOIC	0 to +70	DS1236S	10% MONITOR
	16–Pin SOIC	0 to +70	DS1236S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN–5	5% MONITOR
DS1237	16–Pin DIP	0 to +70	DS1237–x	x = 1 TO 8
	16–Pin SOIC	0 to +70	DS1237S–x	x = 1 TO 8
DS1238	16–Pin DIP	0 to +70	DS1238	10% MONITOR
	16–Pin DIP	0 to +70	DS1238–5	5% MONITOR
	16–Pin SOIC	0 to +70	DS1238S	10% MONITOR
	16–Pin SOIC	0 to +70	DS1238S–5	5% MONITOR
DS1239	16–Pin DIP	0 to +70	DS1239	10% MONITOR
	16–Pin DIP	0 to +70	DS1239–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1239N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1239N–5	5% MONITOR
	16–Pin SOIC	0 to +70	DS1239S	10% MONITOR
	16–Pin SOIC	0 to +70	DS1239S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN–5	5% MONITOR
DS1243Y	28–Pin Encap. DIP	0 to +70	DS1243Y	8K x 8 RAM; 200ns
DS1244Y	28–Pin Encap. DIP	0 to +70	DS1244Y–150	8K x 8 RAM; 150ns
	28–Pin Encap. DIP	0 to +70	DS1244Y–120	8K x 8 RAM; 120ns
DS1245Y/AB		0 to +70	DS1245AB–120	120ns
		0 to +70	DS1245AB–100	100ns
		0 to +70	DS1245AB–85	85ns
		0 to +70	DS1245AB–70	70ns
		–40 to +85	DS1245AB–120–IND	120ns
		–40 to +85	DS1245AB–85–IND	85ns
		–40 to +85	DS1245AB–70–IND	70ns
		0 to +70	DS1245Y–120	120ns
		0 to +70	DS1245Y–100	100ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
		0 to +70	DS1245Y–85	85ns
		0 to +70	DS1245Y–70	70ns
		–40 to +85	DS1245Y–120–IND	120ns
		–40 to +85	DS1245Y–85–IND	85ns
		–40 to +85	DS1245Y–70–IND	70ns
DS1245EE		0 to +70	DS1245EE–120	120ns
		0 to +70	DS1245EE–100	100ns
DS1248Y	32–Pin Encap. DIP	0 to +70	DS1248Y–150	128K x 8 RAM; 150ns
	32–Pin Encap. DIP	0 to +70	DS1248Y–120	128K x 8 RAM; 120ns
DS1250		0 to +70	DS1250	
DS1255U		0 to +70	DS1255U	
DS1258K	Kit	N/A	DS1258K–001	For CyberCard
	Kit	N/A	DS1258K–002	For CyberKey
DS1259	16–Pin DIP	0 to +70	DS1259	
	16–Pin DIP	–40 to +85	DS1259N	
	16–Pin SOIC	0 to +70	DS1259S	
	16–Pin SOIC	–40 to +85	DS1259SN	
DS1260		0 to +70	DS1260–25	250 mAHr
		0 to +70	DS1260–50	500 mAHr
		0 to +70	DS1260–100	1000 mAHr
DS1262	28–Pin DIP	0 to +70		
	28–Pin SOIC	0 to +70	DS1262S	
DS1267	14–Pin DIP	0 to +70	DS1267–10	10K ohms
	14–Pin DIP	0 to +70	DS1267–50	50K ohms
	14–Pin DIP	0 to +70	DS1267–100	100K ohms
	14–Pin DIP	–40 to +85	DS1267N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1267N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1267N–100	100K ohms
	14–Pin SOIC	0 to +70	DS1267S–10	10K ohms
	14–Pin SOIC	0 to +70	DS1267S–50	50K ohms
	14–Pin SOIC	0 to +70	DS1267S–100	100K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–10	10K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–50	50K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–100	100K ohms
DS1275	8–Pin DIP	0 to +70	DS1275	
	8–Pin DIP	–40 to +85	DS1275N	
	8–Pin SOIC	0 to +70	DS1275S	
	8–Pin SOIC	–40 to +85	DS1275SN	
DS1277	24–Pin DIP	0 to +70	DS1277	
	24–Pin DIP	–40 to +85	DS1277N	
DS1280	44–Pin Flat Pack	0 to +70	DS1280FP–44	
	44–Pin Flat Pack	–40 to +85	DS1280FPN–44	
	80–Pin Flat Pack	0 to +70	DS1280FP–80	
	80–Pin Flat Pack	–40 to +85	DS1280FPN–80	
DS1283	28–Pin DIP	0 to +70	DS1283	50 X 8 RAM
	28–Pin SOIC	0 to +70	DS1283S	50 X 8 RAM
DS1284	28–Pin DIP	0 to +70	DS1284	50 X 8 RAM
	28–Pin PLCC	0 to +70	DS1284Q	50 X 8 RAM

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin PLCC	–40 to +85	DS1284QN	50 X 8 RAM
DS1285	24–Pin DIP	0 to +70	DS1285	50 X 8 RAM
	28–Pin PLCC	0 to +70	DS1285Q	50 X 8 RAM
	28–Pin SOIC	0 to +70	DS1285S	50 X 8 RAM
DS1286	28–Pin Encap. DIP	0 to +70	DS1286	50 X 8 RAM
DS1287	24–Pin Encap. DIP	0 to +70	DS1287	50 X 8 RAM
DS1287A	24–Pin Encap. DIP	0 to +70	DS1287A	50 X 8 RAM
DS129X	16–Pin Encap. DIP	0 to +70	DS1290	
	16–Pin DIP	0 to +70	DS1291	
	16–Pin DIP	–40 to +85	DS1291N	
	24–Pin Encap. DIP	0 to +70	DS1292	
	24–Pin DIP	0 to +70	DS1293	
	24–Pin DIP	–40 to +85	DS1293N	
DS1310	40–Pin Socket	0 to +70	DS1310	512 x 8 RAM
DS1311	40–Pin Socket	0 to +70	DS1311	512 x 8 RAM + RTC
DS1336	16–Pin DIP	0 to +70	DS1336	
	16–Pin DIP	–40 to +85	DS1336N	
	16–Pin SOIC	0 to +70	DS1336S	
	16–Pin SOIC	–40 to +85	DS1336SN	
DS1360	20–Pin DIP	0 to +70	DS1360	
	20–Pin DIP	–40 to +85	DS1360N	
	20–Pin SOIC	0 to +70	DS1360S	
	20–Pin SOIC	–40 to +85	DS1360SN	
DS1380	24–Pin DIP	0 to +70	DS1380	
	24–Pin DIP	–40 to +85	DS1380N	
	24–Pin SOIC	0 to +70	DS1380S	
	24–Pin SOIC	–40 to +85	DS1380SN	
DS1381		0 to +70	DS1381	
DS1385	24–Pin DIP	0 to +70	DS1385	4K x 8 RAM
	28–Pin SOIC	0 to +70	DS1385S	4K x 8 RAM
DS1386	32–Pin Encap. DIP	0 to +70	DS1386 8–150	8K x 8 RAM; 150ns
	32–Pin Encap. DIP	0 to +70	DS1386 8–120	8K x 8 RAM; 120ns
	32–Pin Encap. DIP	0 to +70	DS1386 32–150	32K x 8 RAM; 150ns
	32–Pin Encap. DIP	0 to +70	DS1386 32–120	32K x 8 RAM; 120ns
DS1387	32–Pin Encap. DIP	0 to +70	DS1387	4K x 8 RAM
DS1395	24–Pin DIP	0 to +70	DS1395	COMPAQ; 4K x 8 RAM
	28–Pin SOIC	0 to +70	DS1395S	COMPAQ; 4K x 8 RAM
DS1397		0 to +70	DS1397	COMPAQ; 4K x 8 RAM
DS1485	24–Pin DIP	0 to +70	DS1485	8K x 8 RAM
	28–Pin SOIC	0 to +70	DS1485S	8K x 8 RAM
DS1486	32–Pin Encap. DIP	0 to +70	DS1486–150	128K x 8 RAM; 150ns
	32–Pin Encap. DIP	0 to +70	DS1486–120	128K x 8 RAM; 120ns
DS1488	24–Pin Encap. DIP	0 to +70	DS1488	8K x 8 RAM
DS1494		–20 to +70	DS1494L–F5	10 Yrs.
DS1495	24–Pin DIP	0 to +70	DS1495	COMPAQ; 8K x 8 RAM
	28–Pin SOIC	0 to +70	DS1495S	COMPAQ; 8K x 8 RAM
DS1497	24–Pin Encap. DIP	0 to +70	DS1497	COMPAQ; 8K x 8 RAM

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1585	28–Pin DIP	0 to +70	DS1585	8K x 8 RAM
	28–Pin SOIC	0 to +70	DS1585S	8K x 8 RAM
DS1587	28–Pin Encap. DIP	0 to +70	DS1587	8K x 8 RAM
DS1602	8–Pin DIP	0 to +70	DS1602	
	8–Pin DIP	–40 to +85	DS1602N	
	8–Pin SOIC	0 to +70	DS1602S	
	8–Pin SOIC	–40 to +85	DS1602SN	
DS1603	7–Pin Module	0 to +70	DS1603	
	7–Pin Module	–40 to +85	DS1603N	
DS1609	24–Pin DIP	0 to +70	DS1609–35	35ns
	24–Pin DIP	0 to +70	DS1609–50	50ns
	24–Pin DIP	–40 to +85	DS1609N–35	35ns
	24–Pin DIP	–40 to +85	DS1609N–50	50ns
	24–Pin SOIC	0 to +70	DS1609S–35	35ns
	24–Pin SOIC	0 to +70	DS1609S–50	50ns
	24–Pin SOIC	–40 to +85	DS1609SN–35	35ns
	24–Pin SOIC	–40 to +85	DS1609SN–50	50ns
DS1610	16–Pin DIP	0 to +70	DS1610	
	16–Pin DIP	–40 to +85	DS1610N	
	16–Pin SOIC	0 to +70	DS1610S	
	16–Pin SOIC	–40 to +85	DS1610SN	
DS1613		0 to +70	DS1613C	
		0 to +70	DS1613D	
DS1630Y/AB		0 to +70	DS1630AB–120	120ns
		0 to 70	DS1630AB–100	100ns
		0 to 70	DS1630AB–85	85ns
		0 to 70	DS1630AB–70	70ns
		–40 to +85	DS1630AB–70–IND	70ns
		0 to 70	DS1630Y–120	120ns
		0 to 70	DS1630Y–100	100ns
		0 to 70	DS1630Y–85	85ns
		0 to 70	DS1630Y–70	70ns
		–40 to +85	DS1630Y–70–IND	70ns
DS1632	16–Pin DIP	0 to 70	DS1632	
	16–Pin DIP	–40 to +85	DS1632N	
	16–Pin SOIC	0 to +70	DS1632S	
	16–Pin SOIC	–40 to +85	DS1632SN	
DS1633	3–Pin TO–220	–40 to +85	DS1633XX	See factory for complete specifications.
DS1640	16–Pin DIP	0 to 70	DS1640	
	16–Pin DIP	–40 to +85	DS1640N	
	16–Pin SOIC	0 to +70	DS1640S	
	16–Pin SOIC	–40 to +85	DS1640SN	
	16–Pin DIP	0 to +70	DS1640C	Consumer Grade
	16–Pin SOIC	0 to +70	DS1640SC	Consumer Grade
DS1642	28–Pin Encap. DIP	0 to +70	DS1642–120	2K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to +70	DS1642–150	2K x 8 RAM; 150 ns
DS1643	28–Pin Encap. DIP	0 to +70	DS1643–120	8K x 8 RAM; 120 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin Encap. DIP	0 to 70	DS1643–150	8K x 8 RAM; 150 ns
DS1645Y/AB		0 to 70	DS1645AB–120	120ns
		0 to 70	DS1645AB–100	100ns
		0 to 70	DS1645AB–85	85ns
		0 to 70	DS1645AB–70	70ns
		–40 to +85	DS1645AB–70–IND	70ns
		0 to 70	DS1645Y–120	120ns
		0 to 70	DS1645Y–100	100ns
		0 to 70	DS1645Y–85	85ns
		0 to 70	DS1645Y–70	70ns
		–40 to +85	DS1645Y–70–IND	70ns
DS1645EE		0 to 70	DS1645EE–100	100ns
		0 to 70	DS1645EE–85	85ns
		0 to 70	DS1645EE–70	70ns
		–40 to +85	DS1645EE–70–IND	70ns
DS1650Y/AB		0 to 70	DS1650AB–100	100ns
		0 to 70	DS1650AB–85	85ns
		0 to 70	DS1650AB–70	70ns
		–40 to +85	DS1650AB–70–IND	70ns
		0 to 70	DS1650Y–100	100ns
		0 to 70	DS1650Y–85	85ns
		0 to 70	DS1650Y–70	70ns
		–40 to +85	DS1650Y–70–IND	70ns
DS1651	8–Pin DIP	–25 to +85	DS1651	
	8–Pin SOIC	–25 to +85	DS1651S	
DS1652	8–Pin DIP	–25 to +85	DS1652	
	8–Pin SOIC	–25 to +85	DS1652S	
DS1653	8–Pin DIP	–25 to +85	DS1653	
	8–Pin SOIC	–25 to +85	DS1653S	
DS1666	14–Pin DIP	0 to 70	DS1666	
	14–Pin DIP	–40 to +85	DS1666N	
	16–Pin SOIC	0 to 70	DS1666S	
	16–Pin SOIC	–40 to +85	DS1666SN	
DS1667	20–Pin DIP	0 to 70	DS1667	
	20–Pin DIP	–40 to +8	5DS1667N	
	20–Pin SOIC	0 to 70	DS1667S	
	20–Pin SOIC	–40 to +85	DS1667SN	
DS1668	6–Pin Pushbutton	0 to 70	DS1668	
DS1669	8–Pin DIP	0 to 70	DS1669	
	8–Pin DIP	–40 to +85	DS1669N	
	8–Pin SOIC	0 to 70	DS1669S	
	8–Pin SOIC	–40 to +85	DS1669SN	
DS199X–4		–40 to +85	DS1990–R3	
		–20 to +70	DS1991L–F5	10 Yrs
		–20 to +70	DS1992L–F5	10 Yrs
		–20 to +70	DS1993L–F5	10 Yrs
		–20 to +70	DS1994L–F5	10 Yrs

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2009	28–Pin DIP (300 MIL)	0 to 70	DS2009–35	35ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009–50	50ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009–65	65ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009–80	80ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009	120ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009N–35	35ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009N–50	50ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009N–65	65ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009N–80	80ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009N	120ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009D–35	35ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009D–50	50ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009D–65	65ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009D–80	80ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009D	120ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–35	35ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–50	50ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–65	65ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–80	80ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN	120ns
	32–Pin PLCC	0 to 70	DS2009R–35	35ns
	32–Pin PLCC	0 to 70	DS2009R–50	50ns
	32–Pin PLCC	0 to 70	DS2009R–65	65ns
	32–Pin PLCC	0 to 70	DS2009R–80	80ns
	32–Pin PLCC	0 to 70	DS2009R	120ns
	32–Pin PLCC	–40 to +85	DS2009RN–35	35ns
	32–Pin PLCC	–40 to +85	DS2009RN–50	50ns
	32–Pin PLCC	–40 to +85	DS2009RN–65	65ns
	32–Pin PLCC	–40 to +85	DS2009RN–80	80ns
	32–Pin PLCC	–40 to +85	DS2009RN	120ns
DS2010	28–Pin DIP (600 MIL)	0 to 70	DS2010–50	50ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–65	65ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–80	80ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010	120ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–50	50ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–65	65ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–80	80ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N	120ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–50	50ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–65	65ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–80	80ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D	120ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–50	50ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–65	65ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–80	80ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN	120ns
	32–Pin PLCC	0 to 70	DS2010R–50	50ns
	32–Pin PLCC	0 to 70	DS2010R–65	65ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	32–Pin PLCC	0 to 70	DS2010R–80	80ns
	32–Pin PLCC	0 to 70	DS2010R	120ns
	32–Pin PLCC	–40 to +85	DS2010RN–50	50ns
	32–Pin PLCC	–40 to +85	DS2010RN–65	65ns
	32–Pin PLCC	–40 to +85	DS2010RN–80	80ns
	32–Pin PLCC	–40 to +85	DS2010RN	120ns
DS2011	28–Pin DIP (600 MIL)	0 to 70	DS2011–50	50ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–65	65ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–80	80ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011	120ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–50	50ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–65	65ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–80	80ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N	120ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–50	50ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–65	65ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–80	80ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D	120ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–50	50ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–65	65ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–80	80ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN	120ns
	32–Pin PLCC	0 to 70	DS2011R–50	50ns
	32–Pin PLCC	0 to 70	DS2011R–65	65ns
	32–Pin PLCC	0 to 70	DS2011R–80	80ns
	32–Pin PLCC	0 to 70	DS2011R	120ns
	32–Pin PLCC	–40 to +85	DS2011RN–50	50ns
	32–Pin PLCC	–40 to +85	DS2011RN–65	65ns
	32–Pin PLCC	–40 to +85	DS2011RN–80	80ns
	32–Pin PLCC	–40 to +85	DS2011RN	120ns
DS2012	28–Pin DIP (600 MIL)	0 to 70	DS2012–50	50ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–65	65ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–80	80ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012	120ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–50	50ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–65	65ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–80	80ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N	120ns
	32–Pin PLCC	0 to 70	DS2012R–50	50ns
	32–Pin PLCC	0 to 70	DS2012R–65	65ns
	32–Pin PLCC	0 to 70	DS2012R–80	80ns
	32–Pin PLCC	0 to 70	DS2012R	120ns
	32–Pin PLCC	–40 to +85	DS2012RN–50	50ns
	32–Pin PLCC	–40 to +85	DS2012RN–65	65ns
	32–Pin PLCC	–40 to +85	DS2012RN–80	80ns
	32–Pin PLCC	–40 to +85	DS2012RN	120ns
DS2013	28–Pin DIP (600 MIL)	0 to 70	DS2013–50	50ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–65	65ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin DIP (600 MIL)	0 to 70	DS2013–80	80ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013	120ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–50	50ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–65	65ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–80	80ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N	120ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–50	50ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–65	65ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–80	80ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D	120ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–50	50ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–65	65ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–80	80ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN	120ns
DS2015	18–Pin DIP	0 to +70	DS2015	
	20–Pin SOIC	0 to +70	DS2015S	
DS2016	24–Pin DIP	–40 to +85	DS2016	
	24–Pin SOIC	–40 to +85	DS2016S	
DS2064	28–Pin DIP	–40 to +85	DS2064	
	28–Pin SOIC	–40 to +85	DS2064S	
DS2107	16–Pin SOIC	0 to +70	DS2107S	
DS2130	28–Pin DIP	0 to +70	DS2130	
	28–Pin DIP	–40 to +85	DS2130N	
	28–Pin PLCC	0 to +70	DS2130Q	
	28–Pin PLCC	–40 to +85	DS2130QN	
DS2132	28–Pin DIP	0 to +70	DS2132	
	28–Pin DIP	–40 to +85	DS2132N	
	28–Pin PLCC	0 to +70	DS2132Q	
	28–Pin PLCC	–40 to +85	DS2132QN	
DS2141	40–Pin DIP	0 to +70	DS2141	
	40–Pin DIP	–40 to +85	DS2141N	
	44–Pin PLCC	0 to +70	DS2141Q	
	44–Pin PLCC	–40 to +85	DS2141QN	
DS2145	28–Pin DIP	0 to +70	DS2145	
	28–Pin DIP	–40 to +85	DS2145N	
	28–Pin PLCC	0 to +70	DS2145Q	
	28–Pin PLCC	–40 to +85	DS2145QN	
DS2146	28–Pin DIP	0 to 70	DS2146	
	28–Pin DIP	–40 to +85	DS2146N	
	28–Pin PLCC	0 to 70	DS2146Q	
	28–Pin PLCC	–40 to +85	DS2146QN	
DS2165	24–Pin DIP	0 to +70	DS2165	
	24–Pin DIP	–40 to +85	DS2165N	
	28–Pin PLCC	0 to +70	DS2165Q	
	28–Pin PLCC	–40 to +85	DS2165QN	
DS2167	24–Pin DIP	0 to +70	DS2167	
	24–Pin DIP	–40 to +85	DS2167N	
	28–Pin PLCC	0 to +70	DS2167Q	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin PLCC	–40 to +85	DS2167QN	
DS2168	24–Pin DIP	0 to +70	DS2168	
	24–Pin DIP	–40 to +85	DS2168N	
	28–Pin PLCC	0 to +70	DS2168Q	
	28–Pin PLCC	–40 to +85	DS2168QN	
DS2175	16–Pin DIP	0 to +70	DS2175	
	16–Pin DIP	–40 to +85	DS2175N	
	16–Pin SOIC	0 to +70	DS2175S	
	16–Pin SOIC	–40 to +85	DS2175SN	
DS2176	24–Pin DIP	0 to +70	DS2176	
	24–Pin DIP	–40 to +85	DS2176N	
	28–Pin PLCC	0 to +70	DS2176Q	
	28–Pin PLCC	–40 to +85	DS2176QN	
DS2180A	40–Pin DIP	0 to +70	DS2180A	
	40–Pin DIP	–40 to +85	DS2180AN	
	44–Pin PLCC	0 to +70	DS2180AQ	
	44–Pin PLCC	–40 to +85	DS2180AQN	
DS2181A	40–Pin DIP	0 to +70	DS2181A	
	40–Pin DIP	–40 to +85	DS2181AN	
	44–Pin PLCC	0 to +70	DS2181AQ	
	44–Pin PLCC	–40 to +85	DS2181AQN	
DS2182	28–Pin DIP	0 to +70	DS2182	
	28–Pin DIP	–40 to +85	DS2182N	
	28–Pin PLCC	0 to +70	DS2182Q	
	28–Pin PLCC	–40 to +85	DS2182QN	
DS2186	20–Pin DIP	0 to +70	DS2186	
	20–Pin DIP	–40 to +85	DS2186N	
	20–Pin SOIC	0 to +70	DS2186S	
	20–Pin SOIC	–40 to +85	DS2186SN	
DS2187	18–Pin DIP	0 to +70	DS2187	
	20–Pin SOIC	0 to +70	DS2187S	
DS2188	16–Pin DIP	0 to +70	DS2188	
	16–Pin DIP	–40 to +85	DS2188N	
	16–Pin SOIC	0 to +70	DS2188S	
	16–Pin SOIC	–40 to +85	DS2188SN	
DS2190–003		0 to +70	DS2190–003	
DS2219	STIK	0 to +70	DS2219–150	150ns
	STIK	0 to +70	DS2219–120	120ns
DS222X	TO–92	–40 to +85	DS2223	
	SOT–223	–40 to +85	DS2223Z	
	TO–92	–40 to +85	DS2224	
	SOT–223	–40 to +85	DS2224Z	
DS2227	STIK	0 to +70	DS2227–120	120ns
	STIK	0 to +70	DS2227–100	100ns
	STIK	0 to +70	DS2227–70	70ns
DS2229	STIK	0 to +70	DS2229–85	85ns
	STIK	0 to +70	DS2229–100	100ns
	STIK	0 to +70	DS2229–120	120ns

ORDERING INFORMATION

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DS2244T	STIK	0 to +70	DS2244T–24	2400bps
	STIK	0 to +70	DS2244T–12u	1200bps–US only
DS2245	STIK	0 to +70	DS2245–24	2400bps
	STIK	0 to +70	DS2245–12	1200bps
	STIK	0 to +70	DS2245–12u	1200bps–US only
DS2245M	STIK	0 to +70	DS2245M	2400bps w/MNP
DS2249	STIK	0 to +70	DS2249	
DS2249PH	STIK	0 to +70	DS2249PH	
DS2250	STIK	0 to +70	DS2250 8–8	8K RAM; 8 MHz
	STIK	0 to +70	DS2250 8–12	8K RAM; 12 MHz
	STIK	0 to +70	DS2250 8–16	8K RAM; 16 MHz
	STIK	0 to +70	DS2250 32–8	32K RAM; 8 MHz
	STIK	0 to +70	DS2250 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2250 32–16	32K RAM; 16 MHz
	STIK	0 to +70	DS2250 64–8	64K RAM; 8 MHz
	STIK	0 to +70	DS2250 64–12	64K RAM; 12 MHz
	STIK	0 to +70	DS2250 64–16	64K RAM; 16 MHz
DS2250T	STIK	0 to +70	DS2250T 8–8	8K RAM; 8 MHz
	STIK	0 to +70	DS2250T 8–12	8K RAM; 12 MHz
	STIK	0 to +70	DS2250T 8–16	8K RAM; 16 MHz
	STIK	0 to +70	DS2250T 32–8	32K RAM; 8 MHz
	STIK	0 to +70	DS2250T 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2250T 32–16	32K RAM; 16 MHz
	STIK	0 to +70	DS2250T 64–8	64K RAM; 8 MHz
	STIK	0 to +70	DS2250T 64–12	64K RAM; 12 MHz
	STIK	0 to +7	0DS2250T 64–16	64K RAM; 16 MHz
DS2251	STIK	0 to +70	DS2251 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2251 32–16	32K RAM; 16 MHz
	STIK	0 to +70	DS2251 64–12	64K RAM; 12 MHz
	STIK	0 to +70	DS2251 64–16	64K RAM; 16 MHz
	STIK	0 to +70	DS2251 128–12	128K RAM; 12 MHz
	STIK	0 to +70	DS2251 128–16	128K RAM; 16 MHz
	STIK	0 to +70	DS2251T 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2251T 32–16	32K RAM; 16 MHz
	STIK	0 to +70	DS2251T 64–12	64K RAM; 12 MHz
	STIK	0 to +70	DS2251T 64–16	64K RAM; 16 MHz
	STIK	0 to +70	DS2251T 128–12	128K RAM; 12 MHz
	STIK	0 to +70	DS2251T 128–16	128K RAM; 16 MHz
DS2252	STIK	0 to +70	DS2252 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2252 32–16	32K RAM; 16 MHz
	STIK	0 to +70	DS2252 64–12	64K RAM; 12 MHz
	STIK	0 to +70	DS2252 64–16	64K RAM; 16 MHz
	STIK	0 to +70	DS2252 128–12	128K RAM; 12 MHz
	STIK	0 to +70	DS2252 128–16	128K RAM; 16 MHz
	STIK	0 to +70	DS2252T 32–12	32K RAM; 12 MHz
	STIK	0 to +70	DS2252T 32–1	632K RAM; 16 MHz
	STIK	0 to +70	DS2252T 64–12	64K RAM; 12 MHz
	STIK	0 to +70	DS2252T 64–16	64K RAM; 16 MHz

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	STIK	0 to +70	DS2252T 128–12	128K RAM; 12 MHz
	STIK	0 to +70	DS2252T 128–16	128K RAM; 16 MHz
DS2257	28–Pin DIP	–40 to +85	DS2257	
	28–Pin SOIC	–40 to +85	DS2257S	
DS2262	STIK	0 to +70	DS2262–4	4M x 1
	STIK	0 to +70	DS2262–8	8M x 1
	STIK	0 to +70	DS2262–16	16M x 1
	STIK	0 to +70	DS2262–32	32M x 1
DS2264/8	STIK	0 to +70	DS2264	–EXP uses DS2165Q
	STIK	0 to +70	DS2268	–EXP uses DS2165Q
DS2271	STIK	0 to +70	DS2271	
DS2271DK	Kit	N/A	DS2271DK	
DS2280/1	STIK	0 to +70	DS2280	
	STIK	0 to +70	DS2281–75	75 ohm
	STIK	0 to +70	DS2281–120	120 ohm
DS2282	STIK	0 to +70	DS2282	
DS2283	STIK	0 to +70	DS2283	
DS2284	STIK	0 to +70	DS2284	
	STIK	0 to +70	DS2287–32	32K x 8
DS2290	STIK	0 to +70	DS2290	
DS2291	STIK	0 to +70	DS2291	
DS2340	STIK	0 to +55	DS2340 64B	64K RAM; 10 MHz
	STIK	0 to +55	DS2340 256B	256K RAM; 10 MHz
	STIK	0 to +55	DS2340T 64B	64K RAM; 10 MHz
	STIK	0 to +55	DS2340T 256B	256K RAM; 10 MHz
DS2400	TO–92	–40 to +85	DS2400	
	SOT–223	–40 to +85	DS2400Z	
DS2404	16–Pin DIP	0 to +70	DS2404	512 x 8 RAM
	16–Pin SOIC	0 to +70	DS2404S	512 x 8 RAM
DS2569	16–Pin SOIC	0 to +70	DS2569S	
	16–Pin SOIC	–40 to +85	DS2569N	
DS5000	40–Pin Module	0 to +70	DS5000 8–8	8K RAM; 8MHz
	40–Pin Module	0 to +70	DS5000 8–12	8K RAM; 12MHz
	40–Pin Module	0 to +70	DS5000 8–16	8K RAM; 16MHz
	40–Pin Module	0 to +70	DS5000 32–8	32K RAM; 8MHz
	40–Pin Module	0 to +70	DS5000 32–12	32K RAM; 12MHz
	40–Pin Module	0 to +70	DS5000 32–16	32K RAM; 16MHz
DS5000FP	80–Pin FLAT PACK	0 to +70	DS5000FP–8	8 MHz
	80–Pin FLAT PACK	0 to +70	DS5000FP–12	12 MHz
	80–Pin FLAT PACK	0 to +70	DS5000FP–16	16 MHz
	80–Pin FLAT PACK	–40 to +85	DS5000FPN–8	8 MHz
	80–Pin FLAT PACK	–40 to +85	DS5000FPN–12	12 MHz
	80–Pin FLAT PACK	–40 to +85	DS5000FPN–16	16 MHz
DS5000T	40–Pin Module	0 to +70	DS5000T 8–8	8K RAM; 8MHz
	40–Pin Module	0 to +70	DS5000T 8–12	8K RAM; 12MHz
	40–Pin Module	0 to +70	DS5000T 8–16	8K RAM; 16MHz
	40–Pin Module	0 to +70	DS5000T 32–8	32K RAM; 8MHz
	40–Pin Module	0 to +70	DS5000T 32–12	32K RAM; 12MHz

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	40–Pin Module	0 to +70	DS5000T 32–16	32K RAM; 16MHz
DS5000TK	Kit	N/A	DS5000TK	
DS5001FP	80–Pin FLAT PACK	0 to +70	DS5001FP–12	12 MHz
	80–Pin FLAT PACK	0 to +70	DS5001FP–16	16 MHz
DS5002FP	80–Pin FLAT PACK	0 to +70	DS5002FP–12	12 MHz
DS5311FP	80–Pin FLAT PACK	0 to +70	DS5311FP	2.0 MHz
	80–Pin FLAT PACK	0 to +70	DS5311FP–A	3.0 MHz
DS5340FP	80–Pin FLAT PACK	0 to +70	DS5340FP	8 MHz
	80–Pin FLAT PACK	0 to +70	DS5340FP–A	10 MHz
DS6071K	Kit	N/A	DS6071K	
DS620X		0 to +70	DS6201	
		0 to +70	DS6204U	Generic Code #1
		0 to +70	DS6204U–2	Generic Code #2
		0 to +70	DS6204U–3	Generic Code #3
		0 to +70	DS6204U–4	Generic Code #4
		0 to +70	DS6204U–5	Generic Code #5
		0 to +70	DS6204U–xxx	xxx = 001 to 999
		0 to +70	DS6207	Generic Code #1
		0 to +70	DS6207–2	Generic Code #2
		0 to +7	0DS6207–3	Generic Code #3
		0 to +70	DS6207–4	Generic Code #4
		0 to +70	DS6207–5	Generic Code #5
		0 to +70	DS6207–xxx	xxx = 001 to 999
DS6417		0 to +70	DS6417–1	1 Megabit Density
		0 to +70	DS6417–2	2 Megabit Density
		0 to +70	DS6417–4	4 Megabit Density
DS9000			DS9000	
DS9002			DS9002	
DS9003			DS9003	
DS9005			DS9005	
DS9006			DS9006	
DS9006K	Kit		DS9006K	
DS907X		.100" Pitch	DS9071–30V	30 Pos.–Vertical
		.100" Pitch	DS9071–30I	30 Pos.–Inclined
		.100" Pitch	DS9071–35V	35 Pos.–Vertical
		.100" Pitch	DS9071–35I	35 Pos.–Inclined
		.050" Pitch	DS9072–40V	40 Pos.–Vertical
		.050" Pitch	DS9072H–40R	40 Pos.–Rt Angle–Hi
		.050" Pitch	DS9072L–40R	40 Pos.–Rt Angle–Lo
		.050" Pitch	DS9072–68V	68 Pos.–Vertical
		.050" Pitch	DS9072–68I	68 Pos.–Inclined
		.050" Pitch	DS9072H–68R	68 Pos.–Rt Angle–Hi
		.050" Pitch	DS9072L–68R	68 Pos.–Rt Angle–Lo
		.050" Pitch	DS9072–72V	72 Pos.–Vertical
		.050" Pitch	DS9072–72I	72 Pos.–Inclined
		.050" Pitch	DS9072H–72R	72 Pos.–Rt Angle–Hi
		.050" Pitch	DS9072L–72R	72 Pos.–Rt Angle–Lo
			DS9075–40V	40 Pos.–Vert; 40 Pins

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
		.050" Pitch	DS9076–40	40 Pins; 40 Pos.
DS908x			DS9080V	Cyber Key–Vertical
			DS9080A	Cyber Key–Angled
			DS9081V	Cyber Key–Vertical
			DS9081A	Cyber Key–Angled
			DS9082V	Cyber Card–Vertical
			DS9082A	Cyber Card–Angled
			DS9084V	Cyber Card EV Recessed–Vertical
			DS9084A	Cyber Card EV Recessed–Angled
DS9092			DS9092	Panel Mount Reader
			DS9092T	Panel Mount Reader w/ Tactile Pin
			DS9092GT	Wand Reader w/ Tactile Pin
DS9093			DS9093	Key Ring Mount
			DS9093F	Key Ring Mount,
			DS9093S	Permanent Mount, 2 Screw Holes
			DS9093P	Permanent Mount, 1 Screw Hold, 1 Pin Flanged Can(F5)
DS9094			DS9094	3.2mm Can, Thru hole Mount (R3)
			DS9094F	5.8mm Can, Thru hole Mount (F5)
			DS9094FS	5.8mm Can, Surface Mount (F5)
DS9096			DS9096	Semi–permanent Adhesive Pad
DS9096P				Permanent Bond Adhesive Pad
DS9098			DS9098	5.8 SNAP–IN Retainer(F5)
DS12885	24–Pin DIP	0 to +70	DS12885	114 X 8 RAM
	28–Pin PLCC	0 to +70	DS12885Q	114 X 8 RAM
	28–Pin SOIC	0 to +70	DS12885S	114 X 8 RAM
DS12887	24–Pin Encap. DIP	0 to +70	DS12887	114 X 8 RAM
DS12887A	24–Pin Encap. DIP	0 to +70	DS12887A	114 X 8 RAM

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Worthington, OH
(614) 888-3313
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Tulsa, OK
(918) 254-6110
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(512) 258-8848
Dallas, TX
(214) 343-5000
Houston, TX
(713) 781-6100
Washington
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San Diego, CA
(619) 587-0471
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(408) 720-9222
Oregon
Beaverton, OR
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(214) 783-0800
Washington
Kirkland, WA
(206) 820-8100

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Singapore
Dynamar Int.
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South Africa
Tarsus Technologies
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Spain
Comelta, S.A.
34-1-754-3001
34-3-582-1991
Sweden
DIPCOM Electronics AB
46-8-644-9190
Switzerland
Computer Controls AG
41-1-313-0616
Taiwan
Landcol Enterprises
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Thailand
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Austria
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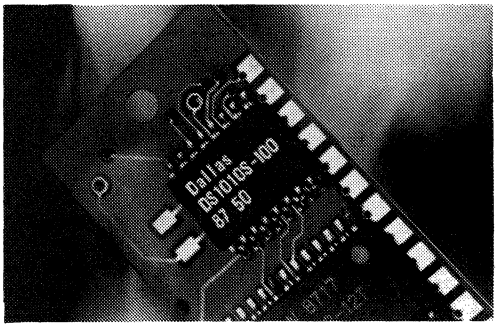
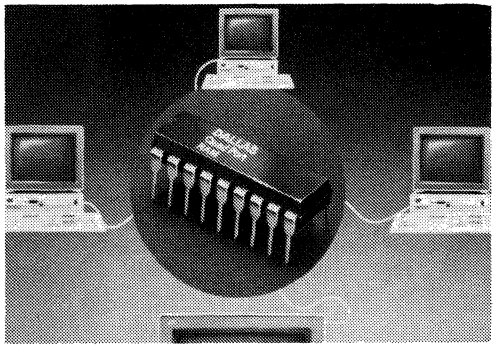


Silicon Timed Circuits

All-silicon time delay lines can withstand the high temperatures associated with surface mounting in small outline packages. They also offer better accuracy than the hybrid approach to delay lines. Laser writing techniques used to customize chips offer maximum flexibility from tailor-made products at off-the-shelf prices.

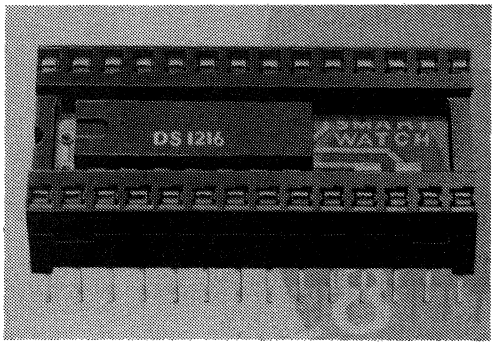


Multiport Memory

A complete line of X9 FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out procedures in storing and retrieving data, the products are dual-ported for simultaneous reads and writes. This product family also includes two- and four-port RAMs that couple up to four computers at low cost.

Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during power loss. Partitionable NV SRAM allows the write protection of critical program and data memory.

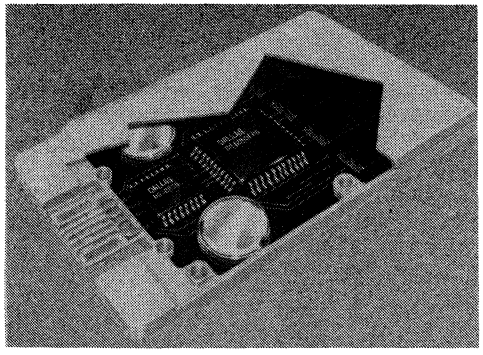


Intelligent Sockets

Intelligent sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.

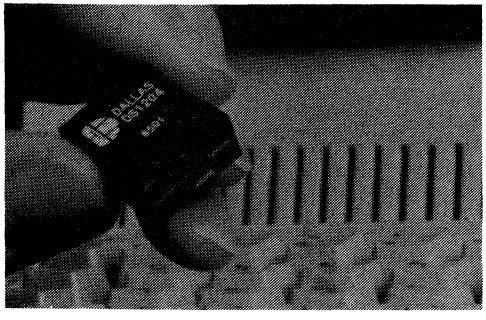
Timekeeping

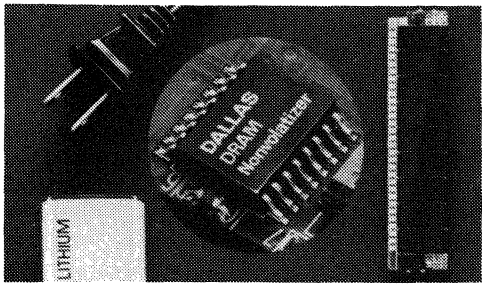
A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, 1-Wire serial, 3-Wire serial, PC DOS, and JEDEC bytewide memory.



User-Insertable Memory

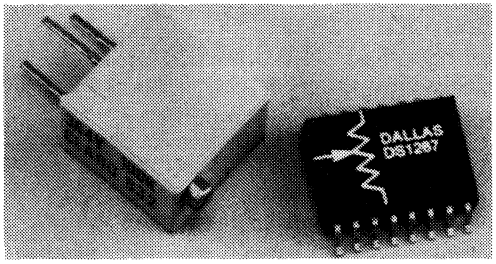
Nonvolatile memories with densities from 256 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. The CyberCard portable data carriers can be inserted and withdrawn 50,000 times. Secured versions of these of these data carriers protect data against unauthorized use. All products can be read or written by a PC.





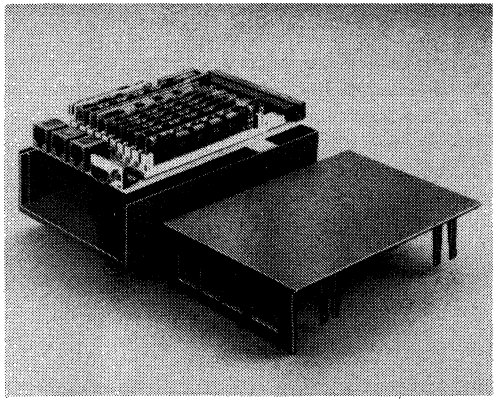
Battery Backup and Battery Chargers

These chips crashproof microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Products nonvolatize both static RAM and dynamic RAM. The battery charger chips optimize charging time for rechargeable batteries.



System Extension

These CMOS products add a variety of special features to systems without encumbering design. The **CPU Supervision** circuits provides all necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. **Digital Resistors** change their resistance under the control of software. **Line Interfaces** such as the DS2107 SCSI Terminator quiet transmission lines with a precision voltage regulator and terminating resistors.



SIP Stik Prefabs

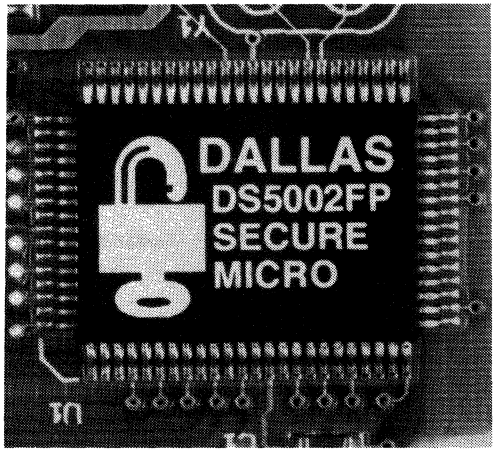
SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.

The Dallas Semiconductor SIP Stik family can provide approximately 80 percent of the circuitry in a typical system. With SIP Stik prototype accessories, a complete system can be mocked up quickly and compactly.

Automatic Identification

With Auto ID technology, a chip attached to an object, or carried by a person, identifies and holds relevant information. These read/write data carriers can be updated via computer while affixed to an object. Auto ID chips can facilitate automation by tracking a work piece as it travels along an assembly line; people can access secure areas with convenience.

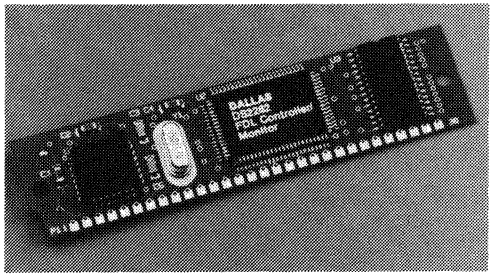
Using Touch technology, a memory chip can be read or written with the touch of a probe. Each Touch Memory is packaged in a stainless steel MicroCan™ 16 mm in diameter. Individual chips are also available along with mounting accessories, probes, and an evaluation kit.



Microcontrollers

Unlike rigid ROM/EPROM microcontrollers, Dallas Semiconductor microcontroller chips are designed for change: they convert industry-standard bytewide SRAM into high-performance, read/write storage that is nonvolatile for more than ten years. This memory is initially loaded via a serial port and can be dynamically partitioned to fit program and data storage requirements. System performance can be improved based on cumulative knowledge maintained in nonvolatile RAM. On-chip crashproof circuitry and an external lithium cell permit task processing to resume after a power outage.

This changeable nature also facilitates security. The DS5002 Secure Micro Chip provides the highest level of protection available for firmware or data memory. Protective measures that foil attack include address and data encryption of memory contents (performed using a 64-bit key); random generation of new keys; a vector RAM area that hides reset and interrupt vectors; a security lock that protects keys and memory contents; and a self-destruct input that wipes memory contents and keys if tampering occurs.

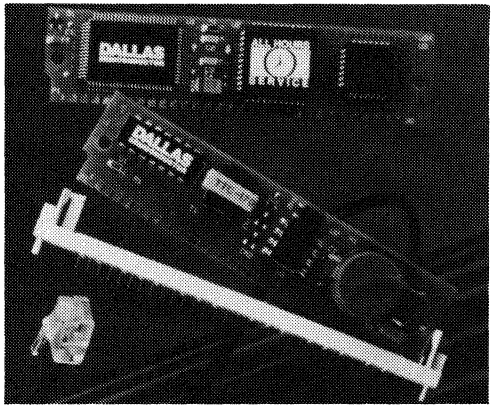


Telecommunications

A comprehensive product family addresses the requirements of high-speed digital voice/data transmission and monitoring in T1, CEPT or Primary Rate ISDN networks. ADPCM processors double or quadruple the capacity of voice communication channels through DSP compression techniques.

Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments—all from a desktop computer over an ordinary telephone line. A growing family of coordinated hardware and software products offers new solutions to service problems at a price well under the cost of an airplane ticket. Components include cartridges for retrofit, modular components for new designs, and a software tool kit.



The DS6071 TeleMemory w/MNP system retrofits a bytewide RAM device in an existing system. Using a 28-pin ribbon cable, the TeleMemory connects to the RAM socket and provides 32K nonvolatile RAM to the target system. A remote user can call the TeleMemory and view, edit or reload the contents of the RAM device. It is also suitable for retrofitting an EPROM and allows remote loading of firmware. The TeleMemory with MNP features error correction and data compression to ensure fast, reliable communication.

CORPORATE FACT SHEET

Dallas Semiconductor designs, manufactures, and markets electronic chips and chip–based subsystems. Rather than build products that others have already made, the company concentrates on one–of–a–kind solutions that span many application areas. Through the use of Late Definition technologies, Soft Silicon™ chips can be tailored after they are made – even during use.

Founded February 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of a variety of industries. The company's development teams constantly attack unsolved problems and introduce new products to the marketplace.

In its eight–year history, Dallas Semiconductor has shipped 150 base products to more than 7,000 customers worldwide. These include Original Equipment Manufacturers (OEMs) in instrumentation, factory automation, personal computers, office equipment, telecommunications, medical equipment, and mainframe computers. Over the last 5 years, the company has spent $57.6 million on research and development.

Chips and subsystems are sold through a direct sales force, distributors and manufacturers' representatives worldwide. Sales for 1991 totaled $103.8 million. Dallas Semiconductor has 662 employees. On March 19, 1990, the company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions – dynamic, flexible, chip–based products that can be molded in the final manufacturing stages or during use. Soft Silicon™ is made possible by the Late Definition technologies of lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crash-proof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub–micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing also allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

The Company's facilities encompass 230,000 square feet in north Dallas. This location includes a six–inch, submicron plant, one of the most sophisticated wafer production plants in the world. It features Class One cleanliness; automated wafer processing; dry etch using plasma techniques; and 0.15 micron direct step alignment tolerances. Automated modular process technology provides substantial flexibility in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. As an example, our pick and place machine assembles Stik subsystems under computer control and can position up to 4,500 chips per hour. All products are shipped from Dallas after final quality assurance and testing.

MARKETING AND SALES

Dallas Semiconductor coordinates its selling activity from its Dallas, Texas headquarters. Eleven area sales managers call on OEM accounts and coordinate the activities of sales representative offices in North America, Europe and Asia. Dallas Semiconductor also markets its products in North America through national and regional stocking distributors.

QUALITY AND RELIABILITY

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL–STD–105.
- *In–Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In–Process Sample Tests:* In order to guarantee the accuracy and completeness of in–process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL–STD–105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state–of–the–art environmental facility allows accelerated stresses to be performed and monitored in–house. In addition, a metallurgical laboratory has been equipped to perform real-time x–ray, x–ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer–based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production–ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

RELIABILITY TESTS

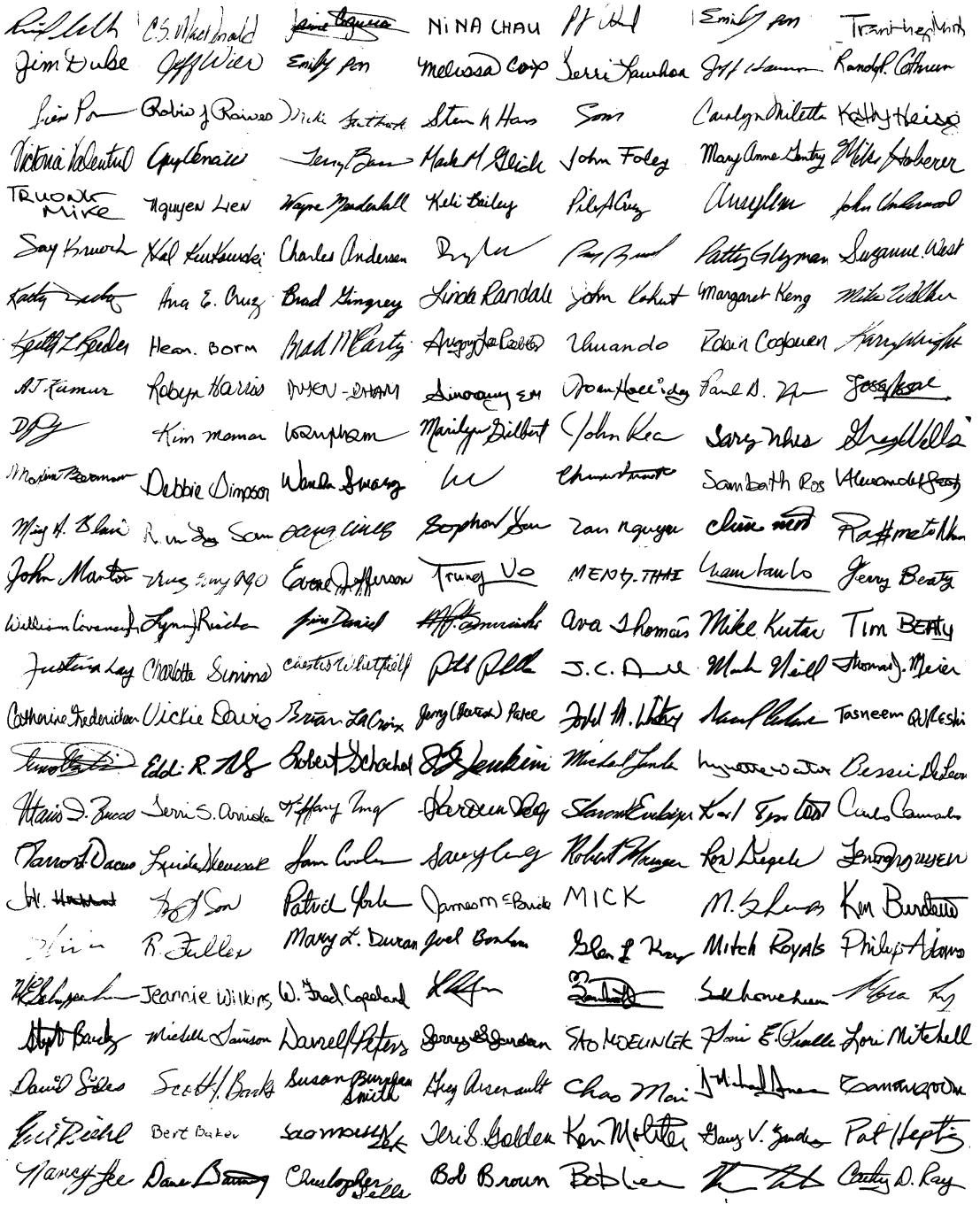
Table 1 lists the tests which an integrated circuit must pass in order to be classified as fully qualified.

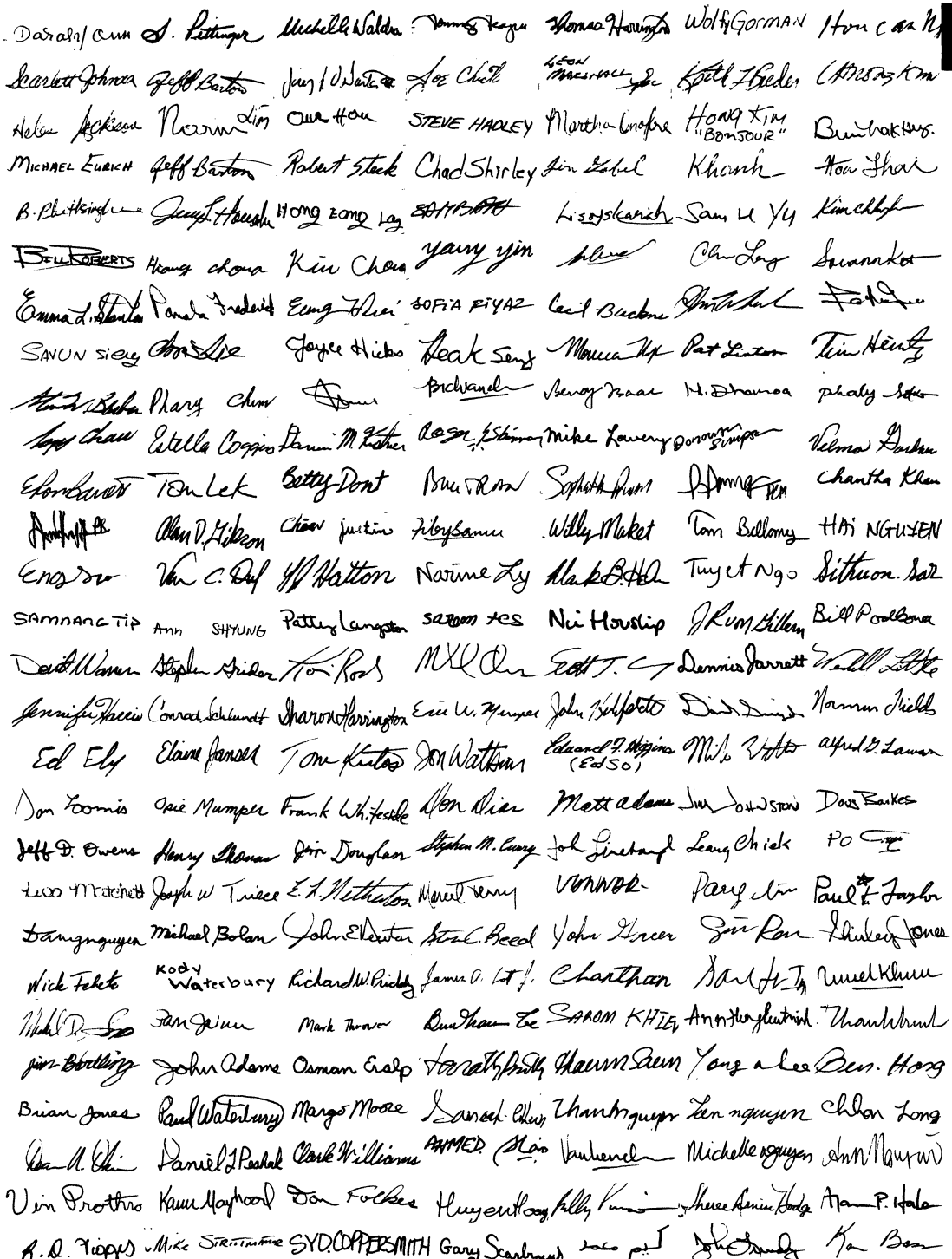
FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUITS Table 1

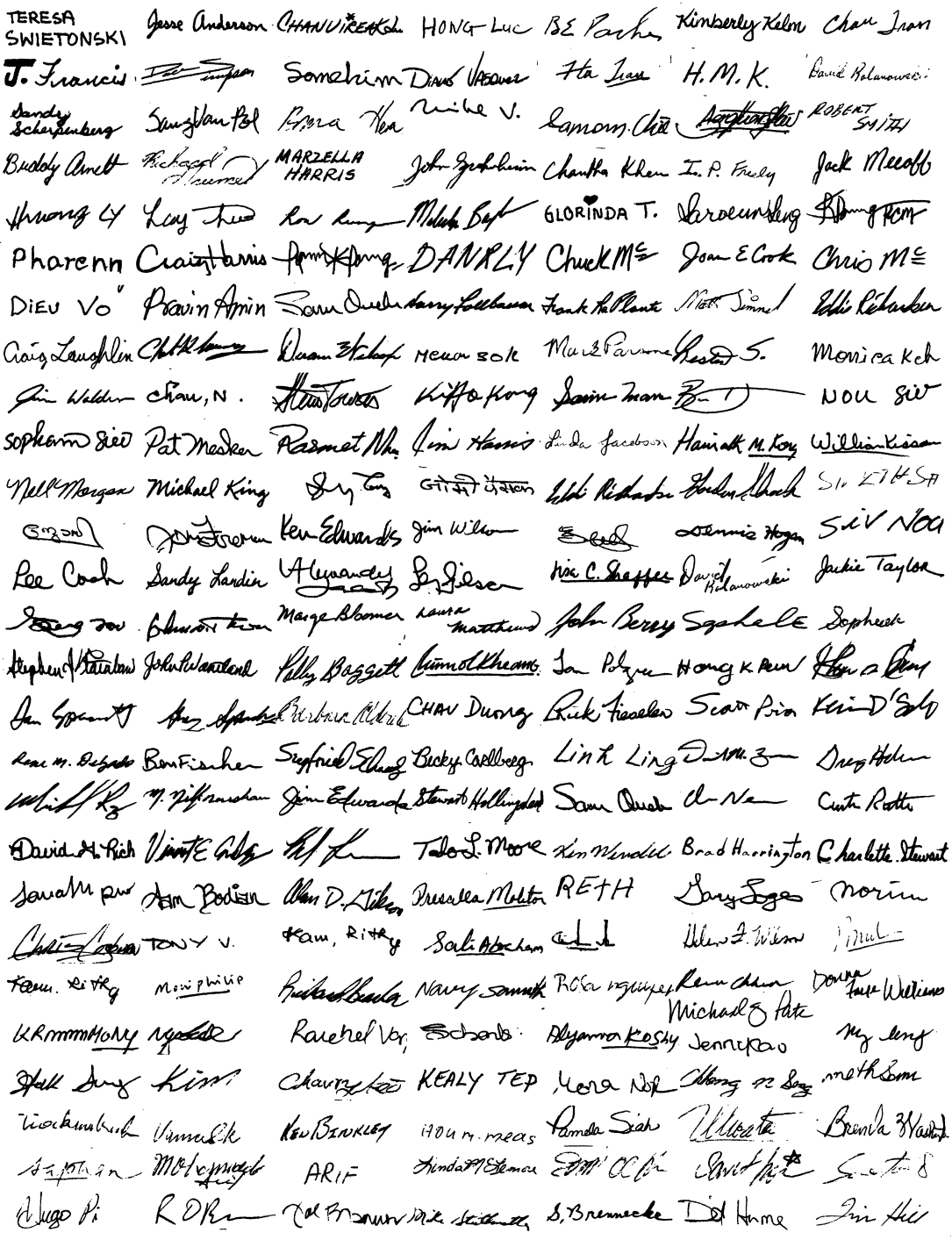
STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
Long Term Life	125°C, 5.5V	1000 Hr.	1.5%
Use Condition Prediction	55°C, 5.5V	10 years	*100 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	3.0%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	2.5%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	–55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Bond Pull	MIL–STD–883 Method 2011	Premold	1.5%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%

* Combined high voltage life and long term life requirement.

Quality Completes Our Innovation







DALLAS SEMICONDUCTOR

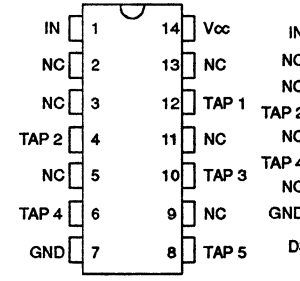
DS1000
5-Tap Silicon Delay Line

2

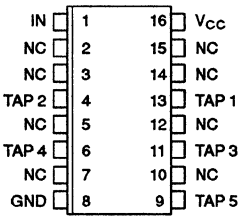
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT

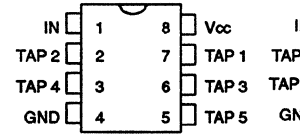


DS1000 14-PIN DIP (300 MIL)
DS1000G 14-PIN GULLWING (300 MIL)
DS1000K 14-PIN SHEARED NC
See Mech. Drawings Sect. 16, Pgs. 1 & 3

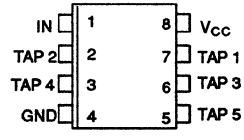


DS1000S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

Also Available In Die Form



DS1000M 8-PIN DIP (300 MIL)
DS1000H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Section 16, Pgs. 1 & 3



DS1000Z 8-PIN SOIC
(150 MIL)
See Mech. Drawing
Sect. 16, Pg. 5

PIN DESCRIPTION

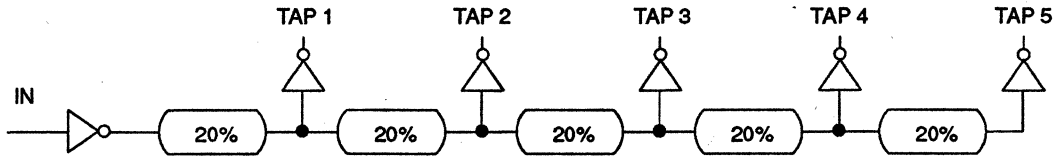
TAP 1-TAP 5	- Tap Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1000-20*	4 ns	8 ns	12 ns	16 ns	20 ns
DS1000-25	5 ns	10 ns	15 ns	20 ns	25 ns
DS1000-30	6 ns	12 ns	18 ns	24 ns	30 ns
DS1000-35	7 ns	14 ns	21 ns	28 ns	35 ns
DS1000-40	8 ns	16 ns	24 ns	32 ns	40 ns
DS1000-45	9 ns	18 ns	27 ns	36 ns	45 ns
DS1000-50	10 ns	20 ns	30 ns	40 ns	50 ns
DS1000-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1000-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1000-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1000-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1000-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1000-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1000-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1000-250	50 ns	100 ns	150 ns	200 ns	250 ns
DS1000-350	70 ns	140 ns	210 ns	280 ns	350 ns
DS1000-450	90 ns	180 ns	270 ns	360 ns	450 ns
DS1000-500	100 ns	200 ns	300 ns	400 ns	500 ns

Custom delays available.
*Consult Dallas Semiconductor for availability.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

2

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		35	75	mA	2,8
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{cc} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6, 9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6, 9
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

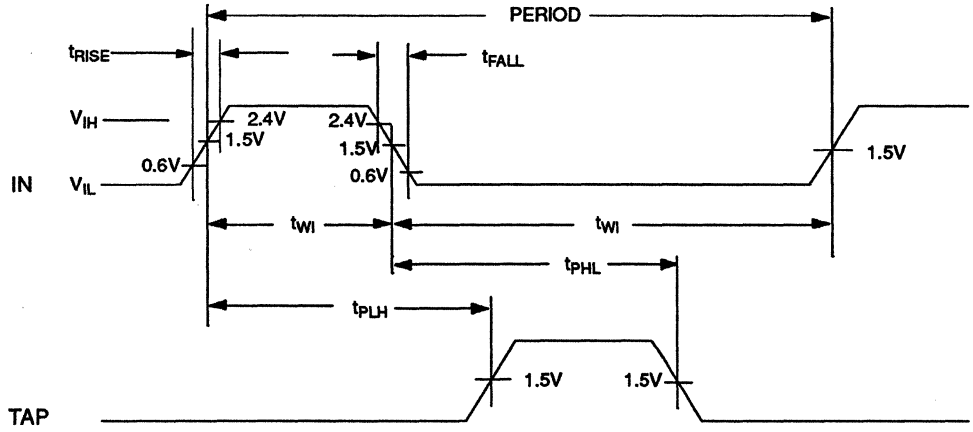
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

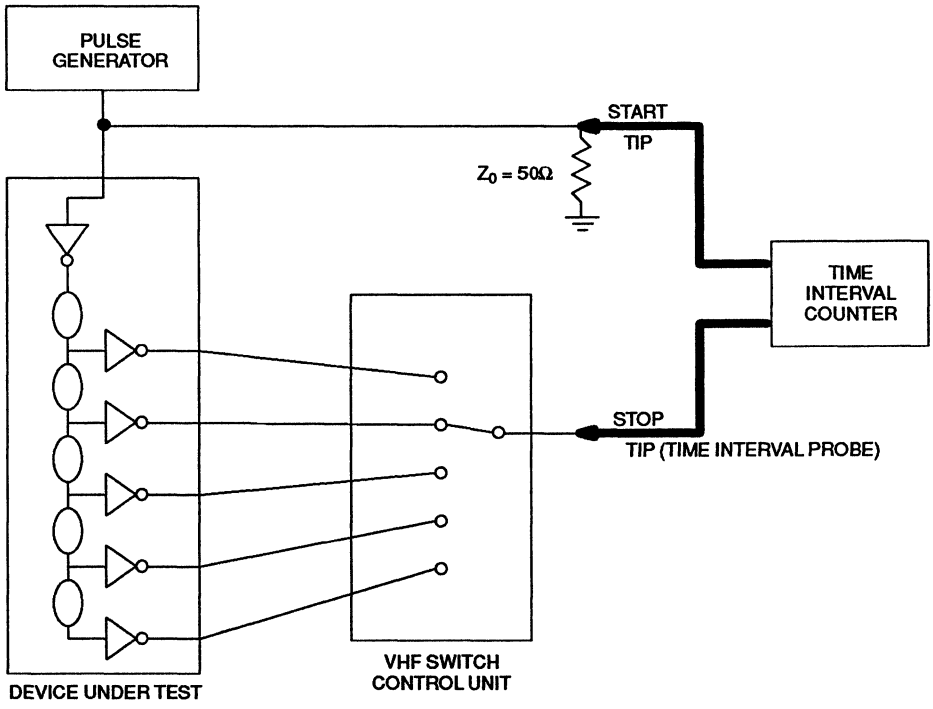
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @25°C. Delays accurate on both rising and falling edges within ±2 ns or 5%, whichever is greater.
4. For DS1000 delay lines with a TAP 5 delay of 50 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input to tap delay shiift of ± 1 ns or ± 3%, whichever is greater.
5. For DS1000 delay lines with a TAP 5 delay less than 50 ns, temperature variations from 25°C to 0°C or 70° may produce an additional input to tap delay shift of ± 1 ns or ± 10%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
7. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (de-coupling, layout, etc.).
8. I_{CC} is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75 mA. For example a -100 will never exceed 30 mA, etc.
9. See "Test Conditions" section at the end of this data sheet.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT :

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	500ns (1us for -500)
Period:	1 us (2us for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

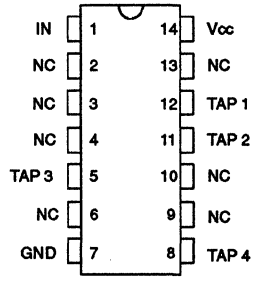
DS1003
4-Tap Silicon Delay Line for RISC Applications

2

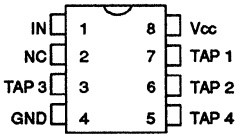
FEATURES

- All-silicon time delay
- Four delayed clock phases from input
- Input frequency independent
- Precise tap-to-tap delays
- Leading and trailing edge precision
- Preserves input symmetry
- Output rise time minimizes ringing
- Economical
- 8- and 14-pin packages available in DIP and surface mount
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays and pinouts available
- Fast turn prototypes

PIN ASSIGNMENT



DS1003 14-PIN DIP
(300 MIL)*
DS1003G 14-PIN GULLWING
(300 MIL)*
See Mech. Drawings
Sect. 16, Pgs. 1 & 3



DS1003M 8-PIN DIP
(300 MIL)*
DS1003H 8-PIN GULLWING
(300 MIL)*
See Mech. Drawings
Sect. 16, Pgs. 1 & 3

Also Available
In Die Form

*Consult Factory for Custom Packaging

PIN DESCRIPTION

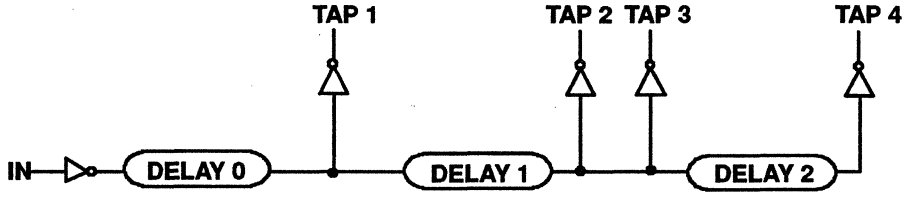
TAP 1 – TAP 4	TAP Output Number
VCC	+5 Volts
GND	Ground
NC	No Connection
IN	Input

DESCRIPTION

The DS1003 Delay Line has been specifically designed to supply the four independent clock timing phases required by some RISC microprocessors and their related coprocessors. For optimum compatibility, the DS1003 accepts TTL input levels and supplies CMOS and TTL compatible output levels. The DS1003 is offered in 8- and 14-pin DIP and gullwing packages for surface mounting. Low cost and superior reliability is achieved by the combination of a 100% silicon delay line and industry standard packaging. The DS1003 series of delay lines provides precise tap-to-tap delays while preserving input waveform symmetry. Since the DS1003 is not based on Phase Locked Loop (PLL) technology, timing is input frequency-independent. Each tap is capable of driving a minimum of four LSTTL or CMOS loads. Tap-to-tap timing accuracy is not affected by the addition of equal capacitive loads (e.g. coprocessors).

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450–5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}) Table 1

PART NO.		DS1003-16	DS1003-20	DS1003-25	DS1003-33	DS1003-40*
INPUT - TAP 1	Delay 0	8 ns ± 2 ns	8 ns ± 2 ns	8 ns ± 2 ns	6 ns ± 2 ns	6 ns ± 2 ns
TAP 1 - TAP 2	Delay 1	6 ns ± .75 ns	6 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns
TAP 1 - TAP 4	Delay 1+ Delay 2	16 ns ± 1 ns	14 ns ± 1 ns	12 ns ± .75 ns	9 ns ± .75 ns	8 ns ± .75 ns
TAP 2 - TAP 3 (Note 10)	——	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns
TAP 3 - TAP 4	Delay 2	10 ns ± .75 ns	8 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns

PERIOD AND WIDTH TABLE Table 2

PART NO.	PERIOD			t_{WI}		
	MIN	NOM	MAX	MIN	NOM	MAX
DS1003-16	29 ns	30 ns	∞	12 ns	15 ns	∞
DS1003-20	24 ns	25 ns	∞	10 ns	12.5 ns	∞
DS1003-25	19 ns	20 ns	∞	8 ns	10 ns	∞
DS1003-33	14 ns	15 ns	∞	6 ns	7.5 ns	∞
DS1003-40*	12 ns	12.5 ns	∞	5 ns	6.25 ns	∞

I_{CC} TABLE Table 3

PART NO.	I_{CC}	
	TYP.	MAX.
DS1003-16	65 mA	75 mA
DS1003-20	75 mA	85 mA
DS1003-25	85 mA	95 mA
DS1003-33	100 mA	110 mA
DS1003-40*	115 mA	125 mA

*Consult factory for availability.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		Table 3	Table 3	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OH} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	Table 2	Table 2	Table 2	ns	6
TAP to TAP Delay (leading edge)	t_{PLH}	Table 1	Table 1	Table 1	ns	3,4,5,6,7
TAP to TAP Delay (trailing edge)	t_{PHL}		Note 9		ns	9
Output Symmetry (Input: 50% ± 5%)		40	50	60	%	3,5
Output Rise Time	t_{OR}		2.0	2.5	ns	8,10
Output Fall Time	t_{OF}		2.0	2.5	ns	8,10
Power-up Time	t_{PU}			100	ms	
Period	Period	Table 2	Table 2	Table 2	ns	

CAPACITANCE

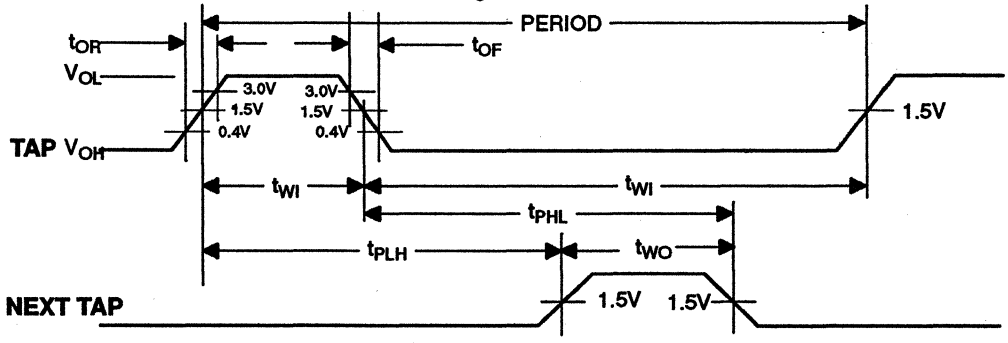
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	10

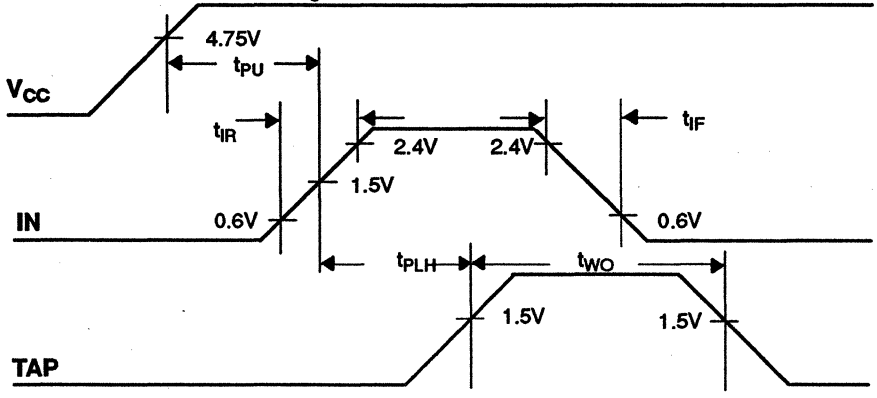
NOTES

1. All voltages are reference to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C.
4. Temperature variations from 25°C to 0°C or 70°C may produce an additional tap-to-tap delay shift of ± 0.5ns. Voltage variations from 5.0V to 4.75V or 5.25V produce a worst case tap-to-tap delay shift of 5%.
5. All tap-to-tap delays vary unidirectionally over temperature or voltage range. For example, if the TAP 1 - TAP 2 delay, t_{PLH}, slows down, the TAP2 - TAP 4 delay, t_{PLH}, will also slow down. Since t_{PHL} tracks t_{PLH}, symmetry is preserved.
6. See "Test Conditions" section at the end of this data sheet.
7. Since all four taps have identical output stages, tap-to-tap delays and waveform symmetry will exhibit minimal variation when capacitive loading is increased identically on all taps at the same time (e.g., the addition of one or more RISC coprocessors).
8. V_{CC} = Min; C_L = 30 pF
9. Trailing edge delays, t_{PHL}, are adjusted to maintain waveform symmetry.
10. Guaranteed by design. Periodically tested.

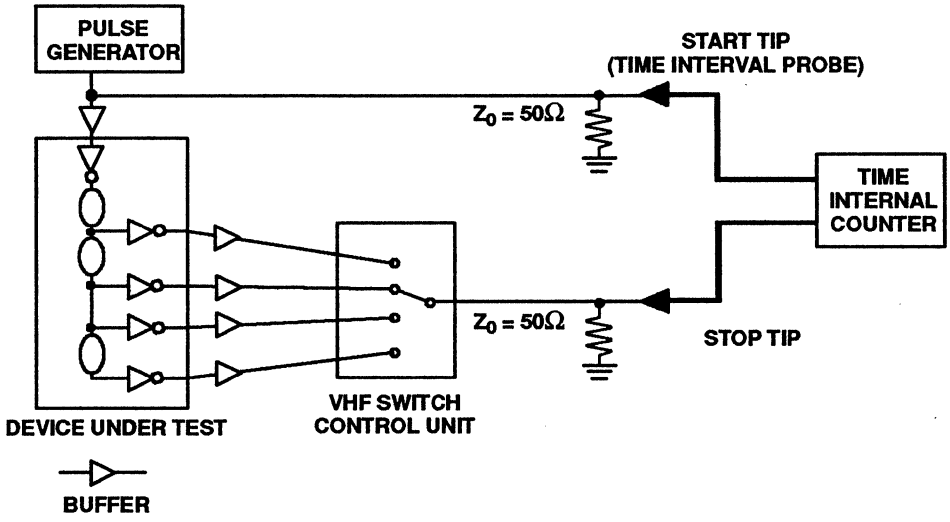
TIMING DIAGRAM - SILICON DELAY LINE Figure 2



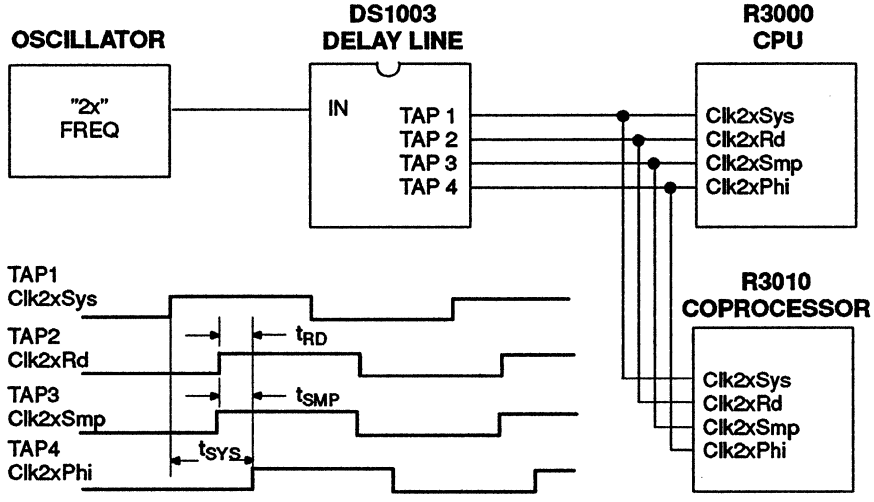
POWER-UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TYPICAL APPLICATION Figure 5



NOTE: TAP 2 can be used for Clk2xSmp with TAP 3 as Clk2xRd.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following pulse.

Symmetry: That percent of the Period when the input or output is above 1.5V.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{IR} (Input Rise Time): The elapsed time between 0.6V and 2.4V on the leading edge of the input pulse.

t_{IF} (Input Fall Time): The elapsed time between 2.4V and 0.6V on the trailing edge of the input pulse.

t_{OR} (Output Rise Rime): The elapsed time between 0.4V and 3.0V on the leading edge of the output pulse.

t_{OF} (Output Fall Time): The elapsed time between 3.0V and 0.4V of the trailing edge output pulse.

t_{PLH} (Time Delay, Rising): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the leading edges.

t_{PHL} (Time Delay, Falling): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the trailing edges.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications are within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1003. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution connected between the input and each tap). Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns
Period:	1000 ns

Output:

Each output is loaded with the equivalent of one 74F04 input. Delays are measured at the 1.5V level.

Note:

Above conditions are for test only. The adjusted test limits and guardbands used assure operation to data sheet timing specifications.

DALLAS SEMICONDUCTOR

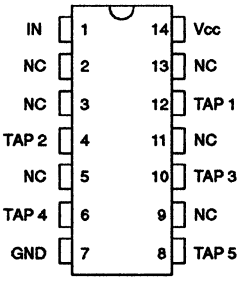
DS1005
5-Tap Silicon Delay Line

2

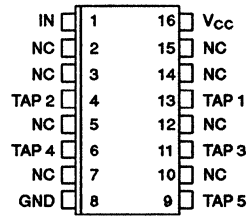
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

PIN ASSIGNMENT

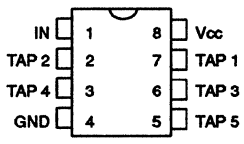


DS1005 14-PIN DIP (300 MIL)
DS1005G 14-PIN GULLWING (300 MIL)
DS1005K 14-PIN SHEARED NC
See Mech. Drawings
Sect. 16, Pgs. 1 & 3



DS1005S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

Also Available
In Die Form



DS1005M 8-PIN DIP (300 MIL)
DS1005H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Sect. 16, Pgs. 1 & 3

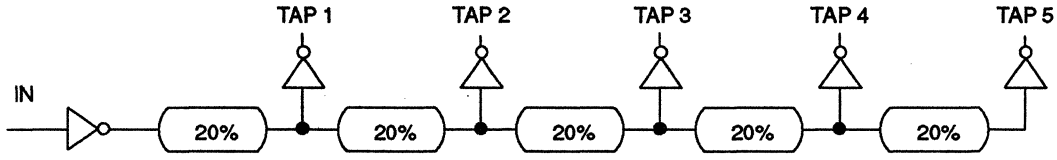
PIN DESCRIPTION

TAP 1 – TAP 5	- Tap Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ± 2 ns or ± 3%, whichever is greater. This device is offered in a standard 14-pin DIP making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. The 14-pin DIP and 8-pin DIP are available in a surface mountable gullwing construction. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1005-60	12ns	24ns	36ns	48ns	60ns
DS1005-75	15ns	30ns	45ns	60ns	75ns
DS1005-100	20ns	40ns	60ns	80ns	100ns
DS1005-125	25ns	50ns	75ns	100ns	125ns
DS1005-150	30ns	60ns	90ns	120ns	150ns
DS1005-175	35ns	70ns	105ns	140ns	175ns
DS1005-200	40ns	80ns	120ns	160ns	200ns
DS1005-250	50ns	100ns	150ns	200ns	250ns

Custom delays available

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	u A	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min. V_{OL} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns or ±3%, whichever is greater.
4. See Test Conditions.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional input-to-tap delay shift of ± 1.5ns or ± 4%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.
7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature	25°C ± 3°C
Supply Voltage (V_{CC})	5.0V ± 0.1V
Input Pulse	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance	50 ohm maximum
Rise and Fall Time	3.0 ns maximum
Pulse Width	500 ns
Period	1us

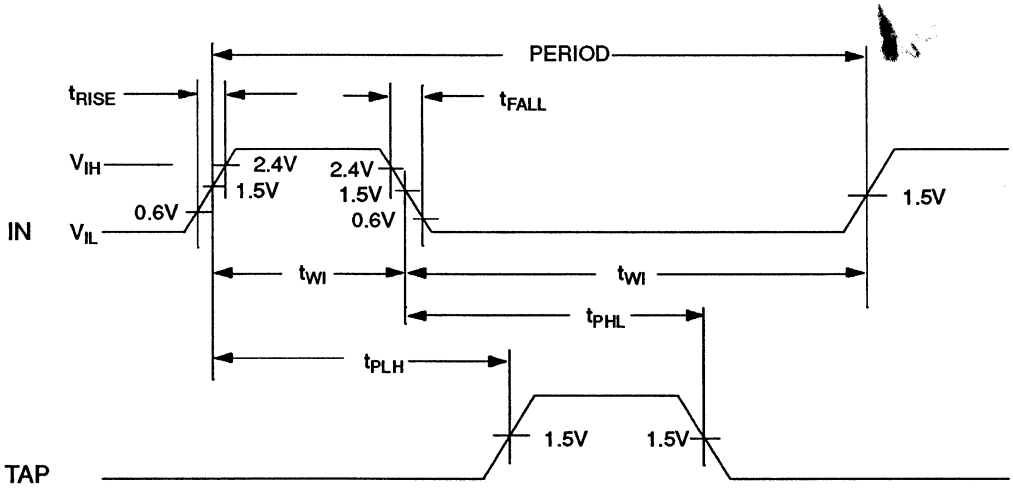
OUTPUT:

Each output is loaded with the equivalent of a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

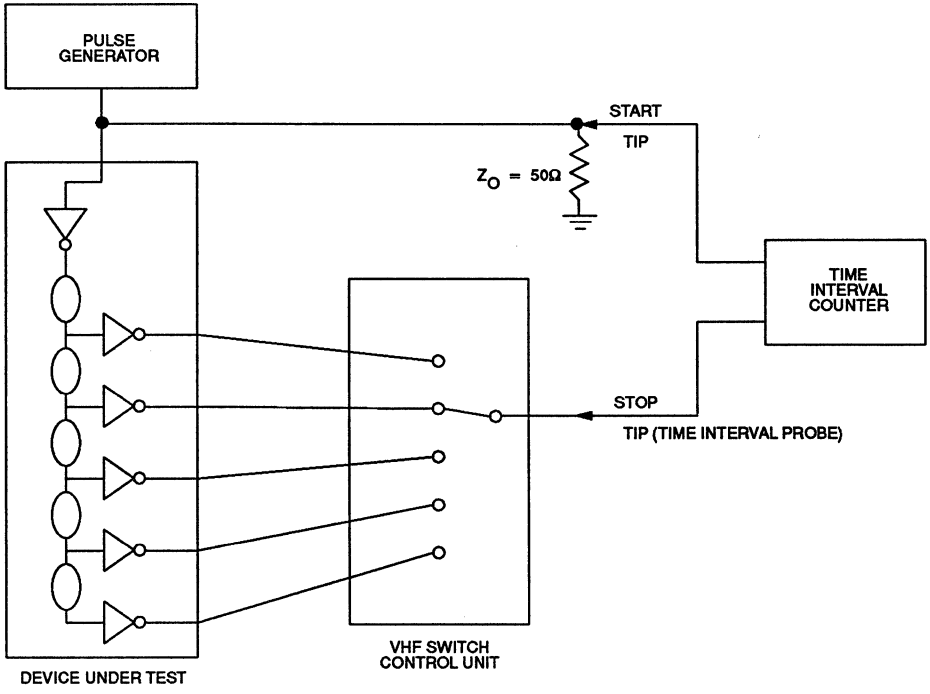
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



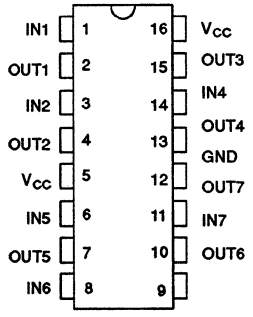
DALLAS SEMICONDUCTOR

DS1007
7-in-1 Silicon Delay Line

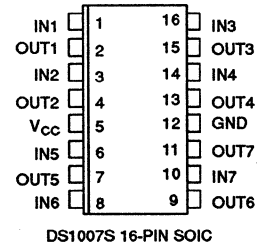
FEATURES

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance ±2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1007 16-PIN DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



DS1007S 16-PIN SOIC
(300 MIL)
See Mech. Drawing Sect. 16, Pg. 6

Also Available
In Die Form

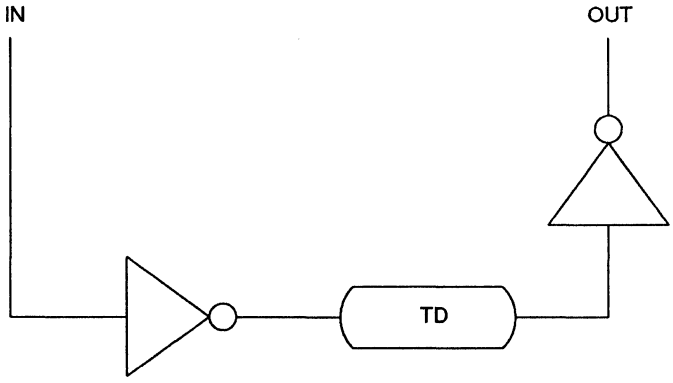
PIN DESCRIPTION

IN1 - IN7	- Inputs
Out1- Out7	- Outputs
GND	- Ground
V_{CC}	- +5 Volts

DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of ±2 ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic state at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



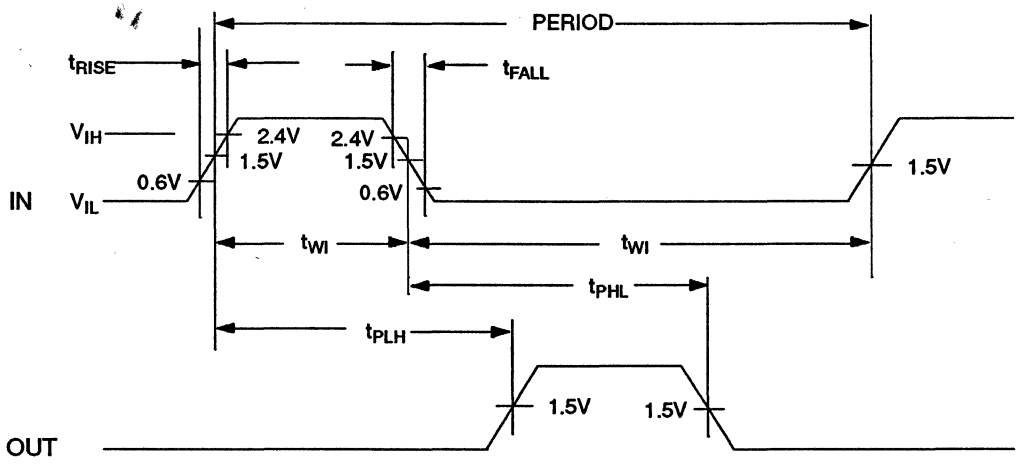
PULSE WIDTH > 100% OF DELAY

PART NUMBER DELAY TABLE (t_{PLH}) Table 1

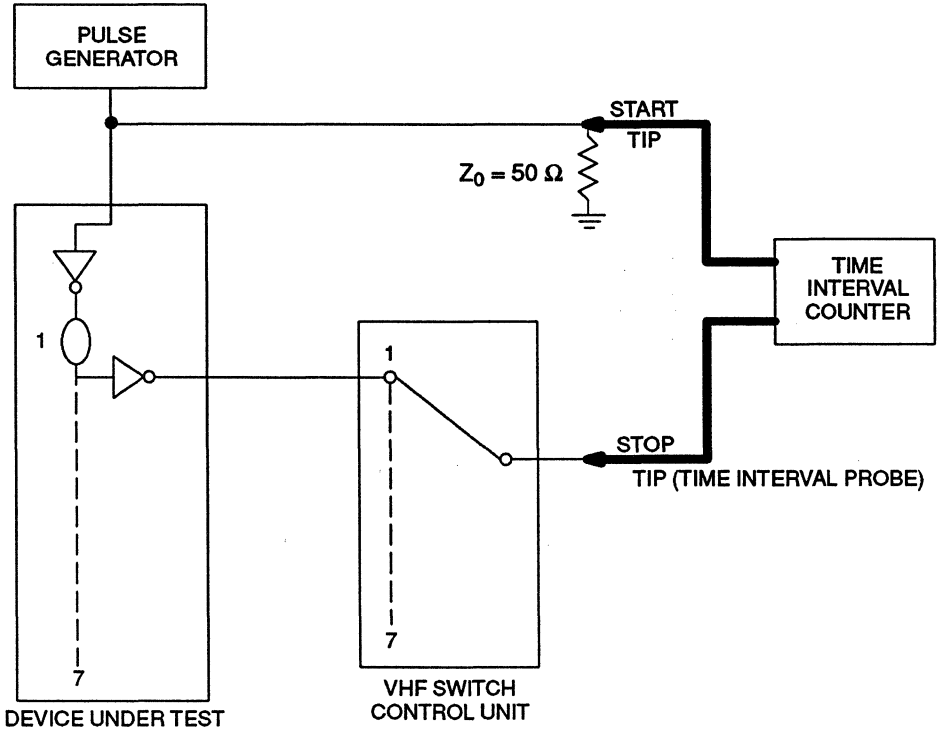
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	7	7	7	25	25	25
DS1007-8	8	8	8	8	30	30	30
DS1007-9	9	9	9	9	35	35	35
DS1007-10	10	10	10	10	40	40	40
DS1007-11	3	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10ns. (Leading edge only accuracy.)
Out 5 through Out 7 can be custom set from 9 to 40ns. (Both leading and trailing edge accuracy.)

TIMING DIAGRAM SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}= Min. V_{OL}= 0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A= 25°C, V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5
Power-up Time	t_{PU}			100	ms	7
	Period	3 (t_{WI})			ns	6

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @2 5°C. Delays accurate on rising edges within ±2 ns.
4. See Test Conditions below.
5. All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if OUT 2 slows down, all other outputs also slow down).
6. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
7. t_{PU} = 0 ms for OUT 1 through OUT 4.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge, and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

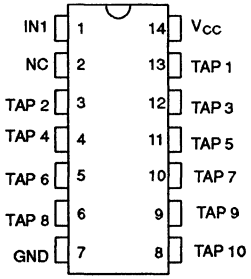
DS1010
10-Tap Silicon Delay Line

2

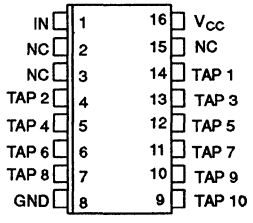
FEATURES

- All-silicon time delay
- 10 taps equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1010 14-PIN DIP
(300 MIL)
DS1010G 14-PIN GULLWING
(300 MIL)
See Mech. Drawings
Sect. 16, Pgs. 1 & 3



DS1010S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

Also Available In Die Form

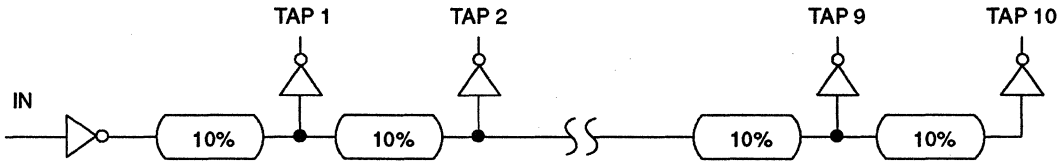
PIN DESCRIPTION

TAP 1-TAP 10	– Tap Output Number
V_{CC}	– 5 Volts
GND	– Ground
NC	– No Connection
IN	– Input

DESCRIPTION

The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces PC board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1010 reproduces the input logic state at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (ns)
DS1010-50	50	5
DS1010-60	60	6
DS1010-75	75	7.5
DS1010-80	80	8
DS1010-100	100	10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-450	450	45
DS1010-500	500	50

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=Max: Period=Min.		40	150	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 10 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6,7,9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6,7,9
Power-up Time	t_{PU}			100	ms	
	Period	4(t_{WI})			ns	8

CAPACITANCE

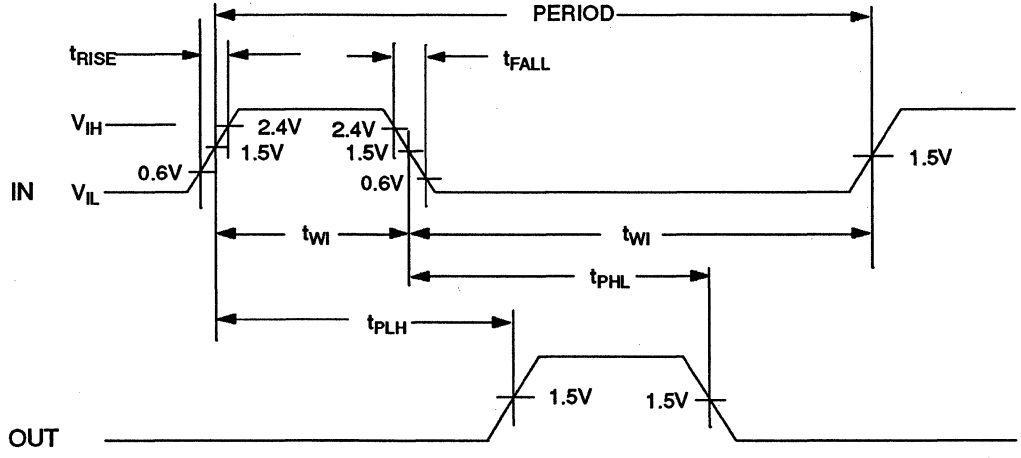
(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

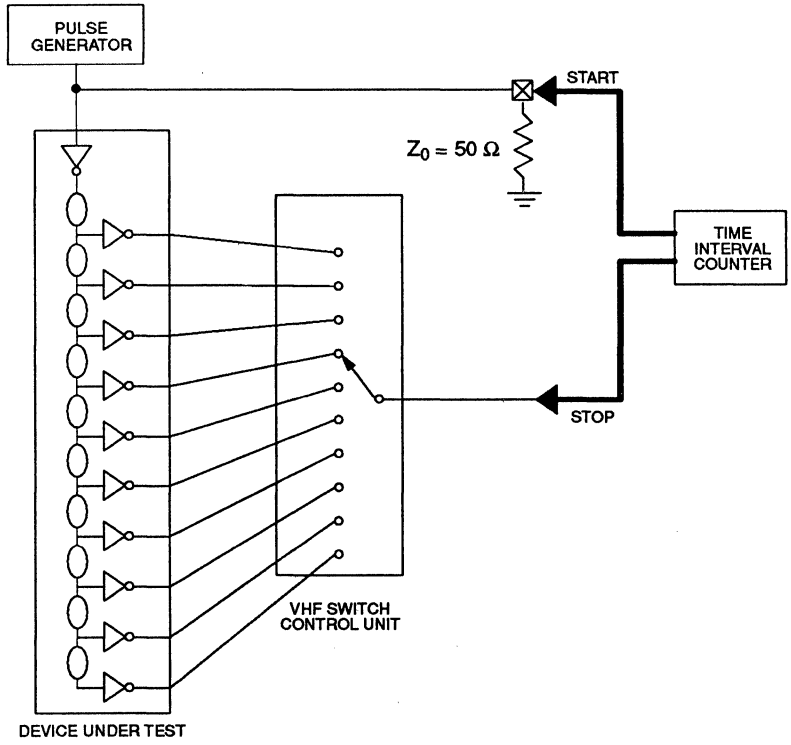
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Input-to-tap delays accurate on both rising and falling edges within ±2 ns or ±5% whichever is greater.
4. See "Test Conditions" section.
5. For DS1010 delay lines with a TAP 10 delay of 100 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±2ns or ±3%, whichever is greater.
6. For DS1010 delay lines with a TAP 10 delay less than 100 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±1ns or ±9%, whichever is greater.
7. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps will also slow dow; TAP 3 can never be faster than TAP 2.
8. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
9. Certain high-frequency applications not recommended for -50 in 16-pin package. Consult factory.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns (1µs for -500)
Period:	1µs (2µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

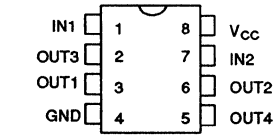
DS1012
2-in-1 Sub-Miniature Silicon Delay Line with Logic

2

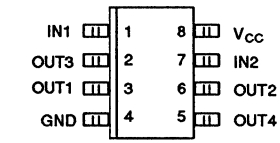
FEATURES

- All-silicon time delay
- 53 µW max. CMOS quiescent mode
- Surface mount 8-pin mini-SOIC and standard 8-pin DIP
- 2 independent buffered delays per input
- Option of complemented output(s)
- Option of timed AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR logic outputs
- Delay tolerance: ±1.5 ns (delays: 3-10 ns), ±2.0 ns (delays: 11-40 ns)
- Vapor phase, IR and wave solderability
- Economical
- TTL/CMOS-compatible
- Quick turn prototypes
- Custom delays and logic options available

PIN ASSIGNMENT



DS1012 8-PIN DIP (300 MIL)
DS1012H 8-PIN GULLWING
See Mech. Drawing – Sect. 16, Pgs. 1 & 3



DS1012Z 8-PIN SOIC (150 MIL)
See Mech. Drawing – Sect. 16, Pg. 5

Also Available In Die Form

PIN DESCRIPTION

IN1, IN2	Inputs
OUT1, OUT2	Outputs (delays)
OUT3, OUT4	Outputs (delays, logic)
GND	Ground
VCC	+5 volts

DESCRIPTION

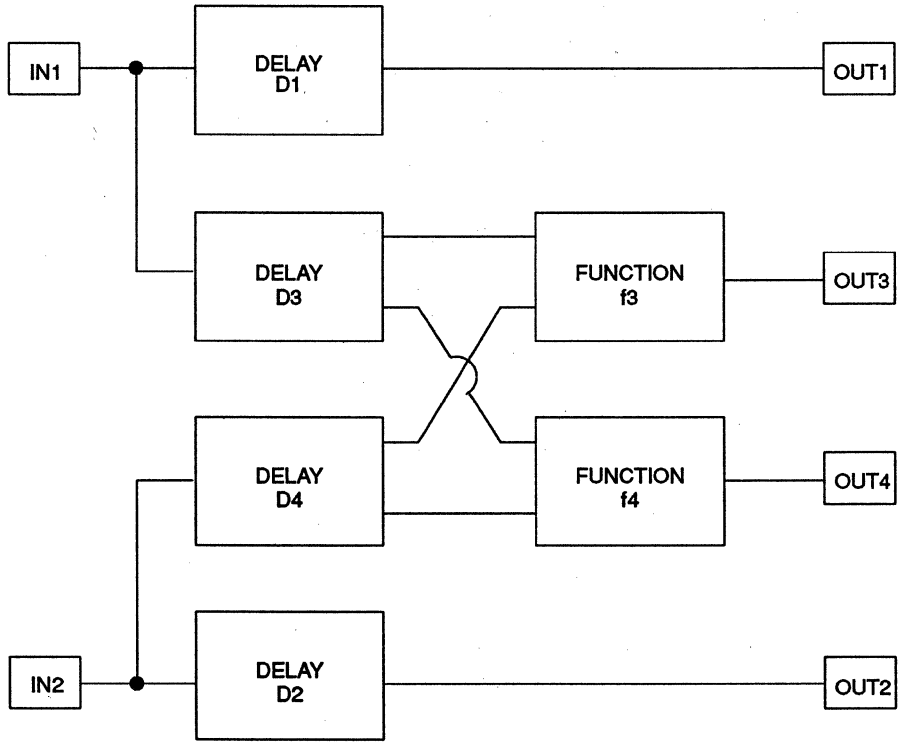
In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. Any of the four outputs can be inverted at the time of manufacture. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration.

For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 and $\overline{D4}$), or NOT HALF-XOR ($\overline{D3}$ OR D4) can be substituted for the simple delay on OUT3. DS1012-2, DS1012-4, and DS1012-5 are examples of catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In any configuration, delays D1 (t_{D1}) and D2 (t_{D2}) can be specified within the range of ~3 ns to 10 ns. Delays D3 (t_{D3}) and D4 (t_{D4}) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is ±2 ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



Function f3 can be one of the following:

D3	$\overline{D3}$
D3 AND D4	D3 NAND D4
D3 HALF-XOR D4	D3 HALF-XNOR D4

Function f4 can be one of the following:

D4	$\overline{D4}$
D3 OR D4	D3 NOR D4
D3 XOR D4	D3 XNOR D4

NOTE: Any output(s) can be inverted at time of manufacture.
If D1 > 10 ns, D1 = D3.
If D2 > 10 ns, D2 = D4.

2

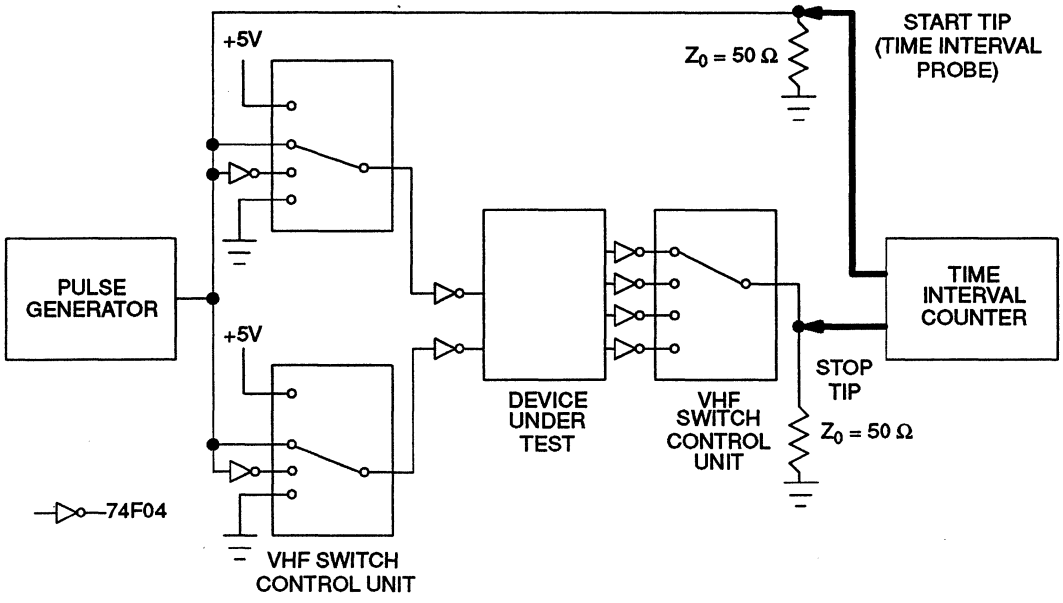
PART NUMBER DELAY AND CONFIGURATION Table 1

CATALOG P/N	t_{D1} (ns)	t_{D2} (ns)	t_{D3} (ns)	t_{D4} (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	5	10	10	D1	$\overline{D2}$	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4
DS1012-7	15	4	4	14	D1	$\overline{D2}$	D3	D3XD4
DS1012-D16	4	19.6	4	19.6	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D20	4	16.5	4	16.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D25	4	14	4	14	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D33	4	11.5	4	11.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D50	4	9	4	9	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V20	25	50	25	50	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$
DS1012-V40	12.5	25	12.5	25	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V50	10	20	10	20	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V60	8.3	8.3	8.3	8.3	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$

NOTE: . = AND, + = OR, X = XOR, HX = HALF–XOR

Contact Dallas Semiconductor for information on custom configurations and timing delays.

TEST CIRCUIT Figure 2



TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters on the DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	50 ns
Period:	100 ns

OUTPUT:
Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE: These conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0° to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC1}	V_{CC} = MAX; PERIOD = MIN		40.0	70.0	mA	2
Quiescent Current	I_{CC2}	V_{CC} = MAX.			10	µA	5
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8.0			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC} = 5V ± 5%)

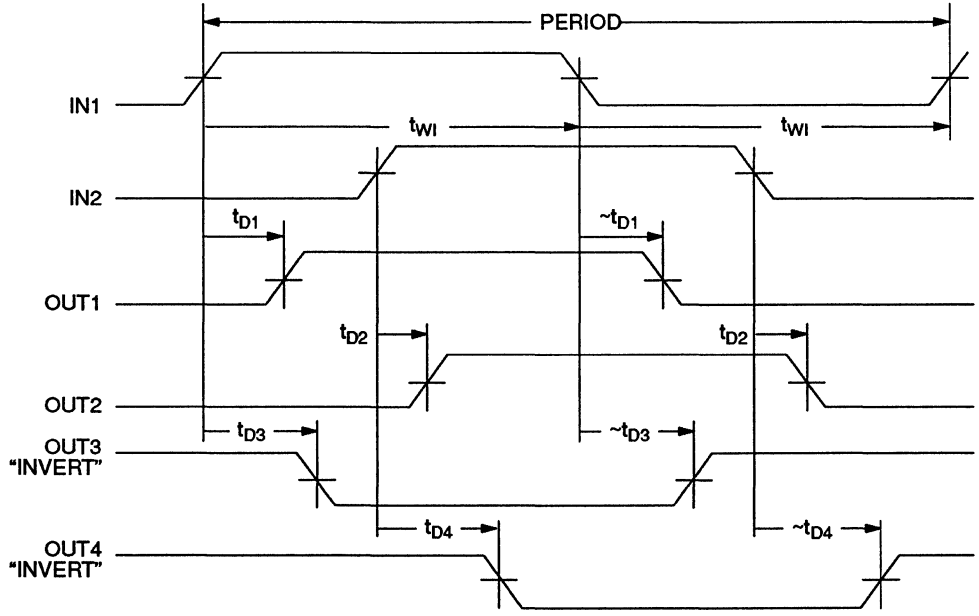
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	6
Input to Output (leading edge)	t_{D1}, t_{D2}, t_{D3}, t_{D4}				ns	3, 4
Power-up Time	t_{PU}			0	ns	7
	Period	2(t_{WI})			ns	

CAPACITANCE

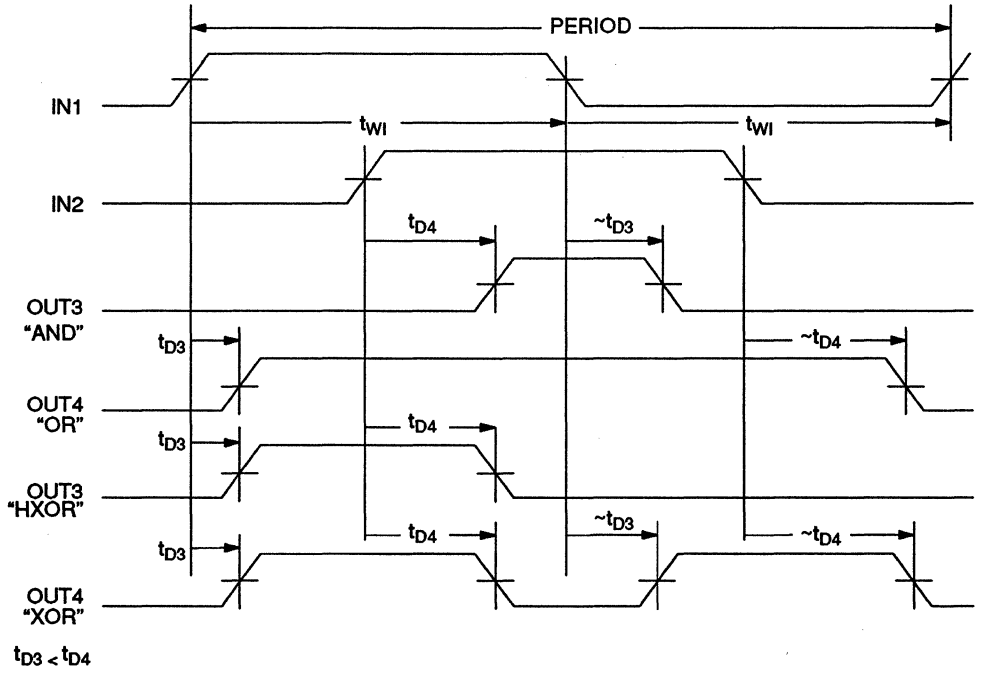
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

DELAY FUNCTION Figure 3



LOGIC FUNCTIONS Figure 4



NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period. I_{CC1} (max.) for any value of Period can be calculated using the formula:

   I_{CC1} (max.) in mA = 840 mA-ns/Period (in ns) + I_{CC2} in mA

   Example: If Period = 50 ns then

   ICC1 (Max) in mA = 840 mA-ns/50 ns + 0.01 mA = 16.81 mA
3. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
4. See the section entitled "Test Conditions."
5. For the quiescent mode, both inputs must meet the conditions
   $0.3V > V_I$ or $VI > V_{CC} - 0.3$
6. For specified accuracy, T_{WI} (min) is the longer of $3(t_{D1})$, $3(t_{D2})$, $3(t_{D3})$, or $3(t_{D4})$. Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., $2(T_{WI})$ = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when T_{WI} is longer than t_{D1}, t_{D2}, t_{D3}, and t_{D4}.
7. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.

DALLAS SEMICONDUCTOR

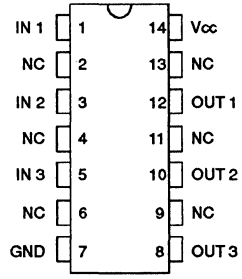
DS1013
3-in-1 Silicon Delay Line

2

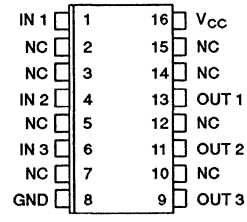
FEATURES

- All-silicon time delay
- 3 independent buffered delays
- Delay tolerance ±2ns for -10 through -65
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy on -15 through -150
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Quick turn prototypes
- Extended temperature ranges available

PIN ASSIGNMENT

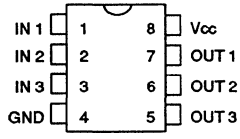


DS1013 14-PIN DIP (300 MIL)
DS1013G 14-PIN GULLWING (300 MIL)
DS1013K 14-PIN SHEARED NC
See Mech. Drawings
Sect. 16, Pgs. 1 & 3



DS1013S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

Also Available
In Die Form



DS1013M 8-PIN DIP (300 MIL)
DS1013H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Sect. 16, Pgs. 1 & 3

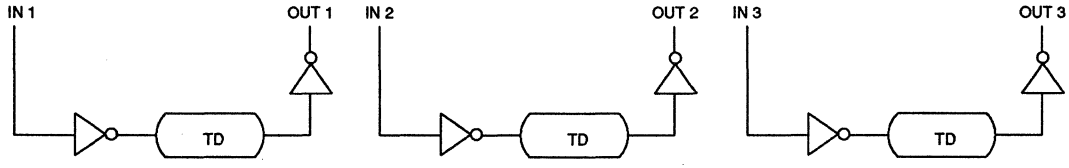
PIN DESCRIPTION

IN 1, IN 2, IN 3	– Inputs
OUT 1, OUT 2, OUT 3	– Outputs
GND	– Ground
V_{CC}	– +5 Volts
NC	– No Connection

DESCRIPTION

The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of ±2ns for delay times ranging from 10 ns to 65 ns, increasing to 5% for delays of 150 ns. The DS1013 delay line reproduces the input logic state at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH},) Table 1

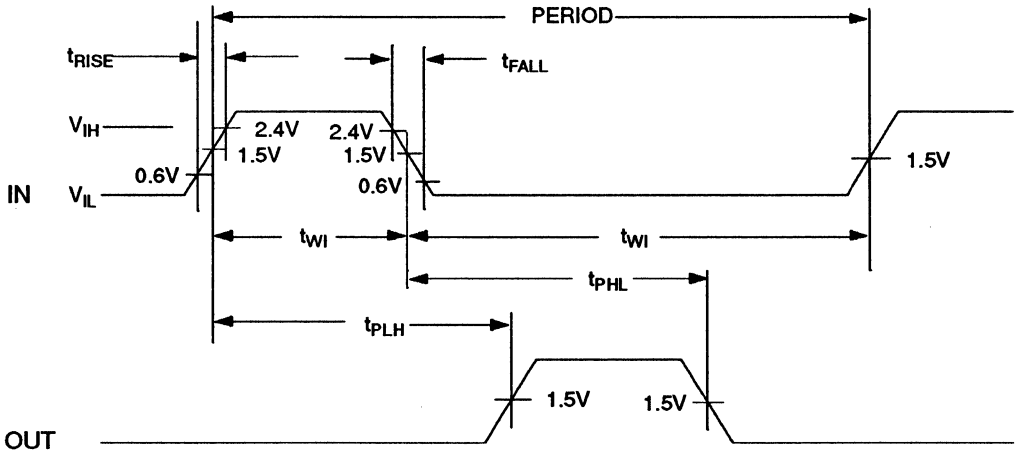
PART NO.	DELAY PER OUTPUT (ns)
DS1013-10*	10/10/10
DS1013-12*	12/12/12
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-35	35/35/35
DS1013-40	40/40/40
DS1013-45	45/45/45
DS1013-50	50/50/50
DS1013-55	55/55/55
DS1013-60	60/60/60
DS1013-65	65/65/65
DS1013-70**	70/70/70
DS1013-75**	75/75/75
DS1013-80**	80/80/80
DS1013-90**	90/90/90
DS1013-100**	100/100/100
DS1013-150***	150/150/150
DS1013–200***	200/200/200

*Leading edge accuracy only.
Custom delays available.

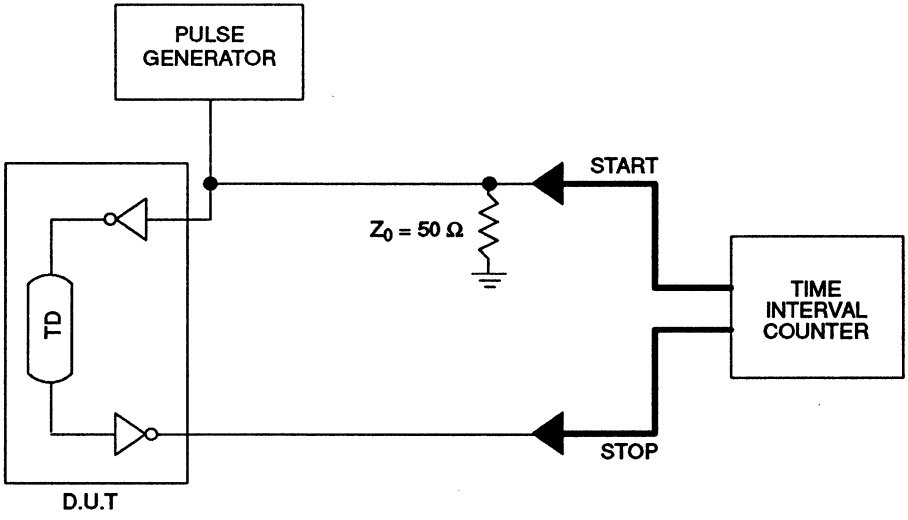
** ±3% tolerance.

*** ±5% tolerance.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V ≤ VI ≤ V_{CC}	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}= Max Period= Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 4.0V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A= 25°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Output Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	3(t_{WI})			ns	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns for -15 to -65, ±3% for -70 to -100 and ±5% for -150 and longer delays. Delays accurate on rising edge only within ±2 ns for -10 and -12.
4. See "Test Conditions" section.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional delay shift of ± 1.5 ns or ± 3%, whichever is greater.
6. All output delays tend to vary unidirectionally over temperature or voltage ranges (i.e., if OUT 1 slows down, all other outputs also slow down).
7. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between each input and corresponding output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1us

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

PRELIMINARY

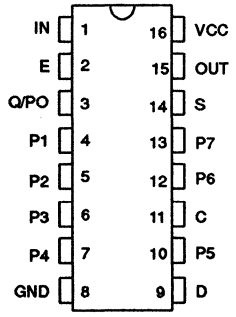
DALLAS SEMICONDUCTOR

DS1020
Programmable 8-Bit Silicon Delay Line

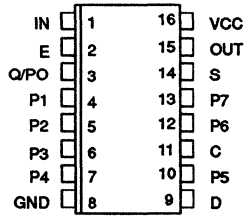
FEATURES

- All-silicon time delay
- Models with 0.25 ns, 0.5 ns, 1 ns, and 2 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Standard 16-pin DIP or 16-pin SOIC
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Extended temperature range available

PIN ASSIGNMENT



DS1020 16-PIN DIP
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



DS1020 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

IN	Delay Input
P0-P7	Parallel Program Pins
GND	Ground
OUT	Delay Output
VCC	+5 Volts
S	Mode Select
E	Enable
C	Serial Port Clock
Q	Serial Data Output
D	Serial Data Input

DESCRIPTION

The DS1020 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The fastest model (-025) offers a maximum delay of 73.75ns with an incremental delay of 0.25ns, while the slowest model (-200) has a maximum delay of 520ns with an incremental delay of 2ns. All models have an inherent (step zero) delay of 10ns. After the user-determined delay, the input logic state is reproduced at the output without inversion. The DS1020 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1020 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1020 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

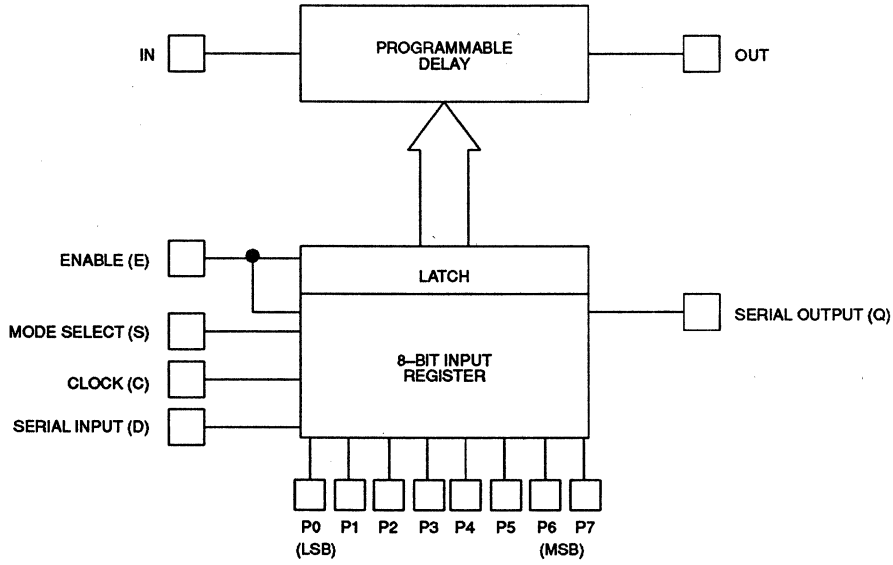
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1020 to the serial input of a second DS1020, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1020 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

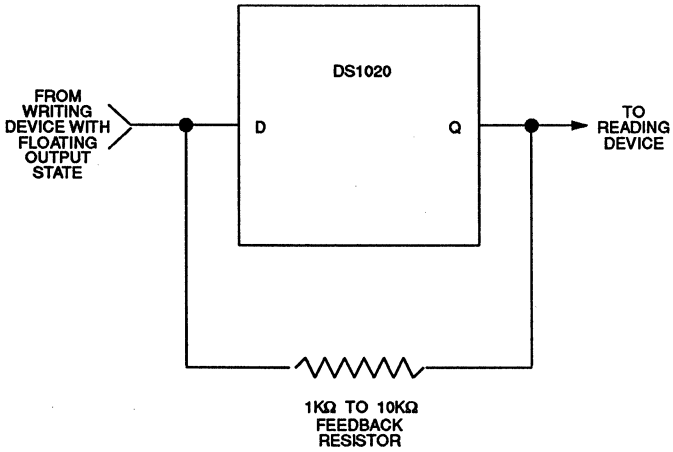
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1020 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

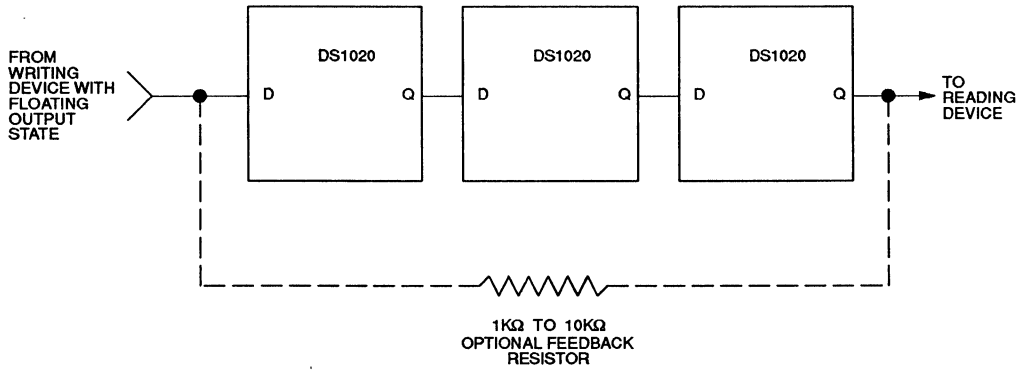
FUNCTION BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

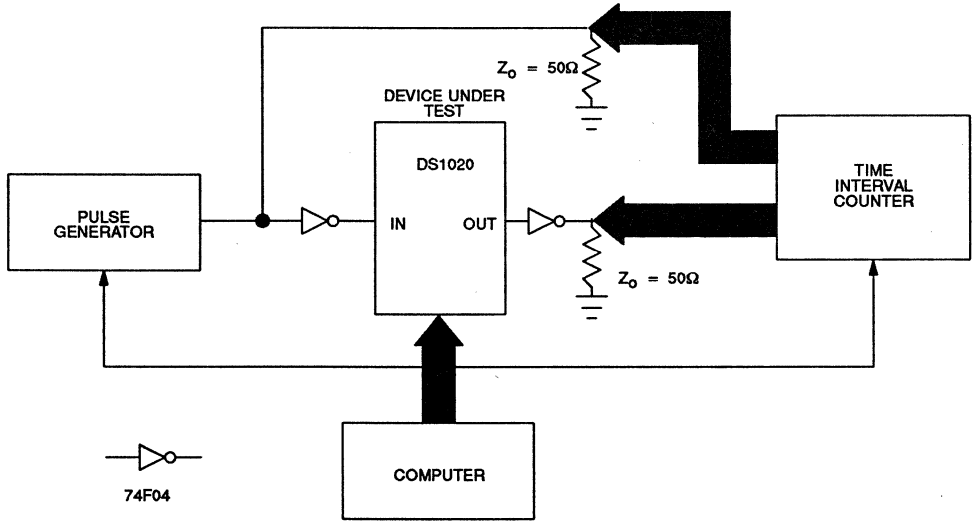
DELAYS AND TOLERANCES (IN ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1020-025	10 ± 2	73.75	0.25	±6
DS1020-050	10 ± 2	137.5	0.5	±8
DS1020-100	10 ± 2	265	1	±20
DS1020-200	10 ± 3	520	2	±40

DELAY VS. PROGRAMMED VALUE Table 2

	STEP ZERO						MAX DELAY			PARALLEL PORT	SERIAL PORT
BINARY	0	0	0	0	0	0	1	1	1	P7	MSB
PROGRAMMED	0	0	0	0	0	0	1	1	1	P6	
VALUE	0	0	0	0	0	0	1	1	1	P5	
	0	0	0	0	0	0	1	1	1	P4	
	0	0	0	0	0	0	1	1	1	P3	
	0	0	0	0	1	1	1	1	1	P2	
PART	0	0	1	1	0	0	0	1	1	P1	
NUMBER	0	1	0	1	0	1	1	0	1	P0	LSB
DS1020-025	10.00	10.25	10.50	10.75	11.00	11.25	73.25	73.50	73.75		
DS1020-050	10.0	10.5	11.0	11.5	12.0	12.5	136.5	137.0	137.5		
DS1020-100	10	11	12	13	14	15	263	264	265		
DS1020-200	10	12	14	16	18	20	516	518	520		

All delays in nanoseconds, referenced to input pin.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1020. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1020 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (DS1020-025)
	2 µs (DS1020-050)
	4 µs (DS1020-100)
	4 µs (DS1020-200)
Period:	1 µs (DS1020-025)
	4 µs (DS1020-050)
	8 µs (DS1020-100)
	8 µs (DS1020-200)

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = MAX; PERIOD = 1 µs			30.0	mA	3
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	12.0			mA	

AC ELECTRICAL CHARACATERISTICS

(0°C to 70°C, V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	
Clock Width	t_{CW}	50			ns	
Data Setup to Clock	t_{DSC}	30			ns	
Data Hold from Clock	t_{DHC}	10			ns	
Data Setup to Enable	t_{DSE}	30			ns	
Data Hold from Enable	t_{DHE}	10			ns	
Enable to Serial Output Valid	t_{EQV}			50	ns	
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	
Clock to Serial Output Valid	t_{CQV}			50	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	

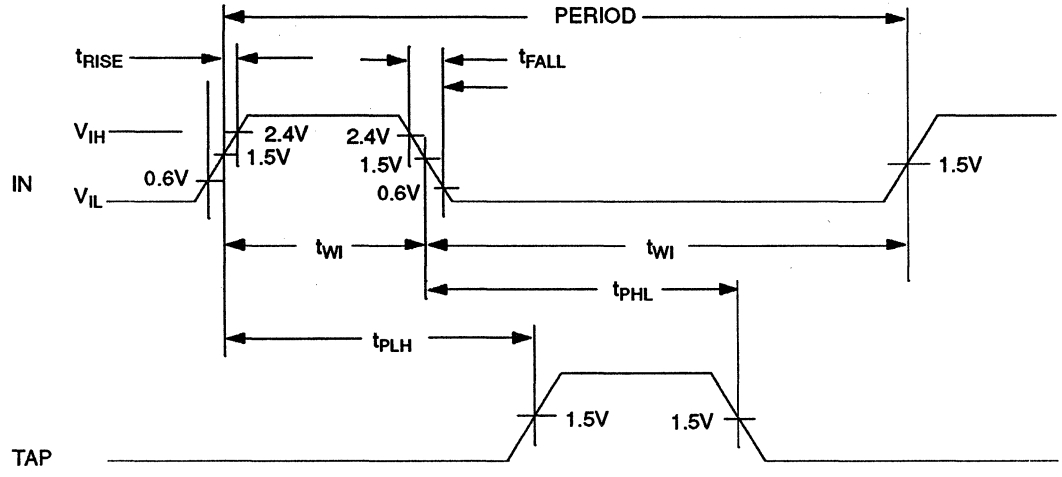
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Enable Setup to Clock	t_{ES}	50			ns	
Enable Hold from Clock	t_{EH}	50			ns	
Parallel Input Valid to Delay Valid	t_{PDV}			50	µs	
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}			50	µs	
Enable to Delay Invalid	t_{EDX}	0			ns	
V_{CC} Valid to Device Functional	t_{PU}			100	ms	
Input Pulse Width	t_{WI}	100% of Output Delay			ns	
Input to Output Delay	t_{PLH}, t_{PHL}		Table 2		ns	2
Input Period	Period	$3(t_{WI})$			ns	4

CAPACITANCE

($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TIMING DIAGRAM: SILICON DELAY LINE Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

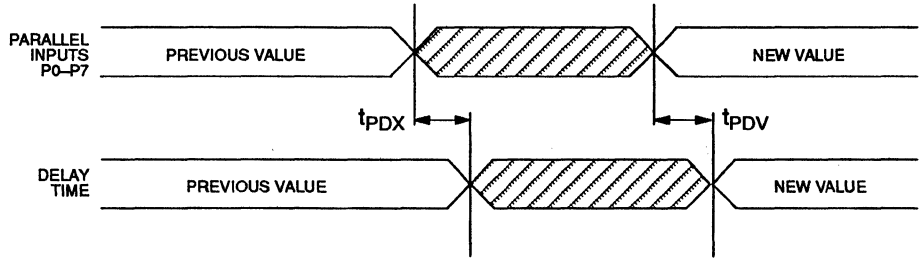
t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

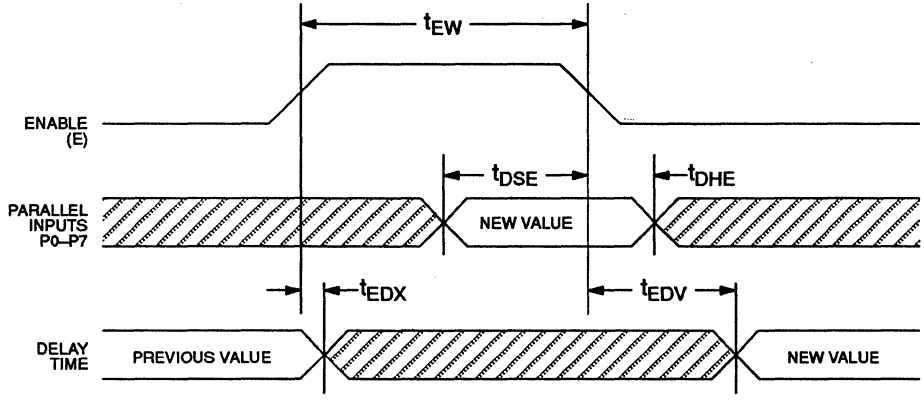
t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

2

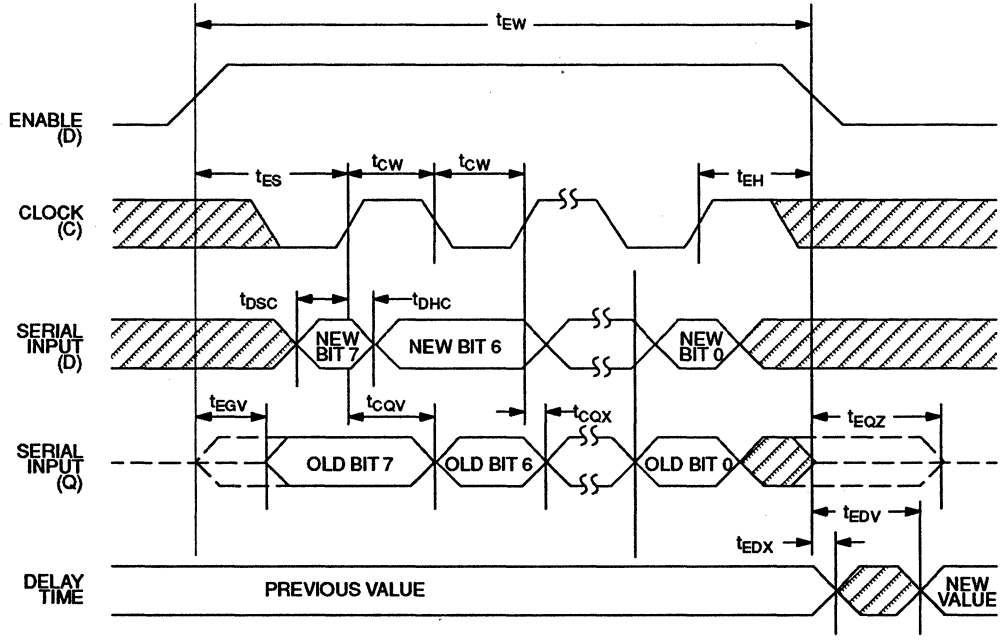
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



NOTES

1. All voltages are referenced to ground.
2. @V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.
3. Measured with output open.
4. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

DALLAS SEMICONDUCTOR

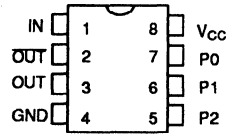
DS1040
Programmable One-Shot Pulse Generator

2

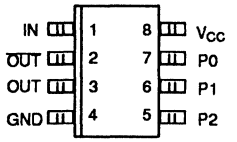
FEATURES

- All-silicon pulse width generator
- Five programmable widths
- Equal and unequal increments available
- Maximum pulse widths from 50 ns to 500 ns
- Widths are stable and precise
- Rising edge-triggered
- Inverted and non-inverted outputs
- Width tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom widths available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1040M 8-PIN DIP (300 MIL)
DS1040H 8-PIN GULLWING (300 MIL)
See Mech. Drawings – Sect. 16, Pg. 1 & 3



DS1040Z 8-PIN SOIC (150 MIL)
See Mech. Drawing – Sect. 16, Pg. 5

Also Available In Die Form

PIN DESCRIPTION

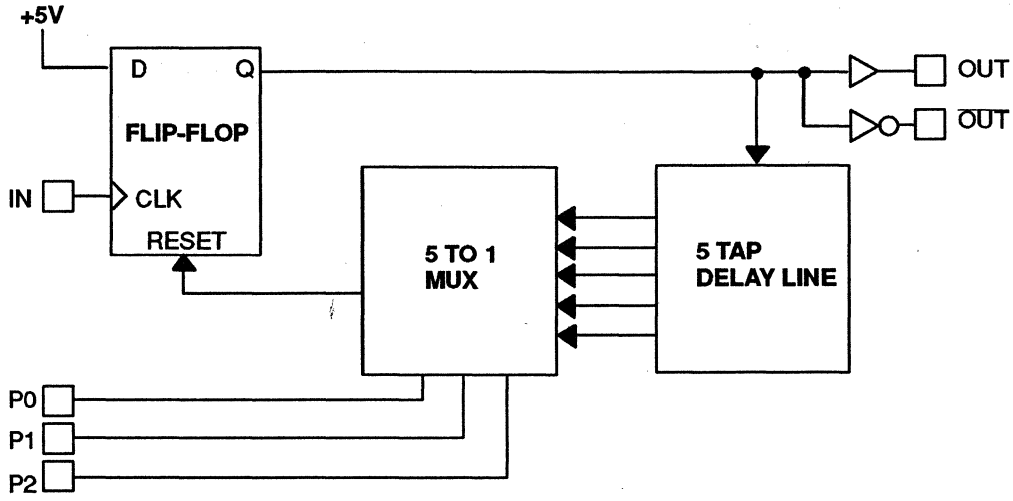
IN	Trigger Input
P0-P2	Programming Pins
GND	Ground
OUT	Pulse Output
$\overline{OUT}$	Inverted Pulse Output
V_{CC}	+5V

DESCRIPTION

The DS1040 Pulse Generator is a user-programmable one-shot with a choice of five precise pulse widths. Maximum widths range from 50 ns to 500 ns; increments range from 2.5 ns to 100 ns. For maximum flexibility in applications such as magneto-optical read/write disk laser power control, varieties are offered with equal and unequal increments. The DS1040 is offered in standard 8-pin DIPs and 8-pin mini-SOICs. Low cost and superior reliability over hybrid technology are achieved by the combination of a 100% CMOS silicon design and industry standard packaging. The DS1040 series of pulse generators provide a nominal width accuracy of ± 5% or ± 2 ns, whichever is greater. In response to the rising edge of the input (trigger) pulse, the DS1040 produces an output pulse with a width determined by the logic states of the three parallel programming pins. For convenience, both inverting and non-inverting outputs are supplied. The intrinsic delay between the trigger pulse and the output pulse is no more than 10ns. Each output is capable of driving up to five 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special request and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PULSE WIDTH VS. PROGRAMMED VALUE Table 1

	PROGRAMMING PINS	MAX WIDTH	MIN WIDTH →				MAX WIDTH	MAX WIDTH	MAX WIDTH
	MSB P2	0	0	0	0	1	1	1	1
	P1	0	0	1	1	0	0	1	1
	LSB P0	0	1	0	1	0	1	0	1
PART NUMBER									
DS1040-75		75	15	30	45	60	75	75	75
DS1040-100		100	20	40	60	80	100	100	100
DS1040-150		150	30	60	90	120	150	150	150
DS1040-200		200	40	80	120	160	200	200	200
DS1040-250		250	50	100	150	200	250	250	250
DS1040-500		500	100	200	300	400	500	500	500
DS1040-B50		50	30	35	40	45	50	50	50
DS1040-D60		60	20	30	40	50	60	60	60
DS1040-A15		15	5	2.5	10	12.5	15	15	15
DS1040-A20		20	10	12.5	15	17.5	20	20	20
DS1040-A32		32.5	22.5	25	27.5	30	32.5	32.5	32.5
DS1040-B40		40	20	25	30	35	40	40	40
DS1040-D70		70	30	40	50	60	70	70	70

All times in nanoseconds.
Custom pulse widths available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min		35	75	mA	2,6
High Level Output Current	I_{OH}	V_{CC} = Min V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OL} = 0.5	8			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Setup	t_{PS}	5			ns	
Programming Hold	t_{PH}	0			ns	
Input Pulse Width at Logic 1	t_{WIH}	5			ns	
Input Pulse Width at Logic 0	t_{WIL}	5			ns	
Intrinsic Delay	t_D	0	5	10	ns	
Output Pulse Width	t_{WO}		Table 1		ns	3,4,5,7
Power-up Time	t_{PU}			100	ms	
Period	Period	t_{WO} + 50			ns	

CAPACITANCE

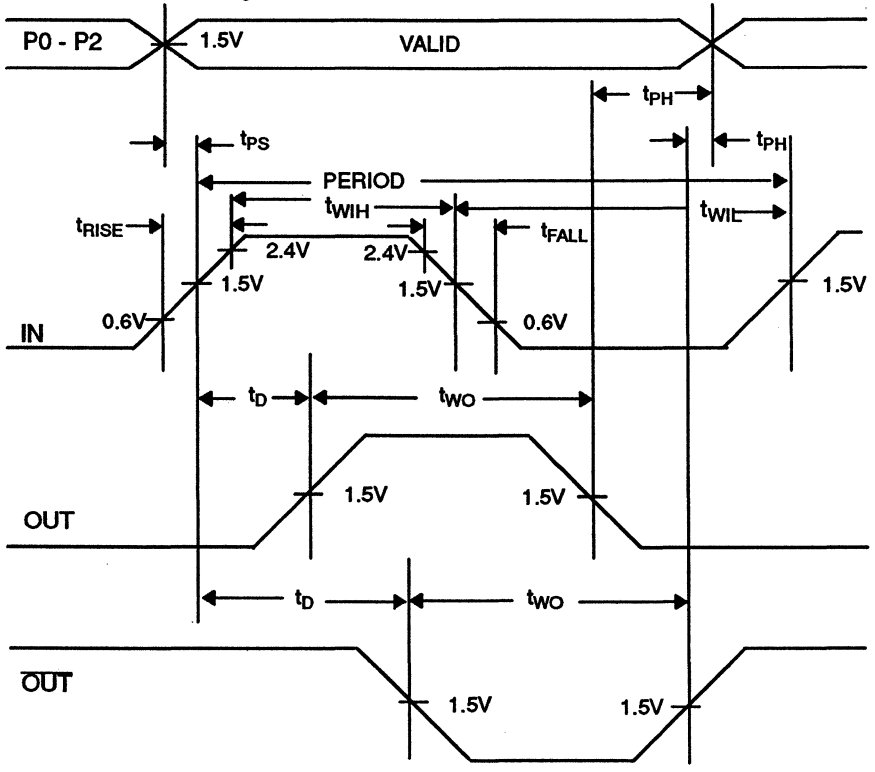
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

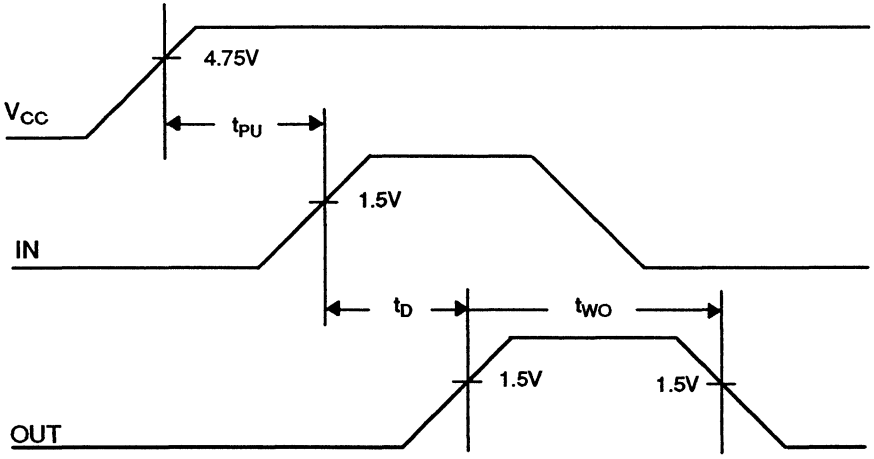
NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C. Width accurate to within ± 2 ns or 5%.
4. Temperature variations between 0°C and 70°C may increase or decrease width by an additional ± 1 ns or ± 3%, whichever is greater.
5. For DS1040 pulse generators with maximum widths less than 50ns, temperature variations between 0°C and 70°C may increase or decrease width by ± 1ns or ± 9%, whichever is greater.
6. I_{CC} is a function of frequency and maximum width. Only a pulse generator operating with 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75mA. For example, a -100 will never exceed 30mA, etc.
7. See "Test Conditions" sections at the end of this data sheet.

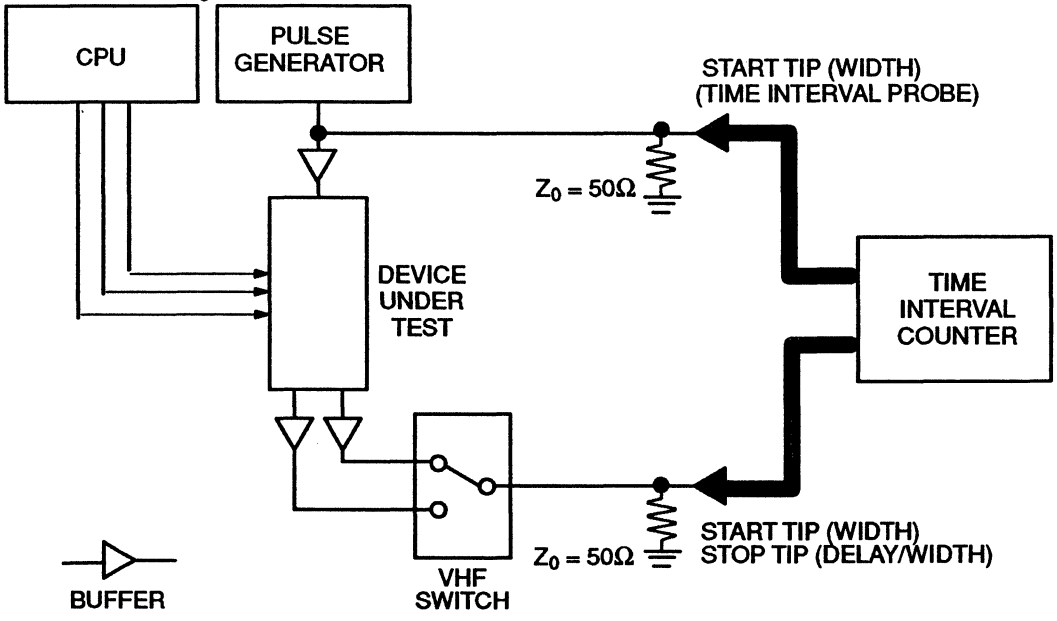
TIMING DIAGRAM Figure 2



POWER -UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following trigger pulse.

t_{WIH}, t_{WIL}, t_{WO} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_D (Intrinsic Delay): The elapsed time between the 1.5 point on the leading edge of the input trigger pulse and the 1.5V point on the leading edge of output pulse.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications is within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1040. The input waveform is produced by a precision pulse generator under software control. The intrinsic delay is measured by a time interval counter (20 ps resolution) connected between the input and each output. Outputs are selected and connected to the counter by a VHF switch control unit. Width measurements are made by directing both the start and stop functions of the counter to the same output. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0ns max. (measured between 0.6V and 2.4)
Pulse Width:	500ns (1µs for -500)
Period:	1µs (2µs for -500)

Output:

The output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

Note:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

DS1280
3-Wire to Bytewide Converter Chip

3

FEATURES

- Adapts JEDEC bytewide memory to a 3-wire serial port
- Supports 512K bytes of memory
- 68-pin version provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- Available in 44- or 80-pin quad flat pack for high density requirements

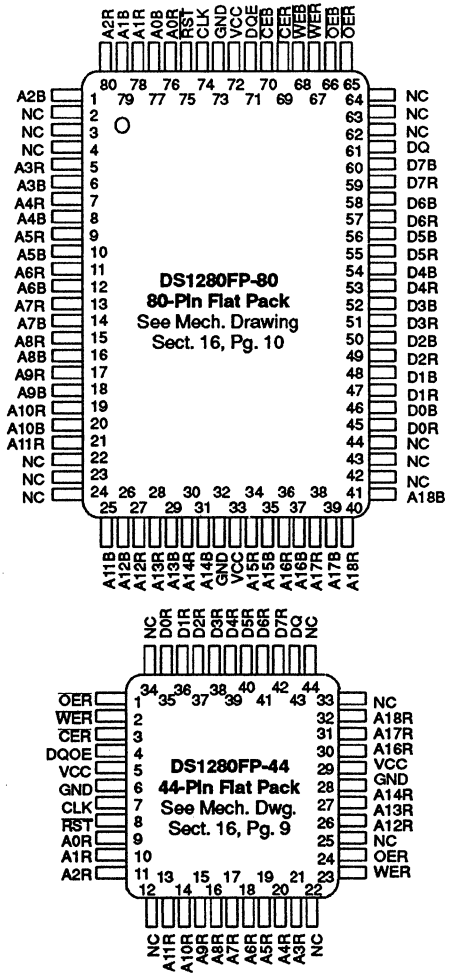
ORDERING INFORMATION

DS1280FP-XX	-80	80-pin Flat Pack
	-44	44-pin Flat Pack

PIN DESCRIPTION

$\overline{RST}$	Reset For Serial Port
DQ	Data Input/Output For Serial Port
CLK	Clock Input For Serial Port
DQE	Serial Port Active Output
$\overline{CEB}$	System Bus Enable
$\overline{OEB}$	System Bus Read Enable
$\overline{WEB}$	System Bus Write Enable
A0B-A18B	System Address Bus
D0B-D7B	System Data Bus
$\overline{CER}$	RAM Chip Enable
$\overline{WER}$	RAM Write Enable
$\overline{OER}$	RAM Output Enable
A0R-A18R	RAM Address Bus
D0R-D7R	RAM Data Bus
GND	Ground
V_{CC}	+5 Volts

PIN ASSIGNMENT



DESCRIPTION

The DS1280 adds a 3-wire serial port to a bytewide static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and bytewide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a 6-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmission for error.

PIN DESCRIPTION

$\overline{RST}$ – The 3-wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK – The clock input signal is used to input or extract data from the 3-wire serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven out onto the 3-wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ – The DQ signal is the bidirectional data signal for the 3-wire serial port.

DQE – The DQE output signal is active (high level) whenever the 3-wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

$\overline{CER}$ – Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable ($\overline{CEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{WER}$ – Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable ($\overline{WEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

$\overline{OER}$ – Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable ($\overline{OEB}$) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

A0R-A18R – Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3-wire serial port and associated timing circuits.

D0R–D7R – Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external bytewide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3-wire serial port and associated timing circuits.

$\overline{CEB}$ – System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM (68-pin package only).

$\overline{OEB}$ – System bus output enable (read) for transfer of data from RAM to the parallel system bus (68-pin package only).

$\overline{WEB}$ – System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM (68-pin package only).

A0B-A18B – System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM (68-pin package only).

D0B-D7B – System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM (68-pin package only).

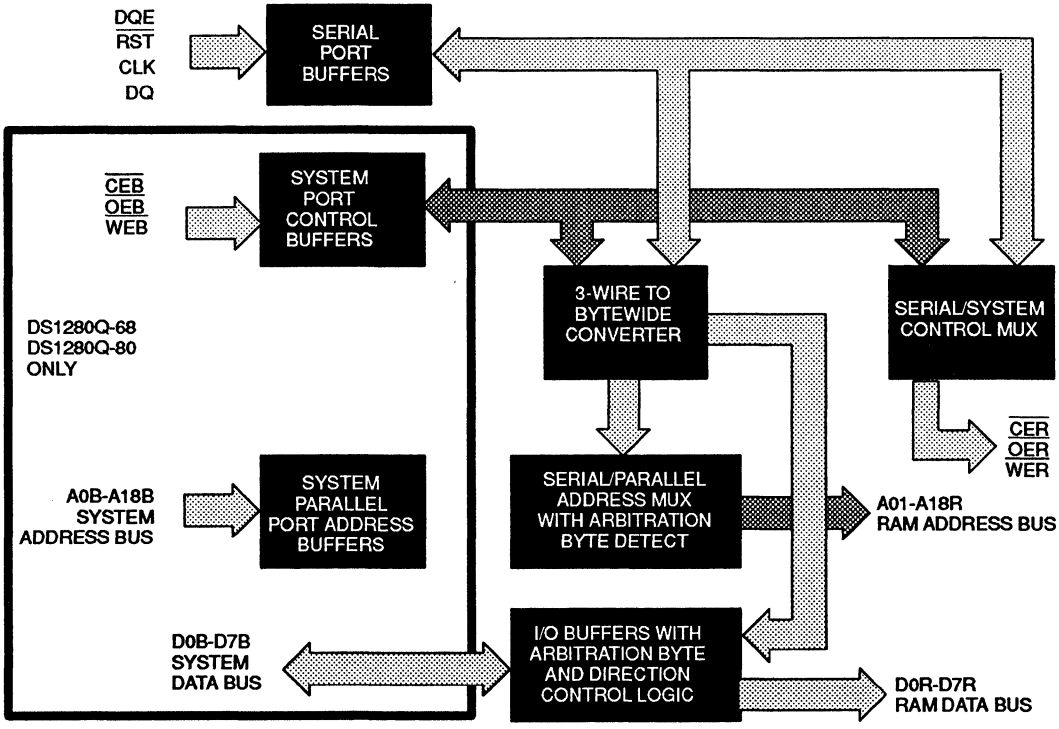
Vcc – +5volt power from the DS1280 (2 pins).

GND – Ground for the DS1280 (2 pins).

OPERATION

Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections: a 3-wire to bytewide converter and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3–wire serial port or a bytewide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3-wire to bytewide converter. The 3-wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3-wire to bytewide converter.

DS1280 BLOCK DIAGRAM Figure 1



SYSTEM BYTEWIDE PARALLEL BUS

If the $\overline{RST}$ signal for the 3-wire serial port is low (inactive), the bytewide parallel port can access associated RAM directly. The bytewide parallel bus addresses (A0B-A18B) and control signals ($\overline{CEB}$, $\overline{OEB}$ and $\overline{WEB}$) are buffered by the DS1280 and become outputs A0R-A18R, $\overline{CER}$, $\overline{OER}$, and $\overline{WER}$ respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the bytewide parallel bus to RAM when $\overline{CEB}$ and $\overline{WEB}$ inputs are both active (low). The $\overline{OEB}$ signal is a "don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when $\overline{CEB}$ and $\overline{OEB}$ signals are both low and $\overline{WEB}$ is high.

3-WIRE SERIAL BUS

If the RST signal for the 3-wire serial port is active (high), the 3-wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3-wire to bytewide converter uses a 56-bit protocol written serially using $\overline{RST}$, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered into the 3-wire while $\overline{RST}$ is high on the low-to-high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last eight bits of the 56-bit protocol are a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56-bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

PROTOCOL: 3-WIRE SERIAL BUS

The 3-wire serial bus protocol can cause eight different actions to occur as shown in Table 1.

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7, and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2.

A burst read uses a 19-bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an 8-bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3-wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19-bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3-wire bus into an 8-bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte-by-byte basis, automatically incrementing the selected address by one location for each successive byte.

PROTOCOL COMMANDS Table 1

1. Burst read
2. Burst write
3. Read protocol select bits
4. Write protocol select bits
5. Burst read masking portions of the protocol select bits
6. Read CRC register
7. Set the address arbitration byte location
8. Poll arbitration byte for status and control

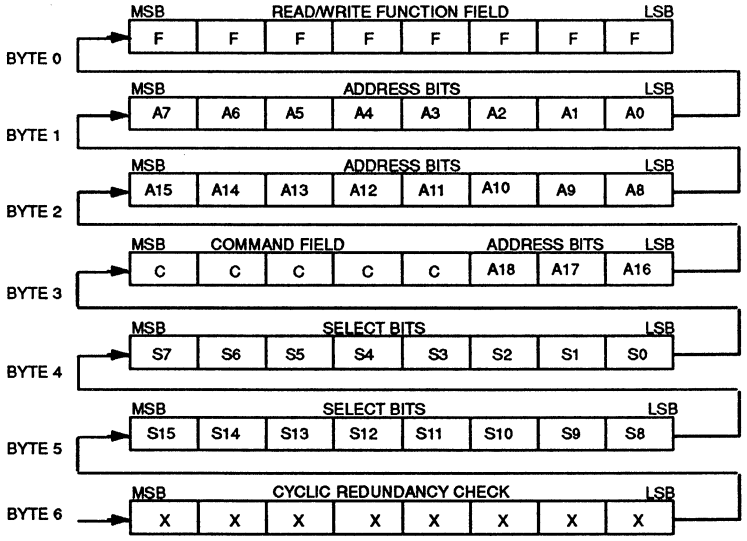
Termination of a current operation will occur at any time when $\overline{RST}$ is taken low. If a byte of data has been loaded into the shift register, a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when $\overline{RST}$ goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the protocol. The 8-bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM.

After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3-wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the CRC for the previous transaction can only be obtained if a read CRC command is issued immediately after $\overline{RST}$ goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever $\overline{RST}$ goes low again, destroying the CRC value of interest. Generation of the CRC byte by the external unit on the 3-wire bus will be covered later in this data sheet.

CONTROL FIELD Table 2

00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 7FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

PROTOCOL Figure 2



In any 2-port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports.

Two commands are used by the 3-wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel bytewide port, a command is added to move the arbitration byte to either address location "00000" or address location "7FFFF." When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 7FFFF in addition to accessing the arbitration byte.

The second command used by the 3-wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed read-write-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56-bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111) and the correct command field.

Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, multiple DS1280s can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have multiple DS1280s in use and uniquely identify each. A read can occur suc-

cessfully without knowing the select bits but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS1280 when more than one is used. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of one or more DS1280s. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (see Figure 3). With these two select bits unmasked, only an exact match of four possible combinations of these two select bits will allow access through the 3-wire port to RAM. The combinations are 00, 01, 10, and 11. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits.

Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. Repetition of unmasking select bit pairs will yield an exact match of 65,536 possible DS1280s in no more than 32 attempts.

ARBITRATION

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3-wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 7FFFF as determined by the protocol input from the 3-wire serial port. The arbitration byte has special restrictions and disciplines so that the 3-wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4.

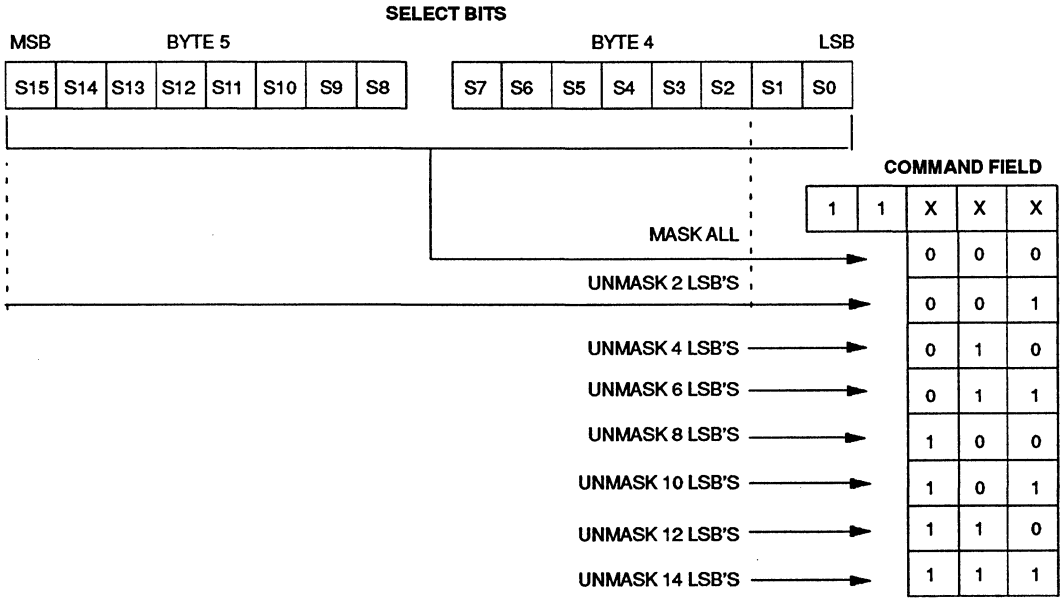
As defined, the 3-wire serial port can read the whole byte but can only write bits S2-S0. The bytewide parallel port can read the whole byte but can only write bits B1-B0. An internal counter controls bits C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3-wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3-wire serial port should then write a one into bit S2. After the write of bit S2, the 3-wire serial port should then read the arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read/write/read sequence which minimizes overhead.

The 3-wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3-wire serial port completes any transfer of data to or from RAM, bit S2 should be written back to zero so that the bytewide parallel port will know that the 3-wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signaling the 3-wire serial port that the RAM is not in use.

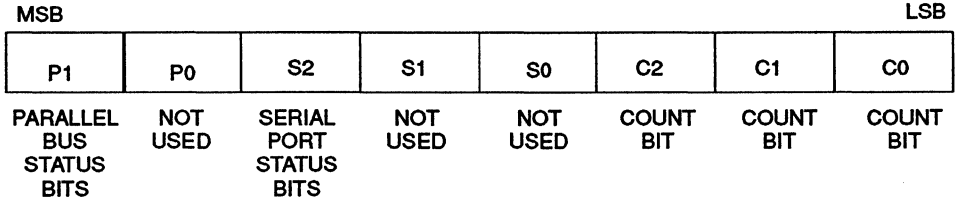
The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information, making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a port desires access to RAM or the amount of RAM written. Another method of arbitration between the 3-wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3-wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3-wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3-wire port.

Since the 3-wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3-wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3-wire clock input. Essentially the 3-wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3-wire serial port.

SELECT BITS MASK Figure 3



ARBITRATION BYTE Figure 4



CRC GENERATION

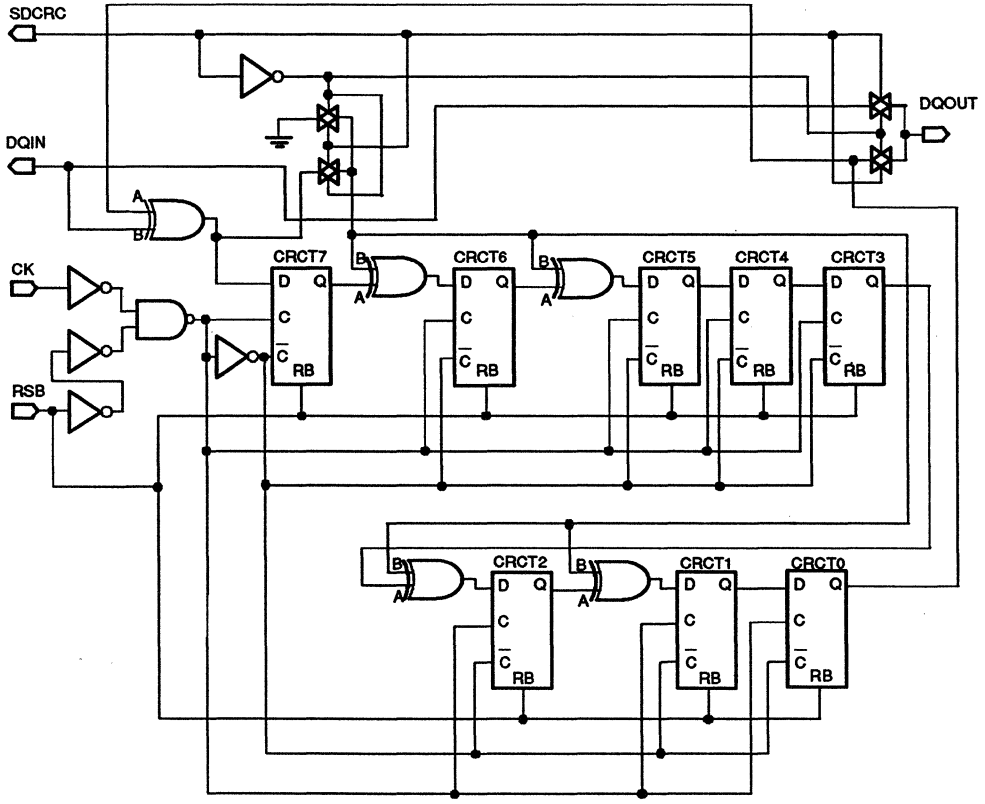
The logic involved in CRC generation is shown in Figure 5. It is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and, at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire serial bus.

The reset signal (RSB) must be high while the CRC generator is being used, as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire serial bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

CRC GENERATION LOGIC Table 3

```
DO_CRC:
        PUSH    ACC             ; Save the Accumulator
        PUSH    B               ; Save the B register
        PUSH    ACC             ; Save bits to be shifted
        MOV     B,      #8      ; Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC     ; Calculate DQIN xor CRCTO
        RRC     A               ; Move it to the last
        MOV     A,      CRC     ; Get the last CRC value
        JNC     ZERO            ; Skip if DQIN xor CRCTO = 0
        XRL     A,      0CCH    ; Update the CRC value
ZERO:
        RRC     A               ; Position the new CRC
        MOV     CRC,    A       : Store the new CRC
        POP     ACC             : Get the remaining bits
        RR      A               ; Position next bit in LSB
        PUSH    ACC             ; Save the remaining bits
        DJNZ    B,      CRC_LOOP ; Repeat for eight bits
        POP     ACC             ; Clean up the stack
        POP     B               ; Restore the B register
        POP     ACC             ; Restore the Accumulator
        RET                     ; Return
```

CRC GENERATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to+125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS

(t_A=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3V	V	
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(t_A=0°C to 70°C ; V_{CC}=+5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		+1	µA	9
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+2			mA	
Supply Current	I_{CC1}			15	mA	2
Supply Current	I_{CC2}			50	mA	3

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%; 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	4
Data to CLK Hold	t_{CDH}	40			ns	4
Data to CLK Delay	t_{CDD}			125	ns	4,5,6
CLK Low Time	t_{CL}	500			ns	4
CLK High Time	t_{CH}	500			ns	4
CLK Frequency	f_{CLK}	DC		1	MHz	4,10
CLK Rise & Fall Time	$t_R t_F$			100	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	4
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	4
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	4
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	4,6
Serial Port Active	t_{DI}			25	ns	4,6
Serial Port Inactive	t_{DI}			25	ns	4,6
Parallel Port Propagation	t_{PD}		12	20	ns	4,6,8

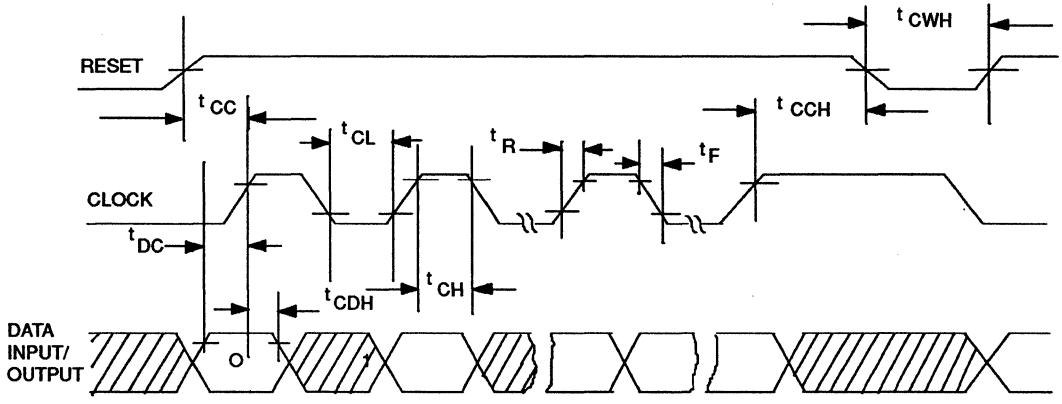
CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	

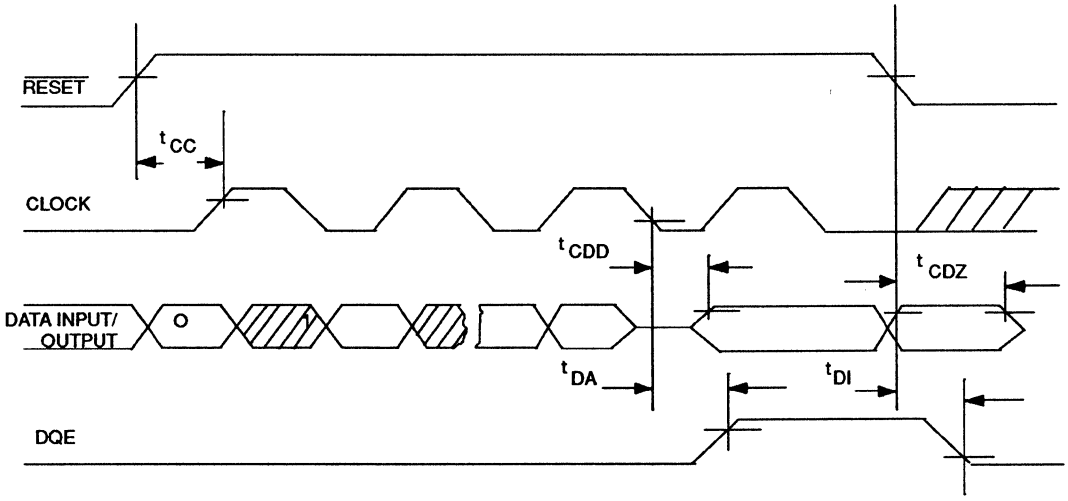
NOTES

1. All voltages are referenced to ground.
2. I_{CC1} is measured with all outputs open and both the 3-wire serial port or the bytewide parallel port inactive.
3. I_{CC2} is measured with all outputs open.
4. Measured at V_{IH} = 2.0 V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
5. Measured at V_{OH}= 2.4 V and V_{OL} = 0.4V.
6. Measured with a load capacitance of 50 pF.
7. The 3-wire serial port will correctly read and write any static RAM with an effective access time of 200ns.
8. Propagation delay is the same for data going either way on the bytewide parallel bus.
9. Pins A0B through A18B, $\overline{RST}$, DQ, $\overline{CEB}$ have pulldown resistors which will leak approximately 50 µA.
10. Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symmetrical waveform.

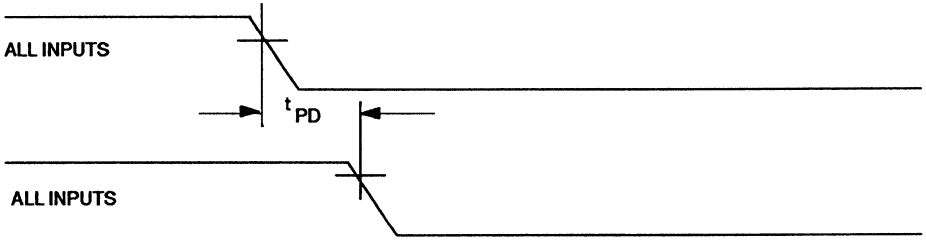
TIMING DIAGRAM-WRITE DATA TRANSFER 3-WIRE SERIAL PORT (7)



TIMING DIAGRAM-READ DATA TRANSFER 3-WIRE SERIAL PORT (7)



PROPAGATION DELAY-DATA TRANSFER: BYTEWIDE PARALLEL DATA BUS (8)



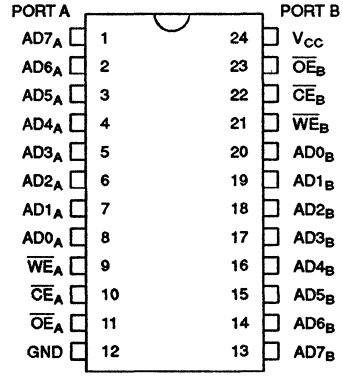
DALLAS SEMICONDUCTOR

DS1609
Dual Port RAM

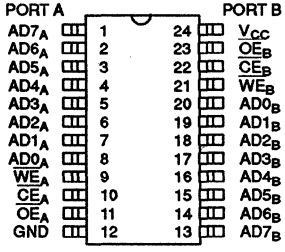
FEATURES

- Totally asynchronous 256 byte dual port memory
- Multiplexed address and data bus keeps pin count low
- Dual port memory cell allows random access with minimum arbitration
- Each port has standard independent RAM control signals
- Fast access time
- Low power CMOS design
- 24 pin DIP or 24 pin SOIC surface mount package
- Both CMOS and TTL compatible
- Reduced performance operation down to 2.5 volts
- Operating temperature of -40°C to +85°C
- Standby current of 100 nA @ 25°C makes the device ideal for battery backup or battery operate applications.

PIN ASSIGNMENT



DS1609
24 PIN DIP (600 mil)
See Mech. Drawing – Sect. 16, Pg. 4



DS1609S
24 PIN SOIC (300 mil)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

V_{CC}	-	+5 volt supply
GND	-	Ground
AD0-AD7	-	Port address/data
$\overline{CE}$	-	Port enable
$\overline{OE}$	-	Output enable
$\overline{WE}$	-	Write enable

DESCRIPTION

The DS1609 is a random access 256 byte dual port memory designed to connect two asyncronous address/data buses together with a common memory element. Both ports have unrestricted access to all 256 bytes of memory and with modest system discipline no arbitration is required. Each port is controlled by three control signals: output enable, write enable, and port enable. The device is packaged in plastic 24 pin DIP and 24 pin SOIC. Output enable access times of 35 ns are available when operating at 5 volts. Reduced performance operation at reduced voltage can be achieved down to 2.5 volts.

OPERATION – READ CYCLE

The main elements of the dual port RAM are shown in Figure 1.

A read cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. Addresses can be removed from the bus provided address hold time is met. Next, the output enable control ($\overline{OE}$) is transitioned low, which begins the data access portion of the read cycle. With both $\overline{CE}$ and $\overline{OE}$ active low, data will appear valid after the output enable access time t_{OEA}. Data will remain valid as long as both port enable and output enable remains low. A read cycle is terminated with the first occurring rising edge of either $\overline{CE}$ or $\overline{OE}$. The address/data bus will return to a high impedance state after time t_{CEZ} or t_{OEZ} as referenced to the first occurring rising edge. $\overline{WE}$ must remain high during read cycles.

OPERATION – WRITE CYCLE

A write cycle to either port begins by placing an address on the multiplexed bus pins AD0 - AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. As with a read cycle, the address can be removed from the bus provided address hold time is met. Next the write enable control signal ($\overline{WE}$) is transitioned low which begins the write data portion of the write cycle. With both $\overline{CE}$ and $\overline{WE}$ active low the data to be written to the selected memory location is placed on the multiplexed bus. Provided that data setup (t_{DS}) and data hold (t_{DH}) times are met, data is written into the memory and the write cycle is terminated on the first occurring rising edge of either $\overline{CE}$ or $\overline{WE}$. Data can be removed from the bus as soon as the write cycle is terminated. $\overline{OE}$ must remain high during write cycles.

ARBITRATION

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports (see Figure 2). Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write arbitration doesn't occur is to perform redundant read cycles. Write/write arbitration needs can be avoided by assigning groups of addresses for write operation to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

FIGURE 1: BLOCK DIAGRAM: DUAL PORT RAM

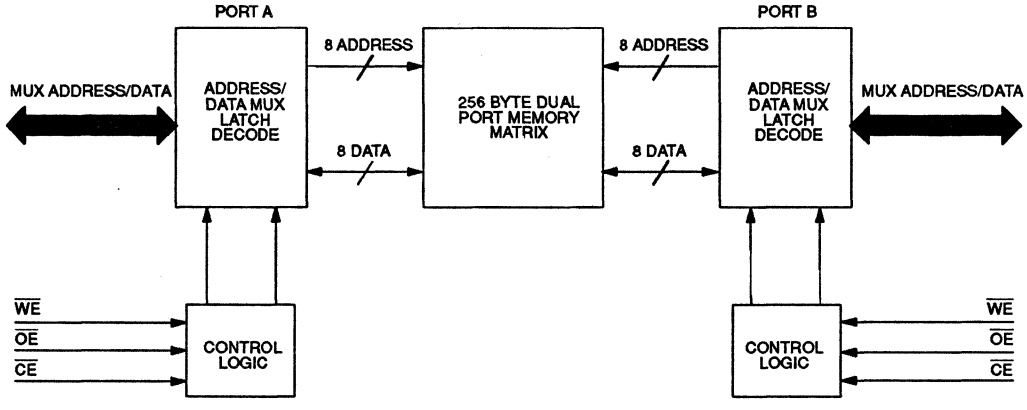
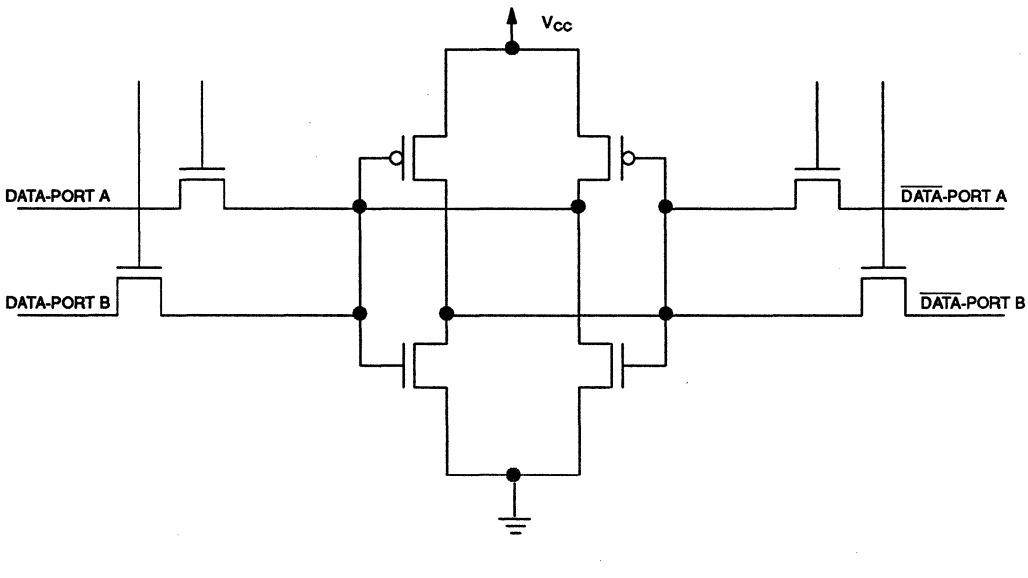


FIGURE 2: DUAL PORT MEMORY CELL



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to 7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (-40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C TO +85°C V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance	Z_{IN}	50K			Ω	2
$\overline{CE}$, $\overline{WE}$, $\overline{OE}$ Leakage	I_{LO}	-1.0		+1.0	µA	
Standby Current	I_{CCS1}		3.0	5.0	mA	3, 4, 13
Standby Current	I_{CCS2}		50	300	µA	3, 5, 13
Standby Current	I_{CCS3}		100		nA	3, 6, 13
Operating Current	I_{CC}		18	30	mA	7, 13
Logic 1 Output	V_{OH}	2.4			V	8
Logic 0 Output	V_{OL}			0.4	V	9

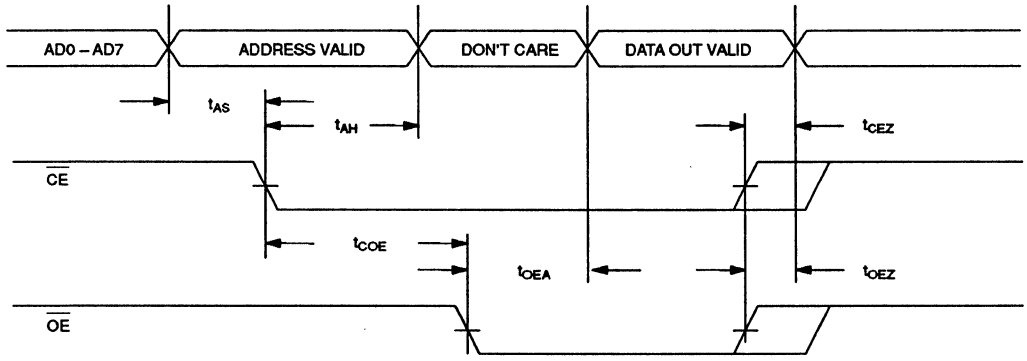
CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
I/O Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C TO +85°C V_{CC} = 5V ± 10%)							
PARAMETER	SYMBOL	DS1609-50		DS1609-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	t_{AS}	5		5		nsec	
Address Hold Time	t_{AH}	25		20		nsec	
Output Enable Access	t_{OEA}	0	50	0	35	nsec	10
$\overline{OE}$ to High Z	t_{OEZ}	0	20	0	40	nsec	
$\overline{CE}$ to High Z	t_{CEZ}	0	20	0	20	nsec	
Data Setup Time	t_{DS}	0		0		nsec	
Data Hold Time	t_{DH}	10		5		nsec	
Write Pulse Width	t_{WP}	50		35		nsec	11
$\overline{CE}$ Recovery Time	t_{CER}	20		15		nsec	12
$\overline{WE}$ Recovery Time	t_{WER}	20		15		nsec	12
$\overline{OE}$ Recovery Time	t_{OER}	20		15		nsec	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25		20		nsec	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25		20		nsec	

AC ELECTRICAL CHARACTERISTICS (-40°C TO +85°C V_{CC} = 2.5V - 4.5V)							
PARAMETER	SYMBOL	DS1609-50		DS1609-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	t_{AS}	5		5		nsec	
Address Hold Time	t_{AH}	25		25		nsec	
Output Enable Access	t_{OEA}	0	100	0	75	nsec	10
$\overline{OE}$ to High Z	t_{OEZ}	0	20	0	20	nsec	
$\overline{CE}$ to High Z	t_{CEZ}	0	20	0	20	nsec	
Data Setup Time	t_{DS}	0		0		nsec	
Data Hold Time	t_{DH}	10		10		nsec	
Write Pulse Width	t_{WP}	100		75		nsec	11
$\overline{CE}$ Recovery Time	t_{CER}	20		20		nsec	12
$\overline{WE}$ Recovery Time	t_{WER}	20		20		nsec	12
$\overline{OE}$ Recovery Time	t_{OER}	20		20		nsec	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25		25		nsec	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25		25		nsec	

DUAL PORT RAM TIMING: READ CYCLE

DURING READ CYCLE $\overline{WE} = V_{IH}$

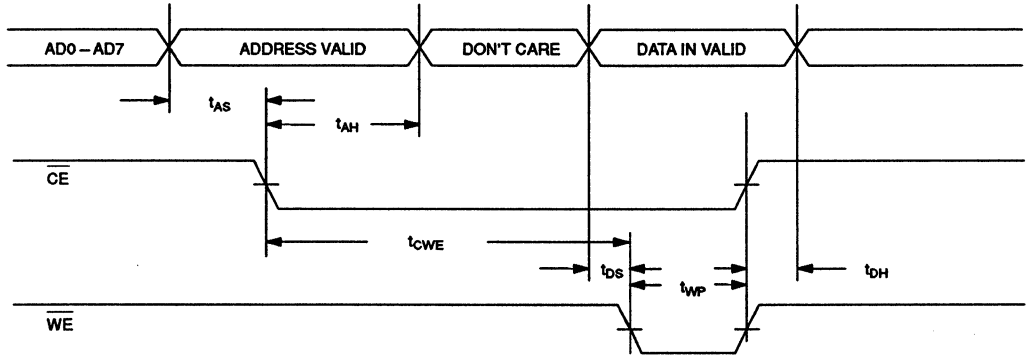


NOTES

1. During read cycle the address must be off the bus prior to t_{OEA} minimum to avoid bus contention.
2. Read cycles are terminated by the first occurring rising edge of $\overline{OE}$ or $\overline{CE}$.

DUAL PORT RAM TIMING: WRITE CYCLE

DURING WRITE CYCLE $\overline{OE} = V_{IH}$



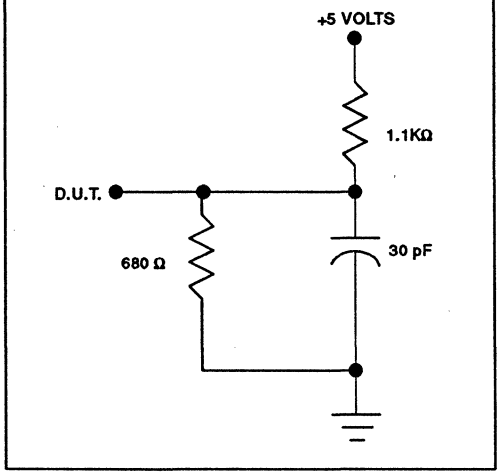
NOTE

1. Write cycles are terminated by the first occurring edge of $\overline{WE}$ or $\overline{CE}$.

NOTES

1. All Voltages are referenced to ground.
2. All pins other than $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, V_{CC} and ground are continuously driven by a feedback latch in order to hold the inputs at one power supply rail or the other when an input is tristated. The minimum driving impedance presented to any pin is 50KΩ. If a pin is at a logic low level, this impedance will be pulling the pin to ground. If a pin is at a logic high level, this impedance will be pulling the pin to V_{CC}.
3. Standby current is measured with outputs open circuited.
4. I_{CCS1} is measured with all pins within 0.3V of V_{CC} or GND and with $\overline{CE}$ at a logic high or logic low level.
5. I_{CCS2} is measured with all pins within 0.3V of V_{CC} or ground and with $\overline{CE}$ within 0.3V of V_{CC}.
6. I_{CCS3} is measured with all pins at V_{CC} or ground potential and with $\overline{CE} = V_{CC}$. Note that if a pin is floating, the internal feedback latches will pull all the pins to one power supply rail or the other.
7. Active current is measured with outputs open circuited, and inputs swinging full supply levels with one port reading and one port writing at 100 ns cycle time. Active currents are a DC average with respect to the number of 0's and 1's being read or written.
8. Logic one voltages are specified at a source current of 1 mA.
9. Logic zero voltages are specified at a sink current of 4 mA.
10. Measured with a load as shown in Figure 3.
11. t_{WP} is defined as the time from $\overline{WE}$ going low to the first of the rising edges of $\overline{WE}$ and $\overline{CE}$.
12. Recovery time is the amount of time control signals must remain high between successive cycles.
13. Typical values are at 25°C.

FIGURE 3: LOAD SCHEMATIC



DALLAS SEMICONDUCTOR

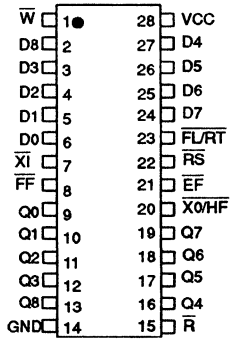
DS2009
512 x 9 FIFO Chip

3

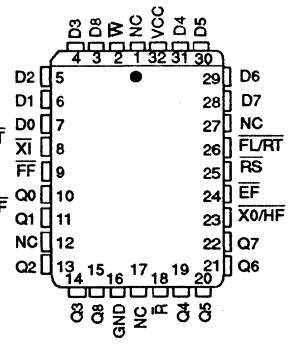
FEATURES

- First-in, first-out memory-based architecture
- Flexible 512 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 35ns, 50ns, 65ns, 80ns, and 120ns access times

PIN ASSIGNMENT



28-Pin DIP(300 and 600 Mil)
See Mech. Drawings
Sect. 16, Pgs. 1 & 4



32-Pin PLCC
See Mech. Drawing
Sect. 16, Pg. 11

PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2009 512 x 9 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2009 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a first-in, first-out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register-based FIFOs, the DS2009 employs a memory-based architecture wherein a byte written into the device does not ripple through. Instead, a byte written into the DS2009 is stored at a specific location where it remains until over-written. The byte can be read and re-read as often as desired.

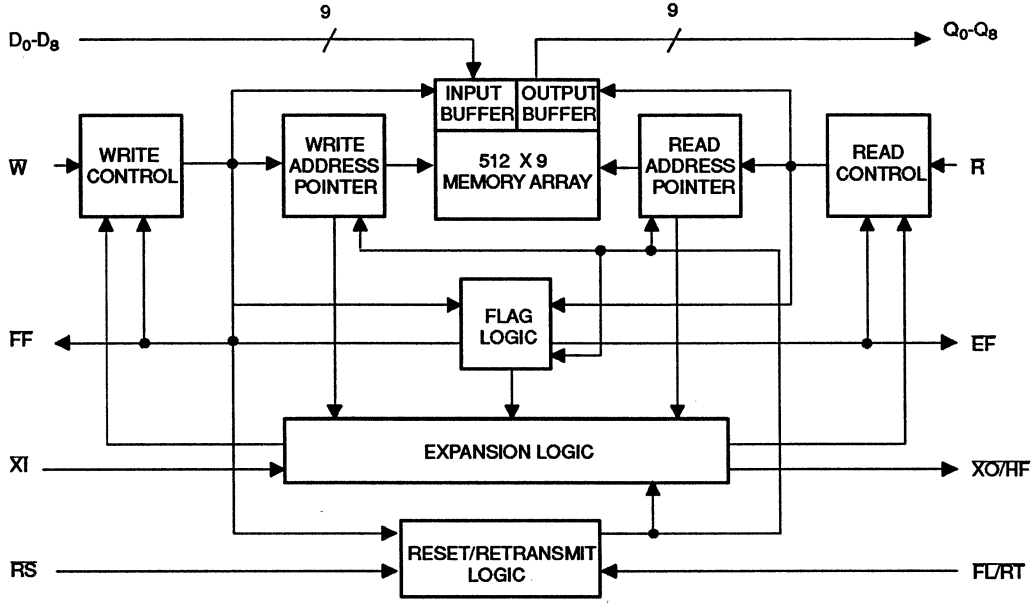
Twin address pointers (ring counters) automatically generate the address required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing unread bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2009 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2009 can connect the read, write, data in, and data out lines of the DS2009 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion in and expansion out pins as appropriate (see the "Expansion Timing" section for a more complete discussion).

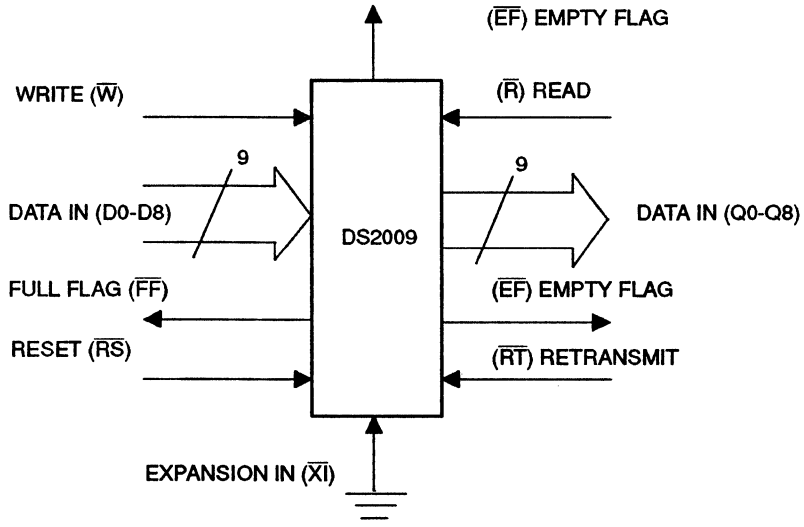
BLOCK DIAGRAM Figure 1



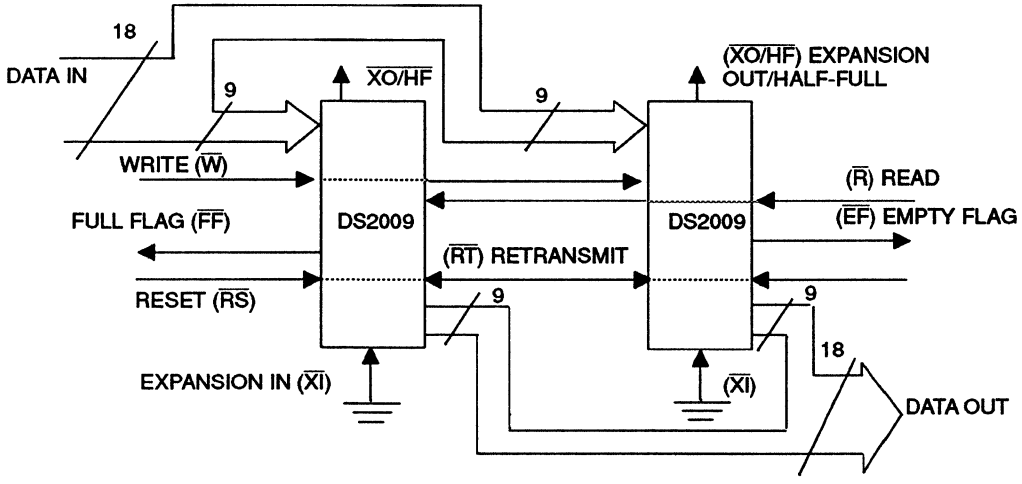
SINGLE DEVICE CONFIGURATION

A single DS2009 can be used when application requirements are for 512 words or less. The DS2009 is placed in single device configuration mode when the chip is reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

A SINGLE 512 X 9 FIFO CONFIGURATION Figure 2



A 512 X 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:
Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

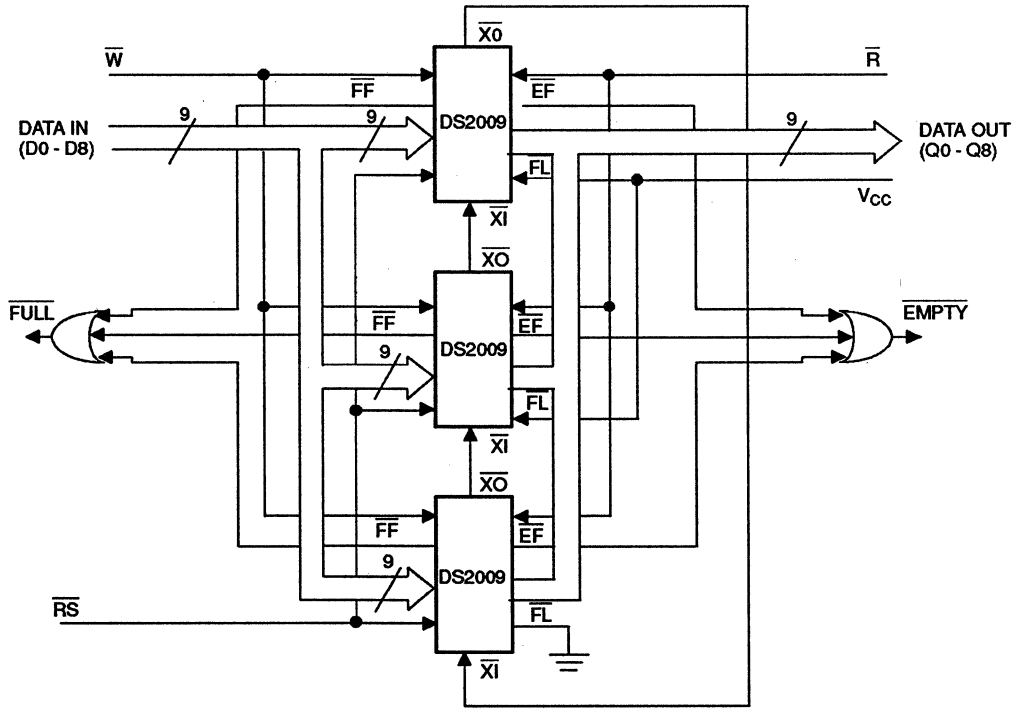
The DS2009 can easily be adapted to applications where more than 512 words are required. Figure 4 demonstrates depth expansion using three DS2009s. Any depth can be attained by adding DS2009s.

External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2009 operates in the depth expansion configuration after the chip is reset under the following conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The retransmit function is not allowed in the depth expansion mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.

A 1536 X 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



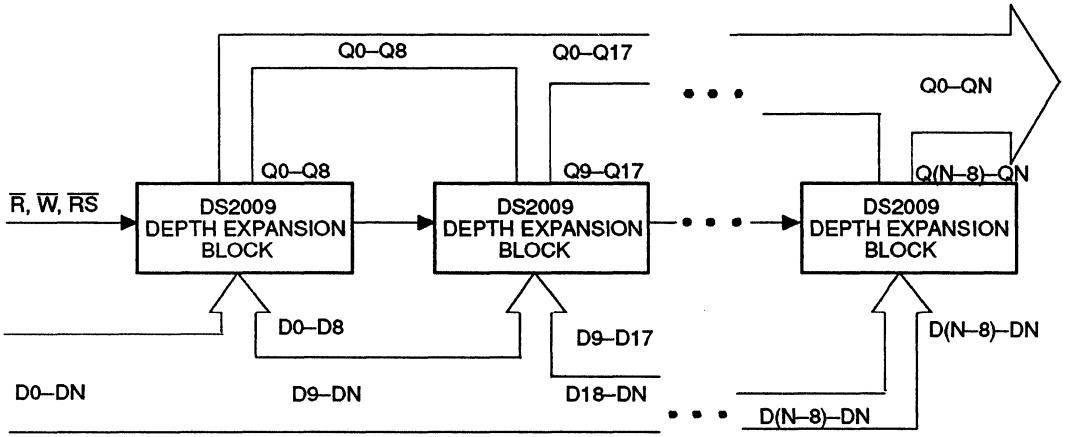
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Bidirectional applications that require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing DS2009s as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion can be used in this mode.

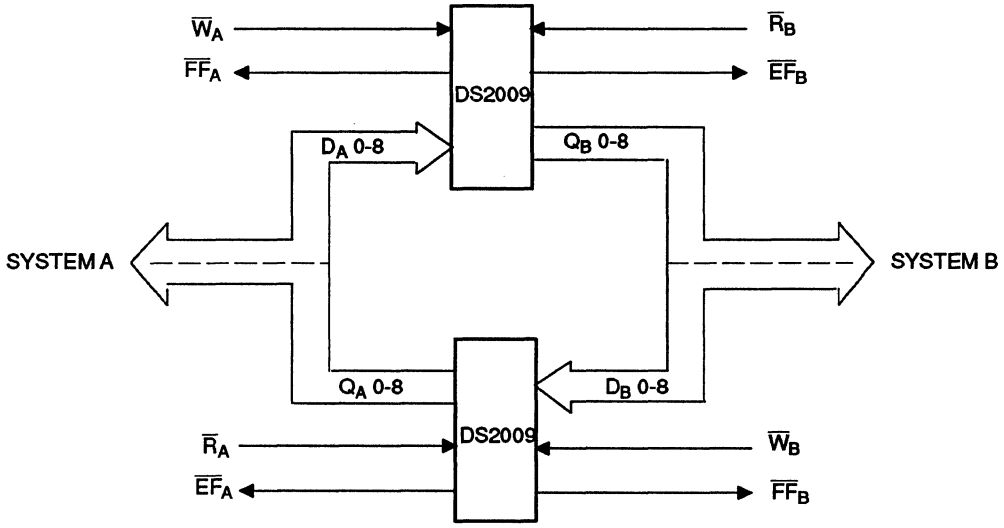
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block diagram see "Depth Expansion" section and Figure 4.
2. For flag operation see "Width Expansion" section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



HALF-FULL CAPABILITY

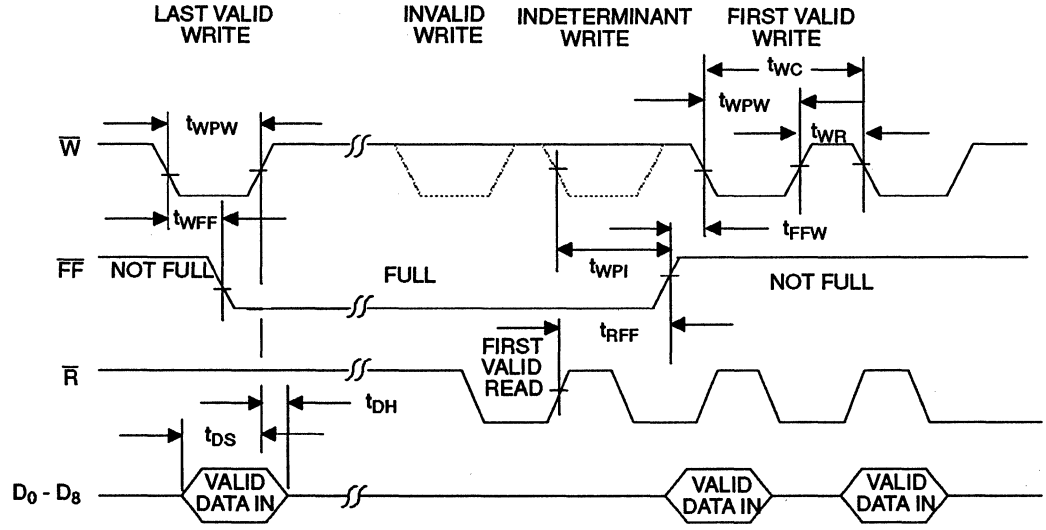
In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The half-full flag is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2009 initiates a write cycle (see Figure 7) on the falling edge of the write enable control input ($\overline{W}$), pro-

vided that the Full Flag ($\overline{FF}$) is not asserted. Data setup and hold time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing read operations. $\overline{FF}$ is asserted during the last valid write as the DS2009 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid read operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

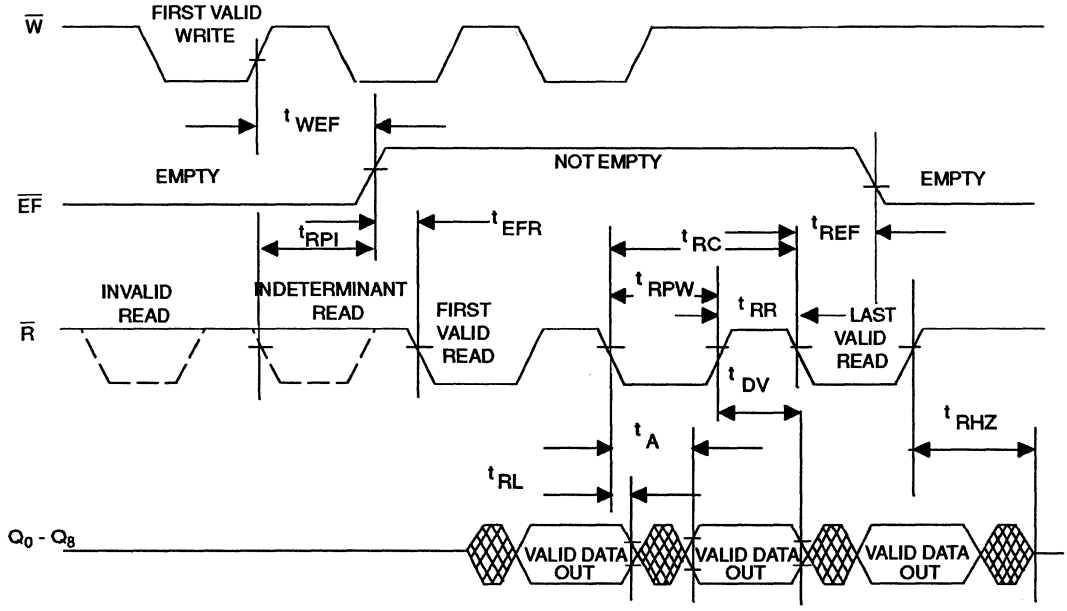
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**NOTES**
Write Cycle Time	t_{WC}	45		65		80		100		140		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		120		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		20		ns	
Data Setup Time	t_{DS}	15		20		25		30		40		ns	
Data Hold Time	t_{DH}	5		5		10		10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		30		45		60		70		110	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		5		5		10		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		30		45		60		70		110	ns	2
Write Protect Indeterminate	t_{WPI}		15		20		25		25		35	ns	2

READ MODE

The DS2009 initiates a read cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the DS2009 provides fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing write operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



READ AC ELECTRICAL CHARACTERISTICS

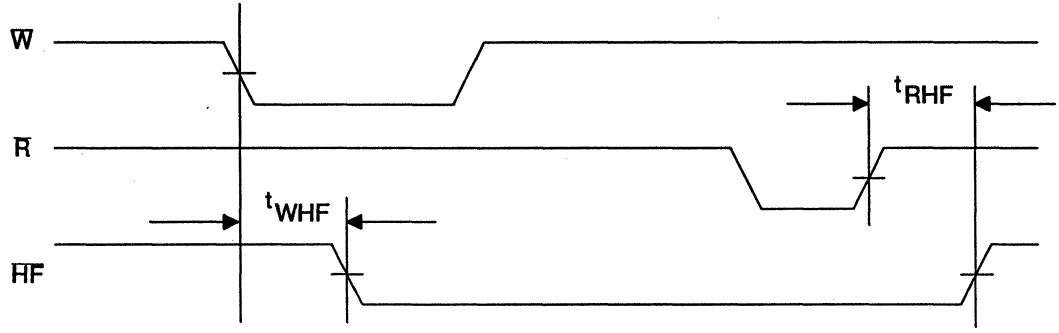
(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	U	NOTES
Read Cycle Time	t_{RC}	45		65		80		100		140		ns	
Access Time	t_A		35		50		65		80		120	ns	1
Read Recovery Time	t_{RR}	10		15		15		20		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		120		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	5		10		10		10		20		ns	2
Data Valid from $\overline{R}$ High	t_{DV}	5		5		5		5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		20		25		25		25		35	ns	2
$\overline{R}$ Low to $\overline{EF}$ Low	t_{REF}		30		45		60		70		110	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		5		5		10		10		10	ns	2
$\overline{W}$ High to $\overline{EF}$ High	t_{WEF}		30		45		60		70		110	ns	2
Read Protect Indeterminate	t_{RPI}		15		20		25		25		35	ns	2

HALF-FULL MODE

Unlike the full and empty flags, the half-full flag does not prevent device reads and writes. This flag is set by the next falling edge of write when the memory is 256 locations full. The flag will remain set until the memory is less than or equal to 256 locations full. The read operation (rising edge), which results in the memory being 256 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



HALF-FULL FLAG AC CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100		140	ns
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100		140	ns

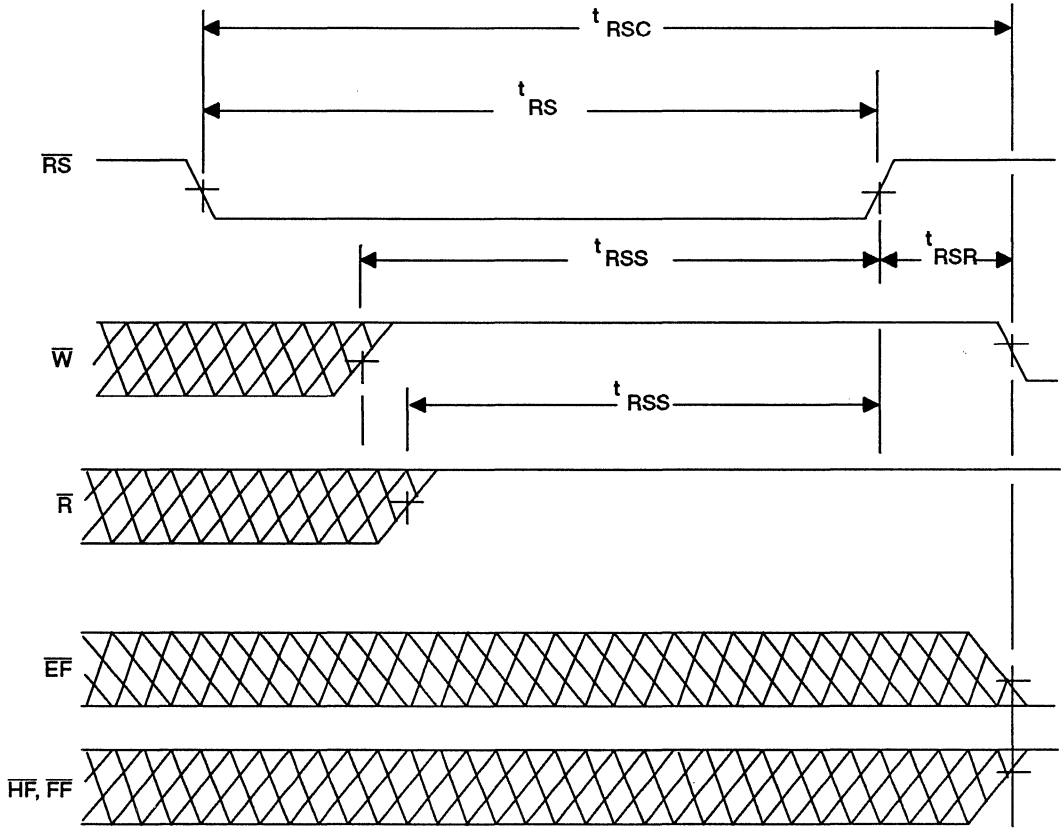
3

RESET

The DS2009 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointer are set to the first location. Reset is required after a power-up before a write operation can begin .

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ are $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during reset.

RESET Figure 10



NOTES
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at t_{RSC}.

RESET AC ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC}=5.0V ± 10%)

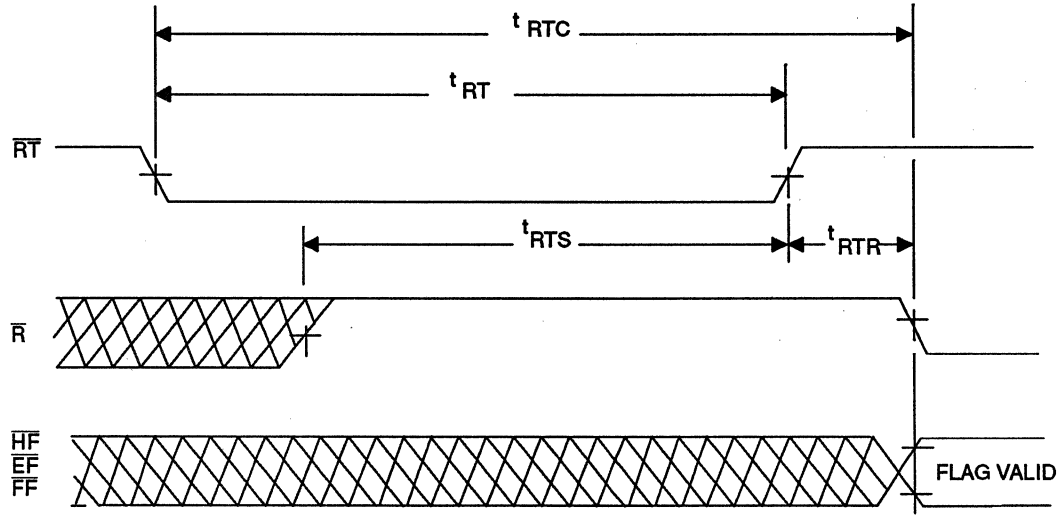
		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Reset Cycle Time	t_{RSC}	45		65		80		100		140		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		120		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		20		ns	
Reset Setup Time	t_{RSS}	30		40		50		60		100		ns	2

RETRANSMIT
The DS2009 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A retransmit operation sets the internal read pointer to the first physical location in the array but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high and must remain high for t_{RTR} afterwards.

The retransmit function is particularly useful when blocks of less than 512 writes are performed between resets. The retransmit feature is not compatible with depth expansion.

RETRANSMIT Figure 11



NOTE:
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		140		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		120		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		20		ns	
Retransmit Setup Time	t_{RTS}	30		40		50		60		100		ns	

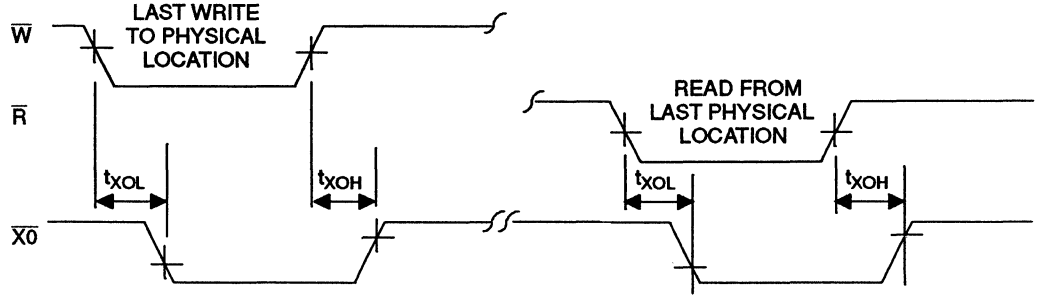
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the expansion out and expansion in signals. Discussion of expansion out/expansion in timing is provided to clarify how depth expansion works. Inasmuch as expansion out pins are generally connected only to expansion in pins, the user need not be concerned with actual timing in a normal depth expanded application unless extreme propagation delays exist between the $\overline{XO}$ and $\overline{XI}$ pin pairs.

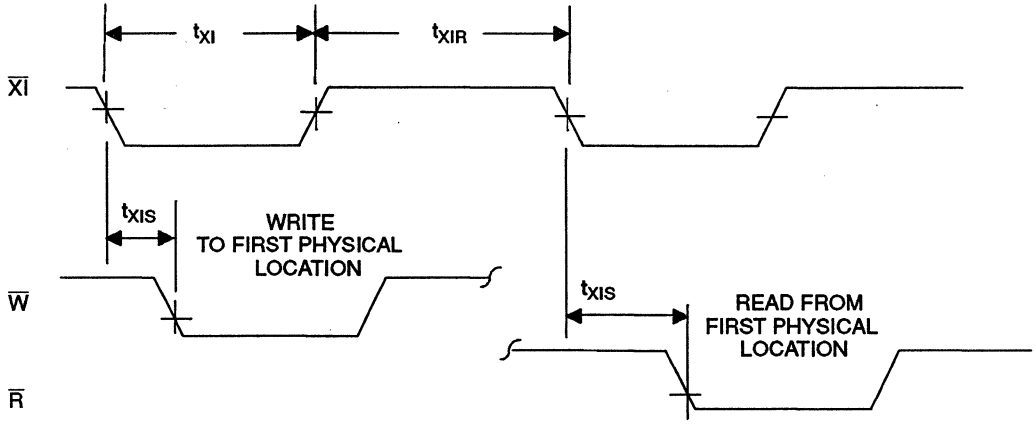
Expansion out pulses are the image of the write and read signals that cause them: delayed in time by t_{XOL} and t_{XOH}. The expansion out signal is propagated when the last physical location in the memory array is written and again when it is read (last read). This is in contrast to when the full and empty flags are activated, which is in response to writing and reading a last available location.

When in depth expansion mode, a given DS2009 will begin writing and reading as soon as valid write and read signals begin, provided $\overline{FL}$ was grounded at reset time. A DS2009 in depth expansion mode with $\overline{FL}$ high at reset will not begin writing until after an expansion in pulse occurs. It will not begin reading until a second expansion in pulse occurs and the empty flag has gone high. Expansion in pulses must occur t_{XIS} before the write and read signals they are intended to enable. Minimum expansion in pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Expansion Out Low	t_{XOL}		30		45		55		70		100	ns	
Expansion Out High	t_{XOH}		30		45		55		70		100	ns	
Expansion in Pulse Width	t_{XI}	35		50		65		80		120		ns	1
Expansion in Recovery Time	t_{XIR}	10		15		15		20		20		ns	
Expansion in Setup Time	t_{XIS}	15		20		25		30		40		ns	

AC TEST CONDITIONS:

Input Levels	GND to 3.0V
Transition Times	5ns
Input Signal Timing Reference Level	1.5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to +70°C
V_{CC}	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	20 mA

*This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

3

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic 1 Voltage All Inputs	V_{IH}	2.0		V_{CC} +0.3	V	3
Logic 0 Inputs	V_{IL}	-0.3		+0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	-1		1	µA	5
Output Leakage Current	I_{OL}	-10		10	µA	6
Output Logic 1 Voltage I_{OUT} = -1mA	V_{OH}	2.4			V	3
Output Logic 0 Voltage I_{OUT} = 4mA	V_{OL}			0.4	V	3
Average V_{CC} Power Supply Current – 35ns, 50ns, 60ns, 80ns, 120ns	I_{CC1}			100	mA	7, 9
Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	I_{CC2}			8	mA	7
Power Down Current (All Input = V_{CC} -0.2V)	I_{CC3}			500	µA	7, 10

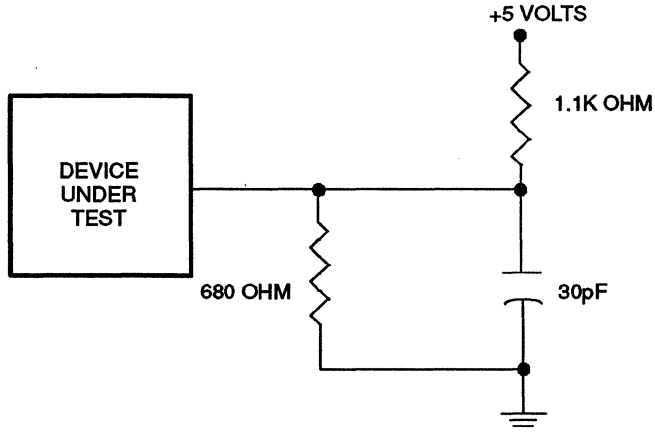
CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_O	12	pF	8

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load diagram.
3. All voltages are referenced to ground.
4. -1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. DS2010, DS2011, DS2012, and DS2013 have I_{CC1}, = 120 mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
10. DS2010 has I_{CC3} = 1mA MAX; DS2011, DS2012, DS2013 have I_{CC3} = 2mA MAX.

OUTPUT LOAD Figure 14



DALLAS SEMICONDUCTOR

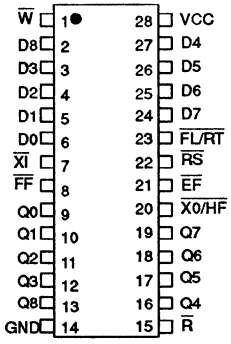
DS2010
1024 x 9 FIFO Chip

3

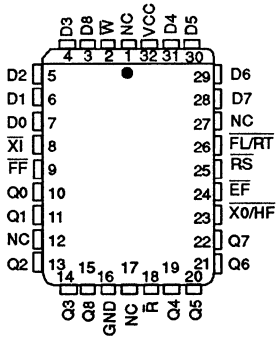
FEATURES

- First-in, first-out memory-based architecture
- Flexible 1024 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access times

PIN ASSIGNMENT



28-Pin DIP
(300 and 600 Mil)
See Mech. Drawings
Sect. 16, Pgs. 1 & 4



32-Pin PLCC
See Mech. Drawing
Sect. 16, Pg. 11

PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2010 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

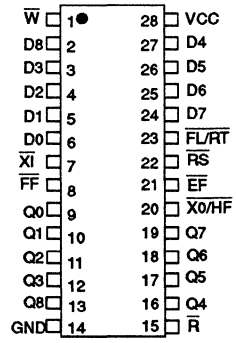
DALLAS SEMICONDUCTOR

DS2011
2048 x 9 FIFO Chip

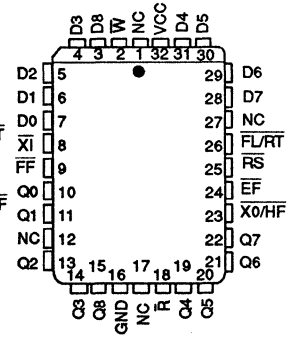
FEATURES

- First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access.

PIN ASSIGNMENT



28-Pin DIP
(300 and 600 Mil)
See Mech. Drawings
Sect. 16, Pgs. 1 & 4



32-Pin PLCC
See Mech. Drawing
Sect. 16, Pg. 11

PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

DALLAS SEMICONDUCTOR

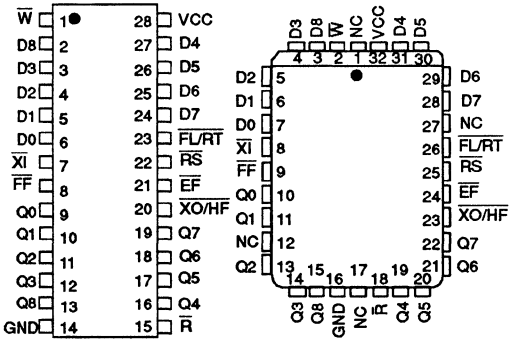
DS2012
4096 x 9 FIFO Chip

3

FEATURES

- First-in, first-out memory-based architecture
- Flexible 4096 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

PIN ASSIGNMENT



28-Pin DIP (600 Mil)
See Mech. Drawing
Sect. 16, Pg. 4

32-Pin PLCC
See Mech. Drawing
Sect. 16, Pg. 11

PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2012 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half full flags, and unlimited expansion capability in both word size and depth. The DS2012 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

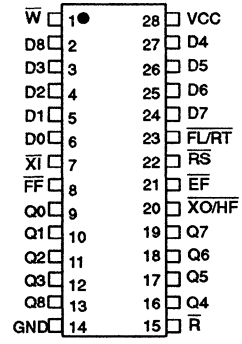
DALLAS SEMICONDUCTOR

DS2013
8192 x 9 FIFO Chip

FEATURES

- First-in, first-out memory-based architecture
- Flexible 8192 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

PIN ASSIGNMENT



28-Pin DIP (300 and 600 Mil)
See Mech. Drawings – Sect. 16, Pgs. 1 & 4

PIN DESCRIPTION

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D^0_{-8}	- Data In
Q^0_{-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2013 8192 x 9 FIFO Chip implements a first-in, first-out algorithm, featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2013 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to DS2009 512 x 9 FIFO Chip data sheet for detailed device description.

DALLAS SEMICONDUCTOR

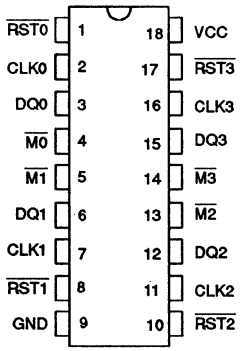
DS2015
Quad Port Serial RAM Chip

3

FEATURES

- Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin-count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes
- Low-power CMOS
- Space saving 18-pin DIP
- Directly interfaces to the DS1206 Phantom Serial Interface Chip
- Provides a low cost interconnect for up to four microprocessor based systems

PIN ASSIGNMENT



18-Pin DIP (300 Mil)
See Mech. Drawing
Sect. 16, Pg. 1

PIN DESCRIPTION

RST0-RST3	Port 0 - Port 3 Reset
D/Q0-D/Q3	Port 0 - Port 3 Data I/O
CLK0-CLK3	Port 0 - Port 3 Clock
M0-M3	Port 0 - Port 3 Message Ready
GND	Ground
Vcc	+5 Volts

DESCRIPTION

The DS2015 Quad Port Serial RAM Chip is a low-cost device which can loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for each port is 64 bits. Access to and from each port takes place over a 3-wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

OPERATION

The DS2015 has four separate three-wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes, each of which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quad-ported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three-wire serial ports contains a three-byte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

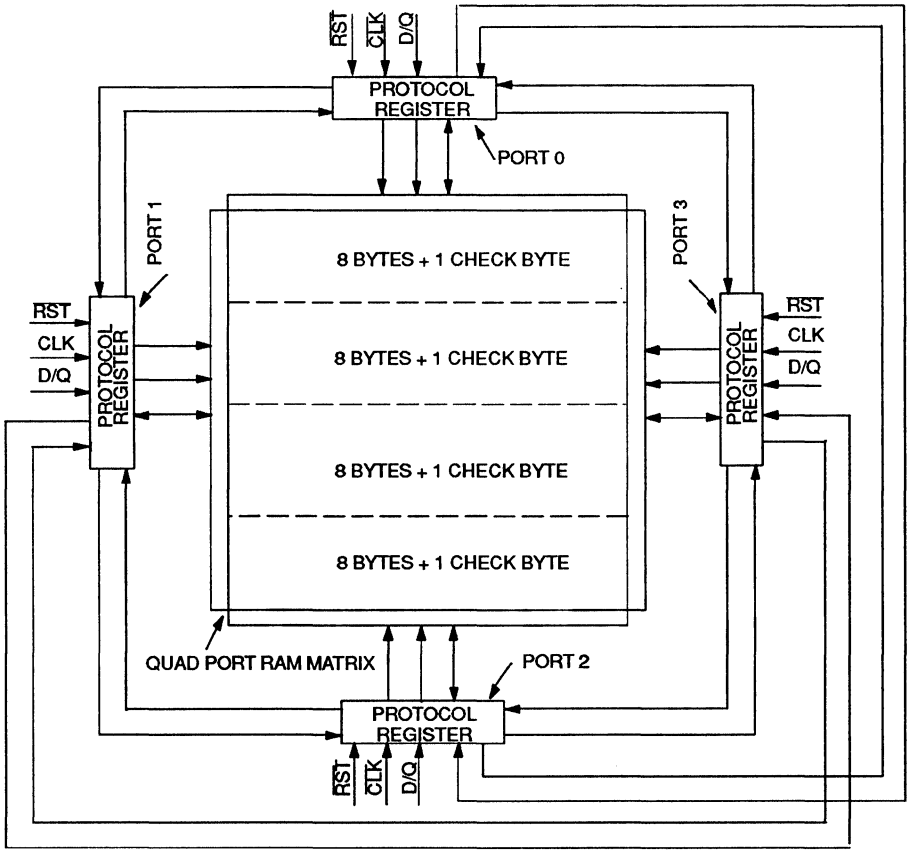
Protocol Register

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight-bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles: messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the $\overline{RST}$ input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while $\overline{RST}$ is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles: the action code and the destination. This byte is write only and data is input on the D/Q line with $\overline{RST}$ inactive and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight-byte message is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

Quad Port RAM

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

QUAD PORT BLOCK DIAGRAM Figure 1



Check Byte

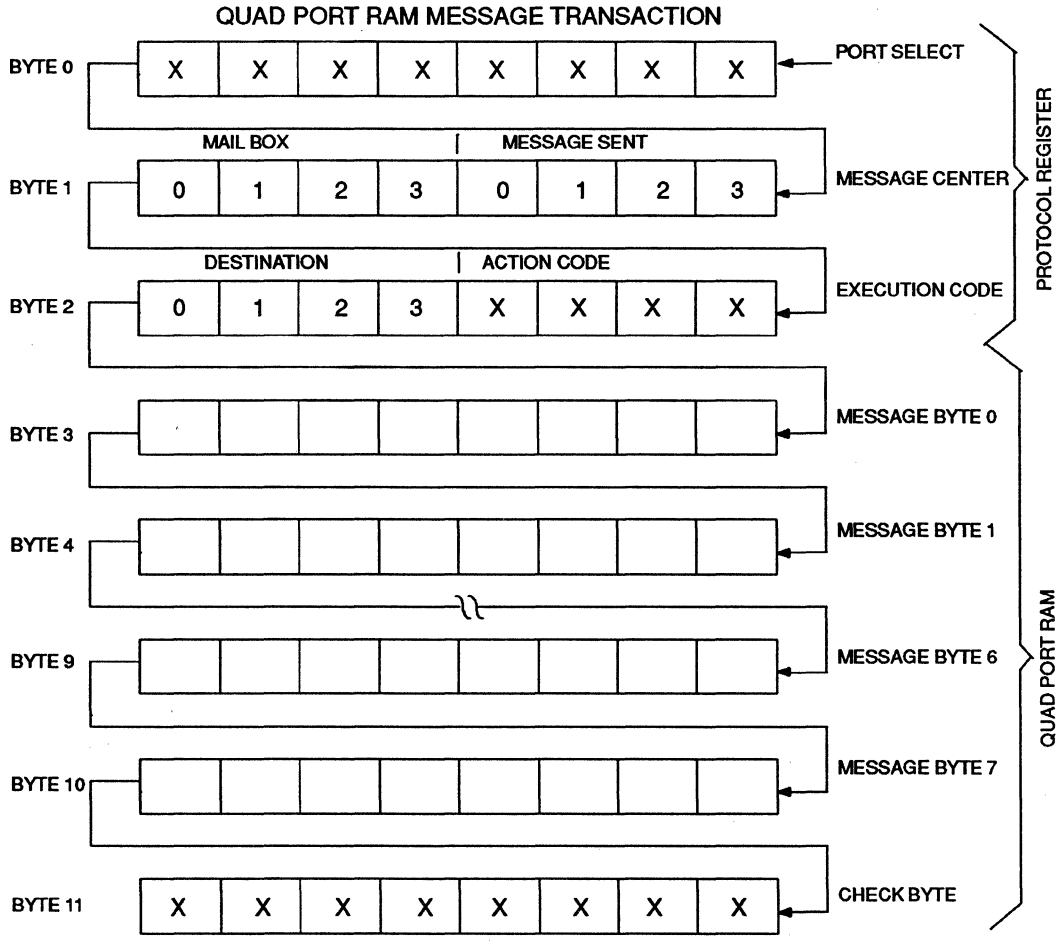
A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

Polling vs. Message Flags

The DS2015 Quad Port Serial RAM Chip has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of

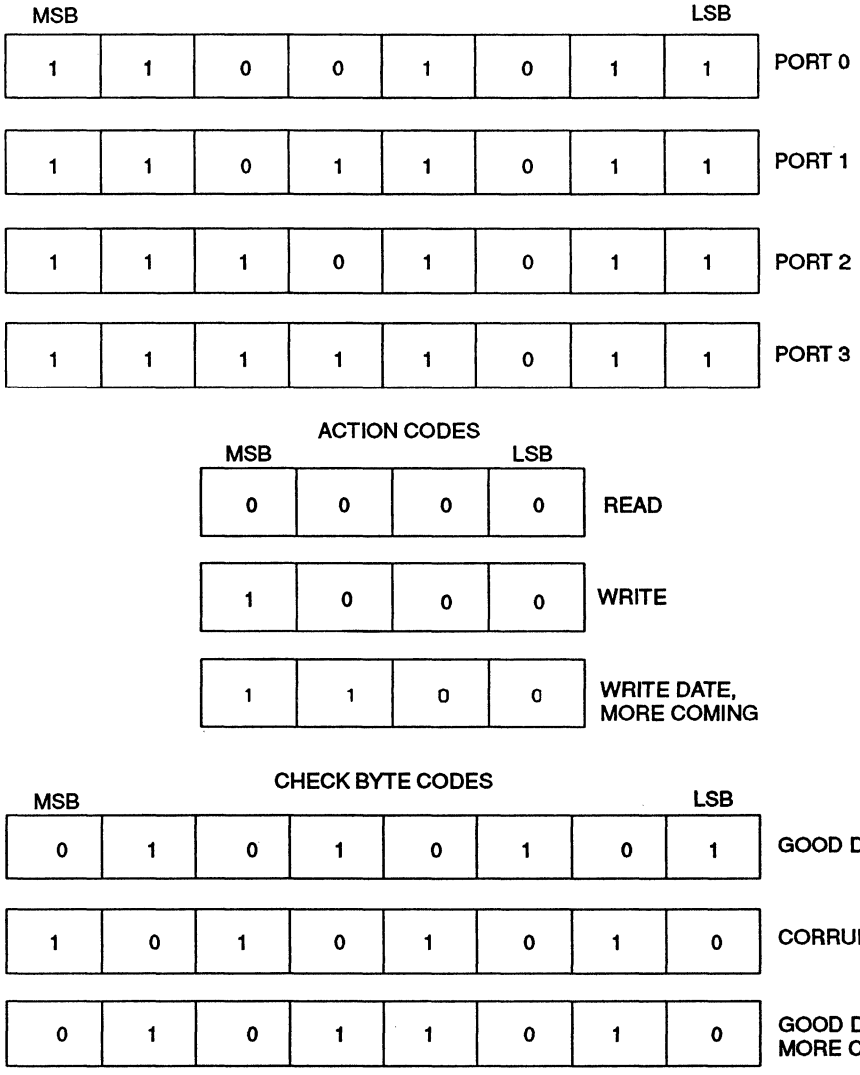
the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the $\overline{RST}$ input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be read. The message ready pins ($\overline{M0}$-$\overline{M3}$) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and $\overline{RST}$ of the sending port is set to the inactive state (low), provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

QUAD PORT RAM MESSAGE TRANSACTION Figure 2



NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE.
BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

PORT SELECT CODE Figure 3



$\overline{\text{RST}}$ Control

All message transactions are initiated by driving the $\overline{\text{RST}}$ port input high. The $\overline{\text{RST}}$ input serves two functions. First, it turns on control logic which allows access to the protocol register. Second, the $\overline{\text{RST}}$ signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

1. While polling the message center for new messages, always terminate the transaction by driving $\overline{\text{RST}}$ low after completing a read of the message center byte and before entering the execution code byte.

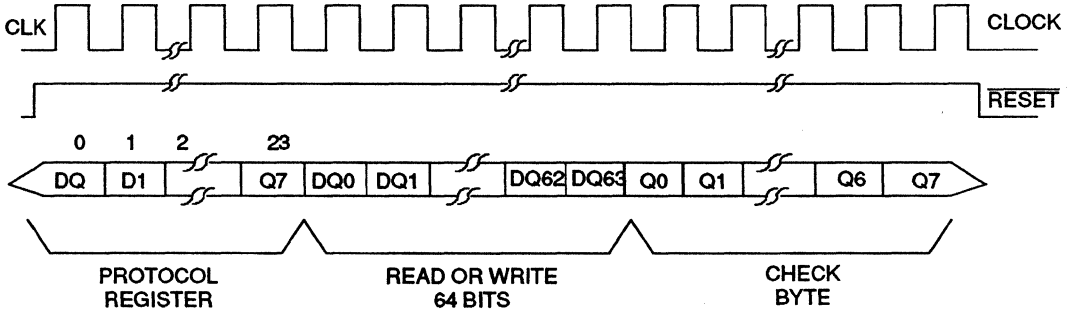
2. When sending a message, all eight message bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

3. When receiving a message, all eight bytes should be read. However, if $\overline{RESET}$ is used to terminate a message which is being read, the message sent bit and the mailbox bit are cleared as $\overline{RST}$ is driven low. When reading a message, the check byte is optional and can be either read or ignored.

CLOCK CONTROL

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be valid during the rising edge of the clock cycle. Protocol bits and message bits are input on the rising edge of the clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if $\overline{RST}$ is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

QUAD PORT MESSAGE TRANSFER Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} +0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
Supply Current	I_{CC}			6	mA	2

3

CAPACITANCE

(t_A=25°C)

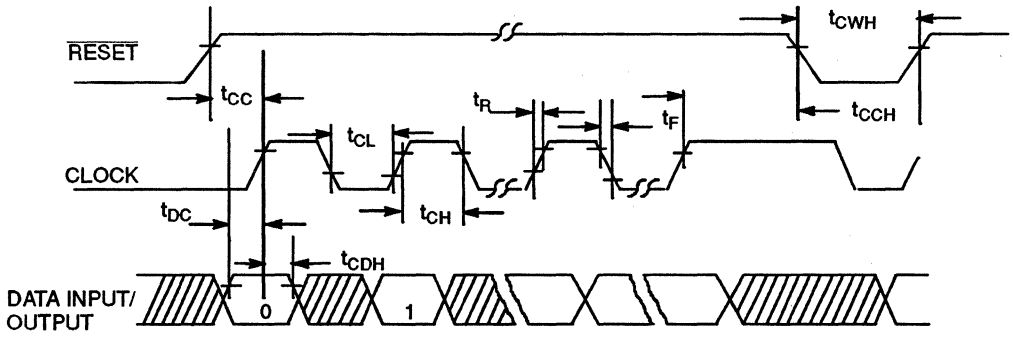
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

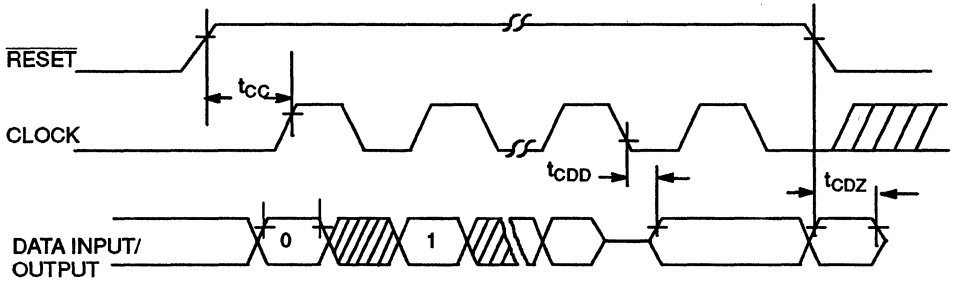
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	
CLK to Data Hold	t_{CDH}	40			ns	
CLK to Data Delay	t_{CDD}			125	ns	
CLK Low Time	t_{CL}	125			ns	
CLK High Time	t_{CH}	125			ns	
CLK Frequency	t_{CLK}	DC		4.0	MHz	
CLK Rise and Fall	t_R, t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	
$\overline{RST}$ to Message Ready	t_{RF}			100	ns	

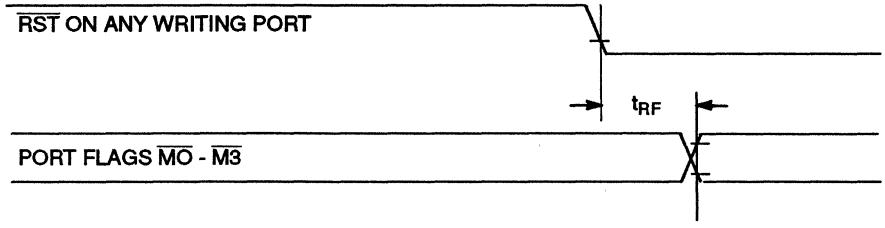
TIMING DIAGRAM-WRITE DATA TRANSFER Figure 5



TIMING DIAGRAM-READ DATA TRANSFER Figure 6



TIMING DIAGRAM-MESSAGE READY Figure 7

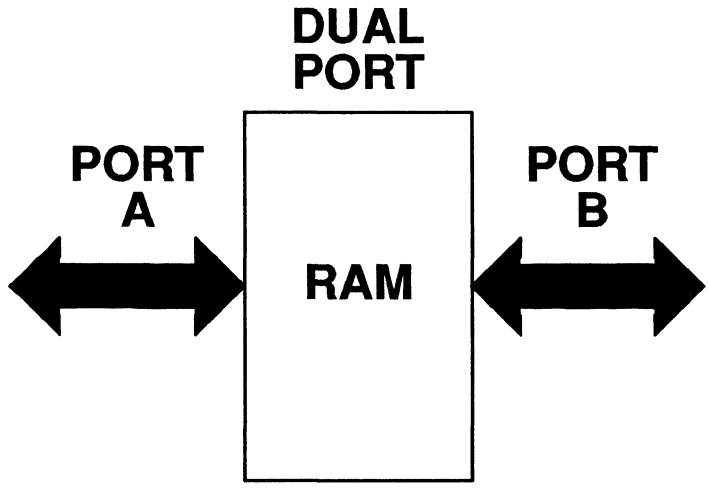


NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.

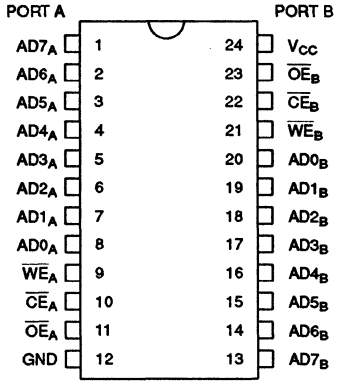
DALLAS SEMICONDUCTOR

Dual Port RAM
Application Note – 62

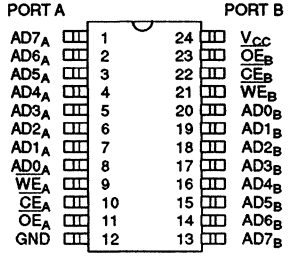


Memory devices and systems are diversifying and becoming more complex out of necessity to support information processing needs. The need to centralize data storage in multiprocessor applications challenges both hardware and software designers. New ways must be found that consolidate system information that is controllable by more than one bus. In addition, systems are becoming more power conscious, particularly portable systems as they typically rely on some kind of rechargeable battery for power. For systems where shared bus access requirements are infrequent, but require many megabytes of memory to be transferred, a shared mass storage device such as a floppy disk drive or networked hard disk drive may suffice. However, for frequent, low density access, media such as hard drives or floppy diskettes are impractical and would greatly slow the rate at which data could be stored and retrieved. The DS1609 Dual Port Ram has been specifically designed to be able to meet high frequency, low volume data storage and retrieval between two asynchronous systems. With its ability to operate at voltages as low as 2.5 volts, the DS1609 also fits easily into any portable application where power availability is limited.

PIN CONFIGURATION



DS1609
24 PIN DIP (600 mil)



DS1609S
24 PIN SOIC (300 mil)

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{CC}	+5 VOLT SUPPLY
GND	GROUND
AD0–AD7	PORT ADDRESS/DATA
$\overline{CE}$	PORT ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE

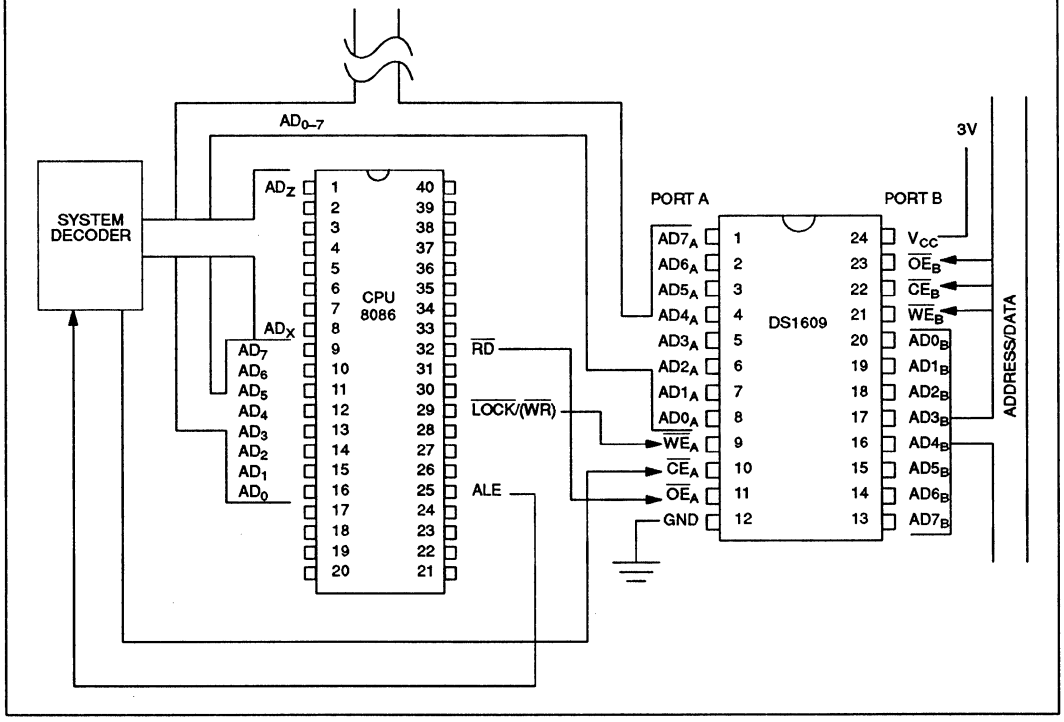
The type of bus which may be connected to either port of the DS1609 is not limited to system level. A multiplexed microprocessor address and data bus can be connected directly to either or both ports of the DS1609. The device can be controlled from either bus port separately by only three signals, $\overline{OE}$, $\overline{CE}$, and $\overline{WE}$. The obvious disadvantage of the multiplexed bus is the slightly reduced system performance because address and data information is being transmitted serially. The equally obvious advantage is the reduced pin count achievable by multiplexing the addressing and data buses.

Read/Write access of either port is transferred as 8 bits address, followed by 8 bits of data. In a read cycle to a port, $\overline{WE}$ is inactive, and the cycle is initiated when $\overline{CE}$ goes active, which with the address latched, data is retrieved under the control of $\overline{OE}$. The rising edge of either $\overline{CE}$ or $\overline{OE}$ terminates the read cycle. For a write cycle, $\overline{OE}$ is inactive, and $\overline{CE}$ becoming active latches the address to be accessed, with $\overline{WE}$ becoming active.

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports. Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or a write from both ports at the same instant. If a write cycle occurs while a read cycle is in progress, the read cycle will likely recover either the old data or new data and not some combination of both. However, the write cycle will update the memory with correct data. Simultaneous write cycles to the same memory location pose the additional concern that the cell may be in contention causing a metastable state. Depending on the timing of the write cycles of port A and port B, the memory location could be left containing the data written from port A or the data from port B or some combination thereof. However, both concerns expressed above can be eliminated by disciplined system software design. A simple way to assure that read/write contention does not occur is to perform redundant read cycles. Write/write contention needs can be avoided by assigning groups of addresses for write operations to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using

a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

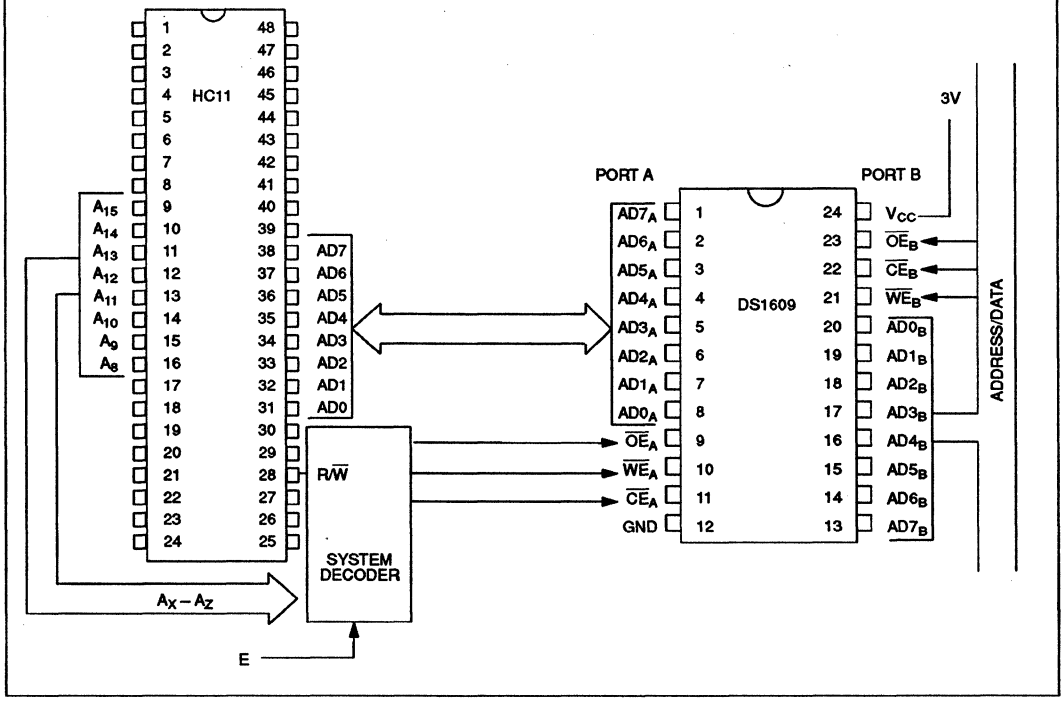
FIGURE 1: DS1609 DUAL PORT INTERFACE TO INTEL 8086 MICROPROCESSOR



The DS1609 is ideally suited for small microprocessor based systems which frequently utilize dedicated 8 bit multiplexed address/data busses the following examples deal with interfacing with the Intel 8086/8088 series and the Motorola HC11 series microprocessors.

For implementation with the Intel 8086/8088 microprocessor family, the address/data pins of either port may be tied directly to the lower 8 address data lines of the Intel 8086 or 8088 microprocessor (Figure 1). The $\overline{RD}$ pin from the microprocessor provides the $\overline{OE}$ input to the port on the DS1609, while $\overline{WR}$ provides the $\overline{WE}$ input to the port. The port's $\overline{CE}$ input may be conditioned by a system decoder, which would require the 8086's ALE output as an input to provide address latching. Several of the unused address/data lines from the 8086 would also be required as inputs to indicate where the DS1609 resides in the system memory map. In applications where multiple DS1609 ports are required, multiple $\overline{CE}$ outputs could be provided from a system decoder using the ALE signal from an Intel 8086/8088 with user specified address lines to generate multiple chip selects (Figure 3).

FIGURE 2: MOTOROLA HC11 EXPANDED MODE



For implementation with the Motorola HC11 microprocessor family, the address/data pins of either port on a DS1609 may be directly ties to port C of an HC11 operating in expanded mode (Figure 2). Address pins from port B of the HC11 ($A_8 - A_{15}$) may be used to provide the DS1609's location in the system memory map. The E signal, which is also an input to the HC11, provides a bus clock to the system decoder indicating whether the HC11 is in an address or data cycle. The R/$\overline{W}$ input to the decoder indicates whether the HC11 is writing or reading data in a data cycle. From these inputs, a system decoder can provide $\overline{OE}$, $\overline{WE}$, and $\overline{CE}$ outputs to DS1609. For applications where more density is required, two DS1609's may be used. The same inputs, including a user selected combination of address lines $A_8 - A_{15}$ can be used to provide $\overline{OE}$, $\overline{WE}$, and multiple $\overline{CE}$ signals for individual DS1609 devices (Figure 4).

The DS1609 may be used with other microprocessors without multiplexed busses, which have a separate address and data bus.

FIGURE 3: MULTIPLEXED INTERFACE

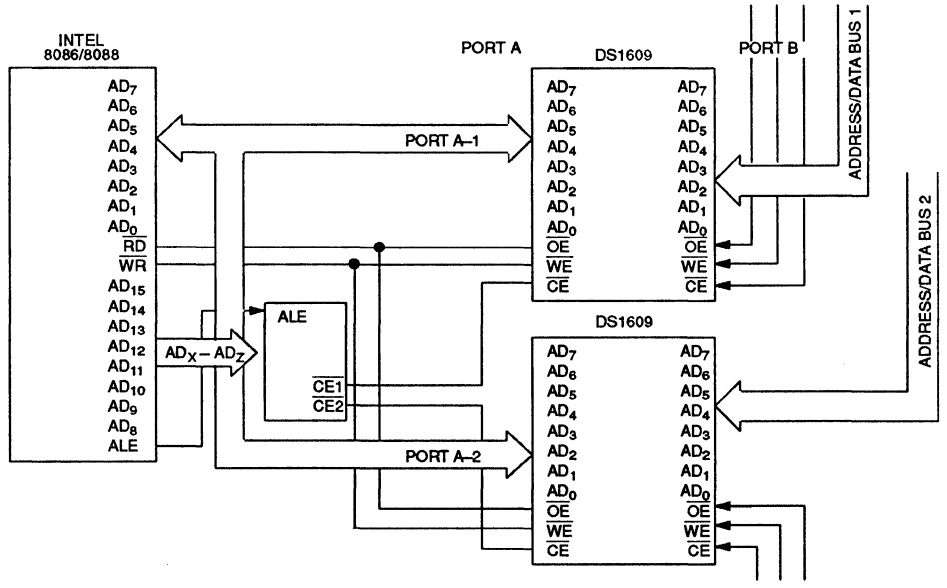
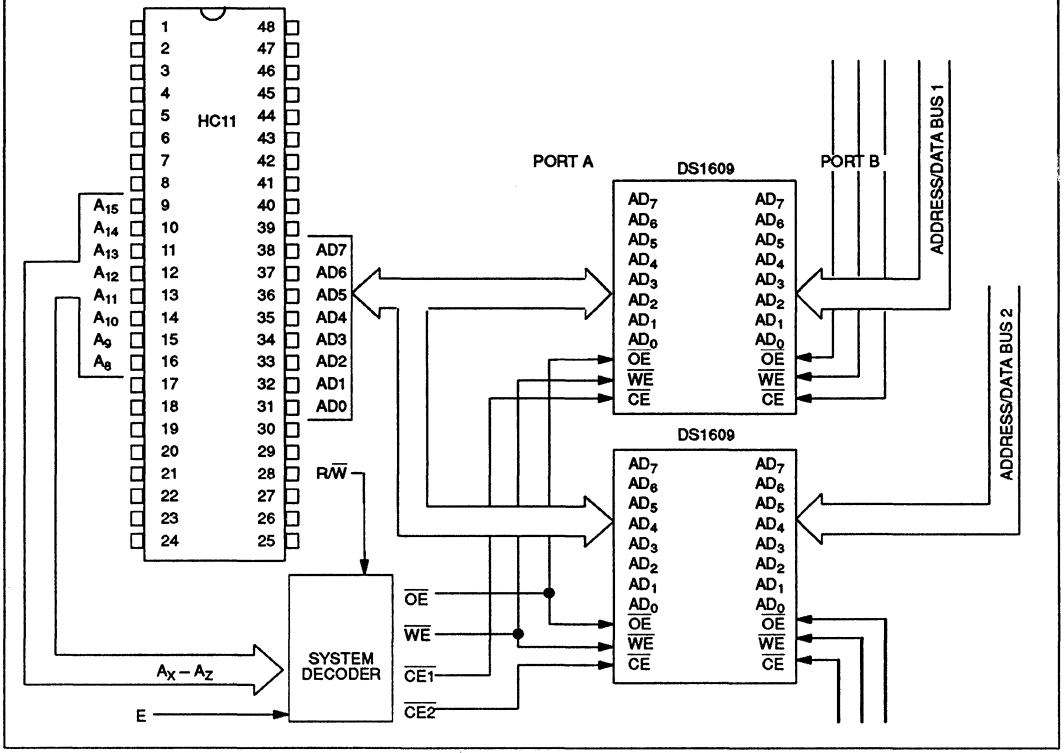
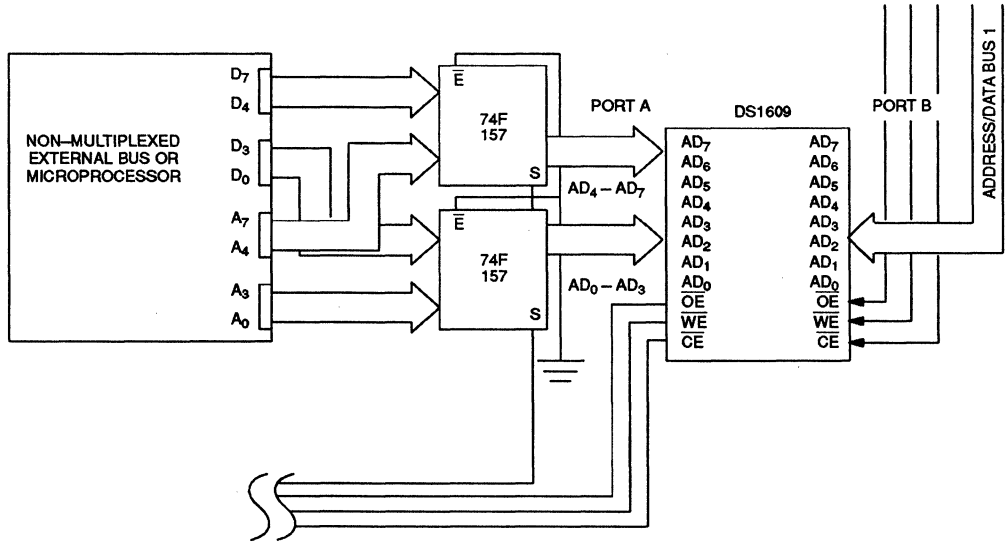


FIGURE 4: MOTOROLA HC11 EXPANDED MODE MULTIPLE DS1609'S



The DS1609 can be used as a go between with non–multiplexed microprocessors such as the Intel 386 or Motorola 68030. Processor cycles to and from a DS1609 must then be multiplexed specifically for the DS1609's address/data/bus. An example implementation is shown below (Figure 5).

FIGURE 5: SAMPLE IMPLEMENTATION; NON–MULTIPLEXED BUS



In this implementation, the lower 8 bits of a microprocessor's address bus and data bus are connected to the multiplexed address and data inputs using two 74F157 quad 2 input multiplexers. Each of the 74F157 devices takes 4 address and 4 data inputs originating from a microprocessor or an external bus master. The 74F157s produce four outputs of multiplexed address/data information which can then be used by a DS1609 port. The $\overline{E}$ inputs of each 74F157 may be tied to ground. The S inputs on the 74F157's become control logic, and direct switching back and forth between passing the address lines or the data lines. Read and write enabling signals must be provided by the microprocessor or external bus master.

IN SUMMARY

The DS1609 Dual Port RAM is tailored for use with 8 bit multiplexed address/data bus microprocessors. The DS1609's unique asynchronous dual port access allows a system design to provide a 256 bytewide registers which may be shared by two independent microprocessors. Multiple DS1609's may be tied together in a system to provide for 3 microprocessors having access to two 256 byte memories. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while providing for the unique asynchronous access. For systems which do not have a multiplexed address/data bus, minimal logic can convert separate address and data lines into a multiplexed address/data bus usable by the DS1609.

Intel, 8086, 8088, and 386 are trademarks of Intel Corporation. Motorola, HC11, and 68030, are trademarks of Motorola, Inc.

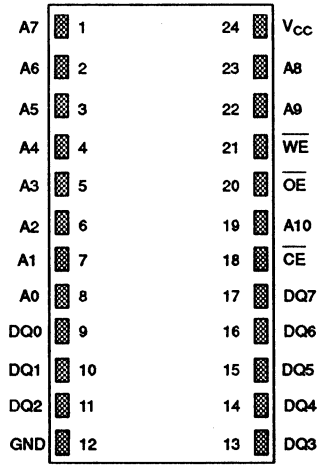
DALLAS SEMICONDUCTOR

DS1220AB/AD
16K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



24-PIN ENCAPSULATED PACKAGE
(720 Mil Extended)

PIN DESCRIPTION

A_0-A_{10}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable

DESCRIPTION

The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220AB/AD also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

SHIPPING AND START-UP

The DS1220AB/AD is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10% for DS1220AD)
(0°C to 70°C; V_{CC}=5V ± 5% for DS1220AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V	

DC TEST CONDITIONS

Outputs open.
All voltages are referenced to ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10% for DS1220AD)
(0°C to 70°C; V_{CC}=5.0V ± 5% for DS1220AB)

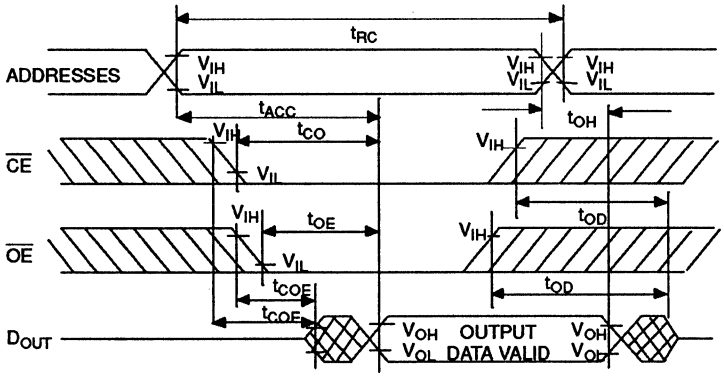
		DS1220AB/AD-100		DS1220AB/AD-120		DS1220AB/AD-150		DS1220AB/AD-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTE
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		5		ns	5

		DS1220AB/AD-100		DS1220AB/AD-120		DS1220AB/AD-150		DS1220AB/AD-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTE**
Output High Z from Deselection	t_{OD}		35		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH}	10		10		10		10		ns	4

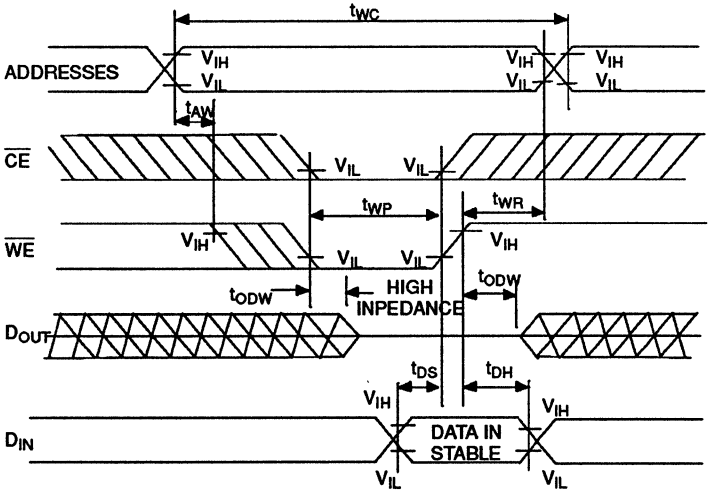
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

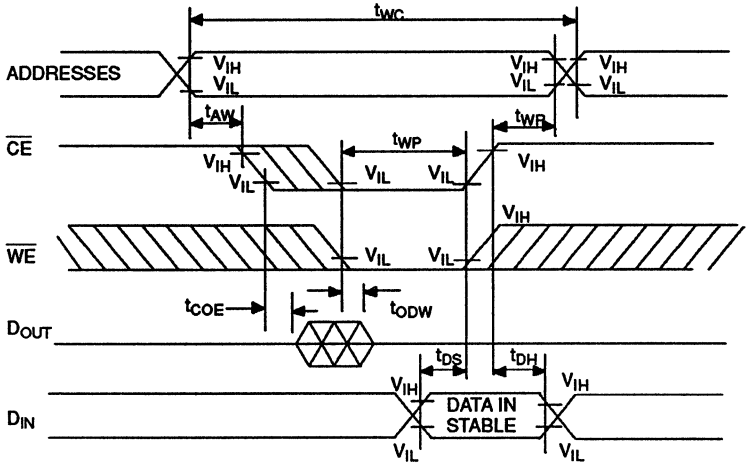
READ CYCLE (1)



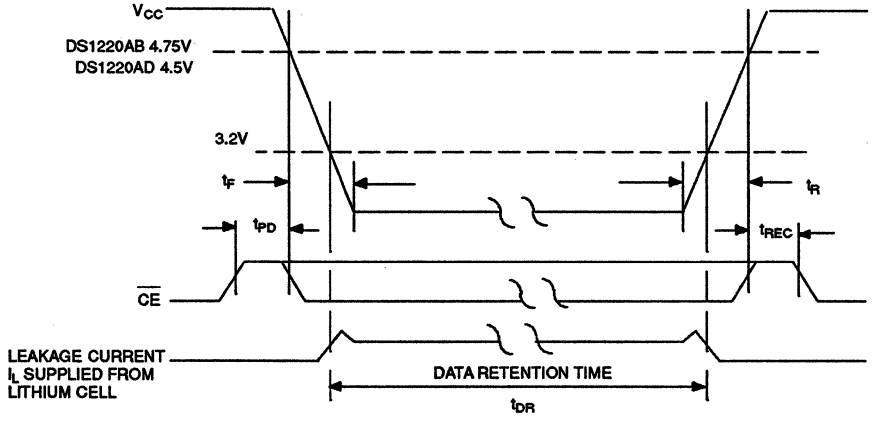
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1220AB
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1220AD
t_R	V_{CC} Slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		µs	DS1220AB
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	DS1220AD
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

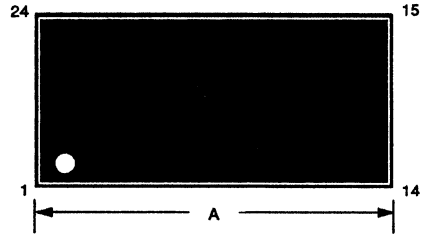
(t_A=25°C)

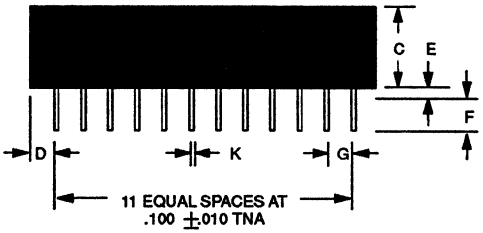
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

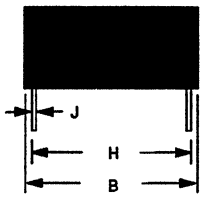
WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

NOTES:
1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1220AB/AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1220AB/AD NV SRAM 24-PIN (720MIL)







PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.340
MM	33.53	34.04
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.390	0.415
MM	9.91	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

4

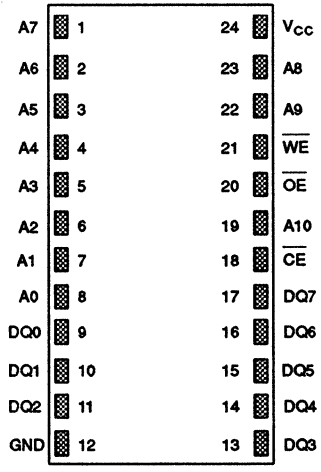
DALLAS SEMICONDUCTOR

DS1220Y
16K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ± 10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



24-Pin Encapsulated Package
(720 mil Extended)

PIN DESCRIPTION

A_0-A_{10}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable

DESCRIPTION

The DS1220Y 16K Nonvolatile SRAM is a 16,384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1220Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		2.0	4.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

AC ELECTRICAL CHARACTERISTICS

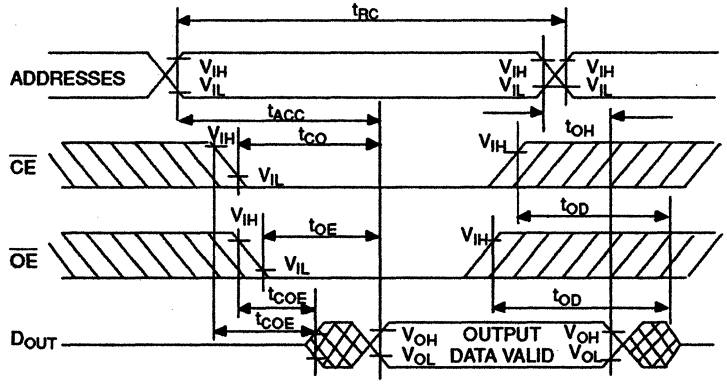
(0°C to 70°C, V_{CC}=5.0V ± 10%)

		DS1220Y-100		DS1220Y-120		DS1220Y-150		DS1220Y-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTE**
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH}	10		10		10		10		ns	4

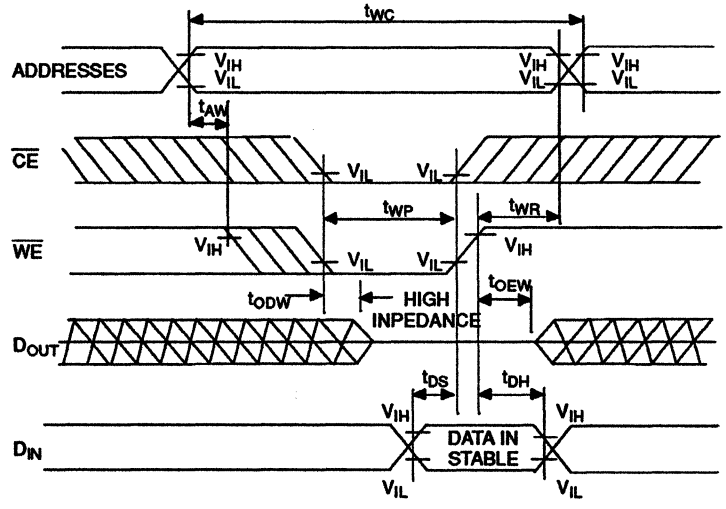
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

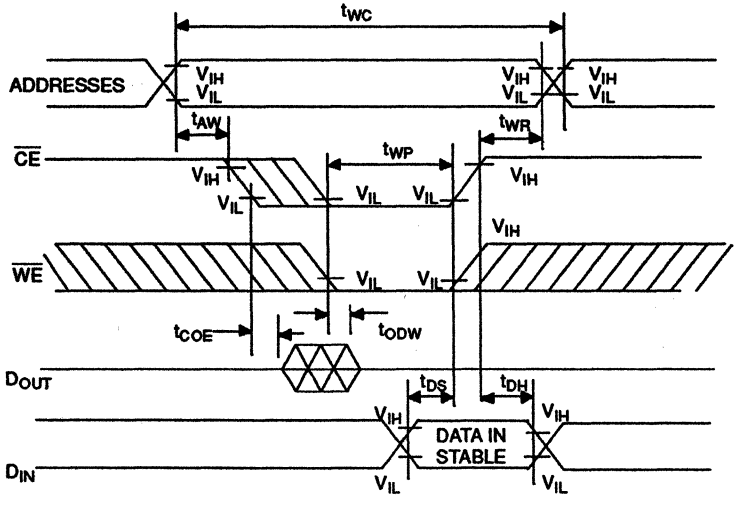
READ CYCLE (1)



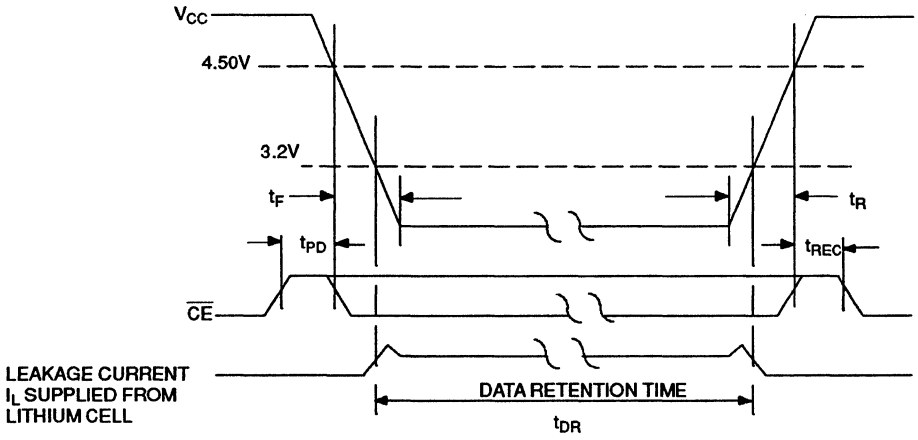
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		µs	
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up		2	ms	

(t_A = 25°C)

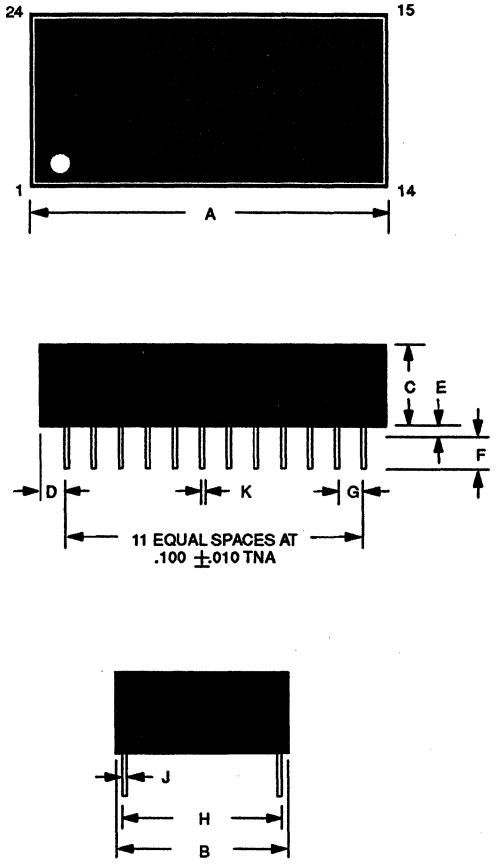
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage of V_{CC}.

DS1220Y NV SRAM 24-PIN (720MIL)



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.340
MM	33.53	34.04
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.390	0.415
MM	9.91	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

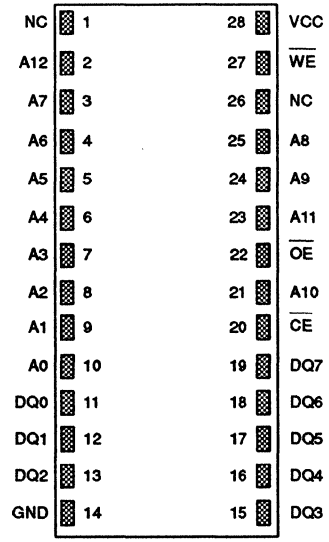
DALLAS SEMICONDUCTOR

DS1225AB/AD
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 150ns, 170ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-Pin Encapsulated Package
(720 Mil Extended)

PIN DESCRIPTION

A0 - A12	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

DESCRIPTION

The DS1225AB and DS1225AD 64K Nonvolatile SRAMs are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data.

The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225AB/AD also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225AB and DS1225AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1225AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The NV SRAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225AD and 4.75 volts for the DS1225AB.

FRESHNESS SEAL

The DS1225AB and DS1225AD are shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10% for DS1225AD)
(0°C to 70°C; V_{CC}=5V ± 5% for DS1225AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE}>V_{IH}<V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

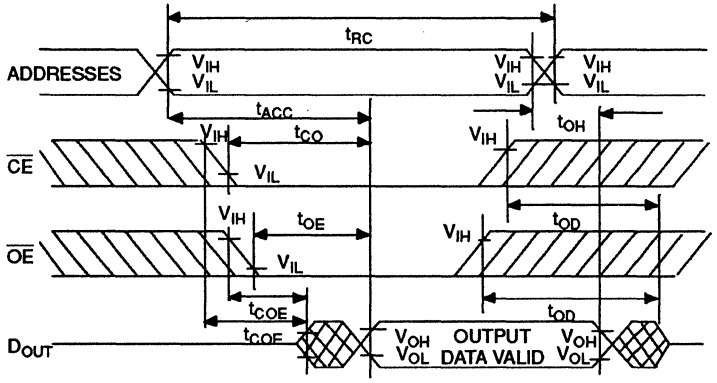
(0°C to 70°C; V_{CC}=5.0V ± 10% for DS1225AD)
(0°C to 70°C; V_{CC}=5.0V ± 5% for DS1225AB)

		DS1225-150		DS1225-170		DS1225-200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		170		200		ns	
Access Time	t_{ACC}		150		170		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		80		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		170		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	150		170		200		ns	
Write Pulse Width	t_{WP}	100		120		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	60		70		80		ns	4
Data Hold Time	t_{DH}	10		10		10		ns	4

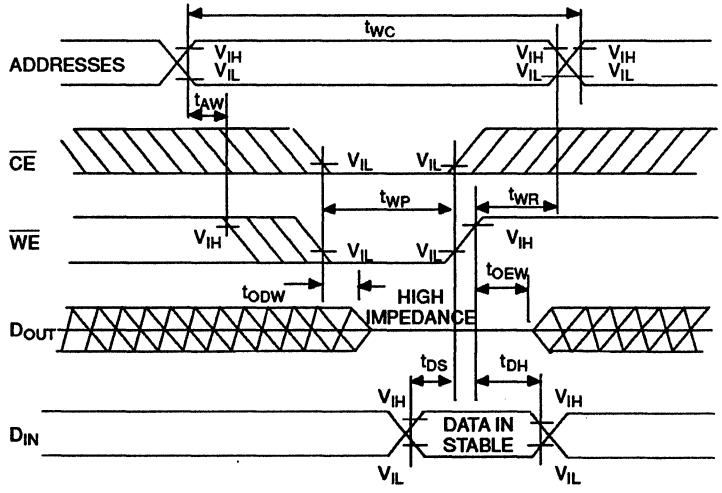
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

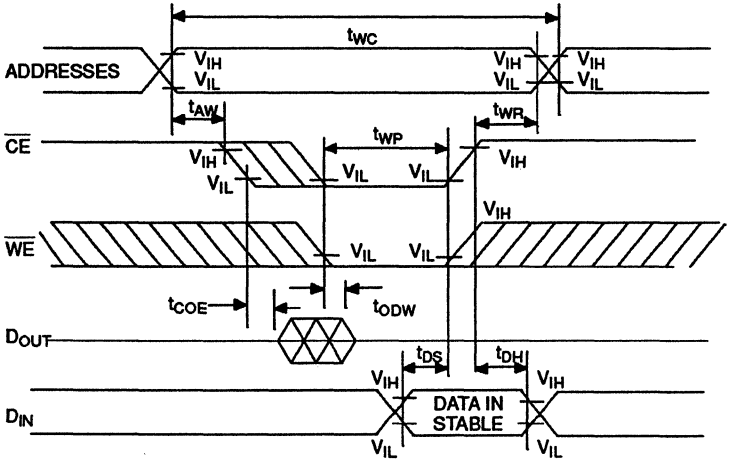
READ CYCLE (1)



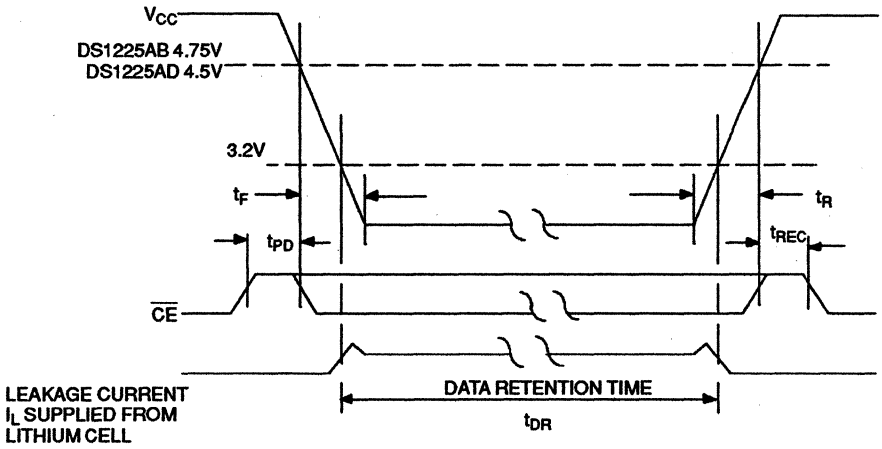
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225AB
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225AD
t_R	V_{CC} Slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		µs	DS1225AB
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	DS1225AD
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

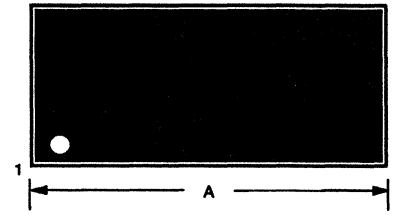
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

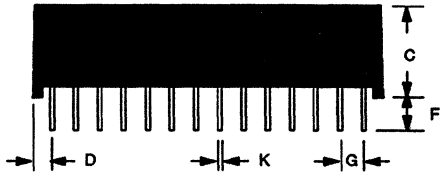
WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

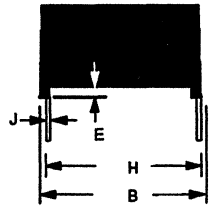
NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225AB/AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1225AB/AD NONVOLATILE SRAM 28-PIN 720 MIL MODULE







PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

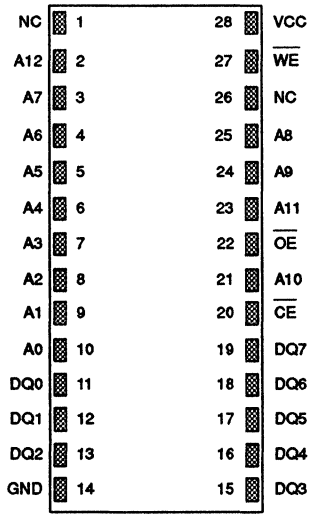
DALLAS SEMICONDUCTOR

DS1225D/E
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, or 120 ns read access times
- Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-Pin Encapsulated Package
(740 Mil Flush Bottom)

PIN DESCRIPTION

A0 - A12	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

NOTE: Pins 1 & 26 missing by design

DESCRIPTION

The DS1225D and DS1225E are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225D/E also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225D/E executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225D/E are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225E provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1225D provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225D/E constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225D and 4.75 volts for the DS1225E.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225D Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
DS1225E Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10% for DS1225D)
(0°C to 70°C; V_{CC}=5V ± 5% for DS1225E)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE}$>V_{IH} <V_{CC}	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=100ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=100ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225D)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225E)	V_{TP}	4.25	4.37	4.5	V	

DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground.

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

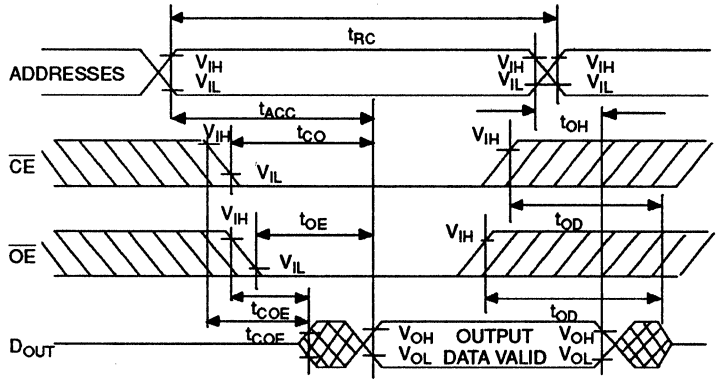
(0°C to 70°C; V_{CC}=5.0V + 10% for DS1225D)
(0°C to 70°C; V_{CC}=5.0V ± 5% for DS1225E)

		DS1225D/E-70		DS1225D/E-85		DS1225D/E-100		DS1225D/E-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	70		85		100		120		ns	
Access Time	t_{ACC}		70		85		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		25		25		25	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		120		ns	
Write Pulse Width	t_{WP}	55		65		75		90		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		25		25		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		50		ns	4
Data Hold Time	t_{DH}	10		10		10		10		ns	4

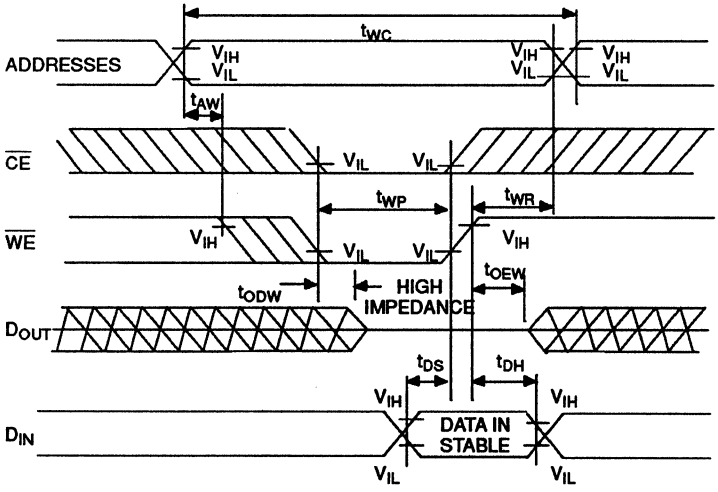
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 – 3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

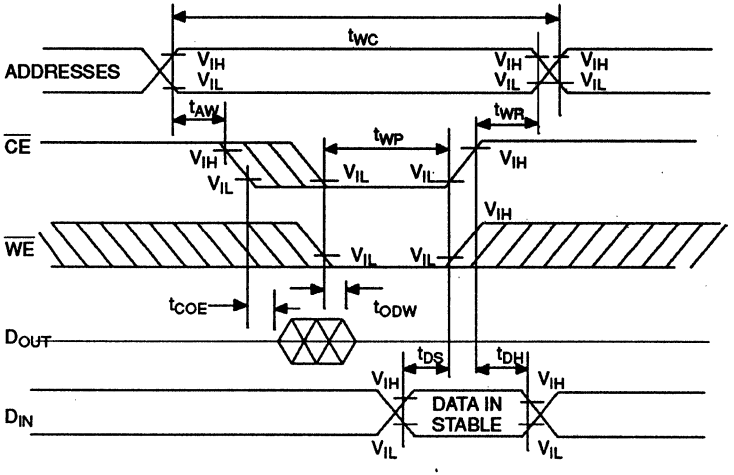
READ CYCLE (1)



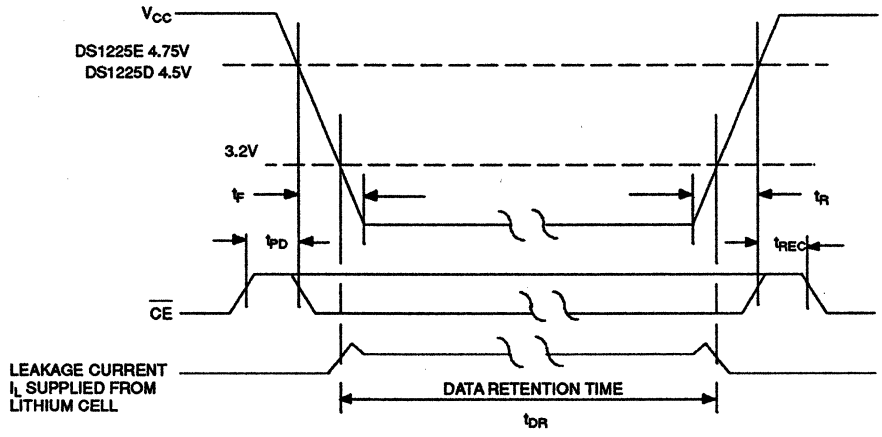
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225E
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	DS1225D
t_R	V_{CC} Slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		µs	DS1225E
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	DS1225D
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

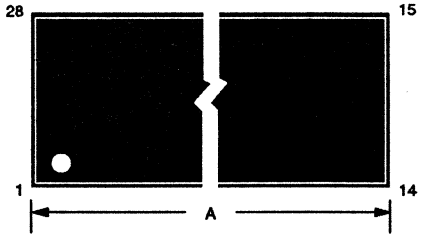
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

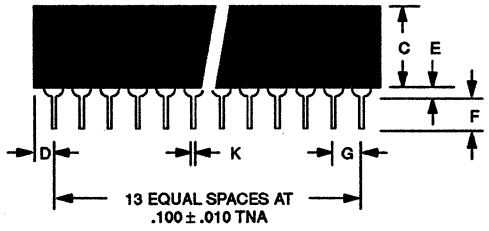
WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

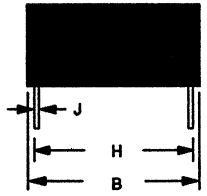
NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225D/E is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1225D/E NONVOLATILE SRAM 28-PIN 740 MIL MODULE







PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.520 38.61	1.540 39.12
B IN. MM	0.695 17.65	0.720 18.29
C IN. MM	0.350 8.89	0.375 9.53
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

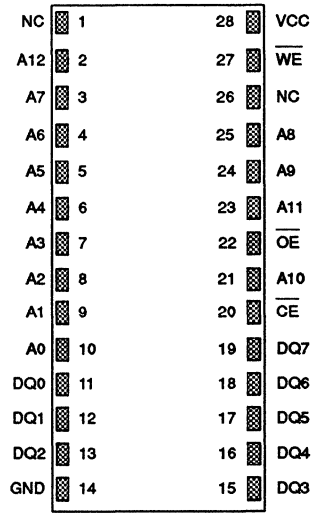
DALLAS SEMICONDUCTOR

DS1225Y
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 150ns, 170ns, or 200ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-Pin Encapsulated Package
(720 Mil Extended)

PIN DESCRIPTION

A_0 - A_{12}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

DESCRIPTION

The DS1225Y 64K Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to +70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	10	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3	5	mA	
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	10

DC TEST CONDITIONS

Outputs open.
All voltages are referenced to ground.

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=5.0V ± 10%)

		DS1225Y-150		DS1225Y-170		DS1225Y-200			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	150		170		200		ns	
Access Time	t_{ACC}		150		170		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		80		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		170		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	150		170		200		ns	
Write Pulse Width	t_{WP}	100		120		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	60		70		80		ns	4
Data Hold Time	t_{DH}	10		10		10		ns	4

AC TEST CONDITIONS

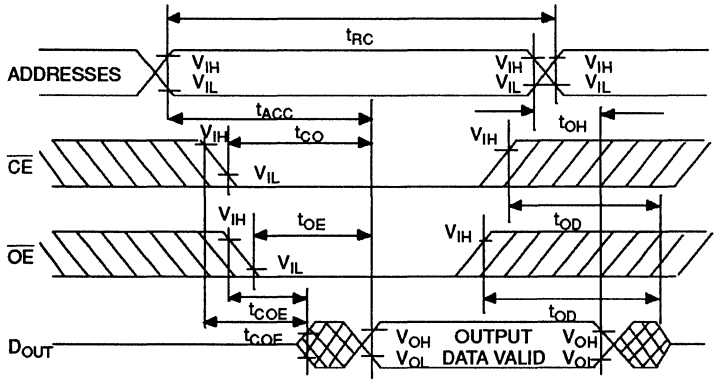
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

CAPACITANCE

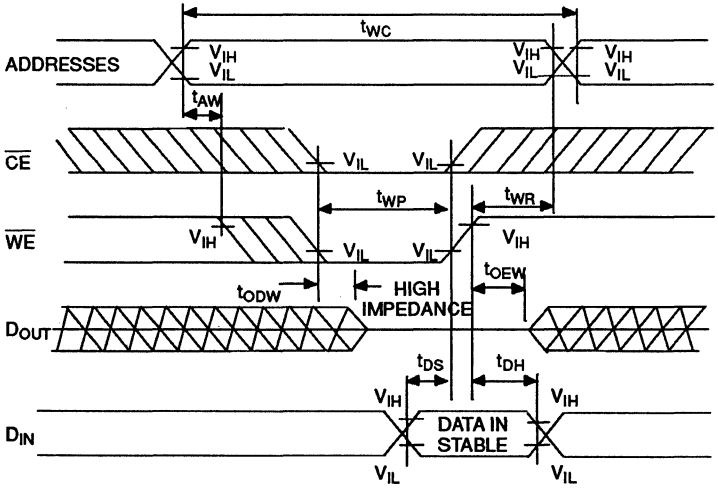
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		10	pF	
Input/Output Capacitance	$C_{I/O}$		10	pF	

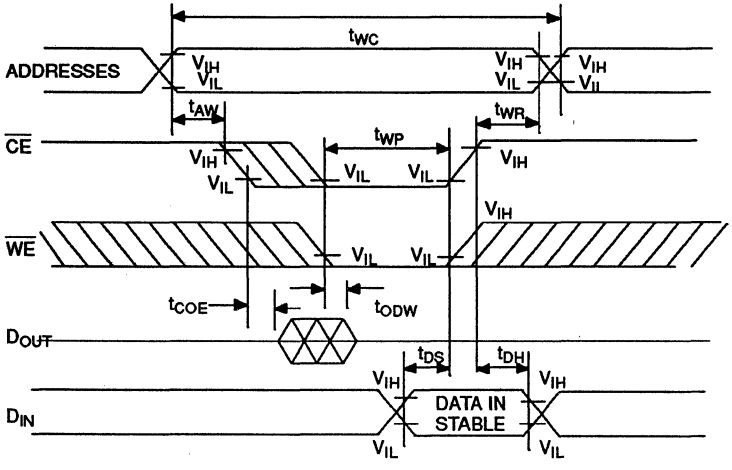
READ CYCLE (1)



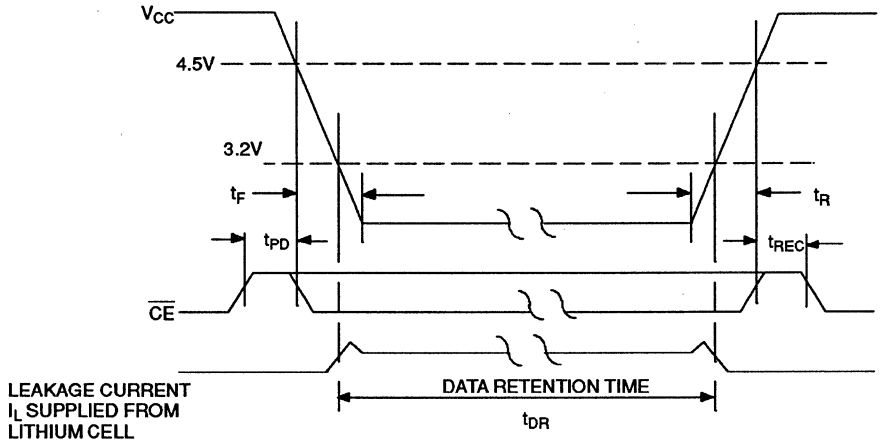
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		µs	
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up		2	ms	

($t_A = 25°C$)

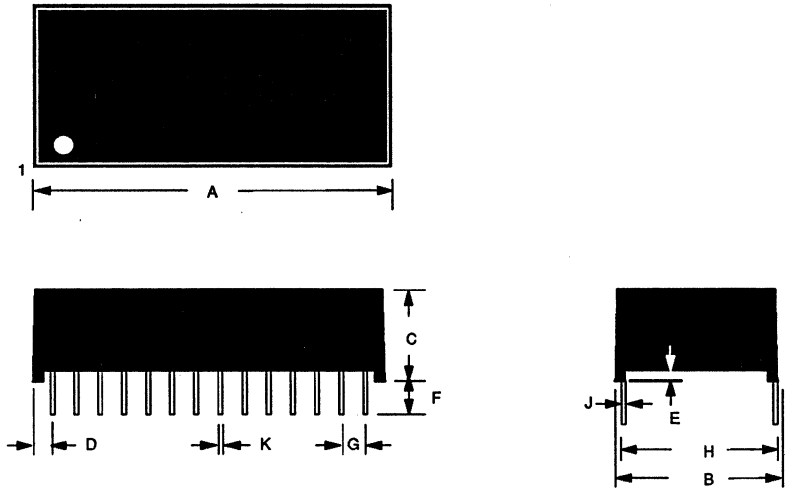
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1225Y NONVOLATILE SRAM 28-PIN 720 MIL MODULE



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

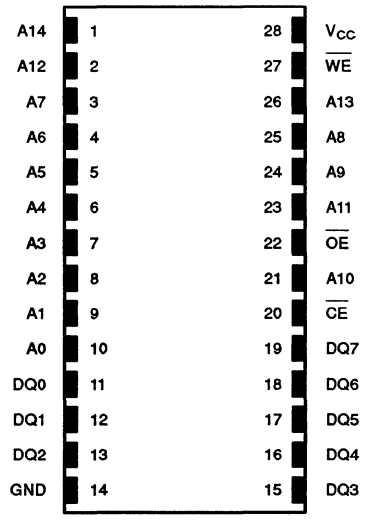
DALLAS SEMICONDUCTOR

DS1230Y/AB
256K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during the decrease in V_{CC} at power loss
- Directly replaces 32K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, 120, 150, or 200 ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A14	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable

DESCRIPTION

The DS1230AB and DS1230Y 256K Nonvolatile SRAMs are a 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 32K x 8 static RAMs directly conforming to the popular bytewide 28 pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

READ MODE

The DS1230Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1230Y/AB is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for DS1230Y and 4.75 volts for the DS1230AB.

FRESHNESS SEAL AND SHIPPING

The DS1230Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

BATTERY REDUNDANCY

Battery redundancy is provided to ensure reliability. The DS1230Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C, -40°C TO +85°C FOR IND PARTS
STORAGE TEMPERATURE	-40°C TO +70°C, -40°C TO +85°C FOR IND PARTS
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		0.8	V	

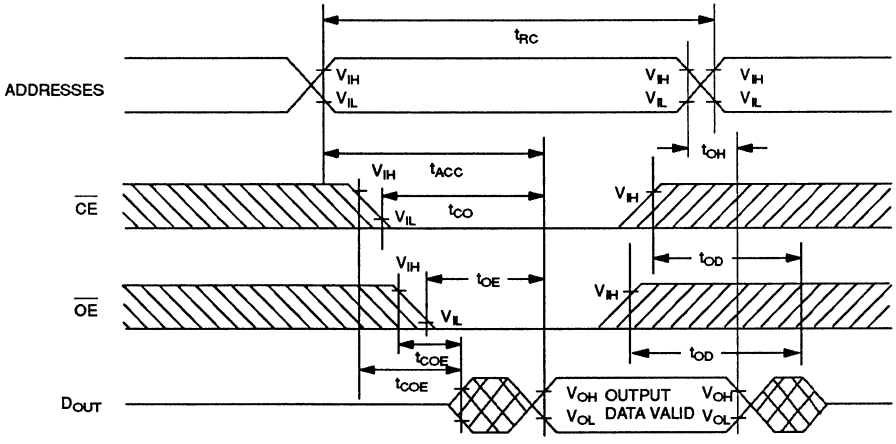
DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1230AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1230Y)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1230AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1230AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1230Y)									
PARAMETER	SYMBOL	DS1230Y-70 DS1230AB-70		DS1230Y-85 DS1230AB-85		DS1230Y-100 DS1230AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Access Time	t_{ACC}		70		85		100	ns	
OE to Output Valid	t_{OE}		35		45		50	ns	
CE to Output Valid	t_{CO}		70		85		100	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	15		15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		30		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	15		15		15		ns	4

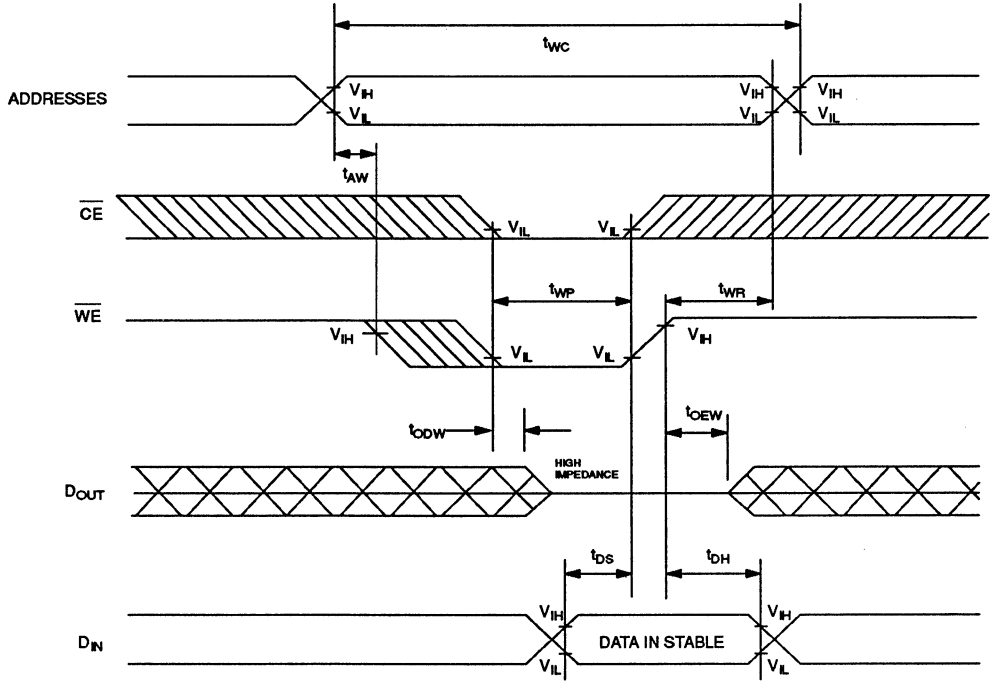
AC ELECTRICAL CHARACTERISTICS - (CONTINUED)									
PARAMETER	SYMBOL	DS1230Y-120 DS1230AB-120		DS1230Y-150 DS1230AB-150		DS1230Y-200 DS1230AB-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
OE to Output Valid	t_{OE}		60		70		100	ns	
CE to Output Valid	t_{CO}		120		150		200	ns	
OE or CE to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		100		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	15		15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	15		15		15		ns	4

READ CYCLE



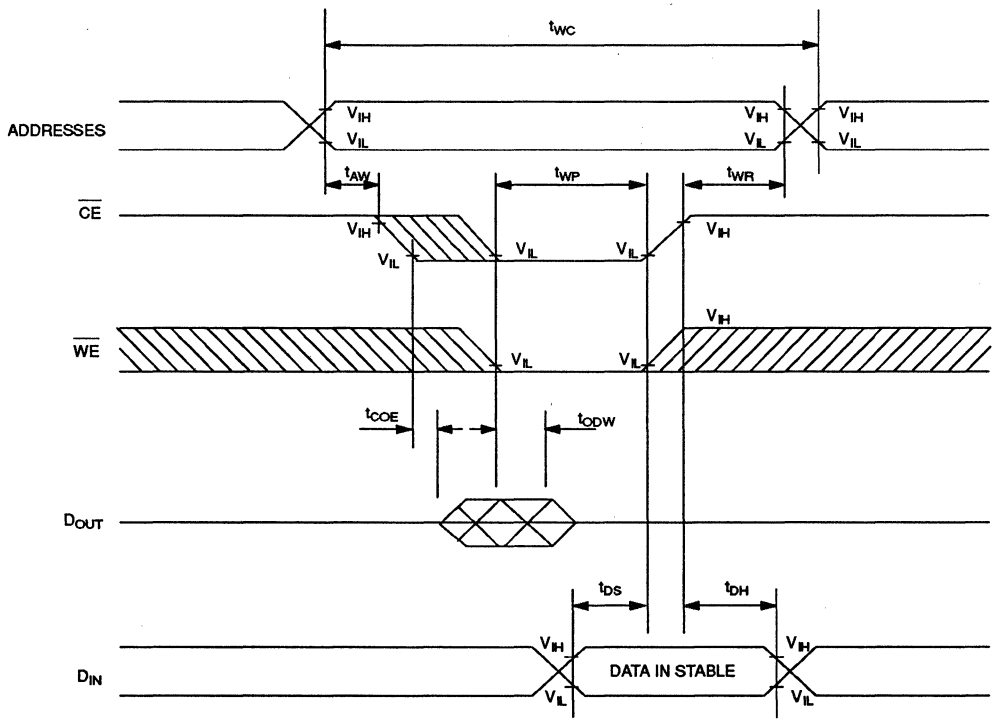
SEE NOTE 1

WRITE CYCLE 1



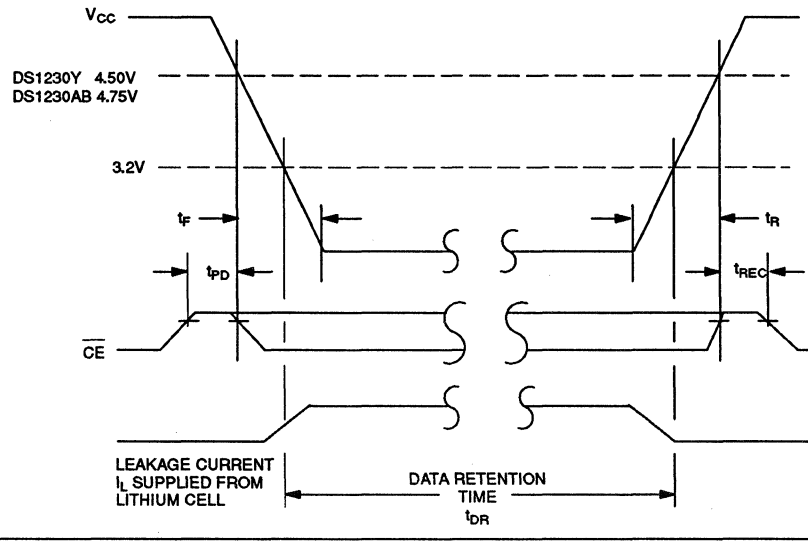
SEE NOTES 2, 6, 7, AND 8

WRITE CYCLE 2



SEE NOTES 2, 6, 7, AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE, at V_{IH} before Power-Down	t_{PD}	0			µs	12
V_{CC} slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	DS1230AB
V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	DS1230Y
V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	DS1230Y
V_{CC} slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	t_R	0			µs	DS1230Y
CE, at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9, 11

WARNING

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1230Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

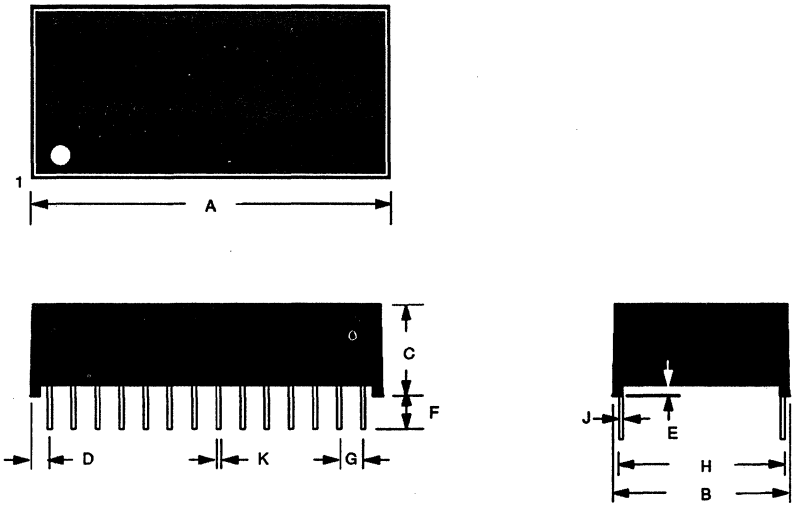
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1230Y/AB NONVOLATILE SRAM 28 PIN 740 MIL MODULE



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

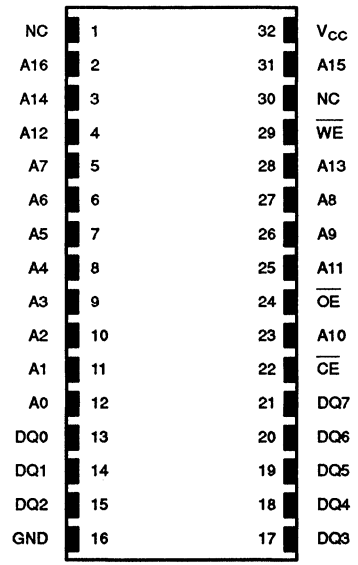
DALLAS SEMICONDUCTOR

DS1245Y/AB
1024K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in 70, 85, 100 or 120 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1245Y)
- Optional ±5% operating range (DS1245AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A16	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

DESCRIPTION

The DS1245Y/AB 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1245Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION - READ MODE

The DS1245Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE MODE

The DS1245Y/AB is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1245AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1245Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1245AB).

FRESHNESS SEAL AND SHIPPING

The DS1245Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

BATTERY REDUNDANCY

Battery redundancy is provided to ensure reliability. The DS1245Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C, –40°C TO + 85°C FOR IND PARTS
STORAGE TEMPERATURE	-40°C TO +70°C, –40°C TO +85°C FOR IND PARTS
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1245Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1245AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1245AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1245Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE} = V_{CC}$-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1245Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1245AB)	V_{TP}	4.50	4.62	4.75	V	

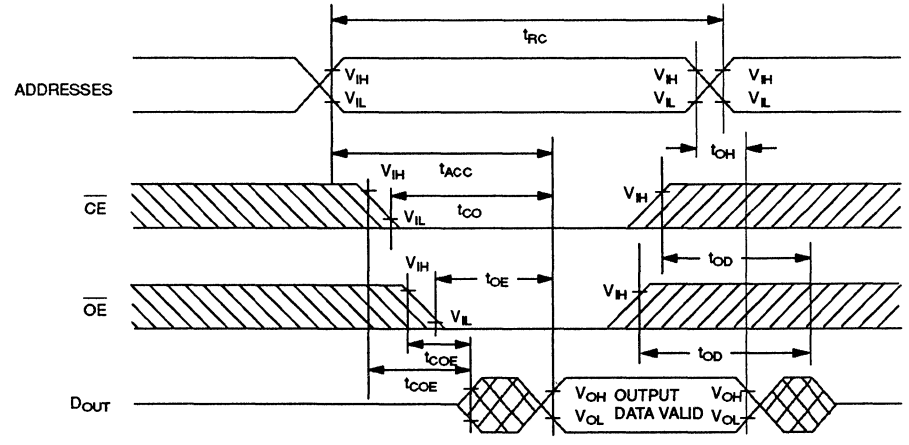
CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1245AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1245Y)					
PARAMETER	SYMBOL	DS1245Y/AB-70		DS1245Y/AB-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH}	15		15		ns	4

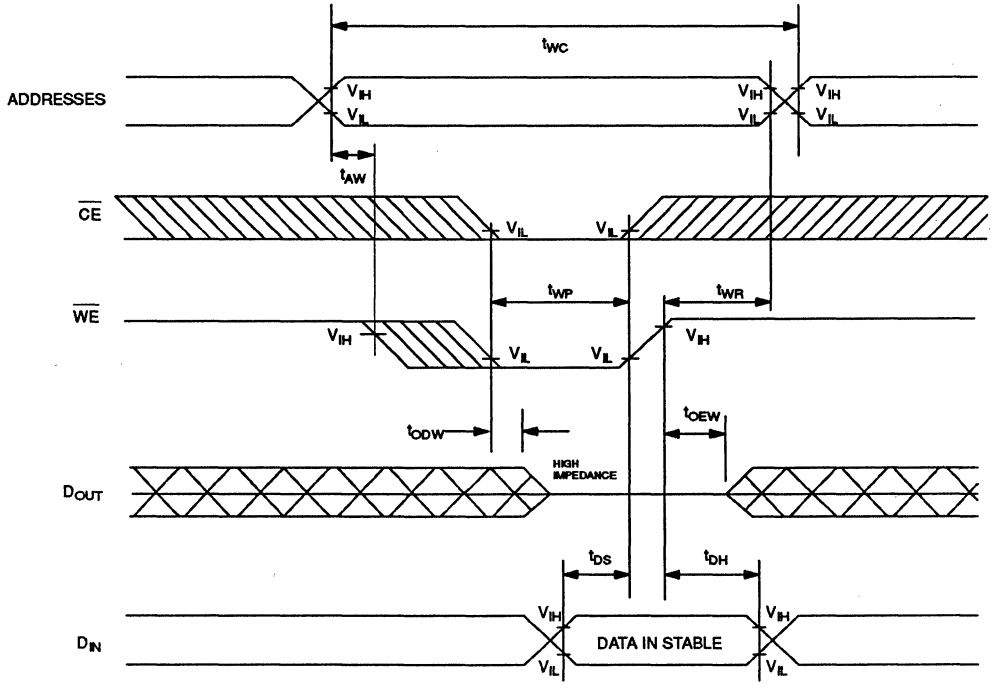
AC ELECTRICAL CHARACTERISTICS - (CONTINUED)							
PARAMETER	SYMBOL	DS1245Y/AB-100		DS1245Y/AB-120		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH}	15		15		ns	4

READ CYCLE



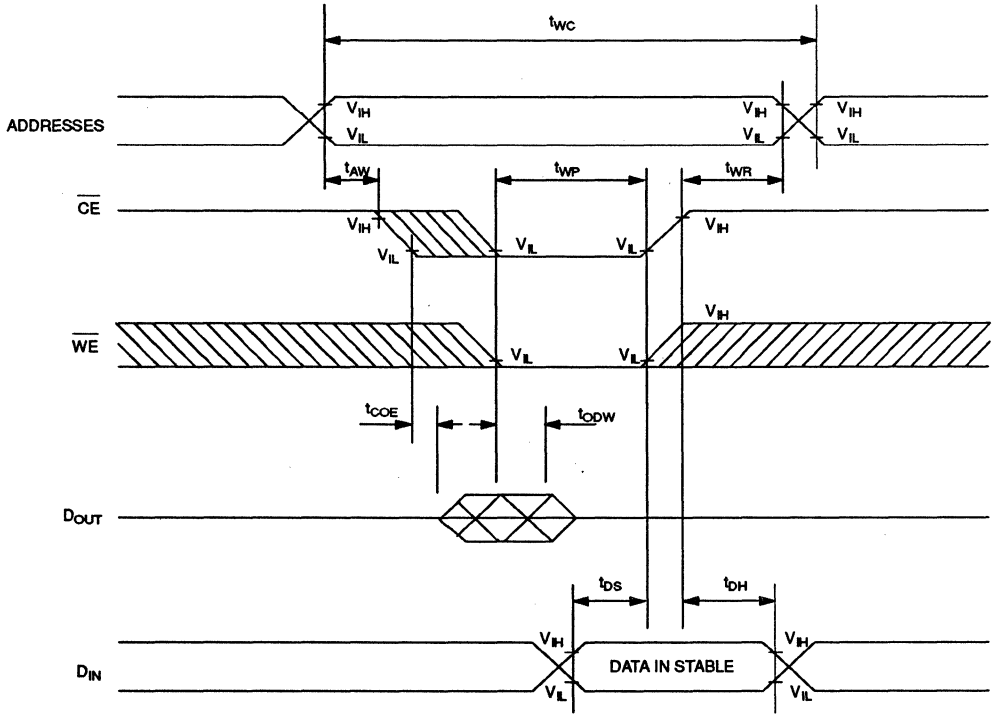
SEE NOTE 1

WRITE CYCLE 1



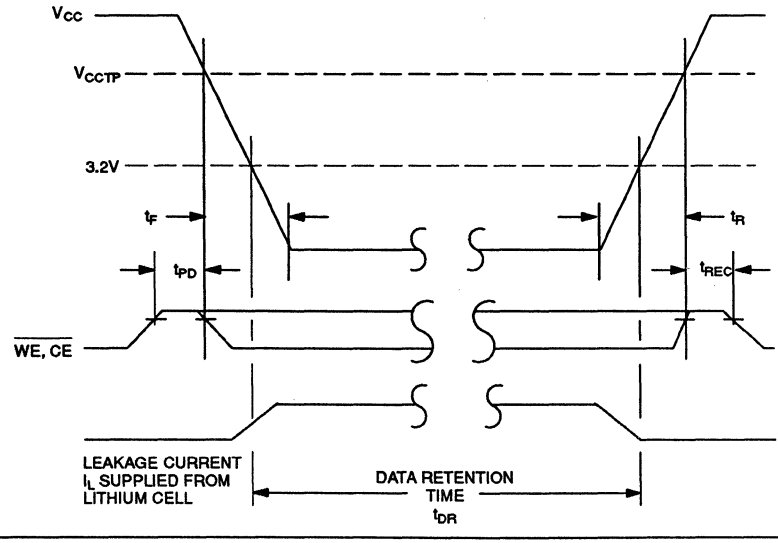
SEE NOTES 2, 6, 7, AND 8

WRITE CYCLE 2



SEE NOTES 2, 6, 7, AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING					
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	0		µs	12
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)					
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9, 11

4

WARNING

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1245Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

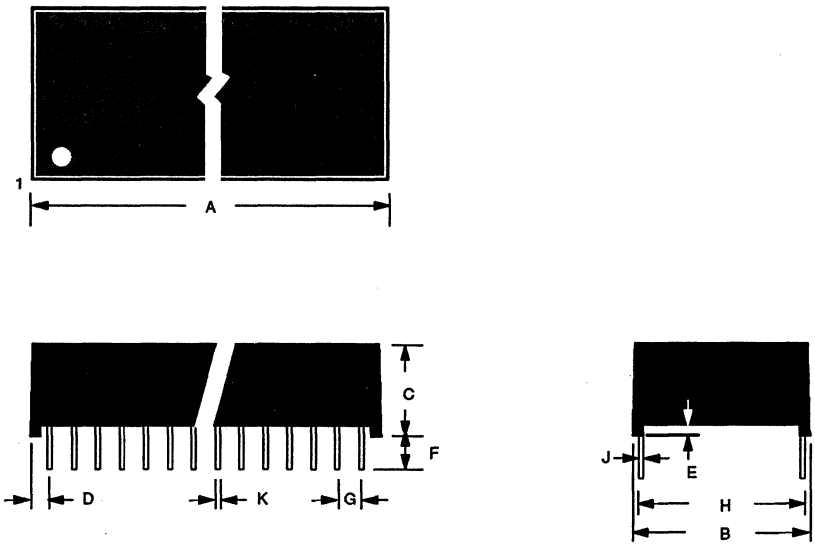
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1245Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

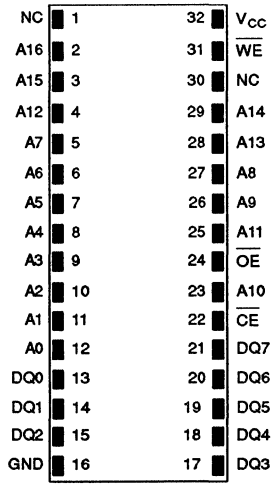
DALLAS SEMICONDUCTOR

DS1245EE
1M Write-Protected NV SRAM

FEATURES

- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Data retention in the absence of V_{CC}
- Directly replaces 128K x 8 EPROM, EEPROM, or FLASH
- Unlimited write cycles
- Standard 32-pin JEDEC pinout
- Available in 120 or 100 read access time
- Full ±10% operating range
- Read cycle time equals write cycle time

PIN ASSIGNMENT



32-Pin Encapsulated Package
(740 Mil Extended)

PIN DESCRIPTION

A0-A16	Address Lines
D0-D7	Data Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
NC	No Connect

DESCRIPTION

The DS1245EE is a 1,048,576-bit fully static, nonvolatile SRAM organized as 131,072 words by 8 bits with a software controlled write inhibit function. The nonvolatile memory has a self-contained lithium energy source and control circuit which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. Two software selectable switches are provided which are capable of inhibiting both the write enable to the RAM and the battery back-up circuitry through a pattern recognition sequence across four address lines. The first switch can inhibit the write enable to the nonvolatile SRAM. This can provide data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery back-up is not needed. The device can be used in place of existing 128K x 8 EPROM, EEPROM, or FLASH conforming to the popular bytewide 32-pin JEDEC standard. There is no limit on the number of write cycles which can be executed and no additional circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1245EE executes a read cycle whenever $\overline{CE}$ (Chip Enable) is active (low) and $\overline{OE}$ (Output Enable) is active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within (t_{ACC}) after the last address input signal is stable, providing that the $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either to for $\overline{CE}$ or t_{OE} for $\overline{CE}$, rather than address access.

WRITE MODE

The DS1245EE is in the write mode only if it has been enabled by the user in software. If activated, a write will occur whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active state (low). The latter occurring falling edge of $\overline{CE}$ (Chip Enable) or $\overline{WE}$ (Write Enable) will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ (Chip Enable) or $\overline{WE}$ (Write Enable). All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ (Write Enable) must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ (Output Enable) control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ enabled) then $\overline{WE}$ (Write Enable) will disable the output buffers in t_{OWD} from its falling edge.

WRITE INHIBIT MODE

The DS1245EE provides two software selectable switches for control of the write enable and nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (See Tables 1 and 2). Prior to entering the pattern recognition sequence which will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointers. Each four-bit compare nibble is clocked into the DS1245EE in the falling edge of $\overline{CE}$ (Chip Enable). A0, A1, and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven address cycles; the last five are used to define the switch settings. The 12th address cycle defines the switch which inhibits the write enable to the device. A logic one in this location allows read/write operations. A logic zero in this location turns the device into a read-only memory device. The next four address cycles, 12 through 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010, activates the nonvolatile controller and data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation. At the completion of the sixteenth cycle, if the pattern recognition sequence is correct, the switch setting defined in cycles 11 through 15 are transferred and are active for the next memory cycle. When the DS1245EE is first installed in a system with V_{CC} power, the device will not be in write protect mode.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and unconditionally write protects at 4.37 volts nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. Should an out of tolerance condition be detected, the DS1245EE will automatically write protect itself and all inputs to the device become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit can connect the lithium energy source to the RAM to retain data if enabled. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy. Normal operation can resume after V_{CC} exceeds 4.5 volts.

ADDRESS INPUT PATTERN Table 1

	CYCLE NUMBER															
Address Inputs	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

* See Table 2

4

CONTROL SELECT Table 2

$\overline{WE}$ Battery Control					Operation
11	12	13	14	15	
0	X	X	X	X	Read Only Operation
1	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

*Any other combination turns controller off

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5		
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE}$ >V_{IH} <V_{CC}	I_{IO}	-1.0		+1.0	µA	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200ns	I_{CC01}			85	mA	
Write Protection Voltage	V_{TP}	4.25	4.37	4.5	V	

DC TEST CONDITIONS

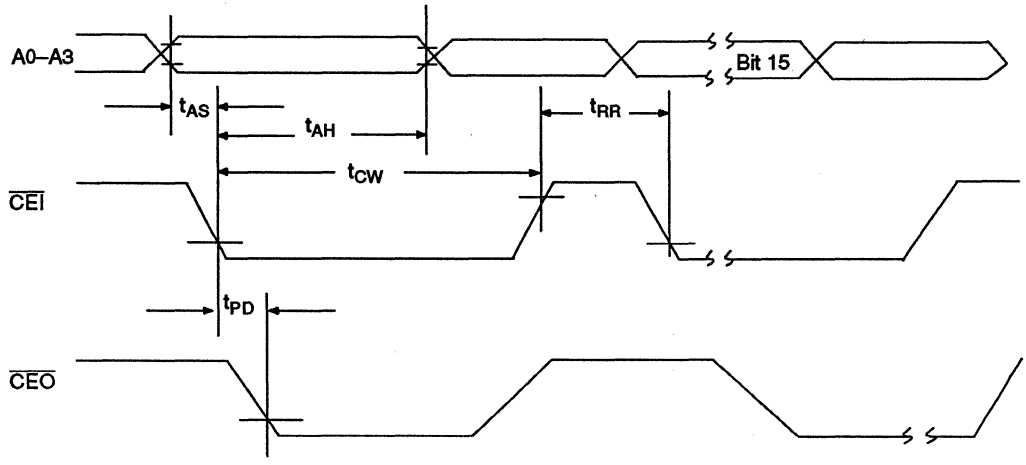
Outputs Open
All Voltages Are Referenced to Ground

SWITCH TIMING

(0°C to 70°C, V_{CCI} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	110			ns	

TIMING DIAGRAM-SWITCH SETTING



CAPACITANCE

(T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

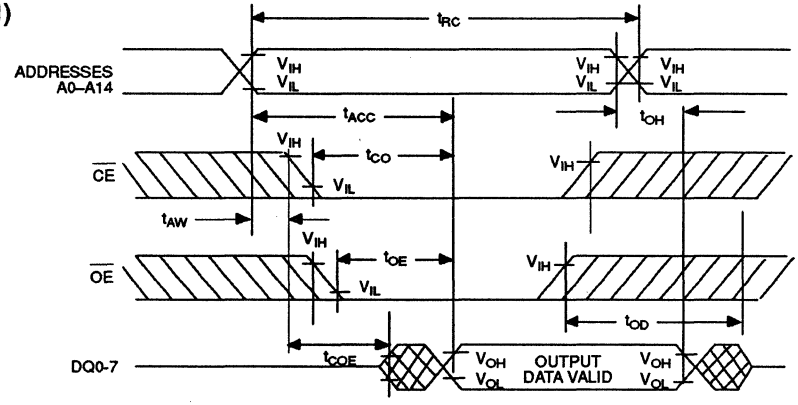
(0°C TO 70°C; V_{CC} = 5V + 10%)

		DS1245EE100		DS1245EE-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z From Deselection	t_{OD}		35		40	ns	5
Output Hold From Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z From $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	15		15		ns	4

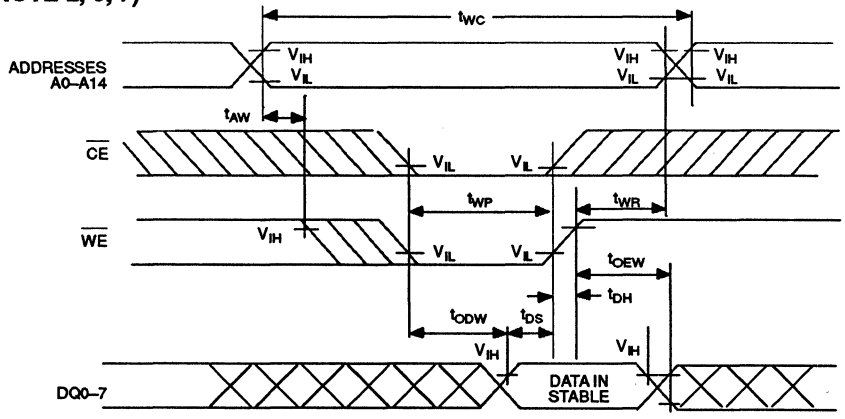
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

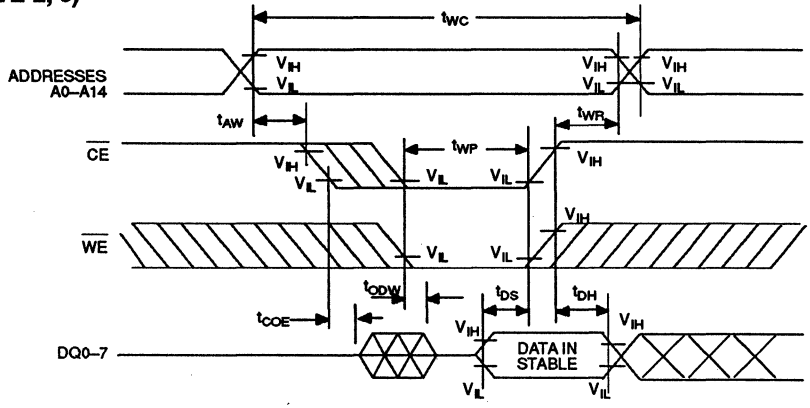
READ CYCLE (NOTE 1)



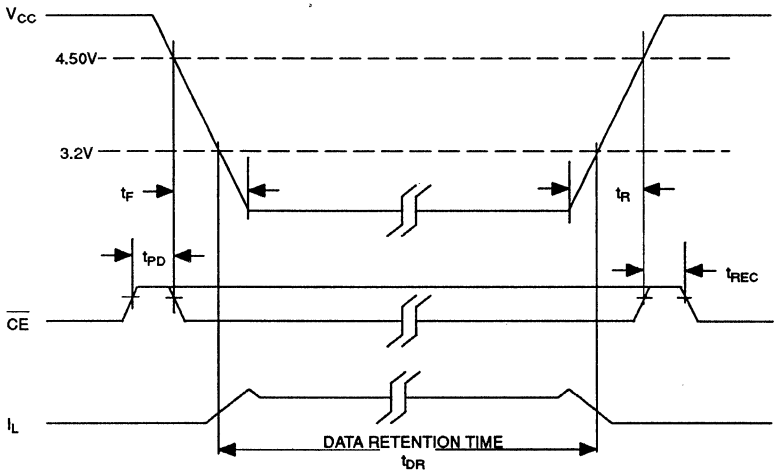
WRITE CYCLE 1 (NOTE 2, 6, 7)



WRITE CYCLE 2 (NOTE 2, 8)



POWER-DOWN/POWER-UP TIMING



LEAKAGE CURRENT
I_L SUPPLIED FROM
LITHIUM CELL

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		us	9
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		us	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		us	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

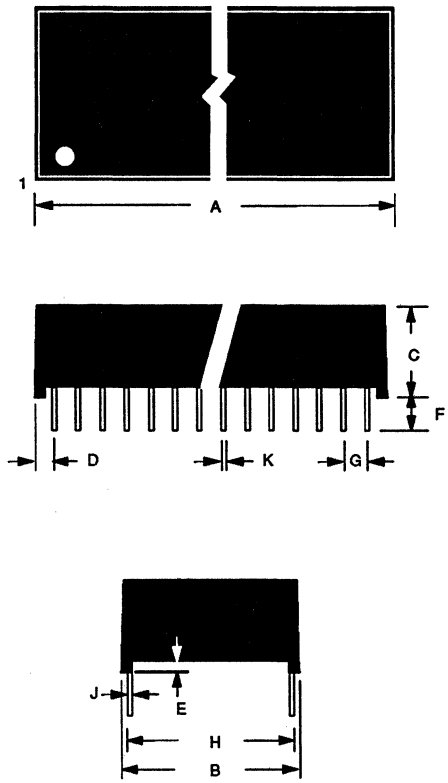
WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state during this period.
9. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

DS1245EE 1M WRITE-PROTECTED NV SRAM 32-PIN 740 MIL MODULE



PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

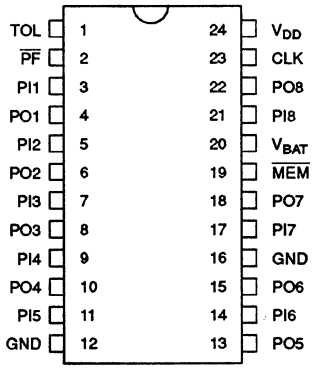
DALLAS SEMICONDUCTOR

DS1380, DS1380S
RAMport

FEATURES

- 2K X 8 Static RAM
- 8-Bit Transparent I/O Port
- Battery connection provided for nonvolatility
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10% of power supply voltage
- Power Fail Interrupt Output
- Low Power CMOS
- 24 Pin Dip Package or optional 24 pin SOIC
- Ideally suited for microcontroller applications as add on memory

PIN ASSIGNMENT



24 PIN DIP OR 24 PIN SOIC

PIN DESCRIPTION

$\overline{PF}$	-	Power Fail Output
PI1 - PI8	-	Port Inputs (µP Ports)
PO1 - PO8	-	Port Outputs (External Ports)
GND	-	Ground
V_{CC}	-	+5 Volts
CLK	-	Clock
$\overline{MEM}$	-	Memory Select
V_{BAT}	-	+ Battery Connection

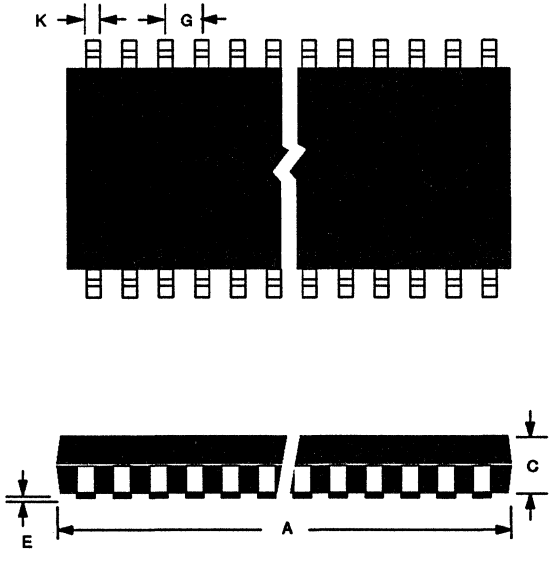
DESCRIPTION

The DS1380 is a 2K X 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1380 for use in the identical manner as previously intended. The reproduced port pins can be both inputs and outputs and will appear as exactly the same I/O structure on the attached microcontroller. The content of memory is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1380 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1380 can be made nonvolatile with direct connection of a 3 volt lithium battery. The DS1380 is controlled by only two signals; the port clock and memory select inputs.

OPERATION

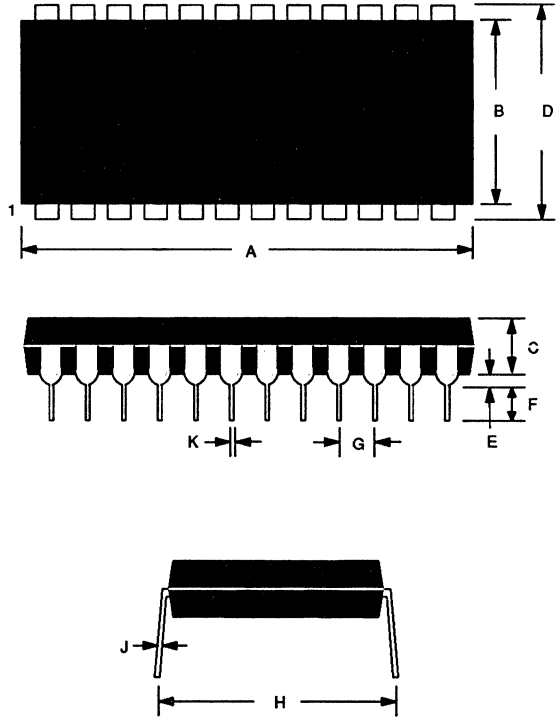
The DS1380 performs exactly to the specifications of the DS1381 with the exception of an external battery connection. The V_{BAT} pin is designed for a battery input voltage between 2.7 volts and 3.5 volts and requires a current of 100 nA at 25°C and 1 uA at 60°C. If battery backup operation is not required, the V_{BAT} input must be grounded. With the external battery connected, the DS1380 is nonvolatile and retains data in the absence of power. When the V_{BAT} input is grounded, the DS1380 is volatile and will not retain data without V_{CC}. For detailed operation and electrical specifications consult the DS1381 data sheet.

DS1380S RAMPORT



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.62
C IN. MM	0.089 2.26	0.095 2.41
D IN. MM	0.325 8.26	0.330 8.38
E IN. MM	0.008 0.20	0.012 0.30
F IN. MM	0.097 2.46	0.105 2.68
G IN. MM	0.046 1.17	0.054 1.37
H IN. MM	0.400 10.16	0.410 10.41
J IN. MM	0.006 0.152	0.011 0.28
K IN. MM	0.013 0.33	0.019 0.48

DS1380 RAMPORT



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

4

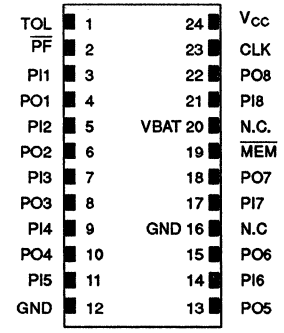
DALLAS SEMICONDUCTOR

DS1381
NV RAMport

FEATURES

- 2K X 8 Nonvolatile Static RAM
- 8-Bit Transparent I/O Port
- Greater than 10 years of data retention in absence of V_{CC}
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10%
- Power Fail Interrupt Output
- Low Power CMOS
- 24 Pin Dip Package
- Ideally suited for microcontroller applications as add on memory

PIN ASSIGNMENT



PIN DESCRIPTION

$\overline{PF}$	-	Power Fail Output
PI1 - PI8	-	Port Inputs (µP Ports)
PO1 - PO8	-	Port Outputs (External Ports)
GND	-	Ground
V_{CC}	-	+5 Volts
CLK	-	Clock
$\overline{MEM}$	-	Memory Select
N.C.	-	No Connection

DESCRIPTION

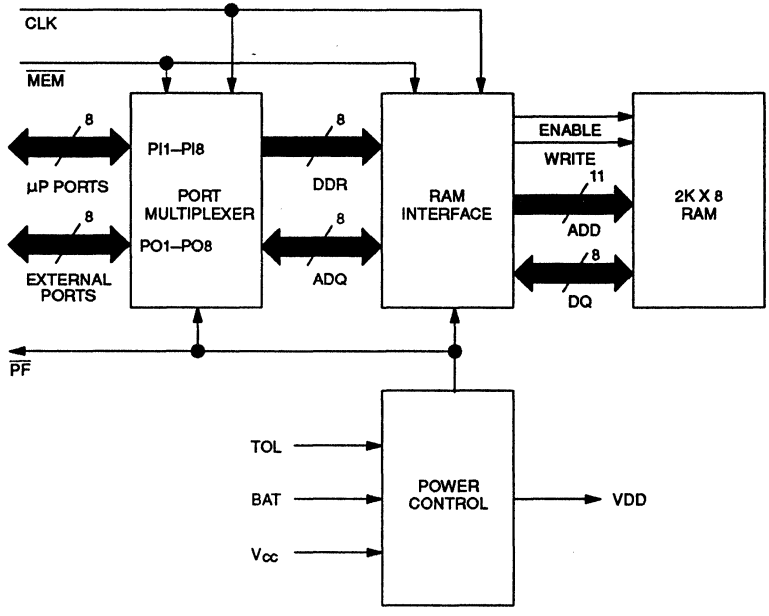
The DS1381 is a 2K X 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1381 for use in the identical manner as previously intended. The reproduced port pins can be both inputs and outputs and will appear as exactly the same I/O structure on the attached microcontroller. The content of memory is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1381 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1381 is nonvolatile and data retention time is over 10 years. The DS1381 is controlled by only two signals; the port clock and memory select inputs.

A block diagram of the DS1381 nonvolatile RAMport is shown in Figure 1. As shown, the DS1381 has four key elements; namely the port multiplexer, the RAM interface, a 2K X 8 static RAM, and a power control section. The port multiplexer is connected to eight microcontroller port pins from which address, data and port data are received. The 8 microcontroller port pins are reproduced at the multiplexer output when the $\overline{MEM}$ pin is high through transmission gates. When the $\overline{MEM}$ pin is low all output pins are latched in their high or low states and inputs go to a high impedance state. With the $\overline{MEM}$ pin low the microcontroller port pins are then free to pass address and data to and from the nonvolatile static RAM. Each read or write cycle to memory is accomplished in three separate steps involving two address transfers and one data transfer. The clock signal (CLK) is used to strobe address and data information through the port multiplexer into the RAM interface circuitry. To accomplish RAM access the high order address (A8-A10) is placed on port input pins PI1 through PI3. PI4 through PI8 contain bits which dictate a read of RAM or a write to RAM. If these bits do not match exactly the bit patterns as shown in Figure 2, completion of the full cycle will be allowed but no action will be taken during the data transfer portion. With the proper bit patterns placed on the port pins, the CLK input is then transitioned high to low and then high again. The clock action allows the address and read/write information to propagate through the port multiplexer and latch the information into the RAM interface. Next the low order address (A0-A7) is placed on the port input pins (PI1 through PI8) and the second address transfer also propagates through the port multiplexer as CLK goes low and returns high. The RAM is now ready for data transfer. If a write cycle is to occur, the microcontroller port pins must deliver the correct data to be written. As the CLK transitions high to low, data propagates through the port multiplexer and the RAM interface and finally to the RAM where data is written into RAM. The write cycle is terminated when the CLK transitions low to high. Data can then be removed from the port input pins. If during the data transfer a read cycle is to occur, the port input pins must not be driven by the microcontroller. Then as CLK transitions high to low, the RAM becomes active and data is presented on the port input pins for the microcontroller to read. A read cycle is terminated when the CLK signal is transitioned low to high and the port input pins are returned to a high impedance state.

After completing the read or write cycle another read or write cycle can be performed without pulsing the $\overline{MEM}$ pin high between cycles. After all access to the RAM is complete, the $\overline{MEM}$ pin must be returned to a high state.

4

FIGURE 1: FUNCTIONAL BLOCK DIAGRAM



OPERATION - WRITING THE DATA DIRECTION REGISTER

The data direction register is written with a logic one in each bit location which will have a corresponding high impedance output pin (PO1-PO8) during reading and writing of the memory of the DS1381 by the microcontroller (see Figure 3). This will avoid contention between PO1-PO8 and devices driving PO1-PO8 as inputs. To write data to the data direction register, the CLK input is driven low prior to $\overline{MEM}$ going low. With CLK low $\overline{MEM}$ is driven low which latches the port output pins and readies the DS1381 for data direction information. Data direction information is then placed on the port input pins by the microcontroller and is written into the data direction register as $\overline{MEM}$ transitions low to high. While the data direction register is being written, the output pins (PO1 through PO8) are latched to the PI1 through PI8 states with their high or low impedance condition determined by the old data direction contents. The new data direction contents will be effective the next time $\overline{MEM}$ is taken to a low state.

OPERATION - POWER FAIL AND DATA RETENTION MODE

The DS1381 has full functional capability when V_{CC} is within normal limits. However, when V_{CC} goes to an out of tolerance level, the nonvolatile RAMport assumes a write protected status such that the memory and data direction register cannot be accessed. In addition the port output signals go to a high impedance state, the port input pins become "don't care" and the transmission gates connecting the 8 microprocessor port pins to the external ports will go to a low impedance state. The power fail pin ($\overline{PF}$) goes to an active low level when power fail occurs and remains low until V_{CC} returns to nominal limits. The point at which write protection occurs depends on the level of the tolerance pin (TOL). When TOL is grounded, write protection will occur between 4.75 volts and 4.5 volts. When TOL is connected to V_{CC}, write protection occurs between 4.5 volts and 4.25 volts. After power fail detection has occurred and the V_{CC} level falls below the voltage level of the internal lithium cell the internal memory and register contents are maintained by this cell which is capable of maintaining data for over 10 years. The switch over from V_{CC} to the lithium cell occurs when V_{CC} is below approximately 3 volts.

FIGURE 2: READ AND WRITE BIT PATTERNS

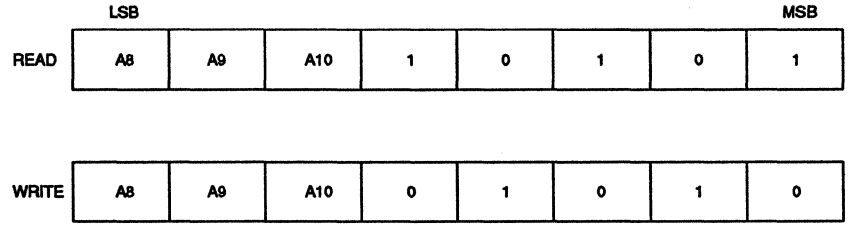
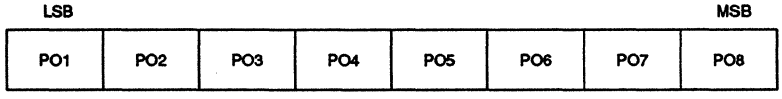


FIGURE 3: DATA DIRECTION REGISTER BITS



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO 7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (TOL=GND)	V_{CC}	4.75	5.0	5.5	Volts	1
Supply Voltage (TOL=V_{CC})	V_{CC}	4.5	5.0	5.5	Volts	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	Volts	1
Logic 0 Input	V_{IL}	-0.3		+0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} WITHIN DC OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current	ICC1		20	25	mA	2
Standby Current	ICC2		3	7	mA	3
Logic 1 Out @ 1 mA	V_{OH}	2.4			Volts	1, 6
Logic 0 Out @ 2 mA	V_{OL}			0.4	Volts	1, 6
VCC Write Protect TOL=GND	V_{CCTP}	4.50	4.62	4.75	Volts	1
VCC Write Protect TOL=VCC	V_{CCTP}	4.25	4.37	4.50	Volts	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	5
Port Pins In to Out Impedance	P_Z		75	150	Ω	7

CAPACITANCE

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C		10	pF	
Output Capacitance	C_{OUT}	t_A=25°C		10	pF	

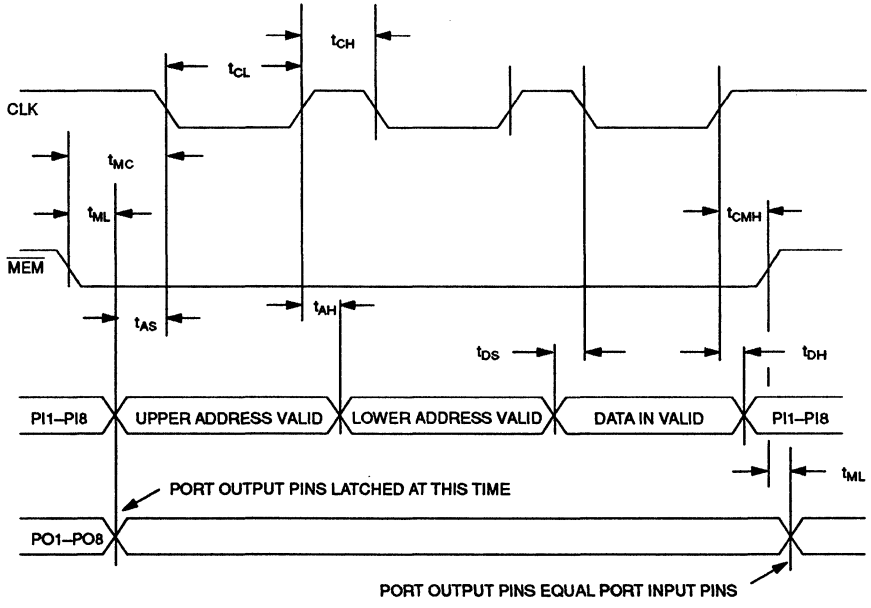
AC ELECTRICAL CHARACTERISTICS
(0°C TO 70°C TOL = V_{CC}, V_{CC} = 4.50 TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Low	t_{CL}	150			ns	
Clock High	t_{CH}	50			ns	
Address Setup	t_{AS}	20			ns	
Address Hold	t_{AH}	0			ns	
Data Setup	t_{DS}	20			ns	
Data Hold	t_{DH}	0			ns	
$\overline{MEM}$ to CLK Low	t_{MC}	40			ns	
$\overline{MEM}$ to Output Latch	t_{ML}	25			ns	
CLK to $\overline{MEM}$ High	t_{CMH}	10			ns	
CLK to Data Valid	t_{CD}			100	ns	
CLK to Data at High Z	t_{DZ}			20	ns	
CLK to $\overline{MEM}$ Active	t_{CM}	40			ns	
DDR Data Setup	t_{DSD}	100			ns	
V_{CC} Slew Rate	t_R, t_F	250			µs	

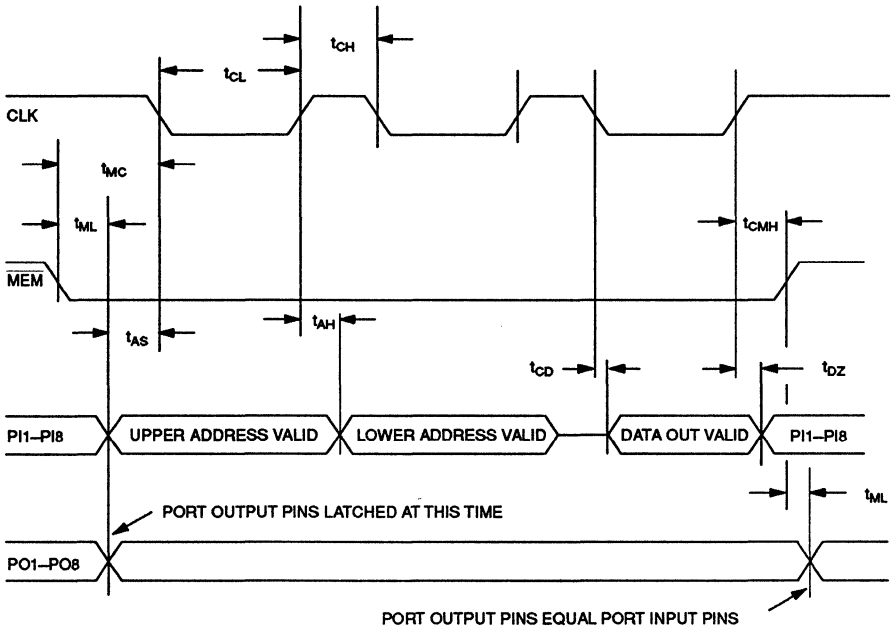
DATA RETENTION (t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention	10		years	

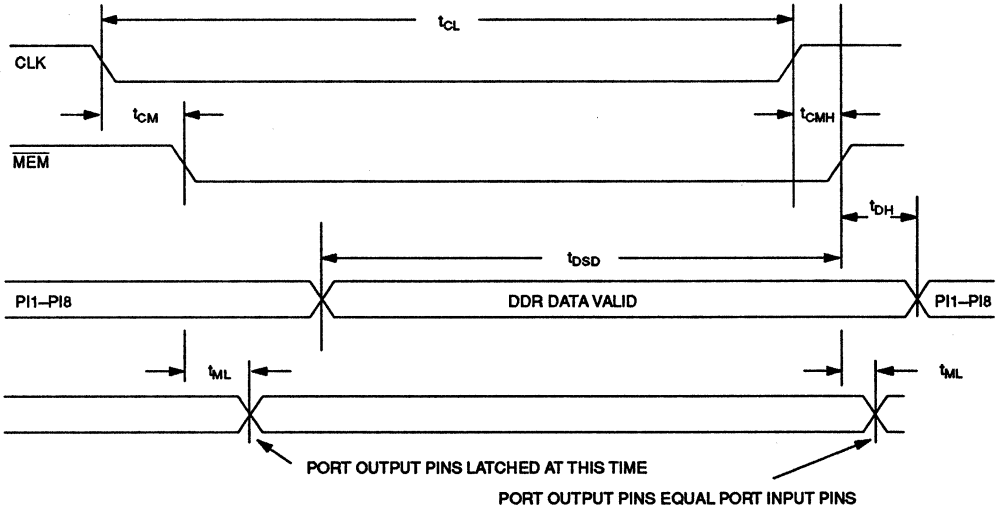
TIMING DIAGRAM: WRITE CYCLE TO MEMORY



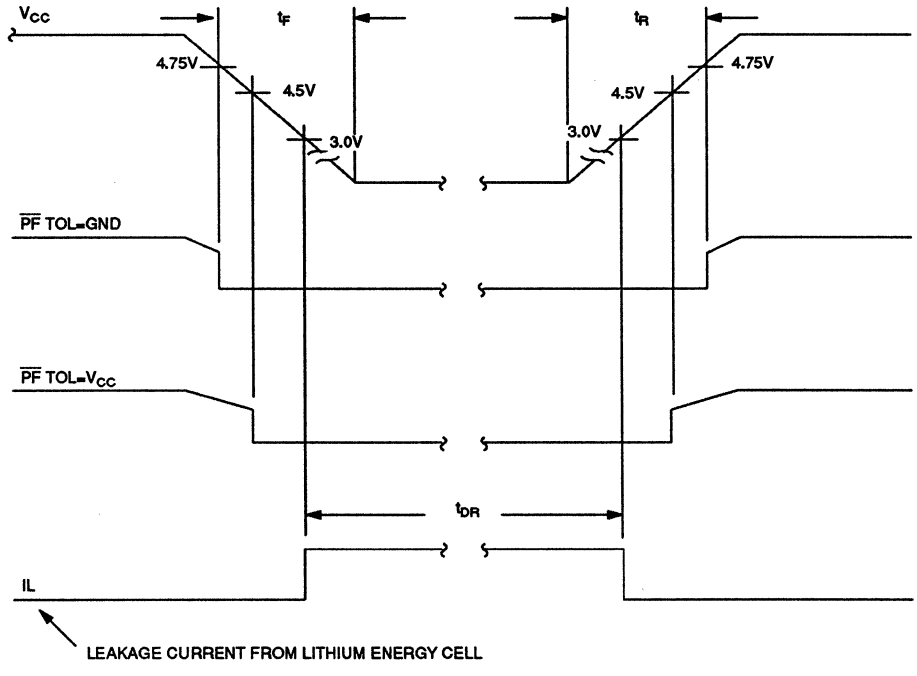
TIMING DIAGRAM: READ CYCLE FROM MEMORY



TIMING DIAGRAM: WRITE CYCLE TO DATA DIRECTION REGISTER



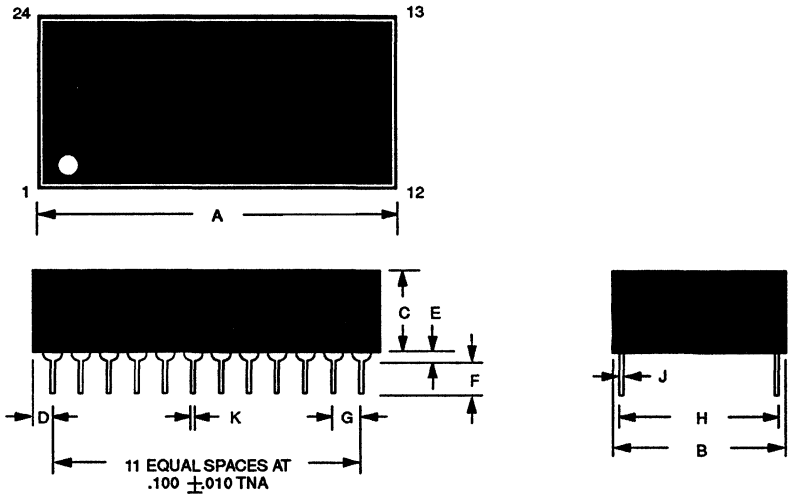
TIMING DIAGRAM: POWER UP - POWER DOWN



NOTES

1. All voltages are reference to ground
2. Active current is defined as $\overline{MEM}$ low with CLK low and all outputs are open
3. Standby current is defined as $\overline{MEM}$ high with CLK high and all outputs are open
4. Input leakage applies to CLK and $\overline{MEM}$ only
5. Output leakage applies to $\overline{PF}$ only
6. Logic levels apply to $\overline{PF}$ and PO1-PO8 when these outputs are latched
7. Port input to output impedance is the on resistance of the transmission gate between port inputs and port outputs with $\overline{MEM}$ high and with less than 4 mA flowing through the transmission gate.

NONVOLATILE RAMPORT



NOTE: PINS 16 AND 20 ARE MISSING BY DESIGN

DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.14	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

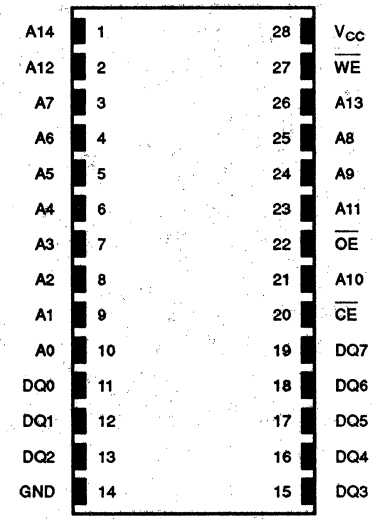
DALLAS SEMICONDUCTOR

DS1630Y/AB
Partitioned 256K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAMs or EEPROMs
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70, 85, 100, and 120 ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range (DS1630Y)
- Optional ±5% operation range (DS1630AB)
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A14	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable

DESCRIPTION

The DS1630Y/AB 256K Nonvolatile SRAM is a 262,144-bit, fully static SRAM organized as 32,768 words by 8 bits. The DS1630Y/AB has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile SRAM can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewide 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

READ MODE

The DS1630Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1630Y/AB is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37V nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1630AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1630Y/AB constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1630AB).

FRESHNESS SEAL AND SHIPPING

The DS1630Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11 - A14. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1630Y/AB to inhibit $\overline{WE}$ internally when A14 A13 A12 A11=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO 7.0V
OPERATING TEMPERATURE	0°C TO 70°C, –40°C TO +85°C FOR IND PARTS
STORAGE TEMPERATURE	-40°C TO 70°C, –40°C TO +85°C FOR IND PARTS
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1630Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1630AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1630Y) (0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1630AB)				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE} = V_{CC}$ - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1630Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1630AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1630AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1630Y)					
		DS1630Y/AB-70		DS1630Y/AB-85			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH}	15		15		ns	4
		DS1630Y/AB-100		DS1630Y/AB-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time	t_{DH}	15		15		ns	4

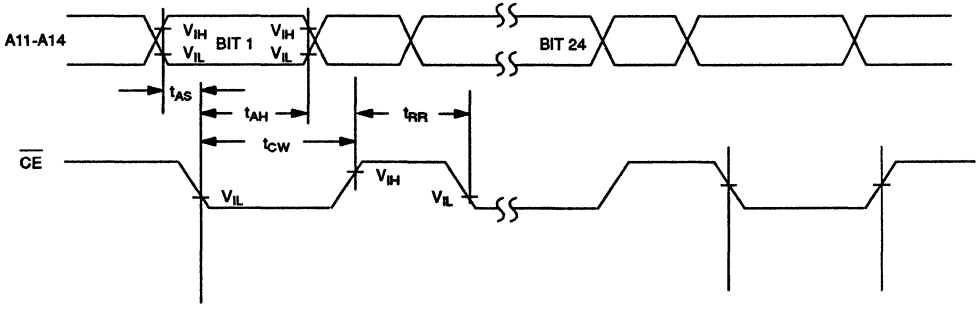
AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CCI} = 4.50V TO 5.50V)*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

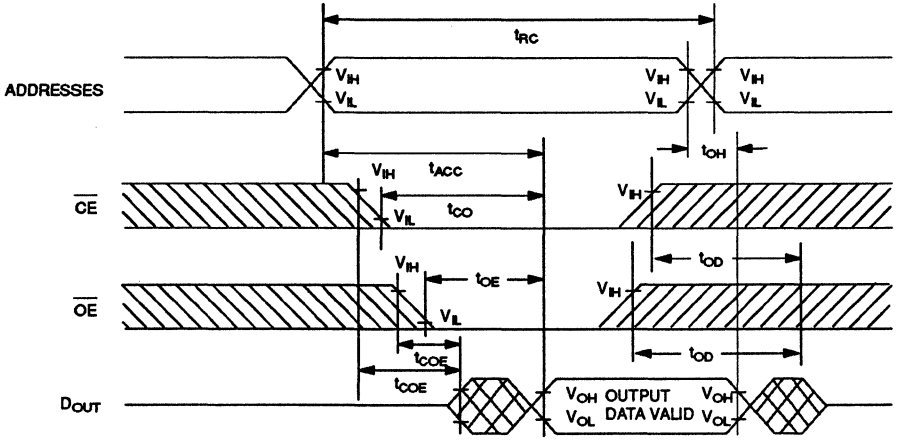
*For loading partition register

4

TIMING DIAGRAM: LOADING PARTITION REGISTER

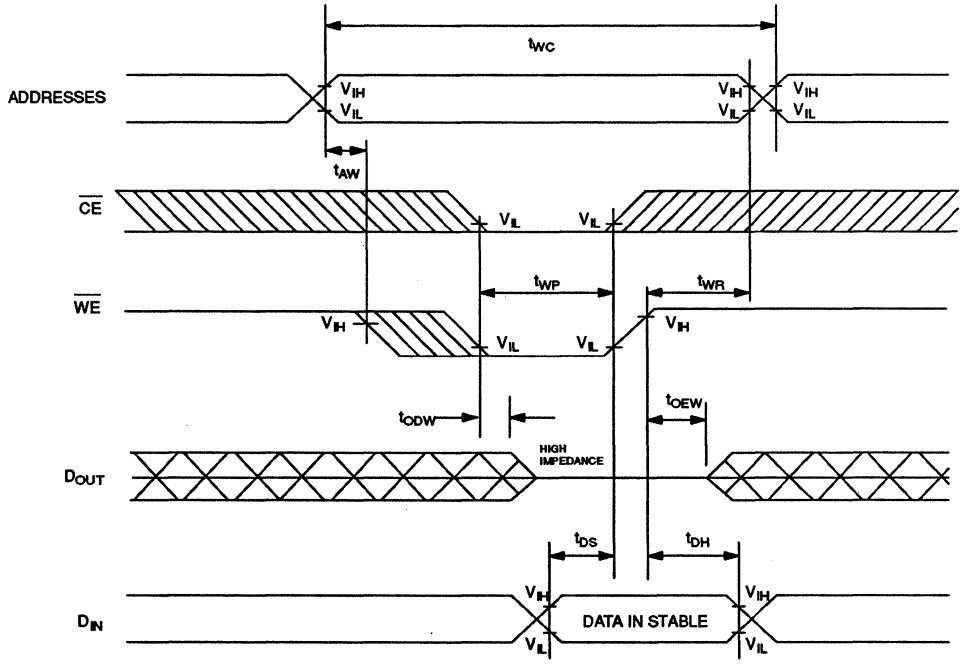


READ CYCLE



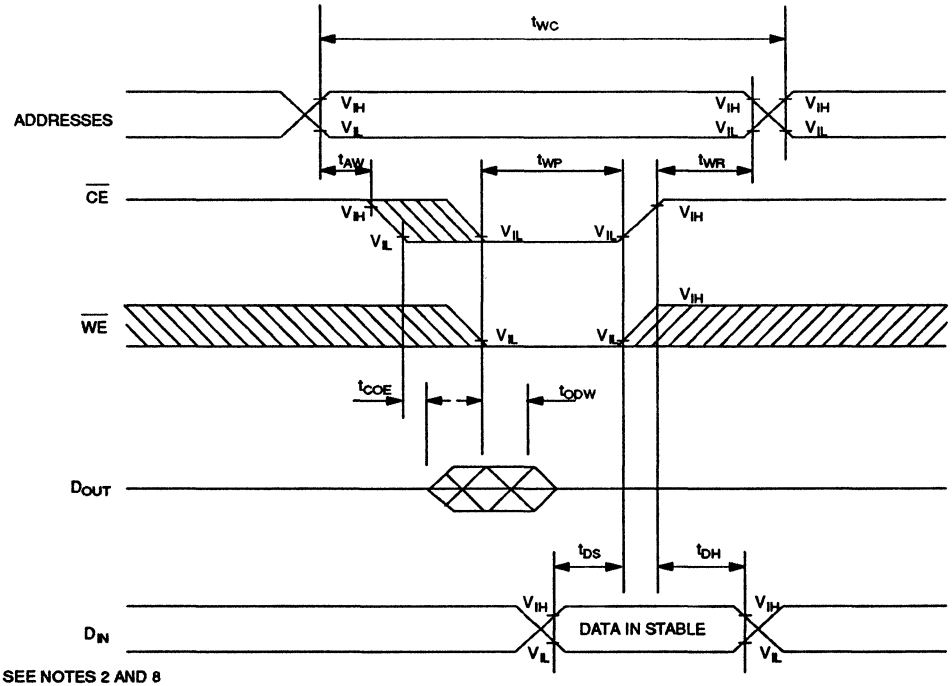
SEE NOTE 1

WRITE CYCLE 1



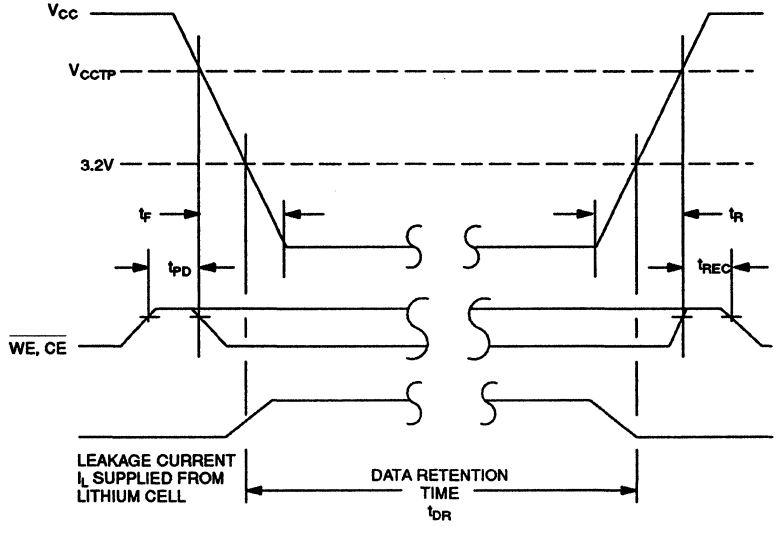
SEE NOTES 2, 6, AND 7

WRITE CYCLE 2



SEE NOTES 2 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	0			µs	12
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300			µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0			µs	
t_{REC}	$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	25		125	ms	

(t_A = 25°C)						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10			years	9, 11

WARNING

Under no circumstance are negative undershoots, below 0.5V, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1630Y/AB has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

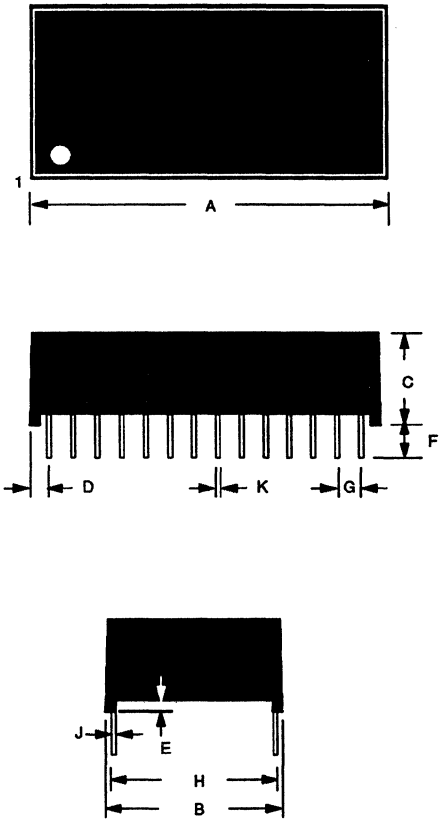
DC TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1630Y/AB NONVOLATILE SRAM 28 PIN 740 MIL MODULE



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

4

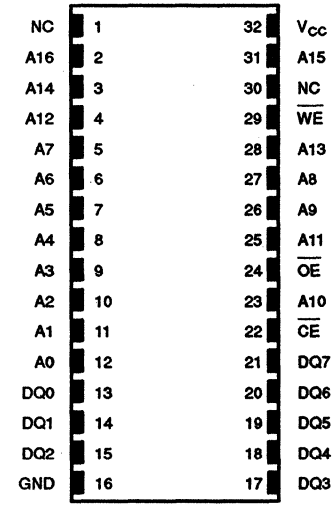
DALLAS SEMICONDUCTOR

DS1645Y/AB
Partitioned 1024K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM or EEPROM
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, 100 or 120 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1645Y)
- Optional ±5% operating range (DS1645AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A16	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

DESCRIPTION

The DS1645Y/AB 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1645Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION – READ MODE

The DS1645Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION – WRITE MODE

The DS1645Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1645AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1645Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1645AB).

FRESHNESS SEAL AND SHIPPING

The DS1645Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

BATTERY REDUNDANCY

Battery redundancy is provided to ensure reliability. The DS1645Y contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A13 - A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 128K/16 or 8K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1645Y/AB to inhibit $\overline{WE}$ internally when A16 A15 A14 A13=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C, –40°C TO +85°C FOR IND PARTS
STORAGE TEMPERATURE	-40°C TO +70°C, –40°C TO +85°C FOR IND PARTS
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1645Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1645AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1645AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1645Y)				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1645Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1645AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1645AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1645Y)					
		DS1645Y/AB-70		DS1645Y/AB-85			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		30	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	15		15		ns	4
		DS1645Y/AB-100		DS1645Y/AB-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	15		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		35		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	15		15		ns	4

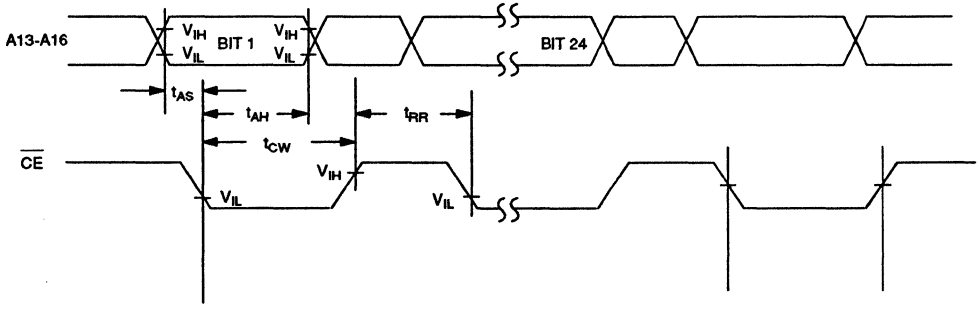
AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CCI} = 4.50V TO 5.50V)*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

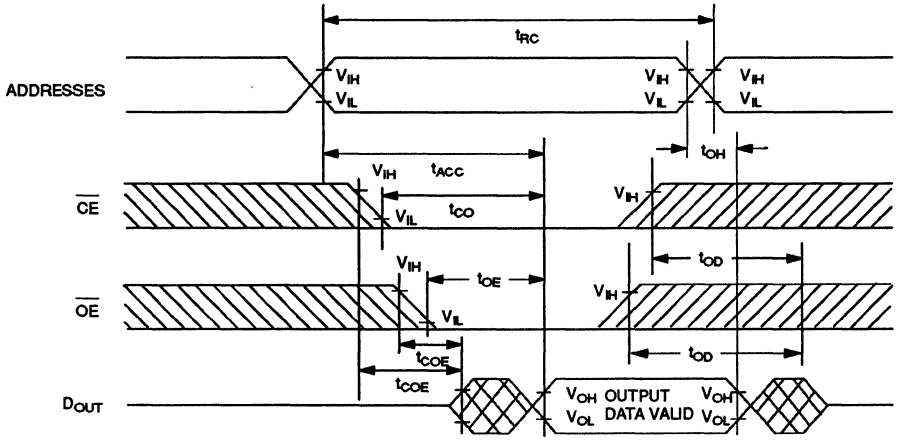
*For loading partition register

4

TIMING DIAGRAM: LOADING PARTITION REGISTER

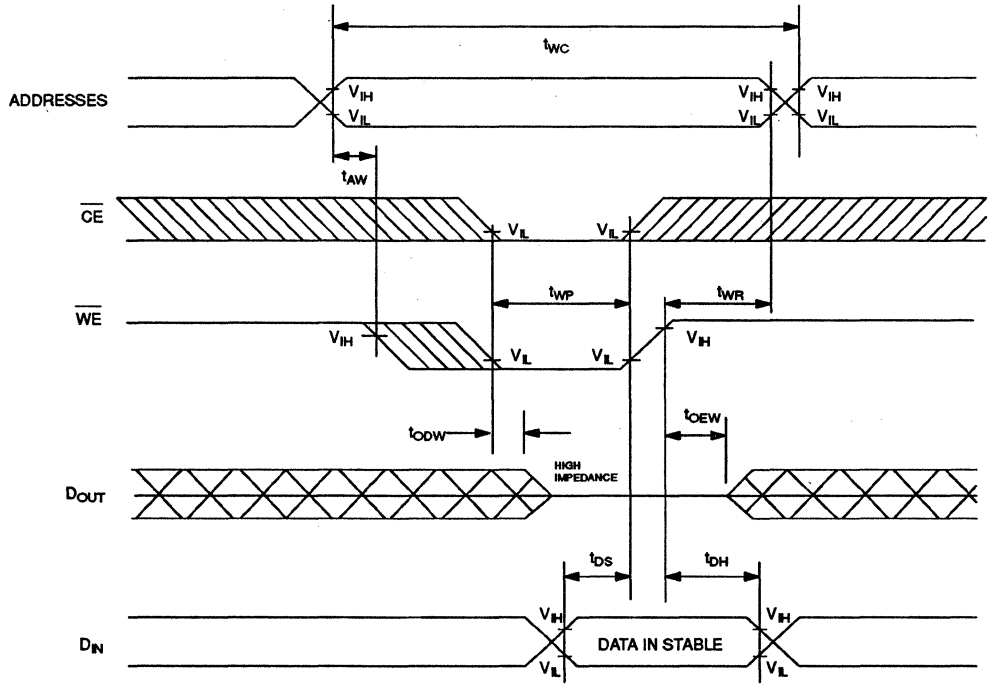


READ CYCLE



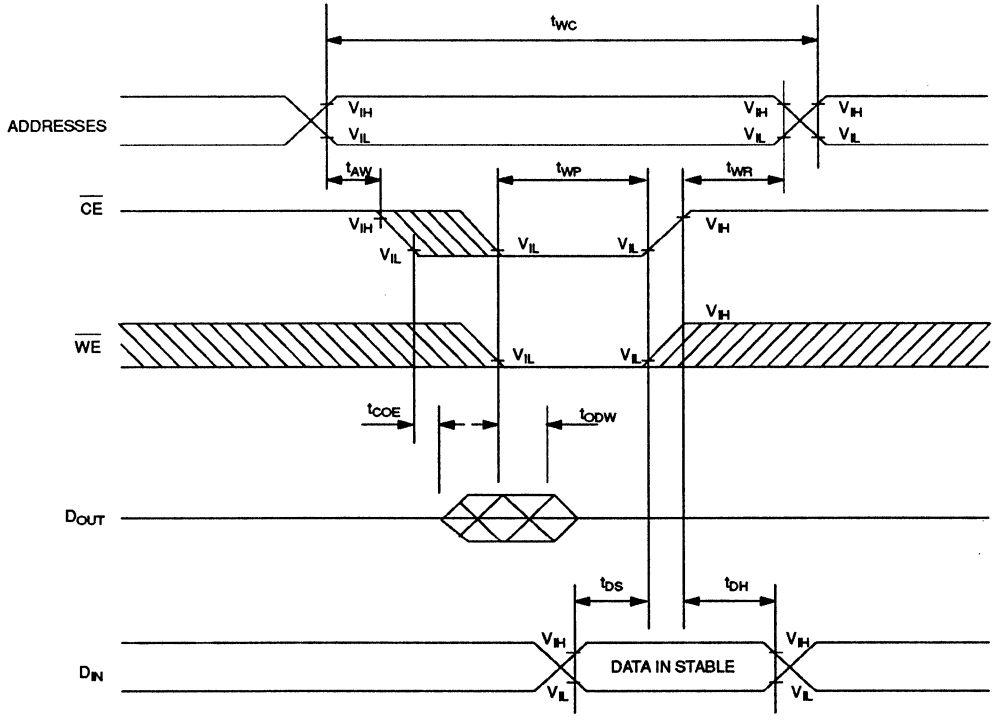
SEE NOTE 1

WRITE CYCLE 1



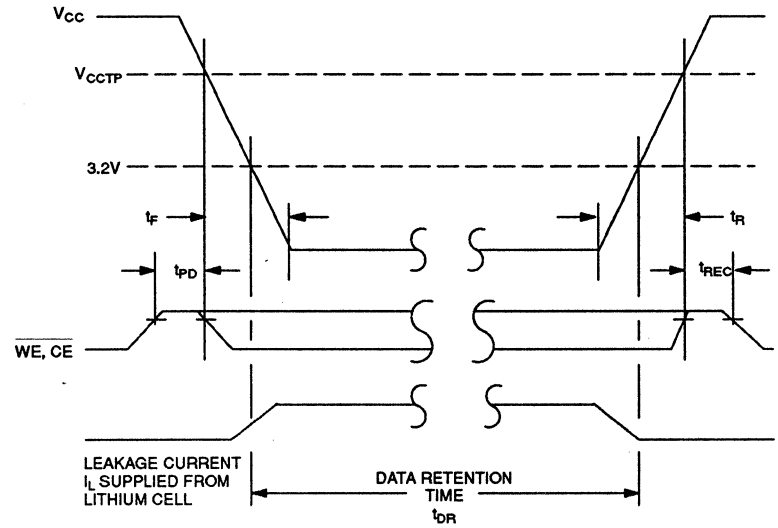
SEE NOTES 2, 6, AND 7

WRITE CYCLE 2



SEE NOTES 2 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$, $\overline{WE}$, at V_{IH} before Power-Down	0			µs	12
t_{TF}	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300			µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0			µs	
t_{REC}	$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	25		125	ms	

(t_A = 25°C)						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10			years	9, 11

WARNING

Under no circumstance are negative undershoots, below 0.5 volts, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1645Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

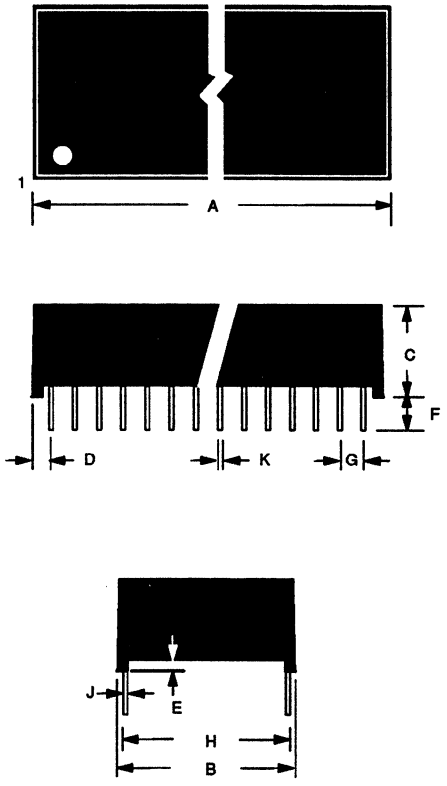
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1645Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

4

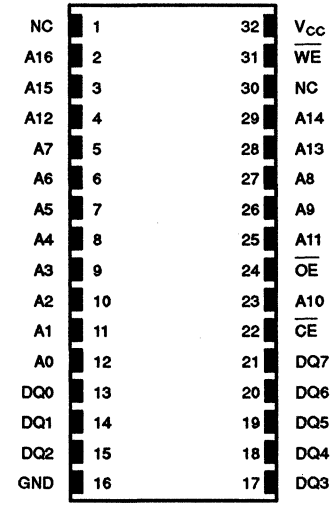
DALLAS SEMICONDUCTOR

DS1645EE
Partitioned 1024K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K x 8 EPROM, EEPROM, or FLASH
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A16	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

DESCRIPTION

The DS1645EE 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1645EE has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 128K x 8 EPROM, EEPROM or FLASH conforming to the popular bytewide 32 pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface. This part is functionally equivalent to the DS1645Y and differs only in pinout. See the DS1645Y/AB 1024K NV SRAM data sheet for technical details.

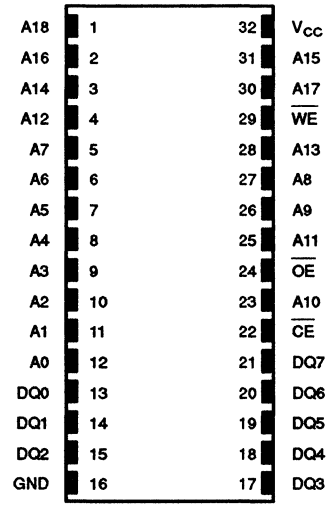
DALLAS SEMICONDUCTOR

DS1650Y/AB
Partitioned 4096K NV SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM or EEPROM
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 70, 85, or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1650Y)
- Optional ±5% operating range (DS1650AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A0 - A18	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ0 - DQ7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect

DESCRIPTION

The DS1650Y/AB 4096K Nonvolatile SRAM is a 4,194,304 bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. The DS1650Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The nonvolatile static RAM can be used in place of existing 512K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION - READ MODE

The DS1650Y/AB executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE MODE

The DS1650Y/AB is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1650AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1650Y/AB constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1650AB).

FRESHNESS SEAL AND SHIPPING

The DS1650Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

BATTERY REDUNDANCY

Battery redundancy is provided to ensure reliability. The DS1650Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1650Y/AB to inhibit $\overline{WE}$ internally when A18 A17 A16 A15=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

4

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{18} A_{17} A_{16} A_{15})
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101
A17	BIT 24	PARTITION 14	1110
A18	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C, –40°C TO +85°C FOR IND PARTS
STORAGE TEMPERATURE	-40°C TO +70°C, –40°C TO +85°C FOR IND PARTS
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1650Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1650AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1650AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1650Y)				
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage (DS1650Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1650AB)	V_{TP}	4.50	4.62	4.75	V	

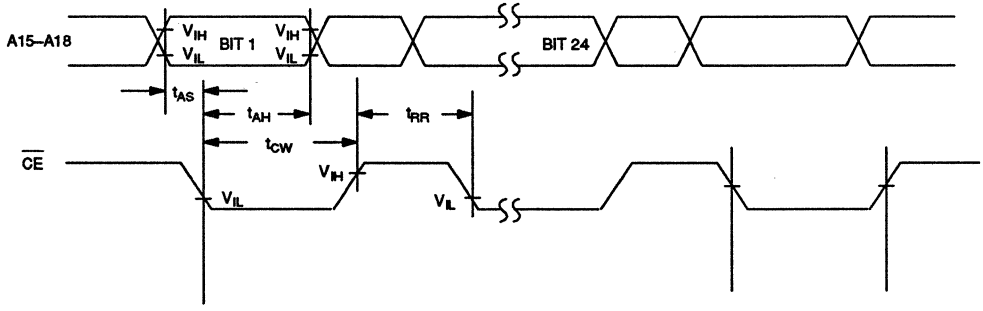
CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS		(0°C TO 70°C; V_{CC} = 5V ± 5% FOR DS1650AB) (0°C TO 70°C; V_{CC} = 5V ± 10% FOR DS1650Y)							
		DS1650Y/AB-70		DS1650Y/AB-85		DS1650Y/AB-100			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		85		100		ns	
Access Time	t_{ACC}		70		85		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35		45		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		85		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	70		85		100		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25		20		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		15		ns	4

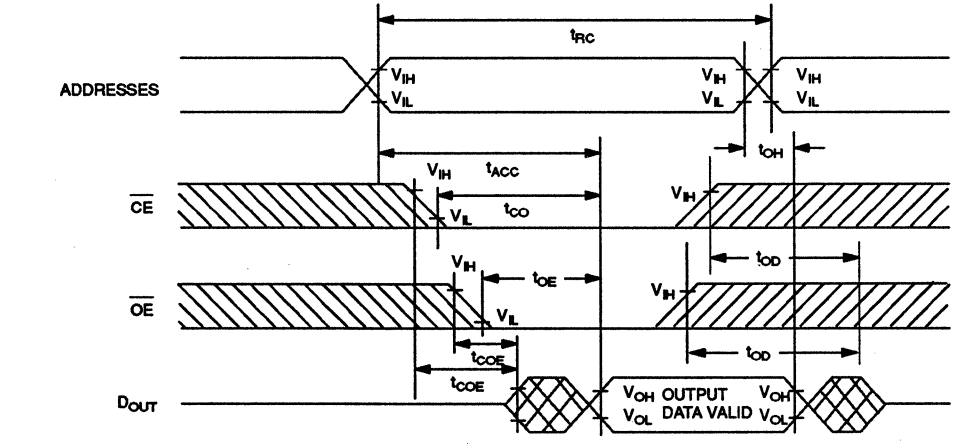
AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CCI} = 4.50V TO 5.50V)*						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

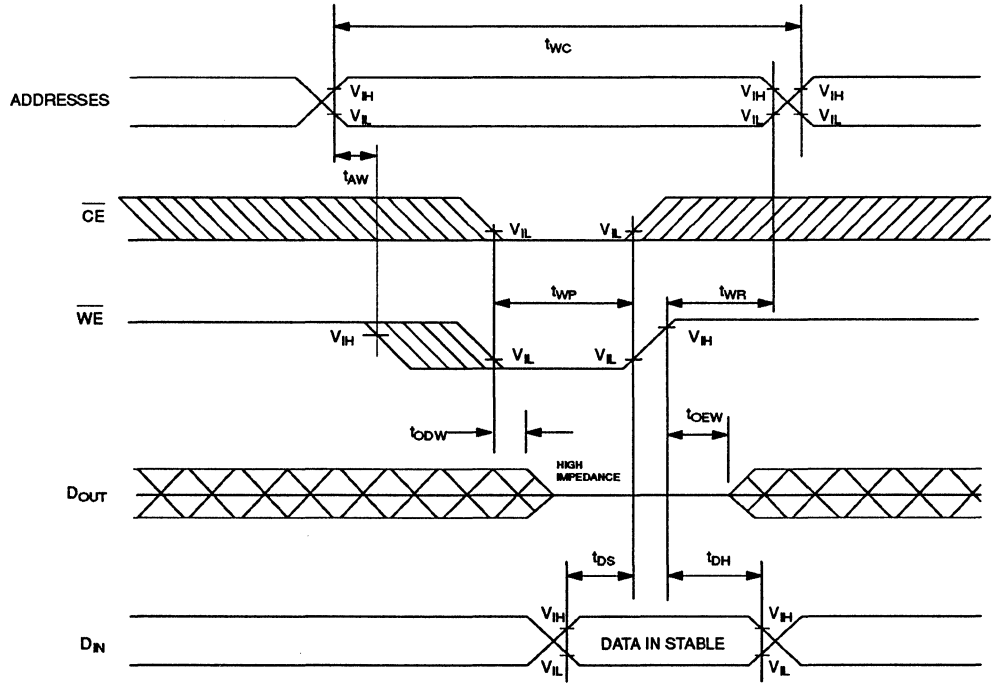


READ CYCLE



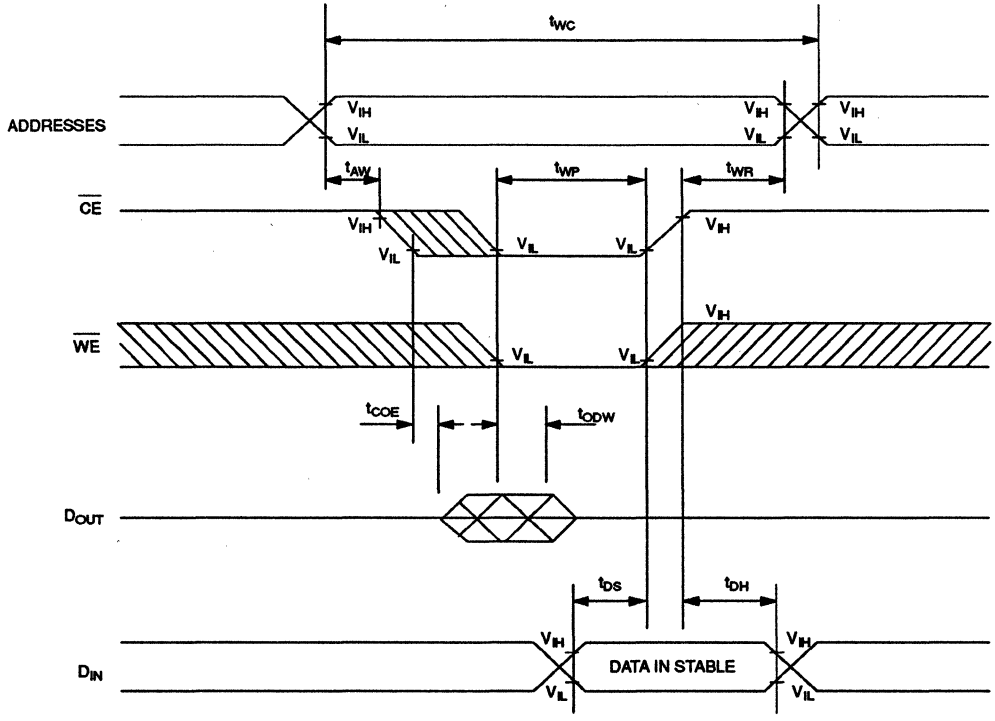
SEE NOTE 1

WRITE CYCLE 1



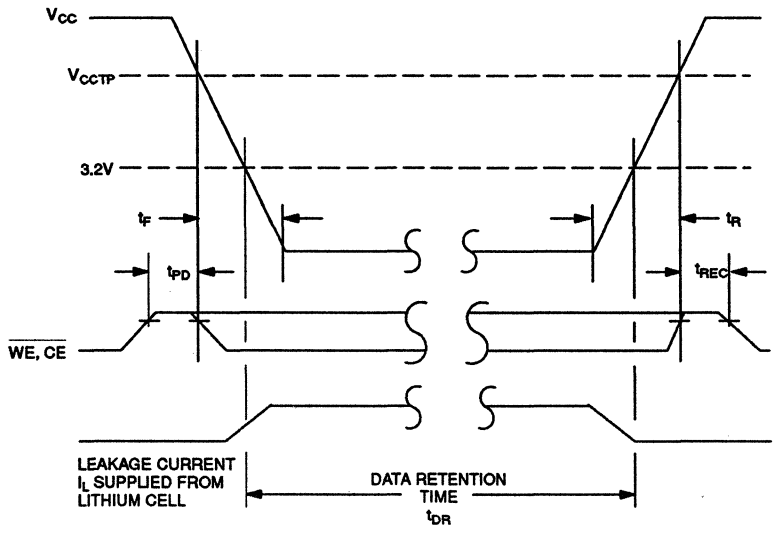
SEE NOTES 2, 6, AND 7

WRITE CYCLE 2



SEE NOTES 2 AND 8

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$, $\overline{WE}$, at V_{IH} before Power-Down	0			µs	12
t_{TF}	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300			µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0			µs	
t_{REC}	$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	25		125	ms	

(t_A = 25°C)						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10			years	9, 11

4

WARNING

Under no circumstance are negative undershoots, below 0.5 volts, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1650Y/AB has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.

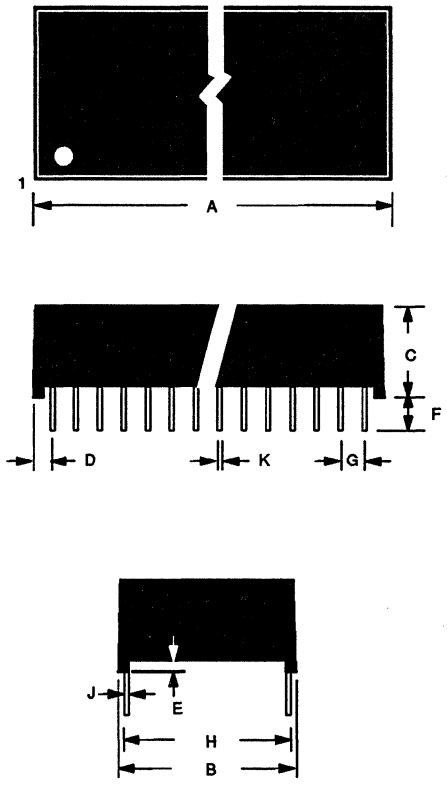
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1650Y/AB NONVOLATILE SRAM 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DALLAS SEMICONDUCTOR

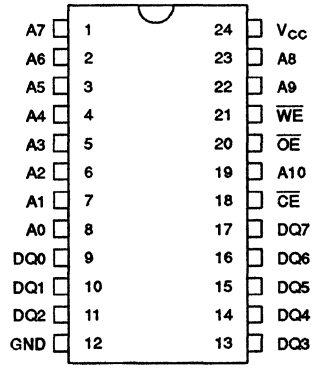
DS2016, DS2016S
2K x 8 3V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  50 nA max at $t_A = 25°C$ $V_{CC} = 3.0V$
  100 nA max at $t_A = 25°C$ $V_{CC} = 5.5V$
  1 µA max at $t_A = 60°C$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 150 ns at 5.0V and 250 ns at 3.0V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 24 pin DIP and 24 pin SOIC packages
- Suitable for both battery operate and battery backup applications

PIN ASSIGNMENT



24 PIN DIP OR 24 PIN SOIC

PIN DESCRIPTION

A0 - A10	-	Address Inputs
$\overline{WE}$	-	Write Enable Input
$\overline{OE}$	-	Output Enable Input
$\overline{CE}$	-	Chip Enable Input
DQ0 - DQ7	-	Data Input/Output
V_{CC}	-	+5 Volts
GND	-	Ground

DESCRIPTION

The DS2016 is a 16384 bit low power, fully static random access memory organized as 2048 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 150 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 250 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2016 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2016 is JEDEC pin compatible with ROM and EPROM of similar density and can be interchanged in the same socket providing flexibility of application in microcomputer systems.

OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 - A10	DQ - DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to V_{CC} + 0.3V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

4

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.3	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=60°C		1	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=25°C		100	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.8V min cycle		55	mA	

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	
Access Time	t_{ACC}			150	ns	
$\overline{OE}$ to Output Valid	t_{OE}			70	ns	
$\overline{CE}$ to Output Valid	t_{CO}			150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}	10		60	ns	
Output Hold from Address Change	t_{OH}	10			ns	

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	120			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			70	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	60			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		5.5	V	
Data Retention Current at 5.5V	I_{CCR1}		0.1*	1	µA	
Data Retention Current at 2.0V	I_{CCR2}		50*	750	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µs	
Recovery Time	t_R	2			ms	

* Typical values are at 25°C

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

4

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.1	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		500	nA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		50	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle		25	mA	

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)

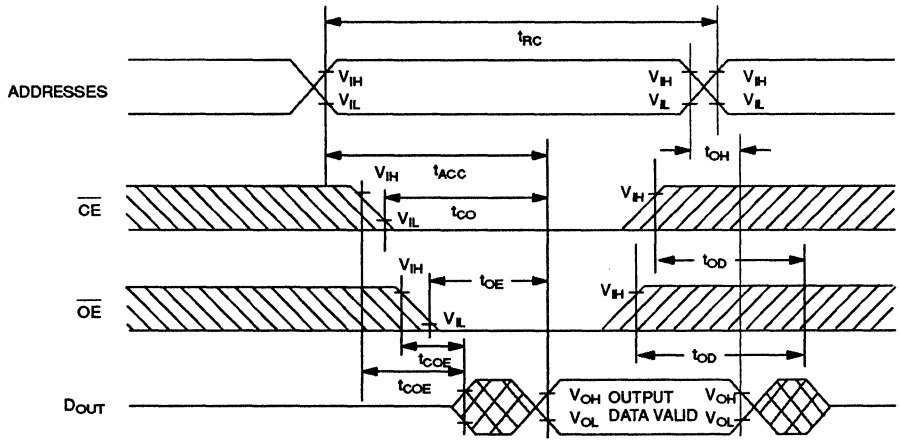
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			120	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	15			ns	
Output High-Z from Deselection	t_{OD}	5		100	ns	
Output Hold from Address Change	t_{OH}	15			ns	

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	190			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			90	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		3.5	V	
Data Retention Current at 3.5V	I_{CCR1}		50*	1000	nA	
Data Retention Current at 2.0V	I_{CCR2}		50*	750	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µs	
Recovery Time	t_R	2			ms	

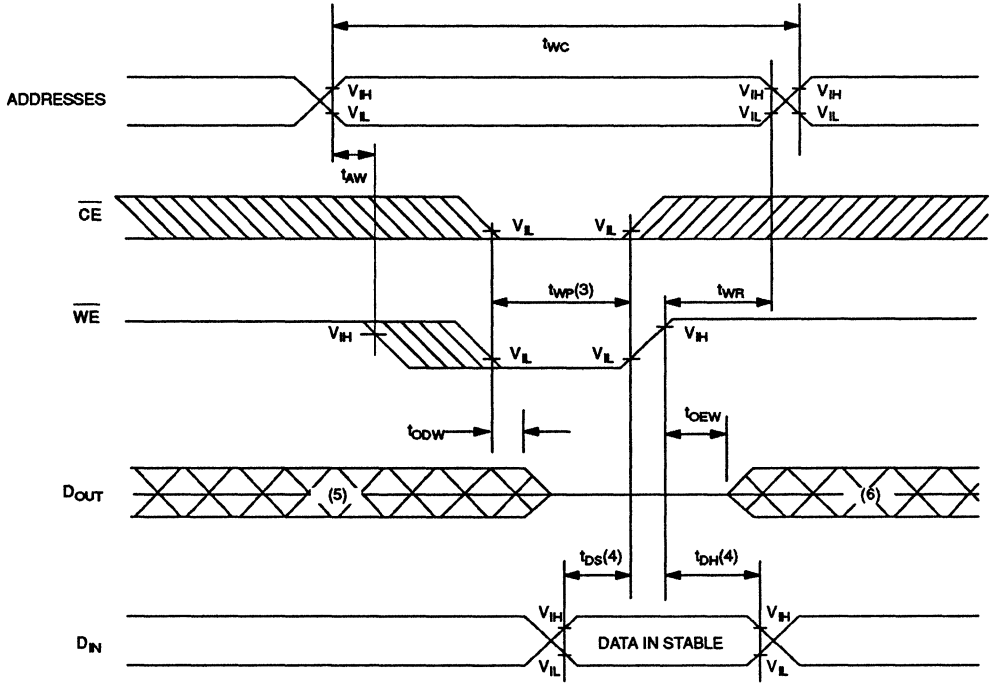
* Typical values are at 25°C

TIMING WAVEFORM: READ CYCLE



SEE NOTE 1

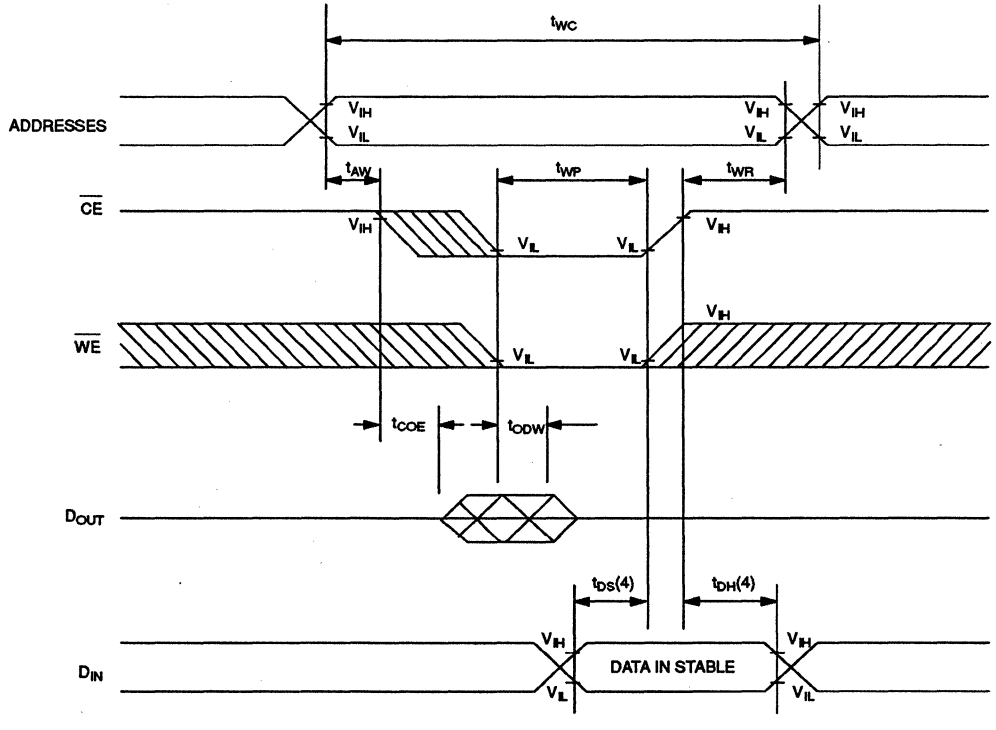
TIMING WAVEFORM: WRITE CYCLE 1



SEE NOTE 2

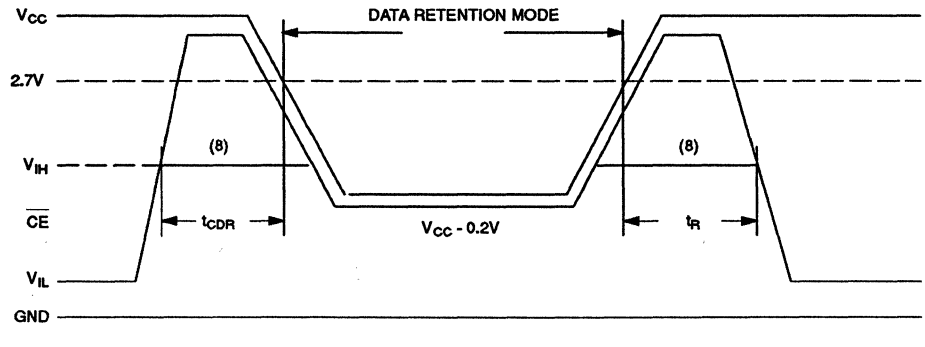
: UNKNOWN

TIMING WAVEFORM: WRITE CYCLE 2



: UNKNOWN

FIGURE 1: TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN

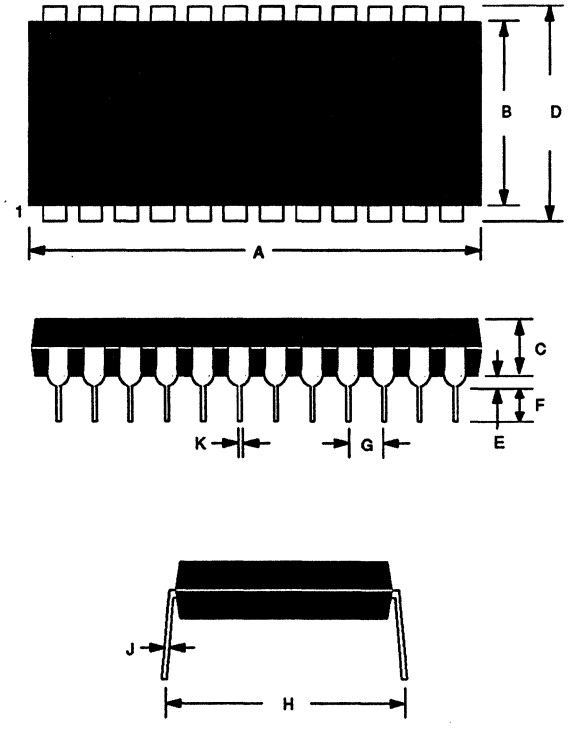


NOTES

1. WE is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V I_{CCS1} current flows.
9. The DS2016 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composit worst case characteristics from both 5V and 3V operation for deisgn purposes.

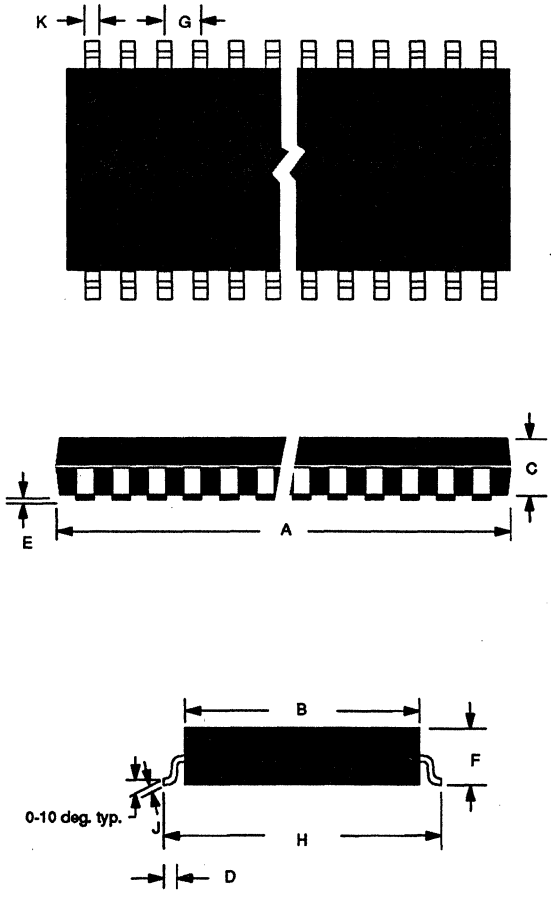
4

DS2016 24 PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS2016S 24 PIN SOIC



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	0.600	0.620
MM	15.240	15.748
B IN.	0.326	0.336
MM	8.280	8.534
C IN.	0.082	0.092
MM	2.083	2.337
D IN.	0.032	0.044
MM	0.813	1.118
E IN.	0.004	0.010
MM	0.102	0.254
F IN.	0.085	0.097
MM	2.159	2.464
G IN.	0.044	0.056
MM	1.118	1.422
H IN.	0.453	0.477
MM	11.506	12.116
J IN.	0.004	0.010
MM	0.102	0.254
K IN.	0.012	0.018
MM	0.305	0.457

DALLAS SEMICONDUCTOR

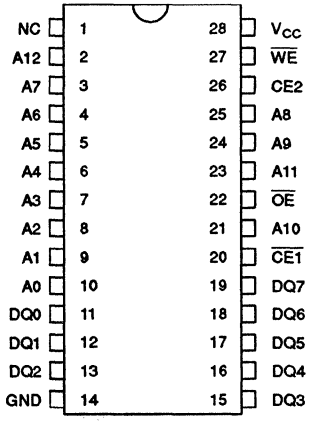
DS2064, DS2064S
8K x 8 3V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  50 nA max at $t_A = 25°C$ $V_{CC} = 3.0V$
  100 nA max at $t_A = 25°C$ $V_{CC} = 5.5V$
  1 µA max at $t_A = 60°C$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 150 ns at 5.0V and 300 ns at 3.0V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts
- Available in 28 pin DIP and 28 pin SOIC packages
- Suitable for both battery operated and battery backup applications

PIN ASSIGNMENT



28 PIN DIP OR 28 PIN SOIC

PIN DESCRIPTION

A0 - A12	-	Address Inputs
$\overline{WE}$	-	Write Enable Input
$\overline{OE}$	-	Output Enable Input
$\overline{CE1}$, CE2	-	Chip Enable Inputs
DQ0 - DQ7	-	Data Input/Output
V_{CC}	-	Power Supply Input 2.7V - 5.5V
GND	-	Ground
NC	-	No Connection

DESCRIPTION

The DS2064 is a 65536 bit low power, fully static random access memory organized as 8192 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 150 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 300 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7V to 5.5 volts. The DS2064 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2064 is JEDEC pin compatible with ROM and EPROM of similar density and can be interchanged in the same socket providing flexibility of application in microcomputer systems.

OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	A0 - A12	DQ - DQ7	POWER
READ	L	H	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	H	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	X	HIGH-Z	I_{CCS}
STANDBY	X	L	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to V_{CC} + 0.3V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

4

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.3	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=60°C		1	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.5V t_A=25°C		100	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.8V min cycle		55	mA	10

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	
Access Time	t_{ACC}			150	ns	
$\overline{OE}$ to Output Valid	t_{OE}			70	ns	
$\overline{CE}$ to Output Valid	t_{CO}			150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}	10		60	ns	
Output Hold from Address Change	t_{OH}	10			ns	

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	120			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			70	ns	7
Output Active from $\overline{WE}$	t_{OEW}	5			ns	7
Data Setup Time	t_{DS}	60			ns	
Data Hold Time	t_{DH}	0			ns	

DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		5.5	V	
Data Retention Current at 5.5V	I_{CCR1}		0.1*	1	µA	
Data Retention Current at 2.0V	I_{CCR2}		50*	750	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µs	
Recovery Time	t_R	2			ms	

* Typical values are at 25°C

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

4

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.1	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		500	nA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		50	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle		25	mA	

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)

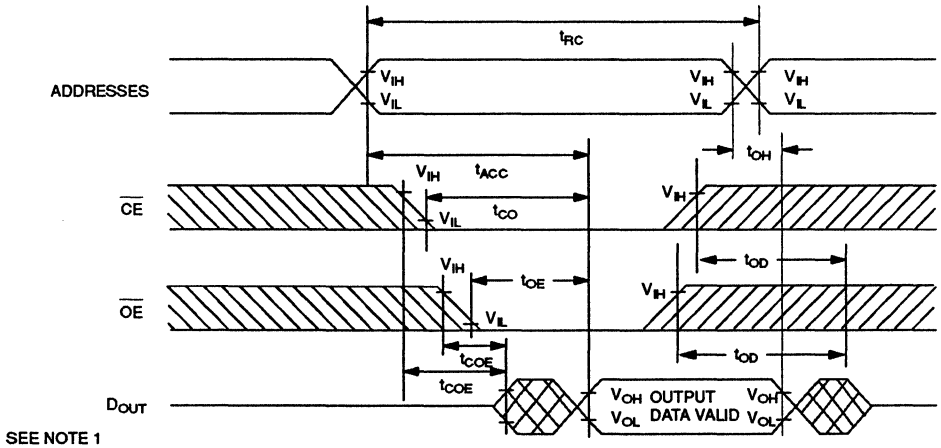
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	300			ns	
Access Time	t_{ACC}			300	ns	
$\overline{OE}$ to Output Valid	t_{OE}			150	ns	
$\overline{CE}$ to Output Valid	t_{CO}			300	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}	5		120	ns	
Output Hold from Address Change	t_{OH}	15			ns	

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	300			ns	
Write Pulse Width	t_{WP}	225			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			100	ns	7
Output Active from $\overline{WE}$	t_{OEW}	5			ns	7
Data Setup Time	t_{DS}	150			ns	
Data Hold Time	t_{DH}	0			ns	

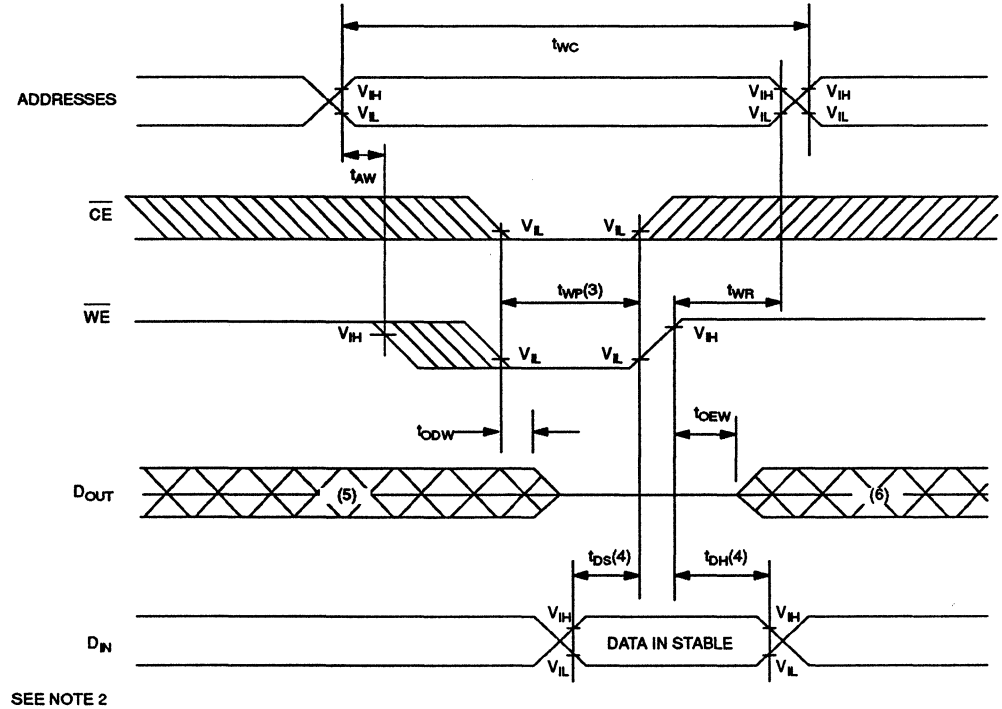
DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		3.5	V	
Data Retention Current at 3.5V	I_{CCR1}		50*	1000	nA	
Data Retention Current at 2.0V	I_{CCR2}		50*	750	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µs	
Recovery Time	t_R	2			ms	

* Typical values are at 25°C

TIMING WAVEFORM: READ CYCLE

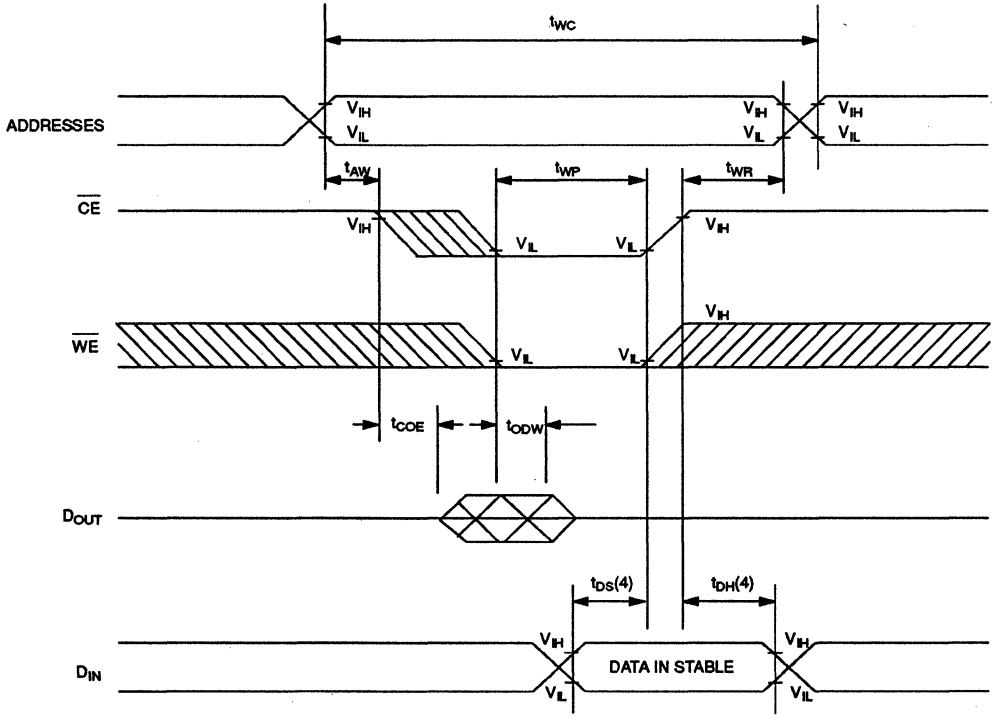


TIMING WAVEFORM: WRITE CYCLE 1



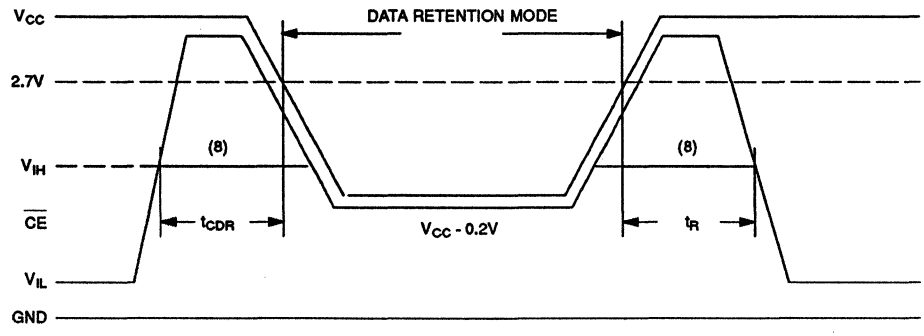
: UNKNOWN

TIMING WAVEFORM: WRITE CYCLE 2



: UNKNOWN

TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN

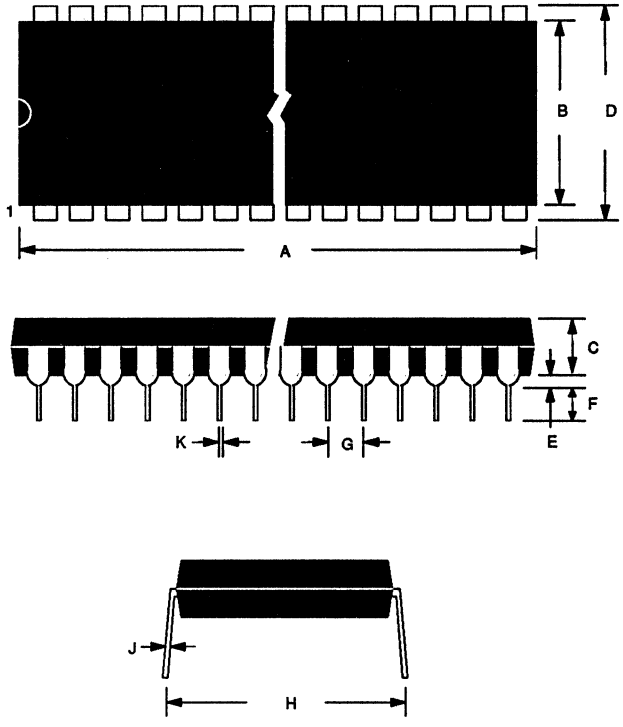


NOTES

1. WE is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V I_{CCS1} current flows.
9. The DS2064 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5 volts, used the composit worst case characteristics from both 5V and 3V operation for deisgn purposes.
10. Operating current is valid over 0°C to +85°C.

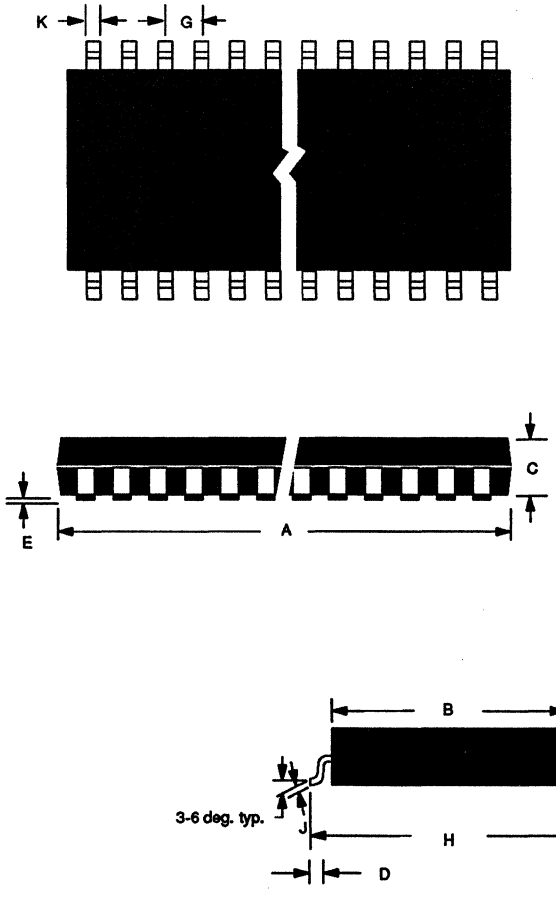
4

DS2064 28 PIN DIP



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.440	1.460
MM	30.99	32.00
B IN.	0.540	0.560
MM	13.72	14.22
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.590	0.625
MM	14.99	15.88
E IN.	0.015	0.040
MM	0.380	1.02
F IN.	0.110	0.135
MM	2.79	3.43
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS2064S 28 PIN SOIC



PKG	28-PIN	
DIM	MIN	MAX
A IN.	0.706	0.718
MM	17.932	18.237
B IN.	0.330	0.342
MM	8.382	8.687
C IN.	0.080	0.084
MM	2.032	2.134
D IN.	0.026	0.050
MM	0.660	1.270
E IN.	0.004	0.012
MM	0.102	0.305
F IN.	0.084	0.096
MM	2.134	2.438
G IN.	0.044	0.056
MM	1.118	1.422
H IN.	0.466	0.486
MM	11.836	12.344
J IN.	0.006	0.012
MM	0.152	0.305
K IN.	0.014	0.024
MM	0.356	0.610

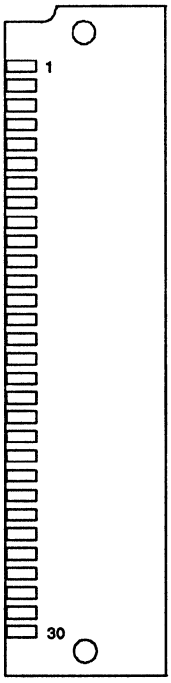
DALLAS SEMICONDUCTOR

DS2219
Nonvolatile DRAM Stik 1M x 9

FEATURES

- Maintains data in the absence of system power
- Compatible with existing DRAM SIMM applications
- Normal operating mode completely unaffected
- Nonvolatile circuitry transparent and independent from host system
- Conforms to popular JEDEC standard
- 30-position SIMM DRAM module
- Accommodates any 6- to 10-volt primary energy cell or rechargeable energy source
- Memory array available as 1024K bytes with parity bit
- $\overline{RAS}$ access time of 120 ns or 150 ns
- Power-fail detection at 10% supply

PIN ASSIGNMENT



30-Pin SIP Stik

DESCRIPTION

The DS2219 Nonvolatile DRAM Stik 1M x 9 provides all necessary timing, refresh generation, and power-down/power-up sequencing necessary to maintain data integrity during system power failure. A primary or a rechargeable energy source can be used to support data retention. Available in 1,048,576 bytes, the memory module conforms to the standard 30-position SIMM pin configuration. The self-contained memory maintenance circuitry resides transparently to the host system, eliminating the need for any additional components. Normal 5-volt operation is completely unaffected as nonvolatile circuitry is transparent to DRAM.

OPERATION – NORMAL POWER CONDITIONS

Under normal 5-volt operating conditions, the DS2219 Nonvolatile DRAM Stik behaves exactly like a standard 1024K x 9 DRAM SIMM such as the Hitachi HB56A19B. The $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs to the Stik are directed through the DS1237 directly to the individual DRAM circuits. The DS2219 will operate in this mode until the 5-volt supply at V_{CC} decays to 4.5 volts during loss of power.

OPERATION – POWER LOSS AND DATA RETENTION

When the 5-volt V_{CC} power begins to drop, the DS1237 senses this change using a precision band gap comparator and isolates all control inputs to the Stik as V_{CC} falls below 4.5 volts. Power to the individual DRAM circuits is switched from the main 5-volt supply to a backup supply connected at position 24 of the Stik. This backup supply is typically a chargeable capacitor or battery; however, any supply between six and ten volts is suitable. All refreshing is accomplished internally within the Stik and is supported continuously until V_{CC} returns to normal levels and the system signals the Stik that it is ready to assume refresh duties.

OPERATION – RETURN TO NORMAL POWER CONDITIONS

When the system 5-volt supply returns and exceeds 4.5 volts, the system supply is reconnected to the DRAM circuits and the backup supply is internally disconnected. At this time, a continuous $\overline{CAS}$ before $\overline{RAS}$ refresh is also generated internally at a cycle time of 350 ns maximum. Refreshing continues without interruption until the system signals the Stik that it is ready to assume refresh responsibility for the DRAMs. Refresh duties are shifted from the Stik to the system when a software-controlled switch is set by sending a specific pattern on address lines A5, A6, and A7 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. This address pattern is clocked into the DS1237 DRAM Nonvolatizer Chip resident on the Stik on the falling edge of $\overline{CAS}$ provided that setup and hold times are met. When the 24th cycle is correctly entered, the system will have full access to RAM and must handle refresh requirements. RAM read and write cycles can then resume without restriction.

CONSERVATION OF BACKUP SUPPLY

Another software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. The bit patterns shown in Figure 2 turn on or off this switch which disconnects or connects the backup supply.

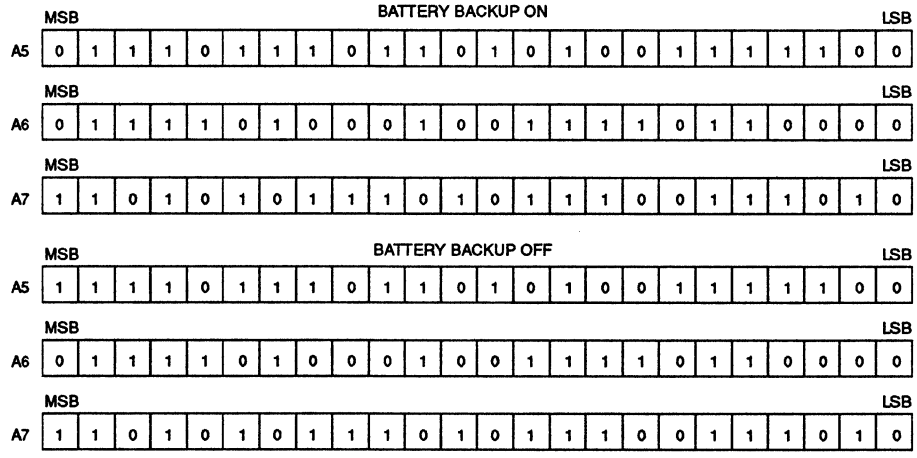
BACKUP CONDITION

The DS2219 contains two features which provide information about the condition of the backup supply. The $\overline{BC}$ (Battery Condition) pin at location 19 of the Stik provides the output for the backup supply information. If this feature is to be used, please review the "Backup Condition" section of the DS1237 DRAM Nonvolatizer Chip data sheet.

SOFTWARE SWITCH FOR PROCESSOR CONTROL POWER-UP Figure 1

	MSB																						LSB
A5	0	1	1	1	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	1	1	0	0
	MSB																						LSB
A6	0	1	1	1	1	0	1	0	0	0	1	0	0	1	1	1	1	0	1	1	0	0	0	0
	MSB																						LSB
A7	1	1	0	1	0	1	0	1	1	1	0	1	0	1	1	1	0	0	1	1	1	0	1	0

SOFTWARE CONTROLLED SWITCH FOR CONSERVATION OF BACKUP SUPPLY Figure 2



NOTE: ABOVE SEQUENCES ENTERED LSB FIRST.

PIN DESCRIPTION Table 1

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	$\overline{BC}$
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	GND
8	A3	23	DQ6
9	GND	24	V_{BAT}
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Except Battery Inputs Relative to Ground	-0.3V to +7V
Voltage on Any Pin Relative to Ground	-0.3V to +12V
Operating Temperature	0°C to +75°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Backup Supply	BKUP	6.0	8.0	10.0	V	2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			15	mA	
Power-Fail Detect	V_{TP}	4.25	4.37	4.5	V	5
Input Leakage	I_{IL}	-1.0		1.0	µA	

(0°C to 70°C, $V_{CC} < V_{TP}$)

Data Retention Current	I_{DR}		7	15	mA	4

CAPACITANCE

(t_A =25°C)

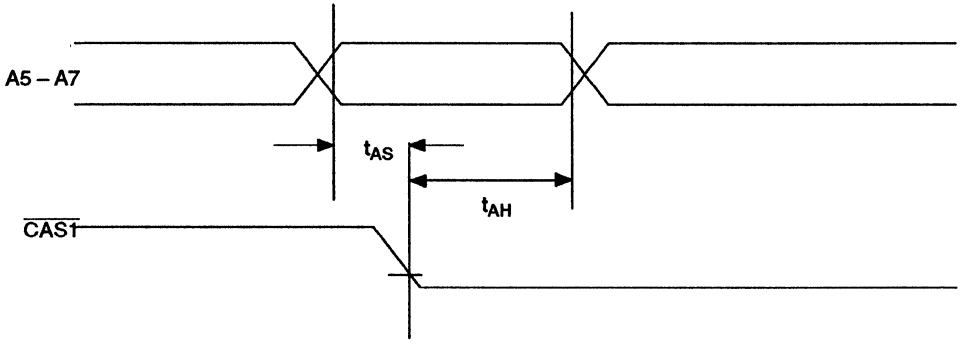
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	

SOFTWARE SEQUENCE ENTRY



NOTES:

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS2219 such that V_{CC} to the DRAMs is never below 4.5 volts, for a backup input voltage of 6.0 volts minimum.
4. This is the average current from the backup supply to maintain memory for the Stik.
5. V_{TP} is the trip point where the internal switching circuit disconnects V_{CC} and connects the internally regulated backup supply to the DRAMs. Rapid refresh is also initiated at this time.

AC ELECTRICAL CHARACTERISTICS

(t_A = 0 to+70°C, V_{CC} = 5V ± 10%)

Test Conditions

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Random Read or Write Cycle Time	t_{RC}	220			ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90			ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120		10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30		10000	ns	
Row Address Setup Time	t_{ASR}	0			ns	
Row Address Hold Time	t_{RAH}	15			ns	
Column Address Setup Time	t_{ASC}	0			ns	
Column Address Hold Time	t_{CAH}	25			ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25		90	ns	7
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20		65	ns	10
$\overline{RAS}$ Hold Time	t_{RSH}	30			ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120			ns	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10			ns	
Transition Time (Rise and Fall)	t_T	3		50	ns	6
Refresh Period	t_{REF}			8	ms	

Read Cycle

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Access Time from $\overline{RAS}$	t_{RAC}			120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}			30	ns	3, 4
Access Time from Address	t_{AA}			55	ns	3, 4
Read Command Setup Time	t_{RCS}	0			ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0			ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10			ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	55			ns	
Output Buffer Turn-Off Delay	t_{OFF}			30	ns	5

Write Cycle

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Command Setup Time	t_{WCS}	0			ns	8
Write Command Hold Time	t_{WCH}	25			ns	
Write Command Pulse Width	t_{WP}	20			ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30			ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30			ns	
Data-In Setup Time	t_{DS}	0			ns	9
Data-In Hold Time	t_{DH}	25			ns	9

Read-Modify-Write Cycle

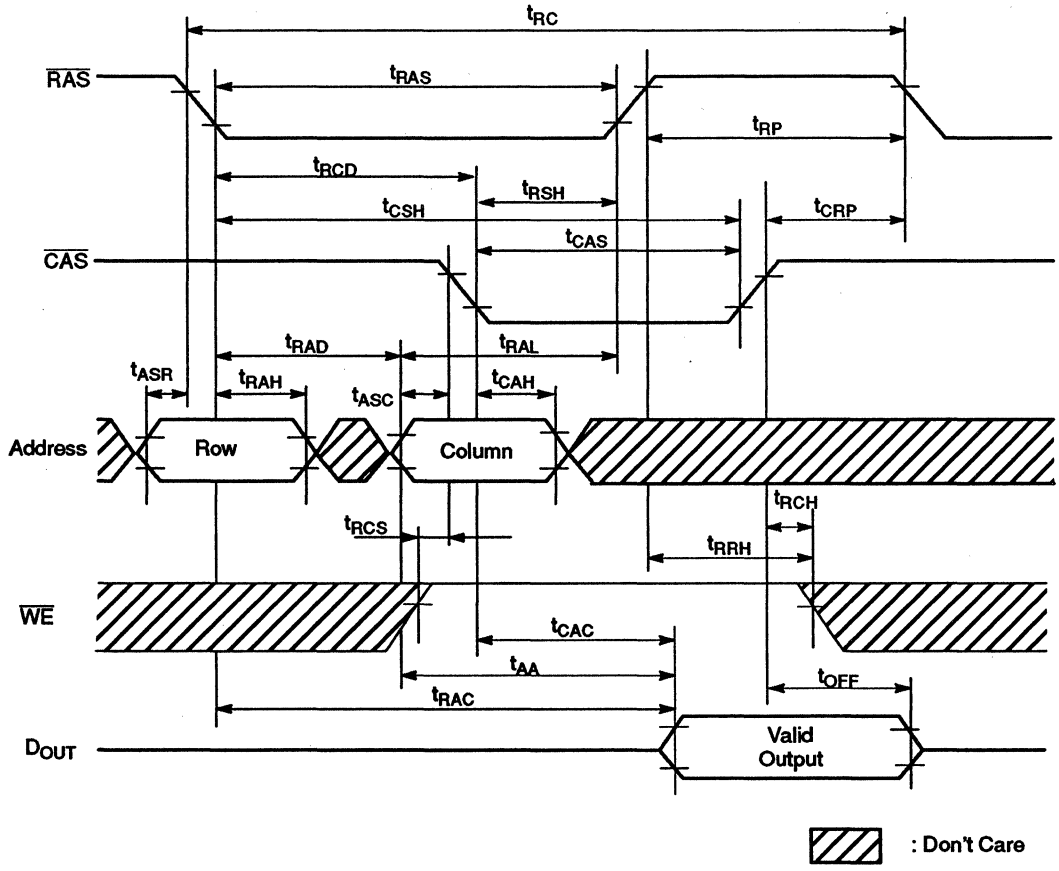
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read-Write Cycle Time	t_{RWC}	245			ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110			ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	30			ns	8
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55			ns	8

NOTES:

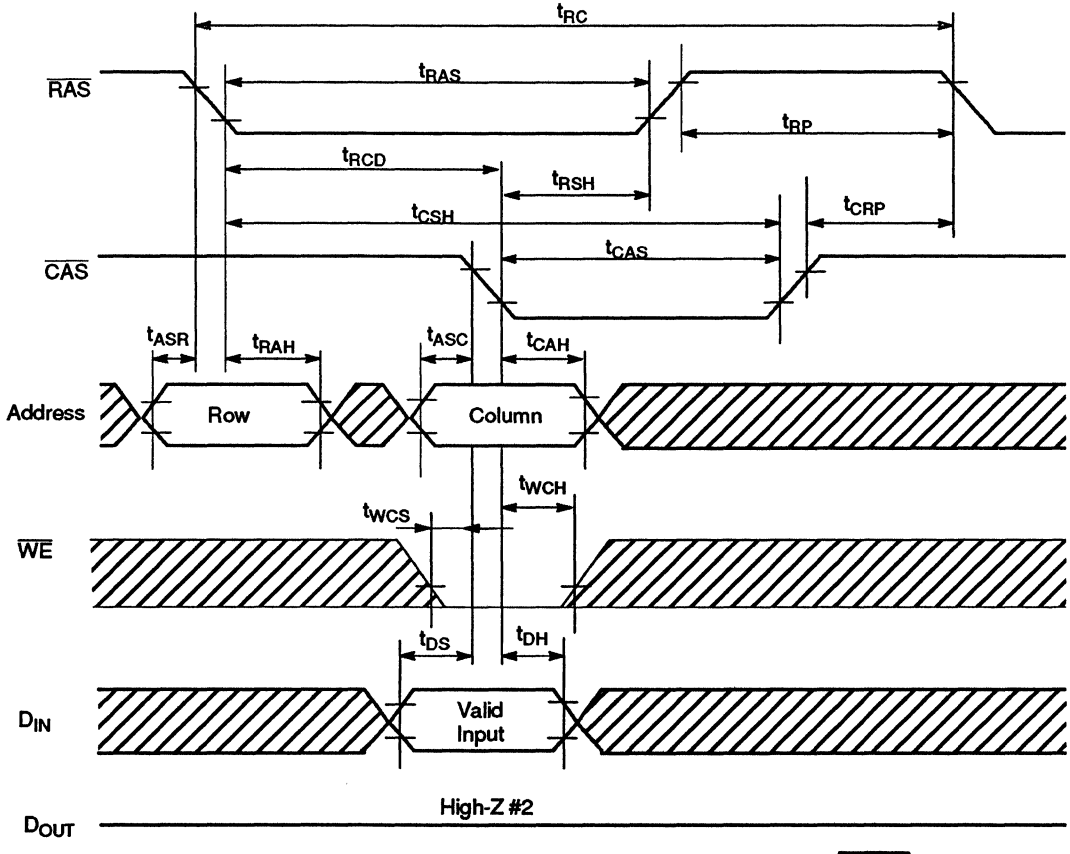
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load cirucit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} (max) is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

TIMING WAVEFORMS

Read Cycle Figure 3



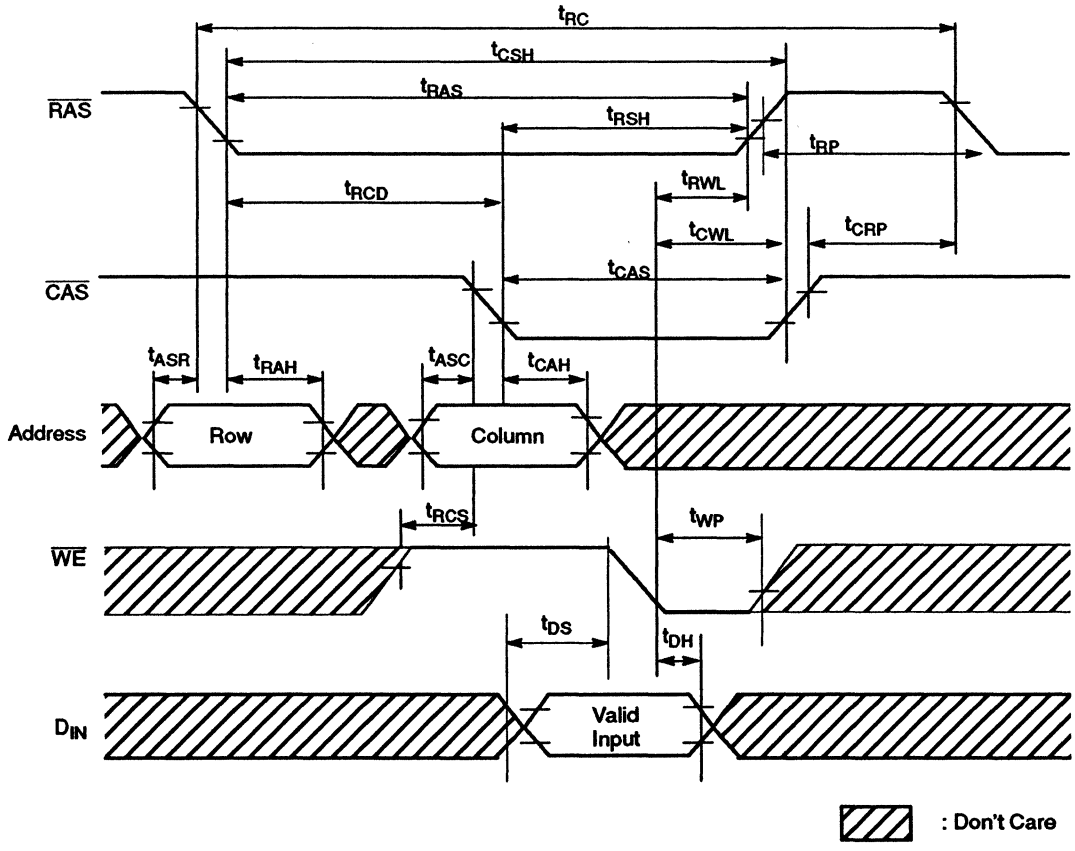
Early Write Cycle Figure 4



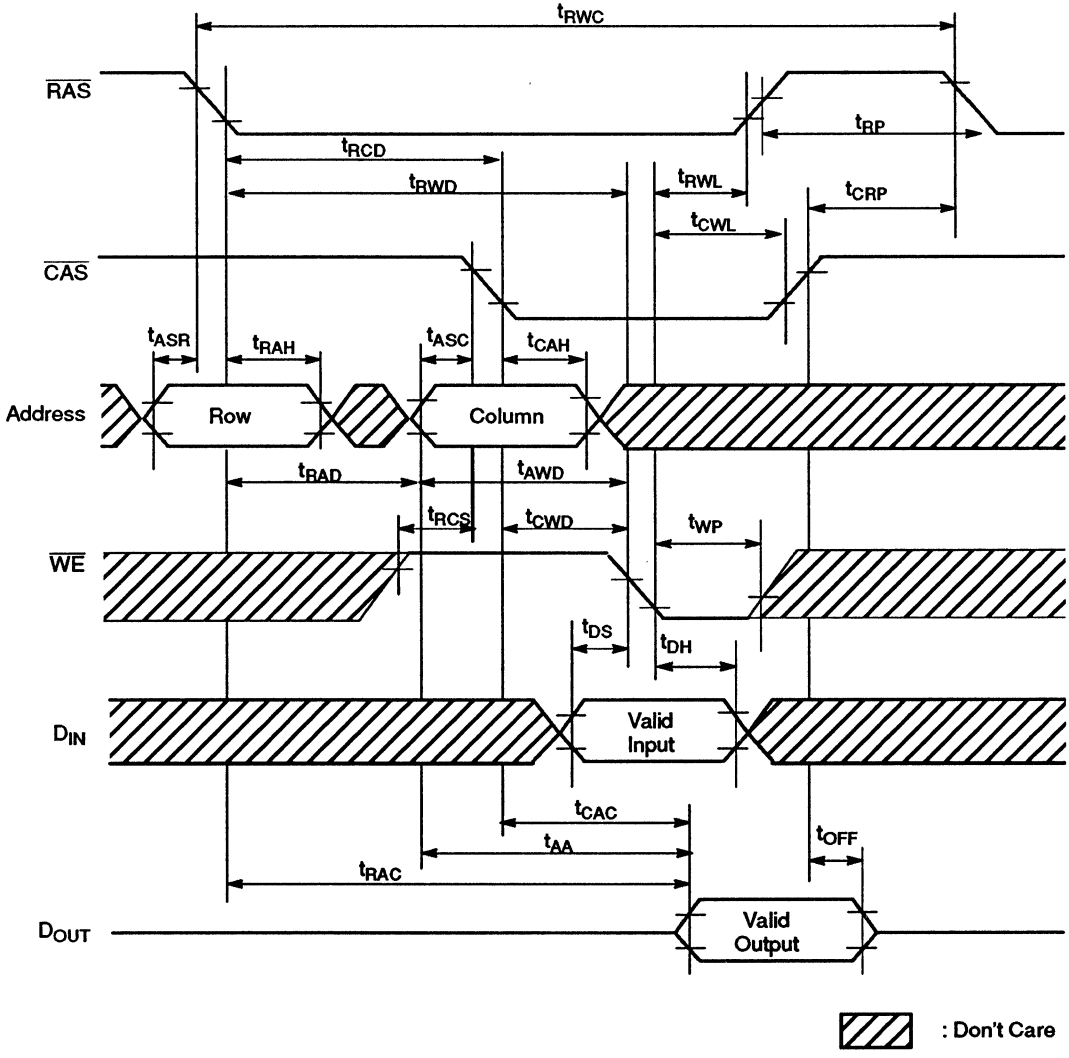
Notes: 1. ▨ : Don't Care

2. $t_{WCS} \geq t_{WCS}$ (min)

Delayed Write Cycle Figure 5



Read-Modify-Write Cycle Figure 6



APPLICATION NOTE: DIODE CONTROL OF BKUP INPUT

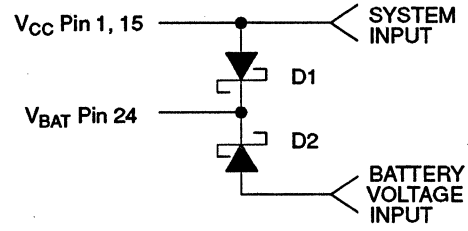
The fabrication of the DS1237 produces an N well for the BKUP Input (pin 14) that must be considered by the user. Because of this, it is imperative that the BKUP input does not go more negative from V_{CCI} input (pin 16) than the amount of one silicon diode.

This requirement can be achieved by using a Schottky diode (D1) between the V_{CCI} input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V_{CCI}.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V_{CCI} input is present.

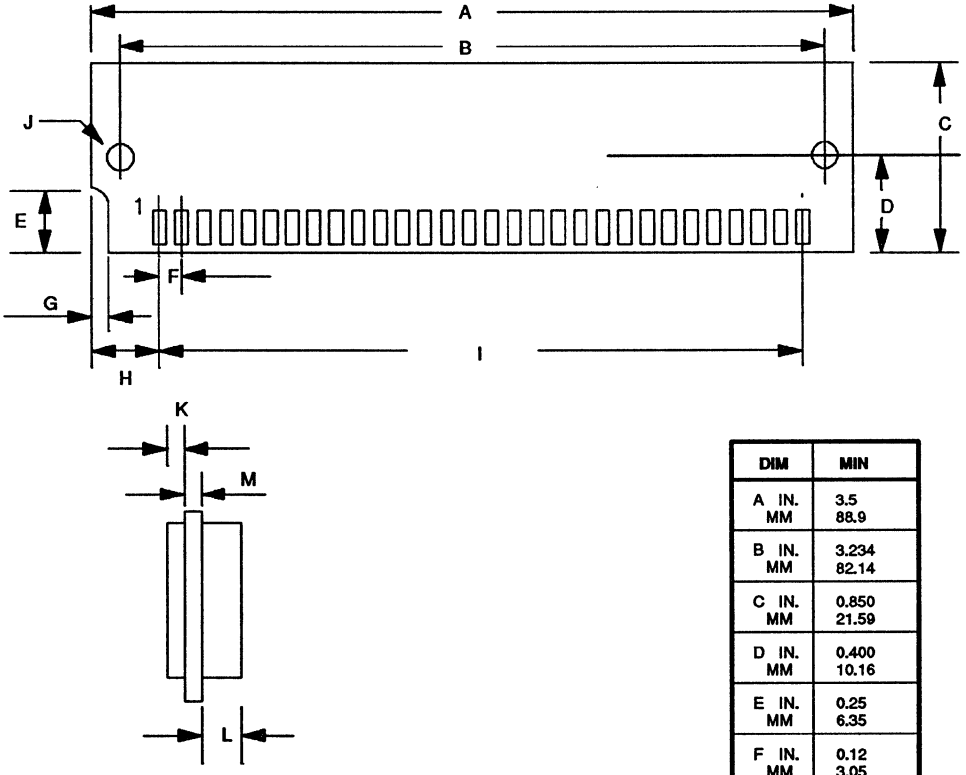
This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive supply lead from the BKUP input when the battery output voltage has decrease.

A shottky diode is suggested for D2.



NOTE: For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.

DS2219 30-PIN SIP STIK



DIM	MIN
A IN. MM	3.5 88.9
B IN. MM	3.234 82.14
C IN. MM	0.850 21.59
D IN. MM	0.400 10.16
E IN. MM	0.25 6.35
F IN. MM	0.12 3.05
G IN. MM	0.100 2.54
H IN. MM	2.90 73.66
J IN. MM	0.125 DIA. 3.18 DIA.
K IN. MM	0.150 3.81
L IN. MM	0.175 4.45
M IN. MM	0.050 1.27

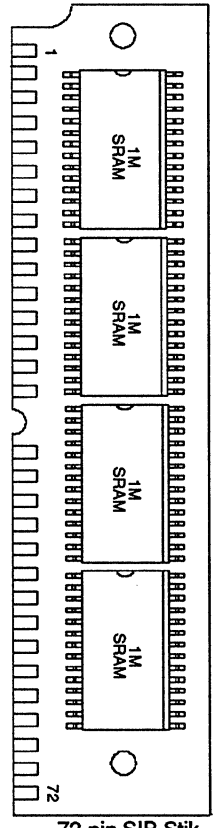
DALLAS SEMICONDUCTOR

DS2227
Flexible NV SRAM Stik

FEATURES

- Flexibly organized as 128K x 32, 256K x 16, or 512K x 8 bits
- Data retention >10 years in the absence of V_{CC}
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate chip enables allow access by byte, word, or long word
- Fast access times: 70ns, 100ns, or 120ns
- Unlimited write cycles
- Read cycle time equals write cycle time
- Employs popular JEDEC standard 72-position SIMM connection scheme
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN ASSIGNMENT



72-pin SIP Stik

DESCRIPTION

The DS2227 Flexible NV SRAM Stik is a self-contained 4,194,304-bit nonvolatile static RAM which can be flexibly organized as 128K x 32 bits, 256K x 16 bits, or 512K x 8 bits. The nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2227 employs the popular JEDEC standard 72-position SIMM connection scheme requiring no additional circuitry.

OPERATION

The DS2227 Flexible NV SRAM Stik is used like any standard static RAM. All the nonvolatile circuitry resides transparently to the user. The flexibility of the part is achieved by providing separate read, write, and chip select pins for each of the four banks of onboard memories (see Figure 1). For operation as a 512K x 8 NV SRAM Stik, tie all data lines from each bank together (i.e., all D0s together, all D1s together, etc.). Read enables and write enables are also tied together. For operation as a 256K x 16 NV SRAM Stik, tie the data lines from two banks together. Chip enables, read enables, and write enables from these banks are also tied together. Connection to the DS2227 is made by using an industry-standard, 72-position SIMM socket DS9072-72V (AMP part number 821824-8). These SIMM sockets are also available in perpendicular, inclined, or parallel mount, depending on the height available. See the DS907x SipStik™ connectors available from Dallas Semiconductor.

READ MODE

The DS2227 executes a read cycle whenever $\overline{WE}$ is inactive (high) and $\overline{CE}$ is active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2227 is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs to t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The DS2227 provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2227 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2227 checks lithium status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2227 the lithium is checked with a precision comparator. If the lithium supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications data integrity is paramount. The DS2227 provides lithium cell redundancy and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the lithium with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user.

PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	V_{CC} Power	38	4-D0
2	1-D0	39	4-D1
3	1-D1	40	4-D2
4	1-D2	41	4-D3
5	1-D3	42	4-D4
6	1-D4	43	40D5
7	1-D5	44	4-D6
8	1-D6	45	4-D7
99	1-D7	46	NC
10	NC	47	4-Chip Enable
11	1-Chip Enable	48	4-Output Enable
12	1-Output Enable	49	4-Write Enable
13	1-Write Enable	50	Ground
14	2-D0	51	V_{CC} Power
15	2-D1	52	A0
16	2-D2	53	A1
17	2-D3	54	A2
18	2-D4	55	A3
19	2-D5	56	A4
20	2-D6	57	A5
21	2-D7	58	A6
22	NC	59	A7
23	2-Chip Enable	60	A8
24	2-Output Enable	61	A9
25	2-Write Enable	62	A10
26	3-D0	63	A11
27	3-D1	64	A12
28	3-D2	65	A13
29	3-D3	66	A14
30	3-D4	67	A15
31	3-D5	68	A16
32	3-D6	69	NC
33	3-D7	70	NC
34	NC	71	NC
35	3-Chip Enable	72	Ground
36	3-Output Enable		
37	3-Write Enable		

NOTE: Leave all pins marked as NC unconnected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40° to +85°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-5.0		+5.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		60	280	mA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	40	pF	
Output Capacitance	C_{OUT}		5	10	pF	

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} Before Power-down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 4.25V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-up	t_{REC}	2	80	125	ms	

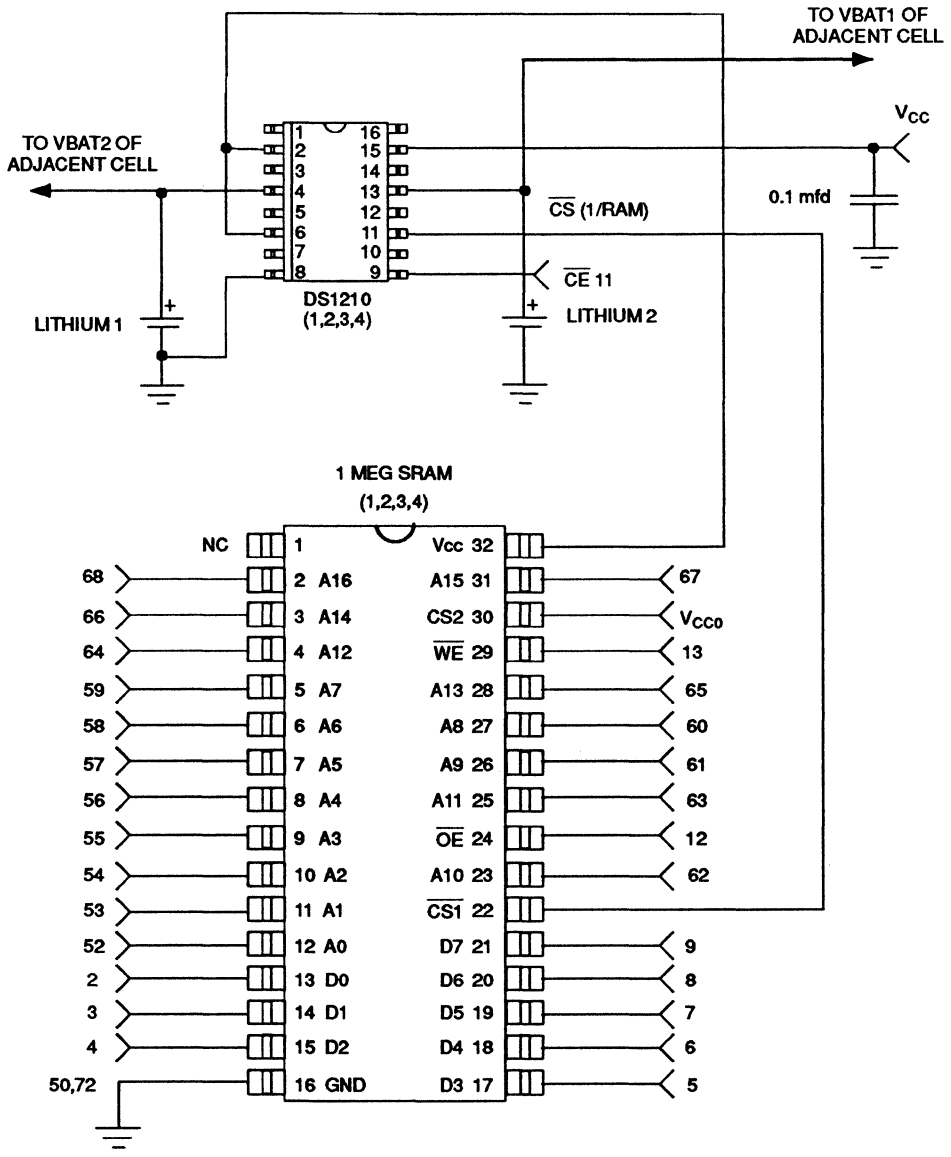
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			Years	

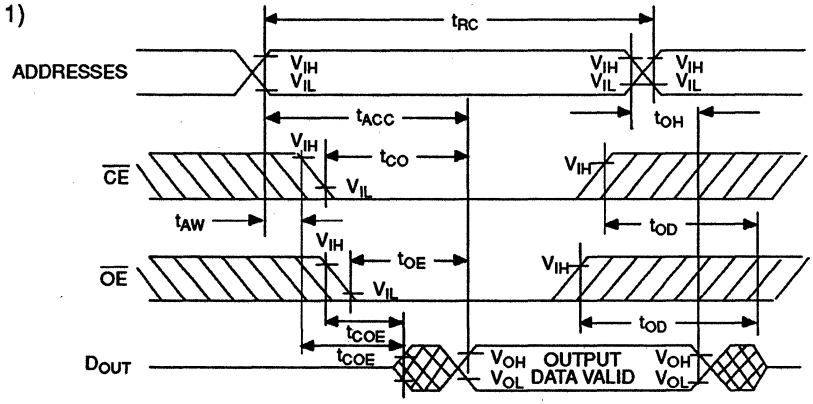
AC ELECTRICAL CHARACTERISTICS

		DS2227-70		DS2227-100		DS2227-120			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	70		100		120		ns	10
Access Time	t_{ACC}		70		100		120	ns	10
$\overline{OE}$ to Output Valid	t_{OE}		35		50		60	ns	10
$\overline{CE}$ to Output Valid	t_{CO}		70		100		120	ns	10
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	10
Output High Z from Deselection	t_{OD}		25		35		40	ns	10
Output Hold from Address Change	t_{OH}	5		5		5		ns	10
Write Cycle Time	t_{WC}	70		100		120		ns	10
Write Pulse Width	t_{WP}	55		75		90		ns	3,10
Address Setup Time	t_{AW}	0		0		0		ns	10
Write Recovery Time	t_{WR}	20		20		20		ns	10
Output High Z from WE	t_{ODW}		25		35		40	ns	10
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	8,10
Data Setup Time	t_{DS}	30		40		50		ns	4,10
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4,5,10

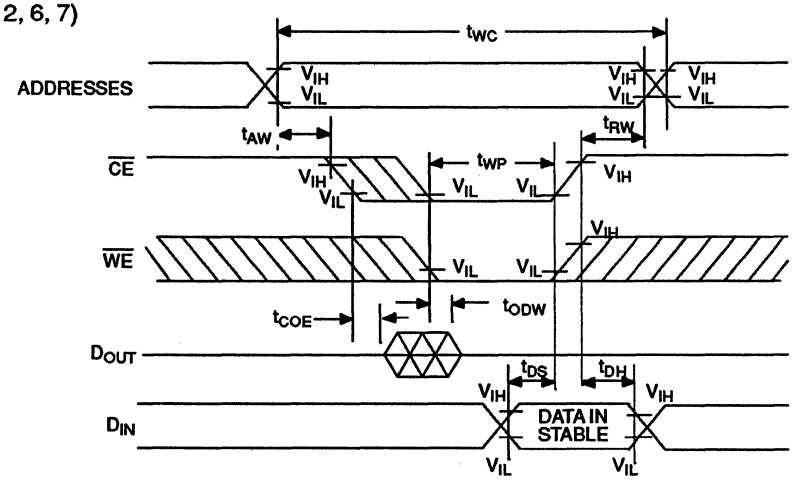
SCHEMATIC (1 CELL) Figure 1



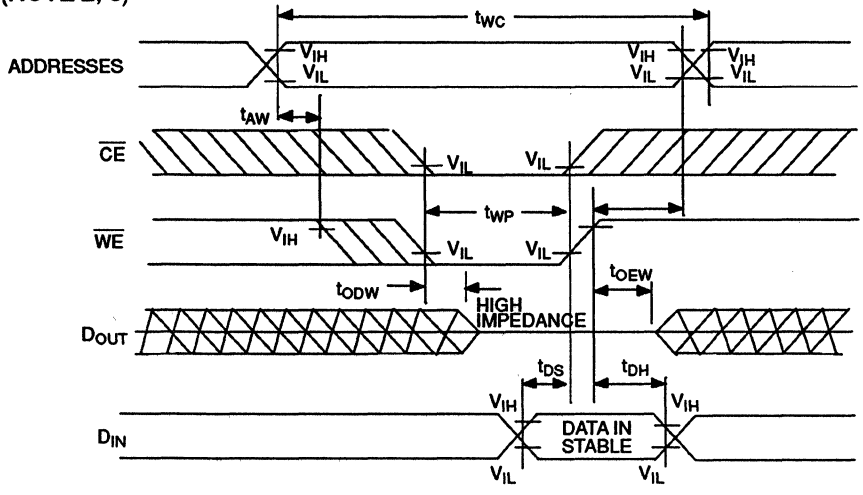
READ CYCLE (NOTE 1)



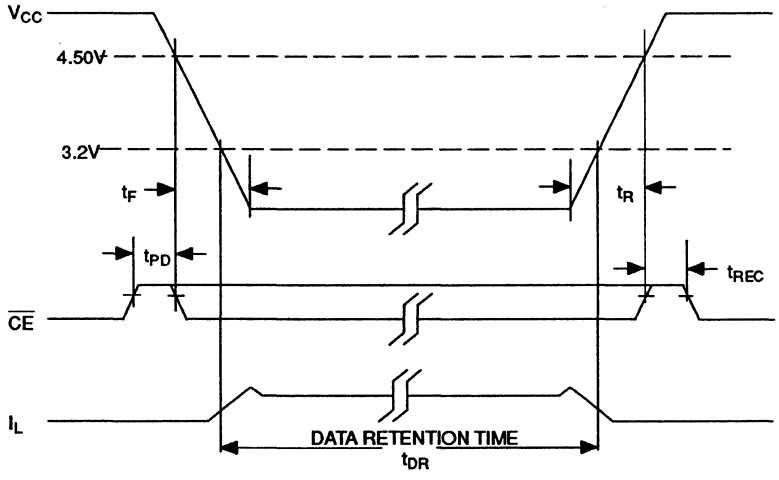
WRITE CYCLE 1 (NOTE 2, 6, 7)



WRITE CYCLE 2 (NOTE 2, 8)



POWER-UP/POWER-DOWN CONDITION



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NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state in this period.
8. If the $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2227 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The minimum expected t_{DR} is defined as starting at the date of manufacture.
10. Timings are valid only when $\overline{CE}$ is tied low.

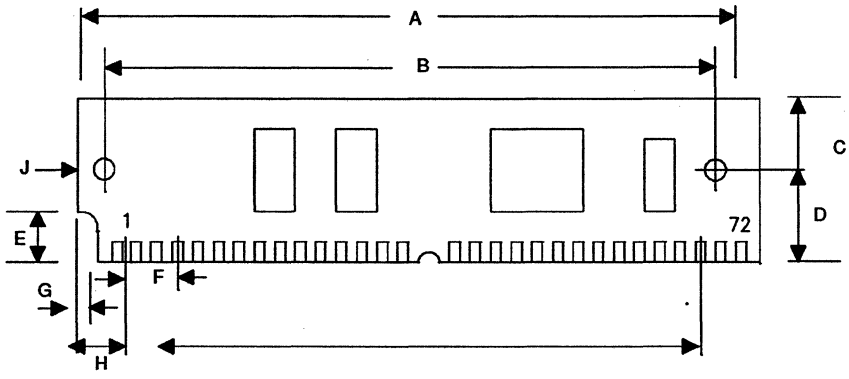
DC TEST CONDITIONS

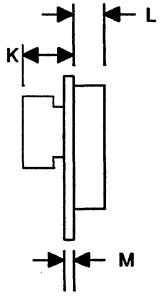
Outputs Open
t cycle = 200 ns
All Voltages are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL gate
Input Pulse Levels: 0 – 3.0 V
Timing Measurements Reference Levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5ns

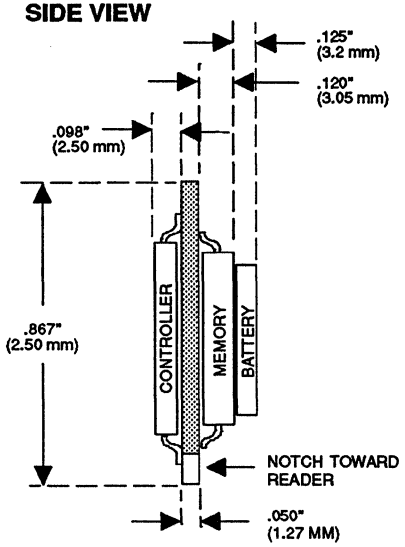
DS2227 72-PIN SIP STIK





DIM	MIN
A IN. MM	4.050 102.87
B IN. MM	3.784 96.11
C IN. MM	0.850 21.59
D IN. MM	0.400 10.16
E IN. MM	0.25 6.35
F IN. MM	0.050 1.27
G IN. MM	0.080 2.03
H IN. MM	0.250 6.35
J IN. MM	0.125 DIA. 3.18 DIA.
K IN. MM	0.300 7.62
L IN. MM	0.173 4.39
M IN. MM	0.050 1.27

SIDE VIEW



SEE 72-PIN SIP STIK FOR OTHER DIMENSIONS

DALLAS SEMICONDUCTOR

DS2229
Word-Wide 8 Meg SRAM Stik

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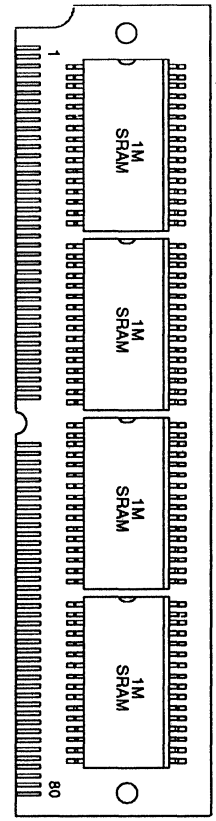
FEATURES

- Organized as a high density 512K x 16 bit Stik™
- Fast access times – 85ns, 100ns, 120ns
- Unlimited write cycles
- Employs popular JEDEC standard 80-position SIMM connector
- Full ± 10% operating range
- Read cycle time equals write cycle time
- Ultra-low standby current < 20 µA
- Suitable for battery-backed applications

PIN ASSIGNMENT



80-pin SIP Stik

DESCRIPTION

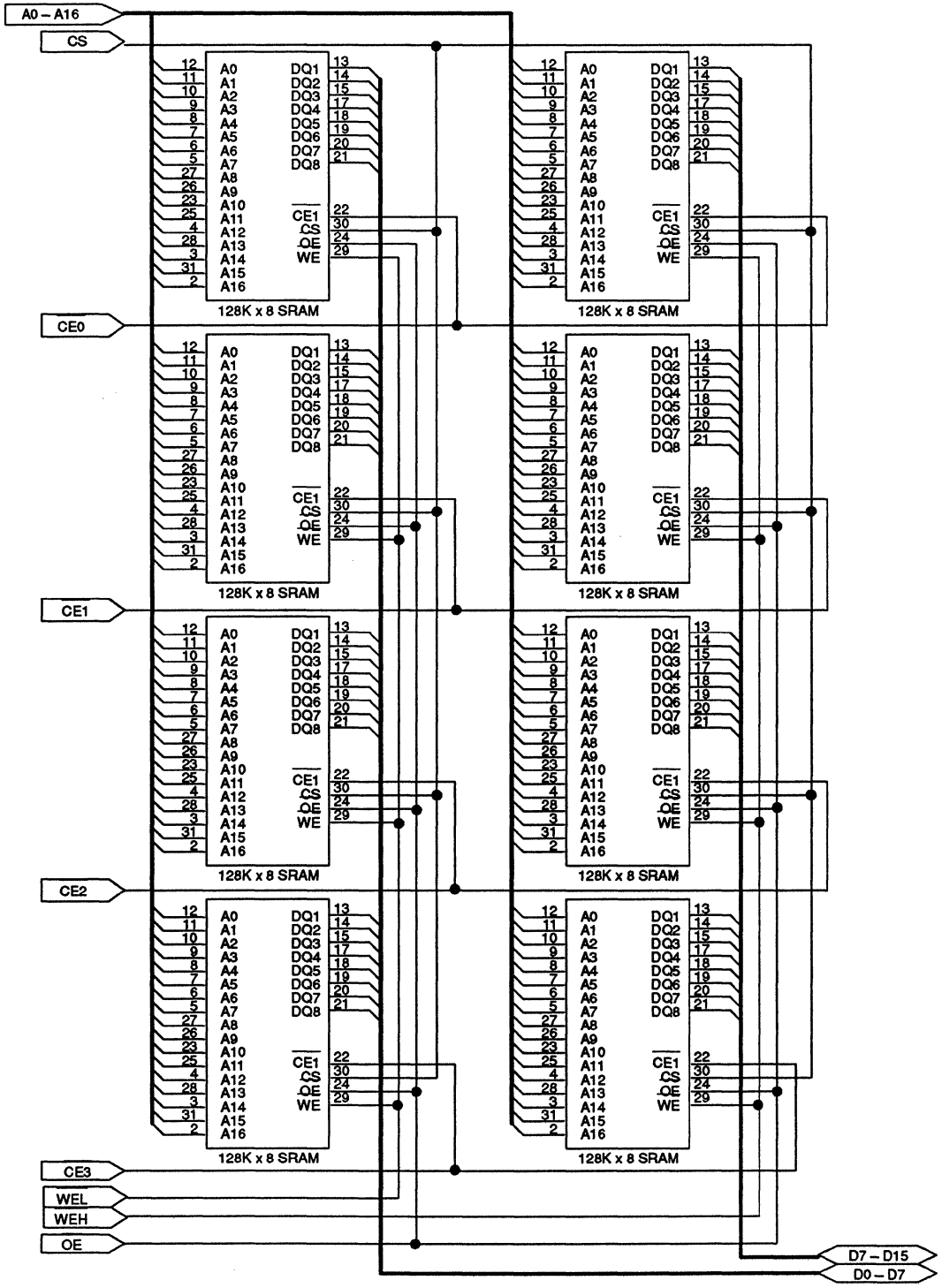
The DS2229 is a 8,388,608-bit low-power fully static Random Access Memory organized as a 524,888 word by 16 bits using CMOS technology. The device employs the popular JEDEC standard 80-pin SIMM connection scheme with no additional circuitry required. The device operates from a single power supply with a voltage input of 4.5 to 5.5 volts. The Chip Enable inputs ($\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$) are used for device selection and can be used in order to achieve the minimum standby current mode which facilitates battery backup. The device provides a fast access time of 85nS. The DS2229 maintains TTL levels over input voltage range 4.5V to 5.5V. The DS2229 is JEDEC pin compatible (see Figure 1) with flash EEPROM memory SIMM boards of similar density.

PIN DESCRIPTION Figure 1

PIN #	PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME
1	GND	32	NC	63	DQ_7
2	V_{CC}	33	NC	64	DQ_6
3	NC	34	NC	65	DQ_5
4	$\overline{OE}$	35	CS	66	DQ_4
5	$\overline{WEH}$	36	A_{16}	67	DQ_3
6	$\overline{WEL}$	37	A_{15}	68	DQ_2
7	NC	38	A_{14}	69	DQ_1
8	NC	39	A_{13}	70	DQ_0
9	NC	40	A_{12}	71	NC
10	NC	41	A_{11}	72	V_{CC}
11	NC	42	A_{10}	73	NC
12	NC	43	A_9	74	GND
13	NC	44	A_8	75	NC
14	NC	45	A_7	76	GND
15	NC	46	A_6	77	GND
16	NC	47	A_5	78	
17	NC	48	A_4	79	
18	NC	49	A_3	80	GND
19	NC	50	A_2		
20	NC	51	A_1		
21	$\overline{CE3}$	52	A_0		
22	$\overline{CE2}$	53	GND		
23	$\overline{CE1}$	54	GND		
24	$\overline{CE0}$	55	DQ_{15}		
25	GND	56	DQ_{14}		
26	NC	57	DQ_{13}		
27	NC	58	DQ_{12}		
28	NC	59	DQ_{11}		
29	NC	60	DQ_{10}		
30	NC	61	DQ_9		
31	NC	62	DQ_8		

PIN NAME	DESCRIPTION
$A_0 - A_{16}$	Address Input
$\overline{WEL}$	Write Enable Input Low
$\overline{WEH}$	Write Enable Input High
$\overline{OE}$	Output Enable Input
NC	No Connect
$\overline{CE0} - \overline{CE3}$	Chip Enable Input
CS	Chip Select
$DQ_0 - DQ_{15}$	Data Input/Output
V_{CC}	+5 Volts
GND	Ground

DS2229 STATIC RAM MODULE FUNCTION DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage	-0.3V to +7.0V
Input, Input/Output Voltage	-0.3 to V_{CC} +0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATION MODE

MODE	$\overline{CE0}$ - $\overline{CE3}$	CS	$\overline{OE}$	$\overline{WE}$	A0 – A16	DQ – DQ15	POWER
READ	L	H	L	H	STABLE	DATA OUT	I_{CC0}
WRITE	L	H	X	L	STABLE	DATA IN	I_{CC0}
DESELECT	L	H	H	H	X	HIGH-Z	I_{CC0}
STANDBY	H	X	X	X	X	HIGH-Z	I_{CCS}
STANDBY	X	L	X	X	X	HIGH-Z	I_{CCS}

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

RECOMMENDED DC OPERATING CONDITIONS

(t_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

DC CHARACTERISTICS

(t_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	0V ≤ V_{IN} ≤ V_{CC}		8	µA	
I/O Leakage Current	I_{LO}	$\overline{CE0}$ – $\overline{CE3}$ = V_{IH}, 0V ≤ $V_{I/O}$ ≤ V_{CC}		8	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE0}$ - $\overline{CE3}$ = 2.0V t_A = 25°C		8	µA	10
Standby Current	I_{CCS}	$\overline{CE0}$ – $\overline{CE3}$ ≥ V_{CC} -0.3V t_A=25°C		10	µA	10
Operating Current	I_{CC1}	$\overline{CE0}$ – $\overline{CE3}$ = 0.8V; Cycle=200nS t_A= 25°C		60	mA	10

LOW VCC DATA RETENTION CHARACTERISTICS

(t_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CE0} - \overline{CE3} \geq V_{CC}$ -0.2V, CS ≥ V_{CC} -0.2V or 0V ≤ CS ≤ 0.2V $V_{IN} \geq$ 0V
Data Retention Current	I_{CCDR}	–	1	8	µA	V_{CC} = 3.0V, $V_{IN} \geq$ 0V $\overline{CE0} - \overline{CE3} \geq V_{CC}$ -0.2V, CS ≥ V_{CC} –0.2V or 0V ≤ CS ≤ 0.2V t_A=25°C
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	5	–	–	ms	

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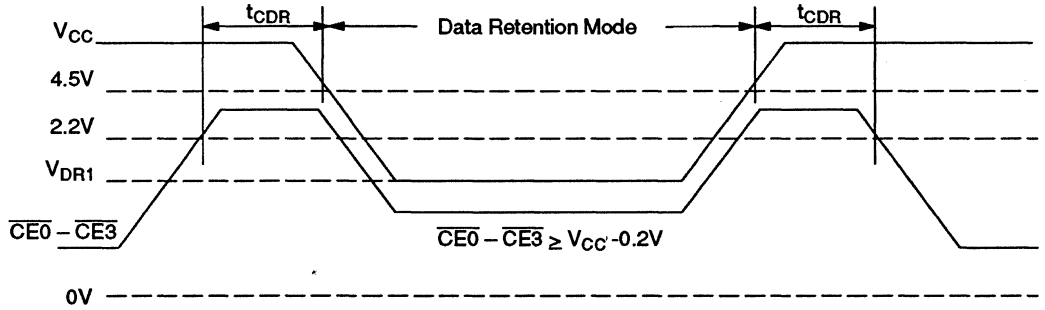
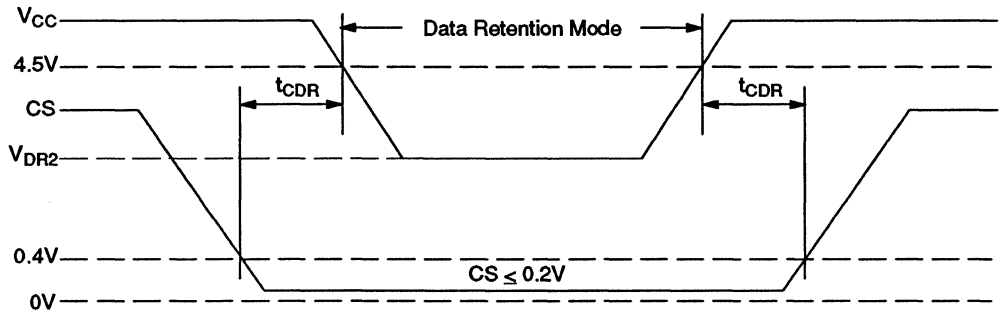
LOW VCC DATA RETENTION TIMING WAVEFORM (1) ($\overline{CE0} - \overline{CE3}$ Controlled) Figure 3



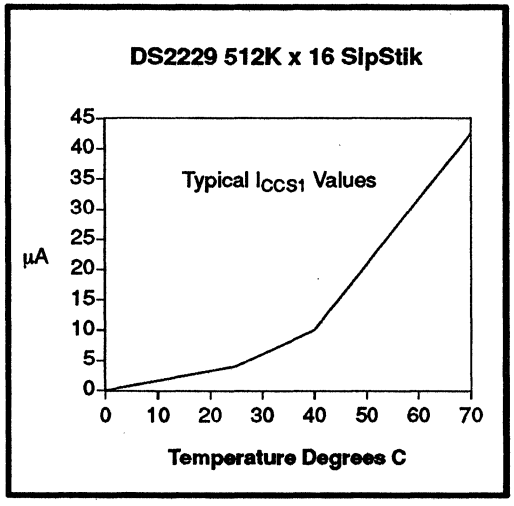
LOW VCC DATA RETENTION TIMING WAVEFORM (2) (CS Controlled) Figure 4

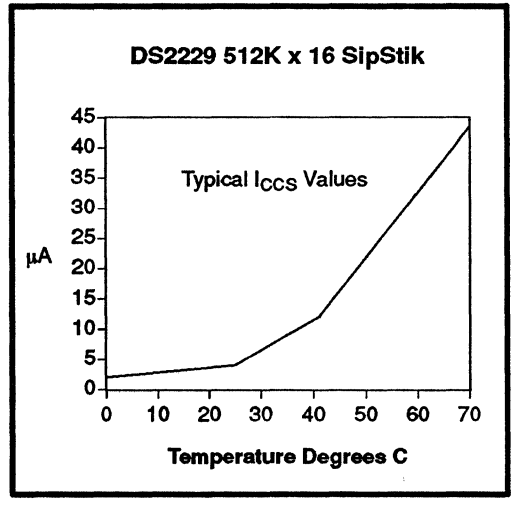


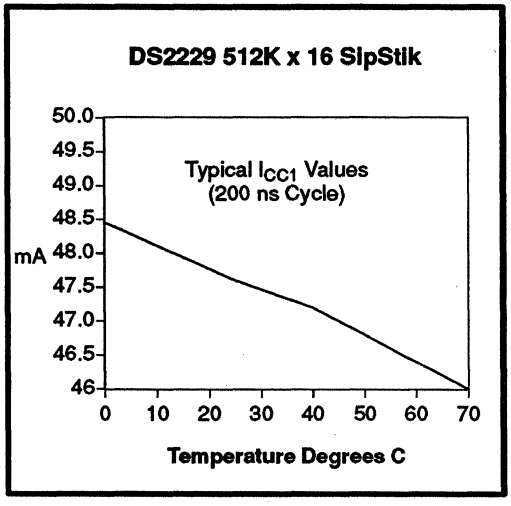
NOTES:

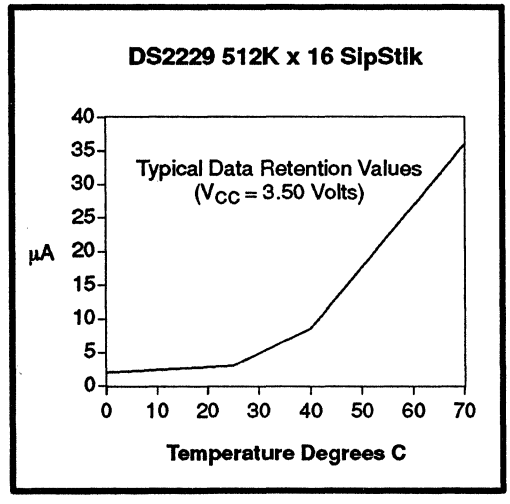
1. CS controls address buffer, $\overline{WE}$ buffer, $\overline{CE0}$ – $\overline{CE3}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If CS controls data retention mode, V_{IN} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CE0}$ – $\overline{CE3}$, I/O) can be in the high impedance state. If $\overline{CE0}$ – $\overline{CE3}$ controls data retention mode, CS must be CS ≥ V_{CC} -0.2V or 0V ≤ CS ≤ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

PRODUCT CHARACTERISTICS









AC ELECTRICAL CHARACTERISTICS READ CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

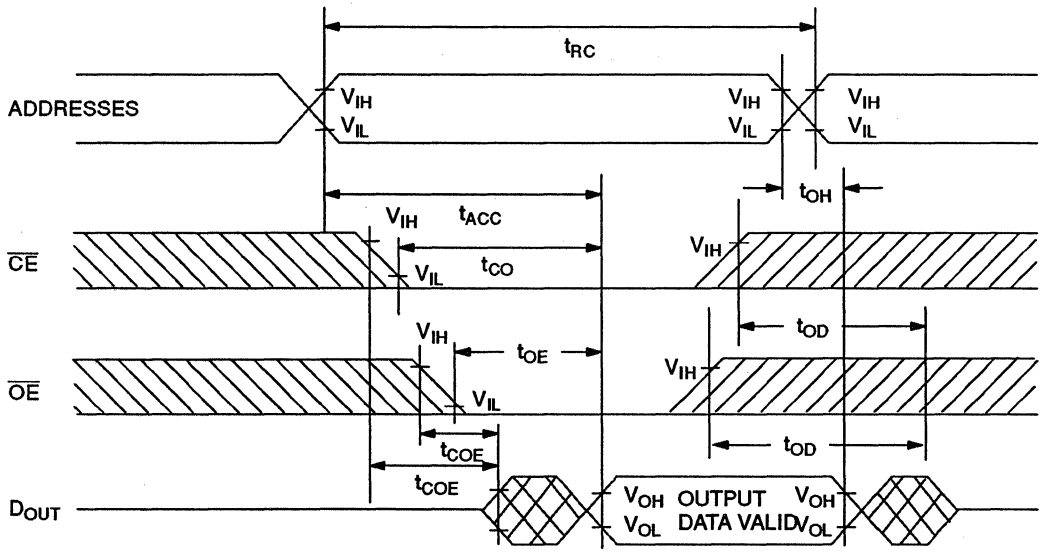
		DS2229-85		DS2229-100		DS2229-120			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	85		100		120		ns	
Access Time	t_{ACC}		85		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		45		50		60	ns	
$\overline{CE0}$ – $\overline{CE3}$ to Output Valid	t_{CO}		85		100		120	ns	
$\overline{OE}$ or $\overline{CE0}$ – $\overline{CE3}$ to Output In Low-Z	t_{COE}	10		10		10		ns	
Output High-Z from Deselection	t_{OD}	0	30	0	35	0	45	ns	
Output Hold from Address Change	t_{OH}	10		10		10		ns	

AC ELECTRICAL CHARACTERISTICS WRITE CYCLE

(0°C to 70°C; V_{CC} = 5V ± 10%)

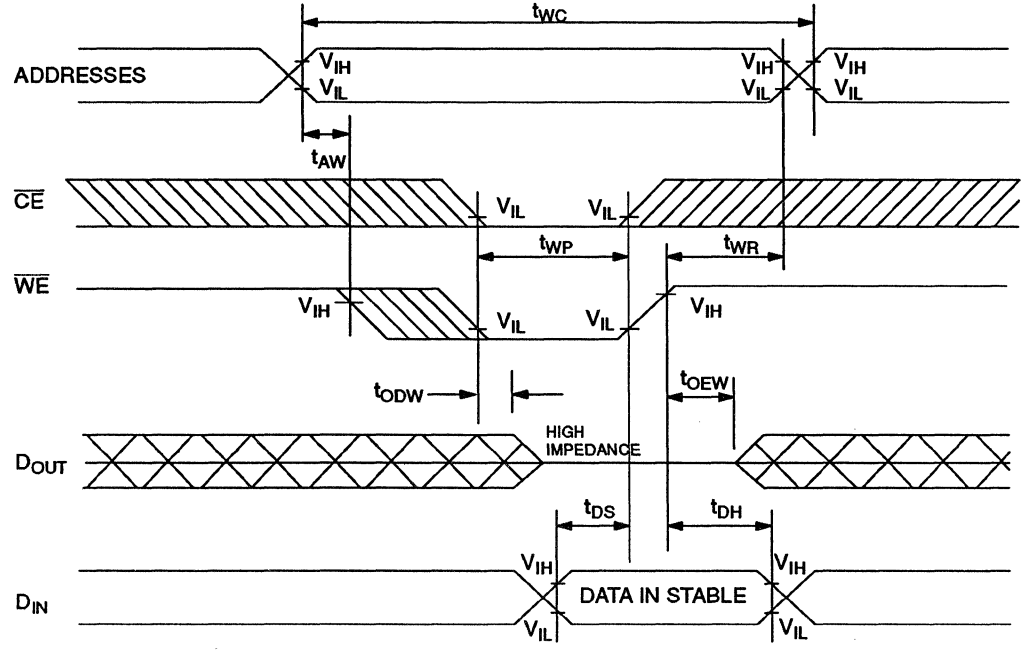
		DS2229-85		DS2229-100		DS2229-120			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	85		100		120		ns	
Write Pulse Width	t_{WP}	65		75		85		ns	
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		15		ns	
Output High-Z from $\overline{WE}$	t_{ODW}	0	30	0	35	0	40	ns	
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	
Data Setup Time	t_{DS}	35		40		45		ns	
Data Hold Time from $\overline{WE}$	t_{DH}	0		0		0		ns	

READ CYCLE Figure 5



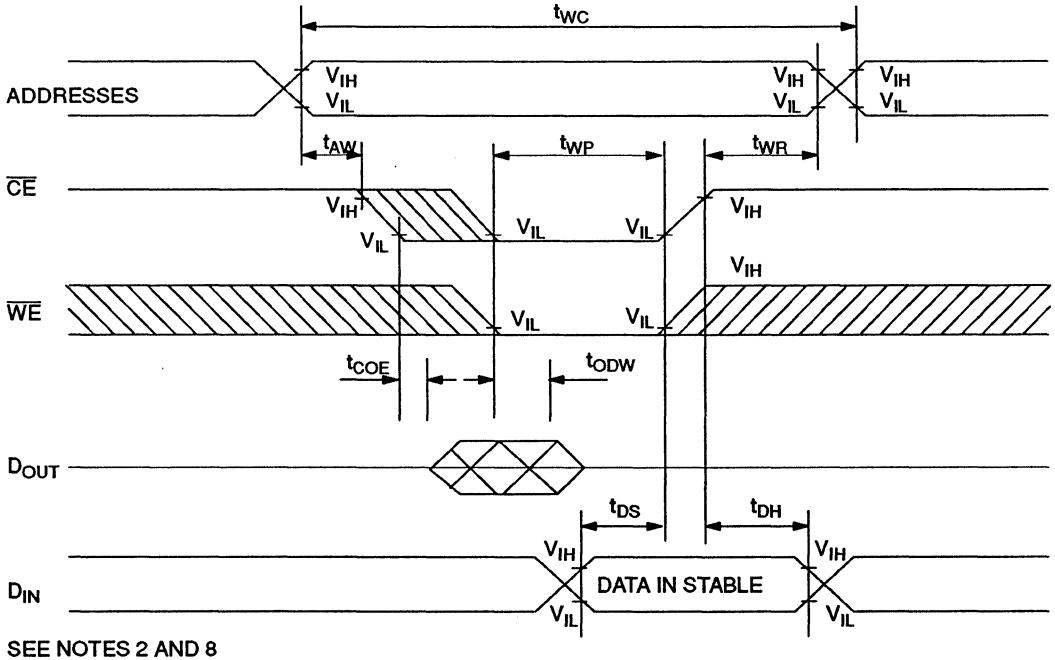
SEE NOTE 1

WRITE CYCLE1 Figure 6



SEE NOTES 2, 6, AND 7

WRITE CYCLE 2 Figure 7



SEE NOTES 2 AND 8

NOTES

*1. A write occurs during the overlap of a low $\overline{CE0}$ – $\overline{CE3}$, a high CS, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CE0}$ – $\overline{CE3}$ going low, CS going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CE0}$ – $\overline{CE3}$ going high, CS going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CE0}$ – $\overline{CE3}$ going low or CS going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CE0}$ – $\overline{CE3}$ or $\overline{WE}$ going high or CS going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

*6. If $\overline{CE0}$ – $\overline{CE3}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.

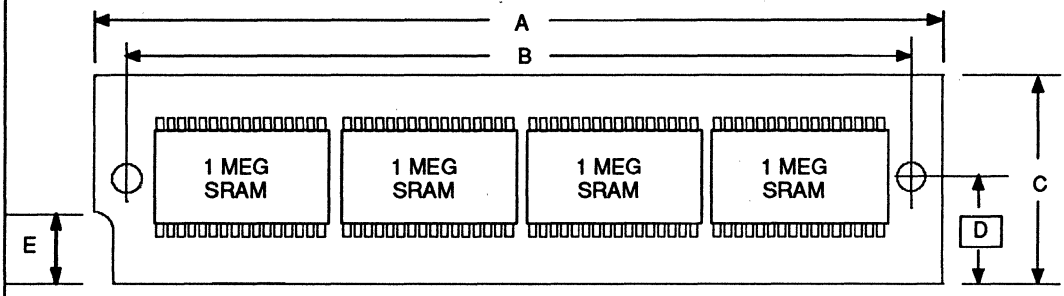
*7. If $\overline{CE0}$ – $\overline{CE3}$ is low and CS is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

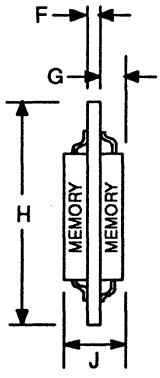
*8. This parameter is sampled and not 100% tested.

*9. This value is measured from CS going low to the end of write cycle.

*10. Only one $\overline{CE}$ active during any read or write cycle.

DS2229 80-PIN SIP STIK





DIM	MIN
A IN.	4.650
MM	118.11
B IN.	4.384
MM	111.35
C IN.	0.714
MM	18.14
D IN.	0.400
MM	10.16
E IN.	0.25
MM	6.35
F IN.	0.540
MM	13.72
G IN.	0.130
MM	3.30
H IN.	0.714
MM	18.14
J IN.	0.314
MM	7.98

DALLAS SEMICONDUCTOR

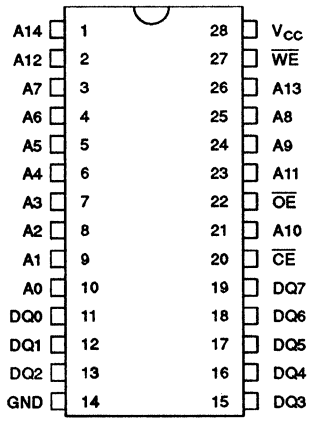
DS2257, DS2257S
32K x 8 3V Operation Static RAM

FEATURES

- Low power CMOS design
- Standby current

  400 nA max at $t_A = 25°C$ $V_{CC} = 3.5V$
  500 nA max at $t_A = 25°C$ $V_{CC} = 5.5V$
  4 µA max at $t_A = 60°C$ $V_{CC} = 5.5V$
  10 µA max at $t_A = 85°C$ $V_{CC} = 5.5V$
- Full operation for V_{CC} = 5.5V to 2.7V
- Data Retention Voltage = 5.5V to 2.0V
- Access time equals 70 ns at 5.0V and 150 ns at 2.7V
- Operating temperature range of -40°C to +85°C
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7 volts.
- Available in 28 pin DIP and 28 pin SOIC packages
- Suitable for both battery operate and battery backup applications

PIN ASSIGNMENT



28 PIN DIP OR 28 PIN SOIC

PIN DESCRIPTION

A0-A14	-	Address Inputs
$\overline{WE}$	-	Write Enable Input
$\overline{OE}$	-	Output Enable Input
$\overline{CE}$	-	Chip Enable Input
DQ0-DQ7	-	Data Input/Output
V_{CC}	-	Power Supply Input 2.7V - 5.5V
GND	-	Ground
NC	-	No Connection

DESCRIPTION

The DS2257 is a 262,144 bit low power, fully static random access memory organized as 32768 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7 volts and 5.5 volts. The chip enable input ($\overline{CE}$) is used for device selection and can be used in order to achieve the minimum standby current mode which facilitates both battery operate and battery backup applications. The device provides fast access time of 70 ns when operated from a 5 volt power supply input, and also provides relatively good performance of 150 ns access while operating from a 3.0 volt input. The device maintains TTL level inputs and outputs over the input voltage range of 2.7 to 5.5 volts. The DS2257 is most suitable for low power applications where battery operation or battery backup for nonvolatility are required.

OPERATION MODE						
MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 - A14	DQ - DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	I_{CCO}
WRITE	L	X	L	STABLE	DATA IN	I_{CCO}
DESELECT	L	H	H	X	HIGH-Z	I_{CCO}
STANDBY	H	X	X	X	HIGH-Z	I_{CCS}

ABSOLUTE MAXIMUM RATINGS		
SYMBOL	PARAMETER	RATING
V_{CC}	Power Supply Voltage	-0.3V to +7.0V
V_{IN}, $V_{I/O}$	Input, Input/Output Voltage	-0.3 to +7.0V
T_{STG}	Storage Temperature	-55°C to +125°C
T_{OPR}	Operating Temperature	-40°C to +85°C
T_{SOLDER}	Soldering Temperature/Time	260°C for 10 seconds

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

+5 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Data Retention Voltage	V_{DR}	2.0		5.5	V	

+5 VOLT OPERATION - CONTINUED

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.4V	-1.0		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.2V		1.0	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=85°C		10	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		4	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		500	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.8V min cycle		60	mA	

AC CHARACTERISTICS (–40°C TO +85°C, V_{CC}=5V ± 10%)					
PARAMETER	SYMBOL	DS2257-70 DS2257S-70		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	70		ns	
Access Time	t_{ACC}		70	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High Z from Deselection	t_{OD}		25	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	70		ns	
Write Pulse Width	t_{WP}	55		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	10		ns	
Output High Z from $\overline{WE}$	t_{ODW}		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	30		ns	4
Data Hold Time	t_{DH}	10		ns	4

+3 VOLT OPERATION

RECOMMENDED DC OPERATING CONDITIONS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.6	V	
Data Retention Voltage	V_{DR}	2.0		3.5	V	

DC CHARACTERISTICS (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$		±0.1	µA	
I/O Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, $0V \le V_{IO} \le V_{CC}$		±0.5	µA	
Output High Current	I_{OH}	V_{OH} = 2.2V	-0.5		mA	
Output Low Current	I_{OL}	V_{OL} = 0.4V	4.0		mA	
Standby Current	I_{CCS1}	$\overline{CE}$ = 2.0V		0.5	mA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$ – 0.3V t_A=85°C		4	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=60°C		1	µA	
Standby Current	I_{CCS2}	$\overline{CE} \ge V_{CC}$-0.3V t_A=25°C		400	nA	
Operating Current	I_{CCO}	$\overline{CE}$=0.6V min cycle		40	mA	

AC CHARACTERISTICS READ CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	
Access Time	t_{ACC}			150	ns	
$\overline{OE}$ to Output Valid	t_{OE}			75	ns	
$\overline{CE}$ to Output Valid	t_{CO}			150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5			ns	
Output High-Z from Deselection	t_{OD}			75	ns	
Output Hold from Address Change	t_{OH}	15			ns	

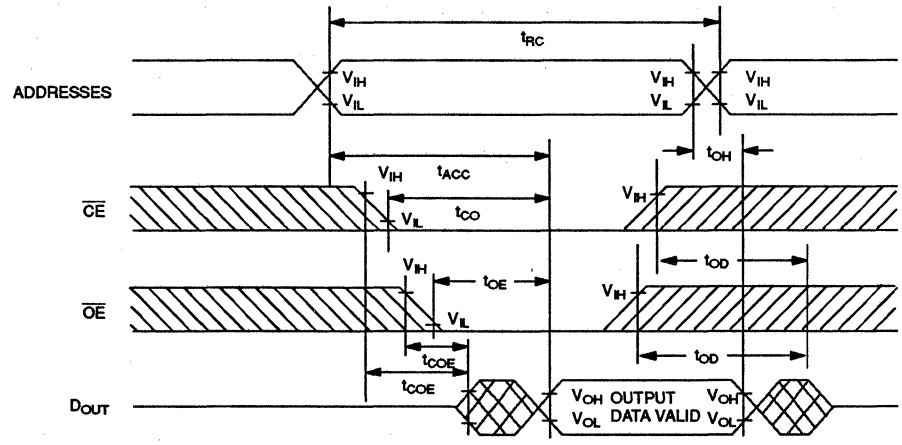
+3 VOLT OPERATION - CONTINUED

AC CHARACTERISTICS WRITE CYCLE (t_A = -40°C TO +85°C, V_{CC} = 2.7V TO 3.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	120			ns	
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	25			ns	
Output High-Z from $\overline{WE}$	t_{ODW}			75	ns	
Output Active from $\overline{WE}$	t_{OEW}	5			ns	
Data Setup Time	t_{DS}	100			ns	
Data Hold Time	t_{DH}	25			ns	

DATA RETENTION CHARACTERISTICS (t_A = -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Supply Voltage	V_{DR}	2.0		5.5	V	
Data Retention Current at 5.5V	I_{CCR1}		0.1*	10	µA	
Data Retention Current at 3.5V	I_{CCR1}		0.5	4	µA	
Data Retention Current at 2.0V	I_{CCR2}		50*	2000	nA	
Chip Deselect to Data Retention	t_{CDR}	0			µA	
Recovery Time	t_R	5			ms	

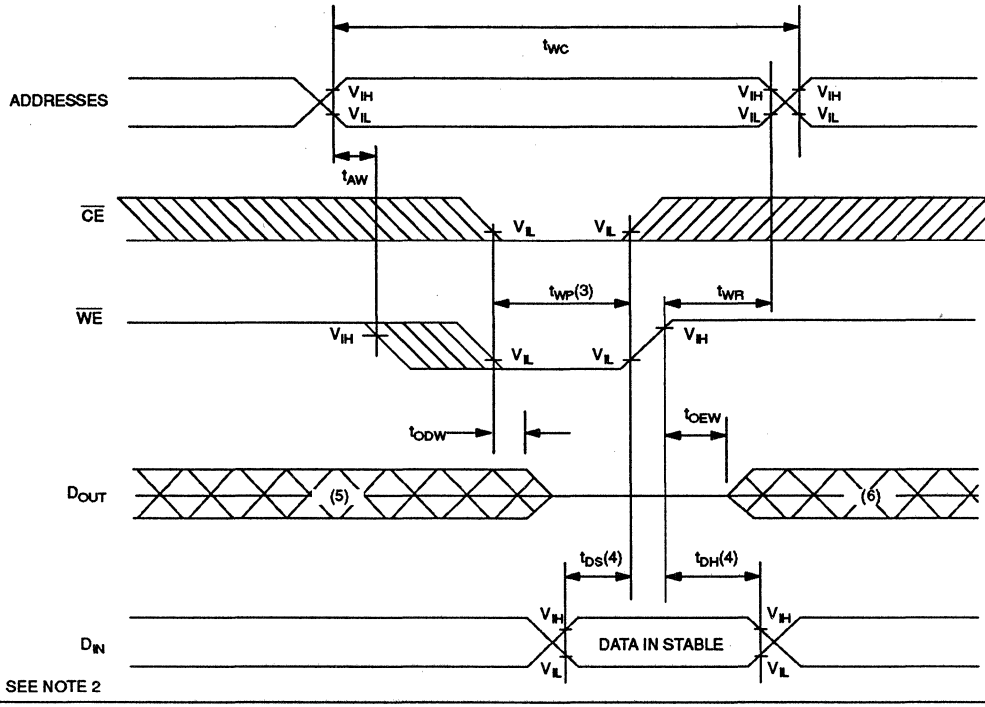
* Typical values are at 25°C

TIMING WAVEFORM: READ CYCLE



SEE NOTE 1

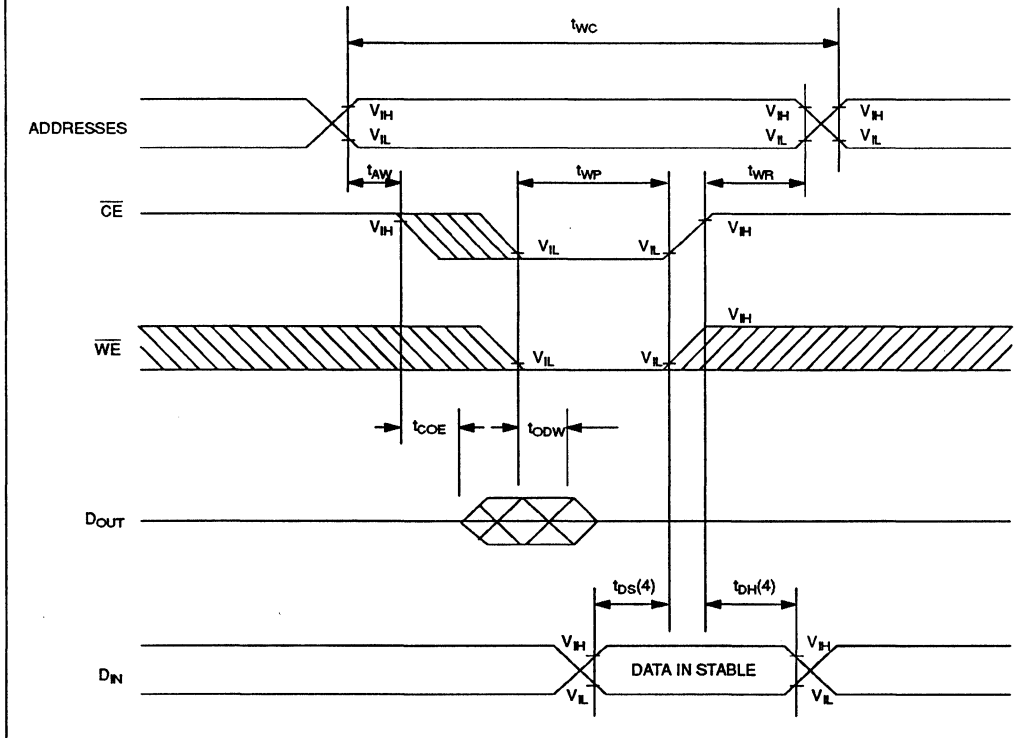
TIMING WAVEFORM: WRITE CYCLE 1



SEE NOTE 2

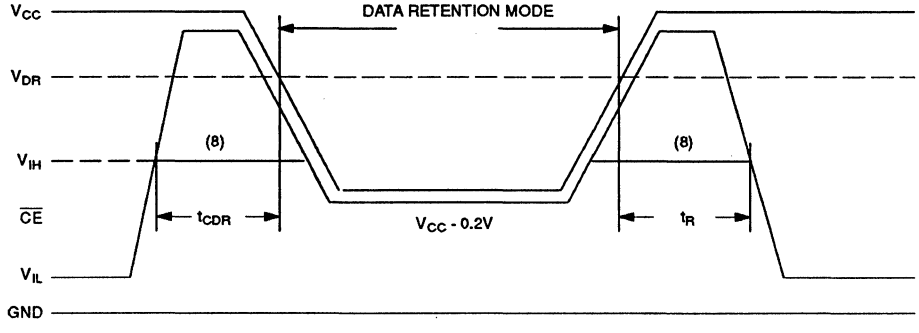
: UNKNOWN

TIMING WAVEFORM: WRITE CYCLE 2



: UNKNOWN

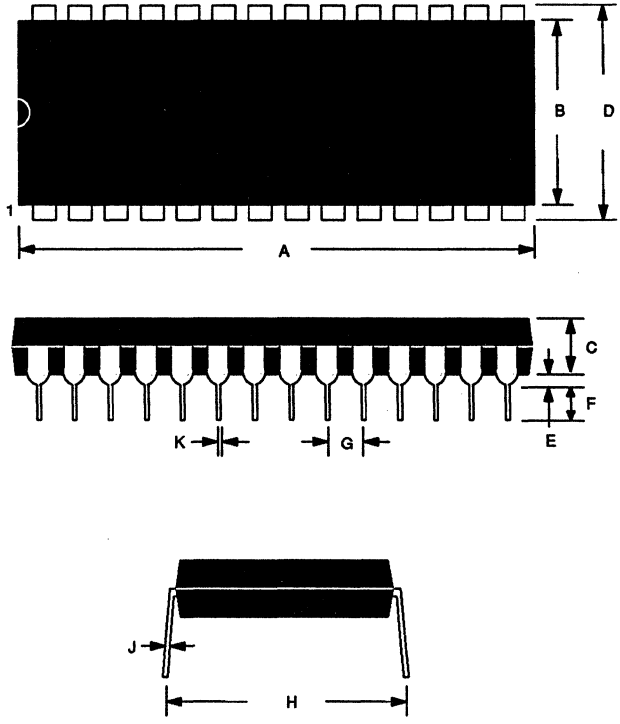
FIGURE 1: TIMING DIAGRAM: DATA RETENTION - POWER UP, POWER DOWN



NOTES

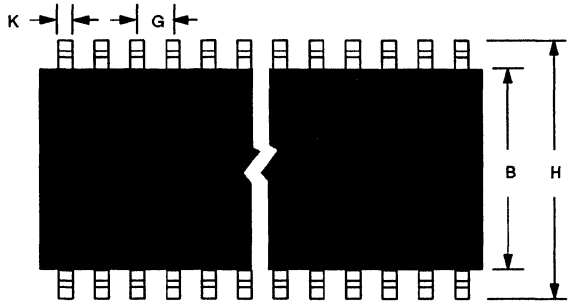
1. WE is high for read cycles.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH} and t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition in write cycle 1, the output buffers remain in a high impedance state.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in write cycle 1, the output buffers remain in a high impedance state.
7. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state.
8. If the V_{IH} level of $\overline{CE}$ is 2.0V during the period that V_{CC} voltage is going down from 4.5V to 2.7V I_{CCS1} current flows.

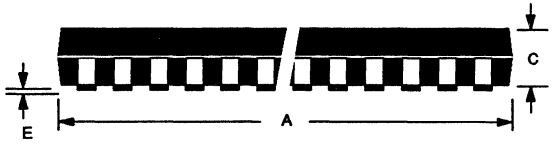
DS2257 28 PIN DIP

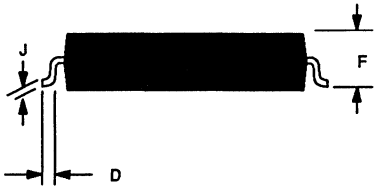


PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.440	1.460
MM	30.99	32.00
B IN.	0.530	0.550
MM	13.46	13.87
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.045
MM	0.380	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS2257S 28 PIN SOIC







PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	0.696	0.713
MM	17.7	18.1
B IN.	0.326	0.335
MM	8.3	8.5
C IN.	0.092	0.104
MM	2.35	2.65
D IN.	0.039 TYP	
MM	1.0 TYP	
E IN.	0.004	0.012
MM	0.100	0.300
F IN.	0.106 TYP	
MM	2.7 TYP	
G IN.	0.044	0.056
MM	1.118	1.422
H IN.	0.453	0.477
MM	11.5	12.1
J IN.	0.004	0.008
MM	0.10	0.20
K IN.	0.012	0.020
MM	0.300	0.500

4

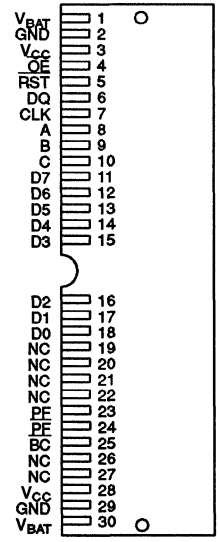
DALLAS SEMICONDUCTOR

DS2262
MegaStore Stik

FEATURES

- Solid-state mass storage subsystem using nonvolatile DRAM
- Versions with 4 and 8 megabits available
- DRAM timing and refresh control performed transparently to host
- Nonvolatile data retention using an external 6-9 volt backup supply
- Low-power data retention mode consumes less that 3 mA (4 megabit version)
- Backup supply can be switched off under host software control for conserving energy
- 3-wire serial port can access DRAM data at up to 1 megabit/second in burst mode
- Unique backup supply gas gauge continuously reports battery condition
- Power fail detect write-protects memory at either 5% or 10% of 5 volt main supply
- Mates with JEDEC-standard 30 pin SIMM edge connectors (right angle and vertical)

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CC}	-	+5V Power Supply
V_{BAT}	-	Battery Supply
$\overline{OE}$	-	Option Enable
$\overline{RST}$	-	Reset
DQ	-	Serial Port Data I/O
CLK	-	Clock
A, B, C	-	DRAM Select
D7-D0	-	DRAM 0-7 Data Outputs
PF, $\overline{PF}$	-	Power Fail Outputs
$\overline{BC}$	-	Battery Condition Output
GND	-	Ground

DESCRIPTION

The DS2262 MegaStore Stik is an extremely compact solid-state mass storage device that provides up to 8 megabits of nonvolatile DRAM for data storage. The DRAM and internal control functions are accessed using a 3-wire serial interface (CLK, D/Q, $\overline{RST}$) which can hook directly to the serial port of popular microprocessor/microcontroller devices such as the DS5000T/2250T Time Microcontroller family. All necessary DRAM timing and refresh duties are performed automatically.

An external backup supply such as a 6-volt battery can be attached to enable DRAM data retention, creating in effect a solid state disk drive. An internal circuit monitors the main +5V supply. Upon its failure, the DRAM is write-protected and the backup supply switched on.

With an inexpensive 1300 mA/Hr lithium battery, a DS2262 with 4 megabits can provide up to 3 weeks of continuous nonvolatile operation. If the failure of the main supply is relatively infrequent, the DS2262 can extend its nonvolatile operation for years, especially if the backup source is a rechargeable battery. A unique gas gauge circuit continuously monitors and reports the backup supply condition, warning the host of impending battery failure.

OPERATION - $\overline{OE}$ (PIN 4) HIGH

The main elements of the DS2262 are shown in Figure 1. Six signals control sending or retrieval of data using the address converter circuit. The signals CLK, $\overline{RST}$, and DQ comprise the DS2262 serial port. The signals A, B, and C control which DRAM data is written to. To transfer data into the DS2262, $\overline{RST}$ is first driven high while CLK is low. After sufficient setup time from $\overline{RST}$, one bit of data is placed onto the DQ line. With valid data on DQ, the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred to the DS2262. If data is to be written to or read from one of the DRAMs, that DRAM must be selected on the A, B, and C pins when $\overline{RST}$ is brought high, and must remain selected until $\overline{RST}$ is brought low again to reset the serial port (see Table 2).

Information is written to the serial port in the form of a 24 bit address field followed by an 8 bit function code. 24 address bits are required regardless of the density of Stick used. Function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from a DRAM or the control registers. Data is read from the control registers by driving CLK low while $\overline{RST}$ is high. Data becomes valid on the DQ line after sufficient time is allowed for access. Reading from a DRAM selected by the A, B and C pins will place the correct data on the corresponding data line (D0-D7) after time is allowed for access, as well as on the DQ line. A read cycle is terminated when $\overline{RST}$ is returned low.

OPERATION - $\overline{OE}$ (PIN 4) LOW

When the $\overline{OE}$ pin is tied low, the A, B and C pins are replaced with a serial interface controlled by $\overline{RST}$, CLK, and DQ. To load the DRAM to be written, the $\overline{RST}$ pin is brought low and the DRAM select signals are clocked in, in the order C, B then A on DQ on the rising edge of the CLK pin. $\overline{RST}$ is then brought high to enable the entry of addresses and function codes into the control registers as described above. When the DS2262 is to be used with the $\overline{OE}$ pin low, the A, B and C pins should be left unconnected.

BURST MODE

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. Burst mode is terminated when $\overline{RST}$ is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt V_{CCI} power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V_{CCI} falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF,$\overline{PF}$) are driven active at this time and will remain active until V_{CCI} is restored to a normal condition. When the data retention mode begins, the DS2262 isolates the 3-wire serial port. If an active DRAM read/write cycle is in progress when power loss occurs, the DS2262 will complete this cycle properly before isolating the 3-wire serial port ($\overline{RST}$, CLK, D/Q). The V_{CCI} input is then disconnected from the V_{CCO} output and the backup supply connected to the V_{BAT} pin is switched in. The V_{BAT} input is normally connected to either a rechargeable battery or super capacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be tied to the V_{CCI} pin; do not tie this pin low when not using the battery-backup function.

BATTERY GAS GAUGE

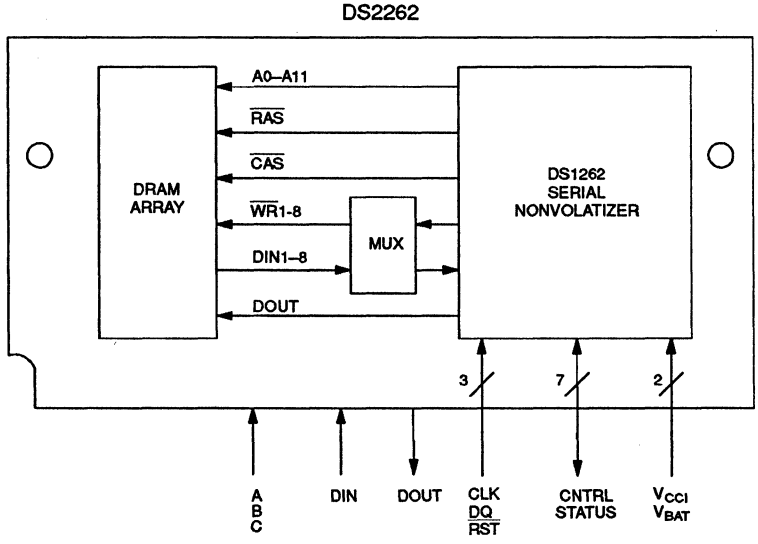
The DS2262 contains two features that provide information about the condition of the backup supply. First, the DS2262 monitors the backup supply input condition. If this input is below V_{CCI} the backup condition output pin ($\overline{BC}$) is driven active low and remains in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is providing power, the $\overline{BC}$ pin remains in a high impedance state.

The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while V_{CCI} is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field, followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field followed by the correct function code. Information in the address field is automatically entered into the battery condition counter when $\overline{RST}$ is brought low to end the

cycle. The battery condition counter value can only be entered when V_{CCI} is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V_{CCI} is within normal limits. No other action will take place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply will be discharged. When the counter reaches zero, the $\overline{BC}$ pin will be driven low as soon as V_{CCI} is within normal limits. The $\overline{BC}$ pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

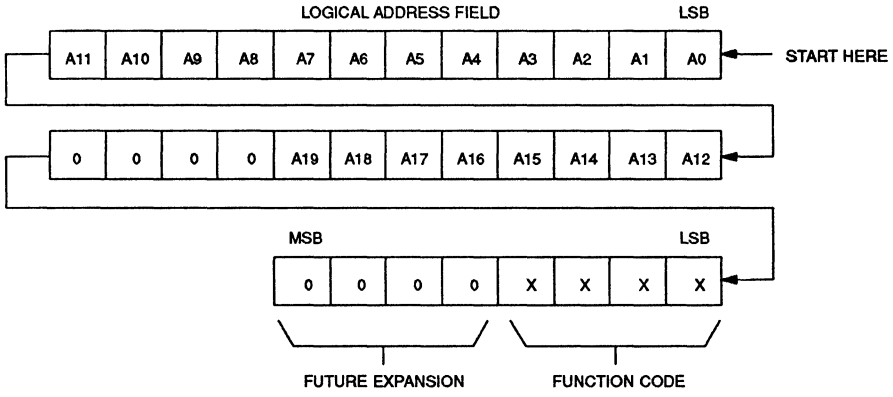
FUNCTIONAL DIAGRAM Figure 1



DRAM SELECTION Table 1

INPUTS			DRAM SELECTED
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

SERIAL PORT PROTOCOL Figure 2



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FUNCTION CODES Table 2

FUNCTION NAME	FUNCTION CODE (HEX)
BURST READ DRAM DATA READ DRAM DATA	00 01
READ BKUP COUNTER WRITE BKUP COUNTER	02 03
BACKUP SUPPLY ENABLED BACKUP SUPPLY DISABLED	0C 0D
WRITE DRAM DATA BURST WRITE DRAM DATA	0E 0F, FF

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
VOLTAGE ON BKUP PIN RELATIVE TO GROUND	-0.3V TO +12V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-55°C TO 125°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Input Logic High	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic Low	V_{IL}	-0.3		+0.8	V	1
Backup Supply	V_{BAT}	5.5	8.0	10.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	
DQ Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Input Supply Current	I_{CCI}		3.0	7.0	mA	
TOL Pin = V_{CCO}	V_{TP}	4.50	4.62	4.75	V	
TOL Pin = GND	T_{TP}	4.25	4.37	4.50	V	
Backup Supply Leakage	I_{BKUPL}		2	4	µA	
Backup Supply Quiescent	I_{BKUPQ}		2.0		MA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C	5	7	pF	
Output Capacitance	C_{OUT}	t_A=25°C	7	10	pF	
I/O Capacitance	$C_{I/O}$	t_A=25°C	7	10	pF	

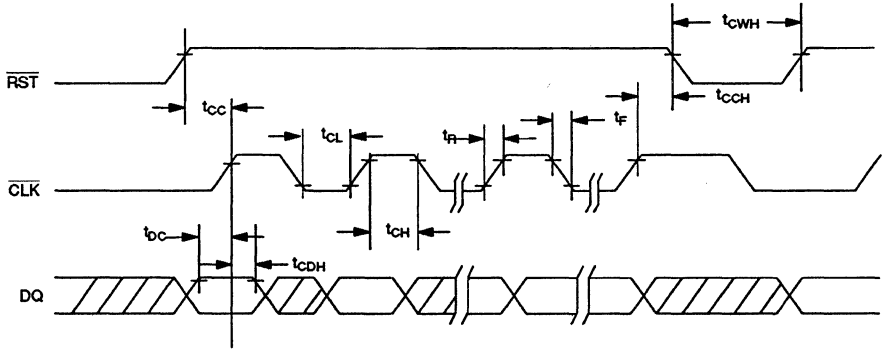
AC ELECTRICAL CHARACTERISTICS

(t_A=25°C, V_{CC}=5V ± 5%)

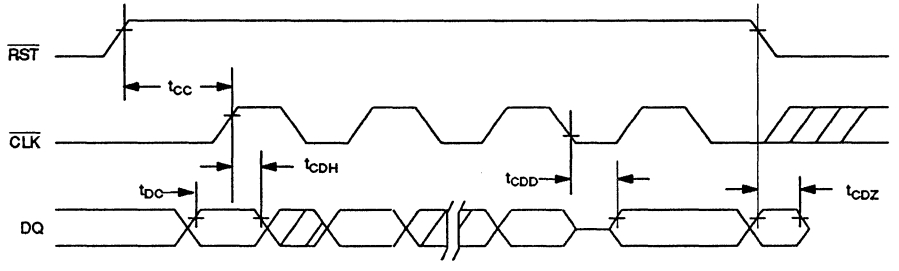
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DQ to CLK Setup	t_{DC}	100			ns	
CLK to DQ Delay	t_{CDD}			200	ns	
CLK Low Time	t_{CL}	500			ns	
CLK High Time	t_{CH}	500			ns	
CLK Frequency	t_{CLK}	DC		1	MHz	
CLK Rise and Fall	t_R, t_F	3	10	20	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	
CLK to $\overline{RST}$ Hold	t_{CCH}	200			ns	
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	
$\overline{RST}$ to DQ in High Z	t_{CDZ}			100	ns	

4

WRITE DATA TRANSFER FROM SERIAL PORT



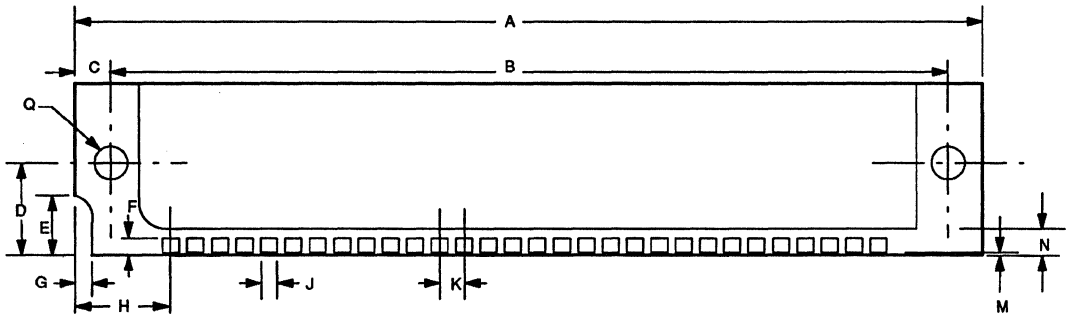
READ DATA TRANSFER FROM SERIAL PORT

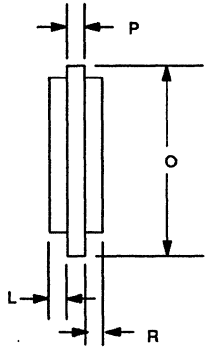


NOTES

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CCI} is within nominal limits and the backup supply is below V_{CCI}.
3. Load capacity is 100 pF.
4. Measured with all outputs open, $V_{CCI} = V_{IH} = 5.5$ V.
5. V_{TP} is the trip point where the internal switching circuits disconnects V_{CCI} and connects the internally regulated backup supply to the DRAMs.
6. Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS2262 is in the data retention mode (V_{CCI}=0V).
7. Backup quiescent current is the current consumed by the DS2262 when in the data retention mode and the backup supply is enabled. Total current into the V_{BAT} pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

DS2262 MEGASTORE STIK



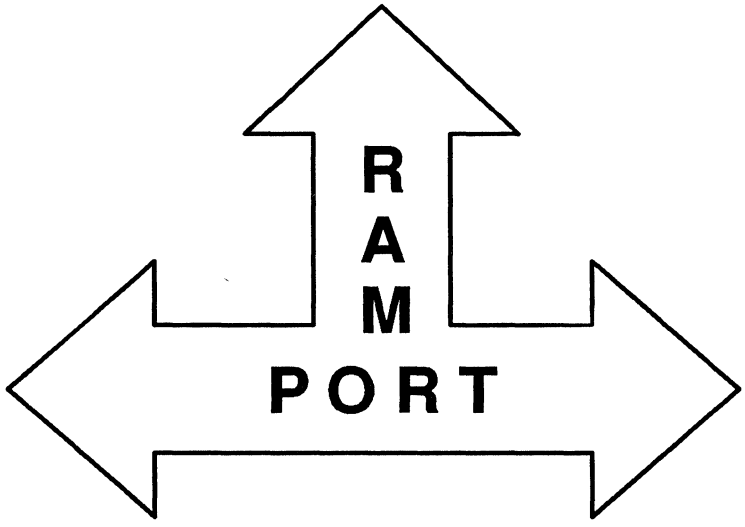


DIM	INCHES MIN
A	3.500
B	3.234
C	.0.133
D	.0.400
E	0.250
F	0.070 MIN.
G	.0.080
H	0.300
J	0.070
K	.0.100
L	.0.185 MAX.
M	.0.010 MAX.
N	0.100 MIN.
O	0.855 MAX.
P	0.054 MAX.
Q	0.125
R	0.185 MAX.

DALLAS
SEMICONDUCTOR

RAMport
Application Note – 61

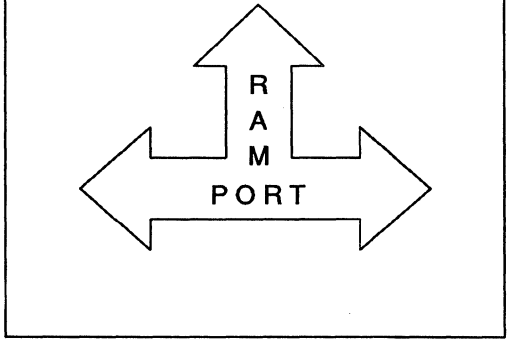
4



RAMport – 2K X 8 NV SRAM AND MORE

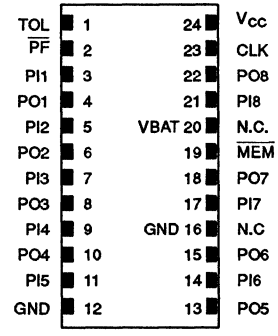
The RAMport memory developed by Dallas Semiconductor was designed to be connected to microcontrollers without robbing the device of valuable port pins. The name "RAMport" was chosen for the DS1381 to try to communicate this advantage to potential users (see Figure 1). Even if the name is effective in conveying this message, the overall capability of the device and the diversity of applications remains concealed.

FIGURE 1: DS1381



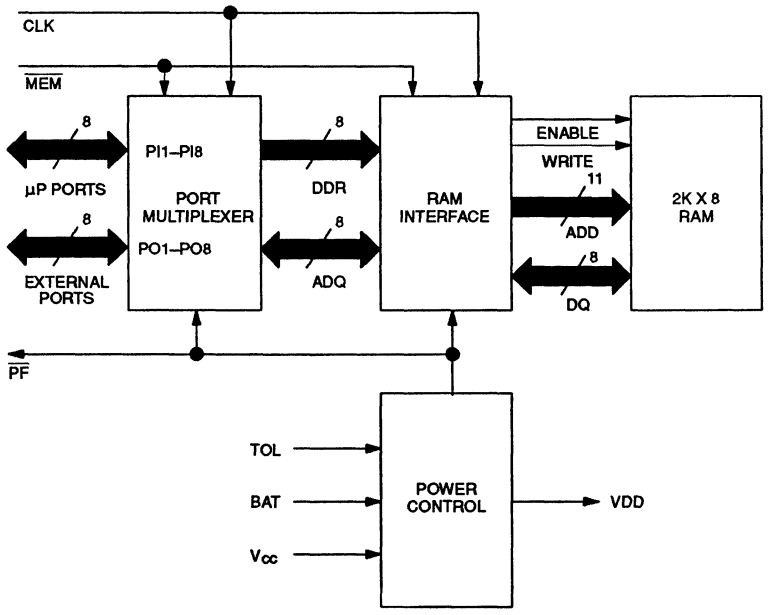
The DS1381 RAMport is a byte organized memory that uses a multiplexed address and data bus. The obvious disadvantage with this scheme is reduced performance because the address and data bits are sent in a serial time sequence. The equally obvious advantage is reduced pin count (see Figure 2). The multiplexing scheme used with the DS1381 requires only 8 pins for address and data. The address is transferred to the device in two subsequent cycles. First the high order byte is transferred which consist of A8 through A10 along with read or write command information. The second address transfer contains the low order address followed by a third transfer which is data. Since the read or write command is transferred as part of the address, the need for read and write control signals is also eliminated reducing control signal requirements to only two pins; memory and clock. The memory and clock controls direct data transfer to and from the memory and also command and control eight port input/outputs which are not found on conventional memories (see Figure 3). The total pin count for memories interface and port input/output plus V_{CC} and ground amounts to 20 pins. This leaves four pins for the special purpose of providing nonvolatility. Two pins provide for a direct connection to a data retention energy cell. These pins do not go outside the package, but are internally connected to a button style energy cell. Since this connection is made with 2 of the 24 pins on a standard dual in line package, cost savings is achieved when compared to alternate interconnect systems or special lead frames. Finally, the DS1381 provides an output when power fail occurs which can be used to interrupt the processor and a separate pin provides selection of the power fail detection point at 5% or 10% of the power supply voltage. The end result is a low cost 24 pin 0.6" DIP that is common with most standard 2K X 8 static RAMs which offers an I/O port and a power fail controller as a bonus.

FIGURE 2: DS1381 PIN INFORMATION



PIN NAME	DESCRIPTION
$\overline{PF}$	POWER FAIL OUTPUT
PI1–PI8	PORT INPUTS (µP PORTS)
PO1–PO8	PORT OUTPUTS (EXTERNAL PORTS)
GND	GROUND
V_{CC}	+5 VOLTS
CLK	CLOCK
$\overline{MEM}$	MEMORY SELECT
N.C.	NO CONNECTION

FIGURE 3: DS1381 FUNCTIONAL BLOCK DIAGRAM



REDUCING TO PRACTICAL – MICROCONTROLLER INTERFACE

As mentioned, the DS1381 was designed to offer the microcontroller user some external nonvolatile memory that does not consume all of the valuable port pins. When using the DS1381 with a microcontroller, the interconnect system is simple and straight forward. Eight port pins of the microcontroller connect directly to the eight input port pins (PI1 – PI8) of the DS1381 (see Figure 3). These port pins are reproduced at the port output pins (PO1 – PO8). During operation when no memory transfer is taking place, the DS1381 port output pins look exactly like the eight microprocessor port pins with the only addition of a small series impedance. Two other port pins of the microprocessor are required to control the DS1381; namely CLOCK and $\overline{\text{MEMORY}}$. Since these port pins must be dedicated to control, they are not reproduced the the DS1381. The $\overline{\text{MEMORY}}$ and CLOCK signals must be generated using software within the microcontroller to establish the proper signal levels and timing relationships. The function of these two controls is to direct data to and from memory or to the data direction register within the DS1381. When data is being transferred to and from the DS1381, the port outputs are latched or become high impedance depending on their assigned function. More detailed information on the control signals is furnished in the DS1381 data sheet.

MICROPROCESSOR INTERFACE USING DS1381 MEMORY

While the hardware interface between the DS1381 and a microcontroller is straight forward, the interface to a microprocessor is also simple although not as obvious. However, only the 2K X 8 nonvolatile memory and power fail controller features are useful in this application (see Figure 5). The key to interfacing the DS1381 to a microprocessor is to use only the data bus for both address and data. Since only the memory is to be used, the $\overline{\text{MEMORY}}$ signal should be grounded. This connection fixes the PO1 – PO8 pins to remain in a status as dictated by the data bus and the DS1381 data direction register at the time that the $\overline{\text{MEMORY}}$ signal is grounded. Because it is difficult and unlikely that these pins contain any useful information under this condition (although some type of programming mode might be implemented to make these outputs useful) these pins should be left as no connections. With the $\overline{\text{MEMORY}}$ pin grounded, the clock input becomes analogous to the chip enable or chip select on a standard bytewide memory. The clock signal can be easily derived with a decoder from selected address lines which place the DS1381 properly in the memory map. To achieve proper timing (setup and hold times) the decode must be gated by a microprocessor control signal. The names and purpose of usable control signals vary with the type of microprocessor used. However, status signals, ad-

dress latch enable, memory request, address strobe, and data strobe usually provide the proper timing relationship with respect to address and data for gating the decoder. The microprocessor and DS1381 data sheets should be consulted for exact timing details. Since only the data bus is used for both address and data, three separate memory cycles must be used to read or write each byte of data. However, this inconvenience is often a small price to pay for hiding a 2K X 8 of nonvolatile RAM in as small as one I/O or memory address space. An additional feature that standard memory does not provide is the power fail interrupt output.

IN CONCLUSION

The DS1381 is primarily tailored for use with microcontrollers. In microcontroller applications, the DS1381 provides an inexpensive nonvolatile RAM without using valuable port pins. In microprocessor applications, 2K X 8 of nonvolatile RAM is easily interfaced to a system with minimum impact on memory space by using the data bus for both address and data. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while additional and useful features are provided which are not found on standard memories. While the multiple uses of the RAMport are difficult to convey to potential users with only a name; closer inspection of the device reveals an economical special purpose nonvolatile memory with many microprocessor and microcontroller applications.

FIGURE 4: MICROCONTROLLER INTERFACE

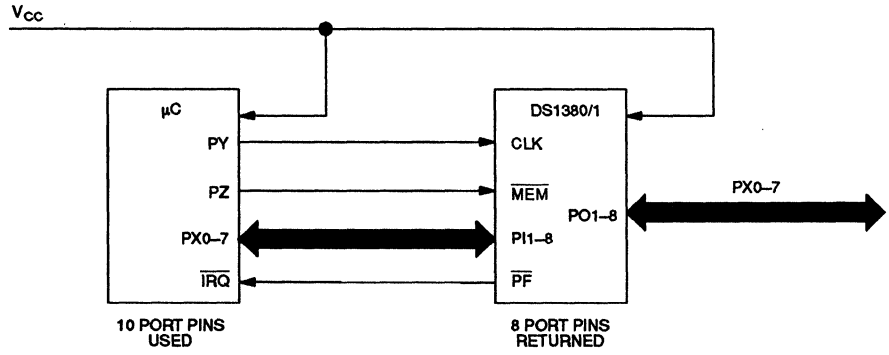
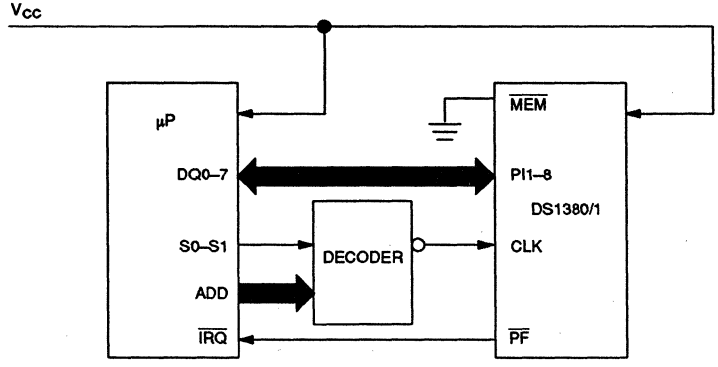


FIGURE 5: MICROCONTROLLER INTERFACE USING DS1380 2K X 8 NV RAM ONLY



DALLAS SEMICONDUCTOR

Using Nonvolatile Static RAMs
Application Note – 63

Vast resources have been expended by the semiconductor industry trying to build a nonvolatile random access read/write memory. The effort has been undertaken because nonvolatile RAM offers several advantages over other memory devices – DRAM, Static RAM, Shadow RAM, EEPROM, EPROM and ROM – which were developed to meet specific applications needs.

Characteristics of the ideal nonvolatile RAM are: low power consumption, higher performance, greater reliability, higher density, low cost, and the ability to be used in any semiconductor memory application.

While the various memory components designed to date do not meet the ideal memory scenario, each excels in meeting one or more of the sought after attributes (Figure 1).

FIGURE 1: MEMORY ATTRIBUTES

	COST	EASE OF INTERFACE	NONVOLATILE	DENSITY	PERFORMANCE	READ/WRITE	DATA RETENTION
DRAM	+++			+++	++	+++	
STATIC RAM		+++		+	+++	+++	
NV SRAM		+++	++	+	+++	+++	++
PARTITIONABLE NV SRAM		+++	++	+	+++	+++	++
PSEUDO STATIC	+	+		++	+	+++	
FLASH	++	++	++	+	++	+	++
EEPROM	+	++	+	+		+	+
EPROM	++	++	++	++	+		++
OTP EPROM	+++	+++	+++	+++	+		+++
ROM	+++	+++	+++	+++	+		+++

+ = Degree of excellence

TYPES OF MEMORY

Many types of memories have been devised to meet varying application needs. However, nonvolatile read/write random access memories can be substituted for all memory types independent of application, if cost is not a primary consideration.

DRAM: Dynamic Random Access Memory. A DRAM, similar to an SRAM, stores information as a 1 or a 0. In an SRAM, this information is stored in a four to six transistor flip–flop which is easy to address, but requires a relatively large memory cell. A DRAM, by comparison, stores its 1 or 0 as a charge on a small capacitor, requiring much more current then an SRAM to maintain the stored data. The net memory cell size is smaller for the DRAM than for the SRAM, so the total cost per bit of memory is less. The DRAM's capacitors must be constantly refreshed so that they retain their charge, and require more sophisticated interface circuitry.

SRAM: Static Random Access Memory. An SRAM is essentially a stable DC flip–flop requiring no clock timing or refreshing. The contents of an SRAM type memory are retained so long as power is supplied, and support extremely fast access times. SRAMs also have relatively few strict timing requirements and a parallel address structure, making them particularly suited for cache and other low density, frequent access applications.

NV SRAM: An NV SRAM is a single package which contains a low current SRAM, a memory controller capable of measuring voltage, and a lithium type battery. When the power supply to this single modular package falls below the minimum requirement to maintain the contents of the SRAM, the memory controller in the module switches the power supply from the external source to the internal lithium battery, and write protects the SRAM. These transitions to and from the external power source are transparent to the SRAM, transforming it into a true non–volatile memory. This unique construction combines the strategic advantages of SRAM–addressing structure, high speed access, and timing requirements, with the non–volatility advantages of EEPROM technologies. Battery backed SRAM modules from Dallas Semiconductor are pin–to–pin compatible with non battery backed SRAMs, making them ideal for any application where a traditional SRAM would be suitable.

PARTITIONABLE NV SRAM: A partitionable Dallas Semiconductor NV SRAM offers the same nonvolatility, addressing structure, and timing requirements of a reg-

ular Dallas Semiconductor NV SRAM product with the additional feature of the ability to write protect selected blocks of memory, regardless of V_{CC}.

The write protection feature requires no additional pins, and is instead controlled by a unique combination of addressing and read cycles (see DS1630 and DS1645 data sheets). This feature allows a designer to use a battery backed SRAM as both a RAM and a ROM – in one device. Because no additional pins are required for control, partitionable devices can be substituted for non–partitionables in existing designs, without making costly hardware changes.

PSEUDO STATIC RAM: Pseudo Static Random Access Memory. The advantages of using a Static Ram are the simplicity of the interface circuitry required, and the fact that the device is by nature "static", not requiring periodic refreshing to retain its data. A DRAM, however, provides lower cost per bit advantages and a higher memory density. A Pseudo static RAM combines the advantages of the SRAM and DRAM by using dynamic storage cells to retain memory, and by placing all the required refresh logic on–chip so that the device functions similarly to an SRAM.

FLASH: A flash memory combines the electrical erase capability of the EEPROM in a cell that is similar to an EPROM. The result is that the modified cell may be block erased electrically instead of with UV light. This feature allows a Flash memory to accept new code updates or information while it is functioning in a system.

EEPROM: Electrically Erasable/Programmable Read Only Memory. A significant disadvantage of the EPROM is the fact that it cannot be reprogrammed while in a circuit. The EPROM requires the external programming device to receive new code or data. An EEPROM eliminates this problem by providing a write function which can be used while the EEPROM is still in a circuit. A penalty of obtaining the write function while the EEPROM is still in a circuit is having to provide a high voltage (12.5V or above) source for the EEPROM to source when accepting new code, or buying a more expensive EEPROM which has a charge pump in its package that allows the EEPROM to be used with a standard 5–>7V input. Although nonvolatile, EEPROM memory cells exhibit slow read/write access rates, making them most suitable for systems where performance is not an issue. The other read/write capable memories listed in Figure 1 provide the ability to frequently read and write data continuously over their entire lifetimes, in excess of 10 years, while EEPROM memory cells can rarely be rewritten more than 10,000 times—you could wear out the EEPROM memory in less than a second! An EEPROM can be placed in a system and accessed as a standard RAM.

EPROM: Electrically Programmable Read Only Memory. An EPROM is a nonvolatile memory source which offers flexibility to both program and erase the contents of the memory multiple times. An EPROM must be programmed using a 12.5 voltage or above PROM programmer, and then transferred into the system in which it is intended to function. EPROMs can be erased by shining ultraviolet light into the window in the top of the IC package. The process of writing data into an EPROM and then erasing it may be repeated almost indefinitely. EPROMs are usually used for product development, and later replaced with less expensive one–time programmable EPROMS.

OTP EPROM: One Time Programmable EPROM. An EPROM which can only be written with code/data once instead of multiple times. Generally, OTP EPROMs are less expensive then erasable EPROMs.

ROM: Mask Programmable Read Only Memory. Mask programmable ROM's are the most durable form of memory storage. They are, however, "read only" and offer fairly slow performance. If a design has code/data that is very stable and will not need to be changed, a custom mask for the IC die can be made which will significantly reduce the cost of the ROM. A drawback to using a masked ROM is the significant cost penalty that must be incurred if an error in the code/data being stored forces a mask set change. The OTP EPROM fills the gap between ROM applications (no changes) and EPROMs (frequent changes).

MEETING APPLICATIONS NEEDS

NMOS DRAM memory provides performance and density, but, on the down side, must be constantly refreshed to retain data. At the opposite extreme are ROMs, offering nonvolatility and density, but lacking the ability to be updated with new data because information is burned in only once. Between these two are a wide range of devices that fulfill some characteristics of the ideal memory.

Two popular devices, EEPROMs and Shadow RAMs, are designed to emulate a static RAM but also have the ability to retain data after a power loss. But despite their capability to retain data, both EEPROMs and Shadow RAMs fall short of meeting the industry's needs for several reasons.

Most notably, the EEPROM requires a special slow write cycle. The EEPROM's inability to support standard write cycle hinders performance in applications where memory is updated immediately as new data is available.

Another problem with EEPROMs is their wear out mechanisms. These raise reliability concerns due to the limited number of write cycles allowed – sometimes as few as 10,000. If a static RAM with a 200 ns cycle time had this limitation, it would wear out in a mere 20 ms. An application that requires constant updating, such as the buffer memory of a cashier's checkout terminal or a printer, the EEPROM's wear out mechanism is not acceptable.

Finally, because of the complexity of programming circuits, the cell structure and the special process technology required, the density of EEPROMs has not kept up with industry demands.

In systems requiring store–and–forward data, the nonvolatile RAM must provide the desired fast write cycle as well as protection of memory in the event of a power loss. Despite the promise of such a memory device and the effort invested by the industry, the ideal nonvolatile RAM remains elusive.

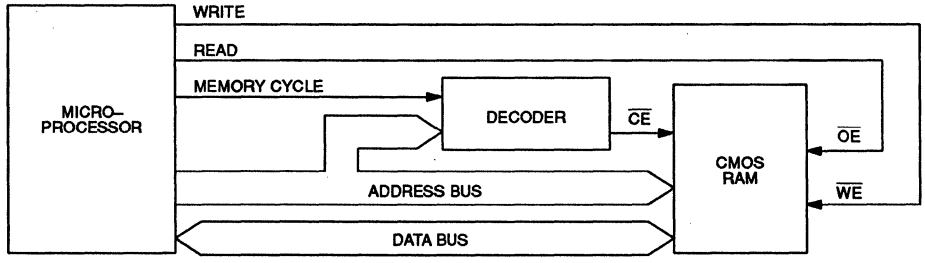
To more nearly emulate the ideal nonvolatile RAM, Dallas Semiconductor combines its intelligent CMOS control circuitry (DS1210), a lithium energy source, and a very low power SRAM to offer a high density, nonvolatile memory.

Four devices, the DS1220 (2K x 8 bits), DS1225 (8K x 8 bits), DS1230 (32K x 8 bits), and DS1245 (128K x 8 bits), use this fusion of technologies to provide a nonvolatile random access memory solution at a density of up to 1024K bits.

CMOS static RAMs currently available have read and write cycle times of under 100 ns, which exceed most system requirements. This alleviates the problem of the EEPROM, because there is no wear–out mechanism or write cycle limitation.

Static RAMs are also the easiest to use and interface because the pinout configurations are standard throughout the industry. In fact, X8 or bytewide static RAMs can be interfaced directly to microprocessors (Figure 2). In addition, CMOS static RAMs offer low power in both active and standby modes, a characteristic sought by many designers. In most designs, RAMs remain in standby much of the time, keeping power consumption negligible. In the standby mode, current drain consists only of leakage currents in the tens of nanoamperes.

FIGURE 2: BYTEWIDE RAM TO MICROPROCESSOR INTERFACE



BYTEWIDE MEMORIES PROVIDE EASY INTERFACE TO MICROPROCESSORS BECAUSE OF THE X8 ORGANIZATION AND CONTROL SIGNAL DEFINITION.

PUTTING LITHIUM AND RAM TOGETHER

The minute leakage current of CMOS RAMs can be sustained with a backup energy source to yield a most attractive nonvolatile memory. However, the actual solution involves more than just a CMOS memory and back up energy source (see Figure 3).

Battery backup design schemes are many and varied. The increase in density and availability of low powered CMOS memories in recent years has made this approach even more attractive. Yet problems still exist with battery backup design due to battery packaging and a lack of the appropriate standard components to implement the support circuitry. One problem is providing isolation between the battery and power supply (see Figure 4). Diodes can provide isolation but produce a voltage drop which requires nonstandard power supplies and also subtracts from the battery voltage. A second problem is the circuitry must be powered from the battery. Unless these devices draw an extremely modest amount of current, battery selection changes drastically. In fact, a current drain of even a couple of microamperes dictates the use of either rechargeable batteries or a replaceable battery scheme. If rechargeable batteries are selected, the recharging circuit can be costly and complex and the best rechargeable battery cannot compare with the electrochemical stability of the lithium primary cell. Even worse, replaceable batteries add maintenance and cost to an in–service system. Battery packaging has also been a serious limitation, taking up valuable space and requiring special handling consideration to prevent discharge.

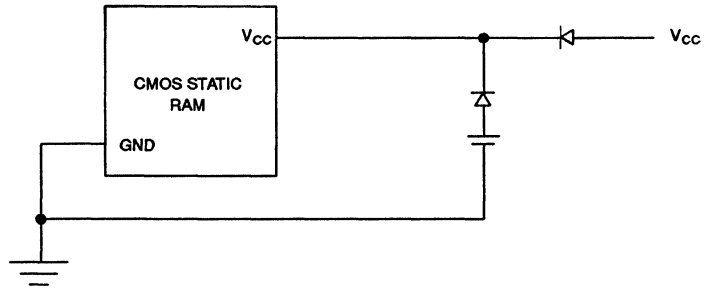
Dallas Semiconductor overcomes these obstacles by using high capacity, non–rechargeable lithium batteries in its battery backed SRAMs.

4

ENERGY SOURCE

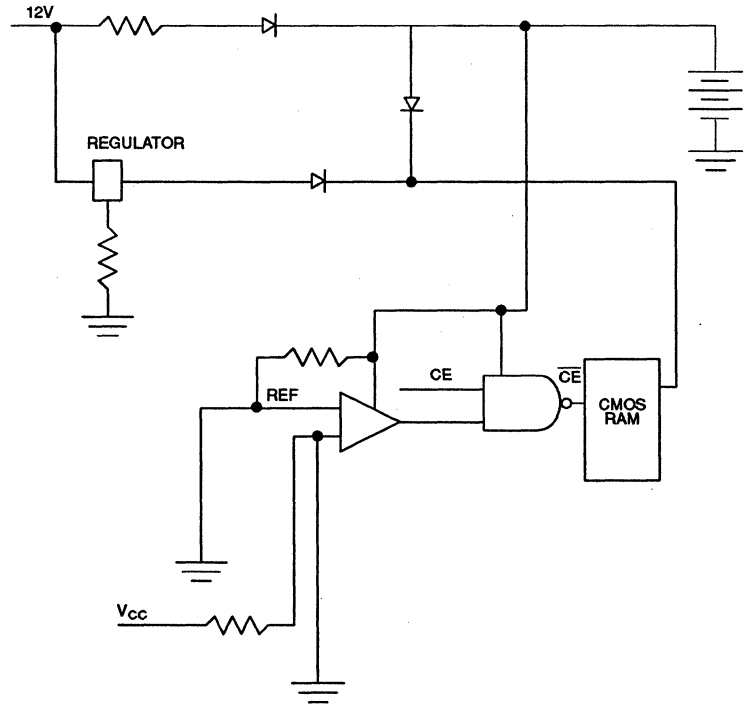
The energy source used to retain data in memory must be capable of outlasting the usefulness of the end product. Dallas Semiconductor NV RAM products use an extremely stable electrochemical system with enough energy to guarantee a shelf life greater than 10 years.

FIGURE 3: BATTERY BACKUP CIRCUIT



CMOS STATIC RAM REQUIRES MORE THAN JUST A BACKUP POWER SUPPLY. DATA MUST ALSO BE PROTECTED DURING POWER TRANSIENTS TO AVOID GARBLED DATA.

FIGURE 4: POWER SUPPLY AND BATTERY ISOLATION CIRCUITRY



SUPPORT CIRCUITRY REQUIRED TO PRODUCE POWER FAIL DETECTION AND WRITE PROTECTION FORCES THE NEED FOR MULTICELL RECHARGEABLE BATTERY OR A LITHIUM BATTERY.

LITHIUM BATTERY BACKUP IS MORE RELIABLE

The lithium energy cell has raised concern about reliability and has been the object of much study. Data taken on the energy cell used in Dallas Semiconductor NV RAMs indicates a cell failure rate less than 0.5% at 55°C over a 10 year period.

Additional life studies taken on the same lithium energy source encapsulated in the manufacture of Dallas Semiconductor's NV RAMs have produced no failures in over 12 million device hours at 85°C. The lithium energy cell, then, is ideal for commercial and industrial semiconductor applications.

RETROFITTING EXISTING DESIGNS

The pinout of Dallas Semiconductor NV RAMs is an established industry standard (Figure 9). The Joint Electronic Devices Engineering Council's Bytewide Version B Standard defines and upgrades from 2K x 8 in density to 128K x 8.

This standard accommodates RAM, ROM, UV EPROMs, and EEPROMs. Because of the flexibility and upgradeability of bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore, many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs, and EEPROMs with Dallas Semiconductor NV SRAMs. These solutions add real time programmability and/or density upgrades to existing systems without redesign. Real time programmability gives the system the ability to be personalized by the end user. In other words, NV SRAMs can be retrofitted into existing designs without making changes to existing hardware. This retrofitting offers a cost effective, practical solution for companies who have invested in other memory devices that are less than ideal for their needs. For example, a design using conventional static RAM can be upgraded to nonvolatile

memory by substituting a Dallas Semiconductor NV SRAM for the RAM memory.

IN–CIRCUIT PROGRAMMABILITY

The advantages of NV SRAM can be related to the capability of software. Modern systems seek customization for the cost of standard product. In this aspect, software can be adapted in a system to perform specialized functions. It is even possible to totally modify a system personality over the telephone. In–circuit programming also reduces maintenance cost by eliminating service calls to update software. Software stored in RAM can be updated as often as necessary, depending on the configuration or application of the system.

PORTABLE APPLICATIONS

The advancement of high density, low power consuming portable personal computers is continuing to drive development requirements. For portable applications, difficult interface circuitry and refresh requirements of DRAM memories make them unsuitable for this application. SRAMs are not only easier to address and consume less power when operating, but also require very little power to maintain the contents of their memory. Even better, a NV SRAM can provide the high performance of a DRAM or SRAM and also guarantee that the main memory of the portable PC is truly nonvolatile. When a portable PC needs to be in standby mode, the main memory can be powered down altogether.

1 MBYTE MEMORY SUBSYSTEM USING NV SRAMS

Figure 6 shows a system block diagram with an Intel 386SL microprocessor with a 1 megabyte main memory of 128K x 8 NV SRAMS (DS1245). Figure 5, Portable Applications: Intel 386SL CPU/NV SRAM Timing, shows the requisite timing for the memory subsystem. The Intel 386SL is one of many microprocessors specially designed for low power, portable applications, and for addressing SRAM type memory.

4

FIGURE 5: PORTABLE APPLICATIONS: INTEL 386SL CPU/NV SRAM TIMING

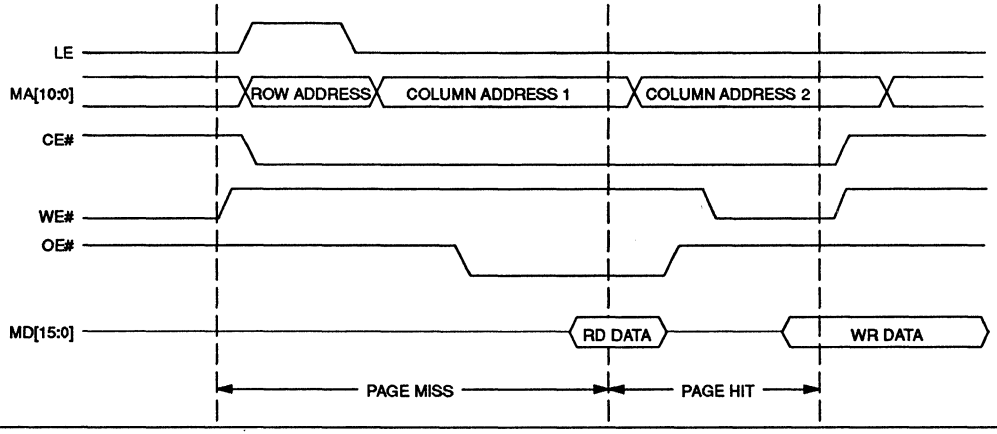
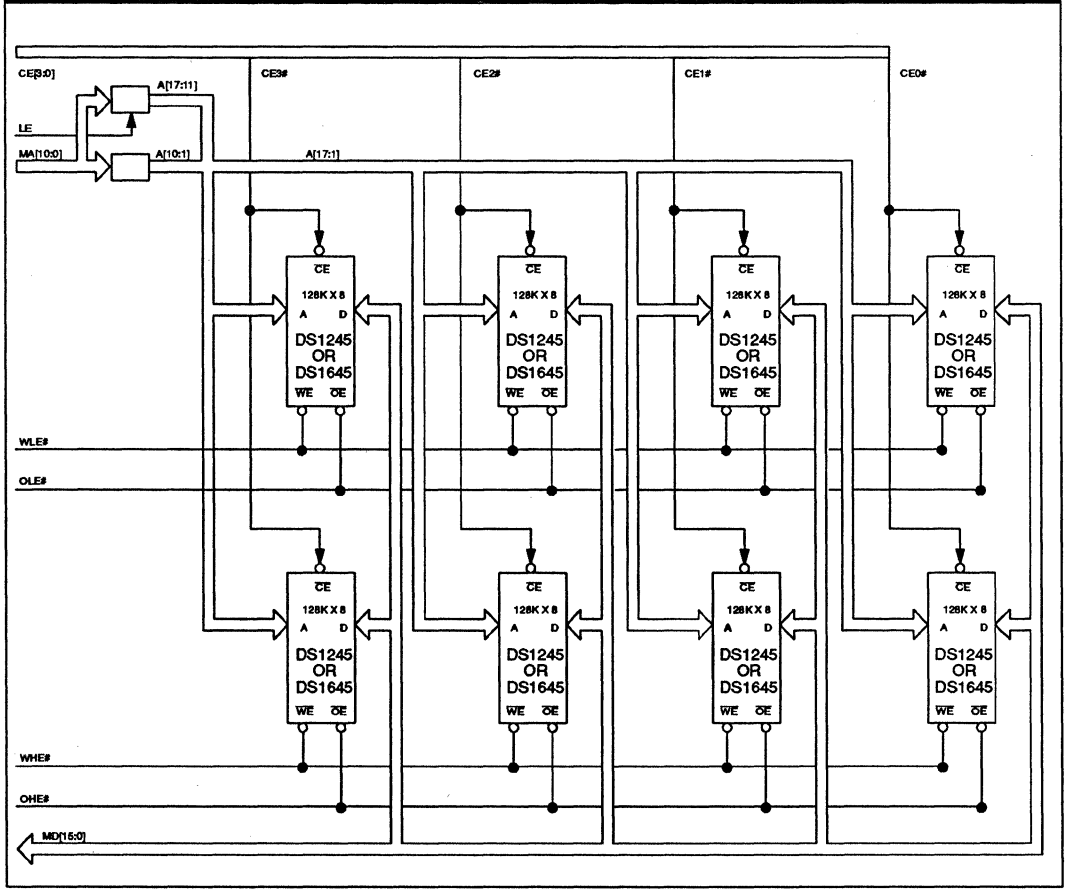


FIGURE 6: 1 MBYTE MEMORY SUBSYSTEM USING NV SRAMS



In Figure 6, eight DS1245Y SRAM memory modules are used to create a four–bank 1Mbyte SRAM memory subsystem. The following signals from the Intel 386SL CPU are required to address the SRAM module based system. The 386SL memory controller must be configured in its SRAM addressing mode for this application.

LE: Latch Enable. This signal selects is active high and serves to indicate that a row address is to be put on the address bus. A row address must be latched at this signal's falling edge. LE is connected to the latch enable input of the SRAM address latch.

MA[10:0]: Multiplexed Memory Address Bus. This bus provides address information for the Memory Controller Unit. The bus provides a 22 bit address in a multiplexed row/column sequence.

$\overline{CE}$[3:0]: Chip Enable outputs. These signals provide upper and lower byte enables for each SRAM bank.

$\overline{WLE}$: Write Low Enable. Indicates a write access to the lower byte of the 386SL CPU memory bus. The lower byte of data is put on the memory bus at the falling edge of $\overline{WLE}$.

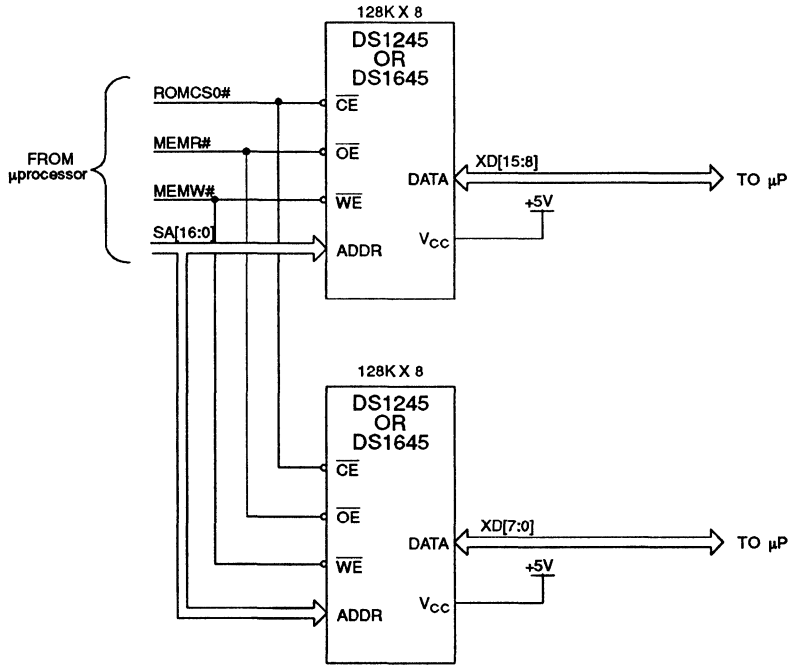
$\overline{WHE}$: Write High Enable. Indicates a write access to the high byte of the 386SL CPU memory bus. The high byte of data is put on the memory bus at the falling edge of $\overline{WHE}$.

$\overline{OLE}$: Output Low Enable. Enables the lower byte output from the SRAM modules.

$\overline{OHE}$: Output High Enable. Enables the high byte output from the SRAM modules.

MD[15:0]: Memory Data Bus. This bus provides data information for the Memory Controller Unit. Accesses from the Memory Controller Unit to the SRAM memory modules take place through this bus.

FIGURE 7: 16 BIT SINGLE BANK NV SRAM BIOS CIRCUIT



16 BIT SINGLE BANK NV SRAM BIOS CIRCUIT

Figure 7 shows Dallas NV SRAMs providing bios memory storage for an Intel 386SL CPU. Using the DS1645 NV SRAMs provide several advantages over using either OTP EPROM or FLASH type memories.

Flash memories require more operating current than NV SRAMs. Flash memories also require a high voltage source, 12V+, for any writes or updates that must be made to bios. NV SRAMs, on the other hand, require only their standard V_{CC} 5V input for both read and write access. Like Flash memories, a DS1645 NV SRAM maintains the contents of its memory in the absence of V_{CC}. A DS1645 has the additional feature that it can be easily programmed (through a series of 20 sequential reads) to write protect user selected blocks of memory. In effect, individual memory blocks in the SRAM module can be configured to appear as ROM memory, without detracting from the DS1645's ability to receive BIOS updates in its non write protected blocks of memory.

Traditional OTP EPROM's, while nonvolatile and very low power consuming like the DS1245 and DS1645 NV SRAMs, are lacking in that they can only be programmed once, and usually require a special fixture to be programmed. DS1245 and DS1645 NV SRAMs are almost equally low power consuming, and provide the capability to update BIOS. DS1245 and DS1645 NV SRAMs also provide fast 100ns access times, negating the need to insert additional wait states into BIOS access timing requirements.

The signals shown in Figure 7 are taken directly from the Intel 386SL CPU:

ROMCSO#: This signal is a dedicated ROM control signal provided by the 386SL CPU, and is active low, used to enable the system BIOS.

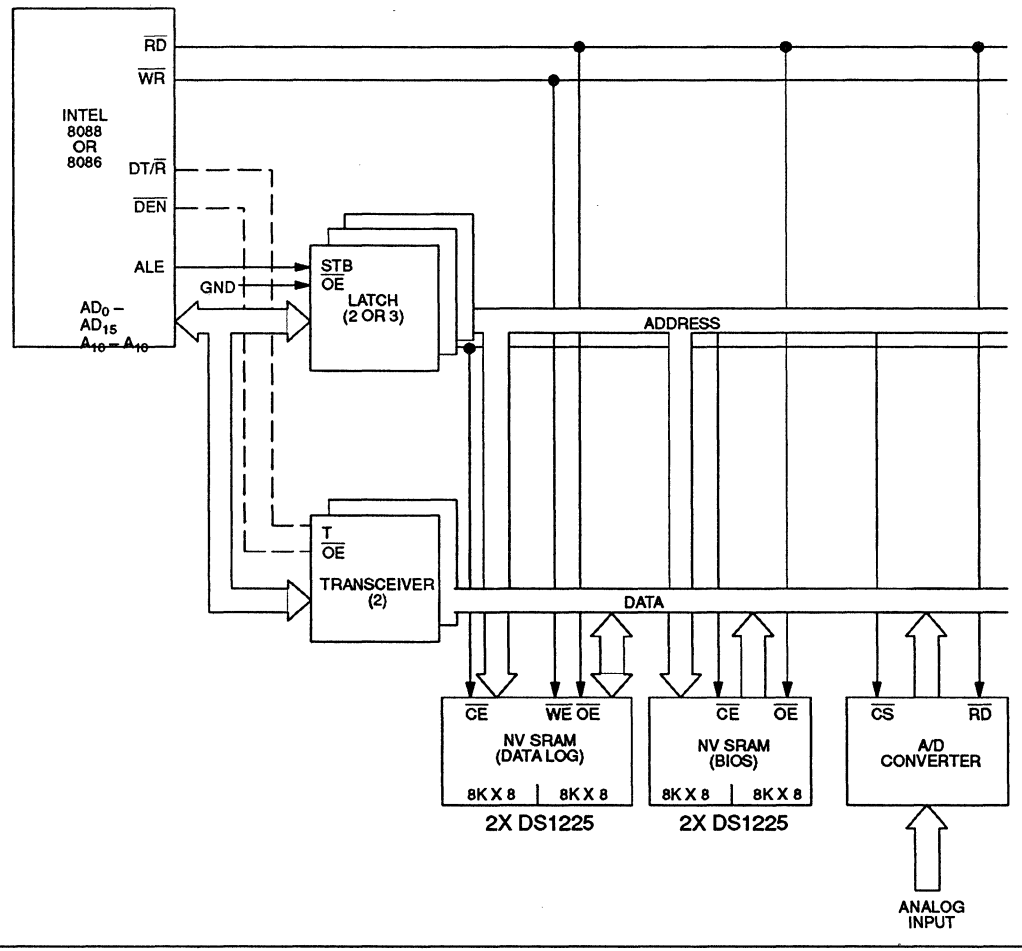
MEMR#: Memory Read. This signal indicates when a memory read access is occurring on the ISA–bus or X–bus, and is active low.

MEMW#: Memory Write. This signal indicates when a memory write access is occurring on the ISA–bus or X–bus, and is active low.

XD[15:0]: X–bus Data. Buffered data lines from the system data bus. These signals are produced using an external transceiver (see Intel 386SL Superset System Design Guide).

SA[16:0]: System Address Bus. This bus is driven by the 386SL CPU for system I/O accesses, and supplies both the ISA–bus and X–bus.

FIGURE 8: DATA LOGGING

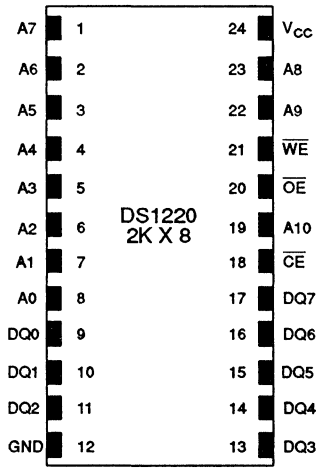


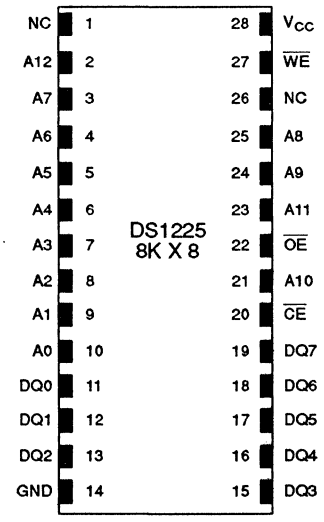
DATA LOGGING

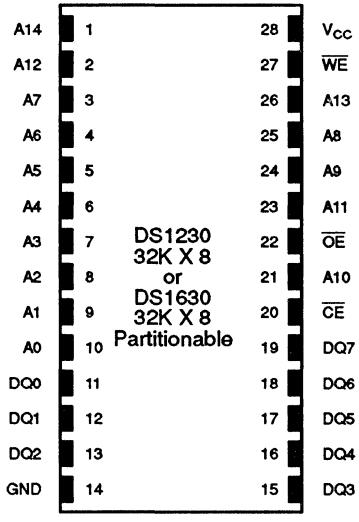
Figure 8 shows Dallas Semiconductor's NV SRAMs can provide a special advantage in environments where the power supply is not entirely reliable, or when power must periodically be shutdown. Dallas Semiconductor NV SRAMs contain memory control circuitry which not only maintains the data in the SRAM in the absence of power, but also write protects the device if V_{CC} is out of tolerance. This feature ensures that an unstable power supply does not corrupt data which has been collected.

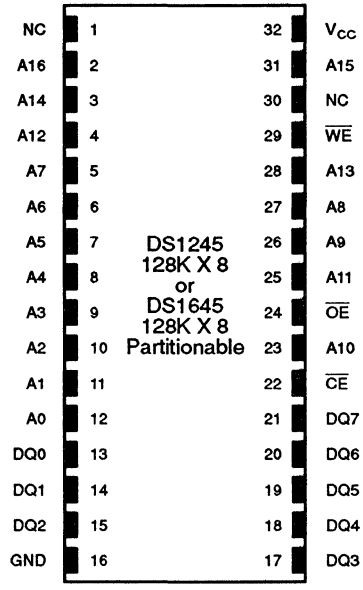
In this application, an Intel 8086 is shown in its minimal mode, connected to an address latch and bus transceiver to demultiplex the 8086's bus (see Figure 8). The resulting address and data busses may then be connected directly to two memory banks, one 8K x 16 bios memory consisting of two DS1225 NV SRAMs, the other an 8K x 16 memory bank consisting of two DS1225's acting as a data log. A data collecting device, such as an A/D converter, can be addressed as a read only peripheral device to sample a value and write it to the DS1225 acting as a data log. The DS1225 acting as the data log can transmit its data on the data bus to another peripheral, or may be removed from the system and taken to another location to have their logs extracted.

FIGURE 9: DALLAS SEMICONDUCTOR BATTERY BACKUP SRAM MODULES









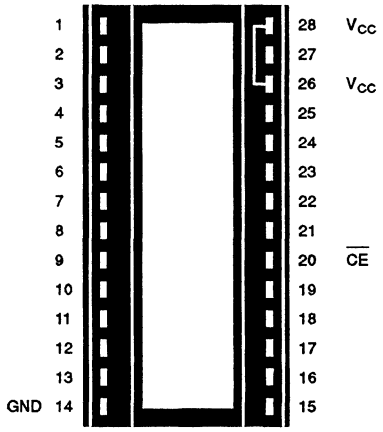
DALLAS SEMICONDUCTOR

DS1213B
SmartSocket 16K/64K

FEATURES

- Accepts standard 2K x 8 or 8K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K x 8 to 8K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass through except 20, 26, 28.

Pin 20	$\overline{CE}$	– Conditioned Chip Enable
Pin 26	V_{CC}	– Switched V_{CC} for 24-pin RAM
Pin 28	V_{CC}	– Switched V_{CC} for 28-pin RAM
Pin 14	GND	– Ground

DESCRIPTION

The DS1213B SmartSocket 16/64K is a 28-pin, 0.6 inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K x 8 or 24-pin 2K x 8 lower-justified JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of the SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pins 28, 26, 20, and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

OPERATION

The DS1213B SmartSocket performs five circuit functions required to battery back up a CMOS memory. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power-fail detection. Power-fail detection occurs between 4.75 and 4.5 volts. The DS1213B constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of V_{CC} or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213B performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1213B SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back up the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cell s contains 35 mA/hr capacity, making the total 70 mA/hr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the V_{CC} pin. In order to read the cell potential, apply V_{CC} and then remove power. The cell potential will then be available on pins 26, 28, and 20.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC}+0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+ 0.8	V	1,3

DC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3,8
PIN 20 L $\overline{CE}$ Input Leakage	I_{IL}	-1.0		+1.0	µA	3, 4
PIN 20 U $\overline{CE}$ Output @ 2.4 V	I_{OH}	-1.0			mA	2, 3
PIN 20 U $\overline{CE}$ Output @ .4V	I_{OL}			4.0	mA	2, 3

($0°C$ to $70°C$, $V_{CC} < 4.5V$)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT}-0.2			V	3
PIN 26 U, PIN 28U Battery Current	I_{BAT}			1	µA	3,6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}			5	3	3
Output Capacitance PIN 20 U	C_{OUT}			7	3	3

AC ELECTRICAL CHARACTERISTICS

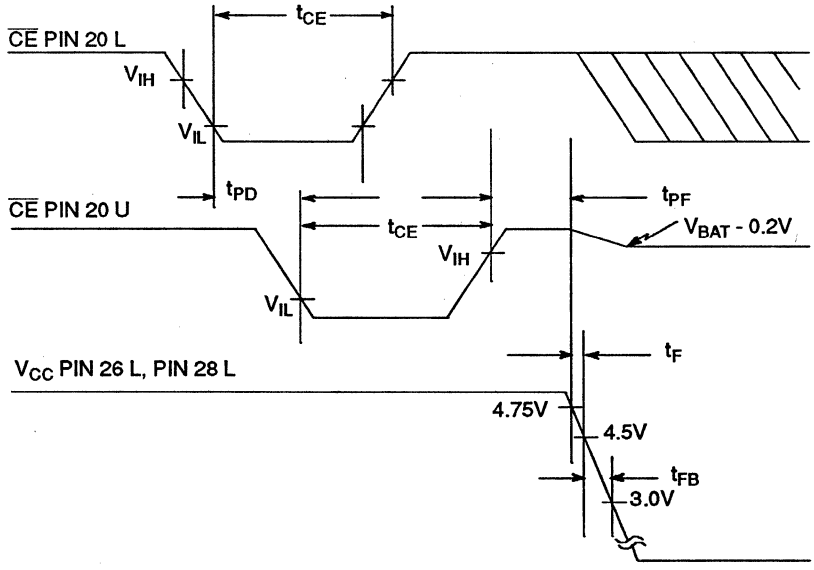
($0°C$ to $70°C$, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

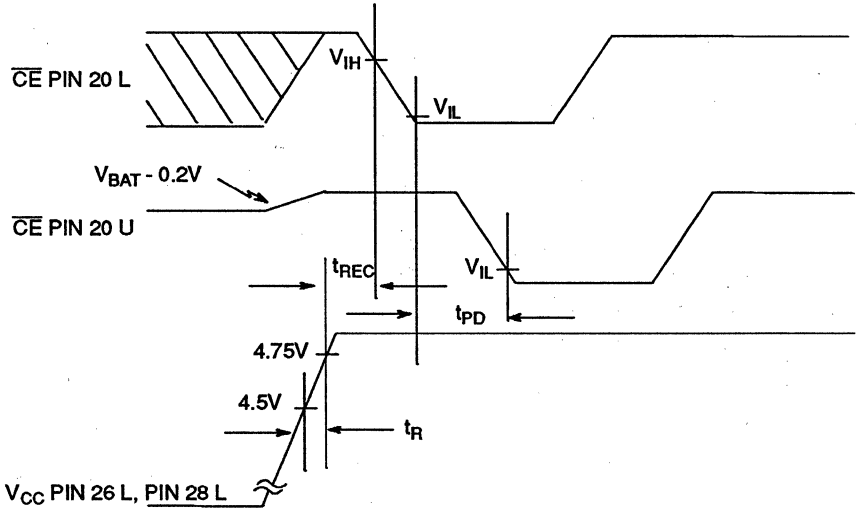
($0°$ to $70°C$, $V_{CCI} < 4.75$ V)

Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			µs	
V_{CC} Slew Rate 4.5 - 3 V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5-4.75 V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7

TIMING DIAGRAM - POWER-DOWN



TIMING DIAGRAM - POWER-UP



WARNING:

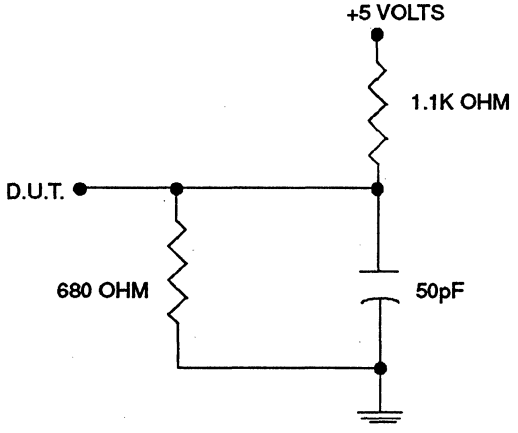
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source as exposed voltage pins are present.

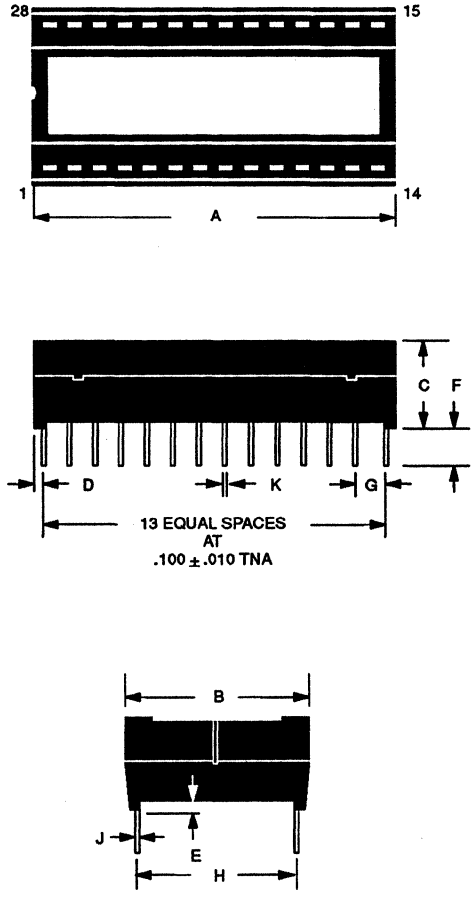
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



DS1213B INTELLIGENT SOCKET 28 PIN (FOR 600 MIL DIP)



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.395 10.03
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

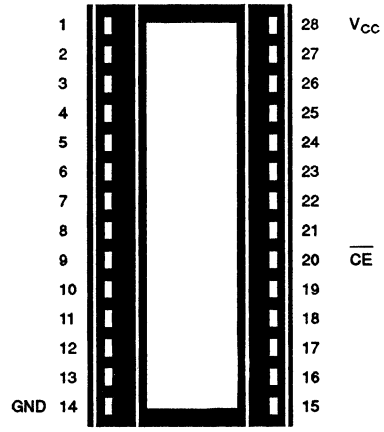
DALLAS SEMICONDUCTOR

DS1213C
SmartSocket 64K/256K

FEATURES

- Accepts standard 8K x 8 or 32K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K x 8 to 32K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass thorough except 20, 28.

Pin 20 $\overline{CE}$ – Conditioned Chip Enable
Pin 28 V_{CC} – Switched V_{CC}
Pin 14 GND – Ground

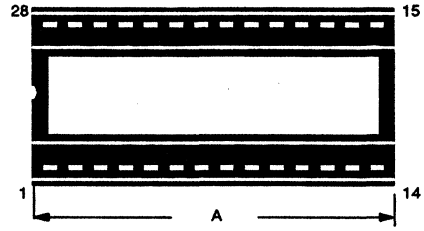
DESCRIPTION

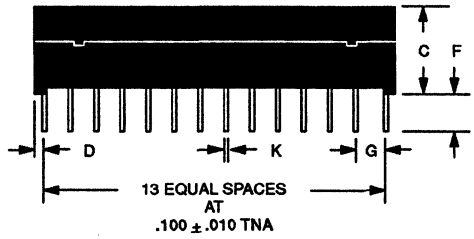
The DS1213C SmartSocket is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

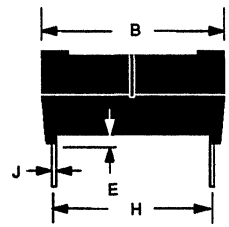
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

DS1213C INTELLIGENT SOCKET 28-PIN (FOR 600 MIL DIP)







PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	1.380 35.05	1.420 36.07
B IN. MM	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.395 10.03
D IN. MM	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

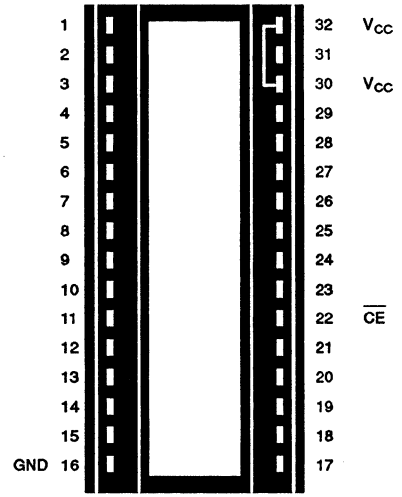
DALLAS SEMICONDUCTOR

DS1213D
SmartSocket 64K/256K/1M

FEATURES

- Accepts standard 8K x 8, 32K x 8, 128K x 8, or 512K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K x 8 to 512K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



32-Pin Intelligent Socket (600 Mil)

PIN DESCRIPTION

All pins pass through except 22, 30 and 32.

Pin 22	$\overline{CE}$	– Conditioned Chip Enable
Pin 32	V_{CC}	– Switched V_{CC} for 32-pin RAM
Pin 30	V_{CC}	– Switched V_{CC} for 28-pin RAM
Pin 16	GND	– Ground

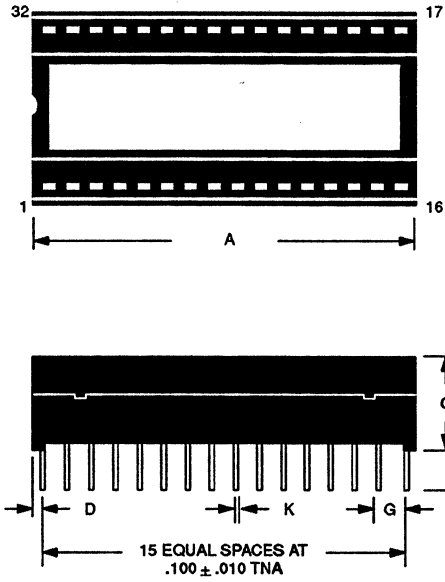
DESCRIPTION

The DS1213D SmartSocket is a 32-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8 or 512K x 8 bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

DS1213D INTELLIGENT SOCKET 32-PIN (FOR 600 MIL DIP)



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.580	1.620
MM	40.13	41.15
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.350	0.410
MM	8.89	10.4
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

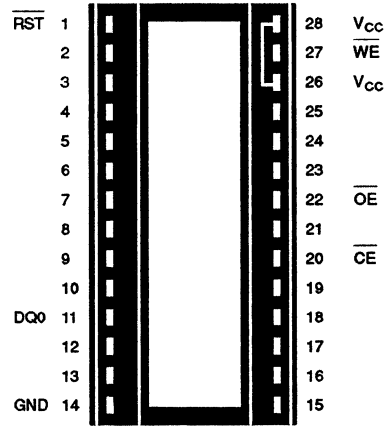
DALLAS SEMICONDUCTOR

DS1216B
SmartWatch/RAM 16K/64K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K x 8 and 8K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All Pins Pass Through Except 20, 26, 28

Pin 1	$\overline{RST}$	- Reset
Pin 11	DQ0	- Data Input/Output 0
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 26	V_{CC}	- Switched V_{CC} for 24 Pin RAM
Pin 27	$\overline{WE}$	- Write Enable
Pin 28	V_{CC}	- Switched V_{CC} for 28 Pin RAM

DESCRIPTION

The DS1216B SmartWatch/RAM 16/64K is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

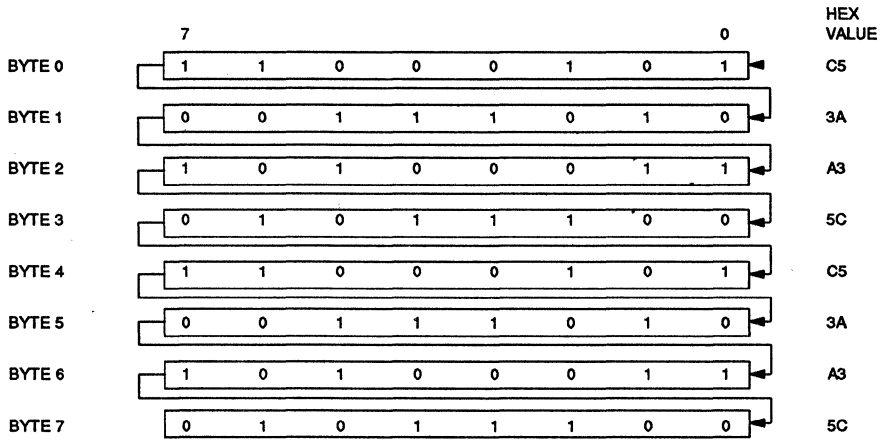
OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}. This pattern is sent to the SmartWatch LSB to MSB.

NONVOLATILE CONTROLLER OPERATION

The DS1216B SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartWatch provides is power-fail detection. Power-fail detection occurs at approximately 4.0 volts. The DS1216B constantly monitors the V_{CC} supply. When V_{CC} goes out of tolerance, a comparator outputs a power-fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of V_{CC} or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each register must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

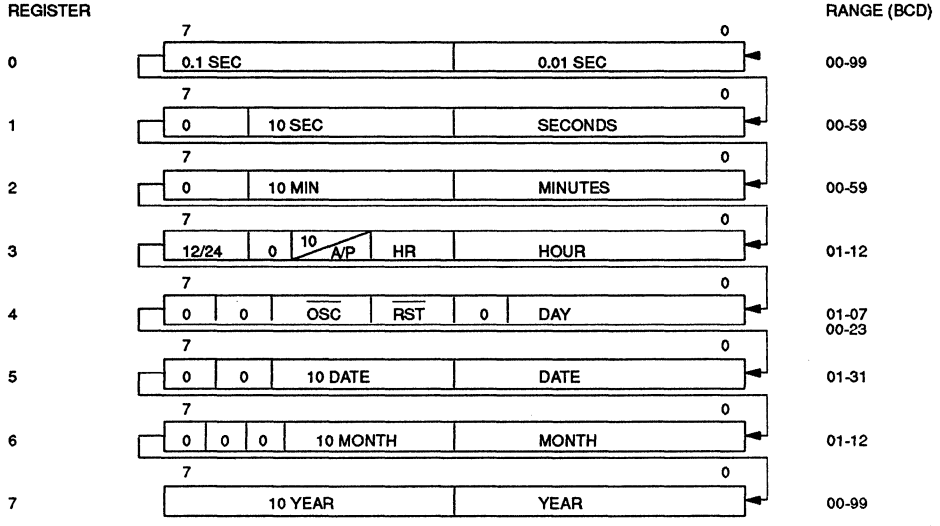
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{RESET}$ and oscillator functions. Bit 4 controls the $\overline{RESET}$ (pin 1). When the $\overline{RESET}$ bit is set to logic 1, the $\overline{RESET}$ input pin is ignored. When the $\overline{RESET}$ bit is set to logic 0, a low input on the $\overline{RESET}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO 7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1, 10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3,4,5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3,8
Input Leakage	I_{IL}	-1.0		+1.0	µA	4,10,13
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°, V_{CC} < 4.5V)

PIN 20U Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	µA	3,6
PIN 26U, PIN 28U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

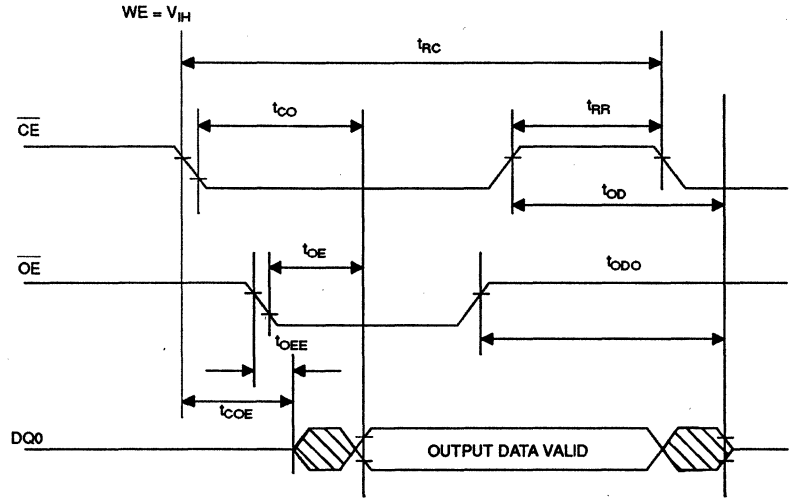
(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Setup Time	t_{DS}	100			ns	12
Data Hold Time	t_{DH}	0			ns	12
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

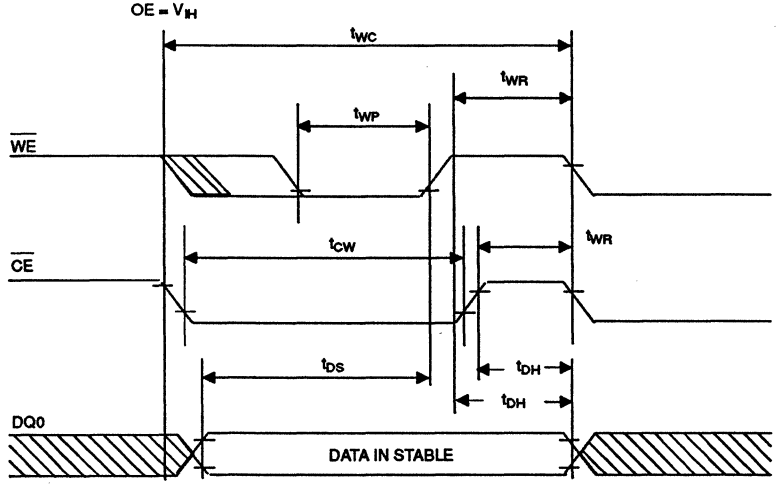
(0°C to 70°C, V_{CC} <4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7

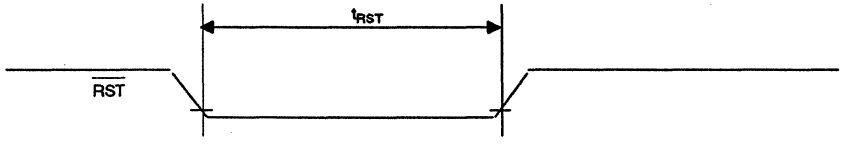
TIMING DIAGRAM-READ CYCLE TO SMARTWATCH



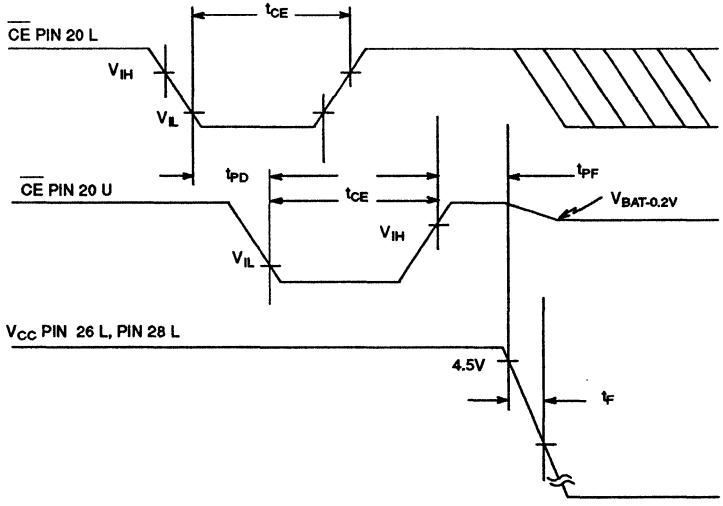
TIMING DIAGRAM-WRITE CYCLE TO SMARTWATCH



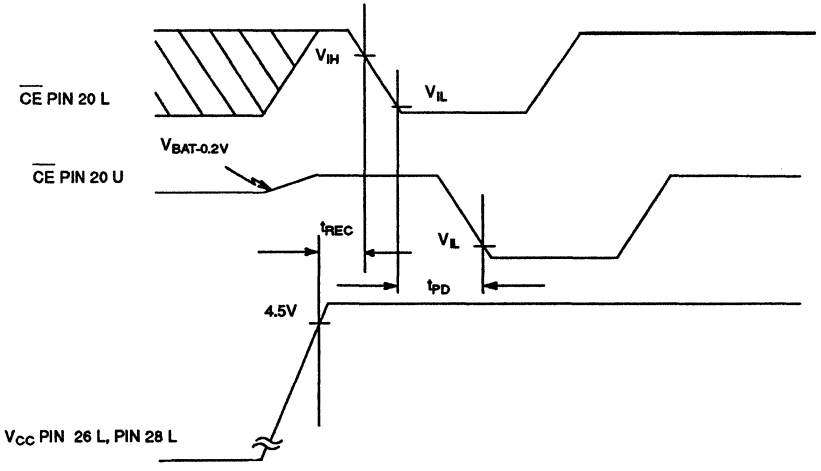
TIMING DIAGRAM-RESET FOR SMARTWATCH



TIMING DIAGRAM-POWER-DOWN



TIMING DIAGRAM-POWER-UP



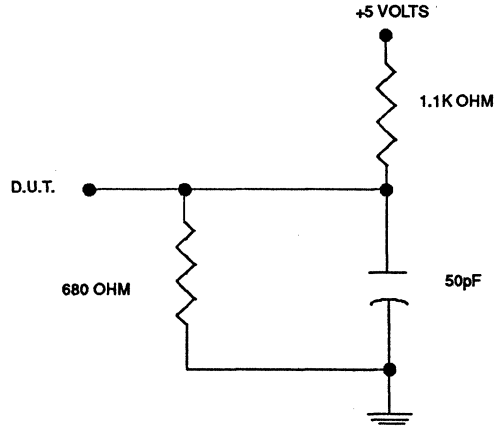
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

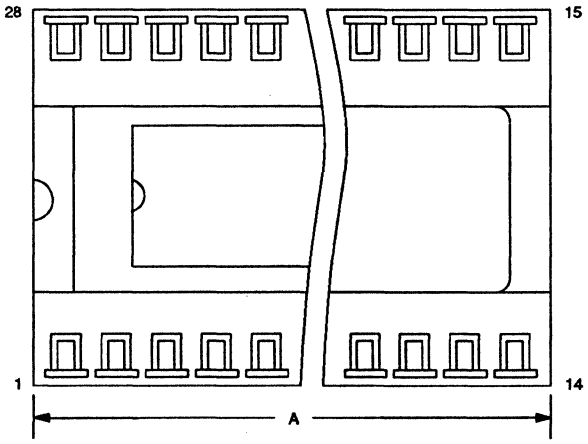
NOTES

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26L can be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L.
11. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

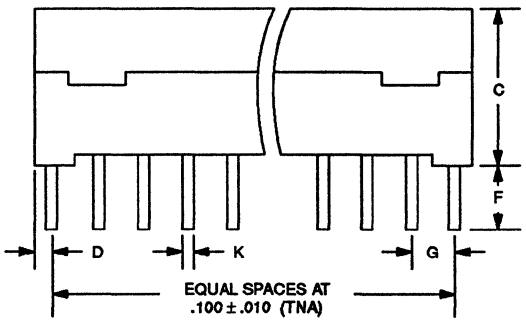
OUTPUT LOAD Figure 3

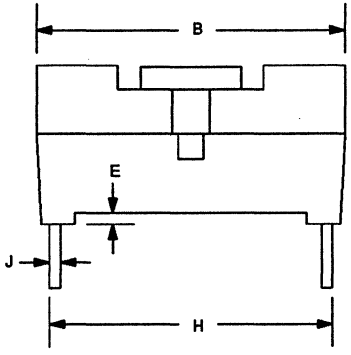


DS1216B SMARTWATCH



PKG	28-PIN		32-PIN	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A IN.	1.390	1.420	1.580	1.620
MM	35.31	36.07	40.13	41.14
B IN.	0.690	0.720	0.690	0.720
MM	17.53	18.29	17.53	18.29
C IN.	0.350	0.395	0.350	0.410
MM	8.89	10.03	8.89	10.40
D IN.	0.035	0.065	0.035	0.065
MM	0.89	1.65	0.89	1.65
E IN.	0.015	0.035	0.015	0.035
MM	0.38	0.89	0.38	0.89
F IN.	0.120	0.160	0.120	0.160
MM	3.04	4.06	3.04	4.06
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.590	0.630	0.590	0.630
MM	14.99	16.00	14.99	16.00
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53





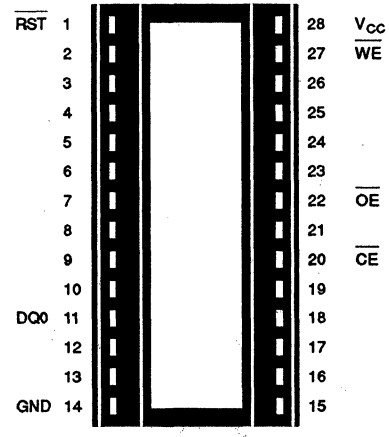
DALLAS SEMICONDUCTOR

DS1216C
SmartWatch/RAM 64K/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K x 8 and 32K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 min./month @ 25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass through except 20, 28.

Pin 1	$\overline{RST}$	- $\overline{RESET}$
Pin 11	DQ0	- Data Input/Output 0
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 27	$\overline{WE}$	- Write Enable
Pin 28	V_{CC}	- Switched V_{CC}

DESCRIPTION

The DS1216C SmartWatch/RAM is a 28-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS stat ic RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

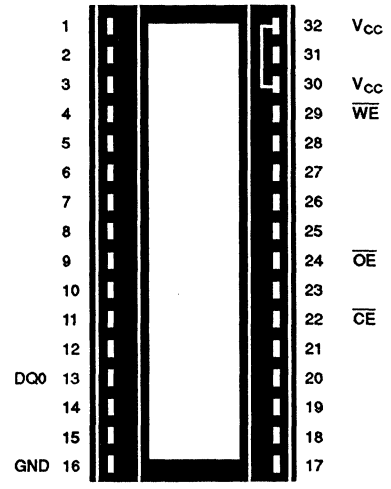
DALLAS SEMICONDUCTOR

DS1216D
SmartWatch/RAM 256K/1M

FEATURES

- Converts standard 8K x 8, 32K x 8, 128K x 8, and 512K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 min./month @ 25°C

PIN ASSIGNMENT



32-Pin Intelligent Socket

PIN DESCRIPTION

All pins pass through except 22, 30 and 32.

Pin 1	$\overline{RST}$	- RESET
Pin 13	DQ0	- Data Input/Output 0
Pin 16	GND	- Ground
Pin 22	$\overline{CE}$	- Conditioned Chip Enable
Pin 24	$\overline{OE}$	- Output Enable
Pin 29	$\overline{WE}$	- Write Enable
Pin 30	V_{CC}	- Switched V_{CC} for 28-pin RAM
Pin 32	V_{CC}	- Switched V_{CC} for 32-pin RAM

DESCRIPTION

The DS1216D SmartWatch/RAM 256K/1M is a 32-pin, 600 MIL wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8, or 512K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS SRAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

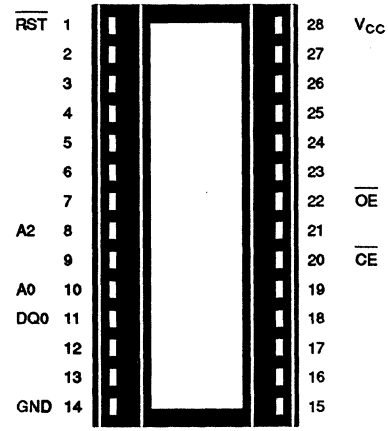
DALLAS SEMICONDUCTOR

DS1216E
SmartWatch/ROM 64K/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within ± 1 minute/month @25°C

PIN ASSIGNMENT



28-Pin Intelligent Socket

PIN DESCRIPTION

Pin 1	$\overline{RST}$	- Reset
Pin 8	A2	- Address Bit 2 ($\overline{READ/WRITE}$)
Pin 10	A0	- Address Bit 0 (Data Input)
Pin 11	DQ0	- I/O_0 (Data Output)
Pin 14	GND	- Ground
Pin 20	$\overline{CE}$	- Conditioned Chip Enable
Pin 22	$\overline{OE}$	- Output Enable
Pin 28	V_{CC}	- +5 VDC to the Socket

All pins pass through to the socket except 20.

DESCRIPTION

The DS1216E SmartWatch/ROM 64/256K is a 28-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of the SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20, and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$), which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnects the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles that are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle.

Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch, ensuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison reg ister and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of $\overline{READ}$/$\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low if enabled, or on power-up. The $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power-fail detection. Power-fail detection typically occurs at approximately 4.0 volts. Finally, the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power-fail detection has occurred. Power-fail detection also has the same effect on data transfer as the $\overline{RESET}$ input.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in eight registers of eight bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of eight bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

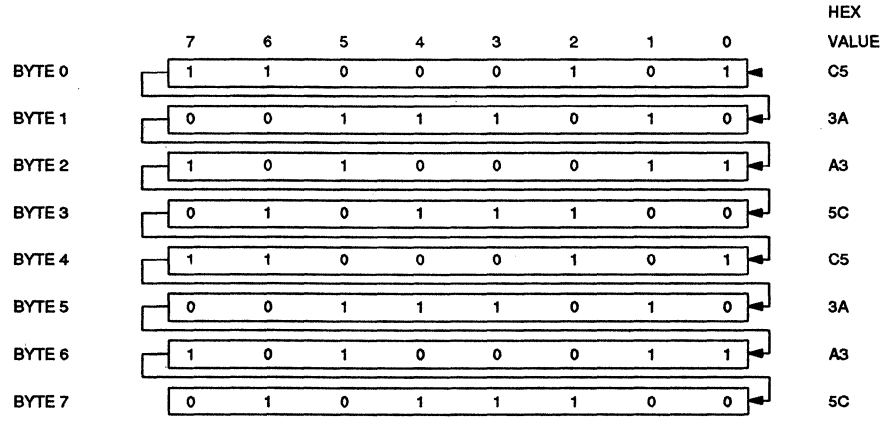
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{RESET}$ and oscillator functions. Bit 4 controls the $\overline{RESET}$ (pin 1). When the $\overline{RESET}$ bit is set to logic 1, the $\overline{RESET}$ input pin is ignored. When the $\overline{RESET}$ bit is set to logic 0, a low input on the $\overline{RESET}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is turned off. When set to logic 0, the oscillator turns on and the watch becomes operational. Both bits are set to a logic 1 when shipped from the factory

ZERO BITS

Registers 1,2,3,4,5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

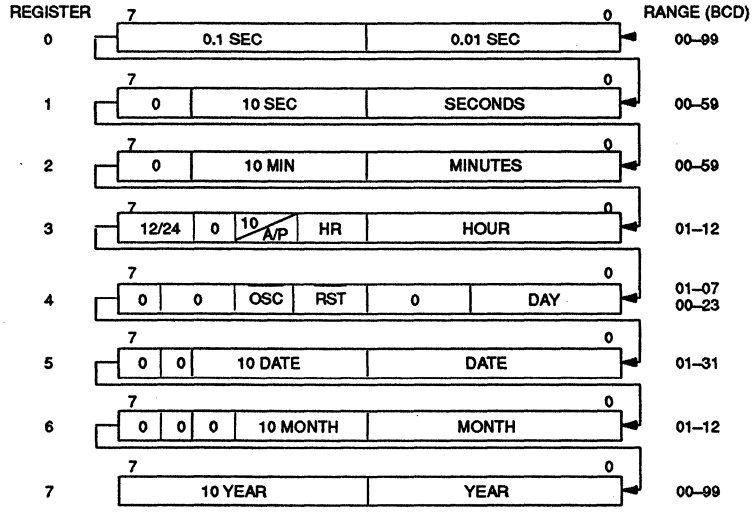
SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE

The pattern recognition sequence in Hex is C5, 3A, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch are less than 1 in 10^{19}. This pattern is sent to the SmartWatch LSB to MSB.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO 7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 6

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DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 28L, Supply Current	I_{CCI}			5	mA	3,4
Input Leakage	I_{IL}	-1.0		+1.0	µA	4,6,10
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

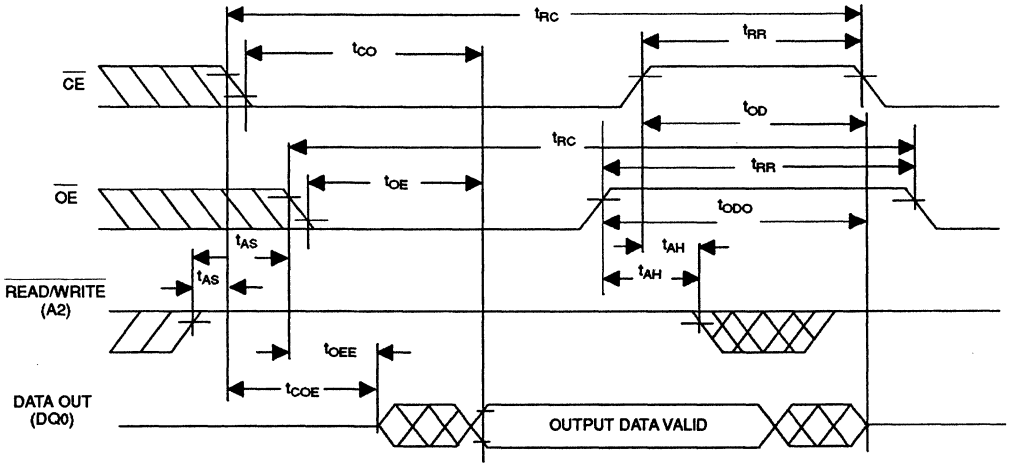
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Address Setup Time	t_{AS}	20			ns	9
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	7
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Setup Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	0			ns	8
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

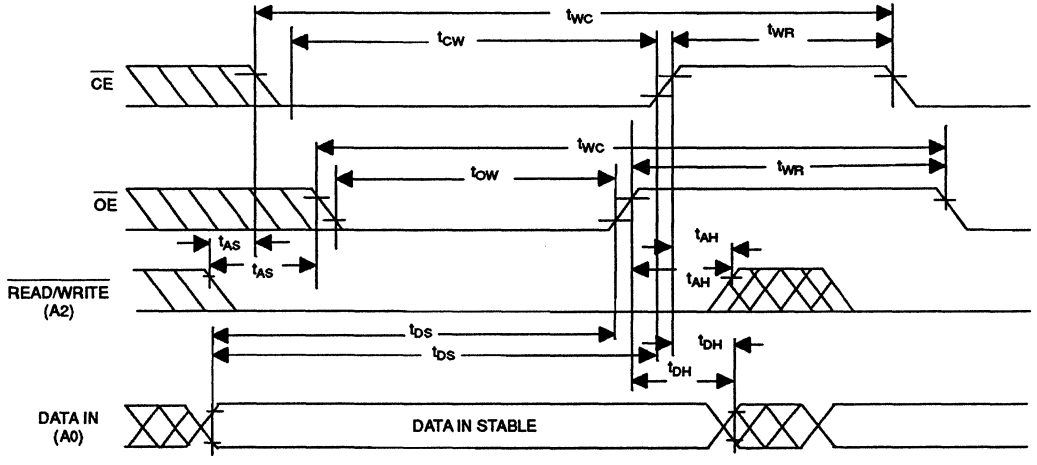
(0°C to 70°C, V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			µs	

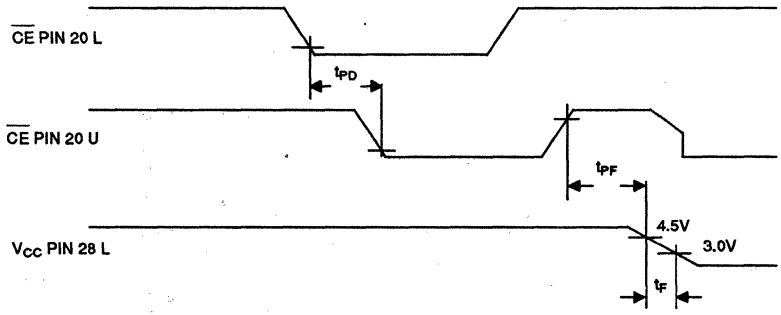
TIMING DIAGRAM - READ CYCLE



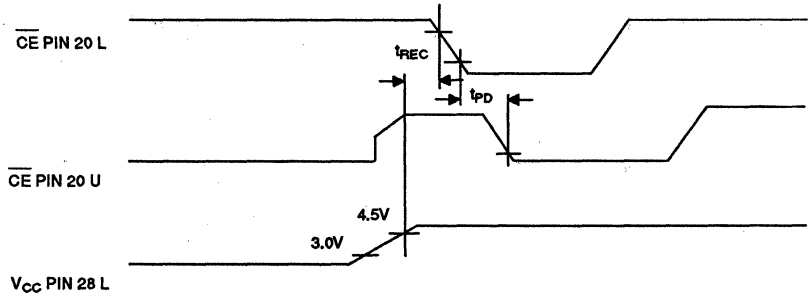
TIMING DIAGRAM - WRITE CYCLE



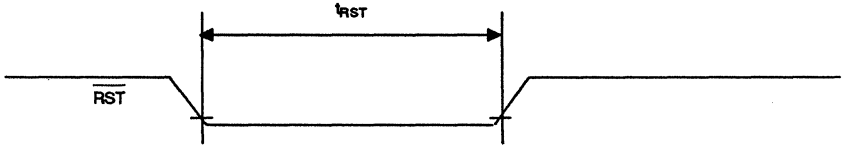
TIMING DIAGRAM - POWER-DOWN



TIMING DIAGRAM - POWER-UP



TIMING DIAGRAM - RESET FOR SMARTWATCH



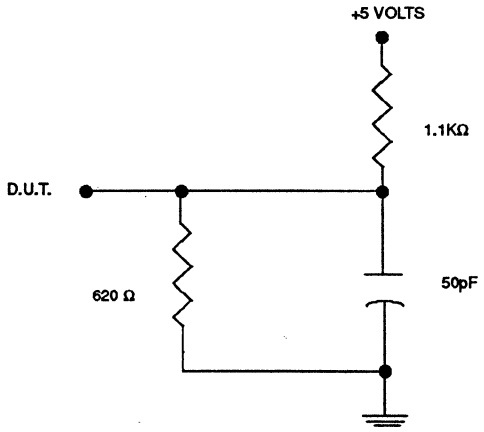
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

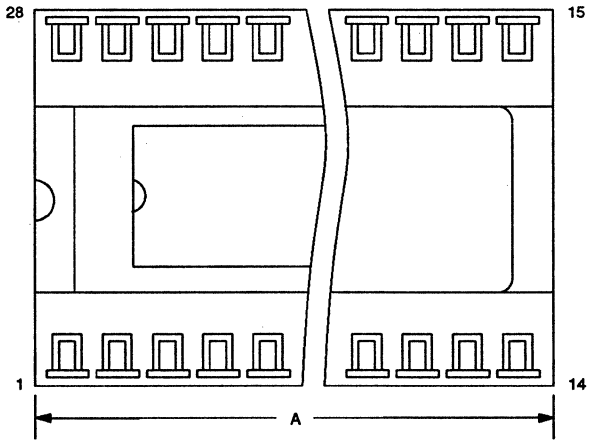
NOTES

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. t_{AH}, t_{DS}, and t_{DH} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
9. t_{AS} is a function of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
10. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

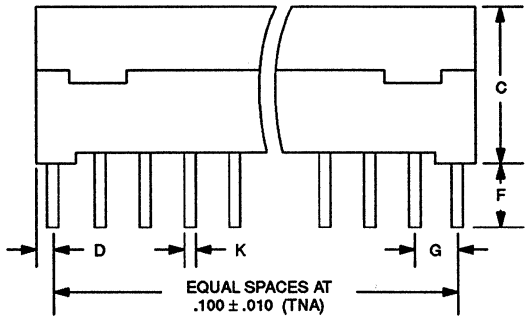
OUTPUT LOAD Figure 3

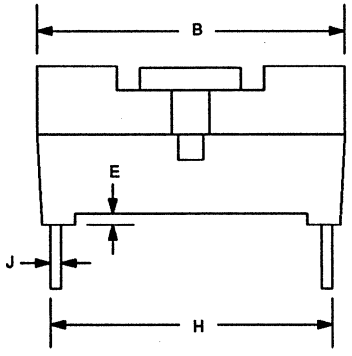


DS1216E SMARTWATCH



PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	1.390 35.31	1.420 36.07	1.580 40.13	1.620 41.14
B IN. MM	0.690 17.53	0.720 18.29	0.690 17.53	0.720 18.29
C IN. MM	0.350 8.89	0.395 10.03	0.350 8.89	0.410 10.40
D IN. MM	0.035 0.89	0.065 1.65	0.035 0.89	0.065 1.65
E IN. MM	0.015 0.38	0.035 0.89	0.015 0.38	0.035 0.89
F IN. MM	0.120 3.04	0.160 4.06	0.120 3.04	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53





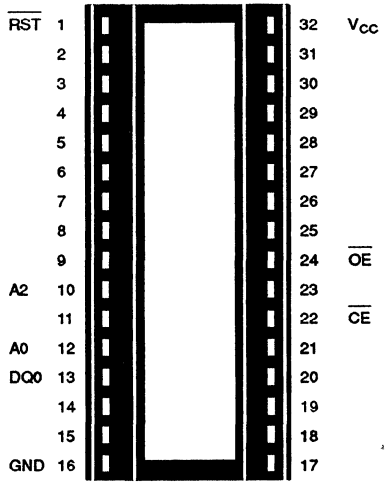
DALLAS SEMICONDUCTOR

DS1216F
SmartWatch/ROM 64K/256K/1M

FEATURES

- Adds timekeeping to any 32-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C

PIN ASSIGNMENT



32-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

Pin 1	$\overline{RST}$	- RESET
Pin 10	A2	- Address Bit 2 (READ/ $\overline{WRITE}$)
Pin 12	A0	- Address Bit 0 (Data Input)
Pin 13	DQ0	- I/O_0 (Data Output)
Pin 16	GND	- Ground
Pin 22	$\overline{CE}$	- Conditioned Chip Enable
Pin 24	$\overline{OE}$	- Output Enable
Pin 32	V_{CC}	- +5 VDC to the Socket

All pins pass through to the socket except 22.

DESCRIPTION

The DS1216F SmartWatch/ROM is a 32-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeping function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source automatically switches on to prevent loss of time and calendar data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22, and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 ($\overline{CE}$), which is inhibited during the transfer of time information.

See the DS1216E SmartWatch/ROM/64/256K data sheet for technical details.

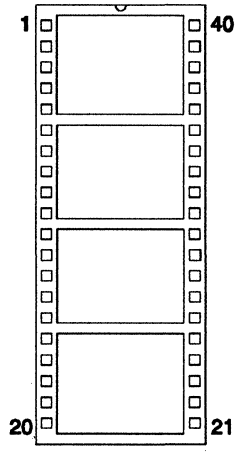
DALLAS SEMICONDUCTOR

DS1310/DS1311
Super Socket

FEATURES:

- Built-in CMOS circuitry adds nonvolatile SRAM and real time clock to existing microcontroller-based designs
- Requires no printed circuit board modification
- 4K bits of NV SRAM for more than 10 years in the absence of V_{CC}
- Optional timekeeper for event dating and activity scheduling
- Accepts any microcontroller in standard 40-pin DIP whose V_{CC} and ground are pins 40 and 20, respectively
- Parasitic serial interface to built-in circuitry via a single microcontroller I/O pin
- Special wake-up pattern for invoking added functionality
- Proven gas-tight socket contacts

PACKAGE OUTLINE



PIN ASSIGNMENTS

(\ indicates condition low.)

All pins pass through except for:

Pin 20 - Ground

Pin 40 - V_{CC}

Any pin except for 20 and 40 can be user-configured for added functionality by closing the appropriate shorting pads of the Super Socket with solder.

CIRCUIT DESCRIPTION

DS131x Super Sockets are 40-pin, 0.6-inch wide DIP sockets with built-in CMOS circuitry that adds new functions to existing microcontroller-based systems. The circuits within the Super Socket are special versions of a 1-Wire peripheral integrated circuit designed to support parasitic communication on a single I/O pin of the microcontroller.

The Super Socket accepts any 40-pin, single-chip microcontroller with V_{cc} and ground on pins 40 and 20, respectively. When mated with a microcontroller, the Super Socket provides access to its built-in, 1-Wire chip by means of a wake-up pattern that is sent via a single bidirectional I/O pin on the microcontroller. As a result, the chip resides as a parasite on an I/O pin without encumbering the pin's normal function.

The DS131x is an effective upgrade option for previously-designed, single-chip systems and requires only slight software modification.

OPERATION

Each Super Socket incorporates a special 1-Wire peripheral chip with some features deleted to support parasitic operation. Table 1 below summarizes the functions associated with each Super Socket along with its built-in, 1-Wire embedded chip.

SUPER SOCKET STANDARD VERSIONS

Table 2

Part Number	Description	Embedded Chip
DS1310-00	4Kbit NVSRAM	DS2413
DS1311-00	4Kbit NVSRAM w/ Timekeeper	DS2414

A special ROM mask configures all chips of this type to have a common 64-bit code that is used as a wake-up pattern in parasitic communication.

The DS2413 and DS2414 are special versions of the DS2403 and DS2404 1-Wire peripherals, respectively. The unique aspects of the DS2413 and DS2414 are described in this data sheet. The user should refer to the DS2403 and DS2404 data sheets for basic 1-Wire operational information.

The DS241x part embedded within the DS131x socket functions identically with its standard 1-Wire counterpart with the exception that Match is the only valid 1-wire command. Read, Skip, Search and Presence Detect, which are used in the Super Sockets, have been ROM-masked out of the DS2413/14. This prevents the DS131x from responding to one of these 8-bit codes when noise on the I/O pin happens to emulate one of these commands. In order to have a known wake-up pattern, all DS131x devices were given the same 64-bit code. This code also allows identical single-chip microcontroller systems to be programmed with the same code changes residing in all systems, thus making manufacturing a large number of identical units much simpler from a software standpoint.

The DS131x remains transparent until the 1-Wire Match command has been issued. The DS241x then checks the ID type, serial number and CRC byte that follow this command. If a match is established, then the DS241x looks for a second command on the I/O pin to be sent. This command will be a Read Scratch, Write Scratch, Copy Scratch to Secure Memory, or Read Secure Memory. When one of these commands has been issued, the DS241x responds with the appropriate action. If this format is not followed exactly, the DS241x will wait in a null state for the microcontroller to issue a 1-Wire reset command. (See the DS2403/04 data sheet for this reset format and other operational information.)

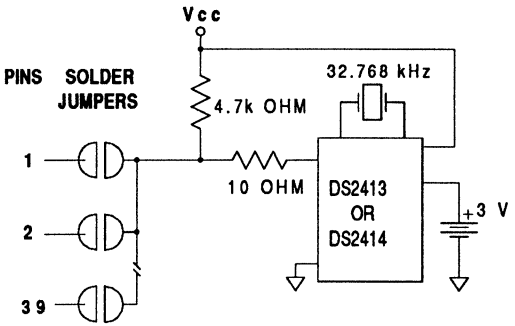
STANDARD VERSION

The DS1310-00 and DS1311-00 are standard versions of the Super Socket. These parts have only pins 20 and 40 connected to the built-in, 1-Wire chip. The data line of the 1-Wire device must be connected to an I/O pin, selected by the customer, by closing the appropriate shorting pad on the DS1310-00. The user has complete control over the I/O pin to be designated as the 1-Wire interface. The DS1311-00 uses one of four predefined I/O pins: 4, 8, 24, or 36.

Each pin of the DS1310-00, with the exception of pins 20 and 40, is connected to one side of a shorting pad (see Figure 1). The other side of this pad is connected to the I/O pin of the DS241x 1-Wire serial IC. With this arrangement, the user can select any I/O pin of the microcontroller, with the exception of pins 20 and 40, to be used as the communication line between the microcontroller and the DS1310-00.

Note that only one set of shorting pads will be closed in the DS1310-00. Any other condition will result in unknown data transfers.

SUPER SOCKET EMBEDDED CIRCUIT Figure 1



SPECIAL VERSIONS

Special versions of the DS1310-00 and DS1311-00 are available from Dallas Semiconductor with fixed I/O designations. Please contact Dallas Semiconductor for ordering information on these special versions.

PARASITIC COMMUNICATION

The 1-Wire interface to the Super Socket's built-in circuitry allows added functionality with minimal impact on existing system hardware in retrofit applications. However, in these situations, the pin used for communication must be appropriately selected in order for the 1-Wire IC to reside as a parasite on that pin.

The following are rules for pin selection:

1. The pin to be used for communication must be a bidirectional I/O pin of the microcontroller.

2. The pin must be able to be toggled without consequence to existing hardware.

3. The pin must be able to time 15*us* and 60 *us* signal transitions. This means that the microcontroller must be clocked at some minimum frequency.

Rules #1 and #3 are requirements for communication with the built-in, 1-Wire IC itself. Rule #2 is a consideration for retrofit applications to eliminate the need for hardware change.

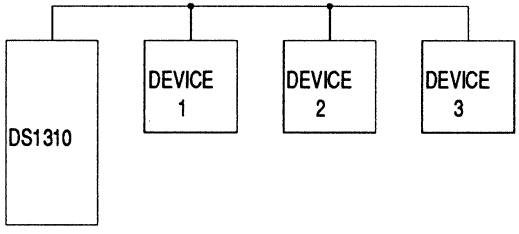
Examples of pins used in typical application which can also serve as the communication line include those used for interface to keyboards and/or displays, as well as those used as data lines to external serial or parallel peripheral devices.

Note that there is a 4.7K pull-up resistor inside the DS131x that is connected to the data line of the built-in, 1-Wire IC (see Figure 1).

EXPANDING THE 1-Wire

By using the same microcontroller I/O pin connected to the embedded 1-Wire IC, the user can expand the 1-Wire serial link to include external 1-Wire devices. It is important to remember that parasitic communication may not be possible with this scheme due to the fact that the other 1-Wire devices can take control of the microcontroller's I/O pin. The diagram below shows how to continue the 1-Wire serial link.

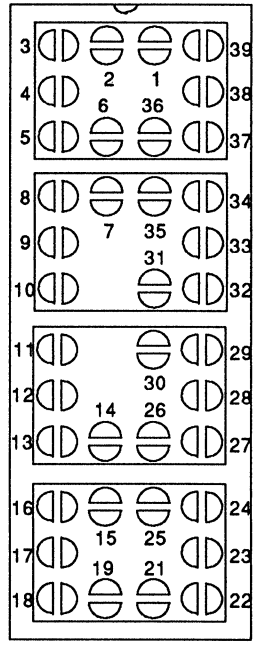
SUPER SOCKET EXPANSION FOR ADDITIONAL 1-WIRE DEVICES. Figure 2



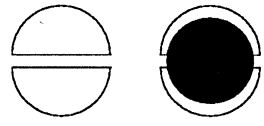
JUMPERING INSTRUCTIONS

Identify the pin of the microcontroller to be used for communication. Locate the shorting pads of the DS131x that correspond to the selected microcontroller pin. Use the jumper guide to locate these pads (see Figure 3). Close these pads by soldering them together with a droplet of solder (see Figure 4). The Super Socket is now ready for installation and use in the desired hardware. Plug in any 40-pin microcontroller (with +5 on pin 40 and ground on pin 20) whose software has been modified for use with the 1-Wire interface.

JUMPER GUIDE Figure 3



JUMPER PADS Figure 4

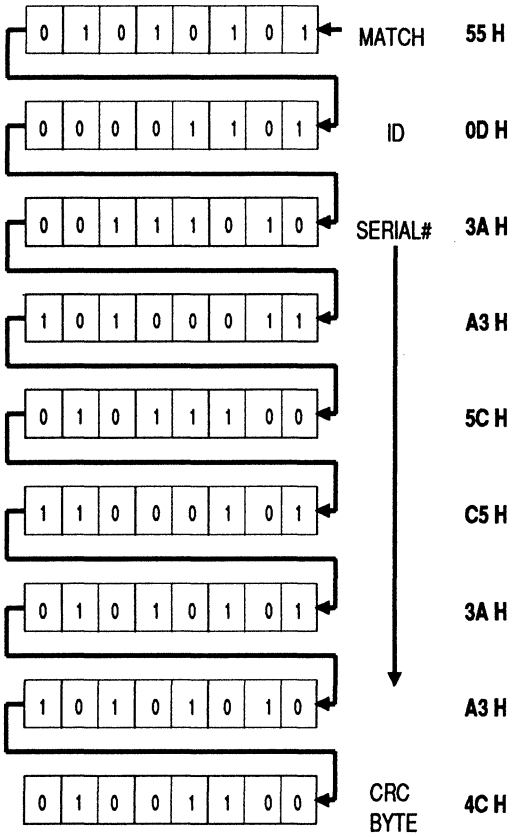


OPEN CLOSED

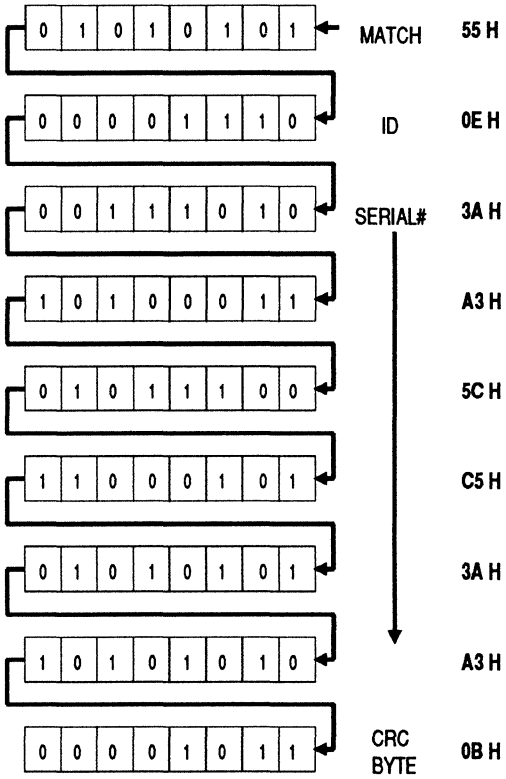
1-WIRE COMMANDS

Only the Match 1-Wire command is enabled in the DS241x. Skip, Read, Search, and Presence Detect are disabled on the DS241x for use in the Super Socket. The Match command must be sent to the Super Socket's embedded IC followed by a one-byte type ID, a six-byte fixed serial number, and a one-byte CRC. This protocol is given in Figures 5 and 6. Once the 1-Wire protocol has been established, the functions of the DS241x are available. A flow diagram for the DS131x is shown in Figure 14. Figures 15-19 are the timing diagrams for Write One, Write Zero, Read Data, Interrupt, and Reset Pulse for the 1-Wire.

DS1310 MATCH COMMAND Figure 5



DS1311 MATCH COMMAND Figure 6



COMMAND MODE

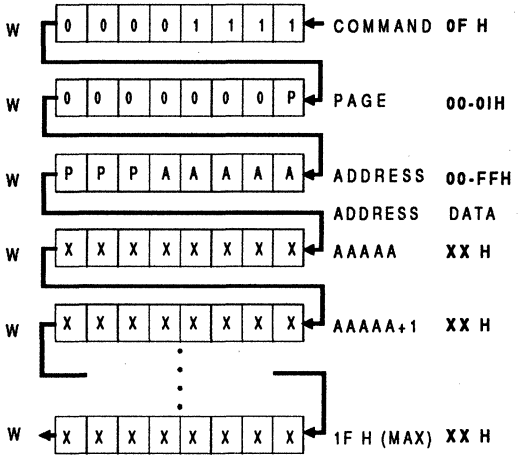
The command mode is the second layer of protocol that must be met before any data can be exchanged between the microcontroller and the Super Socket's embedded IC.

The second layer protocol consists of a command byte followed by the appropriate action. There are four valid command codes: Write Scratch, Read Scratch, Copy Scratch to Secure, and Read Secure. These commands are described separately in the following text.

WRITE SCRATCH (0Fh)

The Write Scratch command is issued by writing a 0Fh to the DS131x after the 1-Wire protocol has been established. The Write command is then followed by writing two bytes of data — the page and starting address of where the data, in the scratch page, will go in the secure memory. Data can now be written to the DS131x. The Write Scratch command is outlined in Figure 7.

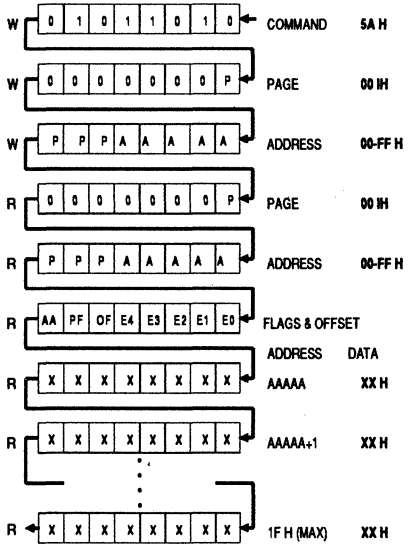
WRITE SCRATCH COMMAND Figure 7



READ SCRATCH (5Ah)

The Read Scratch command is issued by writing a 5Ah to the DS131x after the 1-Wire protocol has been established. The Read command is then followed by writing two bytes of data. These are the page and starting address of where the scratch data will go in the Secure Memory. Three bytes of data must then be read. These are the page and starting address and eight flags. (These three bytes are needed for the Copy command to move data from scratch to secure memory.) The data can now be read from the DS131x. The Read Scratch command is outlined in Figure 8.

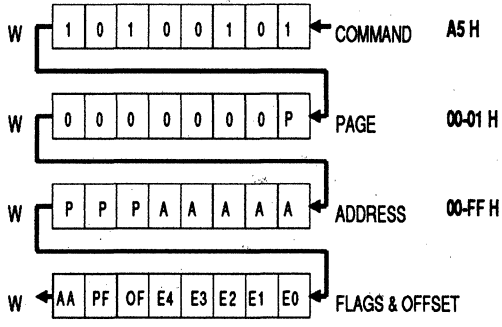
READ SCRATCH COMMAND Figure 8



COPY SCRATCH TO SECURE MEMORY (A5h)

The Copy Scratch to Secure Memory command is issued by writing a A5h to the DS131x after the 1-Wire protocol has been established. The Copy command is then followed by writing three bytes of data. These are the page and starting address and flags that were read from the Read Scratch command. After the last bit of these three bytes is received, the copy will take place using these three bytes as a starting and ending page, as well as the address of where to copy the scratch to. The Copy Scratch to Secure Memory command is outlined in Figure 9.

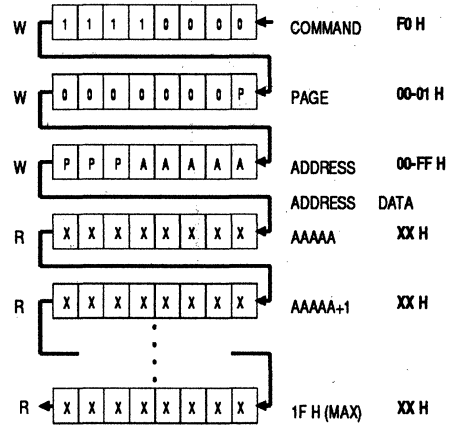
COPY SCRATCH TO SECURE MEMORY Figure 9



(F0h)

The Read Secure command is issued by writing a F0h to the DS131x after the 1-Wire protocol has been established. The read command is then followed by writing two bytes of data. These two bytes are the page and starting address of the data to be read. The data can now be read from the DS131x. The Read Secure command is outlined in Figure 10.

READ SECURE Figure 10



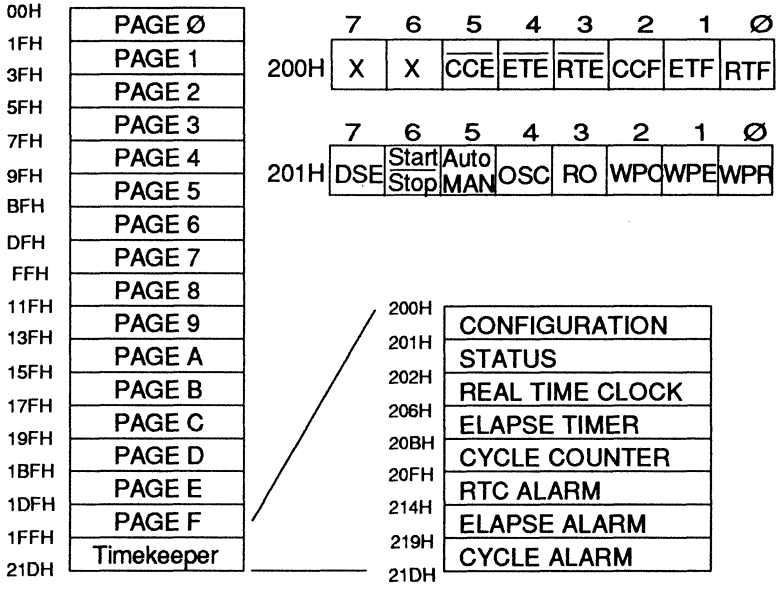
TIMEKEEPER

The timekeeper in the DS1311 is located in a special page of secure memory in the DS2414. A number of control bits are associated with this timekeeper. These are located in the first byte of the timekeeper's memory space. The control bit assignment, timekeeping memory map and data memory map are shown in Figure 11.

The timekeeper is a series of binary counters. The data in the timkeeper registers are accumulated binary counts from the time power was applied and the oscillator was turned on.

NOTE: DS1310 has only 16 pages of secure memory. There is no Timekeeping page.

RTC CONTROL REGISTER Figure 11



200 H

BIT	NAME	FUNCTION
0	RTF	Real time clock interrupt flag. When this bit is a "1" a real time alarm has occurred. This bit is cleared only after bit 0, 1 and 2 of this register are all read.
1	ETF	Elapse time interrupt flag. When this bit is a "1" an elapse time alarm has occurred. This bit is cleared only after bit 0, 1 and 2 of this register are all read.
2	CCF	Cycle counter interrupt flag. When this bit is a "1" a cycle counter alarm has occurred. This bit is cleared only after bit 0, 1 and 2 of this register are all read.
3	RTE\	Real time interrupt enable. When this bit is set to a "0" the real time alarm
4	ETE\	Real time interrupt enable. When this bit is set to a "0" the real time alarm
5	CCE\	Real time interrupt enable. When this bit is set to a "0" the real time alarm interrupt will be enabled.
6	Unused	
7	Unused	

201 H

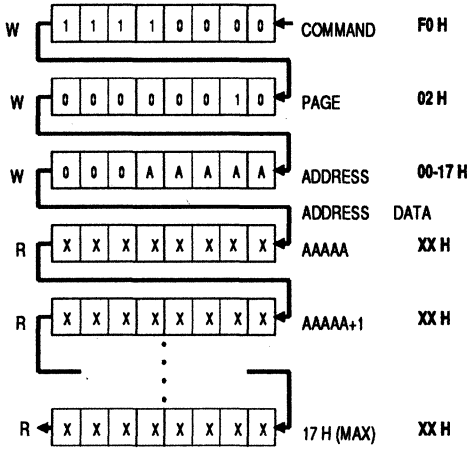
0	WPR	Permanent write protect real time clock bit. This bit if set to a "1" will write protect the real time clock and real time alarm registers permanently.
1	WPE	Permanent write protect elapse timer alarm registers permanently.
2	WPC	Permanent write protect cycle counter bit. This bit if set to a "1" will write protect the cycle counter and cycle counter alarm registers permanently.

3	RO	This bit must be set to a "1" to read data or timekeeper register if any of the write protect bits have been set.
4	OSC	This bit sets the mode of operation for the elapse timer and cycle counter. If this bit is a "0" then the clock oscillator will be stopped.
5	AUTO/ MAN\	This bit sets the mode of operation for the elapse timer and cycle counter. If this bit is set to a "1" then the elapse timer and cycle counter will increment automatically. When this bit is set to a "0" bits 6 and 7 control the elapse timer and cycle counter.
6	START/ STOP\	This bit is used to start and stop the elapse timer when bit 5 (AUTO/MAN\) is set to a "0". If this bit is set to a "1" then the elapse timer will start. If this is set to a "0" then the elapse timer will stop.
7	DSEL	This bit sets the delay for the power cycle counter. When this bit sets the delay forthe power cycle counter. When the bit is a "1" the cycle counter is incremented after 123±2mS of power up. If this bit is set to a "0" the time delay is 3.5±.

READING

The timekeeper is located in a special page of the DS2414. Reading of the timekeeper functions identically to the reading of secure memory with the exception of the special page address. An outline for reading the timekeeper is shown in Figure 12.

READ CLOCK Figure 12

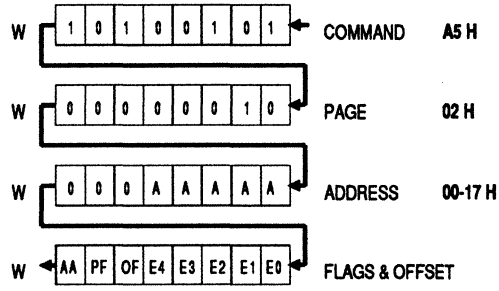


WRITING

Writing data to the timekeeper involves three steps. These steps are outlined below:

1. Write the timekeeper data to scratch memory. (See Figure 7.)
2. Read scratch memory to get offset and flags. (See Figure 8.)
3. Copy scratch to special page of secure memory (clock). (See Figure 13.)

COPY SCRATCH TO CLOCK Figure 13

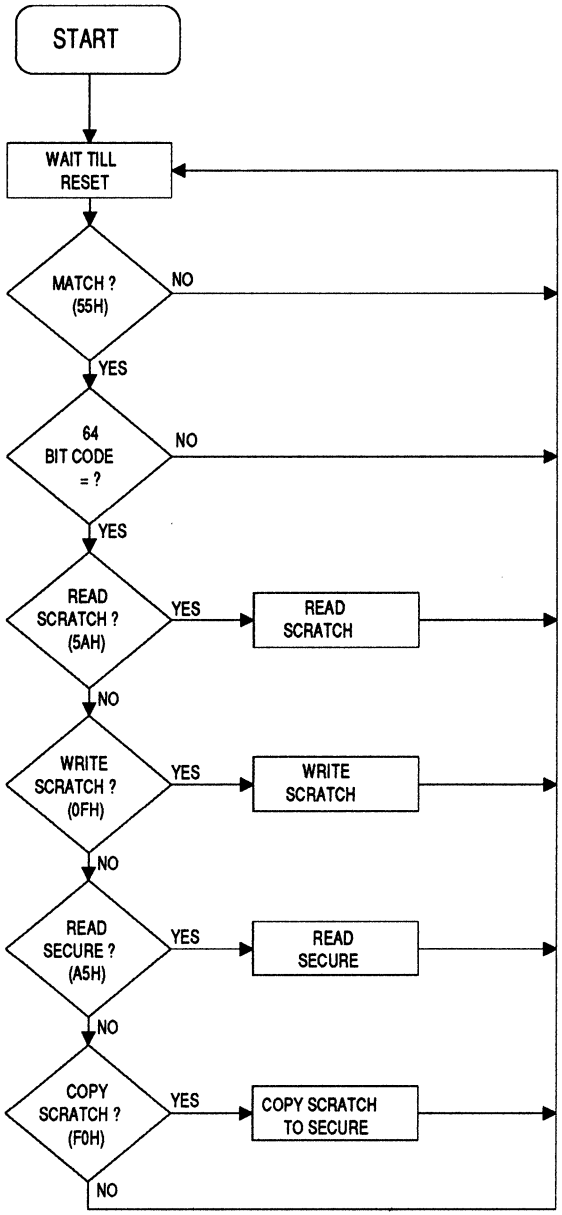


For a more detailed explanation of Read Scratch, Write Scratch, Read Secure and Copy to Secure, see the DS2403/04 data sheet.

COMMANDS

The DS131x responds to commands as shown in the flow diagram in Figure 14.

COMPATIBLE MICROCONTROLLERS Figure 14



COMPATIBLE MICROCONTROLLERS

The microcontrollers listed below are just a few of the many that can be used. If the desired microcontroller is not on this list, it can still be used if it comes in a 40-pin DIP with Vcc on pin 40 and ground on pin 20, and if it has a single bidirectional I/O pin.

P8748H	DS5000	80C31BH	8044AH	MC6805R2
P8749H	8051	80C51BHP	8344AH	MC68HC05C2
8035AHL	8052AH	87C51	8744AH	MC68HC05C3
8039AHL	8031	8752BH	MC6801	MC68HC05C4
8040AHL	8031AH	83C51FA	MC6803	MC68HC05C8
8048AH	8032AH	87C51FA	MC6801U4	MC68HC05C9
8049AH	8751	87C51FB	MC6803U4	MC68HC05T1
8050AH	8751H	83C51FB	MC6805U2	MC68HC705C8

ABSOLUTE MAXIMUM RATINGS*

Voltage in Any Pin

Relative to Ground	-1.0V to +7.0V
Operating Temperature	0° C to 70° C
Storage Temperature	-40° C to +70° C
Soldering Temperature	260° C for 10 seconds

*This is stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 40 Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1
Logic 1 PIN X	V_{IH}	2.2	V_{CC}	+0.3	V	1
Logic 0 PIN X	V_{IL}	-0.3	+0.8		V	1

DC ELECTRICAL CHARACTERISTICS

(0° C to 70° C, V_{CC}=4.75 to 5.5v)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 40 Supply Current	I_{CC}			5	mA	3
PIN X Output @ 2.4V	I_{OH}	-1.0			mA	2
PIN X Output @ 0.4V	I_{OL}		4.0		mA	2

CAPACITANCE

(Ta=25° C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance PIN X	C_{IN}	5	pF	

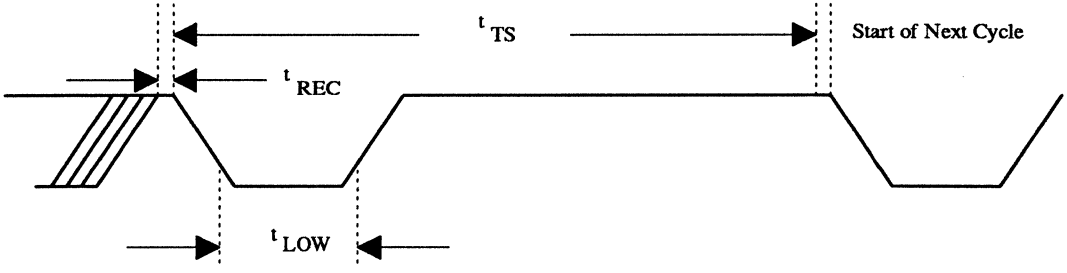
AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0° C to 70° C; V_{CC}=5.0V+/- 10%)

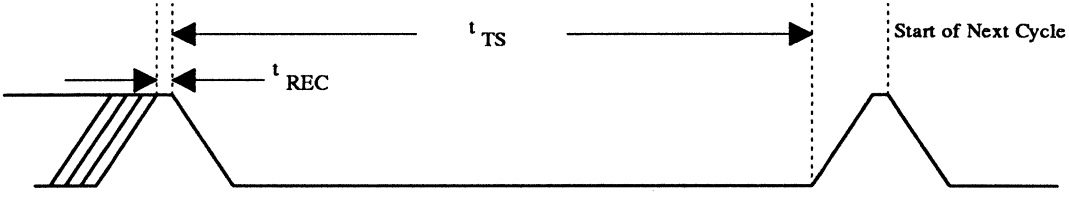
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	T_{TS}	60	120		µs	
Recovery Time	T_{REC}	1			µs	
Low Time	T_{LOW}	1	15		µs	
Reset Time High	T_{RSTH}			480	µs	
Reset Time Low	T_{RSTL}			480	µs	

5

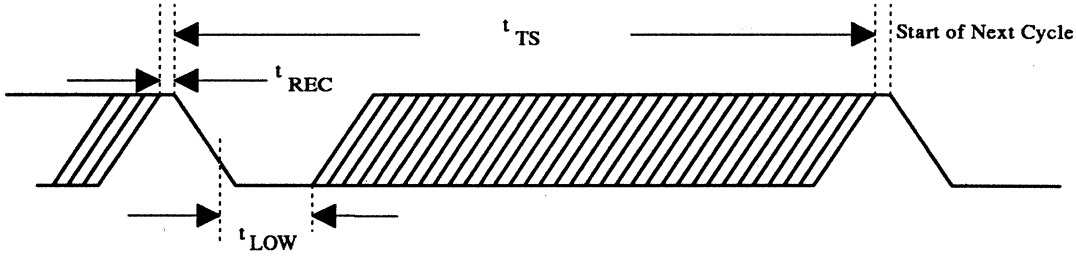
WRITE ONE TIME SLOT Figure 15



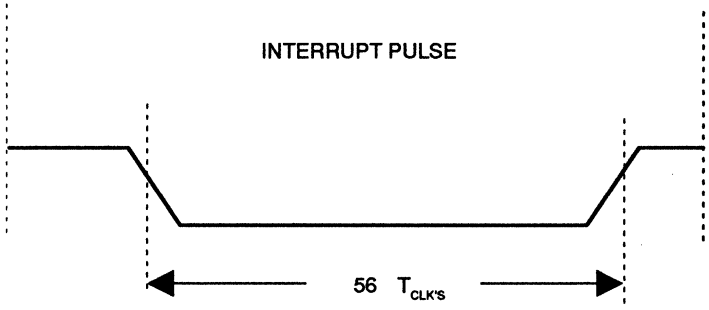
WRITE ZERO TIME SLOT Figure 16



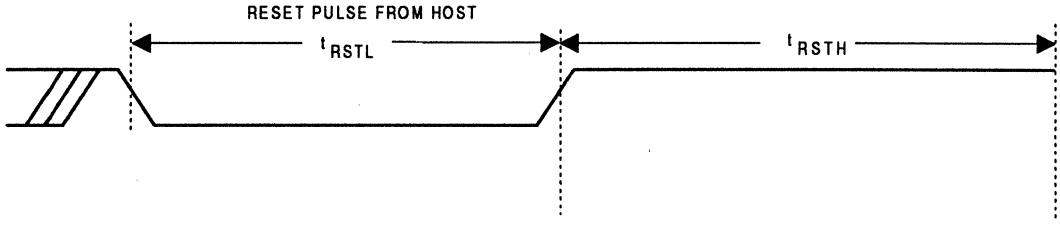
READ DATA TIME SLOTS Figure 17



INTERRUPT PULSE Figure 18



RESET PULSE Figure 19



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 17.
3. No microcontroller inserted in socket.

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

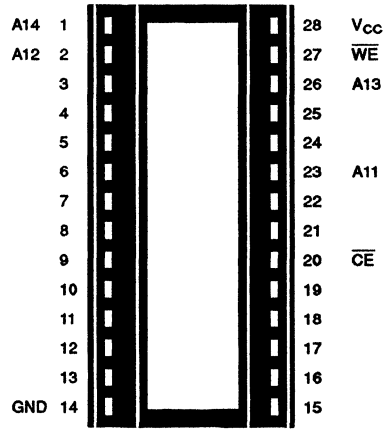
DALLAS SEMICONDUCTOR

DS1613C
Partitioned SmartSocket 256K

FEATURES

- Accepts standard 32K x 8, CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



28-PIN INTELLIGENT SOCKET

PIN DESCRIPTION

A14	-	Address 14
A12	-	Address 12
GND	-	Ground
$\overline{CE}$	-	Conditioned Chip Enable
A11	-	Address 11
A13	-	Address 13
$\overline{WE}$	-	Conditioned Write Enable
V_{CC}	-	Switched V_{CC}

All pins pass through except 20, 28, and 27.

DESCRIPTION

The DS1613C SmartSocket is a 28-pin, 0.6 inch wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts a 32K x 8 JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pins 28, 27 and 20 for RAM control. All other pins are passed straight through to the socket receptacle. Pins 1, 2, 23, and 26 are address inputs used to set memory partitions.

OPERATION

The DS1613C SmartSocket performs five circuit functions required to battery backup a CMOS memory. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power-fail detection. Power-fail detection occurs between 4.75 volts and 4.5 volts. The DS1613C constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable and write enable signals to the memory to within 0.2 volts of V_{CC} or battery supply. If the chip enable signal or write enable is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal and write enable will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. Write enable can be selectively inhibited during nominal power supply conditions by partition programming explained later. The fourth function the DS1613C performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1613C SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery backup the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mA/hr capacity, making the total 70 mA/hr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the V_{CC} pin. In order to read the cell potential, apply V_{CC} and then remove power. The cell potential will then be available on pins 28, 27 and 20.

PARTITION PROGRAMMING MODE

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11-A14. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is determined by the size of the memory. For example, a 32K x 8 memory would be divided into 16 partitions of 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1613C to inhibit $\overline{WE}$ from going low whenever A11 A12 A13 A14=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 16 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST GROUP ENTERED

5

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1, 3
Logic 0	V_{IL}	-0.3		+0.8	V	1, 3

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.75 TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
Pin 28 U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	3, 7
Pin 28 U Supply Current	I_{CCO}			150	mA	3, 7
Pin 20 L $\overline{CE}$, Pin 27 L $\overline{WE}$ Input Leakage Address A11-A14	I_{IL}	-1.0		+1.0	µA	3, 4
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 2.4V	I_{OH}	-1.0			mA	2, 3
Pin 20 U $\overline{CE}$, Pin 27 U $\overline{WE}$ Output @ 0.4V	I_{OL}			4.0	mA	2, 3
Pin 20 U Output Pin 27 U Output	V_{OLH}	V_{CC}-0.2 V_{BAT}-0.2			V	3
Pin 28 U Battery Current	I_{BAT}			1	µA	3
Pin 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance Pin 27 U, Pin 20 U	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.75 TO 5.5V)

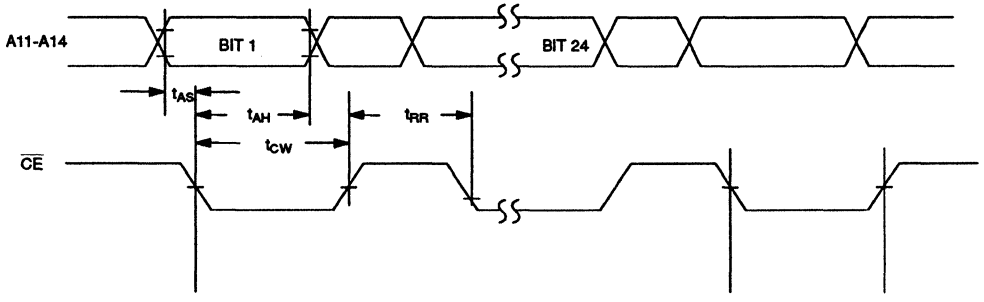
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{WE}$, $\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 8
$\overline{WE}$, $\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CCI} < 4.75V)

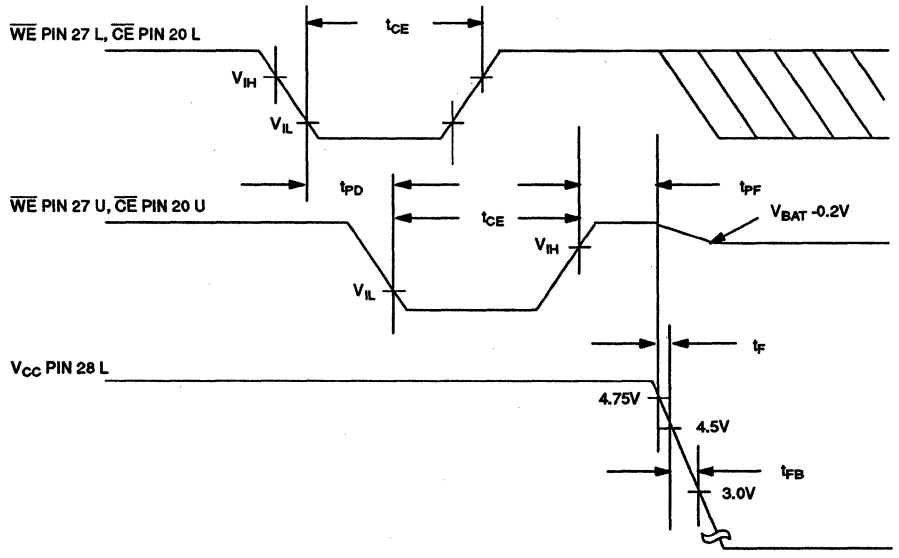
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-up	t_{REC}	25	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5V	t_F	300			µs	
V_{CC} Slew Rate 4.5 - 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.5 - 4.75V	t_R	0			µs	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	6

5

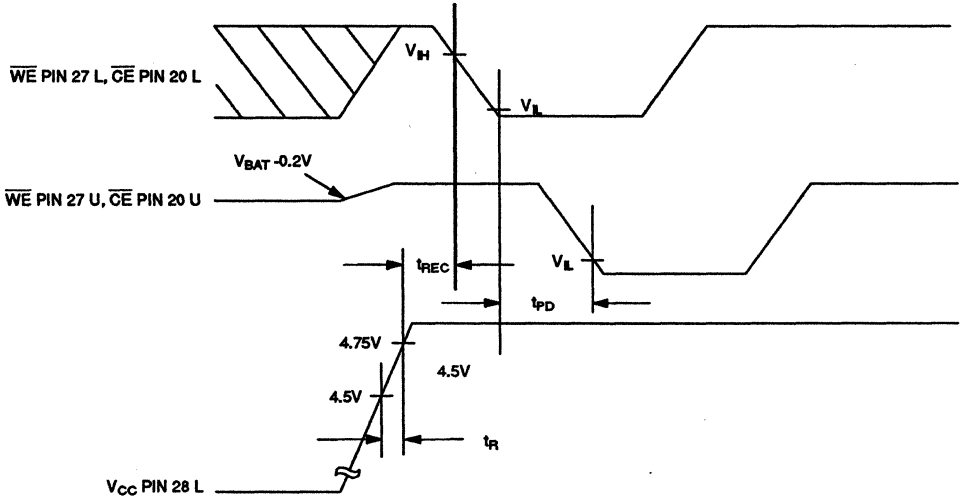
TIMING DIAGRAM: LOADING PARTITION REGISTER



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



WARNING

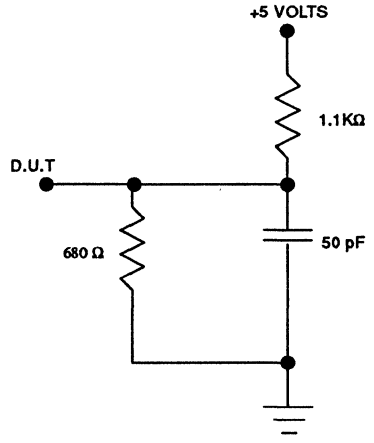
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal will discharge internal lithium source as exposed voltage pins are present.

NOTES

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
6. t_{CE} maximum must be met to ensure data integrity on power loss.
7. V_{CC} is within nominal limits and a memory is installed in the socket.
8. Input pulse rise and fall times equal 10 ns.

FIGURE 1: OUTPUT LOAD



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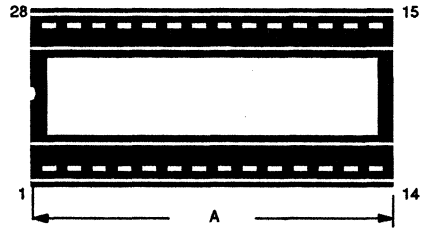
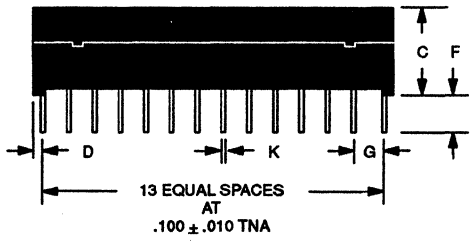
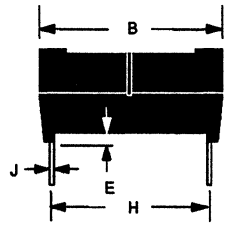
DS1613C INTELLIGENT SOCKET 28 PIN (FOR 600 MIL DIP)







PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.380	1.420
MM	35.05	36.07
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.350	0.395
MM	8.89	10.03
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

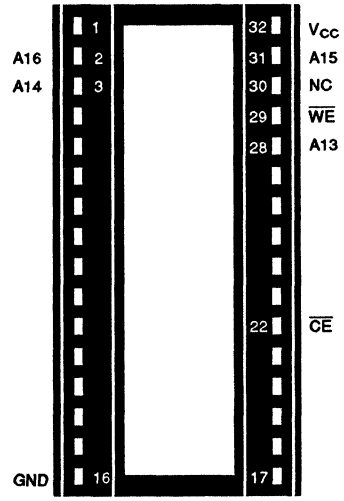
DALLAS SEMICONDUCTOR

DS1613D
Partitioned SmartSocket 1M

FEATURES

- Accepts standard 128K x 8, CMOS static RAM
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Data retention time is greater than 10 years with the proper RAM selection
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN ASSIGNMENT



32-PIN SOCKET (600 MIL)

PIN DESCRIPTION

$\overline{CE}$	-	Conditioned Chip Enable
$\overline{WE}$	-	Conditioned Write Enable
NC	-	No Connection on Socket Bottom-top Side is V_{CC}
V_{CC}	-	Switched V_{CC} for 32-pin RAM
GND	-	Ground
A13–A16	-	Address Lines

All pins pass through except 22, 29, 30 and 32.

DESCRIPTION

The DS1613D SmartSocket is a 32-pin, 0.6 inch wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts 128K x 8 byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space.

Using the SmartSocket saves printed circuit board spacing since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pin 22, 29, 30, and 32 for RAM control. All other pins are passed straight through to the socket receptacle. Pins 2, 3, 28, and 31 are address inputs used to set memory partitions.

The DS1613D is exactly the same as the DS1613C with the exceptions that the DS1613D has 32 pins and the DS1613C is 28 pins and the address and control signals are on different pin numbers and locations. The upper order address lines used to set the memory partitions also differ because of the density of RAM for the SmartSocket. Tables 1 and 2 illustrate the pattern match required for partitioning of the DS1613D. See the DS1613C data for all additional technical details and specifications.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

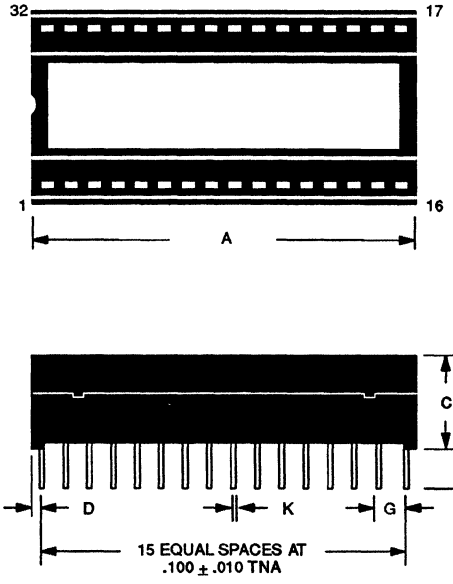
FIRST BITS ENTERED

LAST GROUP ENTERED

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{16} A_{15} A_{14} A_{13})
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

DS1613D INTELLIGENT SOCKET 32 PIN (FOR 600 MIL DIP)



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.580	1.620
MM	40.13	41.15
B IN.	0.690	0.720
MM	17.53	18.29
C IN.	0.350	0.410
MM	8.89	10.40
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.015	0.035
MM	0.39	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

5

	Type of Interface	Product Name and Number	NV SRAM Bytes	Cycle Times	Special Features
TIMEKEEPERS >10 years of lithium and +/- 1 minute\month. Quartz. U.L. listed.	Multiplexed Address/Data Bus	Real Time Clock DS1287	50	385ns	Replaces MC 146818A; MS-DOS compatible; programmable interrupts, square wave output. DS13XX, DS14XX, and DS15XX meet MCA and EISA NVRAM requirements. DS1587 includes silicon serial number.
		RAMified Real Time Clock DS1387, DS1397	4K		
		RAMified Real Time Clock DS1488, DS1497, DS1587	8K		
	Parallel Interface	Watchdog Timekeeper DS1286	50	150ns	CPU watchdog; programmable interrupts; square wave output; wake up interrupts.
		RAMified Watchdog Timekeeper DS1386-8, DS1386-32, DS1486	8K/32K/128K	120ns, 150ns	
	Bytewide SRAM Bus	NV Timekeeper RAM DS1642, DS1643, and DS1644	2K/8K/32K	120ns, 150ns	PIN compatible with MK48T02 and MK48T08. JEDEC bytewide RAM pin compatible.
	Conventional Bytewide SRAM and EPROM Bus with Phantom Interface	SmartWatch/RAM DS1216B, C, D	2K→ 512K		Timekeeper built into a socket; mated SRAM converts to NVRAM.
		SmartWatch/ROM DS1216E, F	(EPROM) 8K→ 512K		
		NV SRAM with Phantom Clock DS1243Y, DS1244Y, DS1248Y	8K/32K/128K	120ns, 150ns, 200ns	NV SRAM packaged with timekeeper.
	Serial Interface	Elapsed Time Counter DS1603	No RAM		Vcc active counter and continuous counter.
CHIPS Add Lithium and Quartz for Time and NV SRAM.	Multiplexed Address/Data Bus	Real Time Clock Chip DS1285	50	385ns	Replaces MC 146818A, MS-DOS compatible; programmable interrupts; square wave output. Meets MCA and EISA NVRAM requirements. DS1585 includes silicon serial number.
		RAMified Real Time Clock Chip DS1385, DS1395	4K		
		RAMifiedReal Time DS1485, DS1585	8K		
	Parallel Interface	Watchdog Timekeeper Chip DS1283, DS1284	50	150ns	Programmable interrupts; square wave output. DS1284 provides battery backup circuitry for SRAM. DS1283 provides 2.5 -5.5 volt operation.
	Conventional Bytewide SRAM and EPROM Bus Controller with Phantom Interface	Phantom Time Chip DS1215	external		Battery backup circuitry for SRAM. Add-in real time clock uses same SRAM/EPROM signals.
	3-Wire Serial Interface	Serial Timekeeper Chip DS1202	24		2.0-5.5 volt operation; serial I/O for minimum pin count.
		Elapsed Time Counter Chip DS1602	No RAM		Vcc active counter and continuous counter.
	3-Wire or 1-Wire Serial Interface	EconoRAM Time Chip DS2404	512		Time of day, elapsed time, power on cycle counter, silicon number.

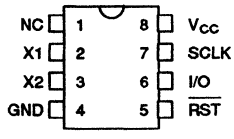
DALLAS SEMICONDUCTOR

DS1202, DS1202S
Serial Timekeeping Chip

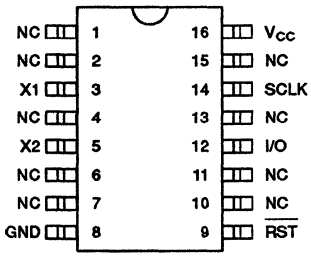
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0-5.5 volt full operation
- Uses less than 300 nA at 2 volts
- Single-byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL-compatible (V_{CC} = 5V)
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



8 PIN DIP



16-PIN SOIC

PIN DESCRIPTION

NC	-	No Connection
X1, X2	-	32.768 kHz Crystal Input
GND	-	Ground
$\overline{RST}$	-	Reset
I/O	-	Data Input/Output
SCLK	-	Serial Clock
V_{CC}	-	Power Supply Pin

DESCRIPTION

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

OPERATION

The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is zero, further action will be terminated. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

FIGURE 1: DS1202 BLOCK DIAGRAM

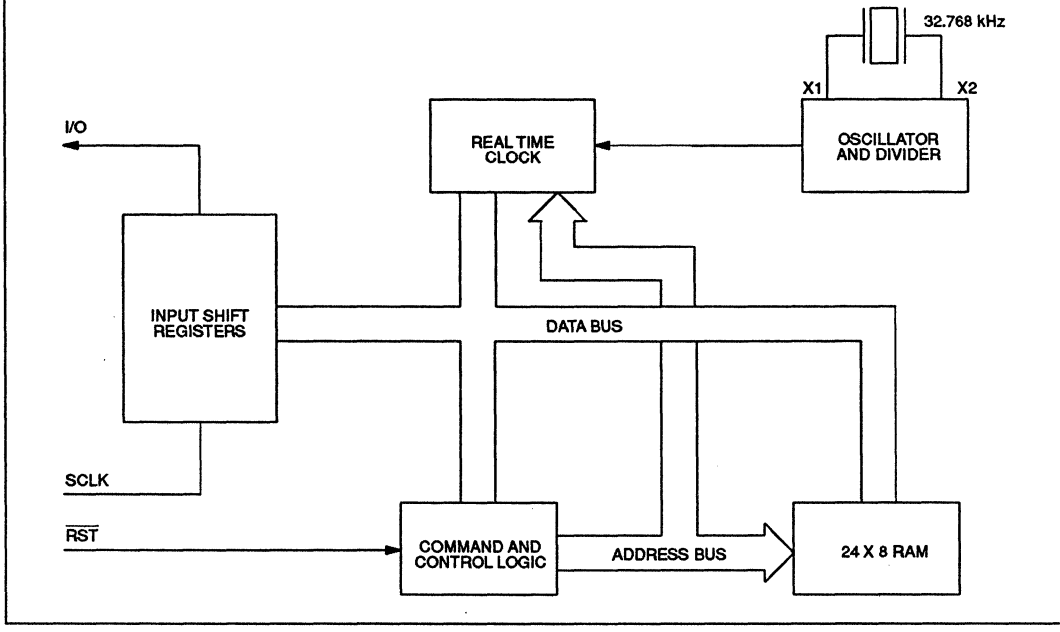
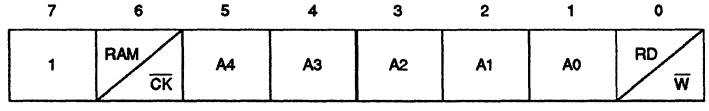


FIGURE 2: ADDRESS/COMMAND BYTE



RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on t he falling edge of clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specified clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM registers.

CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1202 is placed into a low-power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic 0, the clock will start.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

WRITE PROTECT REGISTER

Bit 7 of write protect register is the write protect bit. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

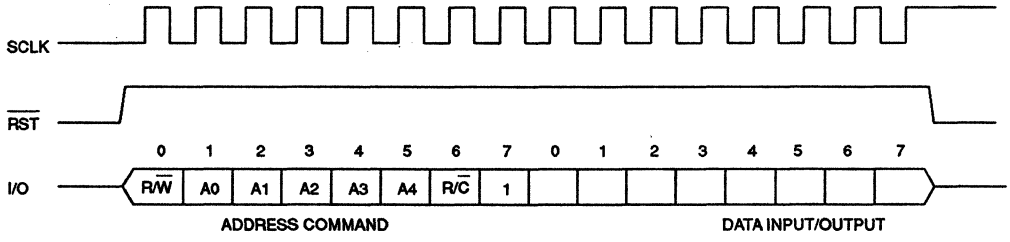
A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

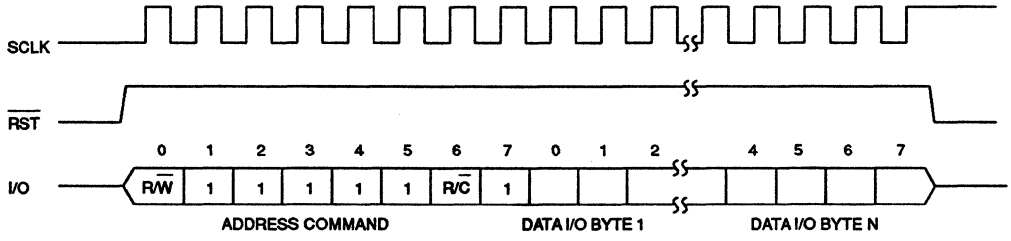
A 32.768 kHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

FIGURE 3: DATA TRANSFER SUMMARY

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

FIGURE 4: REGISTER ADDRESS/DEFINITION

REGISTER ADDRESS
A. CLOCK

	7	6	5	4	3	2	1	0
SEC	1	0	0	0	0	0	0	RD/$\overline{W}$
MIN	1	0	0	0	0	0	1	RD/$\overline{W}$
HR	1	0	0	0	0	1	0	RD/$\overline{W}$
DATE	1	0	0	0	0	1	1	RD/$\overline{W}$
MONTH	1	0	0	0	1	0	0	RD/$\overline{W}$
DAY	1	0	0	0	1	0	1	RD/$\overline{W}$
YEAR	1	0	0	0	1	1	0	RD/$\overline{W}$
CONTROL	1	0	0	0	1	1	1	RD/$\overline{W}$
CLOCK BURST	1	0	1	1	1	1	1	RD/$\overline{W}$

REGISTER DEFINITION

00–59	CH	10 SEC				SEC
00–59	0	10 MIN				MIN
01–12 00–23	12/24	0	10 A/P	HR		HR
01–28/29 01–30 01–31	0	0	10 DATE			DATE
01–12	0	0	0	10 M		MONTH
01–07	0	0	0	0	0	DAY
0–99	10 YEAR					YEAR
	WP	FORCED TO ZERO				

B. RAM

RAM 0	1	1	0	0	0	0	0	RD/$\overline{W}$
RAM 23	1	1	1	0	1	1	1	RD/$\overline{W}$
RAM BURST	1	1	1	1	1	1	1	RD/$\overline{W}$

RAM DATA 0								
RAM DATA 23								

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO +7.0V
OPERATING TEMPERATURE	0°C TO +70°C
STORAGE TEMPERATURE	-55°C TO +125°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.0		5.5	V	1
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.0V	–0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		

DC ELECTRICAL CHARACTERISTICS (0°C TO +70°C, V_{CC} = 2.0 TO 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	6
I/O Leakage	I_{LO}				+500	µA	6
Logic 1 Output	V_{OH}	V_{CC}=2V	1.6			V	2
		V_{CC}=5V	2.4				
Logic 0 Output	V_{OL}	V_{CC}=2V			0.4	V	3
		V_{CC}=5V			0.4		
Active Supply Current	I_{CC}	V_{CC}=2V			.4	mA	5
		V_{CC}=5V			1.2		
Timekeeping Current	I_{CC1}	V_{CC}=2V			0.3	µA	4
		V_{CC}=5V			1		
Leakage Current	I_{CC2}	V_{CC}=2V			100	nA	10
		V_{CC}=5V			100		

*Unless otherwise noted.

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = +5V + 10%*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2V	200			ns	7
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2V	280			ns	7
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2V			800	ns	7, 8, 9
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2V	1000			ns	7
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2V	1000			ns	7, 12
		V_{CC}=5V	250				
CLK Frequency	t_{CLK}	V_{CC}=2V			0.5	MHz	7, 12
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2V			2000	ns	
		V_{CC}=5V			500		
RST to CLK Setup	t_{CC}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
CLK to RST Hold	t_{CCH}	V_{CC}=2V	240			ns	7
		V_{CC}=5V	60				
RST Inactive Time	t_{CWH}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
RST to I/O High Z	t_{CDZ}	V_{CC}=2V			280	ns	7
		V_{CC}=5V			70		

*Unless otherwise noted.

FIGURE 5: TIMING DIAGRAM: READ DATA TRANSFER

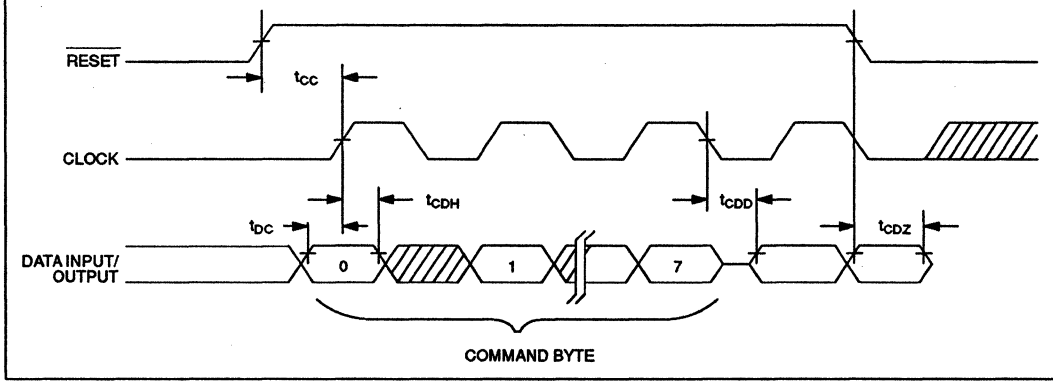
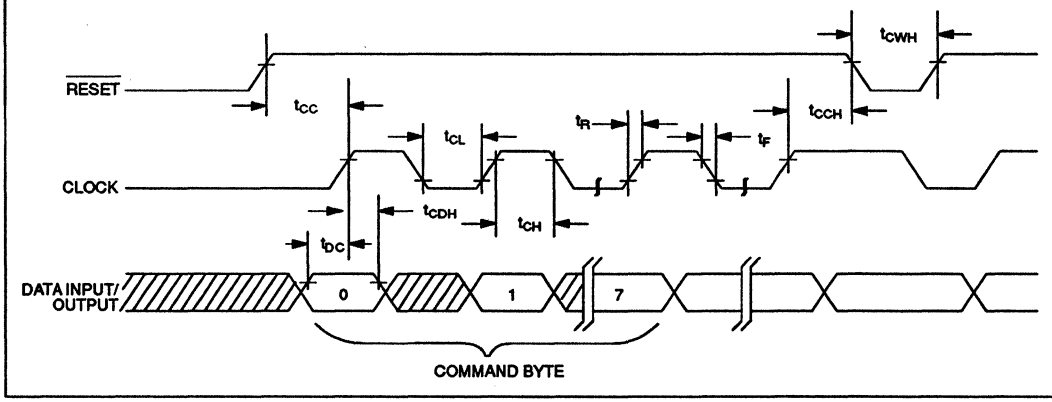


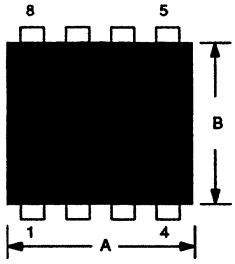
FIGURE 6: TIMING DIAGRAM: WRITE DATA TRANSFER

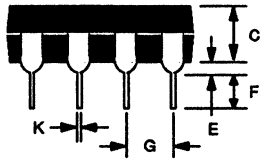


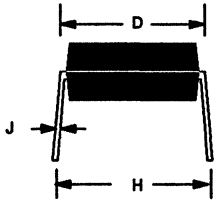
NOTES

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and .4 mA at V_{CC}=2V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2V.
4. I_{CC1} is specified with I/O open, $\overline{RST}$ set to a logic 0, and clock halt flag=0 (oscillator enabled).
5. I_{CC} is specified with the I/O pin open, $\overline{RST}$ high, SCLK=2 MHz at V_{CC}=5V; SCLK=500 kHz, V_{CC}=2V and clock halt flag=0 (oscillator enabled).
6. $\overline{RST}$, SCLK, and I/O all have 40KΩ pulldown resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50 pF.
10. I_{CC2} is specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
11. At power-up, $\overline{RST}$ must be at a logic 0 until $V_{CC} \geq 2$ volts. Also, SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic one state.
12. If t_{CH} exceeds 100 ms with $\overline{RST}$ in a logic one state, then I_{CC} may briefly exceed I_{CC} specification.

DS1202 SERIAL TIMEKEEPER 8 PIN DIP



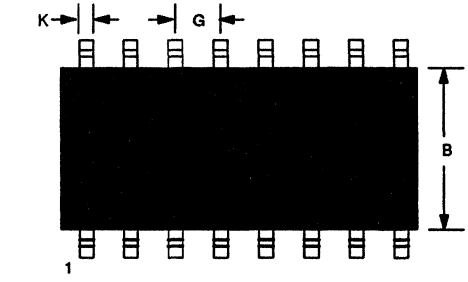


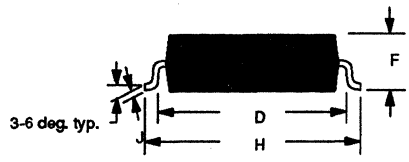


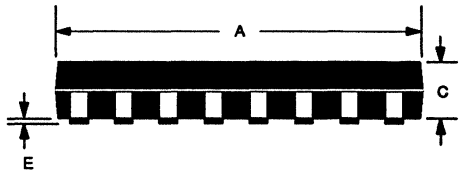
PKG	8–PIN	
DIM	**MIN**	**MAX**
A IN. MM	.360	.400
B IN. MM	.240	.260
C IN. MM	.120	.140
D IN. MM	.300	.325
E IN. MM	.015	.040
F IN. MM	.110	.135
G IN. MM	.090	.110
H IN. MM	.320	.370
J IN. MM	.008	.012
K IN. MM	.015	.021

6

DS1202S SERIAL TIMEKEEPER 16 PIN SOIC







PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	.402	.412
B IN. MM	.292 .	.299
C IN. MM	.090	.100
D IN. MM	.320	.384
E IN. MM	.004	.012
F IN. MM	.097	.105
G IN. MM	.046	.054
H IN. MM	.398	.416
J IN. MM	.009	.013
K IN. MM	.013	.019

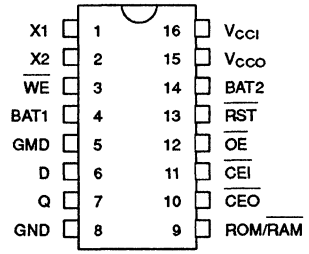
DALLAS SEMICONDUCTOR

DS1215
Phantom Time Chip

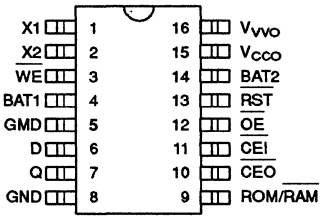
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-reliability applications
- Uses a 32.768 kHz watch crystal
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Space-saving, 16-pin DIP package and SOIC

PIN ASSIGNMENT



16–PIN DIP (300 MIL)



16–PIN SOIC (300 MIL)

PIN DESCRIPTION

X1, X2	-	32.768 kHz Crystal Connections
$\overline{WE}$	-	Write Enable
BAT1	-	Battery 1 Input
GND	-	Ground
D	-	Data In
Q	-	Data Out
ROM/$\overline{RAM}$	-	ROM/RAM Select
$\overline{CEO}$	-	Chip Enable Out
$\overline{CEI}$	-	Chip Enable Input
$\overline{OE}$	-	Output Enable
$\overline{RST}$	-	Reset
BAT2	-	Battery 2 Input
V_{CCO}	-	Switched Supply Output
V_{CCI}	-	+5 VDC Input

NOTE: Both pins 5 and 8 must be grounded.

DESCRIPTION

The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour

mode with an AM/PM indicator or a 24-hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

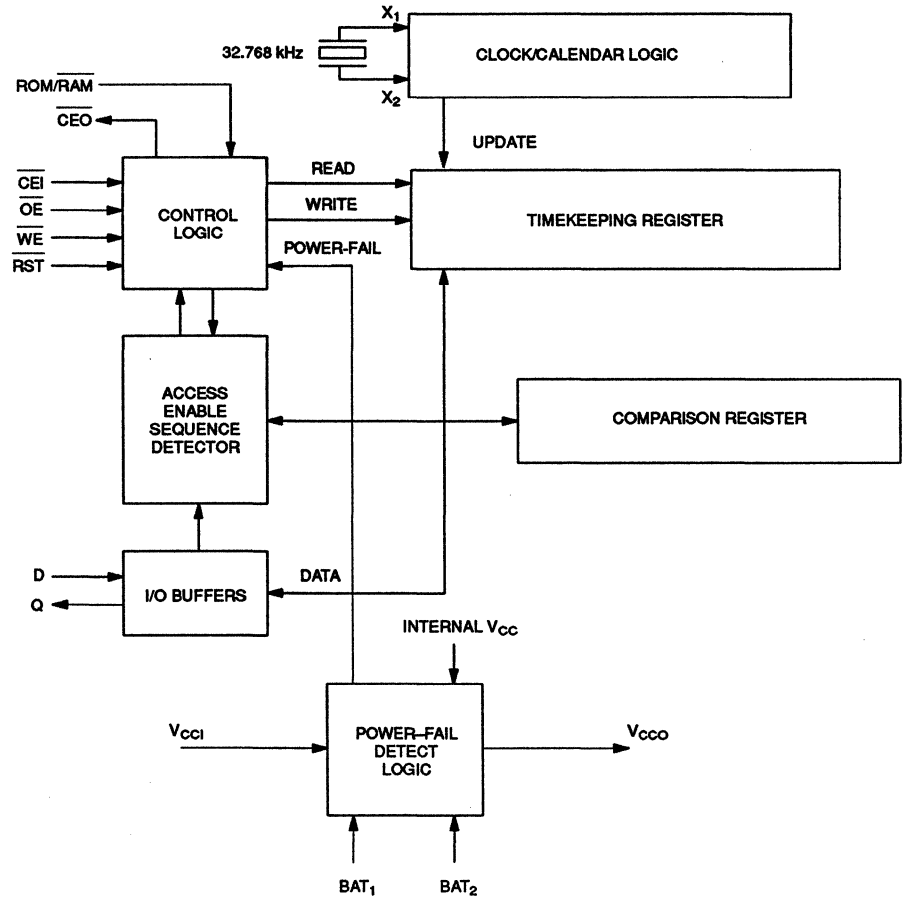
OPERATION

The block diagram of Figure 1 illustrates the main elements of the Time Chip. Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and $\overline{CEO}$ remains high during this time, disabling the connected memory.

Data transfer to an from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the Time Chip starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.

FIGURE 1: TIMING BLOCK DIAGRAM



When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2.) With a correct match for 64 bits, the Time Chip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE1}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A 32,768 Hz quartz crystal, Seiko part no. DS-VT-200 or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF.

FIGURE 2: TIME CHIP COMPARISON REGISTER DEFINITION

	7	6	5	4	3	2	1	0	HEX VALUE
BYTE 0	1	1	0	0	0	1	0	1	C5
BYTE 1	0	0	1	1	1	0	1	0	3A
BYTE 2	1	0	1	0	0	0	1	1	A3
BYTE 3	0	1	0	1	1	1	0	0	5C
BYTE 4	1	1	0	0	0	1	0	1	C5
BYTE 5	0	0	1	1	1	0	1	0	3A
BYTE 6	1	0	1	0	0	0	1	1	A3
BYTE 7	0	1	0	1	1	1	0	0	5C

NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in 10^{19}.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below VTP, which is equal to 1.26 x V_{BAT}. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 20ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/$\overline{\text{RAM}}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force $\overline{\text{CEO}}$ high when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/Time Chip interface is illustrated in Figure 4.

TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping though all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 -23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

FIGURE 3: RAM/TIME CHIP INTERFACE

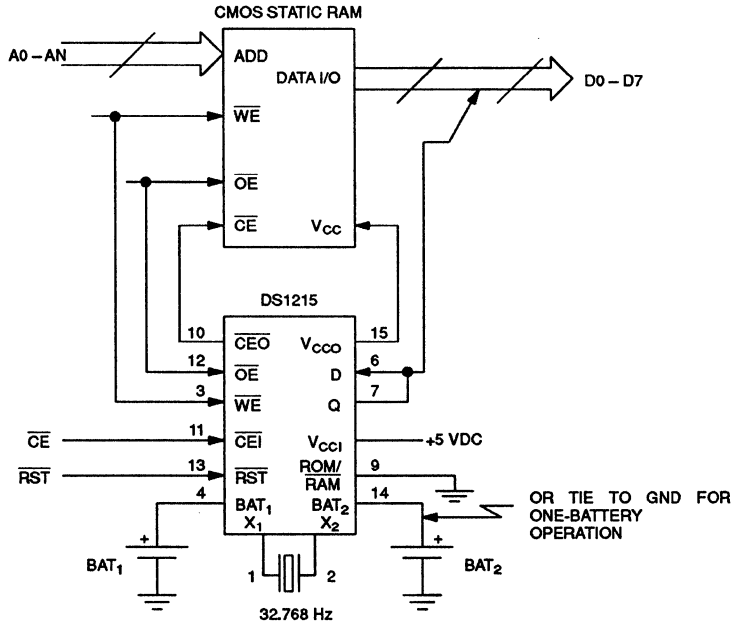


FIGURE 4: ROM/TIME CHIP INTERFACE

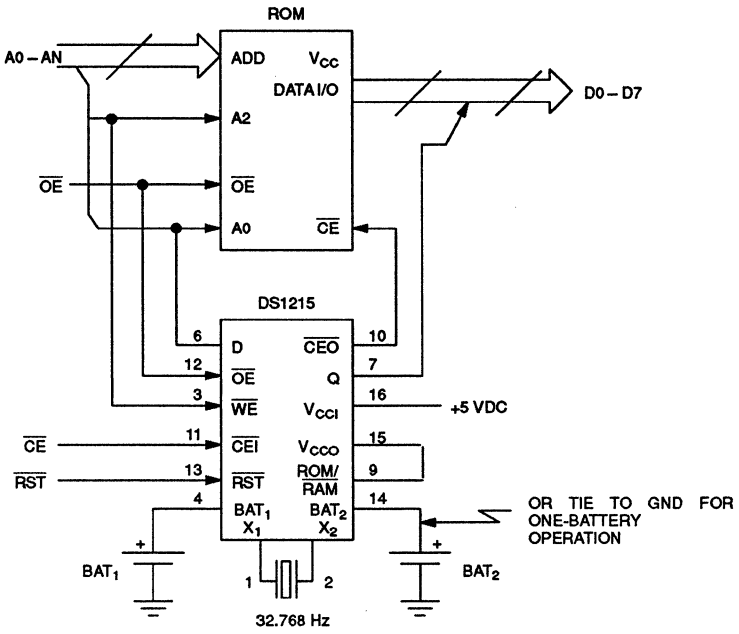
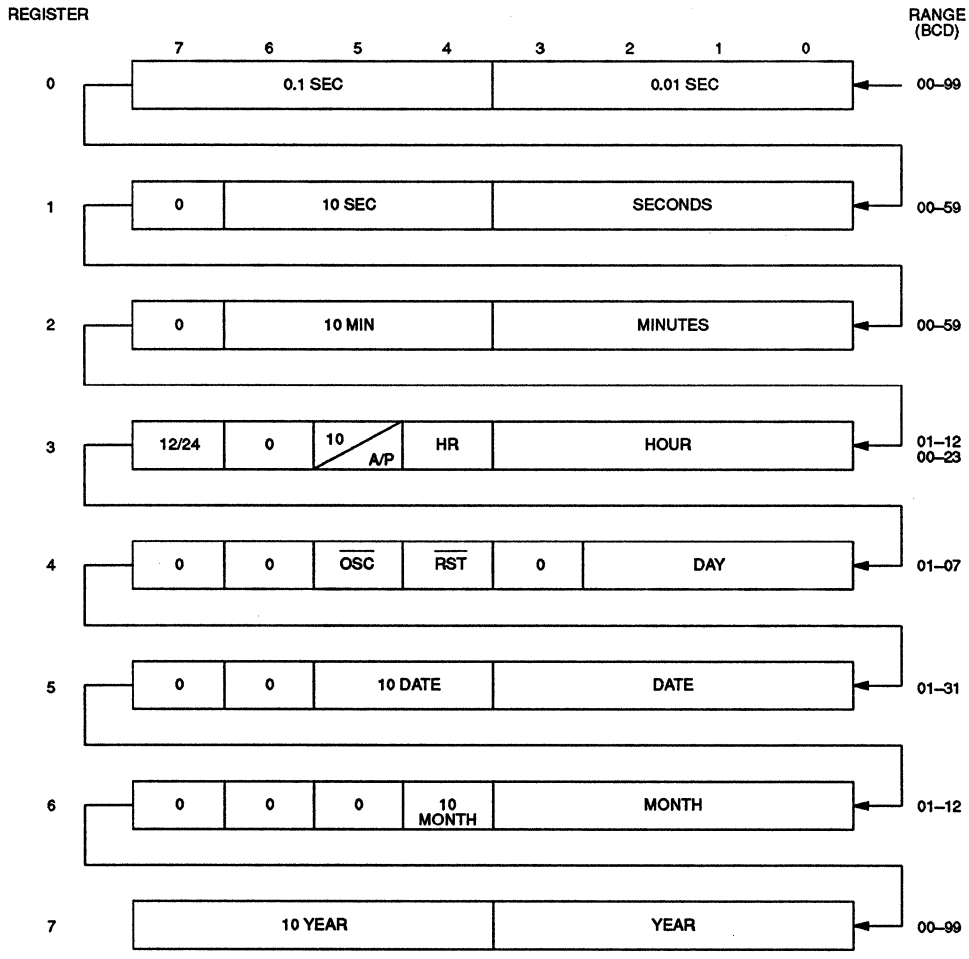


FIGURE 5: TIME CHIP REGISTER DEFINITION



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-55°C TO +125°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3		1
Logic 0	V_{IL}	-0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 4.5 TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO} = V_{CCI}$-0.3	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	-1.0		+1.0	µA	11
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OH1}	V_{CCI} or V_{BAT}-0.2			V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			1	µA	6
Battery Backup Current @ $V_{CCO} = V_{BAT}$-0.2V	I_{CCO2}			10	µA	10

AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = GND (0°C, V_{CC} = 4.5 TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE1}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE1}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE1}$ to Output High Z	t_{OD}			40	ns	
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup	t_{DS}	40			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{CE1}$ Pulse Width	t_{CW}	100			ns	
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE1}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{CE1}$ High to Power-Fail	t_{PF}			0	ns	

AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = GND (0°C TO 70°C, V_{CC} > 4.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

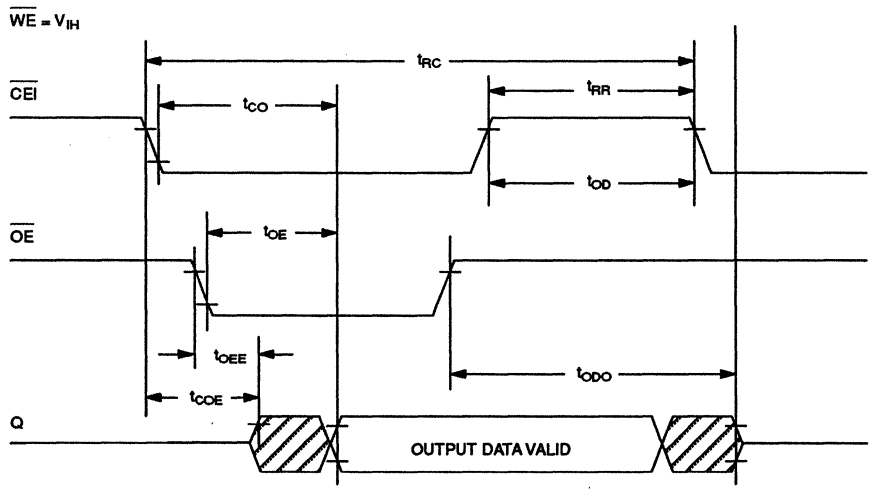
CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = V_{CCO} (0°C TO 70°C; V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output in High Z	t_{OD}			40	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			40	ns	
Address Setup Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{OE}$ Pulse Width	t_{OW}	100			ns	
Write Recovery	t_{WR}	20			ns	4
Data Setup Time	t_{DS}	40			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

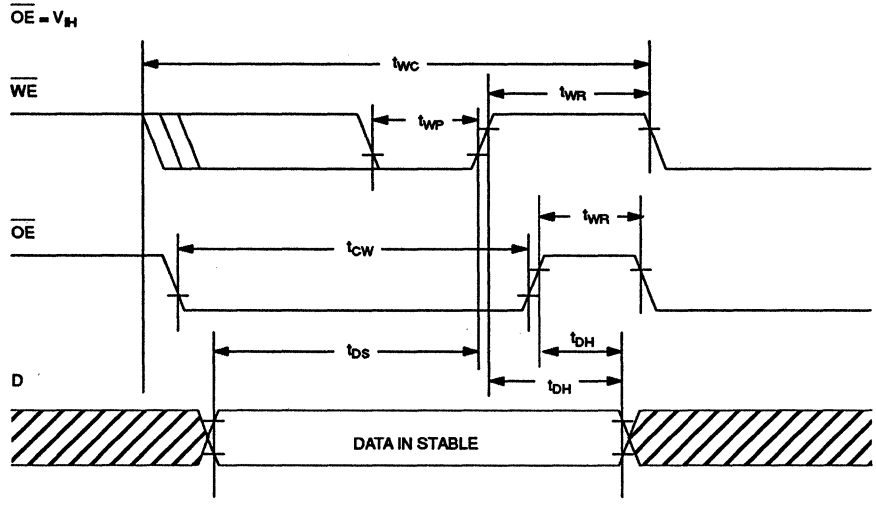
AC ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = V_{CCO} (0°C TO 70°C; V_{CC} < 4.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

6

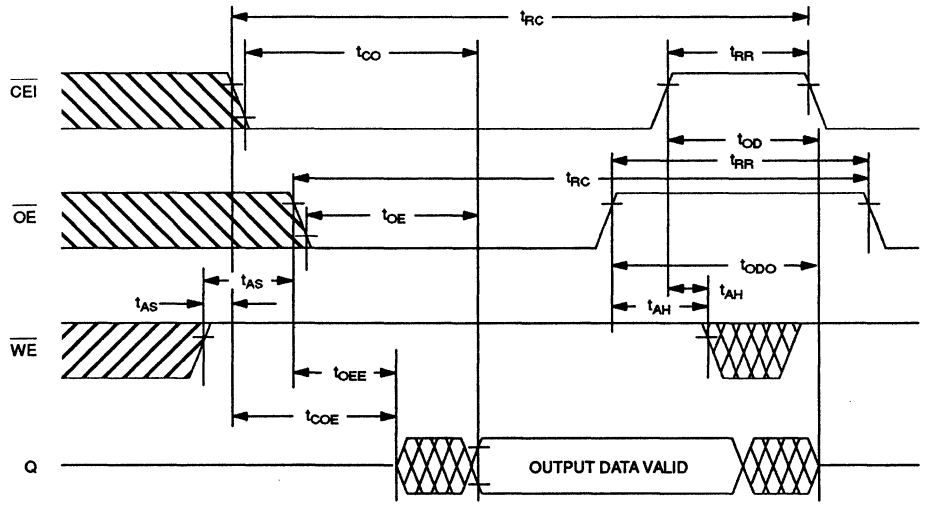
TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/$\overline{RAM}$ = GND



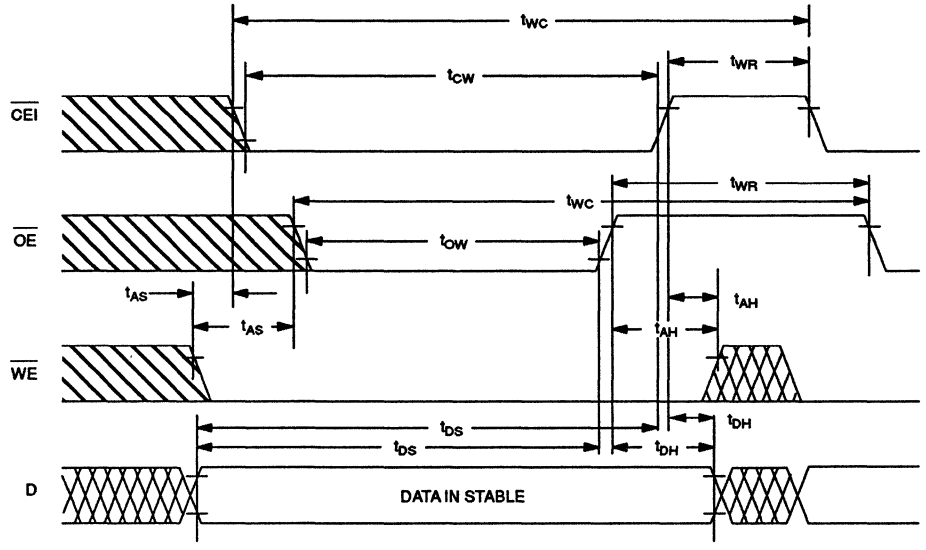
TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/$\overline{RAM}$ = GND



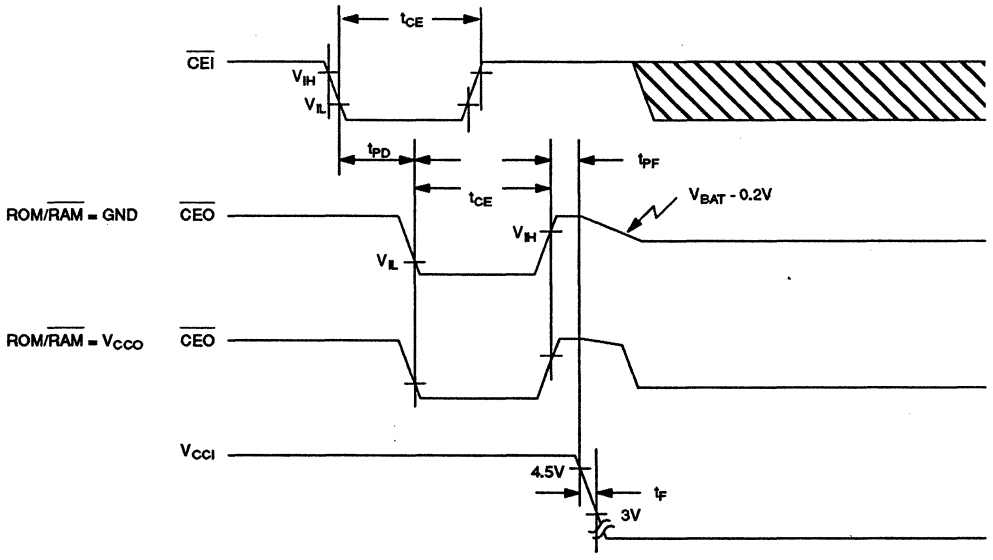
TIMING DIAGRAM: READ CYCLE ROM/$\overline{RAM}$ = V_{CCO}



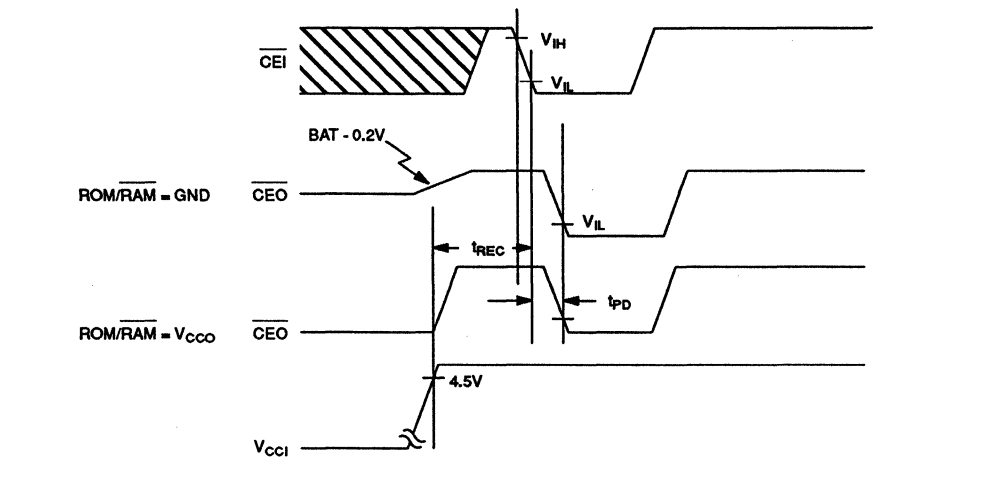
TIMING DIAGRAM: WRITE CYCLE ROM/$\overline{RAM}$ = V_{CCO}



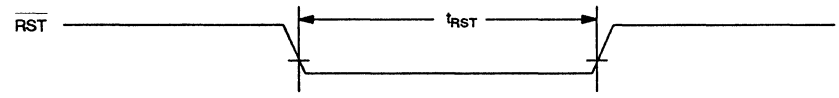
TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



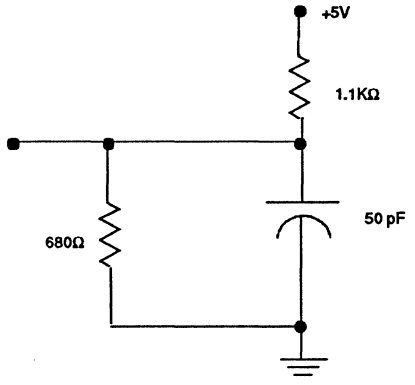
TIMING DIAGRAM: RESET FOR TIME CHIP



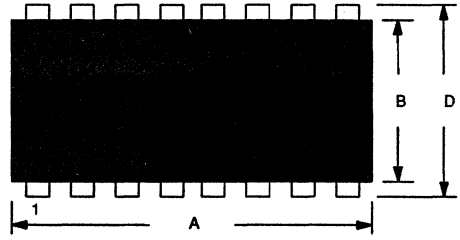
NOTES

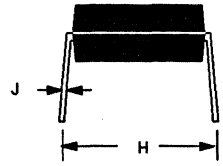
1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode, or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power-fail detect. V_{TP} = 1.26 x V_{BAT}. For 10% V_{CC}= 5V + 10% operation V_{BAT} = 3.5V max.; for 5% operation V_{BAT} = 3.7V max.
8. I_{CC01} is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CC02} is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

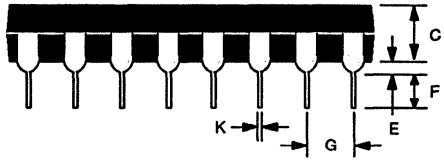
FIGURE 6: OUTPUT LOAD



DS1215 TIME CHIP







PKG	16-PIN	
DIM	**MIN**	**MAX**
A IN. MM	.740	.780
B IN. MM	.240	.260
C IN. MM	.120	.140
D IN. MM	.300	.325
E IN. MM	.015	.040
F IN. MM	.110	.140
G IN. MM	.090	.110
H IN. MM	.300	.370
J IN. MM	.008	.012
K IN. MM	.015	.021

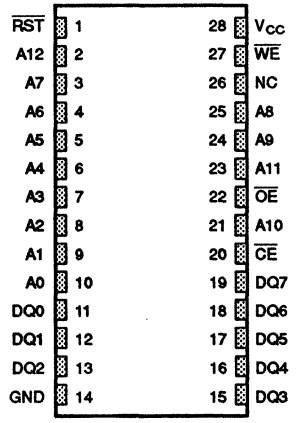
DALLAS SEMICONDUCTOR

DS1243Y
64K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 8K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 200 ns access time

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
(720 MIL EXTENDED)

PIN DESCRIPTION

A_0-A_{12}	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ_0-DQ_7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect
$\overline{RST}$	-	Reset

DESCRIPTION

The DS1243Y 64K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with a built-in real time clock. The DS1243Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1243Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1243Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1243Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

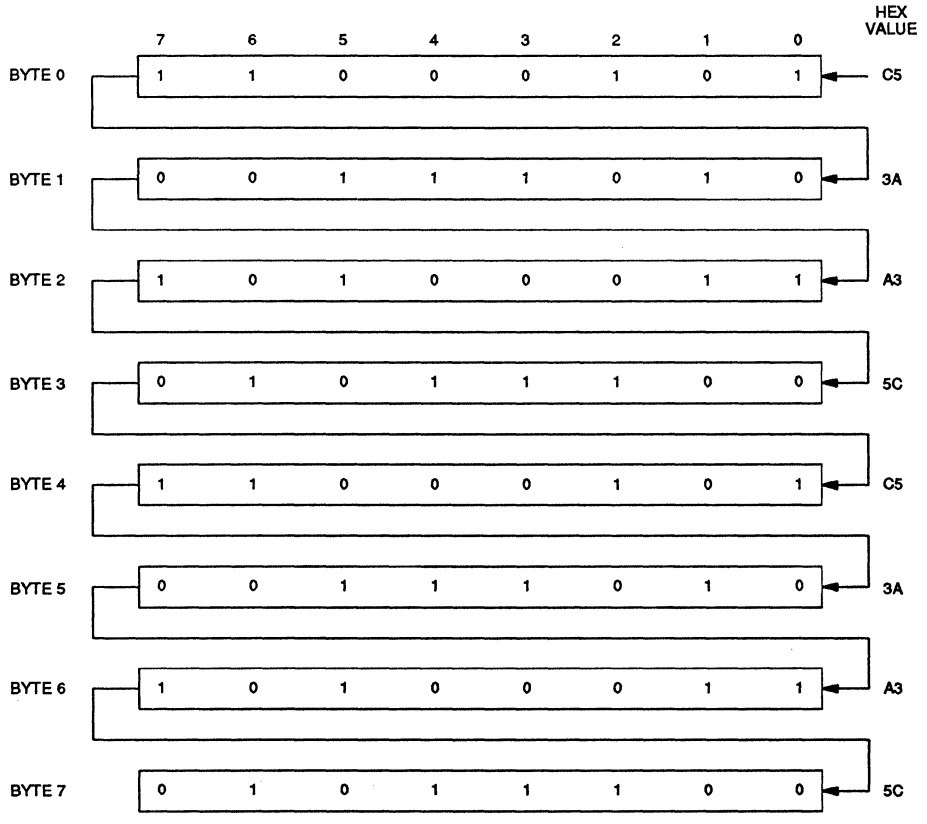
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

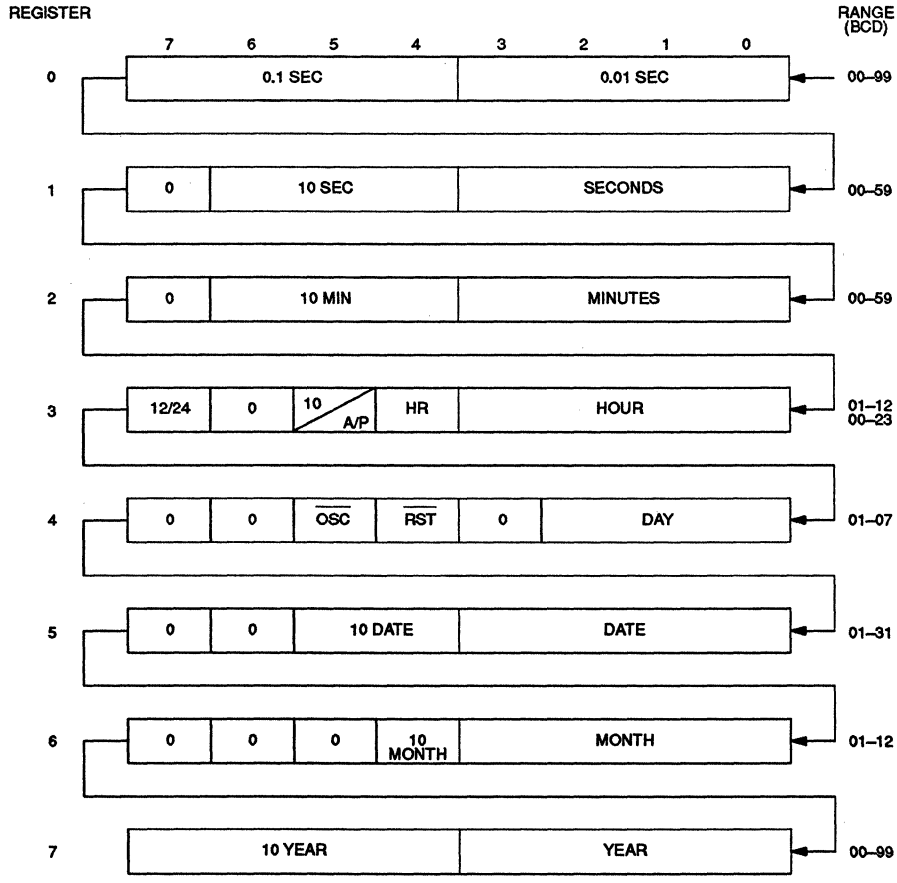
FIGURE 1: PHANTOM CLOCK REGISTER DEFINITION



NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

FIGURE 2: PHANTOM CLOCK REGISTER DEFINITION



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO 7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-55°C TO 125°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5.0V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	200			ns	
Access Time	t_{ACC}			200	ns	
$\overline{OE}$ to Output Valid	t_{OE}			100	ns	
$\overline{CE}$ to Output Valid	t_{CO}			200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Output High Z from Deselection	t_{OD}			100	ns	5
Output Hold from Address Change	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	200			ns	
Write Pulse Width	t_{WP}	150			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z from $\overline{WE}$	t_{ODW}			80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	80			ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20			ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

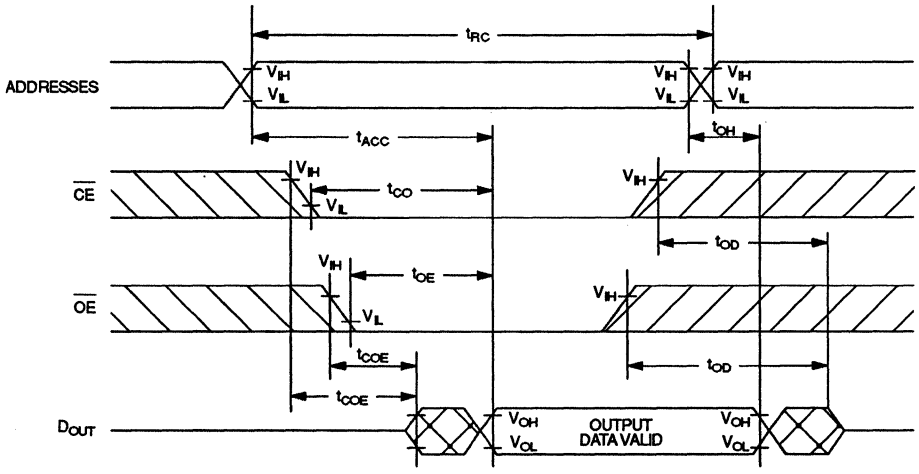
POWER-DOWN/POWER-UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

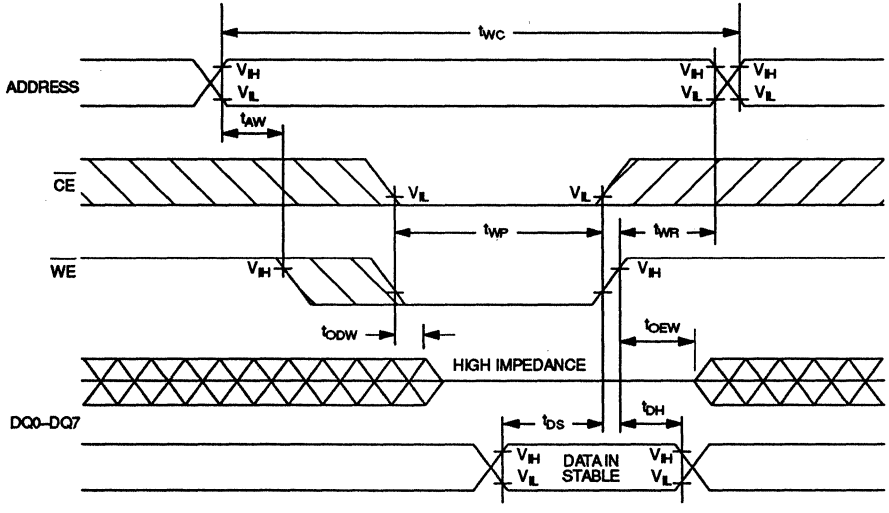
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

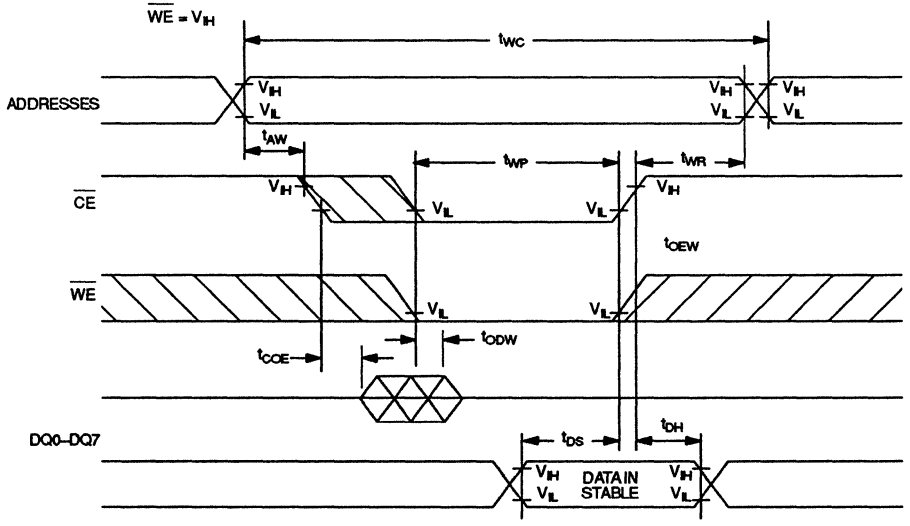
MEMORY READ CYCLE (NOTE 1)



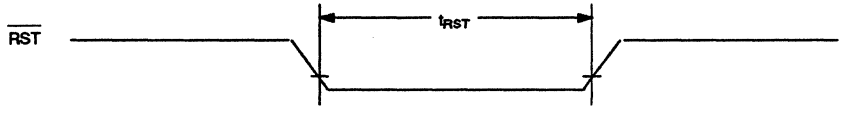
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



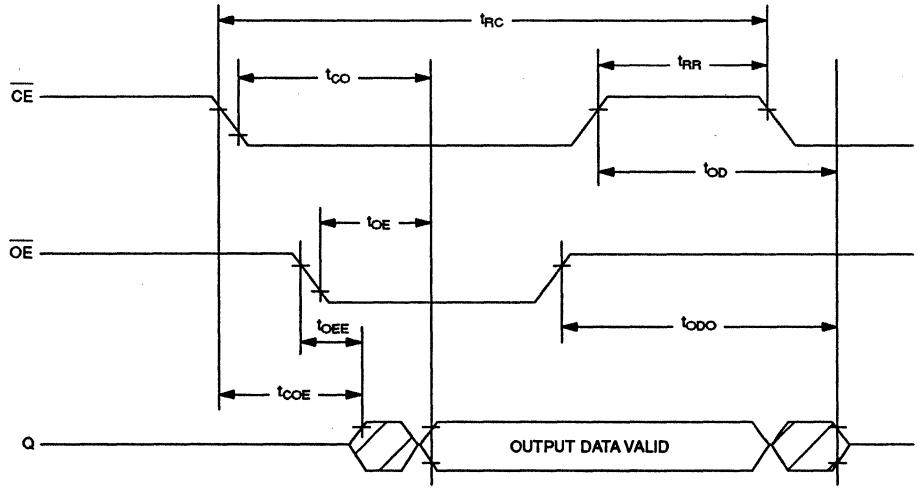
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



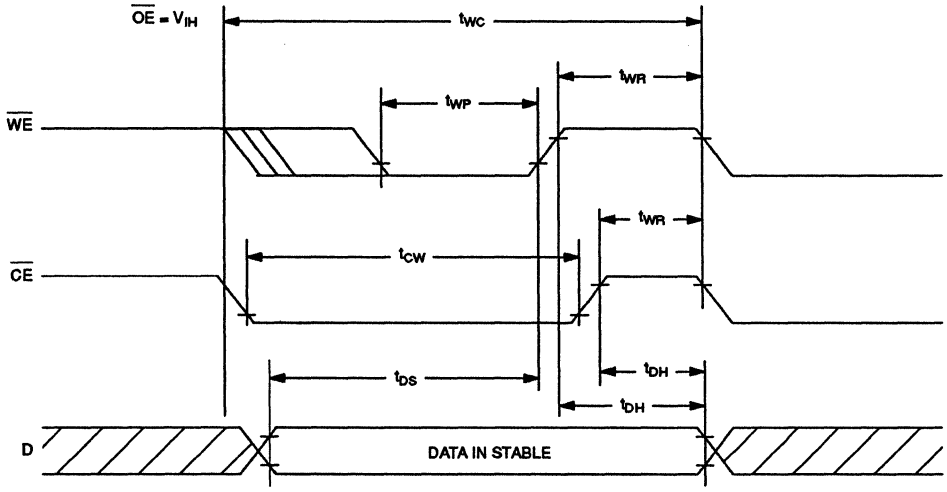
RESET FOR PHANTOM CLOCK



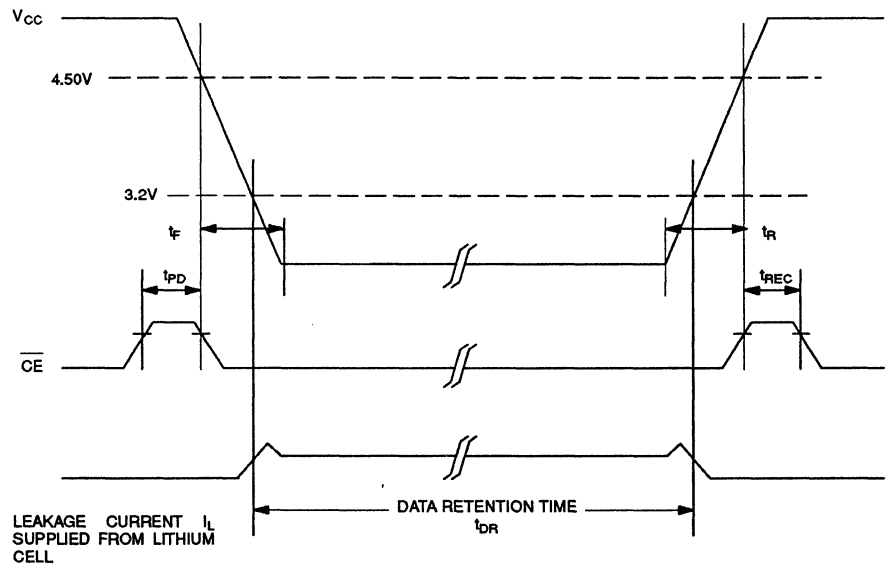
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



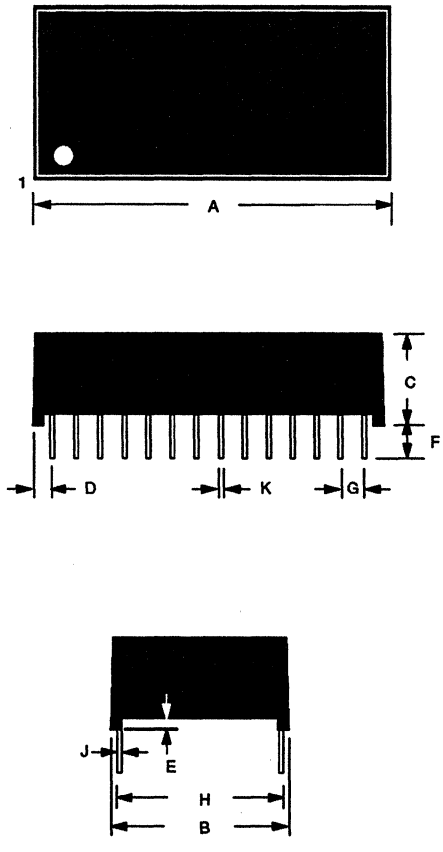
POWER-DOWN/POWER-UP CONDITION



NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1243Y 28 PIN EXTENDED BOTTOM 720 MIL BODY WIDTH (DIMENSION B)



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

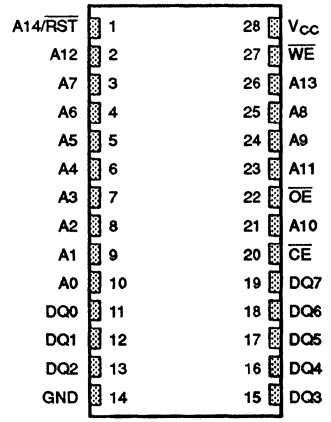
DALLAS SEMICONDUCTOR

DS1244Y
256K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 32K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE
(740 MIL EXTENDED)

PIN DESCRIPTION

A_0-A_{14}	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ_0-DQ_7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect
$\overline{RST}$	-	Reset

DESCRIPTION

The DS1244Y 256K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 32,768 words by 8 bits) with a built-in real time clock. The DS1244Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1244Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1244Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1244Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

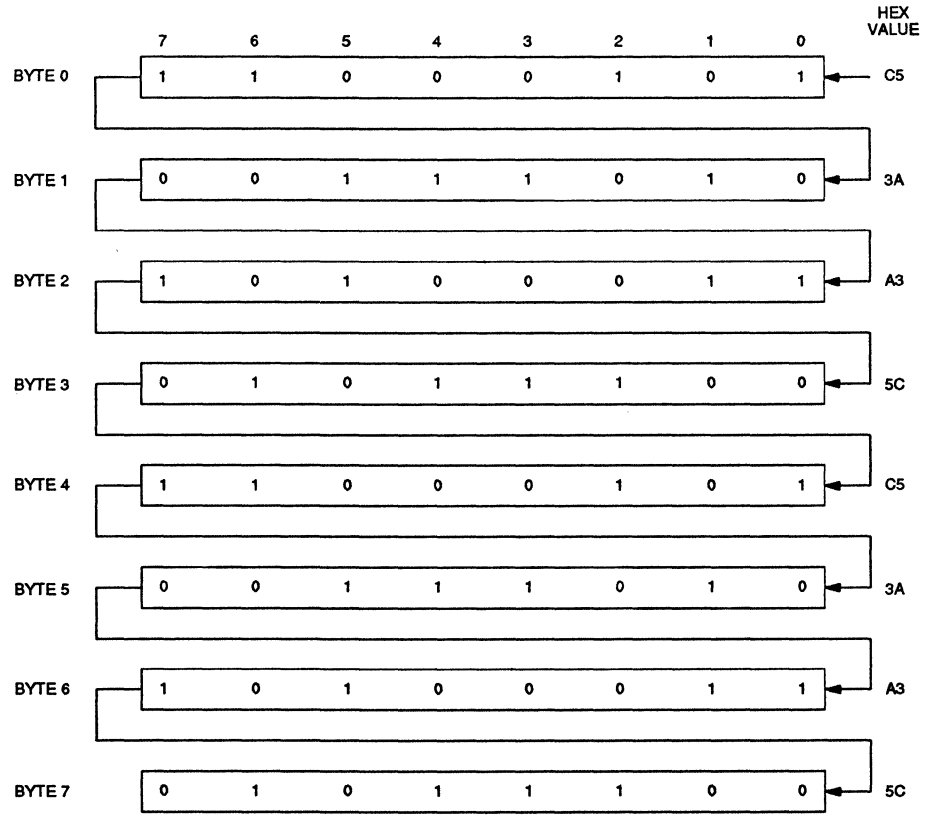
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

FIGURE 1: PHANTOM CLOCK REGISTER DEFINITION



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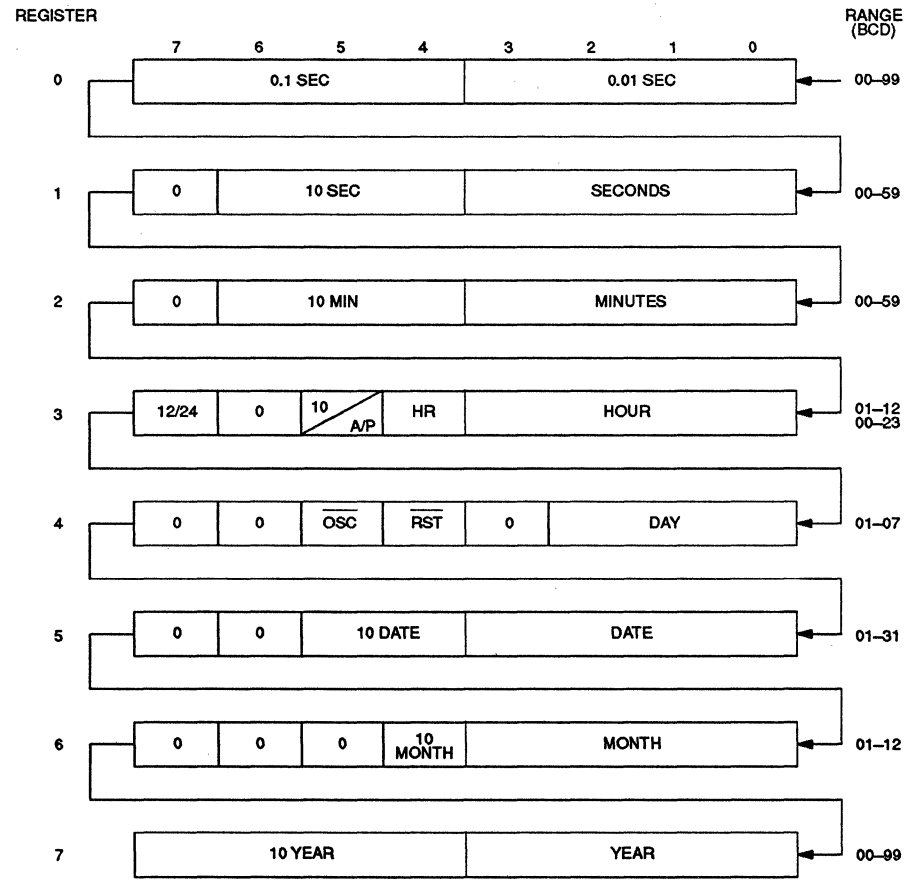
NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

FIGURE 2: PHANTOM CLOCK REGISTER DEFINITION



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	0.3		0.8	V	

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DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5.0V ± 10%)									
PARAMETER	SYMBOL	DS1244Y-120		DS1244Y-150		DS1244Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70		80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

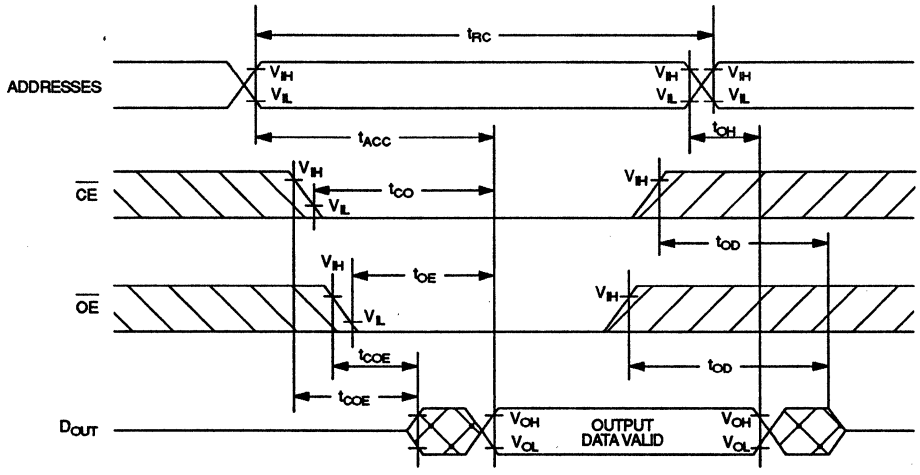
POWER-DOWN/POWER-UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

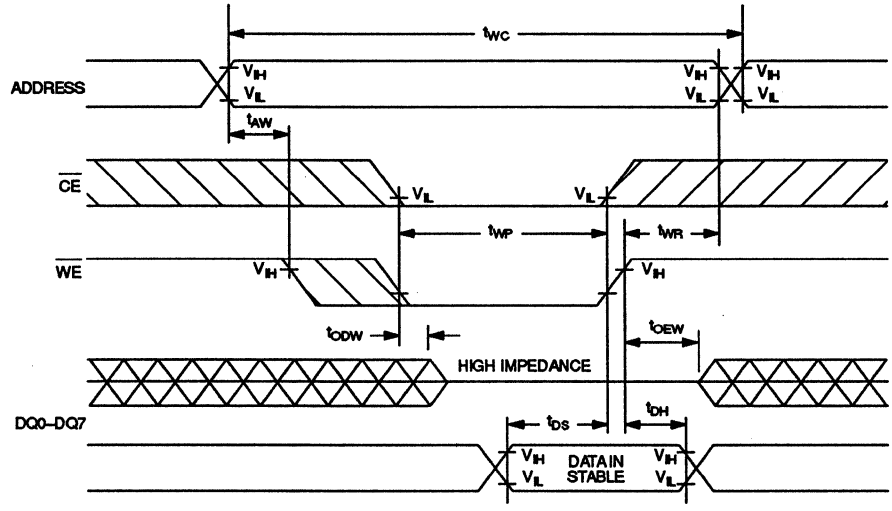
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

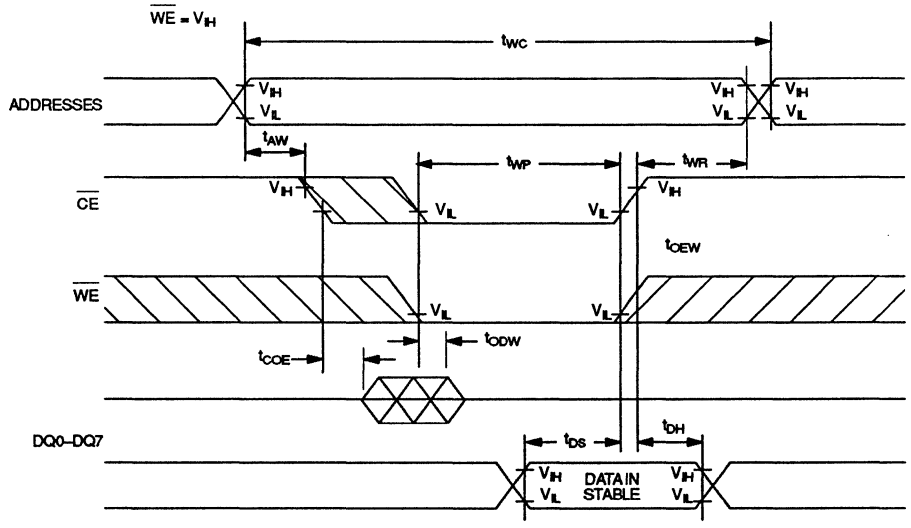
MEMORY READ CYCLE (NOTE 1)



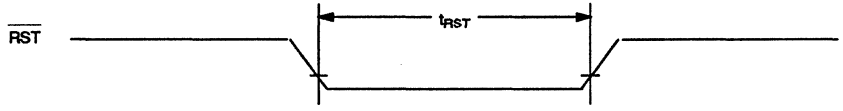
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



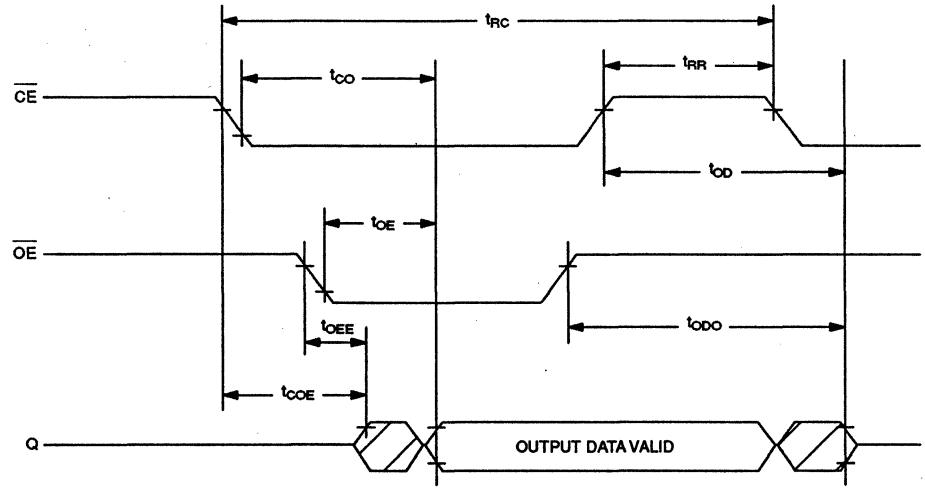
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



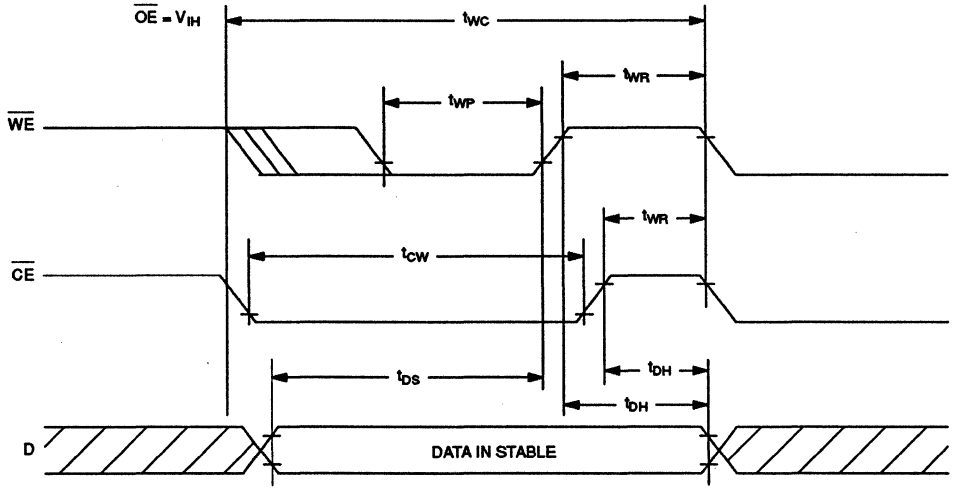
RESET FOR PHANTOM CLOCK



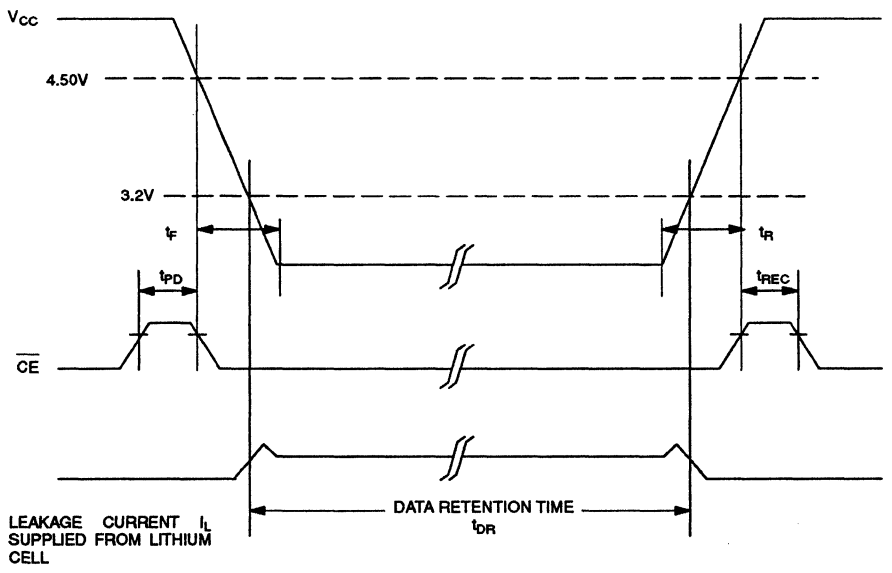
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



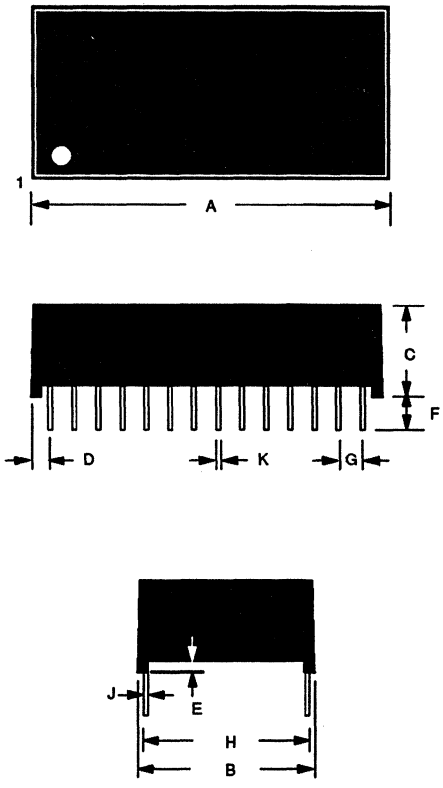
POWER-DOWN/POWER-UP CONDITION



NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1244Y 256K NV SRAM WITH PHANTOM CLOCK



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

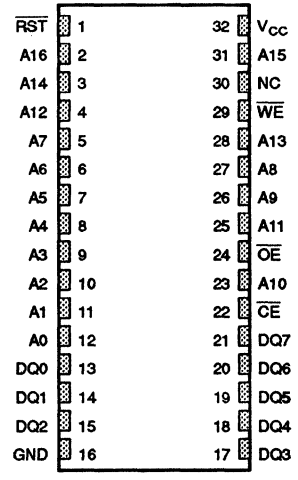
DALLAS SEMICONDUCTOR

DS1248Y
1024K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 128K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 120, 150 and 200 ns access time

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
(740 MIL FLUSH)

PIN DESCRIPTION

A_0-A_{16}	-	Address Inputs
$\overline{CE}$	-	Chip Enable
GND	-	Ground
DQ_0-DQ_7	-	Data In/Data Out
V_{CC}	-	Power (+5V)
$\overline{WE}$	-	Write Enable
$\overline{OE}$	-	Output Enable
NC	-	No Connect
$\overline{RST}$	-	Reset

DESCRIPTION

The DS1248Y 1024K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 128K words by 8 bits) with a built-in real time clock. The DS1248Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

RAM READ MODE

The DS1248Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which of the 128K bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1248Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1248Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by approximately 4.0 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

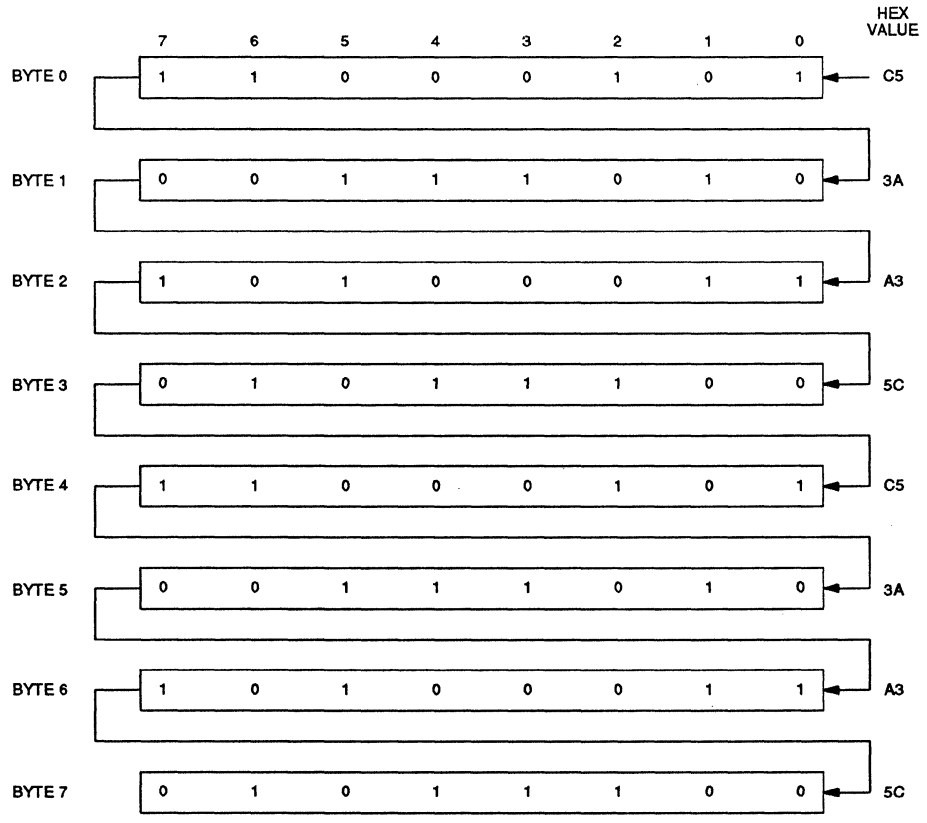
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Phantom Clock register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

FIGURE 1: PHANTOM CLOCK REGISTER DEFINITION

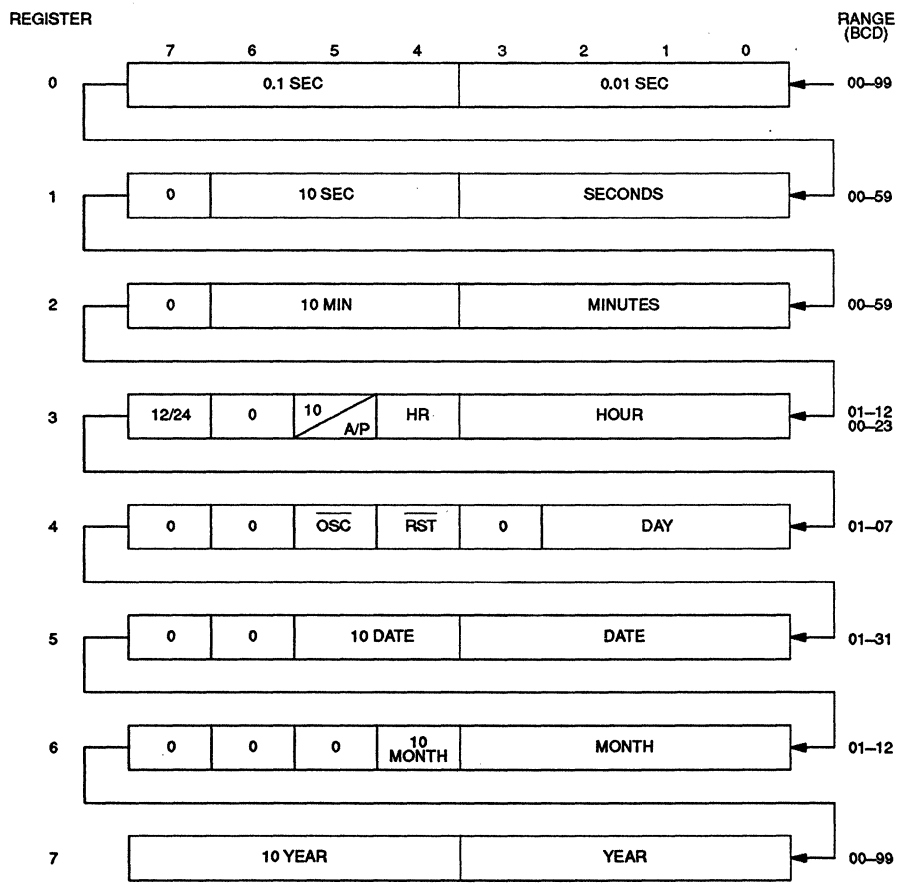


6

NOTE

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

FIGURE 2: PHANTOM CLOCK REGISTER DEFINITION



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the Phantom Clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	
Input Logic 0	V_{IL}	-0.3		0.8	V	

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DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200 ns	I_{CC01}			85	mA	

DC TEST CONDITIONS

Outputs are open; all voltages are referenced to ground.

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CC} = 5.0V ± 10%)									
PARAMETER	SYMBOL	DS1248Y-120		DS1248Y-150		DS1248Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		70		80	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	40			ns	11
Data Hold Time	t_{DH}	10			ns	11
$\overline{CE}$ Pulse Width	t_{CW}	100			ns	
$\overline{RESET}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	

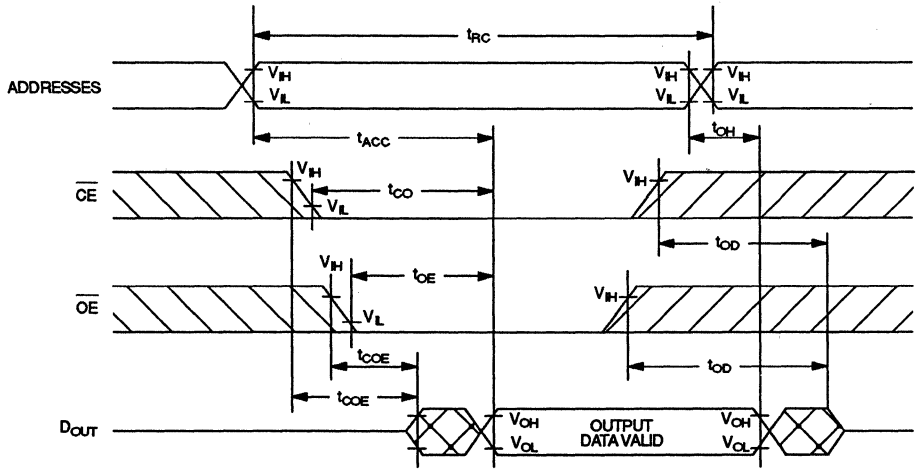
POWER-DOWN/POWER-UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}			2	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

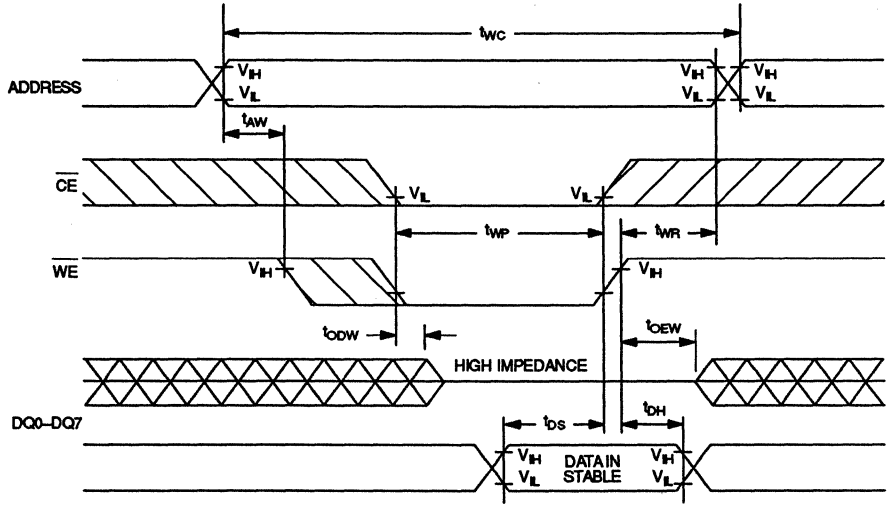
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

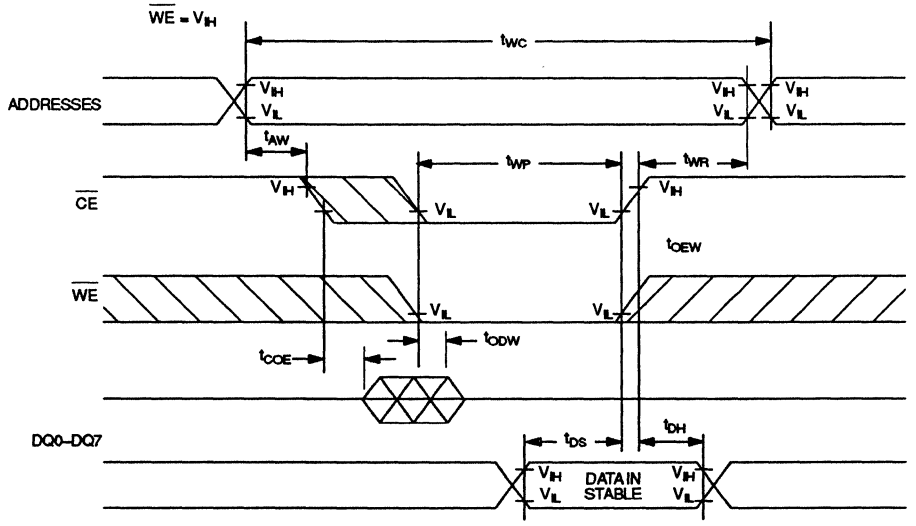
MEMORY READ CYCLE (NOTE 1)



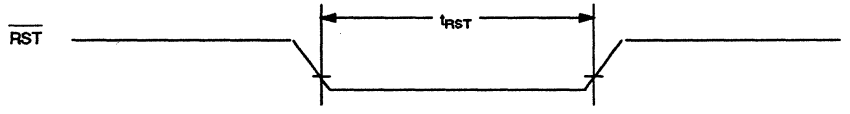
MEMORY WRITE CYCLE 1 (NOTES 2, 6, AND 7)



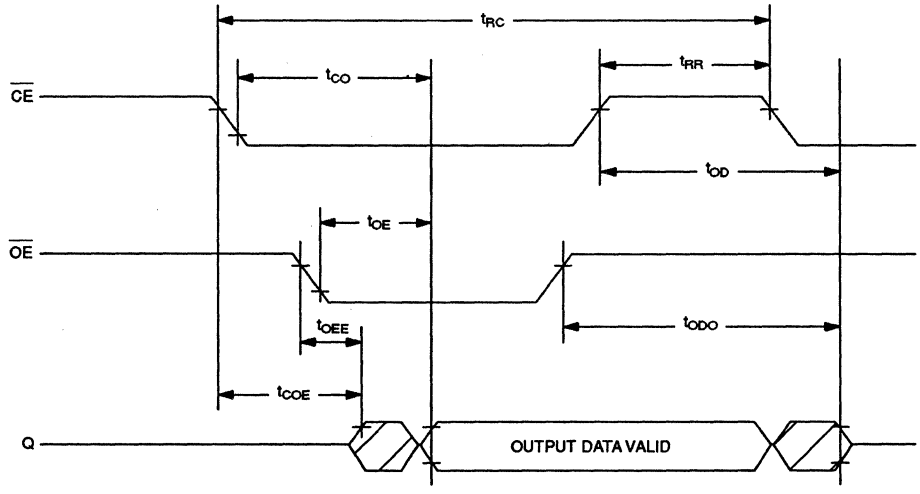
MEMORY WRITE CYCLE 2 (NOTES 2 AND 8)



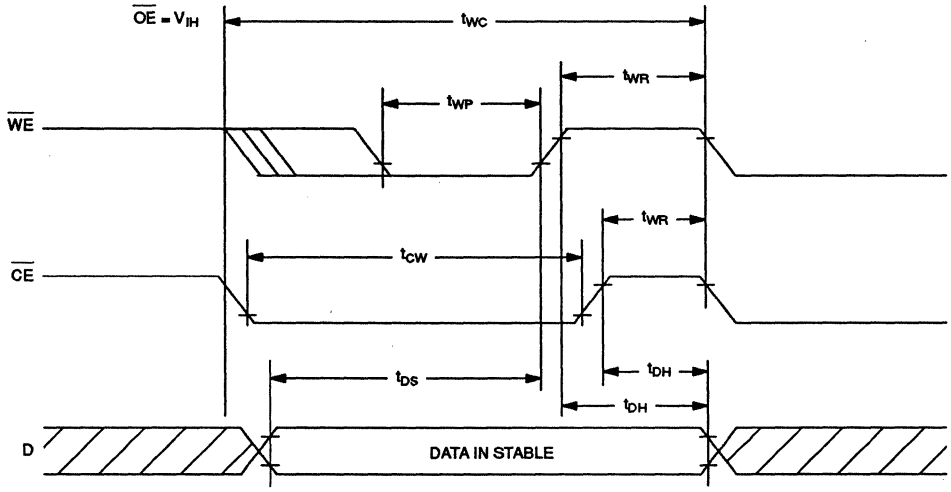
RESET FOR PHANTOM CLOCK



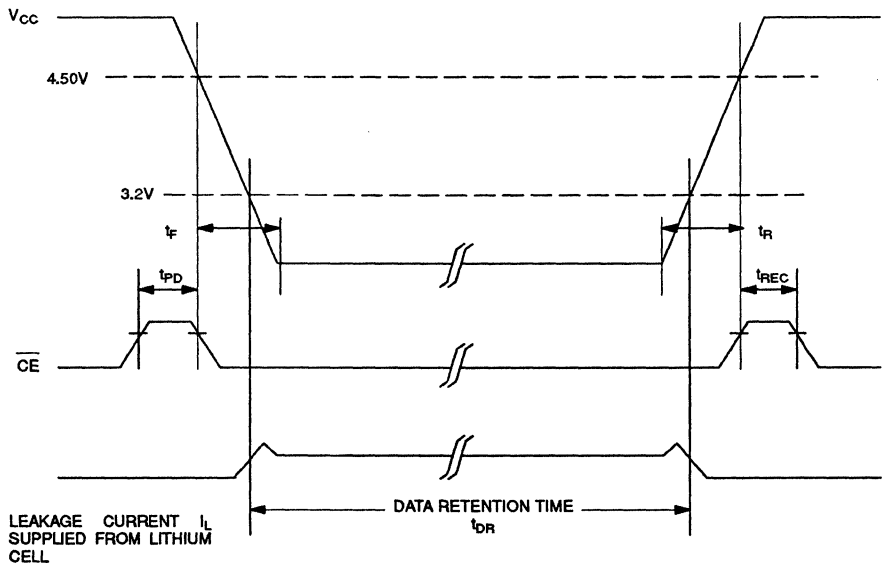
READ CYCLE TO PHANTOM CLOCK



WRITE CYCLE TO PHANTOM CLOCK



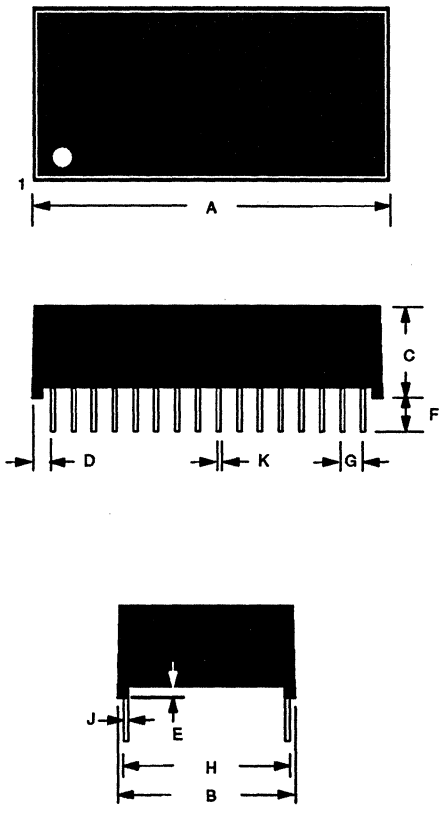
POWER-DOWN/POWER-UP CONDITION



NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 50 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} with the clock oscillator running.
10. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. $\overline{RST}$ (Pin1) has an internal pull-up resistor.

DS1248Y 1024K NV SRAM WITH PHANTOM CLOCK



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

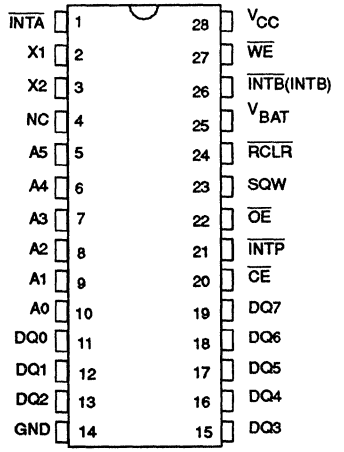
DALLAS SEMICONDUCTOR

DS1283
Watchdog Timekeeper Chip

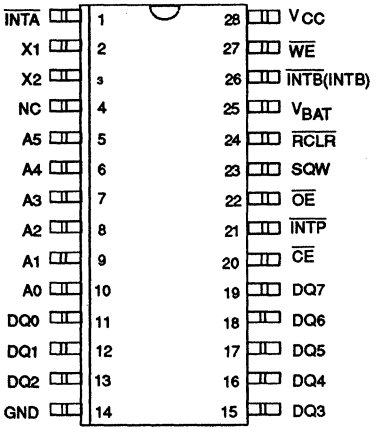
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function provides notice of real time related occurrences
- Designed for battery operation
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minutes/month at 25°C
- 50 bytes of user nonvolatile RAM
- Optional 28-pin SOIC surface mount package
- Low-power CMOS circuitry is maintained on less than 1 µA in standby mode

PIN ASSIGNMENT



DS1283
28-Pin DIP (600 mil)



DS1283S
28-Pin SOIC (330 mil)

NOTE: Pin 4 must be left disconnected.

DESCRIPTION

The DS1283 Watchdog Timekeeper Chip is a self- contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP or 28-pin SOIC surface mount package. The DS1283 is specifically designed to maintain internal operations from a single low voltage supply. In fact, the only two external components required by the DS1283 are a battery and crystal. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, V_{CC}, and $\overline{RCLR}$, see the DS1286 Watchdog Timekeeper data sheet.

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	$\overline{INTA}$	O	Interrupt Output A
2-3	X1,X2	I	32.768 KHz Crystal
4	NC	–	No Connection
5-10	A0-A5	I	Address Inputs: A5=Pin 5; A0=Pin 10
11	DQ0	I/O	Data Input/Output
12	DQ1	I/O	Data Input/Output
13	DQ2	I/O	Data Input/Output
14	GND	–	Ground
15	DQ3	I/O	Data Input/Output
16	DQ4	I/O	Data Input/Output
17	DQ5	I/O	Data Input/Output
18	DQ6	I/O	Data Input/Output
19	DQ7	I/O	Data Input/Output
20	$\overline{CE}$	I	Chip Enable
21	$\overline{INTP}$	O	Interrupt Output P
22	$\overline{OE}$	O	Output Enable
23	SQW	O	Square Wave Output
24	$\overline{RCLR}$	I	RAM Clear
25	V_{BAT}	I	Battery Input
26	$\overline{INTB}$ (INTB)	O	Interrupt Output B
27	$\overline{WE}$	I	Write Enable
28	V_{CC}	I	V_{CC} Input

PIN DESCRIPTIONS

X1, X2 – Connections for a standard 32.768 KHz quartz crystal, Daiwa part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a load capacitance (C_L) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor Part # DS9032.

V_{BAT} – Battery input for a battery or power supply between 5.5 volts and 2.5 volts. When the DS1283 is powered by the V_{BAT} pin alone, V_{CC} and V_{BAT} must be connected together. When a single supply is used, input and output levels and timing are only guaranteed between the ranges of 4.5 volts and 5.5 volts. In this mode, the active current drain is 2 mA ($\overline{CE} = V_{IL}$), the standby current is 0.5 mA ($\overline{CE} = V_{IH}$), and the data retention mode is less than 1 µA typical and 1.5 µA maximum at 5.5 volts ($\overline{CE} = V_{BAT}$ - 0.2 volts). These current drain specifications are stated with all outputs unloaded.

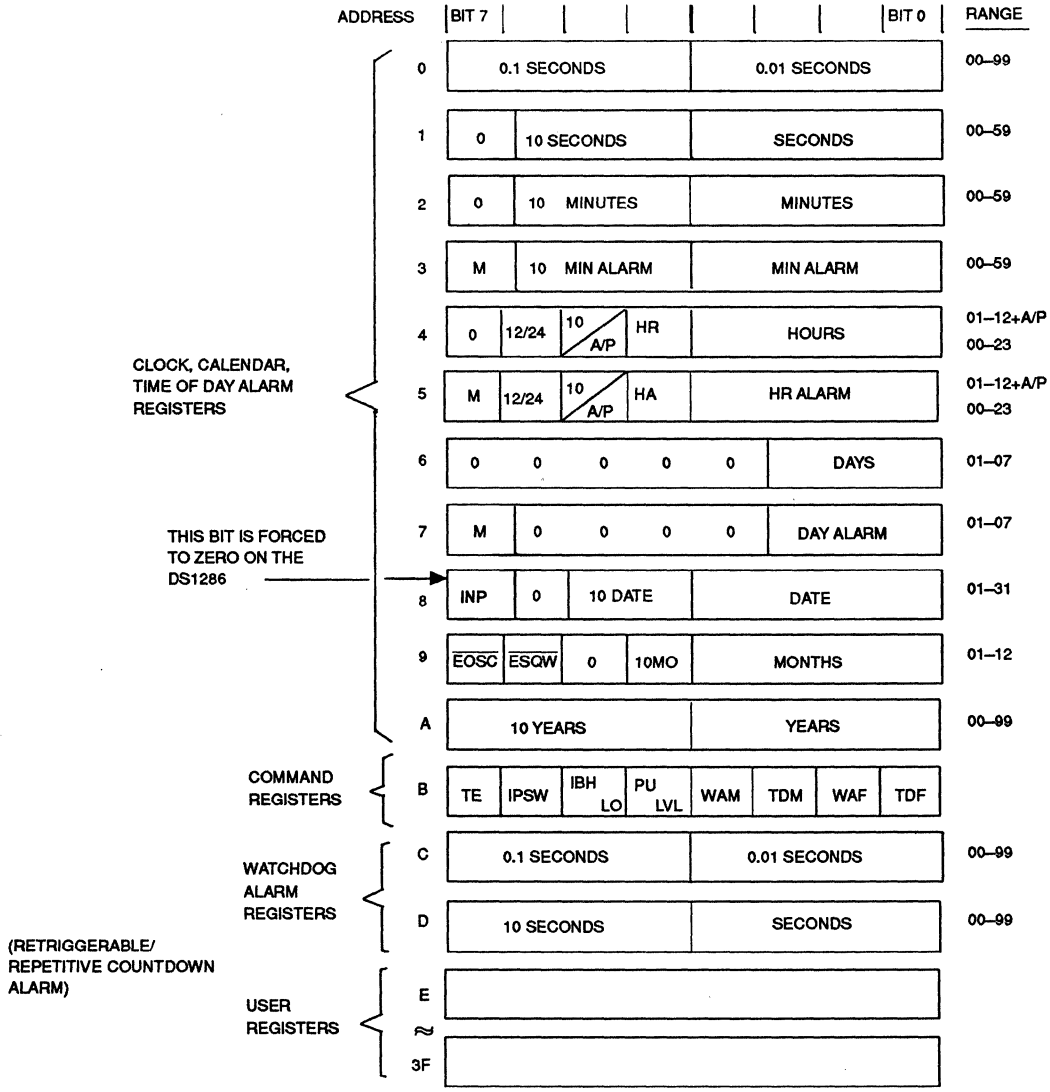
V_{CC} – +5 volt input for connection to the V_{CC} supply. This supply input is used for inputs and outputs only as the internal functions of the device are powered by the V_{BAT} pin. The V_{CC} voltage range should never exceed V_{BAT} by more than 0.3 volts and V_{BAT} is normally connected to V_{CC}. In order to guarantee timing and input/output levels, both V_{CC} and V_{BAT} must be between 4.5 and 5.5 volts. However, the DS1283 maintains internal functions with V_{CC} input as low as 2.5 volts.

$\overline{RCLR}$ – The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of user nonvolatile RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (-0.3 to +0.8 volts). The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

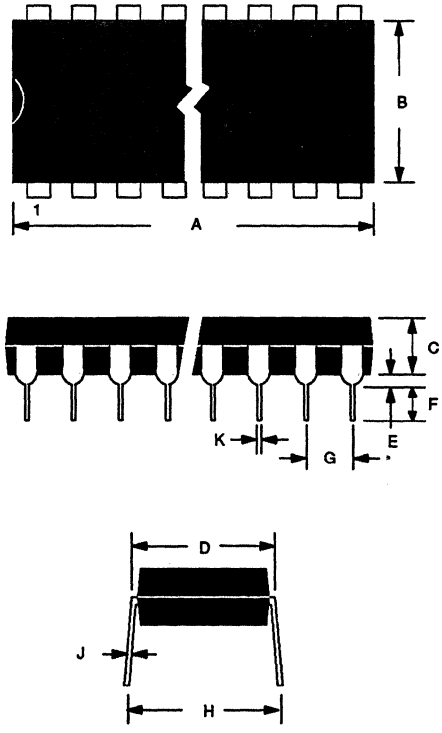
$\overline{INTB}$ – Interrupt B on the DS1283 operates identical to interrupt B on the DS1286 except that the sink and source current is limited to 500 µA. This pin should be pushed up or pulled down if not used.

$\overline{INTP}$ – Interrupt P on the DS1283 was a missing or no connection pin on the DS1286. This interrupt works in the same manner as $\overline{INTA}$ as programmed by the IPSW bit. However, $\overline{INTP}$ is also logically ORed with the MSB of the date register (see Figure 1). This bit is called the INP bit on the DS1283 and is forced to zero on the DS1286. When the INP bit (interrupt P bit) is set to logical one, interrupt P will be held active low. When INP is set to logical zero, $\overline{INTP}$ is always at the same logic state as $\overline{INTA}$. This pin is an open drain capable of sinking 4 mA.

DS1283 WATCHDOG TIMEKEEPER REGISTERS Figure 1

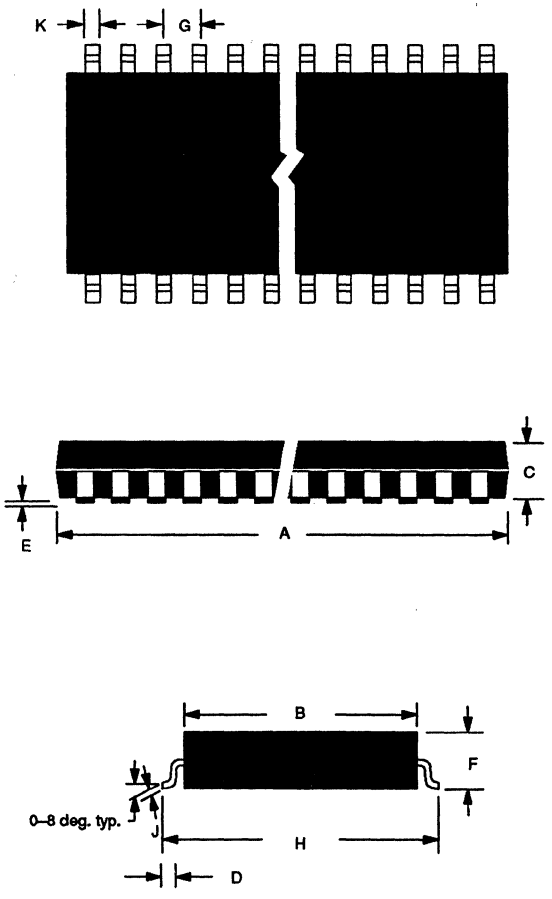


DS1283 28 PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

DS1283 28 PIN SOIC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

6

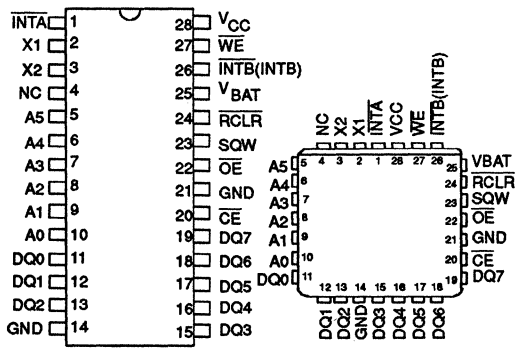
DALLAS SEMICONDUCTOR

DS1284
Watchdog Timekeeper Chip

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- 50 bytes of user NV RAM
- Optional 28-pin PLCC surface mount package
- Low-power CMOS circuitry is maintained on less than 0.5 µA when power is supplied from battery input

PIN ASSIGNMENT



DS1284
28-Pin DIP (600 mil)

DS1284Q
28-Pin PLCC

PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A
$\overline{INTB}$(INTB)	-	Interrupt Output B
A0-A5	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
NC	-	No Connection
SQW	-	Square Wave Output
X1,X2	-	32.768 kHz Crystal Connections
V_{BAT}	-	+3 Volt Battery Input
$\overline{RCLR}$	-	RAM Clear

DESCRIPTION

The DS1284 Watchdog Timekeeper Chip is a self-contained real-time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package or a 28-pin PLCC surface mount package. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS1286 Watchdog Timekeeper data sheet.

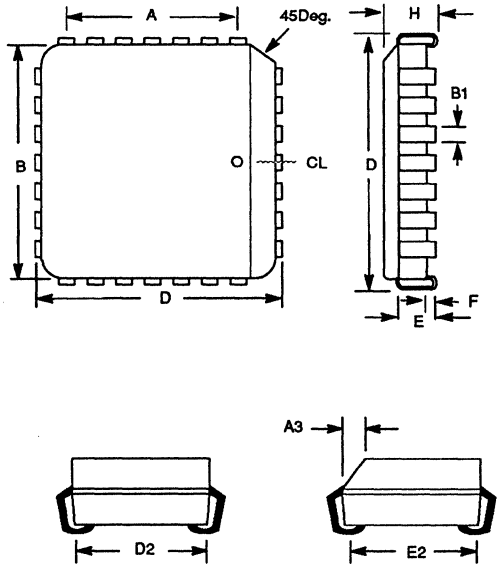
PIN DESCRIPTION

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V_{BAT} - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to registers containing time, watchdog, alarm, and RAM information is denied is set by internal circuitry as 1.26 x V_{BAT}. A maximum load of 0.5 µA at 25°C in the absence of power should be used to size the external energy source. An optional ground pin is provided for connection to battery negative. This pin should be grounded but can be left floating.

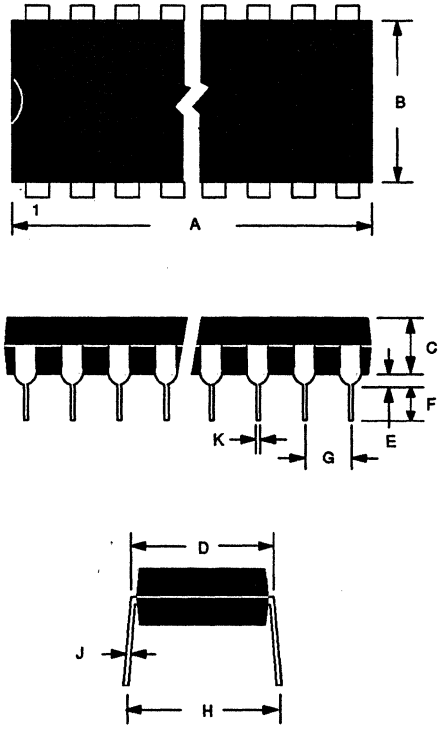
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of user NV RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic zero (-0. 3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

DS1284Q 28 PIN PLCC WATCHDOG TIMEKEEPER



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.300 BSC 7.62	
B IN. MM	0.442 17.68	0.462 11.73
D IN. MM	0.480 12.2	0.500 12.7
D2 IN. MM	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05
E2 IN. MM	0.390 9.91	0.430 10.92
F IN. MM	0.015 0.38	0.020 0.518
H IN. MM	0.100 2.54	0.020 0.518

DS1284 28 PIN DIP WATCHDOG TIMEKEEPER



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445	1.470
B IN. MM	0.530	0.550
C IN. MM	0.140	0.160
D IN. MM	0.600	0.625
E IN. MM	0.015	0.040
F IN. MM	0.120	0.145
G IN. MM	0.090	0.110
H IN. MM	0.625	0.675
J IN. MM	0.008	0.012
K IN. MM	0.015	0.022

DALLAS SEMICONDUCTOR

DS1285, DS1285Q
Real Time Clock

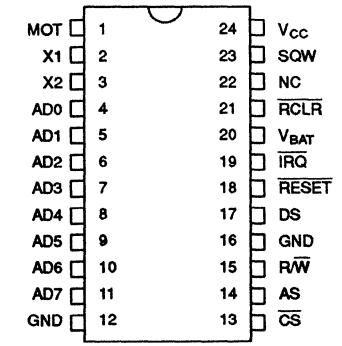
FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818A
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µA to 500 ms
  - End of clock update cycle
- Optional 28-pin PLCC surface mount package

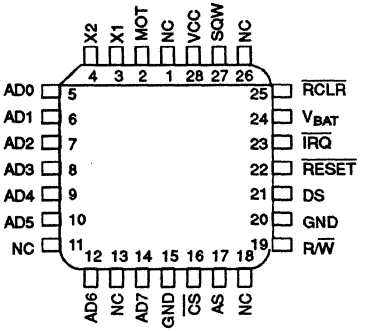
DESCRIPTION

The DS1285 Real Time Chip is a direct replacement for the MC146818A in IBM AT computer clock/calendar and other applications. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS1287 data sheet.

PIN ASSIGNMENT



DS1285 24-PIN DIP
DS1285S 24-PIN SOIC



DS1285Q 28-PIN PLCC

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground
X1,X2	-	32.768 kHz Crystal Connections
V_{BAT}	-	+3 Volt Battery Input
$\overline{RCLR}$	-	RAM Clear

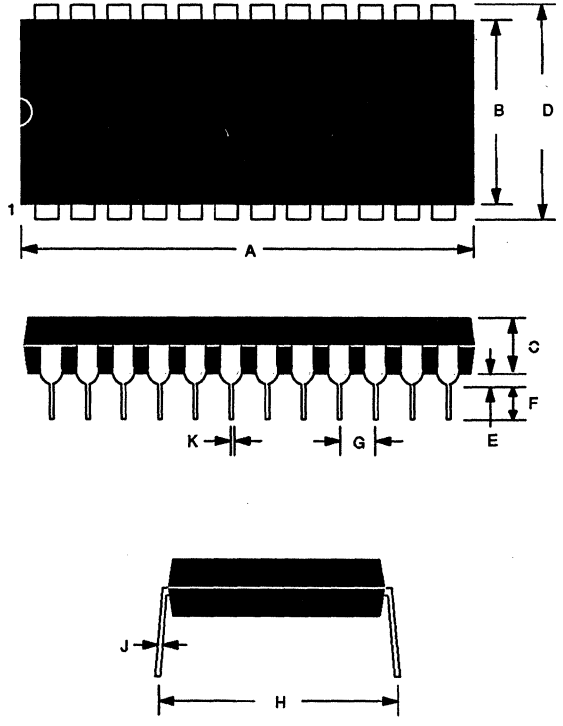
PIN DESCRIPTION

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S, Seiko part number DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. A variable trimming capacitor may be required for extremely high precision timekeeping applications. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of .5 µA at 25°C in the absence of power should be used to size the external energy source.

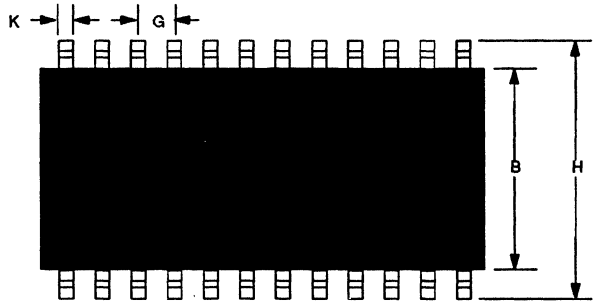
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.

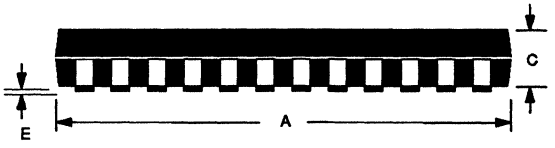
DS1285 24 PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.145	0.165
MM	3.68	4.19
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.559

DS1285 24 PIN SOIC

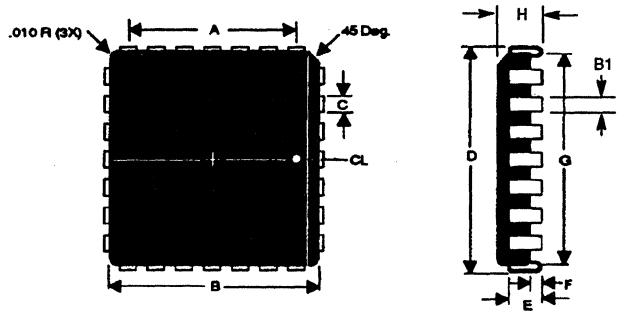




PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.02
phi	0°	8°

6

DS1285Q 28 PIN PLCC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.300 REF 7.62	
B IN. MM	0.442 17.68	0.462 11.73
B1 IN. MM	0.013 0.33	0.021 0.53
C IN. MM	0.027 0.68	0.033 0.84
D IN. MM	0.480 12.2	0.500 12.7
E IN. MM	0.090 2.29	0.120 3.05
F IN. MM	0.020 0.51	MIN MIN
G IN. MM	0.390 9.91	0.430 10.92
H IN. MM	0.165 4.19	0.180 4.57

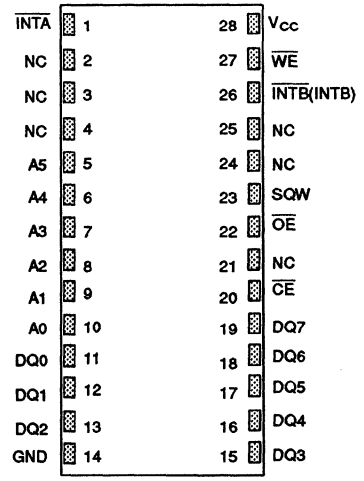
DALLAS SEMICONDUCTOR

DS1286
Watchdog Timekeeper

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real time-related activities
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC}
- 50 bytes of user NV RAM

PIN ASSIGNMENT



28-Pin Encapsulated Package (720 Mil Flush)

PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A
$\overline{INTB}$(INTB)	-	Interrupt Output B
A0-A5	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
NC	-	No Connection
SQW	-	Square Wave Output

DESCRIPTION

The DS1286 Watchdog Timekeeper is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 64 eight-bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with

an AM/PM indicator. The watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

OPERATION - READ REGISTERS

The DS1286 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1286 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

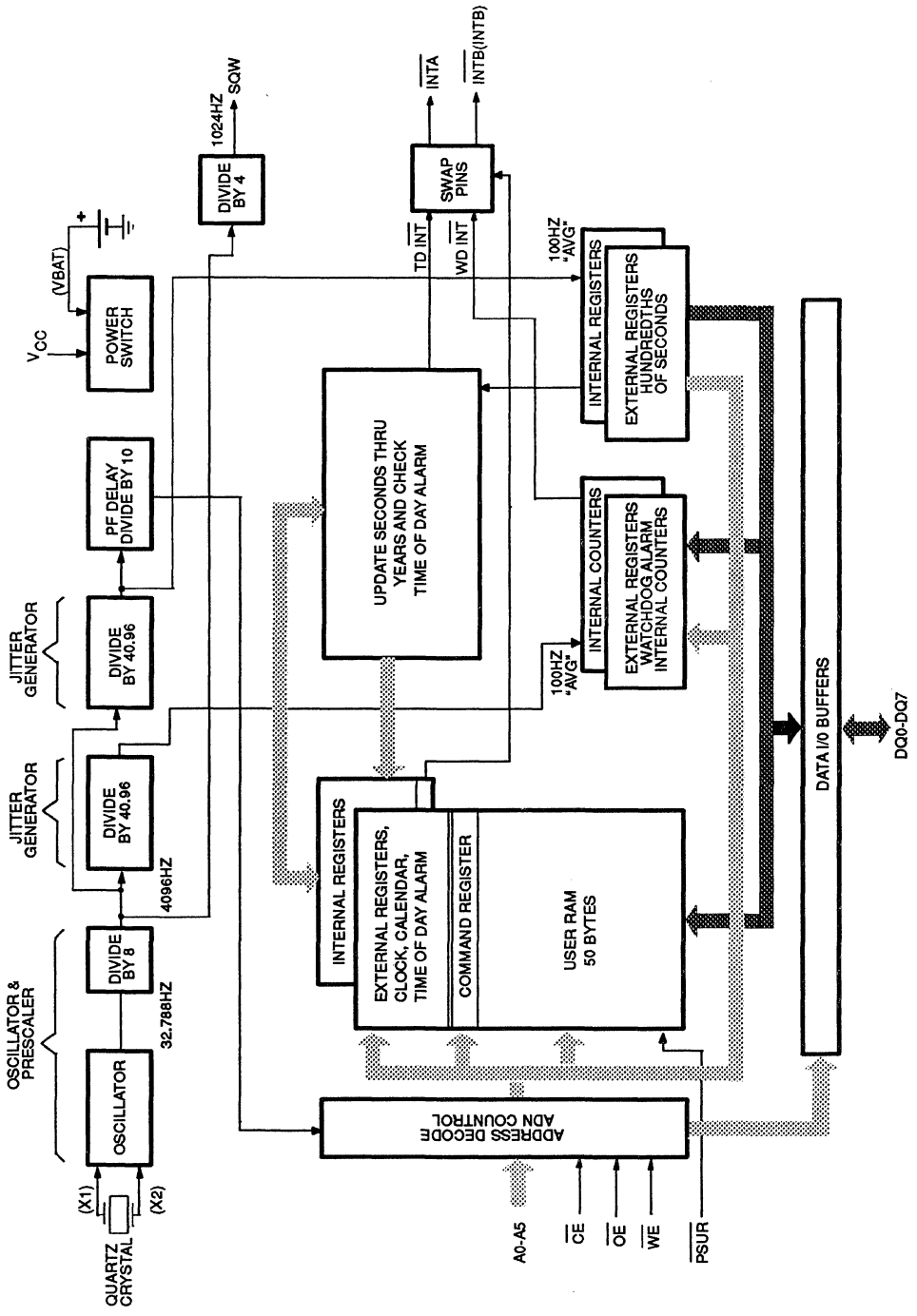
DATA RETENTION

The Watchdog Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1286 constantly monitors V_{CC}. Should the supply voltage decay, the Watchdog Timekeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 150 ms.

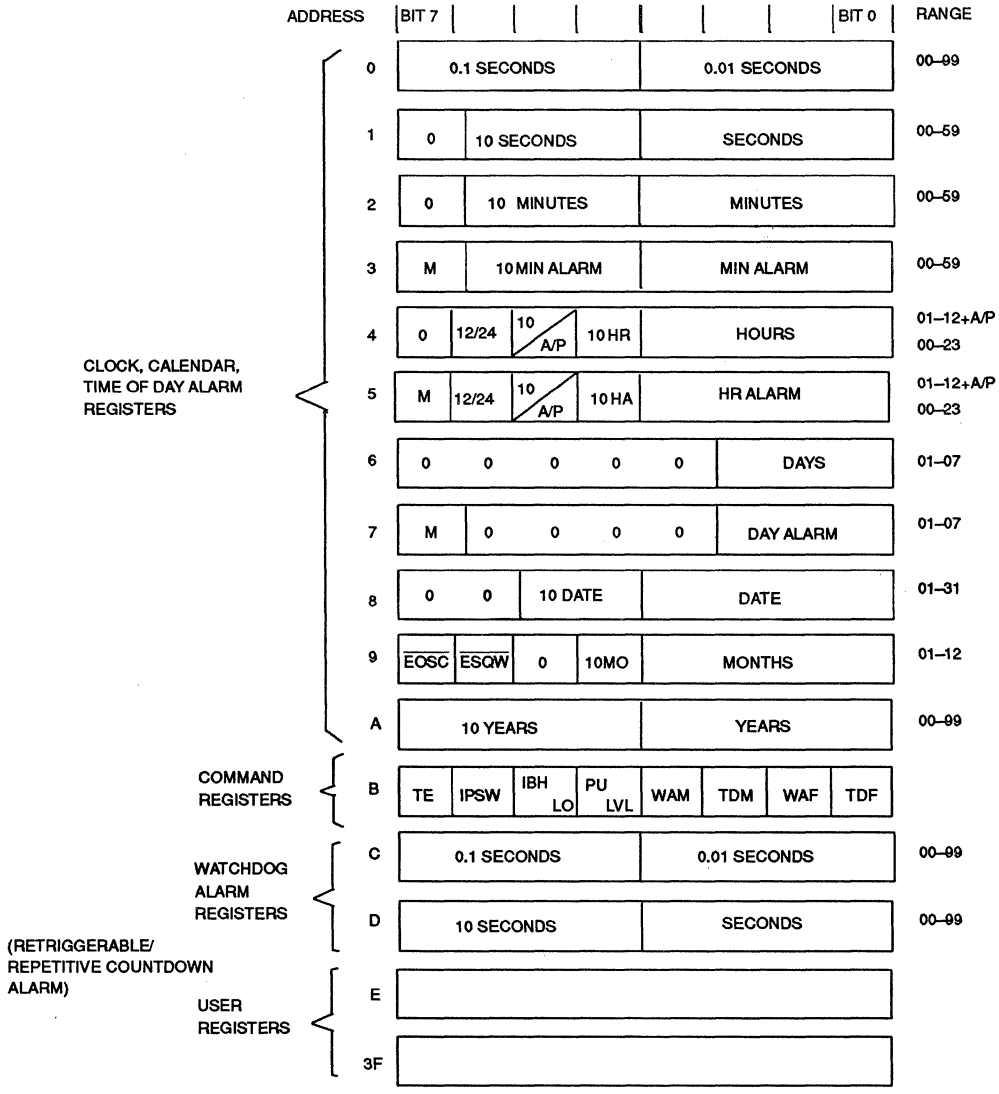
WATCHDOG TIMEKEEPER REGISTERS

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm, and Watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm registers and information which is stored in these two registers is in BCD. Registers E through 3F are user bytes and can be used to contain data at the user's discretion.

BLOCK DIAGRAM Figure 1



DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, $\overline{EOSC}$ (bit 7) enables the Real Time Clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (Pin 23). When set to logic zero, the Square Wave Output pin will output a 1024 Hz Square Wave Signal. When set to logic one the Square Wave Output pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12- or 24- hour Select Bit. When set to logic one, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the real time clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen.

An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds read 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm registers are written and read in the same format as the Time of Day registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Registers C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer countdown is interrupted and reinitialized back to the entered value every time either of the registers is accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm registers always read the entered value. The actual countdown register is internal and is not readable. Writing Registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logic one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm registers. However, if the transfer enable bit is set to logic zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logic one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Watchdog Alarm registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logic one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logic zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask bit (WAM). When this bit is written to a logic one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. Output $\overline{\text{INTB}}$ (INTB) will either sink or source current for a minimum of 3 ms depending on the level of bit 5. When bit 5 is set to logic one, the B interrupt will source current. When bit 5 is set to logic zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$(INTB). When set to logic one, $\overline{\text{INTA}}$ becomes the Time of Day Alarm Interrupt pin and $\overline{\text{INTB}}$(INTB) becomes the Watchdog Interrupt pin. When bit 6 is set to logic zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on $\overline{\text{INTB}}$(INTB) and the Watchdog Interrupt will be output on $\overline{\text{INTA}}$. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day registers.

TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3)MINUTES	(5)HOURS	(7)DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

6

DC ELECTRICAL CHARACTERISTICS

(0°C TO 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ > V_{CC} -0.5	I_{CCS2}			4.0	mA	
Active Current	I_{CC}			15	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A=25°C)

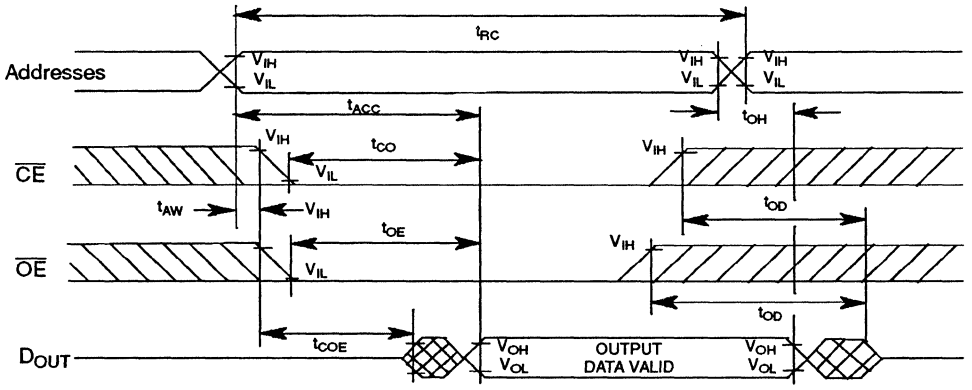
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	10	pF	
Output Capacitance	C_{OUT}		7	10	pF	
Input/Output Capacitance	$C_{I/O}$		7	10	pF	

AC ELECTRICAL CHARACTERISTICS

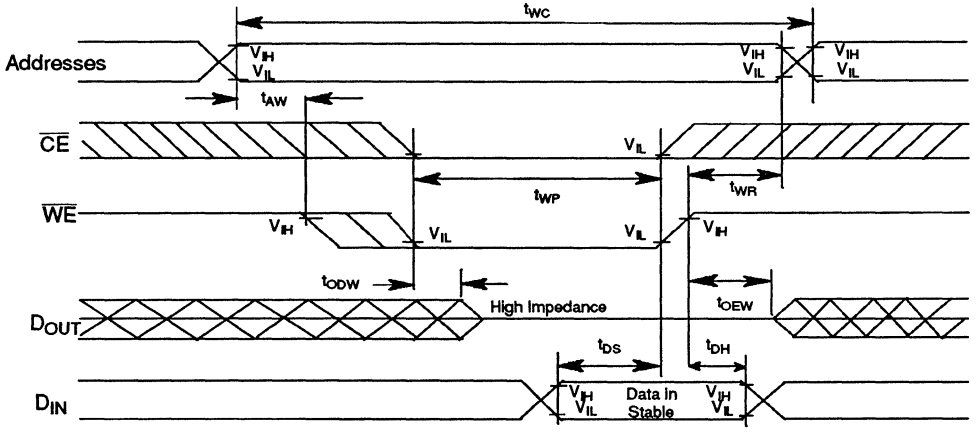
(0°C TO 70° C, V_{CC} = 4.5V TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150			ns	1
Address Access Time	t_{ACC}			150	ns	
$\overline{CE}$ Access Time	t_{CO}			150	ns	
$\overline{OE}$ Access Time	t_{OE}			60	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z from Deselect	t_{OD}			60	ns	
Output Hold from Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	150			ns	
Write Pulse Width	t_{WP}	140			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	10			ns	
Output High Z from $\overline{WE}$	t_{ODW}			50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10			ns	
Data Setup Time	t_{DS}	45			ns	4
Data Hold Time	t_{DH}	0			ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3			ms	11,12

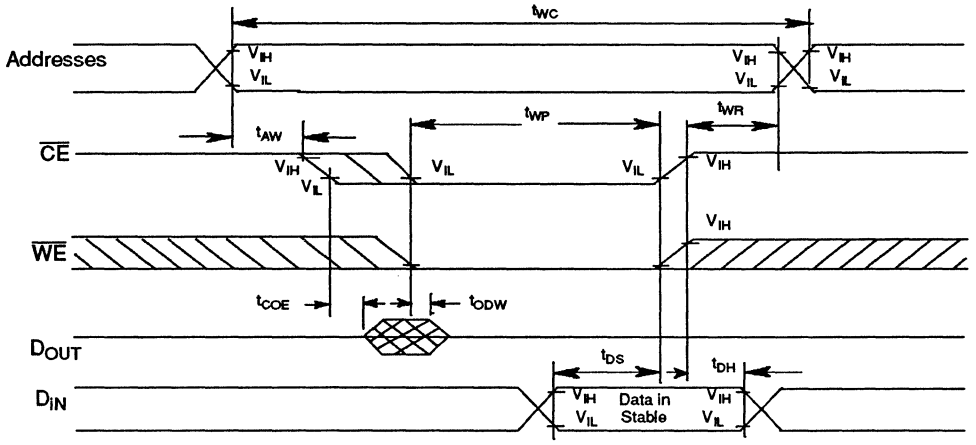
READ CYCLE (Note1)



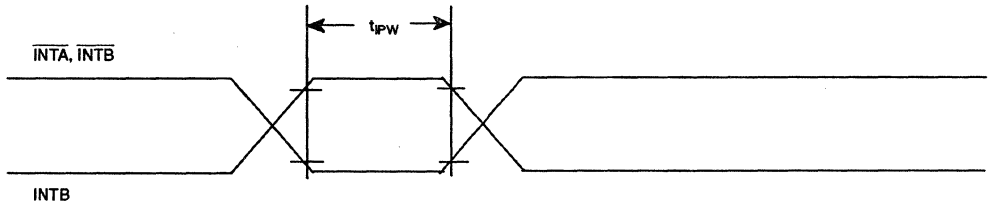
WRITE CYCLE 1 (Notes 2, 6, 7)



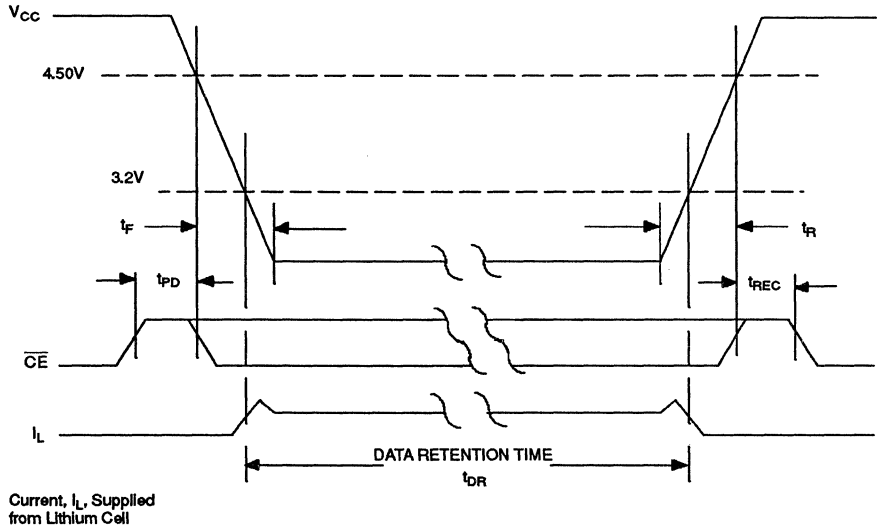
WRITE CYCLE 2 (Notes 2, 8)



TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	350		µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	100		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up		150	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

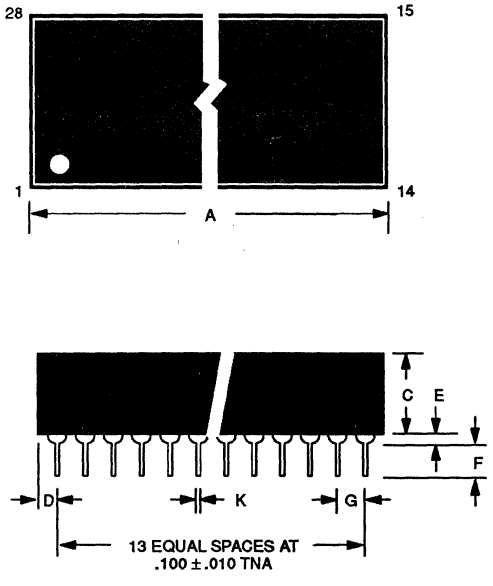
NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

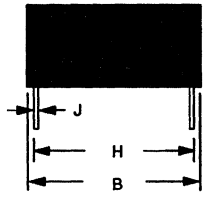
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1286 WATCHDOG TIMEKEEPER



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 21, 24 AND 25 ARE MISSING BY DESIGN.

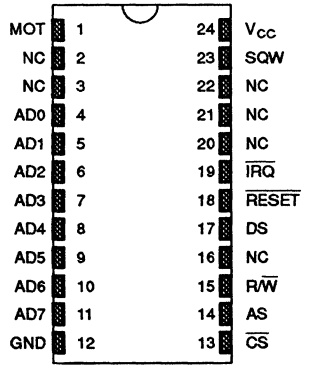
DALLAS SEMICONDUCTOR

DS1287
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0–AD7	-	Multiplexed address/data bus
NC	-	No connection
MOT	-	Bus type selection
$\overline{CS}$	-	Chip select
AS	-	Address strobe
R/$\overline{W}$	-	Read/write input
DS	-	Data strobe
$\overline{RESET}$	-	Reset input
$\overline{IRQ}$	-	Interrupt request output
SQW	-	Square wave output
V_{CC}	-	+5 volt supply
GND	-	Ground

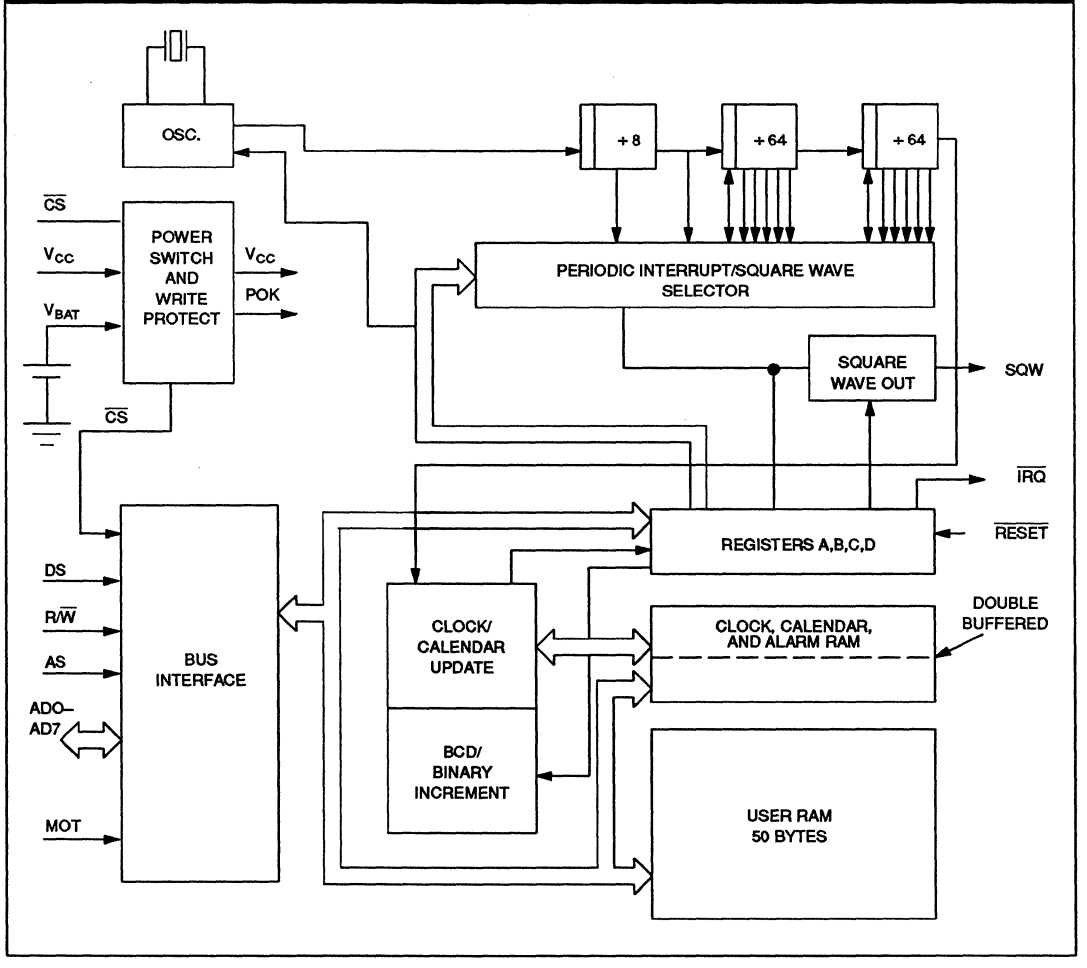
DESCRIPTION

The DS1287 Real Time Clock is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1287. The following paragraphs describe the function of each pin.

FIGURE 1: BLOCK DIAGRAM DS1287



POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

TABLE 1: PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

DS (Data Strobe or Read Input) - The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS1287 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input)-The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS1287 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1287 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{RESET}$ (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS1287 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the follow ing occurs:

A. Periodic Interrupt Enable (PIE) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable ($\overline{SQWE}$) bit is cleared to zero.

J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{RESET}$ can be connected to V_{CC}. This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

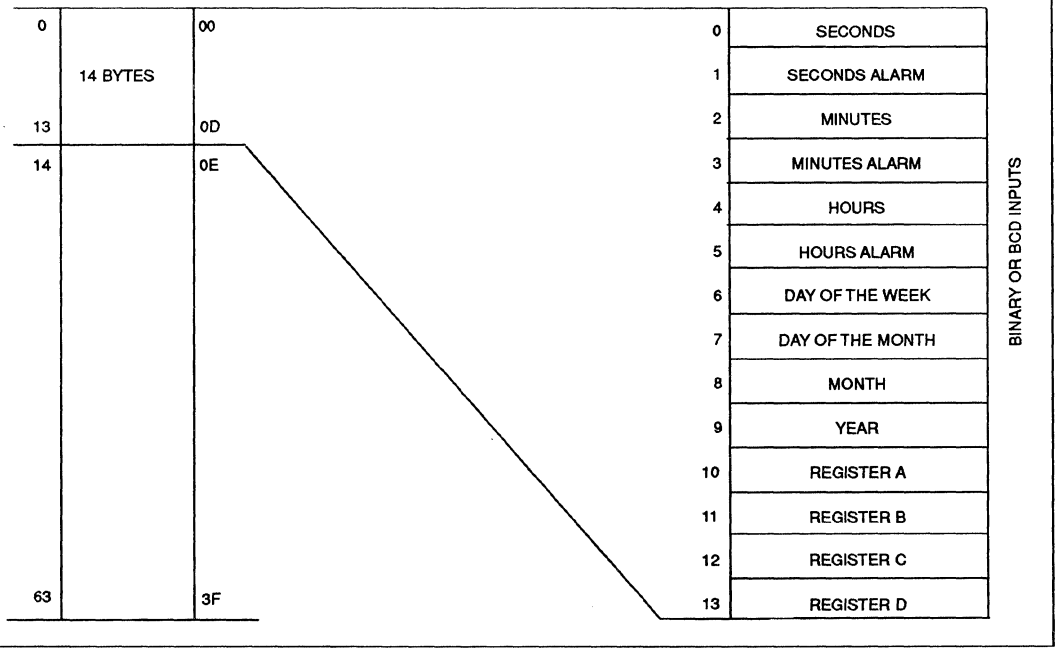
ADDRESS MAP

The address map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

FIGURE 2: ADDRESS MAP DS1287



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one.

The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TABLE 2: TIME, CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

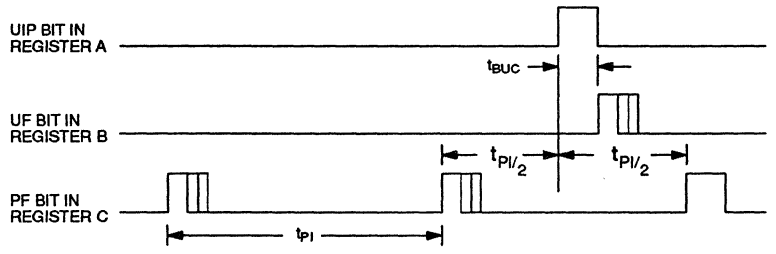
The DS1287 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

FIGURE 3: UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1287 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS1287.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE).

Any time the IRQF bit is a one, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{\text{IRQ}}$ pin will go low and a one will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1

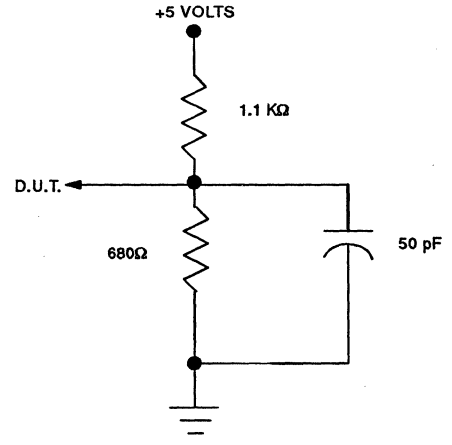
CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5V TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R,t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

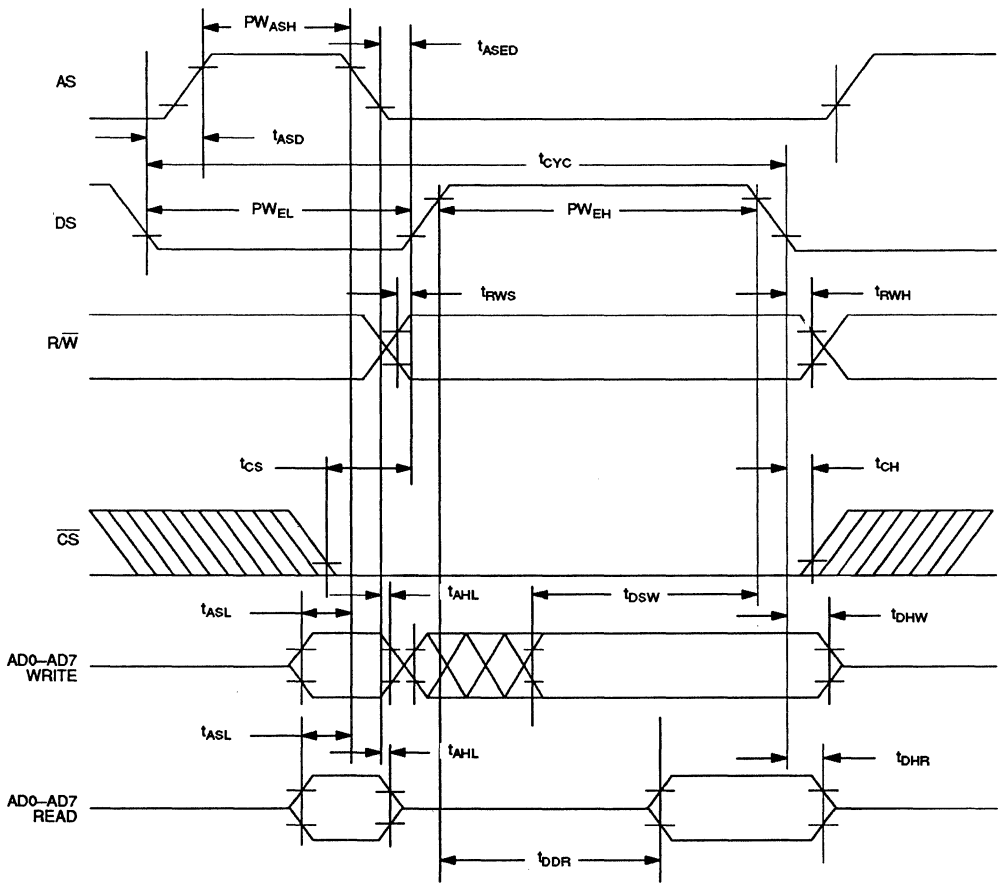
NOTES

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20 KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin,and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

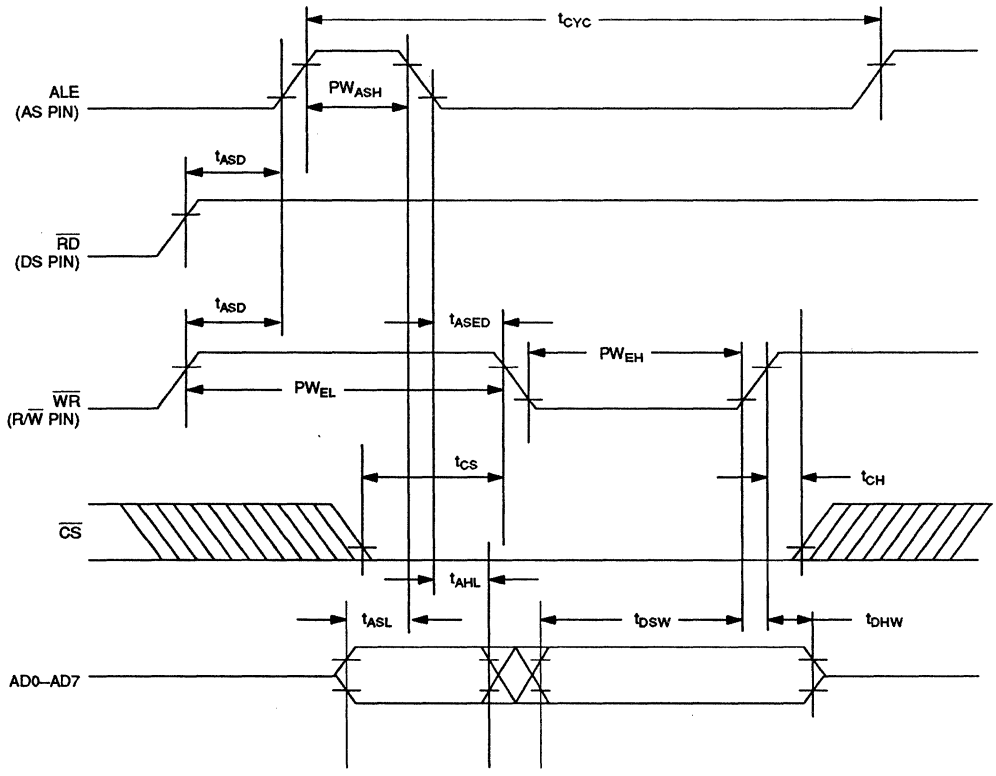
FIGURE 4: OUTPUT LOAD



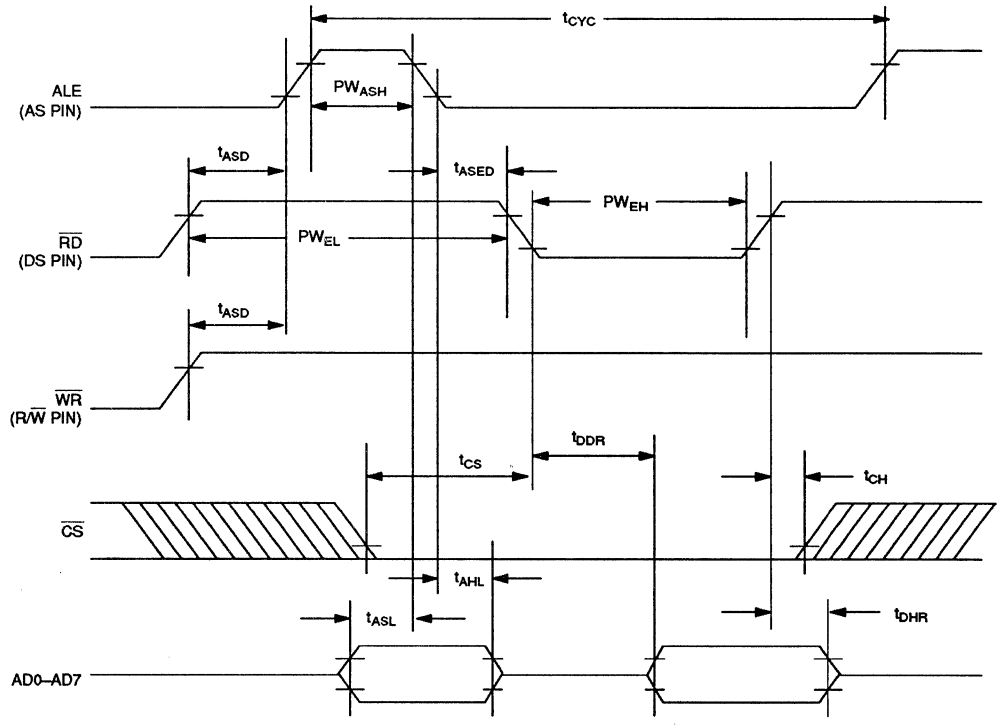
DS1287 BUS TIMING FOR MOTOROLA INTERFACE



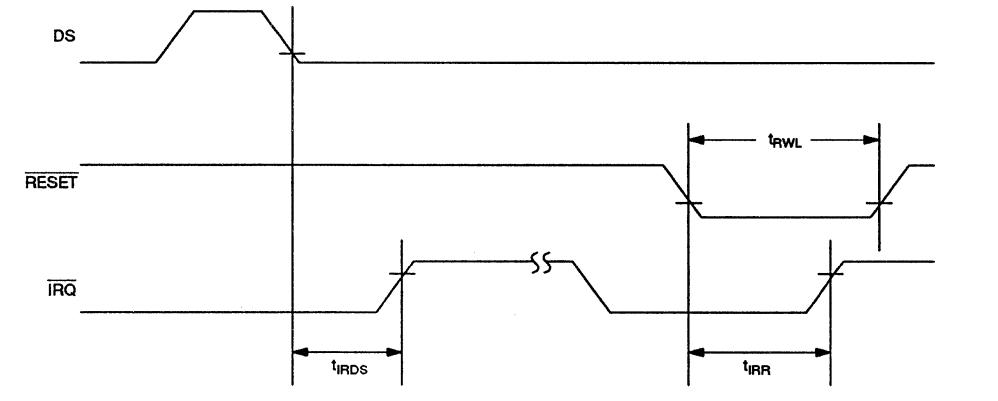
DS1287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



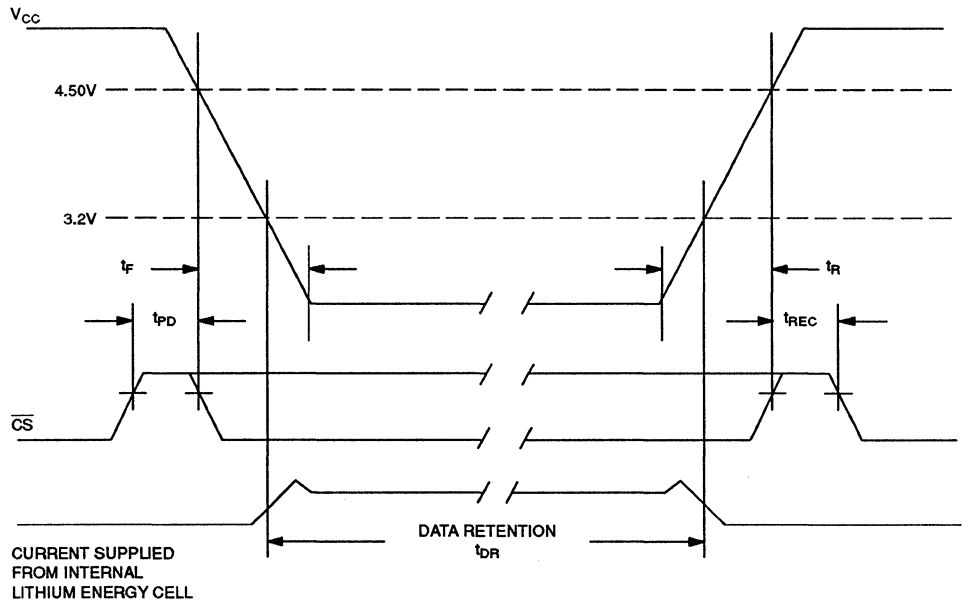
DS1287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS1287 IRQ RELEASE DELAY TIMING



POWER DOWN/POWER UP TIMING



POWER DOWN/POWER UP TIMING						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

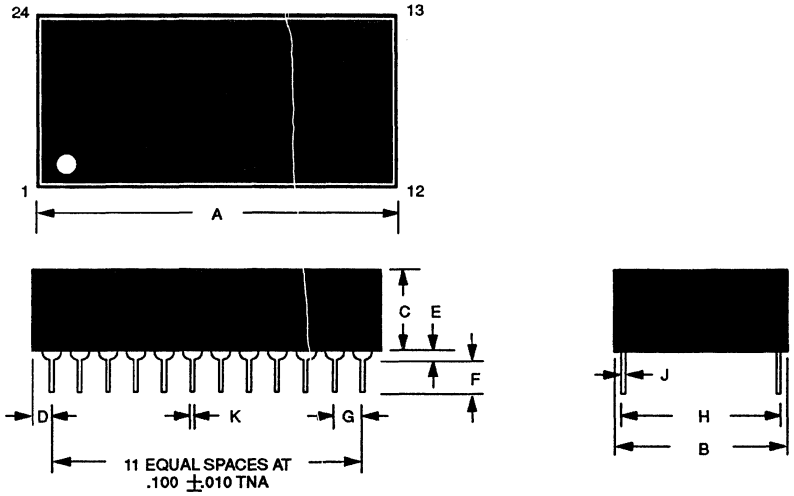
NOTE

The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

DS1287 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, 20, 21 AND 22 ARE MISSING BY DESIGN.

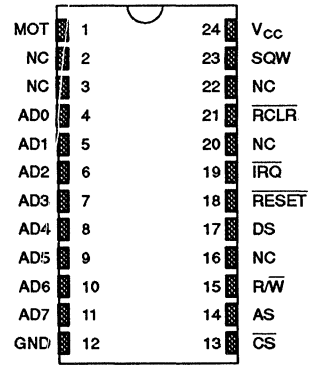
DALLAS SEMICONDUCTOR

DS1287A
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

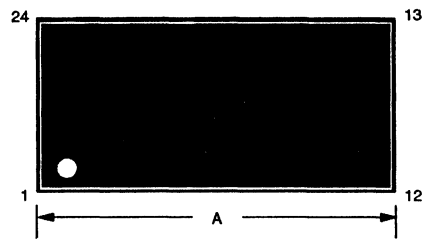
PIN DESCRIPTION

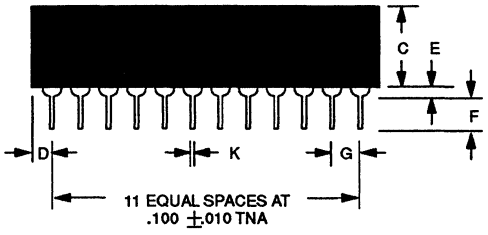
AD0–AD7	-	Multiplexed address/data bus
NC	-	No connection
MOT	-	Bus type selection
$\overline{CS}$	-	Chip select
AS	-	Address strobe
R/$\overline{W}$	-	Read/write input
DS	-	Data strobe
$\overline{RESET}$	-	Reset input
$\overline{IRQ}$	-	Interrupt request output
SQW	-	Square wave output
V_{CC}	-	+5 volt supply
GND	-	Ground
$\overline{RCLR}$	-	RAM clear

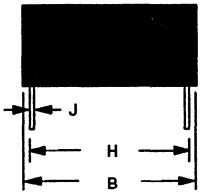
DESCRIPTION

The DS1287A is identical to the DS1287 with the addition of the RAM clear pin. The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery backup mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) an not to be driven with external buffers. All other operation, description and specification is identical to the DS1287.

DS1287A REAL TIME CLOCK PLUS RAM







PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20 AND 22 ARE MISSING BY DESIGN.

NOTE: THIS DEVICE CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL WHICH WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

6

DALLAS SEMICONDUCTOR

DS12885, DS12885Q
Real Time Clock

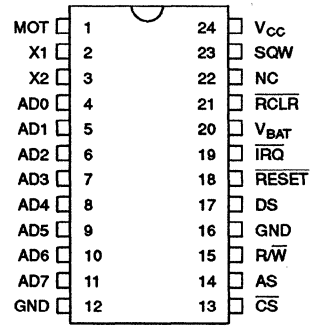
FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818B and DS1285
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µA to 500 ms
  - End of clock update cycle
- Optional 28-pin PLCC surface mount package

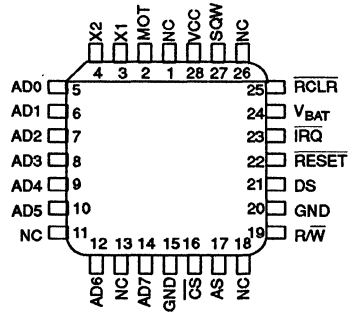
DESCRIPTION

The DS12885 Real Time Clock plus RAM is designed to be a direct replacement for the DS1285. The DS12885 is identical in form, fit, and function to the DS1285, and has an additional 114 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS12887 data sheet.

PIN ASSIGNMENT



DS12885 24-PIN DIP
DS12885S 24-PIN SOIC



DS12885Q 8-PIN PLCC

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground
X1,X2	-	32.768 kHz Crystal Connections
V_{BAT}	-	+3 volt Battery Input
$\overline{RCLR}$	-	RAM Clear

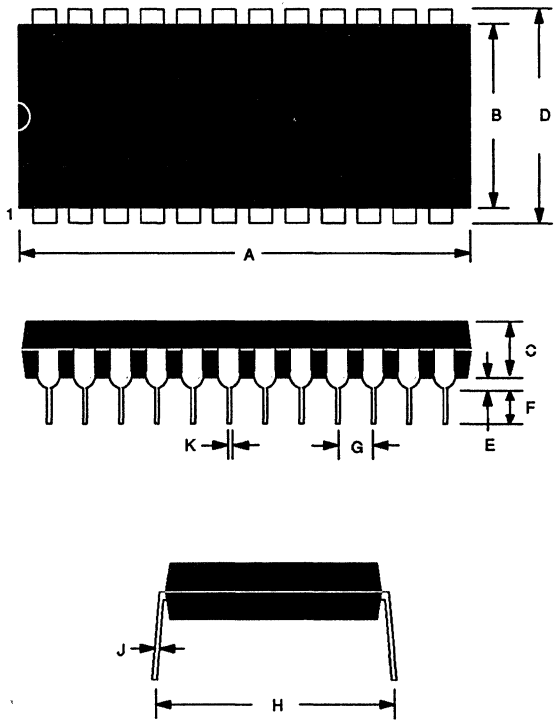
PIN DESCRIPTION

X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S, Seiko part number DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. A variable trimming capacitor may be required for extremely high precision timekeeping applications. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 4 volts for proper operation. A maximum load of .5 µA at 25°C in the absence of power should be used to size the external energy source.

$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.

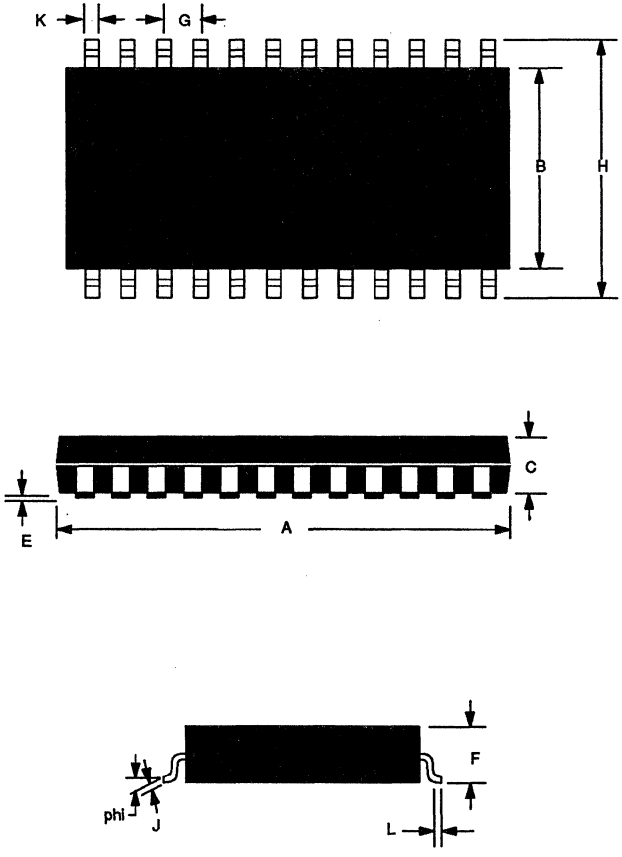
DS12885 24 PIN DIP



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.145	0.165
MM	3.68	4.19
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.559

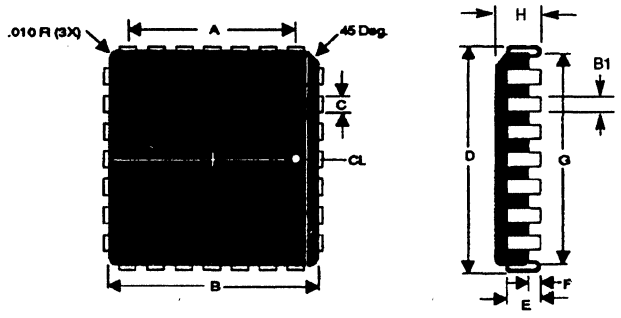
6

DS12885 24 PIN SOIC



PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.406	0.040 1.02
phi	0°	8°

DS12885Q 28 PIN PLCC



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.300 REF 7.62	
B IN. MM	0.442 17.68	0.462 11.73
B1 IN. MM	0.013 0.33	0.021 0.53
C IN. MM	0.027 0.68	0.033 0.84
D IN. MM	0.480 12.2	0.500 12.7
E IN. MM	0.090 2.29	0.120 3.05
F IN. MM	0.020 0.51	MIN MIN
G IN. MM	0.390 9.91	0.430 10.92
H IN. MM	0.165 4.19	0.180 4.57

6

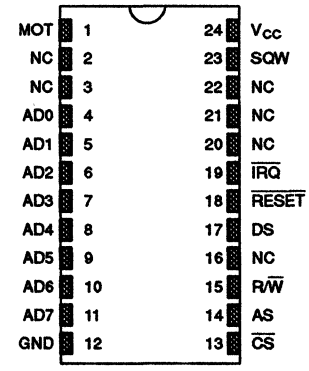
DALLAS SEMICONDUCTOR

DS12887
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground

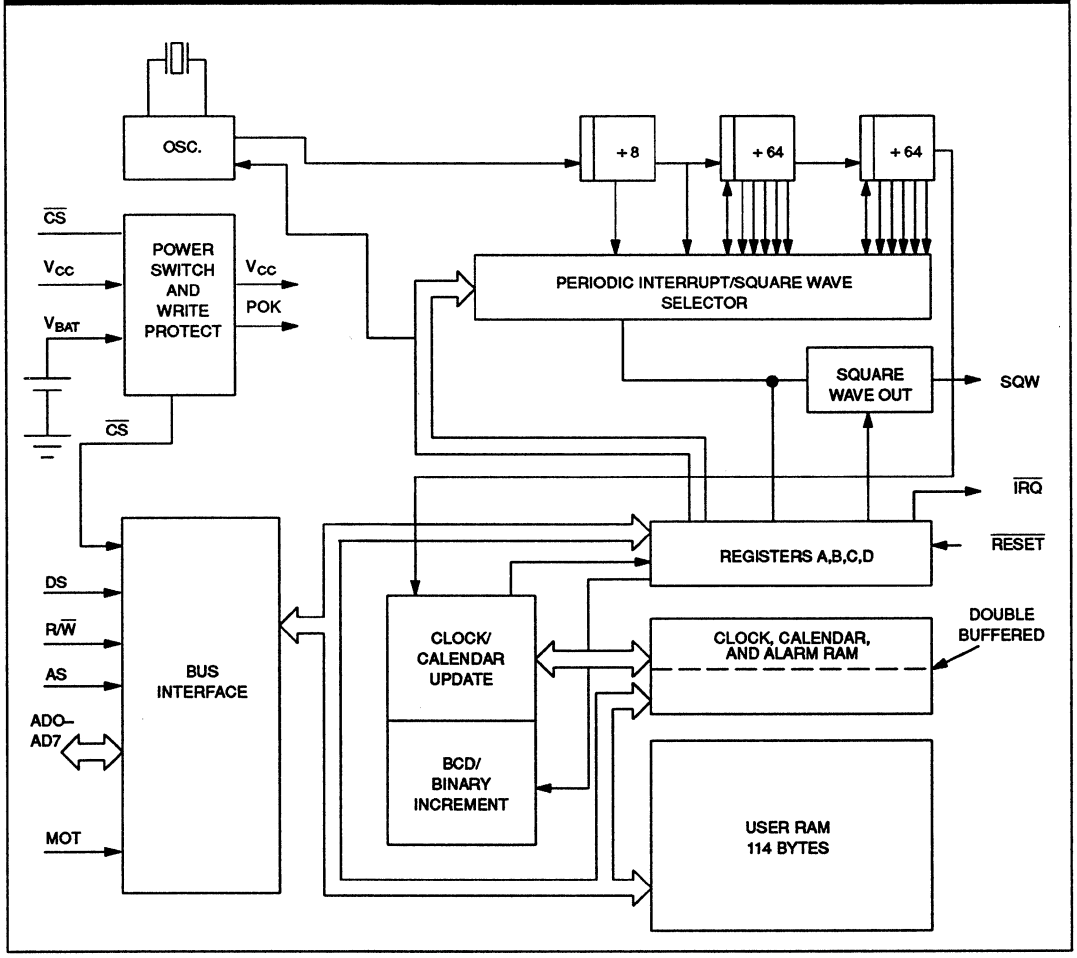
DESCRIPTION

The DS12887 Real Time Clock plus RAM is designed to be a direct replacement for the DS1287. The DS12887 is identical in form, fit, and function to the DS1287, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS12887 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 114 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS12887. The following paragraphs describe the function of each pin.

FIGURE 1: BLOCK DIAGRAM DS12887



POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS12887 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS12887 is, therefore, write-protected. When the DS12887 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

TABLE 1: PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS12887 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS12887 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS12887 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS12887.

DS (Data Strobe or Read Input) - The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS12887 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS12887 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS12887 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input)-The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS12887 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS12887 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS12887 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{RESET}$ (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS12887 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the follow ing occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable ($\overline{SQWE}$) bit is cleared to zero.

J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{RESET}$ can be connected to V_{CC}. This connection will allow the DS12887 to go in and out of power fail without affecting any of the control registers.

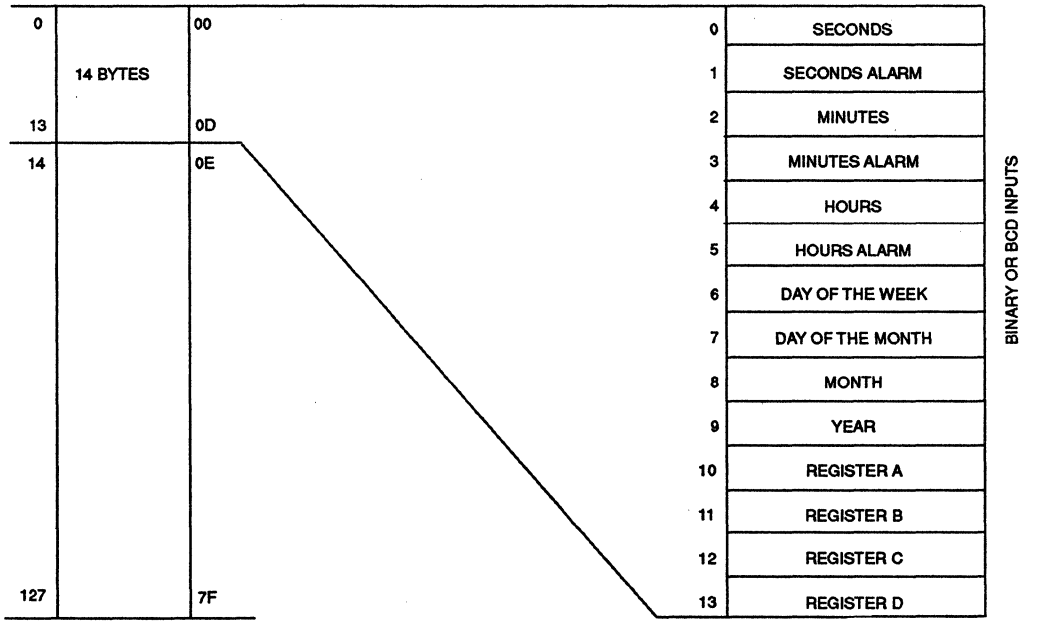
ADDRESS MAP

The address map of the DS12887 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

FIGURE 2: ADDRESS MAP DS12887



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TABLE 2: TIME, CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

6

NONVOLATILE RAM

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS12887. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts a re lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12887. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS12887 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

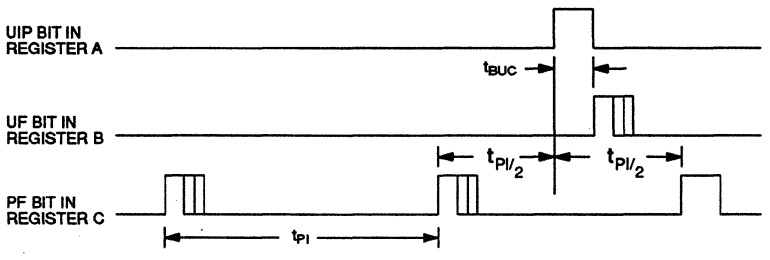
The DS12887 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2} + t_{BUC}$) to ensure that data is not read during the update cycle.

FIGURE 3: UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS12887 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS12887.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS12887 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to zero. The internal functions of the DS12887 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a one, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF

A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{\text{IRQ}}$ pin will go low and a one will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5 TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	4
Input Current	I_{MOT}	-1.0		+500	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1
Write Protect Voltage	V_{TP}	4.0	4.25	4.5	V	

CAPACITANCE (t_A = 25°C)

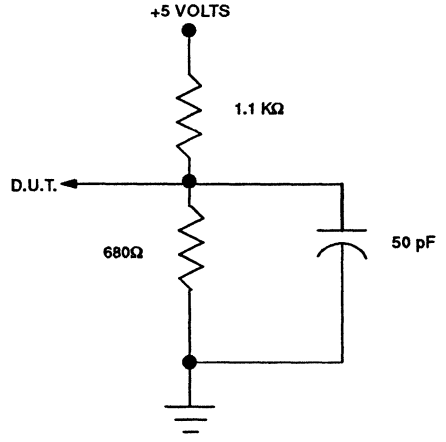
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5V TO 5.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/$\overline{WR}$ Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R,t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

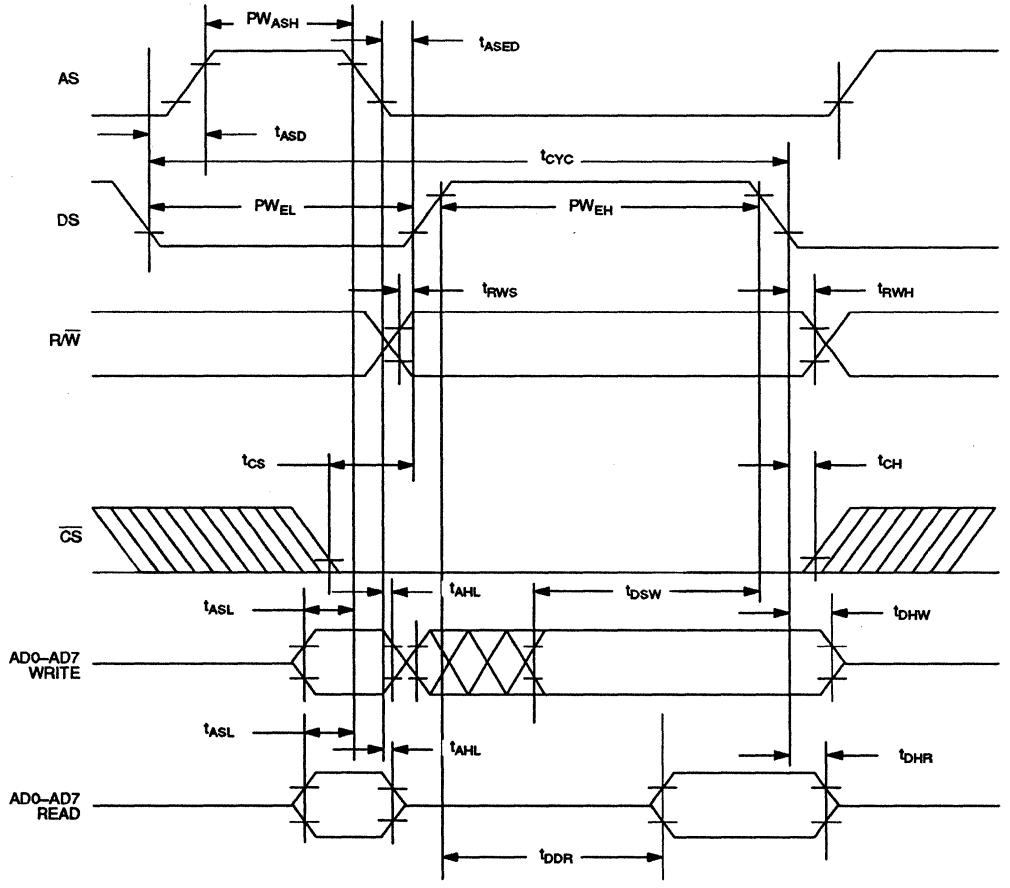
NOTES

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20 KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin,and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

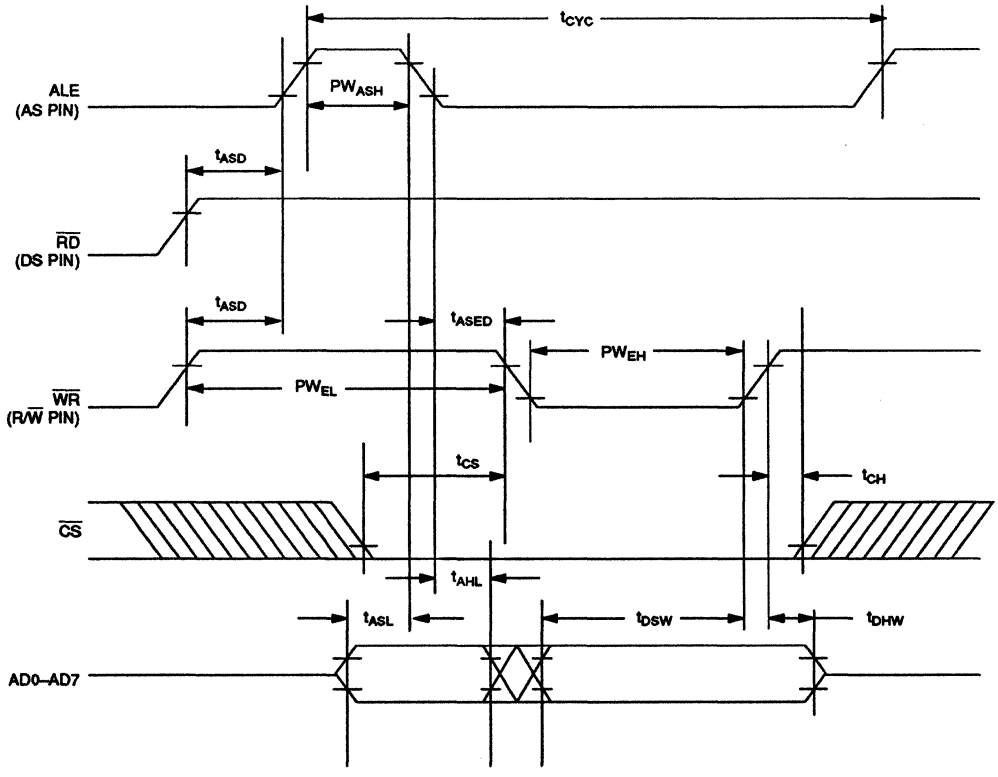
FIGURE 4: OUTPUT LOAD



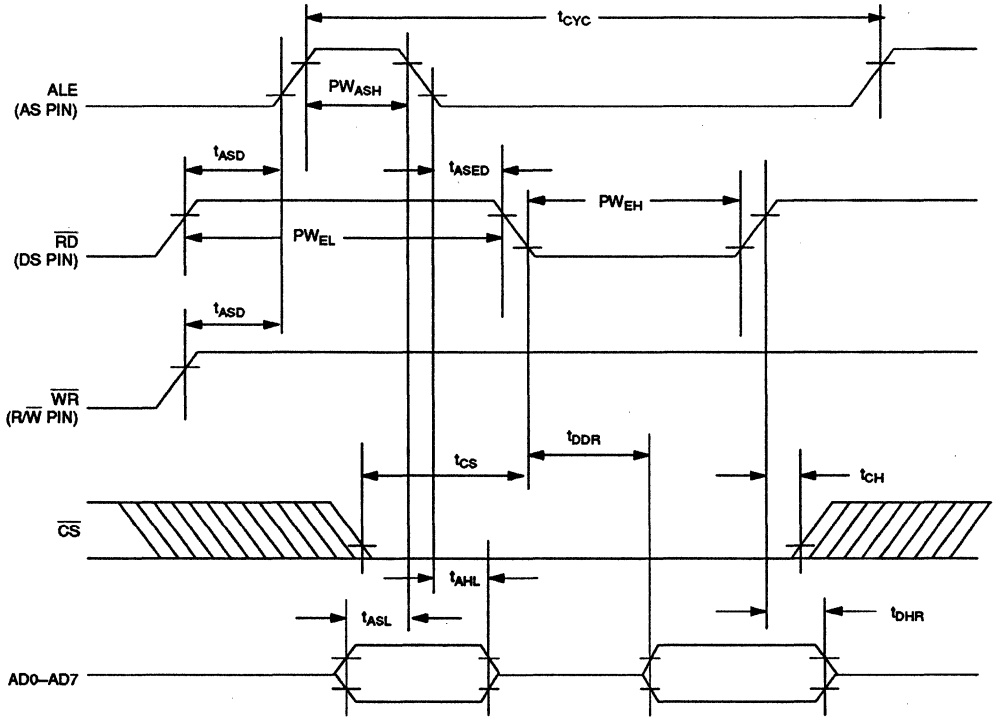
DS12887 BUS TIMING FOR MOTOROLA INTERFACE



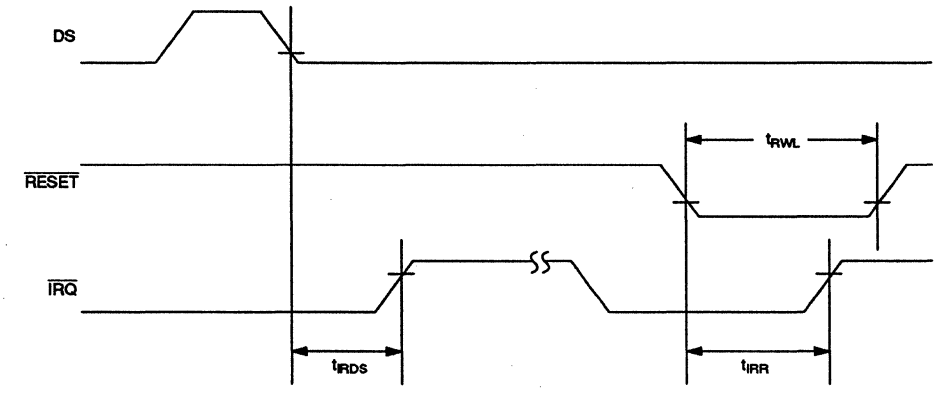
DS12887 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



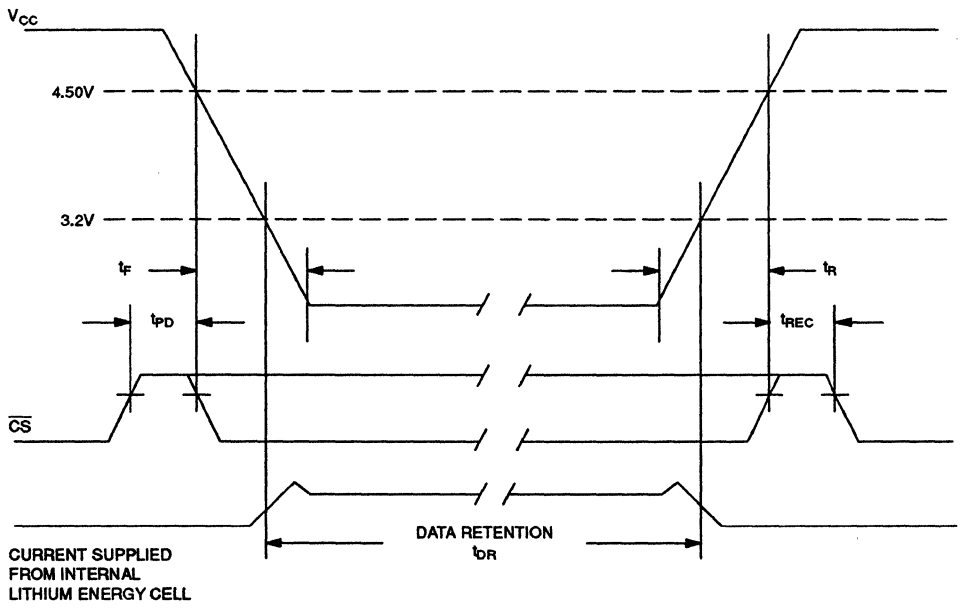
DS12887 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS12887 IRQ RELEASE DELAY TIMING



POWER DOWN/POWER UP TIMING



POWER DOWN/POWER UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	

(t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

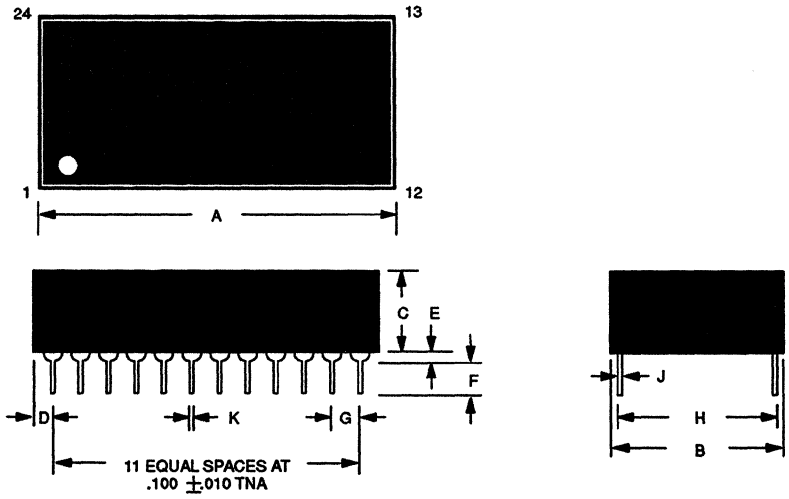
NOTE

The real time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

DS12887 REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20, 21 AND 22 ARE MISSING BY DESIGN.

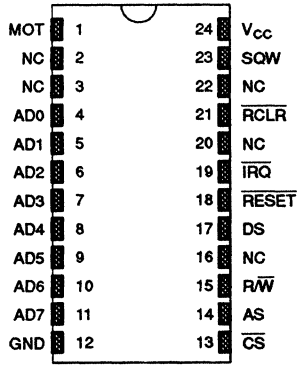
DALLAS SEMICONDUCTOR

DS12887A
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24 PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

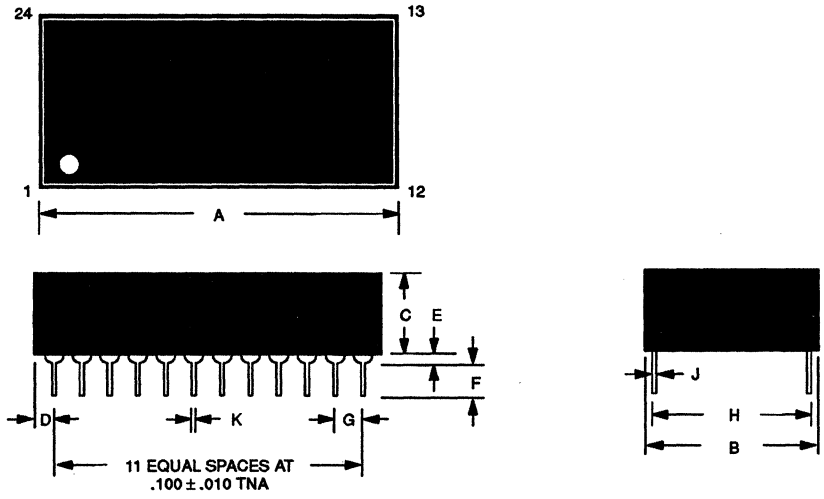
AD0-AD7	-	Multiplexed Address/Data Bus
NC	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
$\overline{RCLR}$	-	RAM Clear
GND	-	Ground

6

DESCRIPTION

The DS12887A Real Time Clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operation, description and specification is identical to the DS12887.

DS12887A REAL TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	MIN	MAX
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20 AND 22 ARE MISSING BY DESIGN.

NOTE: THIS DEVICE CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL WHICH WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

DALLAS SEMICONDUCTOR

DS1385/DS1387
RAMified Real Time Clock 4K x 8

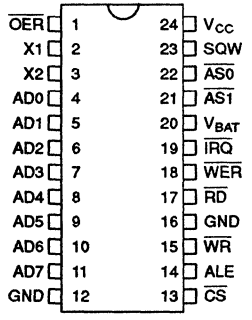
FEATURES

- Upgraded IBM AT computer clock/calendar with 4K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - 4K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- Available as chip (DS1385 or DS1385S) or stand alone module with embedded lithium battery and crystal (DS1387)

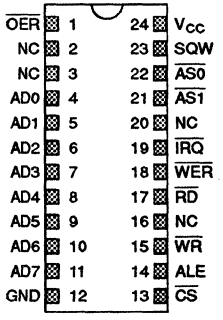
ORDERING INFORMATION

DS1385	RTC Chip; 24 pin DIP
DS1385S	RTC Chip; 28 pin SOIC
DS1387	RTC Module; 24 pin DIP

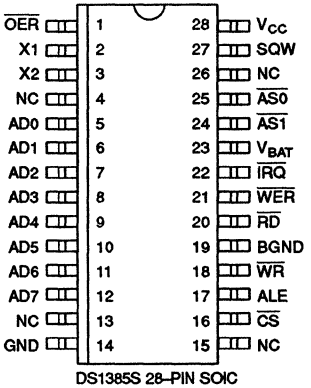
PIN ASSIGNMENT



DS1385 24-PIN DIP
(600 MIL)



DS1387 24-PIN
ENCAPSULATED PACKAGE
(740 MIL FLUSH)



DS1385S 28-PIN SOIC
(330 MIL)

PIN DESCRIPTION

$\overline{OER}$	-	RAM Output Enable
X1	-	Crystal Input
X2	-	Crystal Output
AD0-AD7	-	Mux'ed Address/Data Bus
$\overline{CS}$	-	RTC Chip Select Input
ALE	-	RTC Address Strobe
$\overline{WR}$	-	RTC Write Data Strobe
$\overline{RD}$	-	RTC Read Data Strobe
$\overline{WER}$	-	RAM Write Data Strobe
$\overline{IRQ}$	-	Interrupt Request Output
$\overline{AS1}$	-	RAM Upper Address Strobe
$\overline{AS0}$	-	RAM Lower Address Strobe
SQW	-	Square Wave Output
V_{CC}	-	+5V Supply
GND	-	Ground
V_{BAT}	-	Battery + Supply
BGND	-	Battery Ground
NC	-	No Connection

DESCRIPTION

The DS1385/DS1387 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 4K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system V_{CC} by a lithium battery.

The 4K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1385/DS1387. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the V_{BAT} pin in the case of the DS1385, or to the internal battery in the case of the DS1387. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

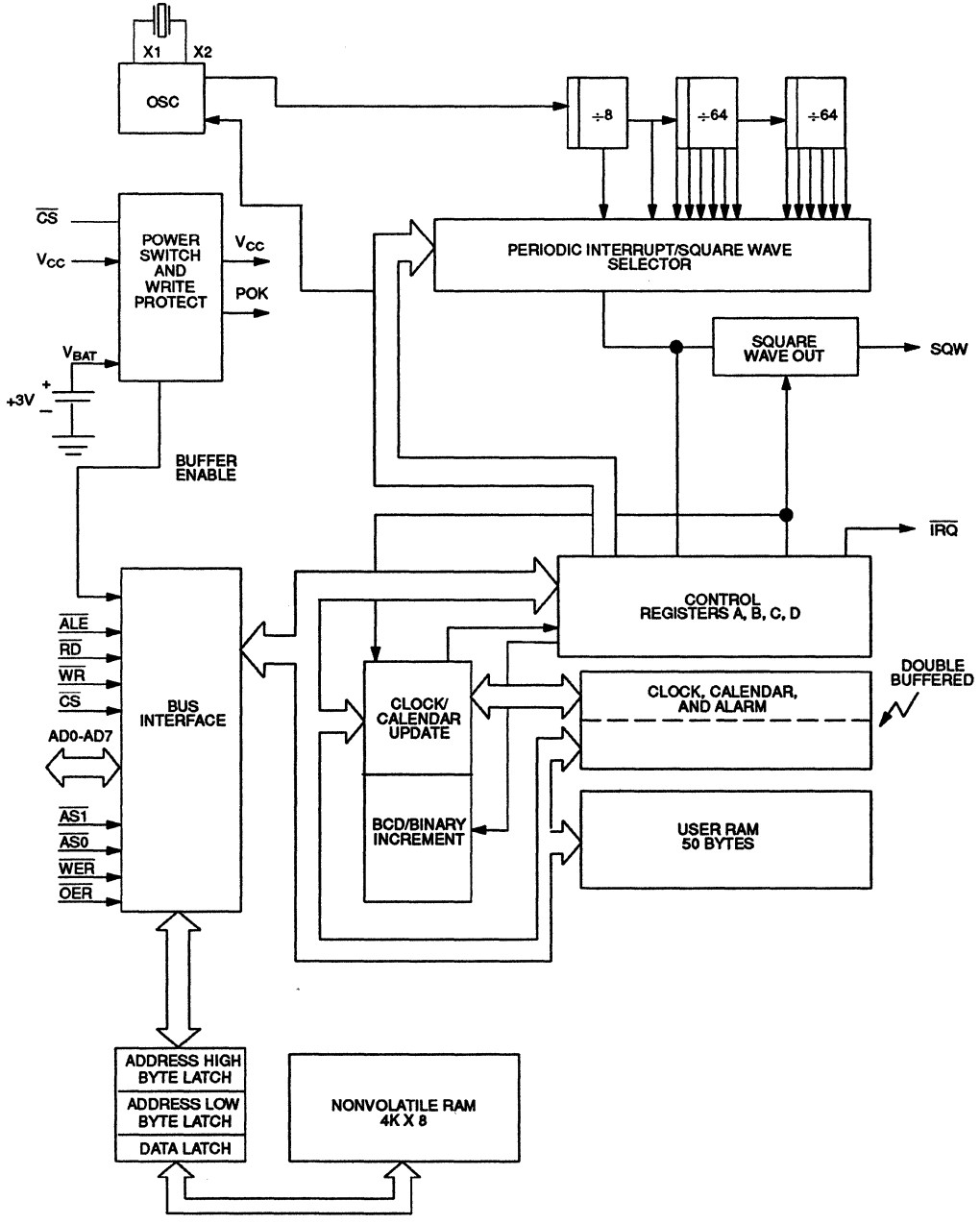
SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1385/DS1387 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1385/DS1387 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle, the DS1385/DS1387 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1385/DS1387.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1385/DS1387 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

DS1385/DS1387 BLOCK DIAGRAM Figure 1



$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1385/DS1387 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1385/DS1387 that can be tied to an interrupt input on a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application program normally reads the C register.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 4K x 8 RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper four bits of the 4K x 8 RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1385/DS1387 drives the bus with RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and is used to perform writes to the 4K x 8 RAM portion of the DS1385/DS1387.

(DS1385 ONLY)
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor Corporation. Order part number DS9032.

V_{BAT}, BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should in the absence of power be used to size the external energy source.

ADDRESS MAP

The address map of the DS1385/DS1387 is shown in Figure 2. The address map consists of the RTC and the 4K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

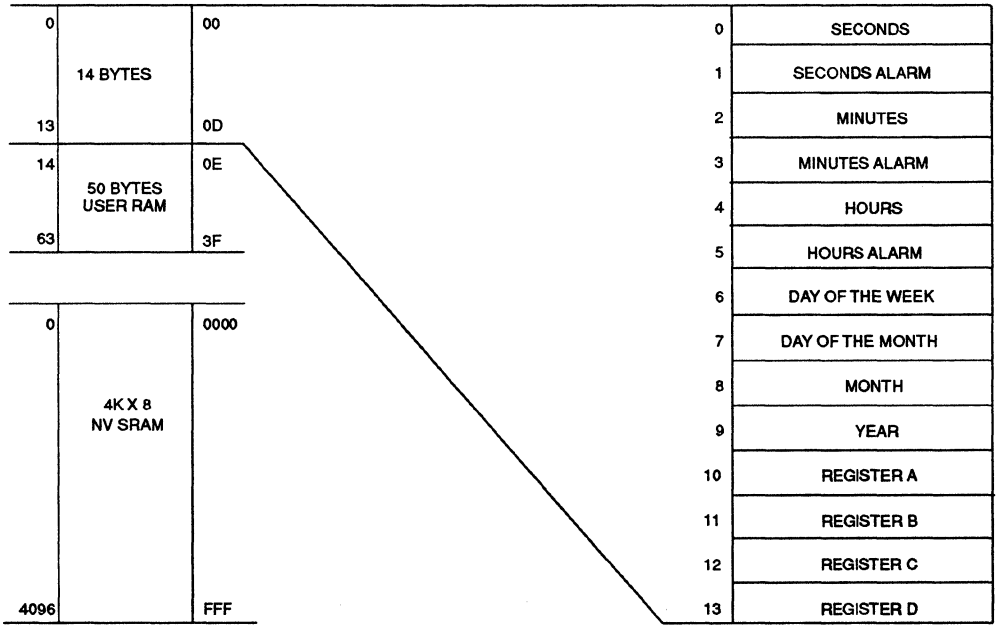
1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The RTC is the same in the DS1287 with the following exceptions:

1. The MOT pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
2. The $\overline{RESET}$ pin on the DS1285/DS1287 is not present on the DS1385/DS1387. The DS1385/DS1387 will operate the same as the DS1285/DS1287 with $\overline{RESET}$ tied to V_{CC}.

ADDRESS MAP DS1385/DS1387 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1385/DS1387. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1385/DS1387 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

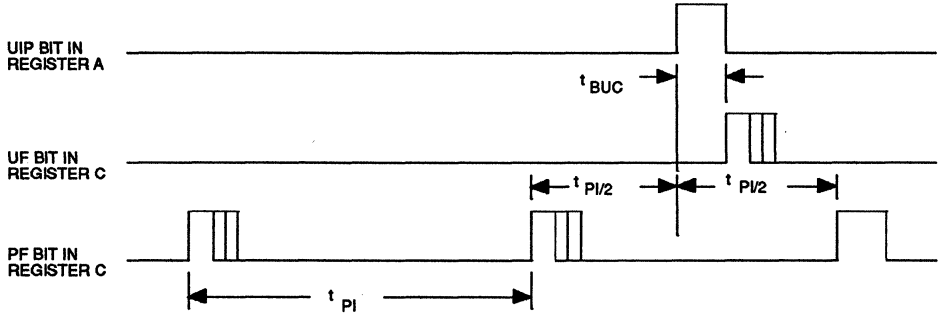
The DS1385/DS1387 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1385/DS1387 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1385/DS1387.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1385/DS1387 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1385/DS1387 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • ALE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

4K X 8 RAM

The DS1385/DS1387 provides 4K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 4K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to FFFH.

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$, are used to access the 4K x 8 SRAM. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 (AS1) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 4-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 4K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 50 bytes of user RAM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

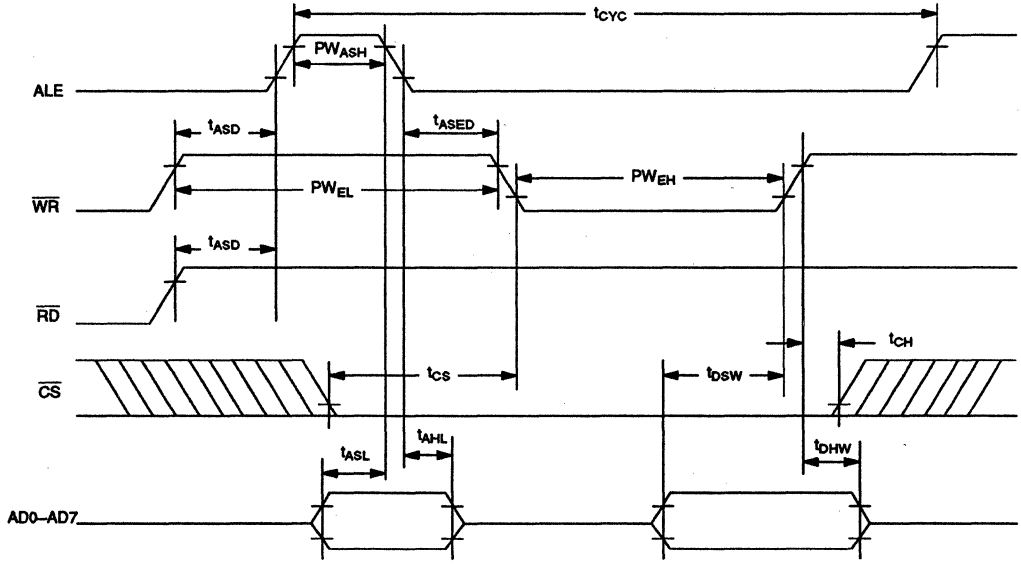
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$, $\overline{OER}$, and $\overline{WER}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,4
Output @ 0.4V	I_{OL}			4.0	mA	1

RTC AC TIMING CHARACTERISTICS

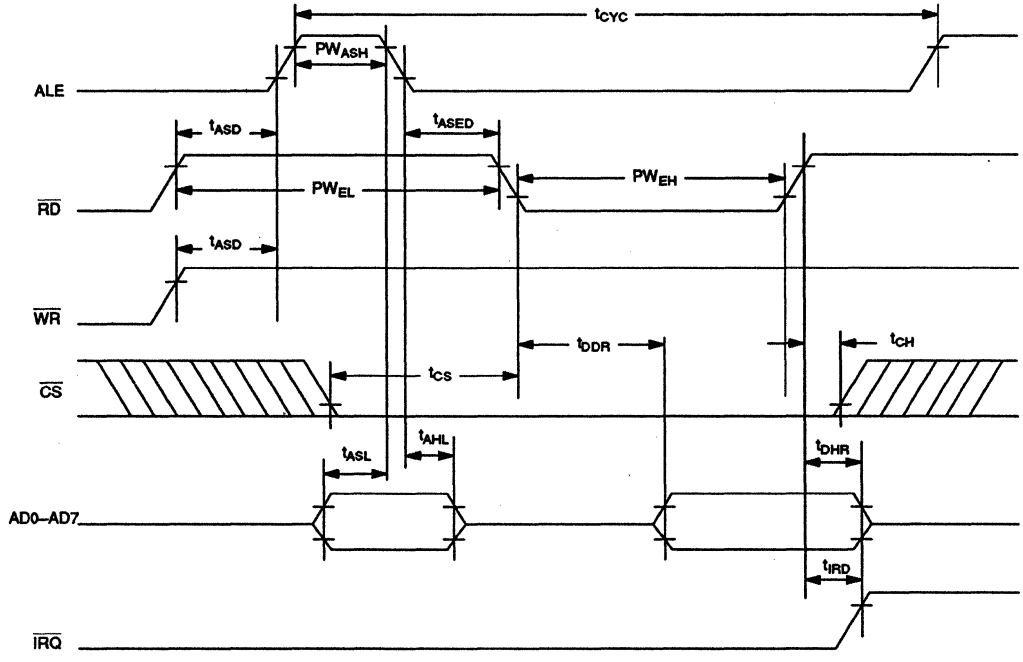
(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{EH}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{EL}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time to Write	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1385/DS1387 BUS TIMING FOR WRITE CYCLE TO RTC



DS1385/DS1387 BUS TIMING FOR READ CYCLE TO RTC



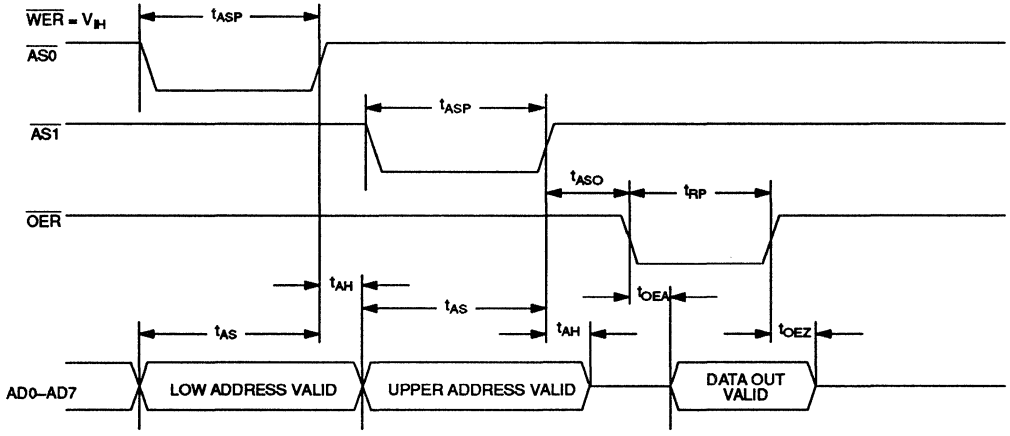
4K X 8 AC TIMING CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

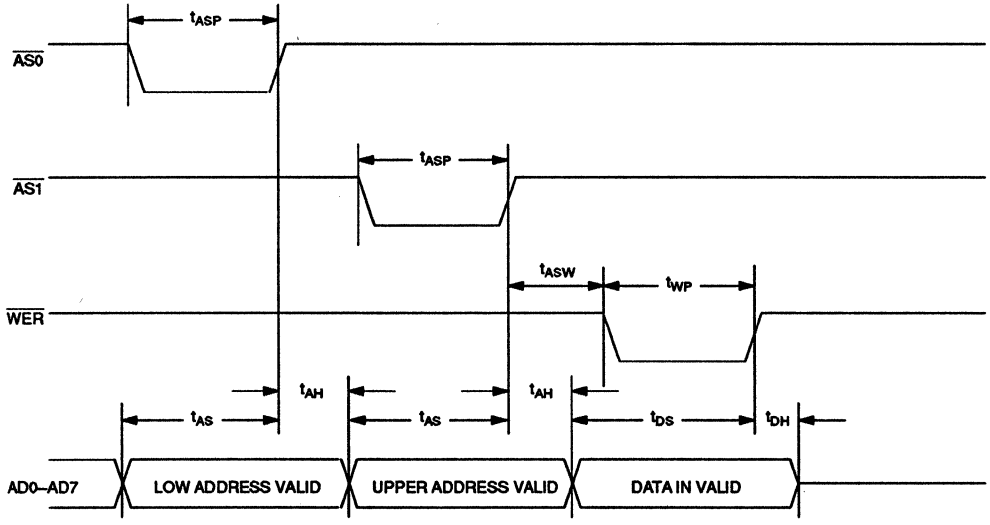
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	200			ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

6

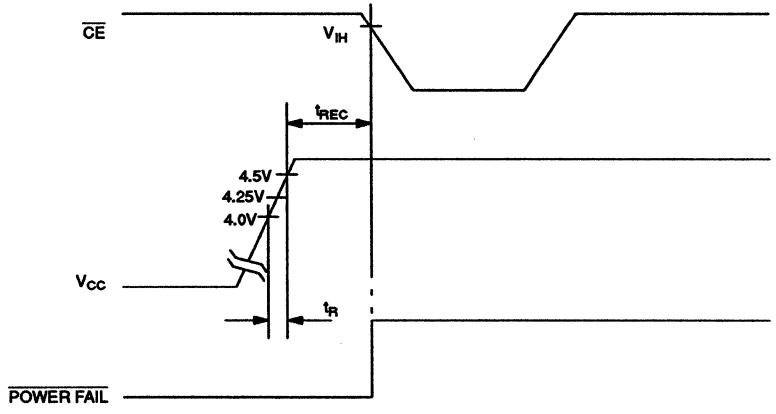
BUS TIMING FOR READ CYCLE TO 4K X 8 NV SRAM



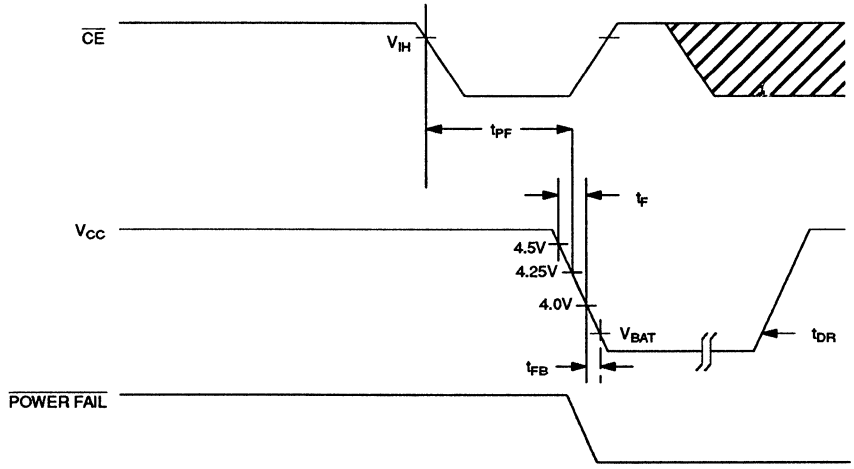
BUS TIMING FOR WRITE CYCLE TO 4K X 8 SRAM



POWER-UP CONDITION



POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

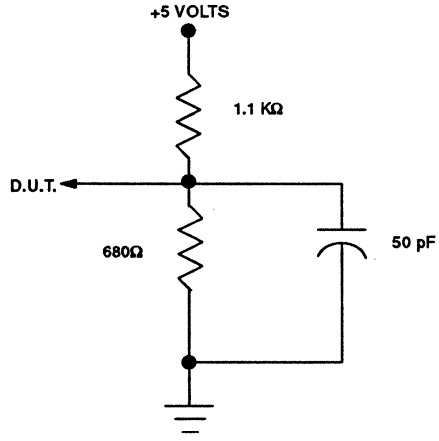
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

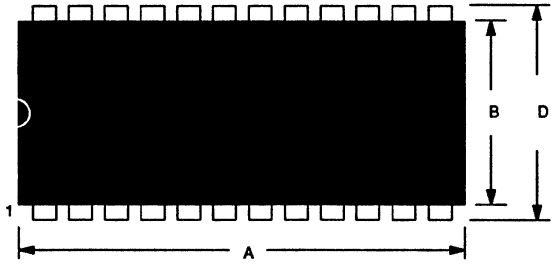
NOTES

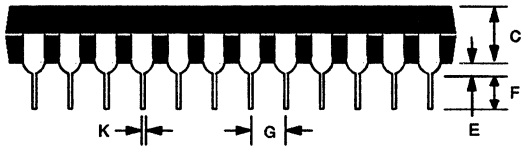
1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 4.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 4.
8. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1385 and DS1385S only.

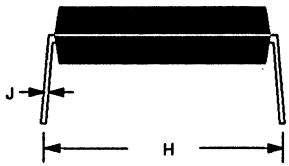
OUTPUT LOAD Figure 4



DS1385 24 PIN DIP

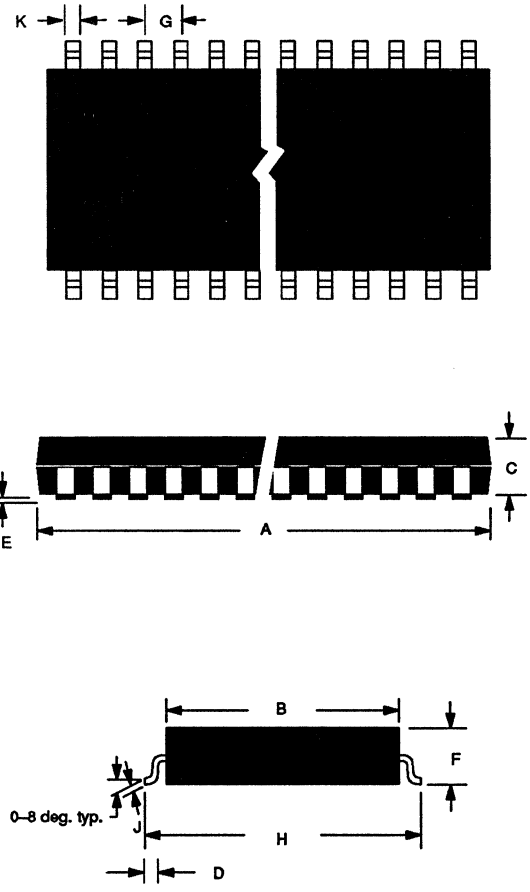






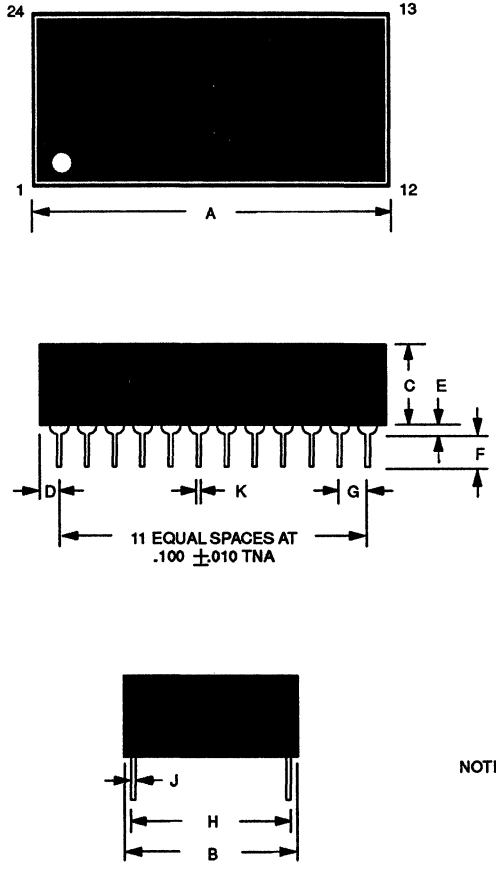
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.245 31.62	1.270 32.26
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

DS1385S 28 PIN SOIC



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

DS1387 24 PIN 740 MIL FLUSH ENCAPSULATED



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

6

DALLAS SEMICONDUCTOR

DS1386
RAMified Watchdog Timekeeper

FEATURES

- 8K or 32K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 28-pin JEDEC footprint when lower justified
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave output
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC}
- Interrupt signals are active in power-down mode

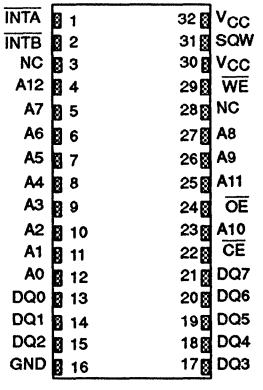
ORDERING INFORMATION

DS1386 XX-XX RTC and NVSRAM; 32 pin DIP

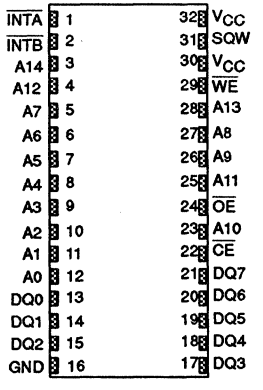
-15 150 ns access
-12 120 ns access

08 8K x 8 NVSRAM
32 32K x 8 NVSRAM

PIN ASSIGNMENT



DS1386 8K x 8
32-Pin Encapsulated Package



DS1386 32K x 8
32-Pin Encapsulated Package

PIN DESCRIPTION

$\overline{INTA}$	-	Interrupt Output A
$\overline{INTB}$(INTB)	-	Interrupt Output B
A0-A14	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
SQW	-	Square Wave Output
NC	-	No Connection

DESCRIPTION

The DS1386 RAMified Watchdog Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1386 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 8K or 32K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Timekeeper information includes hundredths of seconds, seconds, minutes,

hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

OPERATION - READ REGISTERS

The DS1386 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A14) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1386 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention . However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

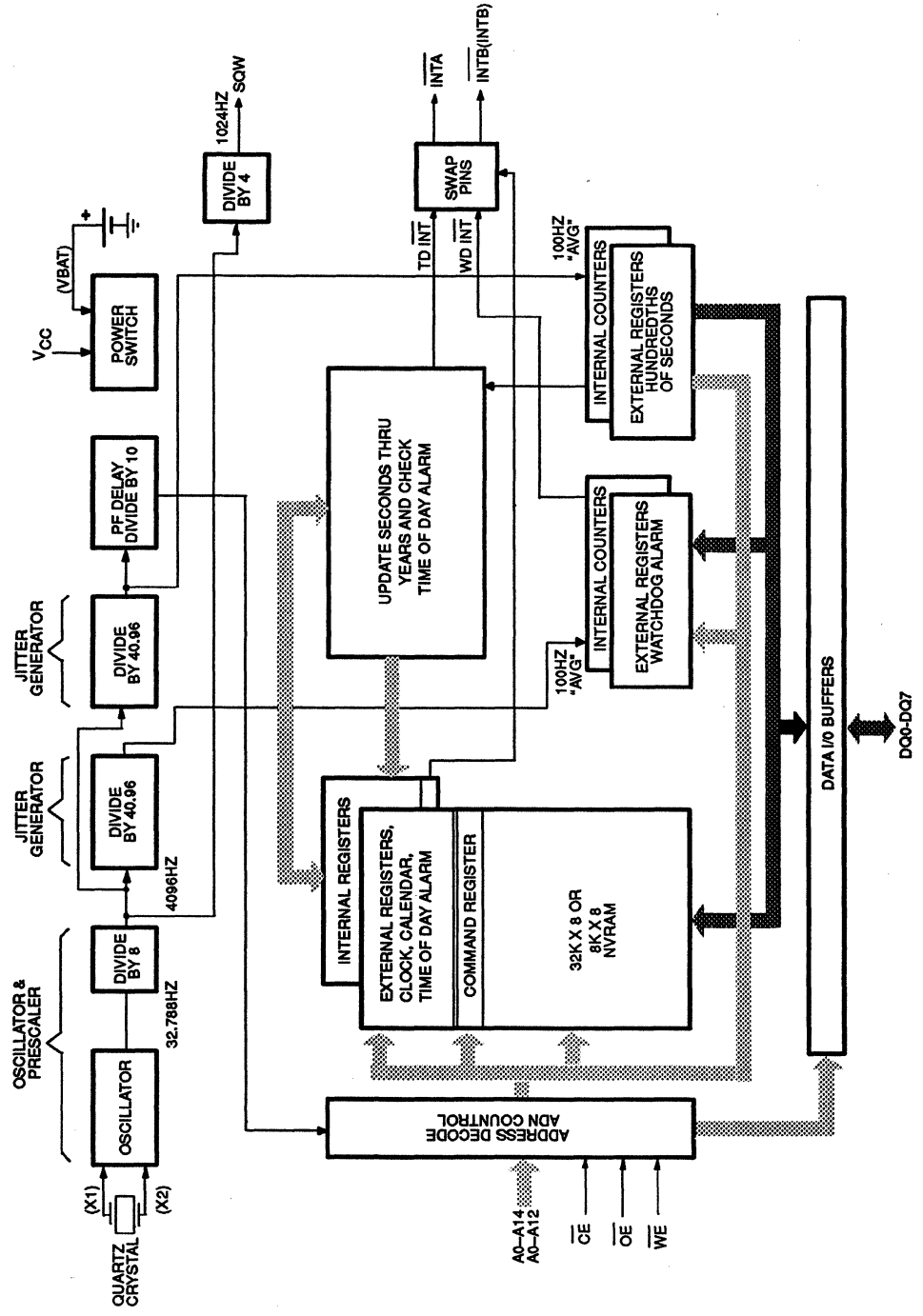
DATA RETENTION

The RAMified Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1386 constantly monitors V_{CC}. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 200 ms.

RAMIFIED TIMEKEEPER REGISTERS

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) copies of the timekeeping data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 8K or 32K bytes of RAM and the 14 external timekeeping registers are accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Registers E through 1FFF or 7FFF are user bytes and can be used to maintain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic 0, $\overline{EOSC}$ (Bit 7) enables the Real Time Clock oscillator. This bit is set to logic 1 as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 31). When set to logic 0, the Square Wave Output Pin will output a 1024 Hz Square Wave Signal. When set to logic 1 the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic 1, the 12 Hour Format is selected. In the 12 Hour Format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24 Hour Mode, bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic 0. This will freeze the External Time of Day Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic 1, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME OF DAY ALARM REGISTERS

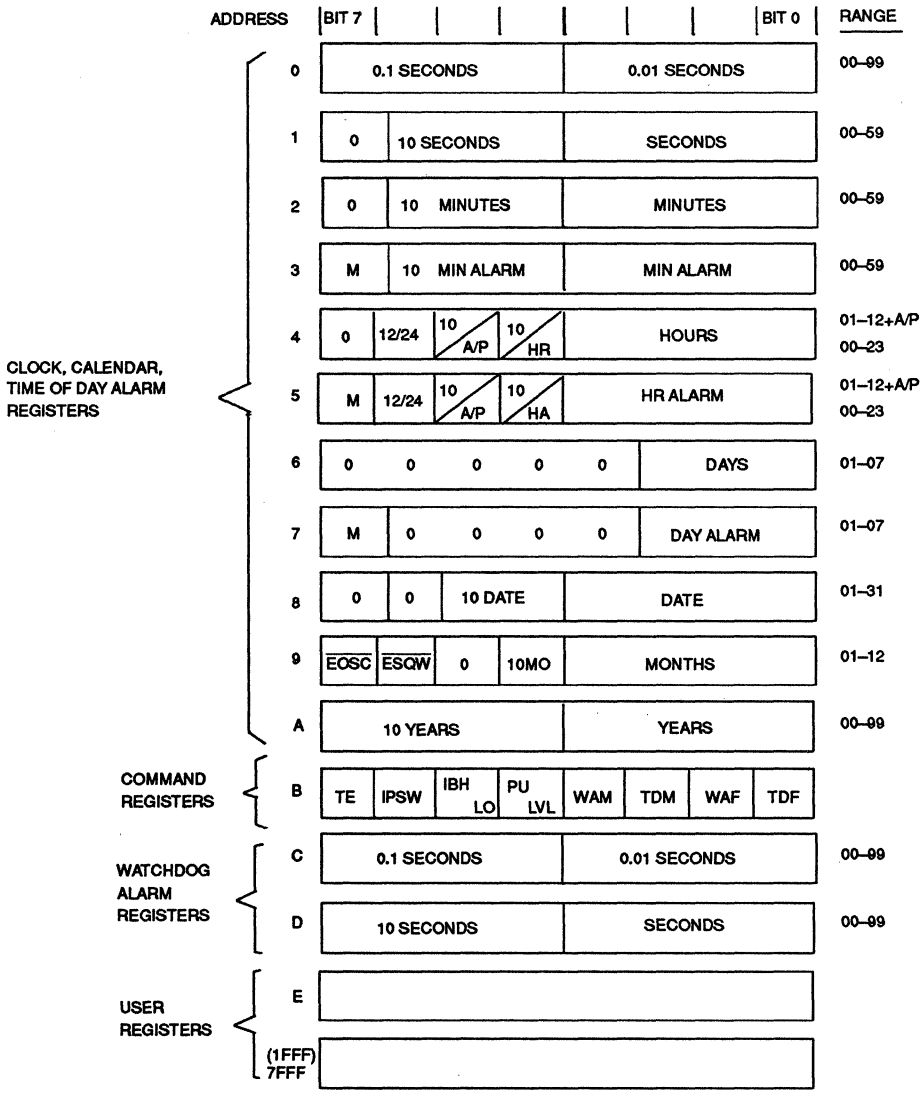
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic 0, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic 1. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count- down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

DS1386 RAMIFIED WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3)MINUTES	(5)HOURS	(7)DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, $\overline{INTA}$ is the Time of Day Alarm and INTB/($\overline{INTB}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{INTA}$ is now the Watchdog Alarm output and INTB/($\overline{INTB}$) is the Time of Day Alarm output.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{INTB}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{INTA}$ and INTB/($\overline{INTB}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{INTA}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{INTB}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1 , the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag - This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO + 70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}			4.0	mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} -0.5	I_{CCS2}		2.0	4.0	mA	
Active Current	I_{CC}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	15	pF	
Output Capacitance	C_{OUT}		7	15	pF	
Input/Output Capacitance	$C_{I/O}$		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

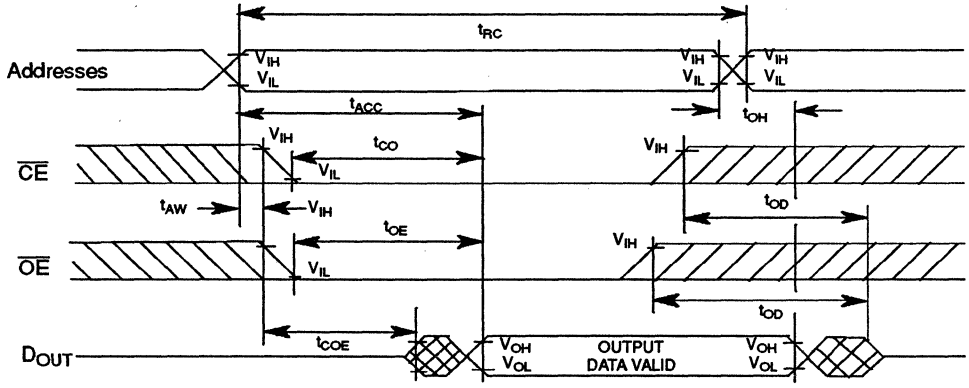
(0°C to +70°C, V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1386XX–12		DS1386XX–15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	1
Address Access Time	t_{ACC}		120		150	ns	
$\overline{CE}$ Access Time	t_{CO}		120		150	ns	
$\overline{OE}$ Access Time	t_{OE}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselect	t_{OD}		40		50	ns	
Output Hold from Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Write Pulse Width	t_{WP}	110		140		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	85		110		ns	4
Data Hold Time	t_{DH}	10		15		ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3		3		ms	11,12

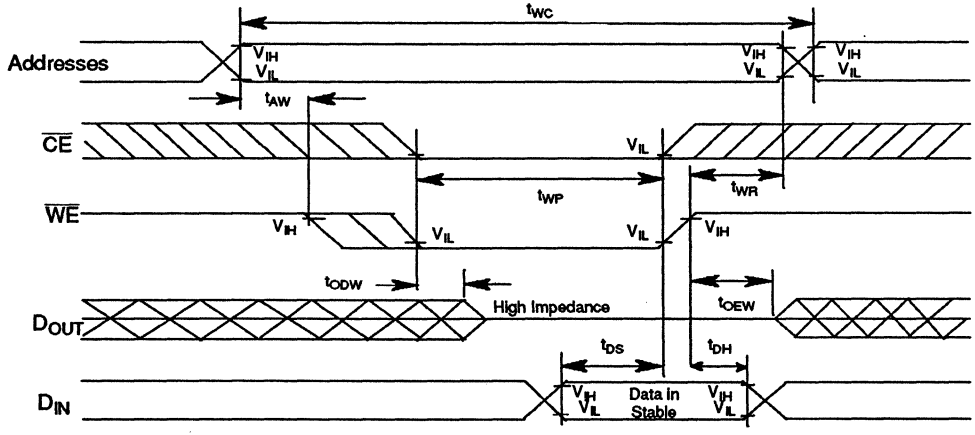
AC TEST CONDITIONS

Input Levels: 0V TO 3V
Transition Times: 5 ns

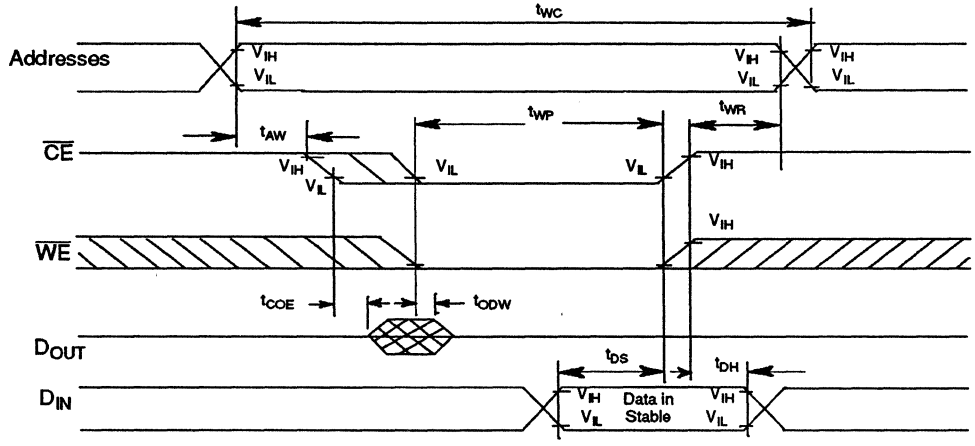
READ CYCLE (Note1)



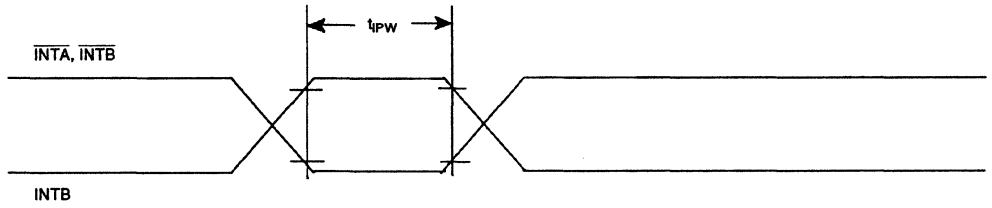
WRITE CYCLE 1 (Notes 2, 6, 7)



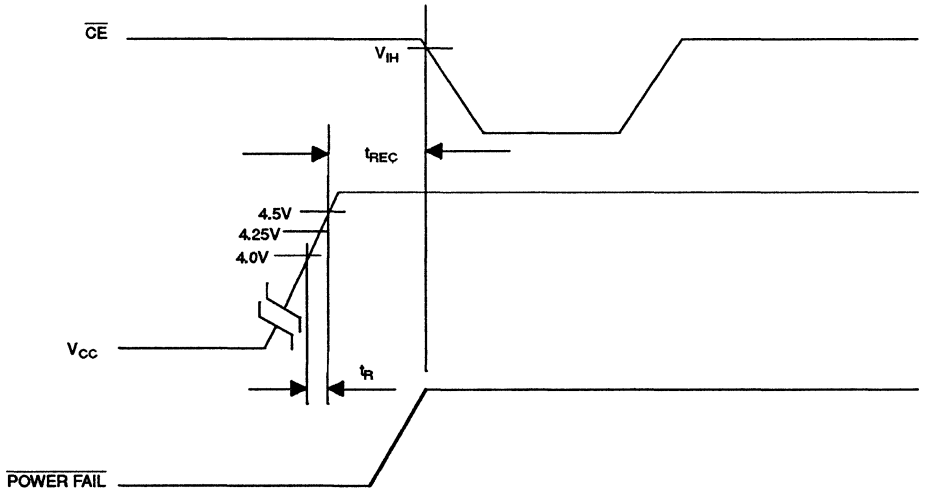
WRITE CYCLE 2 (Notes 2, 8)



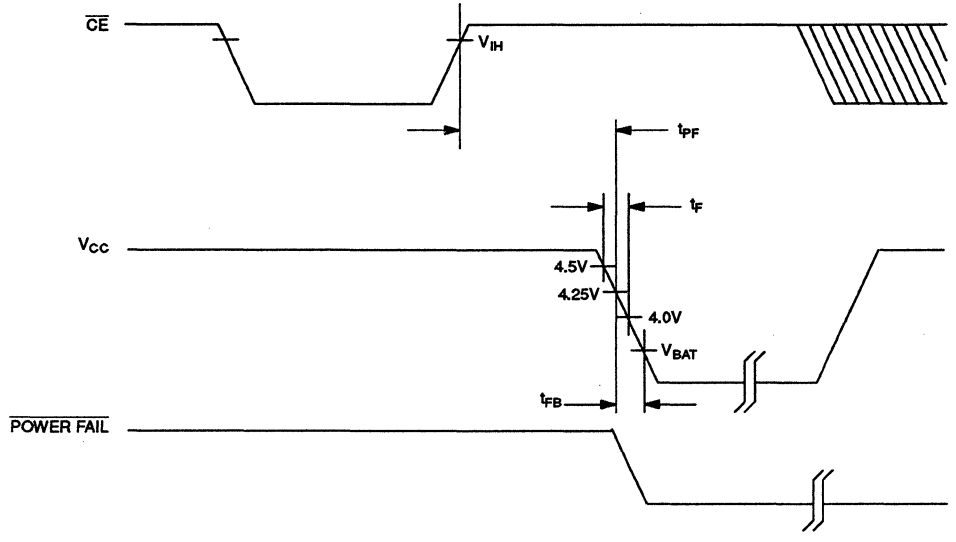
TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-UP CONDITION



POWER-DOWN CONDITION



AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}		0	ns	
Recovery at Power Up	t_{REC}		200	ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300		µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.25V$	10		µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0		µs	
Expected Data Retention	t_{DR}	10		years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

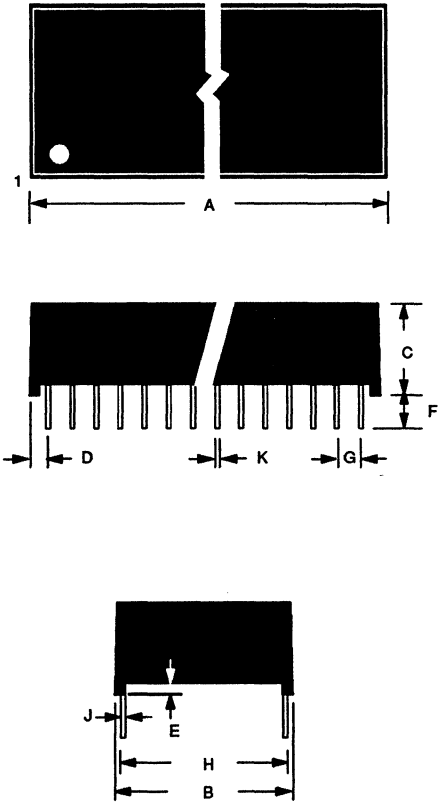
NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1386 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1386 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

6

DALLAS SEMICONDUCTOR

DS1395/DS1397
RAMified Real Time Clock

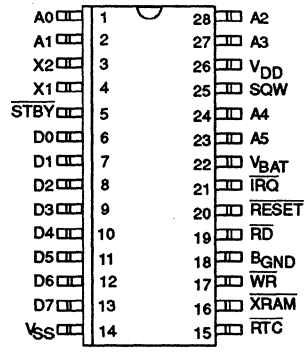
FEATURES

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 kHz mode
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 register/RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general and control registers
  - Separate 4K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- 28-pin JEDEC footprint
- Available as chip (DS1395/DS1395S) or stand alone module with embedded lithium battery and crystal

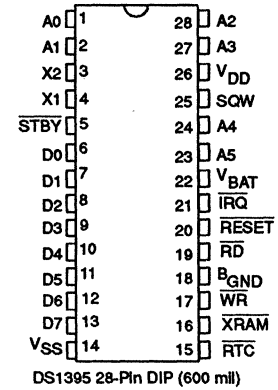
ORDERING INFORMATION

DS1395	RTC Chip; 28 pin DIP
DS1395S	RTC Chip; 28 pin SOIC
DS1397	RTC Module; 28 pin DIP

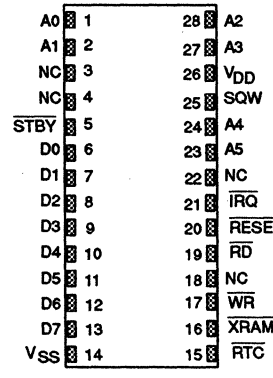
PIN ASSIGNMENT



DS1395S 28-Pin SOIC (330 mil)



DS1395 28-Pin DIP (600 mil)



DS1397 28-Pin Encapsulated Package (720 mil)

PIN DESCRIPTIONS

V_{DD}, V_{SS} – Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 – Data Bus (bidirectional): Data is written into the device from the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a write cycle at the rising edge of a $\overline{WR}$ pulse. Data is read from the device and driven onto the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a read cycle when the $\overline{RD}$ signal is low.

A0-A5 – Address Bus (input): Various internal registers of the device are selected by these lines. When $\overline{RTC}$ is asserted, A0 selects between the indirect address register and RTC data register. When the $\overline{XRAM}$ is asserted, A0-A5 addresses a 32–byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

$\overline{RD}$ - Read Strobe (input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either $\overline{RTC}$ or $\overline{XRAM}$ is asserted.

$\overline{WR}$ - Write Strobe (input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the $\overline{XRAM}$ or $\overline{RTC}$ signals.

$\overline{STBY}$ - Standby (input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the $\overline{STBY}$ signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition (V_{DD} is 4.25 volts, typical) is negated, whichever occurs first.

$\overline{RTC}$ - Real Time Clock Select (input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

SQW - Square Wave (output): Frequency selectable output. Frequency is selected by setting register A bits RS0-RS3. See Table 2 for frequencies that can be selected.

$\overline{XRAM}$ - Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are accessible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM pointed to by the page register. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

$\overline{IRQ}$ - Interrupt Request (output): The $\overline{IRQ}$ signal is an active low, open drain output that is used as a processor interrupt request. The $\overline{IRQ}$ output follows the state of the IRQF bit (bit 7) in status register C. $\overline{IRQ}$ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

$\overline{RESET}$ - Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When $\overline{RESET}$ is low, the following occurs.

1. The following register bits are cleared:
   a. Periodic interrupt (PIE)
   b. Alarm interrupt enable (AIE)
   c. Update ended interrupt (UF)
   d. Interrupt request flag (IRQF)
   e. Periodic interrupt flag (PF)
   f. Alarm interrupt flag (AF)
   g. Square wave output enable (SQWE)
   h. Update ended interrupt enable (UIE)
2. The $\overline{IRQ}$ pin is in the high impedance state.
3. The RTC is not processor accessible.

ADDITIONAL PIN DESCRIPTION

(FOR DS1395, DS1395S)

X1, X2 – Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF.

V_{BAT} – Battery input for any standard +3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} in the absence of power should be used to size the external energy source.

B_{GND} – Battery ground: This pin or pin 14 can be used for the battery ground return.

OPERATION

Power-Down/Power-Up: The real time clock will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V_{DD}. When the voltage level applied to the V_{DD} input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When V_{DD} falls below the CE_{THR} (4.25 volts typical), the chip select inputs $\overline{RTC}$ and $\overline{XRAM}$ are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When V_{DD} falls below 3.2 volts (typical), the module is switched over to an internal power source in the case of the DS1397, or to an external battery connected to the V_{BAT} and BGND pins in the case of the DS1395 and DS1395S, so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when $\overline{RTC}$ is asserted low and represents the real time clock. The second set of registers is active when $\overline{XRAM}$ is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

1. Registers C and D are Read Only (status information)
2. Bit 7 of register A is Read Only
3. Bit 7 of the "Seconds" byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 128 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 128 pages of nonvolatile memory available. The address of the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/O spaces. (See Figure 3.)

TIME, CALENDAR AND ALARM LOCATIONS

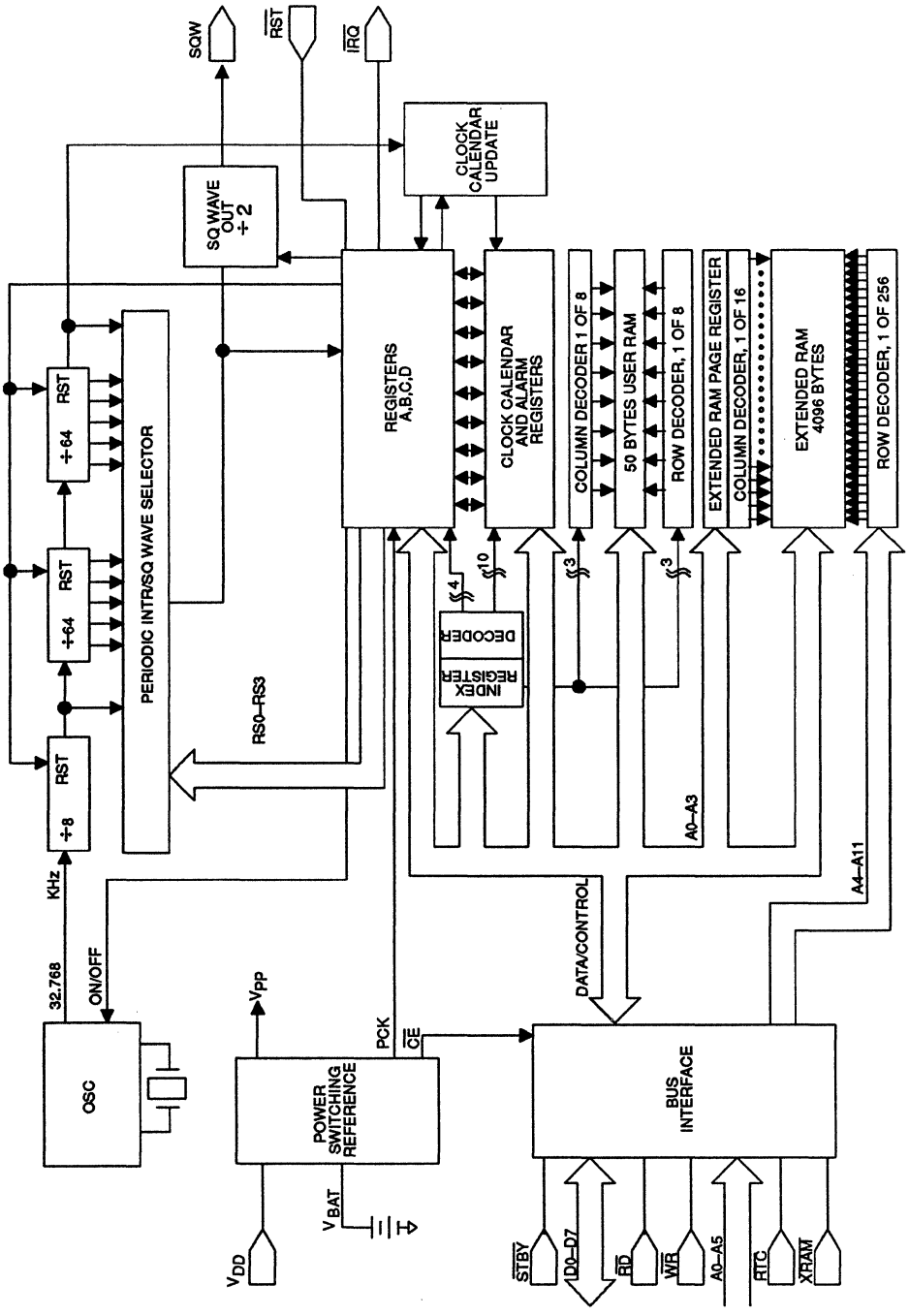
The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

DS139X BLOCK DIAGRAM Figure 1



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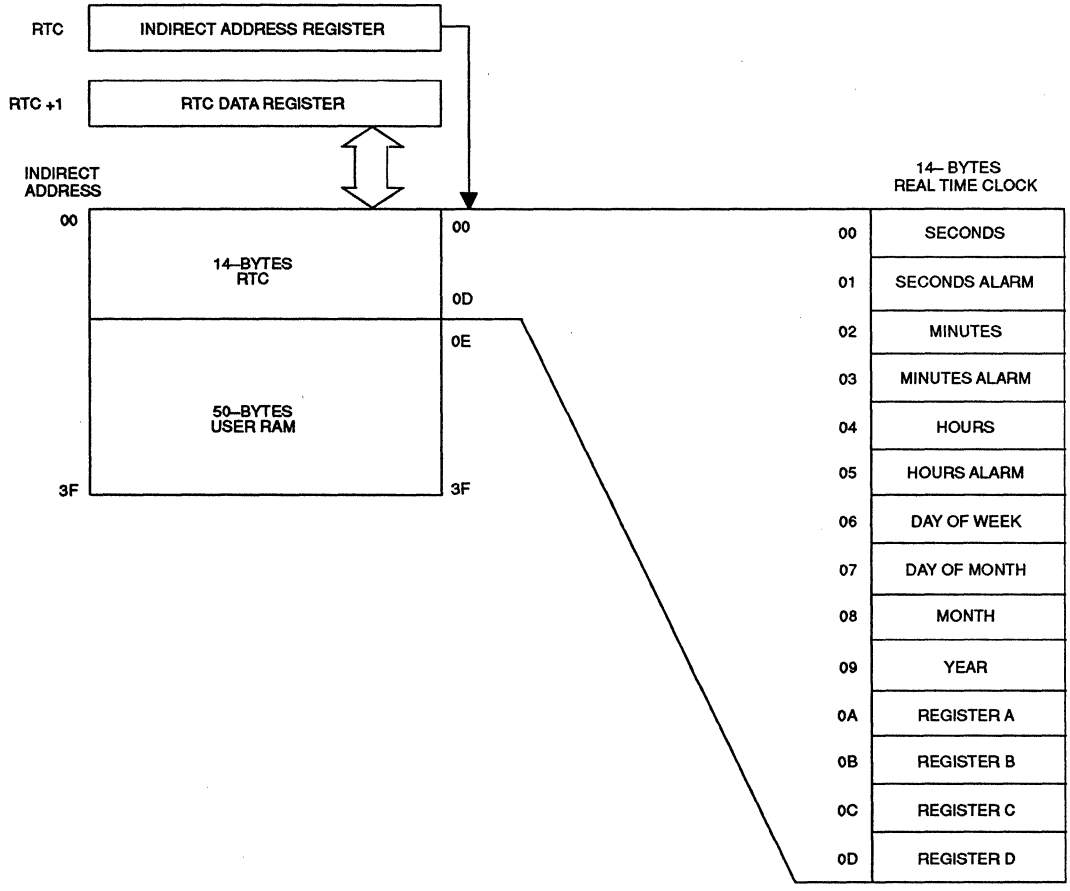
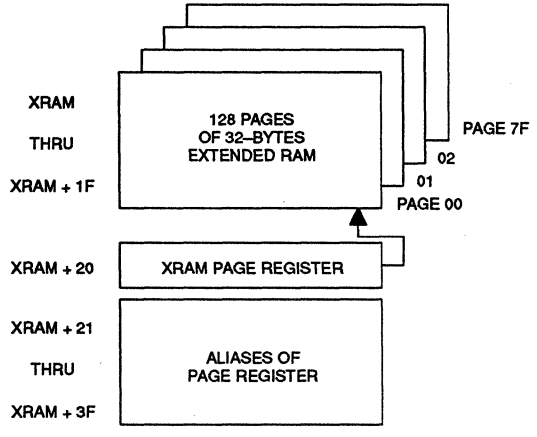
REAL TIME CLOCK RAM MAP Figure 2



EXTENDED RAM ADDRESS MAP Figure 3



TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

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USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1395/DS1397. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1395/DS1397. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1395/DS1397 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

UPDATE CYCLE

The DS1395/DS1397 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

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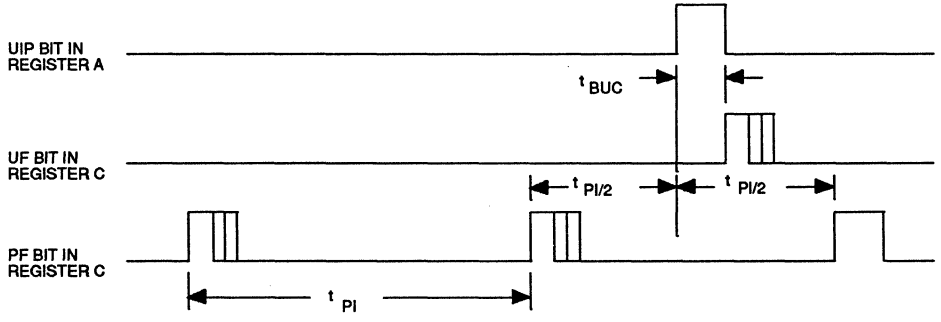
UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1395/DS1397 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1395/DS1397.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1395/DS1397 functions but is cleared by the hardware $\overline{RESET}$ signal.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1395/DS1397 do not affect the AIE bit but is cleared by $\overline{RESET}$.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high or the $\overline{RESET}$ pin going low clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{RESET}$.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C or by $\overline{RESET}$.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C or a $\overline{RESET}$ will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or by $\overline{RESET}$.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

6

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Pin Potential to Ground Pin	-0.3V to +7.0V
Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3V
Power Dissipation	500 mW
Storage Temperature	–40°C to +70°C
Ambient Temperature	0°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High Voltage	Recognized as a High Signal Over Recommended V_{DD} and t_A Range	V_{IH}	2.2	V_{DD}+ 0.3	V V	
Input Low Voltage	Recognized as a Low Signal Over Recommended V_{DD} and t_A Range	V_{IL}	-0.3	0.8	V	
Battery Voltage		V_{BAT}	2.5	3.5	V	

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, t_A = 0° C to 70°C)

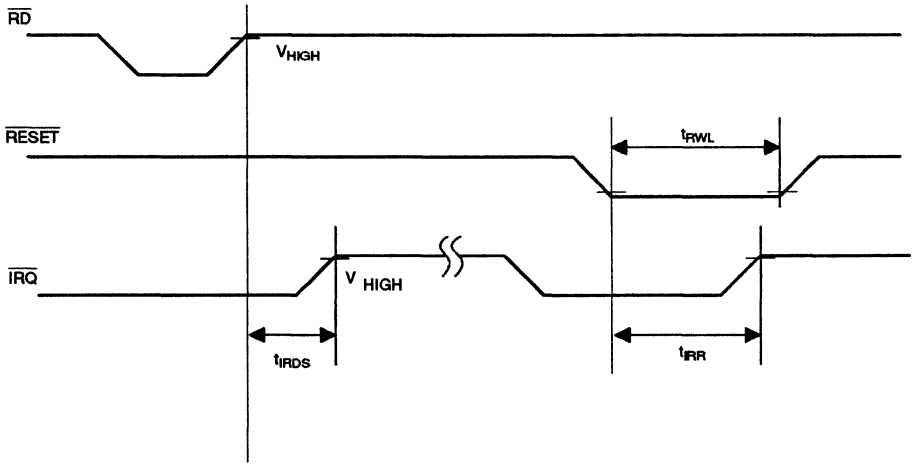
CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Input Leakage V_{IL}=0V, V_{IH}=V_{DD}	For any Single Pin: D0-7, $\overline{RD}$, $\overline{WR}$, A0-5, XRAM, $\overline{RTC}$, $\overline{RESET}$	I_I		±1	µA	
Output High Voltage	V_{DD}=5.0V I_{LOAD} =1 mA	V_{OH}	2.4		V	
Output Low Voltage	V_{DD} = 5.0V I_{LOAD} = 4 mA	V_{OL}		0.4	V	
Power Supply Current	Outputs Unloaded	I_{DD}		50	mA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{DD}	I_{STBY}		+500	µA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{SS}	I_{STBY}		–1	µA	

AC SWITCHING CHARACTERISTICS

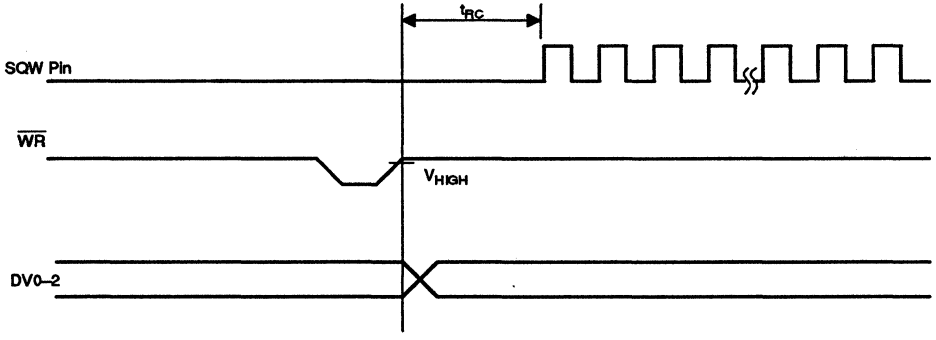
(0°C to 70°C, V_{DD} = 4.5V to 5.5V)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Reset Pulse Width		t_{RWL}	5		µs	
Oscillator Startup	From Software Enable Via DV Bits	t_{RC}		1	s	
IRQ Release from $\overline{RD}$ High		t_{IRDS}		2	µs	
IRQ Release from $\overline{RESET}$ Low		t_{IRR}		2	µs	

IRQ RELEASE DELAY



OSCILLATOR START-UP



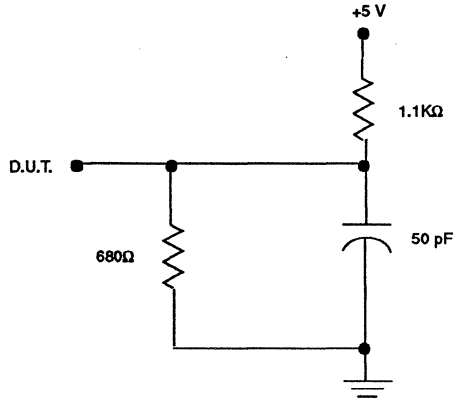
NOTE
Timing assumes RS3-0 Bits = 0011, minimum t_{PI}.

BUS TIMING

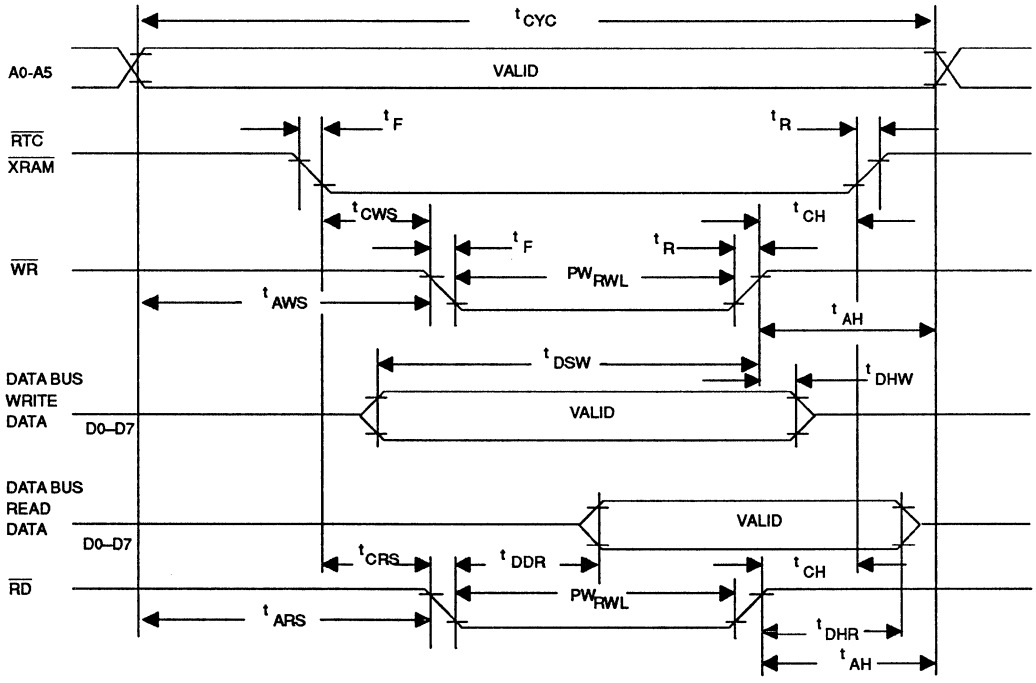
(0° to 70°C, V_{DD} = 4.5V to 5.5V)

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Cycle Time	t_{CYC}	395		DC	ns	
Pulse Width, RD/WR Low	PW_{RWL}	200			ns	
Signal Rise and Fall Time, $\overline{RTC}$, $\overline{XRAM}$, $\overline{RD}$, $\overline{WR}$	t_R, t_F			30	ns	
Address Hold Time	t_{AH}	20			ns	
Address Setup Time Before $\overline{RD}$	t_{ARS}	50			ns	
Address Setup Time Before $\overline{WR}$	t_{AWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{RD}$	t_{CRS}	50			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{WR}$	t_{CWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Hold Time After $\overline{RD}$ or $\overline{WR}$	t_{CH}	20			ns	
Read Data Hold Time	t_{DHR}	10		100	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Output Data Delay Time from RD	t_{DDR}	20		200	ns	
Write Data Setup Time	t_{DSW}	200			ns	

OUTPUT LOAD



BUS READ/WRITE TIMING



POWER-DOWN/ POWER-UP TIMING (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F 4.0 ≤V_{CC} ≤ 4.5V	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} 3.0 ≤V_{CC}≤ 4.0V	10			µs	
V_{CC} Slew Rate Power Up	t_R 4.5V≥V_{CC}≥4.0V	0			µs	
Expected Data Retention	t_{DR}	10			years	

NOTE

$\overline{CE}$ is chip enabled for access, an internal signal which is defined by ($\overline{RD}$ + $\overline{WR}$) ($\overline{XRAM}$ + $\overline{RTC}$).

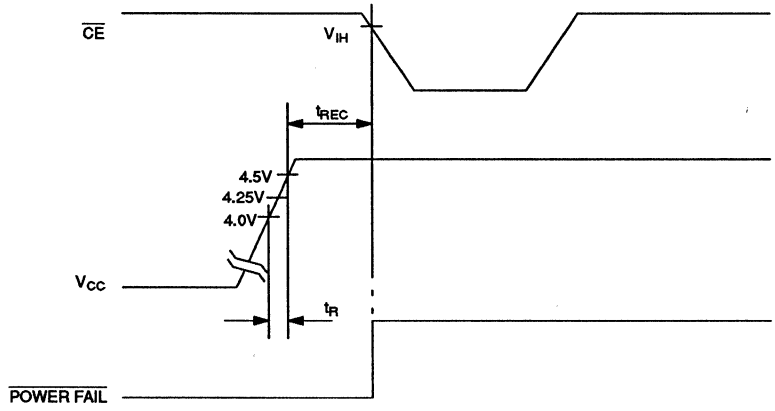
CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

GENERAL INFORMATION

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Expected Data Retention @ 25°C (DS1397 only)	t_{DR}	10			Years	
Clock Accuracy for t_{DR} @ 25°C (DS1397 only)	C_Q	±1			Min/Mo	
Clock Accuracy Temperature Coefficient (DS1397)	K			.050	ppm/°C²	
Clock Temperature Coefficient Turnover Temperature (DS1397 only)	t_O	20		30	0°C	
Chip Enable Threshold (DS1397 only)	CE_{THR}			4.5	V	

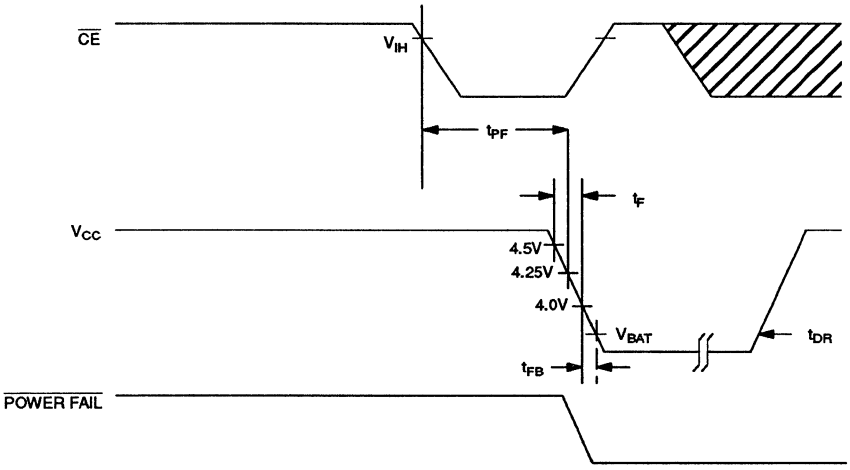
POWER–UP CONDITION



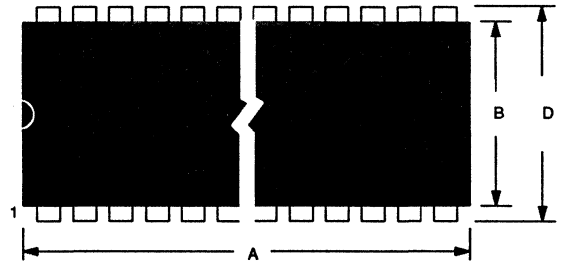
NOTE

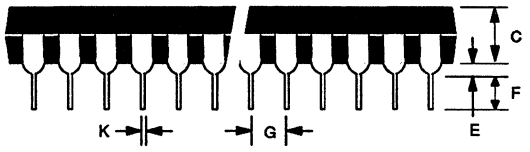
$\overline{CE}$ is an internal signal generated by the power switching reference in the DS139X products.

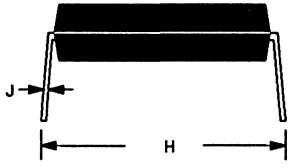
POWER–DOWN CONDITION



DS1395 28 PIN DIP

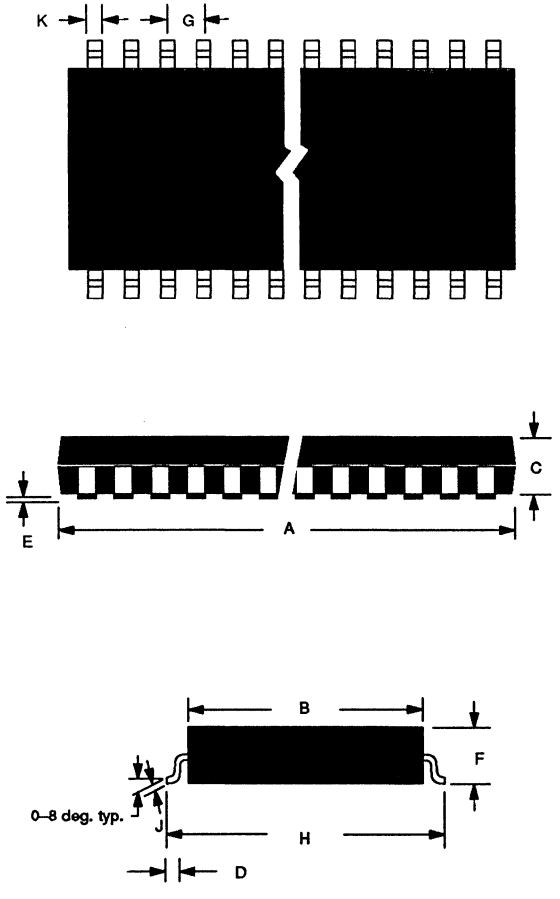






PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.445 36.70	1.470 37.34
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

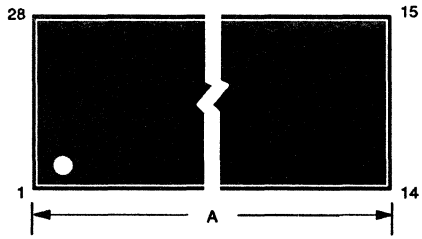
DS1395S 28 PIN SOIC

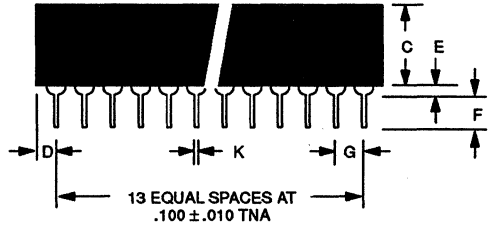


PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

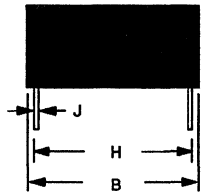
6

DS1397 28 PIN 720 MIL FLUSH ENCAPSULATED





PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 3, 4, 18 AND 22 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1485/DS1488
RAMified Real Time Clock 8K x 8

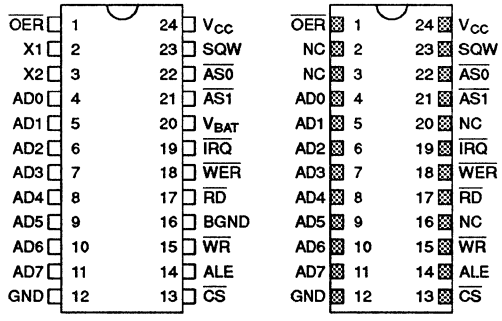
FEATURES

- Upgraded IBM AT computer clock/calendar with 8K x 8 extended RAM
- Totally nonvolatile with over 10 years of operation in the absence of power
- Counts seconds, minutes, hours, day of the week, date, month and year with leap year compensation
- Binary or BCD representations of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 user RAM locations plus 8K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - 8K x 8 SRAM accessible by using separate control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- Available as chip (DS1485) or stand alone module with embedded lithium battery and crystal (DS1488)

ORDERING INFORMATION

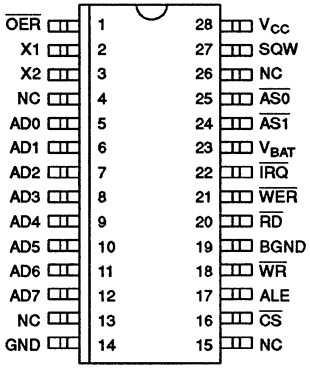
DS1485	RTC Chip; 24 pin DIP
DS1485S	RTC Chip; 28 pin SOIC
DS1488	RTC Module; 24 pin DIP

PIN ASSIGNMENT



DS1485 24-PIN DIP (600 MIL)

DS1488 24-PIN ENCAPSULATED PACKAGE (740 MIL FLUSH)



DS1485S 28-PIN SOIC (330 MIL)

PIN DESCRIPTION

$\overline{OER}$	-	RAM Output Enable
X1	-	Crystal Input
X2	-	Crystal Output
AD0-AD7	-	Mux'ed Address/Data Bus
$\overline{CS}$	-	RTC Chip Select Input
ALE	-	RTC Address Strobe
$\overline{WR}$	-	RTC Write Data Strobe
$\overline{RD}$	-	RTC Read Data Strobe
$\overline{WER}$	-	RAM Write Data Strobe
$\overline{IRQ}$	-	Interrupt Request Output
$\overline{AS1}$	-	RAM Upper Address Strobe
$\overline{AS0}$	-	RAM Lower Address Strobe
SQW	-	Square Wave Output
V_{CC}	-	+5V Supply
GND	-	Ground
V_{BAT}	-	Battery + Supply
BGND	-	Battery Ground
NC	-	No Connection

DESCRIPTION

The DS1485/DS1488 RAMified Real Time Clocks (RTCs) are upward-compatible successors to the industry standard DS1285/DS1287 and the DS1385/DS1387 RTC's for PC applications. In addition to the basic DS1285/DS1287 RTC functions, 8K bytes of on-chip nonvolatile RAM have been added.

The RTC functions include a time-of-day clock, a one-hundred year calendar, time-of-day interrupt, periodic interrupts, and an end-of-clock update cycle interrupt. In addition, 50 bytes of user NV RAM are provided within this basic RTC function which can be used to store configuration data. The clock and user RAM are maintained in the absence of system V_{CC} by a lithium battery.

The 8K x 8 additional NV RAM is provided to store a much larger amount of system configuration data than is possible within the original 50 byte area. This RAM is accessed via control signals separate from the RTC, and is also maintained as nonvolatile storage from the lithium battery.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1485/DS1488. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to the energy source connected to the V_{BAT} pin in the case of the DS1485, or to the internal battery in the case of the DS1488. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

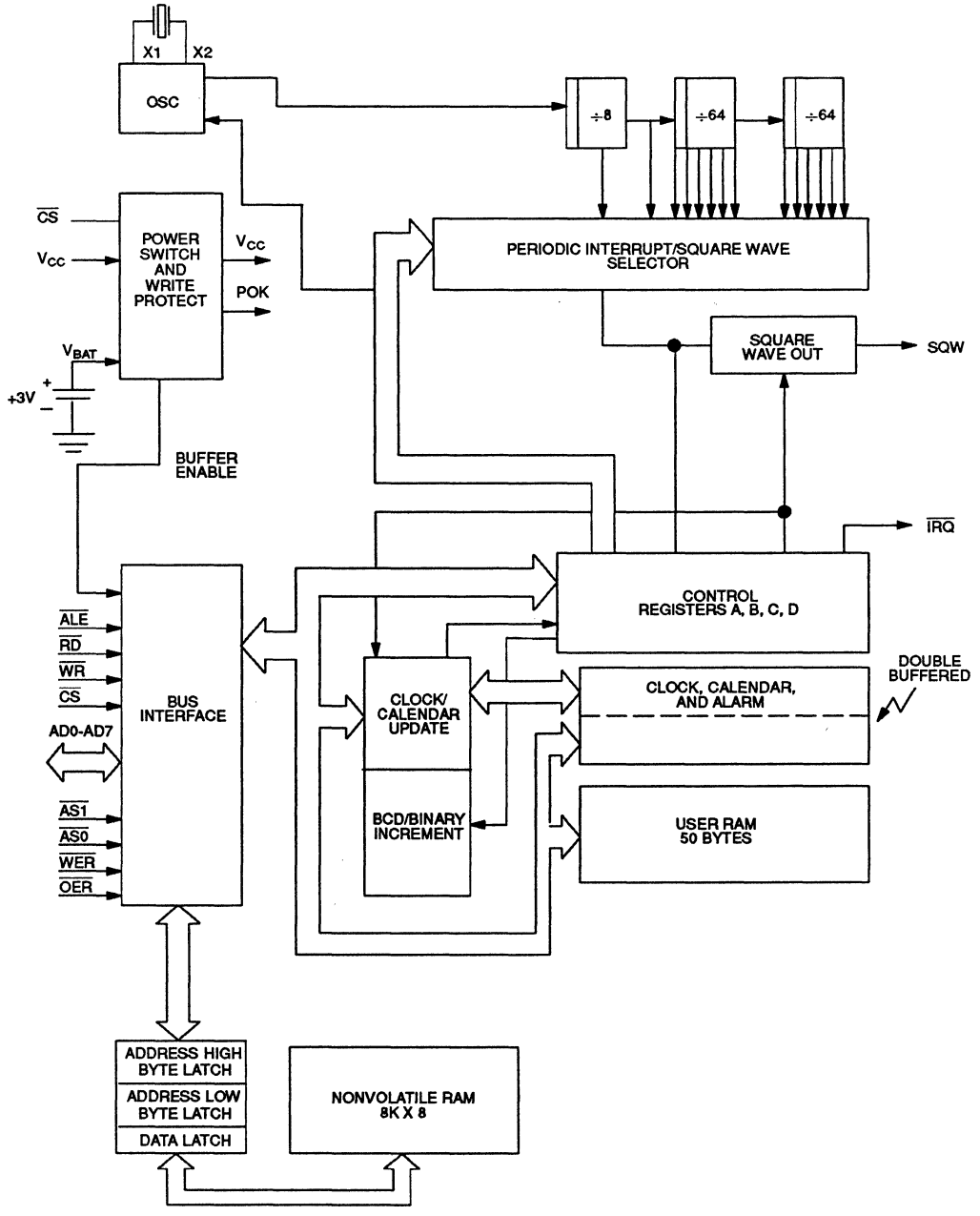
SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1485/DS1488 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1485/DS1488 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle, the DS1485/DS1488 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

ALE (RTC Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1485/DS1488.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1485/DS1488 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

DS1485/DS1488 BLOCK DIAGRAM Figure 1



$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1485/DS1488 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1485/DS1488 that can be tied to an interrupt input on a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application program normally reads the C register.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 8K x 8 RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper five bits of the 8K x 8 RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1485/DS1488 drives the bus with RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and is used to perform writes to the 8K x 8 RAM portion of the DS1485/DS1488.

(DS1485 ONLY)
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Crystals can be ordered from Dallas Semiconductor Corporation. Order part number DS9032.

V_{BAT}, BGND - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should be used to size the external energy source.

ADDRESS MAP

The address map of the DS1485/DS1488 is shown in Figure 2. The address map consists of the RTC and the 8K X 8 NV SRAM section. The RTC section contains 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

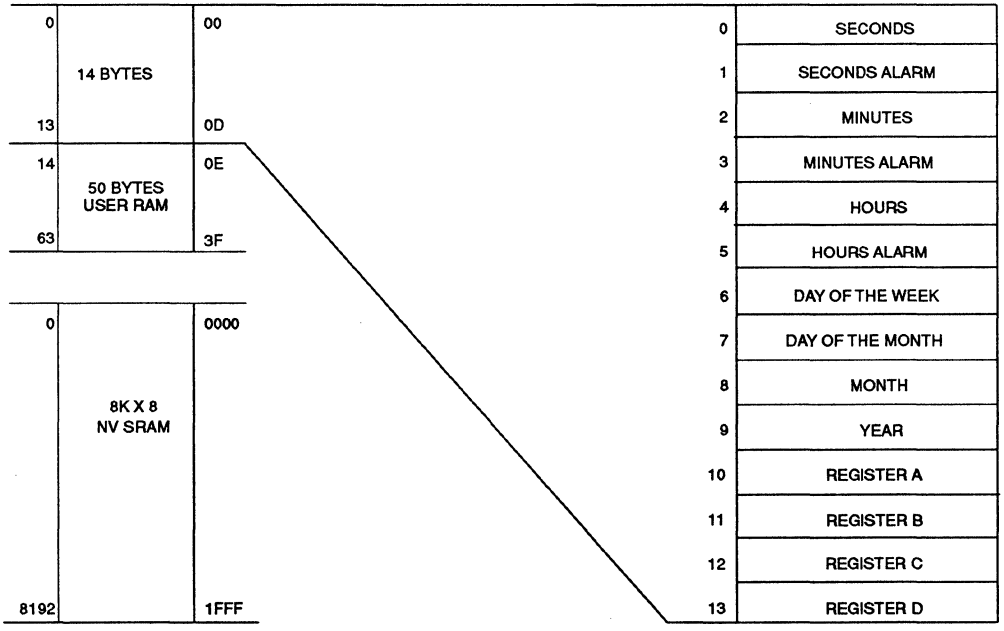
1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

RTC (REAL TIME CLOCK)

The RTC function is the same as the DS1287 Real Time Clock. Access to the RTC is accomplished with four controls: ALE, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The RTC is the same in the DS1287 with the following exceptions:

1. The MOT pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The bus selection capability of the DS1285/DS1287 has been eliminated. Only the Intel bus interface timing is applicable.
2. The $\overline{RESET}$ pin on the DS1285/DS1287 is not present on the DS1485/DS1488. The DS1485/DS1488 will operate the same as the DS1285/DS1287 with $\overline{RESET}$ tied to V_{CC}.

ADDRESS MAP DS1485/DS1488 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1485/DS1488. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1485/DS1488. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1485/DS1488 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

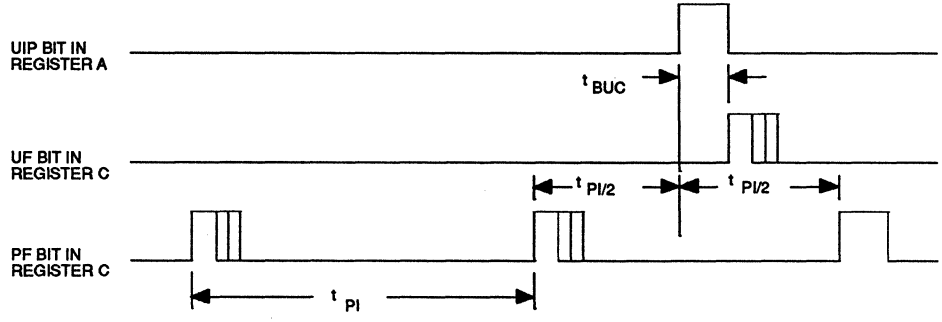
The DS1485/DS1488 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1485/DS1488 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1485/DS1488.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1485/DS1488 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1485/DS1488 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • ALE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

8K X 8 RAM

The DS1485/DS1488 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM is supported.

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$, are used to access the 8K x 8 SRAM. This access mode is identical to that supported by the DS1385/DS1387. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers and the 50 bytes of user RAM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	9

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

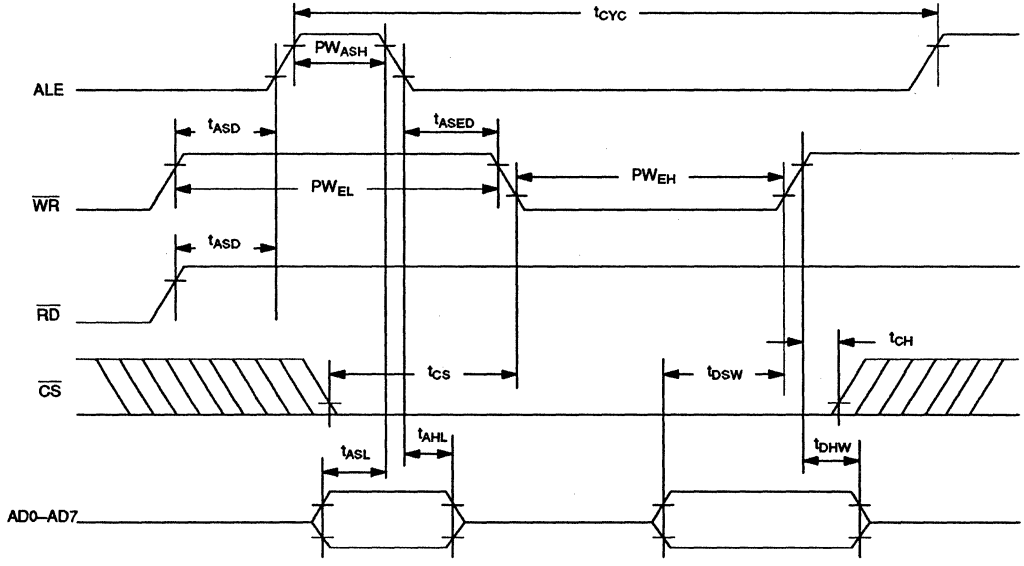
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$, $\overline{OER}$, and $\overline{WER}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,4
Output @ 0.4V	I_{OL}			4.0	mA	1

RTC AC TIMING CHARACTERISTICS

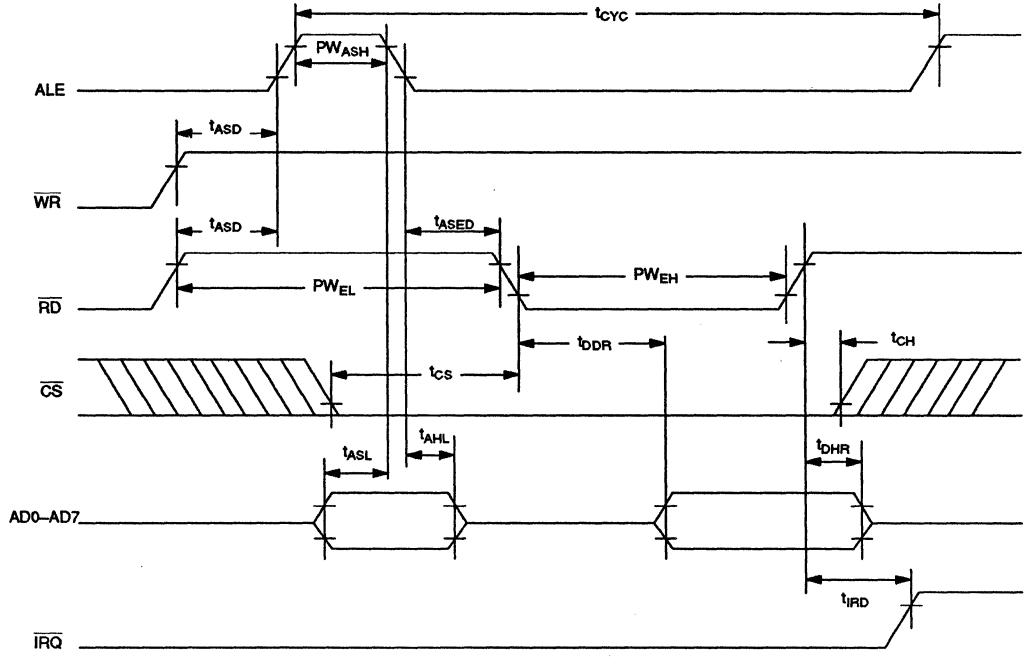
(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{EH}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{EL}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time to Write	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1485/DS1488 BUS TIMING FOR WRITE CYCLE TO RTC



DS1485/DS1488 BUS TIMING FOR READ CYCLE TO RTC



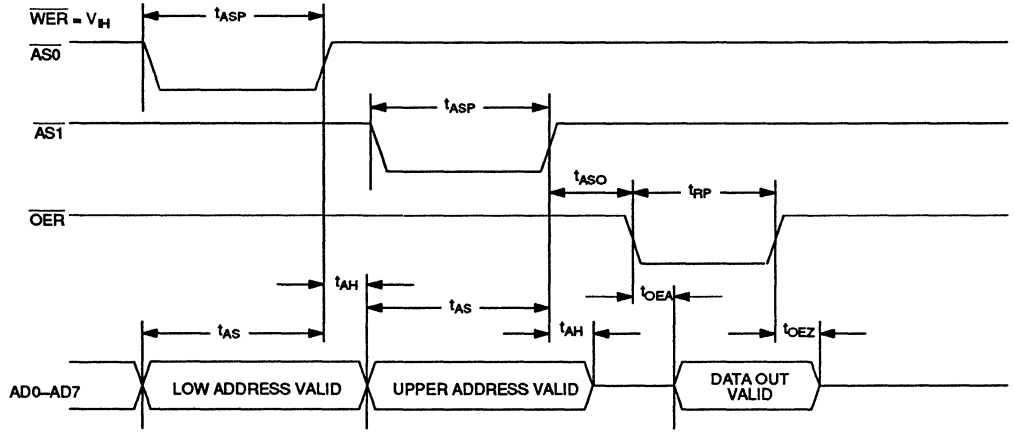
8K X 8 AC TIMING CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V + 10%)

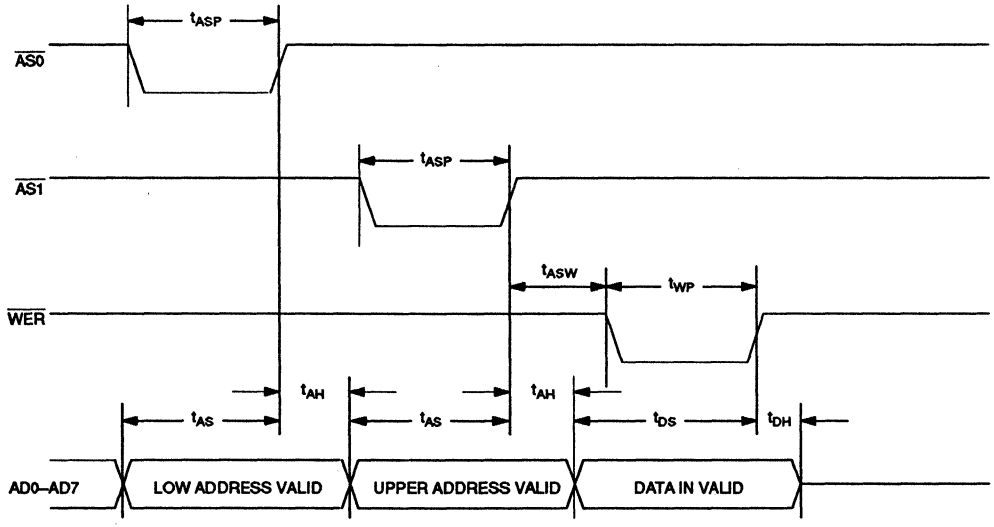
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	7
Write Pulse Width	t_{WP}	200			ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

6

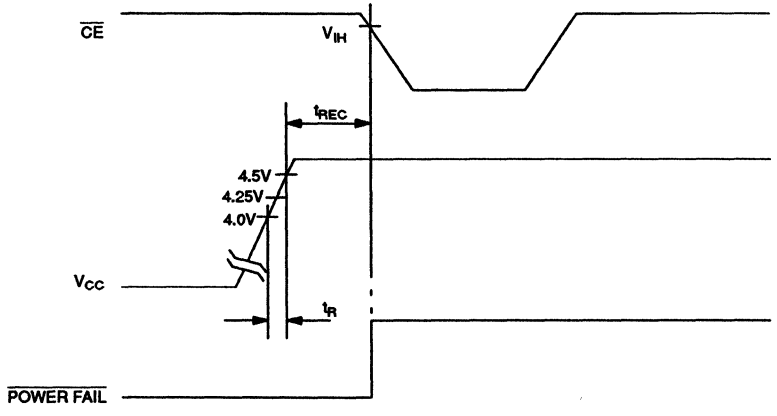
BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM



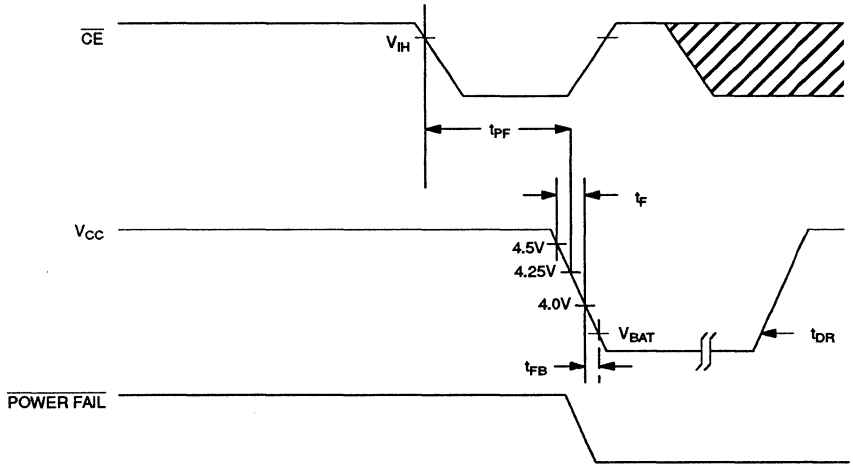
BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM



POWER-UP CONDITION



POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	8

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE

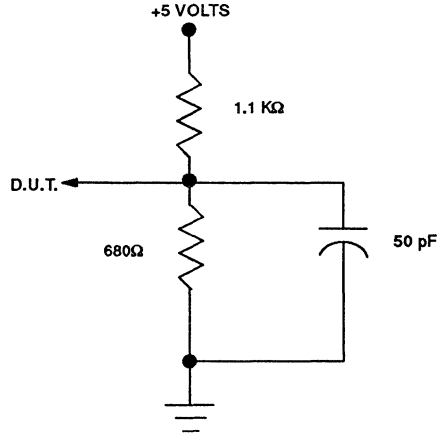
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

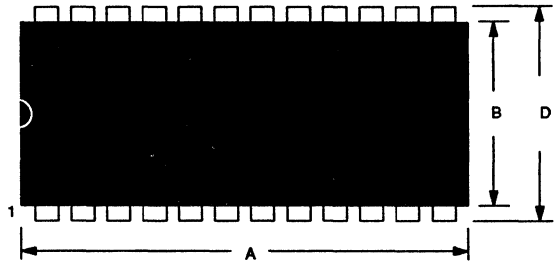
NOTES

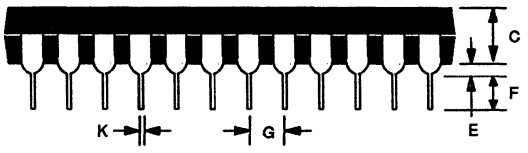
1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 4.
6. All other inputs at CMOS levels.
7. Measured with a load as shown in Figure 4.
8. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
9. Applies to DS1485 only.

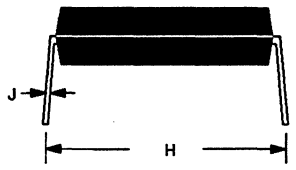
OUTPUT LOAD Figure 4



DS1485 24 PIN DIP

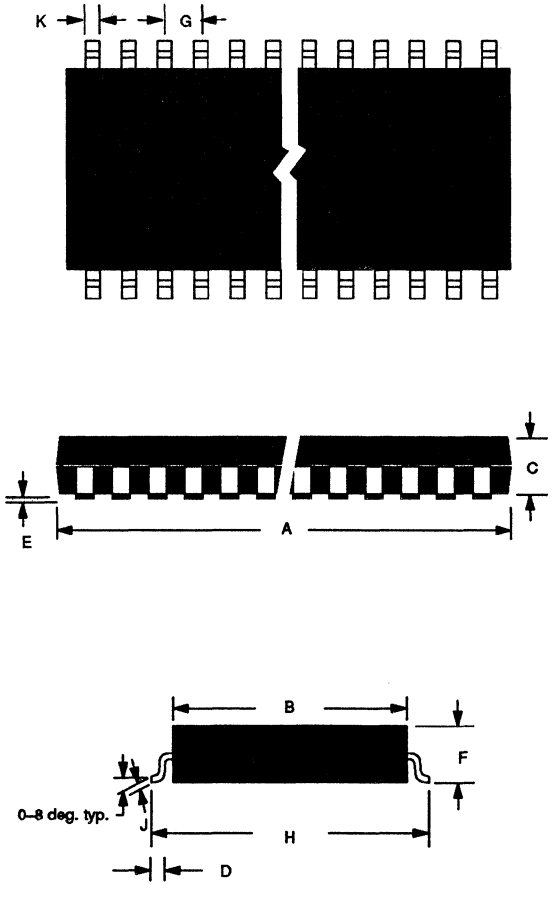






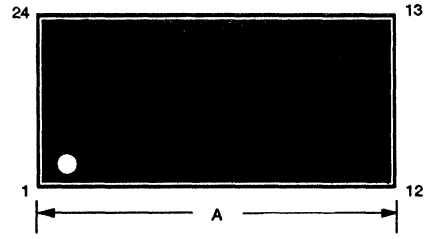
PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.245 31.62	1.270 32.26
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.38	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

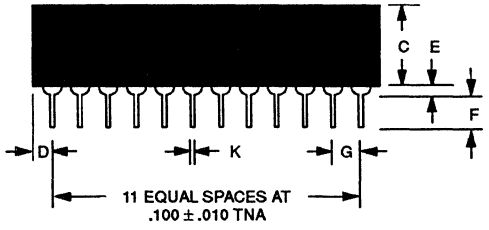
DS1485S 28 PIN SOIC

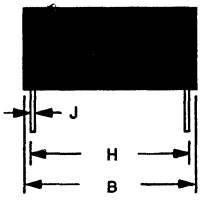


PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

DS1488 24 PIN 740 MIL FLUSH ENCAPSULATED







PKG	24-PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.720 18.29	0.740 18.80
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.89
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.

6

PRELIMINARY

DALLAS SEMICONDUCTOR

DS1486
RAMified Watchdog Timekeeper

FEATURES

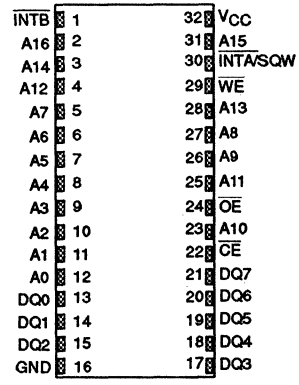
- 128K bytes of user NV RAM
- Real time quartz clock/calendar keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Will operate in 32-pin JEDEC footprint
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities such as system wakeup
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25°C
- Greater than 10 years of timekeeping in the absence of V_{CC} @ 25%
- Interrupt signals active in power-down mode

ORDERING INFORMATION

DS1486-XX — RTC and 128K x 8 NVSRAM

- -12 120 ns access
- -15 150 ns access

PIN ASSIGNMENT



DS1486 128K x 8
32-Pin Encapsulated Package

PIN DESCRIPTION

INTB(INTB)	-	Interrupt Output B
A0-A16	-	Address Inputs
DQ0-DQ7	-	Data Input/Output
CE	-	Chip Enable
OE	-	Output Enable
WE	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
INTA/SQW	-	Interrupt Output A/Square Wave Output

DESCRIPTION

The DS1486 RAMified Timekeeper is a self-contained real time clock (RTC), alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1486 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 128K by 8-bit memory and the timekeeping registers can be read or written in the same manner as bytewide static RAM. The timekeeping registers are located in the first 14 bytes of memory space. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of V_{CC} and write protects memory when V_{CC} is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of V_{CC}. Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm interrupts and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week. Interrupts for both watchdog and RTC will operate when system is powered down. Either can provide system "wake-up" signals.

OPERATION - READ REGISTERS

The DS1486 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (Low). The unique address specified by the address inputs (A0-A16) defines which of the registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1486 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

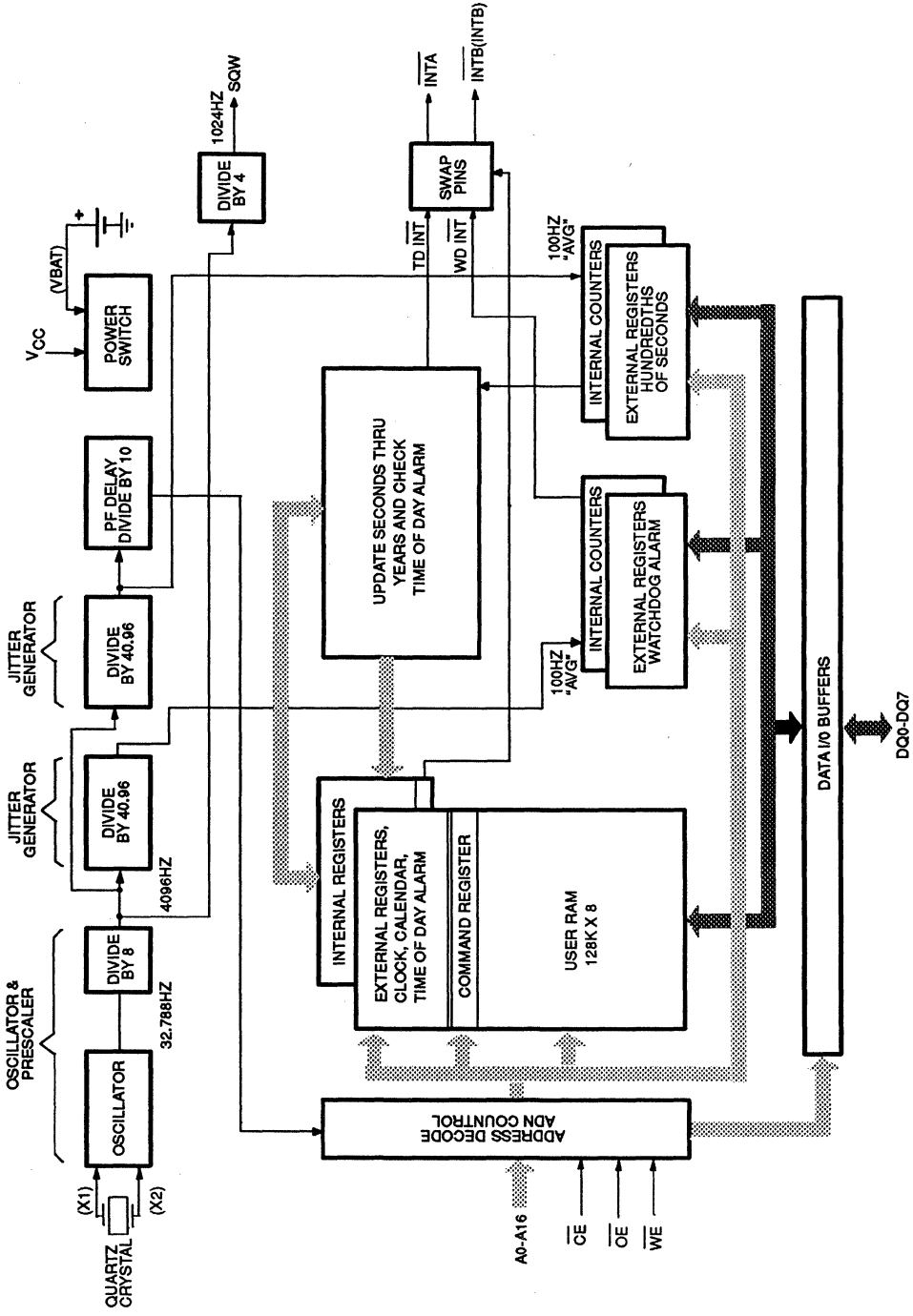
DATA RETENTION

The RAMified Timekeeper provides full functional capability when V_{CC} is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1486 constantly monitors V_{CC}. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become "don't care". The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of V_{CC}. As V_{CC} falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} and disconnects the internal lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a period of 200 ms.

RAMIFIED TIMEKEEPER REGISTERS

The RAMified Timekeeper has 14 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog and control information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register E through 1FFFF are user bytes and can be used to maintain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, $\overline{EOSC}$ (Bit 7) enables the real time clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the $\overline{INTA}$/Square Wave Output (pin 30). When set to logic zero, the $\overline{INTA}$/Square Wave Output pin will output a 1024 Hz square wave signal. When set to logic one the Square Wave Output pin is available for interrupt A output ($\overline{INTA}$) only. Bit 6 of the Hours register is defined as the 12 or 24 hour select bit. When set to logic one, the 12 hour format is selected. In the 12 hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24 hour mode, bit 5 is the second 10 hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME OF DAY ALARM REGISTERS

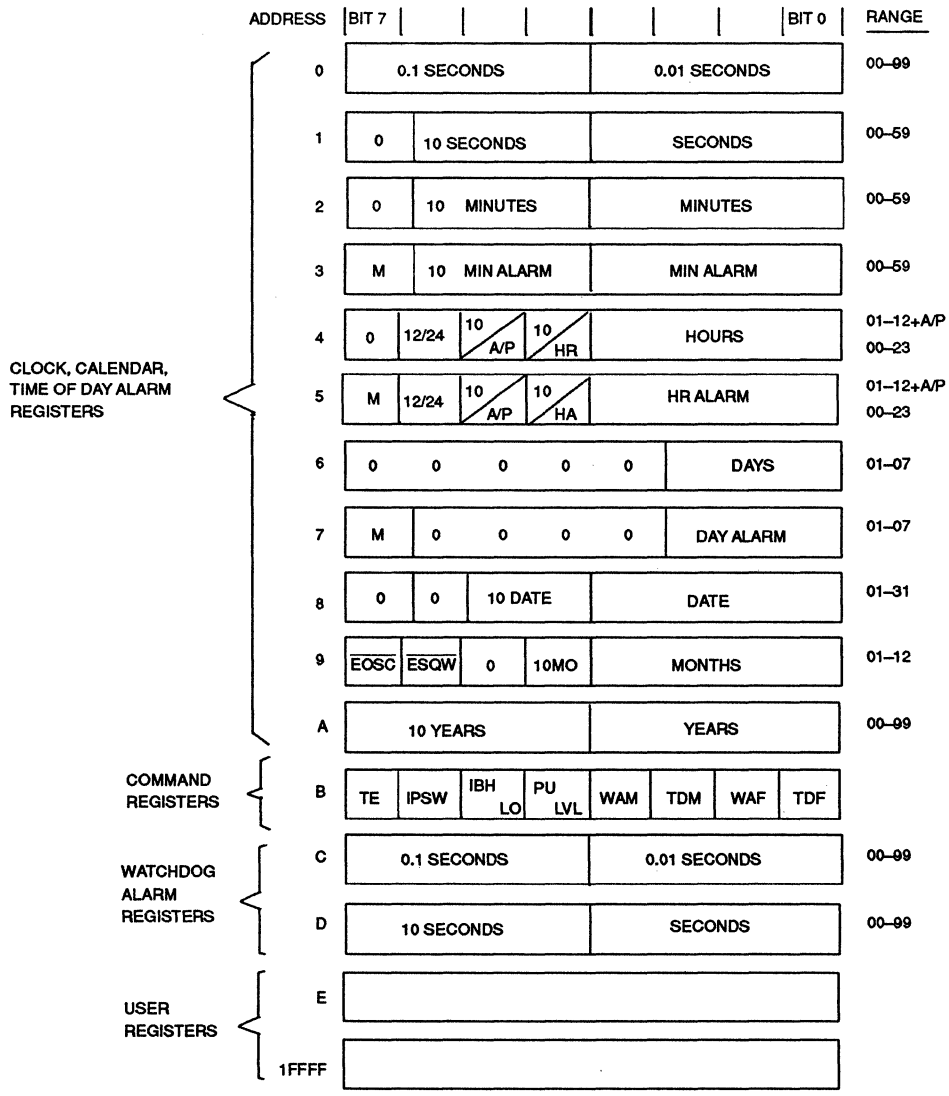
Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count- down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

DS1486 RAMIFIED TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

REGISTER			
(3) MINUTES	(5) HOURS	(7) DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER BIT COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer enable - This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW - Bit 6 Interrupt switch - When set to a logic 1, $\overline{INTA}$ is the Time of Day Alarm and INTB/($\overline{INTB}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{INTA}$ is now the Watchdog Alarm output and INTB/($\overline{INTB}$) is the Time of Day Alarm output. The $\overline{INTA}$/SQW output pin shares both the interrupt A and square wave output function. When $\overline{INTA}$ is active, the square wave function is automatically disabled.

IBH/LO - Bit 5 Interrupt B Sink or Source Current - When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{INTB}$) will source current (see DC characteristics IOH). When this bit is set to a logic 0, INTB will sink current (see DC characteristics IOL).

PU/LVL - Bit 4 Interrupt pulse mode or level mode - This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{INTA}$ and INTB/($\overline{INTB}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{INTA}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{INTB}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3 ms and then release.

WAM - Bit 3 Watchdog Alarm Mask - When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask - When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0,4,5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Time of Day Alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag - This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag - This is a read only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO + 70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	10
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
Input Logic 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
Output Leakage Current	I_{LO}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LIO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}			4.0	mA	13
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} -0.5	I_{CCS2}			4.0	mA	
Active Current	I_{CC}			85	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		7	15	pF	
Output Capacitance	C_{OUT}		7	15	pF	
Input/Output Capacitance	$C_{I/O}$		7	15	pF	

AC ELECTRICAL CHARACTERISTICS

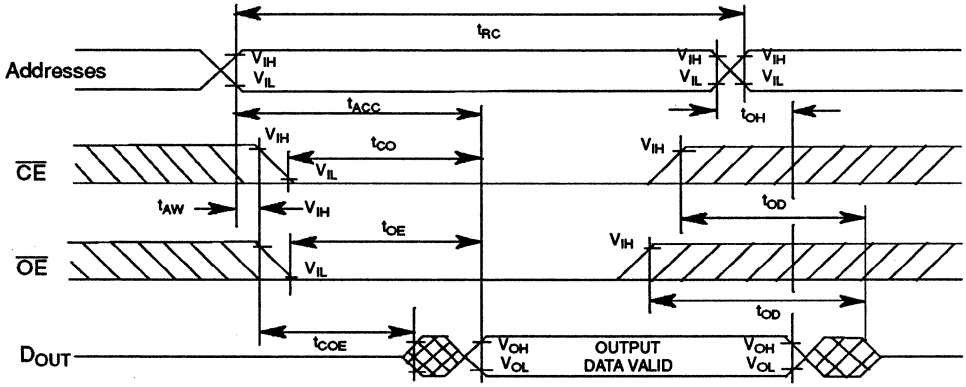
(0°C to +70°C, V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	DS1486–12		DS1486–15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	1
Address Access Time	t_{ACC}		120		150	ns	
$\overline{CE}$ Access Time	t_{CO}		120		150	ns	
$\overline{OE}$ Access Time	t_{OE}		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10		10		ns	
Output High Z from Deselect	t_{OD}		40		50	ns	
Output Hold from Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Write Pulse Width	t_{WP}	110		140		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		15		ns	
Output High Z from $\overline{WE}$	t_{ODW}		40		50	ns	
Output Active from $\overline{WE}$	t_{OEW}	10		10		ns	
Data Setup Time	t_{DS}	85		110		ns	4
Data Hold Time	t_{DH}	10		15		ns	4,5
$\overline{INTA}$, $\overline{INTB}$ Pulse Width	t_{IPW}	3		3		ms	11,12

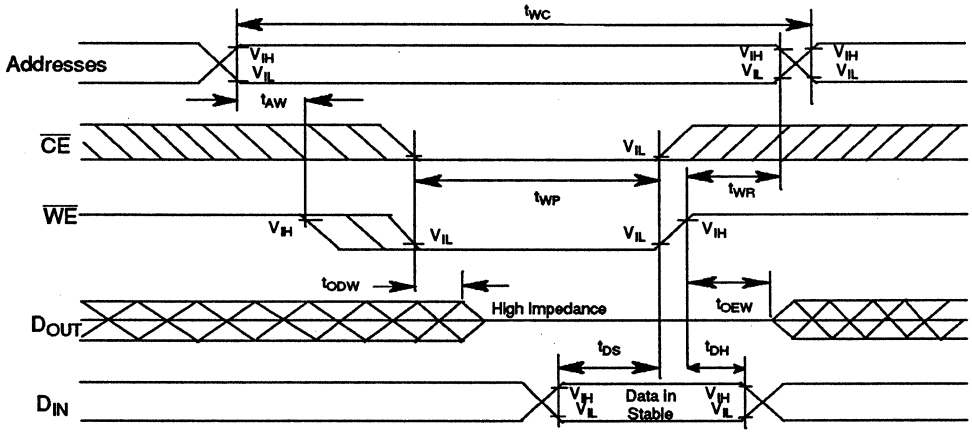
AC TEST CONDITIONS

Input Levels: 0V TO 3V
Transition Times: 5 ns

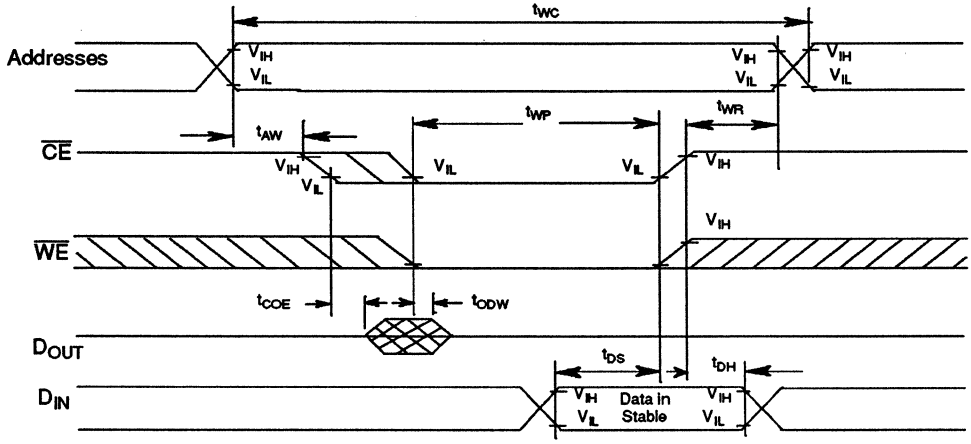
READ CYCLE (Note1)



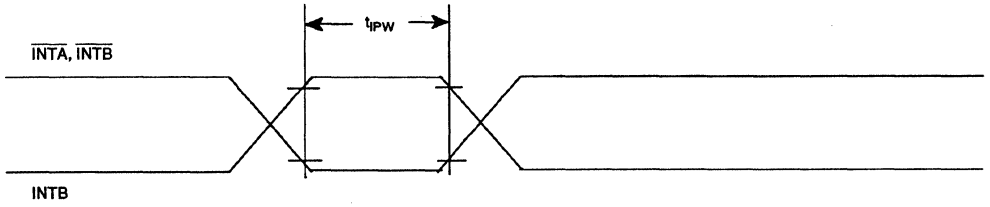
WRITE CYCLE 1 (Notes 2, 6, 7)



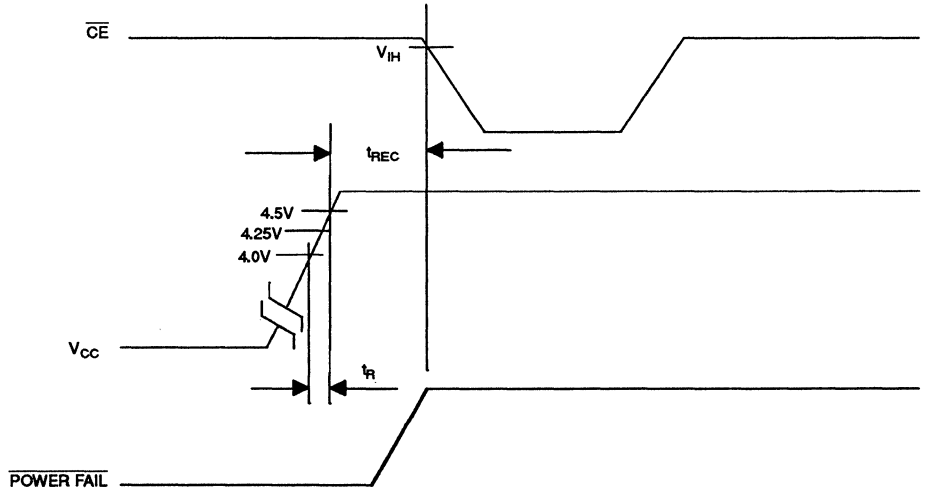
WRITE CYCLE 2 (Notes 2, 8)



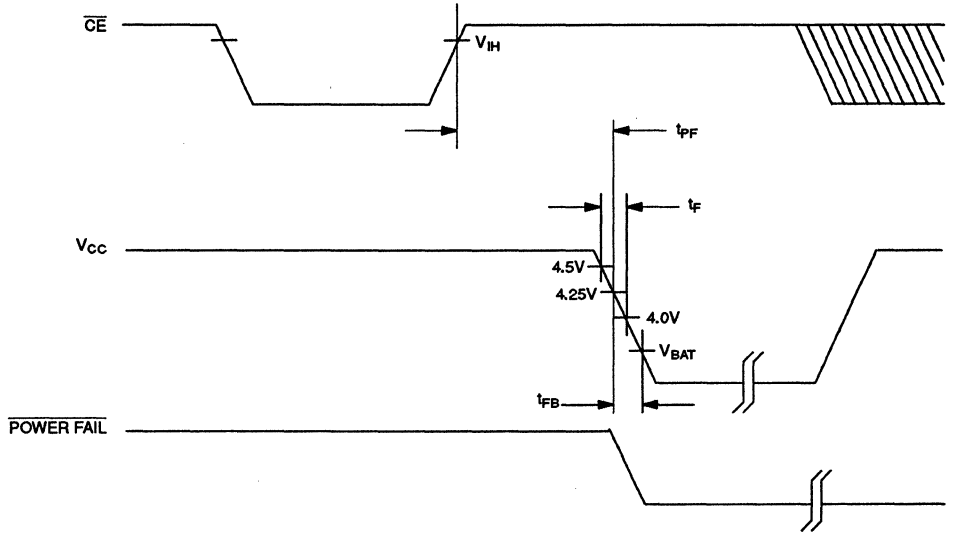
TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-UP CONDITION



POWER-DOWN CONDITION



AC ELECTRICAL CHARACTERISTICS POWER-UP POWER-DOWN TIMING (0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}		0	ns	
Recovery at Power Up	t_{REC}		200	ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300		µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.25V$	10		µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0		µs	
Expected Data Retention	t_{DR}	10		years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

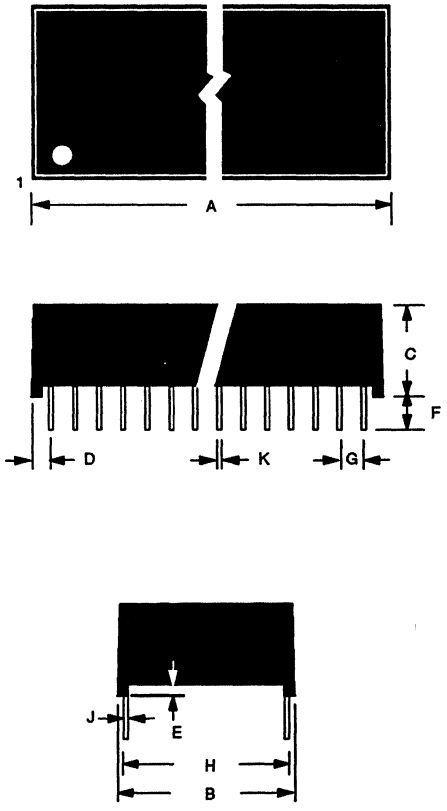
NOTES

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1486 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$(INTB) are open drain outputs.

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1486 32 PIN 740 MIL MODULE



PKG	32-PIN	
DIM	**MIN**	**MAX**
A IN.	1.720	1.740
MM	43.69	44.20
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.090	0.120
MM	2.29	3.05
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

6

PRELIMINARY

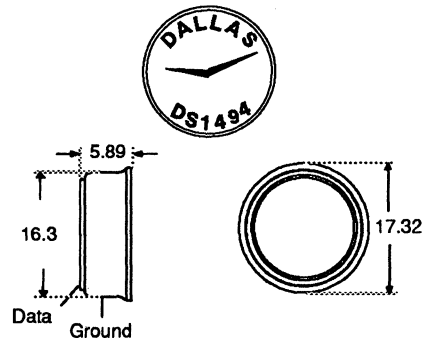
DALLAS SEMICONDUCTOR

DS1494L-F5
Time-In-a-Can

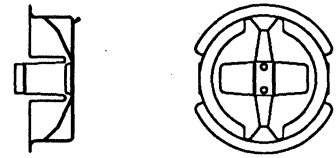
FEATURES
- Miniature timekeeping system sealed in a 16mm MicroCan
- Snaps into a surface-mounted printed circuit board retainer
- Self-powered with greater than 10 years of lithium
- Keeps precise time in 1/256 second increments
- Quartz accuracy to ± 2 minutes per month
- Interval timer measures duration of an activity
- Number of power on/off cycles detected and stored in cycle counter
- Programmable alarms generate interrupts for real time, interval timer and/or cycle count
- 4096 bits of nonvolatile SRAM organized in 16 pages of 256 bits
- Data integrity assured by verifying data in a scratchpad before transferring to memory
- 1-wire interface shares only one I/O pin for 16K bits per second communication
- Unique 48-bit, factory-lasered serial number for identification and traceability
- Tamper-proof lock bits prevent alteration of timers and cycle counter
- Operating temperature range -20 to 70°C
- Applications include computer real-time clock, run time meter, sequence timer, event recorder, warranty information, maintenance records, configuration, and calibration data

DESCRIPTION
The DS1494L-F5 Time-In-a-Can (TIC) supplies accurate time-of-day information, measures run time, schedules activities, and records vital data. Its one and only signal communicates through the lid of a sealed MicroCan. Dallas Semiconductor's development of this minimal signalling technique for integrated circuits, called 1-wire, made it possible to seal a silicon chip, quartz, and a lithium energy source in an inexpensive stainless steel enclosure, not significantly larger than the battery would have been by itself. Furthermore, the solo data signal simplifies mounting to the printed circuit board and lowers the cost of electrical interface. TIC is a full-feature timekeeping system including a unique, lasered serial number, real-time clock, run-time meter, cycle counter, programmable interrupts, 256-bit scratchpad, and 4096 bits of nonvolatile SRAM.

TIME IN A CAN



DS9098 Surface Mount Snap-In Retainer



ACTUAL SIZE

The unalterable serial number is registered for absolute traceability. TIC surface mounts to a printed circuit board by a snap-in retainer (DS9098) or thru-hole mount (DS9094F). Using a contact probe, data can be read or written even when the printed circuit board is without power. All data is nonvolatile for greater than 10 years.

The DS1494L-F5 shares electrical and mechanical specifications with the DS1994L-F5 Touch Memory Plus Time which is used in Automatic Identification applications (see DS1994 data sheet in Section 12, "Automatic Identification").

DALLAS SEMICONDUCTOR

DS1495/DS1497
RAMified Real Time Clock

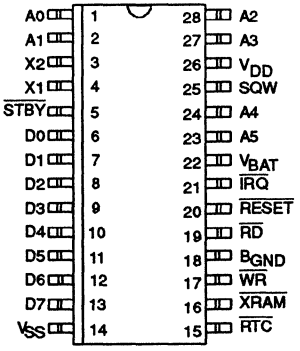
FEATURES

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 kHz mode
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 register/RAM locations plus 8K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general and control registers
  - Separate 8K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End-of-clock update cycle
- 28-pin JEDEC footprint
- Available as chip (DS1495/DS1495S) or stand alone module with embedded lithium battery and crystal

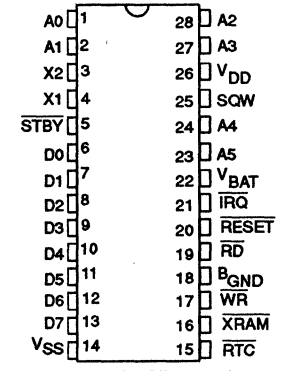
ORDERING INFORMATION

DS1495	RTC Chip; 28 pin DIP
DS1495S	RTC Chip; 28 pin SOIC
DS1497	RTC Module; 28 pin DIP

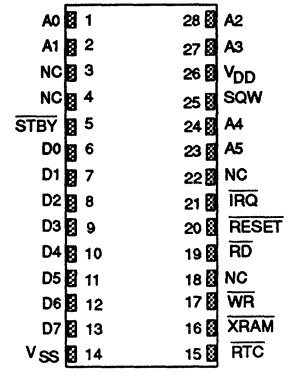
PIN ASSIGNMENT



DS1495S 28-Pin SOIC (330 mil)



DS1495 28-Pin DIP (600 mil)



DS1497 28-Pin Encapsulated Package (720 mil)

PIN DESCRIPTIONS

V_{DD}, V_{SS} – Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 – Data Bus (bidirectional): Data is written into the device from the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a write cycle at the rising edge of a $\overline{WR}$ pulse. Data is read from the device and driven onto the data bus if either $\overline{XRAM}$ or $\overline{RTC}$ is asserted during a read cycle when the $\overline{RD}$ signal is low.

A0-A5 – Address Bus (input): Various internal registers of the device are selected by these lines. When $\overline{RTC}$ is asserted, A0 selects between the indirect address register and RTC data register. When the $\overline{XRAM}$ is asserted, A0-A5 addresses a 32–byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

$\overline{RD}$ – Read Strobe (input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either $\overline{RTC}$ or $\overline{XRAM}$ is asserted.

$\overline{WR}$ – Write Strobe (input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the $\overline{XRAM}$ or $\overline{RTC}$ signals.

$\overline{STBY}$ – Standby (input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the $\overline{STBY}$ signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition (V_{DD} is 4.25 volts, typical) is negated, whichever occurs first.

$\overline{RTC}$ – Real Time Clock Select (input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

SQW – Square Wave (output): Frequency selectable output. Frequency is selected by setting register A bits RS0-RS3. See Table 2 for frequencies that can be selected.

$\overline{XRAM}$ – Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are accessible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM pointed to by the page register. Data is driven onto the data bus when $\overline{RD}$ is low. Data is received from the bus when $\overline{WR}$ is pulsed low and then high.

$\overline{IRQ}$ – Interrupt Request (output): The $\overline{IRQ}$ signal is an active low, open drain output that is used as a processor interrupt request. The $\overline{IRQ}$ output follows the state of the IRQF bit (bit 7) in status register C. $\overline{IRQ}$ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

$\overline{RESET}$ – Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When $\overline{RESET}$ is low, the following occurs.

1. The following register bits are cleared:
   a. Periodic interrupt (PIE)
   b. Alarm interrupt enable (AIE)
   c. Update ended interrupt (UF)
   d. Interrupt request flag (IRQF)
   e. Periodic interrupt flag (PF)
   f. Alarm interrupt flag (AF)
   g. Square wave output enable (SQWE)
   h. Update ended interrupt enable (UIE)
2. The $\overline{IRQ}$ pin is in the high impedance state.
3. The RTC is not processor accessible.

ADDITIONAL PIN DESCRIPTION

(FOR DS1495, DS1495S)

X1, X2 – Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF.

V_{BAT} – Battery input for any standard +3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry at 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} in the absence of power should be used to size the external energy source.

B_{GND} – Battery ground: This pin or pin 14 can be used for the battery ground return.

OPERATION

Power-Down/Power-Up: The real time clock will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V_{DD}. When the voltage level applied to the V_{DD} input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When V_{DD} falls below the CE_{THR} (4.25 volts typical), the chip select inputs $\overline{RTC}$ and $\overline{XRAM}$ are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When V_{DD} falls below 3.2 volts (typical), the module is switched over to an internal power source in the case of the DS1497, or to an external battery connected to the V_{BAT} and BGND pins in the case of the DS1495 and DS1495S, so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when $\overline{RTC}$ is asserted low and represents the real time clock. The second set of registers is active when $\overline{XRAM}$ is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

1. Registers C and D are Read Only (status information)
2. Bit 7 of register A is Read Only
3. Bit 7 of the "Seconds" byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 256 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 256 pages of nonvolatile memory available. The address of the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/O spaces. (See Figure 3.)

TIME, CALENDAR AND ALARM LOCATIONS

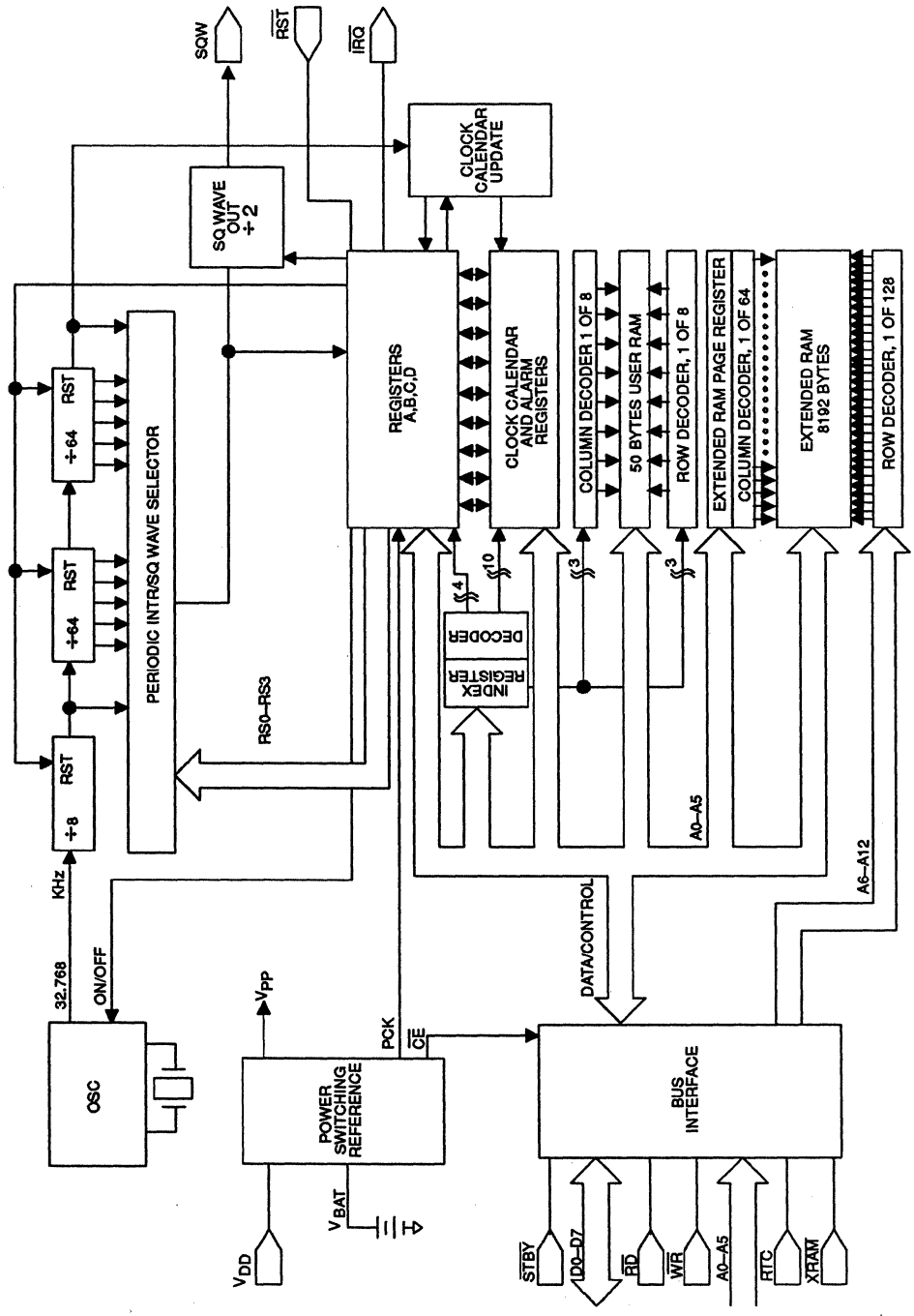
The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

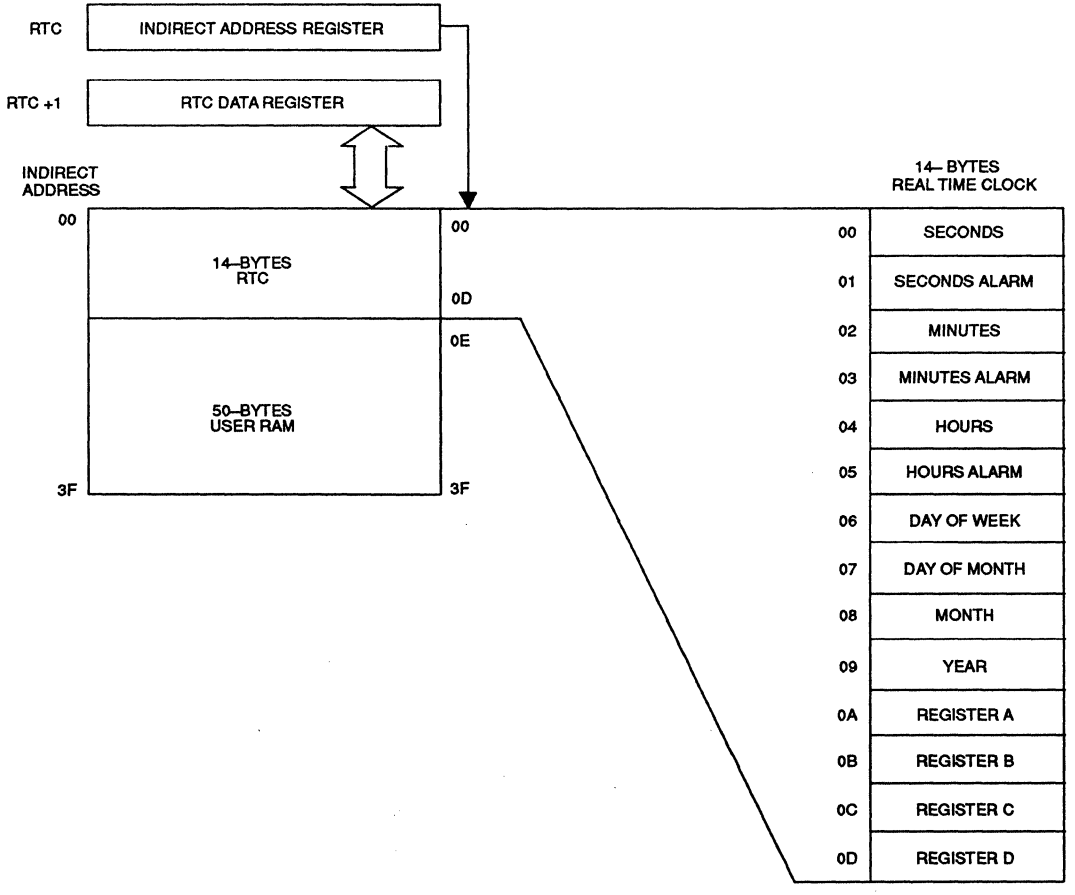
Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high . The second method is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

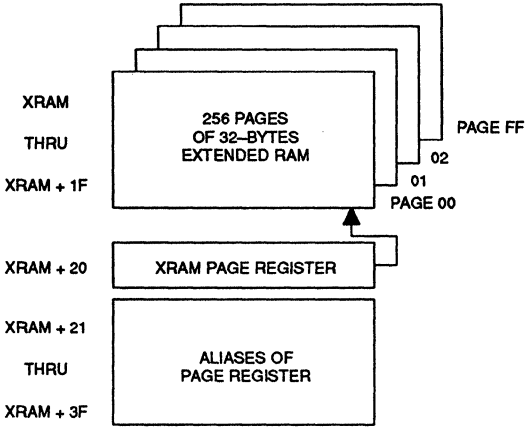
DS149X BLOCK DIAGRAM Figure 1



REAL TIME CLOCK RAM MAP Figure 2



EXTENDED RAM ADDRESS MAP Figure 3



TIME, CALENDAR AND ALARM DATA MODES Table 1

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

USER NONVOLATILE RAM - RTC

The 50 user nonvolatile RAM bytes are not dedicated to any special function within the DS1495/DS1497. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible in the RTC section.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The application program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read. However, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The alternative flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1495/DS1497. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1495/DS1497 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

6

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

UPDATE CYCLE

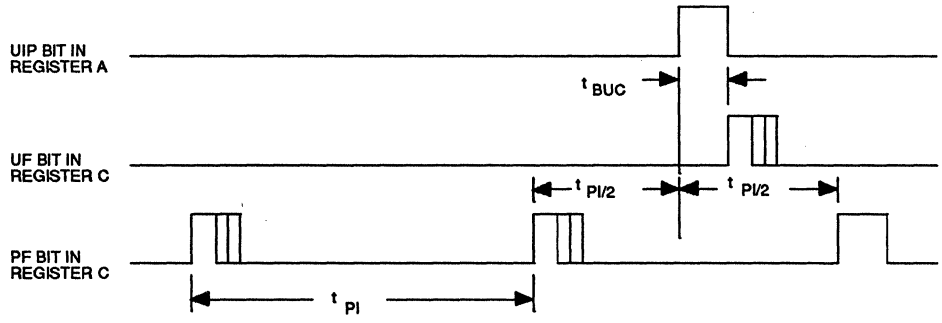
The DS1495/DS1497 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($t_{PI}/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 4



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

REGISTERS

The DS1495/DS1497 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV2, DV1, DV0 - These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1495/DS1497.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1495/DS1497 functions but is cleared by the hardware $\overline{RESET}$ signal.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1495/DS1497 do not affect the AIE bit but is cleared by $\overline{RESET}$.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write bit that enables the Update Ended Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high or the $\overline{RESET}$ pin going low clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{RESET}$.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF – The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
i.e., IRQF = (PF • PIE) + (AF • AIE) + (UF • UIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF – The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C or by $\overline{RESET}$.

AF – A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C or a $\overline{RESET}$ will clear AF.

UF – The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or by $\overline{RESET}$.

BIT 0 THROUGH BIT 3 – These are reserved bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT – The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor Corporation prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 – The remaining bits of Register D are reserved and not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Pin Potential to Ground Pin	-0.3V to +7.0V
Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3V
Power Dissipation	500 mW
Storage Temperature	–40°C to +70°C
Ambient Temperature	0°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High Voltage	Recognized as a High Signal Over Recommended V_{DD} and t_A Range	V_{IH}	2.2	V_{DD}+ 0.3	V V	
Input Low Voltage	Recognized as a Low Signal Over Recommended V_{DD} and t_A Range	V_{IL}	-0.3	0.8	V	
Battery Voltage		V_{BAT}	2.5	3.7	V	

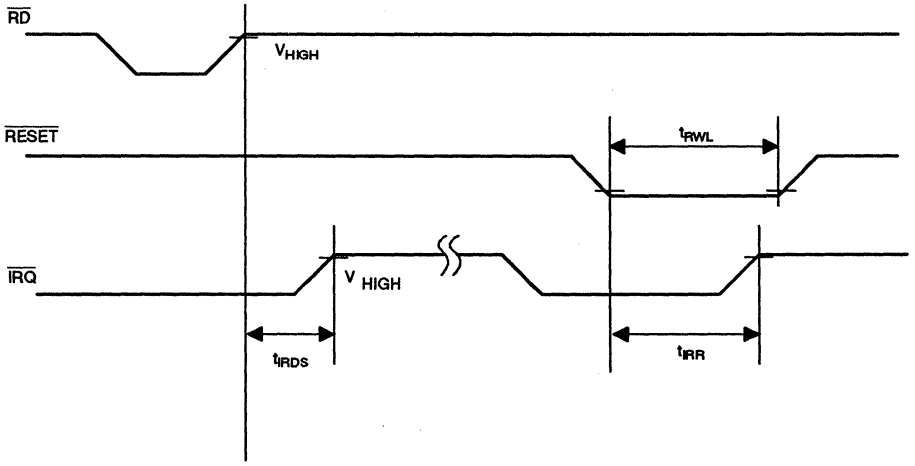
DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, t_A = 0° C to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Input Leakage V_{IL}=0V, V_{IH}=V_{DD}	For any Single Pin: D0-7, $\overline{RD}$, $\overline{WR}$, A0-5, $\overline{XRAM}$, $\overline{RTC}$, $\overline{RESET}$	I_I		±1	µA	
Output High Voltage	V_{DD}=5.0V I_{LOAD} =1 mA	V_{OH}	2.4		V	
Output Low Voltage	V_{DD} = 5.0V I_{LOAD} = 4 mA	V_{OL}		0.4	V	
Power Supply Current	Outputs Unloaded	I_{DD}		50	mA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{DD}	I_{STBY}		+500	µA	
$\overline{STBY}$ pin Input Current	$\overline{STBY}$=V_{SS}	I_{STBY}		–1	µA	

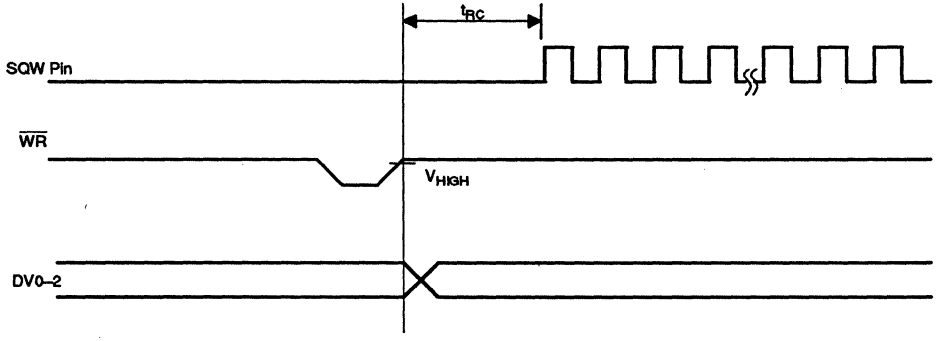
AC SWITCHING CHARACTERISTICS (0°C to 70°C, V_{DD} = 4.5V to 5.5V)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT	NOTES
Reset Pulse Width		t_{RWL}	5		µs	
Oscillator Startup	From Software Enable Via DV Bits	t_{RC}		1	s	
IRQ Release from $\overline{RD}$ High		t_{IRDS}		2	µs	
IRQ Release from $\overline{RESET}$ Low		t_{IRR}		2	µs	

IRQ RELEASE DELAY



OSCILLATOR START-UP



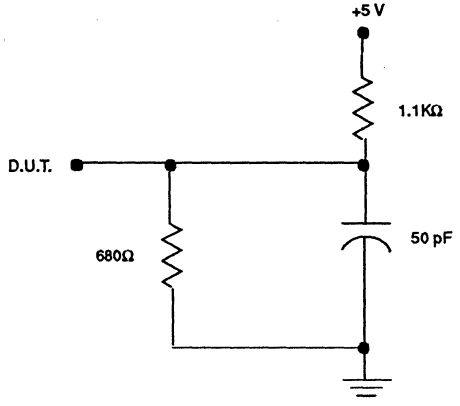
NOTE
Timing assumes RS3-0 Bits = 0011, minimum t_{PI}.

BUS TIMING

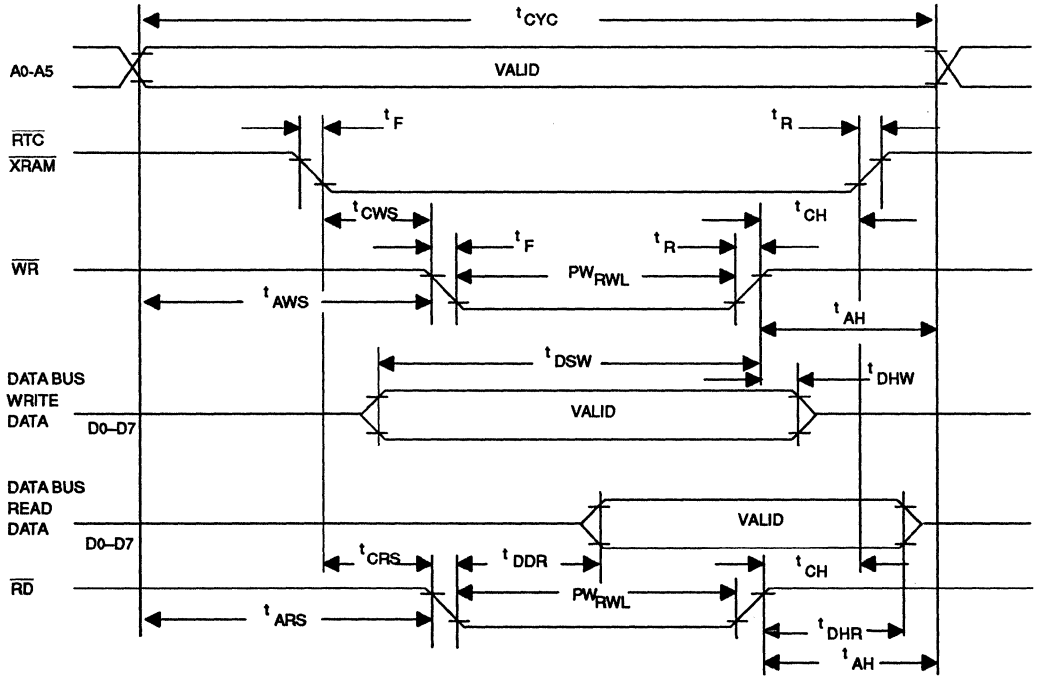
(0° to 70°C, V_{DD} = 4.5V to 5.5V)

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Cycle Time	t_{CYC}	395		DC	ns	
Pulse Width, RD/WR Low	PW_{RWL}	200			ns	
Signal Rise and Fall Time, $\overline{RTC}$, $\overline{XRAM}$, $\overline{RD}$, $\overline{WR}$	t_R, t_F			30	ns	
Address Hold Time	t_{AH}	20			ns	
Address Setup Time Before $\overline{RD}$	t_{ARS}	50			ns	
Address Setup Time Before $\overline{WR}$	t_{AWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{RD}$	t_{CRS}	50			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Setup Time Before $\overline{WR}$	t_{CWS}	0			ns	
$\overline{RTC}$/$\overline{XRAM}$ Select Hold Time After $\overline{RD}$ or $\overline{WR}$	t_{CH}	20			ns	
Read Data Hold Time	t_{DHR}	10		100	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Output Data Delay Time from RD	t_{DDR}	20		200	ns	
Write Data Setup Time	t_{DSW}	200			ns	

OUTPUT LOAD



BUS READ/WRITE TIMING



POWER-DOWN/ POWER-UP TIMING (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	

NOTE

$\overline{CE}$ is chip enabled for access, an internal signal which is defined by ($\overline{RD}$ + $\overline{WR}$) ($\overline{XRAM}$ + $\overline{RTC}$).

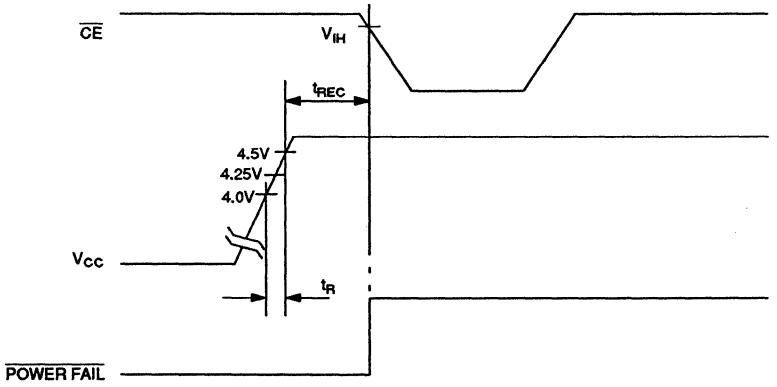
CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

GENERAL INFORMATION

PARAMETER	SYM	MIN	TYP	MAX	UNIT	NOTES
Expected Data Retention @ 25°C (DS1497 only)	t_{DR}	10			Years	
Clock Accuracy for t_{DR} @ 25°C (DS1497 only)	C_Q	±1			Min/Mo	
Clock Accuracy Temperature Coefficient (DS1497)	K			.050	ppm/°C²	
Clock Temperature Coefficient Turnover Temperature (DS1497 only)	t_O	20		30	0°C	
Chip Enable Threshold (DS1497 only)	CE_{THR}			4.5	V	

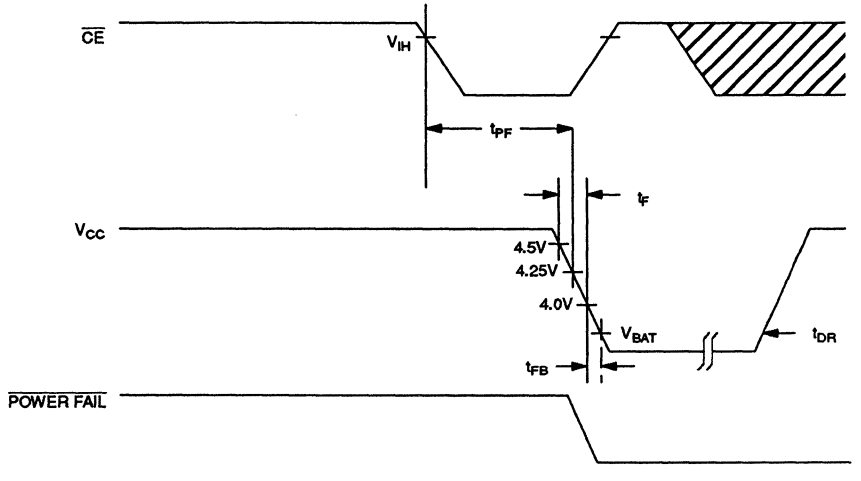
POWER–UP CONDITION



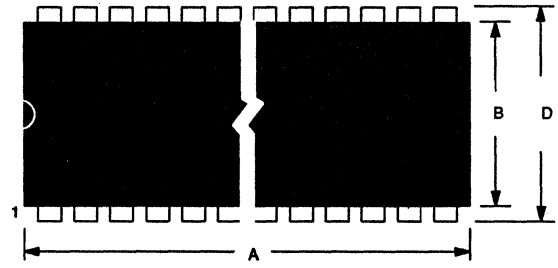
NOTE

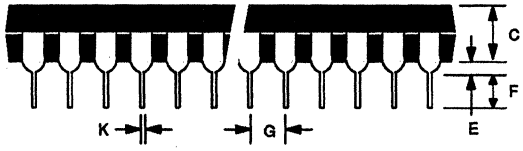
$\overline{CE}$ is an internal signal generated by the power switching reference in the DS149X products.

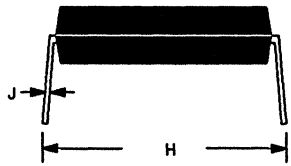
POWER–DOWN CONDITION



DS1495 28 PIN DIP

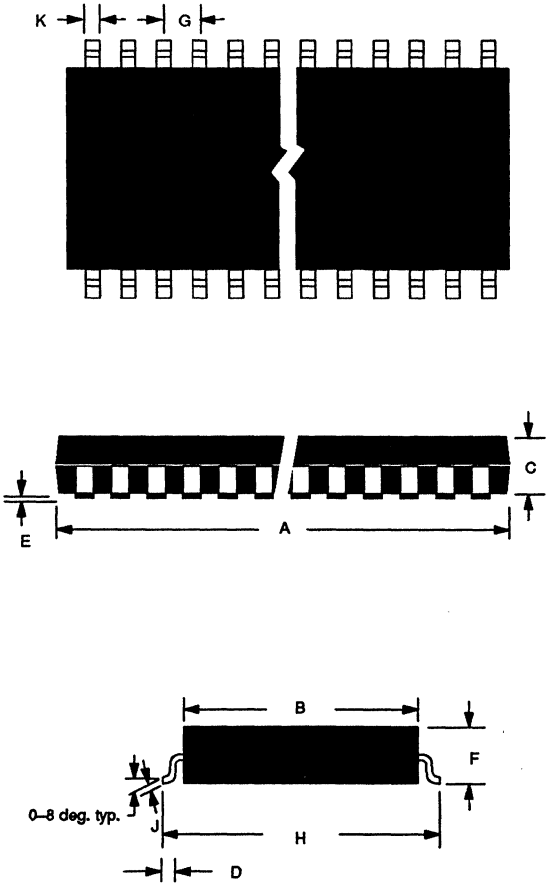






PKG	28–PIN	
DIM	**MIN**	**MAX**
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

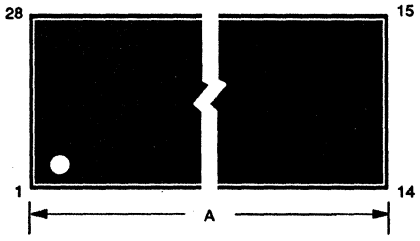
DS1495S 28 PIN SOIC

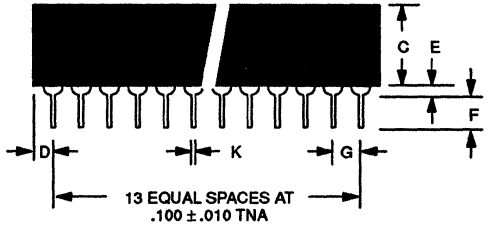


PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	0.480 12.19
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51

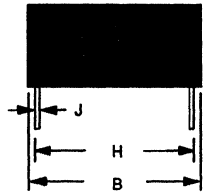
6

DS1497 28 PIN 720 MIL FLUSH ENCAPSULATED





PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 3, 4, 18 AND 22 ARE MISSING BY DESIGN.

DALLAS SEMICONDUCTOR

DS1585/DS1587
Serialized Real Time Clocks

FEATURES

Incorporates industry standard DS1287 PC clock plus enhanced features:

- 64-bit Silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 114 bytes user NVRAM
- 8K bytes additional NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 kHz output for power management

Supports Intel timing mode

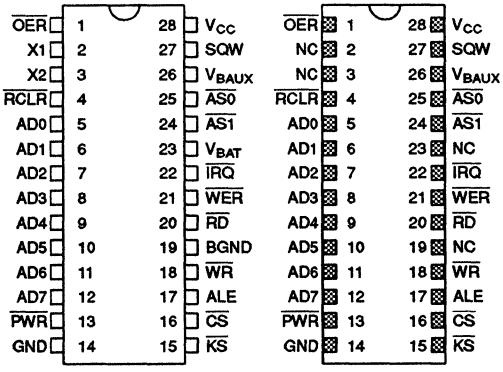
Compatible with existing BIOS for original DS1287 functions

Available as chip (DS1585) or stand-alone module (DS1587) with embedded lithium battery and crystal

PIN DESCRIPTION

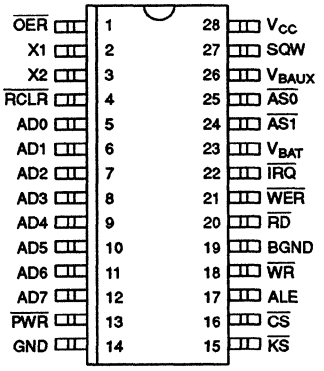
$\overline{OER}$	-	RAM output enable
X1	-	Crystal input
X2	-	Crystal output
$\overline{RCLR}$	-	RAM clear input
AD0-AD7	-	Mux'ed address/data bus
$\overline{PWR}$	-	Power on interrupt output
$\overline{KS}$	-	Kickstart input
$\overline{CS}$	-	RTC Chip select input
ALE	-	RTC address strobe
$\overline{WR}$	-	RTC write data strobe
$\overline{RD}$	-	RTC read data strobe
$\overline{WER}$	-	RAM write data strobe
$\overline{IRQ}$	-	Interrupt request output
$\overline{AS1}$	-	RAM upper address strobe
$\overline{AS0}$	-	RAM lower address strobe
SQW	-	Square wave output
V_{CC}	-	+5V supply
GND	-	Ground
V_{BAT}	-	Battery + supply
V_{BAUX}	-	Auxiliary battery supply
BGND	-	Battery ground

PIN ASSIGNMENT



DS1585 28-PIN DIP (600 MIL)

DS1587 28-PIN ENCAPSULATED PACKAGE (720 MIL)



DS1585S 28-PIN SOIC (330 MIL)

ORDERING INFORMATION

DS1585	RTC Chip; 28 pin DIP
DS1585S	RTC Chip; 28 pin SOIC
DS1587	RTC Module; 28 pin DIP

DESCRIPTION

The DS1585 and DS1587 are RAMified real time clocks (RTC's) designed as upward-compatible successors to the industry standard DS1287, DS1387, DS1487, and DS1488 PC real time clocks. As such, these devices incorporate a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, and 8K bytes of additional NVSRAM.

Each DS1585/DS1587 is individually manufactured with a unique 64-bit serial number. The serial number is written by laser and tested at Dallas to insure that no two devices are alike. As a result, the serial number can be used to electronically identify a system for purposes such as establishment of a network node address, or for maintenance. Blocks of available numbers from Dallas Semiconductor can be reserved by the customer.

The Serialized RTC's also incorporate power control circuitry which allows the system to be powered on via the keyboard or by a time and date (wake up) alarm. The $\overline{PWR}$ output pin can be triggered by one or either of these events, and can be used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

The DS1585 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1587 incorporates the DS1585 chip, a 32.768 kHz crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas such that a minimum of 10 years of timekeeping and data retention in the absence of V_{CC} is guaranteed.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1585/DS1587. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to lithium battery connected either to the V_{BAT} pin or V_{BAUX} pin in the case of the DS1585, or to the internal lithium battery in the case of the DS1587. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 2. The SQW signal can be turned on and off using the SQWE bit in Register B. A 32 kHz SQW signal is output when SQWE=1 and the Enable 32 kHz (E32K) in extended register 04BH and V_{CC} is above 4.25V. A 32 kHz square wave is also available when V_{CC} is less than 4.25 volts typical if E32K=1, ABE=1, and voltage applied to V_{BAUX}.

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1585/DS1587 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the latter portion of ALE, $\overline{AS0}$, or $\overline{AS1}$, at which time the DS1585/DS1587 latches the address from AD0 to AD7. Valid write data must be present and held stable during the latter portion of the $\overline{WR}$ or $\overline{WER}$ pulses. In a read cycle the DS1585/DS1587 outputs 8 bits of data during the latter portion of the $\overline{RD}$ or $\overline{OER}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ or $\overline{OER}$ transitions high.

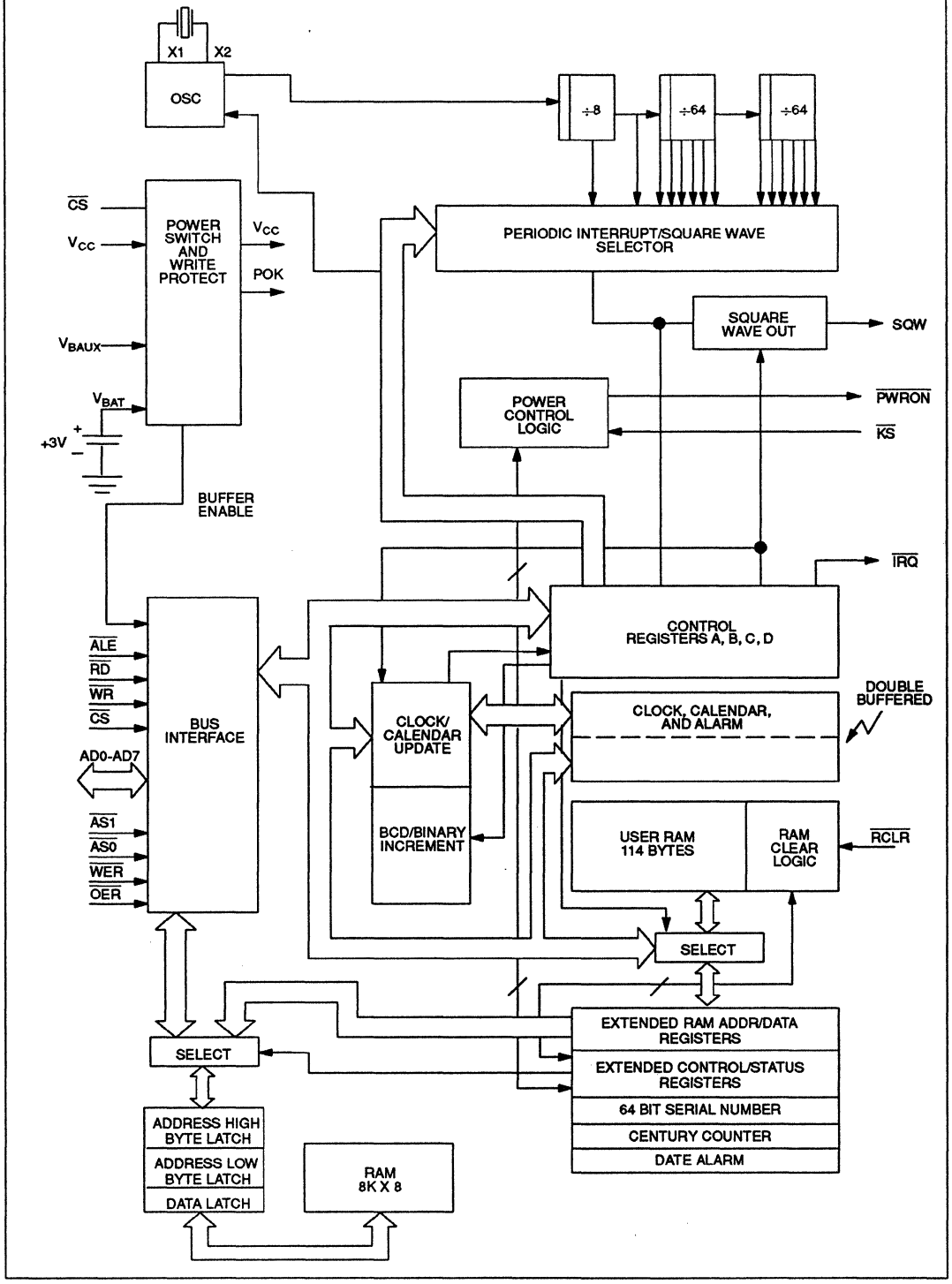
ALE (RTC Address Strobe Input) - A pulse on the address strobe pin serves to demultiplex the bus. The falling edge of ALE causes the RTC address to be latched within the DS1585/DS1587.

$\overline{RD}$ (RTC Read Input) - $\overline{RD}$ identifies the time period when the DS1585/DS1587 drives the bus with RTC read data. The $\overline{RD}$ signal is an enable signal for the output buffers of the clock.

$\overline{WR}$ (RTC Write Input) -The $\overline{WR}$ signal is an active low signal. The $\overline{WR}$ signal defines the time period during which data is written to the addressed clock register.

$\overline{CS}$ (RTC Chip Select Input) - The Chip Select signal must be asserted low during a bus cycle for the RTC portion of the DS1585/DS1587 to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$ timing. Bus cycles which take place with ALE asserted but without asserting $\overline{CS}$ will latch addresses. However, no data transfer will occur.

FIGURE 1: DS1585/DS1587 BLOCK DIAGRAM



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$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS1585/DS1587 that can be tied to the interrupt input of a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to IRQ's active state.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ pin is an open drain output and requires an external pull-up resistor.

$\overline{AS0}$ (RAM Address Strobe Zero) - The rising edge of $\overline{AS0}$ latches the lower eight bits of the 8K x 8 extended RAM address.

$\overline{AS1}$ (RAM Address Strobe One) - The rising edge of $\overline{AS1}$ latches the upper five bits of the 8K x 8 extended RAM address.

$\overline{OER}$ (RAM Output Enable) - $\overline{OER}$ is active low and identifies the time period when the DS1585/DS1587 drives the bus with 8K x 8 extended RAM read data.

$\overline{WER}$ (RAM Write Enable) - $\overline{WER}$ is an active low signal and defines the time period during which data is written to the 8K x 8 extended RAM portion of the DS1585/DS1587.

$\overline{PWR}$ - Power On Output; open drain; active low. The $\overline{PWR}$ pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the DS1585/DS1587, $\overline{PWR}$ may be automatically activated from a Kickstart input via the $\overline{KS}$ pin or from a Wake Up interrupt. Once the system is powered on, the state of the $\overline{PWR}$ can be controlled via bits in the Dallas registers.

$\overline{KS}$ - Kickstart input, active low. When V_{CC} is removed from the DS1585/DS1587, the system can be powered on in response to an active low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and ABE must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. Do not apply positive voltage to the $\overline{KS}$ pin that exceeds V_{BAUX} while in battery-backed mode. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input.

$\overline{RCLR}$ - RAM Clear Input; active low. If enabled by software, taking $\overline{RCLR}$ low will result in the clearing of the 114 bytes of user RAM. When enabled, $\overline{RCLR}$ can be activated whether or not V_{CC} is present.

V_{BAUX} - Auxiliary battery input required for kickstart and wake up features. Also supports clock/calendar and NVRAM function if V_{BAT} at lower voltage or not present. Standard +3 volt lithium cell or other energy source can be used. Battery voltage must be held between +2.5 and +3.7 volts for proper operation. If V_{BAUX} is not going to be used it should be grounded and auxiliary battery enable bit bank 1, register 01BH, should = 0.

(DS1585 ONLY)
X1, X2 - Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S or equivalent. When ordering, request a load capacitance of 6 pF. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF.

V_{BAT} - Battery input for any standard 3 Volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 3.7 volts for proper operation. The nominal write protect trip point voltage is set by the internal circuitry and is 4.25 volts typical. A maximum load of 1 µA at 25°C and 3.0V on V_{BAT} should be used to size the external energy source. This pin is not present on the DS1587 as the battery supply is contained within the package.

BGND - Ground for battery inputs

POWER-DOWN/POWER-UP CONSIDERATIONS

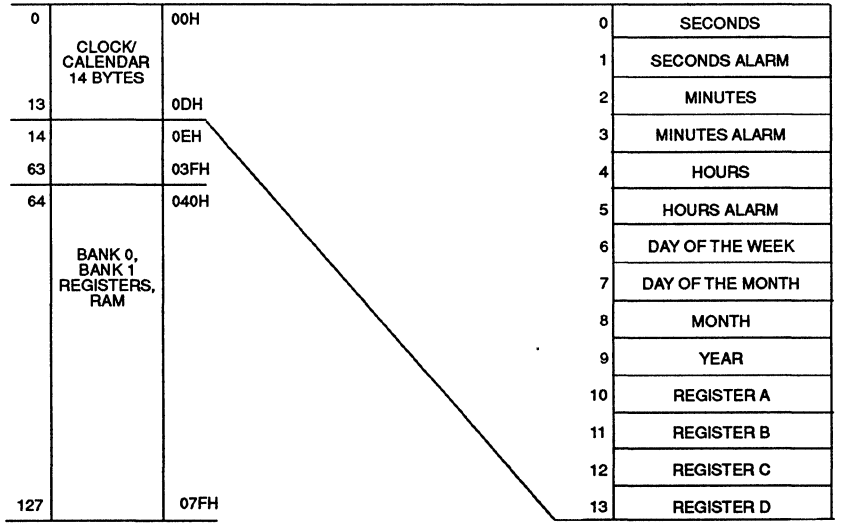
The real-time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1585/DS1587 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip is internally disabled and is, therefore, write-protected. With the possible exception of the $\overline{KS}$, $\overline{PWR}$, and SQW pins, all inputs are ignored and all outputs are in a high impedance state. When the DS1585/DS1587 is in a write-protected state, V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and either the internal lithium energy source or the auxiliary battery supplies power to the real-time clock and the RAM memory.

RTC ADDRESS MAP

The address map for the RTC registers of the DS1585/DS1587 is shown in Figure 2. The address map consists of the 14 clock/calendar registers. Ten registers contain the time, calendar, and alarm data, and four bytes are used for control and status. All registers can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit-7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

FIGURE 2: REAL TIME CLOCK ADDRESS MAP DS1585/DS1587



6

TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate register bytes shown in Table 1. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the time, calendar, and alarm registers can be either Binary or Binary-Coded Decimal (BCD) format. Table 1 shows the binary and BCD formats of the twelve time, calendar, and alarm locations that reside in both bank 0 and in bank 1, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching will be explained later in this text).

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. Also at this time, the data format (binary or BCD), should be set via the data mode bit (DM) of Register B. All time, calendar, and alarm registers must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes.

Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The four alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the four alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second. The three alarm bytes may be used in conjunction with the date alarm as described in the Wakeup/Kickstart section. The century counter will be discussed later in this text.

TABLE 1: TIME, CALENDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
00H	Seconds	0-59	00-3B	00-59
01H	Seconds Alarm	0-59	00-3B	00-59
02H	Minutes	0-59	00-3B	00-59
03H	Minutes Alarm	0-59	00-3B	00-59
04H	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
05H	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
06H	Day of Week Sunday=1	1-7	01-07	01-07
07H	Date of Month	1-31	01-1F	01-31
08H	Month	1-12	01-0C	01-12
09H	Year	0-99	00-63	00-99
BANK 1, 48H	Century	0-99	00-63	00-99
BANK 1, 49H	Date Alarm	1-31	01-1F	01-31

CONTROL REGISTERS

The four control registers; A, B, C, and D reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

NONVOLATILE RAM - RTC

The 114 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1585/DS1587. They can be used by the application program as nonvolatile memory and are fully available during the update cycle. This memory is directly accessible when bank 0 is selected.

INTERRUPT CONTROL

The DS1585/DS1587 includes six separate, fully automatic sources of interrupt for a processor:

1. Alarm interrupt
2. Periodic interrupt
3. Update-ended interrupt
4. Wake up interrupt
5. Kickstart interrupt
6. RAM clear interrupt

The conditions which generate each of these independent interrupt conditions are described in greater detail elsewhere in this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are a total of six bits including three bits in Register B and three bits in Extended Register B which enable the interrupts. The extended register locations are described later. Writing a logic 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ will immediately be set at an active level, even though the event initiating the interrupt condition may have occurred much earlier. As a result, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to a logic 1 in Register C or in Extended Register A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that bits which are set remain stable throughout the read cycle. All bits which were set are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line will be driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ will be held low as long as at least one of the six possible interrupt sources has it s flag and enable bits both set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS1585/DS1587 initiated an interrupt is accomplished by reading Register C and finding IRQF =1. IRQF will remain set until all enabled interrupt flag bits are cleared to 0.

SQUARE WAVE OUTPUT SELECTION

The SQW pin can be programmed to output a variety of frequencies divided down from the 32.768 kHz crystal tied to X1 and X2. The square wave output is enabled and disabled via the SQWE bit in Register B. If the square wave is enabled (SQWE = 1), then the output frequency will be determined by the settings of the E32K bit in Extended Register B and by the RS3-0 bits in Register A. If the E32K = 1, then a 32.768 kHz square wave will be output on the SQW pin regardless of the settings of RS3-0.

If E32K = 0, then the square wave output frequency is determined by the RS3-0 bits. These bits control a 1-of-15 decoder which selects one of thirteen taps that divide the 32.768 kHz frequency. The RS3-0 bits establish the SQW output frequency as shown in Table 2. In addition, RS3-0 bits control the periodic interrupt selection as described below.

If SQWE1, E32K=1, and the Auxiliary Battery Enable bit (ABE, bank 1; register 04BH) is enabled, and voltage is applied to V_{BAUX} then the 32 kHz square wave output signal will be output on the SQW pin in the absence of V_{CC}. This facility is provided to clock external power management circuitry. If any of the above requirements are not met, no square wave output signal will be generated on the SQW pin in the absence of V_{CC}.

OSCILLATOR CONTROL BITS

When the DS1587 timekeeping module with crystal and lithium battery is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium battery from being used until it is installed in a system.

A pattern of 01X in the DV2, DV1, and DV0, bits respectively, will turn the oscillator on and enable the countdown chain. Note that this is different than the DS1287, which required a pattern of 010 in these bits. DV0 is now a "don't care" because it is used for selection between register banks 0 and 1.

A pattern of 11X will turn the oscillator on, but the oscillator's countdown chain will be held in reset, as it was in the DS1287. Any other bit combination for DV2 and DV1 will keep the oscillator off.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same RS3-0 bits in Register A which select the square wave frequency (see Table 2). Changing the bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The Serialized RTC executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

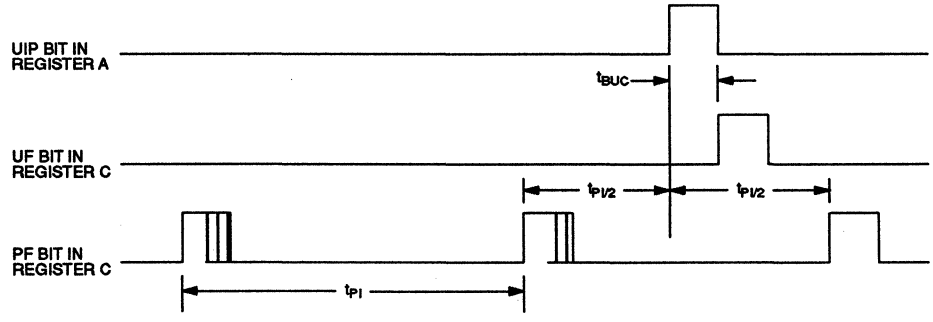
TABLE 2: PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

EXT. REG. B	SELECT BITS REGISTER A				t_{PI} PERIODIC	SQW OUTPUT
E32K	RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	0	None	None
0	0	1	0	1	3.90625 ms	256 Hz
0	0	0	1	0	7.8125 ms	128 Hz
0	0	0	1	1	122.070 µs	8.192 kHz
0	0	1	0	0	244.141 µs	4.096 kHz
0	0	1	0	1	488.281 µs	2.048 kHz
0	0	1	1	0	976.5625 µs	1.024 kHz
0	0	1	1	1	1.953125 ms	512 Hz
0	1	0	0	0	3.90625 ms	256 Hz
0	1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	0	15.625 ms	64 Hz
0	1	0	1	1	31.25 ms	32 Hz
0	1	1	0	0	62.5 ms	16 Hz
0	1	1	0	1	125 ms	8 Hz
0	1	1	1	0	250 ms	4 Hz
1	X	X	X	X	*	32.768 Hz

*RS3-RS0 determine periodic interrupt rates as listed for E32K=0.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within (t_{PI} / 2+t_{BUC}) to ensure that data is not read during the update cycle.

FIGURE 3: UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = PERIODIC INTERRUPT TIME INTERNAL PER TABLE 1
t_{BUC} = DELAY TIME BEFORE UPDATE CYCLE = 244 µs

REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 - These bits are defined as follows:

DV2 = Countdown Chain
- 1 - resets countdown chain only if DV1=1
- 0 - countdown chain enabled

DV1 = Oscillator Enable
- 0 - oscillator off
- 1 - oscillator on

DV0 = Bank Select
- 0 - original bank
- 1 - extended registers

A pattern of 01X is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 01X is written to DV2, DV1, and DV0.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following

Enable the interrupt with the PIE bit;

Enable the SQW output pin with the SQWE bit;

Enable both at the same time and the same rate; or

Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by internal functions of the DS1585/DS1587.

PIE - The Periodic Interrupt Enable bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1585/DS1587 functions.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS1585/DS1587 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 and the E32K bit is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1 WF = WIE = 1
AF = AIE = 1 KF = KSE = 1
UF = UIE = 1 RF = RIE = 1

i.e., IRQF = (PF • PIE) + (AF • ALE) + (UF • UIE) + (WF • WIE) + (KF • KSE) + (RF • RIE)

Any time the IRQF bit is a one, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after Register C is read by the program.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a software read of Register C.

AF - A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C.

BIT 0 THROUGH BIT 3 - These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the internal battery (the battery connected to the V_{BAT} pin in the case of the DS1585) or the battery connected to V_{BAUX}, whichever is at a higher voltage. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

EXTENDED FUNCTIONS

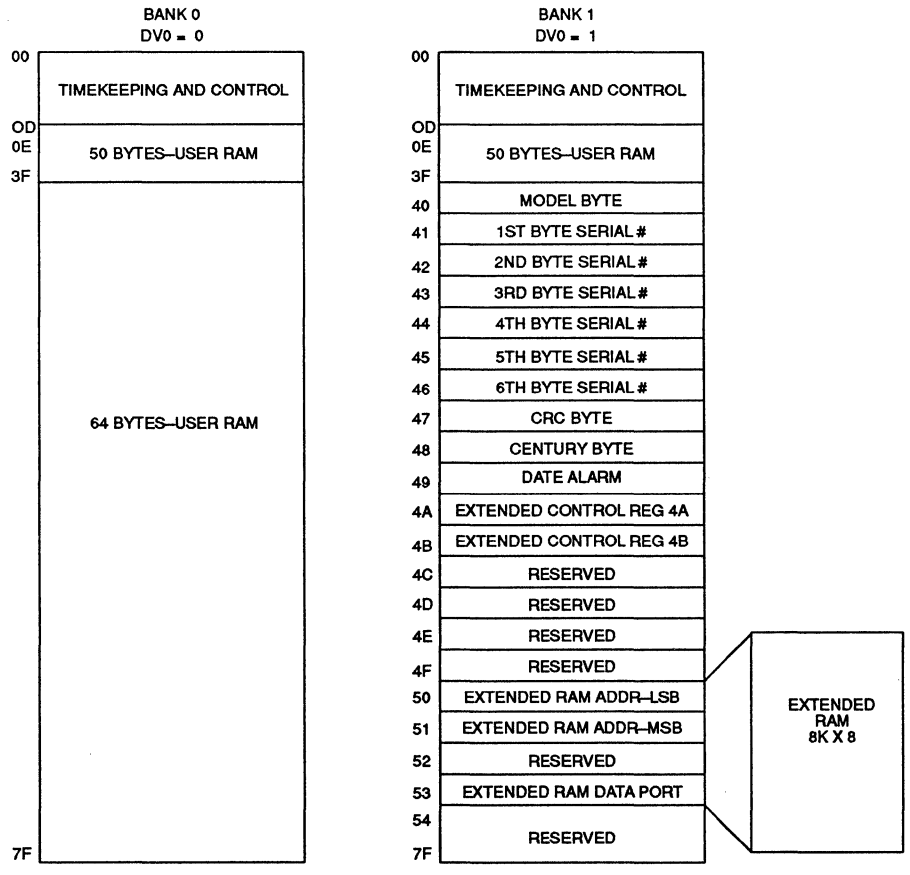
The extended functions provided by the DS1585/DS1587 that are new to the RAMified RTC family are accessed via a software controlled bank switching scheme, as illustrated in Figure 4. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS1585/DS1587 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the Dallas registers which provide control and status for the extended functions will be accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the Dallas registers are listed below:

1. Silicon Revision byte
2. Serial Number
3. Century counter
4. 8 Kbyte Extended RAM access
5. Auxiliary Battery Control/Status
6. Wake Up
7. Kickstart
8. RAM Clear Control/Status

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to a 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and will return a 0 if read.

FIGURE 4: DS1585/DS1587 EXTENDED REGISTER BANK DEFINITION



SILICON SERIAL NUMBER

A unique 64-bit lasered serial number is located in bank 1 registers 40H - 47H. This serial number is divided into three parts. The first byte in register 40H contains a model number to identify the device type and revision of the DS1585/DS1587. Registers 41H-46H contain a unique binary number. Register 47H contains a CRC byte used to validate the data in registers 40H-46H. All 8 bytes of the serial number are read only registers.

The DS1585/DS1587 is manufactured such that no two devices will contain an identical number in locations 41H-48H. Blocks of numbers for these locations can be reserved by the customer. Contact Dallas Semiconductor for special ordering information for DS1585/DS1587's with reserved blocks of serial numbers.

CENTURY COUNTER

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

8K X 8 RAM

The DS1585/DS1587 provides 8K x 8 of on-chip SRAM which is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power OK signal (POK) generated from the write protect circuitry. The POK signal becomes active at 4.25 volts (typical).

The on-chip 8K x 8 nonvolatile SRAM is accessed via the eight multiplexed address/data lines AD7-AD0. Access to the SRAM is controlled by three on-chip latch

registers. Two registers are used to hold the SRAM address, and the third register is used to hold read/write data. The SRAM address space is from 0000H to 1FFFH. A direct hardware interface to the SRAM as well as indirect access under software control is supported.

The hardware access uses four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{OER}$, and $\overline{WER}$ to access the extended SRAM. This access mode is identical to that supported by the DS1385/DS1387 and DS1485/DS1488. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8-bits of address, and $\overline{AS1}$ is used to latch the upper 5-bits of address. It is necessary to meet the setup and hold times given in the Electrical Specifications with valid address information in order to properly latch the address. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation in the hardware access method requires valid data to placed on the bus (AD7-AD0) followed by the activation of the Write Enable RAM ($\overline{WER}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Output Enable RAM ($\overline{OER}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met. The $\overline{WER}$ and $\overline{OER}$ signals should never be active at the same time. In addition, access to the clock/calendar registers and user RAM (via $\overline{CS}$) must not be attempted when the 8K x 8 RAM is being accessed. The RAM is enabled when either $\overline{WER}$ or $\overline{OER}$ is active. $\overline{CS}$ is only used for the access of the clock calendar registers (including the extended Dallas registers) and the 114 bytes of user RAM.

The software method allows access to the 8K x 8 RAM via three of the Dallas registers shown in Figure 2. The Dallas registers in bank 1 must first be selected by setting the DV0 to 1 in Register A. The 13-bit address of the RAM location to be accessed must first be loaded into the two RAM address registers located at 50H and 51H. The least significant address byte should be written to location 50H, and the most significant 5 bits (right-justified) should be loaded in location 51H. Data in the addressed location may be read by performing a read operation from location 53H, or written by performing a write operation to location 53H. Data in any addressed location may be read or written repeatedly without changing the address in locations 50H, 51H.

With the software method, the extended RAM may be accessed using only the control signals assigned to the clock/calendar and 114 byte user RAM; namely, ALE, $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. As a result, the RAM control signals ($\overline{AS1}$, $\overline{AS0}$, $\overline{WER}$, and $\overline{OER}$) do not have to be used and should be tied to their inactive levels.

AUXILIARY BATTERY

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS1585/DS1587's kickstart, wake up, and SQW output features in the absence of V_{CC}. This power source must be available in order to use these auxiliary features when no V_{CC} is applied to the device.

The Auxiliary Battery Enable (ABE; bank 1, register 04BH) bit in extended control register B is used to turn on and off the auxiliary battery for the above functions in the absence of V_{CC}. When set to a 1, V_{BAUX} battery power is enabled, and when cleared to 0, V_{BAUX} battery power is disabled to these functions. In the DS1587, this bit is shipped from the factory cleared to 0.

In the DS1585, this auxiliary battery may be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS1585 is to be backed-up using a single battery with the auxiliary features enabled, then V_{BAUX} should be used and connected to V_{BAT}. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

WAKE UP/KICKSTART

The DS1585/DS1587 incorporates a wake up feature which can power the system on at a pre-determined date through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature can allow the system to be powered up in response to a low going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin. As a result, system power may be applied upon such events as a key closure, or modem ring detect signal. In order to use either the wake up or the kickstart features, the DS1585/DS1587 must have an auxiliary battery connected to the V_{BAUX} pin and the oscillator must be running and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2, DV1, and DV0 are not in this required state, the $\overline{PWR}$ pin will not be driven low in response to a kickstart or wakeup condition, while in battery-backed mode.

The wake up feature is controlled through the Wake up Interrupt Enable bit in extended control register B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake up feature, clearing WIE to 0 disables it. Similarly, the kickstart feature is controlled through the Kickstart Interrupt Enable bit in extended control register B (KSE, bank 1, 04BH).

A wake up sequence will occur as follows: When wake up is enabled via WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar will monitor the current date for a match condition with the date alarm register (bank 1, register 049H). In conjunction with the date alarm register, the hours, minutes, and se-

conds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake up will occur at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm will occur regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin will automatically be driven low. This output can be used to turn on the main system power supply which provides V_{CC} voltage to the DS1585/DS1587 as well as the other major components in the system. Also at this time, the Wake Up flag (WF, bank 1, register 04AH) will be set, indicating that a wake up condition has occurred.

A kickstart sequence will occur when kickstarting is enabled via KSE = 1. While the system is powered down, the $\overline{KS}$ input pin will be monitored for a low going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line will be pulled low, as it is for a wake up condition. Also at this time, the Kickstart Flag (KF, bank 1, register 04AH) will be set, indicating that a kickstart condition has occurred.

The timing associated with both the wake up and kickstarting sequences is illustrated in the Wake Up / Kickstart Timing Diagram in the Electrical Specifications section of this data sheet. The timing associated with these functions is divided into 5 intervals, labeled 1-5 on the diagram.

The occurrence of either a kickstart or wake up condition will cause the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS1585/DS1587 V_{CC} pin rises above the V_{BAT} level before the power on timeout period (t_{POTO}) expires, then $\overline{PWR}$ will remain at the active low level. If V_{CC} does not rise above V_{BAT} voltage in this time, then the $\overline{PWR}$ output pin will be turned off and will return to its high impedance level. In this event, the $\overline{IRQ}$ pin will also remain tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power on sequence will remain set until cleared by software during a subsequent system power on.

If V_{CC} is applied within the timeout period, then the system power on sequence will continue as shown in intervals 2-5 in the timing diagram. During interval 2, $\overline{PWR}$ will remain active and $\overline{IRQ}$ will be driven to its active low level, indicating that either WF or KF was set in initiating the power on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit will be automatically cleared to 0 in response to a successful power on. The $\overline{PWR}$ line will remain active as long as the PAB remains cleared to 0.

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeroes to both of these control bits. As long as no other interrupt within the DS1585/DS1587 is pending, the $\overline{IRQ}$ line will be taken inactive once these bits are reset. Execution of the application software may proceed. During this time, both the wake up and kickstart functions may be used to generate status and interrupts. WF will be set in response to a date, hours, and minutes match condition. KF will be set in response to a low going transition on $\overline{KS}$. If the associated interrupt enable bit is set (WIE and/or KSE) then the $\overline{IRQ}$ line will driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS1585/DS1587 may cause $\overline{IRQ}$ to be driven low. While system power is applied, the on chip logic will always attempt to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake up or kickstart.

The system may be powered down under software control by setting the PAB bit to a logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin will be placed in a high impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake up or kickstart, then the both the WF and KF flags should be cleared and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and nonvolatile RAM is in effect, $\overline{PWR}$ and $\overline{IRQ}$ are tri-stated, and monitoring of wake up and kickstart takes place.

RAM CLEAR

The DS1585/DS1587 provides a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled via the RAM Clear Enable bit (RCE; bank 1, register 04BH). When this bit is set to a logic 1, the 114 bytes of user RAM will be cleared (all bits set to 1) when an active low transition is sensed on the $\overline{RCLR}$ pin. This action will have no effect on either the clock/calendar settings or upon the contents of the 8K x 8 Extended RAM. The RAM clear Flag (RF, bank 1, register 04BH) will be set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE=1, the $\overline{IRQ}$ line will also be driven low upon completion. The interrupt condition can be cleared by writing a zero to the RF bit. The $\overline{IRQ}$ line will then return to its inactive high level provided there are no other pending interrupts. Once the $\overline{RCLR}$ pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in the Electrical Characteristics section.

When RCE is cleared to zero, the RAM clear function is disabled. The state of the $\overline{RCLR}$ pin will have no effect on the contents of the user RAM, and transitions on the $\overline{RCLR}$ pin have no effect on RF.

EXTENDED REGISTERS

Two extended control registers are provided supply controls and status information for the extended features offered by the DS1585/DS1587. These are designated as extended control registers A and B and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows:

EXTENDED CONTROL REGISTER A

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	*	*	PAB	RF	WF	KF

VRT2 - This status bit gives the condition of the auxiliary battery. It is set to a logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as a logic 0, the external battery should be replaced.

INCR - Increment in Progress status bit. This bit is set to a 1 when an increment is in progress to the time/date registers and the alarm checks are being made. INCR will be set to a 1 at 122 µs before the update cycle starts and will be cleared to 0 at the end of each update cycle.

PAB - Power Active Bar control bit. When this bit is 0, the $\overline{PWR}$ pin is in the active low state. This bit can be written to a logic 1 or 0 by the user. If either WF AND WIE = 1 OR KF AND KSE = 1, the PAB bit will be cleared to 0.

RF - Ram Clear Flag. This bit will be set to a logic 1 when a high to low transition occurs on the $\overline{RCLR}$ input (pin 4) if RCE=1. The RF bit is cleared by writing it to a logic 0. This bit can also be written to a logic 1 to force an interrupt condition.

WF - Wake up Alarm Flag - This bit is set to 1 when a wake up alarm condition occurs or when the user writes it to a 1. WF is cleared by writing it to a 0.

KF - Kickstart Flag - This bit is set to a 1 when a kickstart condition occurs or when the user writes it to a 1. This bit is cleared by writing it to a logic 0.

EXTENDED CONTROL REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32K	*	RCE	*	RIE	WIE	KSE

ABE - Auxiliary Battery Enable. This bit when written to a logic 1 will enable the V_{BAUX} pin (pin 26) for extended functions. On the DS1587 with an embedded lithium cell, this bit is shipped from the factory set to a logic 0.

E32K - Enable 32,768 output. This bit when written to a logic 1 will enable the 32,768 Hz oscillator frequency to be output on the SQW pin (pin 27) provided SQWE=1.

RCE - RAM Clear Enable bit. When set to a 1, this bit enables a low level on pin 4 ($\overline{RCLR}$) to clear all 114 bytes of user RAM. When RCE = 0, pin 4 and the RAM clear function are disabled.

RIE - Ram Clear Interrupt Enable. When RIE is set to a 1, the $\overline{IRQ}$ pin will be driven low when a RAM clear function is completed.

WIE - Wake Up Alarm Interrupt Enable. When V_{CC} voltage is absent and WIE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a wake up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to WF being set to 1. When WIE is cleared to a 0, the WF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

KSE - Kickstart Interrupt Enable. When V_{CC} voltage is absent and KSE is set to a 1, the $\overline{PWR}$ pin will be driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin will also be driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ will be driven low in response to KF being set to 1. When KSE is cleared to a 0, the KF bit will have no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

* Reserved bits. These bits are reserved for future use by Dallas Semiconductor. They can be read and written, but have no effect on operation.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-40°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	10
Auxiliary Battery Voltage	V_{BAUX}	2.5		3.7	V	10

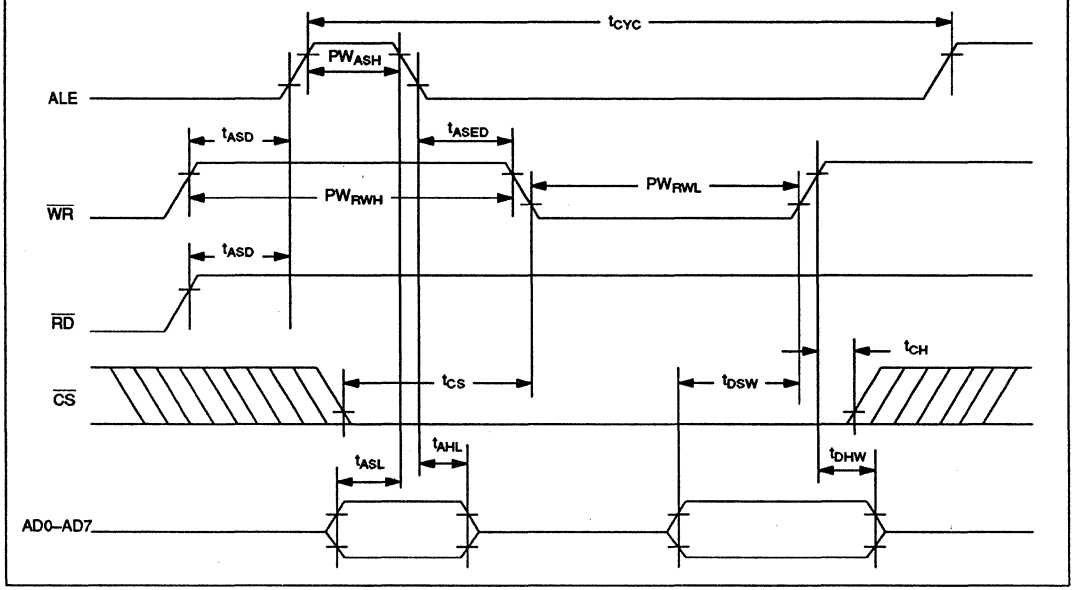
DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		35	50	mA	2
Standby Current $\overline{CS}$ = V_{CC} -0.3V	I_{CC2}		1	5.0	mA	6
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	3, 4
Output @ 2.4V	I_{OH}	-1.0			mA	1, 4
Output @ 0.4V	I_{OL}			4.0	mA	1
Power Fail Trip Point	V_{PF}		4.25		V	1
$\overline{PWR}$ Output @ 0.4V	I_{OLPWR}			10.0	mA	1

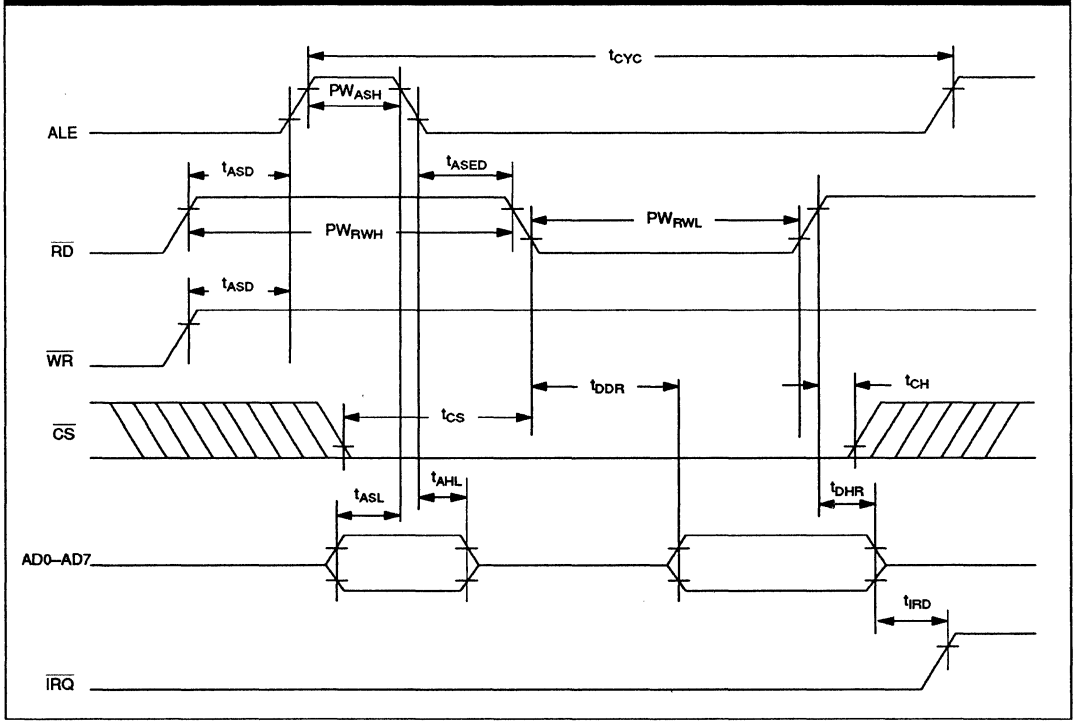
RTC AC TIMING CHARACTERISTICS (0°C TO 70°C, V_{CC} = 4.5V TO 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	305		DC	ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ Low	PW_{OWL}	125			ns	
Pulse Width, $\overline{RD}$/$\overline{WR}$ High	PW_{RWH}	150			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
Chip Select Setup Time Before $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time from ALE fall	t_{AHL}	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}	25			ns	
Pulse Width ALE High	PW_{ASH}	60			ns	
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	t_{ASED}	40			ns	
Output Data Delay Time from $\overline{RD}$	t_{DDR}	20		120	ns	5
Data Setup Time	t_{DSW}	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}			2	µs	

DS1585/DS1587 BUS TIMING FOR WRITE CYCLE TO RTC



DS1585/DS1587 BUS TIMING FOR READ CYCLE TO RTC

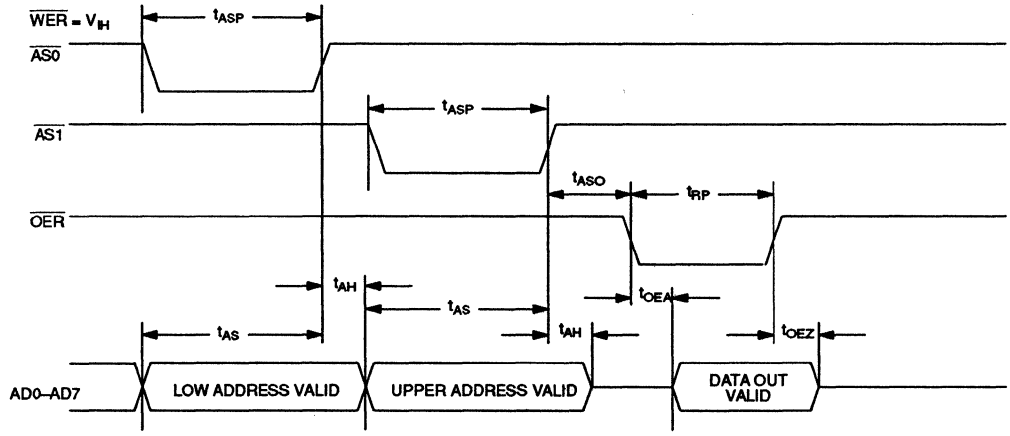


NOTE
Input Levels = 0.8 volts and 2.2 volts.
Output Levels = 0.4 volts and 2.4 volts.

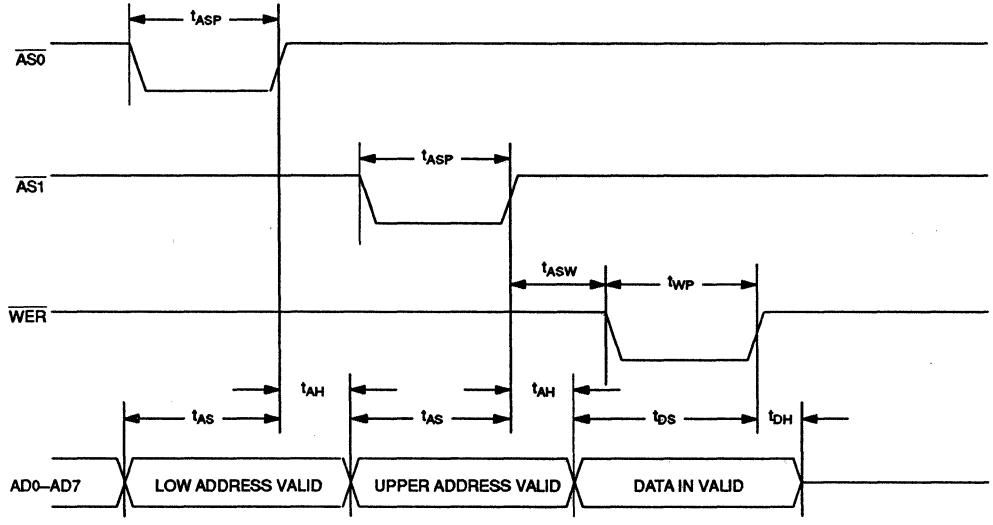
8K X 8 AC TIMING CHARACTERISTICS (0°C TO 70°C, V_{CC} = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access Time	t_{OEA}			200	ns	8
Write Pulse Width	t_{WP}	125			ns	
$\overline{OER}$ to Output in High Z	t_{OEZ}			50	ns	
$\overline{OER}$ Pulse Width	t_{RP}	200			ns	
$\overline{AS0}$, $\overline{AS1}$ Pulse Width	t_{ASP}	75			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{OER}$ Low	t_{ASO}	20			ns	
$\overline{AS0}$, $\overline{AS1}$ High to $\overline{WER}$ Low	t_{ASW}	20			ns	

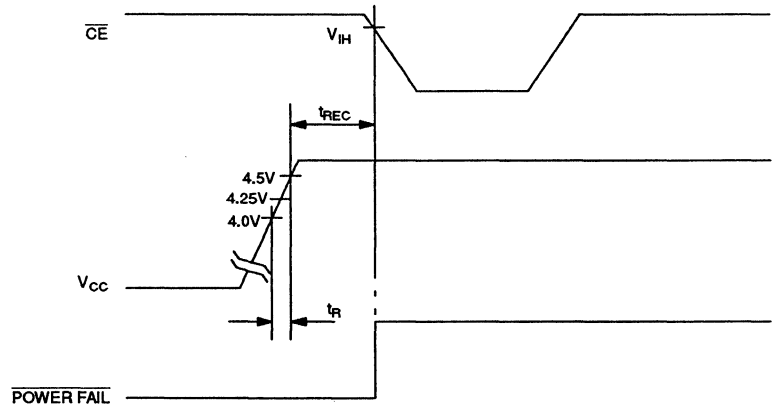
BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM



BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM

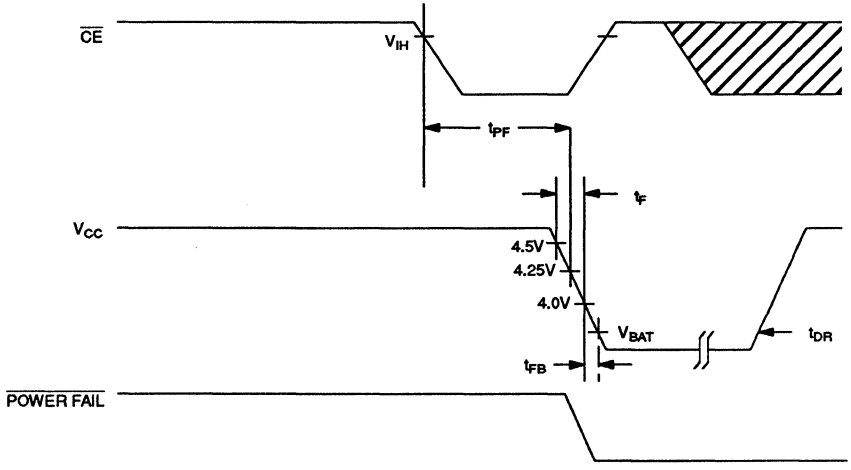


POWER-UP CONDITION



6

POWER-DOWN CONDITION



POWER-UP POWER-DOWN TIMING (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Recovery at Power Up	t_{REC}		150		ms	
V_{CC} Slew Rate Power Down	t_F $4.0 \le V_{CC} \le 4.5V$	300			µs	
V_{CC} Slew Rate Power Down	t_{FB} $3.0 \le V_{CC} \le 4.0V$	10			µs	
V_{CC} Slew Rate Power Up	t_R $4.5V \ge V_{CC} \ge 4.0V$	0			µs	
Expected Data Retention	t_{DR}	10			years	9

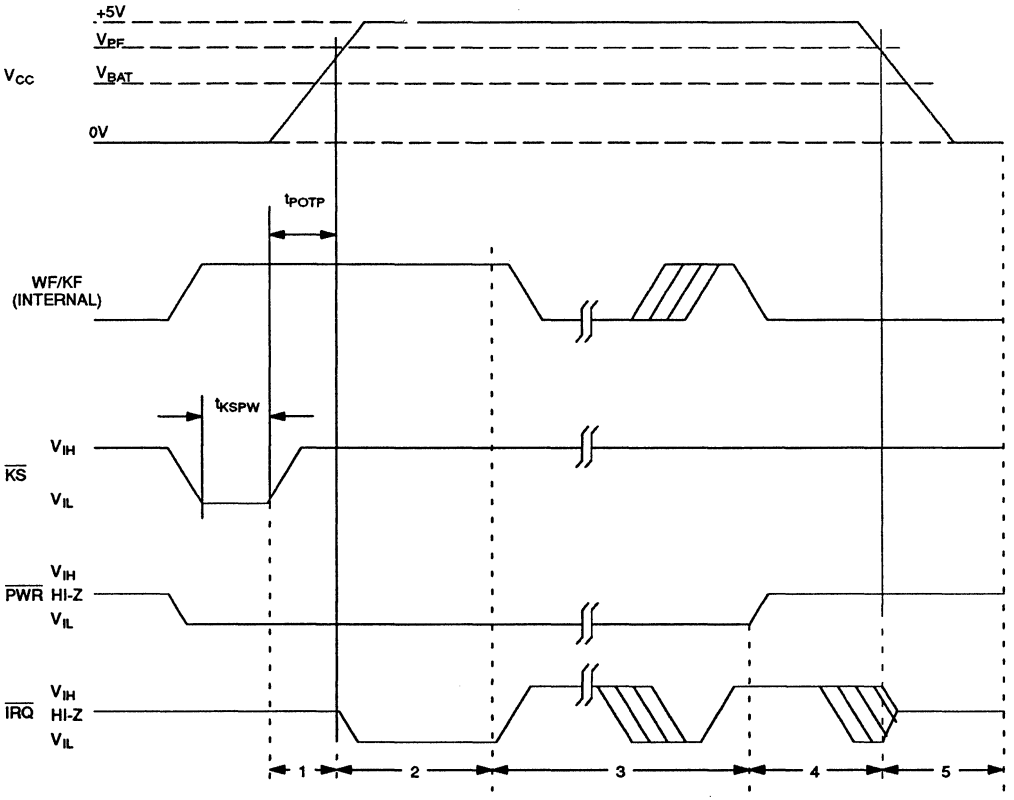
WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			12	pF	
Output Capacitance	C_{OUT}			12	pF	

WAKE UP/KICKSTART TIMING (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t_{KSPW}	2			µs	
Wake up/Kickstart Power On Timeout	t_{POTO}	2			seconds	11

WAKE UP/KICKSTART TIMING



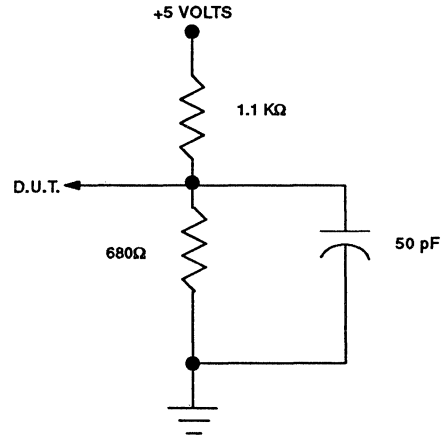
NOTE

Time intervals shown above are referenced in Wake up/Kickstart section.

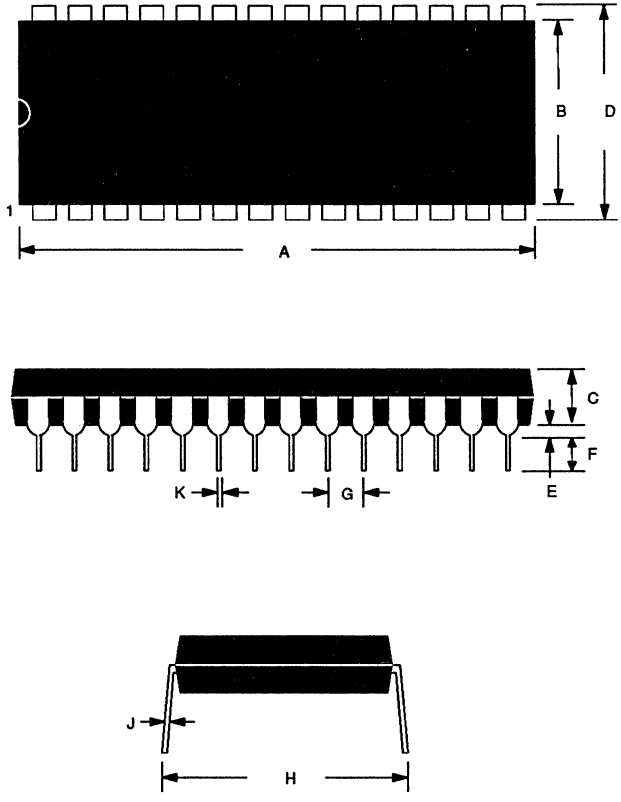
NOTES

1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The $\overline{IRQ}$ pin is open drain.
5. Measured with a load as shown in Figure 5.
6. All other inputs at CMOS levels.
7. Transition current only applies while input is switched from one state to the other. Quiescent input current given by input leakage current specification.
8. Measured with a load as shown in Figure 5.
9. The real-time clock will keep time to an accuracy of ±1 minute per month during data retention time for the period of t_{DR}.
10. Applies to DS1585 only.
11. Wake up/Kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.

FIGURE 5: OUTPUT LOAD



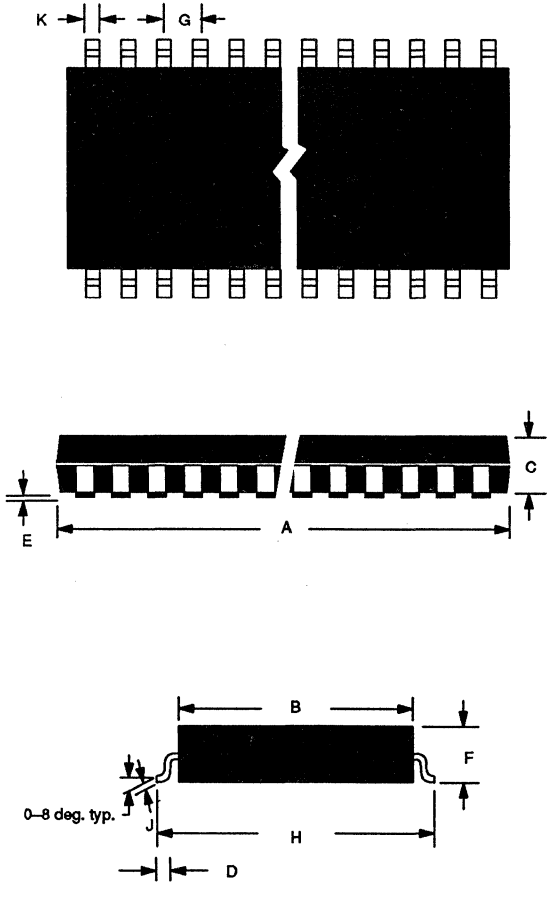
DS1585 28 PIN DIP



PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.445	1.470
MM	36.70	37.34
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

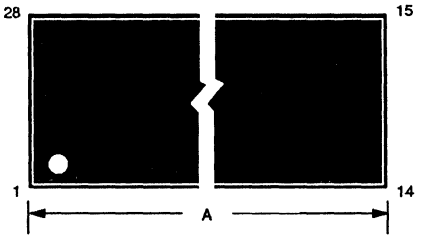
6

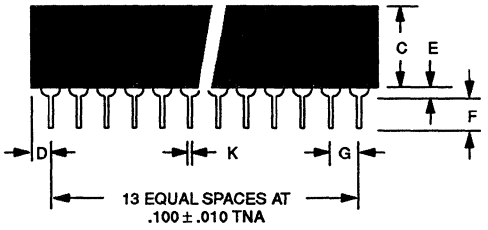
DS1585S 28 PIN SOIC



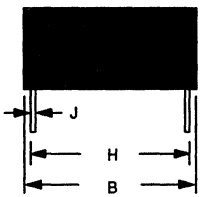
PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	0.706	0.728
MM	17.93	18.49
B IN.	0.338	0.350
MM	8.58	8.89
C IN.	0.086	0.110
MM	2.18	2.79
D IN.	0.020	0.050
MM	0.58	1.27
E IN.	0.002	0.014
MM	0.05	0.36
F IN.	0.090	0.124
MM	2.29	3.15
G IN.	0.050	BSC
MM	1.27	
H IN.	0.460	0.480
MM	11.68	12.19
J IN.	0.006	0.013
MM	0.15	0.33
K IN.	0.014	0.020
MM	0.36	0.51

DS1585 28 PIN 740 MIL MODULE





PKG	28-PIN	
DIM	**MIN**	**MAX**
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.

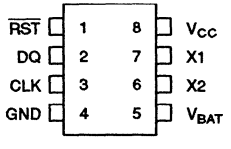
DALLAS SEMICONDUCTOR

DS1602
Elapsed Time Counter

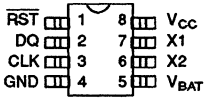
FEATURES

- Two 32 bit counters keep track of real time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V_{BAT} is less than 2.5 volts
- V_{CC} powered counter counts seconds while V_{CC} is above 4.25 volts and retains the count in the absence of V_{CC} under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Maximum current drain of less than 1 µA from V_{BAT} pin when serial port is disabled
- One byte protocol defines read/write, counter address and software clear function
- 8 pin dip or optional 8 pin SOIC
- Operating temperature range = -40°C to +85°C
- Reduced performance operation down to V_{CC} = 2.5V

PIN ASSIGNMENT



DS1602
8 PIN DIP (300 mil)



DS1602
8 PIN SOIC (200 mil)

PIN DESCRIPTION

$\overline{RST}$	-	Reset
CLK	-	Clock
DQ	-	Data input/output
GND	-	Ground
X1, X2	-	Crystal inputs
V_{BAT}	-	+ Battery input
V_{CC}	-	+5 volts

DESCRIPTION

The DS1602 is a real time clock/elapsed time counter designed to count seconds when V_{CC} power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of V_{CC}. The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The V_{CC} powered counter will automatically record the amount of time that V_{CC} power is applied. This function is particularly useful in determining the operational time of equipment in which the DS1602 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1602 takes place via a 3 wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. A low cost 32.768 kHz crystal attaches directly to the XTAL1 and XTAL2 pins. If battery powered only operation is desired, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery.

OPERATION

The main elements of the DS1602 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3 wire serial port. The port is activated by driving $\overline{RST}$ to a high state. With $\overline{RST}$ at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. V_{CC} must be present to access the DS1602. If $V_{CC} < V_{BAT}$ the DS1602 will go into a battery backup mode which disables the serial port to conserve battery capacity. For battery only operations, the V_{BAT} pin must be grounded and the V_{CC} pin must be connected to the battery. This will keep the DS1602 out of battery backup mode. Battery powered operation down to 2.5V is possible with reduced speed performance on the serial port.

PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32 bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V_{CC} active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of $\pm$120 seconds per month at 2°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the I_{BAT} current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to zero when $\overline{RST}$ is taken low. Bit 1 of protocol (designated CVC) is used to clear the V_{CC} active counter. When set to logical 1, the V_{CC} active counter will reset to zero when $\overline{RST}$ is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8 bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input has two functions. First, $\overline{RST}$ turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the $\overline{RST}$ signal provides a method of terminating the protocol transfer or the 32 bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the $\overline{RST}$ input is transitioned low and the D/Q pin goes to a high impedance state. $\overline{RST}$ should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 8 bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until $\overline{RST}$ is transitioned low to end data transfer and then high again to begin new data transfer.

DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32 bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32 bit counter, $\overline{RST}$ must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

CRYSTAL SELECTION

A 32.768 kHz crystal, Daiwa Part No. DT26S or Seiko Part No. DS-VT-200 or equivalent can be directly connected to the DS1602 via pins 2 and 3. The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. Crystals with different load capacitance may cause the RTC oscillator to run faster or slower which effects the clock accuracy.

BATTERY SELECTION

The battery selected for use with the DS1602 should have an output voltage between 2.5 and 3.5 volts. A lithium battery of 35 MAH or greater will run the elapsed time counter for over 10 years in the absence of power. Small lithium coin cell batteries produce both the proper output voltage and have the capacity to supply the DS1602 for the useable lifetime of the equipment where they are installed.

FIGURE 1: DS1602 ELAPSED TIME COUNTER BLOCK DIAGRAM

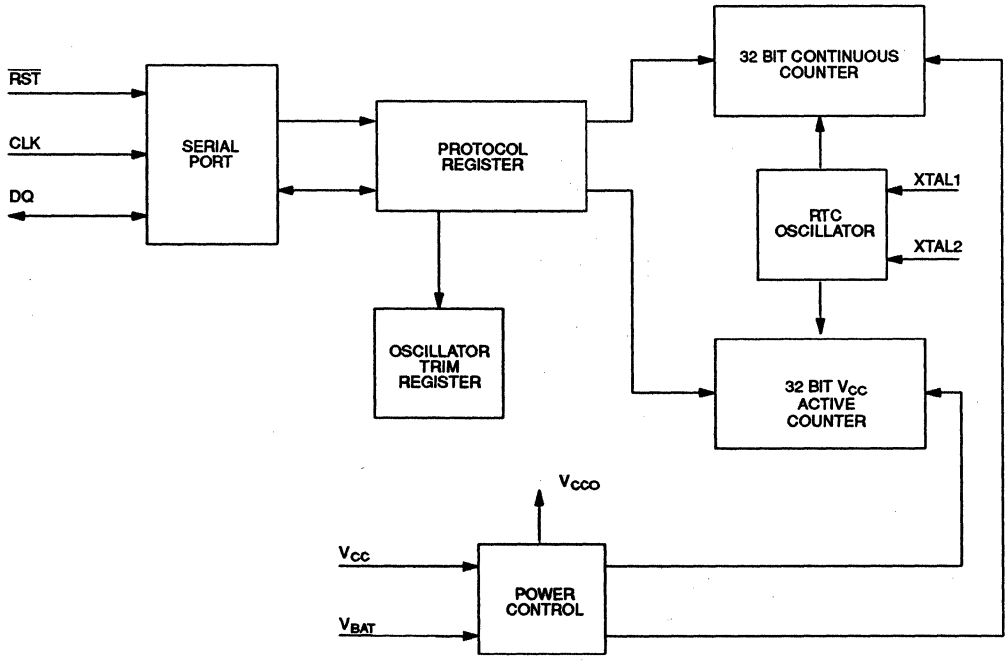


FIGURE 2: PROTOCOL BIT MAP

7	6	5	4	3	2	1	0
ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD

TABLE 1: VALID PROTOCOLS

ACTION	PROTOCOL								DESCRIPTION
	ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD	
Read Continuous Counter	1	0	X	X	X	X	X	1	Output continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V_{CC} Active Counter	0	1	X	X	X	X	X	1	Output V_{CC} active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V_{CC} Active Counter	0	1	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	X	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V_{CC} Active Counter	0	0	X	X	X	X	1	X	Resets the V_{CC} active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	B	C	X	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.

X = Don't Care

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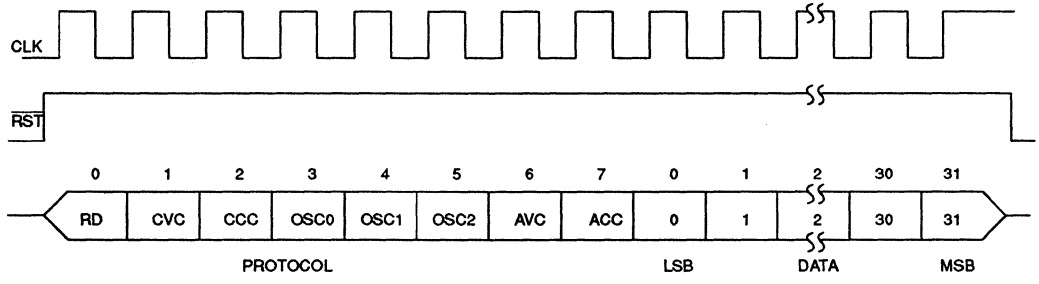
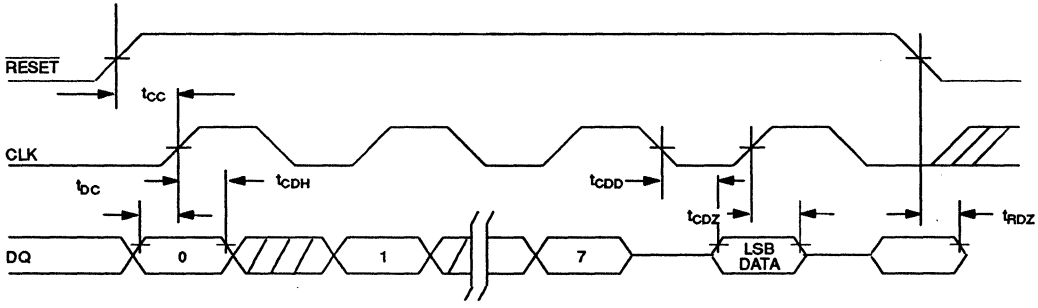
FIGURE 3: DATA TRANSFER

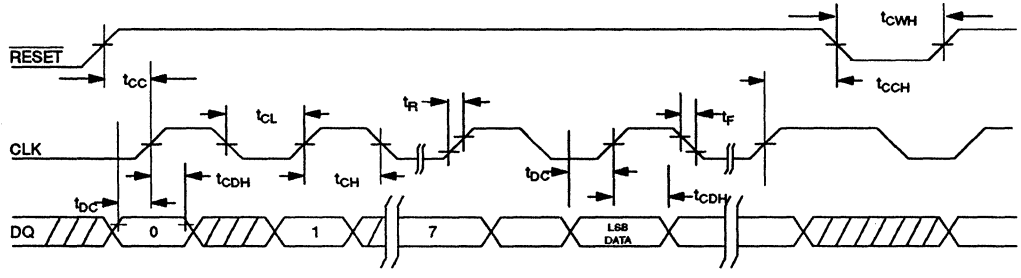


TIMING DIAGRAM: READ/WRITE DATA TRANSFER

READ DATA TRANSFER



WRITE DATA TRANSFER



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	-40°C TO +85°C
STORAGE TEMPERATURE	-55°C TO +125°C
SOLDERING TEMPERATURE	-260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Battery Supply Voltage	V_{BAT}	2.5	3.0	3.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C TO +85°C, V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
I/O Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current	I_{CC}			1	mA	4
Timekeeping Current	I_{CC1}			50	µA	5
Timekeeping Current	I_{BAT}			400	nA	6
Leakage Current	I_{BATL}			100	nA	11

CAPACITANCE (t_A = 25°C)

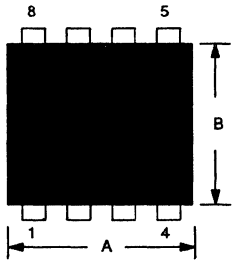
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	10

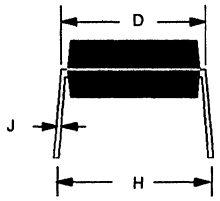
AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5V ±10%, -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	7
CLK to Data Hold	t_{CDH}	70			ns	7
CLK to Data Delay	t_{CDD}			200	ns	7, 8, 9
CLK Low Time	t_{CL}	250			ns	7
CLK High Time	t_{CH}	250			ns	7
CLK Frequency	f_{CLK}	DC		2.0	MHz	7
CLK Rise & Fall	t_F, t_R			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	7
CLK to RST Hold	t_{CCH}	60			ns	7
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	7
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			70	ns	7
CLK High to I/O High Z	t_{CDZ}			20	ns	7

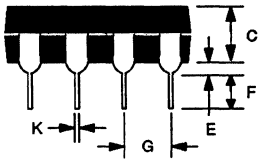
NOTES

1. All voltages are reference to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} is specified with the DQ pin open.
5. I_{CC1} is specified with V_{CC} at 5.0V and $\overline{RST}$ = GND.
6. I_{BAT} is specified with $V_{CC} < V_{BAT}$ and V_{BAT} within DC recommended operating conditions.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
8. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9. Load capacitance = 50 pF.
10. Specified as the load capacitance for which the crystal frequency is guaranteed (see crystal manufacturer's data sheet).
11. Leakage current is the amount of current consumed from the battery when V_{CC} is not present and the oscillator is turned off.

DS1602 8 PIN DIP 300 MIL

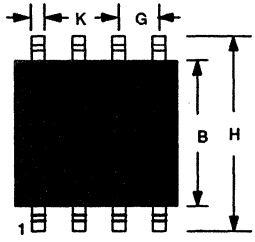


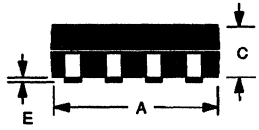




PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.4
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1602 8 PIN SOIC 200 MIL





PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.007 0.254
F IN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.302 7.67	0.318 8.07
J IN. MM	0.006 0.152	0.010 0.254
K IN. MM	0.013 0.33	0.020 0.508
L IN. MM	0.19 4.83	0.030 0.762

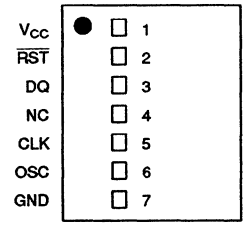
DALLAS SEMICONDUCTOR

DS1603
Elapsed Time Counter Module

FEATURES

- Two 32 bit counters keep track of real time and elapsed time
- Counters keep track of seconds for over 125 years
- Battery powered counter counts seconds from the time battery is attached until V_{BAT} is less than 2.5 volts
- V_{CC} powered counter counts seconds while V_{CC} is above 4.25 volts and retains the count in the absence of V_{CC} under battery backup power
- Clear function resets selected counter to zero
- Read/Write serial port affords low pin count
- Powered internally by a lithium energy cell that provides over 10 years of operation
- One byte protocol defines read/write, counter address and software clear function
- Self contained crystal provides an accuracy of ±1 min per 300 hours of operation
- Operating temperature range = 0°C to +70°C
- Low profile SIP module

PIN ASSIGNMENT



PIN DESCRIPTION

$\overline{RST}$	-	Reset
CLK	-	Clock
DQ	-	Data Input/Output
GND	-	Ground
V_{CC}	-	+5 Volts
OSC	-	1 Hz Oscillator Output
NC	-	No Connection

DESCRIPTION

The DS1603 is a real time clock/elapsed time counter designed to count seconds when V_{CC} power is applied and continually count seconds under battery backup power with an additional counter regardless of the condition of V_{CC}. The continuous counter can be used to derive time of day, week, month, and year by using a software algorithm. The V_{CC} powered counter will automatically record the amount of time that V_{CC} power is applied. This function is particularly useful in determining the operational time of equipment in which the DS1603 is used. Alternatively, this counter can also be used under software control to record real time events. Communication to and from the DS1603 takes place via a 3 wire serial port. A one byte protocol selects read/write functions, counter clear functions and oscillator trim. The device contains a 32.768 kHz crystal which will keep track of time to within ±2 min/mo. An internal lithium energy source contains enough energy to power the continuous seconds counter for over 10 years.

OPERATION

The main elements of the DS1603 are shown in Figure 1. As shown, communications to and from the elapsed time counter occur over a 3 wire serial port. The port is activated by driving $\overline{RST}$ to a high state. With $\overline{RST}$ at high level 8 bits are loaded into the protocol shift register providing read/write, register select, register clear, and oscillator trim information. Each bit is serially input on the rising edge of the clock input. After the first eight clock cycles have loaded the protocol register with a valid protocol additional clocks will output data for a read or input data for a write. V_{CC} must be present to access the DS1603. If V_{CC} < the internal power supply (approximately 3.0 volts) the DS1603 will switch to internal power and disable the serial port to conserve energy. When running off of the internal power supply, only the continuous counter will continue to count and the counter powered by V_{CC} will stop, but retain the count which had accumulated when V_{CC} power was lost.

PROTOCOL REGISTER

The protocol bit definition is shown in Figure 2. Valid protocols and the resulting actions are shown in Table 1. Each data transfer to the protocol register designates what action is to occur. As defined, the MSB (bit 7 which is designated ACC) selects the 32 bit continuous counter for access. If ACC is a logical 1 the continuous counter is selected and the 32 clock cycles that follow the protocol will either read or write this counter. If the counter is being read, the contents will be latched into a different register at the end of protocol and the latched contents will be read out on the next 32 clock cycles. This avoids reading garbled data if the counter is clocked by the oscillator during a read. Similarly, if the counter is to be written, the data is buffered in a register and all 32 bits are jammed into the counter simultaneously on the rising edge of the 32nd clock. The next bit (bit 6 which is designated AVC) selects the 32 bit V_{CC} active counter for access. If AVC is a logical 1 this counter is selected and the 32 clock cycles that follow will either read or write this counter. If both bit 7 and bit 6 are written to a logic high, all clock cycles beyond the protocol are ignored and bit 5, 4, and 3 are loaded into the oscillator trim register. A value of binary 3 (011) will give a clock accuracy of ±120 seconds per month at 25°C. Increasing the binary number towards 7 will cause the real time clock to run faster. Conversely, lowering the binary towards zero will cause the clock to run slower. Binary 000 will stop the oscillator completely. This feature can be used to conserve battery life during storage. In this mode the internal power supply current is reduced to 100 nA maximum. In applications where oscillator trimming is not practical or not needed, a default setting of 011 is recommended. Bit 2 of protocol (designated CCC) is used to clear the continuous counter. When set to logic 1, the continuous counter will reset to zero when $\overline{RST}$ is taken low. Bit 1 of protocol (designated CVC) is used to clear the V_{CC} active counter. When set to logical 1, the V_{CC} active counter will reset to zero when $\overline{RST}$ is taken low. Both counters can be reset simultaneously by setting CCC and CVC both to a logical 1. Bit zero of the protocol (designated RD) determines whether the 32 clocks to follow will write a counter or read a counter. When RD is set to a logical 0 a write action will follow when RD is set to a logical 1 a read action will follow. When sending the protocol, eight bits should always be sent. Sending less than 8 bits can produce erroneous results. If clearing the counters or trimming the oscillator, the data transfer can be terminated after the 8 bit protocol is sent. However, when reading or writing the counters, 32 clock cycles should always follow the protocol.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input has two functions. First, $\overline{RST}$ turns on the serial port logic which allows access to the protocol register for the protocol data entry. Second, the $\overline{RST}$ signal provides a method of terminating the protocol transfer or the 32 bit counter transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For write inputs, data must be valid during the rising edge of the clock. Data bits are output on the falling edge of the clock when data is being read. All data transfers terminate if the $\overline{RST}$ input is transitioned low and the D/Q pin goes to a high impedance state. $\overline{RST}$ should only be transitioned low while the clock is high to avoid disturbing the last bit of data. All data transfers must consist of 8 bits when transferring protocol only or 8 + 32 bits when reading or writing either counter. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 8 bit protocol that inputs write mode, 32 bits of data are written to the selected counter on the rising edge of the next 32 CLK cycles. After 32 bits have been entered any additional CLK cycles will be ignored until $\overline{RST}$ is transitioned low to end data transfer and then high again to begin new data transfer.

DATA OUTPUT

Following the eight CLK cycles that input read mode protocol, 32 bits of data will be output from the selected counter on the next 32 CLK cycles. The first data bit to be transmitted from the selected 32 bit counter occurs on the falling edge after the last bit of protocol is written. When transmitting data from the selected 32 bit counter, $\overline{RST}$ must remain at high level as a transition to low level will terminate data transfer. Data is driven out the DQ pin as long as CLK is low. When CLK is high the DQ pin is tristated.

OSCILLATOR OUTPUT

Pin 6 of the DS1603 module is a 1 Hz output signal. This signal is present only when V_{CC} is applied and greater than the internal power supply. However, the output is guaranteed to meet TTL requirement only while V_{CC} is within normal limits. This output can be used as a one second interrupt or time tick needed in some applications.

INTERNAL POWER

The internal battery of the DS1603 module provides 35 MAH and will run the elapsed time counter for over 10 years in the absence of power.

FIGURE 1: DS1603 ELAPSED TIME COUNTER BLOCK DIAGRAM

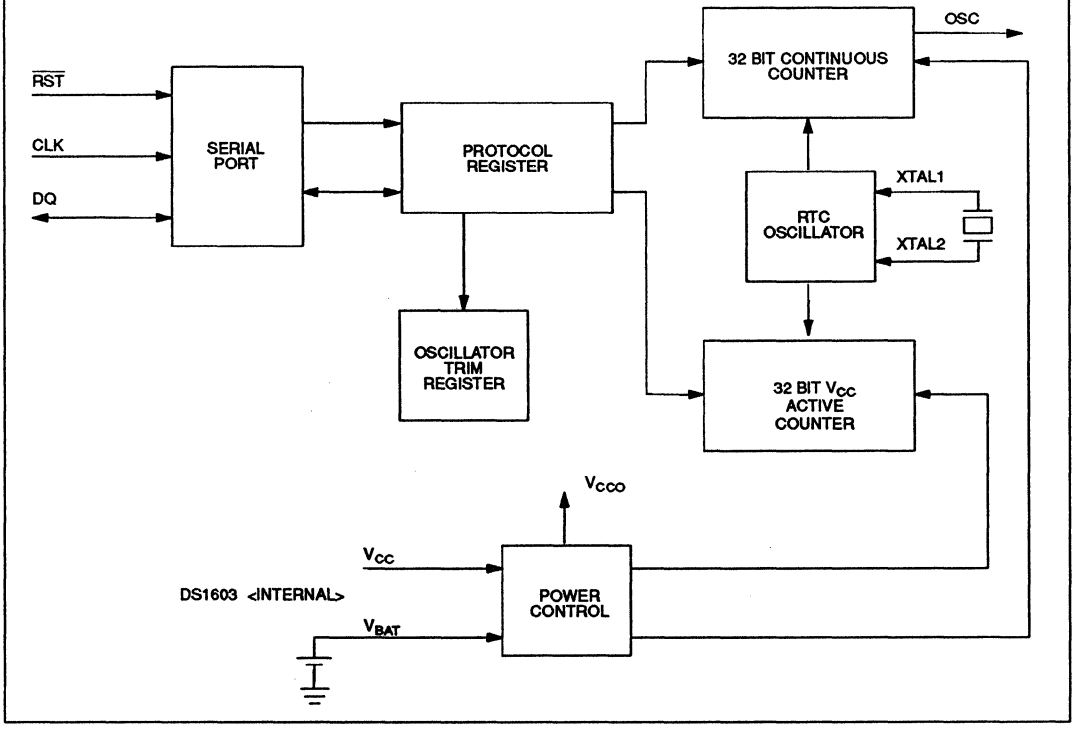


FIGURE 2: PROTOCOL BIT MAP

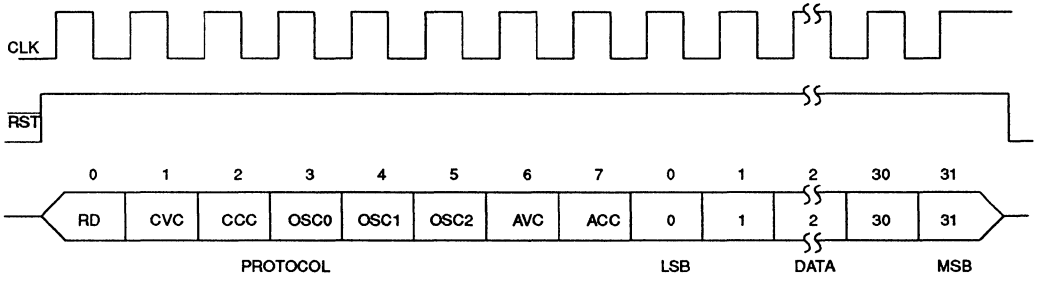
7	6	5	4	3	2	1	0
ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD

TABLE 1: VALID PROTOCOLS

ACTION	PROTOCOL								DESCRIPTION
	ACC	AVC	OSC2	OSC1	OSC0	CCC	CVC	RD	
Read Continuous Counter	1	0	X	X	X	X	X	1	Output continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Write Continuous Counter	1	0	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Read V_{CC} Active Counter	0	1	X	X	X	X	X	1	Output V_{CC} active counter on the 32 clocks following protocol, oscillator trim register is not updated. Counters are not reset.
Write V_{CC} Active Counter	0	1	X	X	X	X	X	0	Input data to continuous counter on the 32 clocks following protocol. Oscillator trim register is not updated. Counters are not reset.
Clear Continuous Counter	0	0	X	X	X	1	X	X	Resets the continuous counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Clear V_{CC} Active Counter	0	0	X	X	X	X	1	X	Resets the V_{CC} active counter to all zeroes at the end of protocol. Oscillator trim register is not updated.
Set Oscillator Trim Bits	1	1	A	B	C	X	X	0	Sets the oscillator trim register to a value of ABC. Counters are unaffected.

X = Don't Care

FIGURE 3: DATA TRANSFER



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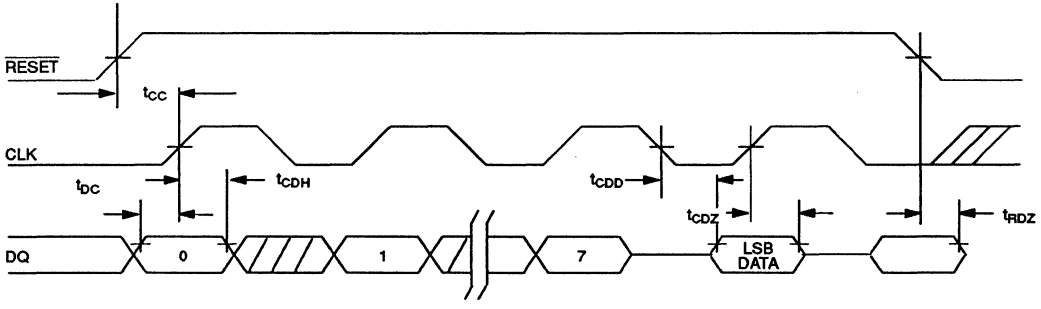
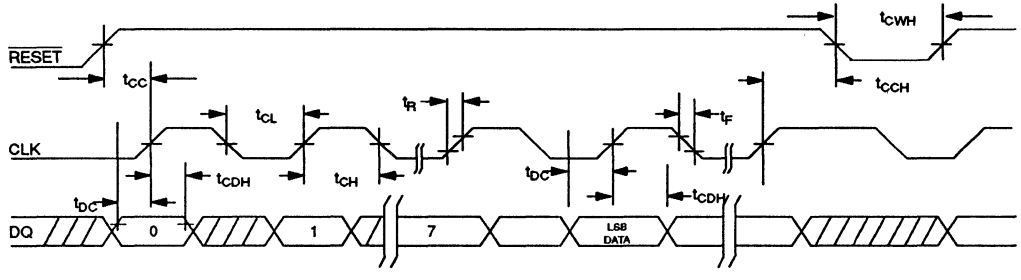
TIMING DIAGRAM: READ/WRITE DATA TRANSFER

READ DATA TRANSFER



WRITE DATA TRANSFER



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.5V TO +7.0V
OPERATING TEMPERATURE	-40°C TO +85°C
STORAGE TEMPERATURE	-55°C TO +125°C
SOLDERING TEMPERATURE	-260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C TO +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C TO +85°C, V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
I/O Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current	I_{CC}			1	mA	4
Timekeeping Current	I_{CC1}			50	µA	5
Battery Trip Point	V_{TP}	2.2		3.7	V	9

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5V ±10%, -40°C TO +85°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	70			ns	6
CLK to Data Delay	t_{CDD}			200	ns	6, 7, 8
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	f_{CLK}	DC		2.0	MHz	6
CLK Rise & Fall	t_F, t_R			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	6
CLK to RST Hold	t_{CCH}	60			ns	6
$\overline{RST}$ Inactive Time	t_{CWH}	1			µA	6
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			70	ns	6
CLK High to I/O High Z	t_{CDZ}			20	ns	6

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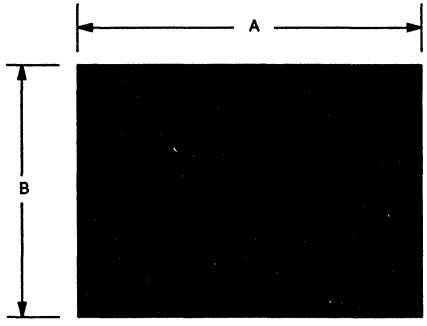
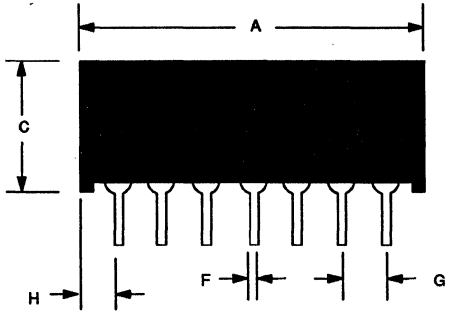
NOTES

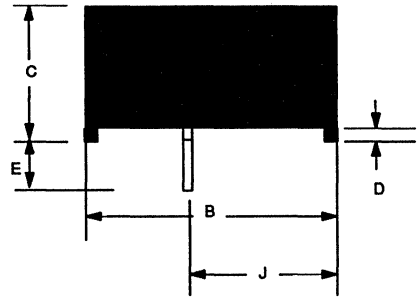
1. All voltages are reference to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} is specified with the DQ pin open.
5. I_{CC1} is specified with V_{CC} at 5.0V and $\overline{RST}$ = GND.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
7. Measured at V_{OH} = 2.4V or V_{OL} - 0.4V.
8. Load capacitance = 50 pF.
9. Battery trip point is the point at which the V_{CC} powered counter and the serial port stop operation.

DS1603 7 PIN MODULE



PKG	7-PIN	
DIM	MIN	MAX
A IN. MM	0.830 21.08	0.850 21.59
B IN. MM	0.650 16.51	0.670 17.02
C IN. MM	0.310 7.87	0.330 8.38
D IN. MM	0.015 0.38	0.030 0.76
E IN. MM	0.110 2.79	0.140 3.56
F IN. MM	0.015 0.38	0.021 0.53
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.105 2.67	0.135 3.43
J IN. MM	0.360 9.14	0.390 9.91





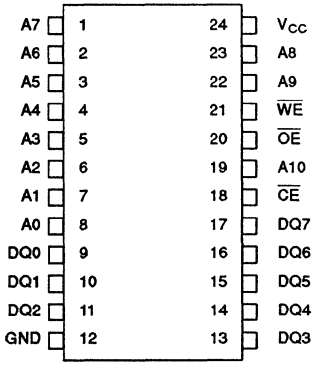
DALLAS SEMICONDUCTOR

DS1642
Nonvolatile Timekeeping RAM

FEATURES

- Form, fit, and function compatible with the MK48T02 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 2K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

PIN ASSIGNMENT



PIN DESCRIPTION

A0-A10	-	Address Input
$\overline{CE}$	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
V_{CC}	-	+5 Volts
GND	-	Ground
DQ0–DQ7	-	Data Input/Output

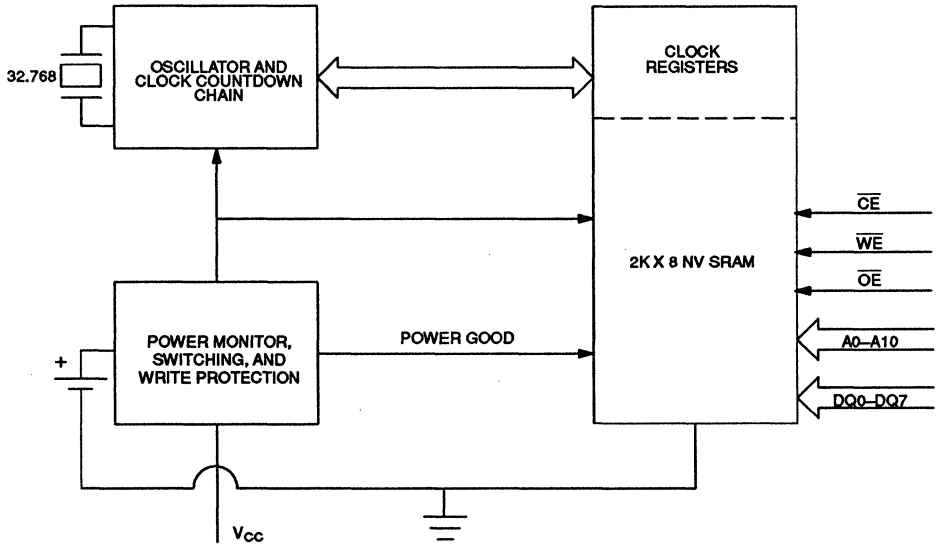
DESCRIPTION

The DS1642 is an 2K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 2K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1642 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1642 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

BLOCK DIAGRAM DS1642 Figure 1



TRUTH TABLE DS1642 Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1642 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, and $\overline{OE}$ low) and address for seconds register remain valid and stable.

CLOCK ACCURACY

The DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1642 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T02 family) will not have any effect even though the DS1642 appears to accept calibration data.

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DS1642 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FF	-	-	-	-	-	-	-	-	YEAR	00-99
7FE	X	X	X	-	-	-	-	-	MONTH	01-12
7FD	X	X	-	-	-	-	-	-	DATE	01-31
7FC	X	FT	X	X	X	-	-	-	DAY	01-07
7FB	X	X	-	-	-	-	-	-	HOUR	00-23
7FA	X	-	-	-	-	-	-	-	MINUTES	00-59
7F9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
7F8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CCI} is within nominal limits ($V_{CC} > 4.5$ volts) the DS1642 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1642 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CCI} supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1642 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1642 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1642 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO +70°C
STORAGE TEMPERATURE	-20°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

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DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ +70°C; V_{CC} (MAX) $\leq V_{CC} \leq V_{CC}$ (MIN))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	–1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{TP}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V + 10%)

PARAMETER	SYMBOL	DS1642-12		DS1642-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V TO 3V
Transition Times: 5 ns

CAPACITANCE

(t_A = 25°C)

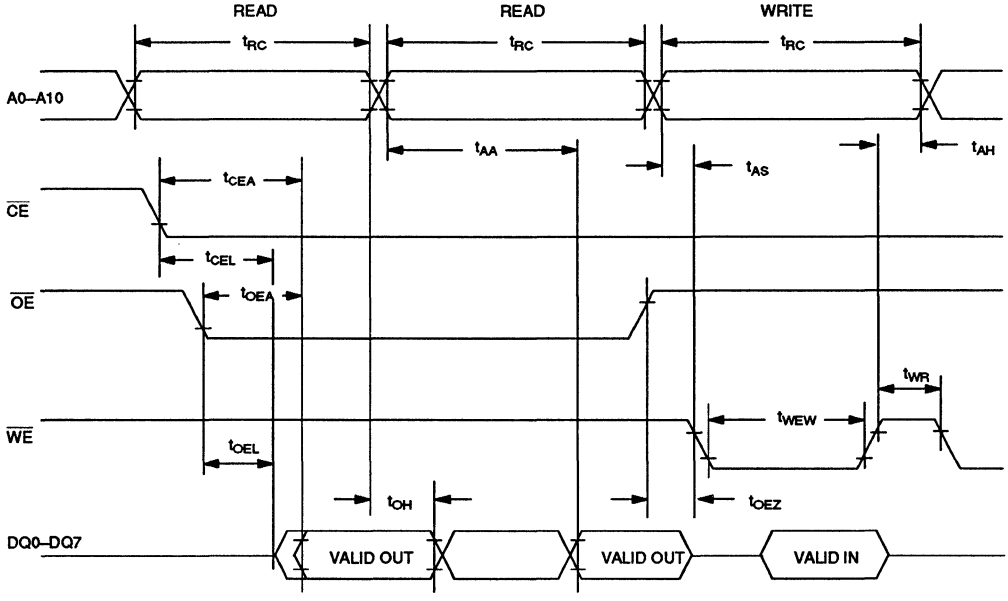
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to +70°C)

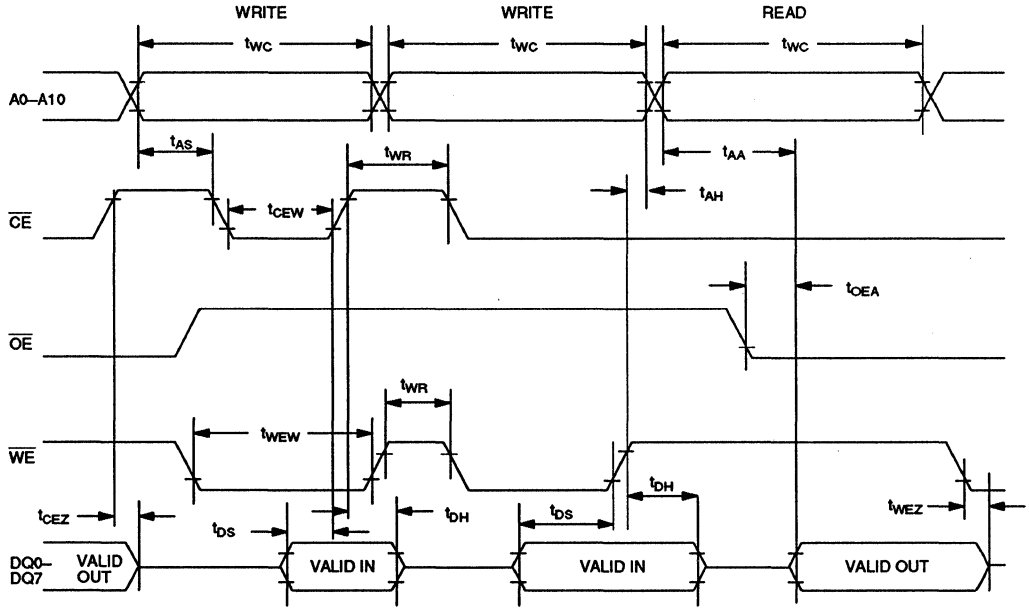
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

6

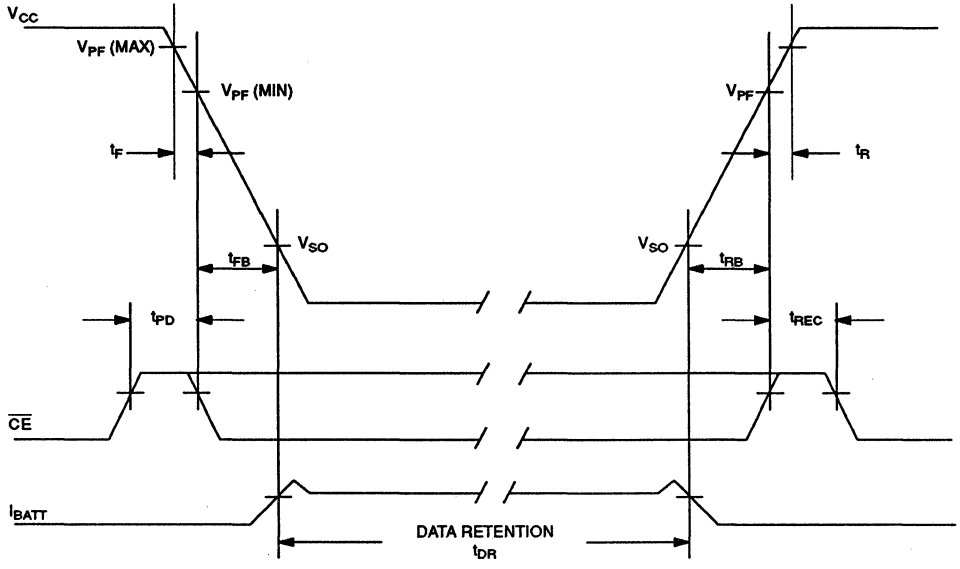
DS1642 READ CYCLE TIMING



DS1642 WRITE CYCLE TIMING



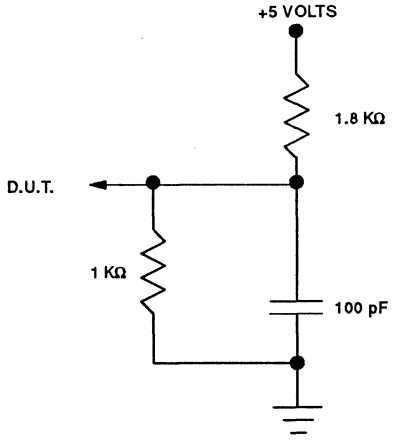
POWER DOWN/POWER UP TIMING



NOTES

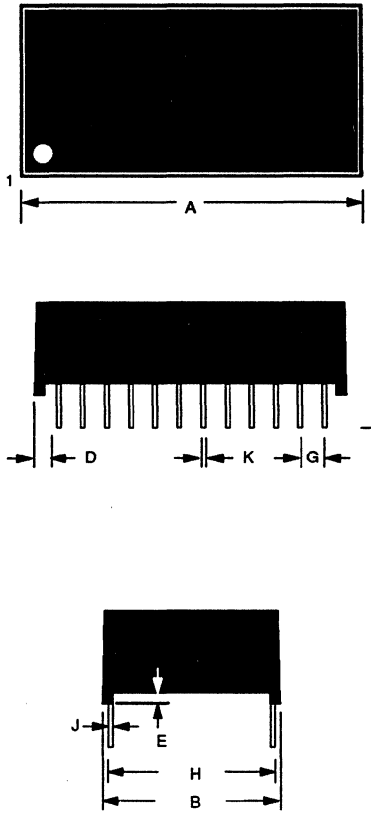
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package plus one year. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD



6

DS1642 24 PIN PACKAGE



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.270	1.290
MM	37.34	37.85
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.315	0.335
MM	8.00	8.51
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.43	0.58

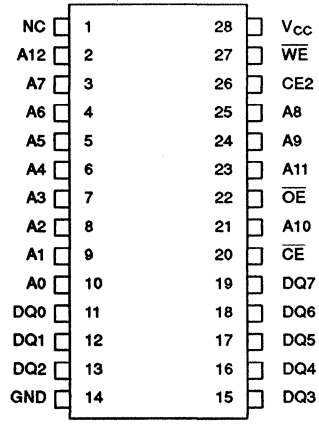
DALLAS SEMICONDUCTOR

DS1643
Nonvolatile Timekeeping RAM

FEATURES

- Form, fit, and function compatible with the MK48T08 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 8K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds
- Power fail write protection allows for ±10% V_{CC} power supply tolerance

PIN ASSIGNMENT



PIN DESCRIPTION

A0-A12	-	Address Input
$\overline{CE}$	-	Chip Enable
CE2	-	Chip Enable
$\overline{OE}$	-	Output Enable
$\overline{WE}$	-	Write Enable
NC	-	No Connection
V_{CC}	-	+5 Volts
GND	-	Ground
DQ0-DQ7	-	Data Input/Output

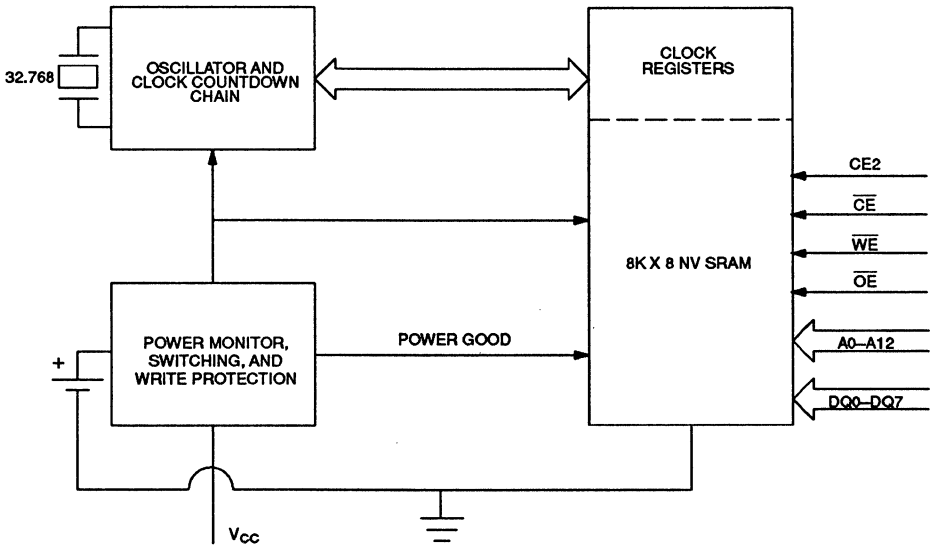
DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS-READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

BLOCK DIAGRAM DS1643 Figure 1



TRUTH TABLE DS1643 Table 1

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	X	DESELECT	HIGH Z	STANDBY
	X	V_{IL}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	V_{IH}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The eighth bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume. Note that both the read bit and write bit perform similar functions and setting both bits during the same access cycle will prevent the clock registers from updating.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, CE2 high, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643 appears to accept calibration data.

DS1643 REGISTER MAP - BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	-	-	-	-	-	-	-	-	YEAR	00-99
1FFE	X	X	X	-	-	-	-	-	MONTH	01-12
1FFD	X	X	-	-	-	-	-	-	DATE	01-31
1FFC	X	FT	X	X	X	-	-	-	DAY	01-07
1FFB	X	X	-	-	-	-	-	-	HOUR	00-23
1FFA	X	-	-	-	-	-	-	-	MINUTES	00-59
1FF9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
1FF8	W	R	-	-	-	-	-	-	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

NOTES

"X" bits are unused but must be set to zero during write cycle to insure proper clock operation.

Bits 0 through 5 of control register A are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever $\overline{WE}$ (write enable) is high, $\overline{CE}$ (chip enable) is low and CE2 (chip enable 2) is high. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$, CE2 and $\overline{OE}$ access times are satisfied. If $\overline{CE}$, CE2, or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$, CE2, and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$, CE2, and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$, $\overline{CE}$, and CE2 are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$, $\overline{CE}$, or CE2. The addresses must be held valid throughout the cycle. $\overline{CE}$, CE2, or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CCI} is within nominal limits (V_{CC} > 4.5 volts) the DS1643 can be accessed as described above by read or write cycles. However, when V_{CCI} is below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ and CE2 signals. When V_{CCI} falls below the level of the internal battery supply, power input is switched from the V_{CCI} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CCI} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1643 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CCI} supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CCI} power. The DS1643 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1643 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CCI} is present. In fact, in most applications, the life expectancy of the DS1643 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
OPERATING TEMPERATURE	0°C TO +70°C
STORAGE TEMPERATURE	-20°C TO +70°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C $\leq t_A \leq$ +70°C; V_{CC} (MAX) $\leq V_{CC} \leq V_{CC}$ (MIN))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}		30	55	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$=V_{CC}-0.2V, CE2=GND+0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Write Protection Voltage	V_{TP}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V + 10%)

PARAMETER	SYMBOL	DS1643-12		DS1643-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ and CE2 Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ and CE2 Data Off Time	t_{CEZ}		40		50	ns	
Output Enable Access Time	t_{OEA}		100		120	ns	
Output Enable Data Off Time	t_{OEZ}		40		50	ns	
Output Enable to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{CE}$ and CE2 to DQ Low-Z	t_{CEL}	5		5		ns	
Output Hold from Address	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	100		120		ns	
Address Hold from End of Write	t_{AH}	15		20		ns	
Write Pulse Width	t_{WEW}	120		150		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10		15		ns	
Data Setup Time	t_{DS}	85		110		ns	
Data Hold Time High	t_{DH}	15		20		ns	

AC TEST CONDITIONS

Input Levels: 0V TO 3V
Transition Times: 5 ns

CAPACITANCE

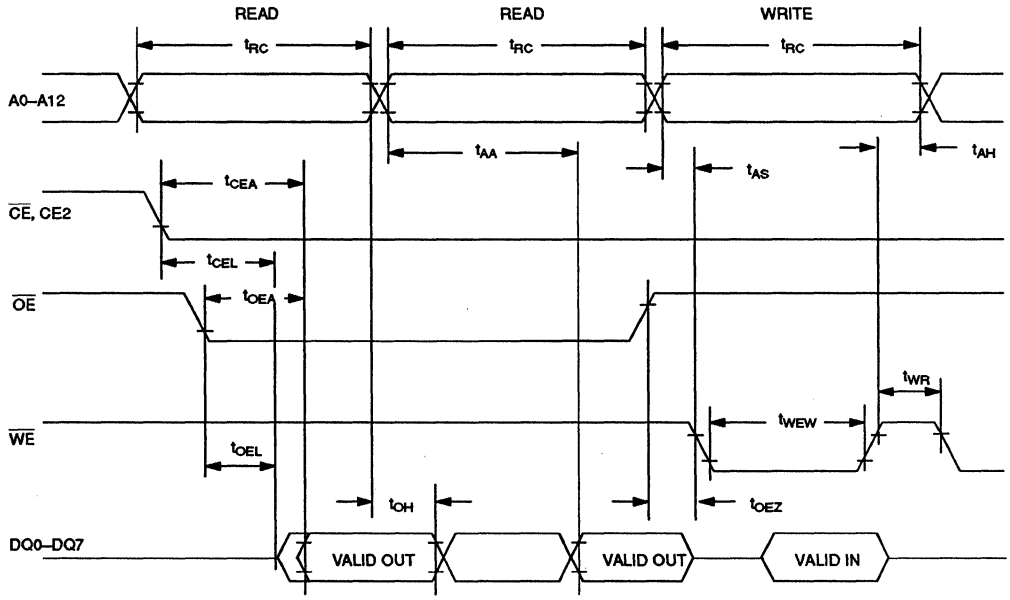
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_I			7	pF	
Capacitance on DQ pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE2, $\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power Up	t_{REC}	15	25	35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

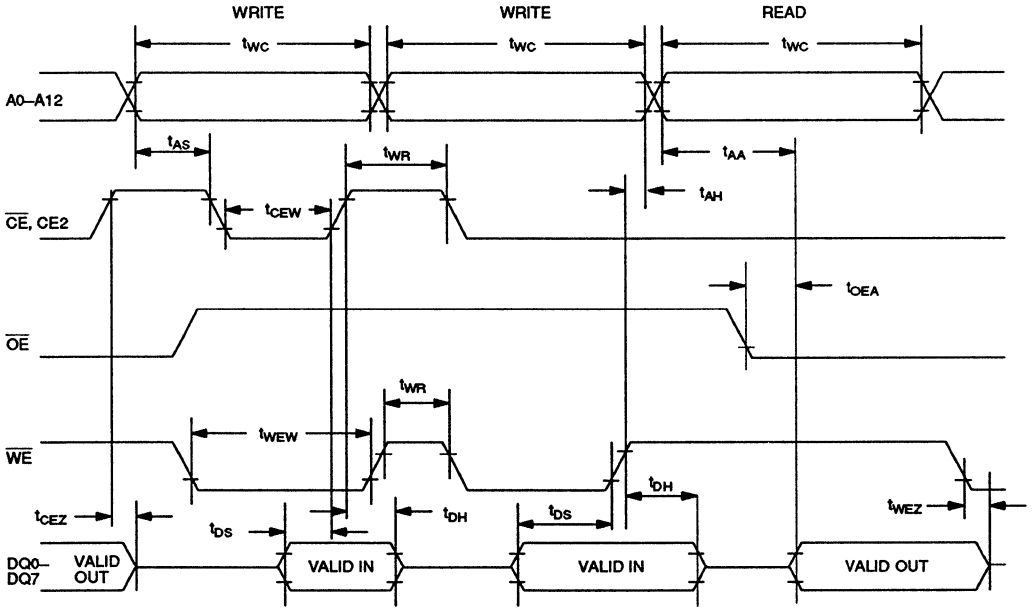
DS1643 READ CYCLE TIMING



NOTE

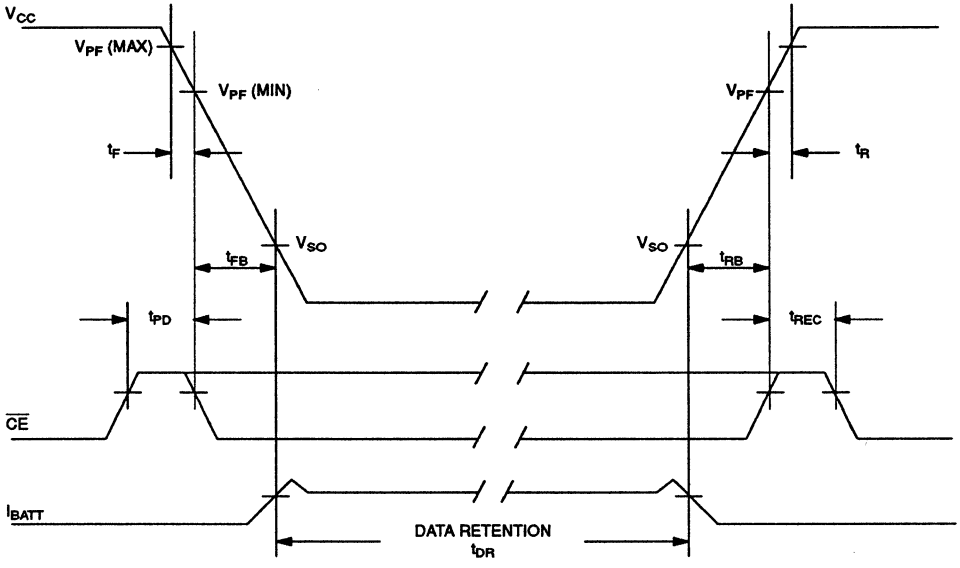
The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to $\overline{CE}$ apply to CE2 with the opposite active state.

DS1643 WRITE CYCLE TIMING



NOTE
The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to $\overline{CE}$ apply to CE2 with the opposite active state.

POWER DOWN/POWER UP TIMING

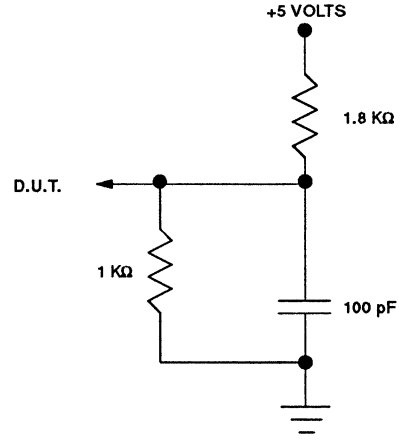


NOTE
The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic for active and inactive levels are exactly opposite. All parameters dimensioned to $\overline{CE}$ apply to CE2 with the opposite active state.

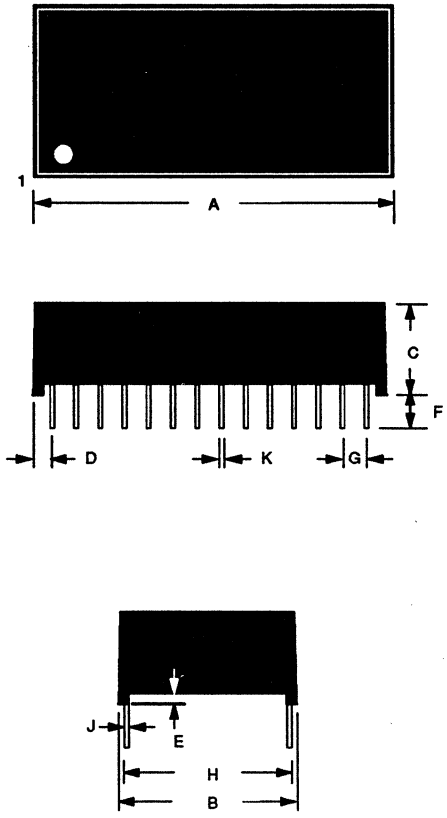
NOTES

1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package plus one year. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225, would mean the 25th week of 1992.

OUTPUT LOAD



DS1643 28 PIN PACKAGE



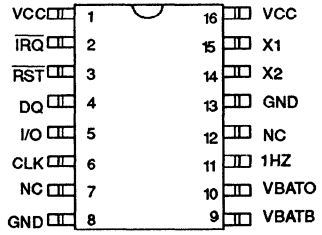
PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.315	0.335
MM	8.00	8.51
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.43	0.58

DALLAS SEMICONDUCTOR

DS2404
EconoRAM Time Chip

FEATURES
- Unique 1-wire interface requires only one port pin for communication
- Contains real-time clock/calendar in binary format
- 4096 bits of SRAM organized in 16 pages, 256 bits per page
- Interval timer can automatically accumulate time when power is applied
- Programmable cycle counter can accumulate the number of system power-on/off cycles
- Programmable alarms can be set to generate interrupts for interval timer, real-time clock, and/or cycle counter
- Write protect feature provides tamper-proof time data
- Programmable expiration date that will limit access to SRAM and timekeeping
- Data integrity assured with strict read/write protocols
- 3-wire I/O available for high speed data communications
- Unique 64-bit factory lasered ROM available
- Space-saving 16-pin SOIC package
- Operating temperature range from -20° C to +85° C
- Operating voltage range from 2.8 to 5.5 Volts

PIN ASSIGNMENT



16 PIN SOIC (300 Mil)

PIN DESCRIPTION

Pin #	Pin Name	Description
Pin 1&16	- V_{CC}	2.8 to 5.5 Volts
Pin 2	- $\overline{IRQ}$	Interrupt Output
Pin 3	- $\overline{RST}$	3-Wire Reset Input
Pin 4	- DQ	3-Wire Input/Output
Pin 5	- I/O	1-wire Input/Output
Pin 6	- CLK	3-Wire Clock Input
Pin 7 & 12	- NC	No Connection
Pin 8 & 13	- GND	Ground
Pin 9	- V_{BATB}	Battery Backup Input
Pin 10	- V_{BATO}	Battery Operate Input
Pin 11	- 1 Hz	1 Hz Output
Pin 14 & 15	- X_1,X_2	Crystal Connections

DESCRIPTION
The DS2404 EconoRAM Time Chip offers a simple solution for storing and retrieving vital data and time information with minimal hardware. The DS2404 contains a unique lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts and 4096 bits of SRAM. Two separate ports are provided for communication, 1-wire and 3-wire. Using the 1-wire port, only one pin is required for communication, and the lasered ROM can be read even when the DS2404 is without power. The 3-wire port provides high speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS2404 insures data integrity. Utilizing backup energy sources, the data is nonvolatile and allows for stand-alone operation.

The DS2404 features can be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, expiration timer, and event scheduler.

DETAILED PIN DESCRIPTION

Pin	Symbol	Description
Pin 1 & 16	V_{CC}	**Power input pins** for V_{CC} operate mode. 2.8 to 5.5 volts operation. Either pin can be used for V_{CC}. Only one is required for normal operation. (See V_{BATO} pin description and "Power Control" section).
Pin 2	$\overline{IRQ}$	**Interrupt output pin:** Open drain.
Pin 3	$\overline{RST}$	**Reset input pin** for 3-wire operation. (See "Parasite Power" section.)
Pin 4	DQ	**Data input/output pin** for 3-wire operation.
Pin 5	I/O	**Data input/output** for 1-wire operation: Open drain. (See "Parasite Power" section.)
Pin 6	CLK	**Clock input pin** for 3-wire operation.
Pin 7 & 12	NC	**No connection pins.**
Pin 8, 13	GND	**Ground pin:** Either pin can be used for ground.
Pin 9	V_{BATB}	**Battery backup input pin:** Battery voltage can be 2.8 to 5.5 volts. (See V_{BATO} pin description and "Power Control" section.)
Pin 10	V_{BATO}	**Battery operate input pin** for 2.8 to 5.5 volt operation. The V_{CC} & V_{BATB} pins must be grounded when this pin is used to power the chip. (See "Power Control" section.)
Pin 11	1Hz	**1 Hz square wave output:** Open drain.
Pin 14, 15	X_1, X_2	**Crystal pins.** Connections for a standard 32.768 kHz quartz crystal, Daiwa part number DT-26S (be sure to request 6 pF load capacitance). Crystals may be ordered directly from Dallas Semiconductor. Part number is DS9032. **NOTE:** X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area.

OVERVIEW

The DS2404 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

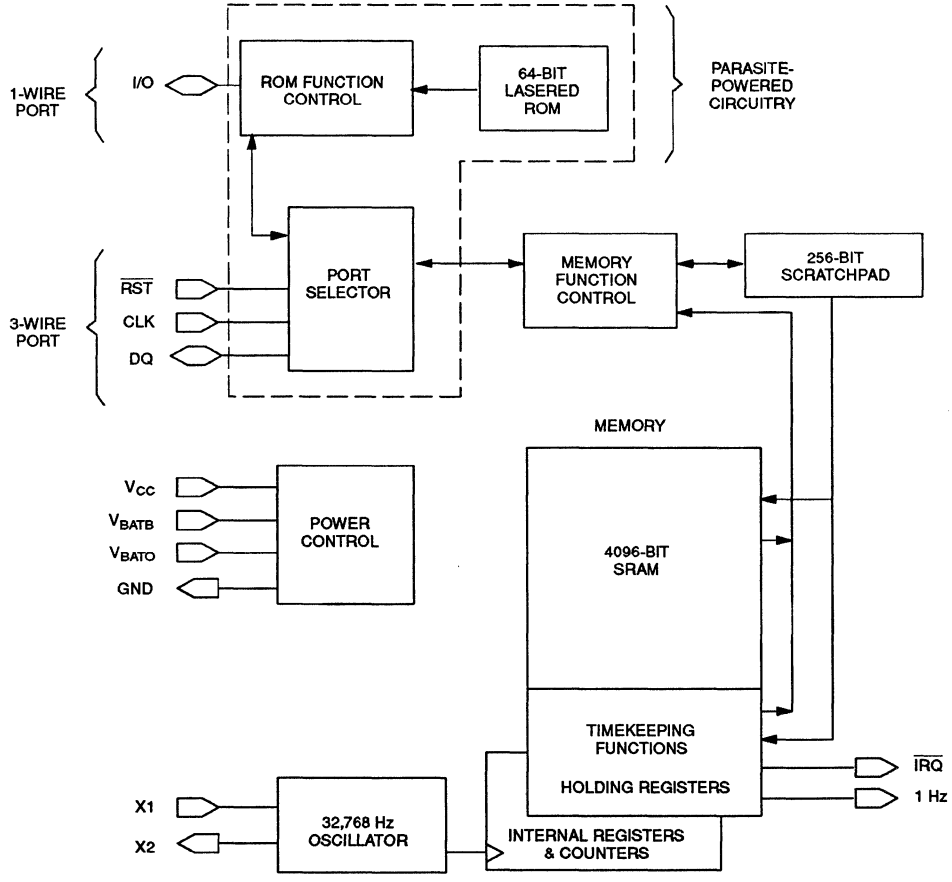
Two communication ports are provided, a 1-wire port and a 3-wire port. A port selector determines which of the two ports is being used. The communication ports and the ROM are parasite-powered via I/O, $\overline{RST}$, or V_{CC}. This allows the ROM to be read in the absence of power. The ROM data is accessible only through the 1-wire port. The scratchpad and memory are accessible via either port.

If the 3-wire port is used, the master provides one of four memory function commands: 1) read memory, 2) read scratchpad, 3) write scratchpad, or 4) copy scratchpad. The only way to write memory is to first write the scratchpad and then copy the scratchpad data to memory. (See Figure 6.)

If the 1-wire port is used, the memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands.

The "Power Control" section provides for two basic power configurations, battery operate mode and V_{CC} operate mode. The battery operate mode utilizes one supply connected to V_{BATO}. The V_{CC} operate mode may utilize two supplies; the primary supply connects to V_{CC} and a backup supply connects to V_{BATB}.

DS2404 BLOCK DIAGRAM Figure 1



COMMUNICATION PORTS

Two communication ports are provided, a 1–wire and a 3–wire port. The advantages of using the 1–wire port are as follows: 1) provides access to the 64–bit lasered ROM, 2) consists of a single communication signal (I/O), and 3) multiple devices may be connected to the 1–wire bus. The 1–wire bus has a maximum data rate of 16.6K bits/second and requires one 5KΩ external pull-up.

The 3-wire port consists of three signals, $\overline{RST}$, CLK, and DQ. $\overline{RST}$ is an enable input, DQ is bidirectional serial data, and the CLK input is used to clock in or out the serial data. The advantages of using the 3-wire port are 1) high data transfer rate (2 MHz), 2) simple timing, and 3) no external pull-up required.

Port selection is accomplished on a first-come, first-serve basis. Whichever port comes out of reset first will obtain control. For the 3-wire port, this is done by bringing $\overline{RST}$ high. For the 1-wire port, this is done on the first falling edge of I/O after the reset and presence pulses. (See "1-Wire Signalling" section.)

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O, $\overline{RST}$, or V_{CC} pins are high. When using the 1–wire port in battery operate mode, $\overline{RST}$ and V_{CC} provide no power since they are low. However, I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off these pins, battery power is conserved and 2) the ROM may be read in absence of normal power. For instance, in battery-operate mode, if the battery fails, the ROM may still be read normally.

In battery-backed mode, if V_{CC} fails, the port switches in the battery but inhibits communication. In order to read the ROM, the parasite-powered circuitry must be allowed to power down. This may be done by insuring that I/O, $\overline{RST}$, and V_{CC} are all low for $\gg$1 s. The ROM may then be read normally over the 1-wire port.

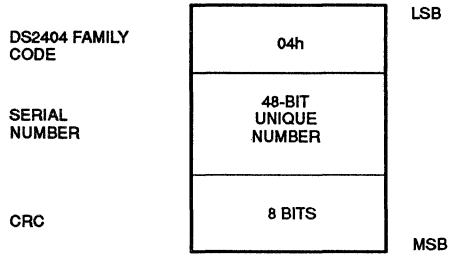
64-BIT LASERED ROM

Each DS2404 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code (DS2404 code is 04h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

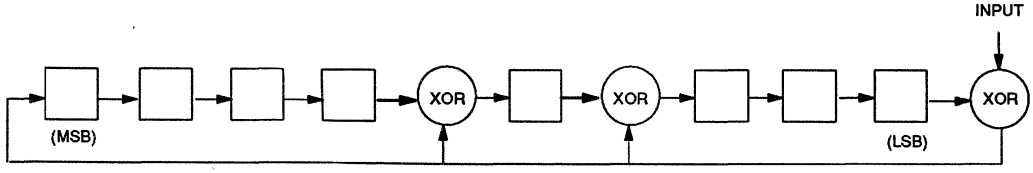
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

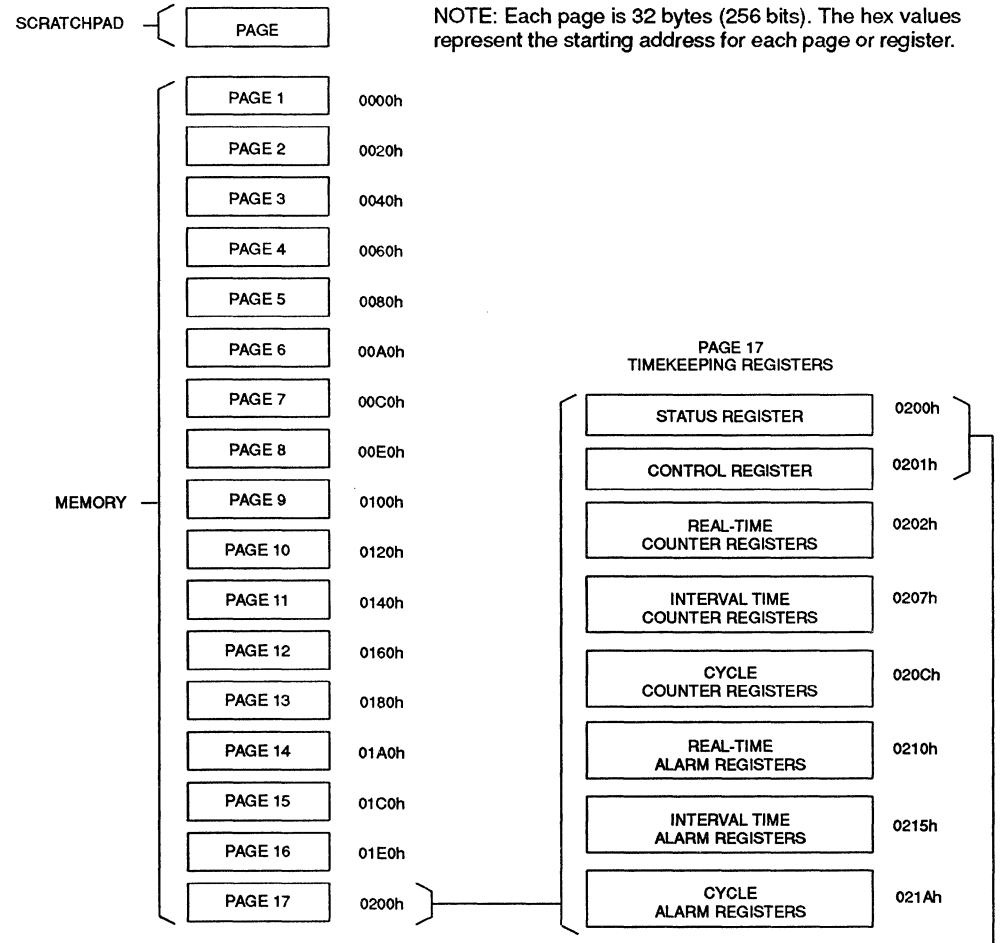
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



MEMORY MAP Figure 4



STATUS REGISTER

7	6	5	4	3	2	1	0	
X	X	$\overline{CCE}$	$\overline{ITE}$	$\overline{RTE}$	CCF	ITF	RTF	0200h

CONTROL REGISTER

7	6	5	4	3	2	1	0	
DSEL	$\frac{STOP}{START}$	$\frac{AUTO}{MAN}$	OSC	RO	WPC	WPI	WPR	0201h

MEMORY

The memory map in Figure 4 shows a page (32 bytes) called the scratchpad and 17 pages called memory. Pages 1 through 16 each contain 32 bytes which make up the 4096-bit SRAM. Page 17 has only 30 bytes which contain the timekeeping registers.

The scratchpad is an additional page of memory that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.

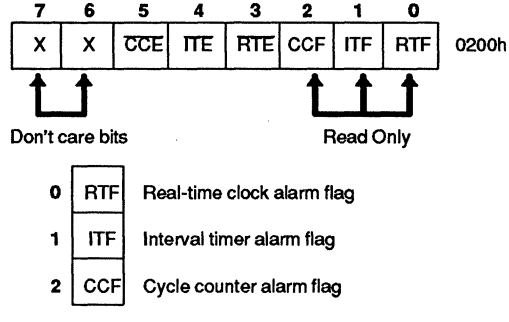
Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

STATUS/CONTROL REGISTERS

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register



When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	RTE	Real-time interrupt enable
4	ITE	Interval timer interrupt enable
5	$\overline{CCE}$	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register

7	6	5	4	3	2	1	0	
DSEL	STOP/$\overline{START}$	AUTO/$\overline{MAN.}$	OSC	RO	WPC	WPI	WPR	0201h

0	WPR	Write protect real-time clock/alarm registers
1	WPI	Write protect interval timer/alarm registers
2	WPC	Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3	RO	Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS2404 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4	OSC	Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5	AUTO/$\overline{MAN}$	Automatic/$\overline{Manual}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{START}$ bit.

6	STOP/$\overline{START}$	Stop/$\overline{Start}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7	DSEL	Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. Two examples follow the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

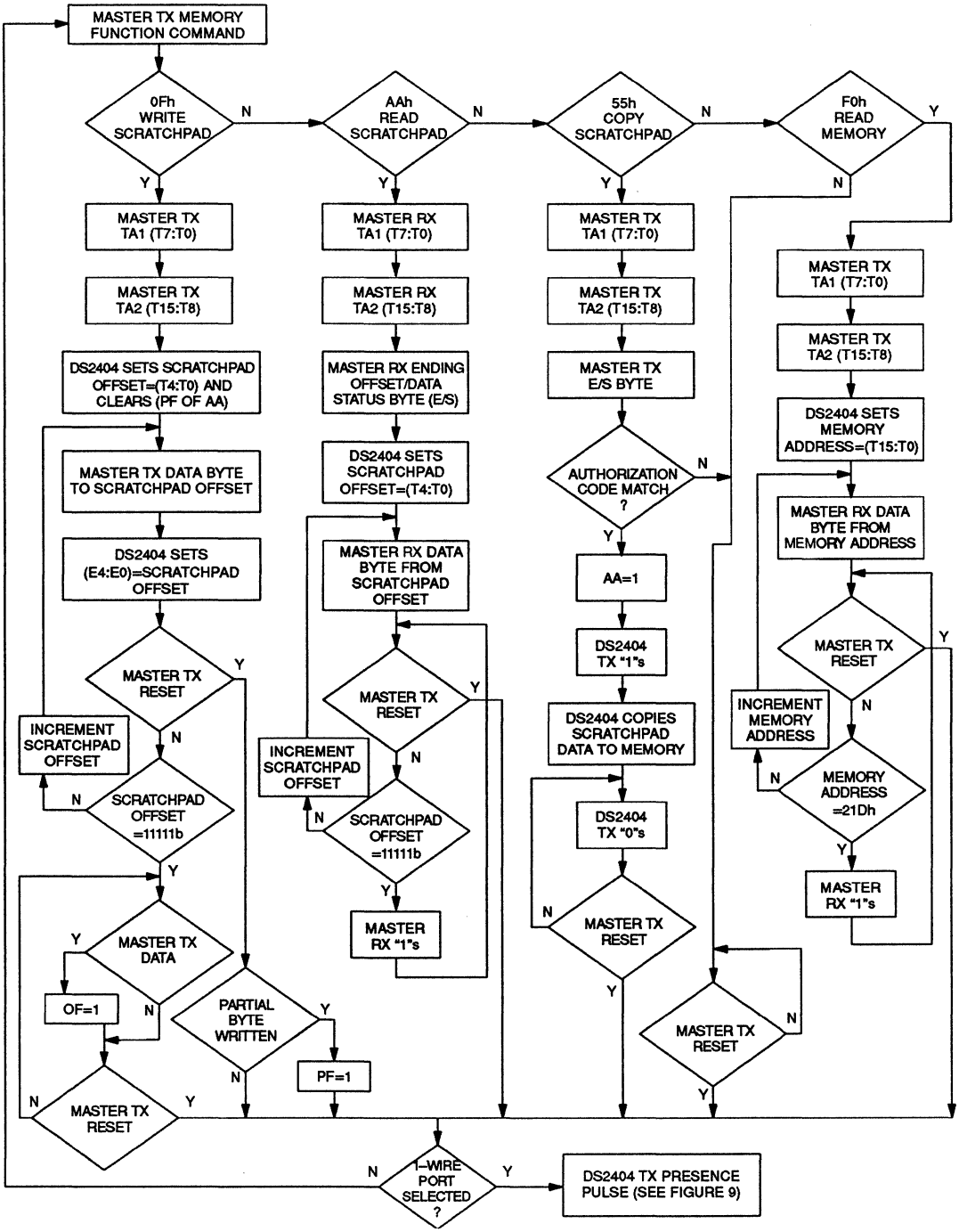
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. At this point, the part will go into a T_X mode, transmitting a logic 1 to indicate the copy is in progress. A logic 0 will be transmitted after the data has been copied. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of page 17. After the end of page 17, logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example 1: Write one page of data to page 16
Read page 16 (3-wire port)

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master pulses $\overline{RST}$ low
TX	0Fh	Issue "write scratchpad" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
TX	<32 data bytes>	Write 1 page of data to scratchpad
TX	Reset	Master pulses $\overline{RST}$ low
TX	AAh	Issue "read scratchpad" command
RX	E0h	Read TA1, beginning offset=0
RX	01h	Read TA2, address=01E0h
RX	1Fh	Read E/S, ending offset=31d, flags=0
RX	<32 data bytes>	Read scratchpad data and verify
TX	Reset	Master pulse $\overline{RST}$ low
TX	55h	Issue "copy scratchpad" command
TX	E0h	TA1 } AUTHORIZATION CODE
TX	01h	TA2 } AUTHORIZATION CODE
TX	1Fh	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until DQ=0 (~30 µs typical)
TX	Reset	Master pulse $\overline{RST}$ low
TX	F0h	Issue "read memory" command
TX	E0h	TA1, beginning offset=0
TX	01h	TA2, address=01E0h
RX	<32 data bytes>	Read memory page 16 and verify
TX	Reset	Master pulse $\overline{RST}$ low, done

Example 2: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory (1-wire port).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
RX	<busy indicator>	Wait until 0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<542 bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

WRITE PROTECT/PROGRAMMABLE EXPIRATION

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS2404 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protects their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".
** Forced to a logic "0".

1-WIRE BUS SYSTEM

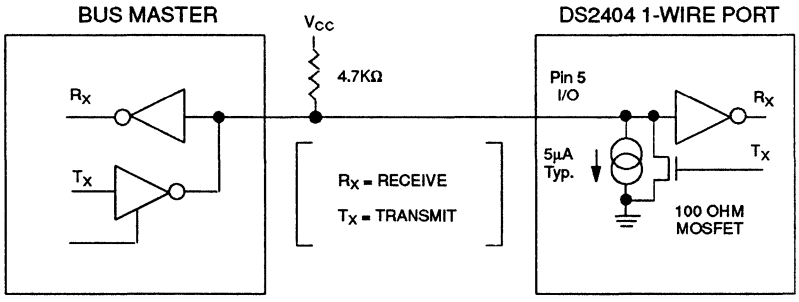
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS2404 behaves as a slave. The exception is when the DS2404 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3-state outputs. The 1-wire port of the DS2404 (I/O pin 5) is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-wire bus with multiple slaves attached. The 1-wire bus requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µS, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS2404 via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2404 is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS2404's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2404 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2404 on a multidrop bus. Only the DS2404 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-wire bus.

3. The bus master reads a bit from the 1-wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 0 onto the 1-wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1-wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-wire bus. ROM1 and ROM4 will place a 1 onto the 1-wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3-step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

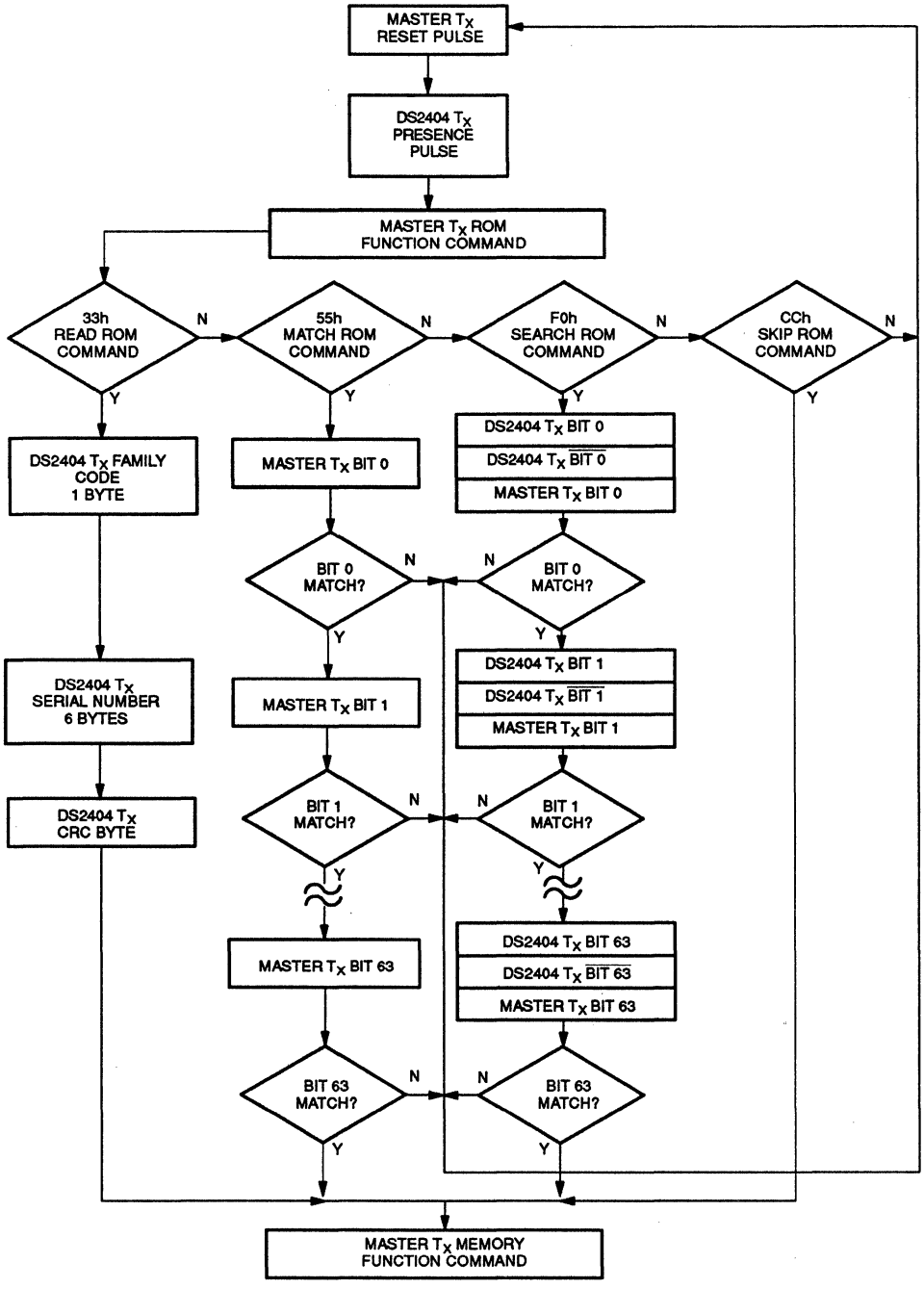
13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two zeros.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

ROM FUNCTIONS FLOW CHART (1-WIRE PORT ONLY) Figure 9



17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

I/O SIGNALLING

The DS2404 requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse. All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

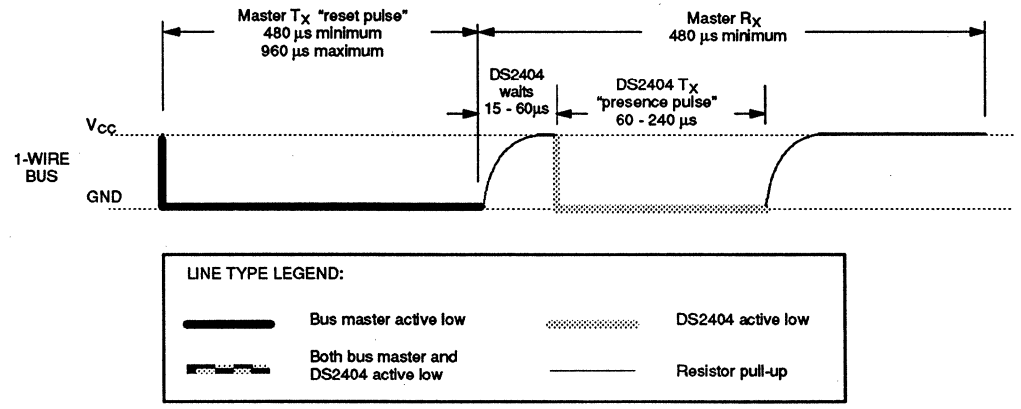
The initialization sequence required to begin any communication with the DS2404 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS2404 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS2404 waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

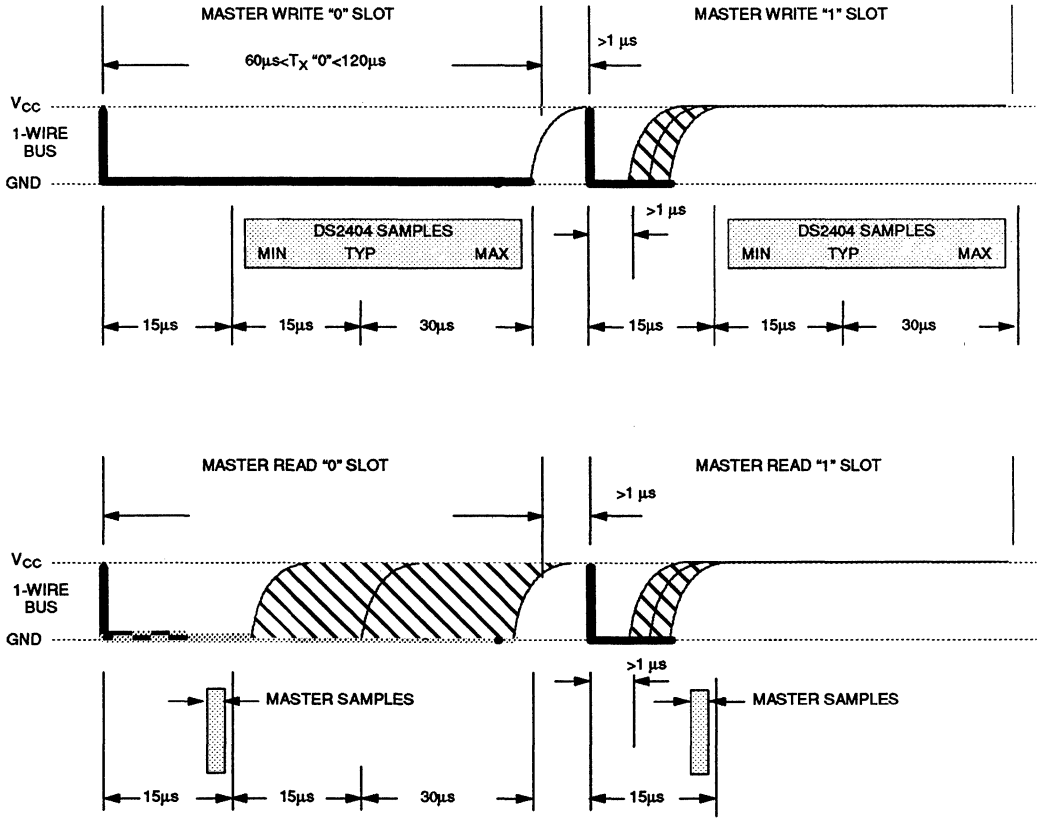
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS2404 to the master by triggering a delay circuit in the DS2404. During write time slots, the delay circuit determines when the DS2404 will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS2404 will hold the I/O line low.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



READ/WRITE TIMING DIAGRAM Figure 11



LINE TYPE LEGEND:

- Bus master active low
- DS2404 active low
- Both bus master and DS2404 active low
- Resistor pull-up

DETAILED MASTER READ "1" TIMING Figure 12

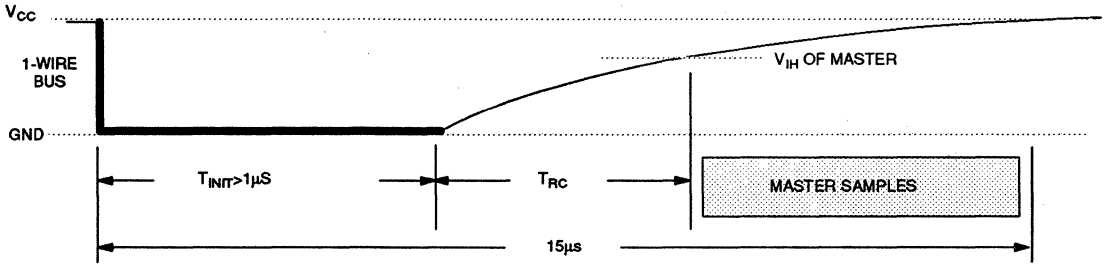
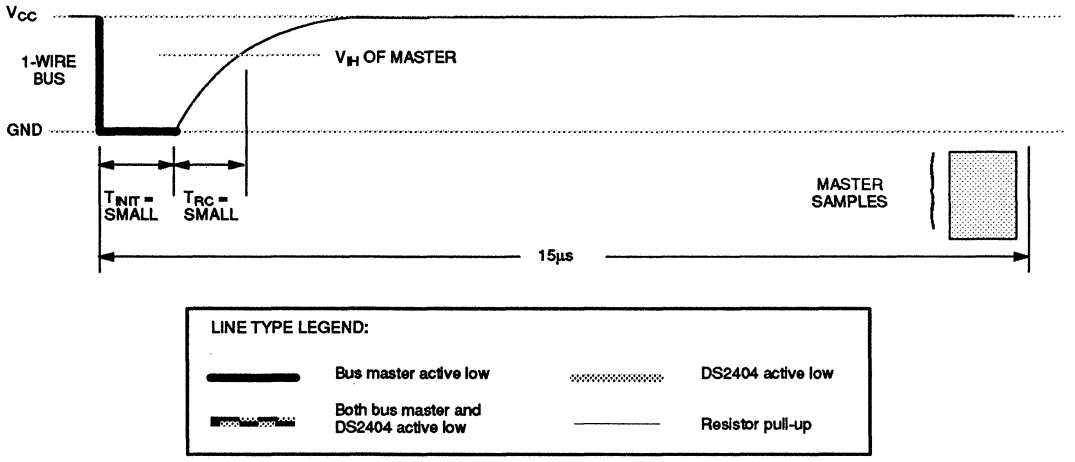


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 13



Interrupts

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled. An interrupt condition may be detected on either the $\overline{IRQ}$ pin or the I/O pin. During the interrupt condition, the open-drain $\overline{IRQ}$ pin is driven low and held low until the interrupt condition ceases.

On the 1-wire port, the part responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 14) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960 µs to 3840 µs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

A type 2 interrupt (Figure 17) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960 µs to 4800 µs. A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

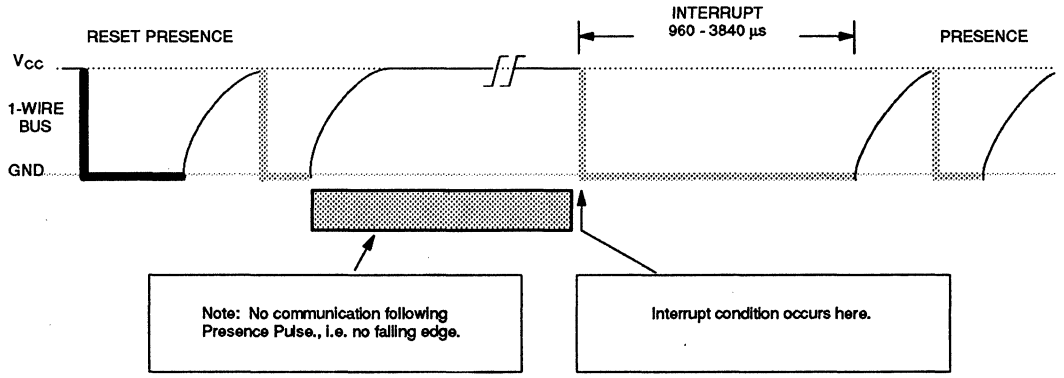
NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

Special cases exist as follows:

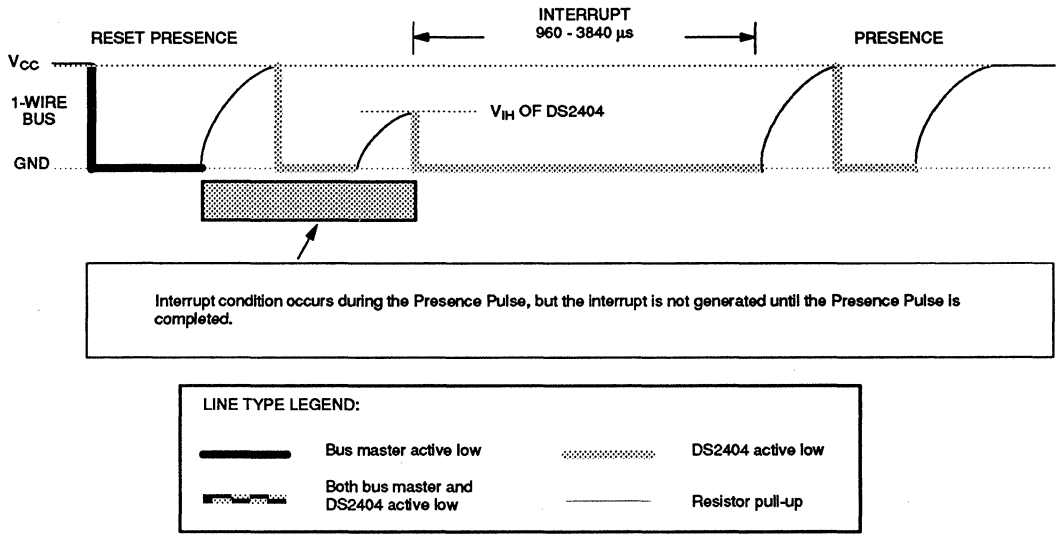
Special Case A (Figure 15): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

Special Case B (Figure 16): If an interrupt condition exists while the parasite-powered circuitry is powered down (i.e., I/O, $\overline{RST}$, and V_{CC} have been low for $\gg$1s), a type 1 interrupt will occur after the first presence pulse following I/O going high, just as in Special Case A.

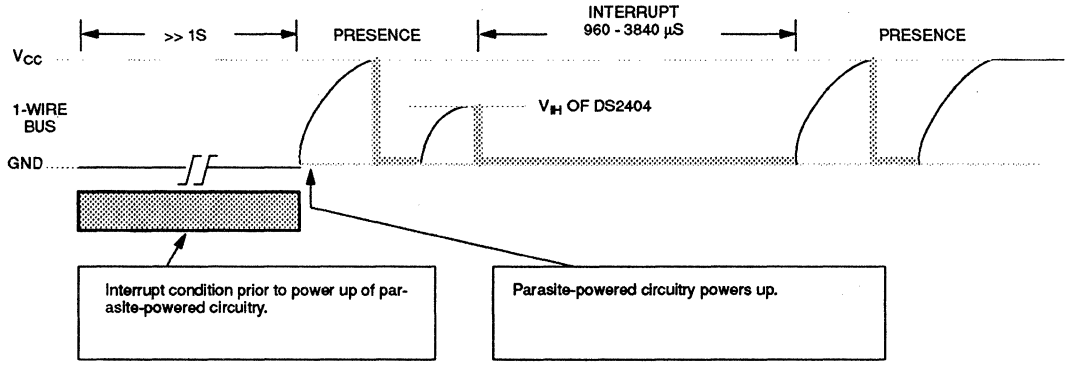
TYPE 1 INTERRUPT Figure 14



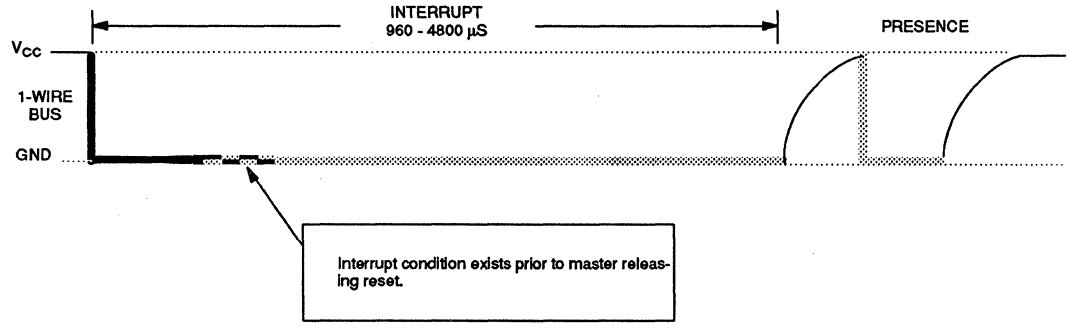
TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15

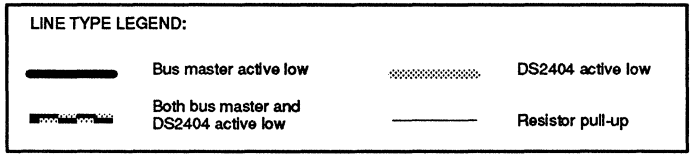


TYPE 1B INTERRUPT (SPECIAL CASE B) Figure 16



TYPE 2 INTERRUPT Figure 17





3-WIRE I/O COMMUNICATIONS

The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. Driving the $\overline{RST}$ input low terminates communication. (See Figures 24 and 25.)

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock.

When reading data from the DS2404, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

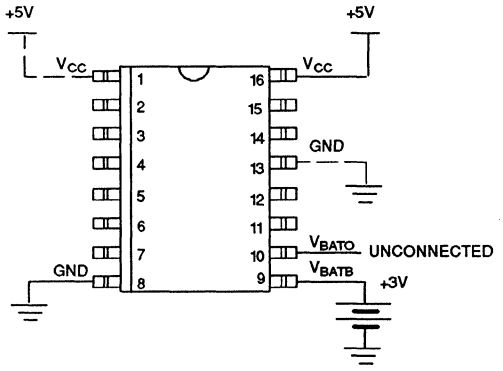
POWER CONTROL

There are two typical methods of supplying power to the DS2404, V_{CC} Operate mode and Battery Operate mode.

V_{CC} Operate Mode (Battery Backed)

Figure 18 shows the necessary connections for operating the DS2404 in V_{CC} Operate mode.

VCC OPERATE MODE Figure 18



V_{CC}	Pin 1 & 16	2.8 to 5.5 volts
V_{BATB}	Pin 9	2.8 to 5.5 volts*
V_{BATO}	Pin 10	must be unconnected

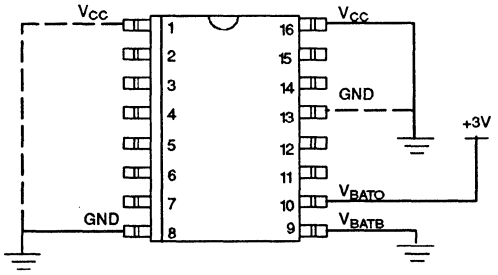
*While V_{BATB} may range from 2.8 to 5.5V, if the voltage on V_{BATB} ever exceeds the voltage on V_{CC}, the DS2404 will retain data, but will not allow access through the 1- or 3-wire port.

The V_{BATB} pin is normally connected to any standard 3-volt lithium cell or other energy source. As V_{CC} falls below V_{BATB}, the power switching circuit allows V_{BATB} to provide energy for maintaining clock functionality and data retention. No communication can take place while V_{BATB} is greater than V_{CC}. During power-up, when V_{CC} rises above V_{BATB} (~200 mV), the power switching circuit connects V_{CC} and disconnects V_{BATB}. If the oscillator is on, no communication can take place until V_{CC} has stayed (~200 mV) above V_{BATB} for 123 ± 2 ms.

Battery Operate Mode

Figure 19 shows the necessary connections for operating the DS2404 in Battery Operate mode.

BATTERY OPERATE MODE Figure 19



V_{CC}	Pin 1 & 16	Ground
V_{BATB}	Pin 9	Ground
V_{BATO}	Pin 10	2.8 to 5.5 volts

The V_{BATO} pin is normally connected to any standard 3-volt lithium cell or other energy source. Battery Operate mode provides low power consumption when used in conjunction with 1-wire interface.

Note: If the the 3-wire interface is used in Battery Operate mode, the voltage on DQ must never exceed the voltage on V_{BATO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-20°C to 85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-20°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 9
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{RST}$ Logic 1		2.8		5.5	V	1
Supply	V_{CC}	2.8		5.5	V	1
Battery	V_{BATB}, V_{BATO}	2.8	3.0	5.5	V	1, 6

DC ELECTRICAL CHARACTERISTICS

(-20°C to 85°C, V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			1	mA	
$\overline{RST}$ Resistance to Ground	Z_{RST}	40	65	90	KΩ	
D/Q Resistance to Ground	Z_{DQ}	40	65	90	KΩ	
CLK Resistance to Ground	Z_{CLK}	40	65	90	KΩ	
Active Current	I_{CC1}			2	mA	5
Standby Current	I_{CC2}			500	µA	
I/O Operate Charge	Q_{BATO}			200	nC	10
Batt Current (OSC On)	I_{BAT1}			350	nA	7
Batt Current (OSC Off)	I_{BAT2}			200	nA	7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	8

AC ELECTRICAL CHARACTERISTICS: 3-WIRE INTERFACE (-20°C to 85°C, V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

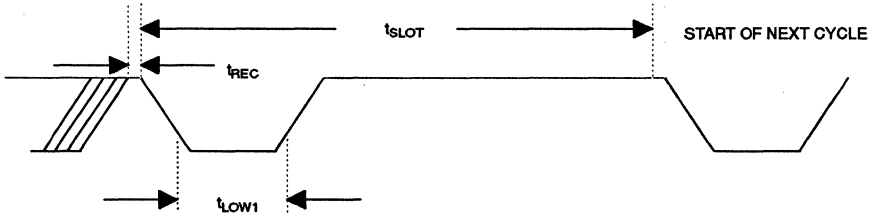
AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE (-20°C to 85°C, V_{CC}=2.8 to 5.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Interrupt	t_{INT}	960		4800	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

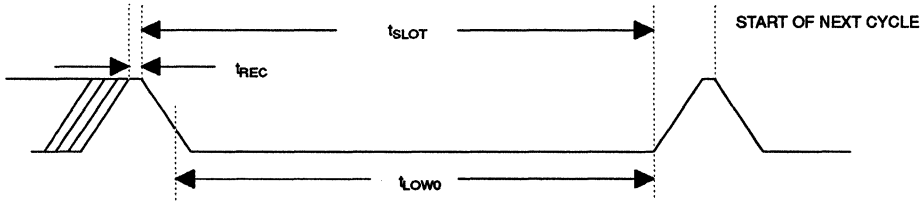
NOTES

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. When battery is applied to V_{BATO} input, V_{CC} and V_{BATB} must be 0V.
7. V_{BATB}, or V_{BATO} = 3.0V; all inputs inactive state.
8. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
9. For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or V_{BATO}.
10. Read or write scratchpad (all 32 bytes) at 3.0V.

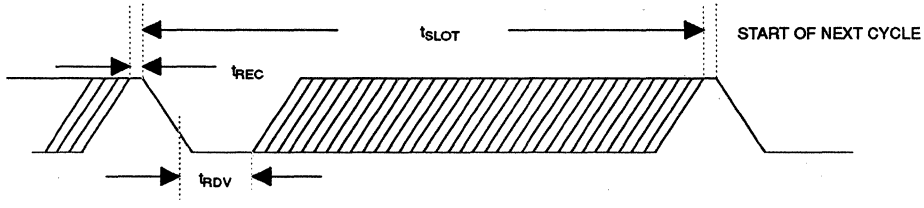
1-WIRE WRITE ONE TIME SLOT Figure 20



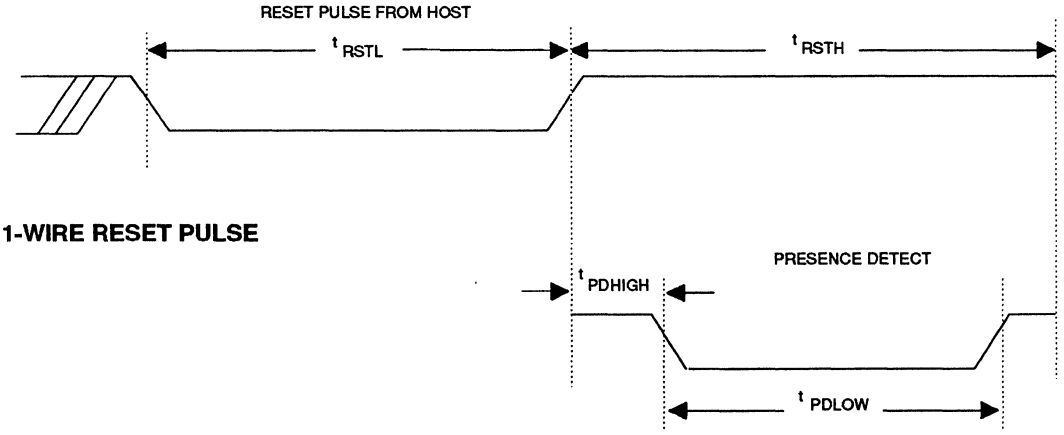
1-WIRE WRITE ZERO TIME SLOT Figure 21



1-WIRE READ ZERO TIME SLOTS Figure 22

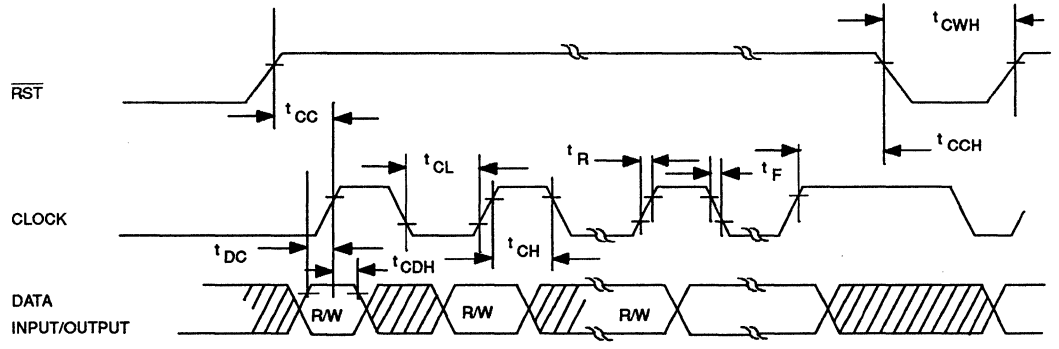


1-WIRE PRESENCE DETECT Figure 23

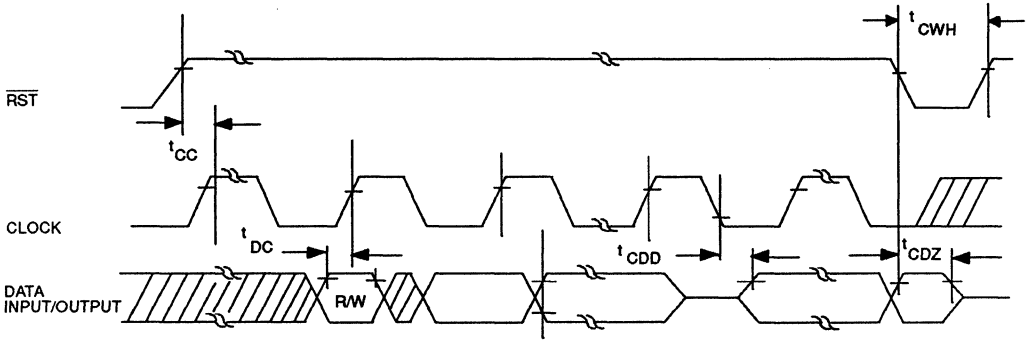


6

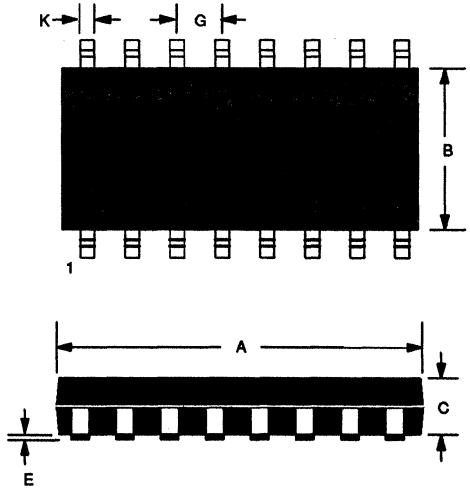
3-WIRE WRITE DATA TIMING DIAGRAM Figure 24

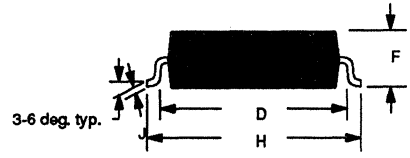


3-WIRE READ DATA TIMING DIAGRAM Figure 25



DS2404 ECONORAM TIME CHIP 16 PIN SOIC





PKG	16-PIN	
DIM	**MIN**	**MAX**
A IN. MM	.402	.412
B IN. MM	.292	.299
C IN. MM	.090	.100
D IN. MM	.320	.384
E IN. MM	.004	.012
F IN. MM	.097	.105
G IN. MM	.046	.054
H IN. MM	.398	.416
J IN. MM	.009	.013
K IN. MM	.013	.019

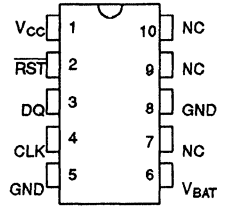
DALLAS SEMICONDUCTOR

DS1200
Serial RAM Chip

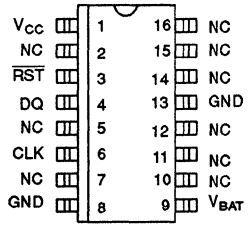
FEATURES

- 1024 bits of read/write memory
- Low data retention current for battery backup applications
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low-power CMOS circuitry
- Applications include:
  - software authorization
  - computer identification
  - system access control
  - secure personnel areas
  - calibration
  - automatic system setup
  - traveling work record

PIN ASSIGNMENT



10-Pin DIP (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 1



16-Pin SOIC (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

V_{CC}	- +5 Volts
$\overline{RST}$	- RESET
DQ	- Data Input/Output
CLK	- Clock
GND	- Ground
V_{BAT}	- Battery (+)
NC	- No Connection

DESCRIPTION

The DS1200 Serial RAM Chip is a miniature read/write memory which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RST}$, and DATA INPUT/OUTPUT.

Nonvolatility can be achieved by connecting a battery of 2 to 4 volts at the battery input V_{BAT}. A load of 0.5 µA should be used to size the external battery for the required data retention time. If nonvolatility is not required the V_{BAT} pin should be grounded.

For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than V_{BAT}, see the DS1201 Electronic Tag 1024-Bit data sheet.

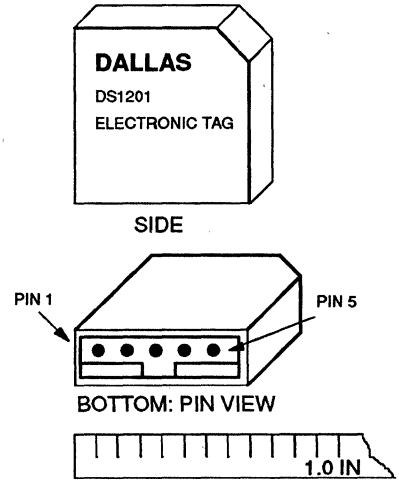
DALLAS SEMICONDUCTOR

DS1201
Electronic Tag

FEATURES

- User-insertable, nonvolatile 1024 bits of read/write memory
- Low-power CMOS circuitry allows for 10 years of data retention
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- Four million bits/second data rate
- Single-byte or multiple-byte data transfer capability
- No restrictions on the number of write cycles
- Applications include computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record.

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 12

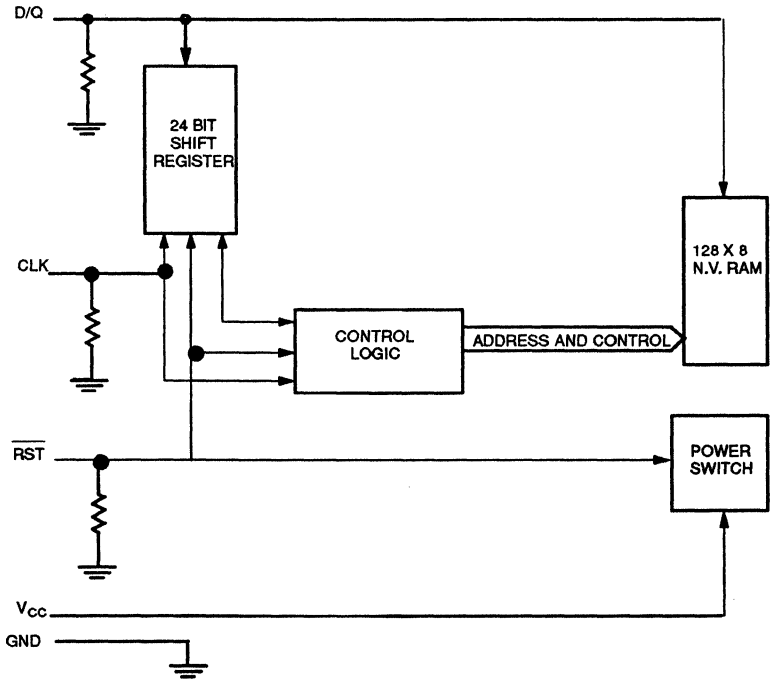
PIN DESCRIPTION

Pin 1	Vcc	+5 Volts
Pin 2	$\overline{RST}$	$\overline{RESET}$
Pin 3	DQ	Data Input/Output
Pin 4	CLK	Clock
Pin 5	GND	Ground

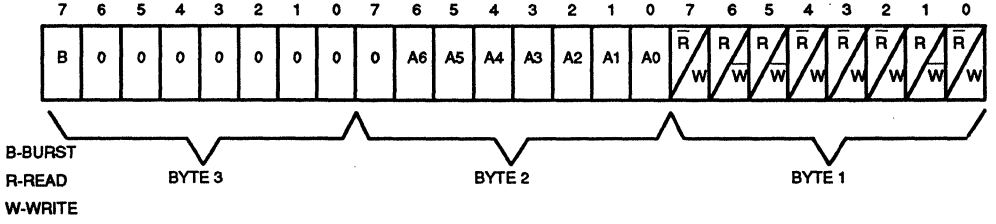
DESCRIPTION

The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

ELECTRONIC TAG BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND Figure 2



OPERATION

The block diagram (Figure 1) of the Electronic Tag illustrates the main elements of the device: shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{RESET}$ is taken high and 24 bits are loaded into the shift register, providing both address and command information. Each bit is input serially on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hardwired applications, active power is supplied by the Vcc pin. Alternatively, for user-insertable applications, power can be supplied by the $\overline{RESET}$ pin.

ADDRESS/COMMAND

Each memory transfer consists of a three-byte input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read . If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logic 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logic 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logic 0 or the cycle is aborted and all future inputs are ignored until $\overline{RESET}$ is brought low and then high again to begin a new cycle. Bit 7 of byte 3 of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logic 0 and bit 7 of byte 3 of the address command equals logic 1, the tag will enter the burst mode after the address/command sequence is complete.

BURST MODE

Burst mode is specified for the Electronic Tag when all address bits (A0-A6) of the address/command are set to logic 0 and bit 7 of byte 3 to logic 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{RESET}$ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RESET}$ input high. The $\overline{RESET}$ input serves three functions. First, $\overline{RESET}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RESET}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RESET}$ of 2 mA @ 3.8 volts is required. However if the Vcc pin is connected to a 5-volt source within nominal limits, then the $\overline{RESET}$ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 µA. Finally, the $\overline{RESET}$ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the $\overline{RESET}$ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using $\overline{RESET}$, the transition of $\overline{RESET}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next eight CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

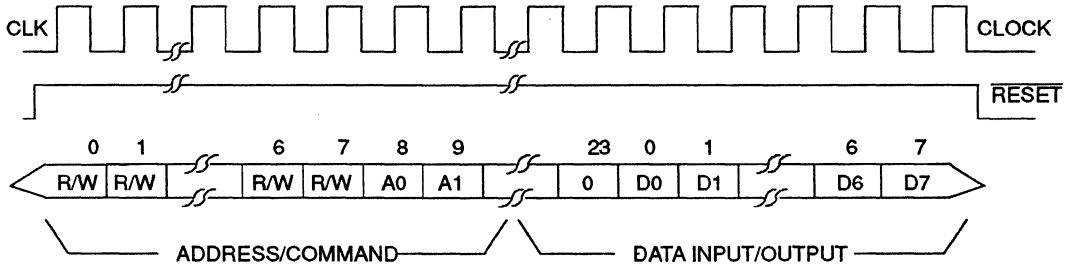
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

TAG CONNECTIONS

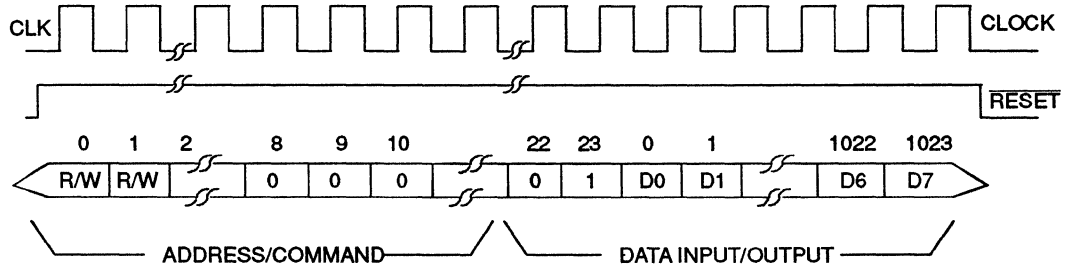
The tag is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to ensure connection integrity before data transfer begins. CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT all have internal 40K ohm pulldown resistors to ground which can be sensed by a reading device.

DATA TRANSFER Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



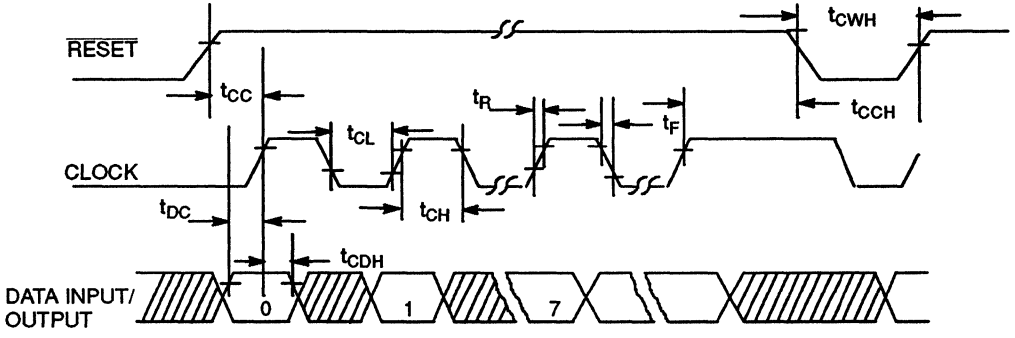
7

NOTES

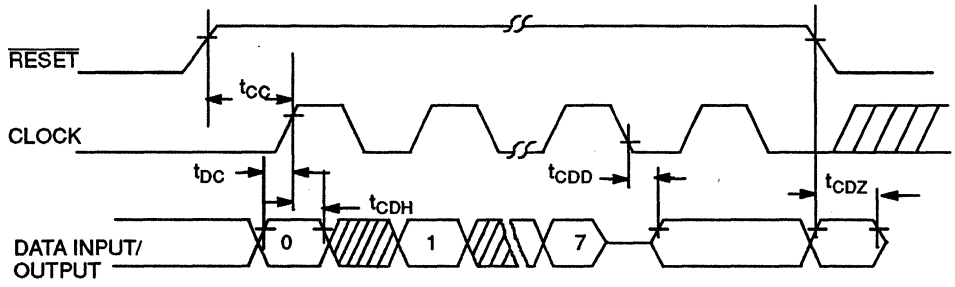
1. Data input sampled on rising edge of clock cycle.
2. Data output changes on falling edge of clock.

READ/WRITE DATA TRANSFER Figure 4

WRITE DATA TRANSFER



READ DATA TRANSFER



NOTES:

1. All voltages and resistances are referenced to ground.
2. Input levels apply to CLK, D/Q, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the tag, then $\overline{RST}$ input reverts to V_{IHE}.
3. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. For CLK, D/Q, $\overline{RST}$ and V_{CC} at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to $\overline{RST}$ when V_{CC} < 3.8 volts.
8. Measured with outputs open.
9. Measured at V_{IH} of $\overline{RST}$ greater than or equal to 3.8V when $\overline{RST}$ supplies power.
10. Logic 1 maximum is V_{CC} + 0.3V if the V_{CC} pin supplies power and $\overline{RST}$ +0.3V if the $\overline{RST}$ pin supplies power.
11. $\overline{RST}$ logic 1 maximum is V_{CC} + 0.3V if the V_{cc} pin supplies power and 5.5V maximum if $\overline{RST}$ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average AC $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})(CL + 140)f$
    I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} current of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 100 ms.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0 to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,2,10
Logic 0	V_{IL}	-0.3		0.8	V	1
$\overline{RESET}$ Logic 1	V_{IHE}	3.8			V	1,7,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_L			+500	µA	5
Output Leakage	I_{LO}			+500	µA	5
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{RST}$ Input Resistance	Z_{RST}	10		40	K ohms	1
D/Q Input Resistance	Z_{DQ}	10		40	K ohms	1
CLK Input Resistance	Z_{CLK}	10		40	K ohms	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			2.5	mA	8
$\overline{RST}$ Current	I_{RST}				mA	7,8,13

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	3,9
Data to CLK Hold	t_{CDH}	40			ns	3,9
Data to CLK Delay	t_{CDD}			125	ns	3,4,6,9
CLK Low Time	t_{CL}	125			ns	3,9
CLK High Time	t_{CH}	125			ns	3,9
CLK Frequency	f_{CLK}	DC		4.0	MHz	3,9
CLK Rise & Fall	t_R,t_F			500	ns	9
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	3,9
CLK to RST Hold	t_{CCH}	40			ns	3,9
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	3,9,14
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	3,9
Expected Data Retention Time	t_{DR}	10			Years	12

DALLAS SEMICONDUCTOR

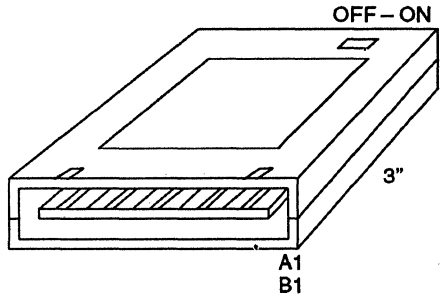
DS1217A
Nonvolatile Read/Write Cartridge

FEATURES

- User-insertable
- Capacity up to 32K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP socket via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

PIN ASSIGNMENT

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground



See Mech. Drawing – Sect. 16, Pg. 14

DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in densities ranging from 2K x 8 to 32K x 8 in 8K byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory contents. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory contents.

READ MODE

The DS1217A executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$); the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217A is in the write mode whenever both the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The last falling edge to occur of either $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217A constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. For this reason, the cartridge provides battery redundancy. The DS1217A features an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems that contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS
DS1217A/16K-25	2K x 8	*Address 11, 12, 13, 14
DS1217A/64K-25	8K x 8	*Address 13, 14
DS1217A/128K-25	16K x 8	*Address 14
DS1217A/192K-25	24K x 8	
DS1217A/256K-25	32K x 8	

*Unused address inputs must be held low (V_{IL}).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Connection Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

7

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Leakage Current	I_{IL}	-60		+60	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	µA	
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10	mA	
Operating Current	I_{CCO1}		35	75	mA	

CAPACITANCE (t_A = 25°C)

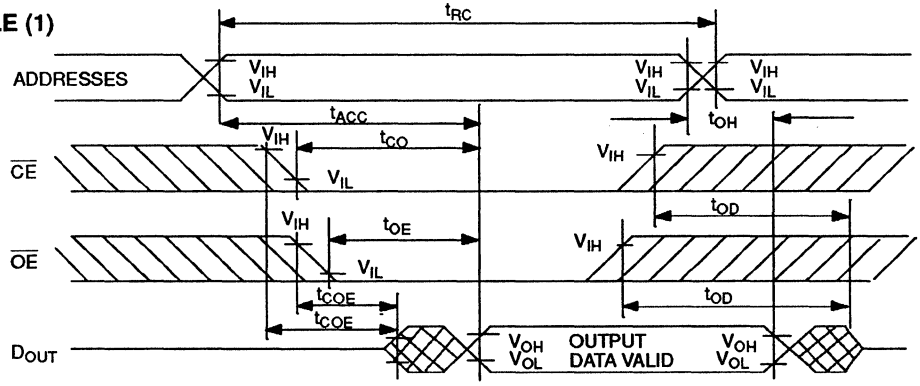
PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}			75	pF	
Input/Output Capacitance	$C_{I/O}$			75	pF	

AC ELECTRICAL CHARACTERISTICS

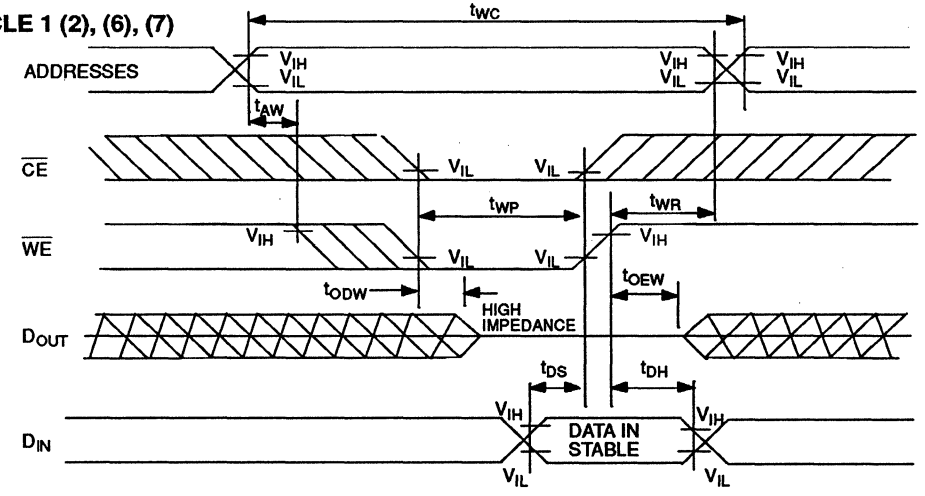
(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Output High Z from Deselection	t_{OD}			125	ns	5
Output Hold from Address Change	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z from $\overline{WE}$	t_{ODW}			100	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20			ns	4

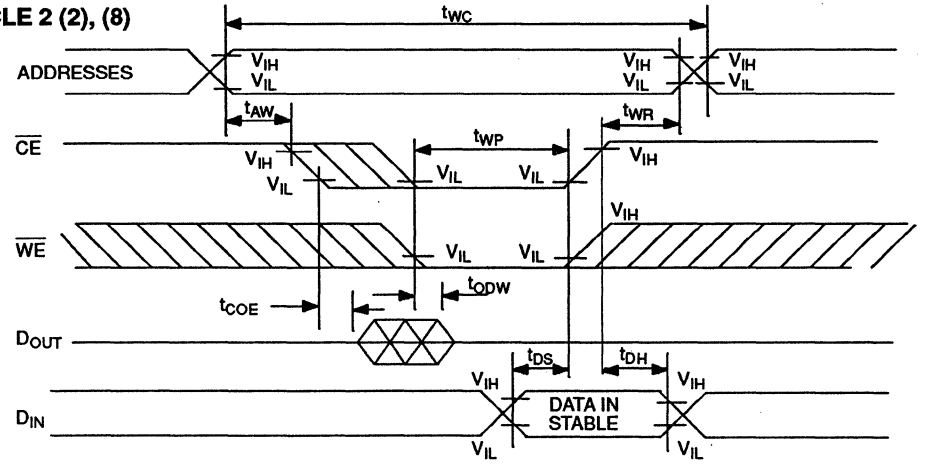
READ CYCLE (1)



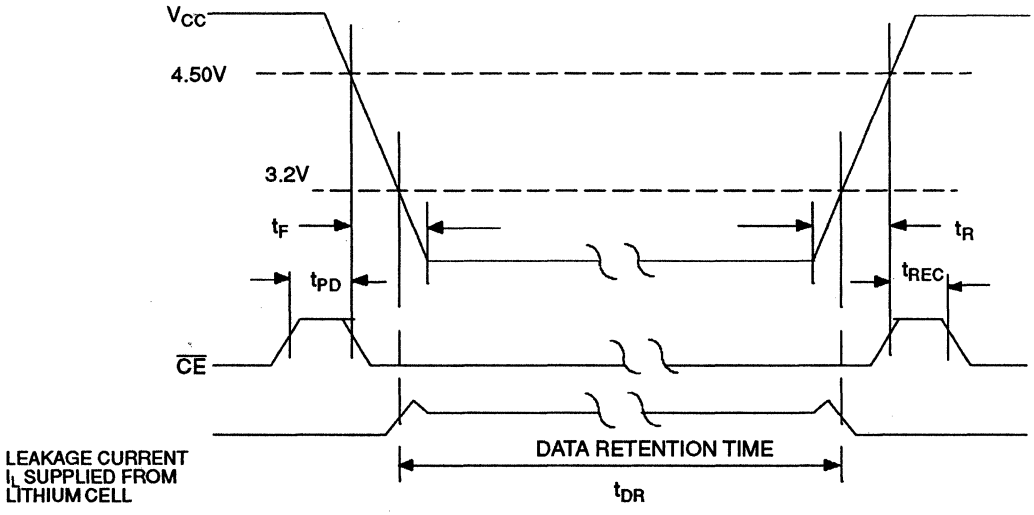
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(0°C to 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power-Down	0		µs	10
t_F	V_{CC} Slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		µs	
t_R	V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during the write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remains in a high impedance state during this period.
9. Each DS1217A is marked with a 4-digit date code AABB. AA designates the year of manufacture; BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

DC TEST CONDITIONS

Outputs Open
t Cycle = 250ns
All Voltages Are Referenced to Ground

7

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5 V

DALLAS SEMICONDUCTOR

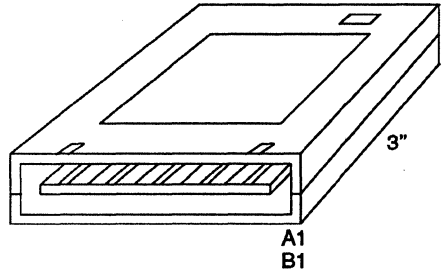
DS1217M
Nonvolatile Read/Write Cartridge

FEATURES

- User-insertable
- Data retention greater than 5 years
- Capacity up to 512K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP via ribbon cable
- Software-controlled banks maintain 32 x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0 – 70°C

PIN ASSIGNMENT

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground



See Mech. Drawing – Sect. 16, Pg. 14

DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The Nonvolatile Cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin bytewide memory sites.

READ MODE

The DS1217M executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the late occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The last occurring falling edge of either $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated.The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The Nonvolatile Cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern which will set the band switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles.The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch Chip data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	4
DS1217M 2-25	156K x 8	8
DS1217M 3-25	384K x 8	12
DS1217M 4-25	512K x 8	16

ADDRESS INPUT PATTERN Table 2

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1	1
A10	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

BANK SELECT TABLE Table 3

BANK	A8 BIT SEQUENCE				
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0

BANK	A8 BIT SEQUENCE				
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground	-0.3V to + 7.0V
Operation Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-60		+60	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	µA	
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		15	25	mA	
Operating Current	I_{CCO1}		50	100	mA	

DC TEST CONDITIONS

Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			100	pF	
Input/Output Capacitance	C_{OUT}			100	pF	

AC ELECTRICAL CHARACTERISTICS

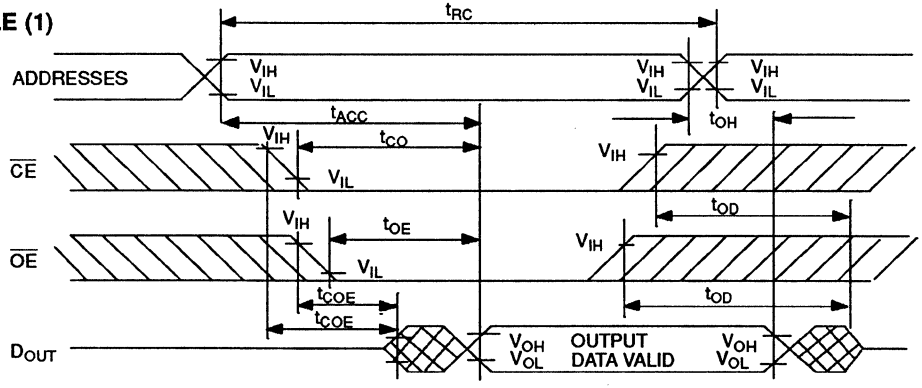
(0°C to 70°C, V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			210	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Output High Z From Deselection	t_{OD}			125	ns	5
Output Hold From Address Change	t_{OH}	5			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	5
Output Active From $\overline{WE}$	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	20			ns	4

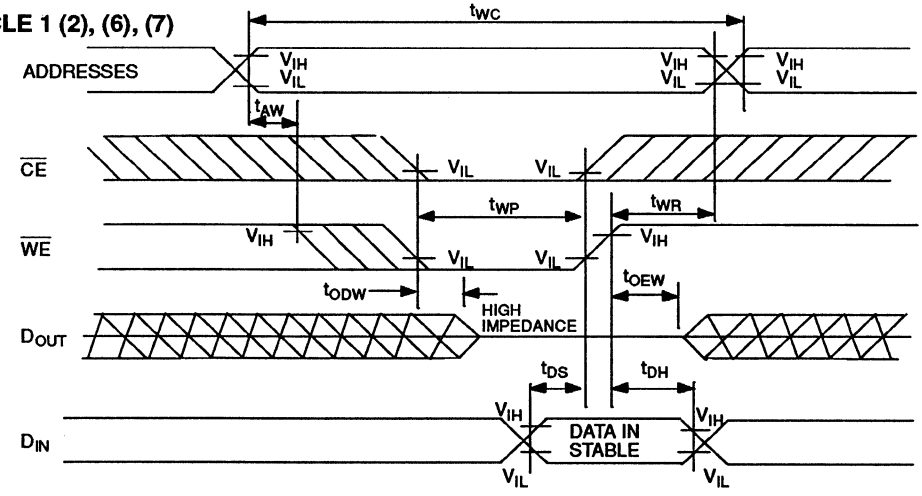
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

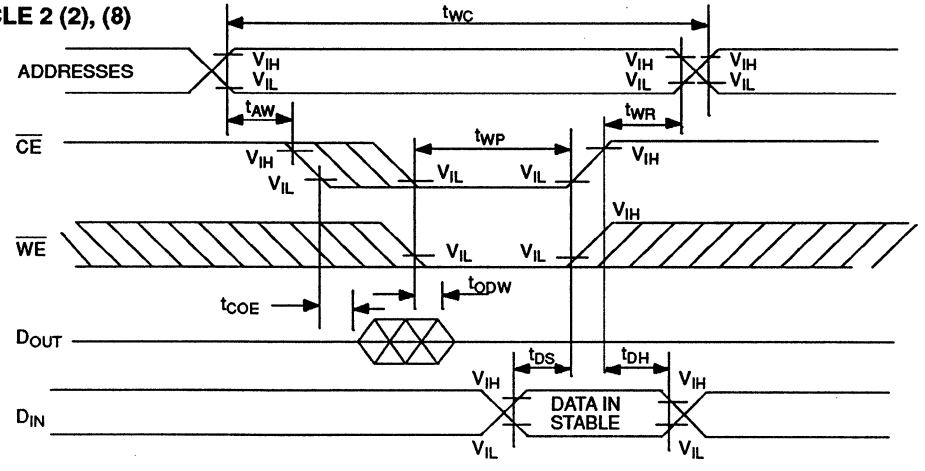
READ CYCLE (1)



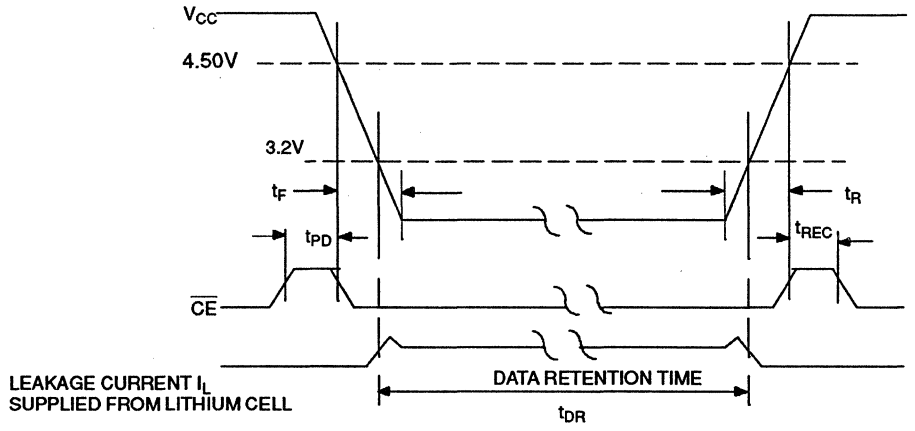
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(0° to 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at VIH before Power-Down	0			µs	10
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100			µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0			µs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2		125	ms	10

(t_A=25°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5			years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:
1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ of $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1217M is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

DALLAS SEMICONDUCTOR

DS1250 KeyRing

FEATURES

- Low-cost, add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 Kbps communication rate
- Up to five Keys and/or Tags resident at one time

PIN CONNECTIONS AND DEFINITIONS

Intermediary Bytewide Socket

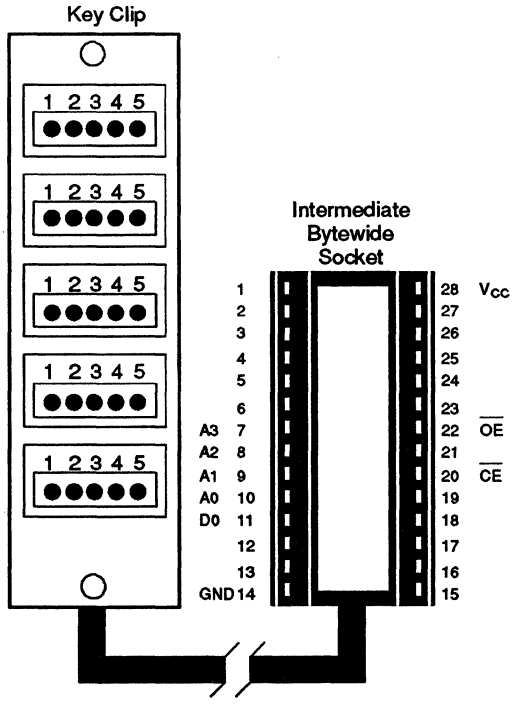
Pin 7 - 10	Address Inputs
Pin 11	D0
Pin 20	Conditioned Chip Enable ($\overline{CE}$)
Pin 22	Output Enable ($\overline{OE}$)
Pin 14	Ground
Pin 28	V_{CC}

* All pins pass through except 20

Key Clip

Pin 1	V_{CC} +5Volts
Pin 2	$\overline{RST}$ – $\overline{RESET}$
Pin 3	DQ – Data In/Out
Pin 4	CLK – Clock
Pin 5	GND – Ground

PIN ASSIGNMENT



DESCRIPTION

The DS1250 KeyRing adapts low pin-count Electronic Keys (DS1204U), TimeKeys (DS1207) or Electronic Tags (DS1201) to JEDEC bytewide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28-pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating five-conductor ribbon cable can be routed out of the system enclosure if desired and the clip can be attached where convenient with the adhesive provided. Up to five Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit that redirects information flow from the bytewide memory to the inserted keys/tags. A special software-generated address sequence causes the redirection to take place. Typical data transfer rates of 50 Kbps are possible with an assembly language software driver.

HARDWARE IMPLEMENTATION: 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board that contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM that is used for boot sequences, basic I/ O system implementation, EPROM storage, or some form of dedicated software monitor application.

To install the KeyRing, remove the existing 28-pin ROM and insert the bytewide KeyRing socket pins into the system board socket. After this is accomplished, reinsert the original ROM into the socket at the top of the KeyRing. Then route the five-conductor ribbon cable that connects the clip to the bytewide socket to the outside of the computer cabinet. Finally, attach the clip to a convenient place on the computer cabinet using the supplied adhesive.

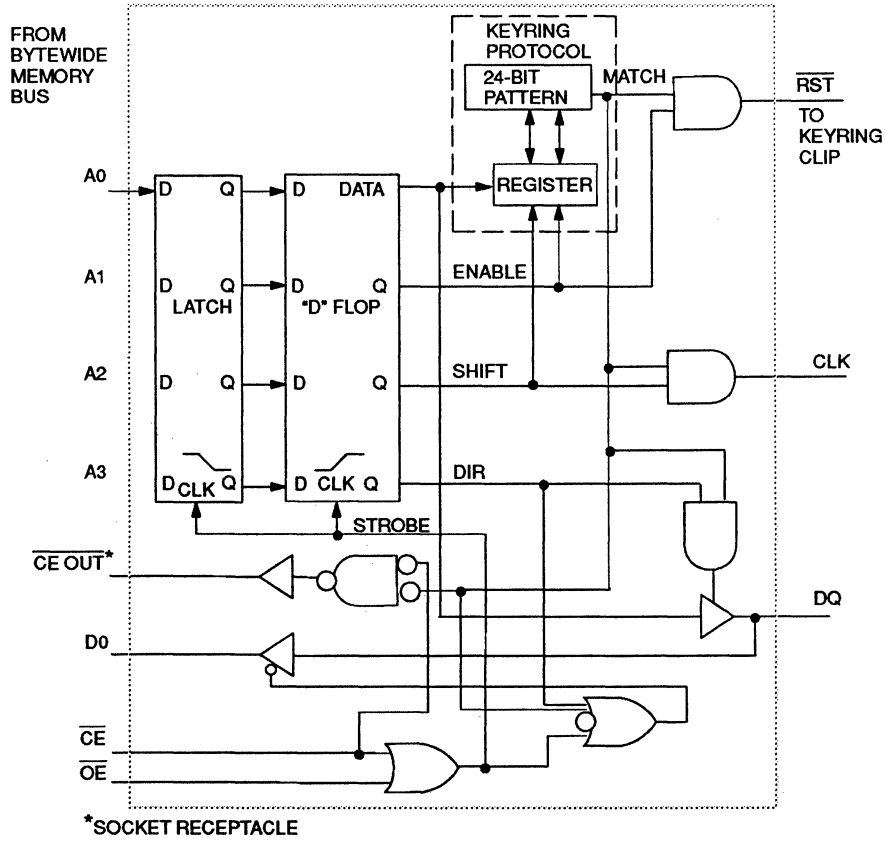
Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM bus becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) that is inserted into the KeyRing clip.

KEYRING OPERATION

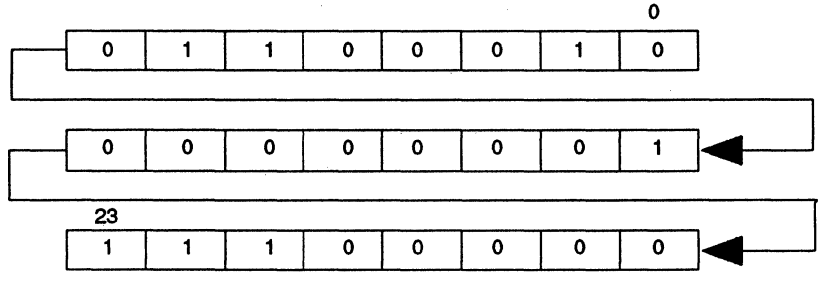
The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}$ In and $\overline{OE}$ In. The $\overline{CE}$ input is connected to the memory bus $\overline{CE}$ and the $\overline{OE}$ input is connected to the memory bus $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic that will generate signals for Keys and Tags. The KeyRing protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal that activates the communications sequence. A0 defines the data that is compared for recognition. A2 is used to clock in information defined by A0. Initially, the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

Data transfer through the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each rising edge of the strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal that causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate that allows Key DQ to drive the D0 line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized at the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

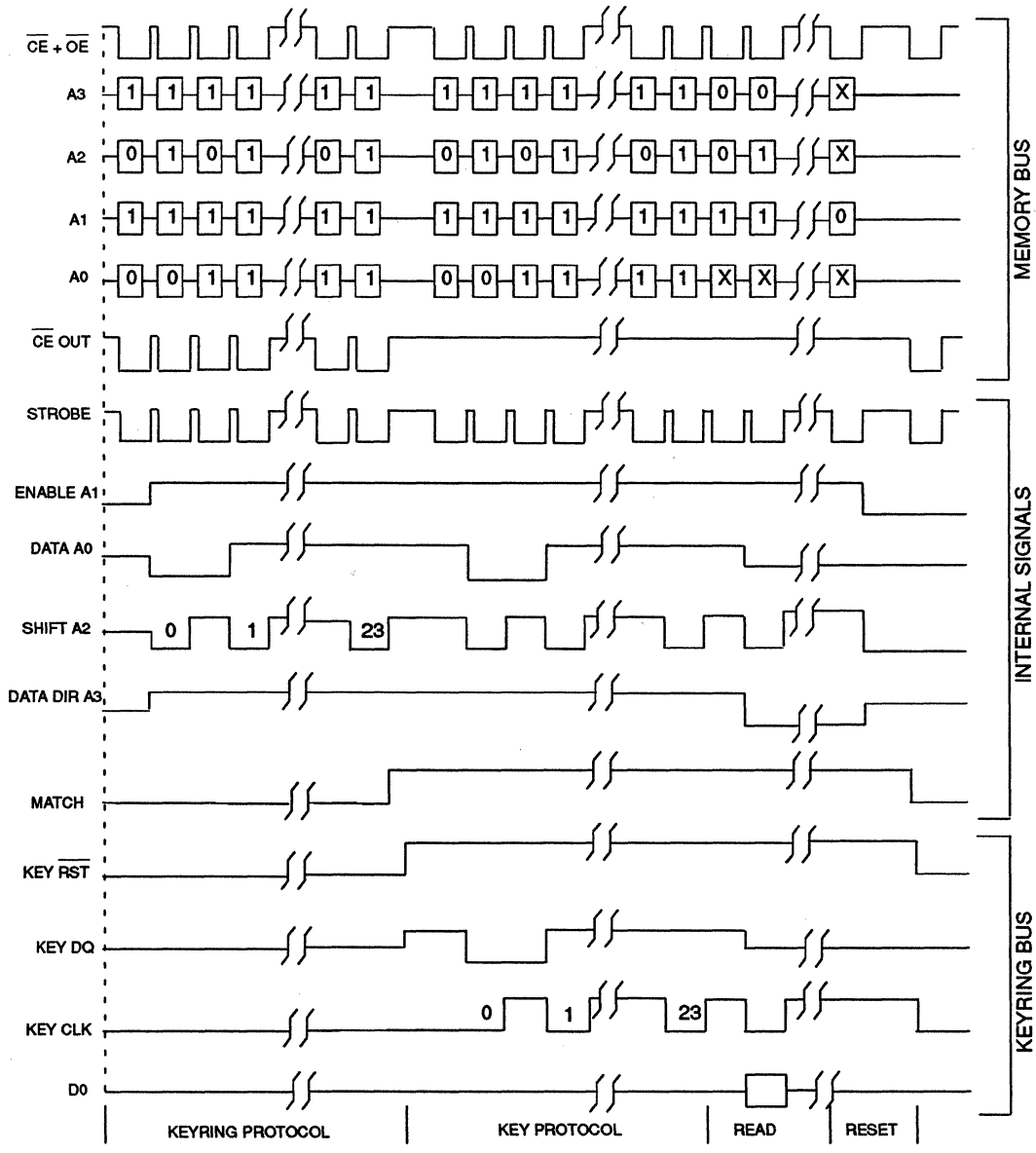
KEYRING BLOCK DIAGRAM Figure 1



KEYRING SIGNALS Figure 2



KEYRING SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

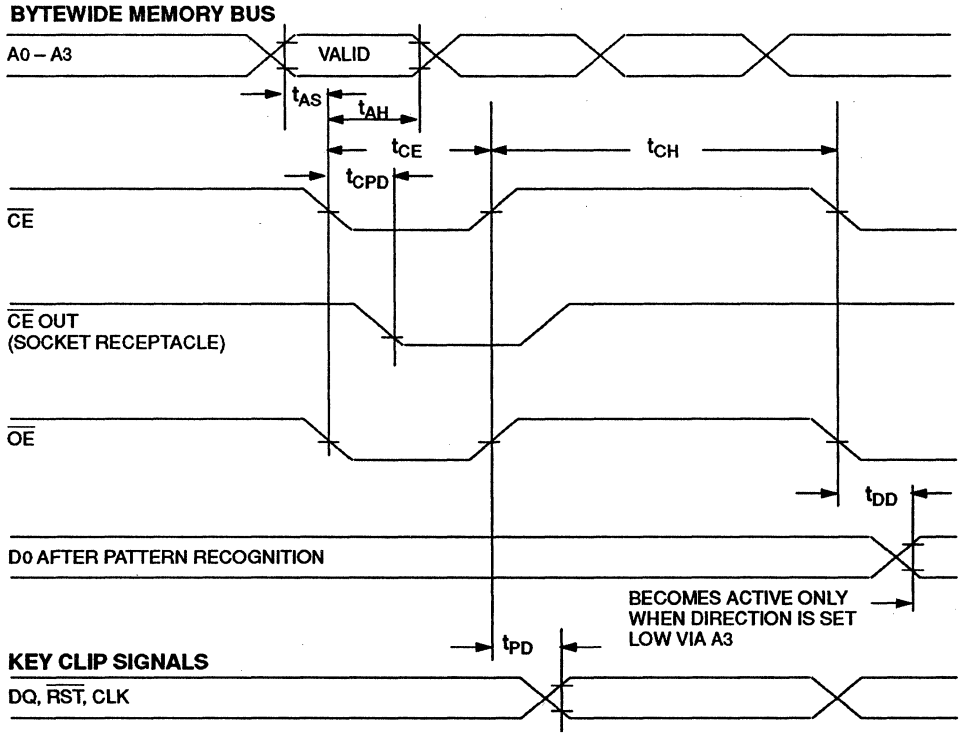
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

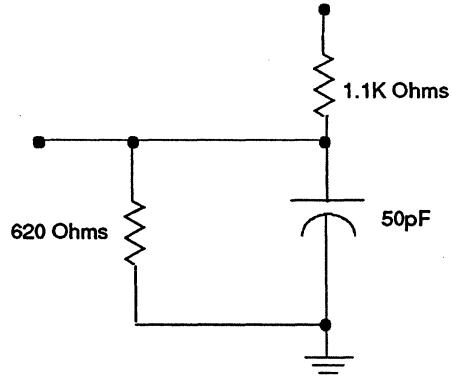
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	
$\overline{CE}$ Propagation Delay	t_{CPD}			10	ns	

BYTEWIDE MEMORY BUS



OUTPUT LOAD Figure 4



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

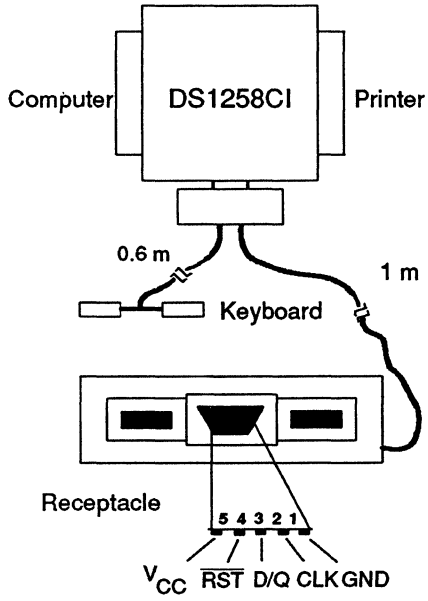
DALLAS SEMICONDUCTOR

DS1258K–001
CyberCard Portable Data Carrier Evaluation Kit

FEATURES

- Read or write any Cyber Portable Data Carriers with a PC host
- No slot required; connects to parallel printer port
- Normal computer to printer operation unaffected
- Compatible with all desktop PC's having a DIN-5 keyboard connector
- Comes with user-linkable drivers for systems integrators
- Example Intel 8051 (DS5000) Assembly Language program
- Includes:
  - DS1258CI Computer Interface
  - DS1258HI Single Slot User Interface
  - DS1258J Cyber Power Cable
  - Floppy Disk Labeled "Cyber EV Kit Disk 1"
  - Data Book
  - DS6417 – 256 Cyber Portable Data Carrier
  - DS6417 – CyberCard User's Guide

PIN ASSIGNMENT



DESCRIPTION

The DS1258K–001 Cyber Products EV Kit serves as a software reference guide for users who are designing with Dallas Semiconductor Cyber products. This cookbook package allows a user to easily interface Portable Data Carrier Cyber products with an IBM-compatible computer. A software diskette is included which contains a demonstration program written in Pascal. With this cookbook, applications software can be easily developed using higher level languages such as 'C', FORTRAN, etc. Additionally, included on the diskette is a source level listing of a program written in DS5000 Assembly Language for reading and writing the various Cyber products.

INSTRUCTIONS

Install the "Cyber Cookbook Diskette" in the default disk drive and type "CYBERCRD". This command will execute the CyberCard demonstration program. For installation instructions, refer to the CyberCard User's Guide.

PRELIMINARY

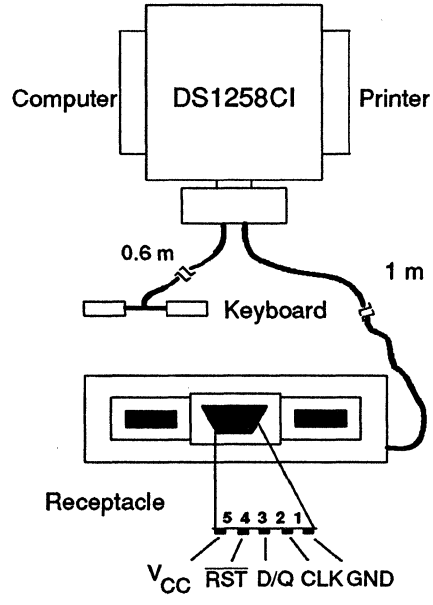
DALLAS SEMICONDUCTOR

DS1258K–002
CyberKey Carrier Evaluation Kit

FEATURES

- Read or write any CyberKey with a PC host
- No slot required; connects to parallel printer port
- Normal computer to printer operation unaffected
- Compatible with all desktop PC's having a DIN-5 keyboard connector
- Comes with user linkable drivers for systems integraters
- Example Intel 8051 (DS5000) Assembly Language program
- Includes:
  - DS1258CI Computer Interface
  - DS1258HI Single Slot User Interface
  - DS1258J Cyber Power Cable
  - Floppy Disk Labeled "CyberKey Kit Disk 1"
  - Data Book
  - DS6201 – 1K RAM CyberKey
  - DS6204 – Secure CyberKey
  - DS6205 – Multi CyberKey
  - DS6207 – Time CyberKey

PIN ASSIGNMENT



DESCRIPTION

The DS1258K–002 CyberKey EV Kit serves as a software reference guide for users who are designing with the Dallas Semiconductor Cyber products. This cookbook package allows a user to easily interface CyberKey products with an IBM compatible computer. A software diskette is included which contains a demonstration program written in Pascal. With this cookbook, applications software can be easily developed using higher level languages such as 'C', FORTRAN, etc. Additionally, included on the diskette is a source level listing of a program written in DS5000 Assembly Language for reading and writing the various Cyber products.

INSTRUCTIONS

Install the "Cyber Cookbook Diskette" in the default disk drive and type "RUN ME". This command will give instructions for printing document files which should be read carefully before proceeding.

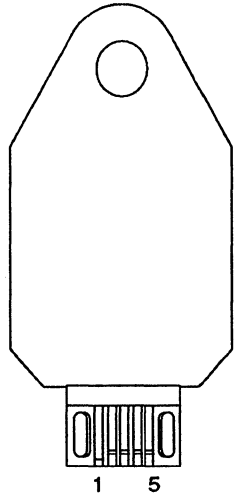
DALLAS SEMICONDUCTOR

DS620x CyberKey

FEATURES

- Greater than 50,000 cycle connector life
- Durable and rugged
- Ground pin makes first and breaks last
- 3-wire serial interface (DQ, CLK, and $\overline{RST}$) simplifies microprocessor interconnect
- Guided entry on mating connector overcomes orientation problems
- Greater than 10 years of data retention with no limitations or restrictions on write cycles
- Low-power CMOS circuitry
- Applications include software authorization, computer identification, system access control, calibration, data storage, automatic system setup, and travelling work record

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 13

PIN DESCRIPTION

1	Ground
2	Clock
3	Data
4	$\overline{RST}$
5	V_{CC}

DESCRIPTION

CyberKeys are miniature electronic memories with self-contained lithium energy sources. Depending upon the memory device internal to the CyberKey, secure, non-secure, time-related, and combinations of these functions are available. Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLK (clock), $\overline{RST}$ (reset), and DQ (data). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user. CyberKeys are designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years. Small, lightweight construction makes the devices suitable for carrying in a pocket or direct attachment to an object. Figure 1 lists the memory devices utilized in the different CyberKeys. For further information please see the referenced data sheets.

CYBERKEY DEVICES Figure 1

CYBERKEY	DESCRIPTION	RELATED DATA SHEET
DS6200	64-bit unique serial number with CRC Checking	DS2400
DS6201	1024 bits non-secure static RAM	DS1200
DS6204	128-bit secure static RAM: 64-bit password and 64-bit ID	DS1204
DS6205	3 secure 384-bit subkeys, 512-bit scratchpad	DS1205
DS6207	384-bit secure static RAM: Internal Time Key (1 to 512 days)	DS1207

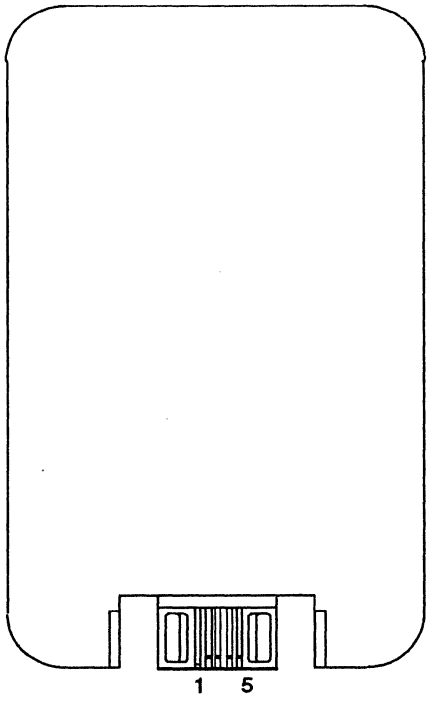
DALLAS SEMICONDUCTOR

DS6417
CyberCard EV 4M-Bit NV SRAM

FEATURES

- Greater than 50,000 insertion connector life
- Durable and rugged
- Ground pin makes first and breaks last
- User-insertable memory
- Capacities from 256K bits to 4M bits of nonvolatile memory
- Up to 1 million bits per second transfer rate
- Automatic write protection circuitry safeguards against data loss
- Cyclic redundancy check monitors serial data transmission for errors
- Compact size and shape
- Wide operating temperature range of -20°C to +70°C

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 13

PIN DESCRIPTION

Pin 1 Ground
Pin 2 Clock
Pin 3 Data
Pin 4 $\overline{RST}$
Pin 5 V_{CC}

DESCRIPTION

The DS6417 CyberCard EV is a nonvolatile serial access RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 256K bits to 4M bits. Data is transferred to and from the RAM through a standard 3-wire serial interface which is comprised of DQ, $\overline{RST}$, and CLK signals. The serial port requires a 7-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmissions for errors.

PIN DESCRIPTION OVERVIEW

$\overline{RST}$ – This pin controls all communication to the DS6417. When this signal is LOW, all communication to the serial port is inhibited. When high, data can be clocked into or out of the serial port.

CLK – This input signal is used to input or extract data from the serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven onto the 3-wire bus after a falling edge during a read cycle and latched into the port on the rising edge during a write cycle.

DQ – This signal is the bidirectional data signal for the 3-wire port.

OPERATION

The block diagram of Figure 1 illustrates the main elements of the DS6417. As shown, the DS6417 has two major sections: the static RAM array and the 3-wire to bytewide converter. The 3-wire to bytewide converter controls the static RAM through the use of the control/ address/data latches and multiplexer.

The 3-wire to bytewide converter uses a 56-bit protocol to determine the action to be taken and the starting address in RAM to be used. Data is entered while $\overline{RST}$ is high on the low to high transition of the CLK signal provided the data is stable on the DQ line for the proper set-up and hold times.

The last 8 bits of the 56-bit protocol contain the cyclic redundancy check byte that ensures all bits of the protocol have been transmitted correctly. If the 56 bits of protocol have not been received properly, the transaction will be aborted. The CRC check byte can catch up to three bit errors within the 56-bit protocol and can also be used on incoming and outgoing data streams to check the integrity of the data being read or written.

PROTOCOL

The 3-wire bus protocol can cause six different actions to be taken by the DS6417 (see Table 1).

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action to be taken involves a read or a write. A read function is defined by the binary pattern [11101000]. This pattern is applicable to commands 1,3,5, and 6 of Table 1. A write function is defined by the binary pattern [00010111]. This pattern is applicable to commands 2 and 4 of Table 1. Any other pattern which is entered into this read/write field will cause the transaction to be terminated. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of protocol referred to as the command field. The command field bits are shown as the binary values in Table 1.

BURST READ

A burst read uses a 19-bit address field which consists of the second byte, third byte, and the first three bits of the fourth byte of the protocol to determine the starting address of the information to be read from the RAM. The byte of data that has been accessed is transferred to the 3-wire bus a bit at a time, LSB first, by driving the DQ line on the falling edge of the next eight clocks.

BURST WRITE

A burst write uses the same 19 bit address field to determine the starting address of information to be written in RAM. Data is shifted from the DQ line into an eight bit shift register on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte by byte basis automatically incrementing the selected address by one location for each successive byte.

PROTOCOL COMMANDS Table 1

1) [00110 binary] burst read
2) [10001 binary] burst write
3) [00101 binary] read protocol select bits
4) [01110 binary] write protocol select bits
5) [11XXX binary] burst read masking portions of the protocol select bits
6) [00011 binary] read the CRC register

Termination of a current transaction will occur at any time the $\overline{RST}$ signal is taken low. If a byte of data has been loaded into the shift register a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when the $\overline{RST}$ signal goes low, no writing occurs. Reads can be terminated at any point since there is no potential for the corruption of RAM data.

READ CRC.

The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the 56-bit protocol. The 8-bit CRC value is valid for both the 56-bit protocol and also all data that is read or written from the RAM. After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in an internal register of the DS6417. If a read CRC register command is issued, the stored CRC value is driven onto the DQ signal line by the first eight clock cycles after the 56-bit protocol is received. The CRC value generated by the DS6417 should match the value generated by the host system which is transmitting or receiving data on the other end of the 3-wire bus.

It should be noted that the CRC for a previous transaction can only be obtained if a read CRC command is issued immediately after the $\overline{RST}$ signal goes low to reset the DS6417, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever the $\overline{RST}$ signal goes low again.

Three commands are used to set the select bits in the protocol. Once the select bits are set to a binary value, they must be matched when protocol is sent or further activity is prevented. The bits allow for up to 65,536 different binary combinations. Therefore, multiple DS6417s can be connected on the same 3-wire bus and only the selected device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field. To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have a large number of DS6417s in use and uniquely identify each one. A read can occur successfully without knowing the select bits, but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS6417 in the presence of many DS6417s. A read in the read/write field and a [11000 binary] in the command field will execute a mask read that ignores all select bits to determine the presence of any DS6417s. With the detection of at least one device, a search can begin by masking all but a single pair of DS6417 select bits. A read in the read/write field and a [11001 binary] in the command field will unmask the first two LSB's of byte 4 of the select bits (Figure 3). With these two select bits unmasked, only an exact match of four possible combinations (00, 01, 10, or 11) of these two select bits will now allow access through the 3-wire port to RAM. Therefore, repeating the unmasking of the two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of the four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will yield an exact match of the one DS6417 out of the possible 65,536 in no more than 32 attempts.

CRC GENERATION

The logic involved in the CRC generation is shown in Figure 4. Basically, the scheme is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQ IN to the CRC generator while each byte is being assembled and at the same time, output data to the output (DQOUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire bus.

The reset signal (RSB) must be high while the CRC generator is being used as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS6417 CRC requirements.

However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Microcontroller. The assembly language procedure DO_CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to cal-

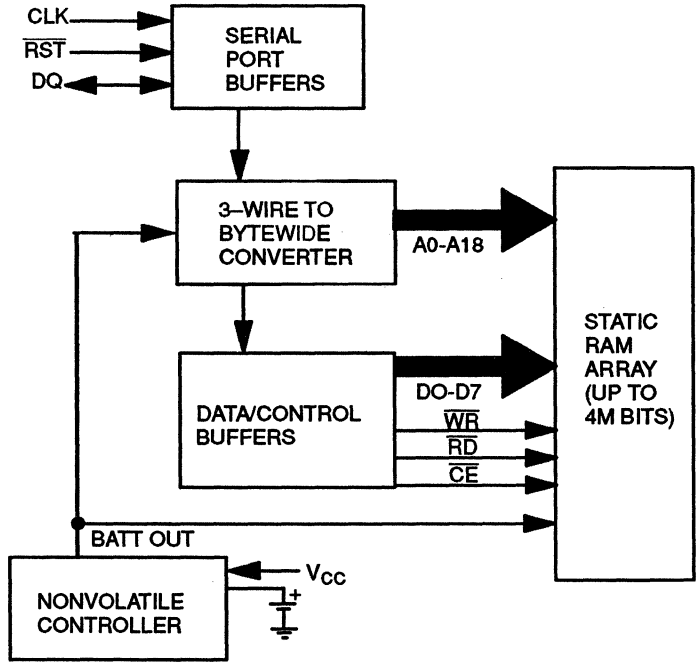
culate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO_CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

3-WIRE BUS

The 3-Wire bus is comprised of three signals. These are the $\overline{RST}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the $\overline{RST}$ is low and the DQ pin goes to a high impedance state. When data transfers to the DS6417 are terminated by the $\overline{RST}$ signal going low, the transition of the $\overline{RST}$ going low must occur during a high level of the CLK signal. Failure to insure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figures 5 and 6 for normal modes of operation.

BLOCK DIAGRAM Figure 1

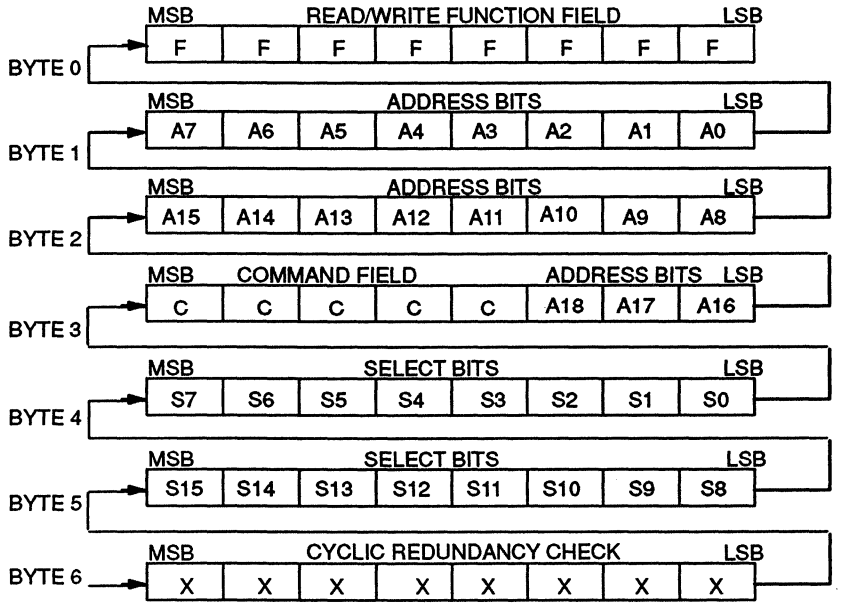


CRC CODE Table 2

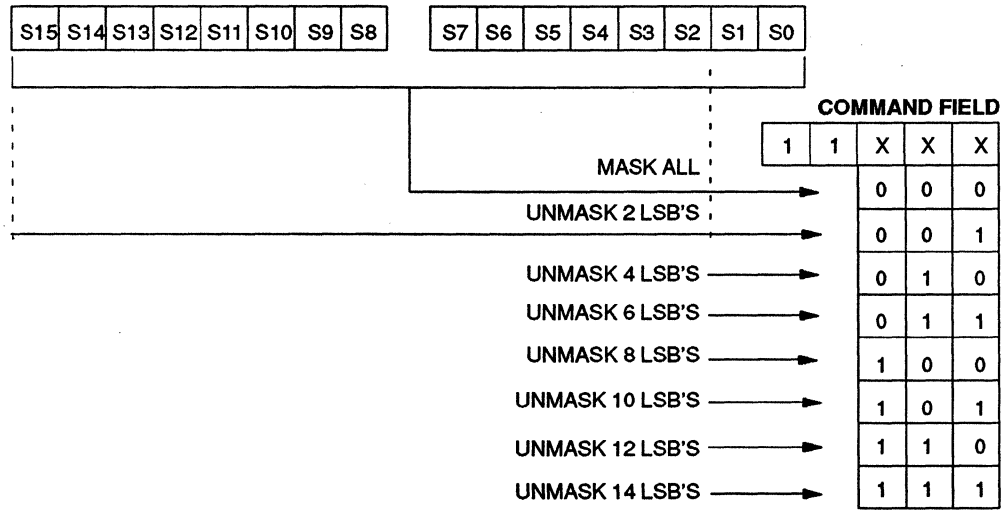
```
DO_CRC:
        PUSH    ACC                     ;Save the Accumulator
        PUSH    B                       ;Save the B register
        PUSH    ACC                     ;Save bits to be shifted
        MOV     B,      #8              ;Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC             ;Calculate DQIN xor CRCTO
        RRC     A                       ;Move it to the last
        MOV     A,      CRC             ;Get the last CRC value
        JNC     ZERO                    ;Skip if DQIN xor CRCTO=0
ZERO:   XRL     A,      0CCH            ;Update the CRC value
        RRC     A                       ;Position the new CRC
        MOV     CRC,    A               ;Store the new CRC
        POP     ACC                     ;Get the remaining bits
        RR      A                       ;Position next bit in LSB
        PUSH    ACC                     ;Save the remaining bits
        DJNZ    B,      CRC_LOOP        ;Repeat for eight bits
        POP     ACC                     ;Clean up the stack
        POP     B                       ;Restore the B register
        POP     ACC                     ;Restore the Accumulator
        RET                             ;Return
```

7

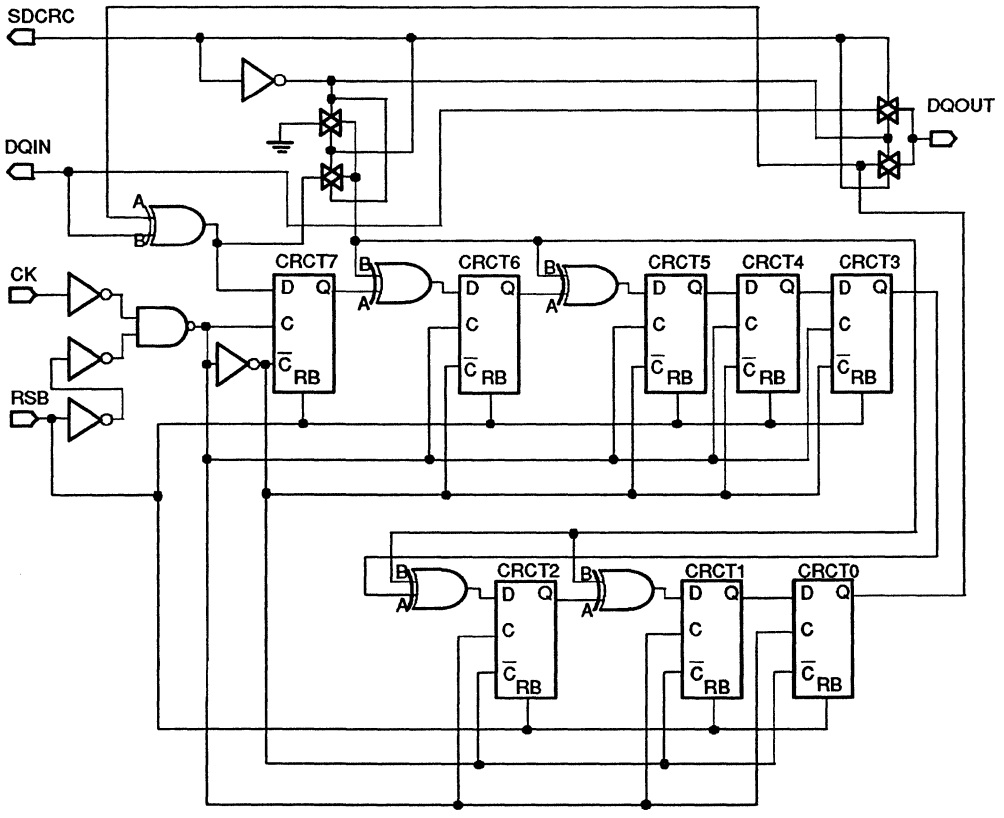
PROTOCOL Figure 2



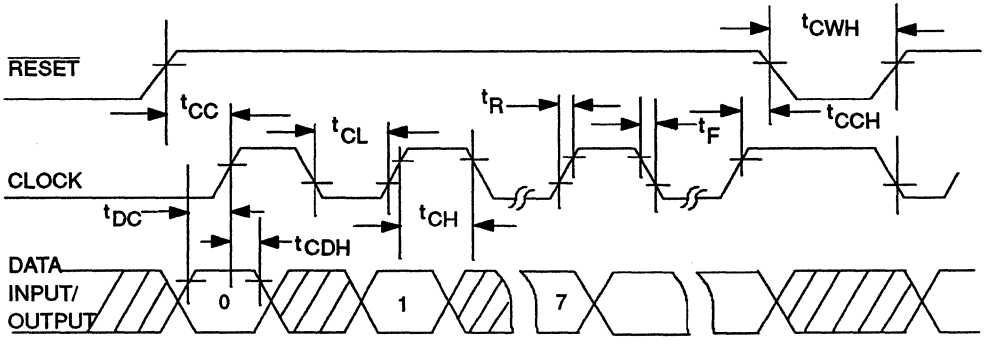
SELECT BITS MASK Figure 3



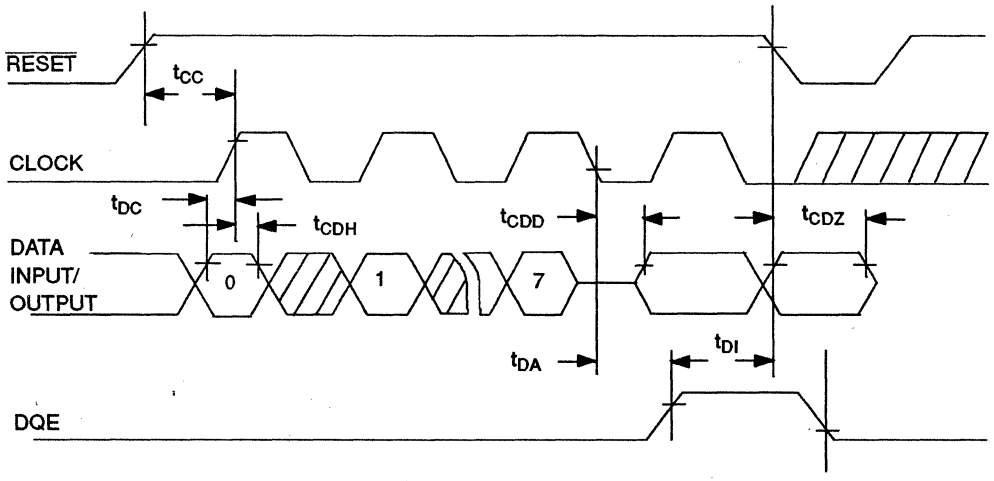
CRC GENERATION Figure 4



TIMING DIAGRAM - WRITE DATA Figure 5



TIMING DIAGRAM - READ DATA Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	-4.5	5.0	5.5	Volts	1
Input High Voltage	V_{IH}	2.2		V_{CC}	Volts	1
Input Low Voltage	V_{IL}	0.0		+0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-60		+60	µA	
I/O Leakage	I_{LO}	-10		+10	µA	
Output Current	I_{OH}	-1.0	-2.0		mA	2
Output Current	I_{OL}	2.0	3.0		mA	3
Operating Current	I_{OP}		10	20	mA	
Input Capacitance	C_{IN}		5		pF	
I/O Capacitance	C_{IB}		5		pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	4
V_{CCI} Slew Rate	t_R	1			µs	4
Power Down to $\overline{PF}$	t_{PF}	0			µs	4
$\overline{PF}$ Recovery	t_{REC}			100	µs	4

AC ELECTRICAL CHARACTERISTICS

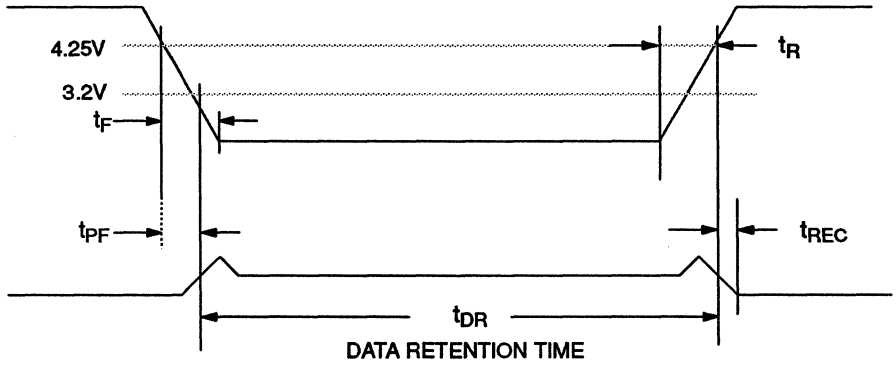
(V_{CC}=5V ± 10%, 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
Data to CLK Hold	t_{CDH}	40			ns	2
Data to CLK Delay	t_{CDD}			125	ns	2,3,5
CLK Low Time	t_{CL}	500			ns	2
CLK High Time	t_{CH}	500			ns	2
CLK Frequency	f_{CLK}	DC		1	MHz	2
CLK Rise & Fall Time	t_R t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	2

NOTES:

1. All voltages are referenced to ground.
2. @ 2.4 volts.
3. @ 0.4 volts.
4. See Figure 7.

POWER-DOWN/POWER-UP CONDITION Figure 7

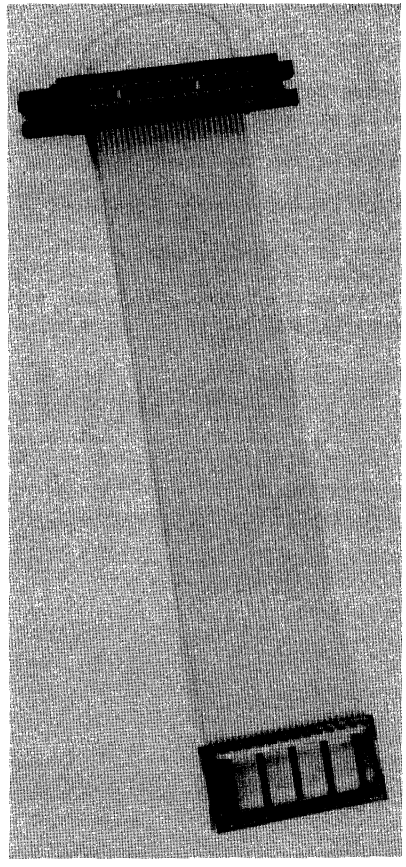


DALLAS SEMICONDUCTOR

DS9000
Bytewide Cable Harness

FEATURES

- Converts 30-position card edge to popular bytewide 28-pin DIP socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- 28-position DIP plug inserts into any standard 28-position IC DIP socket
- Color stripe indicates pin one on 28-pin DIP plug
- Standard six-inch cable length



DESCRIPTION

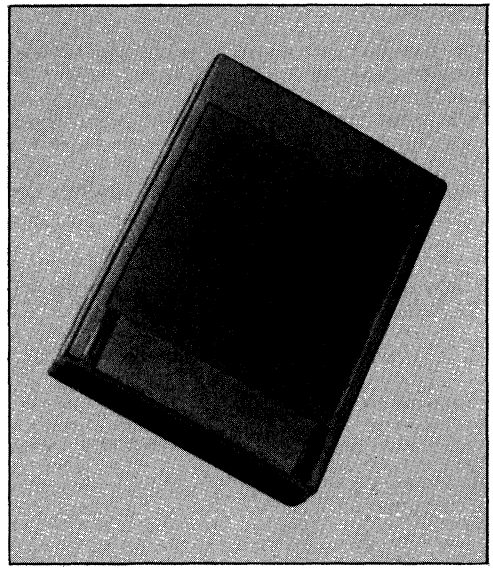
The DS9000 Bytewide Cable Harness is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges or any other 30-position card edge to the popular bytewide 28-pin DIP socket. An additional ground lead and dual key positions allow for proper insertion and withdrawal of Nonvolatile Read/Write Cartridges. A six-inch cable length allows for flexibility in end applications but does not substantially affect the performance characteristics of the DS1217.

DALLAS SEMICONDUCTOR

DS9002
Cartridge Housing

FEATURES

- Two-piece, snap together construction
- Matches form factor of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- Made of rugged, flame-retardant ABS plastic
- Accepts DS9003 Cartridge Proto Board
- Opening for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" PCB



DESCRIPTION

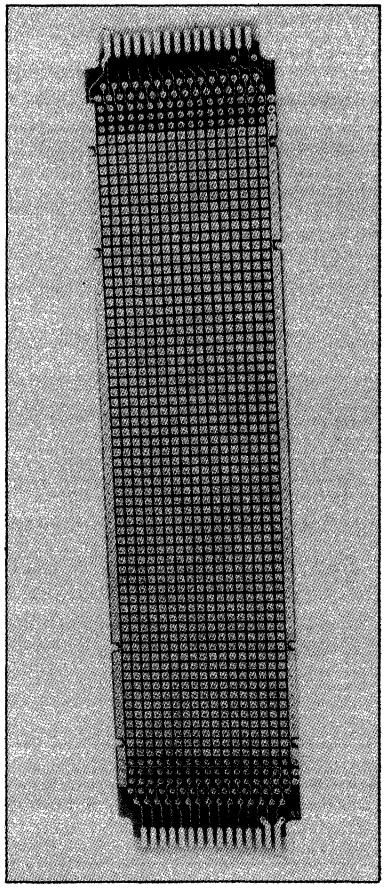
The DS9002 Cartridge Housing is a rugged, two-piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either through-hole mounted or surface mounted on both sides depending upon density requirement and board design. The outside profile of the PCB should match the DS9003 Cartridge Proto Board. Applications include nonvolatile static RAM, ROM, or EPROM memory cartridges.

DALLAS SEMICONDUCTOR

DS9003
Cartridge Proto Board

FEATURES

- Matches profile of DS1217 Nonvolatile Read/Write Cartridges
- Plated through-hole pattern for wire wrap or solder mount development
- Allows for a single double-size cartridge or two standard-size cartridges
- Gold-plated card edge fingers
- Connects to standard 28-pin DIP socket via DS9000 Bytewide Cable Harness
- Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



7

FEATURES

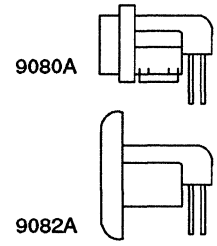
The DS9003 Cartridge Proto Board is a developmental printed circuit board for prototyping portable hand-held cartridges. The gold-plated card edge connections conform to the popular 28-pin bytewide DIP socket pinout when used with the DS9000 Bytewide Cable Harness. The card profile matches that of the DS1217 Nonvolatile Read/Write Cartridges and can be used with the DS9002 Cartridge Housing.

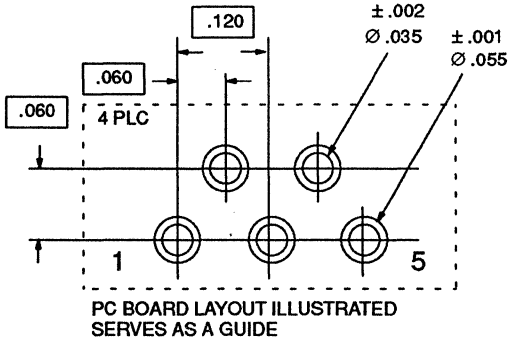
DALLAS SEMICONDUCTOR

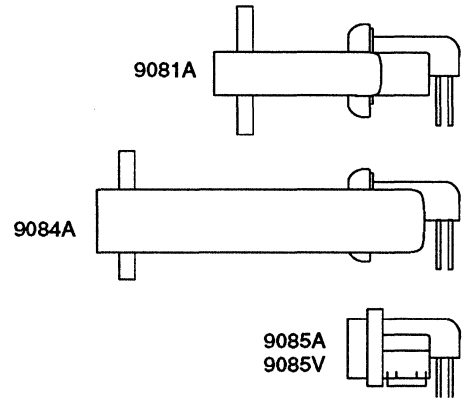
DS908xx
CyberKey/Card Receptacles

FEATURES

- Solid base metal contacts
- Durable and rugged
- Guided entry on receptacle
- High insertion force
- Greater than 50,000 cycle life







PART NUMBER	DESCRIPTION
DS9080V	Flush mount CyberKey receptacle, vertical PCB mount
DS9080A	Flush mount CyberKey receptacle, right angle PCB mount
DS9081V	Recessed CyberKey receptacle, vertical PCB mount
DS9081A	Recessed CyberKey receptacle, right angle PCB mount
DS9082V	Flush mount CyberCard receptacle, vertical PCB mount
DS9082A	Flush mount CyberCard receptacle, right angle PCB mount
DS9084V	Recessed CyberCard EV receptacle, vertical PCB mount
DS9084A	Recessed CyberCard EV receptacle, right angle PCB mount
DS9085A	Flush mount CyberCard receptacle, right angle PCB mount
DS9085V	Flush mount CyberCard receptacle, vertical angle PCB mount

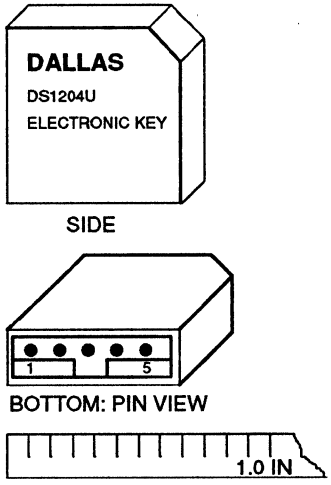
DALLAS SEMICONDUCTOR

DS1204U
Electronic Key

FEATURES

- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit security match code virtually prevents deciphering by exhaustive search with over 10^{19} possibilities
- 128 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification security match code and secure read/write memory can occur if tampering is detected
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low-power CMOS circuitry
- Four million bps data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 12

PIN DESCRIPTION

Pin 1 - V_{CC}	+5 Volts
Pin 2 - $\overline{RST}$	Reset
Pin 3 - DQ	Data Input/Output
Pin 4 - CLK	Clock
Pin 5 - GND	Ground

DESCRIPTION

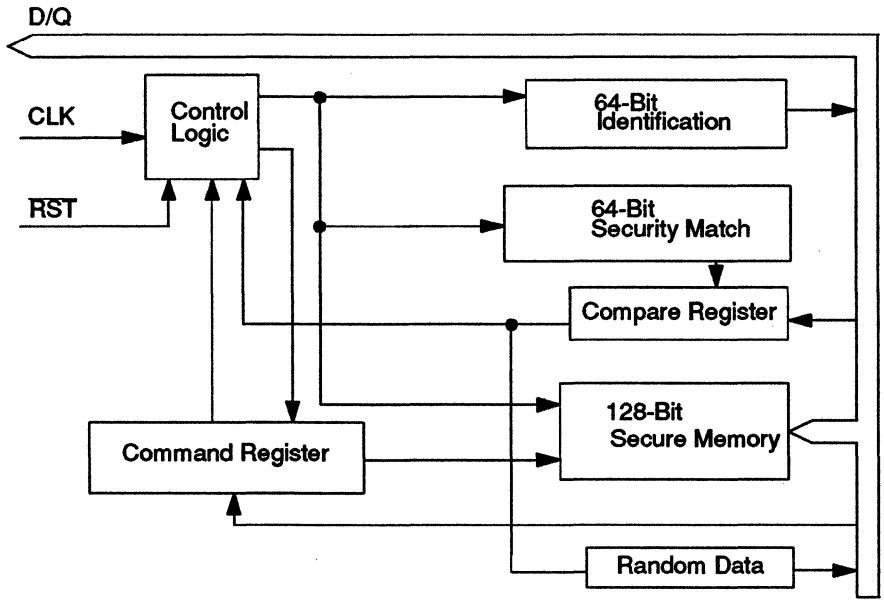
The DS1204U Electronic Key is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a procedure with a serial format to retrieve or update data. Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset ($\overline{RST}$), and Data Input/Output (DQ).

Low pin count and a guided entry for mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

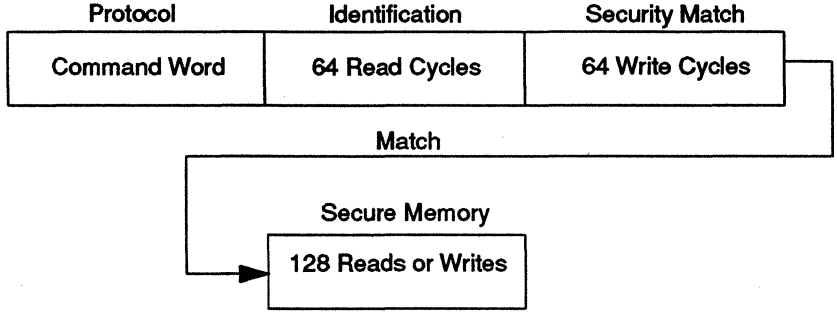
OPERATION - NORMAL MODE

The Electronic Key has two modes of operation: normal and program. The block diagram (see Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, $\overline{RST}$ is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines normal operation for read or write, or communications are ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are reads. Data is clocked out of the key on the high-to-low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

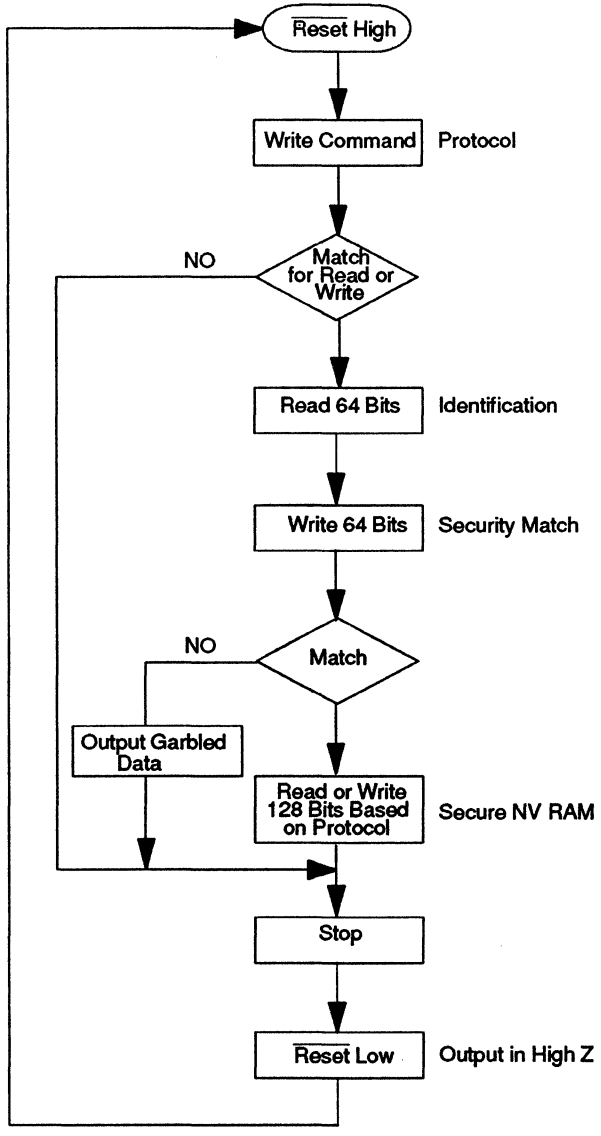
BLOCK DIAGRAM - NORMAL MODE Figure 1



SEQUENCE - NORMAL MODE Figure 2



FLOW CHART - NORMAL MODE Figure 3



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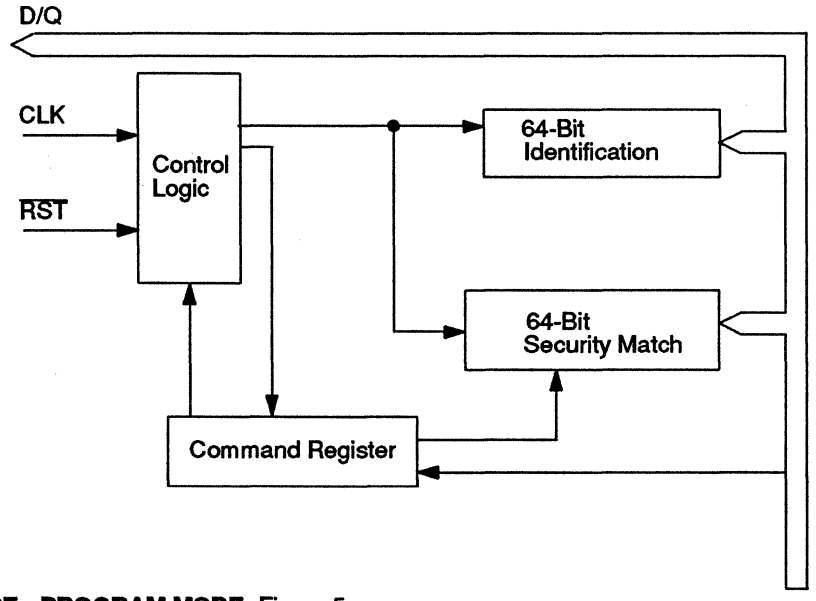
PROGRAM MODE

The block diagram in Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact pattern that defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the 128 bits that follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

BLOCK DIAGRAM - PROGRAM MODE Figure 4



SEQUENCE - PROGRAM MODE Figure 5

Protocol	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

COMMAND WORD

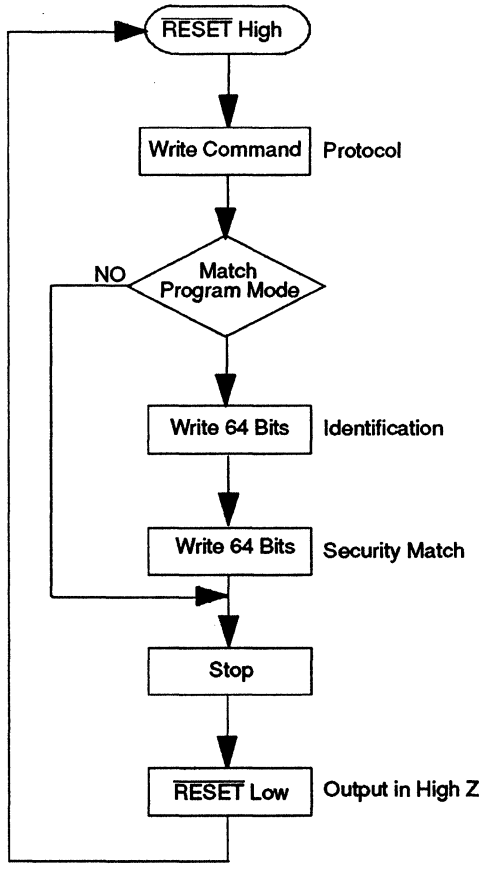
Each data transfer for the normal and program mode begins with a three-byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128-bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern that selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining six bits of byte 2 and the first seven bits of byte 3 form unique patterns that allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has five patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor, the user can specify any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE:
Contact the Dallas Semiconductor sales office for a special command word code assignment that makes possible an exclusive blank key.

FLOW CHART - PROGRAM MODE Figure 6



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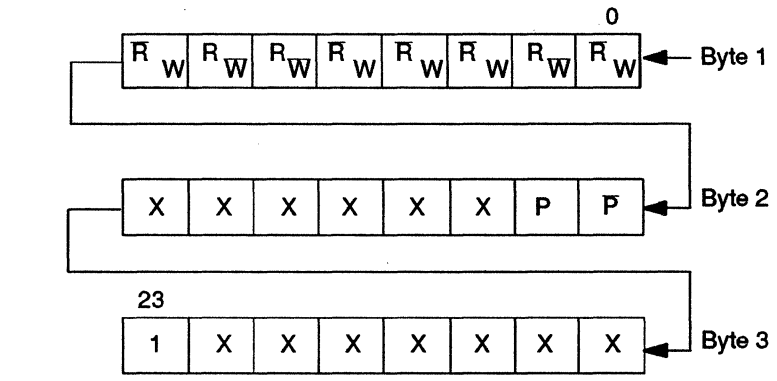
RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, it turns on control logic, which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA @ 3.0 volts is required. However, if the V_{CC} pin is connected to a 5-volt source within nominal limits, the $\overline{RST}$ is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 µA. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at a high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

COMMAND WORD Figure 7

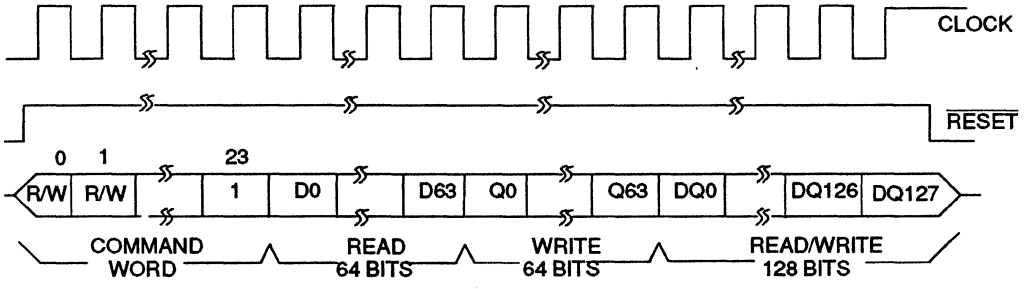


DS1204U-G01	0	0	0	0	0	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-G02	0	0	0	0	0	1	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-G03	0	0	0	0	1	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-G04	0	0	0	0	1	1	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-G05	0	0	0	1	0	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3

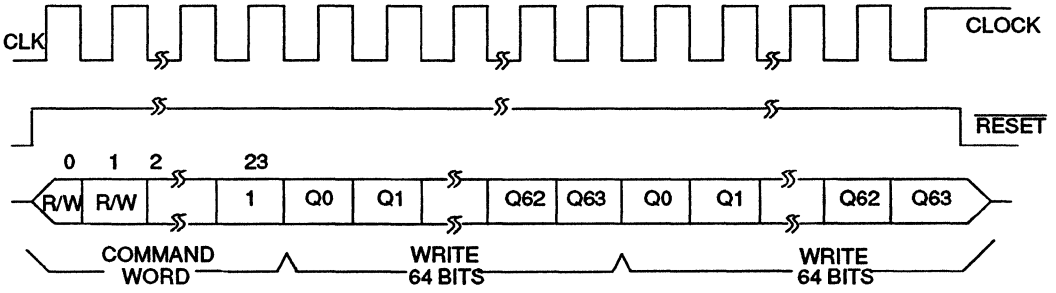
KEY CONNECTIONS

The key is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to ensure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DQ all have internal 20K ohm pulldown resistors to ground that can be sensed by a reading device.

DATA TRANSFER - NORMAL MODE Figure 8



DATA TRANSFER - PROGRAM MODE Figure 9



8

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1, 8, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.0			V	1, 9, 11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	4
Output Leakage	I_{LO}			+500	µA	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
$\overline{RST}$ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
$\overline{RST}$ Current @3.0V	I_{RST}			2	mA	6, 9, 13
Active Current	I_{CC1}			6	mA	6
Standby Current	I_{CC2}			2.5	mA	6

CAPACITANCE

(t_A = 25°C)

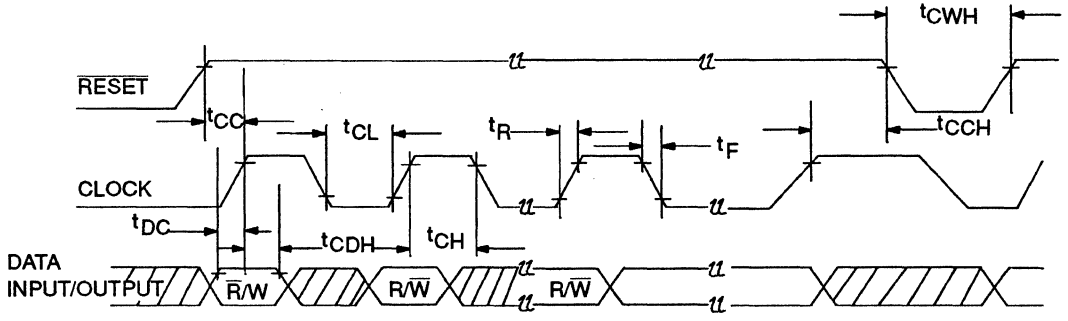
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

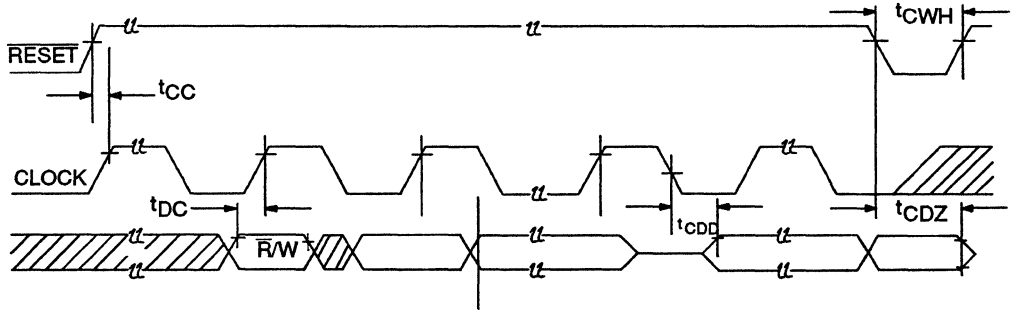
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2, 7
CLK to Data Hold	t_{CDH}	40			ns	2, 7
CLK to Data Delay	t_{CDD}			100	ns	2, 3, 5, 7
CLK Low Time	t_{CL}	125			ns	2, 7
CLK High Time	t_{CH}	125			ns	2, 7
CLK Frequency	f_{CLK}	DC		4.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F	500			ns	2, 7
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2, 7
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2, 7
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2, 7, 14
$\overline{RST}$ to I/O High Z	t_{CDZ}			50	ns	2, 7

TIMING DIAGRAM - WRITE DATA



TIMING DIAGRAM - READ DATA



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NOTES:

1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$.
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST} \geq$ 3.0V when $\overline{RST}$ supplies power.
8. Logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and $\overline{RST}$ + 0.3 volts if the $\overline{RST}$ pin supplies power.
9. Applies to $\overline{RST}$ when $V_{CC} < 3.0V$.
10. Input levels apply to CLK, DQ, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the key, then $\overline{RST}$ input reverts to V_{IHE}.
11. $\overline{RST}$ logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average AC $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})\ (CL + 140)^f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to100 ms average.

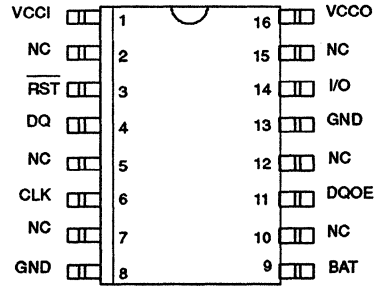
DALLAS SEMICONDUCTOR

DS1205S
MultiKey Chip

FEATURES

- Three secure read/write data partitions of 384 bits each
- One non-secure read/write data partition of 512 bits
- Secure data cannot be deciphered by reverse engineering
- Guaranteed unique, 48-bit, laser etched serial number
- 64-bit password and I.D. fields provide positive identification and security for each secure data partition
- Maximum data transfer rate of 2 million bits/second
- Low-power CMOS circuitry
- Access via 3-wire or 1-wire interface
- Applications include proprietary data, financial transactions, secure personnel areas, and systems access control

PIN ASSIGNMENT



DS1205S 16-Pin SOIC (300 mil)
See Mech. Drawing – Sect. 16, Page 6

PIN DESCRIPTION

V_{CCI}	+5V Supply (Battery Backup Mode)
$\overline{RST}$	Reset (3-Wire)
DQ	Data (3-Wire)
CLK	Clock (3-Wire)
GND	Ground
BAT	Battery (+) (Battery Backup Mode)
DQOE	Data Available (3-Wire)
I/O	Data I/O (1-Wire)
V_{CCO}	Battery (+) (Battery Powered Mode)

DESCRIPTION

The DS1205S MultiKey Chip is an enhanced version of the DS1204U Electronic Key which has both a standard 3-wire interface (data, clock, and reset) and a 1-wire interface. The DS1205S MultiKey has three secure read/write subkeys which are each 384 bits in length. In addition, there is a 512-bit read/write scratchpad which can be used as a non-secure data area or as a holding register for data transfer to one of the three subkeys. Each subkey within the part is uniquely addressable on byte boundaries.

OPERATING MODES

There are two modes of operation for powering the DS1205S MultiKey Chip. In the Normal Mode (Battery Backup), V_{CC} power is supplied to the part on the V_{CCI} pin, while the battery backup source is applied to the BAT pin. In this mode of operation, the chip supply is switched internally between V_{CCI} and BAT (depending on which is higher) and this level is presented internally to the V_{CCO} pin. In the Battery Operate Mode, the battery supply is connected directly to the V_{CCO} pin while the V_{CCI} and BAT pins are grounded.

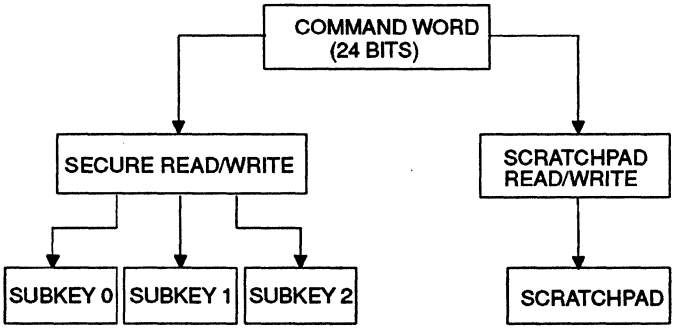
INTERFACES

Two interfaces to the DS1205S are provided. The 1-wire interface requires a 1-wire I/O command for addressing the device. An additional function command word is then passed through the 1-wire interface to access the various DS1205S functions. The 3-wire interface (data (DQ), reset ($\overline{RST}$), and clock (CLK)) requires only the function command word. The four 1-wire I/O commands that deal with the unique lasered ROM are available only through the 1-wire interface. All other functions are available through either interface.

FUNCTIONS

A command word written written to the DS1205S MultiKey specifies the operation to be performed and the partition to be operated on. There are two classes of functions available. One class includes operations on the read/write secure partitions. The other class includes operations on the read/write scratchpad (Figure 1).

COMMAND OPERATIONS Figure 1



The 24 bit function command word is organized into three fields of eight bits each. These one byte fields include the function to be performed, the memory partition to be accessed and the starting byte address for the data transfer operation. The starting byte address and the partition codes are required to be given in both real and complement form. If these values do not match, access to the part will be denied (Figure 2).

The function command word is presented to the DS1205S LSB first. The first byte contains the 8-bit function code that defines which of the six valid function codes is to be executed. Each function code is valid for only certain partition and starting address combinations. Figure 3 illustrates the valid partition code, starting address and function code combinations. The second byte consists of the 2-bit partition code, identifying which partition is being accessed, and the 6-bit starting byte address, which specifies where to start the access of the given partition. The third byte consists of the complement of the 2-bit partition code and the complement of the 6-bit starting byte address.

COMMAND WORD STRUCTURE Figure 2

MSB		LSB
$(KK)_C(AAAAAA)_C$	(KK)(AAAAAA)	FFFFFFFF

(KK) = Two-bit number specifying which partition is to be accessed. 00 specifies subkey 0. 01 specifies subkey 1. 10 specifies subkey 2. 11 specifies the scratchpad.

$(KK)_C$ = Complement of (KK) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

(AAAAAA) = Address field containing address bits that define the starting byte address of the partition to be accessed.

$(AAAAAA)_C$ = Complement of (AAAAAA) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

FFFFFFFF = Function code field. Specifies the action to be taken.

LOCATIONS, AND FUNCTION CODES FOR EACH COMMAND WORD Figure 3

COMMAND	VALID PARTITION CODE KK	VALID BYTE ADDRESS AAAAAA	VALID FUNCTION CODE FFFF FFFF
Set Scratchpad	11	0 - 63	1001 0110
Get Scratchpad	11	0 - 63	0110 1001
Set Secure Data	00, 01, 10	16 - 63	1001 1001
Get Secure Data	00, 01, 10	16 - 63	0110 0110
Set Security Match	00, 01, 10	000000	0101 1010
Move Block	00, 01, 10	000000	0011 1100

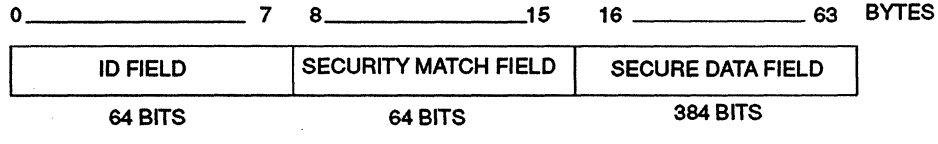
SECURE PARTITION COMMANDS

Each of the three secure partitions within the DS1205S MultiKey is comprised of a 64-bit I.D. field, a 64-bit security match code and a 384-bit secure data field (Figure 4). The three commands that operate on the secure partitions are:

1) Set Security Match
2) Set Secure Data
3) Get Secure Data

As a guard against attackers, the security match code can never be read. Similarly, tampering through reprogramming will immediately clear the entire secure partition.

SECURE PARTITION ORGANIZATION Figure 4



SET SECURITY MATCH

The Set Security Match command is used to enter data into the I.D. and security match fields of the selected secure partition. The DS1205S will respond to the command by outputting the 64-bit I.D. field of the selected secure partition. The next 64 clock cycles are used to echo the I.D. field back to the DS1205S. Upon receipt of the correct I.D., the DS1205S MultiKey will erase the contents of the selected secure partition. The part is then ready to receive the the new 64-bit I.D. and the 64-bit security match code. The flow sequence is shown in Figure 5.

SET SECURE DATA

The Set Secure Data command is used to write data into the selected secure partition. After the command is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is output. The next 64 bits of input comprise a password that must match the security match code of the selected secure partition. If the password and the security match are identical, data is written to the secure data field starting at the address specified in the command word. If the password and the security match code are not identical, the DS1205S will terminate the transaction immediately. The flow sequence is shown in Figure 6.

GET SECURE DATA

The Get Secure Data command is used to retrieve data from the selected secure partition. After the command word is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is returned. The next 64 bits are the password being written to the DS1205S. If the presented password and the security match code of the selected secure partition are identical, the DS1205S will output the contents of the secure data field starting from the byte specified in the command word. If the presented password is not identical to the security match code, the DS1205S MultiKey will use the password as a "seed" for its internal random number generator. This results in a repeatable, seemingly valid yet false response to the invalid password. The flow sequence is shown in Figure 7.

SCRATCHPAD READ/WRITE COMMANDS

The 512-bit read/write scratchpad of the DS1205S MultiKey is not protected by a security match code. This partition is byte addressable. The scratchpad can be used to store unsecured data or it can act as a staging area to build and verify data structures to be transferred to a secure partition. The three commands that operate on the read/write scratchpad are:

1) Set Scratchpad Data
2) Get Scratchpad Data
3) Move Block

SET SCRATCHPAD DATA

The Set Scratchpad Data command is used to enter data into the DS1205S MultiKey scratchpad. The command word must specify the starting byte address for the data transfer. Valid byte addresses are 0 through 63. The DS1205S MultiKey will write data to the scratchpad until byte 63 has been written or until the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 8.

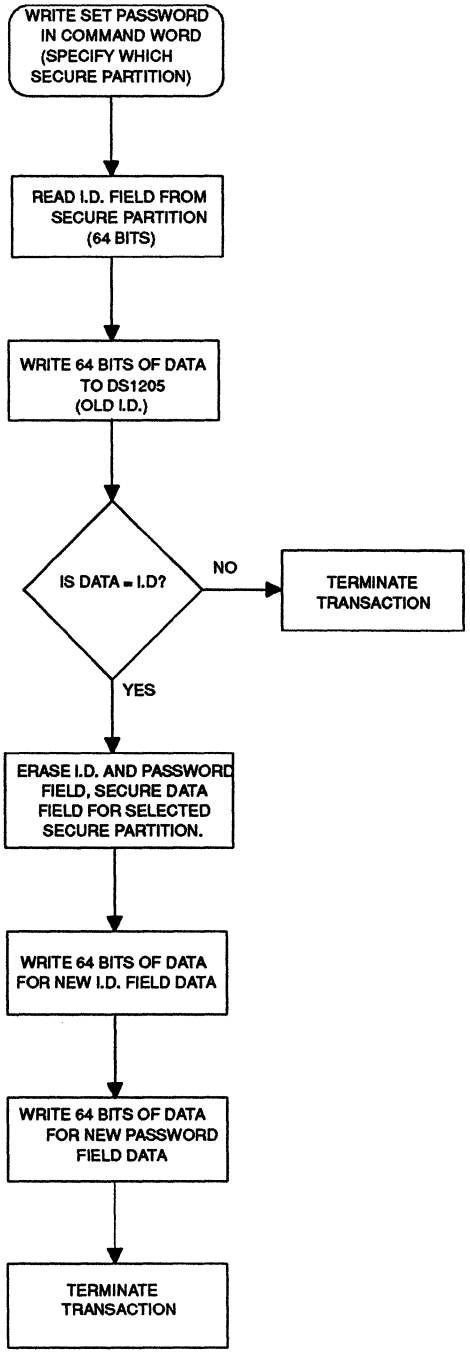
GET SCRATCHPAD DATA

The Get Scratchpad data command is used to retrieve data from the 512-bit scratchpad. The command word must specify the starting byte address for the data retrieval. Valid byte addresses are 0 through 63. The DS1205S MultiKey will retrieve data from the scratchpad until byte 63 has been read or the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 9.

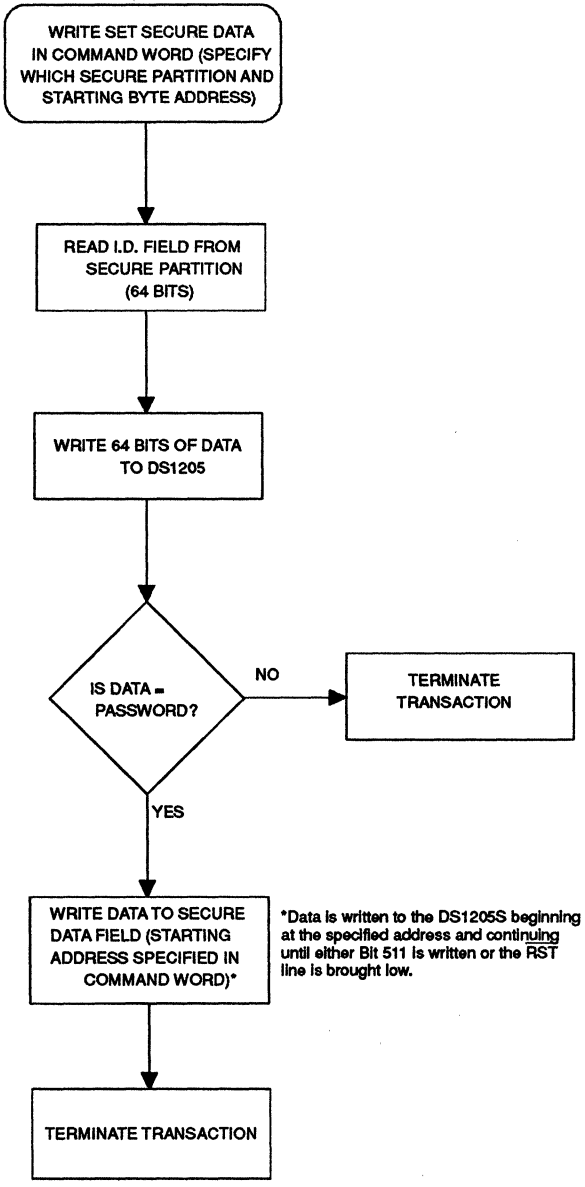
MOVE BLOCK

The Move Block command is used to transfer data, which has been previously entered into the scratchpad and verified, to one of the three secure subkeys. Data can be transferred as one large block of 512 bits or it can be transferred in blocks of 64 bits each (Figure 10). There are nine valid block selectors which are used to specify which block or blocks are to be transferred (Figure 11). As a further precaution against accidental erasure of a secure subkey, the 64-bit password of the destination subkey must be entered and match the destination subkey. If the passwords fail to match, the operation is terminated. The flow sequence is shown in Figure 12.

SET SECURITY MATCH Figure 5

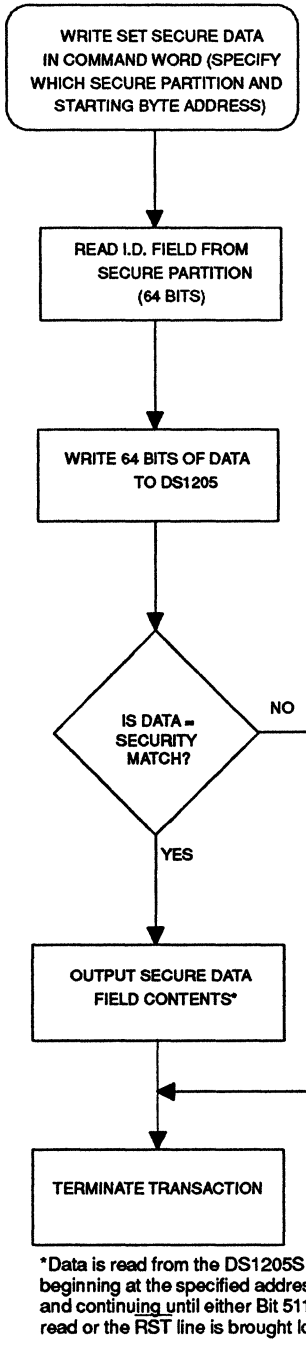


SET SECURE DATA Figure 6



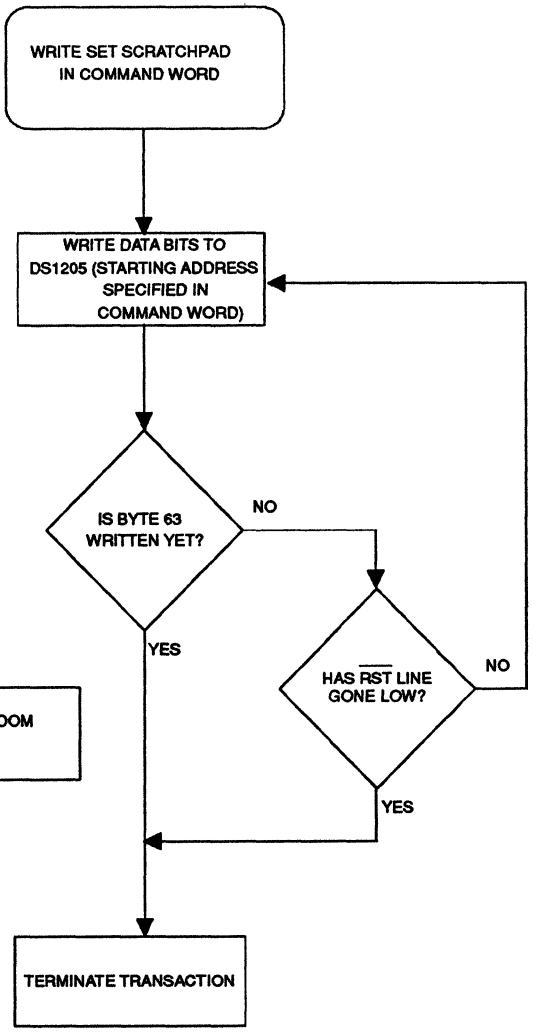
*Data is written to the DS1205S beginning at the specified address and continuing until either Bit 511 is written or the RST line is brought low.

GET SECURE DATA Figure 7



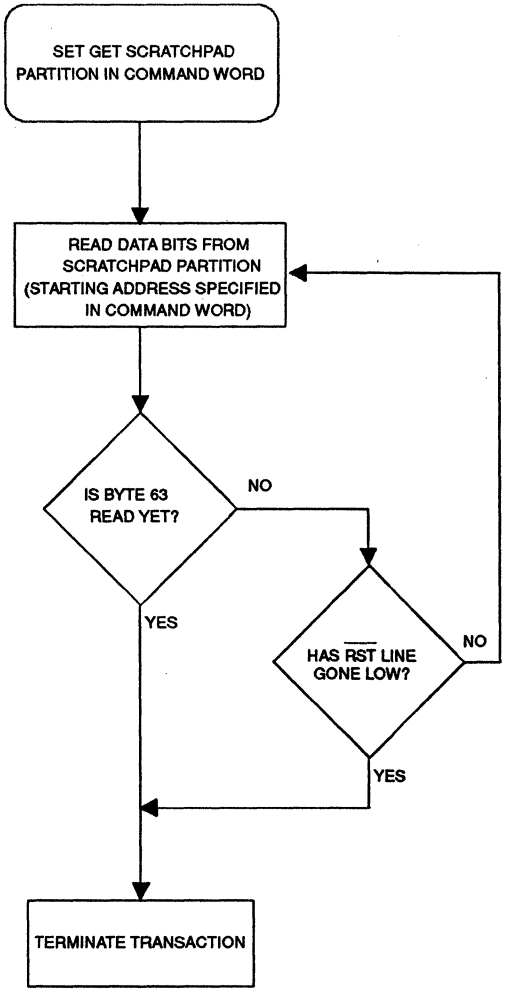
*Data is read from the DS1205S beginning at the specified address and continuing until either Bit 511 is read or the $\overline{RST}$ line is brought low.

SET SCRATCHPAD Figure 8



8

SET SCRATCHPAD Figure 9



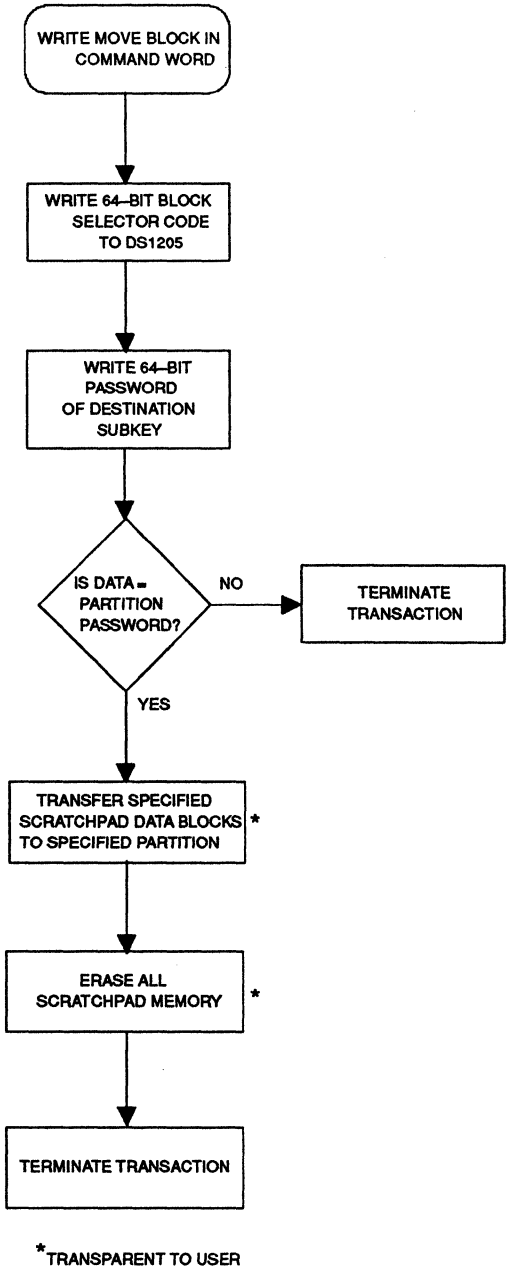
BLOCK SELECTIONS Figure 10

BLOCK NUMBER	BYTE ADDRESS SCRATCHPAD	IN: SUBKEY
0	0-7	0-7(ID)
1	8-15	8-15 (PASSWORD)
2	16-23	16-23 (SECURED)
3	24-31	24-31 (SECURED)
4	32-39	32-39 (SECURED)
5	40-47	40-47 (SECURED)
6	48-55	48-55 (SECURED)
7	56-63	56-63 (SECURED)

BLOCK SELECTOR CODES FOR MOVE BLOCK COMMAND Figure 11

BLOCK #	SELECTOR CODE
0	4C69 6E64 9DB3 9A9A (H)
1	4C69 919B 624C 9A9A (H)
2	4C96 6E9B 62B3 659A (H)
3	4366 616B 6D43 6A6A (H)
4	BC99 9E94 92BC 9595 (H)
5	B369 9164 9D4C 9A65 (H)
6	B396 6E64 9DB3 6565 (H)
7	B396 919B 624C 6565 (H)
ALL BLOCKS	7F5A 5D57 517F 5656 (H)

MOVE BLOCK Figure 12



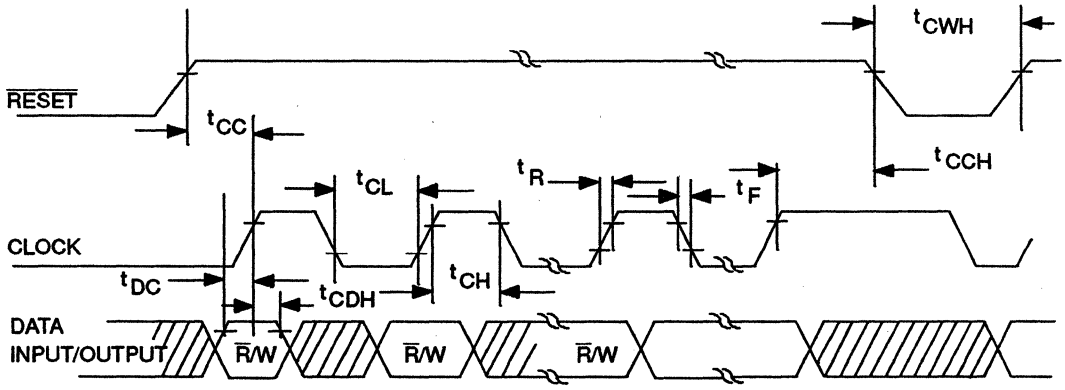
3-WIRE BUS

The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ ($\overline{reset}$) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ signal provides a method of terminating a data transfer.

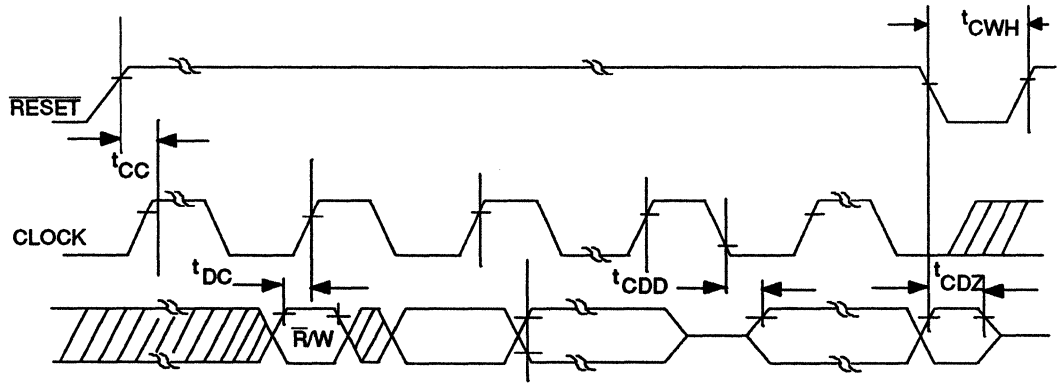
A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if $\overline{RST}$ is low and the DQ pin goes to a high impedance state. When data transfers to the DS1205S are terminated by the $\overline{RST}$ signal going low, the transition of the $\overline{RST}$ going low must occur during a high level of the CLK signal. Failure to ensure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figure 13 and Figure 14 for normal modes of operation.

8

WRITE DATA TIMING DIAGRAM Figure 13



READ DATA TIMING DIAGRAM Figure 14



1-WIRE PROTOCOL

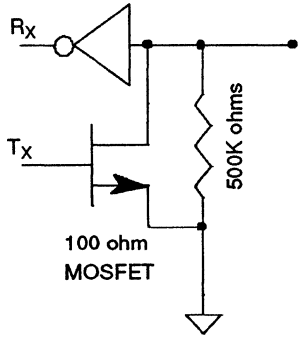
The 1-wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1205S is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence.

Hardware Configuration

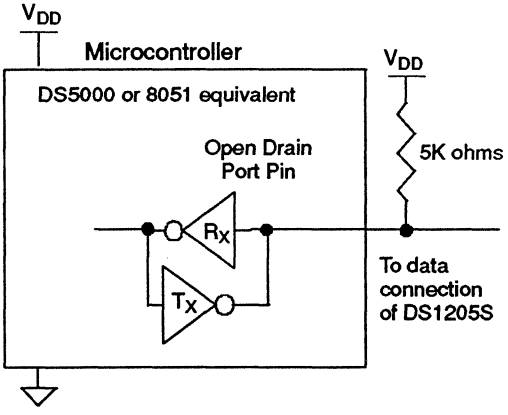
The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain connections. The DS1205S is an open drain part with an internal circuit equivalent to that shown in Figure 15. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 16. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left for more than 560 µS, all components on the bus will be reset.

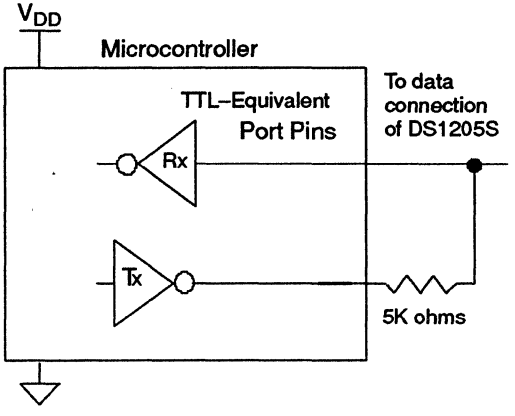
EQUIVALENT CIRCUIT Figure 15



BUS MASTER OPEN DRAIN CIRCUIT
Figure 16A



BUS MASTER STANDARD TTL CIRCUIT
Figure 16B



Transaction Sequence

The protocol for accessing the DS1205S is as follows:

Reset
Presence Detect
1-wire Command Word
Device Command Word
Transaction/Data
CRC

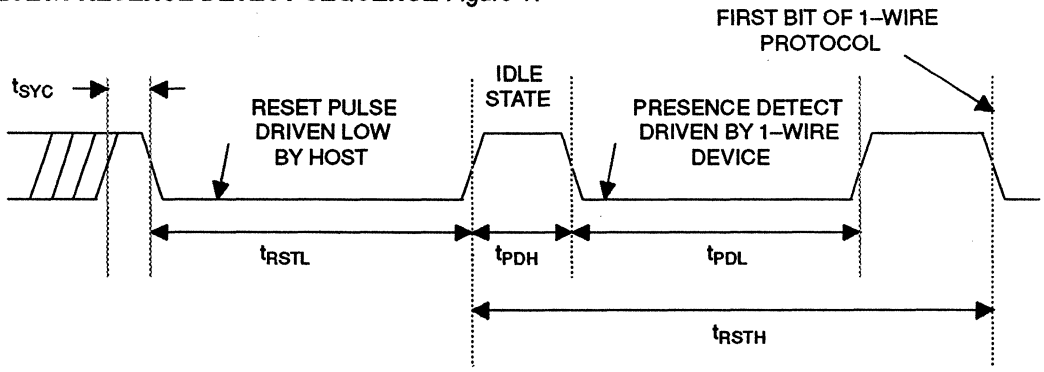
Reset/Presence Detect - All transactions on the 1-wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 560 µS. The DS1205S is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high, the part is taken out of reset, and the part is ready to issue the presence detect.

After detecting a high state on the data line, the DS1205S waits 15 µS minimum and issues its presence detect. This presence detect is a low-going pulse that last 70 µS. This response to the reset pulse lets the bus master know that the DS1205S is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise as the DS1205S is taken on and off the bus. Refer to the timing diagram in Figure 17.

After the DS1205S has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1 µS. The 1 µS interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 17.

8

RESET/PRESENCE DETECT SEQUENCE Figure 17



1-Wire I/O Commands - Once the bus master has detected a presence, it can issue one of the four different 1-wire I/O commands. These commands deal with the laser-etched ROM code which has the following format.

Type ID	Unique Serial Number	CRC
8 bits	48 bits	8 bits

All 1-wire commands are eight bits long. A list of these commands are as follows:

CCh Pass Thru Mode

This command saves time by allowing direct access to the DS1205S without identifying it by ROM ID number. This command can only be used when there is a single slave on the bus. If more than one device is present, there will be bus contention.

33h Read ROM Data

This command allows the bus master to read the DS1205S's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1205S on the bus. If more than one is present, there will be bus contention.

55H Match ROM Data

This mode allows the bus master to single out a specific DS1205S on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple device on the bus.

F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the ID numbers of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins by resetting all devices present on the 1-wire bus. After this, the bus master will attempt to read the family code, serial number, and CRC value for the part.
2. The bus master will then issue the Search ROM Data command on the 1-wire bus.
3. The bus master performs two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the first bit of the devices on the bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

At this point, the bus master repeats the process described above to determine the address of the remaining devices on the 1-wire bus by repeating steps 1 though 7.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ID is:

960 µS + 3(8+64) X 0.06mS = 13.92mS

The bus master is therefore capable of identifying 60 different 1-wire devices per second.

Additionally, the data obtained from the two reads of each set of three have the following interpretations:

00 - There are still devices attached which have conflicting bits in this position.
01 - All devices still coupled have a zero bit in this bit position.
10 - All devices still coupled have a one bit in this bit position.
11 - There are no devices attached to the 1-wire bus.

Transmitting/Receiving Data - All communications on the 1-wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1205S is in the listening mode. The bus master must then transmit the 1-wire command to the DS1205S. To transmit the first bit of the 1-wire I/O command, the master pulls the bus low for 1 µS. This low-going edge informs the DS1205S that the first bit is being sent. After 1 µS, the master does one of two things:

1. holds the line low for an additional 70 µS to output a 0 (write a 0) or,
2. lets the bus go high for an additional 70 µS (write a 1).

The state of the bus during this 70 µS time phase determines the value of the bit. The DS1205S will sense any rising edge during this 70 µS time phase as a one. After the 70 µS has lapsed, the bus master must then drive the bus high for 1 µS. This is the frame sync mentioned earlier. This process is repeated until all the eight bits are transmitted. Refer to the timing diagram in Figure 18.

The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1 µS. This informs the DS1205S that it should have data on the bus no later than the 1 µS from the falling edge. After the 1 µS, the bus master lets go of the bus and the DS1205S drives the bus. The slave must hold the data on the bus for an additional 14 µS minimum (59 µS maximum). During the DS1205S holding time, the bus master reads the state of the bus. Ideally, the bus master should read data from the bus 15 µs after the falling edge. The entire cycle time for one bit lasts a minimum of 70 µS (140 µS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1 µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 19 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1205S must be reset.

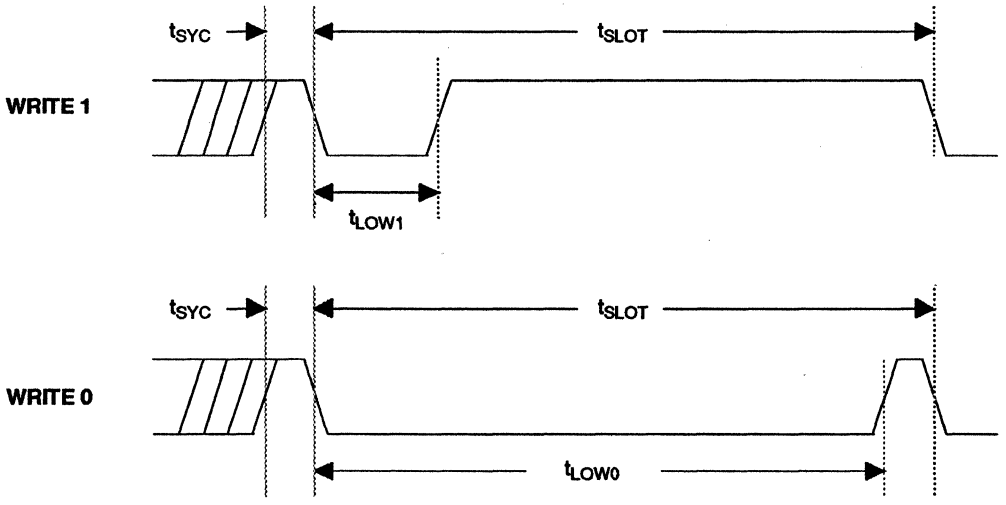
CRC Generation - To validate the transmitted data from the DS1205S, the bus master must generate a CRC value for the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1205S. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. The CRC is calculated using the following polynomial.

$$CRC = px^3 + px^2 + 1$$

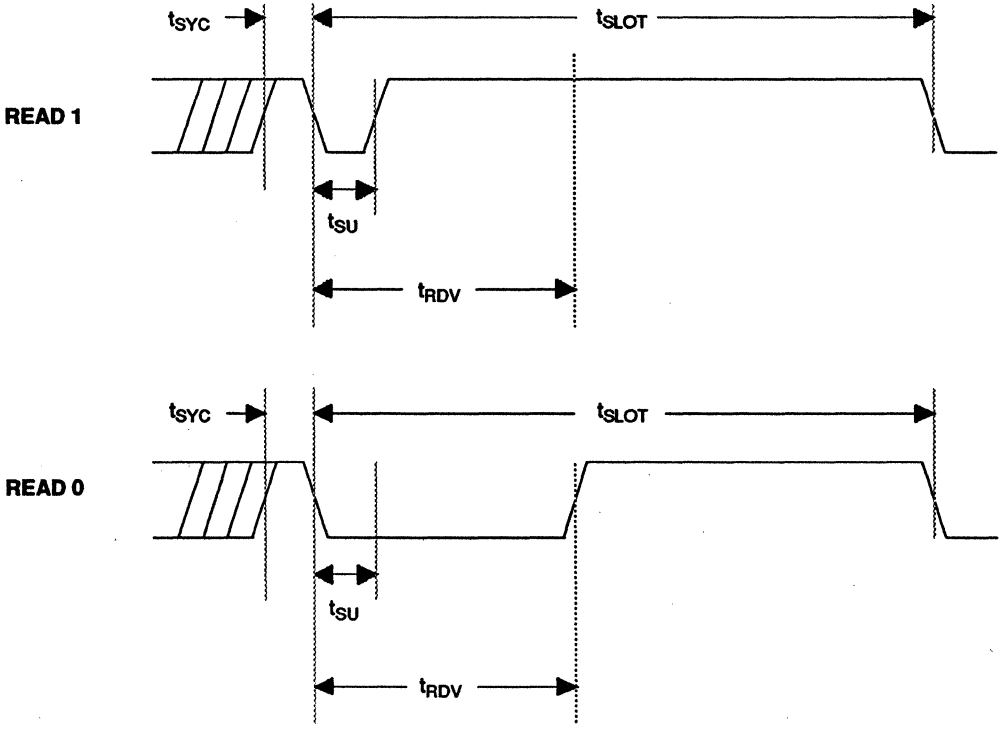
If the two CRC values match, the transmission is error-free.

8

1-WIRE WRITE TIMING Figure 18



1-WIRE READ TIMING Figure 19



PASS-THRU MODE

A host connected to the 1-wire bus may send function commands directly to the DS1205S without preceding them with 1-wire I/O commands by using the pass-thru command (CCh). This command bypasses the serial number and consequently it can only be used when there is one DS1205S on the 1-wire bus.

1-WIRE/3-WIRE ARBITRATION

The DS1205S can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for ext ended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	
Output Leakage	I_{OL}			+500	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+1	mA	
$\overline{RST}$ Input Resistance	Z_{RST}	100		1000	Kohm	
D/Q Input Resistance	Z_{DQ}	100		1000	Kohm	
CLK Input Resistance	Z_{CLK}	100		1000	Kohm	
Active Current	I_{CC1}		3	6	mA	5,6
Standby Current	I_{CC2}			100	µA	5,6
Batt. Operate Consumption	I_{BAT}		200	500	nC	7,8
Batt. Operate Standby Current	I_{BATS}		30	200	nA	7
Batt. Voltage	V_{BAT}	2.0		3.6	V	1
Output Supply Current	I_{CCO}			10	mA	11

CAPACITANCE

(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			200	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0°C to 70°C, V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	t_{SLOT}	70		140	µS	
Write 1 Low Time	t_{LOW1}	1		15	µS	
Write 0 Low Time	t_{LOW0}	70		140	µS	
Read Data Valid	t_{RDV}	15			µS	
Read Data Setup	t_{SU}	1			µS	10
Frame Sync	t_{SYC}	1			µS	
Reset Low Time	t_{RSTL}	560			µS	
Reset High Time	t_{RSTH}	560			µS	9
Presence Detect High	t_{PDH}	15		70	µS	
Presence Detect Low	t_{PDL}	70		280	µS	

NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. (Normal battery backup operation) V_{CC1} = 5.0 Volts ± 10%; V_{BAT} = 3.0 Volts.
7. (Battery operate mode) V_{CCO} = 3.0 Volts.
8. Per transaction (512 bits + protocol).
9. An additional reset or communication sequence cannot begin until the reset high time has expired.
10. Read data setup time refers to the time the host must pull the 1-wire pin low to read a bit. Data is guaranteed to be valid within 1 µS of this falling edge and will remain valid for 14 µS minimum (15 µS total falling edge on 1-wire).
11. $V_{CCO} = V_{CCI}$ - 0.3V

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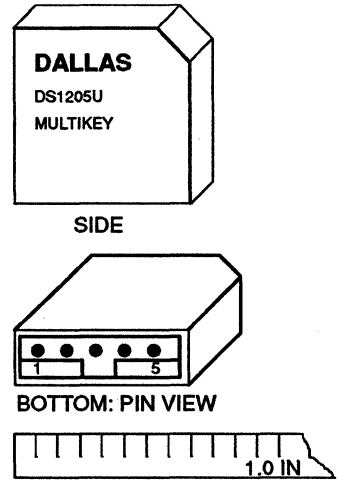
DALLAS SEMICONDUCTOR

DS1205U MultiKey

FEATURES

- Three secure read/write data partitions of 384 bits each
- 64-bit security match and I.D. fields provide positive identification and security for each secure data partition
- One non-secure read/write partition of 512 bits
- Electrical tampering is met with seemingly valid, yet false, responses
- Secure data cannot be deciphered by reverse engineering
- Over 10 years of data retention with no limitations on write cycles
- Access via Dallas 3-Wire Interface
- Applications include software authorization, configuration management, and systems access control

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 12

DESCRIPTION

The DS1205U MultiKey has three, 384-bit read/write data partitions, each protected by its own 64-bit I.D. and security match fields. The security match field, programmed by the customer, can never be read from the DS1205U. An additional security feature, the Intelligent Response generator, uses invalid security match codes as the "seed" to trigger seemingly valid, yet false responses to electronic attack.

Communication with the DS1205U is via the Dallas 3-Wire Interface (Data, Clock, $\overline{\text{Reset}}$). These signals are under host software control.

The DS1205U MultiKey is designed to be plugged into a standard 5-pin, 0.1 inch-center SIP receptacle. A guide is provided to insure proper alignment with the receptacle.

System designers can use the DS1205U to insure that their valuable firmware can only by run when a valid key is present. The MultiKey can also contain data on system configurations and upgrade options. Designers may choose to allow maintenance or diagnostic routines to be run only by an authorized key holder.

See the DS1205S MultiKey Chip data sheet for implementation details.

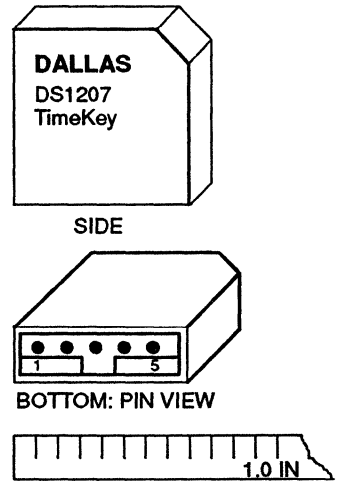
DALLAS SEMICONDUCTOR

DS1207 TimeKey

FEATURES

- Cannot be deciphered by reverse engineering
- Time allotment from one day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit match code virtually prevents discovery by exhaustive search with over 10^{19} possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification, security match code and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 12

PIN DESCRIPTION

Pin 1	NC	No connection
Pin 2	$\overline{RST}$	Reset
Pin 3	DQ	Data input/output
Pin 4	CLK	Clock
Pin 5	GND	Ground

DESCRIPTION

The DS1207 TimeKey is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 384 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a procedure with a serial format to retrieve or update data. The TimeKey is set to expire from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its countdown from the first access by the end user.

Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), $\overline{Reset}$ ($\overline{RST}$) and Data Input/Output (DQ). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

OPERATION – NORMAL MODE

The TimeKey has two modes of operation: normal and program. The normal mode of operation provides the functions of reading and writing the 384-bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey, $\overline{RST}$ is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communications are ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high-to-low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if a normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to write the 384-bit secure memory.

OPERATION - PROGRAM MODE

The program mode of operation provides the functions of programming the identification and security match memory, and setting and reading the amount of time the TimeKey can be used. The block diagram in Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines the program mode for the identification and security match bits or the program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time for which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20-bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by 2^{20} (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20-bit day clock counter is driven by an internal oscillator that has a period of 82.4 ms. If the command register is properly loaded with the function code for reading the 9-bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If the program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the 9-bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the TimeKey will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24-bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register are ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed, provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24-bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is

properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24-bit command word only (see Figure 10). This command will only execute prior to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11). First, program the identification and security match bits to the desired value. Use normal mode operation to write the appropriate secure data. Second, write the number days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20-bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. The lock command should be issued, followed by the arm oscillator command. The TimeKey will start the countdown to expiration on the next access. To guarantee security, a locked TimeKey cannot be unlocked. The key cannot be reprogrammed after expiration. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

COMMAND WORD

Each data transfer for normal and program mode begins with a 3-byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. Eight function codes are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause the transfer to abort. The program mode can be invoked with one of seven function codes: program identification and security match, read the 20-bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining six bits of byte 2 and the first four bits of byte 3 must be written to match one of the five patterns as indicated in Figure 12 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits can be defined by the user as any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 provides a summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode.

Note: Contact the Dallas Semiconductor sales office for special command word code assignment that makes possible an exclusive blank TimeKey.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA at 3.5 volts is required. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the clock cycle. Command bits and data bits are input on the rising edge of the clock. Data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

TIMEKEY CONNECTIONS

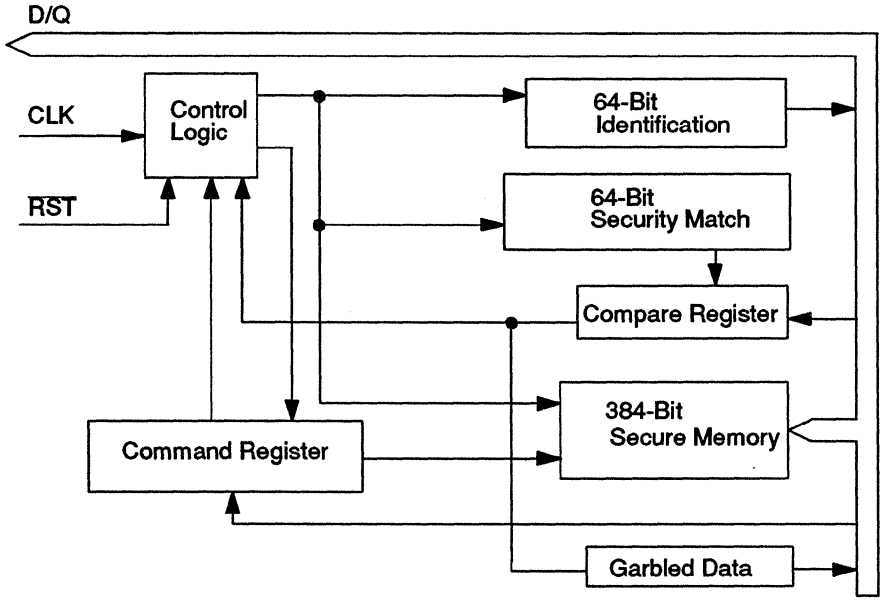
The TimeKey is designed to be plugged into a standard 5-pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to ensure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DQ all have 20K ohm pulldown resistors to ground that can be sensed by a reading device.

COMMAND WORDS Table 1

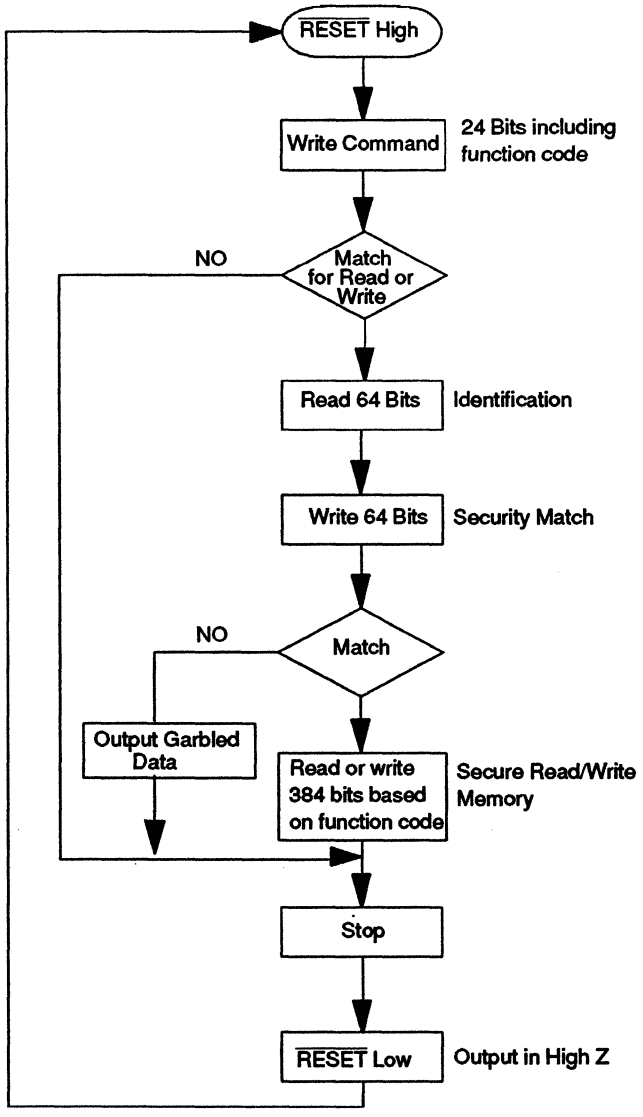
Summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode for the DS1207-G01 only.(See Figure 12 and Figure 13 for detailed command words.)

MODE	FUNCTION	COMMAND WORDS		
		MSB		LSB
NORMAL	READ	B0	01	62
NORMAL	WRITE	B0	01	9D
PROGRAM	WRITE	B0	02	9D
PROGRAM	READ DAY CLOCK COUNTER	B0	02	F1
PROGRAM	READ DAYS REMAINING	B0	02	F3
PROGRAM	WRITE DAYS REMAINING	B0	02	F2
PROGRAM	ARM OSCILLATOR	B0	02	F5
PROGRAM	LOCK NUMBER OF DAYS COUNT	B0	02	F6
PROGRAM	STOP OSCILLATOR	B0	02	F4

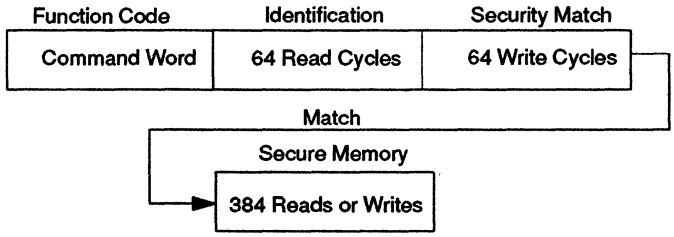
BLOCK DIAGRAM: NORMAL MODE Figure 1



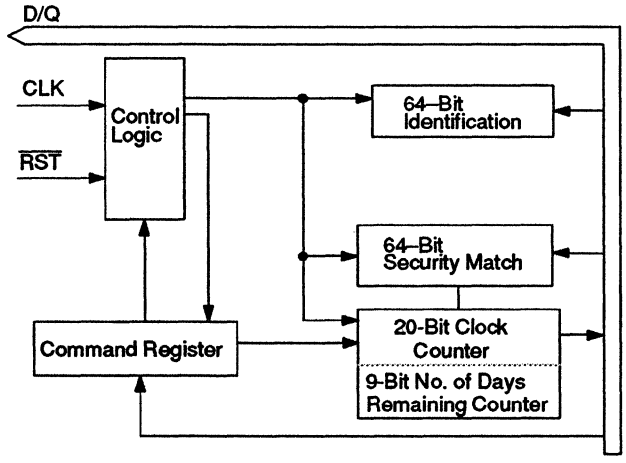
NORMAL MODE: READ OR WRITE SECURE READ/WRITE MEMORY Figure 2A



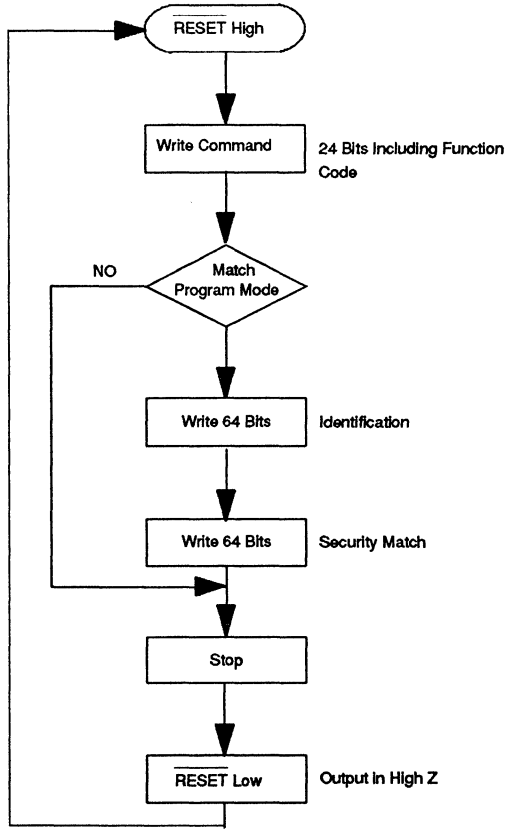
SEQUENCE: NORMAL MODE, READ OR WRITE SECURE MEMORY Figure 2B



BLOCK DIAGRAM: PROGRAM MODE Figure 3



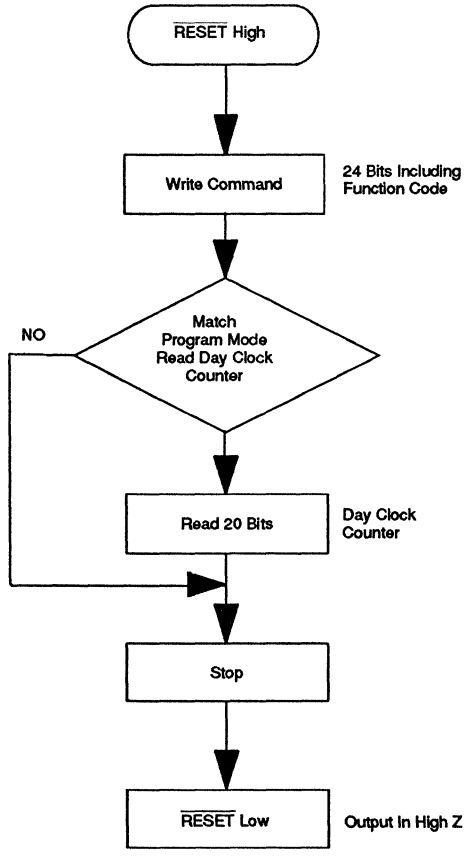
PROGRAM MODE: PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 4A



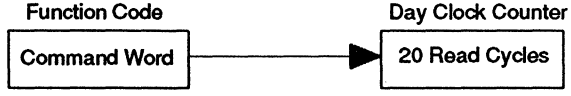
SEQUENCE: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH BITS Figure 4B

Function Code	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

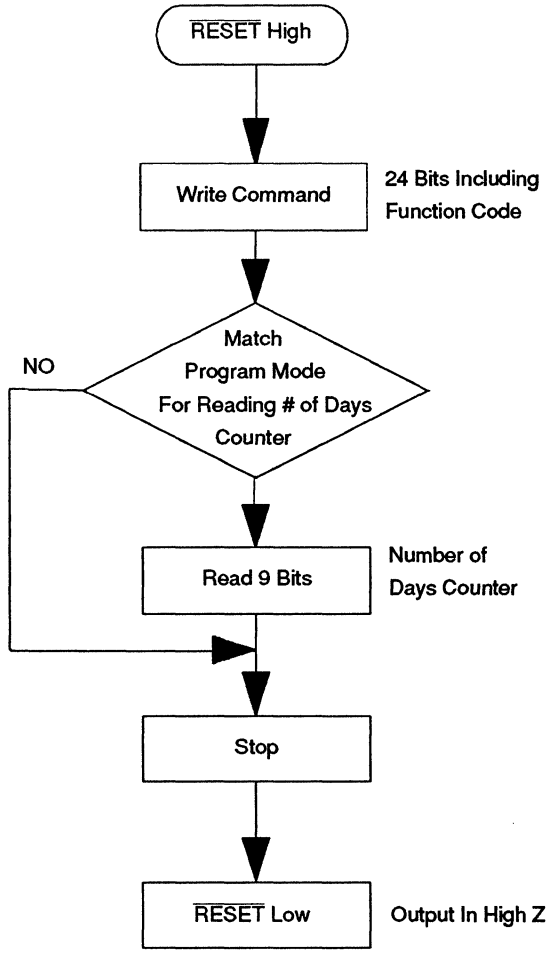
FLOW CHART: PROGRAM MODE, READING THE 20-BIT DAY CLOCK CALENDAR Figure 5A



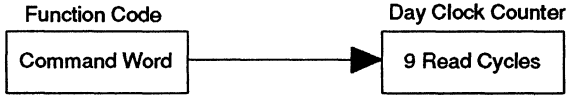
SEQUENCE: PROGRAM MODE, READING THE 20-BIT DAY CLOCK COUNTER Figure 5B



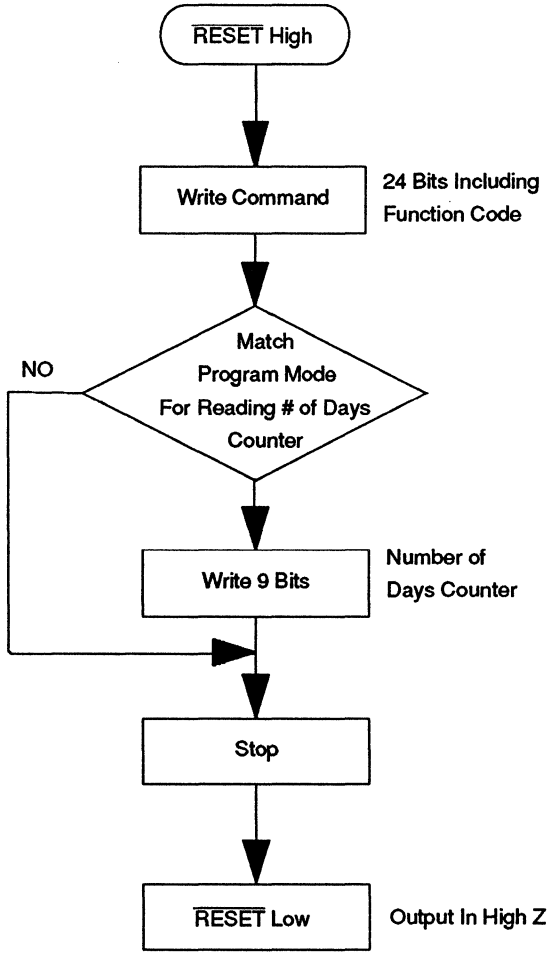
FLOW CHART: PROGRAM, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6A



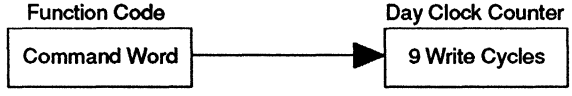
SEQUENCE: PROGRAM MODE, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6B



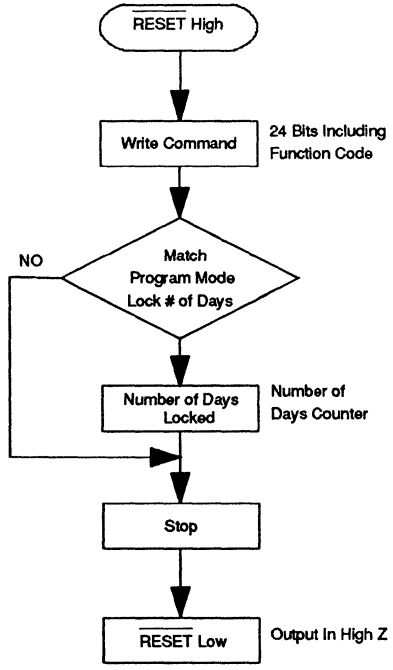
FLOW CHART: PROGRAM MODE, WRITING TO NUMBER OF DAYS COUNTER Figure 7A



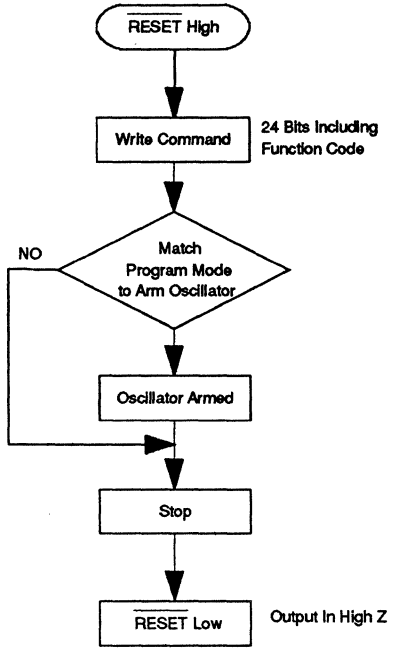
SEQUENCE: PROGRAM MODE, WRITING THE NUMBER OF DAYS COUNTER Figure 7B



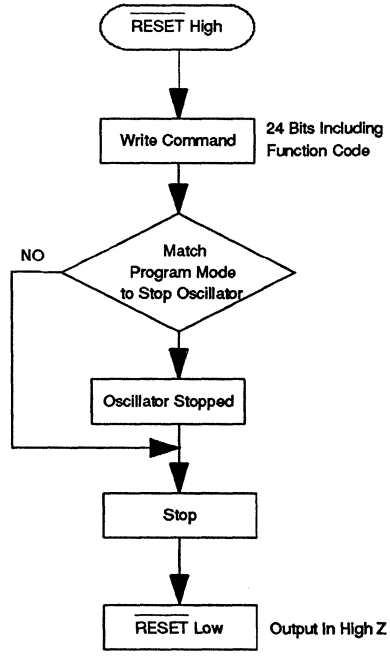
FLOW CHART: PROGRAM MODE, LOCK NUMBER OF DAYS REGISTER Figure 8



FLOW CHART: PROGRAM MODE, ARM OSCILLATOR Figure 9



FLOW CHART: PROGRAM MODE, STOP OSCILLATOR Figure 10

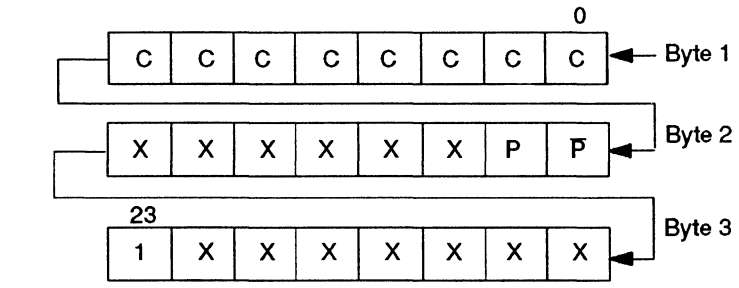


SETTING THE TIME UNTIL EXPIRATION OF THE DS1207 Figure 11

Step 1	Program identification memory Program security match bits Write normal mode secure data
Step 2	Program write the number of days remaining Program read the number of days remaining for verification
Step 3*	Issue arm oscillator command
Step 4*	Do a read of any kind
Step 5*	Program read the day clock counter several times (verify that the oscillator is running)
Step 6*	Issue the stop oscillator command
Step 7	Issue the lock command
Step 8	Issue the arm oscillator command (time of expiration will start on first access)

* Steps 3 through 6 are not required. Dallas Semiconductor tests and guarantees that the oscillator will start without verification.

COMMAND WORD Figure 12



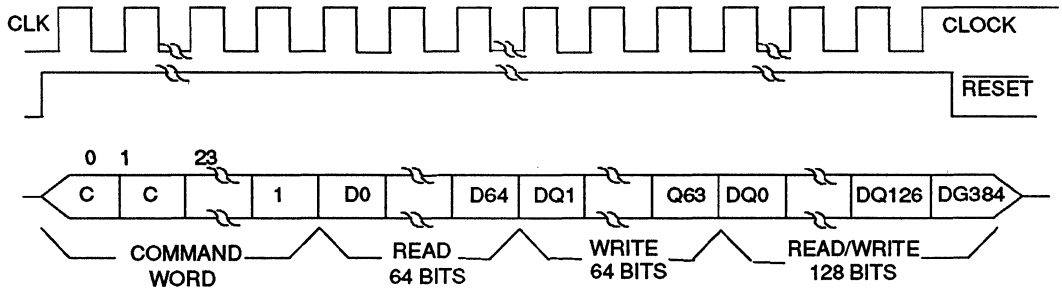
DS1207-G01	0	0	0	0	0	0	P	P̄	Byte 2
	1	0	1	1	0	0	0	0	Byte 3
DS1207-G02	0	0	0	0	0	1	P	P̄	Byte 2
	1	0	1	1	0	0	0	0	Byte 3
DS1207-G03	0	0	0	0	1	0	P	P̄	Byte 2
	1	0	1	1	0	0	0	0	Byte 3
DS1207-G04	0	0	0	0	1	1	P	P̄	Byte 2
	1	0	1	1	0	0	0	0	Byte 3
DS1207-G05	0	0	0	1	0	0	P	P̄	Byte 2
	1	0	1	1	0	0	0	0	Byte 3

8

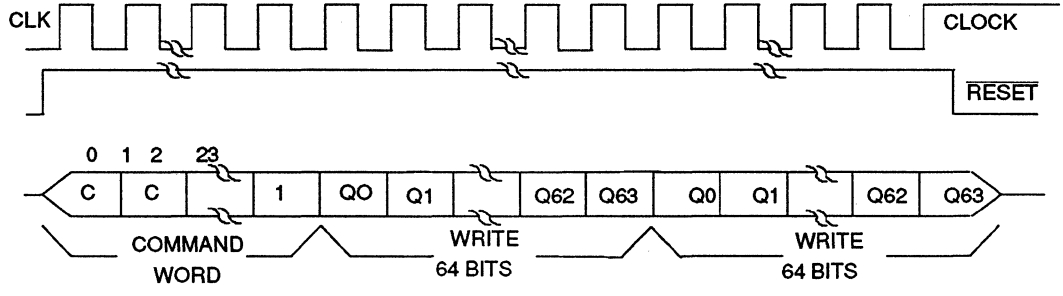
FUNCTION CODES: FIRST BYTE OF COMMAND WORD Figure 13

MSB							LSB	
0	1	1	0	0	0	1	0	READ
1	0	0	1	1	1	0	1	WRITE
1	1	1	1	0	0	0	1	READ DAY CLOCK COUNTER
1	1	1	1	0	0	1	0	WRITE NUMBER OF DAYS REMAINING
1	1	1	1	0	0	1	1	READ NUMBER OF DAYS REMAINING
1	1	1	1	0	1	0	0	STOP OSCILLATOR
1	1	1	1	0	1	0	1	ARM OSCILLATOR
1	1	1	1	0	1	1	0	LOCK NUMBER OF DAYS COUNT

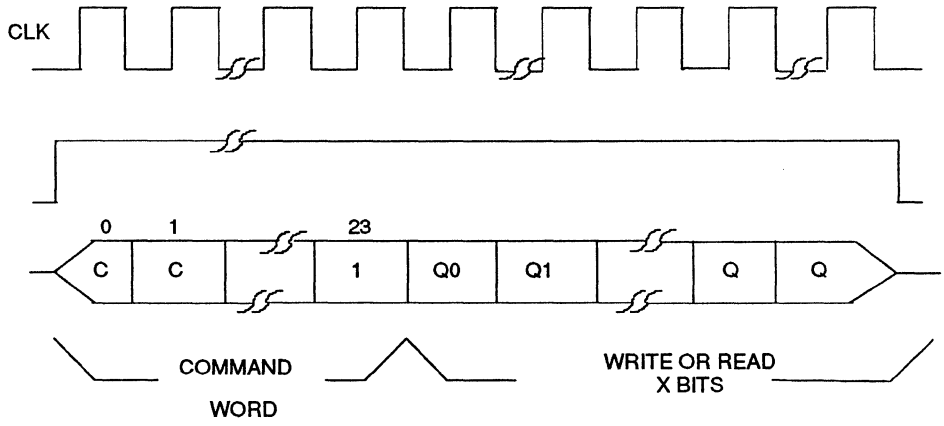
DATA TRANSFER: NORMAL MODE, READ OR WRITE SECURE READ/WRITE MEMORY Figure 14



DATA TRANSFER: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 15A



DATA TRANSFER: PROGRAM MODE, DAY CLOCK, DAYS REMAINING AND OSCILLATOR CONTROL Figure 15B



NOTE: The number of bits which follow the command word will be either 0, 9, or 20 bits based on the function code.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{\text{Reset}}$ Logic 1	V_{IHE}	3.5			V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $\overline{RST}$ = 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	µA	4
Output Leakage	I_{LO}			+500	µA	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
$\overline{\text{RST}}$ Current @3.5V	I_{RST}			2	mA	6, 9

CAPACITANCE

($t_A = 25°C$)

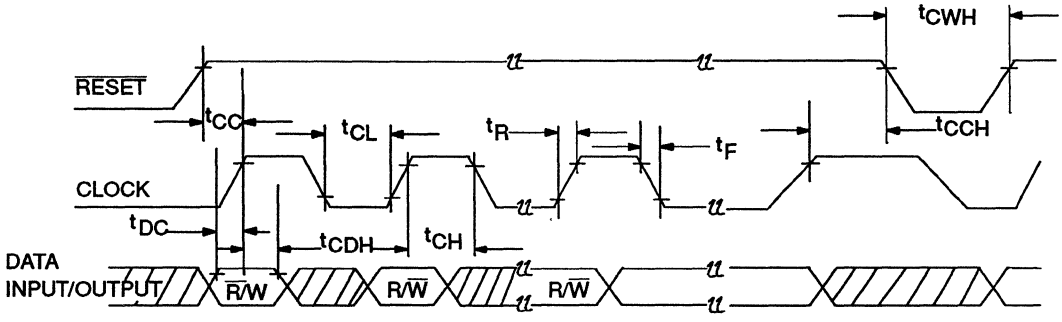
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

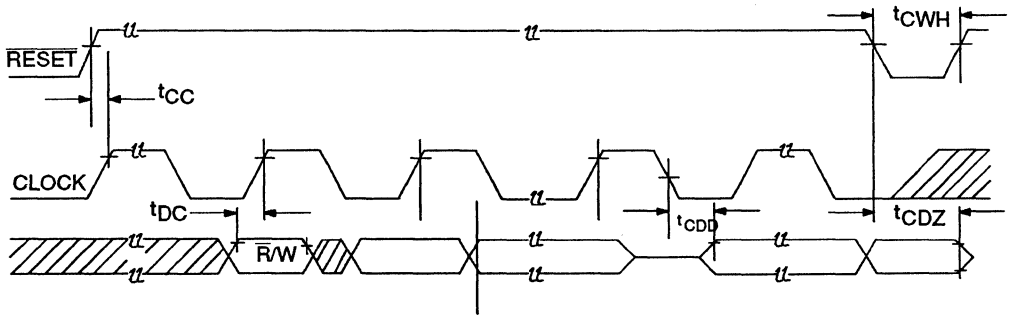
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	2, 7
CLK to Data Hold	t_{CDH}	70			ns	2, 7
CLK to Data	t_{CDD}			200	ns	2, 3, 5, 7
CLK Low Time Delay	t_{CL}	250			ns	2, 7
CLK High Time	t_{CH}	250			ns	2, 7
CLK Frequency	f_{CLK}	DC		2.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F			500	ns	2, 7
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2, 7
CLK to $\overline{RST}$ Hold	t_{CCH}	60			ns	2, 7
$\overline{RST}$ Inactive Time	t_{CWH}	10			ms	2, 7,
$\overline{RST}$ To I/O High Z	t_{CDZ}			70	ns	2, 7

TIMING DIAGRAM - WRITE DATA



TIMING DIAGRAM: READ DATA



NOTES:

1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$.
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST}$ greater than or equal to 3.5 volts.
8. Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
9. Average AC $\overline{RST}$ current can be determined using the following formula:
   $I_{TOTAL} = 2 + I_{LOAD}$ DC + (4 x 10-3)(CL + 280)f
   I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.
   Applying the above formula, a load capacitance of 50 pF
   running at a frequency of 2.0 MHz gives an I_{TOTAL} of 1.6 mA.

8

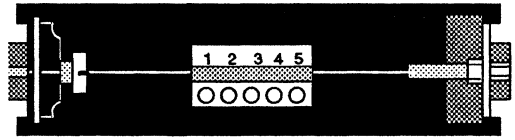
DALLAS SEMICONDUCTOR

DS1255U
Printer Port KeyRing

FEATURES

- Self-contained add-on fixture for user-insertable Electronic Keys, Tags, and TimeKeys
- Connects to the parallel printer port of an IBM XT, AT, PS/2, or compatible computer
- End user installation
- Machine screw SIPS ensure connection to DS1204U key pins
- Two keys may be resident at one time
- Transient suppression circuits protect against electrostatic discharge or accidental connection to serial port
- Key, Tag, and TimeKey communications are totally controlled by software
- Normal computer/printer operation is unaffected
- Applications include software authorization, Key and Tag programmer, computer site identification, and access control

PIN ASSIGNMENT



PIN DESCRIPTION

Pin 1	V_{CC}	+5 Volts
Pin 2	$\overline{RST}$	$\overline{RESET}$
Pin 3	D/Q	Data In/Out
Pin 4	CLK	CLOCK
Pin 5	GND	GROUND

DESCRIPTION

The DS1255U Printer Port KeyRing adapts low-pin Electronic Keys (DS1204U), Tags (DS1201), and TimeKeys (DS1207) to the IBM PC parallel printer port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the KeyRing, and reconnecting the printer to the back connector on the KeyRing. Two Keys or Tags can be resident at the same time. Communication with Keys is established by soft ware-controlled sequences to the parallel printer port. The three control signals ($\overline{Reset}$, Clock, and Data In/Out) for Keys are generated by the parallel port.

OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK, and D/Q must be software-controlled to duplicate the behavior as defined in the respective data sheet for keys. Each signal is a function of a specific output or I/O line of the printer port (Figure 1). Pin 4 on the 25-pin D connector parallel printer port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at high level when communicating with keys. When $\overline{RST}$ is driven low, all communication to keys is terminated. The $\overline{RST}$ signal is also used as a source of power for keys (see respective data sheets).

Pin 5 on the 25-pin D connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of keys. Because the CLK signal provides timing, the relationship between both level and transition is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to keys,

and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will guarantee that data is valid as the CLK changes level.

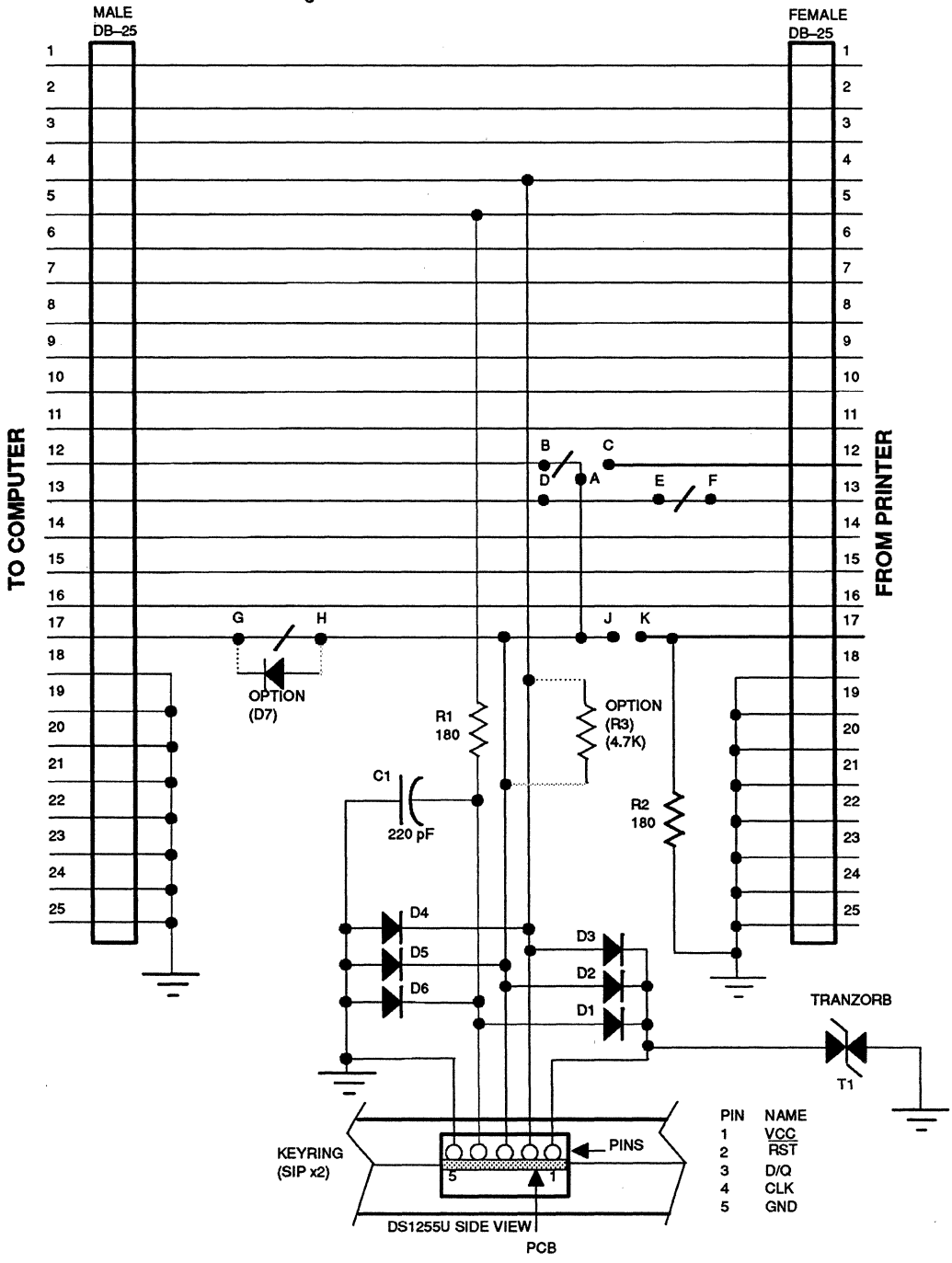
Pin 17 on the 25-pin D connector parallel printer port is called $\overline{\text{SLCTIN}}$ and is used as the data I/O signal for keys. This is a bidirectional signal. Data is output from this port signal during write cycles and input from keys during read cycles. In addition, Pin 12 on the 25-pin D connector parallel printer port is called PAPER EMPTY and can be used to read data from the keys. This would be required for non-compatible printer ports, with Pin 17 as an output only. Pin 18 on the 25-pin D connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. Example software for IBM PC, XT, AT or compatible computers is available from the factory. In order to avoid having the printer interpret key communications as printer commands, the strobe signal (Pin 1 on the 25-pin D connector parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

INSTALLATION

The parallel Printer Port KeyRing is installed by first removing the printer cable. If the parallel printer port is not being used, this step is not necessary. The printer cable is removed by loosening the top and bottom retaining screws and unplugging the cable. The next step is to install the KeyRing by plugging the male side of the KeyRing into the female printer port. The top and bottom retaining screws should be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer cable is secure, a Key, Tag, or TimeKey can be plugged into either of two receptacles and the computer and KeyRing are now ready for use.

DS1255U BLOCK DIAGRAM Figure 1



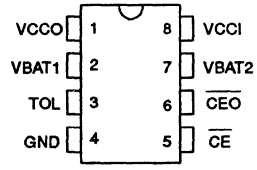
DALLAS SEMICONDUCTOR

DS1210
Nonvolatile Controller Chip

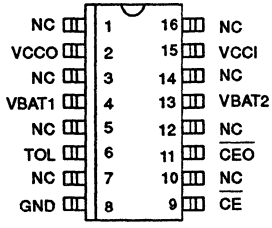
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



DS1210 8-Pin DIP (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 1



DS1210S 16-Pin SOIC (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

V_{CCO}	- RAM Supply
V_{BAT1}	- + Battery 1
TOL	- Power Supply Tolerance
GND	- Ground
$\overline{CE}$	- Chip Enable Input
$\overline{CEO}$	- Chip Enable Output
V_{BAT2}	- + Battery 2
V_{CCI}	- + Supply
NC	- No Connect

DESCRIPTION

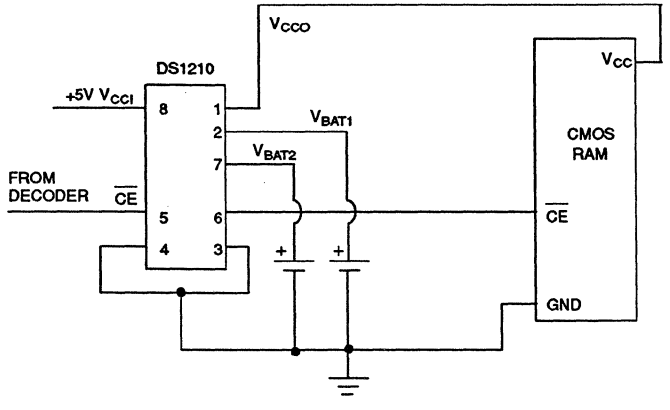
The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the V_{CCI} or battery supply. If $\overline{CE}$ input is low at the time power fail detection occurs, the $\overline{CEO}$ output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the $\overline{CEO}$ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power- up to prevent spurious writes.

SECTION A – BATTERY BACKUP Figure 1

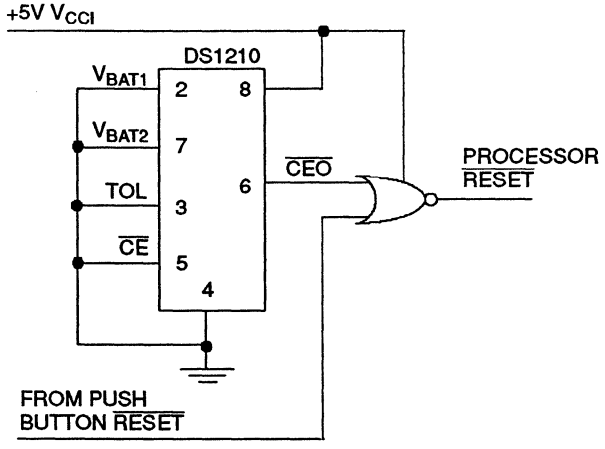


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CC02}	10 µA
Total Drain	10.1 µA

SECTION B - PROCESSOR RESET



9

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

DC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CEO}$ Output @2.4V	I_{OH}	-1.0			mA	5
$\overline{CEO}$ Output @0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

($0°C$ to $70°C$, V_{CCI} = < V_{BAT})

$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	7
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Current @ V_{cco} = V_{BAT} - 0.3V	I_{CCO2}			50	µA	6,7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(V_{CCI} = 4.5 to 5.5V, Pin3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

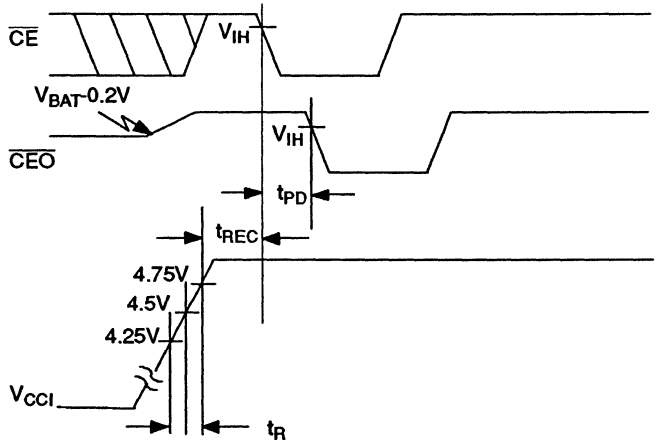
($0°C$ to $70°C$, V_{CCI} < 4.75V, Pin 3 = GND; V_{CCI} < 4.5, Pin 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	8

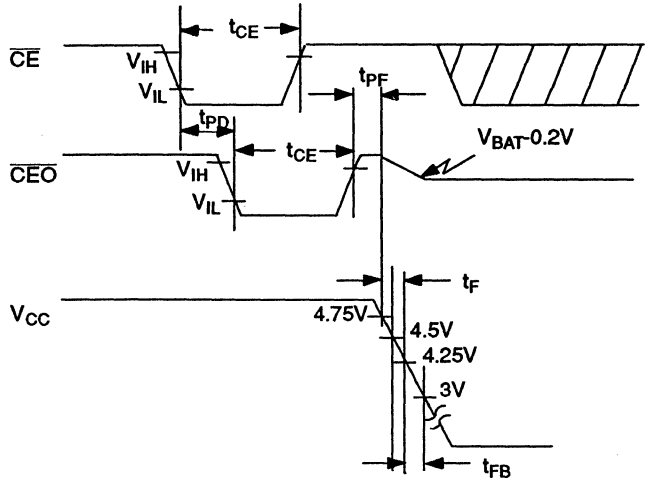
NOTES

1. All voltages are referenced to ground.
2. Only one battery input is required. Unused battery inputs must be grounded.
3. Measured with V_{CCO} and $\overline{CEO}$ open.
4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery back-up mode.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

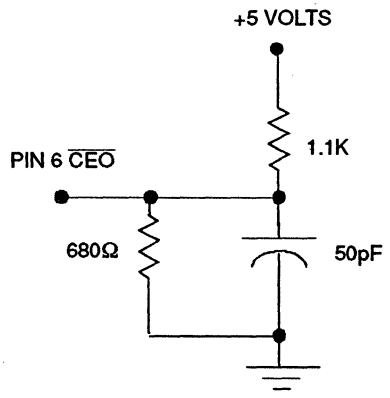
TIMING DIAGRAM - POWER UP



TIMING DIAGRAM - POWER DOWN



OUTPUT LOAD Figure 2



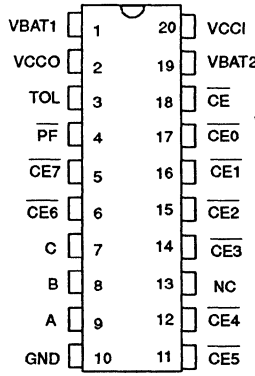
DALLAS SEMICONDUCTOR

DS1211
Nonvolatile Controller X 8 Chip

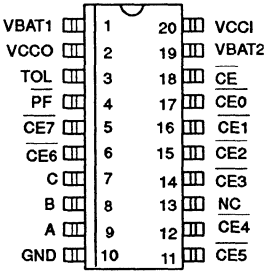
FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to eight CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package
- Optional industrial temperature range of -40° to +85°

PIN ASSIGNMENT



20-Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg.1



20-Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

A, B, C	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE0}$ - $\overline{CE7}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
$\overline{PF}$	- Power Fail
NC	- No Connection

DESCRIPTION

The DS1211 Nonvolatile Controller x 8 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, nonvolatile RAM operation can be achieved for up to eight CMOS memories.

See the data sheet for the DS1212 Nonvolatile Controller x 16 Chip for electrical specifications and operation.

DALLAS SEMICONDUCTOR

DS1212
Nonvolatile Controller X 16 Chip

FEATURES

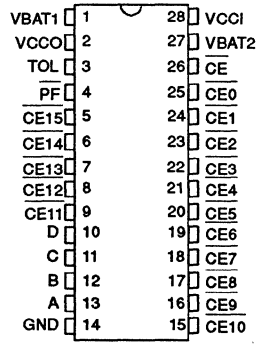
- Converts full CMOS RAM into nonvolatile memory
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package
- Optional industrial temperature range of -40°C to +85°C

DESCRIPTION

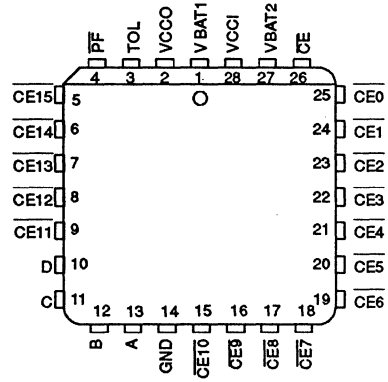
The DS1212 Nonvolatile Controller x16 Chip is a CMOS circuit that solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply the RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process that affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 Nonvolatile Controller chip and lithium batteries, nonvolatile RAM operation can be achieved for up to 16 CMOS memories.

PIN ASSIGNMENT



28-Pin DIP (600 MIL)
See Mech. Drawing – Sect. 16, Pg. 4



28-Pin PLCC
See Mech. Drawing – Sect. 16, Pg. 11

PIN DESCRIPTION

A, B, C, D	- Address Inputs
$\overline{CE}$	- Chip Enable
$\overline{CE0}$-$\overline{CE15}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
$\overline{PF}$	- Power Fail

OPERATION

The DS1212 performs six circuit functions required to decode and battery back up a bank of up to 16 RAMs. First, the 4 to 16 decoder provides selection of one of 16 RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function the DS1212 provides is power fail detection. It constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts, or 4.5 volts, depending o n the level of tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until V_{CCI} is back in normal limits.

The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE15}$) to within 0.2 volts of V_{CCI} or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4-to-16 decoder, shown in Figure 1.

The fifth function the DS1212 performs is a battery status warning so that data loss is avoided. Each time the circuit is powered up, the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted.

The sixth function of the DS1212 provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

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NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS					OUTPUTS															
CE	D	C	B	A	CE0	CE1	CE2	CE3	CE4	CE5	CE6	CE7	CE8	CE9	CE10	CE11	CE12	CE13	CE14	CE15	PF
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level
L = Low Level
X = Irrelevant
NOTE: V_{CCI} input is 250 mV lower when TOL PIN3 = V_{CCO}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCO}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.75 to 5.5V, Pin 3 = GND)
(0°C to 70°C, V_{CCI} = 4.5 to 5.5V, Pin3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Current @ V_{CCO}= V_{CCI}-0.2	I_{CCO1}			80	mA	1,4,10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$-$\overline{CE15}$,$\overline{PF}$ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$-$\overline{CE15}$,$\overline{PF}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CCO})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C, V_{CCI} < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$-CE15 Output	V_{OHL}	V_{BAT}-0.2			V	3,7
Battery Current	I_{BAT}			0.1	µA	2,3
Battery Backup Current @ V_{CCO}=V_{BAT1}-0.5V	I_{CC2}			100	µA	6,10,11

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.75 to 5.5V, Pin 3 = GND)
(0°C to 70°C, V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C, V_{CCI} < 4.75V, Pin 3 = GND)
(0°C to 70°C, V_{CCI} < 4.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power-Down	t_F	300			µs	
V_{CC} Slew Rate Power-Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power-Up	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7,8
Power Fail to $\overline{PF}$ Low	t_{PFL}	300			µs	

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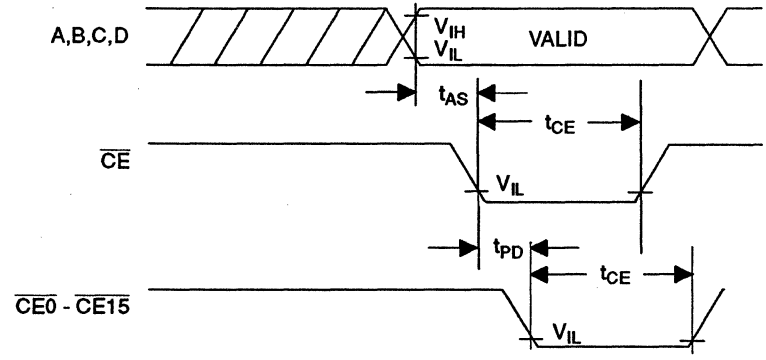
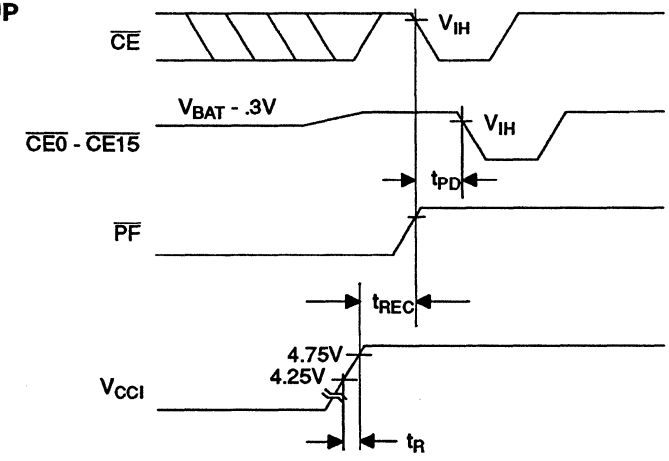
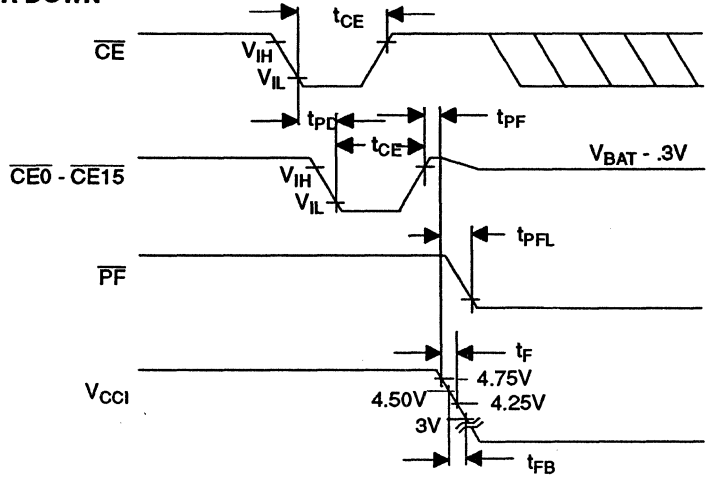
TIMING DIAGRAM - DECODER



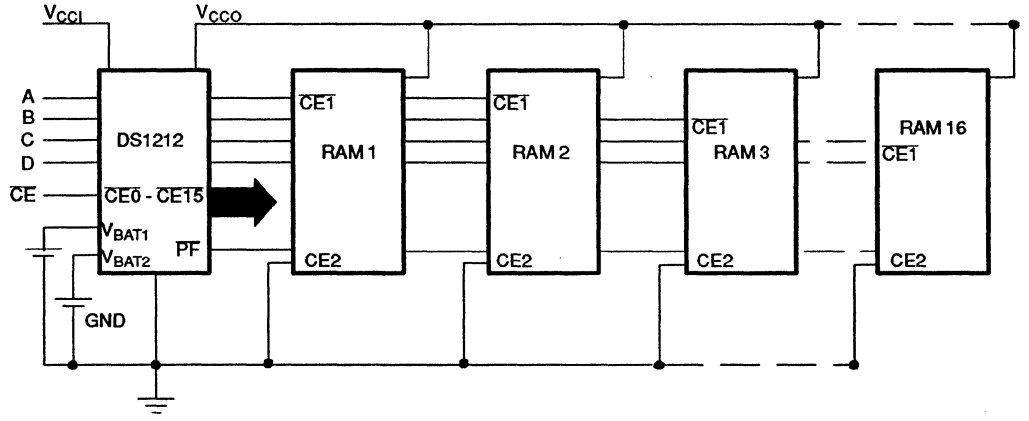
TIMING DIAGRAM - POWER UP



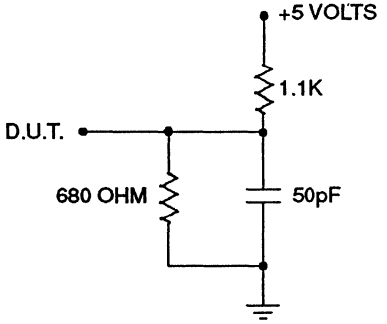
TIMING DIAGRAM - POWER DOWN



TYPICAL APPLICATION Figure 2



OUTPUT LOAD Figure 3



NOTES:

1. All voltages referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$-$\overline{CE15}$ open.
4. I_{CC01} is the maximum average load which the DS1212 can supply to the memories.
5. Measured with a load as shown in Figure 3.
6. I_{CC02} is the maximum average load current which the DS1212 can supply to the memories in the battery back-up mode.
7. Chip enable outputs $\overline{CE0}$-$\overline{CE15}$ can only sustain leakage current in the battery backup mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$-$\overline{CE15}$) will be defined by inputs A through D with a propagation delay of t_{PD} from an A through D input change.
10. For applications where higher currents are required, please see the Battery Manager chip data sheet (DS1259).
11. The DS1212 has a 5K ohm resistor is series with the battery input. As current from the battery increases over 100 µA, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path.

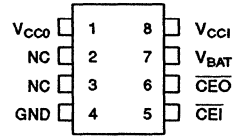
DALLAS SEMICONDUCTOR

DS1218
Nonvolatile Controller

FEATURES

- Converts CMOS RAM into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin mini-DIP/8-pin 150 mil SOIC
- Consumes less than 100 na of battery current

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CCI}	-	Input +5 Volt Supply
V_{CCO}	-	RAM Power (V_{CC}) Supply
$\overline{CEI}$	-	Chip Enable Input
NC	-	No Connection
$\overline{CEO}$	-	Chip Enable Output
V_{BAT}	-	+ Battery
GND	-	Ground

DESCRIPTION

The DS1218 is a CMOS circuit which solves the application problems of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable output is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1218 nonvolatile controller chip with a full CMOS memory and lithium batteries, ten years of nonvolatile RAM operation can be achieved.

OPERATION

The DS1218 Nonvolatile Controller performs the circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or V_{CCI} supply depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1218 constantly monitors the V_{CC} supply. When V_{CCI} falls to 1.26 times the battery voltage a precision comparator outputs a power fail detect signal to the chip enable logic. The third function of write protection is accomplished by holding the chip enable output signal to within 0.2V of the V_{CCI} or battery supply, when a power fail condition is detected.

During nominal supply conditions, the chip enable output will follow chip enable input with a maximum propagation delay of 10 ns.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to 7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

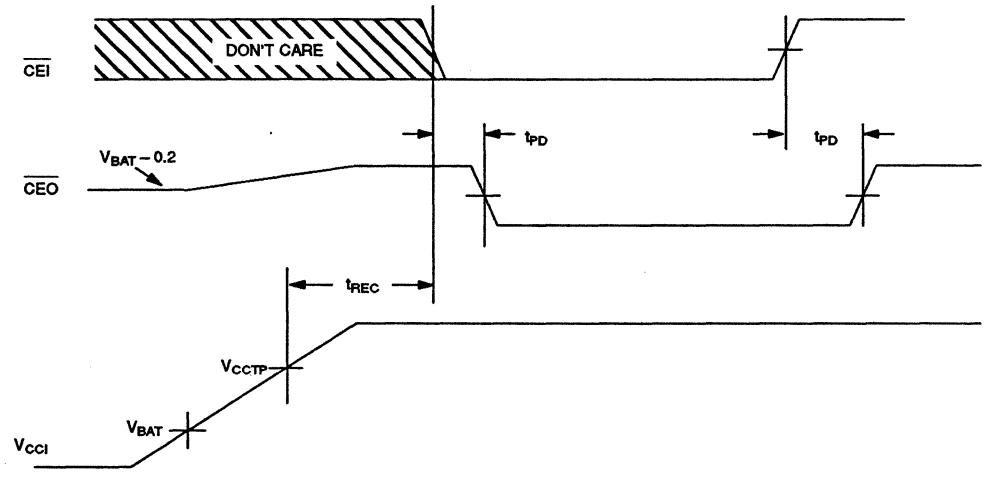
RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		5.5	V	1
Logic 0	V_{IL}	-0.3		0.8	V	1
Battery Supply	V_{BAT}	2.5	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, VCCI = 5V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current	I_{CCI}		2	5	mA	3
Battery Current	I_{BAT}			100	nA	3, 4
RAM Supply	V_{CCO}	V_{CC}-0.2			V	
RAM Current	I_{CCO}			70	mA	5
Input Leakage	I_{IL}	-1.0		1.0	µA	
$\overline{CEO}$ Output @ 2.4V	I_{OH}	-1.0			mA	
$\overline{CEO}$ Output @ 0.4V	I_{OL}			4.0	mA	
V_{CC} Trip Point	V_{CCTP}		1.26XV_{BAT}			

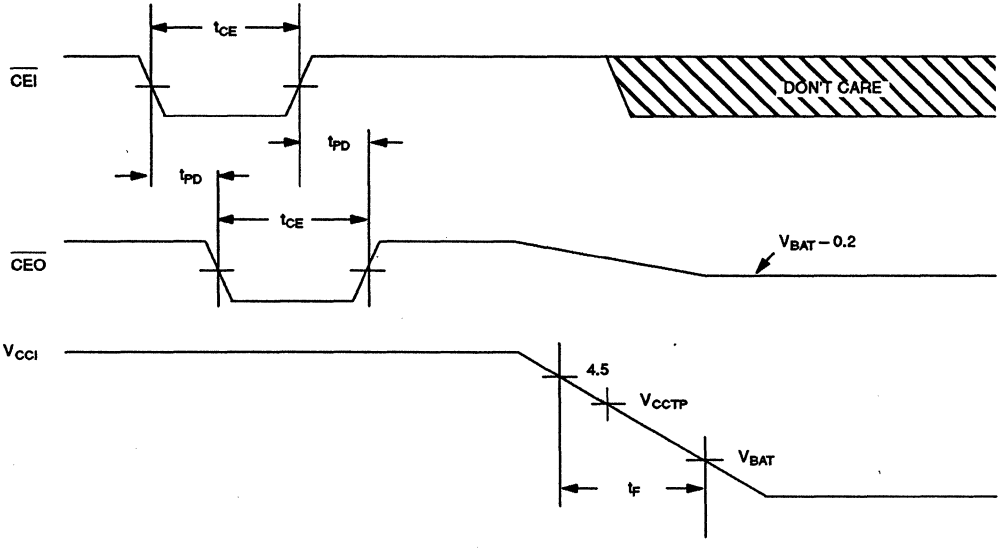
CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC} = 5.0V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}		4	10	ns	2
Recovery at Power Up	t_{REC}	0.2		2	ms	
V_{CC} Slew Rate	t_F	500			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	6, 7

TIMING DIAGRAM: POWER UP



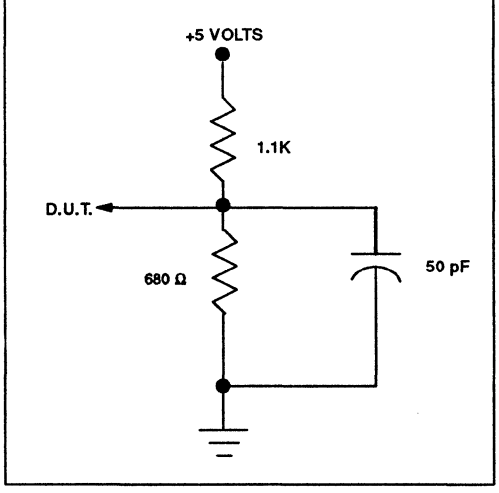
TIMING DIAGRAM: POWER DOWN



NOTES

1. All voltages referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Outputs open
4. Drain from battery when $V_{CC} < V_{BAT}$.
5. Maximum amount of current which can be drawn through pin 1 of the controller.
6. t_{CE} max must be met to ensure data integrity on power loss.
7. $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

FIGURE 1: OUTPUT LOAD



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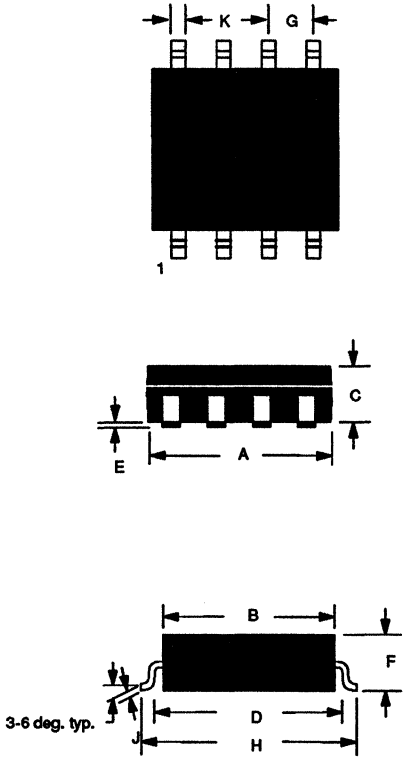
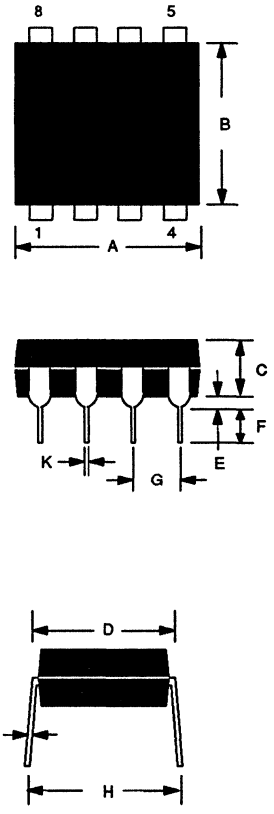
DS1218S NONVOLATILE CONTROLLER 8-PIN 150 MIL SOIC



PKG	8–PIN	
DIM	MIN	MAX
A IN.	0.188	0.195
MM	4.78	4.95
B IN.	0.051	0.157
MM	3.84	3.99
C IN.	0.052	0.061
MM	1.32	1.55
D IN.	0.175	0.193
MM	4.45	4.90
E IN.	0.004	0.010
MM	0.10	0.25
F IN.	0.058	0.068
MM	1.47	1.73
G IN.	0.046	0.054
MM	1.17	1.37
H IN.	0.228	0.244
MM	5.79	6.20
J IN.	0.006	0.011
MM	0.15	0.28
K IN.	0.013	0.019
MM	0.33	0.48

DS1218 NONVOLATILE CONTROLLER 8-PIN 300 MIL DIP



PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN.	0.345	0.400
MM	8.76	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.290	0.310
MM	7.37	7.87
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.110	0.130
MM	2.79	3.30
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.4
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

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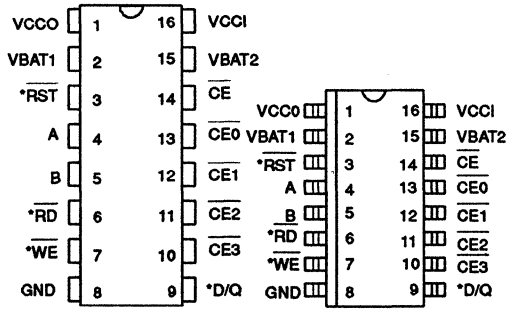
DALLAS SEMICONDUCTOR

DS1221/S
Nonvolatile Controller x 4 Chip

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Data is automatically protected during power loss
- 2-to-4 decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power-up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves PC board space
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C available

PIN ASSIGNMENT



DS1221 16-Pin DIP (300 MIL) See Mech. Drawing Sect. 16, Pg. 1

DS1221 16-Pin SOIC (300 MIL) See Mech. Drawing Sect. 16, Pg. 6

PIN DESCRIPTION

A, B	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE0}$ - $\overline{CE3}$	- Chip Enable Outputs
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
*$\overline{RST}$	- Reset
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
*$\overline{RD}$	- Read Input
*$\overline{WE}$	- Write Input
*D/Q	- Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases.

DESCRIPTION

The DS1221 Nonvolatile Controller x 4 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, nonvolatile operation can be achieved.

CONTROLLER /DECODER OPERATION

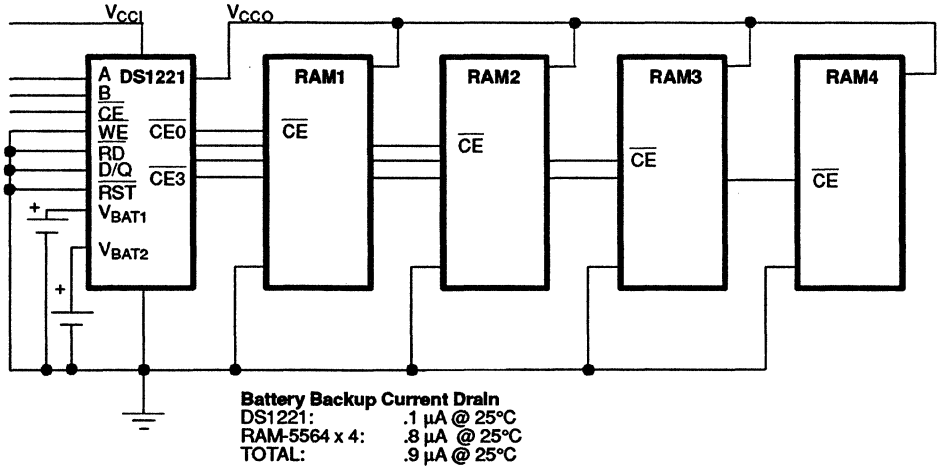
The DS1221 nonvolatile controller performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2-to-4 decoder provides selection of one of four RAMs (see Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller provides is power-fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$ through $\overline{CE3}$) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power-fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2-to-4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery back-up operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

	INPUTS			OUTPUTS			
V_{CCI}	$\overline{CE}$	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
>=4.5	H	X	X	H	H	H	H
< 4.25	X	X	X	H	H	H	H
>=4.5	L	L	L	L	H	H	H
>=4.5	L	L	H	H	L	H	H
>=4.5	L	H	L	H	H	L	H
>=4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

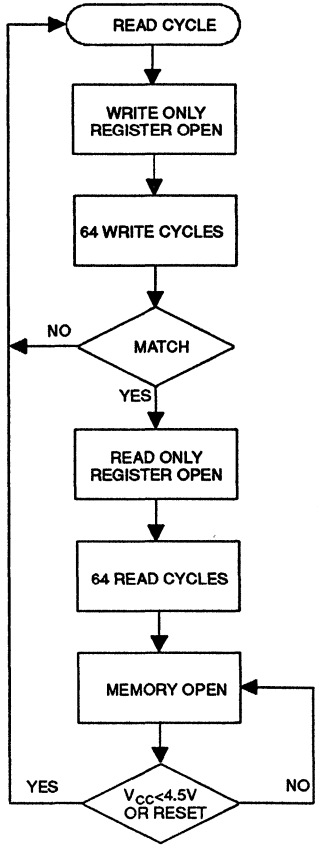
TYPICAL APPLICATION Figure 2



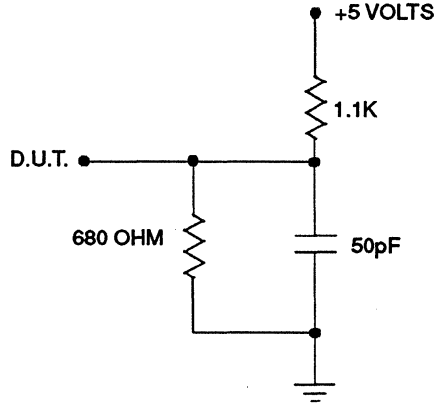
Battery Backup Current Drain

DS1221:	.1 µA @ 25°C
RAM-5564 x 4:	.8 µA @ 25°C
TOTAL:	.9 µA @ 25°C

SECURITY SEQUENCE Figure 3



OUTPUT LOAD Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4, 10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$-$\overline{CE3}$, DQ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$-$\overline{CE3}$, DQ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

(0°C to 70°C, V_{CC}< 4.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$-$\overline{CE3}$ Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	µA	3
Battery Backup Current @ V_{CCO} = V_{BAT} - 0.5V	I_{CCO2}			100	µA	6, 7, 10

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C, V_{CC}< 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			µs	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7, 8

NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE3}$ open.
4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories.
5. Measured with a load as shown in Figure 4.
6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery back-up mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery back-up mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ - $\overline{CE3}$) will be defined by inputs A and B with a propagation delay of t_{PD} from an A or B input change.
10. For applications where higher currents are required, please see the DS1259 Battery Manager Chip data sheet.

SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 3). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead, a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register can be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.

NOTE:
Contact Dallas Semiconductor sales office for code assignments.

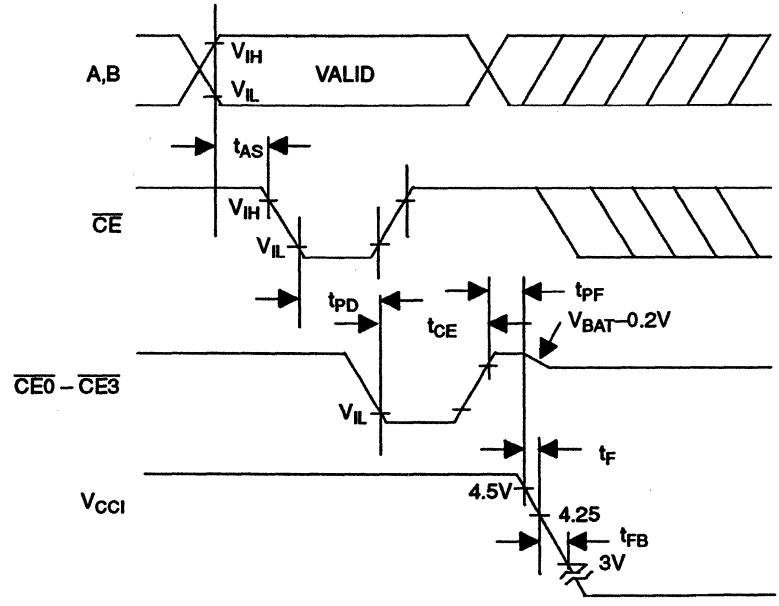
SECURITY OPTION
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

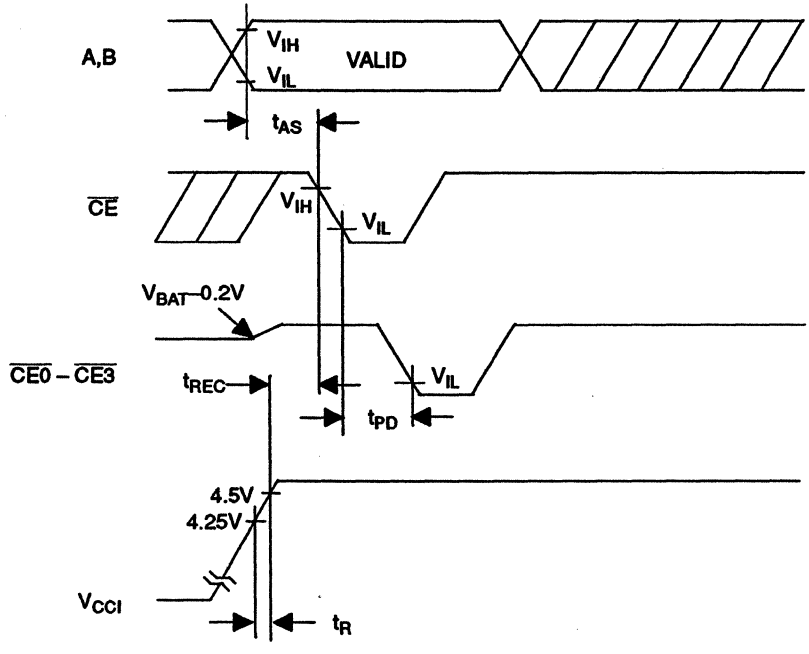
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{RD}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{RD}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			100	ns	
$\overline{RD}$ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	
Data Setup	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	

9

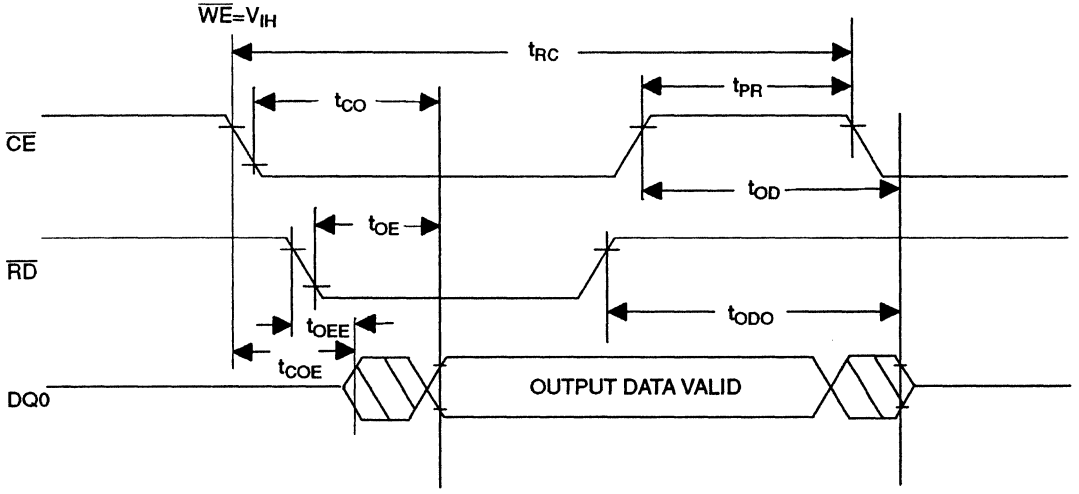
POWER-DOWN Figure 5



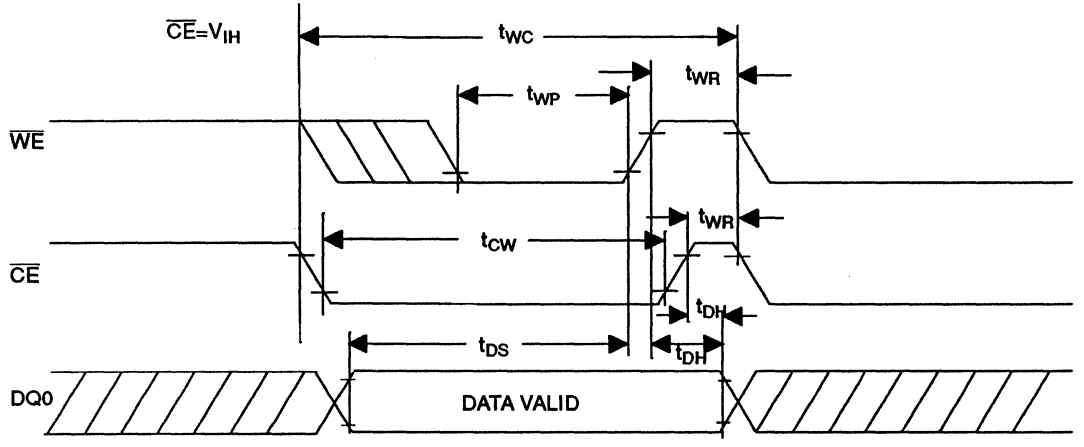
POWER-UP Figure 6



READ CYCLE TO SECURITY OPTION Figure 7



WRITE CYCLE TO SECURITY OPTION Figure 8

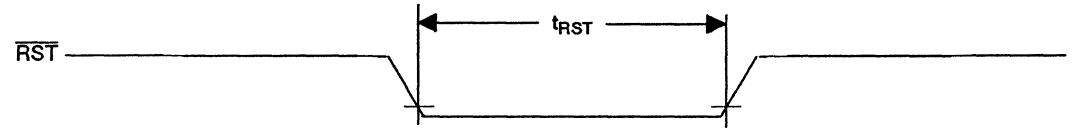


9

NOTES:

1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

RESET FOR SECURITY OPTION Figure 9



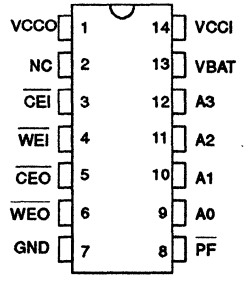
DALLAS SEMICONDUCTOR

DS1234
Conditional Nonvolatile Controller Chip

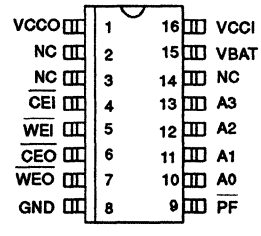
FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software-controlled write inhibit
- Software-controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1234 14-Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



DS1234S 16-Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

V_{CCO}	- RAM Supply
NC	- No Connection
$\overline{CEI}$	- Chip Enable Input
$\overline{WEI}$	- Write Enable Input
$\overline{CEO}$	- Chip Enable Output to RAM
$\overline{WEO}$	- Write Enable Output to RAM
GND	- Ground
$\overline{PF}$	- Power Fail Output
A0-A3	- Address Inputs
V_{BAT}	- Battery Input
V_{CCI}	- +5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit that converts CMOS RAM into nonvolatile memory and adds two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, chip enable and write enable to the RAM are inhibited to accomplish write protection, and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery backup circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery backup is not needed.

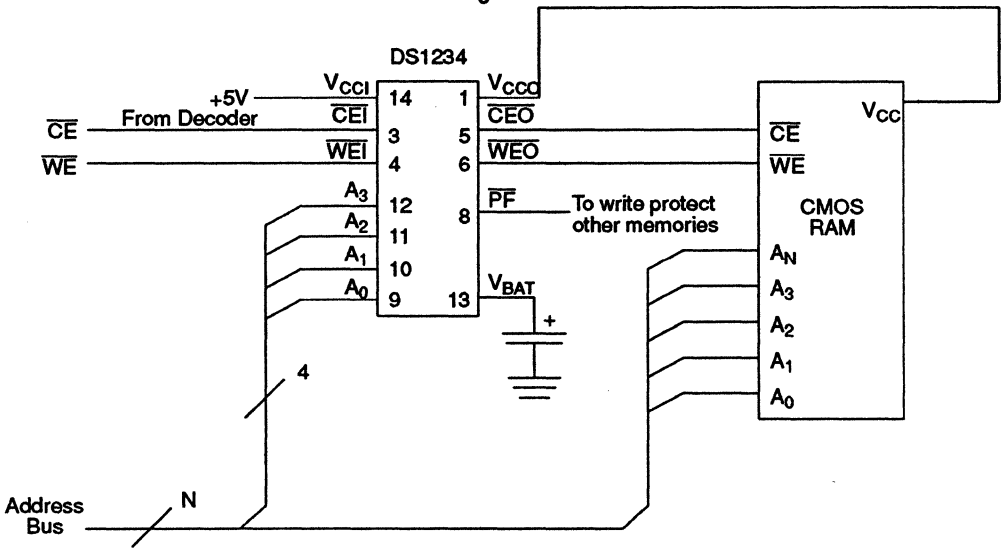
OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out-of-tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the $\overline{CEO}$ and $\overline{WEO}$ output signals to within 0.2 volts of the V_{CCI} or battery supply.

In addition to the nonvolatile controller functions, the DS1234 supplies two software-selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence that will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer of clock zero. Each four-bit compare word is clocked into the DS1234 on the negative edge of $\overline{CEI}$. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven; the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch that inhibits the write enable to the RAM ($\overline{WEO}$). A logic one in this location allows read/write operations so that $\overline{WEO}$ will follow $\overline{WEI}$ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 thorough 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010 activates the nonvolatile controller; data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation.

At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 though 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power, the write enable will be set in read/write operation ($\overline{WEI}$=$\overline{WEO}$).

CONTROLLER TO MEMORY INTERFACE Figure 1



ADDRESS INPUT PATTERN Table 1

	CYCLE NUMBER															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

CONTROL SELECT Table 2

$\overline{WE}$ Battery Control					Operation
11	**12**	**13**	**14**	**15**	
0	X	X	X	X	Read Only Operation
1	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

*Any other combination turns controller off

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.5	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO} = V_{CCI} - 0.2$	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}			4.0	mA	4

(0°C to 70°C; V_{CCI}=< V_{BAT})

$\overline{CEO}$, $\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	6
Battery Current	I_{BAT}			0.1	µA	7
Battery Backup Current @ $V_{CCO} = V_{BAT} - 0.3V$	I_{CCO1}			100	µA	5

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OU}			7	pF	

AC ELECTRICAL CHARACTERISTIC

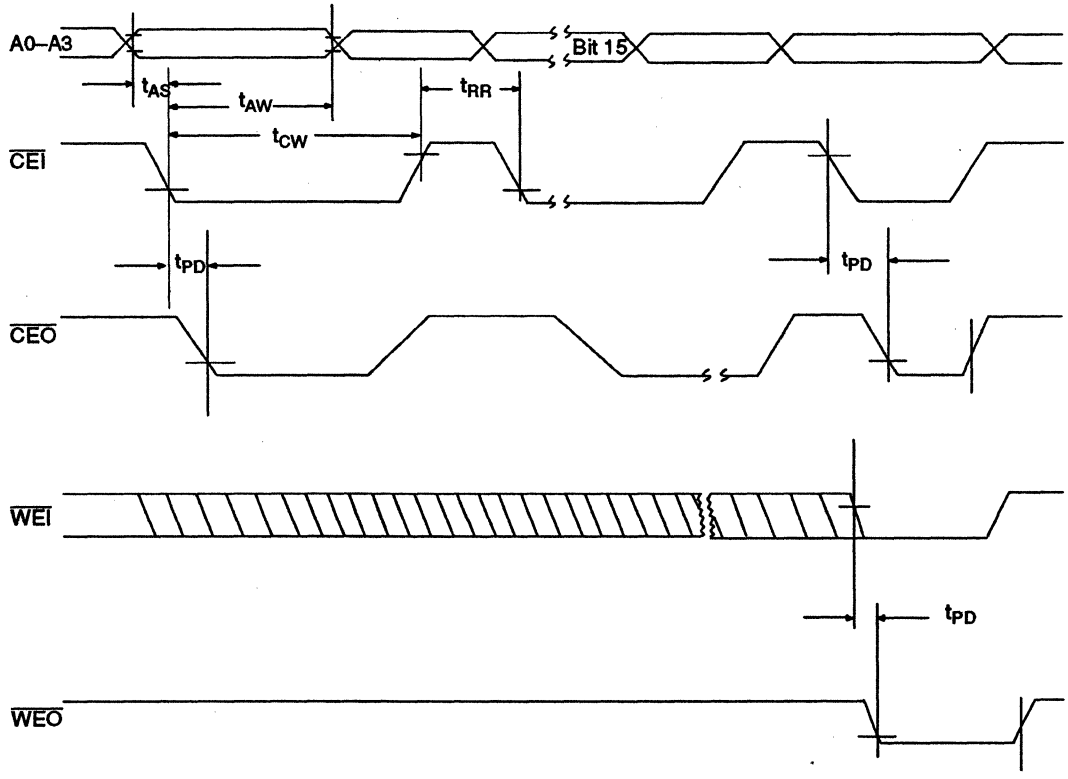
(0°C to 70°C, V_{CCI} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

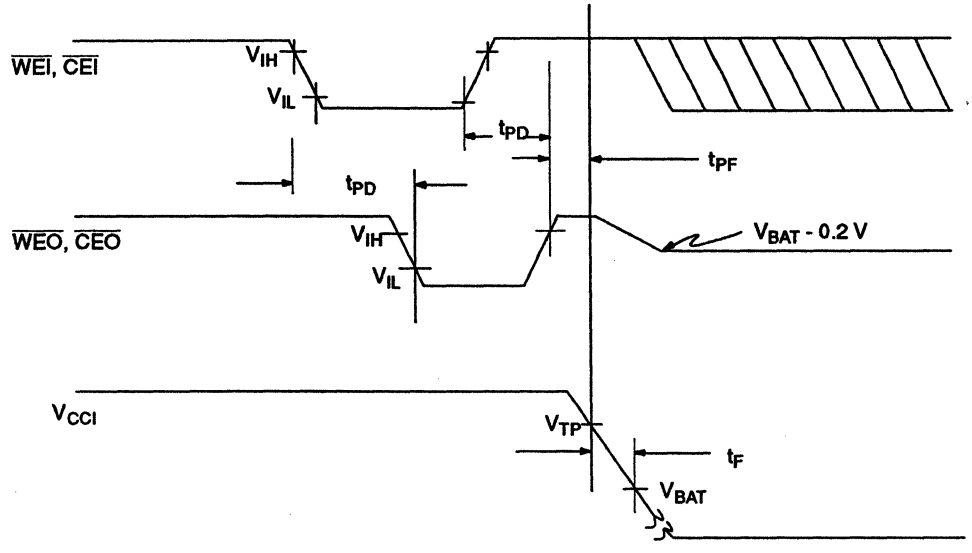
(0°C to 70°C, V_{CCI} < V_{TP})

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_F	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	
$\overline{CEI}$ High to Power Fail	t_{PF}	0			ns	

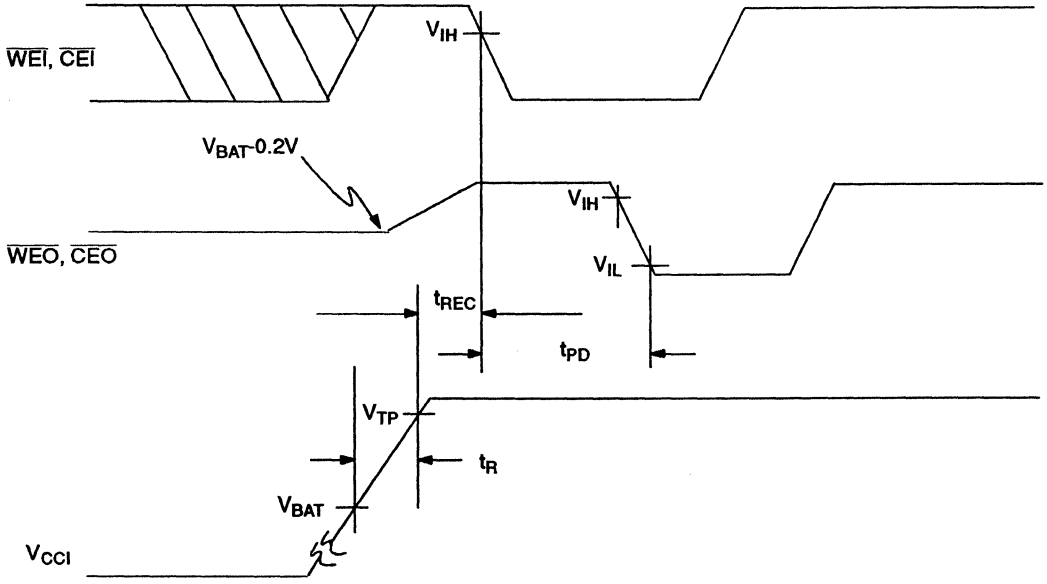
TIMING DIAGRAM-SWITCH SETTING



TIMING DIAGRAM-POWER DOWN



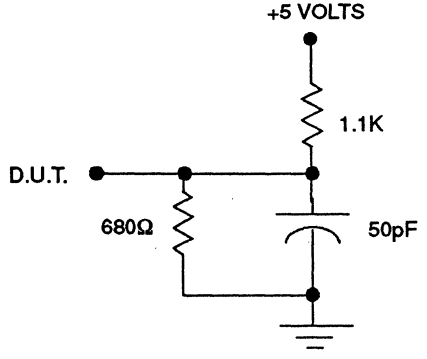
TIMING DIAGRAM-POWER-UP



NOTES:

1. All voltages are referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$ and $\overline{WEO}$ open.
3. I_{CCO} is the maximum average load that the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CCO1} is the maximum average load current that the DS1234 can supply to the memories in the battery backup mode.
6. $\overline{CEO}$ and $\overline{WEO}$, outputs can only sustain leakage current in the battery backup mode.
7. I_{BAT} is the total load current that the DS1234 uses from the battery input pin with V_{CCO}, $\overline{CEO}$, and $\overline{WEO}$ open.

OUTPUT LOAD Figure 2



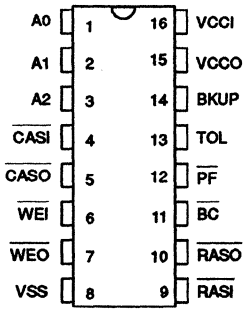
DALLAS SEMICONDUCTOR

DS1237
DRAM Nonvolatizer Chip

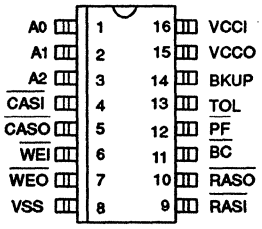
FEATURES

- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power-up under software control
- Space-saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low-power CMOS
- Built-in backup condition circuit warns of impending backup supply failure
- Software-controlled backup supply disconnects switch for storage and shipment
- Software-controlled counter measures backup supply discharge time
- Optional refresh periods of 8 ms, 16 ms, 32 ms, and 64 ms are available to support extended refreshing at reduced power levels

PIN ASSIGNMENT



DS1237 16-Pin DIP
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



DS1237S 16-Pin SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

BKUP	- Backup Supply
$\overline{BC}$	- Backup Condition
TOL	- V_{CCI} Trip Point Select
$\overline{PF}$	- Power Fail Output
A0-A2	- Address Inputs
V_{SS}	- Ground
$\overline{WEI}$	- Write Enable Input
$\overline{WEO}$	- Write Enable Output
$\overline{CASI}$	- $\overline{CAS}$ Input from System
$\overline{CASO}$	- $\overline{CAS}$ Output to DRAM
$\overline{RASI}$	- $\overline{RAS}$ Input from System
$\overline{RASO}$	- $\overline{RAS}$ Output to DRAM
V_{CCO}	- V_{CC} Output to DRAM
V_{CCI}	- +5 Volt Input

DESCRIPTION

The DS1237 DRAM Nonvolatizer Chip is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out-of-tolerance condition. When such a condition occurs, DRAM is isolated from system control and the power supply for the DRAM is switched from V_{CC} to the backup supply. Refresh control is maintained by the DS1237 until the power is within specification. At this time refresh is returned to the system after a highly structured serial sequence on address lines A0, A1, and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply discharging and electrically connect or disconnect the backup supply.

OPERATION – NORMAL POWER CONDITIONS

Under normal operation, system +5 volt power is supplied within the tolerance limits set by pin 13 (TOL). If pin 13 is connected to V_{CCO}, the DS1237 will operate in the normal mode down to 4.75 volts. When pin 13 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs are directly routed to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargeable capacitor or battery; however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output ($\overline{PF}$) is at high level and address inputs A0, A1, and A2 are monitored for software-driven sequences. The backup condition output $\overline{BC}$ will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts on V_{CCI} and the backup counter has not reached zero.

OPERATION – POWER LOSS AND DATA RETENTION

When the 5-volt V_{CC} power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 13, a power fail signal will be generated as V_{CCI} falls below 4.75 volts or 4.5 volts. At this time, the DS1237 enters a data retention mode provided that the backup supply is enabled. The power fail output signal will remain low until V_{CCI} is restored to normal conditions. While entering the data retention mode, the DS1237 isolates all control inputs and starts driving the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ outputs. In addition, if $\overline{RAS}$ = 1, the DS1237 immediately takes control and issues the first refresh burst 62.5 µs later. If $\overline{RAS}$ = 0, the DS1237 will wait for $\overline{RAS}$ to go to a logic 1 level and then take control and issue the first refresh burst 62.5 µs later. If $\overline{RAS}$ = 0 and remains low for more than 10 µs after Power Fail Detect, the DS1237 will take control and drive $\overline{RASO}$ = 1, then issue the first refresh burst 62.5 µs later. The V_{CCI} input is disconnected from V_{CCO} and the regulated backup supply is connected. A burst $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles, depending on the dash number of the device (see Table 1). After the burst refresh is complete, subsequent burst refreshing continues at 8, 16, 32, or 64 ms intervals until V_{CCI} returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The $\overline{WE}$ output is held at the high (inactive) level from the time control is taken by the DS1237 until the system assumes refresh duties. If the DS1237 enters a power loss condition without the backup supply enabled, no refresh activity occurs and data stored into connected DRAMs is lost.

OPERATION – RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds the level determined by the TOL pin, the V_{CCI} input is immediately reconnected to the V_{CCO} output pin while the regulated backup supply is internally disconnected from V_{CCO}. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software-controlled switch is set by sending a specific pattern on address lines A0, A1, and A2 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked, LSB first, into the DS1237 on the falling edge of $\overline{CAS}$ provided that setup and hold times are met. When the 24th cycle is correctly entered, the DS1237 will issue a final refresh burst and then return control to the host system. At this point, the host system will be responsible for handling all refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

ACTIVATION OF BACKUP SUPPLY

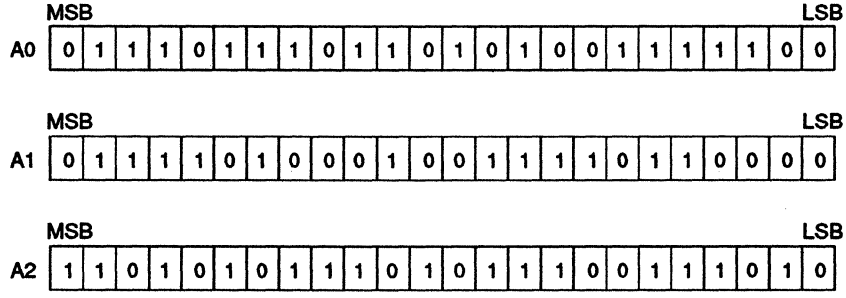
A software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. On the initial connection of the battery, the backup supply switch will be off. Under this condition, no refresh activity will occur when V_{CCI} is out of tolerance. The bit patterns presented in Figure 2 show how the backup supply can be activated or deactivated under software control.

REFRESH INTERVALS Table 1

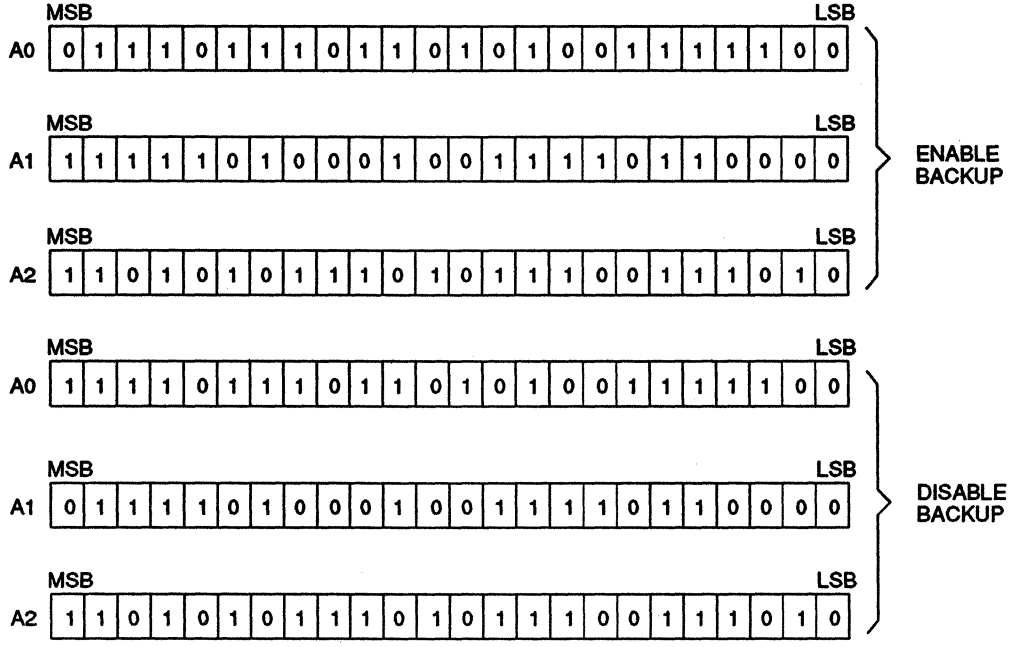
	REFRESH INTERVAL (ms)*			
NUMBER OF CYCLES	8	16	32	64
256K DRAM: 520	-1	-2	-3	-4
1 Meg DRAM: 1032	-5	-6	-7	-8

*Refresh intervals have a tolerance of ±12.5%.

SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER-UP Figure 1



SOFTWARE CONTROLLED SWITCH FOR ACTIVATION OF BACKUP SUPPLY Figure 2



BATTERY CONDITION

The DS1237 has two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V_{CCI}, the backup condition output pin ($\overline{BC}$) is driven to the active state (low) and will remain in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is supplying power, the $\overline{BC}$ pin remains at a logic 0 state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one-second intervals whenever the backup supply is supplying power. This counter is set with a number while V_{CCI} is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1, and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when the $\overline{CASI}$ line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the $\overline{BC}$ pin will be low even though the V_{CCI} supply is within nominal limits. The $\overline{BC}$ pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in ampere hours of the backup supply by the average load current of the DRAMs and converting this value into seconds (see Figure 5). The value in the counter can be read at any time while V_{CCI} is within nominal limits by sending the 24-bit sequence shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 $\overline{CASI}$ cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the $\overline{BC}$ pin. A logic 0 on $\overline{BC}$ while $\overline{CAS}$ is low is a logic 0 for that bit.

BACKUP CONDITION APPLICATIONS

The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the V_{CC} comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargeable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

NOTE:

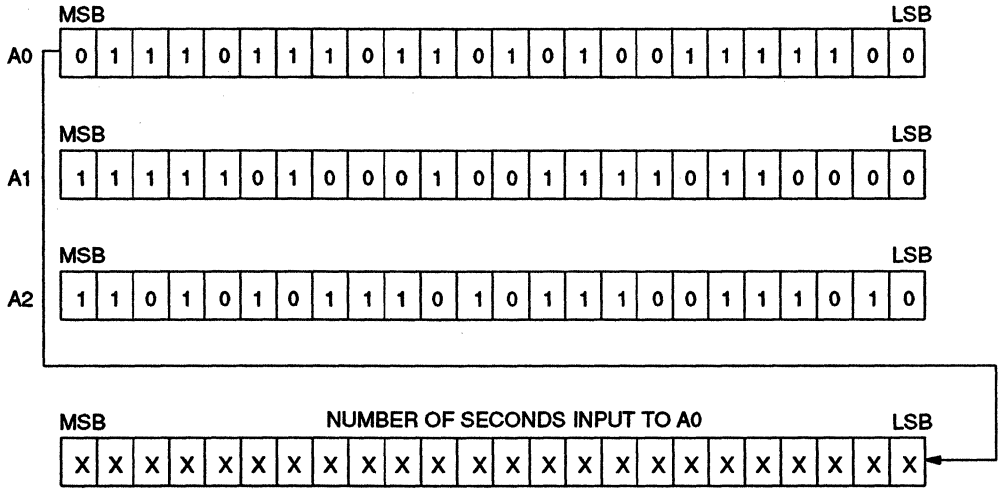
The DS1237 requires capacitive bypassing techniques between V_{CCO} and GND for proper operation. A bypass capacitor between V_{CCI} and BKUP is also essential for proper operation. While applications vary, a 10 µF capacitor value is typically required.

DATA RETENTION TIMES

The equations in Figure 5 are used to find the data retention time of DRAMs using the DS1237 DRAM Nonvolatizer Chip.

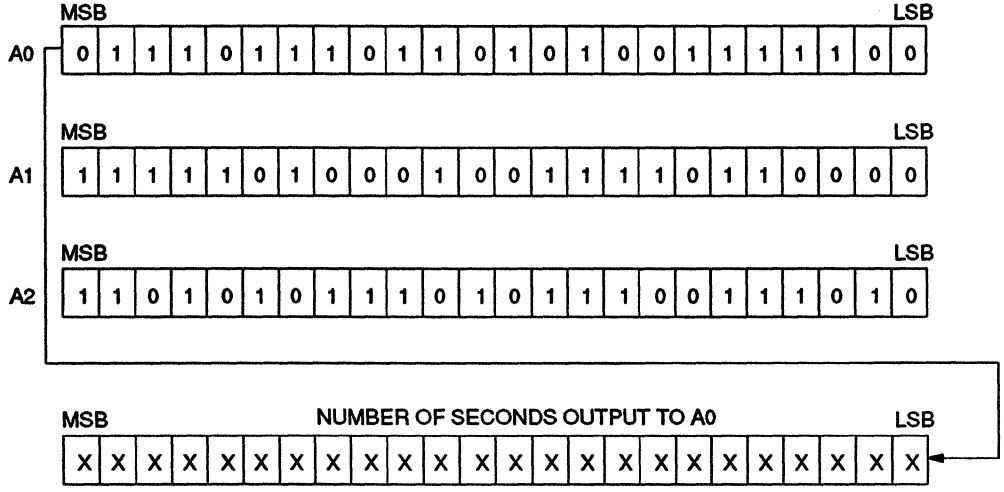
Calculating the actual current consumption of the DRAMs requires special attention since they are placed into the standby mode and then activated only when refreshing is required. This means that the current consumption of the DRAMs will be an average of the standby current and the active currents weighted in proportion to the refresh cycle time and duration.

SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER Figure 3



NOTE:
The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of 2^{24} seconds with an accuracy of ±20%.

SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER Figure 4



DS1237 NONVOLATIZER DRAM DATA RETENTION TIMES Figure 5

$I_{datareten}$ = (# of DRAMs) X [(I_{act} + I_{std}) / 8E–3] + 4 mA

where,

I_{act} = 520 X 350E–9 X I_{active}

520 (burst) => number of refresh cycles

350E–9 => access cycle time of DRAM, and

I_{active} => active current draw of DRAM

I_{std} = (8E–3 – (520 X 350E–9)) X $I_{standby}$

8E–3 => refresh period

520 (burst) => number of refresh cycles

350E–9 => access cycle time of DRAM, and

$I_{standby}$ => standby current draw of DRAM

The foregoing equations can then be used to directly calculate the data retention time:

$$t_{datareten} = Q_{bat} / I_{datareten}$$

ABSOLUTE MAXIMUM RATINGS *

Voltage on Battery Input Pin Relative To Ground	-0.3V to +12V
Voltage on any Other Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3V	V	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Backup Supply	BKUP	6.0V	8.0V	10.0	V	2,3

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.50V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-2.0			mA	1,5
Output Current @ 0.4 V	I_{OL}	+8.0			mA	1,5
Input Supply Current	I_{CCI}		3	7	mA	6
Output Supply Current V_{CCO}=V_{CCI} -0.2 V	I_{CCO}			200	mA	4
$\overline{PF}$ Detect TOL = V_{CCO}	V_{TP}	4.5	4.62	4.75	V	7
$\overline{PF}$ Detect TOL = GND	V_{TP}	4.25	4.37	4.5	V	7
Output Supply Current V_{CCI} < V_{TP}	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUP}			1	µA	9

CAPACITANCE

($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	7		pF	

AC ELECTRICAL CHARACTERISTICS – RAPID REFRESH

(0°C to 70°C, $V_{CCI} < V_{TP}$)

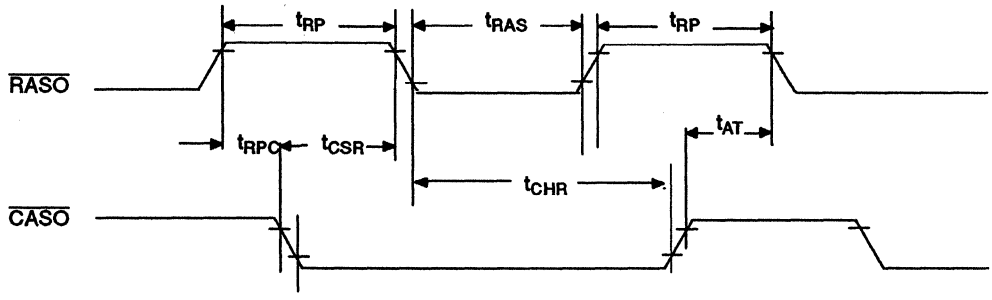
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RASO}$ Precharge Time	t_{RP}	90			ns	
$\overline{RASO}$ Precharge to $\overline{CASO}$ Hold Time	t_{RPC}	60			ns	
$\overline{CASO}$ Setup Time	t_{CSR}	30			ns	
$\overline{CASO}$ Hold Time	t_{CHR}	60			ns	
$\overline{RASO}$ Pulse Width	t_{RAS}	0.120		10	µs	
Elapsed Time Between Rapid Refresh Burst	t_{AT}	SEE TABLE 1			ms	

AC ELECTRICAL CHARACTERISTICS

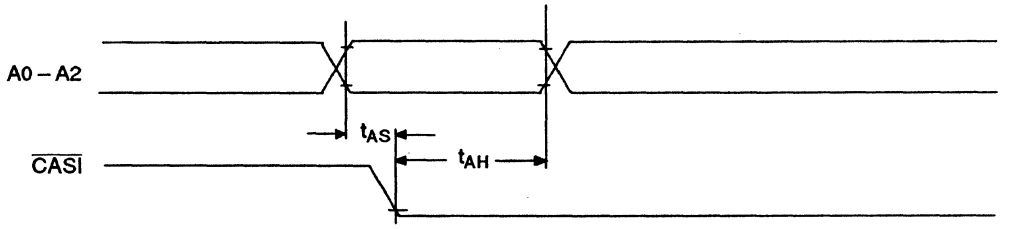
(0°C to 70°C, $V_{CCI} > V_{TP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	
Propagation Delay	t_{PD}		7	15	ns	

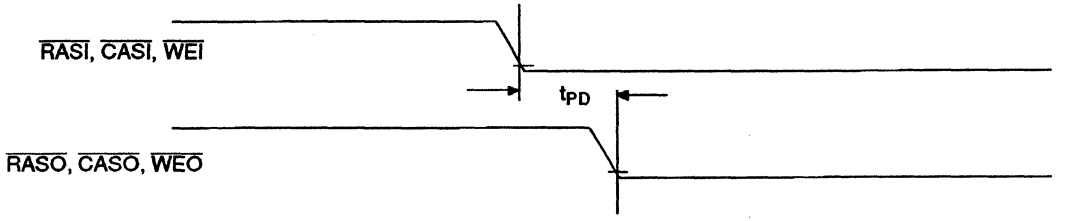
REFRESH CYCLE DURING BURST REFRESH RETENTION ($\overline{WEO}=V_{IH}$) Figure 6



SOFTWARE SEQUENCE ENTRY ($\overline{WEI}$=V_{IH}) Figure 7



PROPAGATION DELAY - NORMAL OPERATION Figure 8



9

NOTES

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS1237 such that V_{CCO} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 300 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnect V_{CCI} and connect the internally regulated backup supply to V_{CCO}. Rapid refresh is also initiated at this time, and the $\overline{PF}$ output is driven active.
8. I_{CCOB} is the maximum current the DS1237 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage is the internal current consumed by the DS1237 in the data retention mode, with battery backup disabled.

APPLICATION NOTE: DIODE CONTROL OF BACKUP INPUT

The fabrication of the DS1237 produces an N well for the BKUP input (pin 14) that must be considered by the user. Because of this it is imperative that the BKUP input does not go more negative from V_{CCI} input (pin 16) than the amount of one silicon diode.

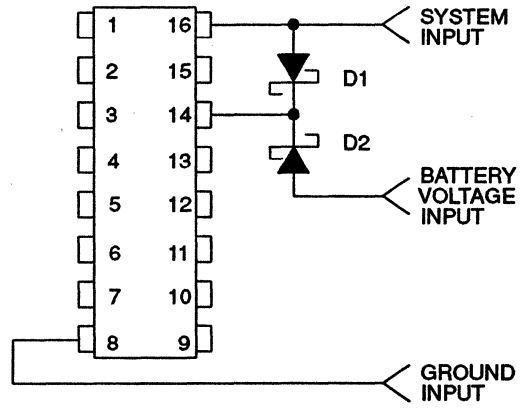
This requirement can be achieved by using a Schottky diode (D1) between the V_{CCI} input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V_{CCI}.

A Shottky diode is required for D1.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V_{CCI} input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive supply lead from the BKUP input when the battery output voltage has decreased.

A Shottky diode is suggested for D2.



NOTE: For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.

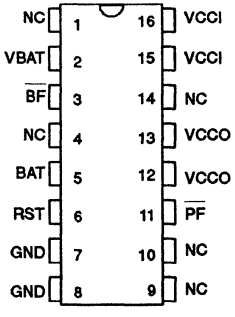
DALLAS SEMICONDUCTOR

DS1259
Battery Manager Chip

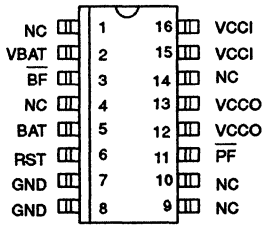
FEATURES

- Facilitates uninterruptible power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16–Pin DIP Package
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



16–Pin SOIC Package
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

NC	- No Connection
V_{BAT}	- Battery Input Connection
$\overline{BF}$	- Battery Fail Output Signal
BAT	- Battery Output
RST	- Reset Input
GND	- Ground
$\overline{PF}$	- Power Fail Output Signal
V_{CCO}	- RAM Supply
V_{CCI}	- +5V Supply

9

DESCRIPTION

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

OPERATION

During normal operation, V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 12 and 13) through an internal switch at a voltage level of V_{CCI}-0.2 volts at 250 mA. During this time the power fail signal ($\overline{PF}$) is held high, indicating valid V_{CCI} voltage (see Figure 1). However, if the V_{CCI} falls below the trip point (V_{TP}), a level of 1.26 times the battery level (V_{BAT}), the power fail signal is driven low. As V_{CCI} falls below the battery level, power is switched from V_{CCI} to V_{BAT} and the battery supplies power to the uninterruptible output (V_{CCO}) at V_{BAT}-0.2 volts at 15 mA.

On power-up, as the V_{CCI} supply rises above the battery, the primary energy source, V_{CCI}, becomes the supply. As V_{CCI} rises above the trip point (V_{TP}), the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level regardless of the level of V_{CCI}.

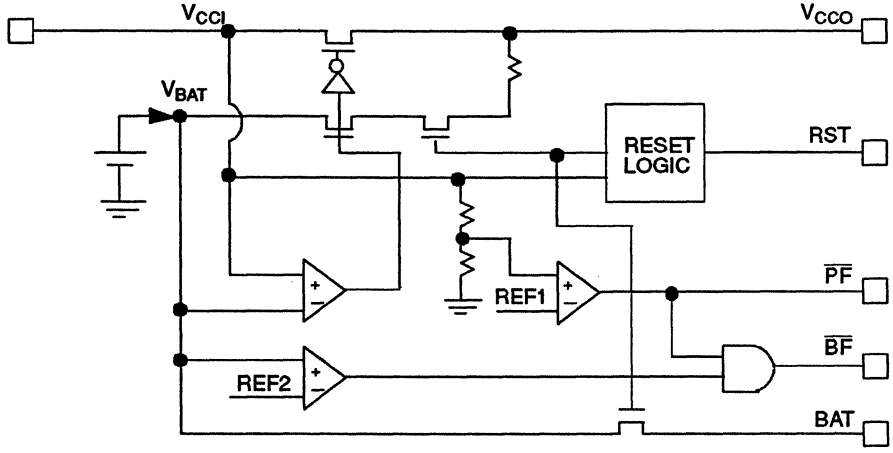
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level provided that the attached battery (V_{BAT}) is greater than 2 volts. If the battery level should decrease to below 2 volts, the $\overline{BF}$ signal is driven low, indicating a low battery. The $\overline{BF}$ signal is always low when the $\overline{PF}$ signal is low.

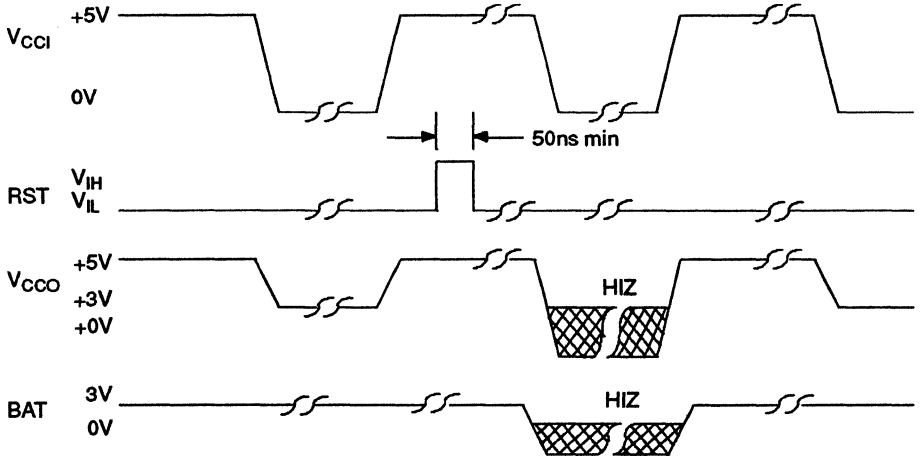
RESET

The reset input can be used to prevent the battery from supplying power to V_{CCO} and BAT even if V_{CCI} falls below the level of the battery. This feature is activated by applying a pulsed input on RST to high level for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the battery or V_{CCI}. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

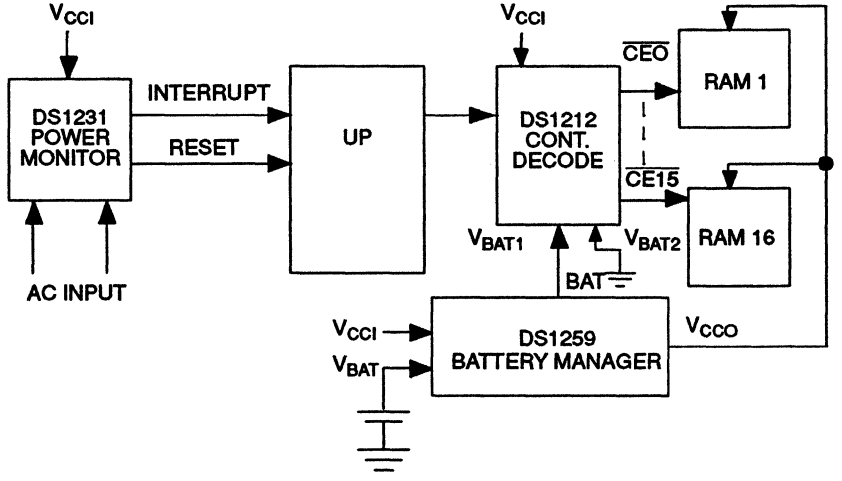
BLOCK DIAGRAM Figure 1



RESET TIMING Figure 2



TYPICAL APPLICATION Figure 3



9

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 Sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage Pin 2	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	V_{BAT}- 0.1			V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+250	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}	(1.26xV_{BAT}) -250mV	(1.26xV_{BAT}) +250mV		V	4,6
Pin 3 $\overline{BF}$ Detect	V_{BATF}	1.5	2.0	2.6	V	7

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8
Pin 5 Battery Output Current	I_{BATOUT}			100	µA	

CAPACITANCE

(t_A = 25°C)

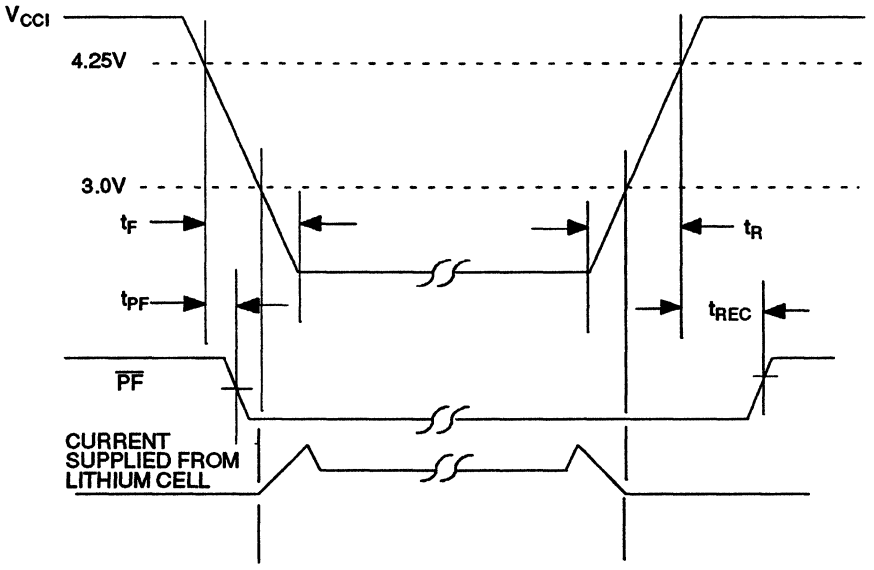
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power-Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power-Up	t_{REC}			100	µs	9

POWER-DOWN/POWER-UP CONDITION



NOTES:

1. All voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. I_{CCO2} may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   $V_{TP} = 1.26 \times V_{BAT} \pm 250$ mV
   For 5% operation: V_{BAT} = 3.7V max.
   For 10% operation: V_{BAT} = 3.5 V max.
7. V_{BATF} is the point that $\overline{BF}$ is driven low. These limits are for 0°C to 70°C operation.
8. Battery leakage is the internal energy consumed by the DS1259.
9. V_{CC} = +5 volts, t_A = 25°C.

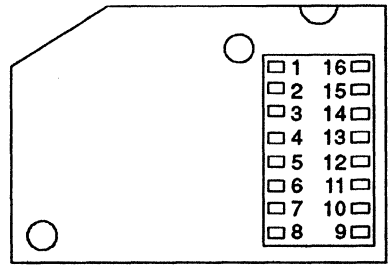
DALLAS SEMICONDUCTOR

DS1260
Smart Battery

FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 mAH @ 3 volts
- Plugs into a standard 16-pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation ensures full capacity after shipping and handling
- Lithium cell automatically reconnects when V_{CC} is applied
- Recessed pins prevent bending
- V_{CC} fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5-inch printed circuit board centers
- Mates directly with DS1212 Nonvolatile Controller to back up 16 SRAMs
- Uninterruptible supply for CMOS and portable devices

PIN ASSIGNMENT



See Mech. Drawing – Sect. 16, Pg. 20

PIN DESCRIPTION

Pins 1, 2, 4, 7, 9, 10, and 14 are No-Connects
Pin 3 is Battery Fail ($\overline{BF}$)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST) Input
Pin 8 is Ground
Pin 11 is Power Fail ($\overline{PF}$)
Pins 12 and 13 are RAM Supply (V_{CCO})
Pins 15 and 16 are +5V Supply (V_{CCI})

DESCRIPTION

The DS1260 SmartBattery is a low-cost, backup energy supply for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic (RESET) circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin, low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

OPERATION

During normal operation V_{CCI} (pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (pins 12 and 13) through an internal switch at a voltage level of V_{CCI} -0.2 volts @ 250 mA. During this time the power fail signal ($\overline{PF}$) is held high, indicating valid primary voltage (see Figure 1). However, if the V_{CCI} falls below the level of 4.25 volts, the power fail signal is driven low. As V_{CCI} falls below the level of the lithium supply (V_{BAT} = 3 volts), power is switched and the lithium energy source supplies power to the uninterruptible output (V_{CCO}) at V_{BAT} -0.2 volts @ 5 mA.

On power-up, as the V_{CCI} supply rises above 3 volts, the primary energy source, V_{CCI}, becomes the supply. As the V_{CCI} input rises above 4.25 volts, the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of V_{CCI}.

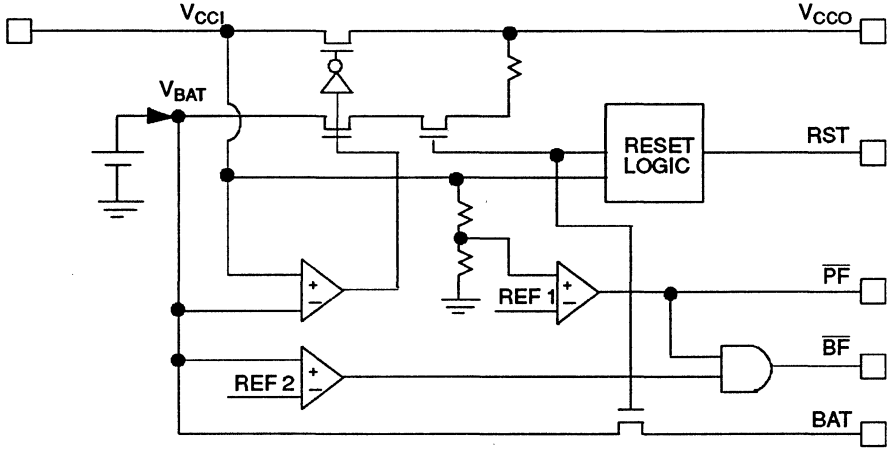
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level (V_{OH}) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the $\overline{BF}$ signal is driven low (V_{OL}), indicating an exhausted lithium battery. The $\overline{BF}$ signal is always low when power is being supplied by the lithium energy source.

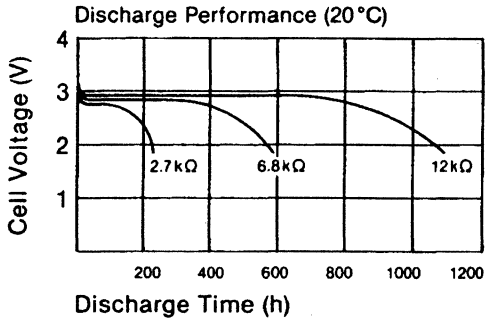
RESET

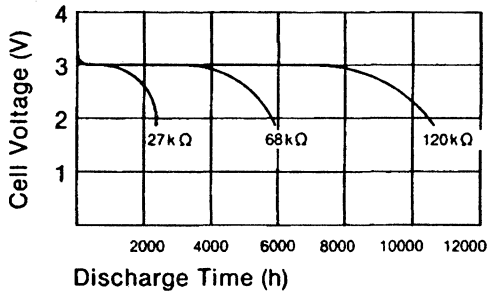
The reset input can be used to prevent the lithium energy source from supplying power to V_{CCO} and BAT even if V_{CCI} falls below 3 volts. This feature is activated by applying a pulsed input on RST to a high level (V_{IH}) for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the lithium energy source when V_{CCI} again falls below 3 volts. BAT will also return to the level V_{BAT}. Figure 3 shows how the SmartBattery is used in a system application.

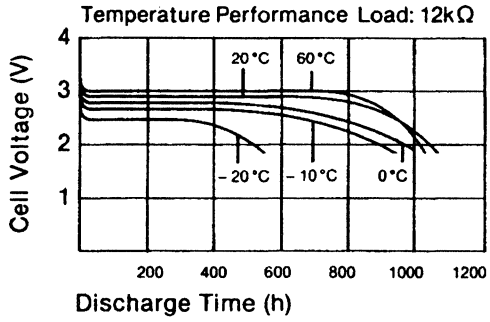
BLOCK DIAGRAM Figure 1

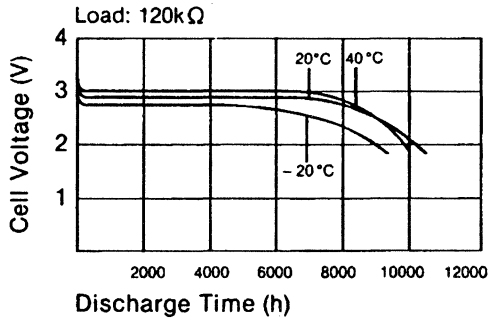


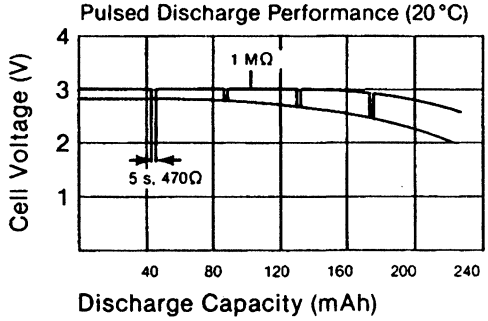
BATTERY PERFORMANCE DS1260-25



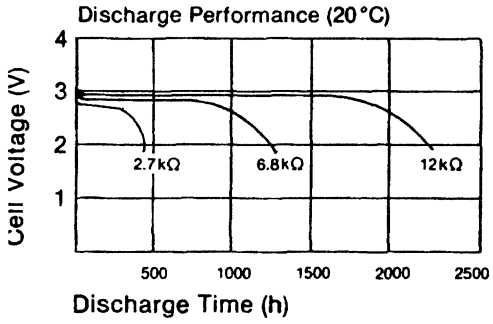


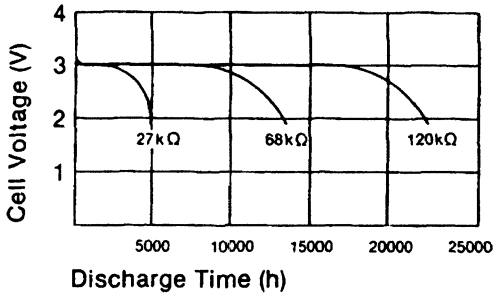


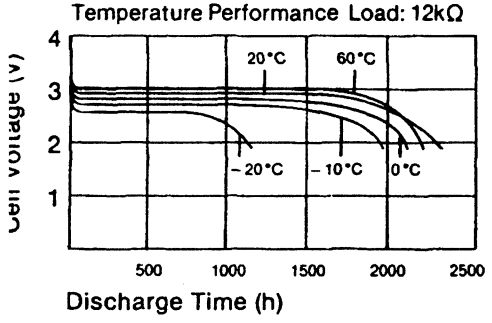


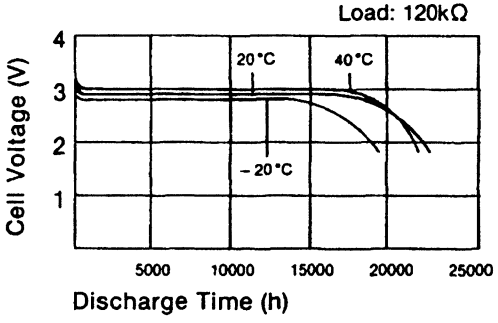


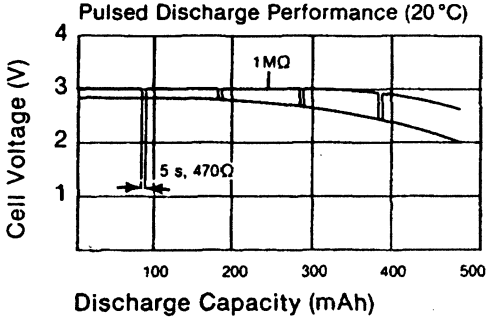
BATTERY PERFORMANCE DS1260-50



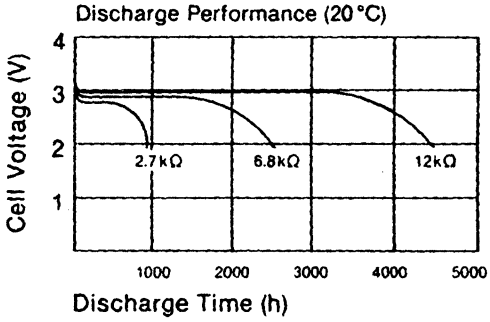


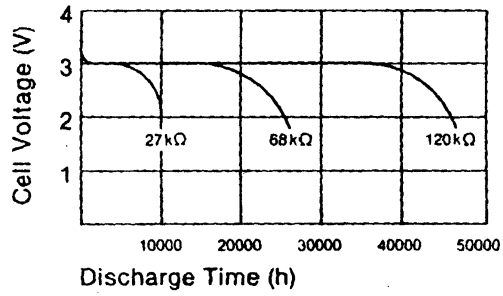


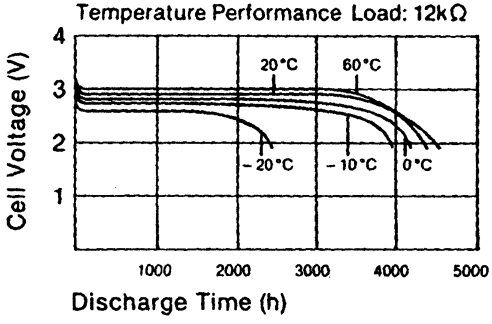


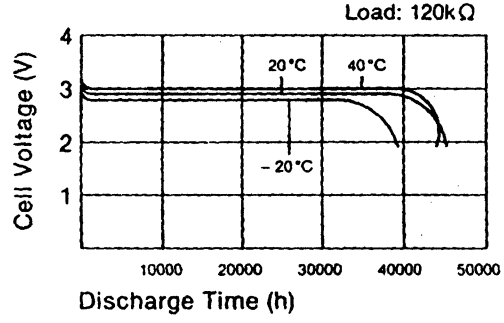


BATTERY PERFORMANCE DS1260-100









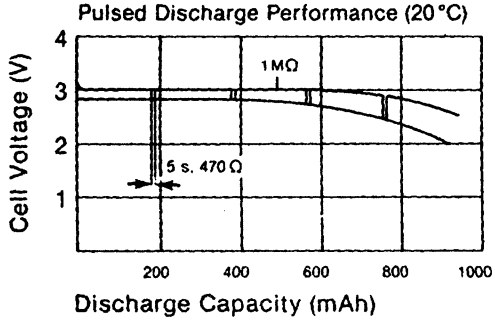
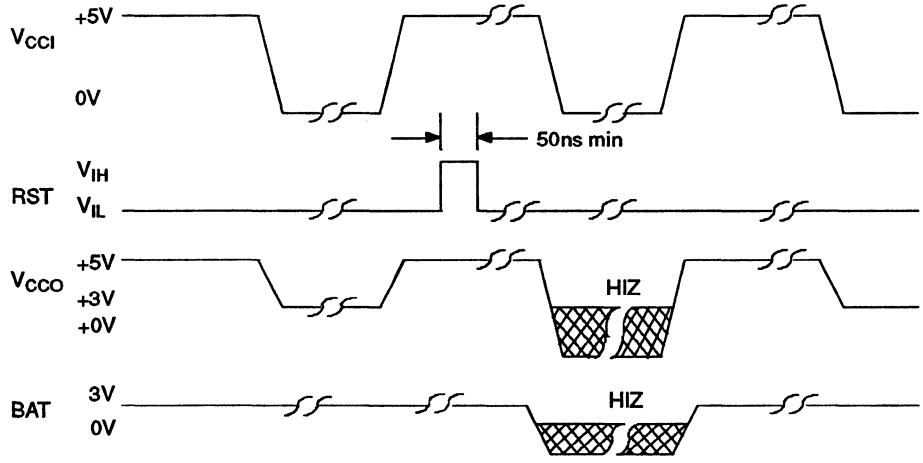


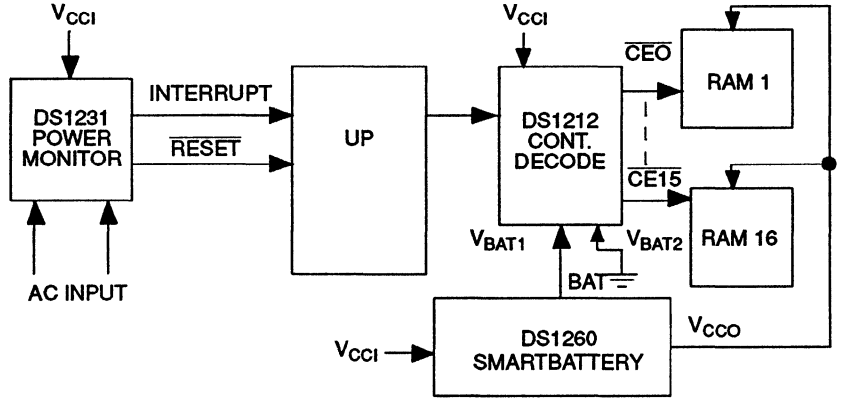
Table 1

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 mAH	3 volts
DS1260-50	480 mAH	3 volts
DS1260-100	960 mAH	3 volts

RESET TIMING Figure 2



INTEGRATED BATTERY BACKUP – APPLICATIONS Figure 3



9

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CCI}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			5	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}		4.25	4.5	V	4
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C; $V_{CCI} < V_{BAT}$)

Pin 5 Battery Voltage	V_{BAT}		3		V	6
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8, 9
Pin 5 Battery Output Current	I_{BATOUT}			100	µA	

CAPACITANCE

(t_A = 25°C)

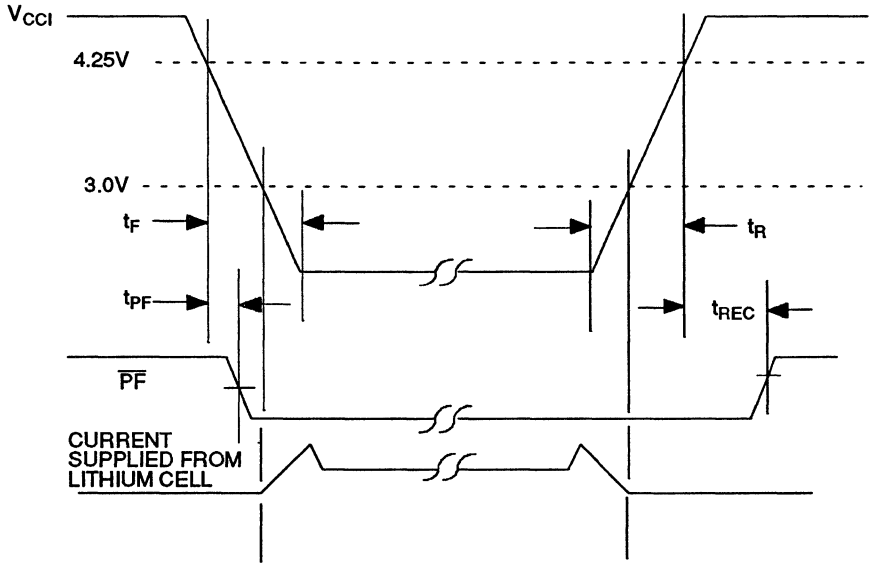
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O		5	10	pF	
Input Capacitance	C_I		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power-Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power-Up	t_{REC}			100	µs	

POWER-DOWN/POWER-UP CONDITION



WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. Sustained I_{CCO2} currents above 1 mA cause a significant drop in battery voltage.
6. V_{BAT} is the internal lithium energy source voltage.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at $25°C$.
10. V_{CCI} = +5 volts; $t_A = 25°C$.

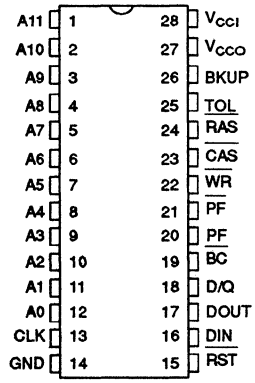
DALLAS SEMICONDUCTOR

DS1262
Serial DRAM Nonvolatizer Chip

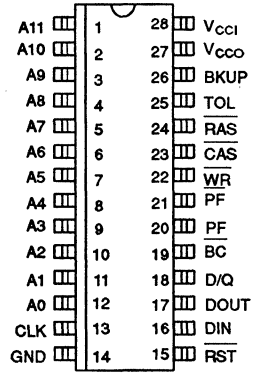
FEATURES

- Provides 3-wire serial access to DRAM
- Converts DRAM into nonvolatile memory using external backup supply
- Addresses up to 16Mx1 of memory
- Data can be read from or written to DRAM via single or multi-bit transfers
- Onboard delay line generates precise DRAM timing signals
- Automatic CAS-before-RAS refresh in active and data retention modes
- Gas gauge for backup supply warns of impending data retention failure
- Selectable refresh periods: 4, 8,16, or 32 ms
- Power fail detection signals provide hardware interrupt to host
- Backup supply range of 6 to 10 volts
- Power fail detect at 5% and 10% of V_{CC}
- 28-pin DIP and SOIC (DS1262S) packages available

PIN ASSIGNMENT



28-PIN DIP (600 MIL)
See Mech. Drawing
Sect. 16, Pg. 4



28-PIN SOIC (330 MIL)
See Mech. Drawing
Sect. 16, Pg. 7

PIN DESCRIPTION

A0 – A11	– Address Outputs to DRAM
DIN	– Data In from DRAM
DOUT	– Data Out to DRAM
$\overline{WR}$	– Write Signal to DRAM
$\overline{RAS}$	– Row Address Strobe for DRAM
$\overline{CAS}$	– Column Address Strobe for DRAM
V_{CCI}	– +5V Primary Supply
V_{CCO}	– V_{CC} Output for DRAM
CLK	– Serial Clock Input
$\overline{RST}$	– Serial Reset Input
D/Q	– Serial Port Data I/O
BKUP	– Backup Supply Input
TOL	– 5% or 10% V_{CC} Supply Select
$\overline{BC}$	– Backup Supply Condition Pin
PF, $\overline{PF}$	– Power Fail Signals
GND	– Ground

DESCRIPTION

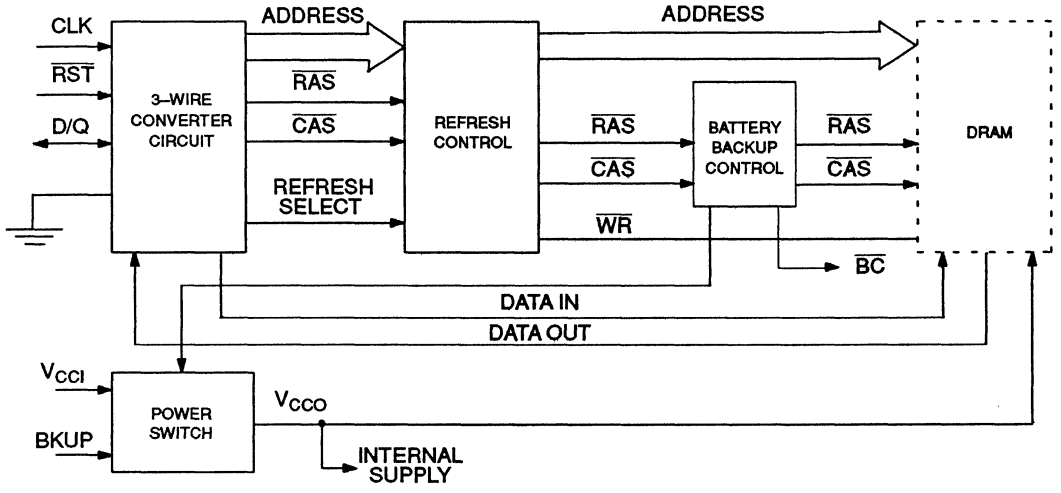
The DS1262 Serial DRAM Nonvolatizer Chip enables read/write access of DRAM from a simple 3-wire serial port. Refresh and RAS/CAS timing for the DRAM is performed automatically, transparent to the operation of the serial port. In addition, the DS1262 performs all of the power switching and refresh duties necessary to retain DRAM data when the primary power supply fails. The backup supply input accepts a wide voltage range, suitable for use with rechargeable batteries. The DS1262 also provides an electronic "gas gauge" which can predict the condition of the backup supply. It can be used with DRAM densities of 256Kx1 to 16Mx1.

OPERATION – SERIAL PORT INTERFACE

The main elements of the DS1262 are shown in Figure 1. Three signals control sending or retrieval of data using the 3-wire converter circuit. The signals CLK, $\overline{RST}$, and D/Q comprise a 3-wire serial port. To transfer data into the DS1262, $\overline{RST}$ is first driven high while CLK is low. After sufficient setup time from $\overline{RST}$, one bit of data is placed onto the D/Q line. With valid data on D/Q the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred into the 3- wire converter. Since the serial port can only accept data one bit at a time, address information must always be sent first to inform the 3-wire converter of the destination of the data that will follow. Address information is always entered starting with the least significant bit of the logical address field and ending with the most significant bit of the address field. Twenty-four address bits are always written to the 3-wire converter regardless of the RAM being used (Figure 2).

After the 24-bit address field is sent, an 8-bit function code is written to instruct the 3-wire converter of the action to be taken on data that will follow. The function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from the DRAM or the control registers within the battery backup control unit. Function codes that control the backup supply or refresh period cause further data transfer to terminate until $\overline{RST}$ is driven low and then high again to begin a new cycle. Data is always written in the same manner as the address and function code information. Data is read by driving the clock low while $\overline{RST}$ is high. Data becomes valid on the D/Q line after sufficient time is allowed for access. The read cycle is terminated when $\overline{RST}$ is returned low.

DS1262 BLOCK DIAGRAM Figure 1



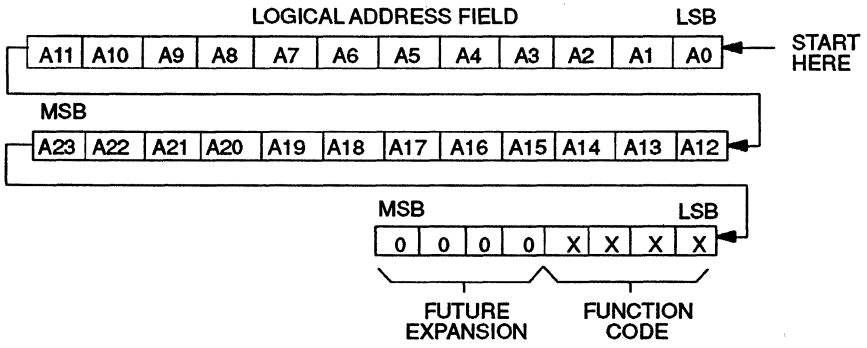
DRAM REFRESH CONTROL

Refresh cycles are always sent to the attached DRAM, regardless of activity on the serial port. When a proper DRAM read/write access code has been entered at the serial port, a normal DRAM read/write cycle will be interlaced with the refresh burst cycles. When V_{CCI} goes to an out-of-tolerance condition (see "DC Electrical Specifications" for details), the DS1262 sends out 258 refresh cycles for each refresh period as selected by the user (4, 8, 16, or 32 msec). The 258 refresh cycles occur at a 500 ns rate for about 129 µsec. All refresh cycles are the CAS-before-RAS type and are sufficiently long to meet the refresh requirements of most DRAM densities. After the refresh burst, the DS1262 remains quiet for the remainder of the refresh period to conserve power, except for DRAM read/write cycles initiated by the serial port.

BURST MODE

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. While low density DRAMs do not require the entire 24-bit address field, 24 bits must be always entered; unused upper address bits should always be the same value (0's are recommended). The DS1262 will always produce the appropriate RAS and CAS address. Burst mode is terminated when $\overline{RST}$ is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers.

SERIAL PORT PROTOCOL Figure 2



FUNCTION CODES Table 1

FUNCTION NAME	FUNCTION CODE (HEX)
BURST READ DRAM DATA	00
READ DRAM DATA	01
READ BKUP COUNTER	02
WRITE BKUP COUNTER	03
REFRESH PERIOD=4MSEC	04
REFRESH PERIOD=8MSEC	05
REFRESH PERIOD=16MSEC	06
REFRESH PERIOD=32MSEC	07
BACKUP SUPPLY ENABLED	0C
BACKUP SUPPLY DISABLED	0D
WRITE DRAM DATA	0E
BURST WRITE DRAM DATA	0F,FF

DRAM TIMING - READ CYCLE

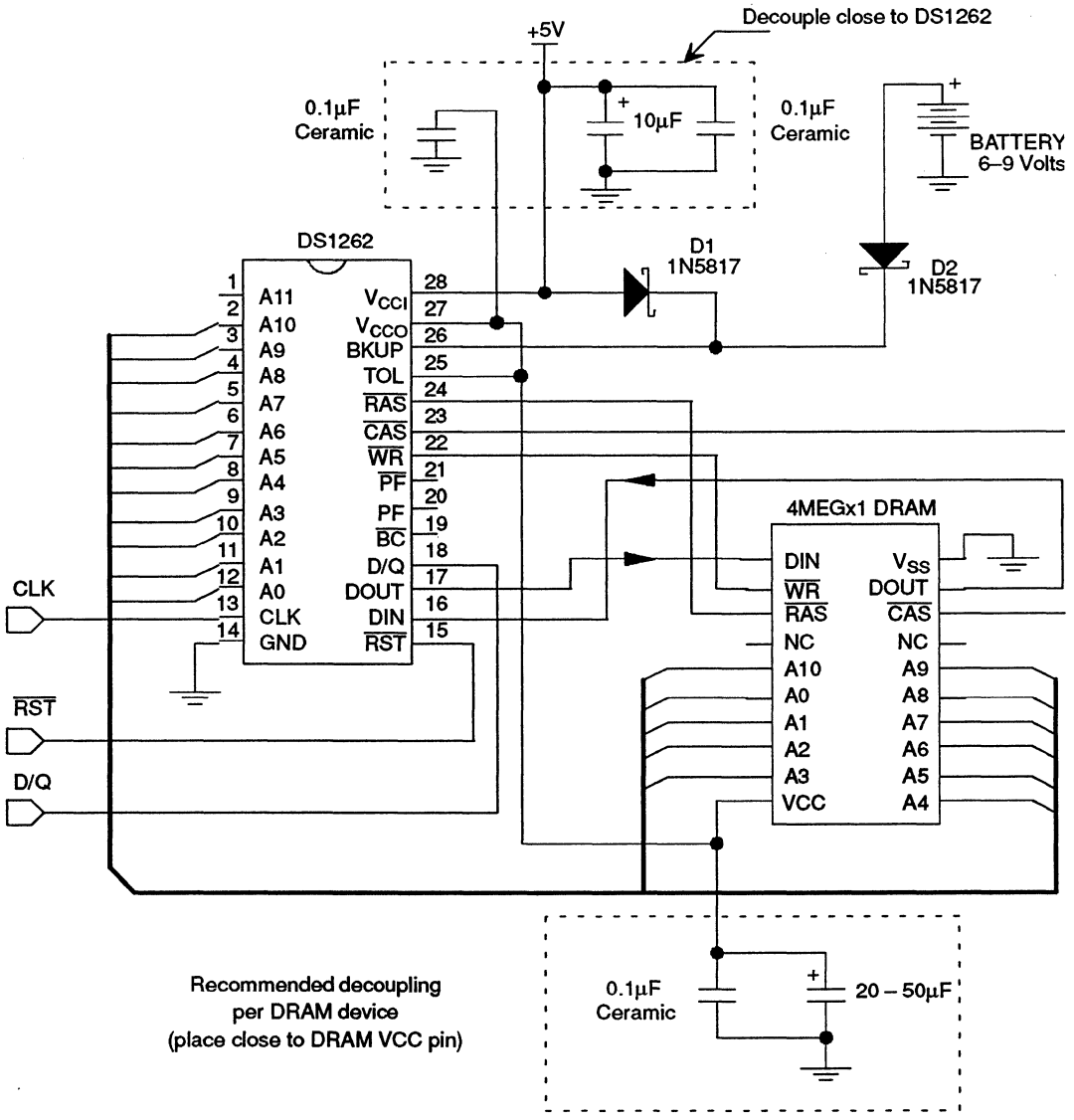
A read cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the $\overline{RAS}$ signal is asserted low and the row addresses are latched into the DRAM. Next the column addresses are asserted valid and after setup time the column address strobe ($\overline{CAS}$) goes active, latching the column address. The $\overline{CAS}$ strobe will stay low for a sufficient time for valid data to be output and received from the DRAM at the DIN pin. The cycle is terminated when both RAS and CAS are returned high. The $\overline{WR}$ signal is always high during the read cycle (see timing diagrams at the back of this data sheet). Unused upper address output pins should always be left unconnected.

DRAM TIMING - WRITE CYCLE

A write cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the $\overline{RAS}$ signal is asserted low and the row addresses are latched into the DRAM. At the same time, valid data is placed on the data output pin (DOUT). Next the $\overline{WRITE}$ signal is asserted low. At the same time, the column address is asserted valid on the address bus. After setup time, the $\overline{CAS}$ is asserted low.

All signals ($\overline{RAS}$, $\overline{CAS}$, A0-A11, $\overline{WR}$, and DOUT) remain active and valid until the write cycle is complete. The cycle is terminated when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WR}$ are returned back high and the data out pin (DOUT) returns to a high impedance state.

DS1262 APPLICATION CIRCUIT WITH 4MX1 DRAM Figure 3



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NOTES:

1. BKUP input must not be allowed to go 0.7 volts more negative than V_{CCI}; otherwise an internal silicon diode in the DS1262 will short V_{CCI} to ground. D1 clamps BKUP so that it can only go 0.3 volts below V_{CCI}.
2. D2 prevents reverse-charging of battery and may be required for UL approval if battery source is the primary source for the user's system.
3. The decoupling capacitors attached to the DRAM V_{CC} input(s) are required because of the switching noise of the regulated V_{CCO} supply from the DS1262. Also, this capacitance satisfies fast rise-time current demands of the DRAM.

OPERATION – POWER LOSS AND DATA RETENTION

When the 5-volt V_{CCI} power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V_{CCI} falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF,$\overline{PF}$) are driven active at this time and will remain active until V_{CCI} is restored to a normal condition. When the data retention mode begins, the DS1262 isolates the 3-wire serial port, drives the address outputs low, and starts driving $\overline{RAS}$, $\overline{CAS}$, and the $\overline{WR}$ outputs. If an active DRAM read/write cycle is in progress when power loss occurs, the DS1262 will complete this cycle properly before isolating the 3-wire serial port ($\overline{RST}$, CLK, D/Q). The V_{CCI} input is then disconnected from the V_{CCO} output and the backup supply connected to the BKUP pin is switched in. The BKUP input is normally connected to either a rechargeable battery or super capacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be tied to the V_{CCI} pin; do not tie this pin low when not using the battery-backup function.

After power loss, a burst CAS-before-RAS refresh cycle is generated at a cycle time of 500 ns. This burst refresh continues for 258 cycles. After the burst refresh is complete, subsequent refreshing continues at intervals determined by the refresh period function code written.

BATTERY GAS GAUGE

The DS1262 contains two features that provide information about the condition of the backup supply. First, the DS1262 monitors the backup supply input condition. If this input is below V_{CCI} the backup condition output pin ($\overline{BC}$) is driven active low and remains in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is providing power, the $\overline{BC}$ pin remains in a high impedance state.

The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while V_{CCI} is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field, followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field followed by the correct function code. Information in the address field is automatically entered into the battery condition counter when $\overline{RST}$ is brought low to end the cycle. The battery condition counter value can only be entered when V_{CCI} is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V_{CCI} is within normal limits. No other action will take place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the $\overline{BC}$ pin will be driven low as soon as V_{CCI} is within normal limits. The $\overline{BC}$ pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

CONSERVATION OF THE BACKUP SUPPLY

Two other function codes are used to control a switch that allows conservation of the backup supply when data retention is not required. The switch is set on or off by entering any value in the address field followed by the function code for turning off or on the backup supply. The bit patterns are shown in Table 1. The backup supply switch can only be set when V_{CCI} is within normal limits. No other action will take place when using these function codes.

REFRESH PERIOD FUNCTION CODES

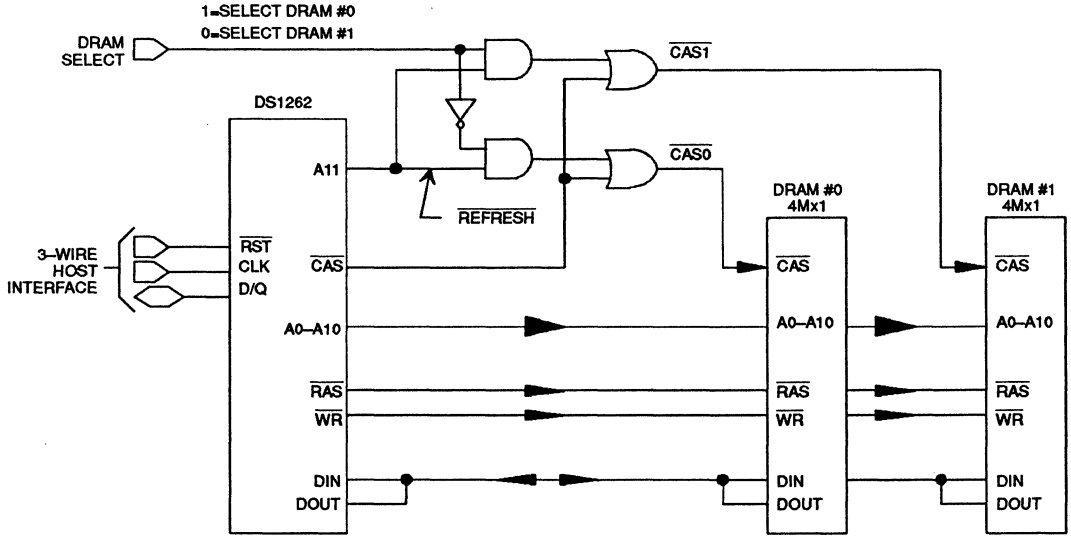
Four function codes are used to set the refresh period for the attached DRAM; all refresh periods contain 258 cycles. As such, most DRAMs will use 256 cycles per 4 msec refresh regardless of the density of the RAM attached. For example, a 1Mx1 DRAM requires 512 cycles in 8 ms while a 4Mx1 DRAM requires 1024 cycles in a 16 ms period. Both devices are satisfied using a 4 msec refresh period since a 4Mx1 DRAM is satisfied in 4

refresh periods (4 x 256 = 1024). However, extended refresh periods can be used in cases where DRAMS have been screened and tested for longer data retention between refresh bursts.

Whenever a function code is written to select the refresh period, the logic address field is ignored by the serial port and can be set to any value; however, all 24 address bits must be entered. Function codes other than proper DRAM read /write codes do not cause any data to be written to the attached DRAM; the $\overline{RST}$ pin must be reset low and then brought high to access the DRAM data after entering these codes. Data sent through the serial port after one of these functions codes is sent will be ignored until $\overline{RST}$ is driven low and then high again to begin a new cycle.

Function codes for backup supply control or refresh control need only be written once after the BKUP supply is attached. The BKUP supply will preserve these codes as long it remains within specified limits.

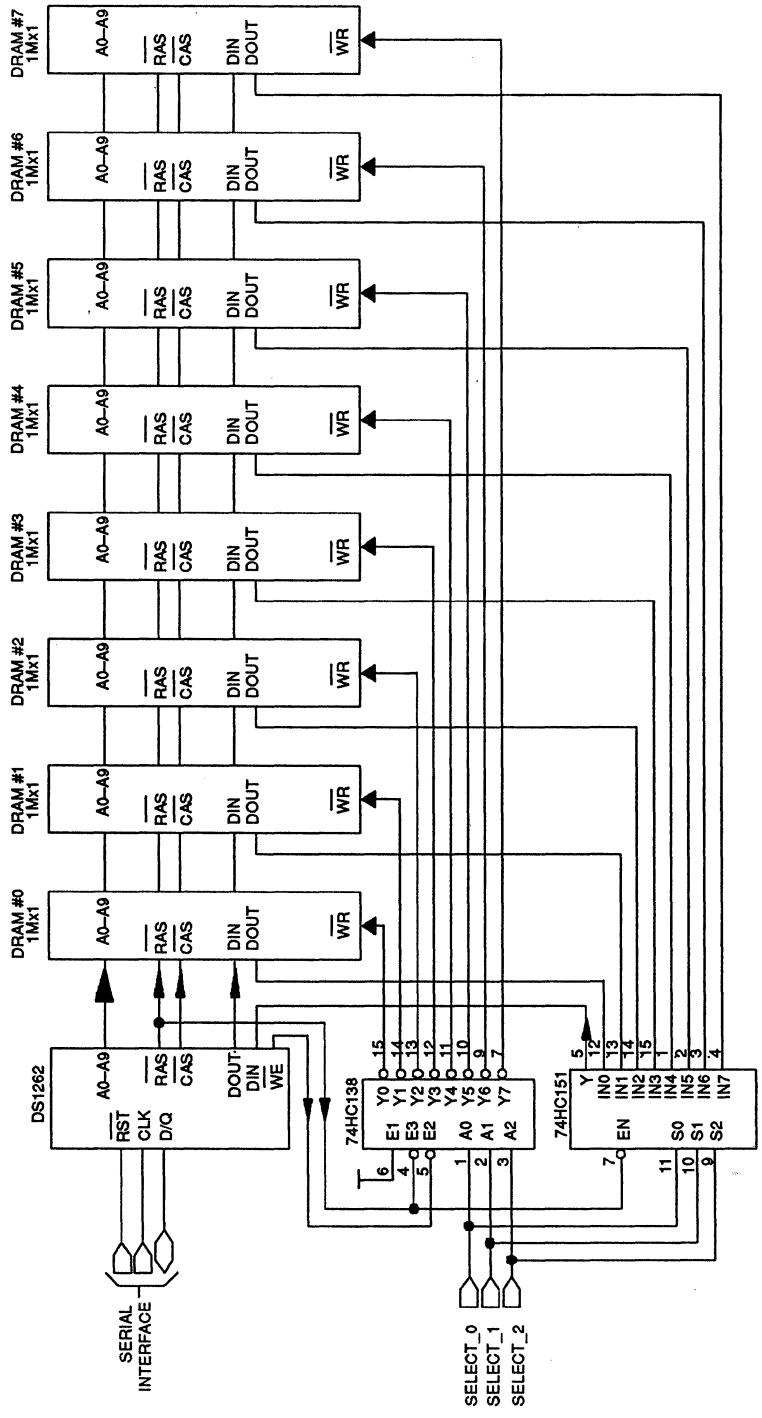
BANK SELECT SCHEME FOR TWO 4MX1 DRAMS Figure 4



NOTES:

1. In this application, the A11 address output serves as a refresh indicator, going low whenever the DS1262 is in a refresh cycle. During refresh cycles, all address outputs are forced to the last row address state. Therefore, the user must program A23 = 0 and A22 = 1; that is, A23 maps to the row address output of A11 while A22 maps to the column address output of A11.
2. Caution must be taken to never program A23, A22 to any state other than 01 nor to allow the DS1262 to inadvertently reach this address in the burst read/write mode.

BANK SELECT SCHEME FOR EIGHT 1MX1 DRAMS Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7V
Voltage on BKUP Pin Relative to Ground	-0.3V to +12V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Input Logic High	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic Low	V_{IL}	-0.3		+0.8	V	1
Backup Supply	BKUP	5.5	8.0	10.0	V	1,2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	
DQ Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1,5
Output Current @ 0.4V	I_{OL}	2.0			mA	1,5
Input Supply Current	I_{CCI}		3.0	15	mA	6
Output Supply Current $V_{CCO} = V_{CCI}$ - 0.2V	I_{CCO}			100	mA	4
TOL pin = V_{CCO}	V_{TP}	4.50	4.62	4.75	V	7
TOL pin = GND	V_{TP}	4.25	4.37	4.50	V	7
Output Supply Current $V_{CCI} < V_{TP}$	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUPL}		2	4	µA	9
Backup Supply Quiescent	I_{BKUPQ}		2.0		mA	10

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	7	pF	
Output Capacitance	C_{OUT}		7	10	pF	
I/O Capacitance	$C_{I/O}$		7	10	pF	

AC ELECTRICAL CHARACTERISTICS

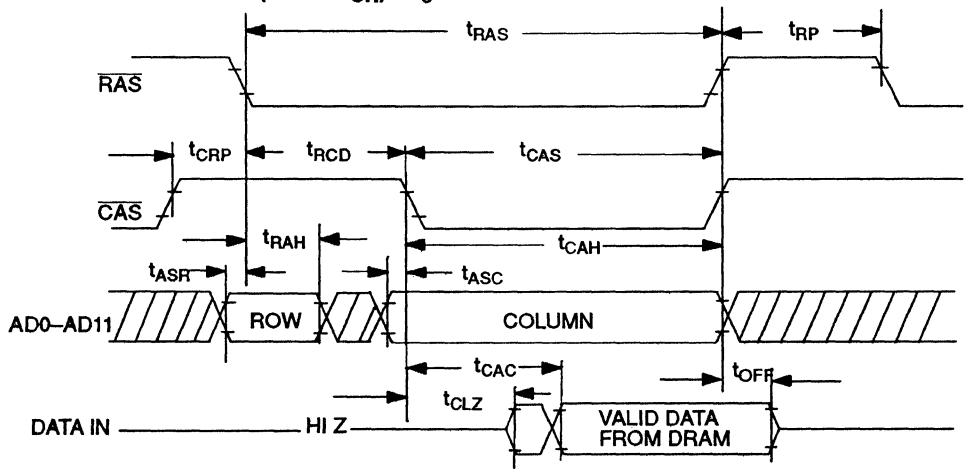
(t_A = 25°C, V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RAS}$ Pulse Width	t_{RAS}	200		350	ns	
$\overline{RAS}$ Precharge	t_{RP}	125		200	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge	t_{CRP}	125		200	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}	70		125	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100		275	ns	
Row Address Setup	t_{ASR}	25			ns	
Row Address Hold	t_{RAH}	25			ns	
Column Address Setup	t_{ASC}	20			ns	
Column Address Hold	t_{CAH}	100			ns	
Access Time From $\overline{CAS}$	t_{CAC}			200	ns	
CAS to Output In Low Z	t_{CLZ}				ns	1
Output Turn Off Delay	t_{OFF}				ns	1
$\overline{RAS}$ to $\overline{CAS}$ Precharge	t_{RPC}	20		175	ns	
$\overline{CAS}$ Setup Time	t_{CSR}	10		50	ns	
$\overline{CAS}$ Hold Time	t_{CHR}	200		350	ns	
Write Pulse Width	t_{WP}	125		300	ns	
Data Setup	t_{DS}	50			ns	
Data Hold	t_{DH}	125			ns	
D/Q to CLK Setup	t_{DC}	100			ns	
CLK to D/Q Delay	t_{CDD}			300	ns	
CLK Low Time	t_{CL}	500			ns	
CLK High time	t_{CH}	500			ns	
CLK Frequency	f_{CLK}	DC		1	MHz	
CLK Rise & Fall	t_R,t_f	3	10	20	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	
CLK to $\overline{RST}$ Hold	t_{CCH}	200			ns	
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	
$\overline{RST}$ to D/Q In High Z	t_{CDZ}			100	ns	

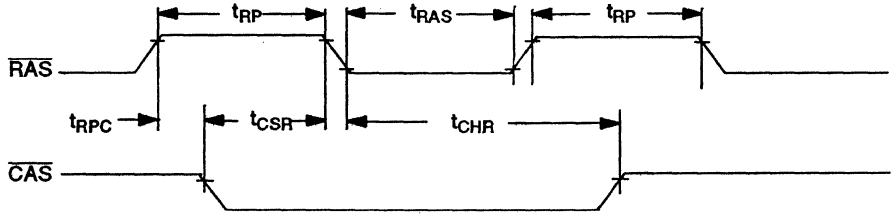
NOTE:

1. See DRAM data sheet.

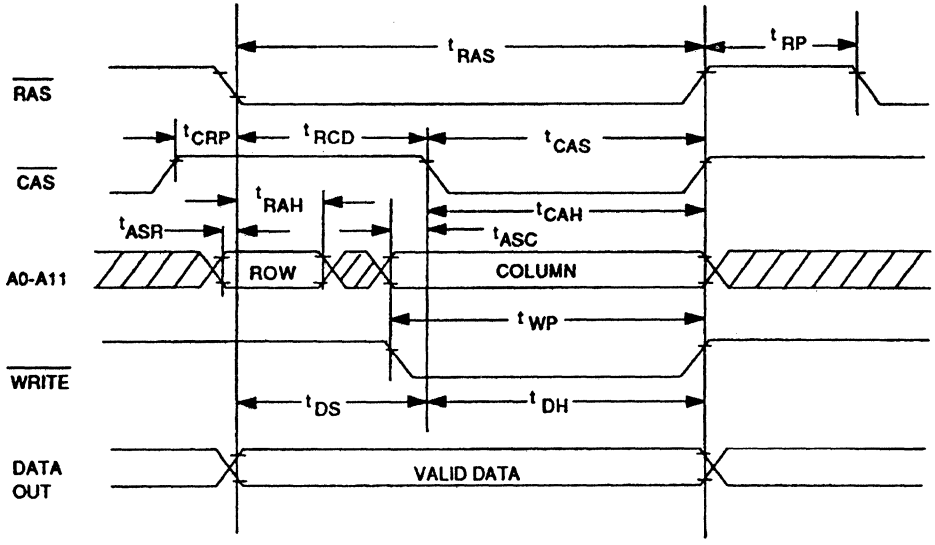
READ CYCLE FROM RAM ($\overline{WR}$ = V_{OH}) Figure 6



REFRESH CYCLE ($\overline{WR}$ = V_{OH}) Figure 7



WRITE CYCLE OUTPUT TO RAM Figure 8



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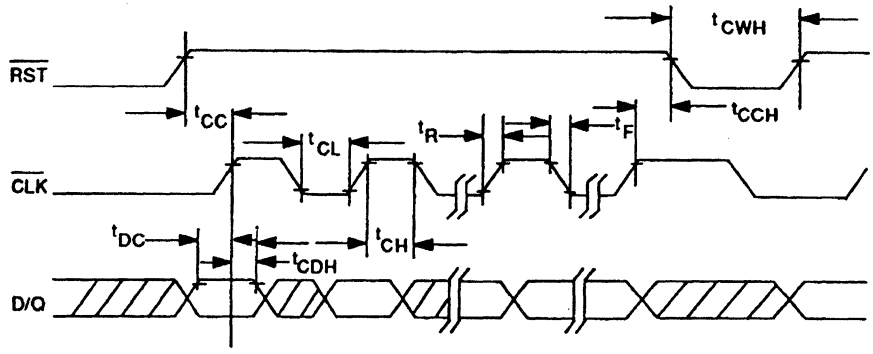
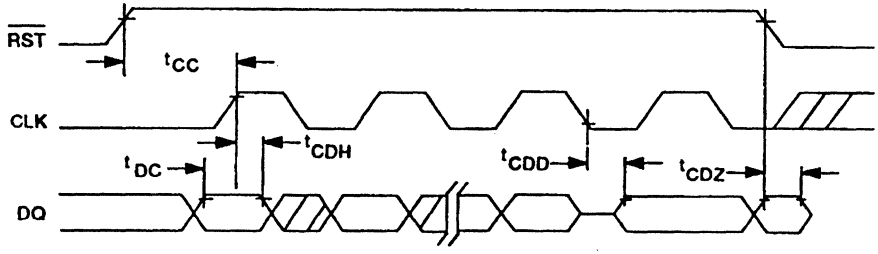
WRITE DATA TRANSFER FROM SERIAL PORT Figure 9



READ DATA TRANSFER FROM SERIAL PORT Figure 10



NOTES:

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CCI} is within nominal limits and the backup supply is below V_{CCI}.
3. Backup input voltage is internally regulated within the DS1262 such that V_{CCI} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1262 can supply RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 100 pF.
6. Measured with all outputs open, $V_{CCI} = V_{IH} = 5.5$ V.
7. V_{TP} is the trip point where the internal switching circuits disconnects V_{CCI} and connects the internally regulated backup supply to V_{CCO}.
8. I_{CCOB} is the maximum current which the DS1262 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS1262 is in the data retention mode (V_{CCI}=0V).
10. Backup quiescent current is the current consumed by the DS1262 when in the data retention mode and the backup supply is enabled. Total current into the BKUP pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

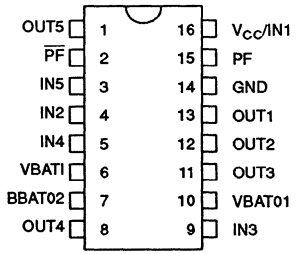
DALLAS SEMICONDUCTOR

DS1336
Afterburner Chip

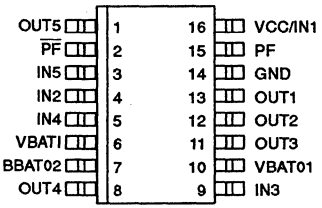
FEATURES

- Provides power switching of up to 1.5 amps at voltages between 3 and 5 volts
- Five separate power switches
- Selectable battery switches for use with battery-backed systems
- Very low on impedance of 0.7Ω
- Battery backup current of 4 mA
- Diode-isolated battery path
- Available in 16-pin DIP or 16-pin SOIC surface mount package
- Low voltage drop battery path
- Connects directly to a variety of Dallas Semiconductor devices adding increased switching capability for large battery backup current applications

PIN ASSIGNMENT



16-Pin DIP (300 mil)
See Mech. Drawing – Sect. 16, Pg. 1



16-Pin SOIC (300 mil)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

V_{CC}/IN1	-	+5V Input and Input 1
IN2 - IN5	-	Inputs 2 - 5
OUT1 - 5	-	Outputs 1 - 5
V_{BATIN}	-	External Battery Input
V_{BAT01}	-	Diode Protected Battery Output
V_{BAT02}	-	Low Voltage Drop Battery Output
PF, $\overline{PF}$	-	Power Fail Inputs
GND	-	Ground

DESCRIPTION

The DS1336 Afterburner Chip is designed to provide power switching between a primary power supply (V_{CC}) and a backup battery power supply (V_{BAT}). Five V_{CC} and two battery paths are provided which can be used individually or in parallel to supply uninterrupted power in applications such as SRAM networks. When used with one of the Dallas power monitoring devices listed in Section 10, Page 119, Table 1, the DS1336 allows a load to be switched from its main power supply V_{CC} to a battery backup supply when V_{CC} falls out of tolerance. A user may selectively tie together any combination of the output pins to provide the desired high current supply, providing up to 300mA per OUT pin or a maximum of 1.5A. Depending upon the user's backup supply load requirements, either of the V_{BAT} outputs may be tied to the OUT pins to supply current when V_{CC} is out of tolerance. The DS1336 switches back to the higher current V_{CC} from battery current when PF and $\overline{PF}$ become inactive.

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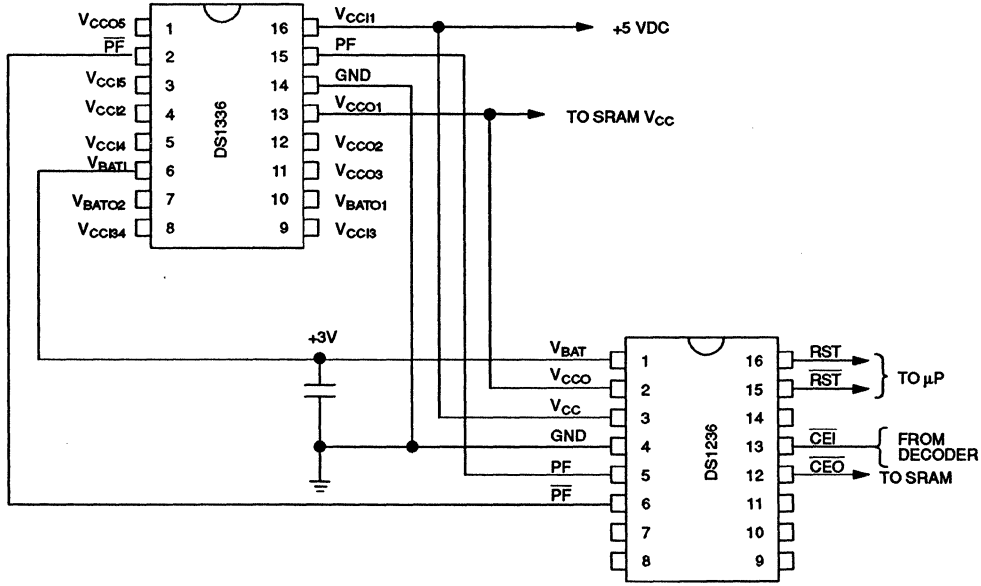
OPERATION

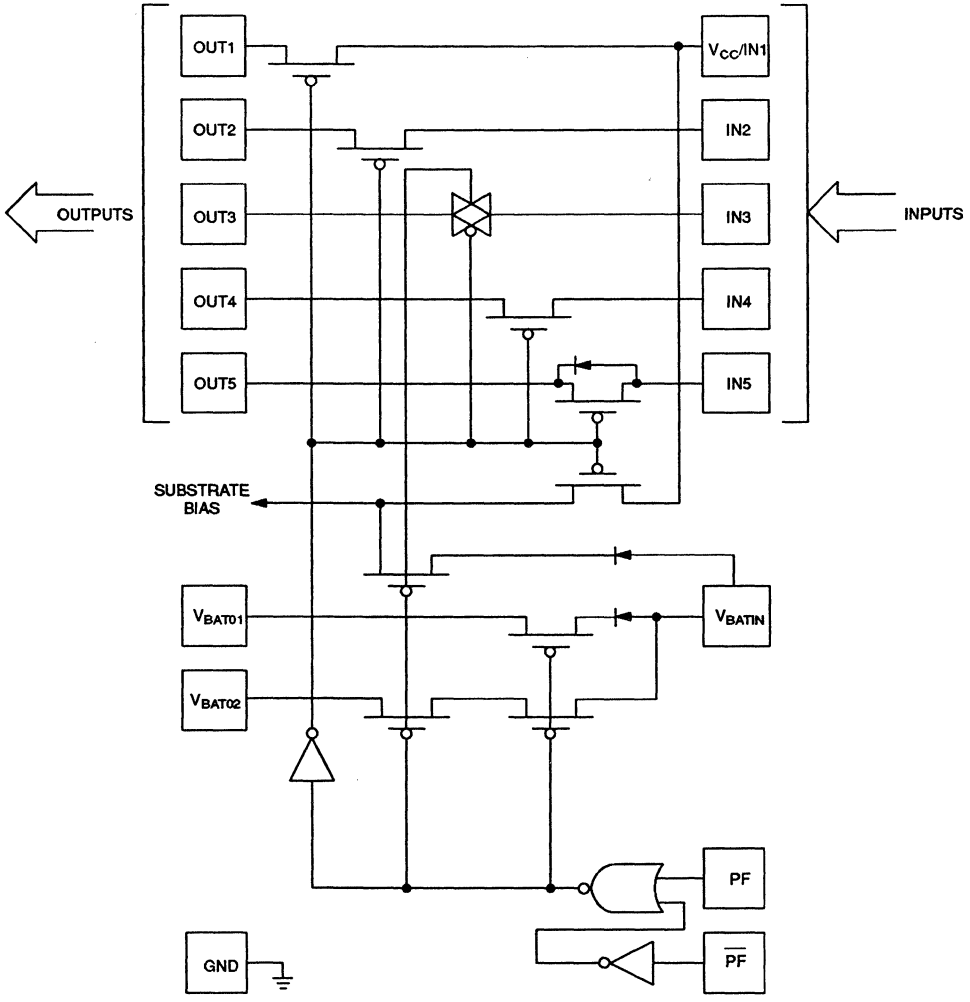
The required PF or $\overline{PF}$ input which controls the switching between the main V_{CC} and backup battery can be supplied by any of the devices listed in Table 1. All of the devices provide the DS1336 with a PF or $\overline{PF}$ signal, switching between a main supply V_{CC} and backup supply V_{BAT} when V_{CC} falls out of tolerance. For applications requiring switching from the V_{CC} supply inputs to V_{BAT}, the required PF or $\overline{PF}$ input to the DS1336 can be provided by the DS1236, DS1239, DS5001, or DS5340. For applications requiring switching from the V_{CC} inputs to the V_{BAT} input when V_{CC} begins falling out of tolerance, any of the Dallas Semiconductor devices listed in Table 1 can provide the DS1336 with the required switching input. A typical application is shown in Figure 1. For applications where switching between V_{CC} and V_{BAT} must occur at a voltage level such that V_{CC} is still greater than V_{BAT}, the OUT5 pin is recommended as it provides a diode path which will provide for a gradual transition between V_{CC} and V_{BAT}. OUT5 can be tied to the other OUTPUT pins to provide a gradual transition for all five current paths. In applications where tri-state switching is desired, OUT5 should be omitted. Only the $\overline{PF}$/PF pin is required for switching. In cases where the PF input will not be used, it should be connected to GND.

When either PF or $\overline{PF}$ is active, either of the V_{BATOX} outputs is available, although they should not be tied together (Figure 2, "DS1336 Block Diagram"). V_{BAT01} is recommended for sensitive applications such as providing backup current to timekeepers, because its diode isolated path provides for increased protection. V_{BAT02} is not recommended for applications where it would be tied to an OUTPUT pin supplying a voltage greater than that of the backup battery because V_{BAT02} is not a diode isolated current path.

TYPICAL APPLICATION Figure 1



DS1336 BLOCK DIAGRAM Figure 2



DALLAS SEMICONDUCTOR DEVICES WHICH PROVIDE PF OR $\overline{PF}$ INPUT TO DS1336 Table 1

DEVICE	SWITCH > V_{BAT}	SWITCH AT 3.0V	DEVICE	SWITCH > V_{BAT}	SWITCH AT 3.0V
DS1211	X		DS1239	X	X
DS1212	X		DS1259	X	
DS1231	X		DS1260	X	
DS1232	X		DS1610	X	
DS1234	X		DS1632	X	
DS1236	X	X	DS5001	X	X
DS1237	X		DS5340	X	X

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC1}	3.0	5.0	5.5	V	1
Supply Current	I_{CC1}				mA	
Input Low Voltage	V_{IL}			0.8	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}	V	1
Current Output V_{CC}=V_{CC1}, PF=0, $\overline{PF}$=1	I_{CCO1}			300	mA	2
Current Output V_{CC}=V_{CC2}, PF=0, $\overline{PF}$=1	I_{CCO2}				mA	2
Current Output V_{CC}=0, PF=1, $\overline{PF}$=0	I_{BATO2}			4	mA	4
Current, Forward Bias of V_{CC5} Diode	I_{FB}			20	mA	
Off Impedance	R_{OFF1}	5			MΩ	5
Off Impedance	R_{OFF2}	10			MΩ	6
On Impedance	R_{ON1}			0.7	Ω	7
On Impedance	R_{ON2}			50	Ω	8

AC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay	t_{PD}		10		ns	9
Switch Delay Power Fail	t_{PF}		100		ns	
Switch Delay Power On	t_{PON}			100	ns	
Capacitance PF, $\overline{PF}$	C_I			7	pF	

NOTES

1. All voltages referenced to ground.
2. I_{CCO} with a voltage drop of 0.2V from any V_{CCO} output.
3. I_{BATO1} with a voltage drop of 0.2V.
4. V_{BATO2} with a voltage drop of 1.0V.
5. R_{OFF1} applies to $V_{CCO1,2,3,4}$.
6. R_{OFF2} applies to $V_{BATO1,2}$.
7. Applies to V_{CCO1-5}, 300 mA.
8. Applies to $V_{BATO1-2}$, 4 mA.
9. V_{CCI3} to V_{CCO3} delay when used as chip enable control for write protection of a memory device. In this application a current 8 mA source current on V_{CCI3} with 50 pF load on V_{CCO3} can be accommodated.

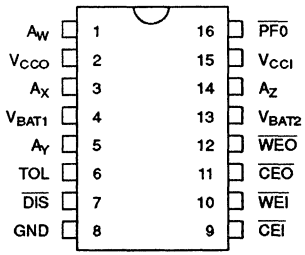
DALLAS SEMICONDUCTOR

DS1610
Partitioned NV Controller

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- SOIC version is pin compatible with the Dallas Semiconductor DS1210 NV Controller
- Unconditionally write protects all of memory when V_{CC} is out of tolerance
- Write protects selected blocks of memory regardless of V_{CC} status when programmed
- Automatically switches to battery backup supply when power fail occurs
- Provides for multiple batteries
- Consumes less than 100 nA of battery current
- Test battery on power up by inhibiting the second memory cycle
- Optional 5% or 10% Power Fail Detection
- 16-pin DIP or 16-pin SOIC Surface Mount Package
- Low forward voltage drop on the V_{CC} switch with currents of up to 150 mA
- Optional industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP and 16-Pin SOIC
See Mech. Drawings – Sect. 16, Pgs. 1 & 6

PIN DESCRIPTION

V_{CCI}	-	Input +5 Volt Supply
V_{BAT1}	-	+ Battery 1 Input
V_{BAT2}	-	+ Battery 2 Input
V_{CCO}	-	RAM Power (V_{CC}) Supply
GND	-	Ground
$\overline{CEI}$	-	Chip Enable Input
$\overline{CEO}$	-	Chip Enable Output
$\overline{WEI}$	-	Write Enable Input
$\overline{WEO}$	-	Write Enable Output
TOL	-	Power Supply Tolerance Select
A_W - A_Z	-	Address Inputs
$\overline{DIS}$	-	Memory Partition Disable
$\overline{PF0}$	-	Power Fail Output

DESCRIPTION

The DS1610 is a low power CMOS circuit which solves the application problems of converting CMOS RAMS into nonvolatile memories. In addition the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. The power supply incoming voltage at the V_{CCI} input pin is constantly monitored for an out of tolerance condition. When such a condition is detected, both the chip enable and write enable outputs are inhibited to protect stored data. The battery inputs are used to supply V_{CCO} with power when V_{CCI} is less than the battery input voltages. Special circuitry uses a low leakage CMOS process which affords precise voltage detection at extremely low current consumption. By combining the DS1610 Partitioned NV Controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

The DS1610 Partitioned NV Controller functions like the Dallas Semiconductor DS1210 NV controller when the ($\overline{DIS}$) disable pin is grounded. An internal pulldown resistor to ground on the $\overline{DIS}$ pin of the DS1610S allows it to retrofit into DS1210S applications. When the $\overline{DIS}$ pin is grounded the address inputs A_W - A_Z and the write enable input $\overline{WEI}$ are ignored. Also the power fail output $\overline{PFO}$ and the write enable output $\overline{WEO}$ are tristated.

OPERATION – DISABLE PIN CONNECTED TO V_{CCO}

The DS1610 performs five circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function provided by the DS1610 is power fail detection. The incoming supply (V_{CCI}) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits both the chip enable output ($\overline{CEO}$) and the write enable output ($\overline{WEO}$). A third function of write protection is accomplished by holding both the chip enable output $\overline{CEO}$ and write enable output $\overline{WEO}$ to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If $\overline{CEI}$ is low at the time that power fail detection occurs the $\overline{CEO}$ signal is kept low until $\overline{CEI}$ is brought high again. However, $\overline{CEO}$ is forced high after 1.5 µsec regardless of the state of $\overline{CEI}$. Similarly, if $\overline{WEI}$ is low at the time that power fail detection occurs, the $\overline{WEO}$ is signal will remain low until $\overline{WEI}$ is brought high or 1.5 µsec elapses. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin TOL grounded. If the tolerance pin is connected to V_{CCO} then power fail detection occurs in the range of 4.5 volts to 4.25 volts. The $\overline{PF0}$ signal is driven low and remains low until V_{CCI} returns to nominal conditions. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ and $\overline{WEO}$ will follow $\overline{WEI}$. The fourth function which the DS1610 performs is a battery status warning so that potential data loss is avoided. Each time V_{CCI} is applied to the device battery status is checked with a precision comparator. If during battery backup, no switch occurred from one battery to the other, the voltage of the battery supplying power when V_{CCI} is applied is checked. If this voltage is less than 2.0 volts the second chip enable cycle after power is applied is inhibited. If any switch from one battery to another did occur the voltage of both batteries is checked. If either voltage is less than 2.0 volts the second chip enable cycle will be inhibited. Battery status can therefore be determined by performing a read cycle after power up to any location in memory, verifying that memory location's contents. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data then the data is in danger of being corrupted. The fifth function of the DS1610 provides for battery redundancy. When data integrity is extremely important it is wise to use two batteries to insure reliability. The DS1610 controller provides an internal isolation switch which allows the connection of two batteries. When entering battery backup operation, the battery with the highest voltage is selected for use. If one battery should fail, the other would then supply energy to the connected load. The switch to a redundant battery is transparent to circuit operation and to the user. In applications where battery redundancy is not a major concern a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. When batteries are first connected to one or both of the V_{BAT} pins V_{CCO} will not show the battery potential until V_{CCI} is applied and removed for the first time.

OPERATION – WRITE PROTECTION PROGRAMMING MODE

When the disable pin is connected to V_{CCI} or V_{CCO}, the DS1610 performs all of the functions described earlier with the addition of a partition switch which selectively write protects blocks of memory. The state of the $\overline{DIS}$ pin is strobed and latched as V_{CCI} crosses the power fail trip point so that the DS1610 maintains its configuration during power loss. If the strobed value of $\overline{DIS}$ is a high the internal pulldown resistor on the $\overline{DIS}$ pin will be disconnected in the power fail state to eliminate the possibility of battery discharge. The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A_W-A_Z. These address lines are normally the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycle will load the partition switch. Since there are 16 possible write protected partitions, the size of each partition is determined by the size of the memory. For example, a 128K X 8 memory would be divided into 16 partitions of 128K/16 or 8K X 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A_W through A_Z and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A_X was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1610 to inhibit $\overline{WEO}$ from going low as $\overline{WEI}$ goes low whenever $A_Z A_Y A_X A_W$=0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM. Also note that on initial battery attach the partition register can power up in any state.

TABLE 1: PATTERN MATCH TO WRITE PARTITION REGISTER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A_W	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A_X	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A_Y	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A_Z	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

TABLE 2: PARTITION REGISTER MAPPING

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_Z A_Y A_X A_W)
A_W	BIT 21	PARTITION 0	0000
A_X	BIT 21	PARTITION 1	0001
A_Y	BIT 21	PARTITION 2	0010
A_Z	BIT 21	PARTITION 3	0011
A_W	BIT 22	PARTITION 4	0100
A_X	BIT 22	PARTITION 5	0101
A_Y	BIT 22	PARTITION 6	0110
A_Z	BIT 22	PARTITION 7	0111
A_W	BIT 23	PARTITION 8	1000
A_X	BIT 23	PARTITION 9	1001
A_Y	BIT 23	PARTITION 10	1010
A_Z	BIT 23	PARTITION 11	1011
A_W	BIT 24	PARTITION 12	1100
A_X	BIT 24	PARTITION 13	1101
A_Y	BIT 24	PARTITION 14	1110
A_Z	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to 7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C TO 70°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 6 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 6 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS ($0°C$ TO $70°C$, V_{CCI} WITHIN DC OPERATING CONDITIONS)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}			5	mA	3, 14
Standby Current	I_{CC2}			200	µA	3, 15
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			150	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1, 16
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.50	V	1, 16
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			30	Ω	5
$\overline{WEI}$ to $\overline{WEO}$ Impedance	Z_{WE}			30	Ω	5
$\overline{DIS}$ Pulldown Resistance	R_{DIS}	50K		250K	Ω	

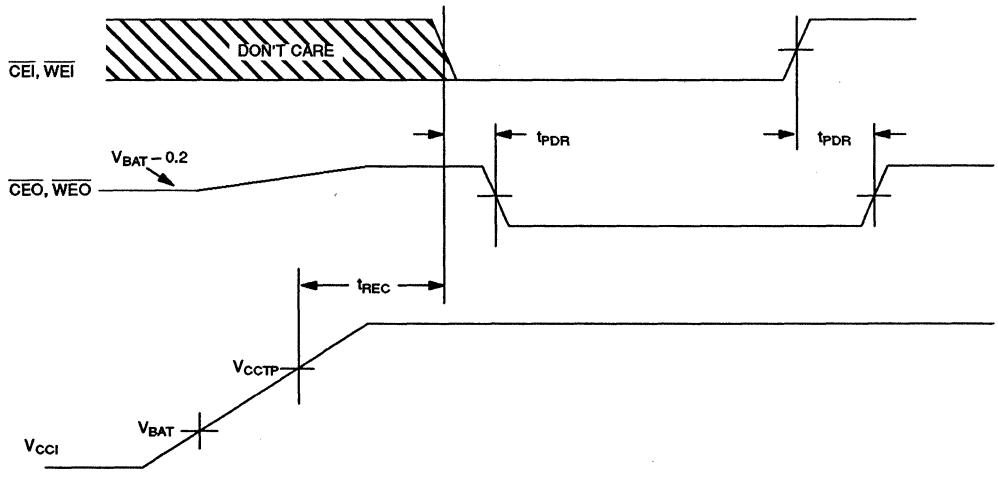
DC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CCI}<V_{BAT})						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
$\overline{WEO}$ Output	V_{OHL}	V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2, 3
Battery Backup Current @ V_{CCO} = V_{BAT} -0.2V	I_{CCO2}			150	µA	6, 7, 8

CAPACITANCE (t_A = 25°C)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

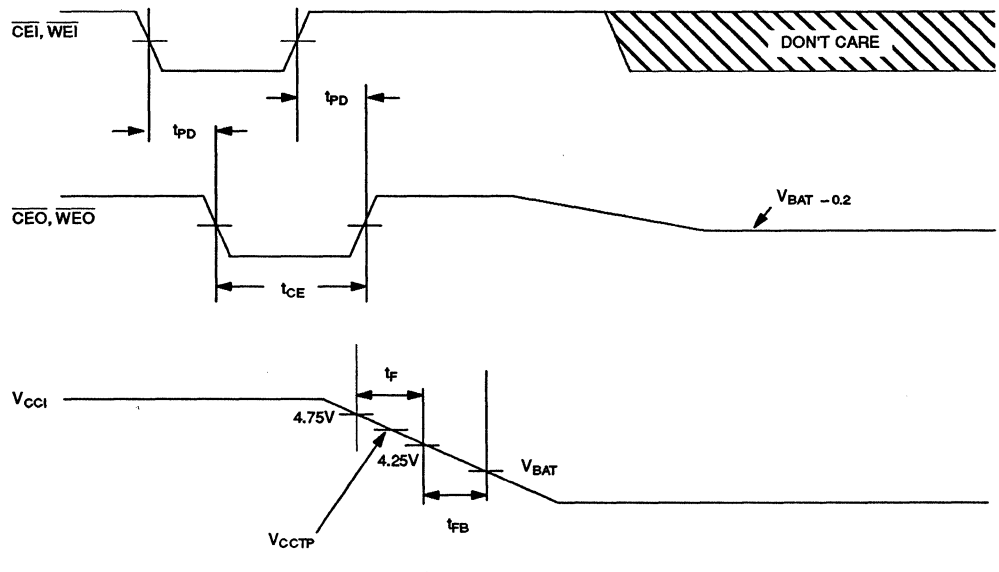
AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C; V_{CCI}=4.75V TO 5.50V, TOL=GND V_{CCI}=4.50V TO 5.50V, TOL–V_{CCO})						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	10			ns	9
$\overline{CEI}$ Pulse Width	t_{CW}	75			ns	
$\overline{CEI}$ to $\overline{CEO}$ Falling Propagation Delay	t_{PDF}			5	ns	10
Later of $\overline{CEI}$, $\overline{WEI}$ to $\overline{WEO}$ Falling Propagation Delay	t_{PDFW}			20	ns	10
$\overline{CEI}$ to $\overline{CEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10, 11
$\overline{WEI}$ to $\overline{WEO}$ Rising Propagation Delay	t_{PDR}			5	ns	10, 11
Write Recovery	t_{WR}	10			ns	11

AC ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{CC}<4.5V)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	25		125	ms	12
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	0			µs	13
$\overline{CEI}$ Pulse Width	t_{CW}			1.5	µs	7, 8
$\overline{WEI}$ Pulse Width	t_{CW}			1.5	µs	7, 8

TIMING DIAGRAM: POWER UP



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: LOADING PARTITION REGISTER

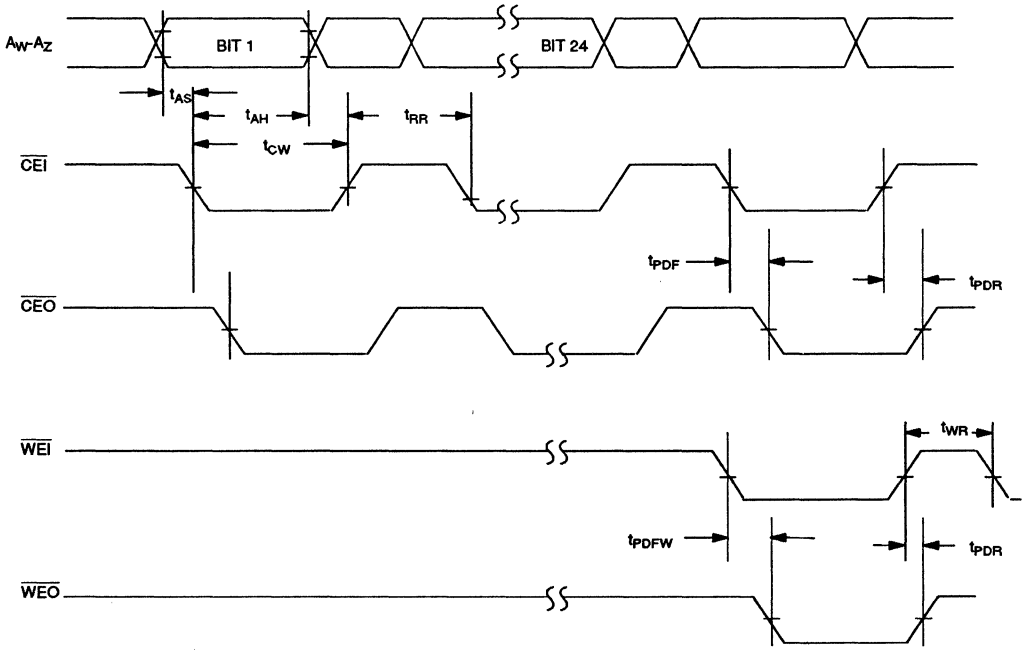


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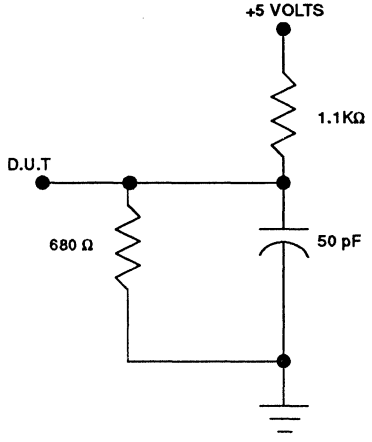
FIGURE 1: OUTPUT LOAD



NOTES

1. All voltages are reference to ground
2. Only one battery input is required.
3. Measured with outputs open circuited.
4. I_{CC01} is the maximum average load which the DS1610 can supply to the memories.
5. Z_{CE} and Z_{WE} are average input-to-output impedances as the input is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE} and Z_{WE}.
6. I_{CC02} is the maximum average load current which the DS1610 can supply to the memories in the battery back-up mode.
7. t_{CW} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery mode.
9. Applies only when loading partition switch.
10. Measured with a load as shown in Figure 1.
11. Measured with $\overline{DIS}$ at a logic high level.
12. $\overline{CEO}$ and $\overline{WEO}$ will be held high for a time equal to t_{REC} (max = 125 msec) after V_{CCI} crosses V_{CCTP}.
13. t_R is the slew rate of V_{CCI} from 4.25V to 4.75V.
14. $\overline{CEI}$, $\overline{WEI}$, A_W - A_Z run at minimum timing set and at voltage levels of 0V to 3V.
15. All inputs within 0.3V of ground or V_{CCI} and $\overline{CEI}$ within 0.3V of V_{CCI}.
16. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL} = 0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA.

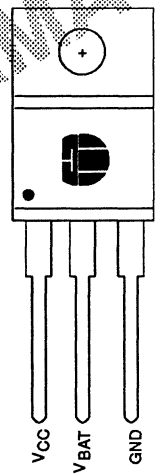
DALLAS SEMICONDUCTOR

DS1633x
High Speed Battery Recharger

FEATURES

- Recharges lithium batteries and NiCad batteries
- Cuts in half normal battery charge time
- Accepts open circuit power supply voltages between 4.75 and 6.0 V, and battery voltages between 0 and 3.75 V
- Retains battery and power supply limits in on–board memory
- Part is programmed and tested in the factory
- 3-pin TO–220 package
- Operating range –10°C to 85°C
- Applications include consumer electronics, portable/ cellular phones, pagers, medical instruments, backup memory systems, security systems
- Supplies a maximum of 100 mA to a charging battery, as DC or pulsed charging current

PIN ASSIGNMENT (DIP PKG)



PIN DESCRIPTION

V_{CC}	Input Voltage, +
V_{BAT}	Battery Voltage Input, +
GND	Ground

9

DESCRIPTION

The DS1633 High Speed Battery Recharger automatically provides a constant current recharge to a battery as long as the battery's voltage is below the specified minimum voltage. The DS1633 charges the battery using its V_{CC} input as a source. When V_{CC} is floated, the DS1633 is dormant. When V_{CC} is reapplied, the DS1633 begins charging.

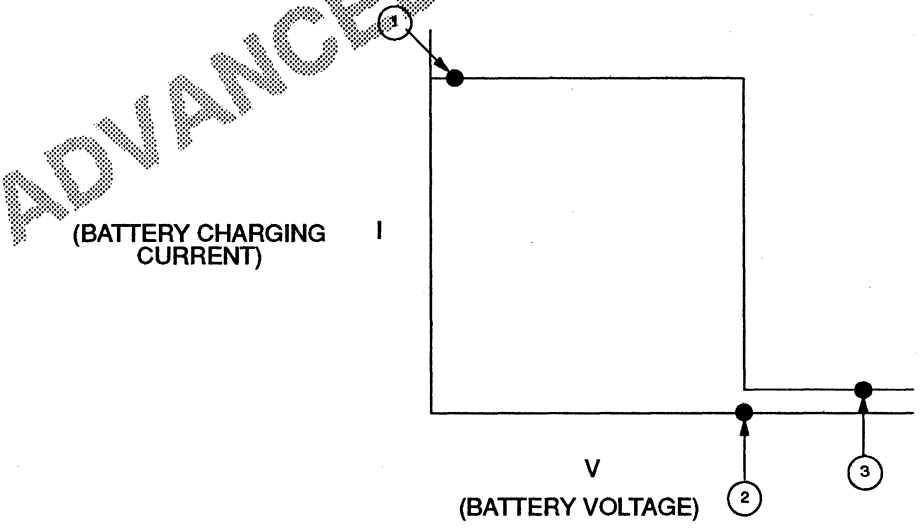
Although a variety of load curves may be used to charge a battery, most do not take advantage of the fact that a battery can accept its maximum (or above) current rating for charging purposes over its entire voltage range. The DS1633 takes advantage of this opportunity by constantly readjusting its current supply to the battery being charged. As the voltage level of the battery being charged rises, and the supply current drops, the DS1633 adjusts itself to boost the current supply back to its maximum. This feature greatly decreases the recharge time required to fully charge a lithium or NiCad cell.

The DS1633 provides a designer with the ability to use a customized battery load line for currents up to 100 mA by selecting a pre-programmed DS1633 from Dallas Semiconductor. A DS1633 solution provides a self contained charging system which requires no backup memory support, user programming, or external interface circuitry.

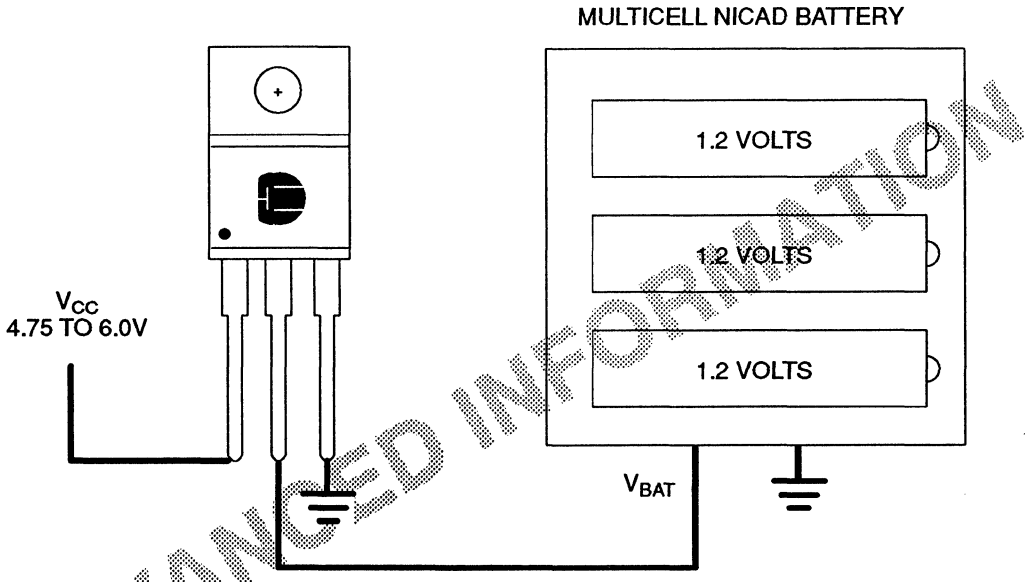
The Profile Characteristics table lists charge curves and part reference designators for the pre–programmed curves that Dallas Semiconductor will initially offer.

For requirements which cannot be met by one of the initial charge curve programs listed, please contact the nearest Dallas Semiconductor Sales Office.

PROFILE CHARACTERISTICS					
DS1633 CHARGE PROFILE	(1) MAXIMUM CURRENT	(1A) MAXIMUM CURRENT FREQUENCY	(2) CUTOFF VOLTAGE	(3) TRICKLE CURRENT	(3A) TRICKLE FREQUENCY
1633A	100 mA	DC	3.6V	17 mA	1/8 sec. pulse/1 sec.
1633B	80 mA	DC	3.6V	9 mA	1/8 sec. pulse/1 sec.
1633C	60 mA	DC	3.6V	7 mA	1/8 sec. pulse/1 sec.
1633D	40 mA	DC	3.6V	5 mA	1/8 sec. pulse/1 sec.
1633E	20 mA	DC	3.6V	5 mA	1/8 sec. pulse/1 sec.



TYPICAL APPLICATION



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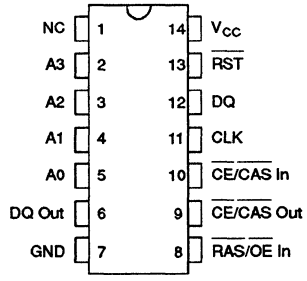
DALLAS SEMICONDUCTOR

DS1206
Phantom Serial Interface Chip

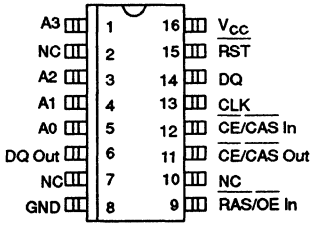
FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth – 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as ten DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



14-Pin DIP (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 1



16-Pin SOIC (300 MIL)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

NC	–	No connection
A0–A3	–	Memory address bus
DQ Out	–	Data out to memory bus
GND	–	Ground
$\overline{RAS}/\overline{OE}$ In	–	Output Enable or $\overline{RAS}$ input from memory bus
$\overline{CE}/\overline{CAS}$ In	–	Chip enable or $\overline{CAS}$ from memory bus
$\overline{CE}/\overline{CAS}$ Out	–	Chip enable or $\overline{CAS}$ to memory circuit
CLK	–	Clock for serial port
DQ	–	Data I/O for serial port
$\overline{RST}$	–	Reset for serial port
V_{CC}	–	+5 Volts

DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. A sequence of software-generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal without affecting

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address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the 3-wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

OPERATION

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

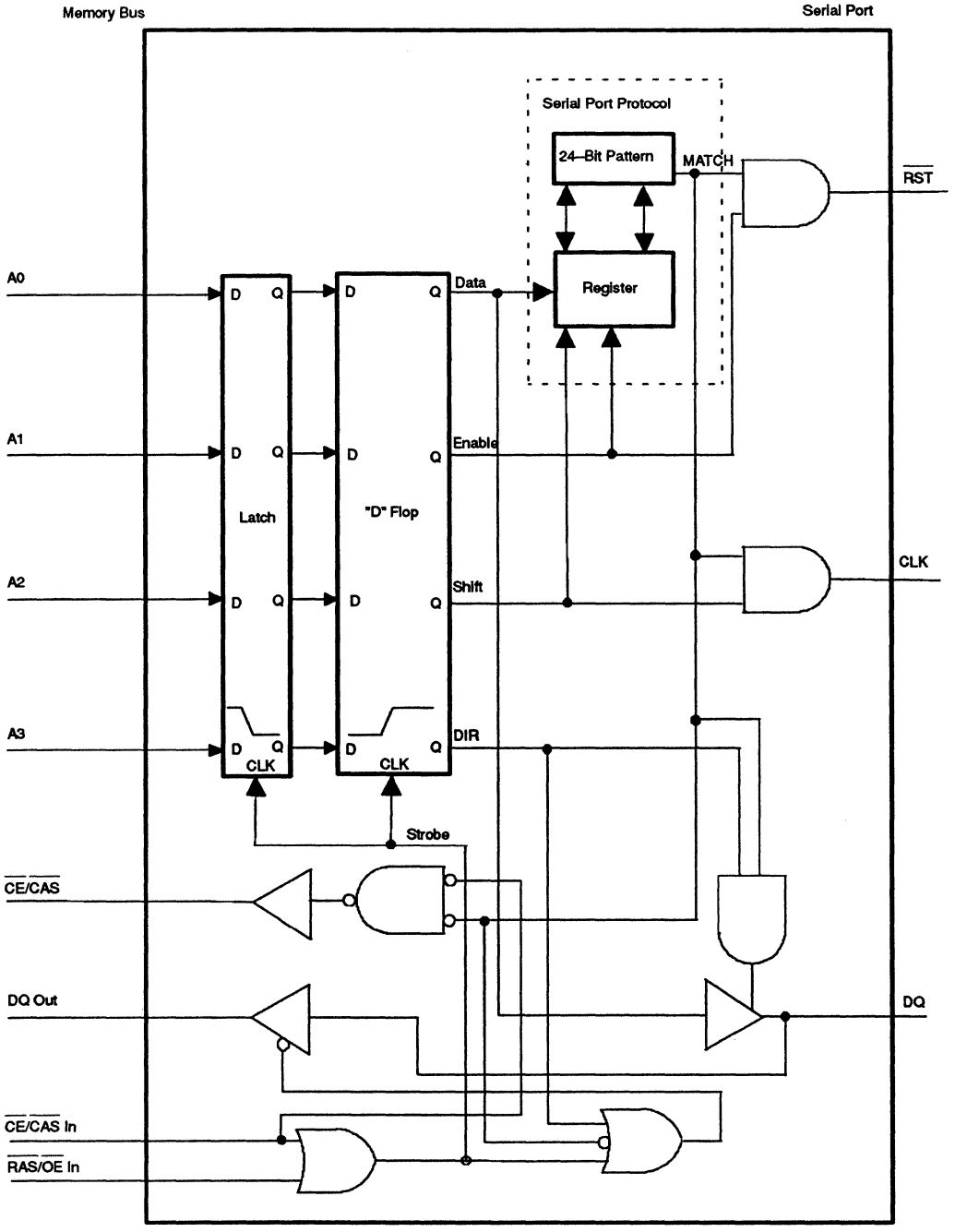
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

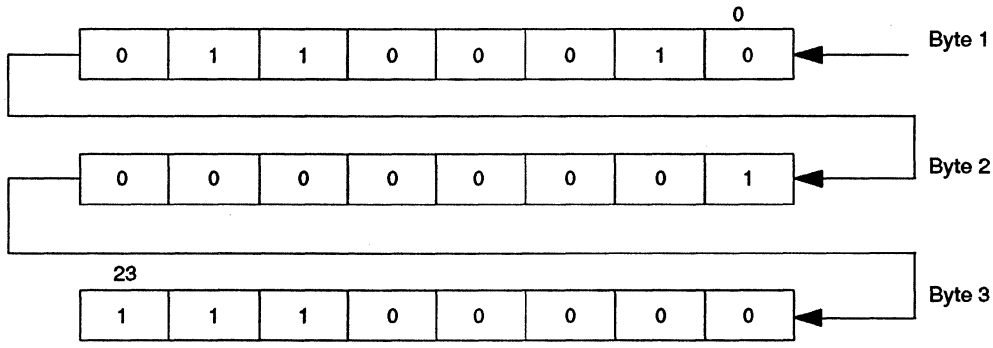
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

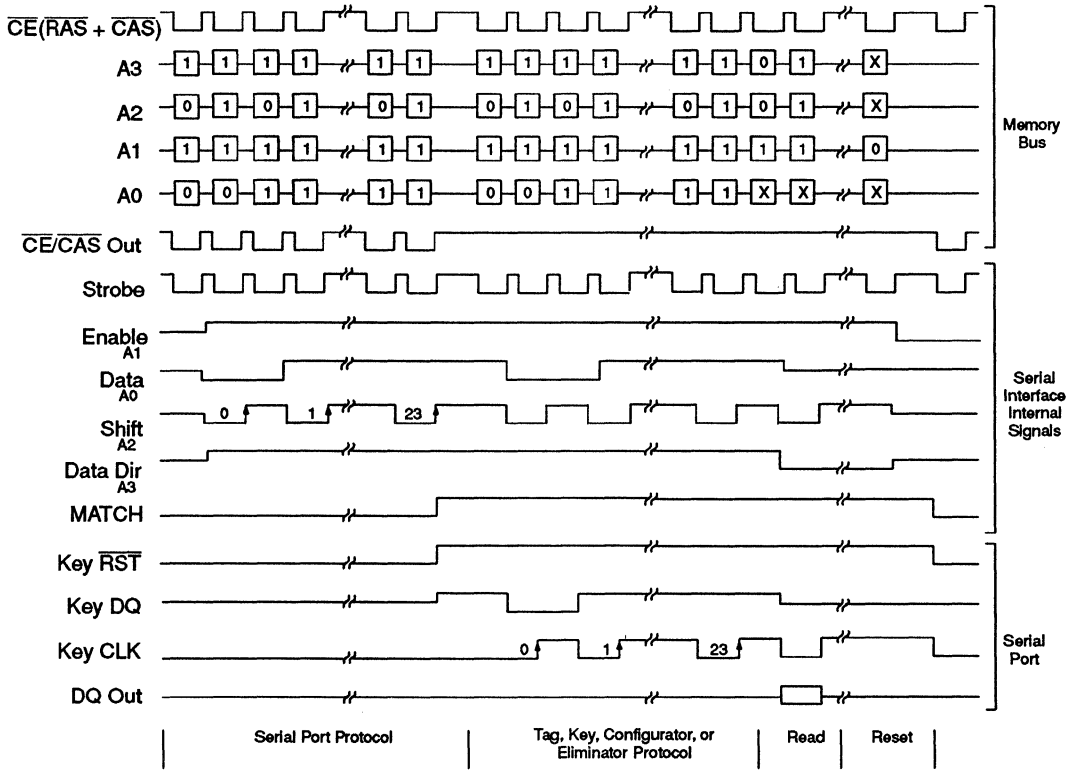
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

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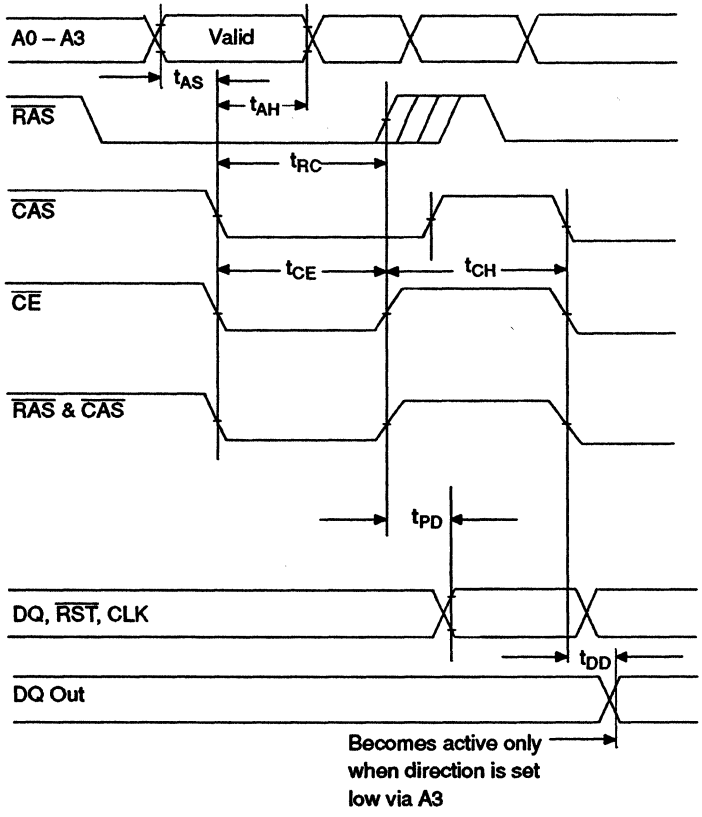
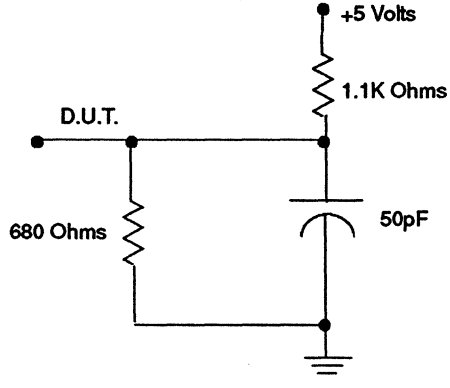
MEMORY BUS INPUTS



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4



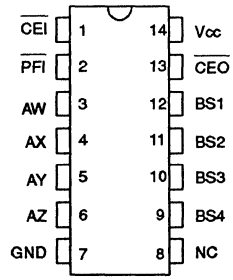
DALLAS SEMICONDUCTOR

DS1222
BankSwitch Chip

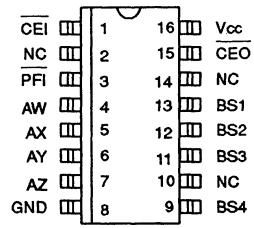
FEATURES

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ± 10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1222 14-Pin DIP
(300 Mil.)
See Mech. Drawing
Sect. 16, Pg. 1



DS1222S16-Pin SOIC
(300 Mil.)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

A_W-A_Z	Address Inputs
$\overline{CEI}$	Chip Enable Input
$\overline{CEO}$	Chip Enable Output
NC	No Connection
BS1,BS2,	Bank Select Outputs
BS3,BS4	Bank Select Outputs
$\overline{PFI}$	Power Fail Input
V_{CC}	+5 Volts
GND	Ground

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DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION – BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. (Note: the power fail input [$\overline{PFI}$] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs AW through AZ should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven

low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses AX, AY, and AZ. However, address line AW defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of $\overline{CEI}$ when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS BIT SEQUENCE Table 1

	BIT SEQUENCE															
ADDRESS INPUTS	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank	**A_W Bit Sequence**					**Outputs**			
Selected	**11**	**12**	**13**	**14**	**15**	**BS1**	**BS2**	**BS3**	**BS4**
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{CEO}$ = V_{IH} independent of $\overline{CEI}$

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

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AC ELECTRICAL CHARACTERISTICS

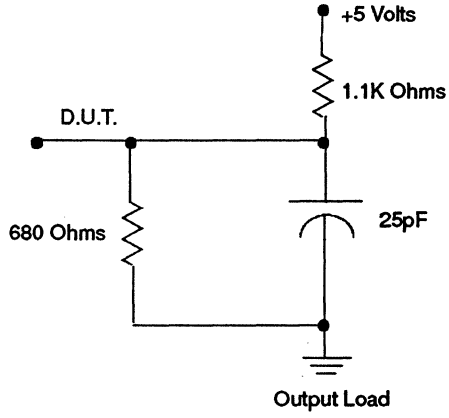
(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First $\overline{CE}$	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

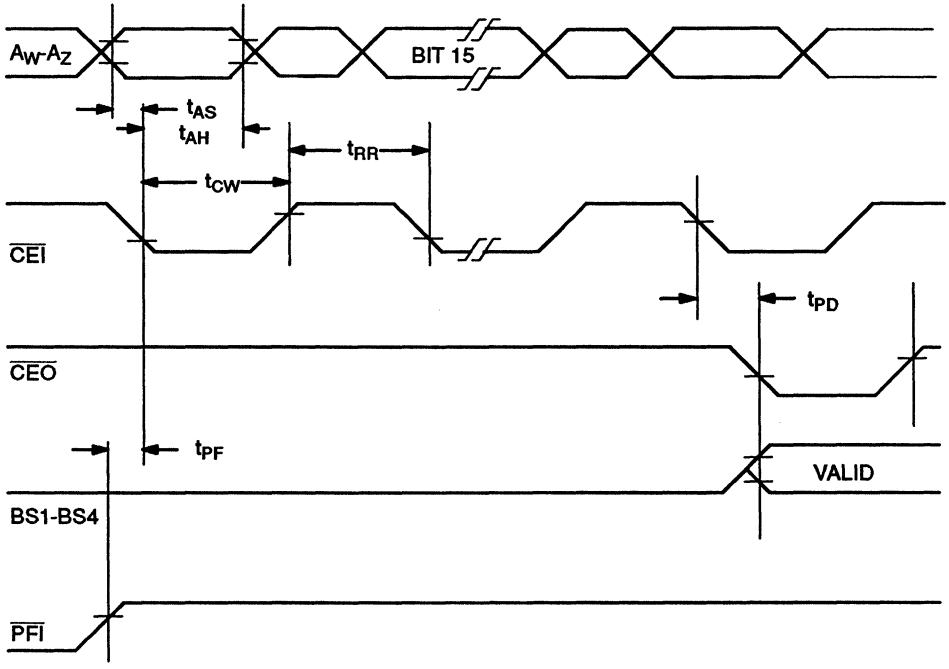
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1



TIMING DIAGRAM-ACCESS TO BANK SWITCH

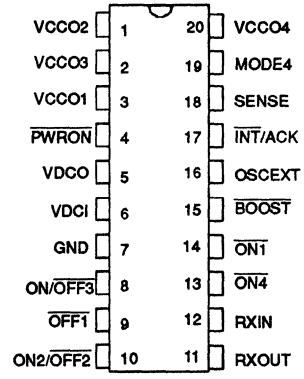


DALLAS SEMICONDUCTOR

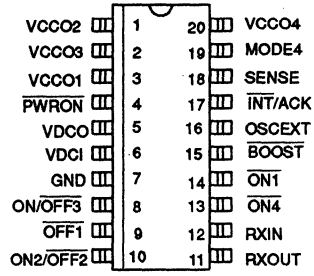
DS1227
KickStarter Chip

FEATURES
- Provides step-up regulation and microenergy management for battery-operated systems
- Converts +3V to +6V DC input power source to +5V DC out for system power
- "Kickstarts" system power upon detection of external stimuli:
  - Clock/calendar alarm
  - Sensor trip; such as from a photo diode
  - Incoming activity to a serial port
  - Any low-level signal transition
- Shuts down microcontroller power under software control when operation complete
- Provides 3 auxiliary power outputs for independent powering of system functions
- Allows design of "power on demand" systems
- Insures maximum life of main power source
- Ideally suited for DS5000-based systems
- Available in 20-pin DIP or SOIC packages

PIN ASSIGNMENT



20-Pin DIP (300 Mil)
See Mech. Drawing - Sect. 16, Pg. 1



20-Pin SOIC (300 Mil)
See Mech. Drawing - Sect. 16, Pg. 6

ORDERING INFORMATION
DS1227: 20-Pin DIP
DS1227S: 20-Pin SOIC

DESCRIPTION
The DS1227 Kickstarter is a unique CMOS circuit which combines power conversion and microenergy management functions for battery operated systems. Using its integral DC-DC converter, the DS1227 supplies +5V on demand from either a 3– or 6–volt battery input. The primary +5V output, typically tied to the microcontroller's V_{CC} pin, is "kickstarted" on in response to any one of several possible momentary, external signal transitions. Two auxiliary +5V power supply outputs can then be independently enabled or disabled under software control. When the primary power supply output is disabled, also under software control, the auxiliary power supply outputs remain in the state selected. In this manner, individual portions of the system can be powered only

when they are required, minimizing the energy consumption of the system.

The Kickstarter activates or kickstarts the primary V_{CC} output in response to external momentary low-going signals. Examples of such signals include a clock/calendar alarm from a DS1283 Watchdog Timekeeper, or an incoming asynchronous serial data word from a host PC via the DS1275 Line Powered Transceiver, or a simple pushbutton switch.

In addition, the DS1227 kickstarts primary system power in response to activity detected by an external sensor circuit. In this case, the Kickstarter can be signalled at regular intervals, typically from a DS1283 Watchdog Timekeeper, to momentarily apply power to the sensor and monitor an input for an active response.

An application using the Kickstarter has the capability to wake-up from a ultra-low power state, perform a task using minimum energy, and then go back to sleep until the DS1227 is signalled to kickstart system operation once again.

PIN DESCRIPTION

PIN	I/O	DESCRIPTION
$\overline{BOOST}$	Input	Regulation mode control.
V_{DCO}	Output	Main DC supply voltage output.
V_{DCI}	Input	Main DC supply voltage input.
GND	–	System ground.
V_{CCO1}	Output	Primary switched supply voltage output.
$\overline{ON1}$	Input	On control for V_{CCO1}. $\overline{ON1}$ is negative edge triggered and internally pulled high via a weak resistor.
$\overline{INT}$/ACK	Input/Output	Interrupt output/input; internally pulled low via a weak resistor during output; level activated via strong high voltage for input.
$\overline{OFF1}$	Input	Off control for V_{CCO1}; edge-triggered active low.
$\overline{PWRON1}$	Output	V_{CCO1} Power On signal output; Indicates when V_{CCO1} is powered on; Sometimes required for controlling external tri-state buffers in systems where micro-energy management techniques are employed.
V_{CCO2}	Output	Auxiliary switched supply voltage outputs.
ON2/$\overline{OFF2}$	Input	On/Off controls for V_{CCO2}/V_{CCO3}; level activated.
ON3/$\overline{OFF3}$	Input	
V_{CCO4}	Output	Momentarily switched VCC output.
$\overline{ON4}$	Input	V_{CCO4} trigger; edge activated; active low.
SENSE	Input	Sense input sampled just prior to V_{CCO4} off; turns on V_{CCO1} if active; active high.
MODE4	Input/Output	Selects V_{CCO4} on time; level sensitive input/current source output.
RXIN	Input	Serial I/O input; On control for V_{CCO1} when serial activity detected; edge activated.
RXOUT	Output	Serial I/O output; Echos incoming serial data from RXIN when V_{CCO1} is turned on.
OSCEXT	Output	Oscillator Signal Output; Gated by internal comparator when $\overline{BOOST}$ is enabled. Continuous when $\overline{BOOST}$ is disabled.

INPUT SUPPLY VOLTAGE

The Kickstarter is capable of operating either in a regulated step-up DC-to-DC conversion (boost) mode or in a non-regulated supply voltage Pass-Through mode.

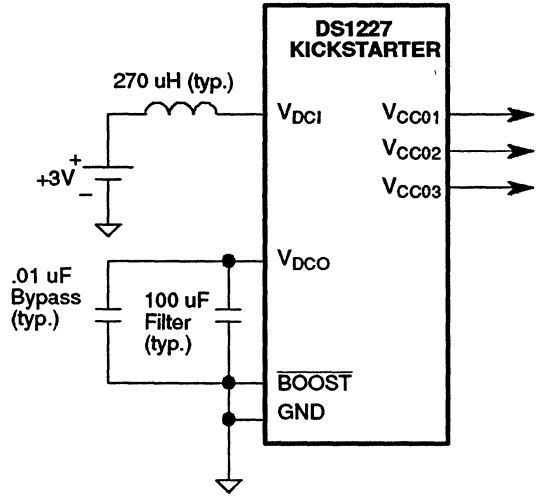
In boost mode, the Kickstarter is designed to provide a regulated +5V output on the V_{CCO1}, V_{CCO2}, or V_{CCO3} voltage supply output pins from a +3V lithium source. Figure 1 illustrates the standard configuration for use of this mode. The $\overline{BOOST}$ pin should be tied low in order to enable step-up DC-to-DC conversion. V_{DCI} is used for the DC power supply input and is tied through an inductor (270 µH typical) to a +3V lithium cell. V_{DCO} is the main DC output which is switched to the V_{CCO1}, V_{CCO2}, and V_{CCO3} outputs. This pin requires a large capacitor (typically 100 µF) to ground for the boost regulation low pass output network. Further details of the boost voltage regulator operation are given in the "Boost Mode Operation" section of this data sheet.

Figure 2 and Figure 3 illustrate the required configurations to select the supply voltage Pass-Through mode of operation. In both of these configurations the $\overline{BOOST}$ pin should be strapped directly to the V_{DCO} pin. This connection causes the $\overline{BOOST}$ pin to remain at a high level at all times that a battery is connected. As a result, the internal boost regulator will be disabled when kickstarting occurs. When a +5V supply is used as the input DC power source, it should be directly connected to the V_{DCO} in parallel with a filter capacitor as shown in Figure 2. The V_{DCI} input itself should be grounded in this configuration.

If a +6V supply is used, then it should be connected to the V_{DCI} pin. A filter capacitor should still be connected to V_{DCO}. The voltage on V_{DCO} and subsequently on V_{CCO1}, V_{CCO2}, and V_{CCO3} (when they are enabled following kickstarting) will be a diode drop below the V_{DCI} voltage.

In both the Boost and Pass-Through modes, the DS1227 uses the voltage on V_{DCO} as its own internal supply.

DS1227 BOOST MODE CONFIGURATION Figure 1



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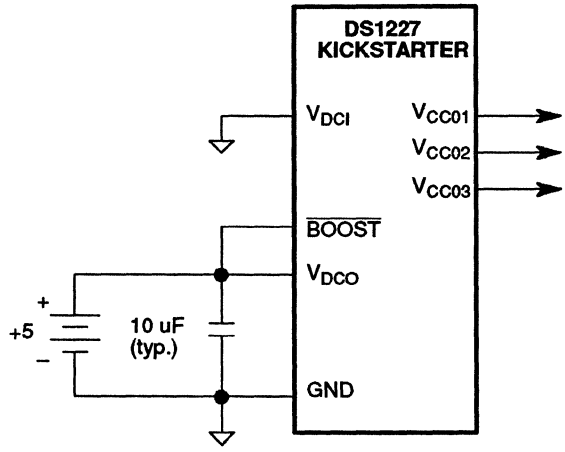
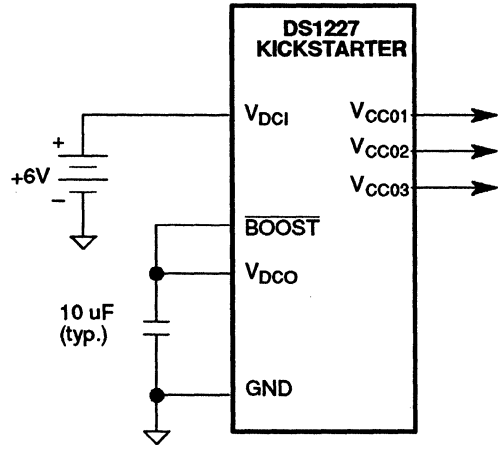
DS1227 +5V PASS-THROUGH MODE CONFIGURATION Figure 2



DS1227 +6V PASS-THROUGH MODE CONFIGURATION Figure 3



KICKSTARTER OPERATION

A conceptual block diagram of the internal circuitry of the DS1227 is illustrated in Figure 4 for reference. While in an initial power down state, the DS1227 will sense activity from an external stimulus applied to one of three input pins and kickstart system power by applying voltage from the input power source to the primary V_{CCO} output (V_{CCO1}). Activity detected on any of the $\overline{ON1}$, RXIN, and SENSE pins initiates the kickstarting action.

When kickstarting occurs and the DS1227 is configured for boost operation, the on-chip, step-up DC-to-DC converter is started and the voltage on V_{DCO} will be boosted from its initial V_{BAT} level to V_{DCON} before V_{CCO1} is turned on. If the DS1227 is configured for voltage Pass-Through operation, then the DC-to-DC converter will remain disabled and voltage on the V_{DCO} line will be switched to the V_{CCO1} pin immediately following the detection of an active transition on a stimulus input.

Initially, when V_{CCO1} is off, the $\overline{INT}$/ACK pin is collapsed to ground. At the time that voltage is switched to the V_{CCO1} output pin during kickstarting, the $\overline{INT}$/ACK pin will be latched such that it will remain in a low state. This signals the microcontroller that a power on reset has occurred. The OFF1, ON2/$\overline{OFF2}$, and ON3/$\overline{OFF3}$ inputs are all ignored until the microcontroller acknowledges this power on reset condition. This acknowledgement is performed via the same $\overline{INT}$/ACK pin, which also performs the function of an interrupt acknowledge input. This is made possible due to the fact that the pin has a weak NMOS pulldown which forms a latch. When $\overline{INT}$/ACK is externally driven with a sufficiently strong high signal (as described in the "Electrical Characteristics" section) the state of the latch will be switched and as a result the interrupt condition will be reset.

After the power on reset interrupt has been acknowledged and the DS1227 is in a power on condition, the $\overline{INT}$/ACK pin will be again taken low to signal the detection of active signalling on the $\overline{ON1}$ or SENSE inputs. Further activity on the RXIN input will not cause a subsequent interrupt condition. The $\overline{INT}$/ACK can be returned to its high (reset) state again by externally driving it with a sufficiently strong high signal.

The $\overline{OFF1}$ input is used to turn off the V_{CCO1} output under software control. It is typically interfaced to the system microcontroller via a port pin configured as an output. As noted above, it is active only when V_{CCO1} is on and $\overline{INT}$/ACK has been set high.

STIMULUS INPUTS

$\overline{ON1}$ is a simple TTL-level compatible input which is designed to detect a negative-going edge. V_{CCO1} is kickstarted whenever an active edge is detected on this pin.

The RXIN input can be used to initiate the kickstarting action in response to the detection of incoming serial data. In this configuration, the RXIN pin is interfaced to an incoming serial data line, typically from an RS232 transceiver. RXOUT is the corresponding output and is used to route the serial data to the microcontroller. RXIN remains internally disconnected from RXOUT until V_{CCO1} is powered on. At that time, the two lines are connected and serial data is passed straight through the device to the microcontroller.

The SENSE pin is intended to be connected to an external sensor circuit which is powered from V_{CCO4}. This circuit is then momentarily powered from the Kickstarter's V_{CCO4} output in response to a negative going edge applied to the $\overline{ON4}$ input. V_{CCO4} will stay powered for an amount of time determined by the circuitry on the MODE4 pin. During the time that V_{CCO4} is on, the SENSE pin has an internal pulldown device which is activated. SENSE is sampled just prior to the V_{CCO4} output being disconnected. If SENSE is externally driven high (V_{IH}) at this time, it kickstarts V_{CCO1} power. Any time that V_{CCO4} power is off, the SENSE pin appears as a high impedance to external circuitry.

The amount of time that V_{CCO4} is on is determined by the configuration of the MODE4 pin. MODE4 is intended to either be tied high (typically to V_{DCO}) or tied to an external capacitor. The V_{CCO4} on time is thereby determined either by the amount of time between falling edges on $\overline{ON4}$ or by the value of the capacitor.

If the MODE4 pin is tied high at the time that $\overline{ON4}$ is activated, then V_{CCO4} will remain on until the next falling edge is detected on $\overline{ON4}$. Figure 5 illustrates the timing associated with this mode of operation. If the Kickstarter is also configured for boost regulation and V_{CCO1}, V_{CCO2}, and V_{CCO3} are turned off, the DC-DC converter will be briefly enabled so that +5V will be supplied on V_{CCO4} for the duration of the time that it is on.

The alternative MODE4 configuration is illustrated in Figure 6A. As shown in the figure, it is recommended for most applications that a large resistor also be connected between MODE4 and ground in addition to the capacitor. For the configuration shown, the MODE4 pin will be sensed low by the Kickstarter just following the negative-going edge at $\overline{ON4}$. Following this condition, a constant current specified as I_{M4ON} is supplied out of the MODE4 pin. This will cause the voltage on MODE4 to rise linearly. V_{CCO4} will remain on until the voltage on MODE4 reaches a threshold specified as VM4OFF (approximately 0.5 V_{DCO}). At this time, V_{CCO4} will be shut off. At the same time, the constant current source on the MODE4 pin will be disconnected and an internal resistive element (specified as R_{M4DIS}) will be connected between the MODE4 pin and ground. This internal resistive element along with any external resistance will cause the voltage on the capacitor to decay exponentially until it reaches a threshold specified as V_{M4DIS} (approximately 0.1 V_{DCO}). When this condition is reached, the internal resistive element will be disconnected, and the MODE4 pin will appear as a high impedance until the next active transition occurs on $\overline{ON4}$. The external re-

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sistor (if present) will then cause the voltage on MODE4 to further decay until it reaches ground or until the next $\overline{ON4}$ negative transition, whichever comes first.

When MODE4 is initially grounded as described above, V_{CCO4} power is switched from the V_{DCO} pin, regardless of whether or not V_{CCO1}, V_{CCO2}, or V_{CCO3}, are powered on. This means that V_{CCO4} will be switched with the voltage present on V_{DCO}, which could be from +3V to +5V depending on the configuration, input battery voltage used, and whether or not V_{CCO1}, V_{CCO2}, or V_{CCO3} are switched on.

The above described sampling operation of V_{CCO4} and SENSE in response to $\overline{ON4}$ also takes place when a kickstart has already occurred and V_{CCO1} is on. If SENSE is found to be active in this condition, an interrupt will be signalled on the INT/$\overline{ACK}$ pin.

MICRO ENERGY MANAGEMENT

In addition to the kickstarting features described above, the DS1227 allows sections of system circuitry to be individually powered up or down under command of the microcontroller. This capability is referred to as the Micro Energy Management feature of the DS1227.

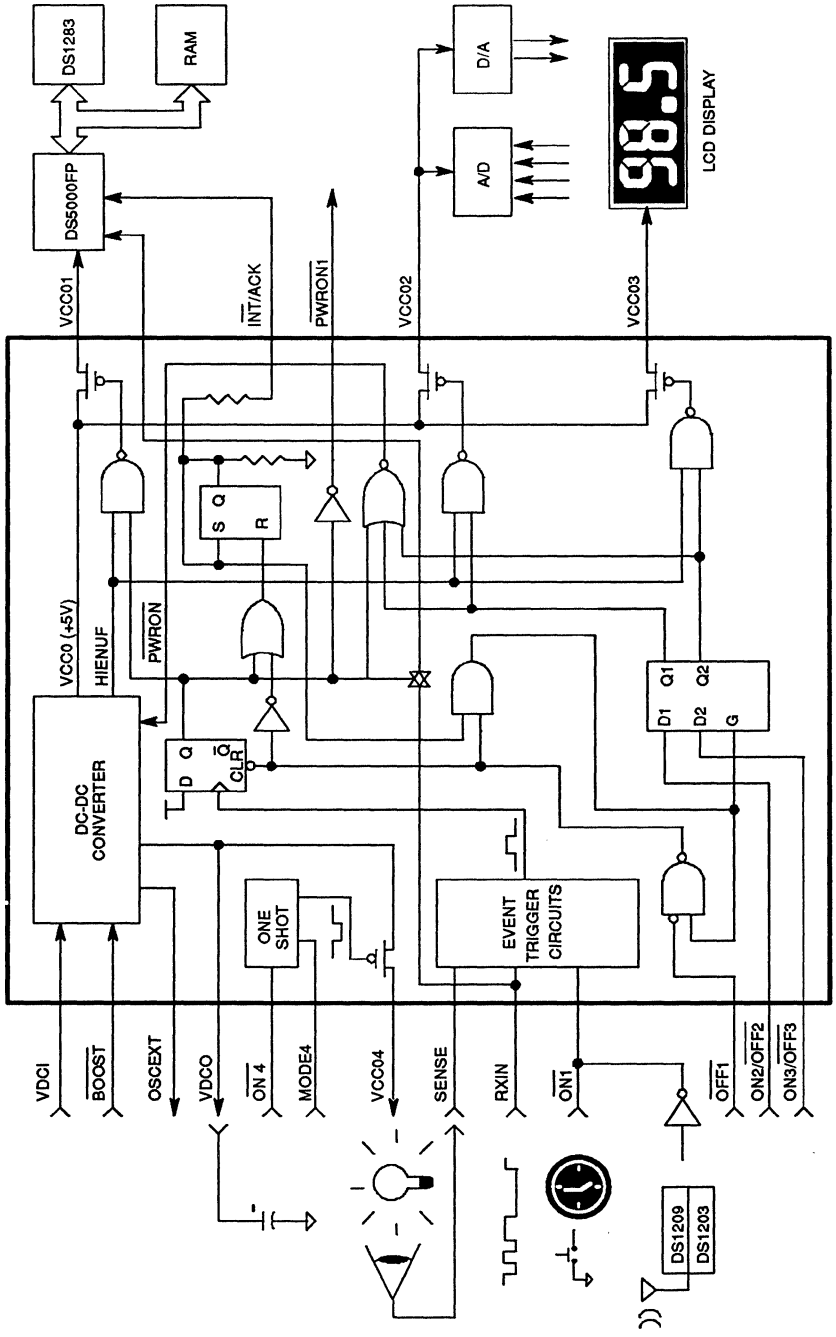
V_{CCO2} and V_{CCO3} are auxiliary power supply outputs which may be switched on or off via the ON2/$\overline{OFF2}$ and ON3/$\overline{OFF3}$ pins, respectively. The ON2/$\overline{OFF2}$ and ON3/$\overline{OFF3}$ control pins are intended for connection to two microcontroller's port pins configured as outputs. The corresponding V_{CCO} output pins can then be turned on or off as desired under control of the system application software.

The ON2/$\overline{OFF2}$ and ON3/$\overline{OFF3}$ inputs are level activated. The corresponding V_{CCO} output therefore turns on when the on/off pin is high and off when it is low. These inputs are active only if the V_{CCO1} output is on and the $\overline{INT}$/ACK output has been set to a high state signalling a power on reset condition.

When V_{CCO2} or V_{CCO3} are turned on, they will remain on until the corresponding control input is taken low by the software. This is true even if the $\overline{OFF1}$ input is taken to its active low state at the time that either ON2/$\overline{OFF2}$, ON3/$\overline{OFF3}$, or both, are high.

Once $\overline{OFF1}$ is activated, the current states of ON2/$\overline{OFF2}$ and ON3/$\overline{OFF3}$ are internally latched and further activity on these pins is ignored. If both of the corresponding outputs (V_{CCO2} and V_{CCO3}) are turned off at this time and boost operation has been selected, then the internal oscillator is killed and the DC-to-DC converter will be shut down. If either V_{CCO2} and/or V_{CCO3} are left switched on when $\overline{OFF1}$ is activated, they will remain switched on even after V_{CCO1} has been turned off. If the DS1227 has been configured for boost operation, the DC-to-DC converter will remain operational during the entire time that V_{CCO1} is turned off so that +5 volts will continue to be supplied on either or both of these output pins. These pins can be shut off only when kickstarting occurs once again and V_{CCO1} is switched on and $\overline{INT}$/ACK has been set high.

DS1227 KICKSTARTER BLOCK DIAGRAM Figure 4



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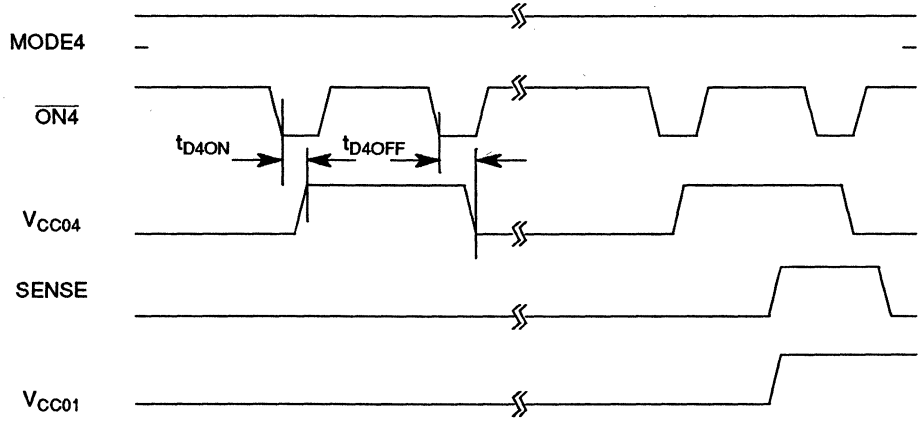
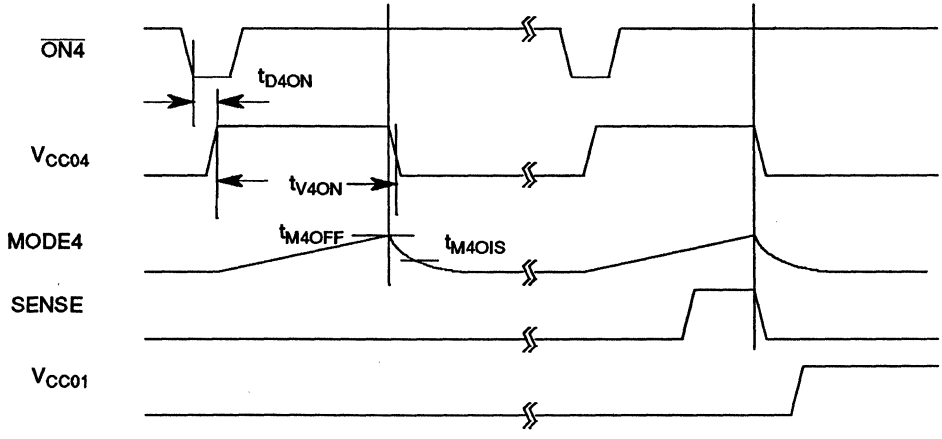
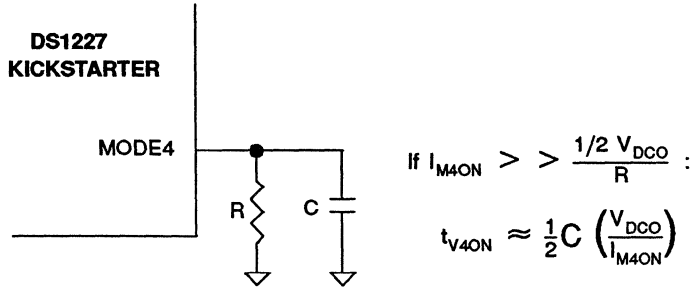
SENSE INPUT TIMING; MODE4 STRAPPED HIGH Figure 5



MODE4 RC NETWORK CONNECTION Figure 6A



SENSE INPUT TIMING; MODE4 WITH RC NETWORK Figure 6B



BOOST MODE OPERATION

The DS1227 Kickstarter incorporates all of the necessary control and power switching functions required for its +3V to +5V step-up DC-to-DC converter. These functions include a bandgap reference, oscillator, voltage comparator, catch diode and an N-channel MOSFET. The only external components required are an output filter capacitor and a low cost inductor. The block diagram shown in Figure 7 illustrates the DC-to-DC converter.

When kickstarting occurs from an initial powered down state (i.e., V_{CCO1}, V_{CCO2}, and V_{CCO3} turned off), an internal start sequence is initiated within the DS1227. During this sequence, the V_{CCO1} output remains shut off and the $\overline{BOOST}$ pin is sampled in order to determine if the DS1227 is configured for boost mode operation. If $\overline{BOOST}$ is low, then boost mode operation is enabled and the DC-to-DC converter is started.

The internal DC-to-DC converter is started by enabling the on-chip 40 KHz oscillator. It then begins to build up the voltage on the V_{DCO} filter capacitor. Internal counter logic insures that the DC-to-DC converter stays in start mode for a minimum of six clock periods (nominally 150 µs @ 40 KHz). After this initial delay time, the V_{DCO} output is monitored by the internal Error Comparator as it slews up to V_{DCON}. As long as the V_{DCO} voltage remains below the preset value, the Error Comparator will be switched high and the internal 40 KHz oscillator will be connected to the gate of the V_{DCI} driver.

The V_{DCI} driver is a large N-channel MOSFET with a typical ON resistance of less than 4 Ohms and is capable of supplying a peak current of 450 mA. The output device is turned on during each ON half-cycle generated by the internal square-wave oscillator, and is turned off during each OFF half-cycle. During each ON half-cycle, the current through the inductor rises linearly, storing energy in the coil. When the output device is turned off, the external inductor's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at V_{DCI} then rises until the internal diode is forward biased, delivering power to the V_{DCO} output. The converter is thereby powered from its own V_{DCO} output. This is often referred to as "bootstrapped" operation, since the circuit figuratively "lifts" itself up. In order to guarantee that the Kickstarter can bootstrap itself up to operating voltage, the V_{DCI} voltage must be at the minimum level of V_{DCISU} as listed in the DC characteristics section of this data sheet.

When the voltage on V_{DCO} rises to the V_{DCON} threshold, the internal signal called "HIENUF" will be active and the V_{CCO1} PMOS device is switched on. As noted above, internal circuitry insures that this device will not be switched on for a minimum of 6 clock cycles from the time that the DC-to-DC converter is started. However, since the recommended values for the external LC components result in a time constant which is much longer than six cycles, the actual slew rate will in practice be much longer than this delay time.

If loading of the V_{CCO} outputs causes V_{DCO} to drop below V_{DCOFF} the DS1227 will deactivate HIENUF and the V_{CCO1} PMOS device as well as the other V_{CCO} PMOS devices will be switched off. The V_{DCO} voltage will then be monitored for the V_{DCON} trip point before reconnecting the load. As a result, the power control regulation loop could oscillate between these two states until the V_{CCO1} node had sufficient charge to remain above the V_{DCOFF} threshold. To prevent this from occurring, the value of the filter capacitor must be sufficiently large. For large capacitive loads on V_{CCO1} the output may dip below V_{DCOFF} as a result of charge sharing and a larger regulation capacitor at V_{DCO} may be required. For large resistive loads the inductance and capacitance values may need to be adjusted using a smaller inductor value and large capacitance. In order not to violate the peak V_{DCI} current it may be necessary to use the external oscillator OSCEXT to drive an additional switchmode boost regulator, as shown in Figure 8.

Following the above described start sequence, normal boost operation is performed by the converter. V_{DCO} output voltage is constantly monitored by the error comparator. When V_{DCO} voltage drops below the preset value, the error comparator switches high and connects the internal 40 KHz oscillator to the gate of the V_{DCI} output driver. When the output voltage reaches the desired level, the error comparator inhibits the V_{DCI} output driver until the load on V_{CCO1} discharges the output filter capacitor to less than the desired output level.

INDUCTOR SELECTION

The available output current from the Kickstarter's on-chip DC-DC boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most applications, the inductor is the only design variable since the internal oscillator is preset to a fixed value of 40 KHz. The proper inductor must have the following characteristics:

1) the correct inductance value must be selected.

2) the inductor must be able to handle the required peak currents.

3) the inductor must have acceptable series resistance and must not saturate.

When the internal N-channel MOSFET turns on, the current through the inductor rises linearly since:

$$\frac{di}{dt} = \frac{V}{L}$$ where L is the inductance value

At the end of the on-time, t_{ON}, the peak current, I_{PK} is:

$$I_{PK} = \frac{V\ t_{ON}}{L} \text{ where : } t_{ON} = \frac{1}{2f_O}$$

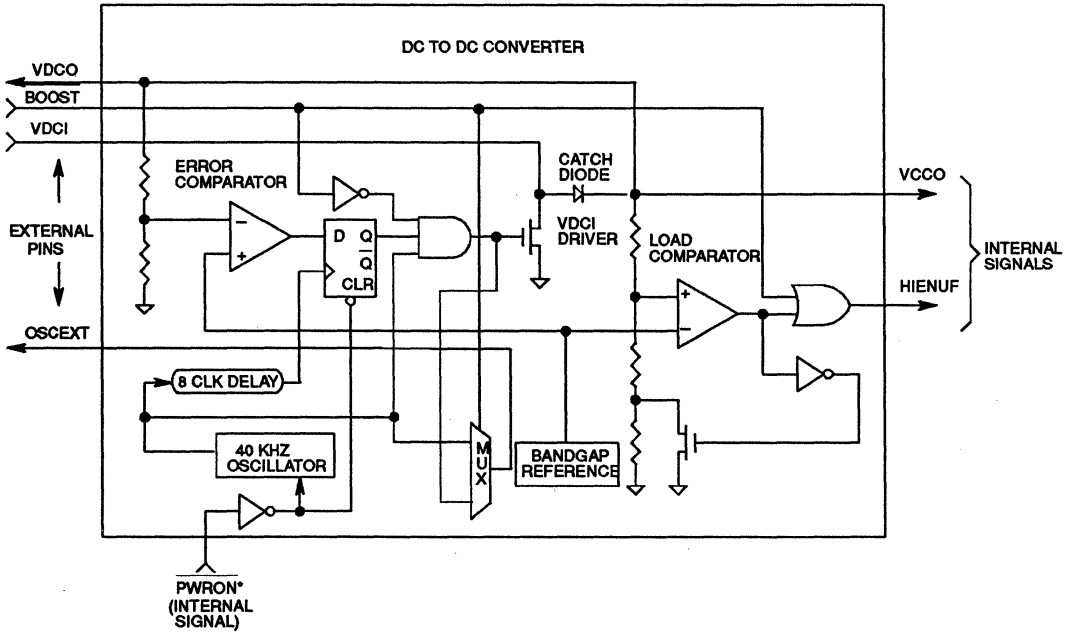
The energy in the inductor is:

$$E_L = \frac{L\ I_{PK}^{\ 2}}{2}$$

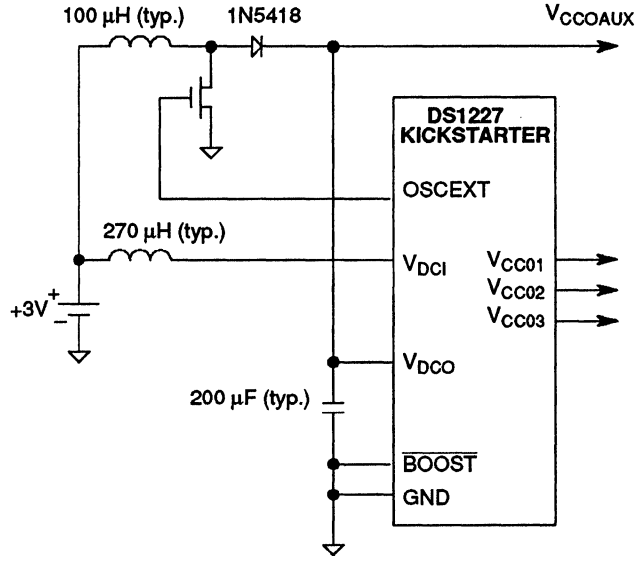
At maximum load this cycle is repeated f_0 (typically 40 KHz) times per second, and the power transferred through the coil is $P_L = f_0 \times E_L$. Since the coil only supplies the voltage above the input voltage:

$$I_{OUT} = \frac{P_L}{V_{OUT} - V_{IN}}$$

DC-DC CONVERTER Figure 7



AUXILIARY BOOST SUPPLY CONFIGURATION Figure 8



The DC-DC converter's output current is provided both by the inductor and directly from the battery. If the load draws less than the maximum current, the V_{DCI} n-channel MOSFET is turned on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the DS1227 will not be able to deliver the desired output power, even with the MOSFET turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

$$L_{MAX} = \frac{V_{IN}^2}{8\, f_O\, P_L}$$

$$\text{since : } P_L = \frac{L\, I_{PK}^2\, f_O}{2} \text{ and : } I_{PK} = \frac{V_{IN}}{2}\, f_O\, L$$

The required output power must include what is dissipated in the forward drop of the catch diode and each of the V_{CCO1}, V_{CCO2}, and V_{CCO3} pass transistors. This can be expressed as follows:

$$P_{OUT} = V_F\, I_{OUT} + (I_{OUT12}\, R_{ON1} + I_{OUT2}^2\, R_{ON2} + I_{OUT3}^2\, R_{ON3} + I_{OUT42}\, R_{ON4}) + V_{OUT}\, I_{OUT}$$

where:

$$I_{OUT} = I_{OUT1} + I_{OUT2} + I_{OUT3} + I_{OUT4}$$

If the inductance value is too low, the current at V_{DCI} may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}}{2\, f_O\, I_{MAX}} (I_{MAX} + 450\ mA)$$

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TYPES OF INDUCTORS

The following is a brief discussion of various types of inductors which may be typically used with the DS1227 Kickstarter to facilitate boost mode operation. Table 1 lists some typical manufacturers of these types of inductors. Table 2 summarizes performance of the circuit for various inductors.

Molded Inductors

These are cylindrically wound coils which look similar to 1-watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types of inductors.

Potted Toroidal Inductors

A typical 1 mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685 in diameter by 0.385 high and

mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode power supply applications since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production, the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective core area differs between the post, side, top, and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permally powder (MFP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

COIL AND CORE MANUFACTURERS Table 1

TYPE	TYPICAL MANUFACTURER	PART #	DESCRIPTION
Molded	Dale	1HA-104	500 µH, 0.5 ohms
"	Cadell-Burns	7070-29	220 µH, 0.55 ohms
"	Gowanda	1B253	250 µH, 0.44 ohms
"	Nytronics	WEE-470	470 µH, 10 ohms
"	TRW	LL-500	500 µH, 0.75 ohms
Potted Toroidal	Dale	TE-3Q4TA	1 mH, 0.82 ohms
"	Gowanda	050AT1003	100 µH, 0.05 ohms
"	TRW	MH-1	600 µH, 1.9 ohms
"	Torotel Prod.	PT 53-18	500 uH, 5 ohms
Toroidal Core	Allen Bradley	T0451S100A	500 nH/T^2
"	Siemans	B64290-K38-X38	4 µH/T^2
"	Magnetics	555130	53 nH/T^2
Ferrite Core	Stackpole	57-3215	14 mm x 8 mm
"	Magnetics	G-41408-25	14 x 8, 250 nH/T^2

Note: This list does not constitute an endorsement by Dallas Semiconductor and is not intended to be a comprehensive list of all manufacturers of these components.

INDUCTOR SELECTION FOR COMMON DESIGNS Table 2

V_{IN} (V)	V_{DCO} (V)	I_{OUT} (mA)	EFF. (%)	INDUCTOR		
				PART #	uH	Ohms
2	5	5	78	CB 6860-21	470	0.4
2	5	10	74	G 1B253	250	0.44
2	5	15	61	G 1B103	100	0.25
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55

Note: CB = Cadell-Burns, NY (516) - 746 -2310
G = Gowanda Electronics Corp., NY (716) - 532-2234
Other manufacturers listed in Table 1.

OUTPUT FILTER CAPACITOR

In boost regulation mode, the DS1227's output voltage ripple on V_{DCO} has two components, with approximately 90° phase difference between them. One component is created by the change in the capacitor's stored charge with each output pulse. The other ripple component is the product of the capacitor's charge/discharge current and its ESR (Effective Series Resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than that caused by the change in charge.

$$V_{ESR} = I_{PK} \times ESR = \frac{V_{IN}}{2Lf_O} \times ESR \text{ (Volts p – p)}$$

Where V_{IN} is the coil input voltage, L is its inductance, f is the oscillator frequency, and ESR is the equivalent series resistance of the filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C} \text{ where, } Q = \frac{t_{DIS} \times I_{peak}}{2}$$

$$\text{and, } I_{peak} = \frac{t_{CHG} \times V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN} \times t_{CHG} \times t_{DIS}}{2LC}$$

Where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor 1/2 f_O can be used for nominal calculations).

High quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved in the 100 to 500 µF range, in parallel with a 0.1 µF ceramic capacitor.

OSCEXT FUNCTIONS

The OSCEXT pin is connected to the internal 40 KHz oscillator (nominal frequency). When Boost mode is enabled ($\overline{BOOST}$ = 0) and the DC-to-DC converter is running, OSCEXT is active at the same time whenever the error comparator is switched high, i.e., whenever the internal oscillator is enabled to the gate of the V_{DCI} driver. In this configuration it may be used to drive an auxiliary switch mode boost regulator as shown in Figure 8. In this circuit, OSCEXT drives an external NMOS switch with its drain pin connected to an additional inductor and filter capacitor as well as an external catch diode. The amount of supply current which can be realized at the +5V output is determined by the power ratings of the external components. Through proper selection of the these components, increased supply current can be realized than is possible using the Kickstarter's internal V_{DCI} driver and catch diode.

When the Pass-Through mode is enabled ($\overline{BOOST}$ = 1) and at least one of the V_{CCO} outputs is switched on, the OSCEXT pin will be continuously driven with the 40 KHz frequency. In this configuration this pin could potentially be used to generated negative or doubled voltages as shown in Figure 9.

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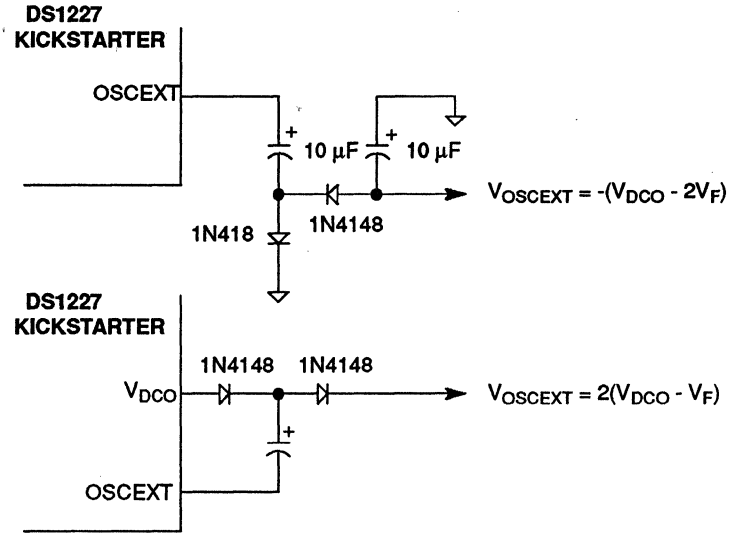
VOLTAGE INVERTOR AND DOUBLER CONFIGURATIONS Figure 9



NOTE: V_F = FORWARD 1N418 DIODE VOLTAGE

APPLICATION BRIEF

The schematic shown in Figure 10 illustrates a typical application of the DS1227 Kickstarter in a microcontroller-based, battery powered system. Together with the Kickstarter, the system incorporates a DS5000FP Soft Microcontroller, a DS1283 Watchdog Timekeeper, and a DS1275 Line Powered RS232 Transceiver. Although the system is not designed to serve a specific application, this chip set could serve the majority of requirements for many types of hand-held instruments.

Using the illustrated configuration provides the following major features:

- Permanently powered operation from a +3V source for many applications
- Data and event logging with time stamp and date
- Reprogrammable through RS232 serial interface
- Buttonless (autonomous) operation for many tasks

COMPONENT DESCRIPTION

The DS5000FP is an 8-bit microcontroller which is instruction set-compatible with the industry standard 8051. It provides an embedded interface to 32 Kbytes of nonvolatile static RAM which can be dynamically partitioned for program and data storage, and may be loaded at any time via the on-chip serial port. With proper selection of RAM and the backup lithium source, nonvolatile storage can be maintained for over 10 years in the absence of V_{CC}. The DS5000FP offers the standard low power operating and standby modes (i.e., Idle, Stop). More importantly, sophisticated crashproof circuitry in conjunction with the lithium energy source allows it to retain its entire operating state for the duration of a power outage without drawing current from its V_{CC} line.

Timekeeping is provided by the DS1283 Watchdog Timekeeper. Incorporating a self-contained clock and calendar, the DS1283 tracks hundredths of seconds, seconds, minutes, hours, days, date of the month, month, and years. When its chip enable is inactive (no read or write), the DS1283 consumes extremely low current, typically 500 nA. Two alarm functions are provided: a time-of-day Alarm, and a watchdog alarm. The time-of-day Alarm can generate an interrupt pulse up to one week in advance of the current time. The watchdog alarm can produce an interrupt at regular intervals ranging from .01 seconds to 99.99 seconds. Both alarms function when the part is operating in low power standby mode.

The DS1275 Line Powered RS232 Transceiver allows the instrument to communicate with the RS232 port on a host computer (e.g., COM port on an IBM PC). It operates from a +5V supply and draws no power from the instrument's main energy source to create negative voltages. Instead, it steals power from the incoming RXD line to generate the negative voltages needed during transmission.

INSTRUMENT OPERATION

A common requirement of instruments is event logging with time stamp and date. The Dallas chip set provides this capability using the DS5000 and DS1283. The DS1283 interfaces directly to the DS5000FP embedded bus, and may be accessed by $\overline{CE2}$. In this way, valuable port pins are conserved. Events can be recorded by the microcontroller and logged in RAM with the date and time. In the absence of V_{CC}, the data will be retained in RAM by the backup lithium cell. The same energy cell provides backup to the DS1283, so that timekeeping is maintained in the absence of a primary energy source. Therefore, events may be time stamped and dated with confidence that the correct time has been maintained. Backup lithium current is managed by the DS5000FP and is distributed from the V_{CCO} line in the absence of V_{CC}.

PERMANENTLY POWERED OPERATION

In order to achieve permanently powered operation, Dallas Semiconductor uses several techniques which conserve the life of a primary energy source. First, the illustrated chip set operates at extremely low power. These components are also capable of very low power data retention. Second, the crashproof circuitry of the DS5000 allows V_{CC} to be removed and restored without disruption. This allows the energy management circuits of the Kickstarter to power down the microcontroller during periods when it is unused. Since the DS1227 can monitor external events and wakeup the DS5000 as necessary, the microcontroller and other circuitry may remain in low power data retention mode until needed. The DS5000, RAM, and DS1283 will be backed up via the button cell as show in Figure 1. Finally, the Kickstarter allows software-controlled powering of auxiliary circuits when tasks require them.

Low operating power is a basic requirement of battery-operated systems. The illustrated Dallas chip set can perform most instrument functions using minimal power. Using a 3.57 MHz crystal, the circuit in Figure 1 will draw approximately 8 mA during microcontroller operation. When the Kickstarter turns off the DS5000, the circuit draws approximately 5 µA from the primary energy source. If a similar configuration were created with an ordinary CMOS microcontroller in stop mode, the current could be as high as 55 µA. Idle mode operation would consume approximately 3 mA, which would excessively drain a primary power source over extended periods. The Dallas low power chip set provides a ten-to-one improvement over previously available alternatives.

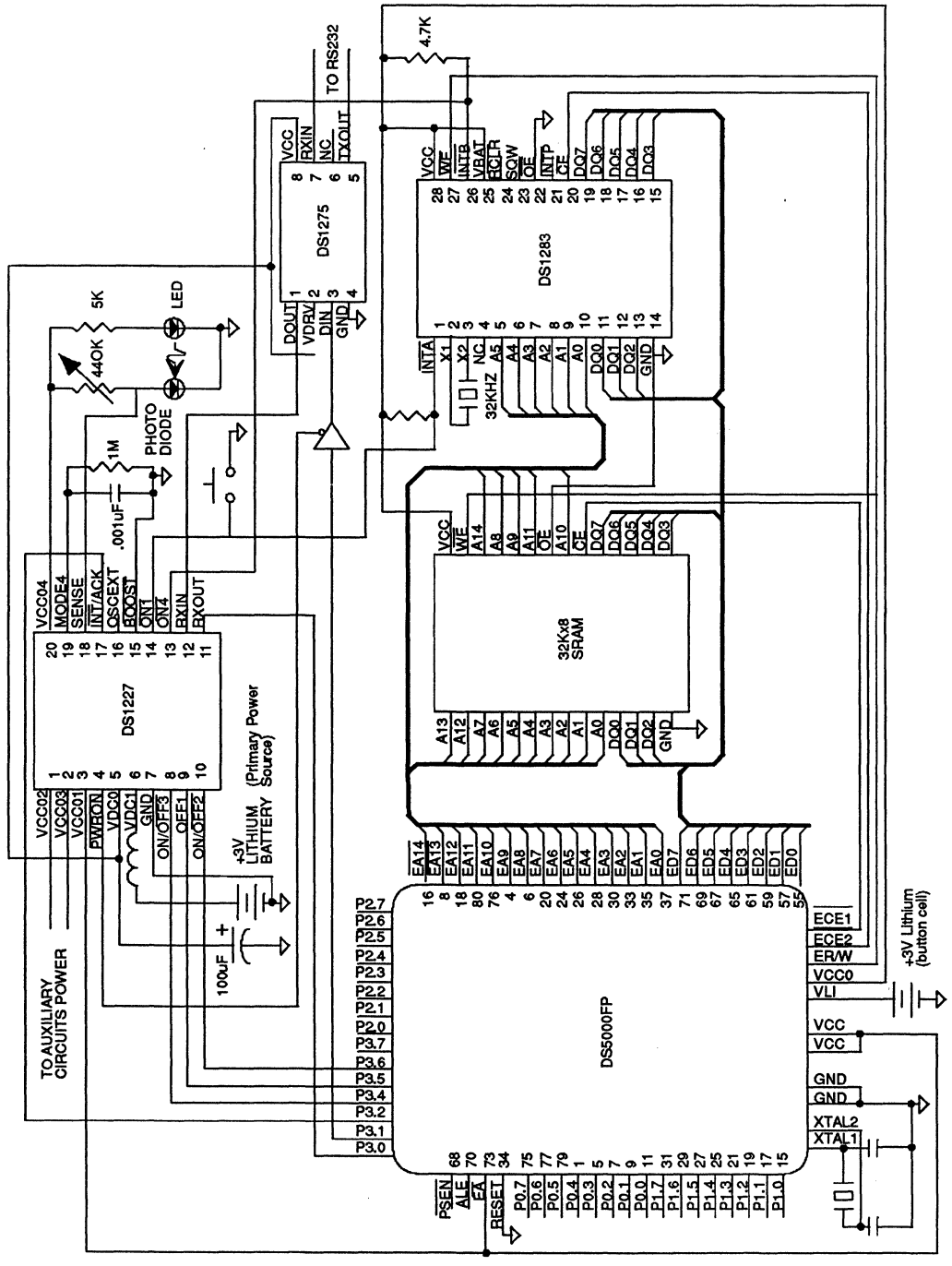
Achieving the lowest power instrument requires the DS1227 Kickstarter. Using the Kickstarter, low power operation is achieved by powering down the microcontroller. When this occurs, the DS5000 effectively consumes zero power. RAM and key registers are backed by the lithium button cell, with no power draw from V_{CC}. When a task must be performed, the Kickstarter powers up the DS5000 to execute a function and powers it down when the function is complete (under software direction). The period for which power remains on is minimized in this way. Since most tasks require minimal processing time with long periods of waiting, the instrument may remain in a low power data retention mode for the majority of time. Therefore, even if an operator interface is necessary, the microcontroller can remain on for milliseconds (or microseconds) to perform a task, and remain off for the seconds between operations.

The ability to react to external stimuli allows the instrument to operate autonomously for many applications. Fundamental to this operation is the kickstart caused by external stimuli. The following section describes the operation of the Kickstarter with respect to four different stimuli.

KICKSTARTING OPERATION

The DS1227 receives primary power from a +3V lithium battery. Prior to a kickstart, battery voltage is present on V_{DCO}, which is the main voltage output. When the system receives a kickstart stimulus, an on-chip boost regulator raises V_{DCO} to +5V. Upon completion of power up, +5V is switched to the DS5000 on V_{CC01}. Prior to kickstart, no power was supplied to this line.

TYPICAL APPLICATION OF DS1227 KICKSTARTER Figure 10



The schematic in Figure 1 demonstrates four kickstart stimuli. They are real time clock alarm, RS232 incoming data, a sensor input, and a user switch. During the low power standby prior to kickstart, V_{CCO} from the DS5000 provides battery power to the RAM and real time clock from the button cell. V_{DCO} supplies the RS232 transceiver. While operating on battery power, the RTC can still issue alarms. If a time of day alarm is programmed, $\overline{INTA}$ will be taken low by the RTC when the alarm occurs. Th is is connected to $\overline{ON1}$, and issues a Kickstart.

Incoming RS232 activity will allow the transceiver to Kickstart the DS1227. Following the initial interrupt, all additional RS232 data is passed through the RXIN/RXOUT pins of the DS1227 to the DS5000 without further action. In this way, the instrument can collect a table of data and dump it to a PC for analysis when necessary. Since the instrument will kickstart when it detects RS232 communication, it is unnecessary for an operator to take further action. Enough time should be allowed for the DS5000 to complete a power-on reset before sending meaningful data.

Two additional methods of kickstarting are illustrated. One method involves the use of a sampled sensor. A periodic pulse (the watchdog alarm) from the DS1283 causes V_{CC04} to be applied to the LED. For example, this might occur every 250 ms. It remains on for the time it takes to charge the capacitor on Mode4 to 1/2 V_{DCO} (1.5V). In this example, the on period is approximately 75 µsec. Just prior to removing V_{CC04}, the sense line is sampled. If the LED light path to the photodiode is blocked, the sense line will be high and the system will be kickstarted. If the light path is clear, the sense line will be low, and nothing will happen. This facilitates checking for the presence of an ID card in a reader. In the other method a user switch, which is momentarily closed, will start the system. This is tied to $\overline{ON1}$ in a wired-OR configuration. All of the above kickstart stimuli cause the boost regulator to raise V_{DCO} and turn on V_{CC01}. In summary, the four kickstart stimuli are:

1) Time of Day Alarm - $\overline{INTA}$ goes low and Kickstarts V_{CC01}.
2) RS232 Activity - Powers up V_{CC01} and routes all RS232 straight through to the DS5000.
3) $\overline{INTB}$ goes low periodically, V_{CC04} turns on, and the sense line is sampled. If high, a kickstart occurs. If low, no action.
4) A user switch momentarily pulls $\overline{ON1}$ low and kick starts.

Although the user switch is easily implemented, it may be unnecessary. By allowing the instrument to power up and determine the cause of the Kickstart, it is possible to achieve buttonless operation in many applications. Automatic response allows the instrument to function autonomously and save power by turning off unused circuits.

Once the DS5000 receives power, it must read the $\overline{INT}$/ACK line (tied to $\overline{INT0}$). A power-on condition causes this signal to be low. The DS5000 port pin should then acknowledge power up by driving this line high. This recognizes the interrupt and enables the kickstarter for further activity. The DS5000 may now turn on auxiliary loads V_{CC02} and V_{CC03} using ON/$\overline{OFF}$ 2 and 3 (tied to any port pins). These auxiliary supplies may supply circuits which are not always necessary (e.g. an A/D converter). Peripheral circuits remain powered down until needed. After an operation is complete, the DS5000 can turn off the auxiliary circuits. When processing of a task is complete, it may turn itself off using $\overline{OFF1}$. An application may require that an auxiliary circuit remain on when the microcontroller is off. This might occur with an LCD display or dual slope A/D converter. Since the dual slope A/D takes a relatively long period to convert (40-50 mS), the microcontroller may be powered down while waiting.

Since the INT/$\overline{ACK}$ line is tied to INT0, additional kickstart stimuli which occur while VCC01 is on will cause the DS5000 to receive an interrupt. This allows the DS5000 to take action for specific conditions.

Precautions against excessive current drain are taken in this application. For example, the data input to the DS1275 RS232 transceiver is tri-stated when VCC01 is off. This is necessary to prevent a high signal from driving the RS232 bus and consuming power while the DS5000 is off. Similar precautions should be taken by the user in designing systems with switched power supplies.

ABSOLUTE MAXIMUM RATINGS *

Input Voltage on any Pin Relative to Ground	-0.3 to 7.0V
V_{DCI} Peak Input Current	450 mA
Power Dissipation	
Plastic DIP (derate 7.41 mW/°C above +50°C)	- 555 mW
Small Outline (derate 12.5 mW/°C above +50°C)	- 937 mW
Operating Temperature	0° to +70°C
Storage Temperature	-55°C to +125°C
Lead Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

(t_A = 0° C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Startup Voltage	V_{DCISU}	1.8			V	1
V_{DCO} Voltage Threshold for V_{CCO} Turn-ON	V_{DCON}	4.38	4.50	4.62	V	
V_{DCO} Voltage Threshold for V_{CCO} Turn-OFF	V_{DCOFF}			3.00	V	
Operating Supply Current ($\overline{BOOST}$=0) ($\overline{BOOST}$=1)	I_{CC}		1.5 0.5	3.0 1.0	mA mA	4 2
Standby Supply	I_{SB}			200	nA	
V_{CCO1} DC Source Current (V_{CCO1} = V_{DCO} -0.25V)	I_{CCO1}			100	mA	2, 7
V_{CCO2}, V_{CCO4} DC Source Current (V_{CCO2}, V_{CCO4} = V_{DCO} - 0.25V)	I_{CCO2} I_{CCO4}			50	mA	2, 7
V_{CCO3} Source Current (V_{CCO3} = V_{DCO} - 0.25V)	I_{CCO3}			10	mA	2, 7
V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4} Voltage	V_{OUTB}	4.75	5.00	5.25	V	1, 4
V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4} Voltage	V_{OUTP}	V_{DCO} -0.25			V	2
V_{CCO4} Voltage	V_{OUT4}	V_{DCO} -0.25			V	
V_{CCO1} ON Resistance	R_{VCCO1}			2.5	Ohms	
V_{CCO2}, V_{CCO4} ON Resistance	$R_{VCCO2,4}$			5.0	Ohms	
V_{CCO3} ON Resistance	R_{VCCO3}			25	Ohms	
Efficiency			80		%	1, 8

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Line Regulation $+0.5V_{CCO} < +V_S < V_{CCO}$	V_{CCO}			0.4	%	1
Oscillator Frequency			40		KHz	
Oscillator Duty Cycle			50		%	
OSCEXT ON Resistance	R_{OSCEXT}		50	75	Ohms	
V_{DCI} Driver ON Resistance (@ I_{VDCI} = 100 mA)	R_{VDCION}		6	12	Ohms	1
V_{DCI} Driver OFF Leakage Current (t_A = 25° C)	I_{VDCIL}			30	µA	1
Catch Diode Forward Voltage	V_F			1.0	V	
Output Low Voltage, (OSCEXT, $\overline{PWRON1}$) I_{OL} = 1.6 mA	V_{OL}			0.45	V	
Output High Voltage (OSCEXT, $\overline{PWRON1}$) I_{OH} = -80 µA	V_{OH}	2.4			V	
Input Low Current ($\overline{INT}$, ON2/$\overline{OFF2}$, ON3/$\overline{OFF3}$, $\overline{ON4}$, $\overline{BOOST}$)	I_{IL1}	-1.0		1.0	µA	
Input Low Current ($\overline{ON1}$, RXIN)	I_{IL2}	-50			µA	6
Output High Current ($\overline{PWRON1}$)	I_{OH}	-400			µA	
Output Low Current ($\overline{PWRON1}$)	I_{OL}	2.0			mA	
RXIN Current (V_{RXIN} - $V_{RXOUT} \leq$ 500 mV)	I_{RXIN}	10			mA	
$\overline{INT}$/ACK Input Transition Current	I_{ACKT}			± 2.0	mA	5
$\overline{INT}$/ACK Input Leakage Current $0.0 \leq V_{IN} \leq 0.1$, or V_{DCO} - $0.1 \leq V_{IN} \leq V_{DCO}$	I_{ACKL}			± 200	µA	5
SENSE Resistance (V_{CCO4} ON)			250		KOhms	
MODE4 Source Current (MODE4 = 0 when $\overline{ON4}$ goes from 1 to 0)	I_{M4ON}	10	45	80	µA	
MODE4 Source Current Shutoff Voltage	V_{M4OFF}		$0.5V_{DCO}$			
MODE4 Discharge Resistance (Following current source shutoff)	R_{M4DIS}			2	KOhms	
MODE4 Discharge Resistance Shutoff Voltage	V_{M4DIS}			$0.1V_{DCO}$		

NOTES:

1. Applicable only when Boost mode operation is in effect.
2. Applicable only when Pass Through mode operation is in effect.
3. Valid when $2.5V \leq V_{DCO} \leq 5.0V$.
4. Measured with Boost Mode operation in effect; $I_{CCO1} = I_{CCO2} = I_{CCO3} = I_{CCO4} = 0$. This value represents the amount of current drawn by the DS1227 itself during and does not include current supplied on the I_{CCO} outputs nor does if boost operator includes inefficiencies of DC-to-DC conversion.
5. Input transition current on the INT/$\overline{ACK}$ pin is specified to indicate the amount of current required to switch the pin from a high to a low or from a low to a high condition. Once the pin has switched states, then the leakage current specification is applicable.
6. $\overline{ON1}$ and RXIN have internal weak p-channel pull-up devices.
7. When BOOST operation is in effect, the total combined current supplied out of V_{CCO1}, V_{CCO2}, V_{CCO3}, and V_{CCO4} is limited by the V_{DCI} peak current.
8. Actual efficiency is dependent on external discrete component characteristics.

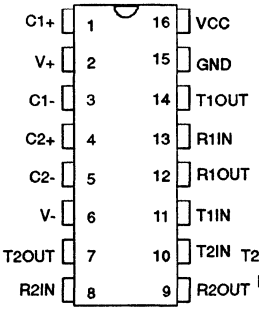
DALLAS SEMICONDUCTOR

DS1228
+5V Powered Dual RS-232 Transmitter/Receiver

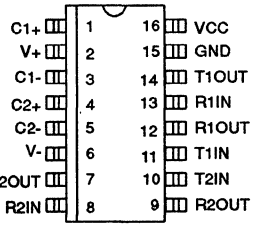
FEATURES

- Operates from a single 5V power supply
- Two drivers and two receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ± 30V input levels
- ± 9V output levels with + 5V supply
- Low-power CMOS
- Pin-compatible with the MAX 232
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16–Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



16–Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

C1+, C1	Capacitor 1 Connections
C2+, C2	Capacitor 2 Connections
V+, V-	± 10 Volts
T1IN, T2IN	Transmitter In
T1OUT, T2OUT	Transmitter Out
R1IN, R2IN	Receiver In
R1OUT, R2OUT	Receiver Out
V_{CC}	+5 Volts
GND	Ground

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DESCRIPTION

The DS1228 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single, +5 volt supply. The DS1228 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate -10 volts. The DS1228 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ± 9V RS-232 outputs. The other two level translators are capable of operating with up to ±30 V inputs. The DS1228 is suitable for all RS-232 communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1228 supplies ± 10 volts from the V_{CC} input.

See the DS1229 data sheet for electrical specifications and operation.

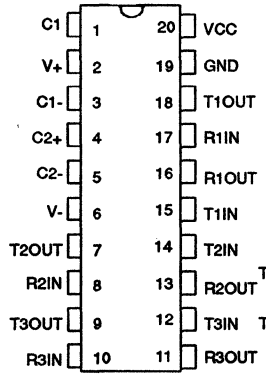
DALLAS SEMICONDUCTOR

DS1229
+5V Powered Triple RS-232 Transmitter/Receiver

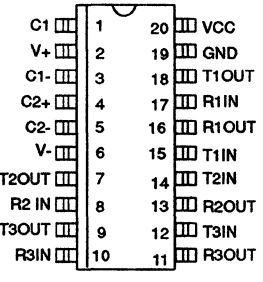
FEATURES

- Operates from a single 5V power supply
- 3 drivers and 3 receivers
- Meets all EIA RS-232-C specifications
- Onboard voltage doubler
- Onboard voltage inverter
- ±30V input levels
- ±9V output levels with ±5V supply
- Low-power CMOS
- Optional 20-Pin SOIC surface mount package

PIN ASSIGNMENT



20-Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg.1



20-Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

C1+, C1-	Capacitor 1 Connections
C2+, C2-	Capacitor 2 Connections
V+, V-	± 10 Volts
T1IN, T2IN, T3IN	Transmitter In
T1OUT, T2OUT, T3OUT	Transmitter Out
R1IN, R2IN, R3IN	Receiver In
R1OUT, R2OUT, R3OUT	Receiver Out
V_{CC}	+5 Volts
GND	Ground

DESCRIPTION

The DS1229 is a triple RS-232-C receiver/transmitter that meets all EIA specifications while operating from a single +5V supply. The DS1229 has two internal charge pumps which are used to generate ±10V. The DS1229 also contains six level translators, three of which are RS-232 transmitters that convert TTL/CMOS inputs into +9V RS-232 outputs. The other three level translators are RS-232 receivers that convert RS-232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS-232-C communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1229 supplies ±10V from the V_{CC} input.

OPERATION

The DS1229 consists of three major sections: a triple transmitter, a triple receiver and a dual charge pump which generates ±10V from the 5V supply.

CHARGE PUMP SECTION

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the V_{CC} input to +10V. The second charge pump uses external capacitor C2 to invert the +10V to -10V. Capacitors C3 and C4 are used to filter the +10V and -10V power supply. The recommended size of capacitors C1-C4 is 22 µF but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the +10V supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1 µF where size is critical.

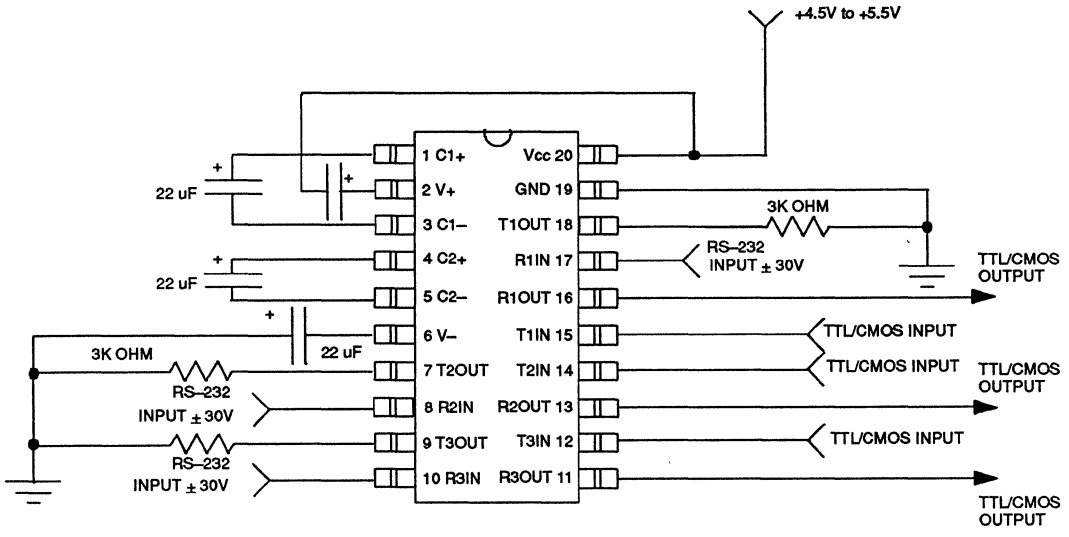
TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal +10V supply. The input is TTL/CMOS-compatible. Each input has an internal 750K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from + 10V to -10V. Worst-case conditions for RS-232-C of ±5V driving a 3K load are met at maximum allowable ambient temperature and a V_{CC} level of 5.0V. Typical voltage swings of ±9V occur with outputs of 5K and V_{CC} equal to 5V. The slew rate at the output is limited to less than 30V/us and the power-down output impedance will be a minimum of 300 ohms with ± 2V applied to the outputs and V_{CC} at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3K ohms and 7K ohms and can withstand up to ±30V with or without V_{CC} applied. The input switching thresholds are within the ±3V limit of RS-232-C specification with a V_{IL} of 0.7V and a V_{IH} of 2.4V. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8V and -30 V.

DS1229 RS-232 TRANSMITTER/RECEIVER Figure 1



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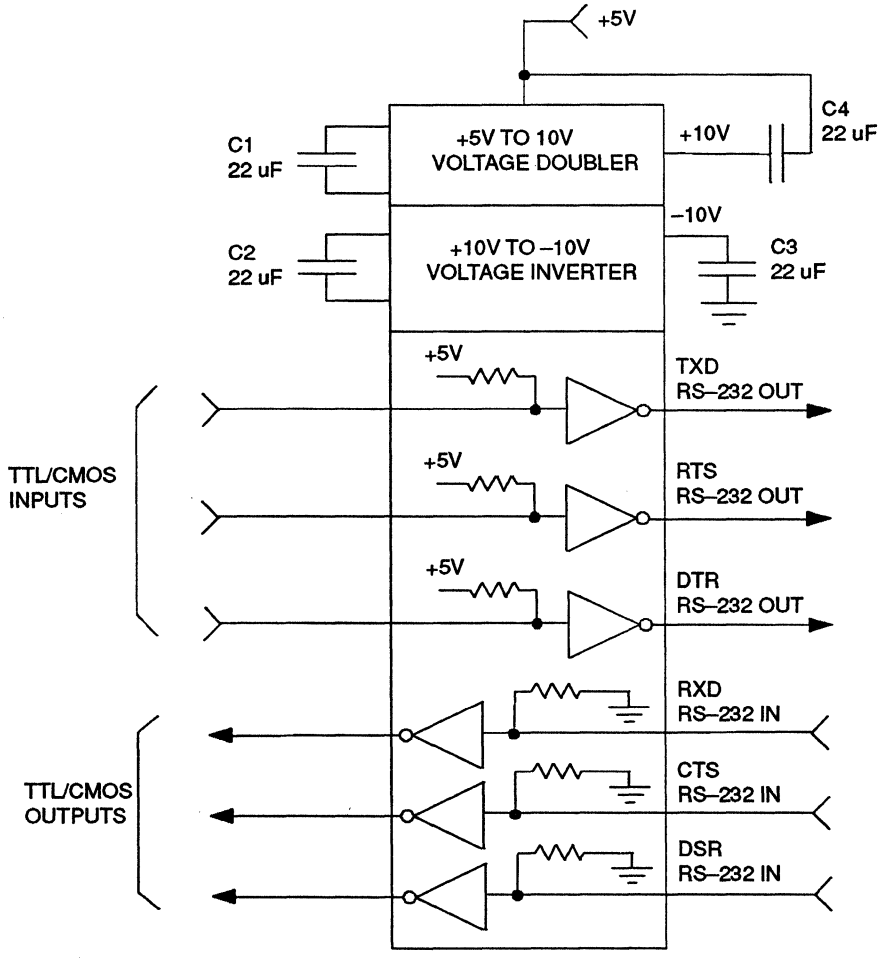
TYPICAL APPLICATIONS Figure 2



ABSOLUTE MAXIMUM RATINGS*

V_{CC}	7.0V
V+	+12 volts
V-	-12 volts
Transmitter Inputs	-0.3V to (V_{CC} +0.3V)
Receiver Inputs	± 30 volts
Transmitter Outputs	(V+ + 0.3V) to (V --0.3V)
Receiver Outputs	-0.3V to (V_{CC} + 0.3V)
Storage Temperature	55°C to 125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
RS-232 Input Voltage	V_{RS}	-30		+30	V	1,2,11

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS-232 Output Voltage	V_{ORS}	±4	± 9	± 10	V	3,12
Power Supply Current	I_{DD}		5	10	mA	4
Transmitter Pull-up Current	I_{TP}		5	200	µA	5
RS-232 Input Threshold Low	V_{TL}	0.7	1.2		V	6
RS-232 Input Threshold High	V_{TH}		1.7	2.4	V	6
RS-232 Input Hysteresis	V_{HY}	0.2	0.5	1.0	V	
Receiver Output Current @ 2.4V	I_{OH}	-1.0			mA	
Receiver Output Current @ 0.4V	I_{OL}			3.2	mA	
Output Resistance	R_{OUT}	300			ohms	7
RS-232 Output Current @ 0.4 V	I_{SC}			± 25	mA	
Propagation Delay	t_{PD}		3		µS	8
Transmitter Output Instantaneous Slew Rate	t_{SR}			30	V/µS	9
Transmitter Output Transition Slew Rate	t_{TSR}		3		V/µS	10

10

NOTES

1. All voltages are referenced to ground.
2. Applies to Receiver Inputs only.
3. T1, T2, and T3 loaded with 3K ohms to ground.
4. All outputs are unloaded.
5. T1, T2, and T3 Inputs = 0 volts.
6. V_{CC} = + 5 volts.
7. V_{OUT} = ± 2 volts.
8. RS-232 to TTL or TTL to RS-232.
9. C_L = 10 pF, R_L = 3K, t_A = 0°C. This parameter is sample tested only.
10. R_L = 3K, C_L = 2500 pF measured from +3 volts to -3 volts or -3 volts to +3 volts.
11. This parameter is sample tested only.
12. Negative output level of -5V is increased to -4.0 for the DS1229 only. Positive output level remains at +5V. Use of a +10%, -5% power supply will restore the negative level to -5V.

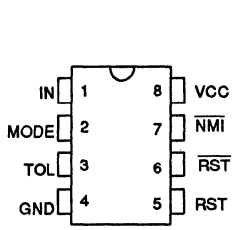
DALLAS SEMICONDUCTOR

DS1231/S
Power Monitor Chip

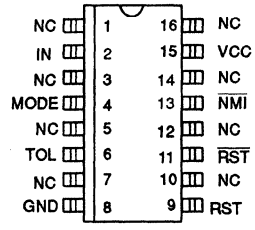
FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying nonvolatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1231 8-Pin DIP
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



DS1231S 16-Pin SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

IN	- Input
MODE	- Selects input pin characteristics
TOL	- Selects 5% or 10% V_{CC} detect
GND	- Ground
RST	- Reset (Active High)
$\overline{RST}$	- Reset (Active Low, open drain)
$\overline{NMI}$	- Nonmaskable interrupt
V_{CC}	- +5 V Supply
NC	- No Connections

10

DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature-compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (V_{TP}) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V_{CC}, detection occurs at V_{TP}-. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V_{TP}+. In this mode Pin 1 sources 30 µA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power-up, $\overline{NMI}$ is released as soon as the input threshold voltage (V_{TP}) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

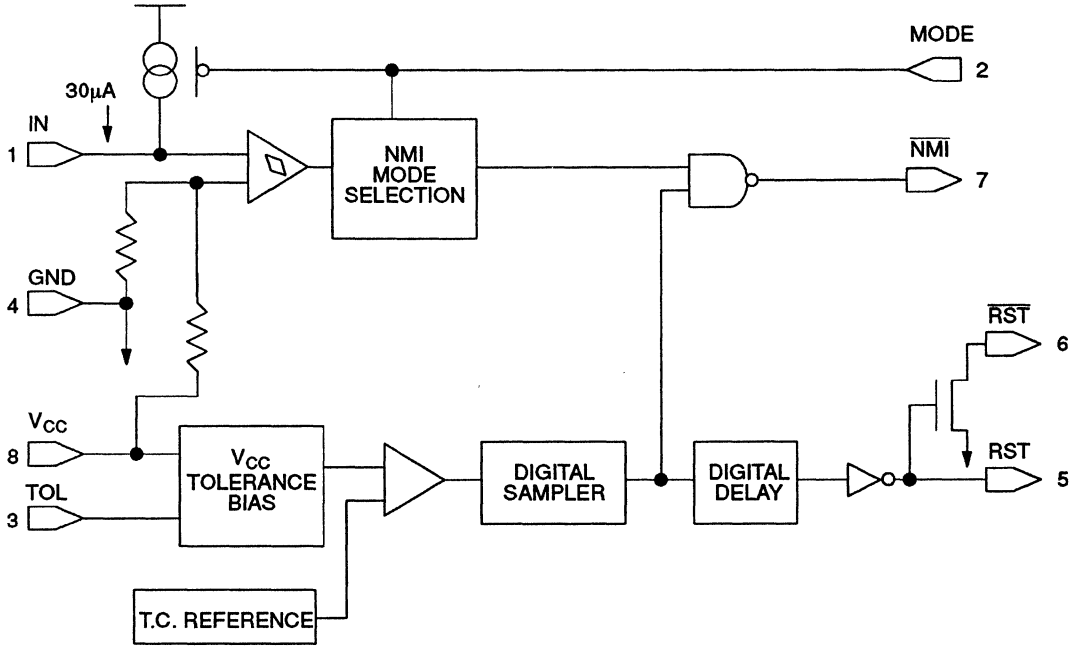
APPLICATION – MODE PIN CONNECTED TO V_{CC}

When the Mode pin is connected to V_{CC}, pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

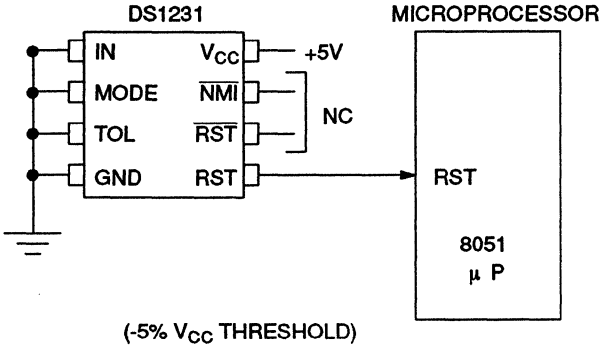
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V_{TP}- is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0=.46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high enough impedance to keep power consumption low, and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

POWER MONITOR BLOCK DIAGRAM Figure 1



POWER-UP RESET Figure 2



(-5% V_{CC} THRESHOLD)

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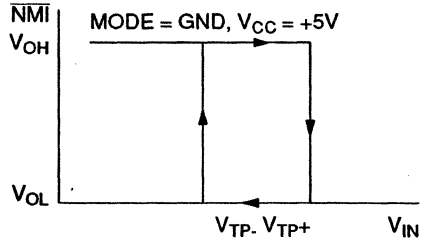
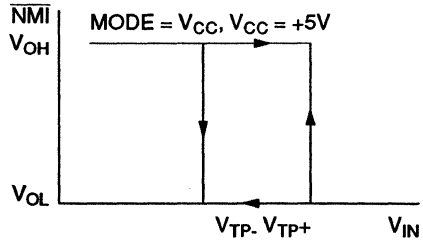
INPUT PIN HYSTERESIS Figure 3

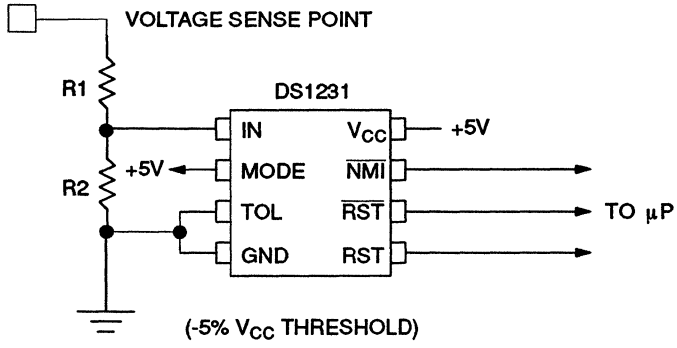




	-20	-35	-50
V_{TP-}	2.3	2.15	2.0
V_{TP+}	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS ±60 mV

APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V\ SENSE = \frac{R1 + R2}{R2} \times 2.3 \qquad V\ MAX = \frac{V\ SENSE}{VTP -} \times 5.0$$

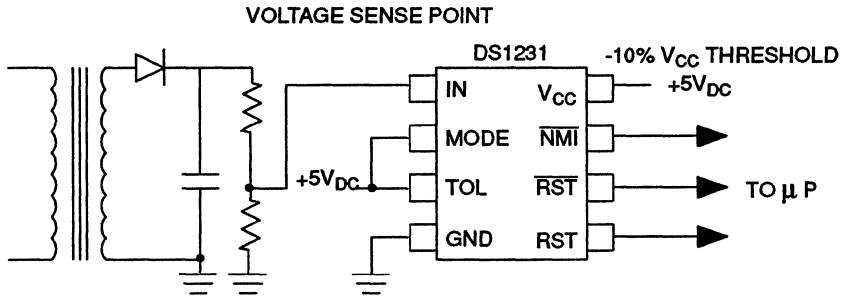
EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

$$\text{THEN } 8 = \frac{R1 + 10K}{10K} \times 2.3 \qquad R1 = 25K$$

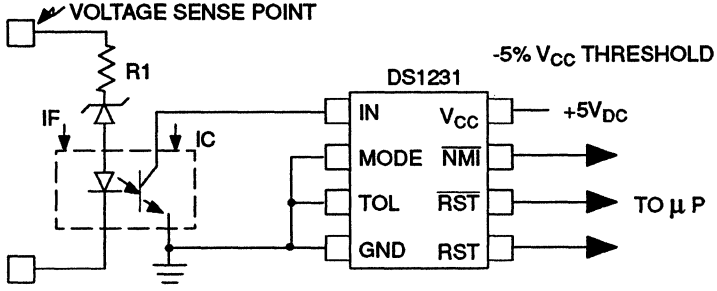
APPLICATION – MODE PIN CONNECTED TO GROUND

When the Mode pin is connected to ground, pin 1 is a current source of 30 µA with a V_{TP}+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 µA of collector current required by pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



APPLICATION WITH MODE PIN GROUNDED Figure 6



$$\text{VOLTAGE SENSE POINT (TRIP VALUE)} = VZ + \frac{IC}{CTR} \times R1$$

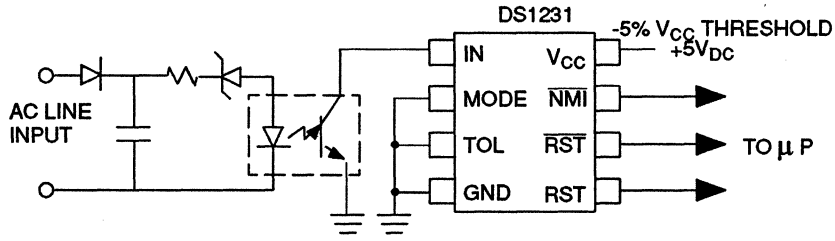
$$CTR = \frac{IC}{IF}$$

CTR = CURRENT TRANSFER RATIO
VZ = ZENNER VOLTAGE

EXAMPLE: CTR = 0.2 IC = 30 µA IF = 150 µA
VOLTAGE SENSE POINT = 105 AND
VZ = 100 VOLTS

$$\text{THEN } 105 = 100 + \frac{30}{0.2} \times R1 \qquad R1 = 33K$$

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-10		+10	μA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	5
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode=GND)	I_C	15	25	50	μA	
Input Pin 1 (Mode=V_{CC})	I_C			0.1	μA	
IN Trip Piont (Mode=GND)	V_{TP}	See Figure 3				1
IN Trip Point (Mode=V_{CC})	V_{TP}					1
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

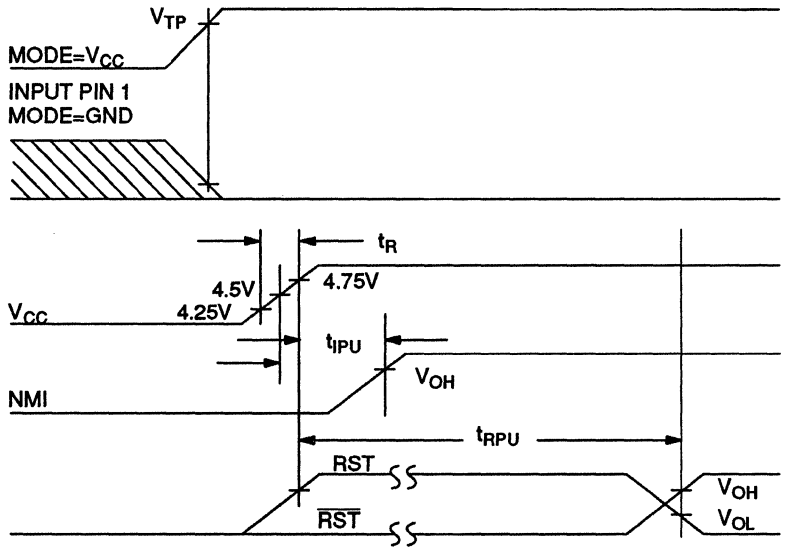
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	µs	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	µs	4
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	150	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

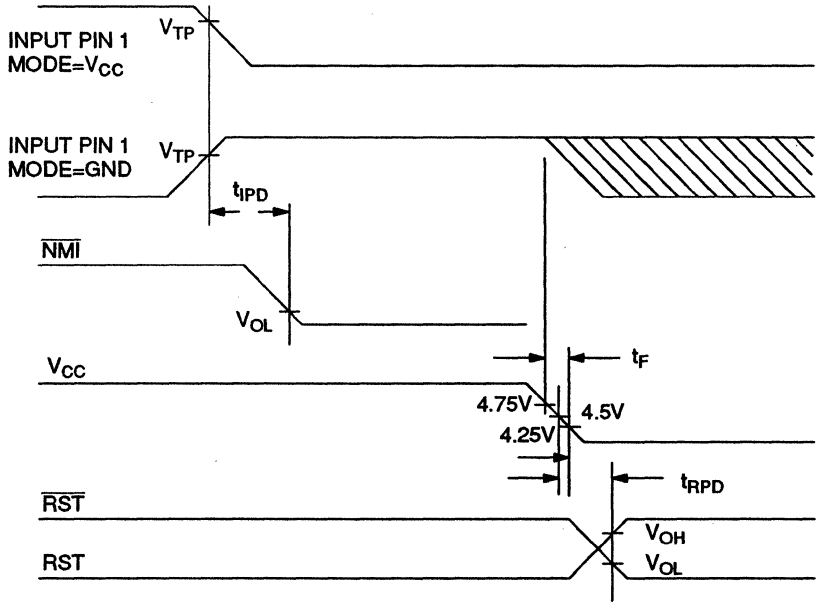
NOTES:

1. All voltages referenced to ground.
2. V_{CC} = +5.0 volts with outputs open.
3. Measured with outputs open.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.

TIMING DIAGRAM-POWER-UP



TIMING DIAGRAM-POWER-DOWN



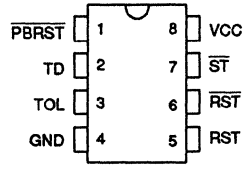
DALLAS SEMICONDUCTOR

DS1232
MicroMonitor Chip

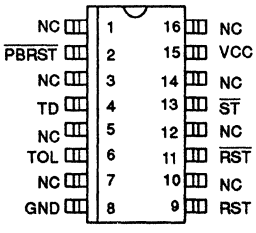
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

PIN ASSIGNMENT



DS1232 8-Pin DIP
(300 Mil)
See Mech. Drawing
Sect. 16, Pg. 1



DS1232S 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

$\overline{PBRST}$	- Pushbutton Reset Input
TD	- Time Delay Set
TOL	- Selects 5% or 10% V_{CC} Detect
GND	- Ground
RST	- Reset Output (Active High)
$\overline{RST}$	- Reset Output (Active Low, Open Drain)
$\overline{ST}$	- Strobe Input
V_{CC}	- +5 Volt Power
NC	- No Connections

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DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION – POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

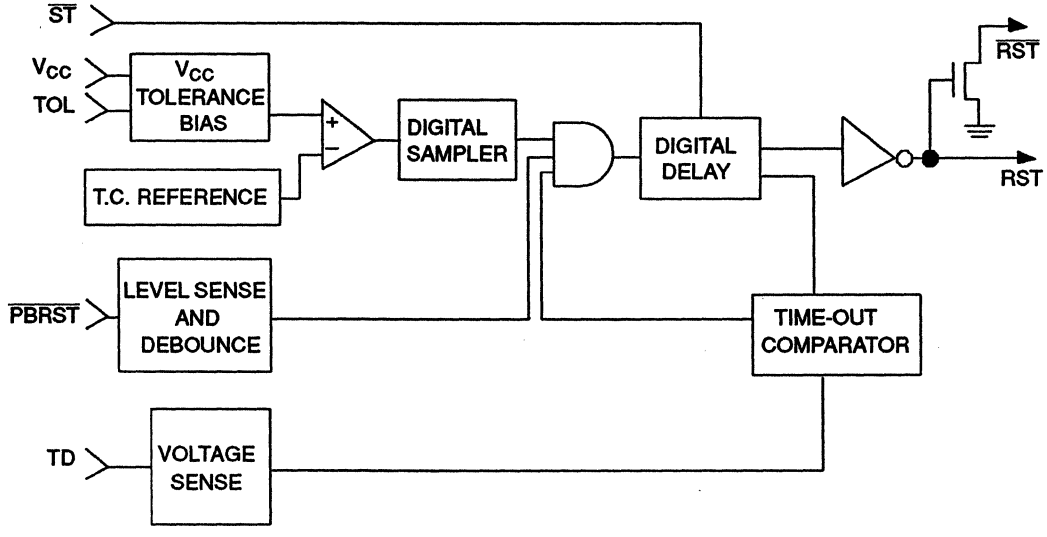
OPERATION – PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

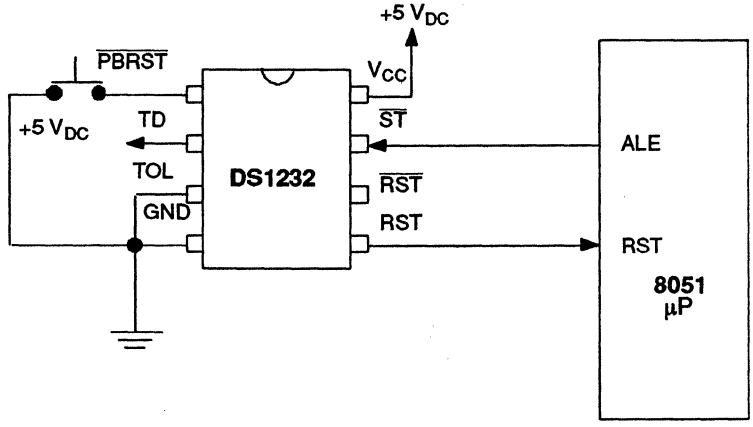
OPERATION – WATCHDOG TIMER

A watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

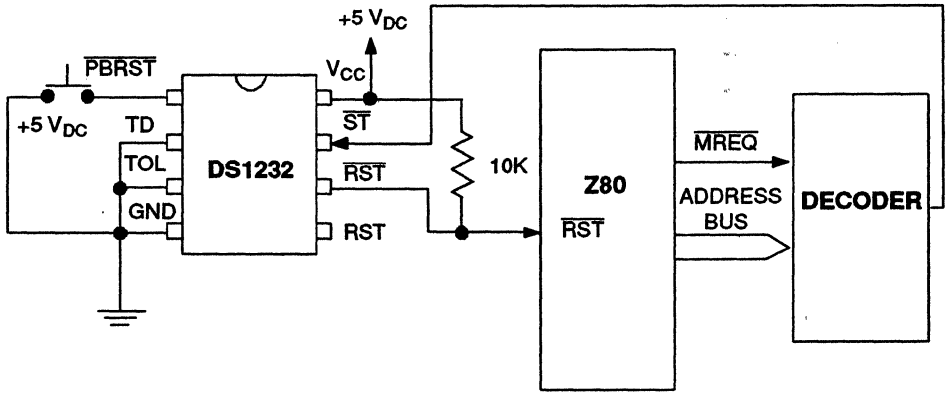
MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



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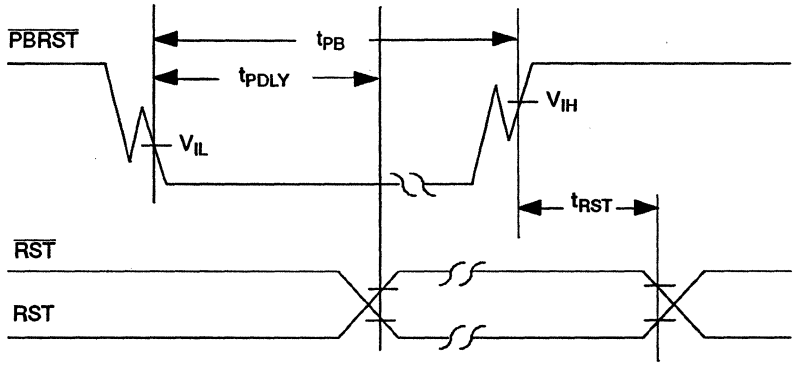
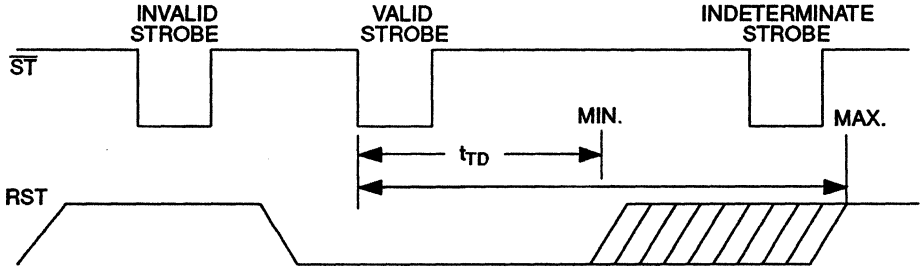
TIMING DIAGRAM - PUSHBUTTON RESET Figure 4



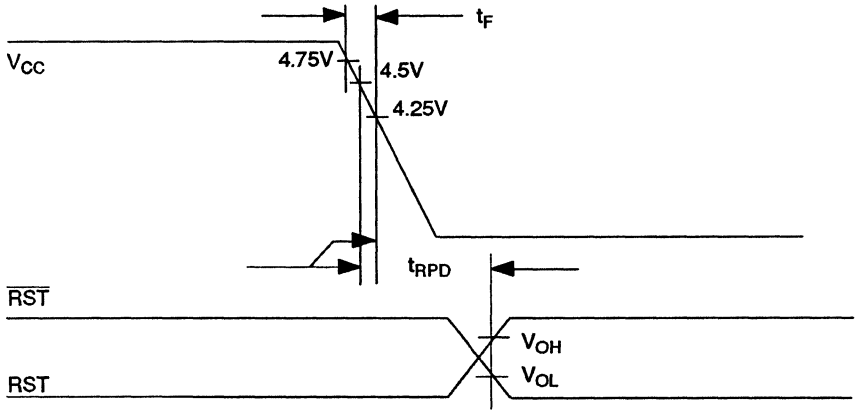
TIMING DIAGRAM - STROBE INPUT Figure 5



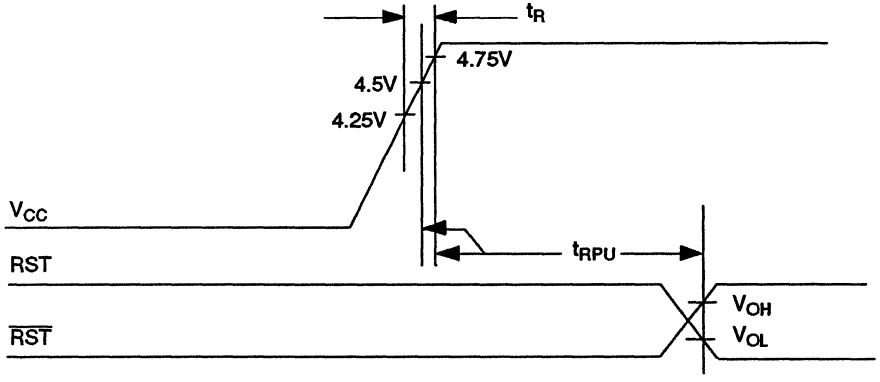
WATCHDOG TIMEOUTS Table 1

TD PIN	TIME-OUT		
	MIN	TYP	MAX
GND	62.5ms	150ms	250ms
Float	250ms	600ms	1000ms
V_{CC}	500ms	1200ms	2000ms

TIMING DIAGRAM - POWER DOWN Figure 6



TIMING DIAGRAM - POWER UP Figure 7



10

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Output Voltage @ -500 µA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS			NOTES
Input Capacitance	C_{IN}	5	pF			
Output Capacitance	C_{OUT}	7	pF			

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Transition	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0	5		µs	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5 of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.

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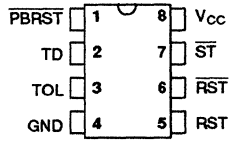
DALLAS SEMICONDUCTOR

DS1232LP/LPS
Low Power MicroMonitor Chip

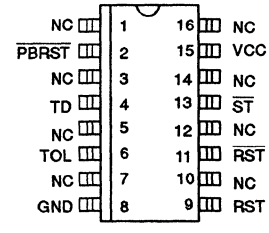
FEATURES

- Super low-power version of DS1232
- 50 µA quiescent current
- Halts and restarts an out-of-control microprocessor
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- 8-pin DIP or 8-pin SOIC package
- Optional 16-pin SOIC package available
- Industrial temperature -40°C to +85°C available

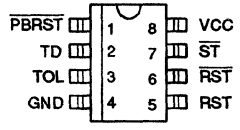
PIN ASSIGNMENT



DS1232LP 8-Pin DIP
(300 Mil)
See Mech. Drawing
Sect. 16, Pg. 1



DS1232LPS 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Sect. 16, Pg 6



DS1232LPS-2 8-Pin SOIC
(150 Mil)
See Mech. Drawing
Sect. 16, Pg 5

PIN DESCRIPTION

$\overline{PBRST}$	- Pushbutton Reset Input
TD	- Time Delay Set
TOL	- Selects 5% or 10% V_{CC} Detect
GND	- Ground
RST	- Reset Output (Active High)
$\overline{RST}$	- Reset Output (Active Low, Open Drain)
$\overline{ST}$	- Strobe Input
V_{CC}	- +5 Volt Power

DESCRIPTION

The DS1232LP/LPS Low Power MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232LP/LPS performs is pushbutton reset control. The DS1232LP/LPS debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232LP/LPS has an internal timer that forces the reset signals to the active state if

the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION – POWER MONITOR

The DS1232LP/LPS detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

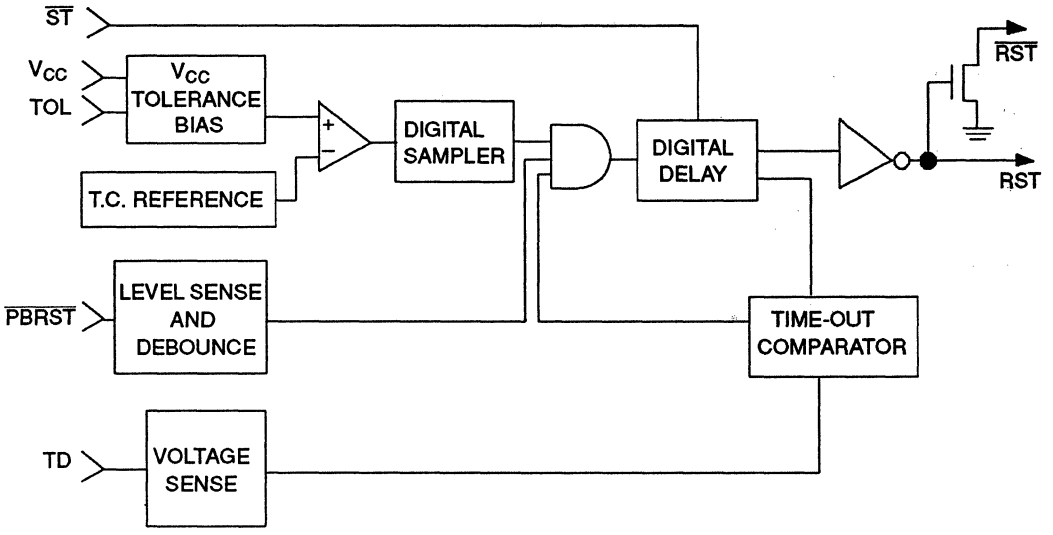
OPERATION – PUSHBUTTON RESET

The DS1232LP/LPS provides an input pin for direct connection to a pushbutton (Figure 1). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

OPERATION – WATCHDOG TIMER

The watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 2.

MICROMONITOR BLOCK DIAGRAM



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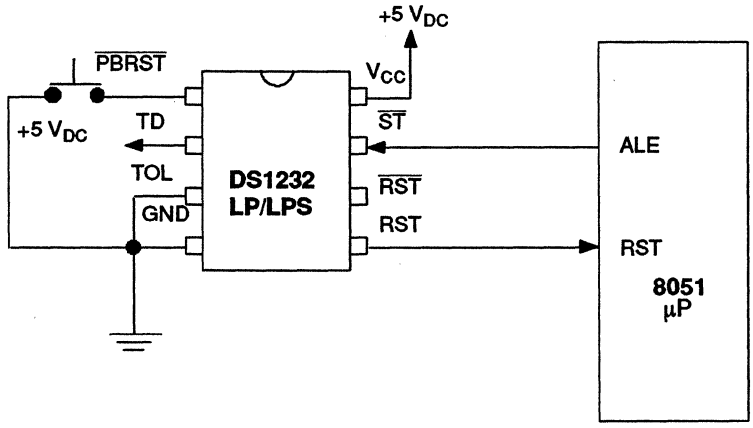
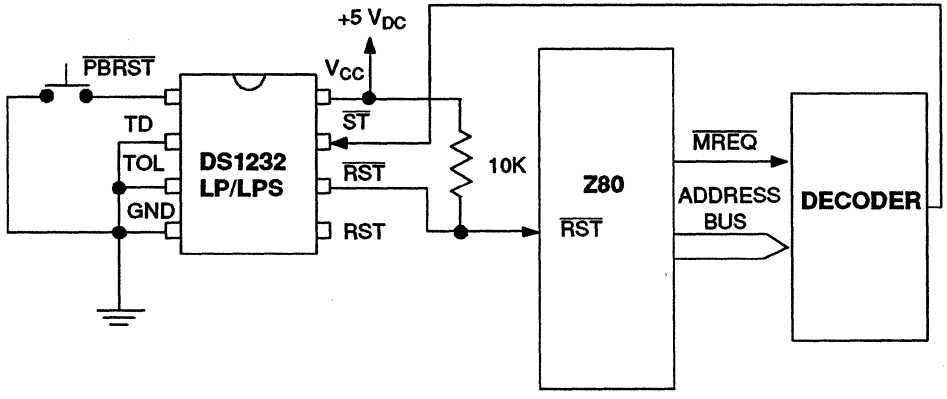
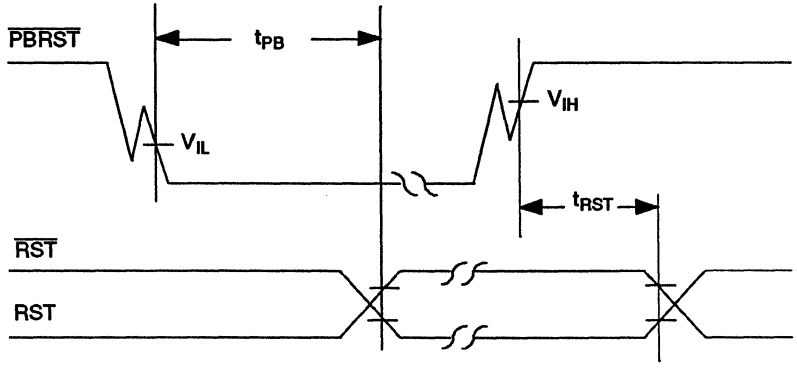
PUSHBUTTON RESET Figure 1



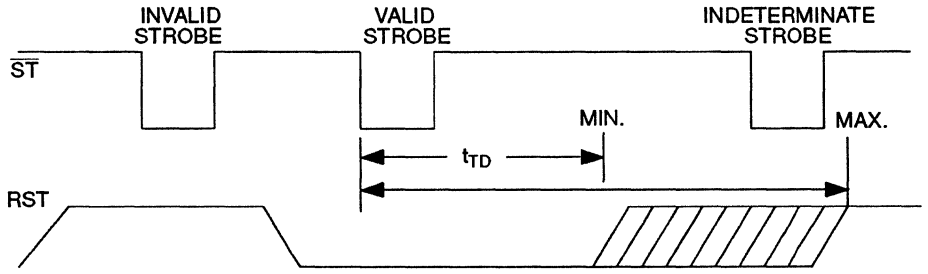
WATCHDOG TIMER Figure 2



TIMING DIAGRAM – PUSHBUTTON RESET Figure 3



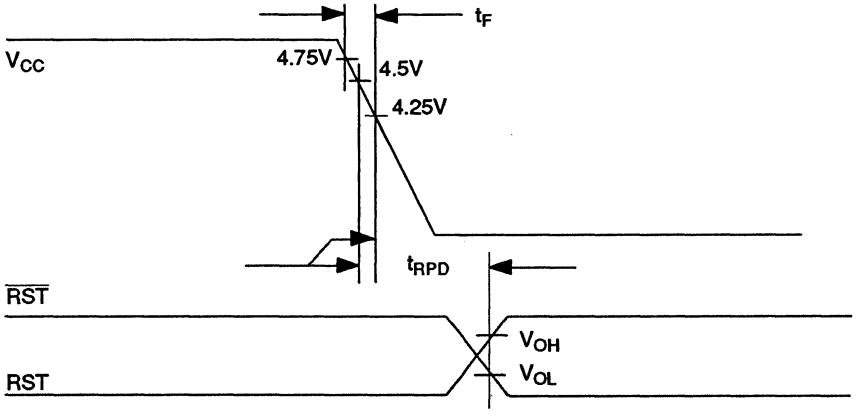
TIMING DIAGRAM – STROBE INPUT Figure 4



WATCHDOG TIME-OUTS Table 1

TD	TIME-OUT		
	MIN	TYP	MAX
GND	62.5ms	150ms	250ms
Float	250ms	600ms	1000ms
V_{CC}	500ms	1200ms	2000ms

TIMING DIAGRAM – POWER DOWN Figure 5



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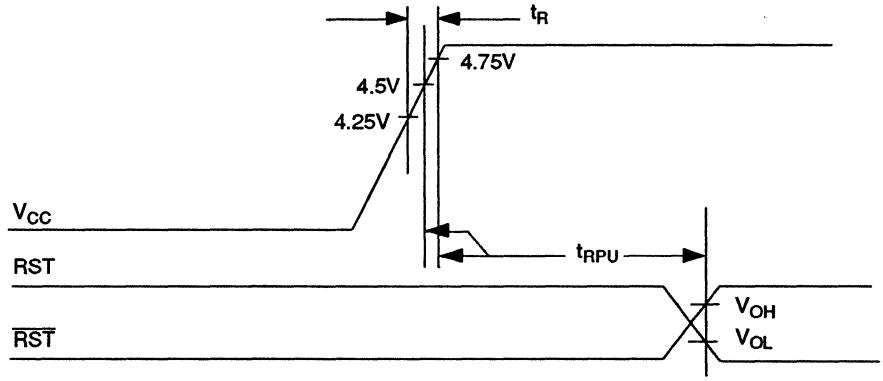
TIMING DIAGRAM – POWER UP Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	10			mA	
Output Voltage @ -500 uA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	7
Operating Current	I_{CC}			50	µA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	40			ns	6
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	150			µs	
V_{CC} Detect to RST and $\overline{RST}$ Inactive	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0			ns	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40K typical.
4. t_R = 5µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5 of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.

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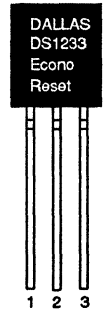
DALLAS SEMICONDUCTOR

DS1233
5V EconoReset

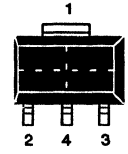
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K ohm pull-up resistor

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawing
Sect. 16, Pg. 18



SOT-223 Package
See Mech. Drawing
Sect. 16, Pg. 19

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}

DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION - POWER MONITOR

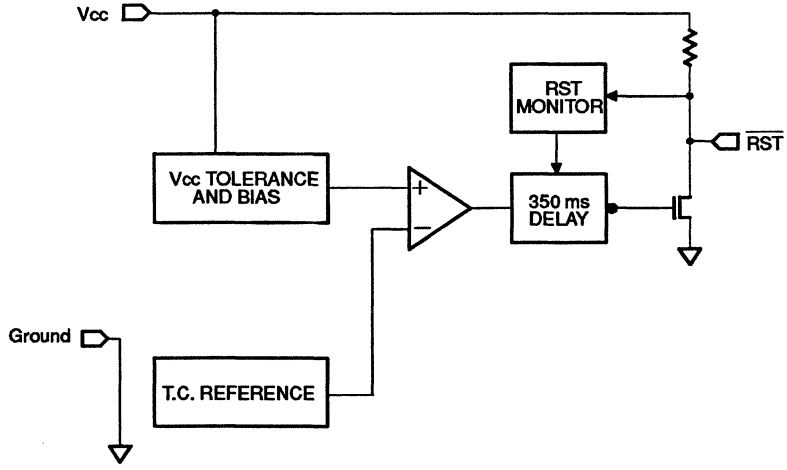
The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

OPERATION - PUSHBUTTON RESET

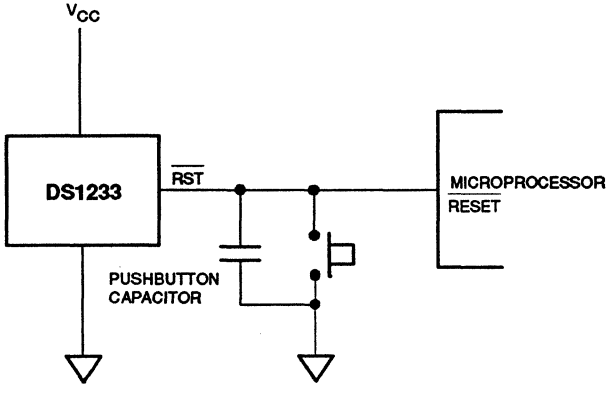
The DS1233 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

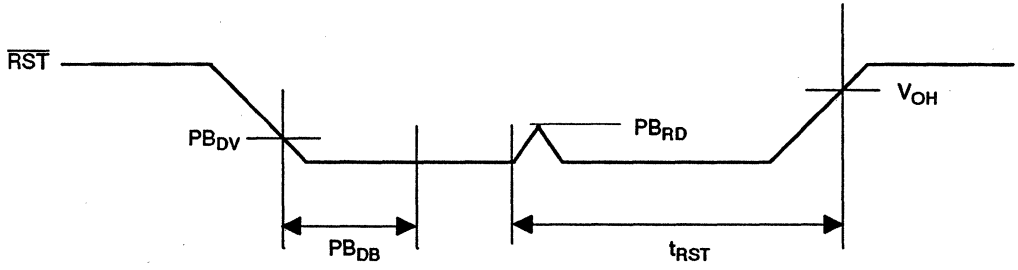
BLOCK DIAGRAM Figure 1



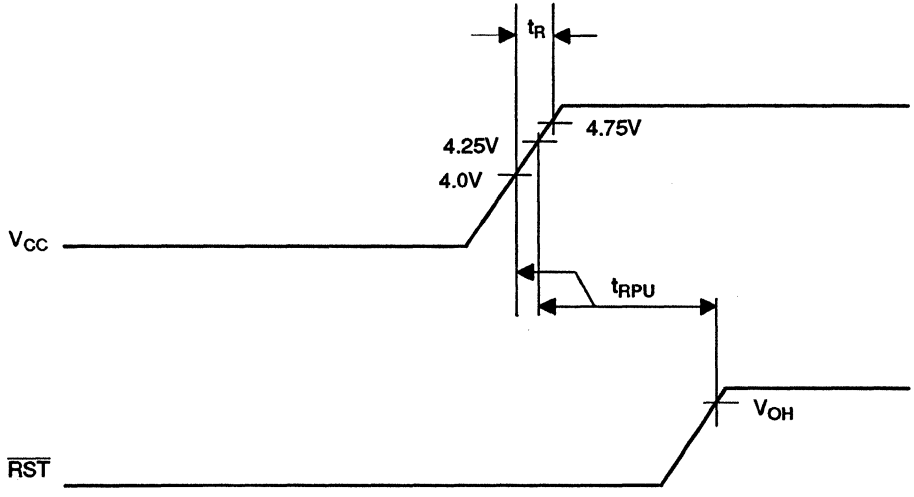
APPLICATION EXAMPLE Figure 2



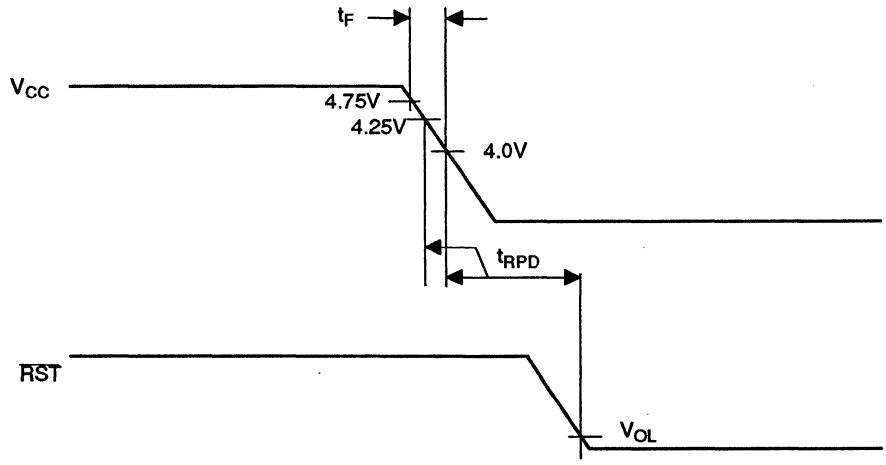
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	Volts	1

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DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	Volts	
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current				50	µA	
V_{CC} Trip Point 10%	V_{CCTP1}	4.25	4.375	4.49	Volts	1
V_{CC} Trip Point 15%	V_{CCTP2}	4.0	4.125	4.24	Volts	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect 10%	PB_{DV}	1.8		3.3	Volts	1
Pushbutton Detect 15%	PB_{DV}	1.8		3.3	Volts	1
Pushbutton Release	PB_{RD}		0.3	0.8	Volts	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KOhm	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

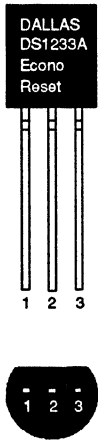
DALLAS SEMICONDUCTOR

DS1233A
3.3V EconoReset

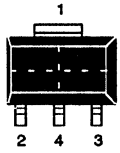
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 3.3V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K ohm pull-up resistor

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawing
Sect. 16, Pg. 18



SOT-223 Package
See Mech. Drawing
Sect. 16, Pg. 19

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PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}

DESCRIPTION

The DS1233A EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233A is pushbutton reset control. The DS1233A debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION – POWER MONITOR

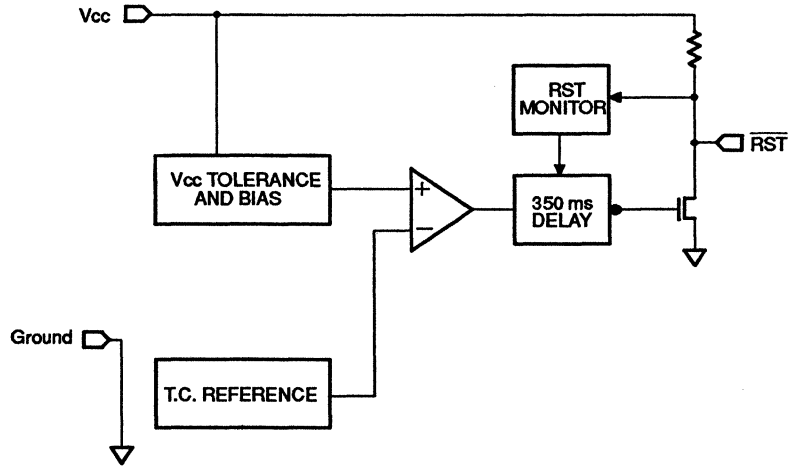
The DS1233A provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

OPERATION – PUSHBUTTON RESET

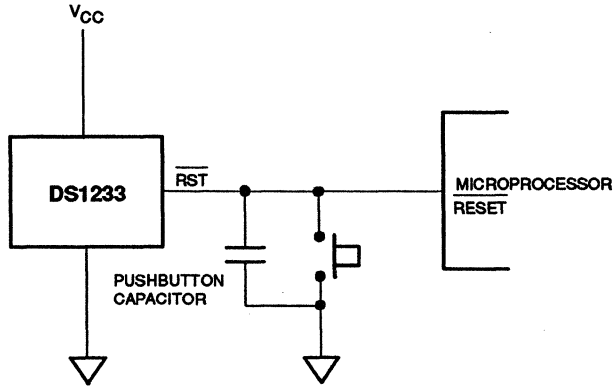
The DS1233A provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233A is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233A will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233A will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233A will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233A will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

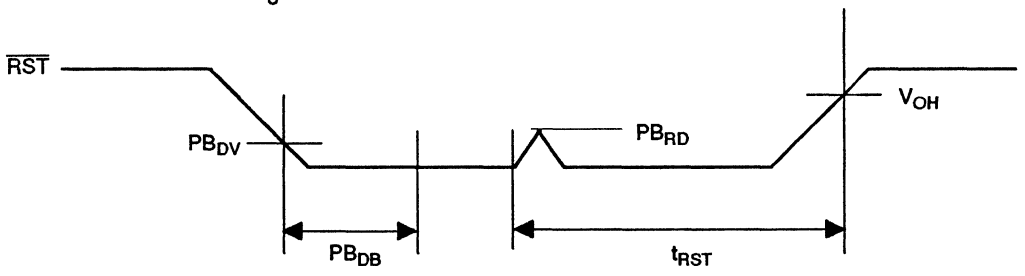
BLOCK DIAGRAM Figure 1



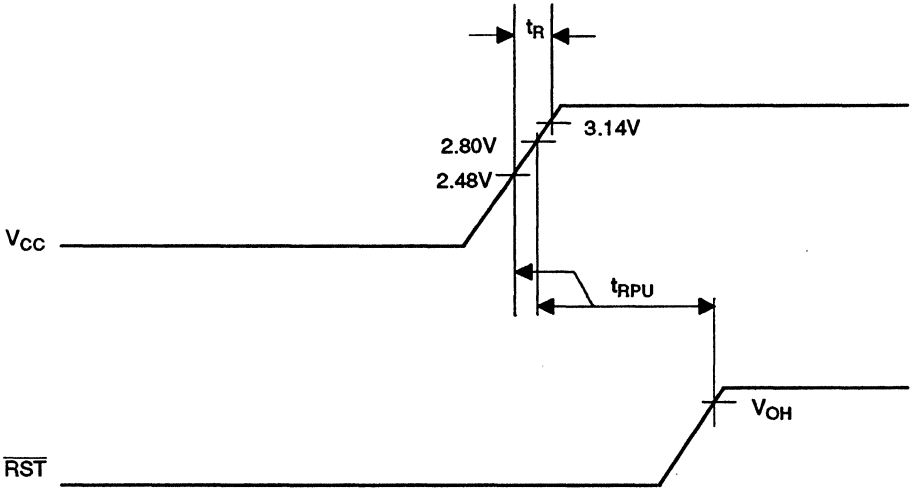
APPLICATION EXAMPLE Figure 2



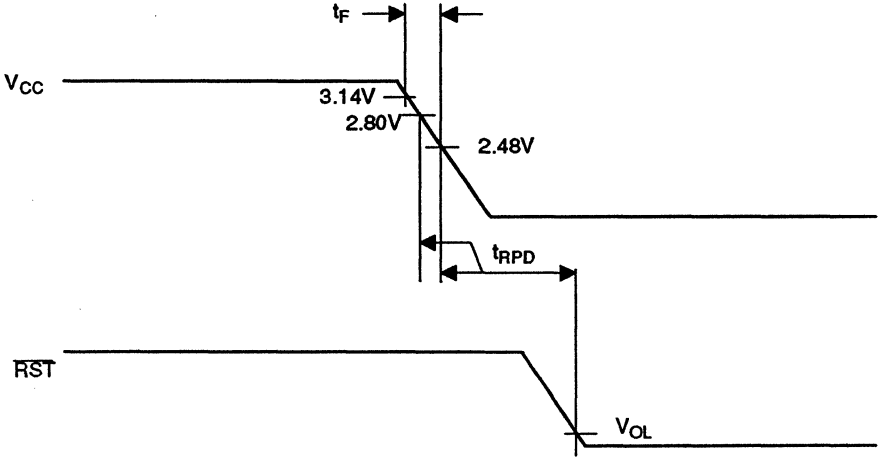
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* These are stress ratings only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	3.3	5.0	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	Volts	
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current				50	µA	
V_{CC} Trip Point 10%	V_{CCTP1}	2.80	2.88	2.97	Volts	1
V_{CC} Trip Point 15%	V_{CCTP2}	2.64	2.72	2.80	Volts	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect 10%	PB_{DV}	1.8		3.0	Volts	1
Pushbutton Detect 15%	PB_{DV}	1.8		3.0	Volts	1
Pushbutton Release	PB_{RD}		0.3	0.8	Volts	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KOhm	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (2.85V – 2.3V)	t_F	300			µs	
V_{CC} Slew Rate (2.3V – 2.85V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

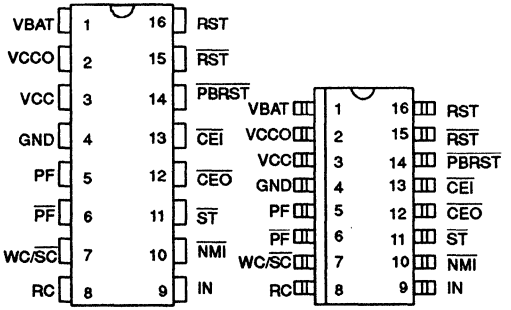
DALLAS SEMICONDUCTOR

DS1236
MicroManager Chip

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawing
Sect. 16, Pg. 1

16-Pin SOIC (300 Mil.)
See Mech. Drawing
Sect. 16, Pg 6

PIN DESCRIPTION

V_{BAT}	+3 Volt Battery Input
V_{CCO}	Switched SRAM Supply Output
V_{CC}	+5 Volt Power Supply Input
GND	Ground
PF	Power Fail (Active High)
$\overline{PF}$	Power Fail (Active Low)
WC/$\overline{SC}$	Wake-Up Control (Sleep)
RC	Reset Control
IN	Early Warning Input
$\overline{NMI}$	Non-Maskable Interrupt
$\overline{ST}$	Strobe Input
$\overline{CEO}$	Chip Enable Output
$\overline{CEI}$	Chip Enable Input
$\overline{PBRST}$	pushbutton Reset Input
$\overline{RST}$	Reset Output (Active Low)
RST	Reset Output (Active High)

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DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery-backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. Th e V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236 for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The $\overline{PBRST}$ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$-generated RST is illustrated in Figure 5.

NON-MASKABLE INTERRUPT

The DS1236 generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236 pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any detected IN pin levels be low V_{TP} by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above

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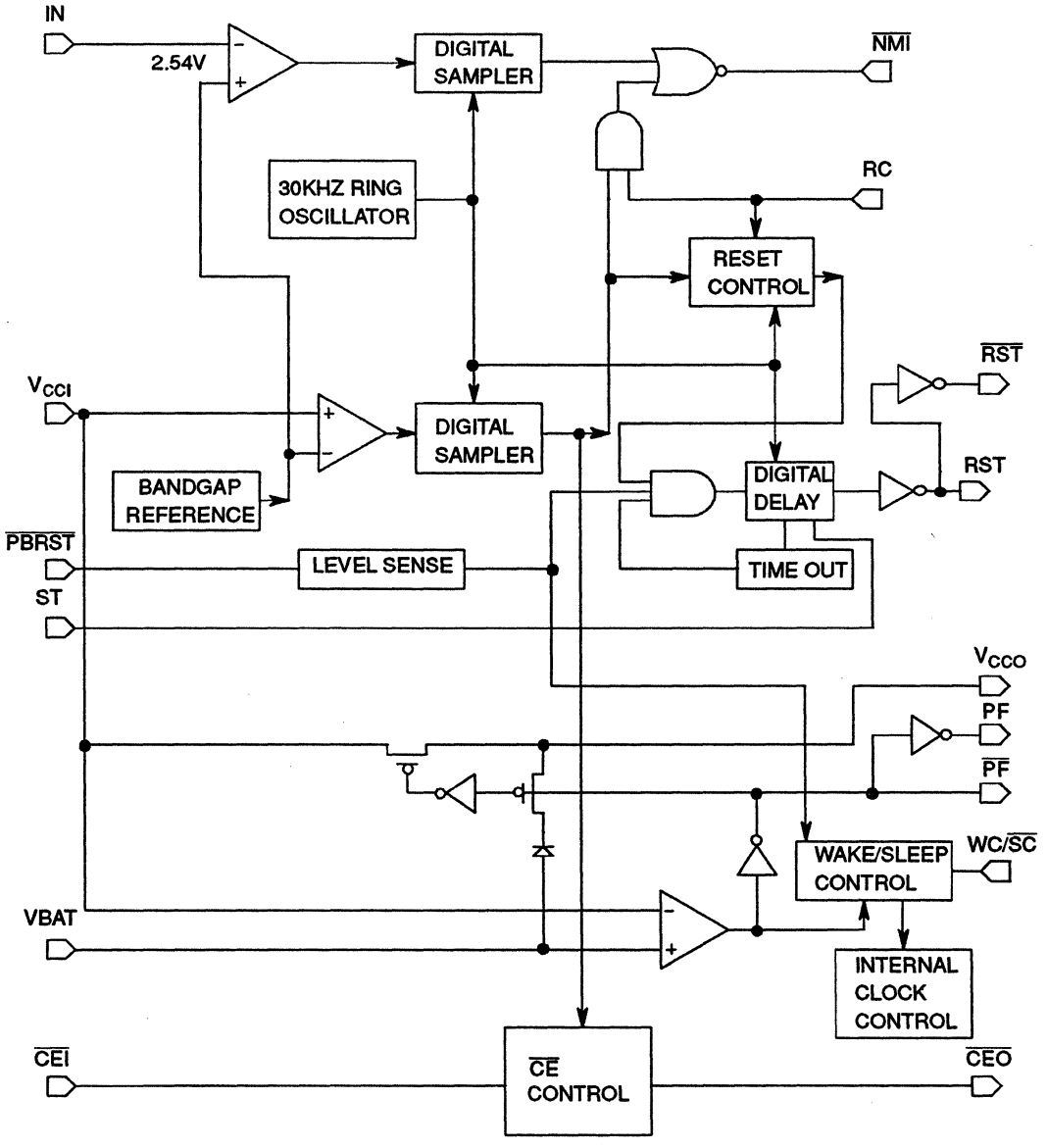
V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power-up. This is of no consequence, however, since a $\overline{RST}$ will be active.

DS1236 FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3 volt clock to TP1.

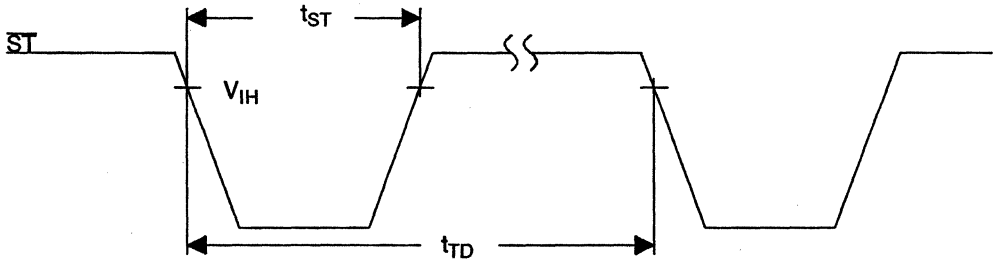
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power- up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

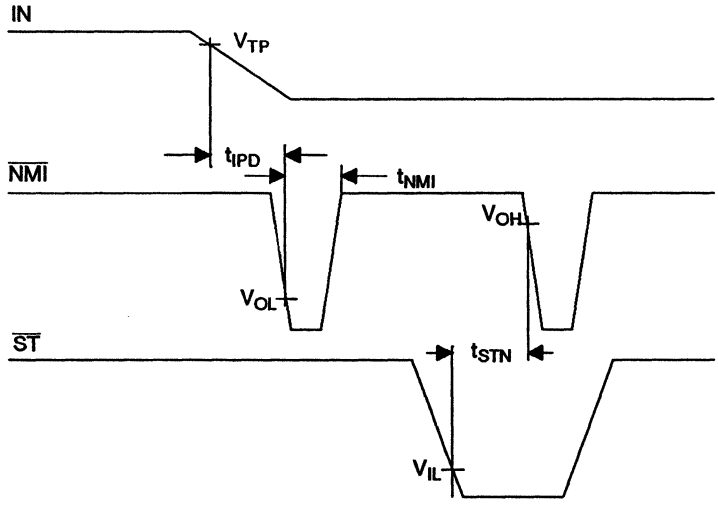
RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

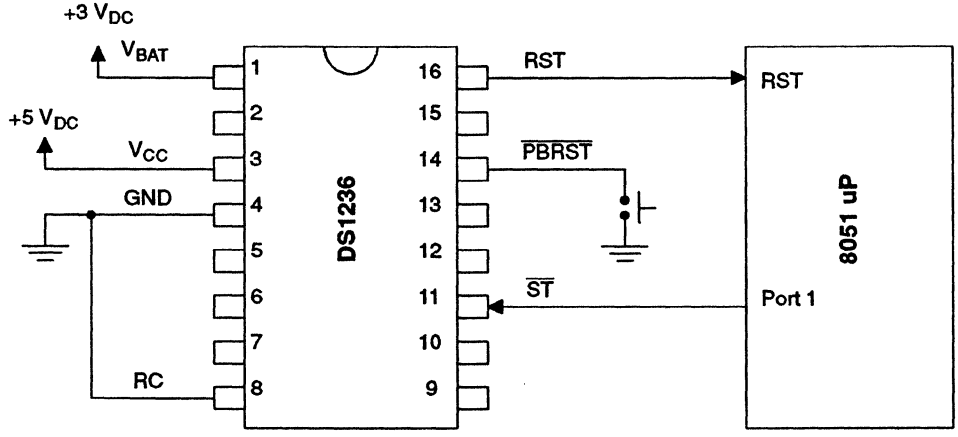
ST/INPUT TIMING Figure 2



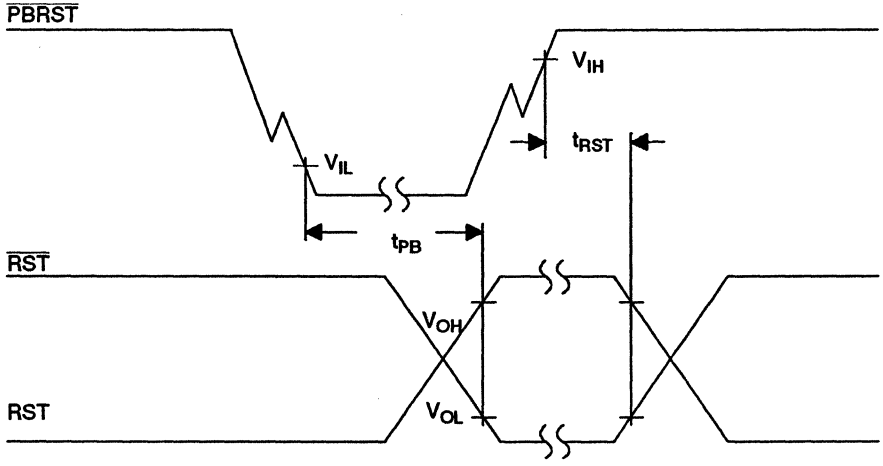
NMI/FROM ST/INPUT Figure 3



POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



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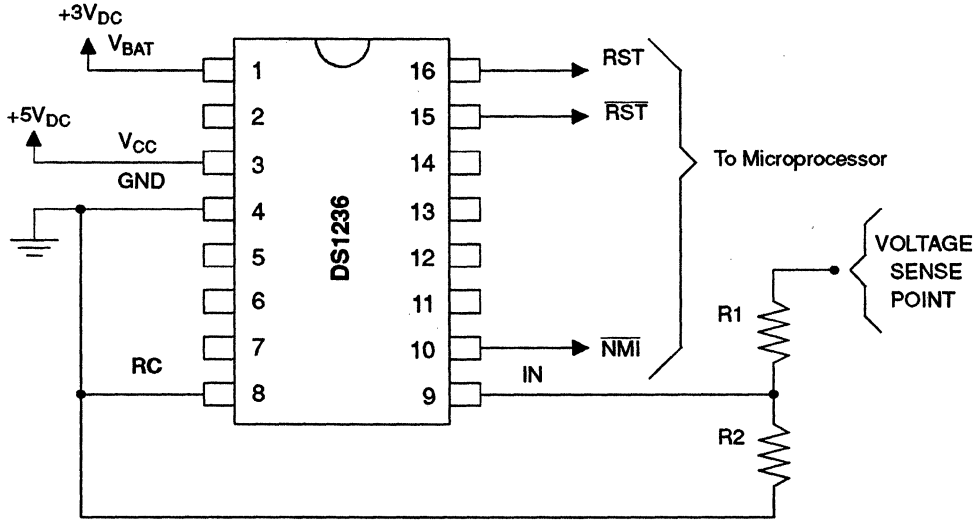
NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 4.80 VOLTS

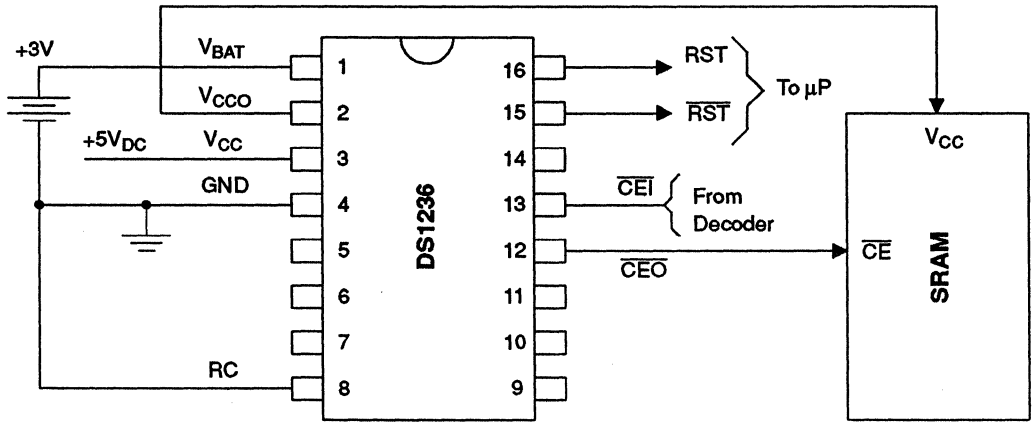
$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K \text{ OHM}$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K \text{ OHM}$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7 \text{ VOLTS}$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and $\overline{RST}$ signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low- power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 10, Figure 11, Figure 12, and Figure 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for

power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and $\overline{PF}$ pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

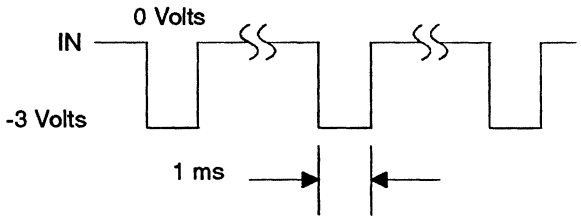
Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

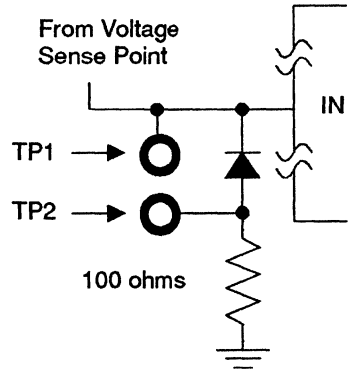
The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236 can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 15.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236.

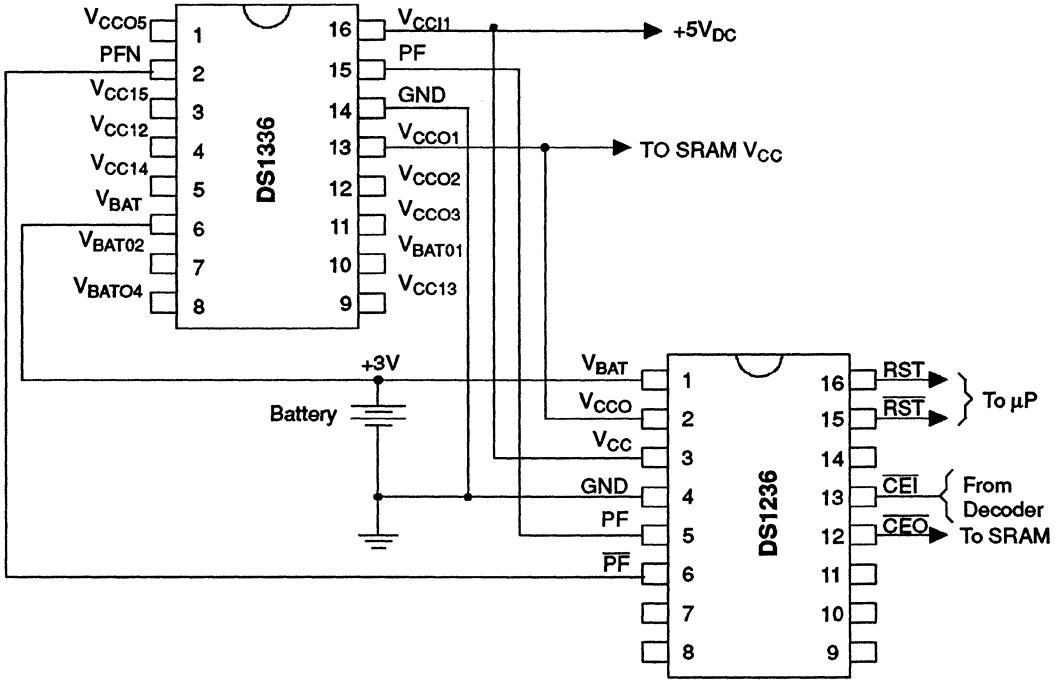
FRESHNESS SEAL Figure 8



Note: This series of pulses must be applied during normal +5 volt operation.



POWER SWITCHING Figure 9



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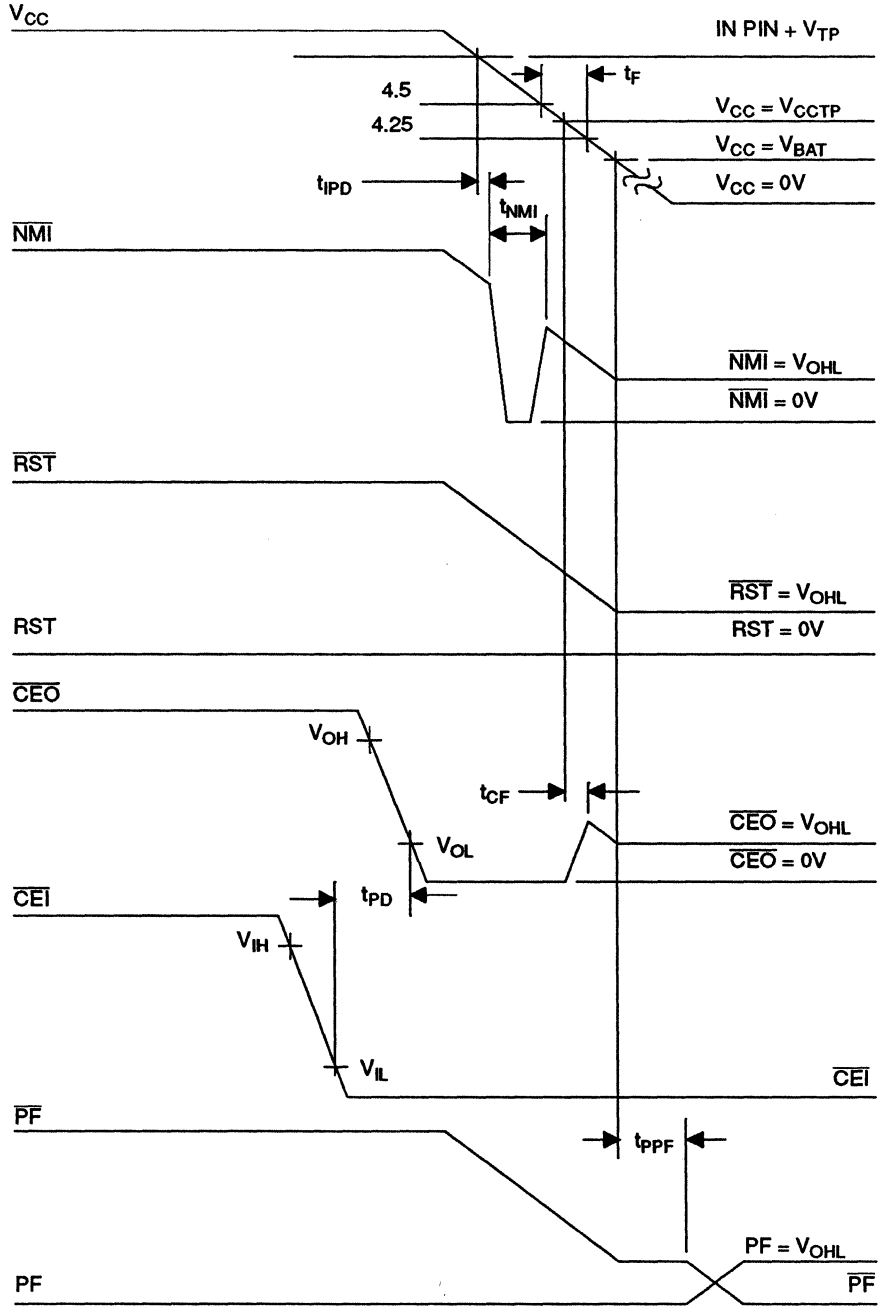
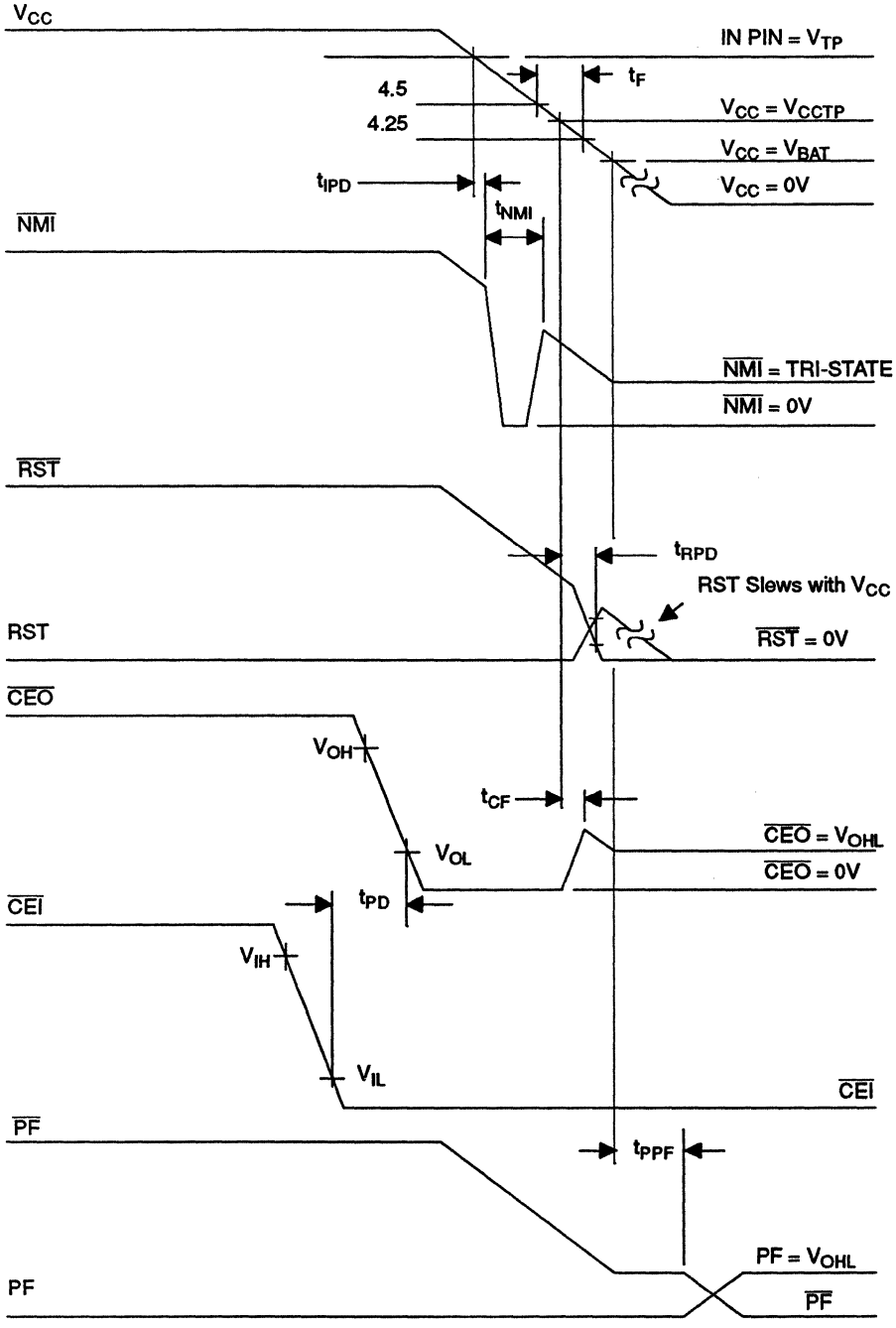
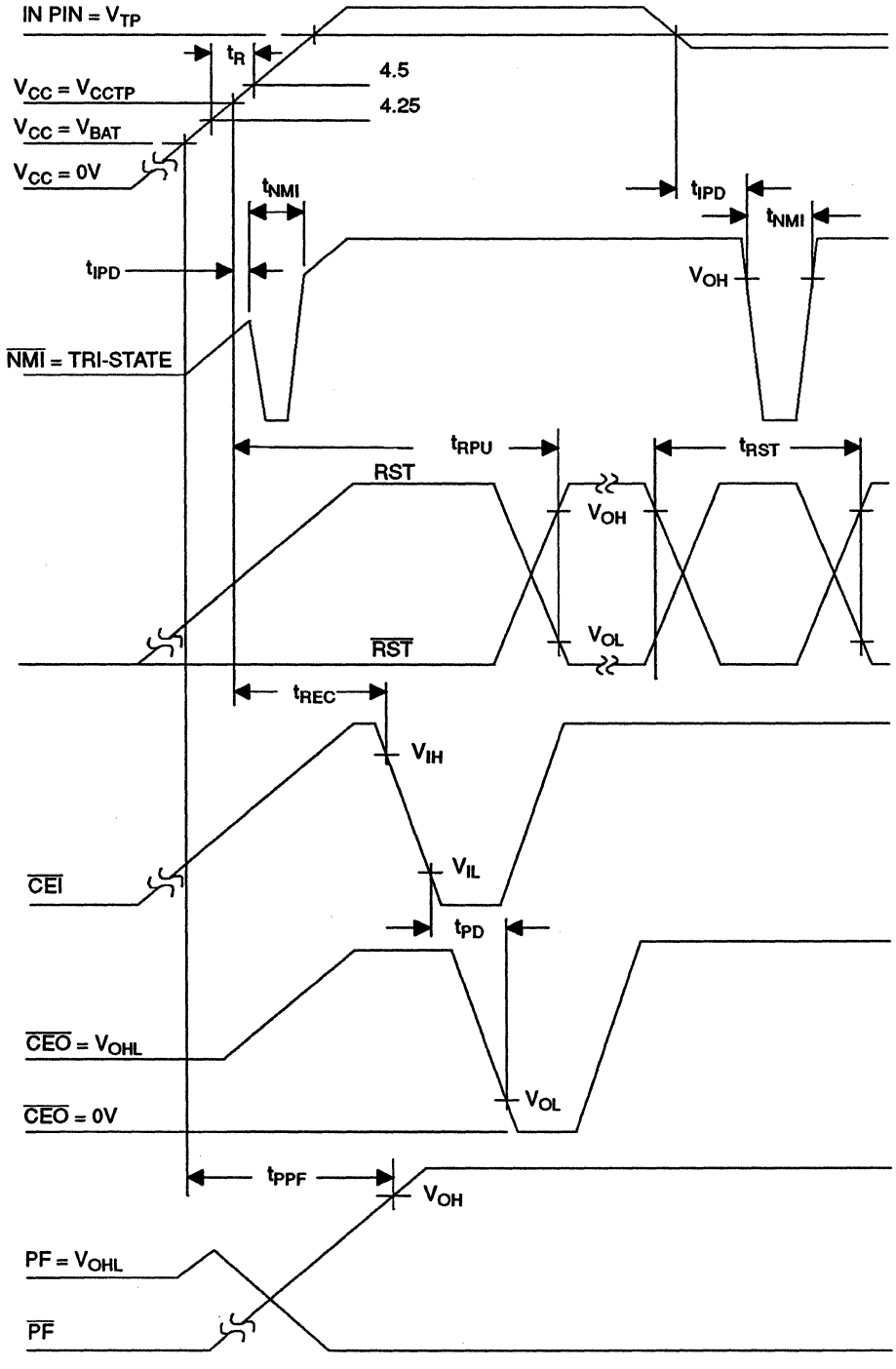
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 10



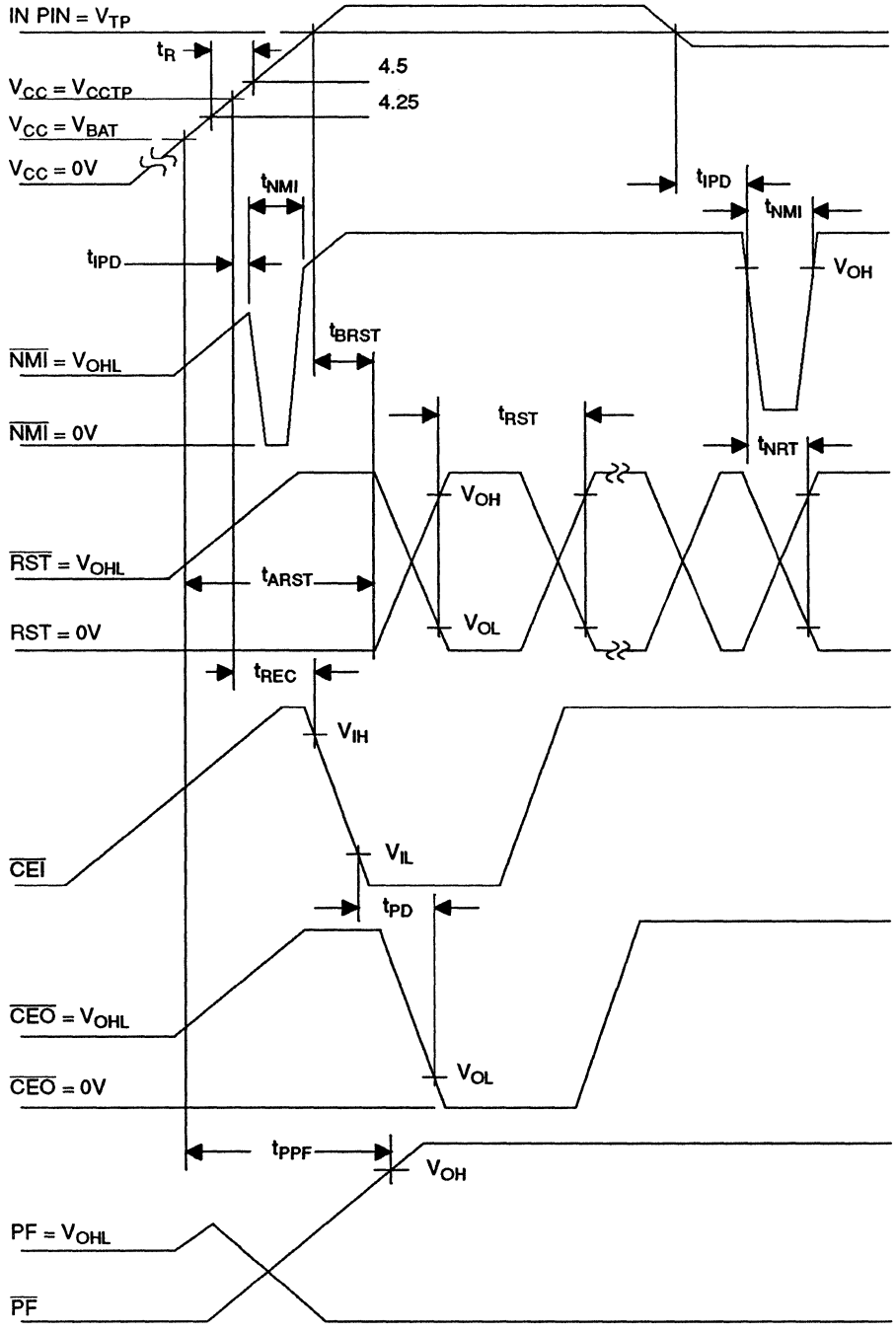
NMOS MODE POWER-DOWN (RC = GND) Figure 11



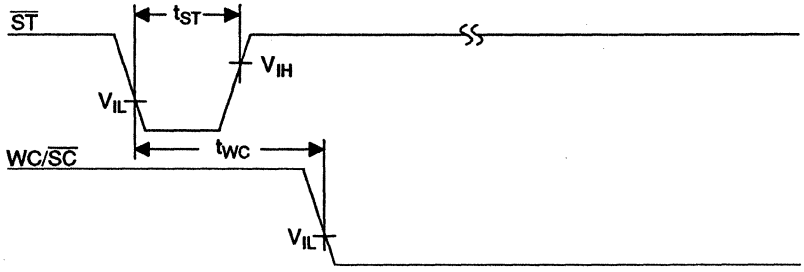
NMOS MODE POWER-UP (RC = GND) Figure 12



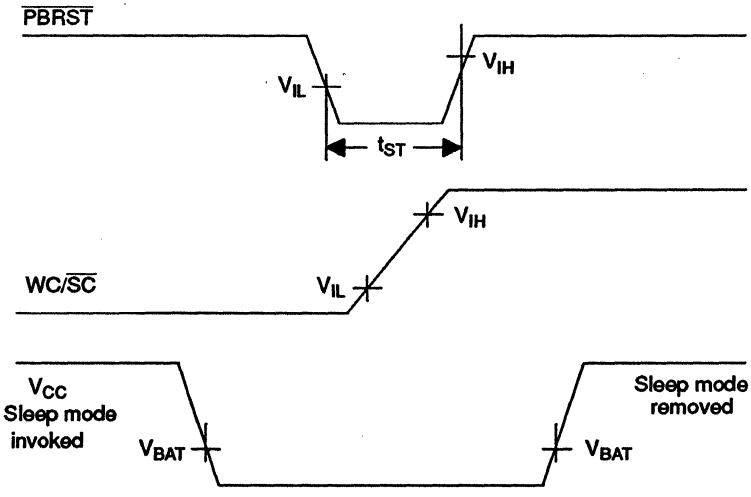
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 13



WAKE/SLEEP CONTROL Figure 14



OPTIONS FOR INVOKING WAKEUP Figure 15



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature on the Leads	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC} -0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT} -0.7		V	1,6
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.7		V	1,6
$\overline{PBRST}$ Pull Up Resist	R_{PBRST}	10K			Ohms	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage	I_{LO}	-1.0		+1.0	µA	18
Output Current @0.4V	I_{OL}			4.0	mA	12
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µS	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µS	
RESET Active Time	t_{RST}	25	100	150	mS	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µS	14
$\overline{ST}$ Pulse Width	t_{ST}	20			nS	
$\overline{PBRST}$ @ V_{IL}	t_{PB}	30			mS	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µS	
Chip Enable Propagation Delay	t_{PD}			20	nS	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µS	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	nS	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	mS	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µS	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µS	8
Chip Enable Output Recovery Time	t_{REC}	.1			µS	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µS	
Chip Enable Pulse Width	t_{CE}			5	S	10
Watchdog Time Delay	t_{TD}	100	400	600	mS	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µS	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µS	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	nS	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	nS	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µS	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µS	16

CAPACITANCE

($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With $t_R = 5$ µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}/\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA maximum.
13. All outputs except $\overline{RST}$ which is 25 µA minimum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 uamps in normal operation and ±1 µamp in the sleep mode.

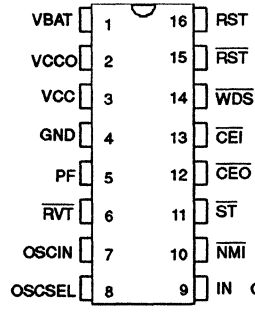
DALLAS SEMICONDUCTOR

DS1238 MicroManager

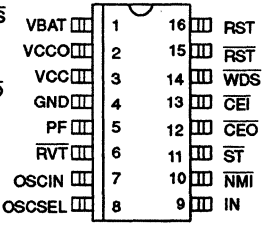
FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238-5
- Provides orderly shutdown in microprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawing
Sect. 16, Pg 1



16-Pin SOIC (300 Mil.)
See Mech. Drawing
Sect. 16, Pg 6

PIN DESCRIPTION

V_{BAT}	+3 Volt Battery input
V_{CCO}	Switched SRAM Supply Output
V_{CC}	+5 Volt power supply input
GND	Ground
PF	Power Fail
$\overline{RVT}$	Reset Voltage Threshold
OSCIN	Oscillator In
OSCSEL	Oscillator Select
IN	Early Warning input
$\overline{NMI}$	Non Maskable Interrupt
$\overline{ST}$	Strobe input
$\overline{CEO}$	Chip Enable output
$\overline{CEI}$	Chip Enable input
$\overline{WDS}$	Watchdog status
$\overline{RST}$	Reset output (active low)
RST	Reset output (active high)

DESCRIPTION

The DS1238 MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset debounce circuit connected to the $\overline{RST}$ pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via $\overline{WDS}$ and $\overline{RVT}$, respectively. A block diagram of the DS1238 is shown in Figure 1.

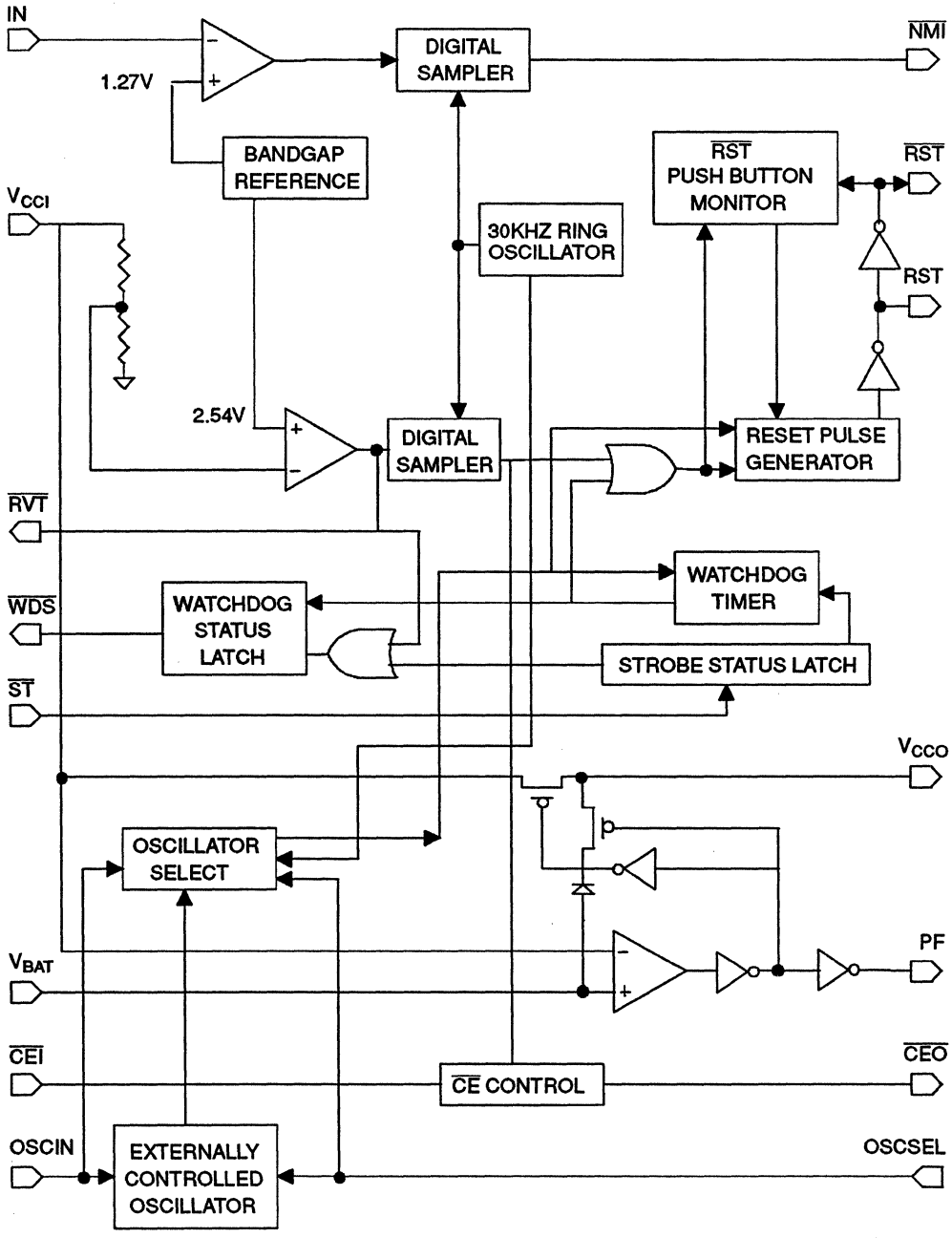
PIN DESCRIPTION

Pin Name	Description
V_{BAT}	+3V Battery Input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{RVT}$	Reset Voltage Threshold. Indicates that V_{CC} is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high to low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{WDS}$	Watchdog Status. Indicates that a watchdog timeout has occurred.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

POWER MONITOR

The DS1238 employs a band gap voltage reference and a precision comparator to monitor the 5 volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the $\overline{RVT}$, RST, and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the $\overline{RVT}$, RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1238-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, $\overline{RVT}$ will become inactive as soon as V_{CC} rises above V_{CCTP}. However, the RST and $\overline{RST}$ signals remain active for a minimum of 50 mS (100 mS typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize.

DS1238 FUNCTIONAL BLOCK DIAGRAM Figure 1



WATCHDOG TIMER

The DS1238 provides a watchdog timer function which forces the $\overline{WDS}$, RST, and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is described below in Table 1. The Watchdog timeout period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to timeout, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on $\overline{ST}$ must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the $\overline{WDS}$, RST, and $\overline{RST}$ outputs are driven to the active state. $\overline{WDS}$ is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The $\overline{WDS}$ pin will remain low until one of three operations occurs. The first is to strobe the $\overline{ST}$ pin with a falling edge, which will both set the $\overline{WDS}$ as well as the watchdog timer count. The second is to leave the $\overline{ST}$ pin open, which disables the Watchdog. Lastly the $\overline{WDS}$ pin is set whenever V_{CC} falls below V_{CCTP} and activates the $\overline{RVT}$ signal. The $\overline{ST}$ input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the Watchdog timer prior to time out. The Watchdog is disabled by leaving the $\overline{ST}$ input open, or as soon as V_{CC} falls to V_{CCTP}.

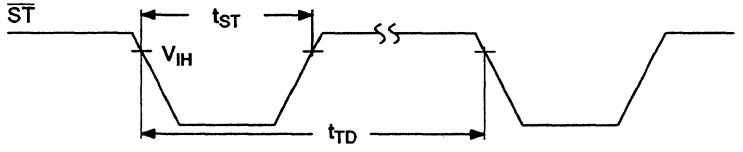
NON-MASKABLE INTERRUPT

The DS1238 generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238 requires that the voltage at the IN pin be limited to V_{IH}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1238 will force the $\overline{NMI}$ output to an active state. Noise is removed from the $\overline{NMI}$ power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore , the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power up, any IN pin levels below V_{TP} detected by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential active $\overline{NMI}$ will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power up depends on the relative voltage relationship between V_{CC} and the IN pin voltage. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to $V\overline{BAT}$, the $\overline{NMI}$ pin will enter a tri-state mode.

$\overline{ST}$ INPUT TIMING Figure 2

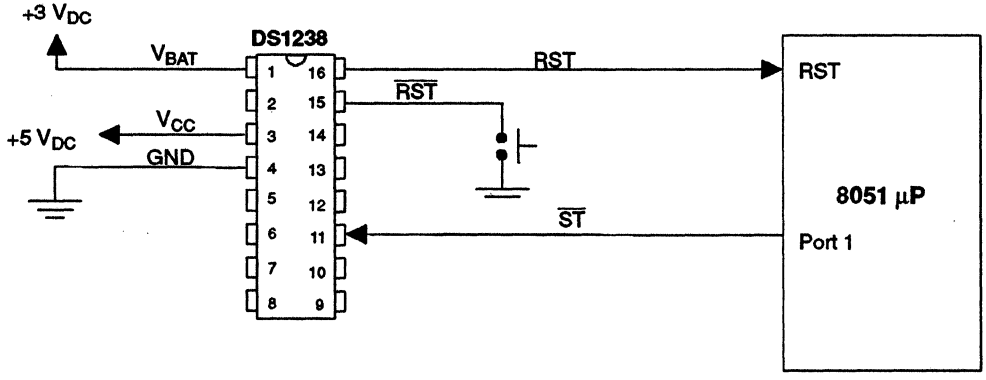


OSCILLATOR CONTROLS Table 1

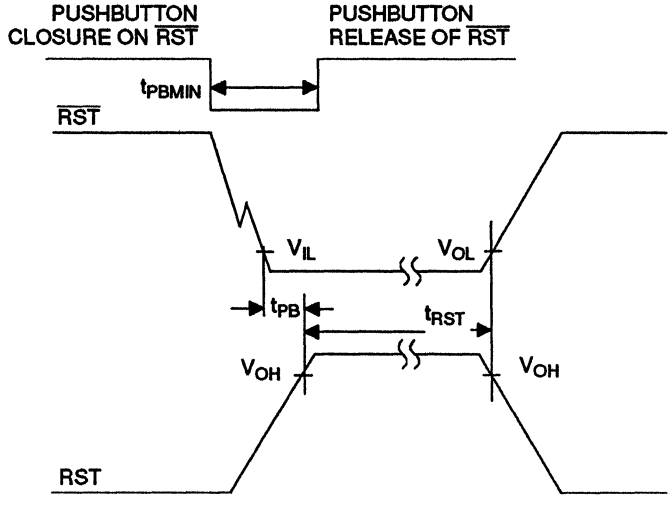
	OSCIN	OSCSEL	Watchdog Timeout Period (typ)		
			First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{550\ ms}{47\ pf}$ X Cpf	$\cong \frac{2.2\ sec}{47\ pf}$ X Cpf	$\cong \frac{69\ ms}{47\ pf}$ X Cpf
Internal	Low	Hi/Open	2.7 sec	170 mS	85 mS
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 mS

Note that the OSCIN and OSCSEL pins are tri-stated when V_{CC} is below V_{BAT}.

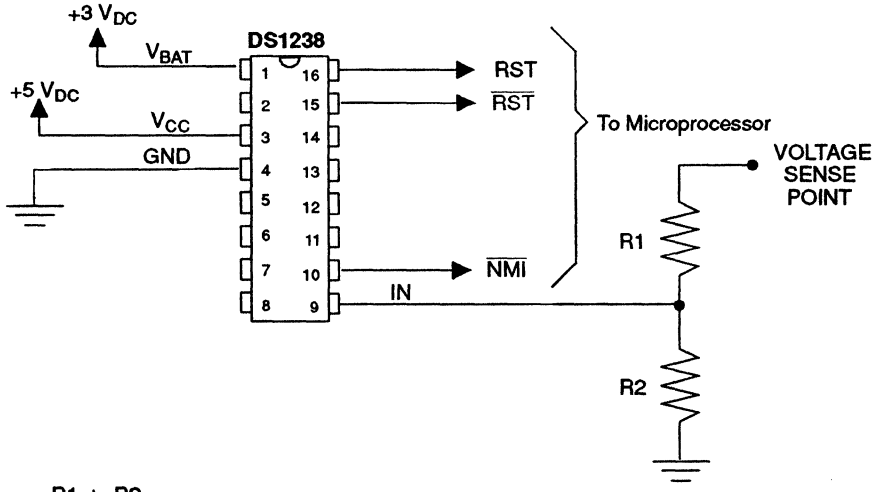
POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



PUSHBUTTON RESET TIMING Figure 4



NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

$$MAXVOLTAGE = \frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$$

Example 1: 5 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 4.8 Volts

$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1$$

$$= 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

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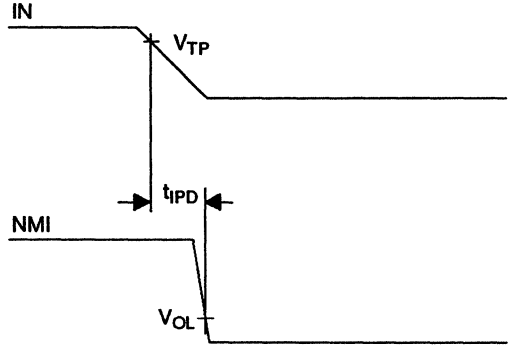
NMI FROM IN INPUT Figure 6



MEMORY BACKUP

The DS1238 provides all of the necessary functions required to battery backup a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. The output voltage diode drop from V_{BAT} (0.7 V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

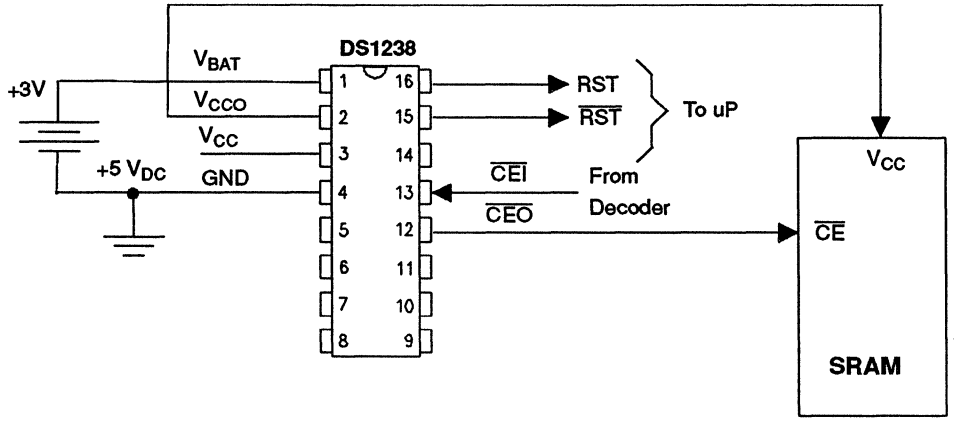
In order to conserve battery capacity during storage and/or shipment of an end system, the DS1238 provides an internal freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will result in the tri-state of outputs V_{CCO}, RST, $\overline{RST}$, and $\overline{CEO}$. The PF pin is not disabled by the freshness mode and will continue to source power from the V_{BAT} pin whenever V_{CC} is below V_{BAT}. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3-volt clock to TP1.

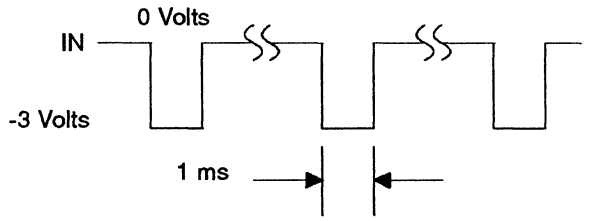
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238 may be too small to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power down, and from battery to V_{CC} on power up. The DS1336 is designed to use the PF output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

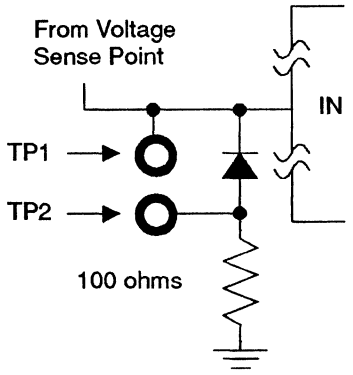
NONVOLATILE SRAM Figure 7



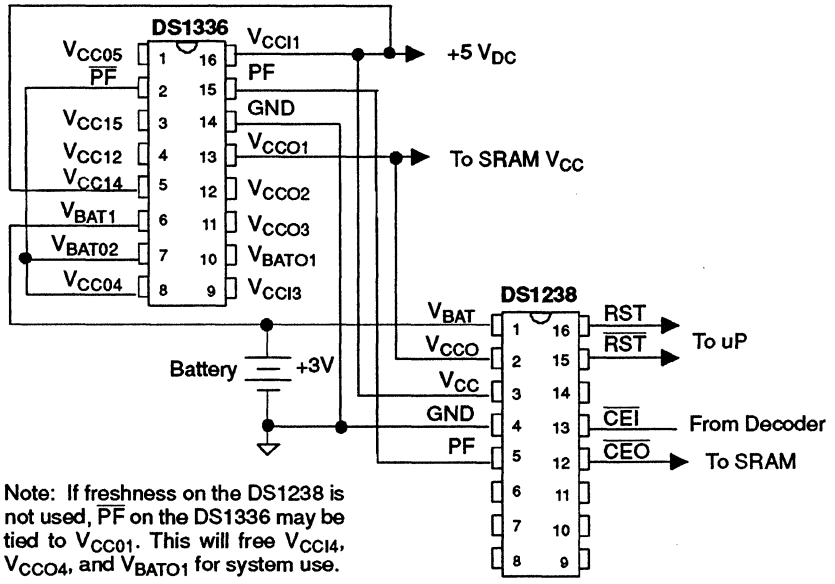
FRESHNESS SEAL Figure 8



Note: This series of pulses must be applied during normal +5 volt operation.



POWER SWITCHING Figure 9



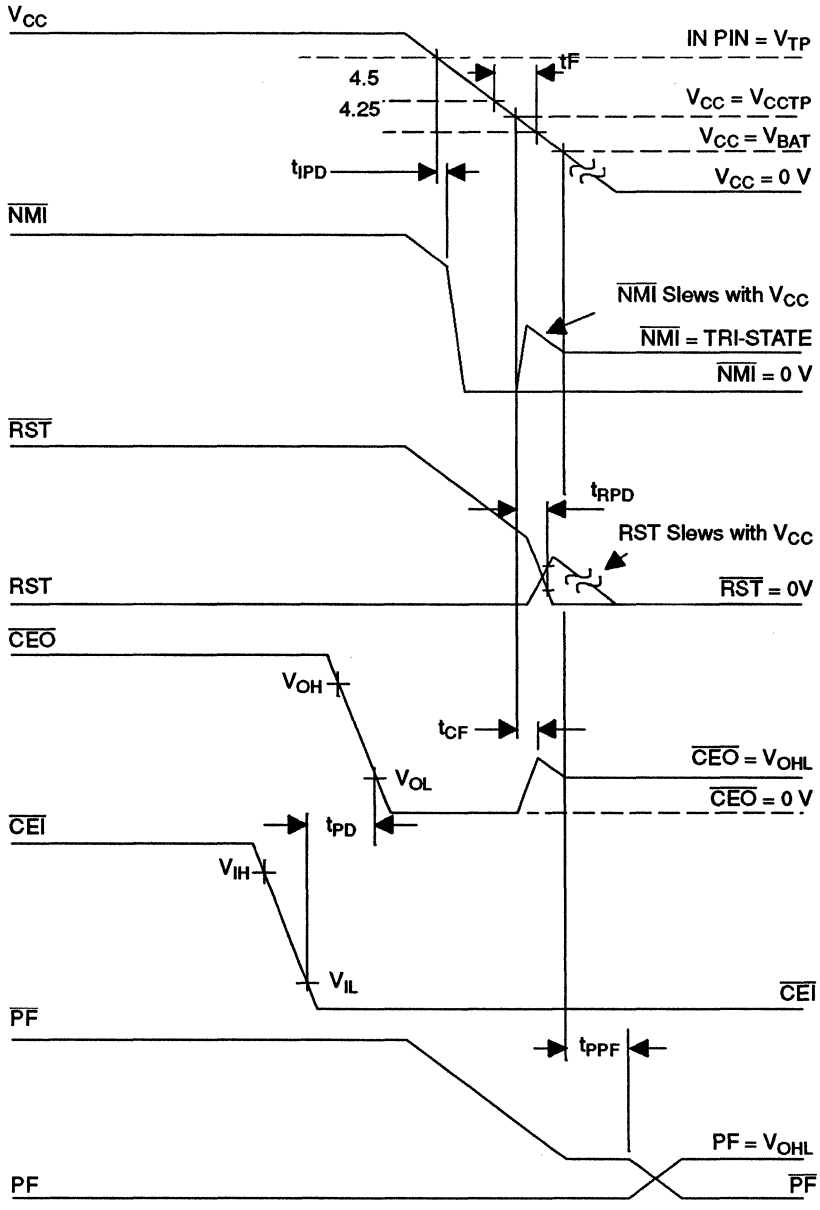
Note: If freshness on the DS1238 is not used, $\overline{PF}$ on the DS1336 may be tied to V_{CCO1}. This will free V_{CCI4}, V_{CCO4}, and V_{BATO1} for system use.

TIMING DIAGRAMS

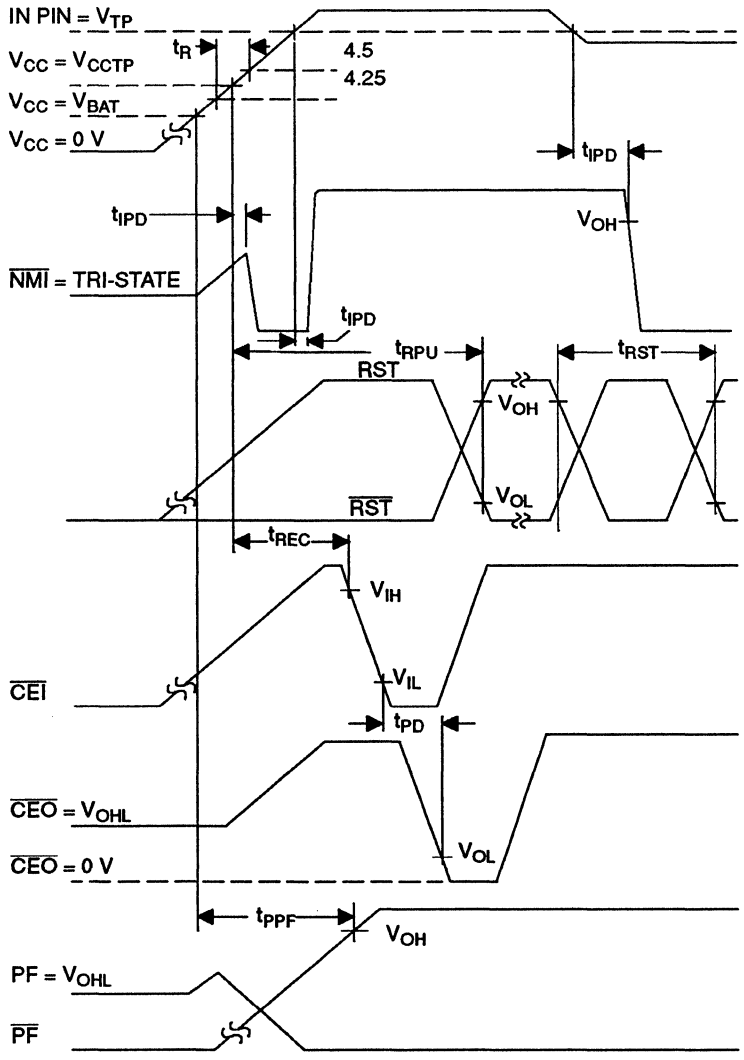
This section provides a description of the timing diagrams shown in Figure 10 and Figure 11. Figure 10 illustrates the relationship for power down. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. When V_{CC} reaches V_{CCTP}, and active RST and $\overline{RST}$ are given. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF pin.

Figure 11 shows the power up sequence. As V_{CC} slews above V_{BAT}, the PF pin is deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RPU} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue an $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

POWER DOWN TIMING Figure 10



POWER UP TIMING Figure 11



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	0		V_{CC}	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Battery Current	I_{BAT}	0		0.1	µA	2
Supply Output Current (V_{CCO} = V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Out Current (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}	V_{CC} -0.3			V	1
Battery Back Voltage	V_{CCO}		V_{BAT} -0.7		V	6
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.7		V	6
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	12
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @0.4V	I_{OL}			4.0	mA	9
Output Current @2.4V	I_{OH}	-1.0			mA	10
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	1.23	1.27	1.31	V	1

AC ELECTRICAL CHARACTERISTIC

($0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fall Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µS	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µS	
RESET Active OSCSEL=high	t_{RST}	50	85	150	mS	
$\overline{ST}$ Pulse Width	t_{ST}	20			nS	
PBRST @ V_{IL}	t_{PB}	30			mS	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µS	
Chip Enable Prop Delay	t_{PD}			20	nS	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	144	µS	11
V_{CC} Valid to RST (RC = 1)	t_{FPU}			100	nS	
V_{CC} Valid to RST	t_{RPU}	50	100	150	mS	5
V_{CC} Slew to 4.25 to V_{BAT}	t_{FB1}	10			µS	
Chip Enable Output Recovery Time	t_{REC}	.1			µS	7
V_{CC} Slew 4.25 to 4.75	t_R	0			µS	
Chip Enable Pulse Width	t_{CE}			5	µS	8
Watchdog Time Delay int clock Long period	t_{TD}		2.7		S	
Short period			170		mS	
Watchdog Time Delay, ext clock, After reset	t_{TD}		20480		clocks	
Normal			5120		clocks	
V_{BAT} Detect to PF	t_{PPF}			2	µS	
OSC IN Frequency	f_{OSC}	0		250	KHz	

CAPACITANCE

($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1238 can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1238 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. t_{REC} is the minimum time required before $\overline{CE}$/CEO memory access is allowed.
8. t_{CE} maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is 50 µA max.
10. All outputs except $\overline{RST}$ which is 50 µA min.
11. The $\overline{ST}$ pin will sink ± 50 µA in normal operation. The OSCIN pin will sink ± 5 µA in normal operation. The OSCSEL pin will sink ± 10 µA in normal operation.

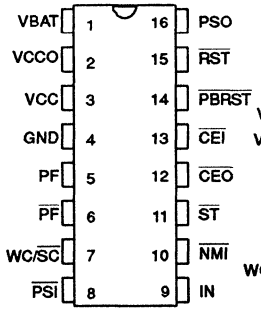
DALLAS SEMICONDUCTOR

DS1239
MicroManager Chip

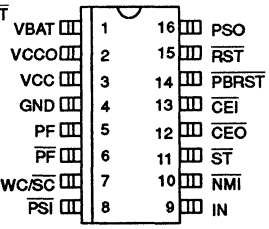
FEATURES

- Provides necessary control for start up and shutdown of power supply from keyboard
- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1239-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operate hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



DS1239 16-Pin DIP
(300 Mil)
See Mech Drawing
Sect. 16, Pg 1



DS1239 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Sect. 16, Pg 6

PIN DESCRIPTION

V_{BAT}	+3 Volt Battery Input
V_{CCO}	Switched SRAM Supply Output
V_{CC}	+5 Volt Power Supply Input
GND	Ground
PF	Power Fail (Active High)
$\overline{PF}$	Power Fail (Active Low)
WC/$\overline{SC}$	Wake-Up Control (Sleep)
$\overline{PSI}$	Power Supply Control Input
IN	Early Warning Input
$\overline{NMI}$	Non-Maskable Interrupt
$\overline{ST}$	Strobe Input
$\overline{CEO}$	Chip Enable Output
$\overline{CEI}$	Chip Enable Input
$\overline{PBRST}$	Push Button Reset Input
$\overline{RST}$	Reset Output (Active low)
PSO	Power Supply Control Outputs

DESCRIPTION

The DS1239 MicroManager provides all the necessary functions for power supply control and monitoring, reset control, and memory backup in microprocessor-based systems. Using the DS1239, an AC power switch is no longer required for microprocessor-based systems. A keyboard control system for power supply start up and shutdown is provided through the use of the Power Supply Control Input and Output. In other respects, the DS1239 is functionally identical to a DS1236 in the NMOS mode. For a complete description of the other DS1239 features, refer to the DS1236 data sheet. Pin-out of the DS1239 is identical to the DS1236 with two exceptions. The RC and RST pins have been replaced with $\overline{PSI}$ and PSO, respectively. Other pins and functions operate exactly as the DS1236 in NMOS mode. Operation of the power supply control function is described below.

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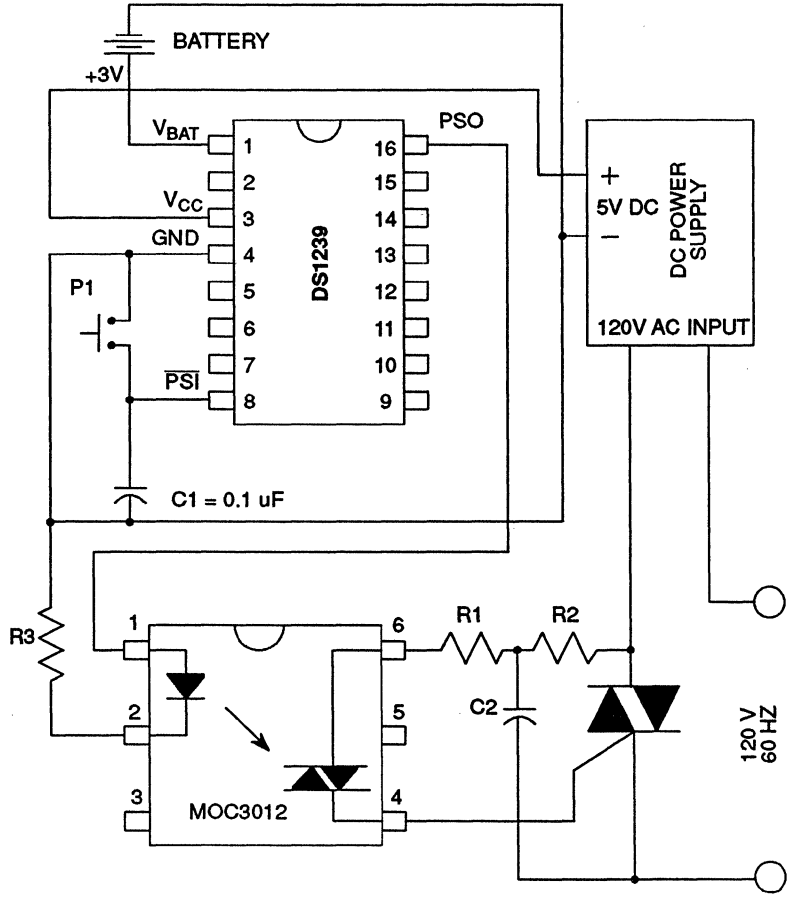
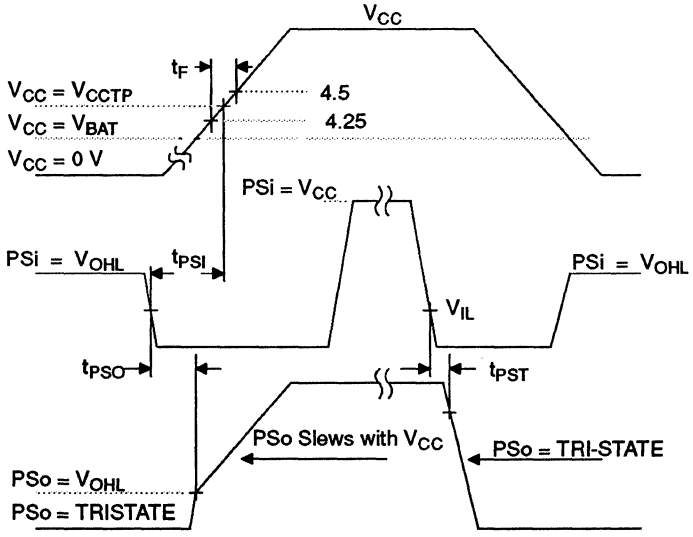
POWER SUPPLY CONTROL

The DS1239 facilitates the power-up and power down sequencing of a main power supply from a keyboard or pushbutton. The Power Supply Control Input ($\overline{PSI}$) and Power Supply Control Output (PSO) are used for this purpose. Prior to establishing a voltage on V_{CC} (+5V), the $\overline{PSI}$ is internally held at a high level at all times with the V_{BAT} supply. When $\overline{PSI}$ is forced low via a key pad or other source, the PSO is connected to the V_{BAT} to provide a high level. As shown in Figure 1, this active high signal can be wired directly to an optically isolated SCR to initiate an AC to DC power-up sequence. This in turn will provide the supply voltage for V_{CC}. The timing is illustrated in Figure 2. Holding the $\overline{PSI}$ input low, the PSO output will supply a connection to the V_{BAT} pin until the V_{CC} reaches V_{BAT}, or a maximum of 200 mS. If the supply voltage on V_{CC} rises above the V_{BAT} level before the t_{PSI} time-out, the PSO pin will remain high and track the V_{CC} input. If V_{CC} does not rise above V_{BAT} before either t_{PSI} or $\overline{PSI}$ is allowed to return to a high level, the PSO output will return to tristate. Once the PSO output and V_{CC} are set at a high level, a subsequent falling edge on $\overline{PSI}$ will tristate PSO to initiate a shut down condition. The 10 microamp current supplied by the $\overline{PSI}$ pin allows the use of a 0.1 µF capacitor as a simple pushbutton debounce circuit. The battery size for this application must be selected to provide the SCR on-current for the power supply response time and is consequently application-specific.

POWER SUPPLY CONTROL Figure 1



POWER SUPPLY CONTROL TIMING Figure 2



NOTES:

1. Minimum turn-on response time for AC-to-DC power supply.
2. PSO pulse width for V_{CC} held below V_{BAT}.
3. PSO will typically source 1.5 mA at 1.5V with V_{CC} = 0V, V_{BAT} = 3V.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature on the Leads	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

These specifications reflect the power supply control feature of the DS1239. For complete electrical specifications, refer to the DS1236 data sheet.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ Output Current	I_{PSI}		3		µA	
PSO Output Current	I_{PSO}	10			mA	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ to Valid V_{CC}	t_{PSI}			200	ms	1
$\overline{PSI}$ to PSO Tri-state	t_{PST}			20	ns	
$\overline{PSI}$ to Valid PSO	t_{PSO}			100	ns	
PSO Pulse Width	t_{PSP}		200	500	ms	2

DALLAS SEMICONDUCTOR

DS1267
Dual Digital Potentiometer Chip

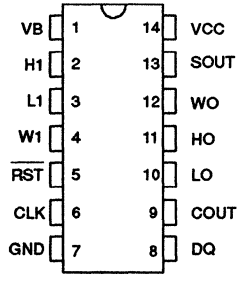
FEATURES

- Ultra-low power consumption
- Quiet, pumpless design
- Two digitally controlled, 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power-up is 50%
- Resistive elements are temperature-compensated to ± 0.3 LSB relative linearity
- Operating temperature range of 0° C to 70° C
- 16-Pin SOIC for surface-mount applications
- Resistance values:

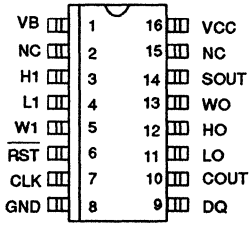
Device	Resolution	-3dB
DS1267-10: 10K	39 ohms	*1 MHz
DS1267-50: 50K	195 ohms	*200KHz
DS1267-100: 100K	390 ohms	*100KHz

* into voltage follower.

PIN ASSIGNMENT



14-Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg 1



16-Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg 6

PIN DESCRIPTION

L0, L1	Low end of resistor
H0, H1	High end of resistor
W1, W2	Wiper end of resistor
V_B	Substrate bias
S_{OUT}	Wiper for stacked configuration
$\overline{RST}$	Serial port reset input
DQ	Serial port data input
CLK	Serial port clock input
C_{OUT}	Cascade serial port output
V_{CC}	+5 volt input
GND	Ground
NC	No connection

DESCRIPTION

The DS1267 is a dual solid-state potentiometer that is set to value by digitally selected resistive elements. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistance array is set by an 8-bit register that controls which tap point is connected to the wiper output. Each 8-bit register can be read or written by sending or receiving data bits over a three-wire serial port.

In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1267 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same.

OPERATION

The DS1267 contains two potentiometers, each of which has its wiper set by a value contained in an 8-bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end. An 8-bit wiper register controls a 256-to-1 multiplexer that selects which tap point is connected to the wiper output.

In addition, the potentiometers can be stacked by connecting them in series such that the high end of Potentiometer 0 is connected to the low end of Potentiometer 1. When stacking potentiometers, the Stack Select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (S_{OUT}). A 0 written to the stack multiplexer will connect Wiper 0 to the S_{OUT} pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, Wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is present at the S_{OUT} pin.

Information is written and read from the Wiper 0 and Wiper 1 register and the Stack Select bit via the 17-bit I/O Shift register. The I/O Shift register is always serially loaded by a 3-wire serial port consisting of $\overline{RST}$, DQ, and clock. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17-bit shift register only when the $\overline{RST}$ input is at a high level. While at a high level, the $\overline{RST}$ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until $\overline{RST}$ is taken to low a level, which terminates data transfer. While $\overline{RST}$ input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O Shift register while $\overline{RST}$ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. **Data is always entered starting with the value of the Stack Select bit.** The 17th bit to be entered, therefore, will be the least significant of the Wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, not sending 17 bits may produce indeterminate potentiometer settings.

As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (C_{OUT}). By connecting the C_{OUT} pin to the DQ pin of a second DS1267, multiple devices can be daisy-chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1267s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the C_{OUT} pin of the last device connected in a daisy chain (one or more) must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between C_{OUT} and DQ when writing to the device (see Figure 3).

When reading data, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the resistor. This data bit can now be read by the reading device. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ. After 17 bits (17X devices for daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the Wiper 0 and Wiper 1 register and the Stack Select bit is loaded from the I/O shift register.

When power is applied to the DS1267, the device always has the wiper settings at half position and the Stack Select bit is at zero.

DS1267 LINEARITY MEASUREMENTS

An important specification for the DS1267 is linearity; that is, for a given digital input, how close is the analog output relative to that which is expected.

The test circuit used to measure the linearity of the DS1267 is shown in Figure 5. The part is set up in a worst case situation for linearity, which is the stacked configuration. This gives 512 possible settings for the composite potentiometer. Note that to get an accurate output voltage, it is necessary to assure that the output current is 0 in order to negate the effects of wiper impedances RW1 and RW0, which are typically 400 ohms. For any given setting N for the pot, the expected voltage out put at S_{OUT} is:

$$V_O = -5 + (10 \times [N/512]) \text{ [in volts]}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/512 or 0.01953 volts. The equation for the absolute linearity of the DS1267 is:

$$\frac{V_O \text{ (actual)} - V_O \text{ (expected)}}{\text{LSB}} = \text{AL (in LSBs)}$$

The specification for absolute linearity of the DS1267 is ± 0.75 LSB typical.

Figure 6 is a plot of absolute linearity AL and relative linearity (rel) versus wiper setting for a typical DS1267 at 25°C.

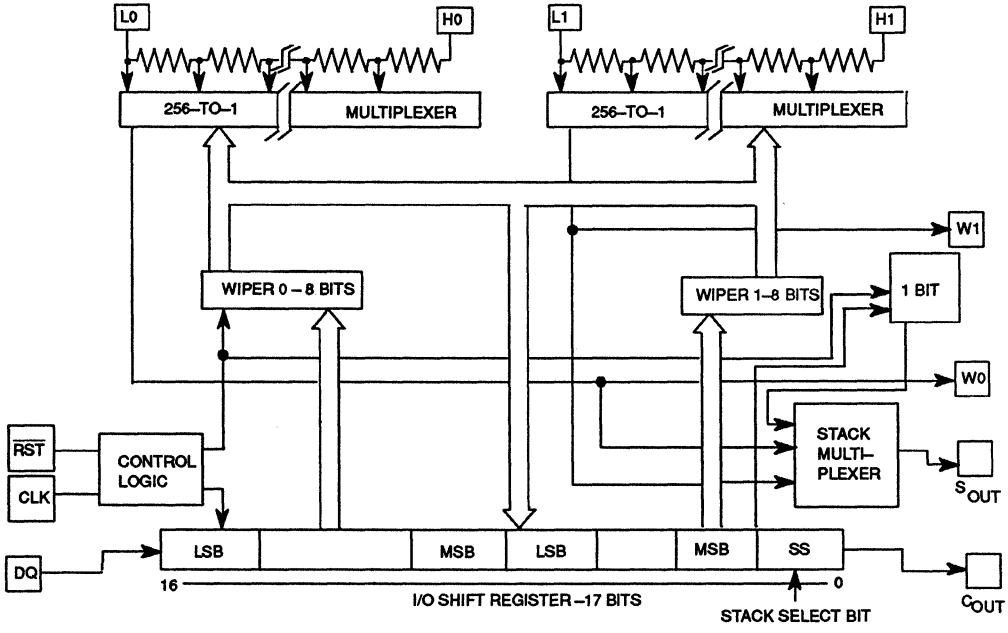
ANALOG CHARACTERISTICS

End-to-End Resistance Tolerance = ± 20%
Noise = < -120dB/ Hz Ref: 1V (Thermal)
Absolute Linearity = ± 0.75 LSB typical
Relative Linearity = ± 0.3 LSB typical
Temperature Coefficient = ± 800 PPM/°C typical

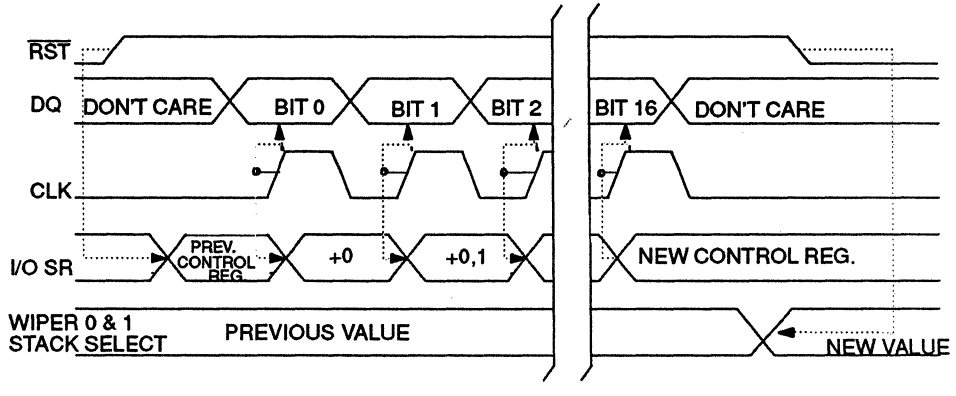
NOTES:

1. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
2. Relative linearity is used to determine the change in voltage between successive tap positions.
3. Typical values are for t_A = 25°C and nominal supply voltage.

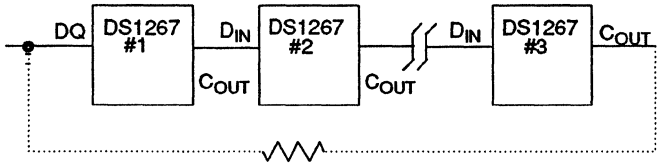
BLOCK DIAGRAM Figure 1



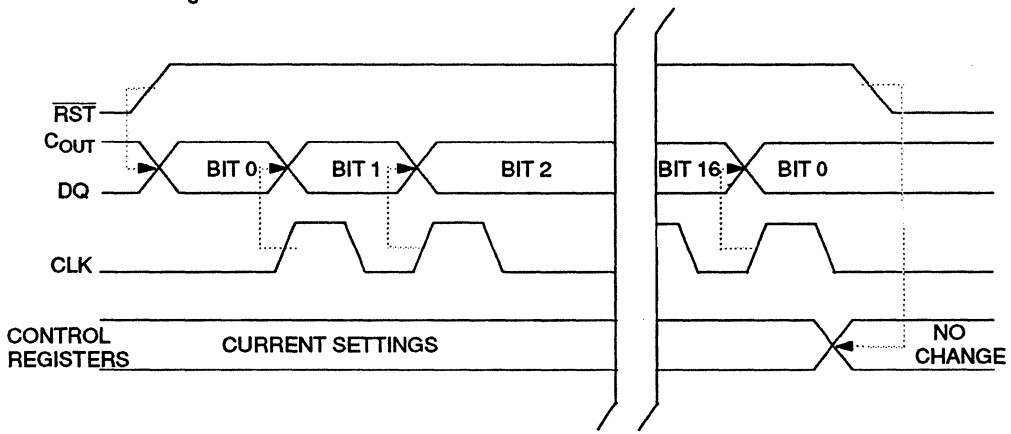
WRITING DATA Figure 2



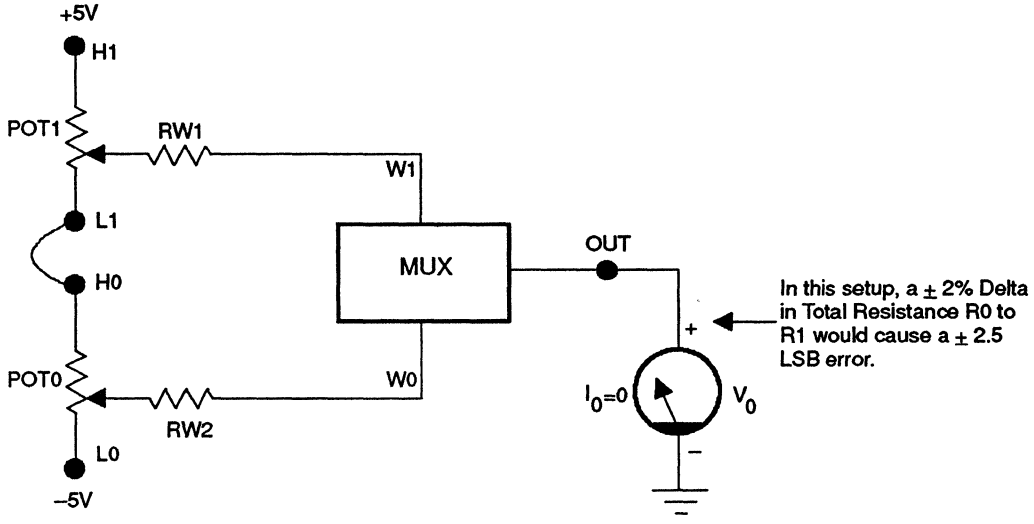
CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



LINEARITY MEASUREMENT CONFIGURATION Figure 5



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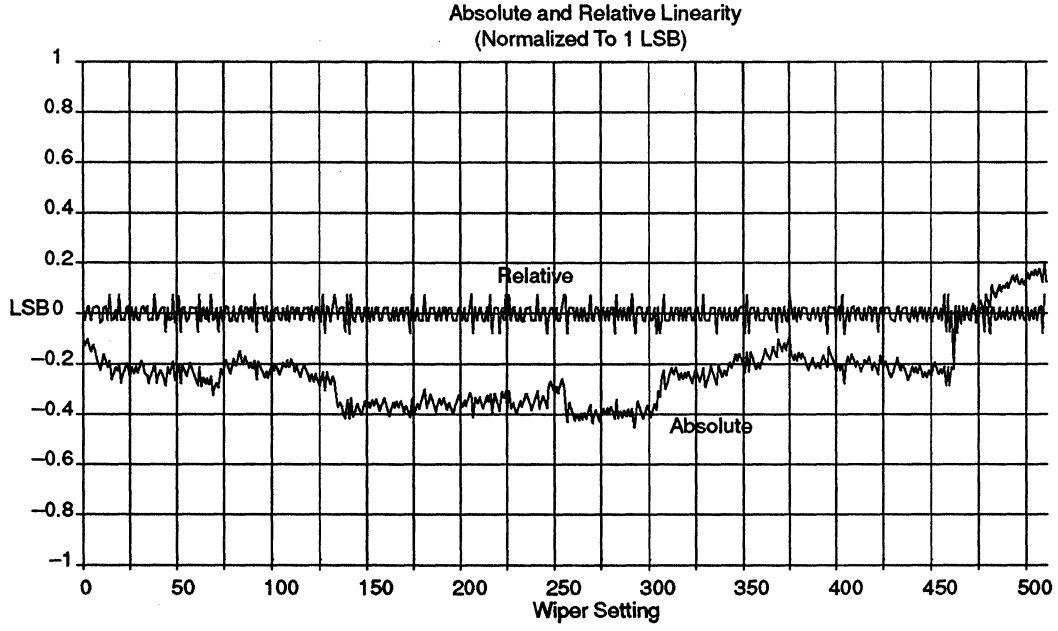
DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground (V_B=GND)	-1.0V to +7.0V
Voltage on Resistor Pins when V_B= -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	-0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.0	Volts	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	Volts	1
Input Logic 0	V_{IL}	-0.5		+0.8	Volts	1
Substrate Bias	V_B	-5.5		GND	Volts	1
Resistor Inputs	L,H,W	V_B -0.5		V_{CC} +0.5	Volts	2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		22	650	µA	6
Input Leakage	I_{LI}	-1		+1	µA	
Wiper Resistance	R_W		400	1000	Ohms	
Wiper Current	I_W		1		mA	
Output Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	-1.0			mA	4
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	4
Standby Current	I_{STBY}		22		µA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

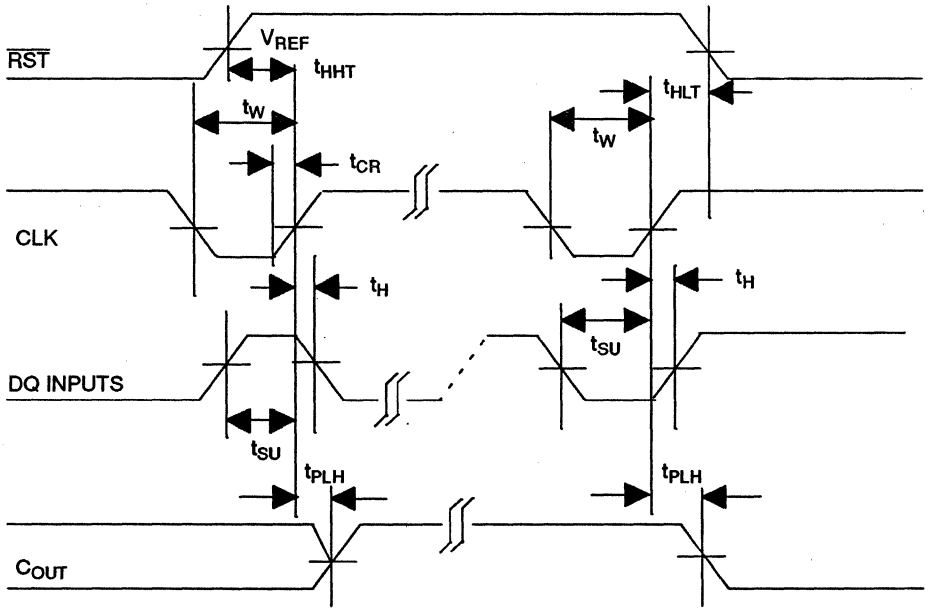
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	
$\overline{RST}$ High to Clock Input High	t_{HHT}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	
CLK Rise Time	t_{CR}			50	ns	

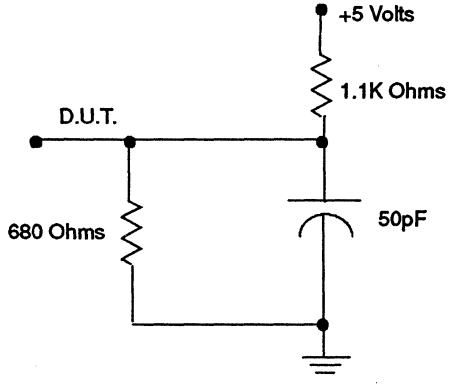
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction.
3. Measured with a load as shown in Figure 8.
4. V_{REF} = 1.5 volts.
5. See Figure 9.

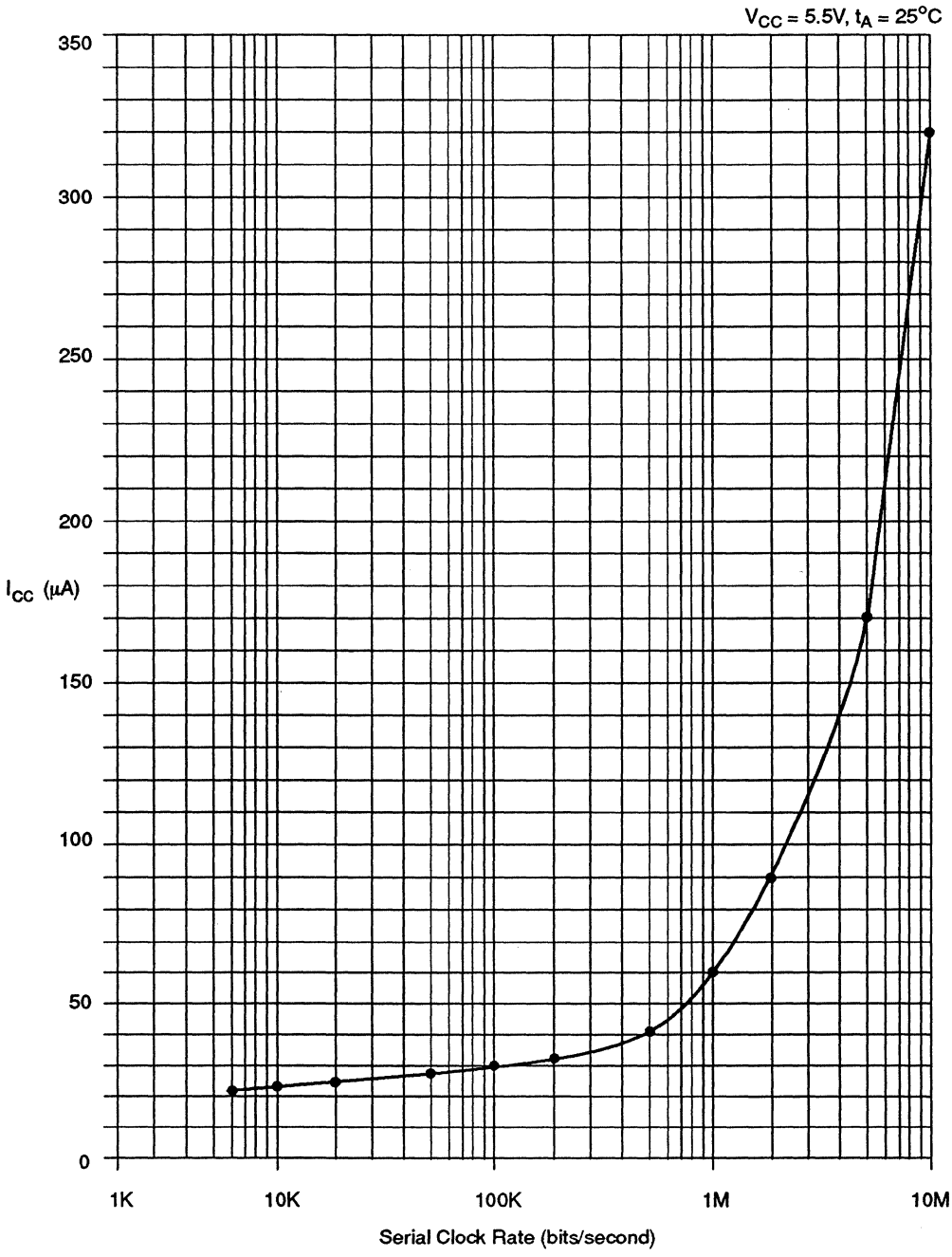
TIMING DIAGRAM Figure 7



DIGITAL OUTPUT LOAD SCHEMATIC Figure 8



TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 9



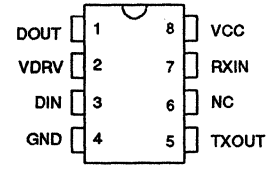
DALLAS SEMICONDUCTOR

DS1275
Line-Powered RS-232 Transceiver Chip

FEATURES

- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-C port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-C signals
- Available in 8-pin, 150-mil wide SOIC package (DS1275S)
- Low-power CMOS

PIN ASSIGNMENT



DS1275 8-Pin DIP (300 Mil.)
See Mech. Drawing – Sect. 16, Pg. 1

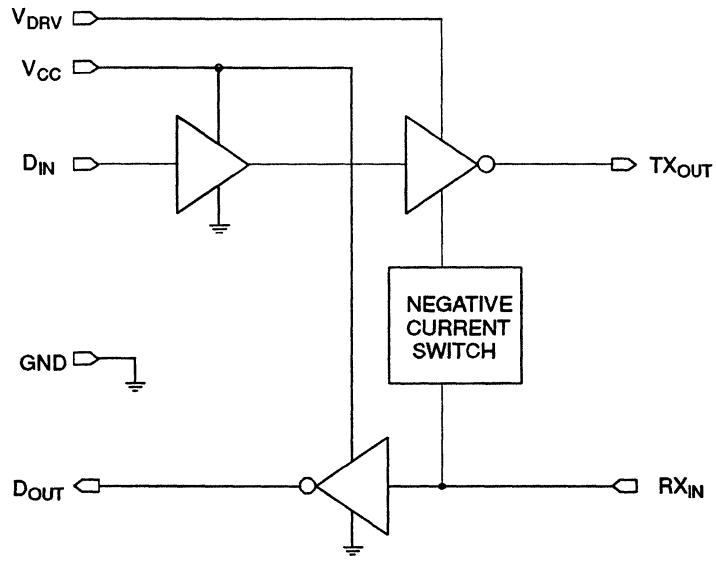
PIN DESCRIPTION

D_{OUT}	- Digital data out
V_{DRV}	- Transmit driver +V
D_{IN}	- Digital data in
GND	- System ground (0V)
TX_{OUT}	- Transmit RS-232 out
NC	- No connection
RX_{IN}	- Receive RS-232 in
V_{CC}	- System logic supply (+5V)

DESCRIPTION

The DS1275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS1275 BLOCK DIAGRAM Figure 1



OPERATION

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RX_{IN}) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TX_{OUT}) when data is sent. However, since synchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RX_{IN} pin is the receive input for an RS-232 signal whose levels can range from ± 3 to ± 15 volts. A negative data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RX_{IN} is D_{OUT} which swings from $+V_{CC}$ to ground. Therefore, a mark on RX_{IN} produces a logic 1 at D_{OUT}; a space produces a logic 0.

The input threshold of RX_{IN} is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause D_{OUT} to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause D_{OUT} to switch again. An open on RX_{IN} is interpreted as a mark, producing a logic 1 at D_{OUT}.

TRANSMITTER SECTION

D_{IN} is the CMOS/TTL-compatible input for digital data from the user system. A logic 1 at D_{IN} produces a mark (negative data signal) at TX_{OUT} while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the RX_{IN} line for swinging to negative levels. The RX_{IN} line must be in a marking or idle state to take advantage of this design; if RX_{IN} is in a spacing state,

TX_{OUT} will only swing to ground. When TX_{OUT} needs to transition to a positive level, it uses the V_{DRV} power pin for this level. V_{DRV} can be a voltage supply between 5 to 12 volts, and in many situations it can be tied directly to the +5 volt V_{CC} supply. *It is important to note that V_{DRV} must be greater than or equal to V_{CC} at all times.*

The voltage range on V_{DRV} permits the use of a 9-volt battery in order to provide a higher voltage level when TX_{OUT} is in a space state. When V_{CC} is shut off to the DS1275 and V_{DRV} is still powered (as might happen in a battery-backed condition) , only a small leakage current (about 50-100 nA) will be drawn. If TX_{OUT} is loaded during such a condition, V_{DRV} will draw current only if RX_{IN} is not in a negative state. During normal operation (V_{CC}=5 volts), V_{DRV} will draw less than 2 uA when TX_{OUT} is marking. Of course, when TX_{OUT} is spacing, V_{DRV} will draw substantially more current – about 3 mA depending upon its voltage and the impedance that TX_{OUT} sees.

The TX_{OUT} output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TX_{OUT} should be inadvertently shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

RS-232 COMPATIBILITY

The intent of the DS1275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least ± 5 volts minimum when terminated by a 3K ohm load and V_{DRV}= +5 volts. Typically a voltage of 4 volts will be present at TX_{OUT} when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

APPLICATIONS INFORMATION

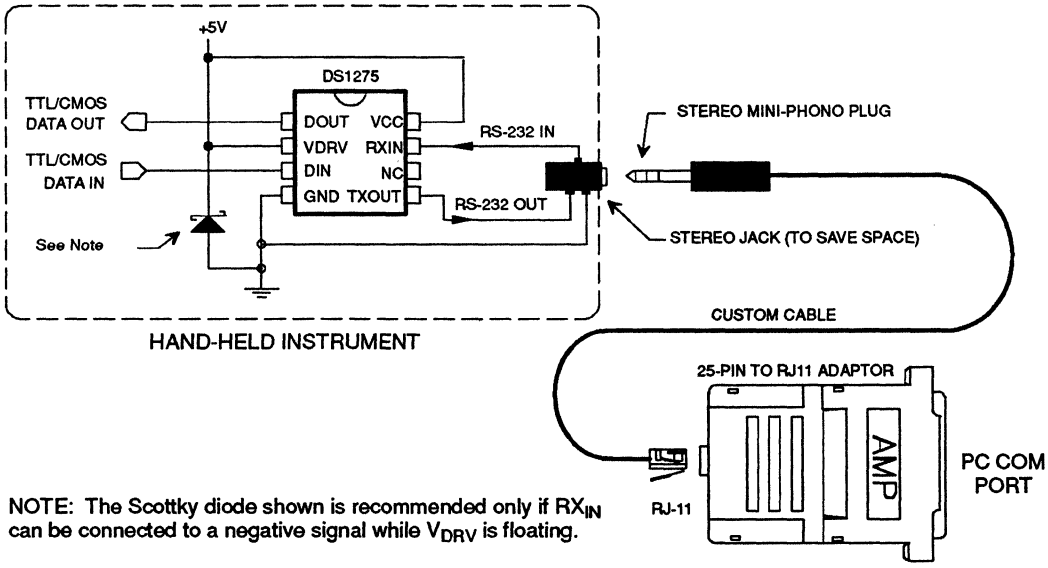
The DS1275 is designed as a low-cost, RS-232-C interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS1275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TX_{OUT} output, the DS1275 only draws significant V_{DRV} current when TX_{OUT} transitions positively (spacing). This current flows primarily into the RS-232 receiver's 3-7K ohm load at the other end of the attaching cable. When TX_{OUT} is marking (a negative data signal), the V_{DRV} current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

To obtain the lowest power consumption from the DS1275, observe the following guidelines. First, to minimize V_{DRV} current when connected to an RS-232 port, always maintain D_{IN} at a logic 1 when data is not being transmitted (idle state). This will force TX_{OUT} into the marking state, minimizing V_{DRV} current. Second, V_{DRV} current will drop to less than 100 nA when V_{CC} is grounded. Therefore, if V_{DRV} is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

FULL-DUPLEX OPERATION

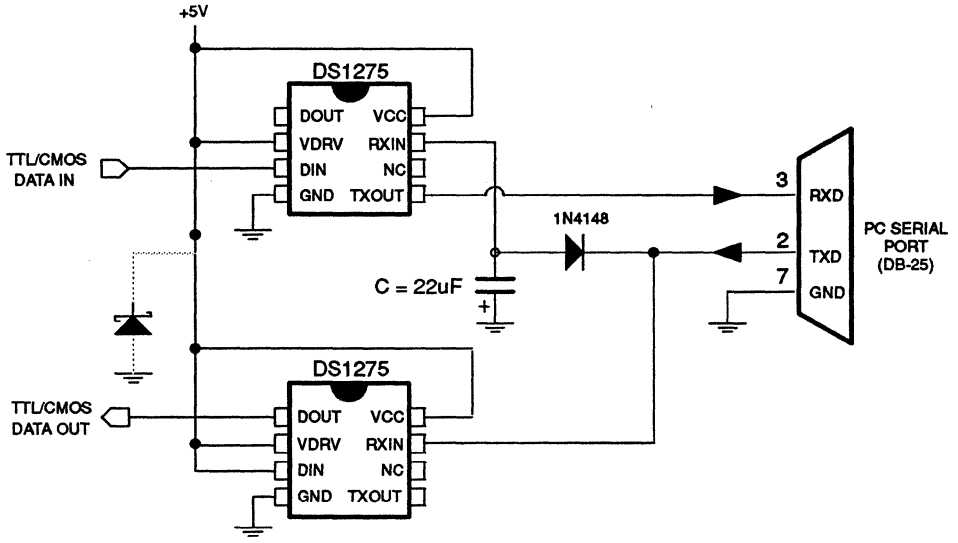
The DS1275 is intended primarily for half-duplex operation; that is, RX_{IN} should remain idle in the marking state when transmitting data out TX_{OUT} and visa versa. However, the part can be operated full-duplex with most RS-232-C serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-C receiver device. The 5-volt swing occurs when TX_{OUT} attempts to swing negative while RX_{IN} is at a positive voltage, which turns on an internal weak pull-down to ground for the TX_{OUT} driver's negative reference. So, transmit mark signals at TX_{OUT} may have voltage jumps from some negative value (corresponding to RX_{IN} marking) to approximately ground. One possible problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full- duplex circuit shown in Figure 3 can be used as an alternative. The 22 µF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TX_{OUT} still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7K ohms). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TX_{OUT} signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TX_{OUT} to swing both positive and negative in full-duplex operation with this device.

HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



NOTE: The Scottky diode shown is recommended only if RX_{IN} can be connected to a negative signal while V_{DRV} is floating.

FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



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NOTE:

The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS1275's TX_{OUT} uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TX_{OUT} is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TX_{OUT}. However, when TXD is marking, the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

LATCHUP PROTECTION

In most cases the DS1275 offers a high level of ESD and latchup protection. However, latchup can occur if V_{DRV} is left floating (high impedance) while a negative signal is attached to RX_{IN}. One possible scenario for this is as follows: if the handheld device is powered off with a FET switch, floating V_{DRV}, and at the same time the user still has the the RS-232-C port connected. In order to eliminate this latchup potential, a Schottky diode from V_{DRV} to ground is recommended as shown in Figure 2. The lower clamp voltage of the Schottky (300 mV) is required to prevent an internal silicon diode on the DS1275 from turning on, which precipitates the latchup condition.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	-0.3 to +7 volts
V_{DRV}	-0.3 to +13 volts
RX_{IN}	± 15 volts
D_{IN}	-0.3 to V_{CC} + 0.3 volts
TX_{OUT}	± 15 volts
D_{OUT}	-0.3 to V_{CC} + 0.3 volts
Storage Temperature	-55° to + 125°C
Operating Temperature	0° to 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V_{CC}	4.5	5.0	5.5	volts	1
Transmit Driver Supply	V_{DRV}	4.5	5-12	13.0	volts	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	volts	2
Logic 0 Input	V_{IL}	-0.3		+ 0.8	volts	
RS-232 Input Range (RX_{IN})	V_{RS}	-15		+15	volts	
Dynamic Supply Current $D_{IN} = V_{CC}$ D_{IN} = GND	 I_{DRV1} I_{CC1} I_{DRV1} I_{CC1}		 0.1 0.5 3.8 0.5	 5.0 5.0 5.0 5.0	 mA mA mA mA	3
Static Supply Current $D_{IN} = V_{CC}$ D_{IN} = GND	 I_{DRV2} I_{CC2} I_{DRV2} I_{CC2}		 1.5 10.0 3.8 10.0	 15.0 15.0 5.0 30.0	 µA µA mA µA	4
Driver Leakage Current (V_{CC}= 0V)	I_{DRV3}		0.05	1.0	µA	5

DC ELECTRICAL CHARACTERISTICS

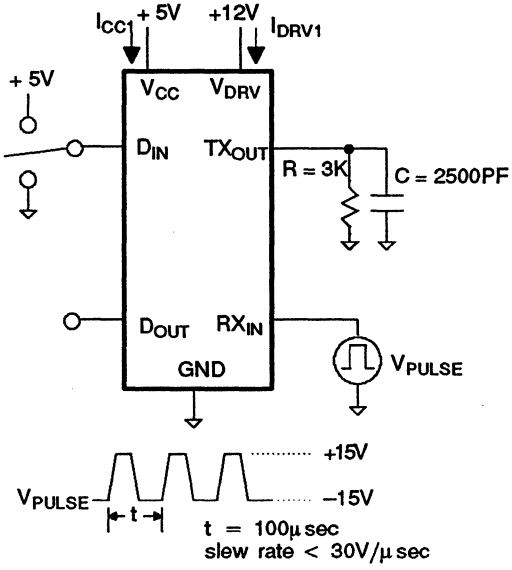
(0° to 70°C, $V_{CC} = V_{DRV} = 5V \pm 10\%$)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
TX_{OUT} Level High	V_{OTXH}	3.5	4.0	4.5	volts	6
TX_{OUT} Level Low	V_{OTXL}	-8.5	-9.0		volts	7
TX_{OUT} Short Circuit Current	I_{SC}		+60	+85	mA	
TX_{OUT} Output Slew Rate	t_{SR}			30	V/µs	
Propagation Delay	t_{PD}		5		µs	8
RX_{IN} Input Threshold Low	V_{TL}	0.8	1.2	1.6	volts	
RX_{IN} Input Threshold High	V_{TH}	1.6	2.0	2.4	volts	
RX_{IN} Threshold Hysteresis	V_{HYS}	0.5	0.8		volts	9
D_{OUT} Output Current @ 2.4 V	I_{OH}	-1.0			mA	
D_{OUT} Output Current @ 0.4 V	I_{OL}			3.2	mA	

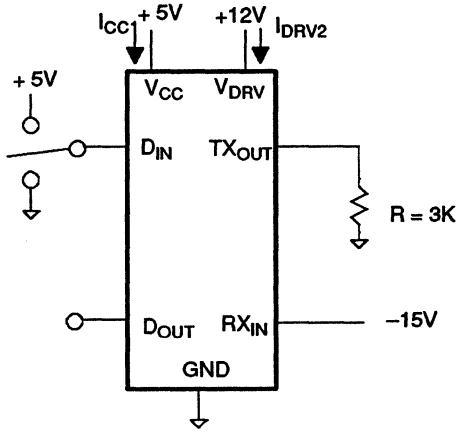
NOTES:

1. V_{DRV} must be greater than or equal to V_{CC}.
2. $V_{CC} = V_{DRV} = 5V \pm 10\%$.
3. See test circuit in Figure 4.
4. See test circuit in Figure 5.
5. See test circuit in Figure 6.
6. $D_{IN} = V_{IL}$ and TX_{OUT} loaded by 3K ohms to ground.
7. $D_{IN} = V_{IH}$, RX_{IN} = -10 volts and TX_{OUT} loaded by 3K ohms to ground.
8. D_{IN} to TX_{OUT} - see Figure 7.
9. $V_{HYS} = V_{TH} - V_{TL}$.

DYNAMIC OPERATING CURRENT TEST CIRCUIT Figure 4



STATIC OPERATING CURRENT TEST CIRCUIT Figure 5



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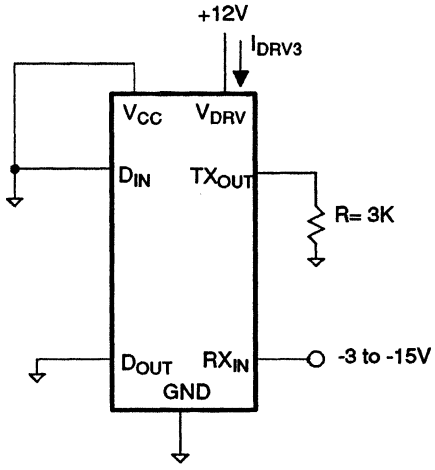
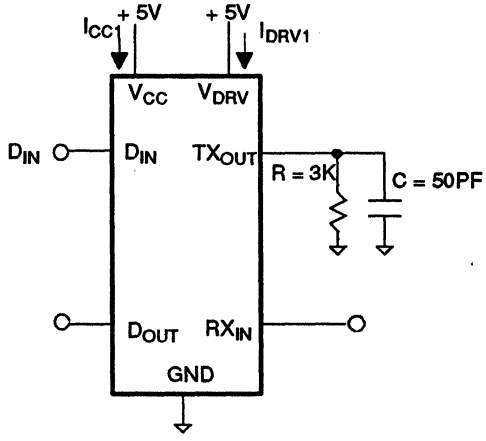
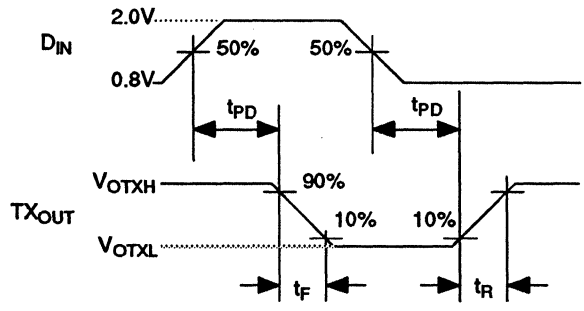
DRIVER LEAKAGE TEST CIRCUIT Figure 6



PROPAGATION DELAY TEST CIRCUIT Figure 7





$$t_{SR} = \frac{0.8(V_{OTXH} - V_{OTXL})}{t_F \text{ or } t_R}$$

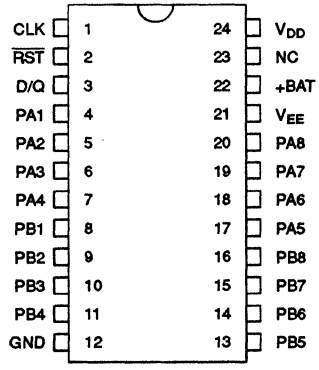
DALLAS SEMICONDUCTOR

DS1277
8–Channel Crosspoint Switch

FEATURES

- Any port A input/output can be programmed for connection to any port B input/output
- Registers which define port connections are programmable via a 3–wire serial port
- All port input/output pins will accept both analog and digital signals
- Optional +5 volts and ±5 volts operation
- Switch registers can be made nonvolatile with external connection of a 3-volt lithium battery
- Applications include:
  - digital/analog switching and multiplexing
  - data scrambling for secure transmission

PIN ASSIGNMENT



24-Pin DIP (600 mil)
See Mech. Drawing
Sect. 16, Pg 4

PIN DESCRIPTION

+BAT	-	Battery Input
NC	-	No Connection
V_{EE}	-	Optional -5 Volts Supply Input
PA1 - PA8	-	Port A Input/Output
GND	-	Ground
PB1 - PB8	-	Port B Input/Output
D/Q	-	Serial Port Data Input/Output
CLK	-	Serial Port Clock
$\overline{RST}$	-	Serial Port Reset
V_{DD}	-	5 Volts Power Supply

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DESCRIPTION

The DS1277 8-Channel Crosspoint Switch Chip is a programmable, low-power CMOS switching device which has the capacity to interconnect eight digital or analog signals in any combination. Interconnection is controlled by eight data registers of eight bits each which are read and written via a 3-wire serial port. The eight registers define the 64 possible combinations of the internal crosspoint switch. The DS1277 can be operated from a single +5 volts supply or optional ±5 volts operation can be selected to allow inputs and outputs to swing above and below ground.

OPERATION – GENERAL

With the -5 volts input grounded and +5 volts applied to pin 24, input/output pins of ports A and B will accept voltage levels between 0 and 5 volts. When V_{EE} is connected to -5 volts with +5 volts applied to pin 24, the input/output pins of ports A and B will accept voltage levels between -5 and +5 volts. Regardless of the voltage selections, applied voltages on port pins will be reproduced on pins which are interconnected by the internal crosspoint switch as defined by the data register settings.

The data registers are shown in Figure 1. As defined, each register specifies one port B I/O pin. Each of the eight bits of the register specifies connection or no connection to each of the port A I/O pins. A logic 1 causes a connection and a logic 0 is a no connection. When the DS1277 is powered up, all register bits are forced to a zero unless a battery voltage of greater than 2 volts is present on pin 22. With proper battery voltage, all registers are retained in the programmable state. If the nonvolatile feature is not used then pin 22 must be grounded.

OPERATION – SERIAL PORT

The eight data registers of the DS1277 are written and read via a 3-wire serial port consisting of $\overline{RST}$, CLK, and D/Q. To initiate data transfer with the DS1277, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines either a read or a write. If a match does not exist communication will be ignored. If the command register is properly loaded then communication is allowed to continue and the next 64 cycles to the DS1277 will either update the data registers or read the data register content when the data registers are being updated. Switch settings are not affected until $\overline{RST}$ is driven low at the end of the 64-bit data transfer.

COMMAND WORD

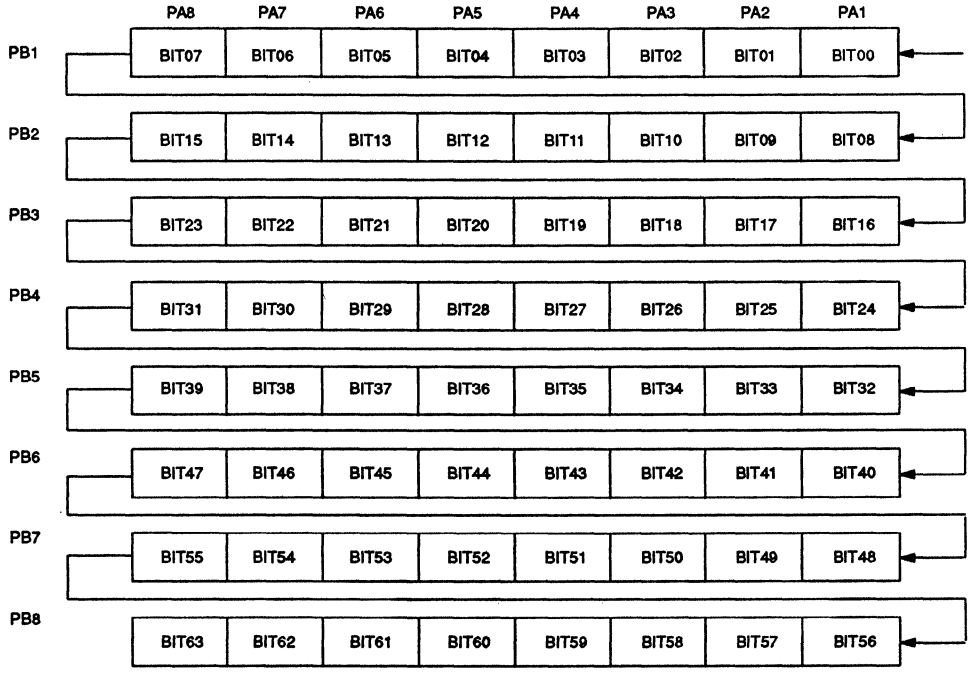
Each data transfer begins with a 3-byte command word as shown in Figure 3. The first byte of the command word specifies whether the 64-bit data registers will be written or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted. The 8-bit pattern for read is 01000110. The pattern for write is 10111001. The second and third bytes of the command word must match the exact pattern 00000000, 11110000 or data transfer is aborted.

RESET AND CLOCK CONTROLS

All data transfers are initiated by driving the $\overline{RST}$ input high. $\overline{RST}$ must remain high for the entire 24-bit command word and the 64-bit data stream. The $\overline{RST}$ input terminates communication and updates the switch settings only after all 64 bits of the data registers have been written when reset is driven low. Reading of registers can be terminated at any time by driving $\overline{RST}$ low.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate and D/Q goes to a high impedance state if the $\overline{RST}$ input is low. Transfer of register data to switches occurs as $\overline{RST}$ is driven low only if 64 bits of data have been written. $\overline{RST}$ has no other effect on the register content. Data transfer is illustrated in Figures 4, 5 and 6.

DATA REGISTERS Figure 1



NOTE: Logic 1 closes switch
Logic 0 opens switch

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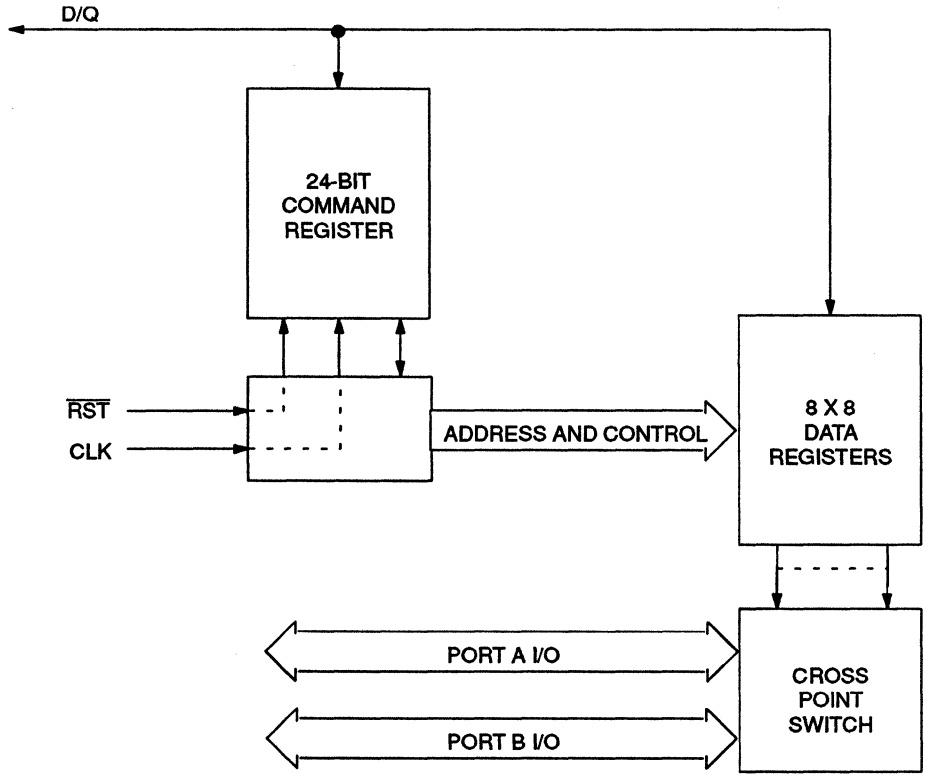
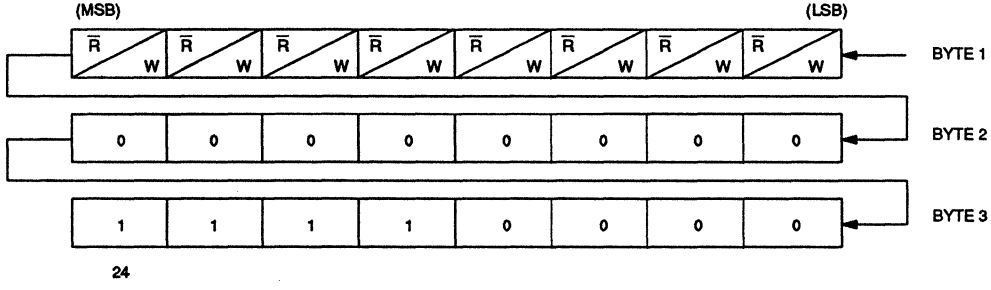
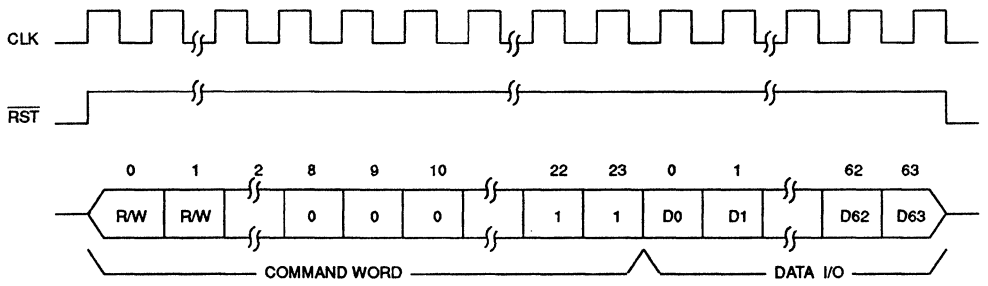
BLOCK DIAGRAM Figure 2



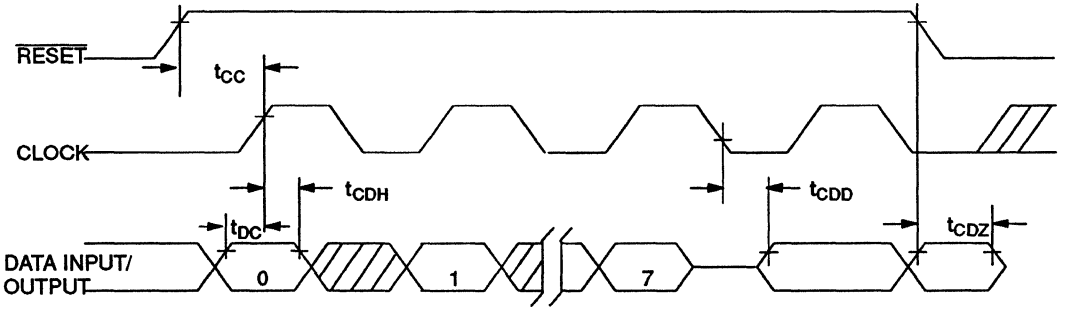
COMMAND REGISTER Figure 3



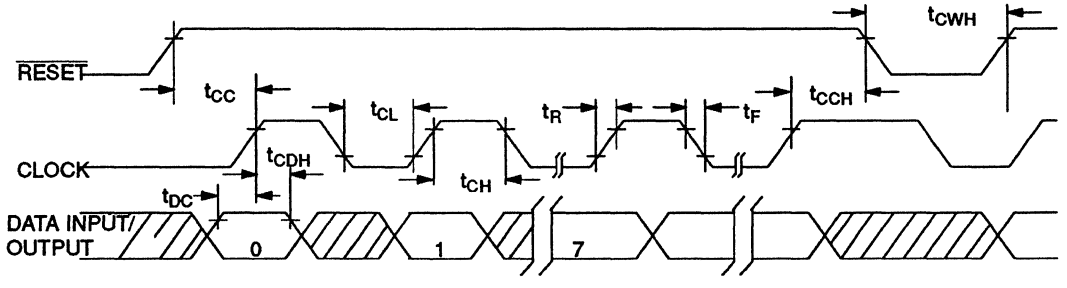
COMMAND WORD/DATA TRANSFER Figure 4



READ DATA TRANSFER Figure 5



WRITE DATA TRANSFER Figure 6



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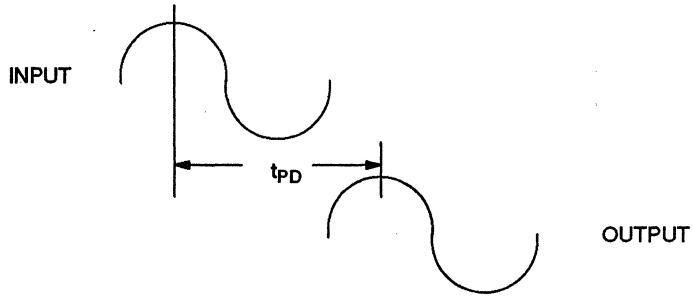
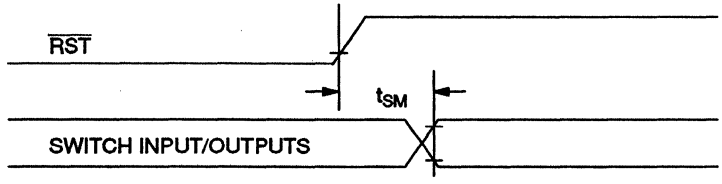
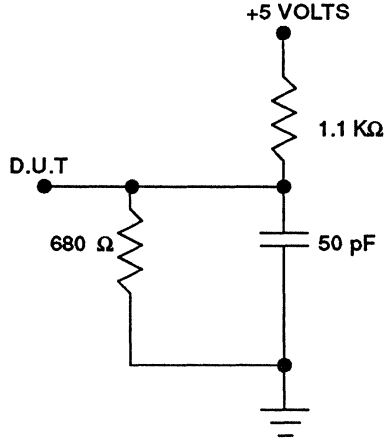
TIMING DIAGRAM: SWITCH PROPAGATION DELAY Figure 7



TIMING DIAGRAM: SWITCH CONNECT t_{PD} Figure 8



OUTPUT LOAD Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–5.5V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	V_{DD}	4.5	5.0	5.5	V	1
- Supply Voltage	V_{EE}	0	-5.0	-5.5	V	1
Serial Port Logic 0	V_{IL}	-0.3		0.8	V	1
Serial Port Logic 1	V_{IH}	2.0		V_{DD} +0.3	V	1
A @ B Port Input	V_{IN}	0		V_{DD}	V	-Supply=GND
A @ B Port Input	V_{IN}	$-V_{EE}$		V_{DD}	V	-Supply=-5.0V
+Battery Input	V_{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{EE} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
D/Q Output Current @ 2.4V	I_{OH}	-1			mA	2
D/Q Output Current @ 0.4V	I_{OL}			+4	mA	2
Input Leakage	I_{IL}	-1		+1	µA	3
Output Leakage	I_{OH}	-1		+1	µA	3
X Switch On Impedance	X_{ON}		250	500	ohms	4
+ Supply Current Active	I_{DD1}			10	mA	
+ Supply Current Quiescent	I_{DD2}		7		mA	5
- Supply Current	I_{EE}			1	mA	
X Switch Off Impedance	X_{OFF}	1 Meg			ohms	
Battery Current @ 3V	I_{BAT}			100	nA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	
Feedthrough Capacitance	C_{IN}-C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	50			ns	6
CLK to Data Delay	t_{CDD}			200	ns	2, 6, 7
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	s_{CLK}	DC		2.0	MHz	6
CLK Rise and Fall	t_{RTF}			500	ns	6
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	6
CLK to $\overline{RST}$ Hold	t_{CCH}	50			ns	6
RST to I/O High Z	t_{CDZ}			75	ns	6
Input to Output Delay	t_{PD}			50	ns	
$\overline{RST}$ Low to Switch Transition	t_{SM}			50	ns	
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	

NOTES

1. All voltages are referenced to ground (V_{SS}).
2. Measured with a load as shown in Figure 9.
3. V_{DD} = +5 volts, V_{EE} = -5 volts, V_{SS} = GND: all other pins open.
4. X switch impedance is the terminal resistance of connected switch inputs to outputs.
5. V_{DD} = +5 volts, V_{EE} = -5 volts, V_{SS} = GND, $\overline{RST}$ = V_{IL}: all other pins open.
6. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise (t_R) and fall times (t_F).
7. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.

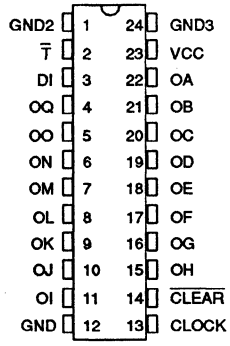
DALLAS SEMICONDUCTOR

DS129x Eliminator

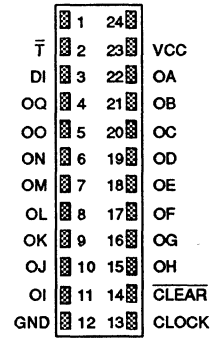
FEATURES

- Replaces 8 or 16 hard-to-get-at manual switches
- Options printed circuit board via software
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention for DS1290 and DS1292

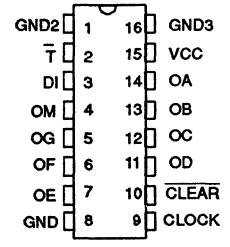
PIN ASSIGNMENT



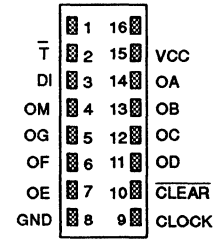
DS1293 24-Pin DIP (300 Mil) See Mech. Drawing Sect. 16, Pg 1



DS1292 24-Pin Encapsulated Package (450 Mil) See Mech. Drawing – Sect. 16, Pg. 8



DS1291 16-Pin DIP (300 Mil) See Mech. Drawing Sect. 16, Pg 1



DS1290 16-Pin Encapsulated Package (450 Mil) See Mech. Drawing – Sect. 16, Pg 8

DESCRIPTION

The DS129x Eliminator replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

PIN DESCRIPTION

$\overline{T}$	Transfer
DI	Data Input
O_A–O_Q	Switch Outputs
CLOCK	Clock Input
$\overline{CLEAR}$	All Outputs Set Low
V_{CC}	+5 Volts
GND	Ground
GND2	Missing on DS1292. Must be grounded on DS1293.
GND3	Missing on DS1292. Must be grounded on DS1293.

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OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see "Block Diagram" in Figure 1). The DS1290/DS1291 Eliminator is an 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input ($\overline{T}$) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state that was set prior to $\overline{T}$ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

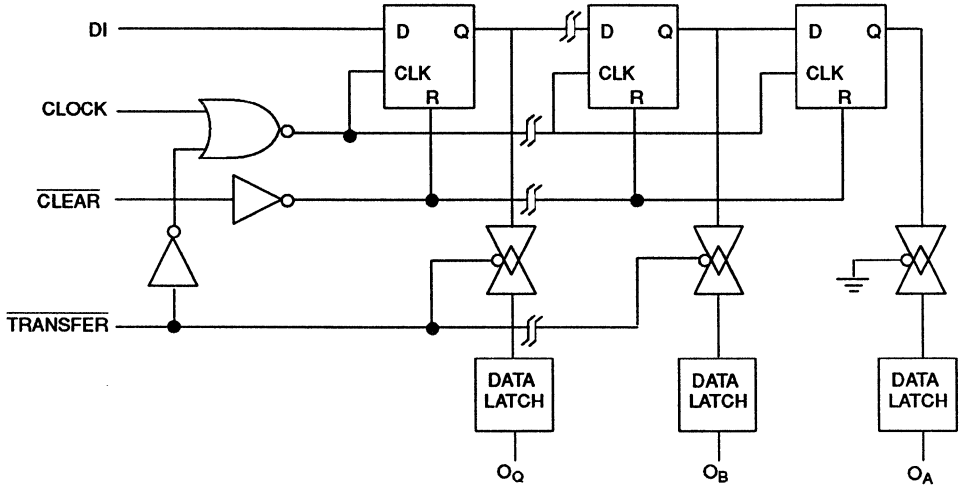
DATA RETENTION MODE

The DS129x Eliminator provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of V_{CC} if set to logic 1 and will remain at ground level if set to Logic 0.

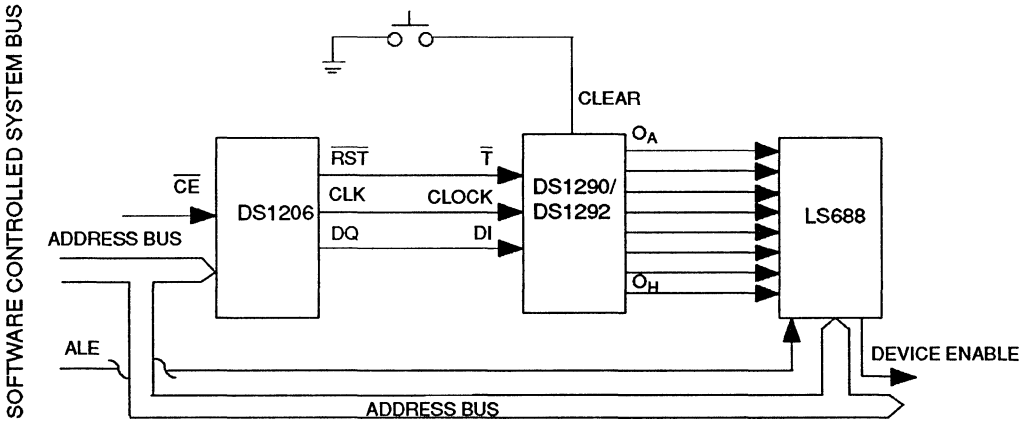
TYPICAL APPLICATION – ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

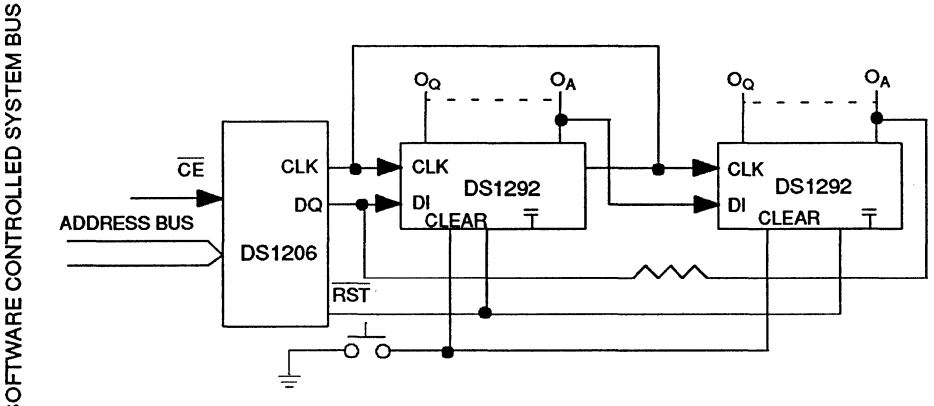
BLOCK DIAGRAM - DS129x Figure 1



PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Logic 1 Output @ 2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

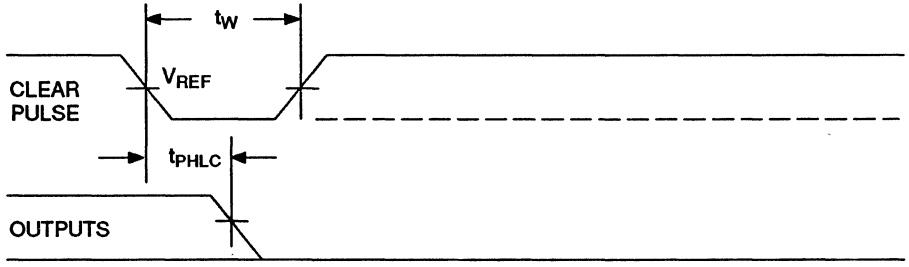
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Setup Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3

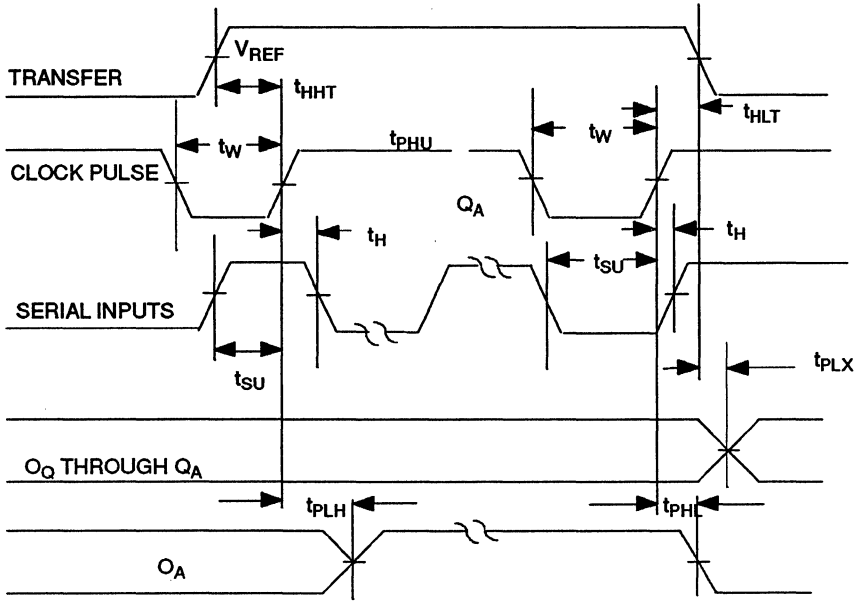
AC ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power-Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

TIMING DIAGRAM - CLEAR CONTROL (3)



TIMING DIAGRAM - TRANSFER DATA (3)



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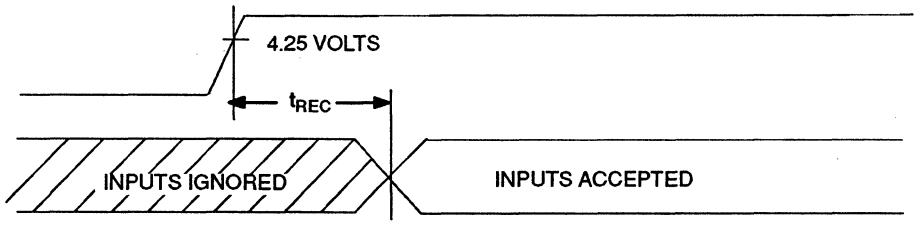
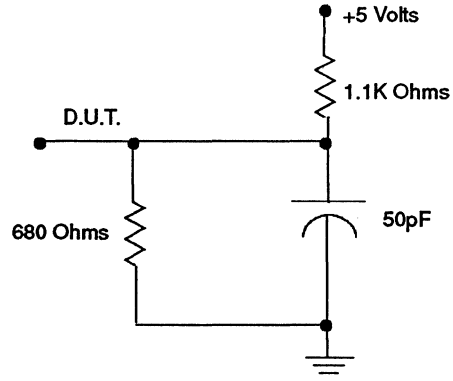
TIMING DIAGRAM - POWER-UP (3)



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. V_{REF} = 1.5 volts.
4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

OUTPUT LOAD Figure 4



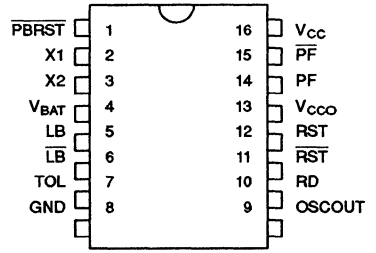
DALLAS SEMICONDUCTOR

DS1632
PC Power Fail and Reset Controller

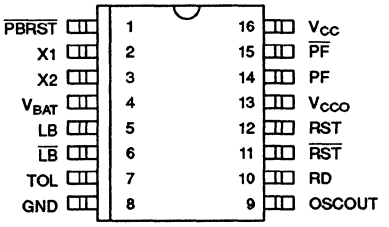
FEATURES

- Power fail detector for personal computers and workstations
- Connects directly to popular personal computer chip sets
- On chip 32.768 KHz oscillator for real time clock
- Provides battery backup power to clock chip
- Pushbutton reset input
- Accurate 5% or 10% +5 volt power supply monitoring
- Complementary outputs for reset, power fail, and low battery
- Provides for reset pulse width of either 100 ms or 200 ms
- Eliminates the need for discrete components
- Low–power CMOS circuitry
- 16-pin DIP or SOIC surface mount package
- 0°C to 70°C operation

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawing – Sect. 16, Pg 1



16-Pin SOIC (300 Mil)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

PBRST	-	Pushbutton Reset Input
X1, X2	-	Crystal Inputs
V_{BAT}	-	Battery Input
LB, $\overline{LB}$	-	Low Battery Outputs
RST, $\overline{RST}$	-	Reset Outputs
RD	-	Reset Duration
TOL	-	Selects 5% Or 10% Detection
GND	-	Ground
OSCOUT	-	Oscillator Out
V_{CCO}	-	Switched Power Out
PF, $\overline{PF}$	-	Power Fail Outputs
V_{CC}	-	+5 Volt Power In

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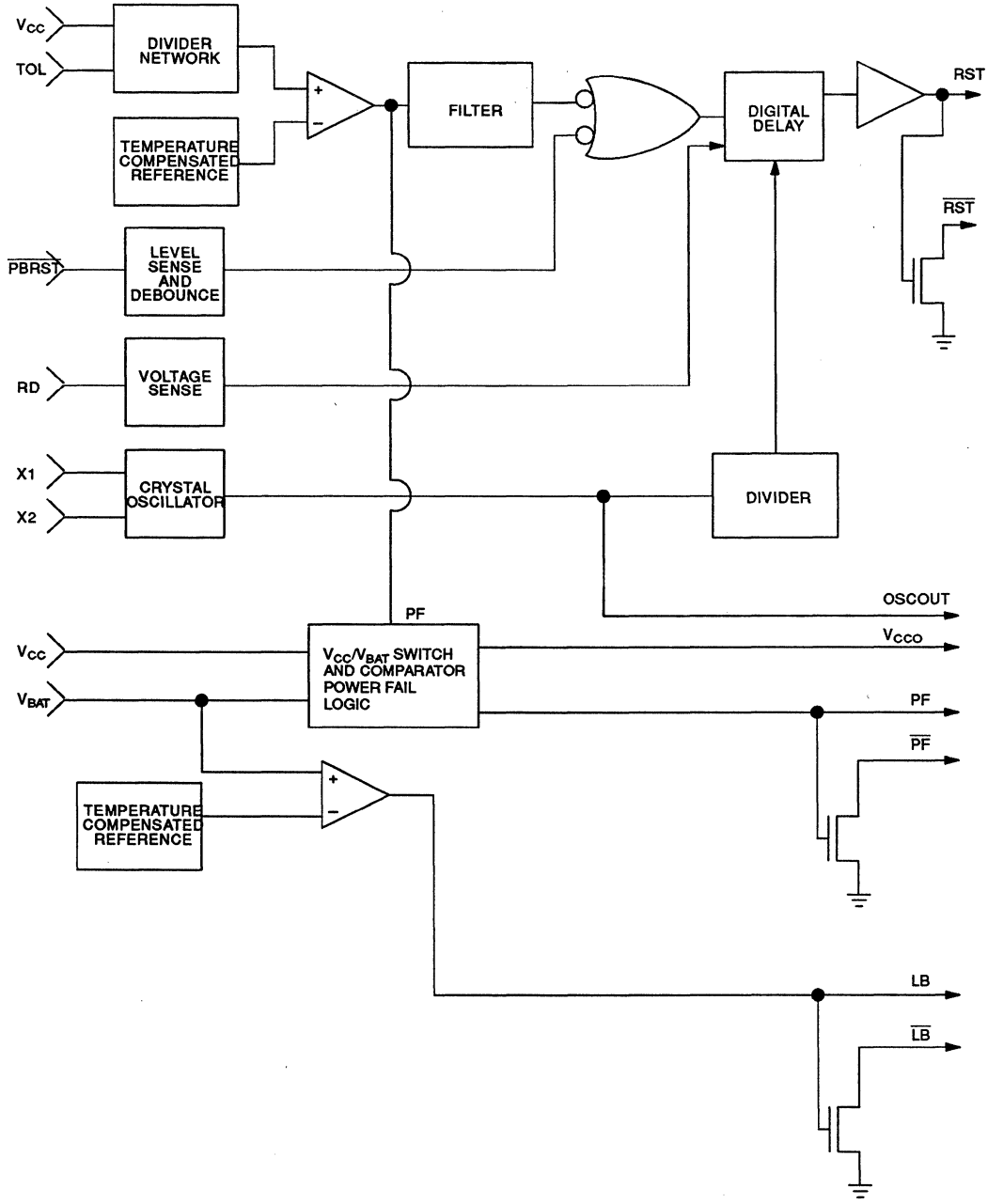
DESCRIPTION

The DS1632 PC Power Fail and Reset Controller is designed to do various functions involving battery backup and other functions typically accomplished with discrete components. The DS1632 provides a 32.768 KHz battery backed up crystal oscillator and switched V_{CC}/V_{BAT} power via V_{CCO} for the real–time clock function located in accompanying chip sets. In addition, the DS1632 provides for reset on both power up and via pushbutton input, power fail status signals for the processor, and low battery warning signals. The DS1632 is capable of detecting power failure at both the 5% and 10% power supply tolerances, and the reset pulse width can be set for either 100 ms or 200 ms. The device is designed to connect directly to popular laptop and notebook chip sets which eliminates the need for discrete components and reduces cost. (See Figure 1.)

BLOCK DIAGRAM Figure 1



OPERATION – CRYSTAL OSCILLATOR SECTION

The DS1632 crystal oscillator is designed to be hooked directly to a 32.768 KHz crystal. By using the Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, the oscillator will be accurate enough to run a real time clock to within ±2 minutes per month. If another crystal is to be selected, it should have a specified load capacitance (C_L) of 6 pF. The crystal oscillator will run as long as either V_{CC} or V_{BAT} is present, providing that V_{BAT} is greater than 2.3V. The oscillator output provides a rail to rail swing with regards to V_{CC} or V_{BAT}, whichever is greater. The crystal oscillator is also used internally as a time base.

OPERATION – POWER FAIL, BATTERY BACKUP

The DS1632 provides a switch to direct power from the battery (V_{BAT}) or the incoming supply (V_{CC}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The V_{CC} input is constantly monitored by a precision comparator for an out of tolerance condition. When such a condition occurs, the power fail signals are driven to their active state immediately. The reset signals are also driven active, but this action is delayed by a time determined by the level of the input on the reset duration pin (RD). If RD is tied to ground then reset signals will become active after 10 ms. If RD is tied to V_{CC}, then reset signals will become active after 20 ms. Once active, both the reset signals and the power fail signals will remain active as long as a (V_{CC}) out of tolerance condition persists. If an out of tolerance condition is not long enough to activate the reset signals, then only the power fail signals would be affected. When power returns to within nominal limits the power fail signals will return immediately to the inactive state. However, the reset signals remain in the active state for a time which is dependent on the state of the RD pin. If RD is tied to ground, the reset signals will remain active for 100 ms. If RD is tied to V_{CC}, then the reset signals will remain active for 200 ms after power is within nominal limits. The delay action on the reset signals allows time for the power supply and microprocessor clock oscillators to stabilize. The tolerance pin (TOL) selects the point at which power fail detection occurs. With the tolerance pin grounded, power fail detection occurs in the range of 4.75V to 4.5V. If the tolerance pin is connected to V_{CC}, then power fail detection occurs in the range of 4.5V to 4.25V. During most power supply conditions the V_{CC} input will supply power to all functions within the chip and also to the V_{CCO} pin. The battery pin (V_{BAT}) only supplies power when V_{CC} is less than V_{BAT}. When V_{CC} is below the level of V_{BAT} only the V_{CCO} and the OSC OUT pin remain powered by V_{BAT}. All other outputs will be driven to ground when in a logic low state and will be driven to V_{CC} when in a logic high state. This is done to preserve battery capacity by avoiding battery drain resulting from loads on these outputs. The output ground level will be maintained for all levels of V_{CC}, even V_{CC} = GND. However, the output V_{CC} level will be maintained only for V_{CC} > 2.0V. Internal battery power consumption is less than 2 µA while V_{BAT} is supplying power. The external load on OSC OUT and V_{CCO} must be added to internal consumption to determine the total load on the battery.

OPERATION – PUSHBUTTON RESET

The DS1632 provides an input pin for direct connection to a pushbutton. The pushbutton reset input $\overline{PBRST}$ requires an active low level input. While TTL levels are sufficient to properly activate this input, it has been primarily designed for contact closure. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of 100 ms or 200 ms minimum are generated. If RD is tied to ground, then a reset pulse of 100 ms is generated. If RD is tied to V_{CC} then a reset pulse of 200 ms is generated. The delay time is started as the pushbutton reset input is released from low level.

OPERATION – LOW BATTERY WARNING

The DS1632 provides outputs which warn of a low battery condition. Whenever V_{CC} is within nominal limits, the V_{BAT} input is continuously monitored. If the V_{BAT} input is below 2.5V, the low battery outputs are driven to their active states, and will remain in the active state as long as V_{CC} is within nominal limits or until the battery input is restored to an in limit status. On power up, if the V_{BAT} input is below 2.5V, the low battery outputs are not guaranteed active until power fail is deactivated, but guaranteed active prior to reset inactive. When V_{CC} is below the V_{CC} fail trip point both LB and $\overline{LB}$ will be driven to ground.

For application information, please reference Application Note #64, published separately.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1, 3
$\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1, 3
Battery Supply Voltage	V_{BAT}	2.3	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 2.4V	I_{OH}	1			mA	5, 7
Output Current @ 0.4V	I_{OL}	4			mA	7
Output Voltage @ -500 µA	V_{OH}	V_{CC}-0.5V	V_{CC}-0.1V		V	6
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.50	V	1
Battery Fail Trip Point	V_{BATTP}	2.30	2.45	2.55	V	1
Supply Voltage Output	V_{CCO}	V_{CC}-0.2			V	
Supply Current Output	I_{CCO1}			100	mA	4

DC ELECTRICAL CHARACTERISTICS

(0°C; V_{CC} = < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}			2	µA	
Battery Backup Current	I_{CCO2}			500	µA	4

CAPACITANCE

(t_A = 25°C)

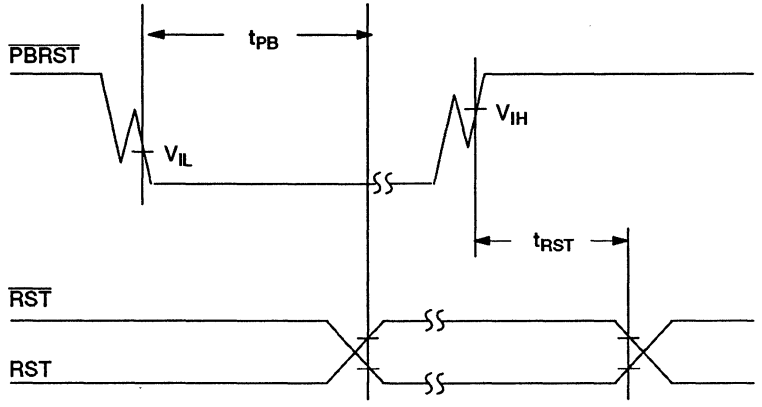
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0° to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	t_{RPD}			ms	
Reset Pulse Width	t_{RST}	95		105	ms	RD=GND
Reset Pulse Width	t_{RST}	190		210	ms	RD=V_{CC}
Reset Active on Power Up	t_{RPU}	95		105	ms	RD=GND
Reset Active on Power Up	t_{RPU}	190		210	ms	RD=V_{CC}
Reset Active on Power Down	t_{RPD}	9		11	ms	RD=GND
Reset Active on Power Down	t_{RPD}	18		22	ms	RD=V_{CC}
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	10			µs	

TIMING DIAGRAM: PUSHBUTTON RESET



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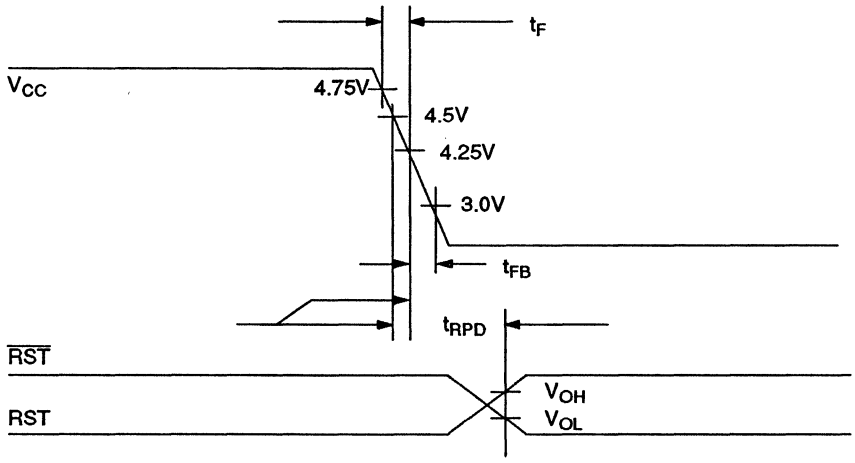
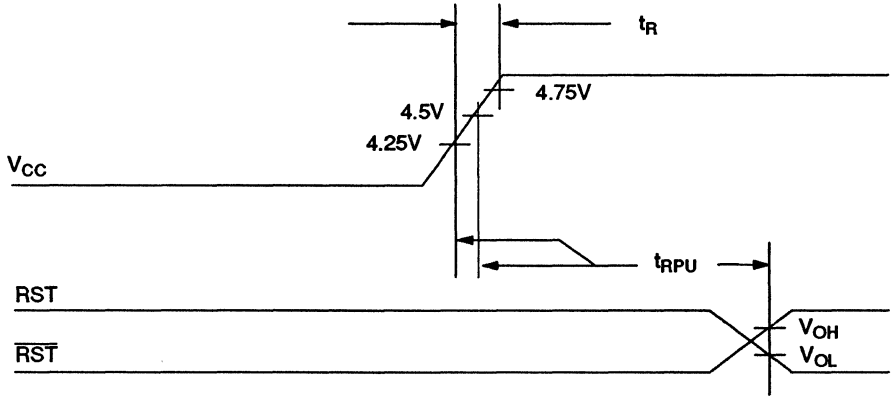
TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. The $\overline{PBRST}$ input has an internal pull up of 10KΩ to V_{CC}.
4. Supply current output is specified with 0.2V drop from V_{BAT} or V_{CC}.
5. $\overline{RST}$, $\overline{PF}$, and $\overline{LB}$ are open drain outputs.
6. RST and PF remain within 0.5 volts of V_{CC} on power down until V_{CC} drops below 2.0V.
7. Sink and source currents apply to all outputs except OSC OUT which has a drive capability of sourcing 500 µA at $V_{OH} = V_{CCO} - 0.5V$ and sinking 1 mA at $V_{OL} = 0.5$ V.

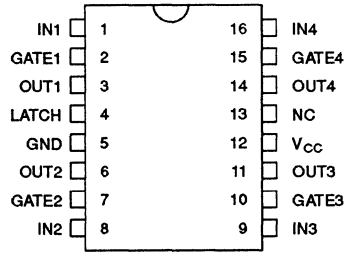
DALLAS SEMICONDUCTOR

DS1640/DS1640C
Personal Computer Power FET

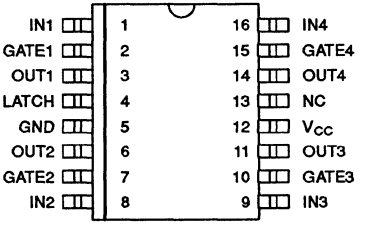
FEATURES

- Contains four P channel power FET switches that can each supply over 300 mA @ 0.2 volts drop
- Controlled directly from CMOS or TTL level signals
- Fast switching time of less than 10 µs at rated supply current
- 16-pin DIP or 16-pin SOIC surface mount package
- Positive logic signal turns each FET on and ground or low level signal turns each FET off
- Off condition allows less than 50 nA of current flow
- Low control gate capacitance of less than 5 pF
- FET gates can either follow inputs or be latched
- Designed for use with power supplies ranging from +3 to +5 volts

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawing – Sect. 16, Pg. 1



16-Pin SOIC (300 Mil)
See Mech. Drawing – Sect. 16, Pg. 6

10

PIN DESCRIPTION

V_{CC}	-	+3 to+5 Volt Input
GND	-	Ground
IN1-IN4	-	FET Sources
OUT1-OUT4	-	FET Drains
GATE1-GATE4	-	FET Control Gates
NC	-	No Connection
LATCH	-	Gate Inputs Latch Control

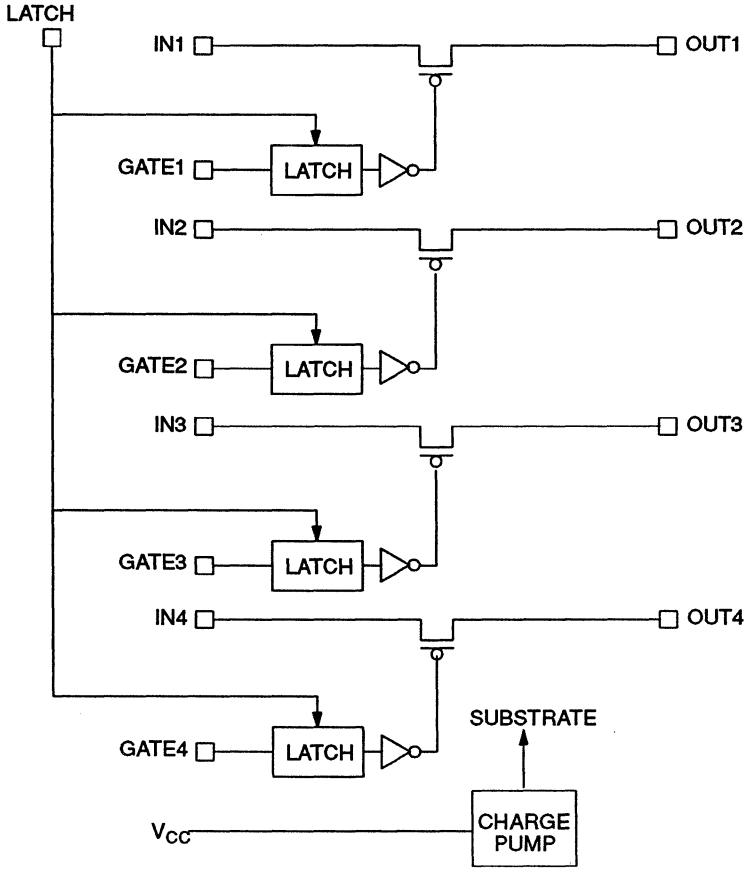
DESCRIPTION

The DS1640 contains four P channel power MOS FET's designed as switches to conserve power in personal computer systems. When connected to power management control units, power consuming devices like disk drives or display panel backlights can be routinely shut down to conserve battery or main power supply energy. The P channel power MOS FET's are individually controlled and are capable of handling 300 mA each continuously with less than 0.2 volts drop from input to output. The device requires a +3 → +5 volt power supply input which is used to power internal logic and to operate a gate bias generator.

OPERATION

With +3 ➛ +5 volts applied between the V_{CC} pin and ground, any one of four inputs can be connected or disconnected from its respective output based on the bias applied to the control gate (see Figure 1). A set of four internal latches is controlled by the latch input. The logic levels passed to the FET gates are controlled by the gate inputs and latch pin status. When the latch pin is logic 0, the gate input levels are inverted and passed directly to the control gates, enabling the switches to be switched both independently and asynchronously. With a transition from logic 0 to logic 1 on the latch pin, the input levels present on the gate inputs are locked by the four internal latches, maintaining the corresponding FET gates at those levels. As long as the latch input is maintained at logic 1, the FET gate levels are maintained. When the latch input is returned to logic 0, the gate inputs again are inverted and passed to the FET control gates without being latched. A TTL or CMOS logic 1 turns a switch completely on and TTL or CMOS logic 0 turns a switch completely off. The four switches can be operated independently or two or more can be connected in parallel for added current carrying capability. The four switches contained within the DS1640 are not designed to be operated in a linear manner. When V_{CC} is not applied to the DS1640 or if V_{CC} is not within nominal limits, the output levels and current carrying capability of the four switches are not guaranteed. When all four gate inputs are off (logic 0) the device enters a low V_{CC} current standby mode because the onboard charge pump is turned off. The gate and latch inputs are CMOS-compatible throughout the entire V_{CC} range and are TTL-compatible when V_{CC} falls between 4.5 and 5.5V.

DS1640 BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0		5.5	V	1, 2
Logic 0 Input 3.0 V ≤ V_{CC} ≤ 4.5 V	V_{IL2}	-0.3		+0.5	V	
Logic 0 Input 4.5 V ≤ V_{CC} ≤ 5.0 V	V_{IL1}	-0.3		+0.8	V	1
Logic 1 Input 3.0 V ≤ V_{CC} ≤ 5.0 V	V_{IH}	2.0		V_{CC}+0.5	V	1, 7
Source Voltage	V_{SOURCE}			V_{CC}+0.5	V	1, 7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC1}		0.3	1	mA	3
Supply Current	I_{CC2}		0.1	1	µA	4
Switch Off Leakage	I_{SL}			100	nA	
Switch On Resistance	R_{ON}		0.3	.67	Ω	
Switch Current @ V_F = 200 mV	I_S			300	mA	5
Input Leakage	I_{IL}	-1		+1	µA	6
Gate Input Capacitance	C_G			5	pF	7

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Switching Time (OFF → ON)	t_{STON}			10	µs	
Switching Time (ON → OFF)	t_{STOFF}			10	µs	
Minimum Time to Engage Latch	t_{LM}			50	ns	

NOTES

1. All voltages are referenced to ground.
2. When V_{CC} is below minimum limits output levels are not guaranteed.
3. I_{CC1} is the supply current with one or more switches on.
4. I_{CC2} is when all switches are off and all inputs are within 0.5V of a supply rail.
5. Each switch is capable of carrying 300 mA maximum at 200 mV forward drop.
6. Input leakage applies to the four gate inputs and the latch input only.
7. Applies to each of four gate inputs and the latch input.

Dallas Semiconductor devices are built to the highest quality standards and manufactured for long term reliability. All DS1640 devices are made using the same quality materials and manufacturing methods. However, consumer versions of the DS1640 are not exposed to environmental stresses that some commercial device manufacturing flows require. Devices that are designated as consumer product have a "C" designator in the product number. For example, the DS1640C is a consumer grade product.

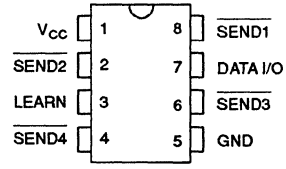
DALLAS SEMICONDUCTOR

DS1652B Key Code Memory

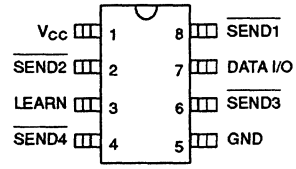
FEATURES

- The key forms the basis of a secure access system
- The DS1652B is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64 bit code prevents unauthorized copying of keys
- Each key capable of generating 4–code conditions.
- Keys are programmed from an external device only under controlled user access/secure conditions
- Low cost, economical
- Key codes may be changed as many times as necessary
- 3V operation, 5V for programming
- –25°C to +85°C operating range
- All stored 64 bit codes in the key are non–volatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification.

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawing – Pg. 1



8-Pin SOIC (200 Mil)
See Mech. Drawing – Pg. 5

PIN DESCRIPTION

V_{CC}	–	+3V to +7V Input
GND	–	Ground
DATA I/O	–	Serial Data Input/Output
$\overline{SEND1}$	–	Send Input 1
$\overline{SEND2}$	–	Send Input 2
$\overline{SEND3}$	–	Send Input 3
$\overline{SEND4}$	–	Send Input 4
LEARN	–	Learn Input

10

DESCRIPTION

The DS1652B key operates as part of a system to limit access of any secure system or area to keyholders. The DS1652B key contain a 64 bit memory which acts as the security code, controlling access. Once set, the code is nonvolatile.

To gain access to a locked system, the key's code must be transmitted to the lock via some user transmission media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a lock system must compare the requesting key's 64 bit code to the lock's systems programmed code. If the key code matches the lock system code, the lock system must generate a match signal, which can be used to allow access to the secure system.

OPERATION DS1652B KEY

The operation of the DS1652B key is shown in Figure 1. The key is programmed with code from an external source with the key in Learn mode.

For the DS1652B key to be programmed, the LEARN pin must be driven active high, with V_{CC} on the DS1652B at 5V. The DS1652B key's data input/output pin must be physically connected to the external programming device for the DS1652B key to successfully accept a code. Once connected and in the Learn mode, the DS1652B key is ready to accept its 64 bit code. The DS1652B key will recognize the 1600 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the external programming device, become latched into the nonvolatile 64 bit code memory of the DS1652B key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652B to its operation mode. The DS1652B key will transmit a reset signal and its code memory out of its data input/output pin a maximum of ten times as long as the $\overline{SENDX}$ input is asserted. The DS1652B key will transmit a version of the code that is specifically tailored to $\overline{SENDX}$ input being triggered (see diagram, Page 10–141).

SERIAL PULSE PROTOCOL

The DS1652B transmits and receives data serially, according to the protocol listed in the timing diagram.

The transmission and reception of data begins with the rising edge of the 1600 µs reset signal. The DS1652B then begins looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1652B will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the 64 bit code memory. This iterative process continues through all 64 bits until they are written. For the DS1652B, after 64 bits are written, the key may be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1652B key provides a security code matching system which can be used as the code control logic of any security system.

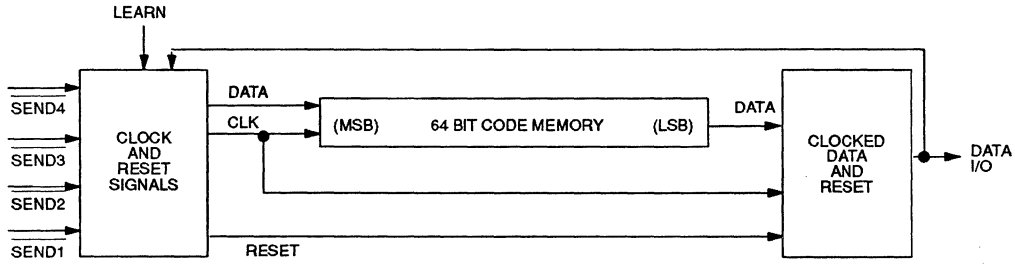
The DS1652B key is programmed from an external programming device and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of a DS1652B key based system is limiting the manner by which a key may be programmed with the code to open the lock. The only way in which a DS1652B key will accept code is to connect its data input/output pin directly to the external programming device. Therefore the only method of transferal is by physically connecting the device holding the DS1652B key with the device holding the programmer. A quick and efficient method of implementing this interface is illustrated on Page 10–137

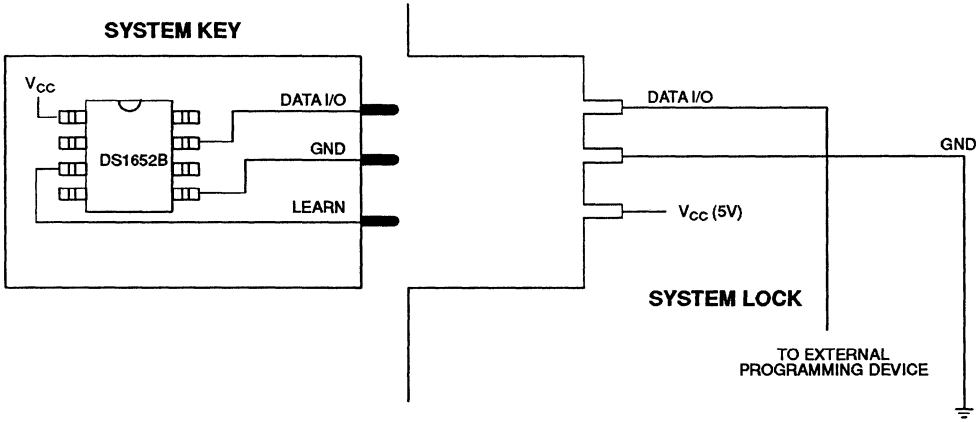
By designing the system key with three external leads, one tied to V_{CC}(5V), one tied to ground, and one tied to the input pin, the system key may accept a new code from a system lock only through these three connections.

As many keys as needed may be programmed. As required for security purposes, or in case of the loss of a key a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.

DS1652B KEY BLOCK DIAGRAM Figure 1



INTERIOR OF LOCK SECURED AREA

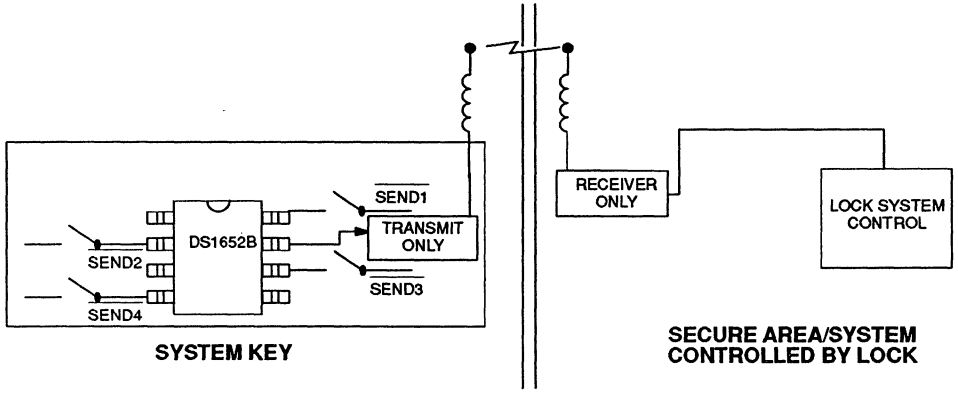


TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652B key to the system lock.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1652B's serial pulse protocol may be used to link the key to the users lock system.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25° to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.5	5.0	7.0	V	1
Logic 1 Input	V_{IH}	2.0	–	V_{CC}+0.3	V	1, 6, 7, 4
Logic 0 Input	V_{IL}	–0.3	–	+0.8	V	1, 6, 7

DC ELECTRICAL CHARACTERISTICS

(-25° to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_L	5	6	7	V	1, 5, 6
Input Leakage (Data Input)	I_{L1}	–1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1652B KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	1200	1600	2000	µs	
Logic 1 Active	t_1	600	800	1000	µs	
Logic 0 Active	t_0	300	400	500	µs	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	300		2000	µs	
Active Signal Pulse Width $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$	t_S	10		20	ms	
Delay Between LEARN Pin Transition and Operation Mode Change	t_T			10	ms	
Delay Between Minimum $\overline{SENDX}$ Assertion and Data Out Transmitted	t_{SD}			100	µs	
Number of Words Transmitted for 1 $\overline{SENDX}$ Input Recognized		10				

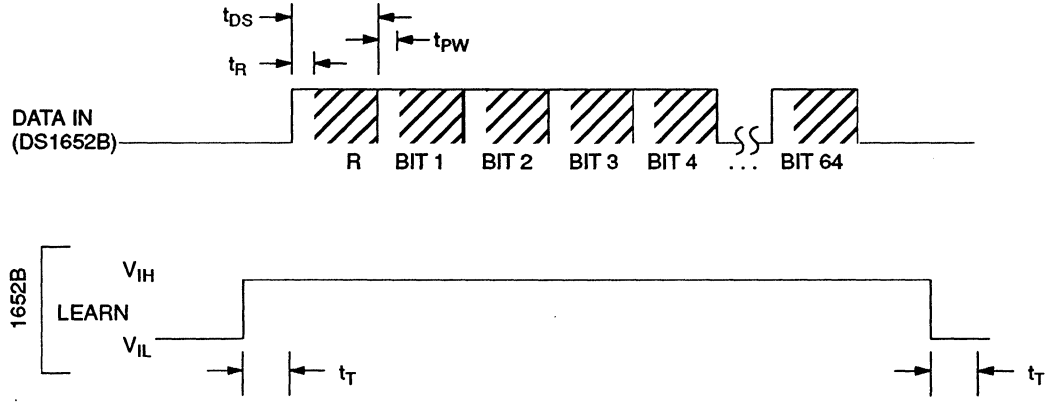
CAPACITANCE

(t_A = 25°C)

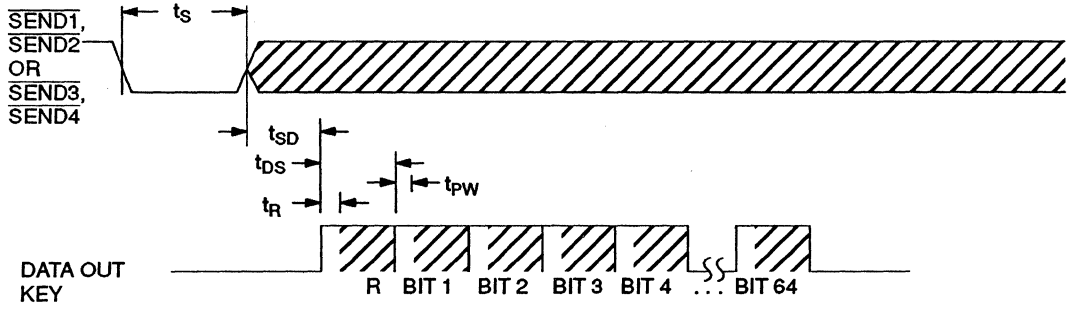
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

10

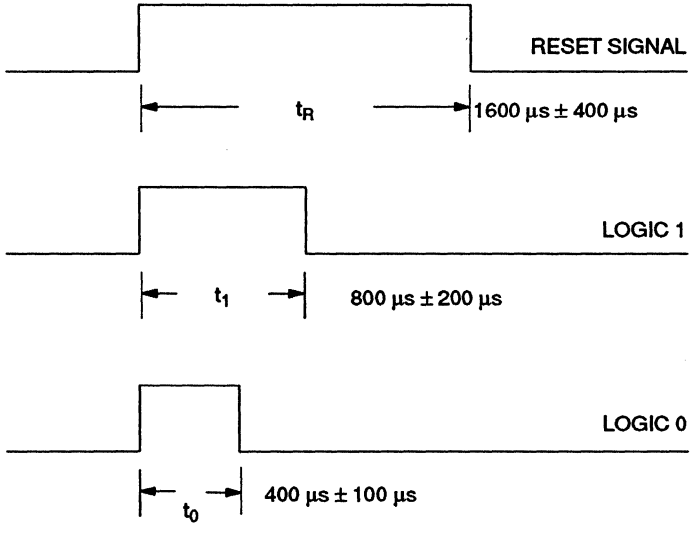
LEARN MODE DS1652B KEY



OPERATION DS1652B KEY



LOGIC TIMING DIAGRAMS



INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$ (DATA)*	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$ ($\overline{DATA}$)	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$ ($\overline{ODD}$)	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$ ($\overline{EVEN}$)	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

*The bit pattern transmitted by the $\overline{SEND1}$ trigger it the unaltered contents of the DS1652B code memory. $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ transmit modified versions of this code a listed above.

NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652B data input only.
4. Absolute maximum rating is 7.0V on any pin.
5. Input voltage on the V_{CC} pin is required to be in the Learn mode, for the DS1652B to properly accept new code data.
6. The DS1652B LEARN pin is internally pulled down with approximately a 10KΩ resistor.
7. The DS1652B $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ inputs are internally pulled up with approximately 10KΩ resistors.

PRELIMINARY

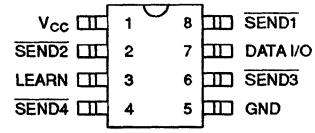
DALLAS SEMICONDUCTOR

DS1651 3-Code Lock, DS1652 Key Match Memory System

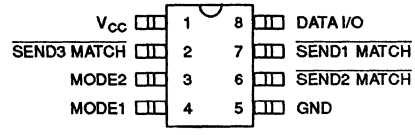
FEATURES

- The two chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64 bit code or internally generated random 64 bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 3-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low cost, economical
- Lock codes may be changed as many times as necessary
- 3V operation, 5V for programming
- -25°C to +75°C operating range
- All stored 64 bit codes in the lock and key are non-volatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and
DS1652S 8-Pin SOIC (200 Mil)
See Mech. Drawings – Sect. 16, Pgs. 1 & 5



DS1651 8-Pin DIP (300 Mil) and
DS1651S 8-Pin SOIC (200 Mil)
See Mech. Drawings – Sect. 16, Pgs. 1 & 5

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1}}$	-	Send Input 1
$\overline{\text{SEND2}}$	-	Send Input 2
$\overline{\text{SEBD3}}$	-	Send Input 3
$\overline{\text{SEND4}}$	-	Send Input 4
LEARN	-	Learn Input

DS1651 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +7V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1 MATCH}}$	-	Code Match Signal for SEND1
$\overline{\text{SEND2 MATCH}}$	-	Code Match Signal for SEND2
$\overline{\text{SEND3 MATCH}}$	-	Code Match Signal for SEND3

DESCRIPTION

The DS1651 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1651 Lock and DS1652 Key contain a 64 bit memory which acts as the security code, controlling access. The code memory within the DS1651 Lock may be user programmed with a known 64 bit code, or the DS1651 can generate a 64 bit code from a random number generator within the DS1651. Once set, the code is nonvolatile, and can then be transferred to a DS1652 Key(s) under secure conditions.

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a DS1651 Lock will compare the requesting key's 64 bit code to the lock's programmed 64 bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1651 LOCK

The main functional components of both the DS1651 and DS1652 are shown in Figures 1 and 2. The diagram shows that the internal functions of the lock and key are similar. From Figure 1, the primary components of the lock are its 64 bit wide registers. The 64 bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64 bit data memory records the 64 bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1651 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user provided 64 bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated random 64 bits.

The Learn modes and duplicate mode may only be entered from operation mode. The DS1651 samples the level of MODE1 and MODE2 10 ms after a low to high transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating.

In the Learn modes, the DS1651 Lock's code memory may be either programmed directly by the user, or programmed using a random set of 1's and 0's created by the DS1651's random number generator. A user must have physical access to the DS1651 to place it in Learn mode. To place the DS1651 Lock in Learn mode, the DS1651's V_{CC} input must be at 5V minimum with, mode1 or both mode1 and mode2 pins driven high, telling the DS1651 to enable the contents of its code memory to be rewritten. If mode1 is high, then the DS1651 enables its code memory to be rewritten using a user defined 64 bit code, which it expects to see on its data I/O pin. At the end of sending the 64 bit code to the DS1651, the mode1 pin must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes, DS1651 Lock".) If mode2 and mode1 are high, then the DS1651 Lock performs an internal operation in which it uses its internal random number generator to create a 64 bit pattern of 1's and 0's and load it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1651 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1651 to operation mode, before entering any other mode.

The DS1651 will not reprogram its 64 bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its mode2 and mode1 pins.

For the DS1651 Lock to transfer its code memory into a DS1652 Key the DS1651 Lock must be in duplication mode. To enter the duplication mode, the mode2 pin must be driven high. The transition from 0 to 1 on the mode2 pin, and its maintenance at 1 causes the DS1651 Lock to transmit a reset signal followed by its 64 bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64 bit code copy. The data input/output pin of the DS1651 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1651 and DS1652.

The DS1651 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 us is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written in the data memory for compari-

son to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1651 drives the appropriate $\overline{\text{SENDX MATCH}}$ signal. If the code does not match, the DS1651 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1651 (Figure 2). The key is programmed with code generated by the DS1651 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1651 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1651 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64–bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64–bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to $\overline{\text{SENDX}}$ input being triggered (see diagram, Page 10–151).

SERIAL PULSE PROTOCOL

The DS1651 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1651 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical 0 is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1651 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1651 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key may be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1651 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1651 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64–bit codes, that can only be changed by having physical access to the lock. If known codes are not required, the DS1651 can generate its own 64–bit code randomly. If the random number generator of the DS1651 Lock is used, not even the person programming the lock knows the 64 bit code.

The DS1652 Key is programmed from the DS1651 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of the DS1651 Lock is limiting the manner by which a lock may program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1651 Lock. Therefore the only method of transferal is by physically connecting the device holding the DS1652 Key with the device holding the DS1651 Lock. A quick and efficient method of implementing this interface is illustrated on page 4.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the Data I/O pin, the system key may accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1651 Lock

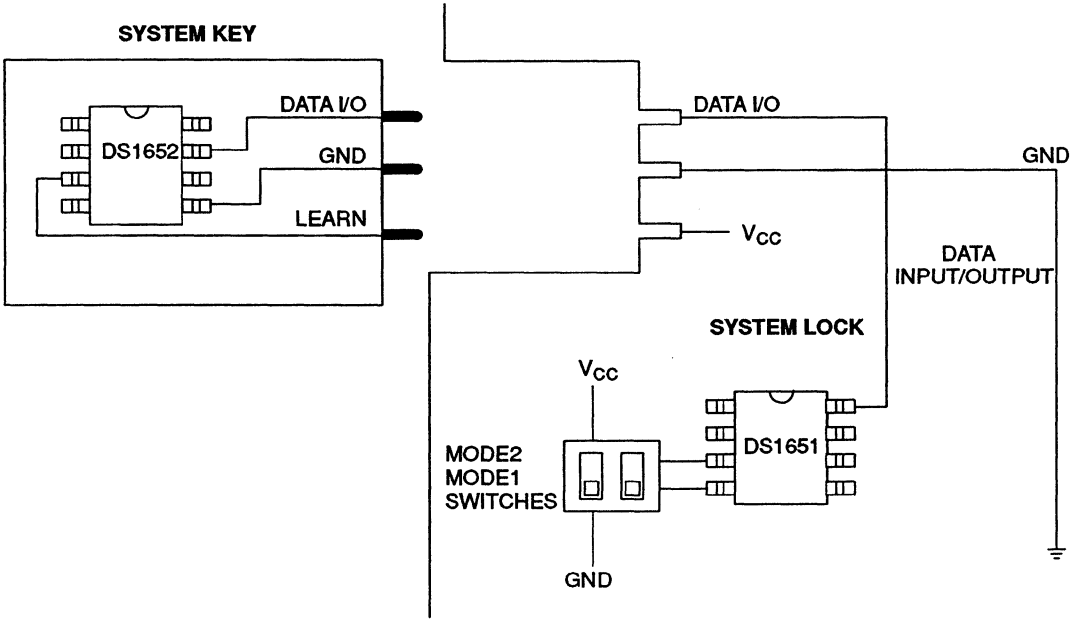
could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who may program keys
2. limits who can generate codes for the lock
3. limits who may, by generating a new code, invalidate the existing programmed keys.

As many keys as needed may be programmed. As required for security purposes or in case of the loss of a key, a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA

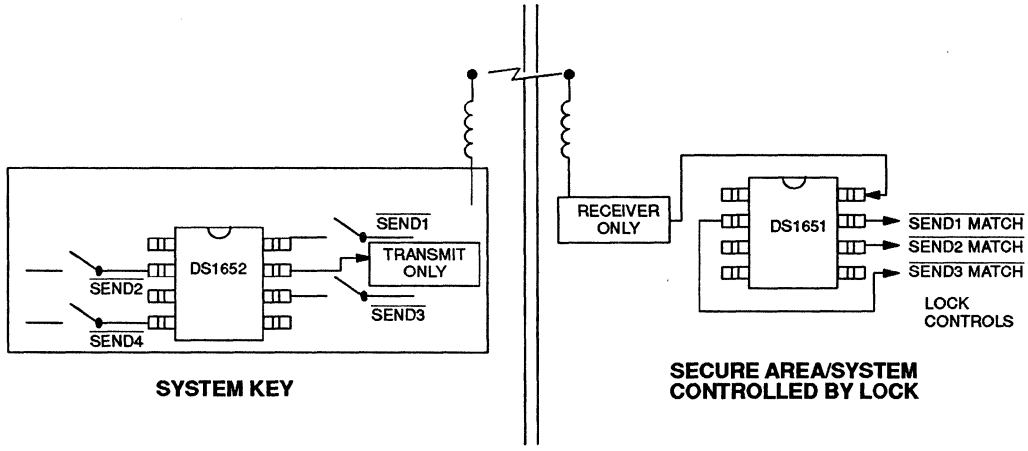


TYPICAL APPLICATION

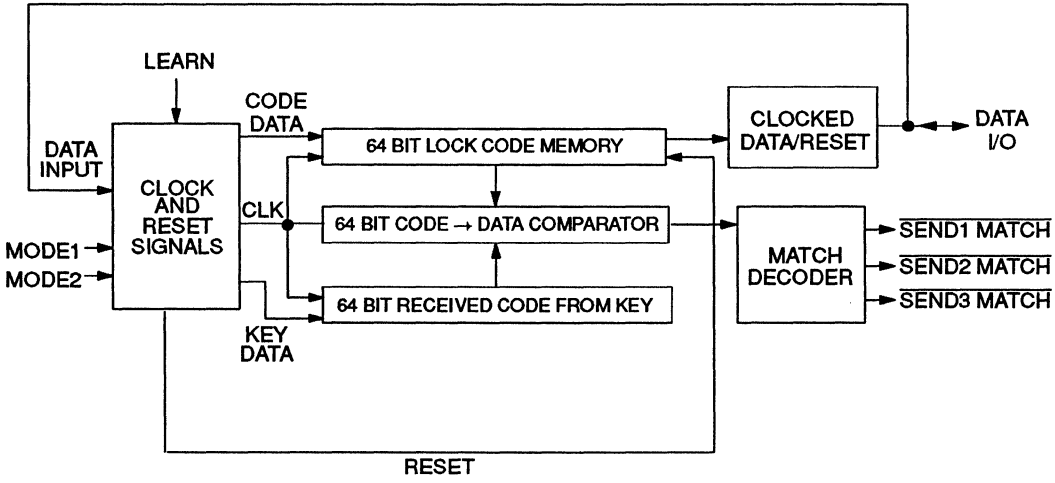
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1651's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1651 and DS1652's serial pulse protocol may be used to link the key to a lock.

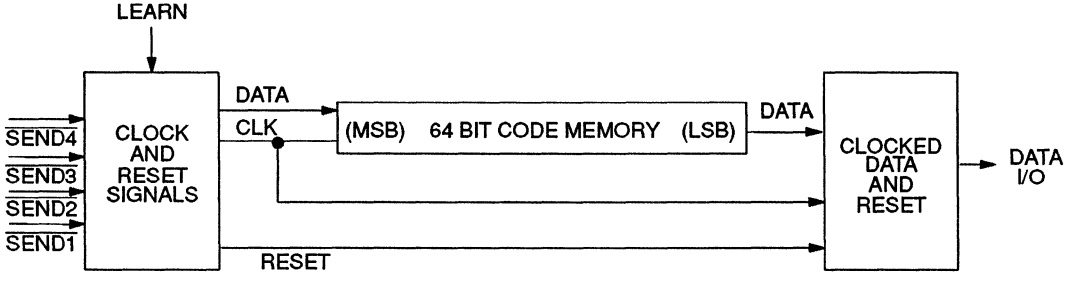
TYPICAL APPLICATION



DS1651 LOCK BLOCK DIAGRAM Figure 1



DS1652 KEY BLOCK DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V-0.5V to +7.0V
Operating Temperature	–25°C to +75°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 15 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C + 77°C) DS1651 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.5	5.0	7.0	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 6, 7, 8
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 6, 7, 8

DC ELECTRICAL CHARACTERISTICS

(-25°C to 75°C) DS1651

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
Supply Current, V_{CC} Pin, Learn Mode	I_{LRN}		2	3	mA	
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}			1	mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

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DC ELECTRICAL CHARACTERISTICS

(-10°C to 70°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}	50	75	100	nA	2
V_{CC} Voltage, Learn Mode	V_L	5	6	7	V	1, 5, 6
Supply Current, Learn Mode	I_{LRN}		2	3	mA	
Input Leakage (Data Input)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1651 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

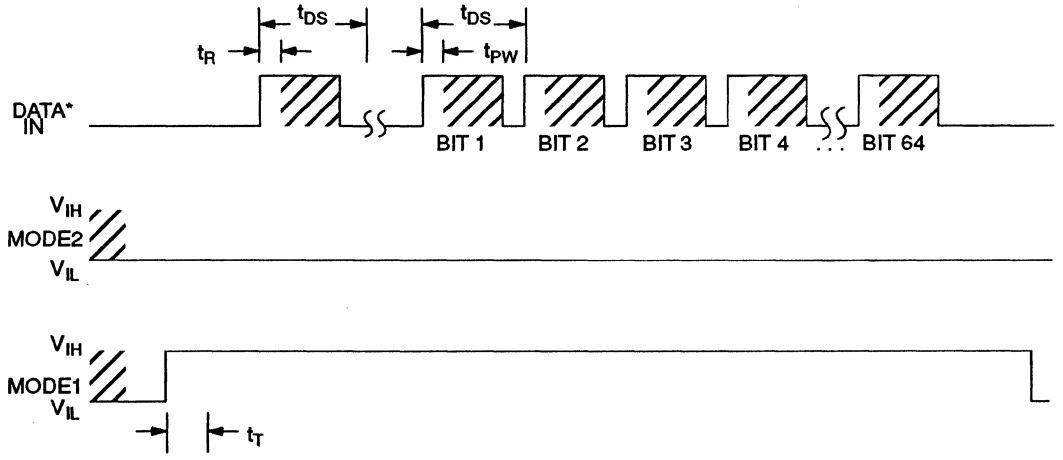
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	540	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
$\overline{\text{SEND1 MATCH}}$, $\overline{\text{SEND2 MATCH}}$, and $\overline{\text{SEND2 MATCH}}$	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{\text{SEND1}}$ and $\overline{\text{SEND2}}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

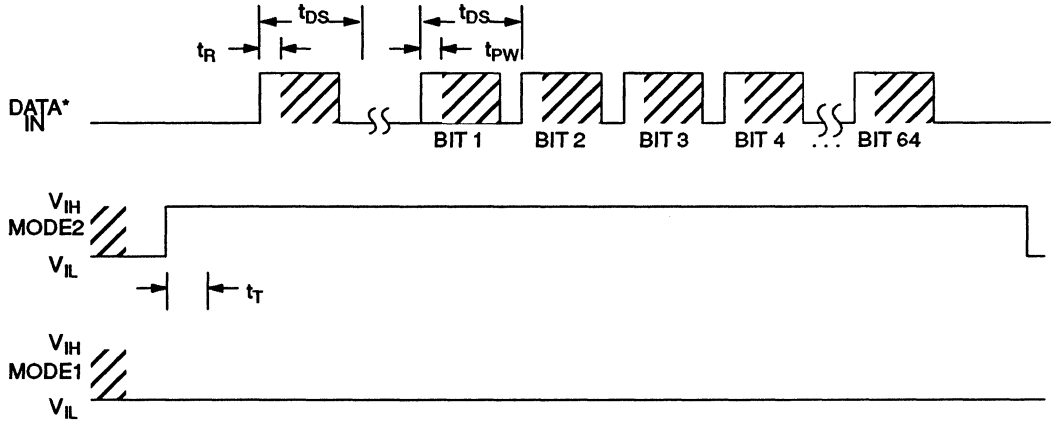
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

LEARN MODE DS1651 LOCK; USER PROGRAMMING



DS1652 LOCK; DUPLICATION MODE



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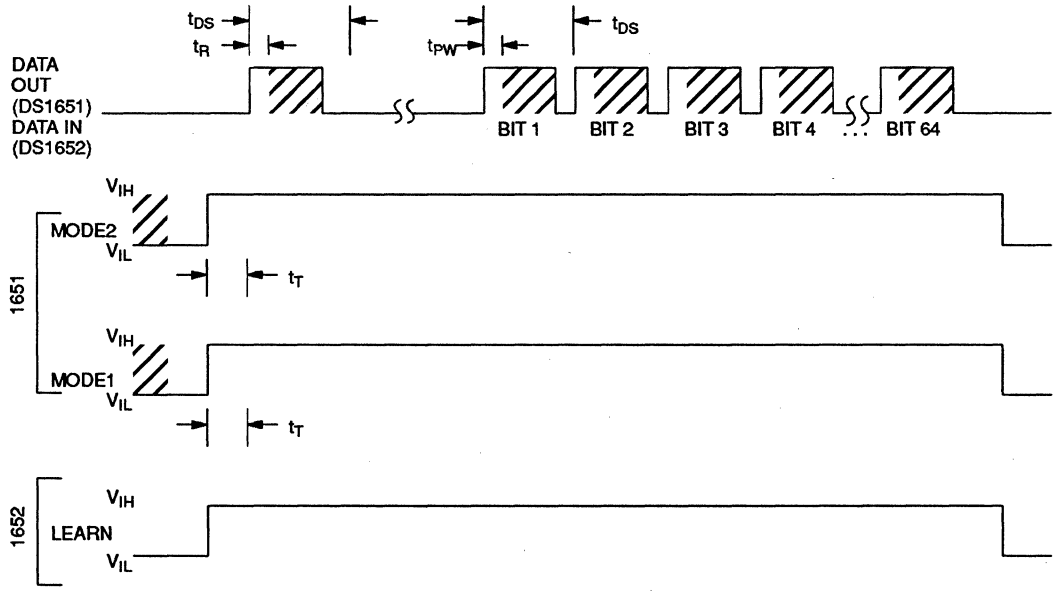
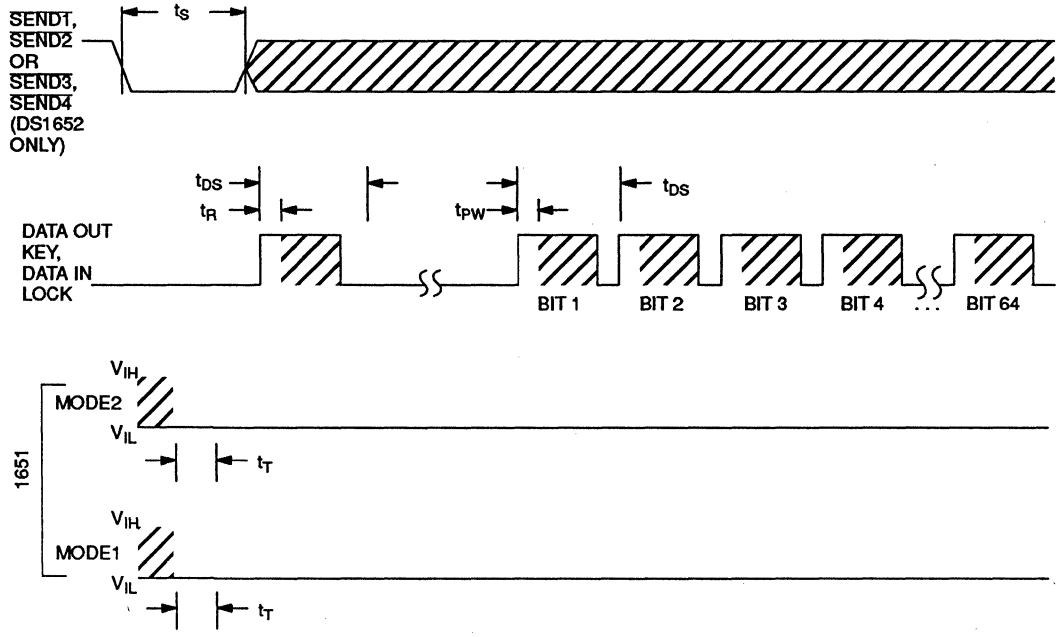
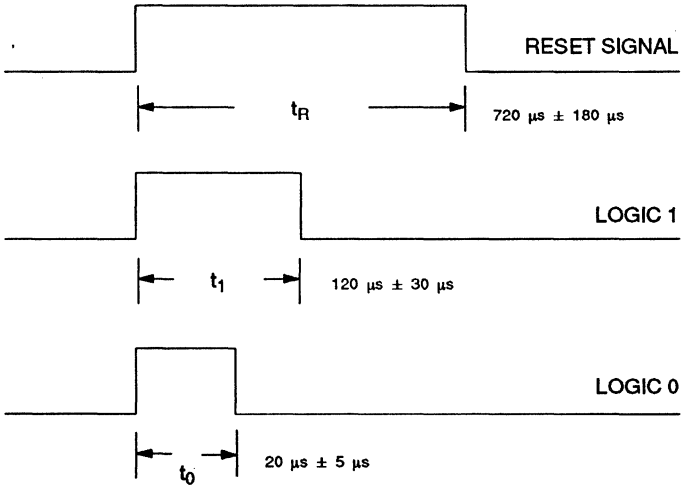
LEARN MODE DS1652 KEY; LEARN MODE DS1651 LOCK, INTERNAL PROGRAMMING



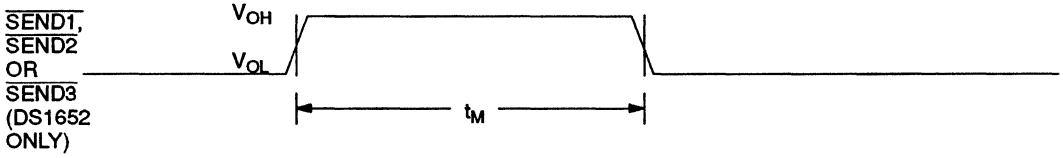
OPERATION DS1651 LOCK AND DS1652 KEY



LOGIC TIMING DIAGRAMS



DS1651 LOCK, MATCH SIGNALS



When the DS1651 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

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INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data input only.
4. Input/output leakage applies to the DS1651 data input/output pin.
5. Input voltage on the LEARN pin is required to be in the Learn mode, for the DS1651 and DS1652 to properly accept new code data.
6. The DS1652 LEARN pin is internally pulled down with a 10KΩ resistor.
7. The DS1651 $\overline{DUPL}$ pin is internally pulled up with a 10KΩ resistor.
8. The DS1652 $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ inputs are internally pulled up with 10KΩ resistors.

PRELIMINARY

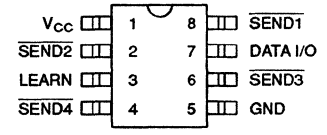
DALLAS SEMICONDUCTOR

DS1653 4-Code Lock, DS1652 Key Match Memory System

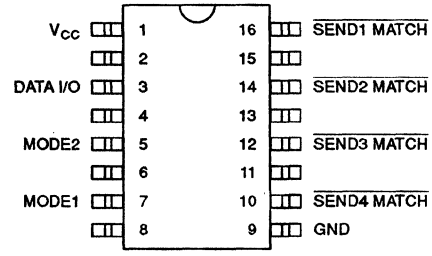
FEATURES

- The two chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user programmable 64–bit code or internally generated random 64–bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 4-code match conditions.
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low cost, economical
- Lock codes may be changed as many times as necessary
- 3V operation, 5V for programming
- -25°C to +85°C operating range
- All stored 64–bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and
DS1652S 8-Pin SOIC (200 Mil)
See Mech. Drawings – Sect. 16, Pgs. 1 & 5



DS1653 16-Pin DIP (300 Mil) and
DS1653S 16-Pin SOIC (300 Mil)
See Mech. Drawings – Sect. 16, Pgs. 1 & 6

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1}}$	-	Send Input 1
$\overline{\text{SEND2}}$	-	Send Input 2
$\overline{\text{SEND3}}$	-	Send Input 3
$\overline{\text{SEND4}}$	-	Send Input 4
LEARN	-	Learn Input
V_{CC}	-	+3V to +7V Input

DS1653 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +7V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1 MATCH}}$	-	Code Match Signal for SEND1
$\overline{\text{SEND2 MATCH}}$	-	Code Match Signal for SEND2
$\overline{\text{SEND3 MATCH}}$	-	Code Match Signal for SEND3
$\overline{\text{SEND4 MATCH}}$	-	Code Match Signal for SEND4

DESCRIPTION

The DS1653 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1653 Lock and DS1652 Key contain a 64 bit memory which acts as the security code, controlling access. The code memory within the DS1653 Lock may be user programmed with a known 64 bit code, or the DS1653 can generate a 64–bit code from a random number generator within the DS1653.

Once set, the code is nonvolatile, and can then be transferred to a DS1652 Key(s) under secure conditions.

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as, RF, optical, IR, ultrasound, or another serial media. Upon receiving a transmission of a 64 bit key code, a DS1653 Lock will compare the requesting key's 64 bit code to the lock's programmed 64 bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1651 LOCK

The main functional components of both the DS1653 and DS1652 are shown in Figures 1 and 2. The diagram shows that the internal functions of the lock and key are similar. From Figure 1, the primary components of the lock are its 64–bit wide registers. The 64 bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64–bit data memory records the 64–bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1653 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user provided 64 bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated random 64 bits.

The Learn modes and duplicate mode may only be entered from operation mode. The DS1653 samples the level of MODE1 and MODE2 10 ms after a low to high transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating

In the Learn modes, the DS1653 Lock's code memory may be either programmed directly by the user, or programmed using a random set of 1's and 0's created by the DS1653's random number generator. A user must have physical access to the DS1653 to place it in Learn mode. To place the DS1653 Lock in Learn mode, the DS1653's V_{CC} input must be at 5V minimum with, mode1 or both mode1 and mode2 pins driven high, telling the DS1653 to enable the contents of its code memory to be rewritten. If mode1 is high, then the DS1653 enables its code memory to be rewritten using a user defined 64–bit code, which it expects to see on its data I/O pin. At the end of sending the 64–bit code to the DS1653, the mode1 pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes, DS1653 Lock".) If mode2 and mode1 are high, then the DS1653 Lock performs an internal operation in which it uses its internal random number generator to create a 64–bit pattern of 1's and 0's and load it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1653 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1653 to operation mode, before entering any other mode.

The DS1653 will not reprogram its 64–bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its mode2 and mode1 pins.

For the DS1653 Lock to transfer its code memory into a DS1652 Key the DS1653 Lock must be in duplication mode. To enter the duplication mode, the mode2 pin must be driven high. The transition from 0 to 1 on the mode2 pin, and its maintenance at 1 causes the DS1653 Lock to transmit a reset signal followed by its 64–bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64 bit code copy. The data input/output pin of the DS1653 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1653 and DS1652.

The DS1653 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written in the data memory for comparison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1653 drives the appropriate $\overline{\text{SENDX MATCH}}$ signal. If the code does not match, the DS1653 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1653 (Figure 2). The key is programmed with code generated by the DS1653 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1653 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1653 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64 bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64 bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to $\overline{\text{SENDX}}$ input being triggered (see diagram, page 10).

SERIAL PULSE PROTOCOL

The DS1653 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1653 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1653 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1653 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key may be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1653 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1653 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64 bit codes, that can only be changed by having physical access to the lock. If known codes are not required, the DS1653 can generate its own 64 bit code randomly. If the random number generator of the DS1653 Lock is used, not even the person programming the lock knows the 64 bit code.

The DS1652 Key is programmed from the DS1653 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of the DS1653 Lock is limiting the manner by which a lock may program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1653 Lock. Therefore the only method of transferal is by physically connecting the device holding the DS1652 Key with the device holding the DS1653 Lock. A quick and efficient method of implementing this interface is illustrated on page 4.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the Data I/O pin, the system key may accept a new code

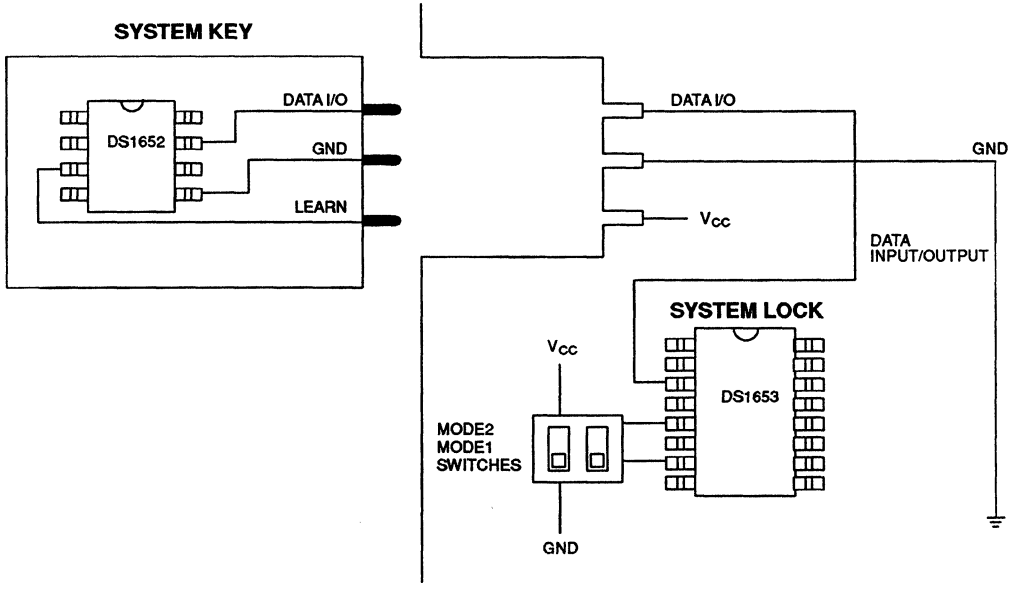
from a system lock only through these three connections. Once placed in a system lock, the DS1653 Lock could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who may program keys
2. limits who can generate codes for the lock
3. limits who may, by generating a new code, invalidate the existing programmed keys.

As many keys as needed may be programmed. As required for security purposes or in case of the loss of a key, a new code may be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys, and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA



TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1653's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1653 and DS1652's serial pulse protocol may be used to link the key to a lock.

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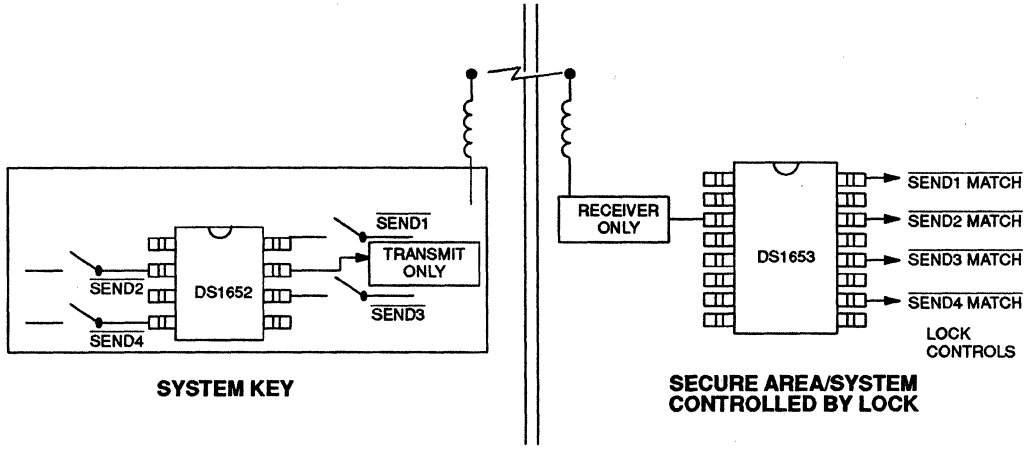
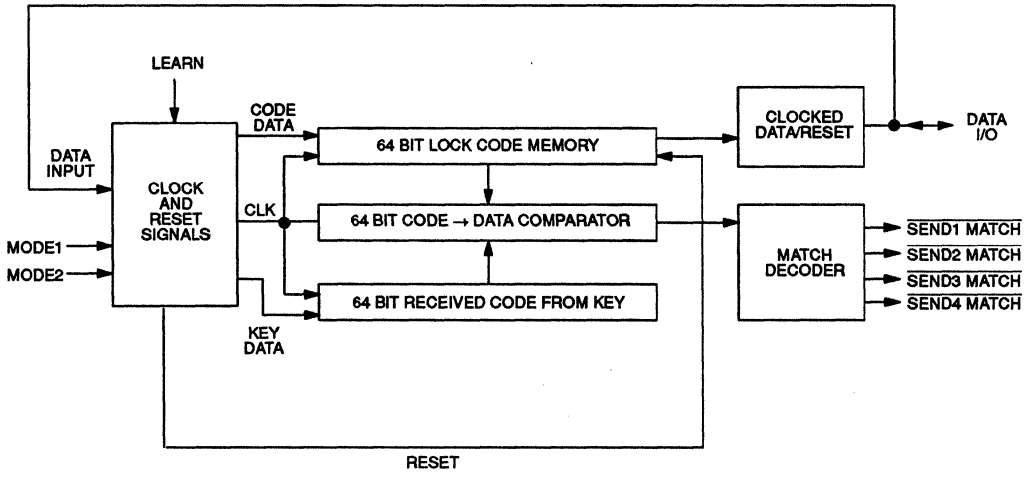
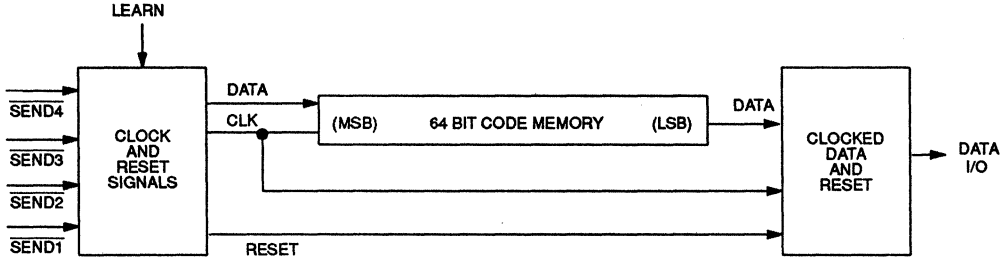
TYPICAL APPLICATION



DS1653 LOCK BLOCK DIAGRAM Figure 1



DS1652 KEY BLOCK DIAGRAM Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V -0.5V to +7.0V
Operating Temperature	-25°C to +85°C
Programming Temperature	-10°C to +85°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 15 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C + 85°C) DS1653 AND DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	5.0	7.0	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 6, 8
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 6, 8

DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1653

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
Supply Current, V_{CC} Pin, Learn Mode	I_{LRN}		2	3	mA	
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}			1	mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

10

DC ELECTRICAL CHARACTERISTICS

(-10°C to 85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_L	5	6	7	V	1, 5, 6, 7
Supply Current, Learn Mode	I_{LRN}		2	3	mA	1, 5, 6, 7
Input Leakage (Data Input)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1,9
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 9
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1653 LOCK AND DS1652 KEY DATA TRANSMISSION PARATEMTERS

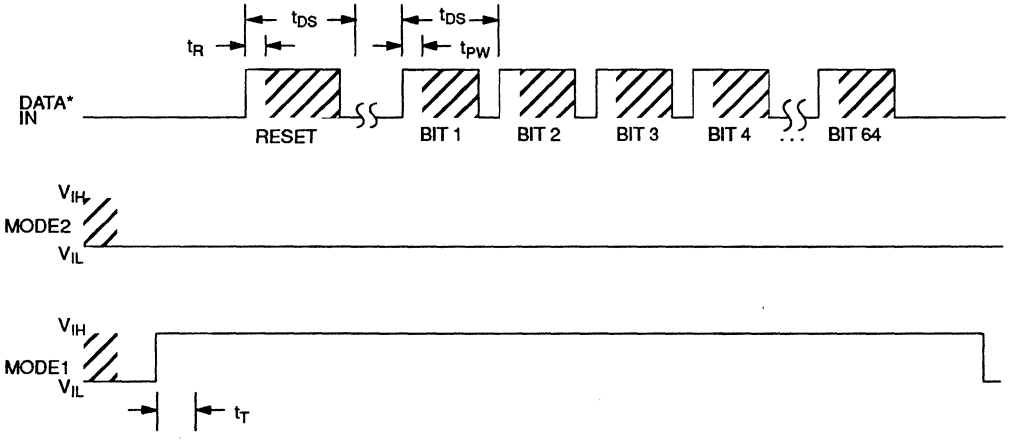
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	340	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
$\overline{\text{SEND1 MATCH}}$, $\overline{\text{SEND2 MATCH}}$, $\overline{\text{SEND3 MATCH}}$, and $\overline{\text{SEND4 MATCH}}$	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{\text{SEND1}}$ and $\overline{\text{SEND2}}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

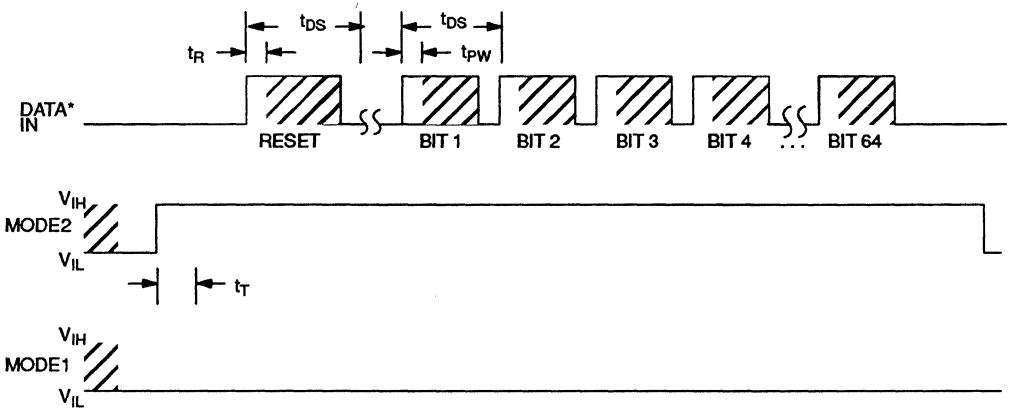
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

LEARN MODE DS1653 LOCK; USER PROGRAMMING



DS1653 LOCK; DUPLICATION MODE



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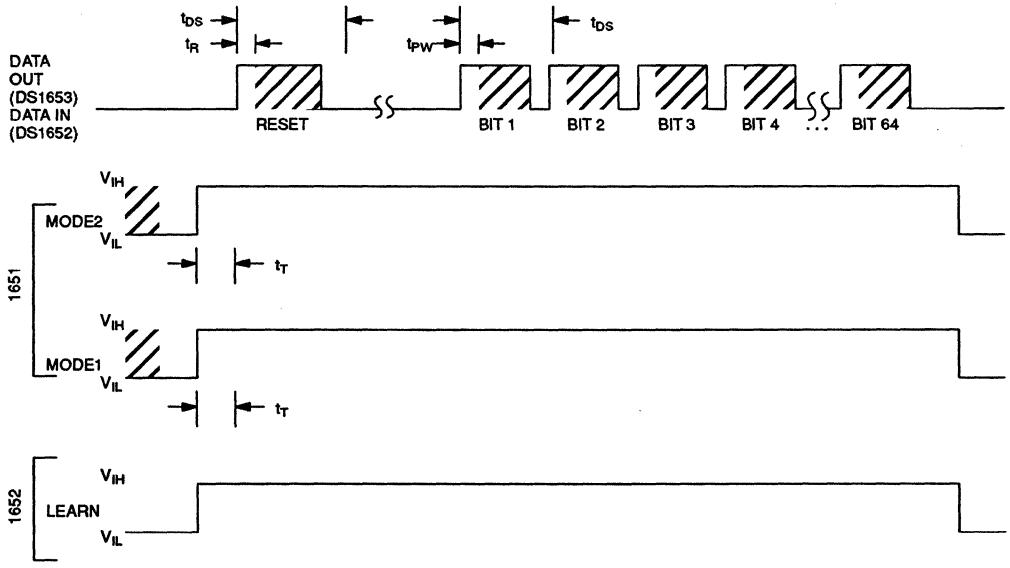
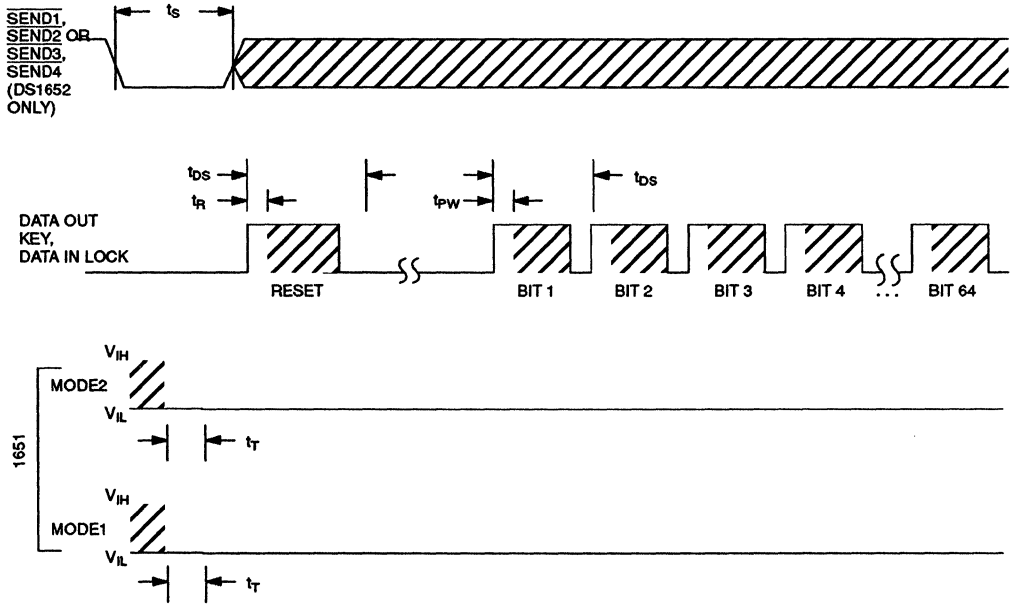
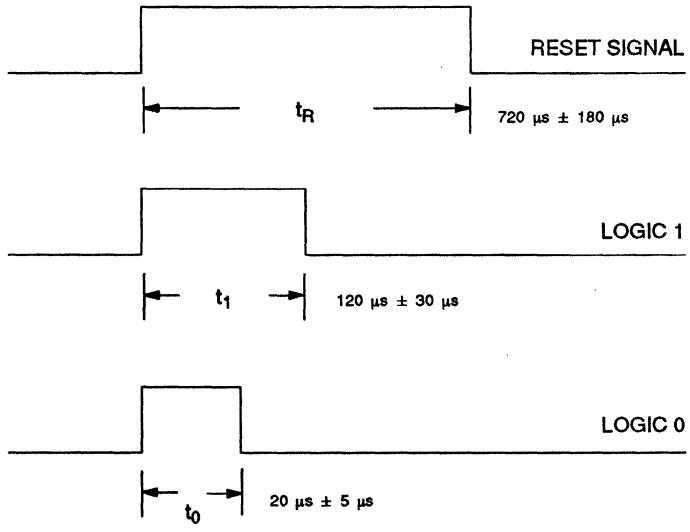
LEARN MODE DS1652 KEY; LEARN MODE DS1653 LOCK, INTERNAL PROGRAMMING



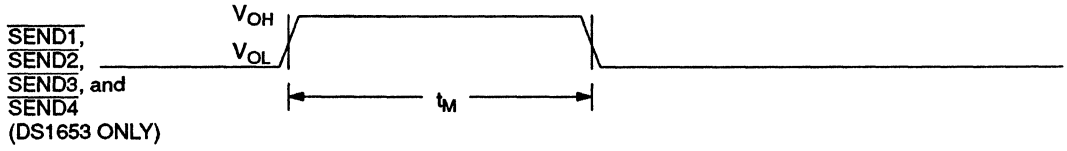
OPERATION DS1653 LOCK AND DS1652 KEY



LOGIC TIMING DIAGRAMS



DS1653 LOCK, MATCH SIGNALS



When the DS1653 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data input only.
4. Input/output leakage applies to the DS1653 data input/output pin.
5. Input voltage on the LEARN pin is required to be in the Learn mode, for the DS1653 and DS1652 to properly accept new code data.
6. The DS1652 LEARN pin should be externally ties to ground when not in use.
7. Temperature range for programming is -10°C to +85°C.
8. The DS1652 $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ inputs are internally pulled up with 25KΩ resistors.
9. These output voltages are valid for a typical V_{CC} of 5.0V ± 10%.

DALLAS SEMICONDUCTOR

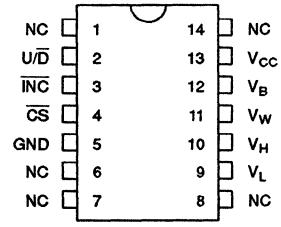
DS1666, DS1666S
Audio Digital Resistor

FEATURES

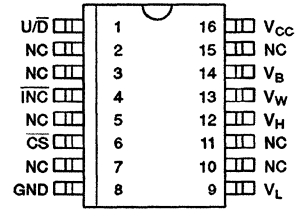
- 128 position, digitally controlled potentiometer
- Operates from a +5 volts power supply with TTL signal inputs
- Wide analog voltage range of ±5 volts.
- Resistive elements are temperature compensated to ±20 percent end to end
- Low–power CMOS
- 14–pin DIP or 16 pin SOIC for surface mount applications
- Default position on power up sets wiper position at 10%
- Operating temperature range 0°C to 70°C

		Resolution/Step		
Resistance values		Low End	High End	-3dB Point
DS1666-10	10KΩ	24Ω	110Ω	1.1 MHz
DS1666-50	40KΩ	122Ω	554Ω	200 KHz
DS1666-100	100KΩ	243Ω	1.1KΩ	100 KHz

PIN ASSIGNMENT



14-Pin DIP (300 Mil)
See Mech. Drawing – Sect. 16, Pg. 1



16-Pin SOIC (300 Mil)
See Mech. Drawing – Sect. 16, Pg. 6

PIN DESCRIPTION

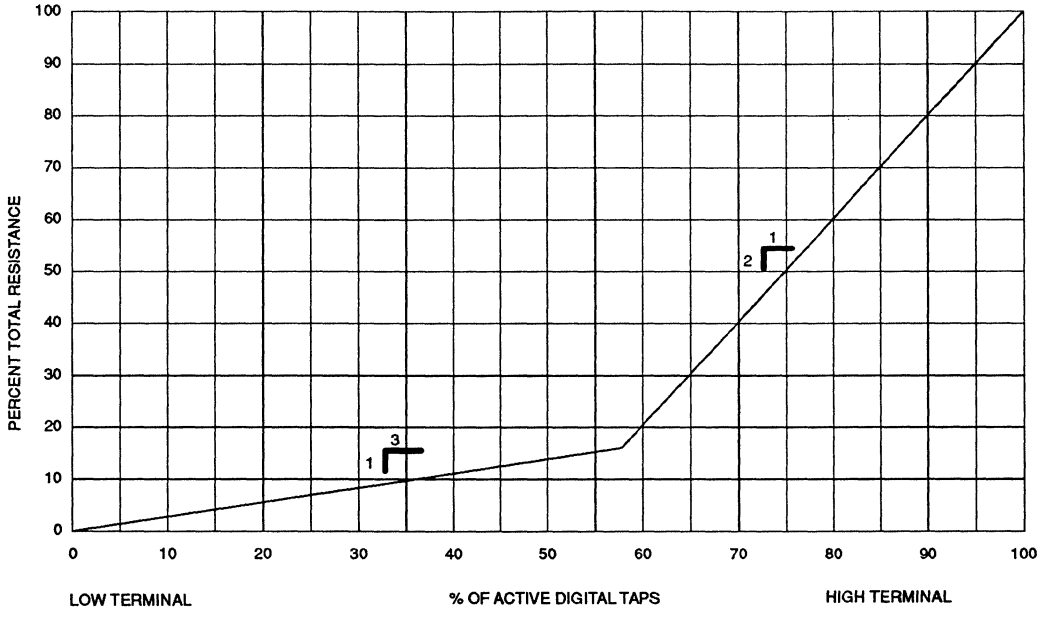
V_H	-	High Terminal of Resistor
V_L	-	Low Terminal of Resistor
V_W	-	Wiper Terminal of Resistor
U/$\overline{D}$	-	Up/Down Control
$\overline{INC}$	-	Wiper Movement Control
$\overline{CS}$	-	Chip Select for Wiper Movement
NC	-	No Connection
V_{CC}	-	+5 Volts
GND	-	Ground
V_B	-	Substrate Bias -5 Volts

DESCRIPTION

The DS1666 is a solid–state potentiometer which is set to value by digitally controlled resistive elements. The potentiometer is composed of 127 resistive sections. Between each resistive section and both ends of the potentiometer are TAP points accessible to the wiper. The position of the wiper on the resistance array is controlled by the $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs. The position of the wiper defaults to the 10% position on power up. The resolution of the DS1666 is shown in Table 1.

The DS1666 Digital Audio Resistor is uniquely designed to provide a potentiometer that is logarithmic rather than linear across its entire range. The lower half of the potentiometer advances 1% of total resistance for each 3% of scale advanced, providing for precise amplification of low volume signals. The upper half of the potentiometer advances 2% of resistance for every 1% of scale advanced, providing for the lower resolution gain required for high volume amplification.

GRAPH OF AUDIO TAPER Table 1



OPERATION

The $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs control the position of the wiper along the resistor array (Figure 1). When $\overline{CS}$ is active (low), a high to low transition on the $\overline{INC}$ will increment or decrement an internal counter depending on the level of the U/$\overline{D}$ pin. When the U/$\overline{D}$ pin is low, the counter will decrement. When the U/$\overline{D}$ pin is high, the counter will increment. The state of the U/$\overline{D}$ pin can be changed while $\overline{CS}$ is active allowing for precise adjustment during calibration. The output of the counter is decoded to set the position of the wiper. When the $\overline{CS}$ input transitions to the high (inactive) level, the value of the counter is stored and the wiper position is maintained until power (V_{CC}) is lost. When power is restored, the DS1666 returns to the default setting and positions the wiper to 10 percent. The value of the end-to-end and end-to-wiper position is indeterminate while V_{CC} is not applied.

The DS1666 has a resistor array that resembles an audio taper potentiometer as shown in Table 1. Since the taper is not linear, exact resistance values for each of the 128 positions of the resistor is not specified. However, the end-to-end resistance is specified to be within ±20 percent of the stated resistor value over a temperature range of 0°C to 70°C.

ANALOG CHARACTERISTICS

End-to-End Resistance Tolerance = ±20 percent
Typical Noise = <120 dB/Hz REF:IV
Temperature Coefficient = ±800 PPM/°C typical
Resistance at tap #74=18% ± 2%of total resistance.

PIN DESCRIPTIONS

V_H	The high end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_L	The Low end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_W	The wiper terminal of the potentiometer. The value of the wiper is controlled by the U/$\overline{D}$ and the $\overline{INC}$ pins.
Up/Down (U/$\overline{D}$)	The U/$\overline{D}$ input controls the direction of the wiper movement when setting the potentiometer.
Increment ($\overline{INC}$)	Toggling $\overline{INC}$ will move the potentiometer wiper by either incrementing or decrementing the counter.
Chip Select ($\overline{CS}$)	The device is selected when $\overline{CS}$ input is low. The current counter value is stored when CS is returned high.

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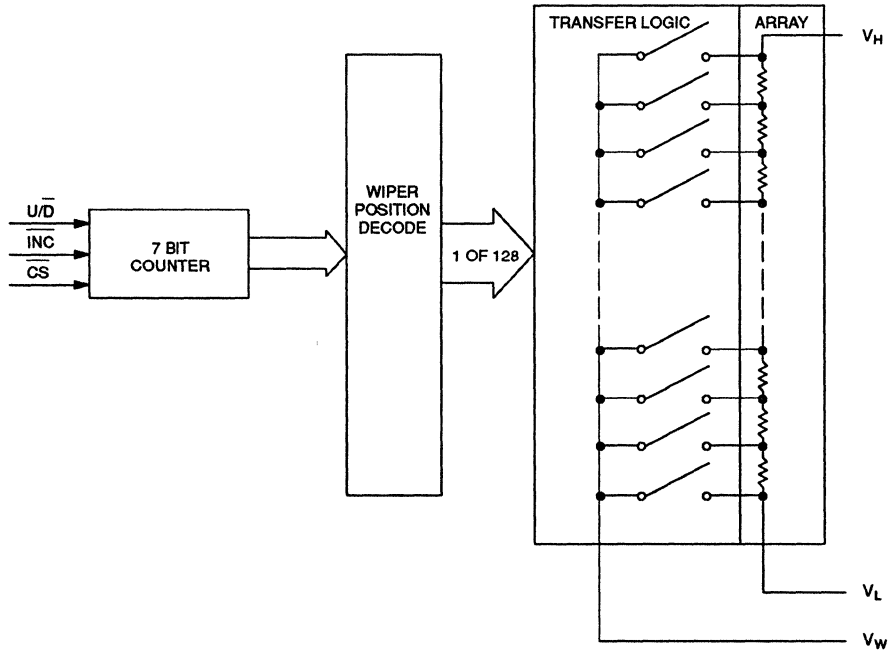
BLOCK DIAGRAM Figure 1



MODE SELECTION Figure 2

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	WIPER UP
L	↓	L	WIPER DOWN
↑	H	X	STORE WIPER POSITION

ABSOLUTE MAXIMUM RATINGS*

Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, and V_{CC} Relative to Ground	–0.5V to +7.0V
Voltage on V_H, V_L, and V_W Relative to Ground	-6.5V to +6.5V
Voltage on V_B	-6.5V to Ground
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
V_H, V_L, V_W Voltage	V_R	V_B-0.3		V_{CC}+0.3	V	1
V_B Voltage	V_B	-5.5		GND	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		0.1	5	mA	3
Input Leakage	I_{LI}	-1		+1	µA	2
Wiper Resistance	R_W		350	650	Ω	
Wiper Current	I_W		1		mA	3

10

CAPACITANCE

(t_A = 25°C)

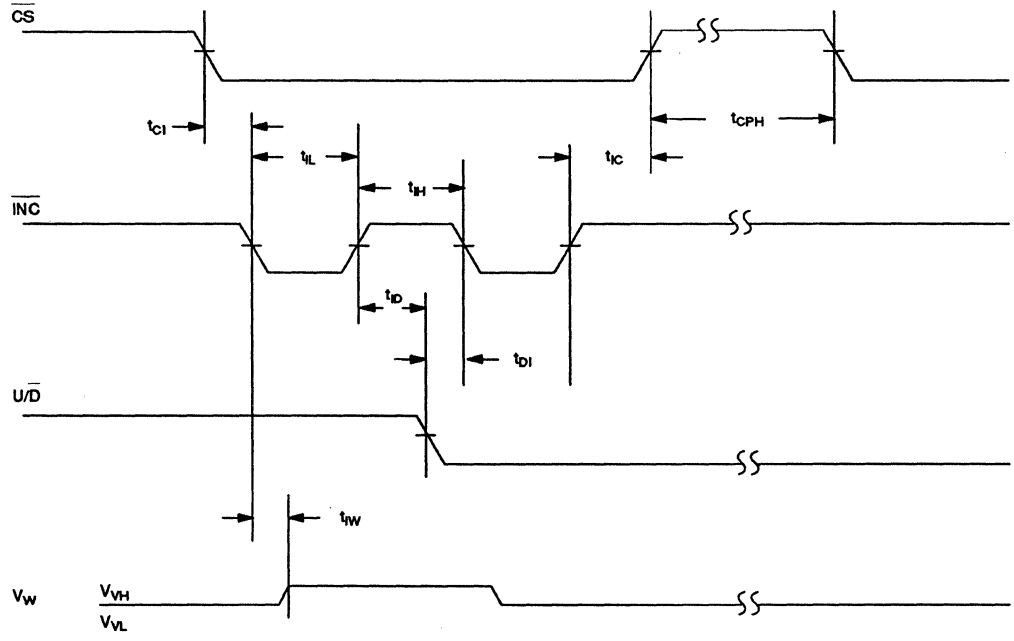
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Capacitance	C_{IN}	t_A=25°C	6	10	pF	2

AC ELECTRICAL CHARACTERISTICS

(t_A = 0°C to 70°C, V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100			ns	
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}	100			ns	
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	1			µs	
$\overline{INC}$ Low Period	t_{IL}	500			ns	
INC High Period	t_{IH}	1			µs	
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	500			ns	
$\overline{CS}$ Deselect Time	t_{CPH}	100			ns	

AC TIMING Figure 3



NOTES

1. All voltages are referenced to ground.
2. This parameter is periodically sampled and not 100% tested.
3. Typical values are for t_A = 25°C and nominal supply voltages.
4. Wiper output open circuited.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10 ns
Input Level	1.5V

DALLAS SEMICONDUCTOR

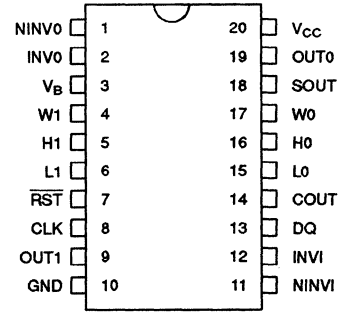
DS1667
Digital Resistor with OP AMP

FEATURES

- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power up is 50%
- Resistive elements are temperature compensated to ±20% end to end
- Two high gain wide bandwidth operational amplifiers
- Low power CMOS design
- Applications include analog–to–digital and digital–to–analog converters, variable oscillators, and variable gain amplifiers
- 20–pin DIP package or optional 20–pin SOIC surface mount package
- Operating temperature range of 0°C to 70°C
- Resistance Values

		RESOLUTION	-3 dB POINT
DS1667-10:	10K	39 ohms	1.1 MHz
DS1667-50:	50K	195 ohms	200 kHz
DS1667-100:	100K	390 ohms	100 kHz

PIN ASSIGNMENT



20-Pin DIP (300 Mil) and 20-Pin SOIC
See Mech. Drawings – Sect 16, Pgs.1 & 6

PIN DESCRIPTION

V_{CC}	-	+5 Volt Supply
GND	-	Ground
L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W0, W1	-	Wiper End of Resistor
V_B	-	Substrate Bias and OP AMP Negative Supply
SOUT	-	Wiper for Stacked Configuration
$\overline{RST}$	-	Serial Port Reset Input
DQ	-	Serial Port Input/Output
CLK	-	Serial Port Clock Input
COUT	-	Cascade Serial Port Output
NINV0, NINVI	-	Noninverting OP AMP Input
INV0, INVI	-	Inverting OP AMP Input
OUT0, OUT1	-	OP AMP Outputs

10

DESCRIPTION

The DS1667 is a dual–solid state potentiometer that is adjustable by digitally selected resistive elements. Each potentiometer is composed of 256 resistive elements. Between each resistive section of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit register that controls which tap point is connected to the wiper output. Each 8–bit register can be read or written by sending or receiving data bits over a 3–wire serial port. In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1667 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same. The DS1667 also contains two high gain wide bandwidth operational amplifiers. Each amplifier has both the inverting and non-inverting inputs and the output available for user configuration. The operational amplifiers can be paired with the resistive ele-

ments to perform such functions as analog to digital conversion, digital to analog conversion, variable gain amplifiers, and variable oscillators.

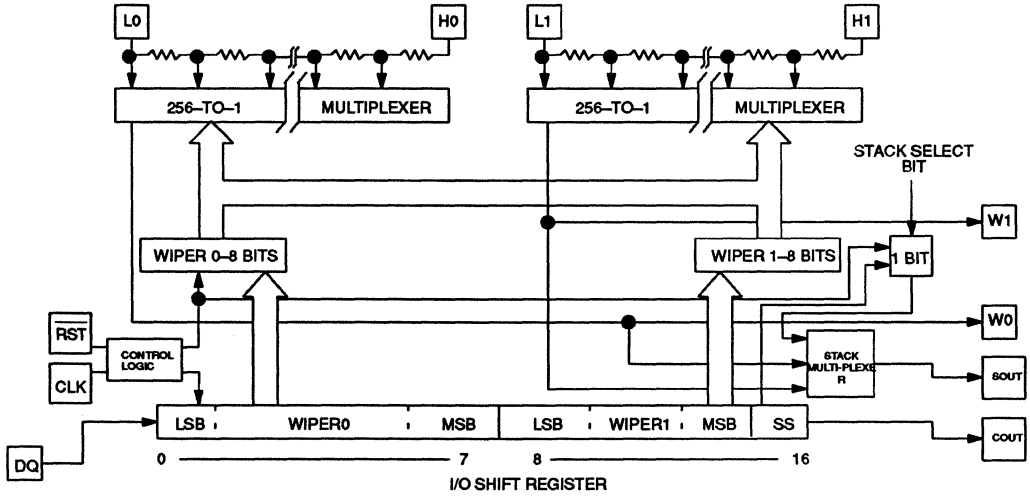
OPERATION - DIGITAL RESISTOR SECTION

The DS1667 contains two potentiometers, each of which has its wiper set by a value contained in an 8 bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end.

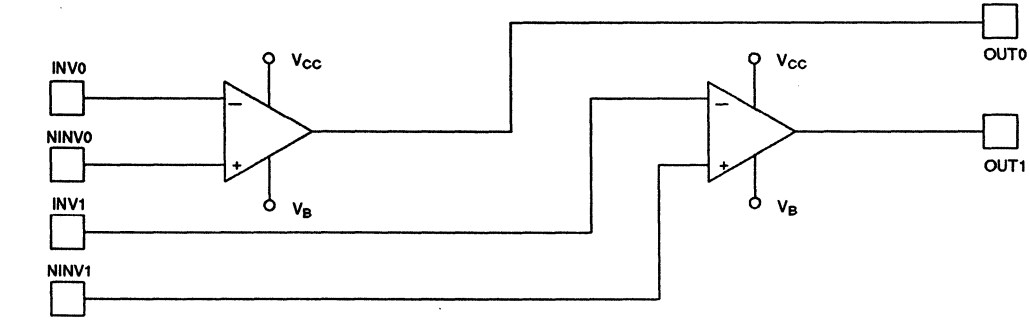
In addition, the potentiometer can be stacked by connecting them in series such that the high end of potentiometer 0 is connected to the low end of potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (SOUT). A zero written to the stack multiplexer will connect wiper 0 to the SOUT pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is presented at the SOUT pin.

BLOCK DIAGRAM Figure 1

RESISTOR SECTION



OP AMP SECTION



Information is written to and read from the wiper 0 and wiper 1 registers and the stack select bit via the 17-bit I/O shift register. The I/O shift register is serially loaded by a 3 wire serial port consisting of $\overline{RST}$, DQ, and CLK. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17 bit shift register only when the $\overline{RST}$ input is at a high level. While at a high level, the $\overline{RST}$ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until $\overline{RST}$ is taken to a low level, which terminates data transfer. While $\overline{RST}$ input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O shift register while $\overline{RST}$ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The next 8 bits to be entered are those specifying the wiper 1 setting. The MSB of these 8 bits is sent first. The next 8 bits to be entered are those specifying the wiper 0 setting, sent MSB first. The 17th bit to be entered, therefore, will be the least significant bit of the wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, sending other than 17 bits can produce indeterminate potentiometer settings.

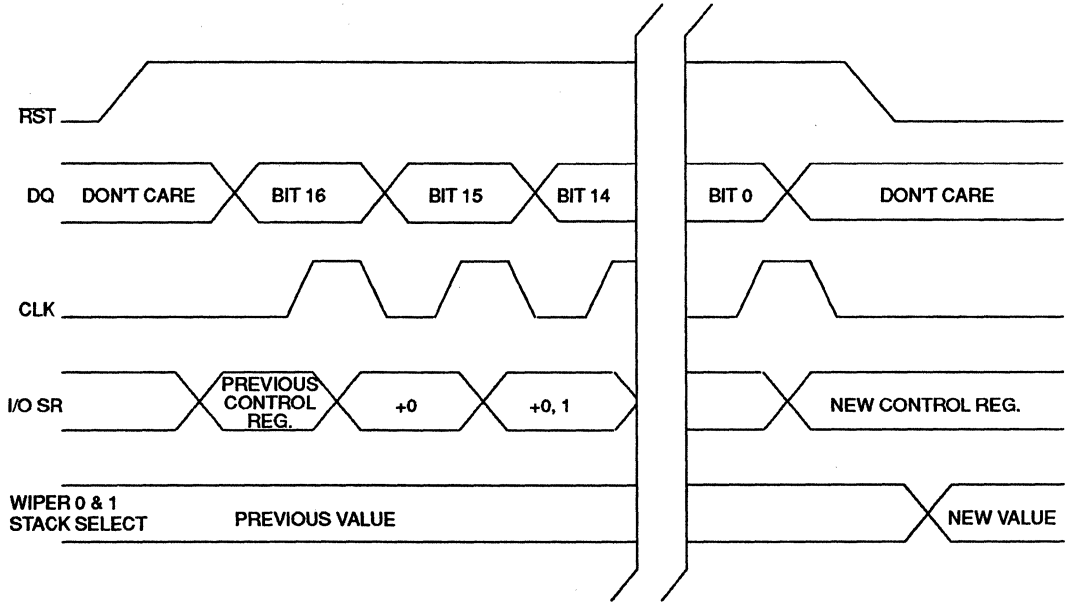
As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (COUT). By connecting the COUT pin to the DQ pin of a second DS1667, multiple devices can be daisy chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1667s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the COUT pin of the last device connected in a daisy chain must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between COUT and DQ when writing to the device (see Figure 3).

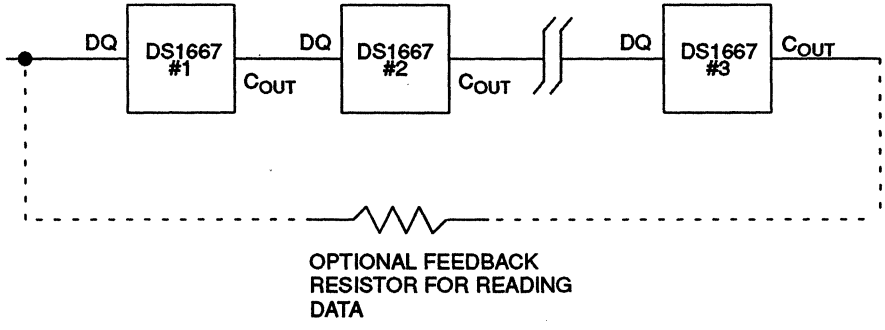
When reading data, the DQ line is left floating by the reading device. When $\overline{RST}$ is held low, bit 17 is always present on the COUT pin, which is fed back to the input DQ pin through the resistor (see Figure 4).This data bit can now be read by the reading device. The $\overline{RST}$ pin is then transitioned high to initiate a data transfer. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on COUT and DQ. After 17 bits (or 17 times the number of devices for a daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the wiper 0 and wiper 1 registers and the stack select bit.

When power is applied to the DS1667, the device always has the wiper settings at half position and the stack select bit is at zero.

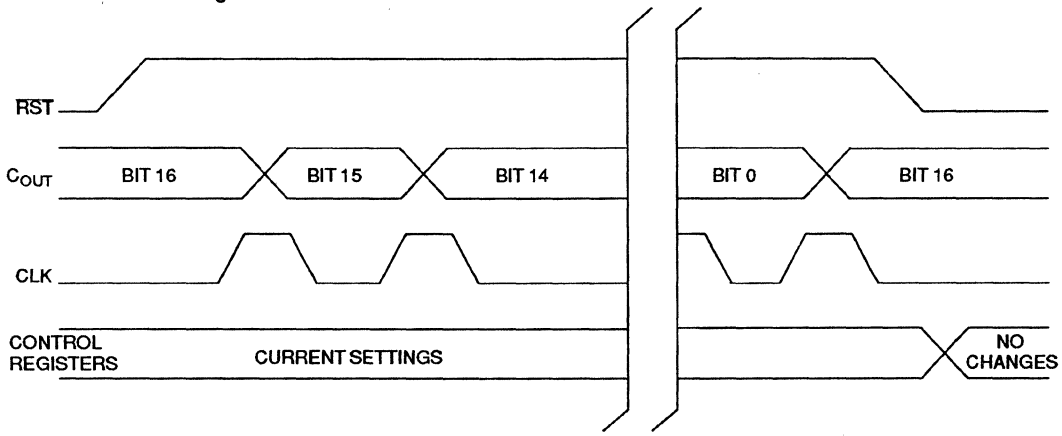
WRITING DATA Figure 2



CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



DS1667 LINEARITY MEASUREMENTS

An important specification for the DS1667 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1667 is shown in Figure 5. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW which is typically 400 ohms. For any given setting N for the pot, the expected voltage output at SOUT is:

$$VO = -5 + [10 \times (N/256)] \text{ (in volts)}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above, and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/256 or 0.03906 volts. The equation for the absolute linearity of the DS1667 is:

$$\frac{V_O(\text{actual}) - V_O(\text{expected})}{LSB} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1667 is ± 1 LSB typical.

Relative linearity is a comparison of the difference of actual output voltages of two successive taps and the difference of the expected output voltages of two successive taps. The expected difference of output voltages is 1 LSB or 0.03906V for the measurement system of Figure 5. Relative linearity is expressed in terms of an LSB and is given by the equation:

$$\frac{\Delta V_O(\text{actual}) - LSB}{LSB} = RL$$

The specification for relative linerity of the DS1667 is ± 0.5 LSB typical.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (RL) versus wiper setting for a typical DS1667 at 25°C.

DESCRIPTION AND OPERATION - OP AMP SECTION

The DS1667 contains two operational amplifiers which are ideal for operation from a single 5V supply and ground or from ±5V supplies (see Figure 1). An internal resistor divider defines the internal reference of the op amp to be halfway between the power supplies, i.e.:

$$\frac{V_{DD} + V_B}{2}$$

For optimal performance, choose analog ground to be this value. The operational amplifiers feature rail to rail output swing in addition to an input common mode range that includes the positive rail. Performance features include broad band noise immunity as well as voltage gain into realistic loads specified at both 600 ohms and 2K ohms. High voltage gain is produced with low input offset voltage and low offset voltage drift. Current consumption is less than 1.9 mA per amplifier and the device is virtually immune to latchup.

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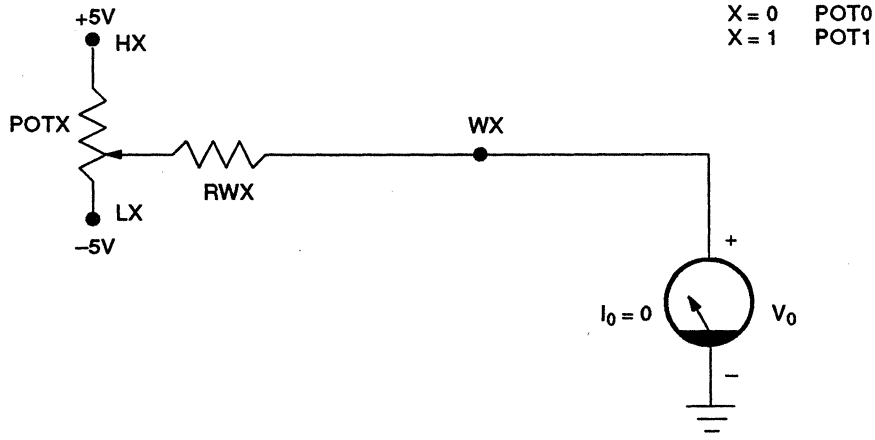
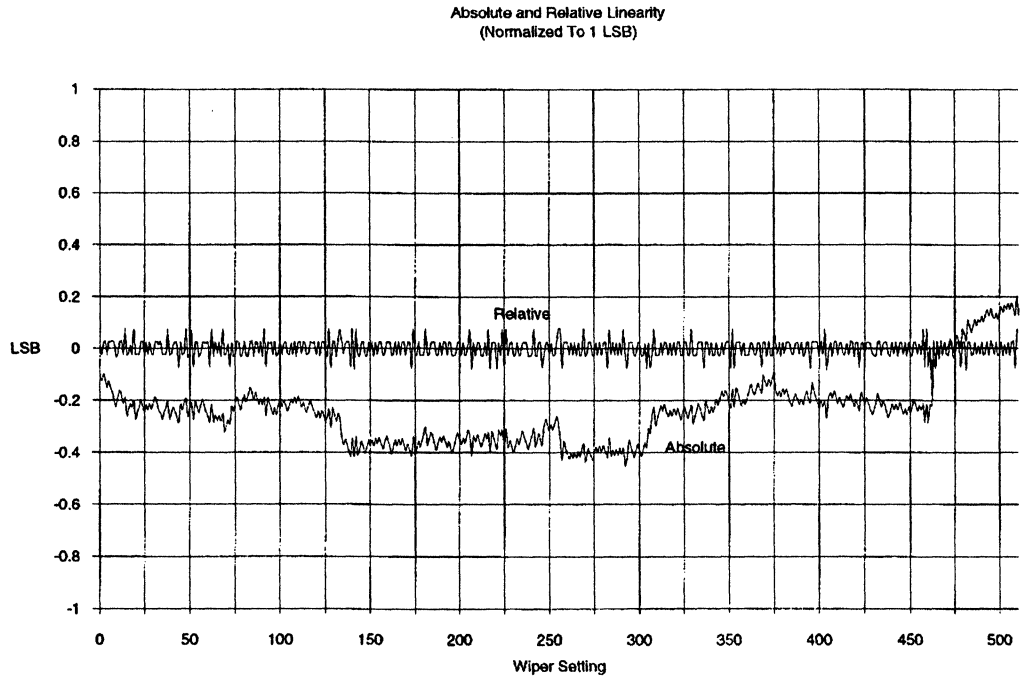
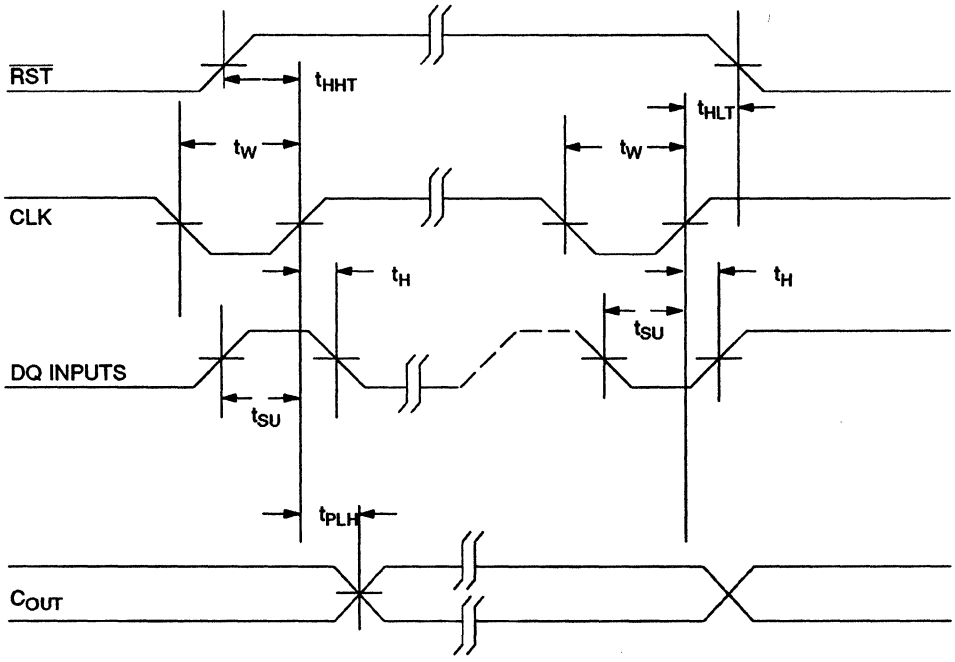
LINEARITY MEASUREMENT CONFIGURATION Figure 5



DS1667 ABSOLUTE AND RELATIVE LINEARITY Figure 6



TIMING DIAGRAM: RESISTOR SECTION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B = GND)	–0.5V to +7.0V
Voltage on Resistor Pins when V_B = -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS RESISTOR SECTION (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
Negative Supply Voltage	V_B	-5.5		GND	V	1
Resistor Inputs	L, H, W	V_B - 0.5		V_{CC} + 0.5	V	2

DC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C, V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Current	I_{CC}		3	5	mA	8
Negative Supply Current	I_B		3	5	mA	8
Input Leakage	I_U	-1		+1	µA	
Wiper Resistance	R_W		400	1000	ohms	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	-1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	-1.0			mA	
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	
End-to-End Resistor Tolerance	TOL_R	-20		+20	%	
Noise (ref: 1V)	N		-120		$\frac{dB}{\sqrt{Hz}}$	
Absolute Linearity	AL		1.0		LSB	
Relative Linearity	RL		0.5		LSB	
Resistor Temperature Coefficient	TC_R			850	$\frac{ppm}{°C}$	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS RESISTOR SECTION (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}			10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
$\overline{RST}$ High to Clock Input High	t_{HHT}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	

OPERATIONAL AMPLIFIER SECTION DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage	V_{OS}		5	10	mV	
Input Offset Voltage Drift	V_{OSD}		10		uV/°C	
Common Mode Rejection	CM_R		62		dB	
Positive Power Supply Rejection	$+PS_R$		62		dB	4
Negative Power Supply Rejection	$-PS_R$		62		dB	4
Input Common Mode Voltage Range	C_{CCM}	V_B+1.5V		V_{CC}	V	
Large Signal Voltage Gain			106		dB	R_L = 2KΩ
Large Signal Voltage Gain			96		dB	R_L = 600KΩ
Output Swing	V_{SWGH}	4.6	4.7		V	R_L = 2KΩ toGND
Output Swing	V_{SWGL}		-4.7	-4.6	V	V_B = -5V
Output Swing	V_{SWGH}	4.5	4.6		V	R_L = 600Ω toGND
Output Swing	V_{SWGL}		-4.6	-4.5	V	V_B = -5V
Output Current	$V_{O, SOURCE}$	13	58		mA	V_O = 0 Volts
Output Current	$V_{O, SINK}$	13	63		mA	V_O = +5 Volts

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OPERATIONAL AMPLIFIER SECTION AC ELECTRICAL CHARACTERISTICS

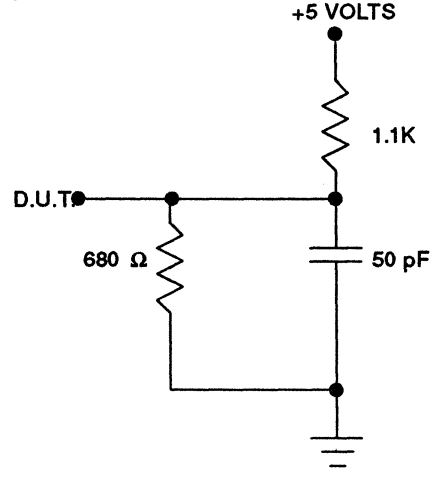
(0°C to 70°C V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	V_{SL}	0.7	2		V/µs	6
Gain Bandwidth Product	GBP		2.5		MHz	5
Phase Margin	PM		75		deg	5
Gain Margin	GM		20		dB	5
Amp to Amp Isolation	AAI		130		dB	
Input Referred Voltage Noise	IRVF		100		$nV/\sqrt{Hz}$	F=1 KHz
Input Referred Current Noise	IRVI		.0002		$pA/\sqrt{Hz}$	F=1 KHz
Total Harmonic Distortion	HD		0.1		%	F = 10 kHz AV = − 10 RL = 2KΩ V_O = 1V_{PP}

NOTES

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction
3. Measured with a load as shown in Figure 8.
4. Over a frequency range of 0 - 1 KHz.
5. Load is R_L = 600 Ω C_L = 10 pF
6. V_{DD} = +5.0V V_B = -5.0V connected as voltage follower with 10V step input and R_L = ∞.
7. To achieve best op amp performance, V_{DD} = +5.0V V_B = -5.0V and analog ground = 0V. In general analog ground = $\frac{V_{DD} + V_B}{2}$.
8. OP AMPS idle, no load.

LOAD SCHEMATIC Figure 8



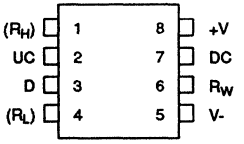
DALLAS SEMICONDUCTOR

DS1668, DS1669, DS1669S
Dallastat™ Electronic Digital Rheostat

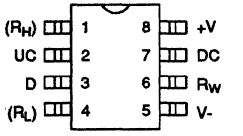
FEATURES

- Replaces mechanical variable resistors
- Available as the DS1668 with manual interface or the DS1669 integrated circuit
- Human engineered interface provides easy control with DS1668
- Electronic interface provided for digital as well as manual control
- Wide differential input voltage range between 4.5 and 8 volts
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8 pin SOIC and 8 pin DIP packages for DS1669
- Standard resistance values for Dallastat
  - DS1668/DS1669–10 ~ 10KΩ
  - DS1668/DS1669–50 ~ 50KΩ
  - DS1668/DS1669–100 ~ 100KΩ

PIN ASSIGNMENT DS1669



8-Pin DIP (300 Mil)
See Mech. Drawing Sect. 16, Pg. 1

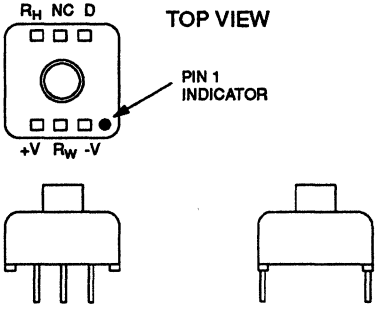


8-Pin SOIC (200 Mil)
See Mech. Drawing Sect. 16, Pg. 5

PIN DESCRIPTION DS1669

R_H	-	Resistor High End (Option)
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input
NC	-	No Connect

PIN ASSIGNMENT DS1668



PIN DESCRIPTION DS1668

+V	-	Positive Voltage Input
-V	-	Negative Voltage
R_W	-	Resistor Wiper
D	-	Digital Input
R_H	-	Resistor High End
NC	-	No Connection - Pin Missing

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DESCRIPTION

The Dallastat is a digital rheostat or potentiometer which is adjusted to a desired value by a contact closure input. Alternatively, the desired setting can be achieved from a digital source input. When supplied as a 6 pin device, the contact closure is provided on the top of the package. In this configuration (DS1668), -V is connected to R_L on the bottom side of the package, and R_W, +V, D and R_H are single connections on the bottom side of the package. The 6 pin Dallastat is a self contained substitute for rheostat and potentiometer applications. Any time the button on the top of the package is depressed the resistance between pins -V and R_W will increase or decrease provided that a potential of +4.5V to +8V exist between -V and +V inputs. The 8 pin packaged versions of the Dallastat (DS1669) can be used in a similar manner as the 6 pin version with -V connected to R_L; +V connected to a positive source greater than +4.5 volts relative to -V, and a contact closure between the inputs and -V. Under this condition the wiper pin (R_W) provides a variable resistance relative to -V and is increased or decreased based on a sequence of contact inputs between UC, DC, or D, and -V.

Both the DS1668 and DS1669 can also be controlled by a digital input which functions in parallel with a contact closure or instead of contact closure. In addition, the DS1669 can be configured with and up/down two button arrangement.

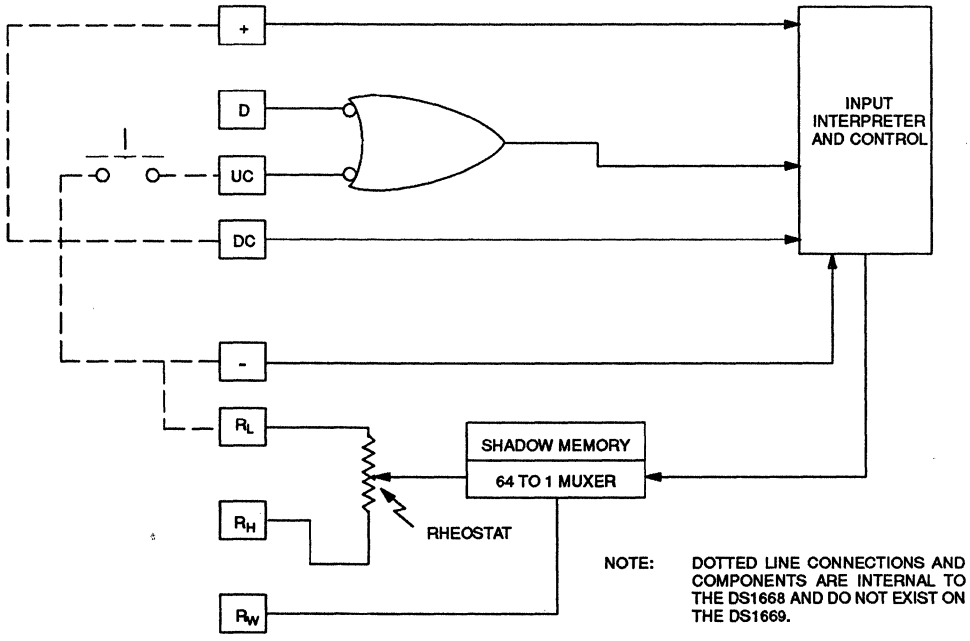
OPERATION

The main elements of the Dallastat are shown in the block diagram of Figure 1. The diagram shows that the rheostat or variable resistor setting is determined by the value of a 64 to 1 muxer which is controlled by the input interpreter. The input interpreter takes a UC, DC, or D input, and sends control information to the multiplexer. The way the interpreter derives the control information is key to the operation of the Dallastat. The dotted lines shown in the block diagram are included in the DS1668 device and serve as a typical application example for the use of the DS1669 DIP and SOIC devices. As shown, a pushbutton contact is between UC and -V and pulls the input of an "OR" gate to the negative supply. Note that "D" assumes a logic high level when not connected. When the input of the OR gate is first connected low, the interpreter sends a pulse to the multiplexer which will either increment or decrement the rheostat wiper position $^1/_{64}$ of the total taper (see flow diagram Figure 2 and 3). Increment or decrement determination is based on prior activity. A single input from contact closure of a duration of greater than 1 ms is sufficient to cause a wiper position change of $^1/_{64}$ of total. Subsequent inputs will increment or decrement $^1/_{64}$ of total for each additional contact closure. However, if the contact input remains active for greater than 1 second, increments/decrements of $^1/_{64}$ of total occur at intervals of 100 ms for as long as the input is active or until the top or bottom of the rheostat taper is reached. Anytime that input activity stops for a period of time greater than 1 second, the next action taken as a result of subsequent input activity will be reversed; i.e., if the Dallastat was incrementing, it will decrement, and if decrement was the prior action, the next action taken will be increment. If input activity is maintained for a period of time such that the upper or lower limits of the rheostat are reached, successive action is in the opposite direction. Total time of movement from one end of the taper to the other requires 64 X 100 ms + 1 second or 7.4 seconds. The DS1669 version of the Dallastat can be configured for two button operation such that the DC input can be used for decrementing and the UC input is then used only for incrementing. Upon power up, the device will internally sense the impedance between the DC input and V+. For this reason, the DC input must be connected to +V when not in use. Otherwise, the DS1669 version of the Dallastat performs as described above with the contact input attached external to the device package. Connection between contact inputs and -V of less than 10K is all that is required to be interpreted as activity. Alternatively, the D input accepts a low going signal of 0.8 volts maximum with respect to -V. The input pulse width must exceed 1 us to guarantee recognition. Successive input pulses can be any length apart provided they are not separated by more than 1 second. As with manual inputs, increment/decrement action reverses if input activity stops for a period of time greater than 1 second. If the D input is held low for more than 1 second, incrementing/decrementing occurs automatically on $^1/_{64}$ of total intervals. The flow chart for electronic control is shown in Figure 2, as the D input acts the same as the UC input. When the DS1669 is used, the rheostat low end and wiper may be connected to voltage sources other than -V or +V. The voltage applied to any rheostat element must not exceed -V - 0.5 volts on the low end or +V + 0.5 volts on the high end. If -V is connected to ground, then all other input voltages are referenced to ground.

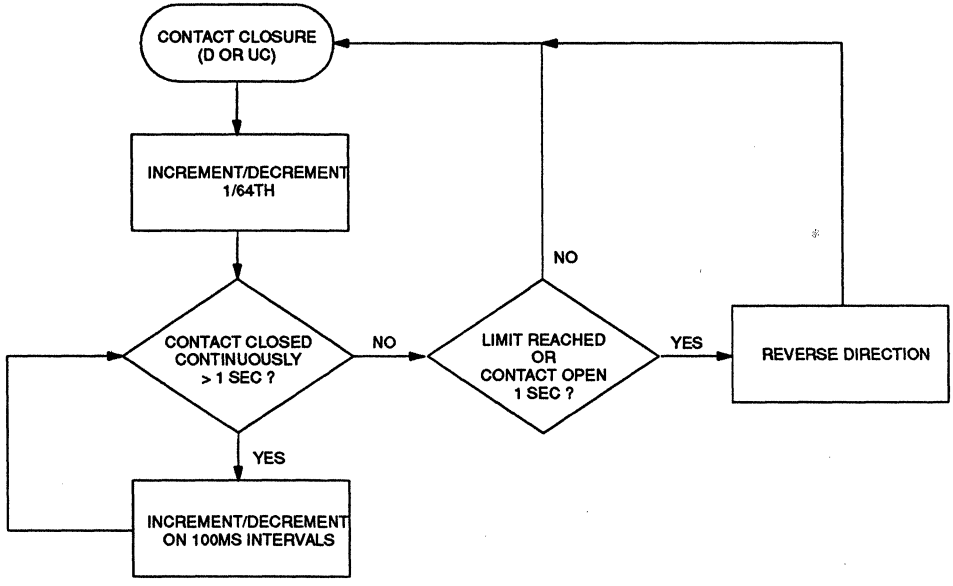
NONVOLATILE WIPER SETTINGS

The wiper setting of the Dallastat is maintained in the absence of power in the shadow memory. During normal operation the position of wiper is determined by the multiplexer. The shadow memory is periodically updated by the multiplexer during normal operation. The manner in which an update occurs has been optimized for reliability, durability, and performance and is totally transparent to the user. When power is applied to the Dallastat, the wiper setting is set at the last value recorded in the shadow memory. On an initial power up for the first time, the wiper position may therefore be random. If the Dallastat setting is changed after power is applied, the new value will be stored in the shadow memory after a delay of about 2 seconds. The initial storing of a new value after power up always occurs when the first change is made regardless of when this change occurs after power up. After the initial change, subsequent changes in the Dallastat setting of less than 12.5% are not copied in the shadow memory. Since the Dallastat contains a 64 to 1 multiplexer, a change in the 3 LSB's is not copied into the shadow memory except for change after power up. Changes greater than 12.5% or changes large enough to affect the 4 LSB or greater are always copied into the shadow memory. As on power up, a copy from the multiplexer to shadow memory allows for a 2 second delay to guarantee that the new setting changes are finalized, and all shadow updates are transparent to the user. On power down (loss of power) the shadow memory is not changed and retains the most recent update resulting from a setting change. This value is used to set the Dallastat value on power up. The shadow memory is made with E^2 PROM type memory cells that will accept at least 80 thousand value changes before wearout. If the E^2 PROM cells ever reach a wearout condition, the Dallastat will still continue to operate properly while power is applied, but will return to the last accepted value of the shadow RAM on power up.

DS1668 DALLASTAT™ BLOCK DIAGRAM Figure 1

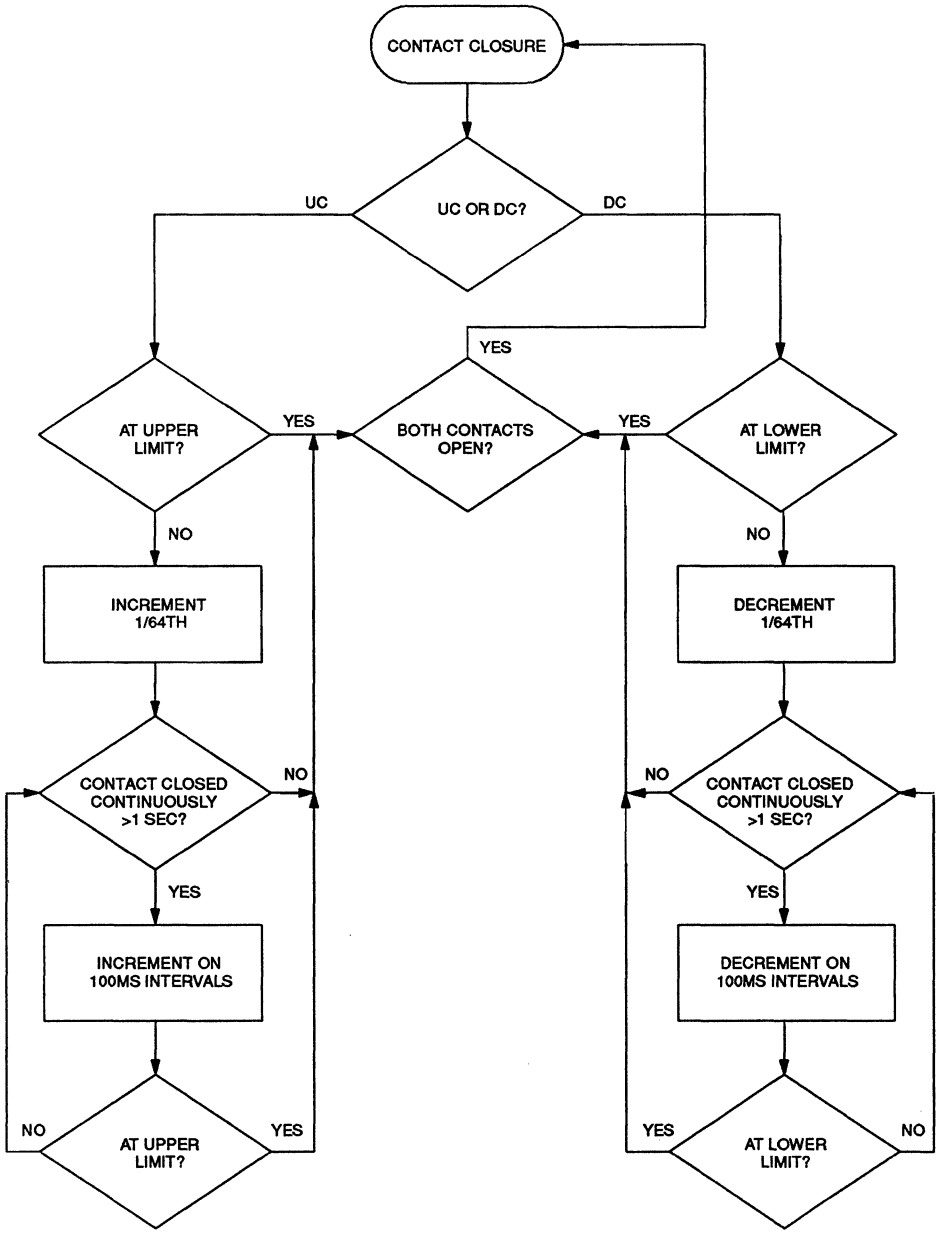


FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 2



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1s ± 10%

FLOWCHART: TWO BUTTON OPERATION Figure 3



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 sec. ± 10%

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	–10°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 15 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-10°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 4.5		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 4.5	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2
Logic Input 0	V_{IL}			+0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(-10°C to +70°C -V to +V = 4.5V to 7.0V)

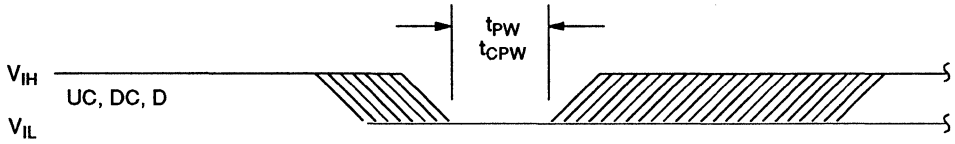
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State	I_{CC2}			100	nA	9
Wiper Resistance	R_W		500	1000	Ω	
Wiper Current	I_W			2	mA	5
Rheostat Current	I_H, I_L			2	mA	5

AC ELECTRICAL CHARACTERISTICS

(-10°C to +70°C -V to+V = 4.5V to 7.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{PW}	1		DC	µs	1, 7, 8
Contact Pulse Width	t_{CPW}	1		DC	ms	1, 7, 8
Capacitance	C_{IN}		5	10	pF	6

TIMING DIAGRAM

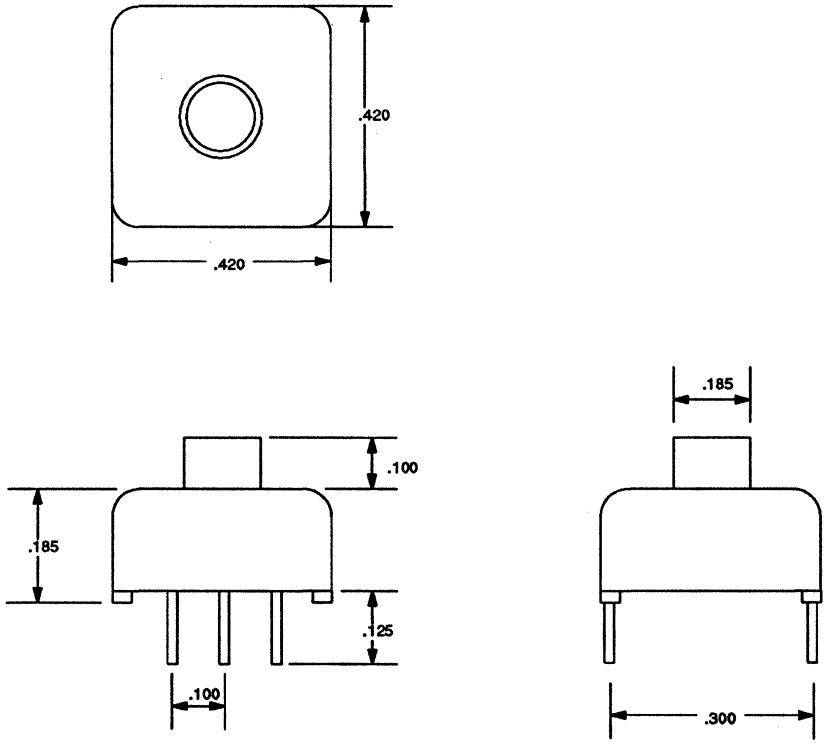


NOTES

1. All inputs; UV, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input.
9. Idle state supply current is measured with no pushbutton depressed and with the wiper. R_W tied to a CMOS load.

10

DS1668 PUSHBUTTON DIMENSIONS



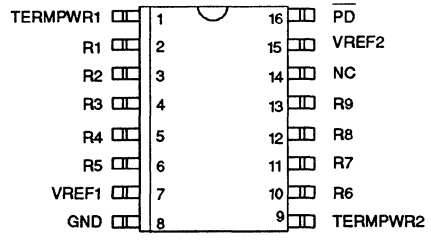
DALLAS SEMICONDUCTOR

DS2107S
SCSI Terminator

FEATURES

- Fully compliant with SCSI and SCSI-2 standards
- Provides active termination for 9 signal lines
- Laser-trimmed 110 ohm termination resistors have 1% tolerance
- Low dropout voltage
- 16-pin plastic SOIC package
- Power-down mode isolates termination resistors from the bus

PIN ASSIGNMENT



16-Pin SOIC (300 mil)
See Mech. Drawing – Sect. 16, Pg. 6

10

DESCRIPTION

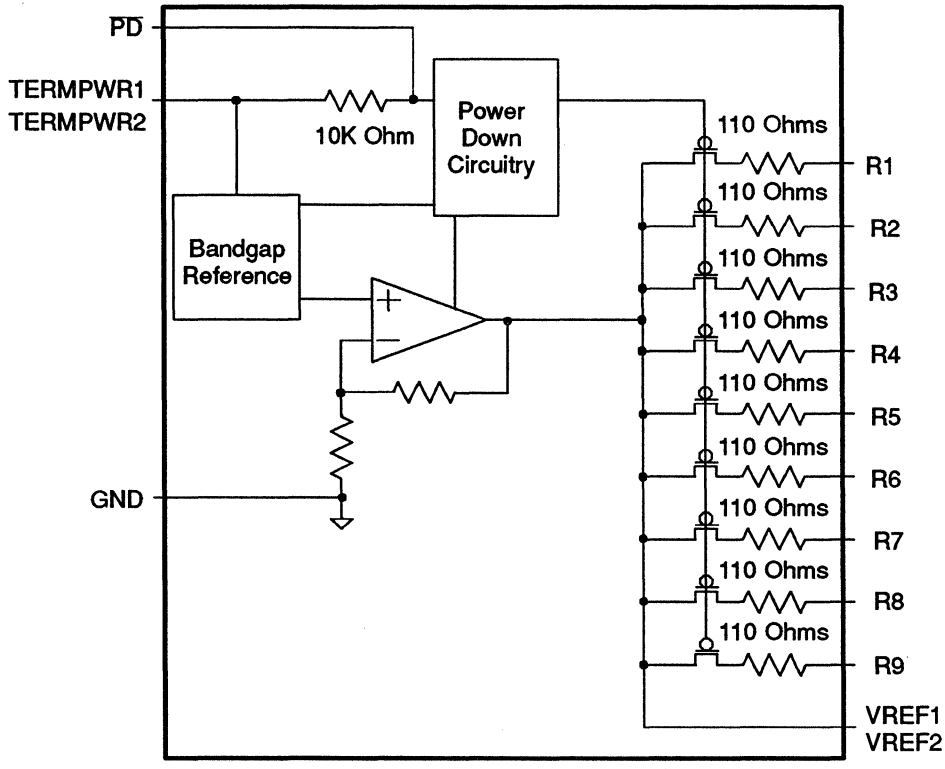
The SCSI-2 standard recommends the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS2107S SCSI Terminator, which is fully compliant with the standard, enables the designer to gain the benefits of active termination: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS2107S integrates a regulator and nine precise switched 110 ohm termination resistors into a monolithic IC.

FUNCTIONAL DESCRIPTION

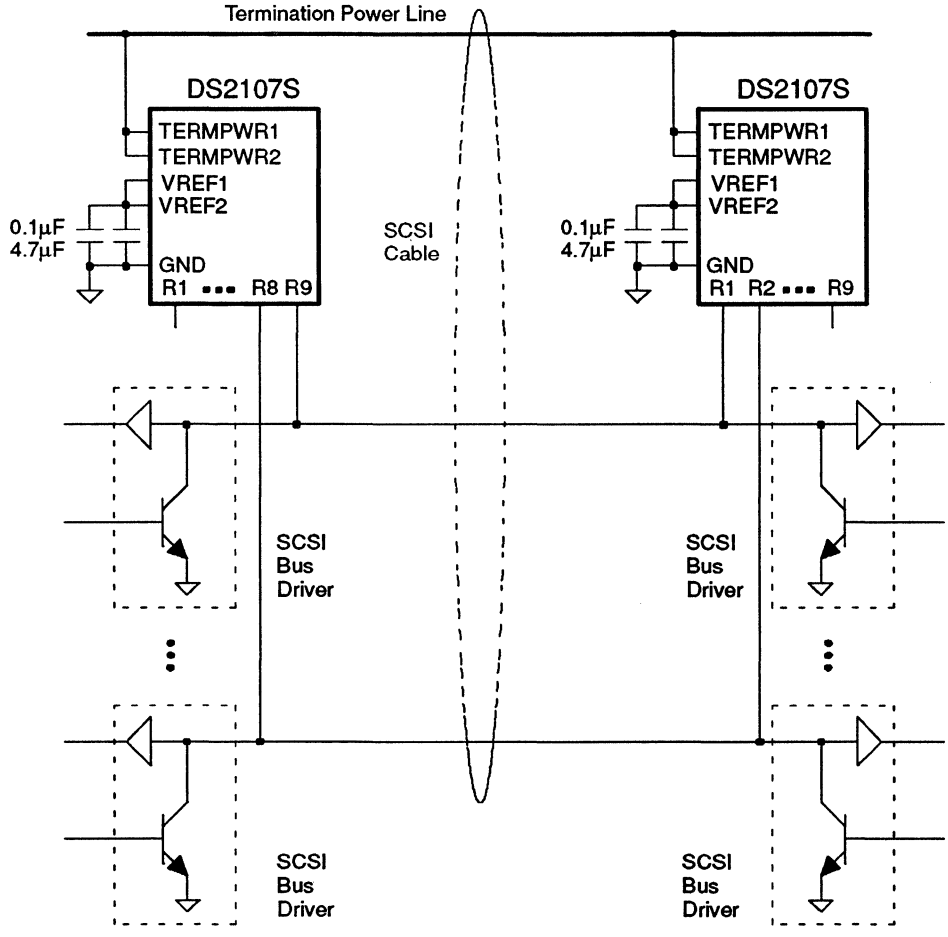
The DS2107S consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level which is fed to a buffer amplifier. The buffer produce s a 2.85V level and is capable of sourcing 24 mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator will pull the signal line to 2.85V (quiescent state). When all lines settle in the quiescent state, the regulator will sink about 10 mA. When the DS2107S is put into power-down mode by bringing $\overline{PD}$ low, the power-down circuitry will turn off the transistors on each signal line. This will isolate the DS2107S from the signal lines and effectively remove it from the circuit. The power-down pin ($\overline{PD}$) has an internal 10K ohm pull-up resistor. To place the DS2107S into an active state, the $\overline{PD}$ pin should be left open circuited.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS2107S requires parallel 0.1 µF and 4. 7 µF capacitors connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit wide SCSI bus arrangement ("A" Cable), two DS2107S's would be needed at each end of the SCSI cable in order to terminate the 18 active signal lines. In a 16-bit wide SCSI bus arrangement ("P" Cable), three DS2107S's would be needed at each end of the SCSI cable in order to terminate the 27 active signal lines.

DS2107S BLOCK DIAGRAM Figure 1



TYPICAL SCSI BUS CONFIGURATION Figure 2



10

PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	TERMPWR1	**Termination Power 1.** Should be connected to the SCSI TERMPWR line. See Figure 2.
2	R1	**Signal Termination 1.** 110 ohm termination.
3	R2	**Signal Termination 2.** 110 ohm termination.
4	R3	**Signal Termination 3.** 110 ohm termination.
5	R4	**Signal Termination 4.** 110 ohm termination.
6	R5	**Signal Termination 5.** 110 ohm termination.
7	VREF1	**Reference Voltage 1.** Must be externally connected to the VREF2 pin. Must be decoupled with a 4.7µF and a 0.1µF as shown in Figure 2.
8	GND	**Ground.** Signal ground; 0.0V.
9	TERMPWR2	**Termination Power 2.** Should be connected to the SCSI TERMPWR line. See Figure 2.
10	R6	**Signal Termination 6.** 110 ohm termination.
11	R7	**Signal Termination 7.** 110 ohm termination.
12	R8	**Signal Termination 8.** 110 ohm termination.
13	R9	**Signal Termination 9.** 110 ohm termination.
14	NC	**No Connect.** Do not connect any signal to this pin.
15	VREF2	**Reference Voltage 2.** Must be externally connected to the VREF1 pin. Must be decoupled with a 4.7µF and a 0.1µF as shown in Figure 2.
16	$\overline{PD}$	**Power Down.** When tied low, the DS2107S enters a power-down mode. Contains an internal 10K pull-up. Strap low to deactivate the DS2107S, leave open circuited to activate the DS2107S.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V_{TP}	4.00		5.25	V	
$\overline{PD}$ Active	V_{PDA}	-0.3		0.8	V	
$\overline{PD}$ Inactive	V_{PDI}	2.0		V_{TP} +0.3	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I_{TP}			245	mA	1,3
	I_{TP}			15	mA	1,4
Power Down Current	I_{PD}			750	µA	1,2,5
Termination Resistance	R_{TERM}	108	110	112	ohms	1,2

REGULATOR CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{REF}	2.79	2.85	2.91	V	1,2
Drop Out Voltage	V_{DROP}		0.8	1.0	V	1.3
Line Regulation	LI_{REG}		0.1	0.25	%	1,4
Load Regulation	LO_{REG}		1	2	%	1,2

NOTES

1. 4.00V < TERMPWR < 5.25V.
2. 0.0V < signal lines < 3.0V.
3. All signal lines = 0.0V.
4. All signal lines open.
5. $\overline{PD}$ = 0.0V.

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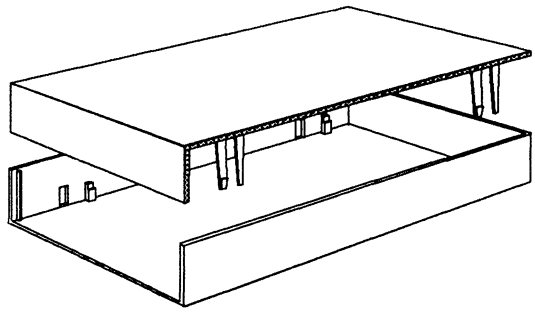
DALLAS SEMICONDUCTOR

DS9005
Eurocard Enclosure

FEATURES

- Low-cost molded enclosure
- Two-piece, snap together construction
- Made of rugged, flame-retardant polyester PBT plastic
- Accepts DS9006 SIP Stik Motherboard or any other single size Eurocard printed circuit board
- Can be custom machined to allow for connector requirements
- Component clearance of .230" solder side, 1.000" circuit side using .062" board
- Smooth indents on bottom side for rubber bumpers
- Hole knockouts for mounting



See Mech. Drawing - Sect. 16, Pg. 21

DESCRIPTION

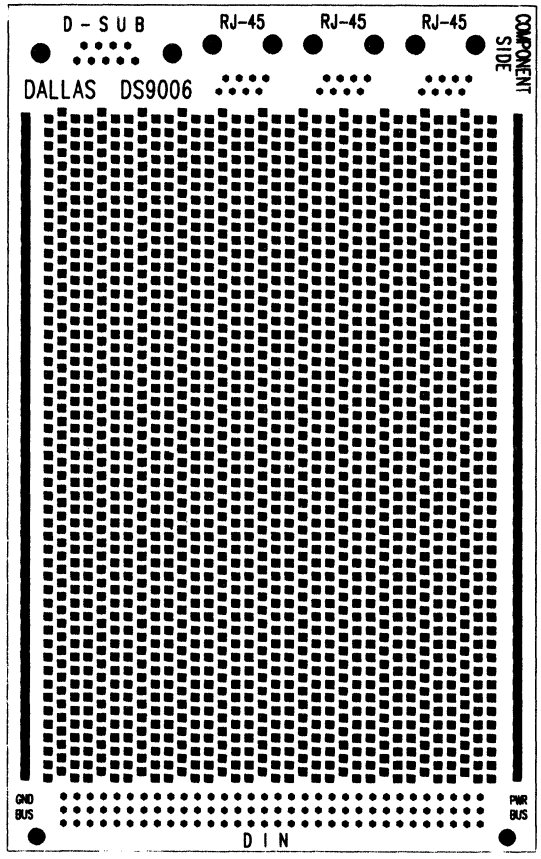
The DS9005 Eurocard Enclosure is a rugged, two-piece snap together plastic enclosure for any standalone system application. The PCB is offset in the enclosure to allow for components such as transformers and SIP Stiks to be positioned on the topside of the board while still leaving room for standard IC packages and discretes on the bottom side of the board. The housing is constructed of flame-retardant polyester PBT plastic to allow for applications requiring a very wide range of temperatures and is highly resistant to most chemicals. The size of the board and location of I/O connectors should match the DS9006 SIP Stik Motherboard. Applications include control units, handheld remote communications, and security systems.

DALLAS SEMICONDUCTOR

DS9006
SIP Stik Motherboard

FEATURES

- Fits into DS9005 Eurocard Enclosure
- Plated through-hole pattern for wire wrap or solder mount development
- Allowance for up to 12 Stik connectors
- Hole layout for RJ45, D-SUB, and Eurocard DIN connectors
- Full length buses for distributing power and ground
- 1700 hole array for 0.1" center ICs and Stiks



See Mech. Drawing – Sect. 16, Pg. 22

DESCRIPTION

The DS9006 SIP Stik Motherboard is a developmental printed circuit board for prototyping circuit designs which utilize Stik prefabs and/or RJ11/45 connector schemes. Many SIP Stiks mate with connectors that have staggered rows of pins. This makes it difficult to prototype these modules since most off-the-shelf wire wrap boards have a grid of 0.1" center holes. The DS9006 contains several rows of holes that are offset to accommodate both SIP Stiks and standard 300 mil and 600 mil DIPs.

Hole patterns for three RJ11/45, one 9-pin D-SUB, and 64/96-pin Eurocard connectors are located on the ends of the PCB in a right angle fashion to enable the finished circuit board assembly to mount in the DS9005 enclosure. This allows the designer to have a "complete" looking unit for presentation while still in the prototyping stage of design.

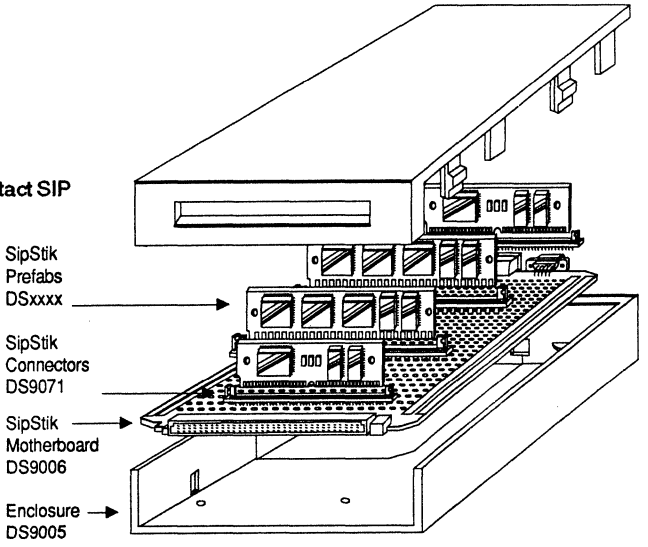
DALLAS SEMICONDUCTOR

DS9006K
SIP Stik Prototyping Kit

FEATURES

- DS9005 Eurocard Enclosure
- DS9006 SIP Stik Motherboard
- Sample connectors for 30–, 35–, and 40–contact SIP Stiks
- Adaptor pins for wire wrap
- Application note

3–D PACKAGING BOOSTS DENSITY



Eurocard Form Factor Shown. Stiks, RJ45, D–Sub, and DIN not included.

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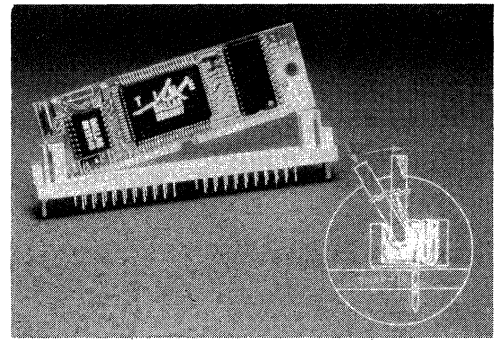
DESCRIPTION

The DS9006K SIP Stik Prototyping Kit includes a printed circuit board for prototyping SIP Stiks. The wire–wrapped unit can then be housed in a molded enclosure for standalone applications. An application note explains how to maximize use of th e DS9006 SIP Stik Motherboard printed circuit board using SIP Stiks. See data sheets for the DS9005 Eurocard Enclosure and DS9006 for more information on these items.

DALLAS SEMICONDUCTOR

DS907x
SIP Stik Connectors



FEATURES

- Provides snap–in connection between SIP Stiks and motherboard
- Provides 200 grams minimum contact force on JEDEC standard modules
- Redundant contacts
- Low insertion force
- Heat–resistant housing (rated at 200°C)
- .050" and .100" centerlines as specified in table below
- Reference AMP Inc. MICROEDGE™ SIMM connector catalog for more detailed specifications.

Part Number	Description	Ref. AMP Part #	Length (In.)
DS9071–30V	30 contact vertical position .100" pitch	821828–2	3.800
DS9071–30I	30 contact inclined position .100" pitch	821876–2	3.800
DS9071–35V	35 contact vertical position .100" pitch	821828–3	4.300
DS9071–35I	35 contact inclined position .100" pitch	821876–3	4.300
DS9071H–35R	35 contact high profile right angle position .100" pitch	3–382488–5	4.300
DS9072–40V	40 contact vertical position .050" pitch	821918–2	2.950
DS9072H–40R	40 contact high profile right angle position .050" pitch	4–382486–0	2.950
DS9072L–40R	40 contact low profile right angle position .050" pitch	4–382480–0	2.950
DS9072–68V	68 contact vertical position .050" pitch	821–824–7	4.350
DS9072–68I	68 contact inclined position .050" pitch	821–907–6	4.350
DS9072H–68R	68 contact high profile right angle position .050" pitch	6–382486–8	4.350
DS9072L–68R	68 contact low profile right angle position .050" pitch	6–382480–8	4.350
DS9072–72V	72 contact vertical position .050" pitch	821824–8	4.550
DS9072–72I	72 contact inclined position .050" pitch	821907–7	4.550
DS9072H–72R	72 contact high profile right angle position .050" pitch	7–382486–2	4.550
DS9072L–72R	72 contact low profile right angle position .050" pitch	7–382480–2	4.550

Also available are 40–position DIP–to–SIP and SIP–to–DIP adaptors for development of DS2250 Micro Stik products.

Part Number	Description
DS9075	SIP–to–DIP Adaptor 40 contact, horizontal DIP plug with 40 contact, low profile vertical position, .050 pitch SIMM connector
DS9076	DIP–to–SIP Adaptor 40 contact, .050 pitch, vertical SIMM edge card with 40 contact, vertical DIP socket.

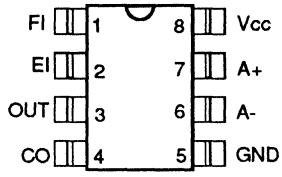
DALLAS SEMICONDUCTOR

DS1203S-B1
MicroPower Receiver Chip

FEATURES

- Input channel continuously listens for input signals up to 250 KHz
- Ultra low-power listening gives longevity to the 3-volt supply
- 25 mV P-P input signal drives output to supply levels
- Electronic freshness seal eliminates power consumption during storage
- Applications include RF, IR, or magnetic front end for wireless devices
- Space-saving; small outline surface mount package

PIN CONNECTIONS



8-PIN SOIC
(150 MIL)

See Mechanical Drawing
Section 16, pg. 5

PIN NAMES

Vcc	-	3-volt Supply
GND	-	Ground
FI	-	Freshness Input
EI	-	Enable Input
OUT	-	Signal Output
CO	-	Cycle Output
A+	-	Non-inverting Input
A-	-	Inverting Input

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DESCRIPTION

The DS1203S-B1 MicroPower Receiver Chip is an ultra low-power comparator circuit designed to listen for signals of up to 250 KHz. Input signals as small as 25 mV peak-to-peak are presented at the output as full power supply level signals. The DS1203S-B1 makes an ideal front end for wireless communication links via RF, IR, ultrasound or magnetic field. The ultra low power feature allows remote applications to be permanently powered by a single three-volt lithium energy source capable of lasting over ten years. A freshness seal can disconnect the power supply so that energy loss is avoided during periods of storage. The freshness seal is activated or deactivated through the use of a pulse packet protocol and the Freshness Input pin.

OPERATION

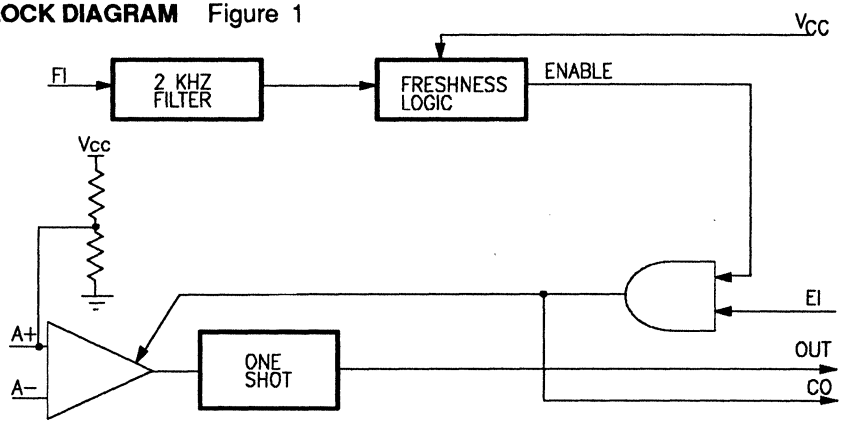
A block diagram of the DS1203S-B1 MicroPower Receiver Chip is shown in Figure 1. The device consists of a comparator which can be enabled by two sources. The enable input (EI) can be used to turn on the comparator directly, provided the freshness seal has been enabled. When the comparator is enabled, signals present at inputs A+ and A- of a magnitude greater than 25 mV peak-to-peak produce voltage swings between power supply input and ground at the output. In addition, the A+ input has a bias resistor of R_B approximately equal to 10M ohms to place the A+ pin at approximately $V_{DD}/2$. This facilitates differential reception.

FRESHNESS SEAL

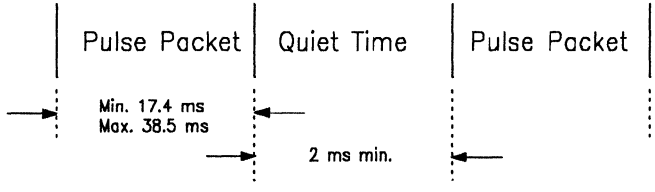
The freshness seal input pin (FI) is used to either stop or start DS1203S-B1 power consumption. This input accepts a pulse packet which is comprised of a series of pulses, representing either a logic 0 or a logic 1, separated by a 2-millisecond quiet time. Each pulse packet has a minimum aperture time of 17.4 milliseconds and a maximum aperture time of 38.5 milliseconds (see Figure 2). When the seal is broken, the comparator continuously listens for activity at the inputs. When the seal is intact, no listening occurs and the DS1203S-B1 enters a no-power consumption mode.

Within this aperture time, a logic 0 is represented as 32 to 47 pulses. A logic 1 is represented as 48 to 63 pulses. The type of pulse packet command, either a seal or a break, is illustrated in Figure 3.

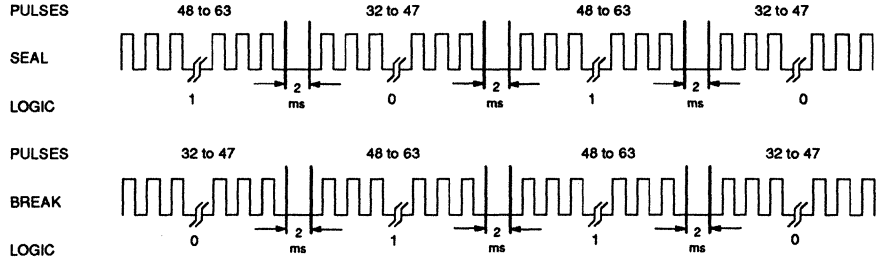
DS1203 BLOCK DIAGRAM Figure 1



FRESHNESS SEAL Figure 2



SEAL AND BREAK COMMAND Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	0.5V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.5	3.0	5.5	Volts	1
Input Logic 1	V_{IH}	2.0		V_{CC} +0.3	Volts	1, 2
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1, 2
Input Sensitivity	V_{SIN}	25	20		mVolts	
FI Input Logic 1	V_{IHF}	2.0		V_{CC} +0.3	Volts	1
FI Input Logic 0	V_{ILF}	-0.3		0.4	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=2.5 to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		1.0	µA	
Output Logic 1	V_{OH}	V_{CC} -0.3			Volts	1
Output Logic 0	V_{OL}			0.4	Volts	1
Operating Current	I_{CC}			3	µA	5
Power Down Current	I_{CC1}			50	µA	3
Output Current Logic 1	I_{OH}			250	µA	
Output Current Logic 0	I_{OL}			500	µA	
Propagation Delay	t_{PD}			30	µS	4
Comparator Sensitivity	V_{SINE}	25	20		mVpk-pk	6
Comparator Frequency	C_{FREQ}	0		250	KHz	
Comparator Input Resistance	R_{IMP}	1			M ohm	
Input Capacitance	C_{IMP}			5	pF	

NOTES:

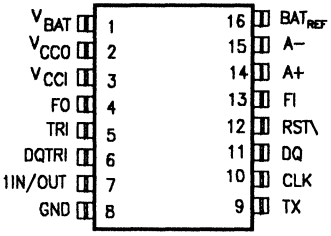
1. All voltages are referenced to ground.
2. Applies to the EI pin only.
3. Power drain from Vcc input when freshness seal is enabled; 2 µA when freshness seal is broken.
4. Propagation delay from comparator inputs to output.
5. Only for V_{CC}< 3.5 volts.
6. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.

DALLAS SEMICONDUCTOR

DS1209S-B1
Wireless to 3-Wire Converter Chip

FEATURES
- Adapts a wireless device to a 3-wire serial port (DQ, CLK, and RST\ signals)
- Up to 65,536 devices can be uniquely addressed within the same wireless proximity
- Receives IR, RF, or magnetic pulses as small as 25 millivolts peak-to-peak and frequencies up to 250 KHz
- Low-power operation for both battery backup and battery operate modes
- Makes allowances for extra or missing pulses induced by noise in transmission path
- Counts input pulse packets to interpret data and commands
- Internal state machine generates commands and routes data to and from the 3-wire serial port
- Output pin can gate a variety of transmitting devices
- Simplex 1-wire port can override comparator inputs for input/output to 3-wire serial port
- 3-wire serial port connects to large family of products: DS1201 Electronic Tag, DS1204U Electronic Key, DS5000 Soft Microcontroller, DS1280 3-Wire to Bytewide Converter Chip

PIN CONNECTIONS



16-PIN SOIC
(300 MIL)

See Mechanical Drawing Section 16, pg. 6

PIN NAMES (\ Denotes Condition Low)

BAT_{REF}	Battery Reference
V_{BAT}	Battery Input
V_{CCO}	Switched Output
V_{CCI}	+5V Input
1IN/OUT	1-Wire Input/Output Port
GND	Ground
TRI	Tri-state DQ, CLK, RST\ Input
DQ TRI	Tri-state Only DQ Input
TX	Wireless Transmit
RST\	RESET (3-Wire Port)
CLK	Clock (3-Wire Port)
DQ	Data Input/ Output (3-Wire Port)
FI/FO	Freshness Seal Input/Output
A+	Non-Inverting Comparator Input
A-	Inverting Comparator Input

DESCRIPTION
The DS1209S-B1 Wireless to 3-Wire Converter Chip is a low-power CMOS device designed to implement an addressable, full-duplex wireless to 3-wire communications channel. An internal state machine interprets pulse packets which are received at the comparator input pins and routes data to and from the 3-wire serial port. The TX output pin provides a return transmission link for data received from the 3-wire serial port and can gate a variety of transmitting devices. The low-power input comparator, internal to the DS1209S-B1, is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz. The DS1209S-B1 also contains a 16-bit chip select value which is stored in the internal command prefix register. This chip select value allows up to 65,536 devices to be uniquely addressed within the same wireless proximity. The 1-wire input/output pin can be used to override the comparator inputs and allow a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. Additionally, a sophisticated power switching circuit is provided which allows for both battery backup and battery operate modes.

PIN DESCRIPTIONS

V_{BAT} - This input is designed to be connected to a battery with a voltage range between 2.5 and 4.0 volts. When V_{CCI} is grounded, the DS1209S-B1 acts as a battery-operated device and power is supplied from the V_{BAT} pin at all times. This input should NEVER be grounded. If single supply operation is selected, this pin MUST be the power input for the device.

V_{CCI} - This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to the V_{CCO} pin as long as V_{CCI} is greater than V_{BAT}. However, when V_{BAT} is the greater, its voltage will be output. When both V_{CCI} and V_{BAT} inputs are used, the DS1209S-B1 is in the battery backup mode. V_{CCI} should be grounded when not being used.

V_{CCO} - Switched V_{BAT} or V_{CCI} output. V_{CCO} will always be the greater of V_{BAT} or V_{CCI}.

BAT_{REF} - This output pin represents the battery voltage input (V_{BAT}) less 0.6 volts. It is designed to be connected to the battery input pin on the attached 3-wire device.

1IN/OUT - This input/output pin provides an override for the comparator inputs and allows a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. The pin acts as an input pin for pulse packets containing both command and data input to the 3-wire serial port. Data is also output on the same pin when memory content is read via the 3-wire serial port.

FI/FO - The FI (Freshness In) and FO (Freshness Out) pins combine to give the DS1209S-B1 a method of conserving battery power until placed in service and determine if the low power consumption mode has been entered. The FI pin is used to start (break freshness seal) or stop (enable freshness seal) the continuous power consumption of the comparator on the DS1209S-B1 that is connected to the comparator input pins A+ and A- (Figure 6).

A+,A- - These are the inputs for the low-power comparator.

TRI - This input is used to tri-state the 3-wire outputs CLK, RST\, and DQ. The TRI pin is active in a high state.

DQ TRI - This input is used to tri-state the 3-wire DQ pin only. The DQ TRI pin is active in a high state.

TX - This output pin contains the data which is output from the 3-wire serial port. In a typical application this pin is used to key the wireless transmitter which will send data back to a wireless receiver.

RST - This output signal is the reset signal for the 3-wire serial port. When RST\ is at high level, the 3-wire port is active and data can be written into or read from the port.

CLK - This output signal is the clock signal for the 3-wire serial port. The clock signal synchronizes data into and out of the DQ line of the 3-wire serial port.

DQ - This input/output is the data input/output for the 3-wire serial port. In a typical application, RST\, CLK, and DQ connect directly to the RST\, CLK, and DQ pins on the DS1204 Electronic Key, DS1201 Electronic Tag, DS1207 TimeKey, or DS1280 3-Wire to Bytewide Converter Chip.

GND - This pin is the ground.

OPERATION

The principle blocks of circuitry contained within the DS1209B-S1 are shown in Figure 1. During normal input conditions, pulse packets present at the comparator input pins pass through the input selector to the pulse counter. The 1-wire port is selected for data input by exception when data is present at the 1-wire port. This data will override the comparator inputs. The 1-wire port pin will be discussed in more detail later in this text. Input pulses arriving at the pulse counter are deciphered into various command codes which affect the command prefix shift register, the state machine, and ultimately the 3-wire serial port. The various command codes are listed in Table 1.

Pulse packets are input to the pulse counter with a 50 μs dead time after the last pulse in each packet. The DS1209S-B1 uses the dead time to determine how many pulses were sent and the action to be taken. In addition, if input to the pulse counter is low (inactive) for longer than 1.5 mS, the DS1209S-B1 will time out, reset the command prefix shift register, and place the state machine into an inactive state.

As can be seen in the block diagram of Figure 1 and the command codes listed in Table 1, the input pulses are sent in two different directions. If a pulse packet of 100 pulses (greater than 90) arrives at the pulse counter, the next 24 pulse packets are sent to the command prefix shift register and the state machine is set inactive. The 100-pulse packet always sets the state machine to inactive regardless of any action which may have been occurring (aborts current action/conversation).

The 24 pulse packets which go to the command prefix shift register will cause a normal wake-up or mask wake-up, a read of the chip select bits, a write of the chip select bits, or a lock of the chip select bits. The chip select bits make up the first 16 bits of the 24-bit command prefix shift register. The last eight bits comprise the function field. See Figure 2 and Table 2.

NORMAL WAKE-UP AND MASK WAKE-UP

Wake-up refers to the sequence of 24 20- or 40-pulse packets received after a 100-pulse packet is sent to set the DS1209S-B1. The 24 pulse packets contain a 16-bit chip select and 8-bit function code which will cause the device state machine to become active. A normal wake-up requires all 16 chip select bits to be matched to those stored on the device before the device becomes active. A masked wake-up requires only a partial match, starting with the least significant bit pair (bit 0,1) and proceeding to the most significant bit pair left unmasked. For example, if the wake-up command (see Table 2) having function code 00011101 -- "mask CS bits 10-15" -- is issued to the DS1209S-B1, then chip select bits 0 through 9 must be correctly matched before the device will become active. The following step-by-step procedure will illustrate normal and mask wake-up:

1. First, a 100-pulse packet is sent to the comparator input pins, which puts the state machine into an inactive state.

2. Issue wake-up or mask wake-up by sending the 8-bit function code followed by the 16 chip select bits to enable the state machine. The command prefix register is always loaded by sending write zeros (20-pulse packets) or write ones (40-pulse packets). The loaded pulse packets are compared to values stored in the 8-bit Function Code Table and the previously stored 16 chip select bits (storing the chip select values will be covered later).

Pulse packets of 50 to 89 pulses are ignored when loading the command prefix shift register. A pulse packet of greater than 90 pulses always initializes the command prefix shift register back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wake-up is decoded, the command prefix shift register will no longer allow data bits to be written into it and the enable output will become active and remain active until another 100-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corresponding to the number of pulses received as shown in Table 1.

A pulse packet of 80 pulses, followed by a 20-pulse packet, followed by a 40-pulse packet, enables the beacon mode of the state machine. Beacon mode turns on and off the TX pin at a 5 KHz rate for 1.2 seconds. In a typical application utilizing the DS6065A, this signal can be used to key a transmitter (the DS6065A operates at 303.875 MHz), which allows a base unit to lock onto the transmitted beacon.

3. The DS1209S-B1 is now placed in the active state by issuing a 60-pulse packet which takes RST\ high on the 3-wire serial port. This same 60-pulse packet also turns off the beacon if it has not already timed out. With RST\ high, a conversation can now take place between devices placed on the 3-wire port (DS1201, DS1204U, DS1207, or DS1280) from the comparator inputs, and data is returned to the sending unit via the TX pin. As pulse packets continue to be received, the device attached to the 3-wire port will be written and read using 20- and 40-pulse packets and reset with a 60-pulse packet. The reset pulse packet will take RST\ low until the next pulse packet is detected after the 50 us dead time. When data is read from the 3-wire port, it is always sent to the TX pin for transmission back to the sending unit.

4. If an 80-pulse packet is received, the state machine will go to an inactive state but still remains alert for new pulse packets.

5. If no pulse packets are received for more than 1.5 mS, the DS1209S-B1 will time out, initialize the command prefix shift register, and set the state machine back to the inactive state. The DS1209S-B1 now waits for new inputs to the protocol serial shift register which begin with a 100-pulse packet.

READING THE CHIP SELECT BITS

The 16-bit chip select (CS) value stored in the command prefix shift register can be determined in several ways. In fact, an exhaustive search could be implemented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 2^{16} possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the unmasked chip select fields as each set of bits is identified. However, the simplest method of determining the 16-bit CS value is to read the 16-bit value directly. The following step-by-step procedure will illustrate how to read the chip select bits.

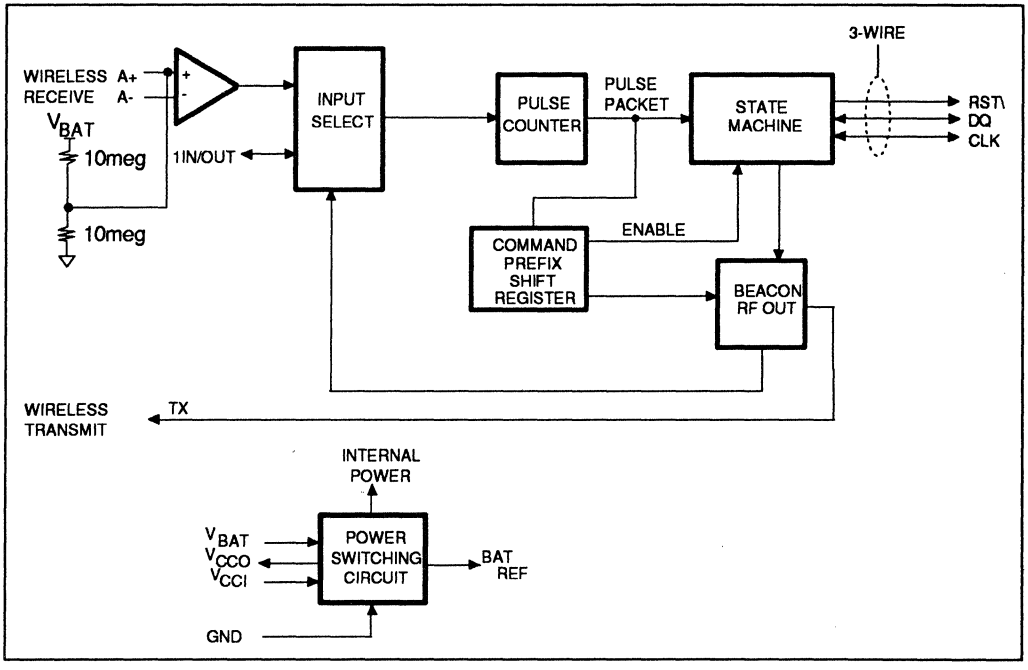
1. Wake up the DS1209S-B1 by using the mask all function code. This is accomplished by sending a 100-pulse packet followed by 24 20-pulse and 40-pulse packets. The first eight pulse packets must match the mask all function code. The last 16 pulse packets can be any combination of 20- and 40-pulse packets as the 16 CS bits are masked. Next, the beacon mode of the state machine is enabled by sending an 80-pulse packet followed by a 20- and then a 40-pulse packet. If the beacon mode has been enabled, it should be disabled after receiver lock-on by sending a 60-pulse packet to the comparator inputs.

B1 COMMAND CODES Table 1

Number of Pulses			Command
Min.	Typ.	Max.	
5	20	29	Write 0 or READ
30	40	49	Write 1
50	60	69	Take RST\ High
70	80	89	Return to Inactive State
90	100	109	Initialize Protocol and Put State Machine Inactive

NOTE: Pulse packets are sent with a minimum of 50 µs quiet time after each pulse packet and a maximum quiet time of approximately 1.5 ms.

DS1209S-B1 BLOCK DIAGRAM Figure 1



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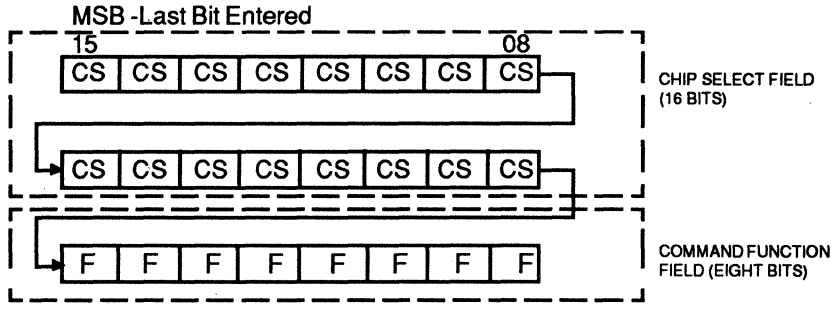
24-BIT COMMAND PREFIX SHIFT REGISTER BIT PATTERN Figure 2



B1 FUNCTION CODES Table 2

FUNCTION	MSB			FUNCTION CODE				LSB	RESULTS
Wakeup	0	0	0	1	1	0	0	0	Mask All Bits
Wakeup	0	0	0	1	0	0	0	1	Mask CS Bits 2-15
Wakeup	0	0	0	1	0	0	1	0	Mask CS Bits 4-15
Wakeup	0	0	0	1	1	0	1	1	Mask CS Bits 6-15
Wakeup	0	0	0	1	0	1	0	0	Mask CS Bits 8-15
Wakeup	0	0	0	1	1	1	0	1	Mask CS Bits 10-15
Wakeup	0	0	0	1	1	1	1	0	Mask CS Bits 12-15
Wakeup	0	0	0	1	0	1	1	1	Mask CS Bits 14-15
Wakeup	0	0	1	0	1	0	0	0	Use all CS Bits
Read CS Bits	0	0	1	0	1	0	1	1	Ignore CS Bits
Store CS Bits	0	0	1	0	1	1	0	1	Use all CS Bits
Lock CS Bits	0	0	1	0	1	1	1	0	Use all CS Bits

2. Now load the DS1209S-B1 command prefix shift register with the read CS bits function code. This is accomplished by sending a 100-pulse packet followed by 24 20- or 40-pulse packets. As before, the first eight pulse packets must match the read CS bits function code. However, the last 16 pulse packets can be any combination of 20- and 40-pulse packets, as the 16 CS bits are ignored. During the 24-bit command prefix shift register load, pulse packets of 60 and 80 are ignored. As usual, pulse packets of 100 will initialize the command prefix shift register and set the state machine inactive.

3. If the 8-bit function code in the command prefix shift register is correctly matched, then for each 20-pulse packet (read command) received at the comparator input pins, one bit of the 16-bit CS field will be read at the TX pin, the LSB of the field appearing first. Thus, it will receive 16 packets of 20 pulses each to read the entire CS field. If more than 16 read pulse packets are sent to the comparator input pins in this mode, the DS1209S-B1 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 40, 60, or 80 pulses are ignored and 100-pulse packets will initialize the command prefix shift register and set the state machine inactive. This is a non-destructive read and can be aborted at any time during the read process.

4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 20- and 100-pulse packet are ignored by the state machine. As usual, the 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

STORING THE CHIP SELECT BITS

In order to store a new value into the chip select bits of the protocol shift register, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the procedure described in the "Reading Chip Select Bits" section. After obtaining the existing chip select values, a new value can be entered by using the step-by-step procedure which follows:

1. Load the proper 24-bit pattern into the command prefix shift register for storing the chip select bits. This pattern consists of 24 20-pulse and 40-pulse packets. The first eight packets must match the stored CS bits function code. The last 16 pulse packets must match the existing CS bits. During the 24-bit shift register load, only 20- and 40-pulse packets are accepted while 60- and 80-pulse packets are ignored. As always, 100-pulse packets will initialize the command prefix shift register and set the state machine inactive.

2. If the 8-bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 20-pulse and 40-pulse packets are accepted. Pulse packets of 60 and 80 are ignored and 100-pulse packets cause the stored CS bit command to abort, initializing the command prefix shift register and returning the state machine to inactive. The DS1209S-B1 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new packets will continue to shift in, storing the last 16 packets that are received.

3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 100-pulse packet, which will initialize the command prefix shift register and return the state machine to an inactive state. A timeout of 1.5 mS will have the same effect as a 100-pulse packet.

LOCKING THE CHIP SELECT BITS

The design of the DS1209S-B1 allows for both battery backup and battery operation. The device consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the command prefix shift register CS bits, are nonvolatile. A special latch is provided so that upon initial power up (when battery is first connected) the nonvolatile chip select bits can be written with a store CS function code.

The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip select bits cannot be changed until power is removed (battery disconnected) from the DS1209S-B1. The lock CS bit can be accomplished by the following step-by-step procedure.

1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.

2. The 8-bit function code for locking the CS bits is transmitted, followed by the 16-bit chip select value. Only 20- and 40-pulse packets are accepted; 60- and 80-pulse packets are ignored. A 100-pulse packet will cause the lock CS bits to abort, initializing the command prefix shift register and returning the state machine to the inactive state.

3. Once the 24-bit command prefix shift register is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.

4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock CS operation the main state machine is disabled so that all pulse

packets have no effect. As usual, a 100-pulse packet or a timeout of 1.5 mS will initialize the command prefix shift register and return the state machine to inactive.

POWER SWITCHING CIRCUIT

As shown in the block diagram of Figure 1, the DS1209S-B1 can receive its power from two different sources: the V_{CCI} input or the V_{BAT} input. The DS1209S-B1 is designed to work off of a battery supply as low as 2.5 volts. However, if an alternate supply is available, it can be connected to the V_{CCI} pin. A voltage level of 3 volts minimum is required on the V_{BAT} pin for proper operation. With both the V_{CCI} pin and the V_{BAT} pin attached to appropriate power sources, the DS1209S-B1 will automatically select the supply input which is the higher level. If only one power source is connected, it **MUST** be connected to the V_{BAT} input. The V_{REF} output is designed specifically to supply power to a connected 3-wire device such as a DS1204U, DS1201, DS1207, or DS1280. The V_{REF} output is equal to the V_{BAT} input less a voltage drop of about 0.5 volts. This pin is capable of sourcing a current of 2 mA.

PULSE PACKETS

The minimum time between pulse packets is 50 *us* and the idle time of 1.5 mS will always cause the protocol shift register to initialize and the state machine to go inactive.

Pulse packets range from 20 pulses to 100 pulses, depending on the action to be taken (see command codes in Table 1). If a read pulse packet is detected, data is to be read from a device connected on the 3-wire serial port and the TX pin will become active high for a logic 1 or remain low for a 0. Time is allotted beyond the 50 *us* between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 375 *us* window. If a logic 0 is being sent, the TX pin will remain low for the entire window. If a logic 1 is being sent, the TX pin will be driven to high level within a maximum of 75 *us* and will remain high for a minimum of an additional 150 *us*.

However, if a minimum of four pulses is received at the comparator inputs, the TX pin activity is terminated on the assumption that a logic 1 has been received and the sending unit has started the next pulse packet. The timing diagram of Figure 3 illustrates the comparator output and the TX pin timing relationship.

COMPARATOR OPERATION

The low-power comparator inputs are brought out to the user on the A+ and A- pins. The low- power input comparator is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz.

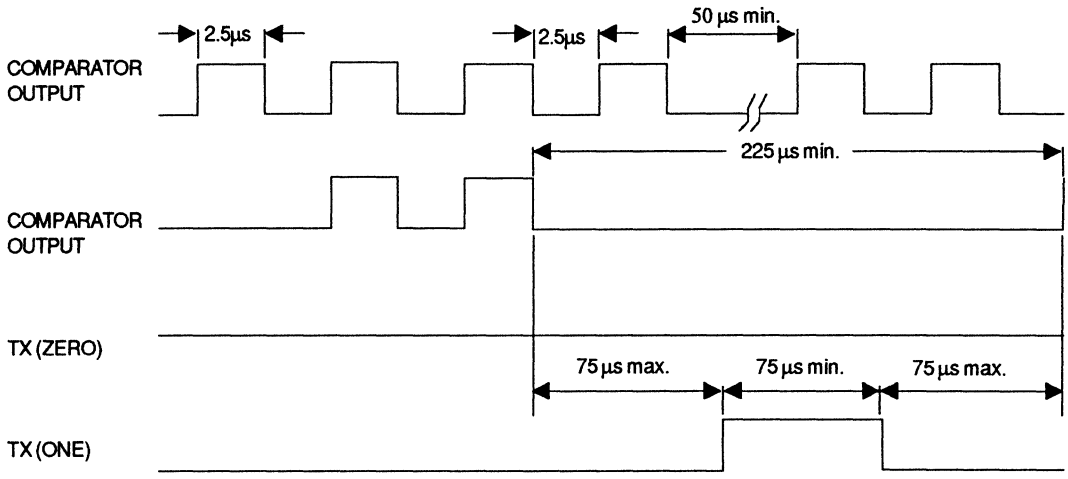
1IN/OUT

This pin is an input/output one-wire signal port designed to override the comparator input pins and multiplex the TX pin on a single connection. Data is input on the port pin using a frequency of one-half the comparator input frequency with a symmetrical high and low time of 5 *us* ± 20%. Therefore, the time between pulse packets is 2X the time allotted between pulse packets when 250 KHz is used. If a read pulse packet is detected, time is allotted beyond the 100 *us* between pulse packets for the DS1209S-B1 to send out a 1 or a 0. This time is specified as a 450 *us* window. If a logic 1 is being sent, the 1IN/OUT pin will remain low for the entire window. If a logic 0 is being sent, the 1IN/OUT pin will be tri-stated to a high impedance state by the DS1209B and should be pulled high using a pullup resistor. This high impedance state will occur within a maximum of 150 *us* and remain for a maximum of 150 *us*. The 1IN/OUT pin is guaranteed to be inactive after a third 150 *us* time period. The timing diagram of Figure 4 illustrates the 1IN/OUT timing.

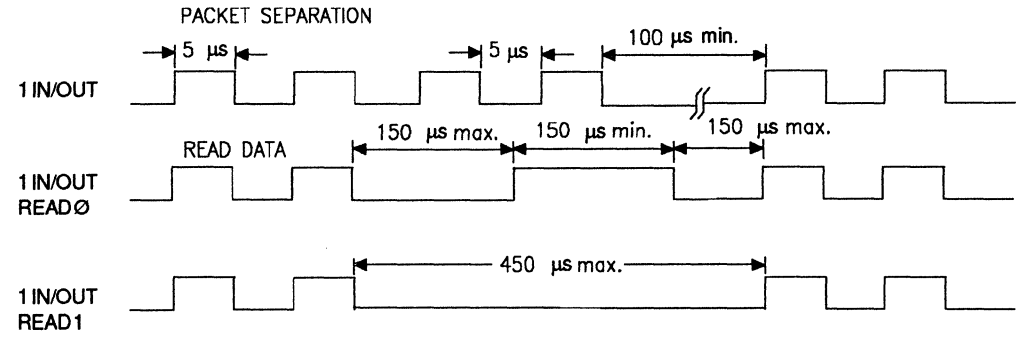
RST\, CLK, AND DQ

The 3-wire serial port on the DS1209S-B1 consists of the RST\, CLK, and DQ signals. These signals are designed to connect directly to the CLK, RST\, and DQ lines of various 3-wire devices, such as the DS1204U, DS1207, DS1201, or DS1280. The RST\ pin on the DS1209S-B1 is driven to a high level whenever a 60-pulse packet is received by the state machine. The RST\ signal remains high until a 80- or 100-pulse packet is received or until 1.5 mS has elapsed without activity at the comparator inputs. The CLK pin on the DS1209S-B1 is normally high until the RST\ signal is high. When RST\ is high and a 20- or 40-pulse packet is received by the state machine (indicating a "read from" or "write to" the 3-wire port), the CLK pin is driven low for a period of 500 ns minimum to 1.0*us* maximum. If data is being read from a device on the 3-wire serial port, it will become valid within 200 ns of the falling edge of the clock returned to the sending unit. The output will be a high level for a logic 1 or remain at low level for a logic 0. If data is being written to a device on the 3-wire serial port, then data will be sent from the state machine to the DQ line prior to the falling edge of the clock. This data will remain valid until the clock transitions back to a high level. The TX pin remains low while data is being written to the 3-wire serial port. A timing diagram for the 3-wire serial port is shown in Figure 5. For more detailed information on the 3-wire serial port, see the data sheets on the DS1201, DS1207, or DS1280.

COMPARATOR INPUT TIMING Figure 3



1IN/OUT TIMING Figure 4



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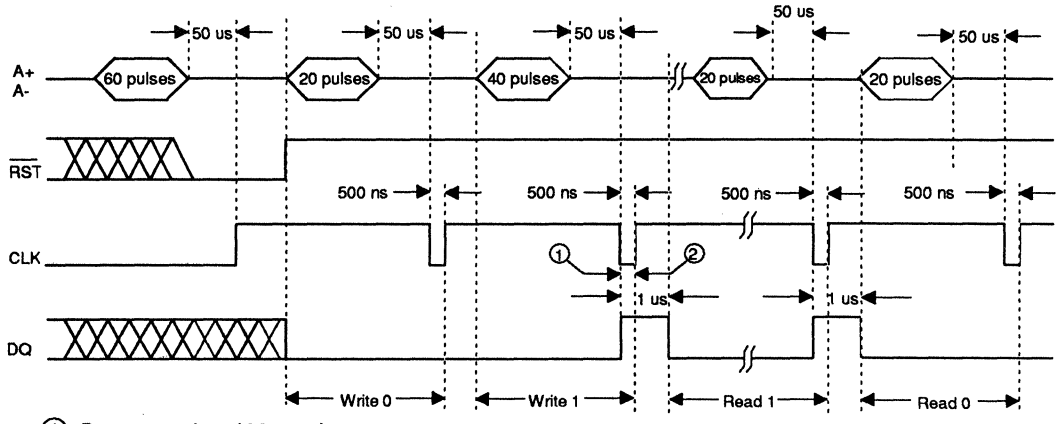
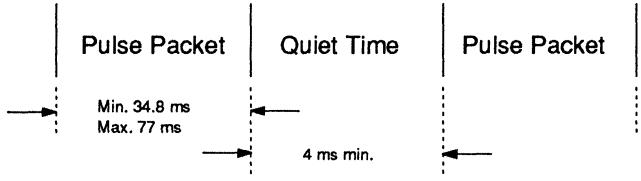
RST\, CLK, AND DQ TIMING Figure 5



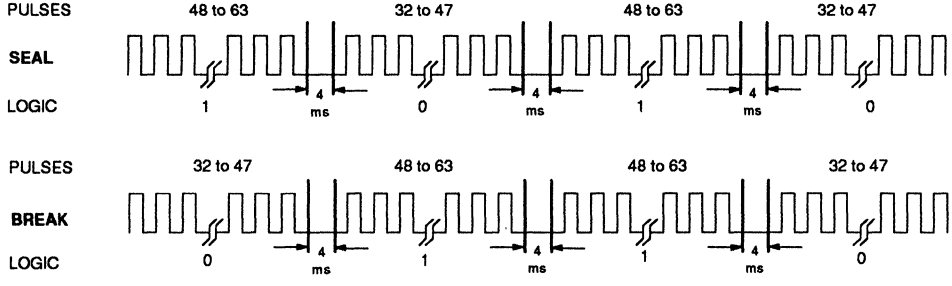
① Data setup time:100 ns min.

② Data hold time: 100 ns max.

FRESHNESS SEAL Figure 6



SEAL AND BREAK COMMAND



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to Ground	0.5V to +7V
Storage Temperature	-55° to +125°C
Operating Temperature	0° to 70° C
Soldering Temperature	260° for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Input	V_{CCI}	3.0	5.0	5.5	Volts	1,2
Battery input	V_{BAT}	2.5		4.0	Volts	1,2
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,3
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, V_{BAT} =3 V, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Reference	V_{REF}	V_{BAT} -0.7		V_{BAT}	Volts	1
Switched Voltage Out	V_{CCO}	V_{CCI} -0.3			Volts	1,4
Switched Current Out	I_{CCO}	3	4		mA	5
Operating Current	I_{CC}		2	75	uA	6
Standby Current	I_{cc1}			2	uA	7
Output Logic 1	V_{OH}	V_{CC} -10%			Volts	1,3
Output Logic 0	V_{OL}			0.4	Volts	1
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Comparator Leakage Current	I_L	-1.0		1.0	uA	8
Comparator Sensivity	V_{SINE}	25	20		mV	9
Comparator Frequency	C_{FREQ}	40		250	KHz	
Comparator Input Resistance	R_{IMP}	1			M ohm	
Input Capacitance	C_{IO}			5	pF	

NOTES:

1. All voltages are referenced to ground.
2. When both the battery and supply pins are being used, V_{CCI} should be at least 500 mV higher than V_{BAT} when V_{CCI} is supplying power.
3. V_{CC} applies to the greater of V_{CCI} or V_{BAT} depending on which input is supplying power.
4. V_{CCO} is either V_{CCI} -0.3 V or V_{BAT} -0.3 V.
5. I_{CCO} is current coming from V_{BAT} or V_{CCI} depending on which input is supplying power.
6. Operating current comes from V_{CCI} or V_{BAT} depending on which is supplying power and if power is consumed by the DS1209S-B1 when comparator or 1-wire is active.
7. With freshness seal not broken, receiver standby current is 50 nA.
8. Leakage current applies to all inputs except V_{CCI} and V_{BAT}. 1 IN/OUT, TRI, and DQTRI have 150 µA max. leakage to ground.
9. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.

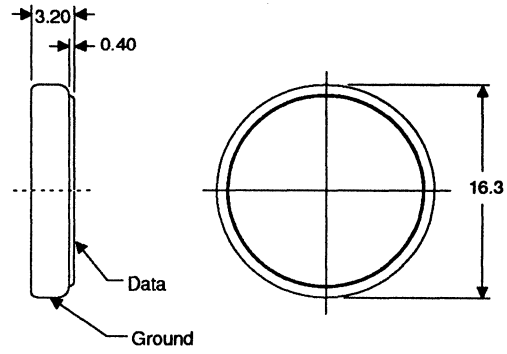
PRELIMINARY

DALLAS SEMICONDUCTOR

DS1990
Touch Serial Number

DS1990 SPECIAL FEATURES
- Unique 48-bit serial number
- Low-cost electronic key for access control
- 8-bit CRC for checking data integrity
- Can be read in less than 5 msec
- Operating temperature range: -40 to +85° C

TOUCH FAMILY FEATURES
- Electronic identification by momentary contact
- Chip-based data carrier compactly stores information
- Can be accessed while affixed to object
- Economically communicates to host with a single digital signal
- Standard 16mm diameter and 1-Wire protocol ensure compatibility with Touch Memory family
- Coin-shape is self-aligning with mating receptacles
- Durable stainless steel case resists environmental hazards
- Unique, factory-lasered 48-bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing
- Presence detect signal announces connection to host



Dimension Tolerance: ±.005
(All dimensions shown in millimeters)

R3 PACKAGE

CONTACTS		
	Rim	Ground
	Inner Face	Data

ACCESSORIES	
DS9092	Touch Memory Probe, Hand-Grip or Panel Mount
DS9093	Touch Memory KeyRing Mount
DS9094	Touch Memory Clip
DS9096	Self-Stick Adhesive Pad

ORDERING INFORMATION	
DS1990-R3	R3 Package

DESCRIPTION

The DS1990 Touch Serial Number is a rugged data carrier that acts as an electronic serial number for automatic identification. The DS1990 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return.

The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1990 to be easily used by human operators. Accessories permit the DS1990 to be mounted on plastic key fobs, photo-ID badges, printed-circuit boards or any smooth surface of an object. Applications include access control, work-in-progress tracking, tool management and inventory control.

OPERATION

The DS1990's internal ROM is accessed via a single data line. The 48-bit serial number, family code and CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

1-Wire Protocol

The 1-Wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1990 is a slave device. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence. For a more detailed protocol description, refer to Application Note #23, "Using the 1-Wire Protocol."

Hardware Configuration - The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection. The DS1990 is an open drain part with an internal circuit equivalent to that shown in Figure 2. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 3. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

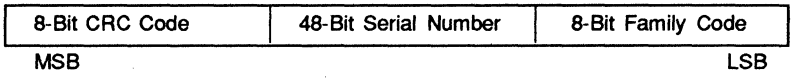
The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 uS, all of the slave devices on the bus will be reset.

Transaction Sequence

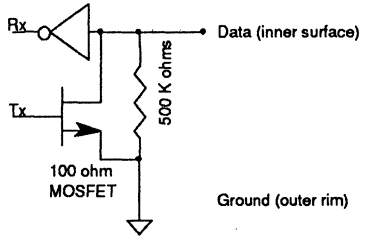
The sequence between the bus master and the DS1990 is as follows:

Reset
Presence Detect
1-Wire Command Word
Family Code
48-Bit Serial Number
CRC Byte

DS1990 MEMORY MAP Figure 1

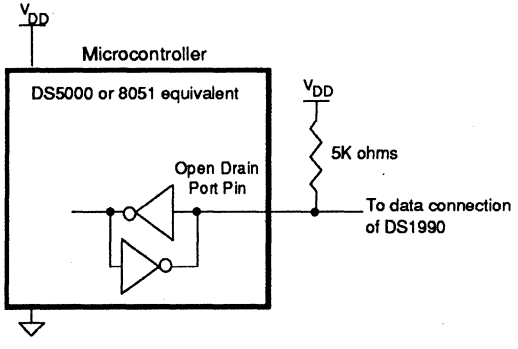


DS1990 EQUIVALENT CIRCUIT Figure 2

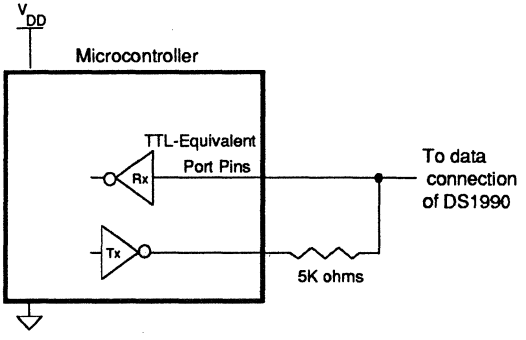


BUS MASTER CIRCUIT

Open Drain Figure 3A



Standard TTL Figure 3B



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Reset/Presence Detect - All transactions on the 1-Wire bus begin with a reset. The DS1990 is reset by holding the data line low for more than 480µS. (When the DS1990 is not connected to the bus, it is held in reset by an internal pull-down, but when connected to the bus, the data line is pulled high and the part is taken out of reset and is ready to issue its presence detect.)

After detecting a high data line, the DS1990 waits 15µS minimum and issues its presence detect. This presence detect is a low-going pulse that lasts a minimum of 60µS. This response to the reset pulse lets the bus master know that the DS1990 is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from the noise as devices are taken on and off the bus. Refer to the timing diagram in Figure 4.

After the DS1990 has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1µS. This 1µS interval is like a frame sync. After each bit is transmitted on the bus, there is a frame pulse to sync up for the next transmission.

Once the bus master has detected a presence on the bus, it transmits the read command 0Fh to the DS1990 LSB first. This will set the DS1990 into the transmit mode.

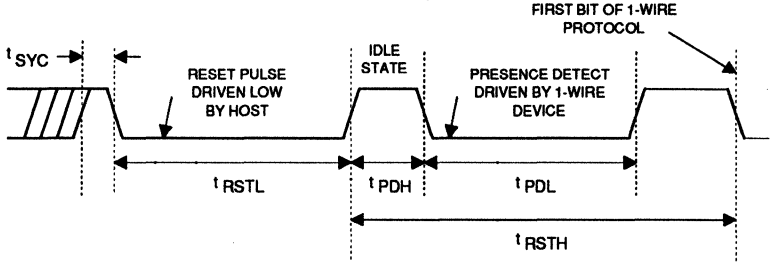
After receipt of the read command, the DS1990 will send back, in order, the 8-bit family code (01h for the DS1990), the 48-bit serial number and the 8-bit CRC, with the LSB of each field sent first.

Transmitting /Receiving Data

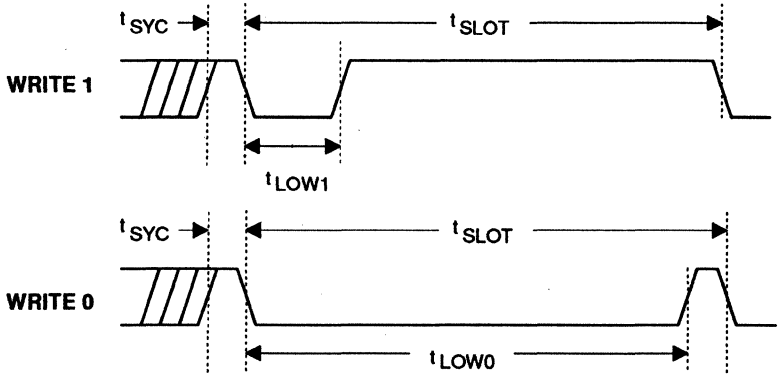
All communications on the 1-Wire bus begin with the reset and presence detect sequence. The bus master then transmits the 1-Wire read command to tell the DS1990 to get ready to transmit data. To transmit the first bit of the Read command word, the master pulls the bus low for 1µs. This low-going edge informs the DS1990 that the first bit is being sent. After 1µS, the master does one of two things:

1) Holds the line low for an additional 60µS to output a zero (write a 0) or,
2) Lets the bus go high for an additional 60µS (write a 1).

1-WIRE RESET/PRESENCE DETECT TIMING Figure 4



1-WIRE WRITE TIMING Figure 5



The state of the bus during this 60µS time phase determines the value of the bit. This process is repeated until all eight bits are transmitted. Refer to the timing diagram in Figure 5.

The bus master now reads in order, LSB first of each field, the family code, serial number and CRC. A read cycle is similar to a write cycle. It is started with the bus master pulling the bus low for 1µS. This informs the DS1990 that it should have its data on the bus no later than the 1µS from the falling edge. After the 1µS, the bus master lets go of the bus and lets the DS1990 drive the bus. The DS1990 must then hold the data on the bus for an additional 14µS minimum (59µS maximum). During this holding time, the bus master reads the state of the bus.The bus master should read data from the bus within 15µS after the falling edge. The entire cycle for a bit lasts a minimum of 60µS (120µS maximum) from the falling edge. At the end of the cycle, the bus master must drive the bus high for 1µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 6 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1990 must be reset.

CRC GENERATION

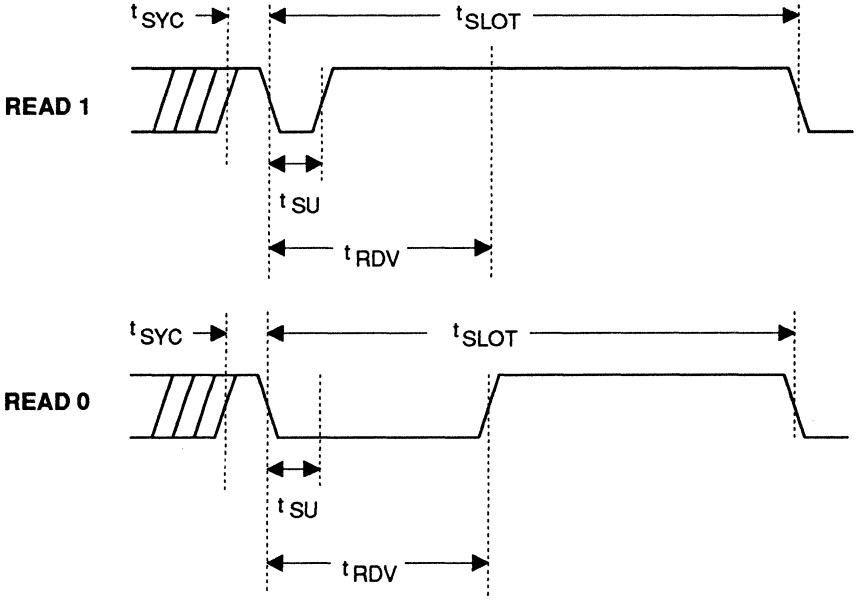
To validate the data transmitted from the DS1990, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1990. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but *not* over the stored CRC value itself. If the two CRC values match, the transmission is error-free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the 5000 Soft Microcontroller which is compatible with the 8031/51 Microcontroller family. The procedure DO_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. It should be noted that the variable CRC needs to be initialized to 0 before the procedure is executed. Each byte of the data is then placed in the accumulator and DO_CRC is called to update the CRC variable. After all the data has been passed to DO_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is :

$$CRC = x^8 + x^5 + x^4 + 1$$

For more details, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

1-WIRE READ TIMING Figure 6



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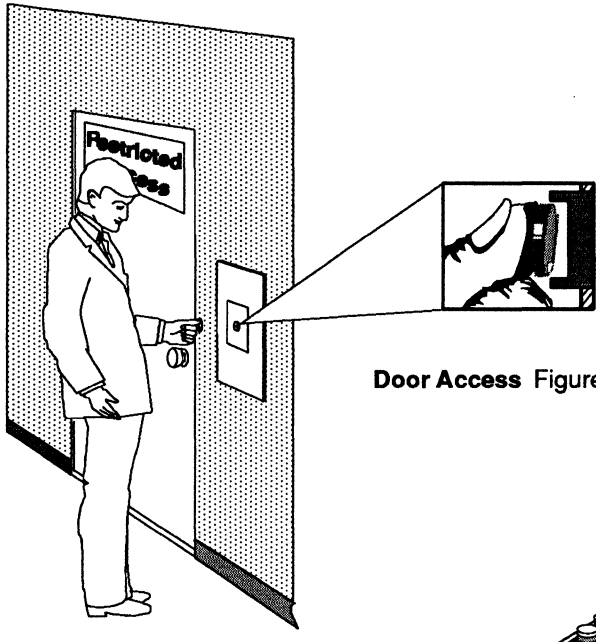
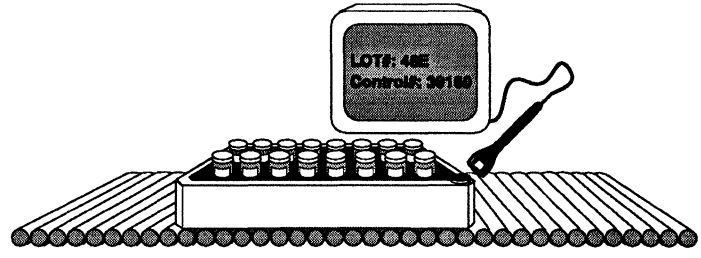
CRC ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC             ; save the accumulator
            PUSH    B               ; save the B register
            PUSH    ACC             ; save bits to be shifted
            MOV     B,#8            ; set shift = 8 bits
                                    ;
CRC_LOOP:   XRL     A,CRC           ; calculate CRC
            RRC     A               ; move it to the carry
            MOV     A,CRC           ; get the last CRC value
            JNC     ZERO            ; skip if data = 0
            XRL     A,#18H          ; update the CRC value
                                    ;
ZERO:       RRC     A               ; position the new CRC
            MOV     CRC,A           ; store the new CRC
            POP     ACC             ; get the remaining bits
            RR      A               ; position the next bit
            PUSH    ACC             ; save the remaining bits
            DJNZ    B,CRC_LOOP      ; repeat for eight bits
            POP     ACC             ; clean up the stack
            POP     B               ; restore the B register
            POP     ACC             ; restore the accumulator
            RET
```

DS1990 APPLICATIONS



Door Access Figure 7A



Inventory Control Figure 7B

ABSOLUTE MAXIMUM RATINGS*

Voltage On Data Pin Relative to Ground	-0.5V to +7V
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to 85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5		5.5	Volts	1
Pull-up Voltage	V_{PUP}	4.5		5.5	Volts	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V + 10%, -40°C to 85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5		0.4	Volts	6
Input Logic High	V_{IH}	3.0	5.0	5.5	Volts	4, 6
Output Logic Low @ 4mA	V_{OL}			0.4	Volts	6
Output Logic High	V_{OH}			5.5	Volts	6
Input Resistance	R_I		500K		Ohms	2
Operating Charge	I_{OP}			30	nC	5,6

AC ELECTRICAL CHARACTERISTICS

(-40°C to 85°C, V_{IH} = 5V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t_{SLOT}	60		120	µS	
Write 1 Low Time	t_{LOW1}	1		15	µS	
Write 0 Low Time	t_{LOW0}	60		120	µS	
Read Data Valid	t_{RDV}			15	µS	
Read Data Setup	t_{SU}	1			µS	7
Frame Sync	t_{SYC}	1			µS	
Reset Low Time	t_{RSTL}	480			µS	3
Reset High Time	t_{RSTH}	480			µS	
Presence Detect High	t_{PDH}	15		60	µS	
Presence Detect Low	t_{PDL}	60		240	µS	

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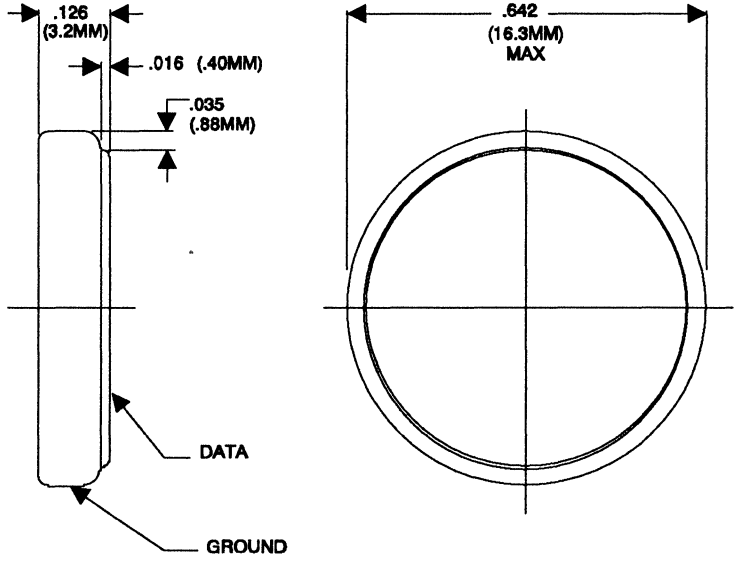
NOTES:

1. All voltages are referenced to ground.
2. Input is pulled to ground.
3. An additional reset or communications sequence cannot begin until the reset high time has expired.
4. V_{IH} is a function of the external pull-up resistor and the V_{CC} supply.
5. 30 nanocoulombs per 72 time slots @ 5.0V.
6. @V_{CC} = 5.0 volts with a 5K pull-up to V_{CC} and a maximum time slot of 120µs.
7. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1µS of this falling edge and will remain valid for 14µS minimum (15µS total from falling edge on 1-Wire).

DS1990 TOUCH SERIAL NUMBER

R3 PACKAGE



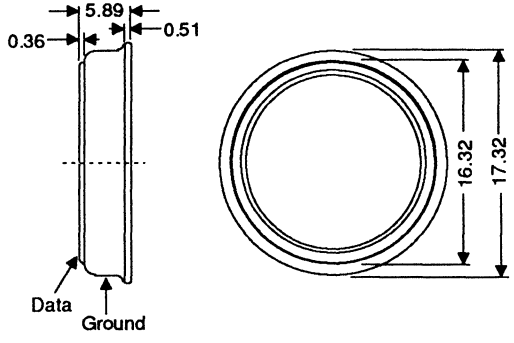
DIMENSION TOLERANCE : ±.005

DALLAS SEMICONDUCTOR

DS1991
Touch MultiKey

DS1991 SPECIAL FEATURES
- 1,152-bit secure read/write, nonvolatile memory
- Secure memory cannot be deciphered without matching 64-bit password
- Memory is partitioned into 3 blocks of 384 bits each
- 64-bit password and ID fields for each memory block
- 512-bit scratchpad ensures data transfer integrity
- Operating temperature range: -20° to +70° C
- Over 10 years of data retention

TOUCH MEMORY FEATURES
- Electronic identification by momentary contact
- Chip-based data carrier compactly stores information
- Can be accessed while affixed to object
- Economically communicates to host with a single digital signal
- Standard 16mm diameter and 1-Wire protocol ensure compatibility with Touch Device family
- Coin shape is self-aligning with mating receptacles
- Durable stainless steel case resists environmental hazards
- Unique, factory-lasered 48-bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing or snap-in flange
- Presence detect signal announces connection to host



(All dimensions shown in millimeters)

F5 PACKAGE

CONTACTS		
	Rim	Ground
	Inner Face	Data

ACCESSORIES	
DS9092	Touch Memory Probe, Hand-Grip or Panel Mount
DS9093F	Touch Memory KeyRing Mount
DS9094F	Touch Memory Clip
DS9096	Self-Stick Adhesive Pad

ORDERING INFORMATION	
DS1991L-F5	10 year expected life, flanged rim, 5.89mm thickness

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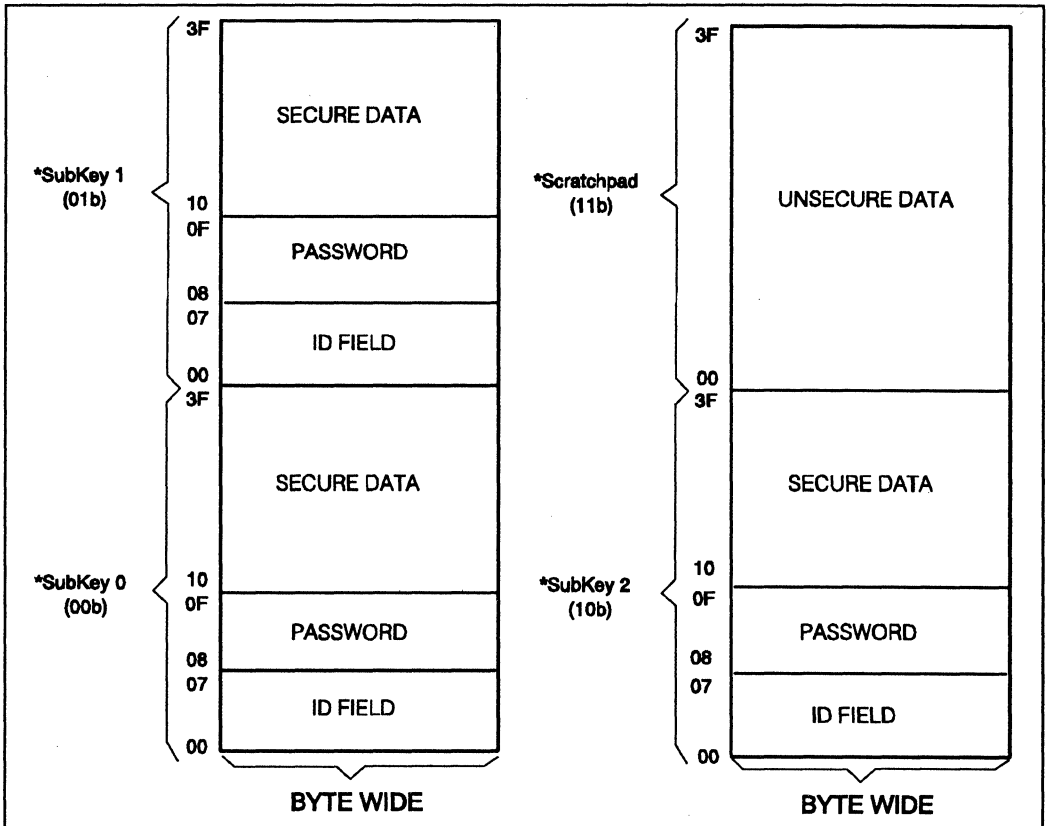
DESCRIPTION
The DS1991 Touch MultiKey is a rugged data carrier that acts as three separate electronic keys, offering 1,152 bits of secure, read/write nonvolatile memory. Each key is 384 bits long with distinct 64-bit password and public ID fields. The password field must be matched in order to access the secure memory. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return.

The 512-bit scratchpad serves to ensure integrity of data transfers to secure memory. A 64-bit factory-lasered ROM provides a unique identity to each DS1991, with an 8-bit family code, a 48-bit serial number, and an 8-bit CRC. The family code for the DS1991 is 02h. in order to access the secure memory. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground

MEMORY MAP Figure 1



***NOTE:** Each subkey or the scratchpad has its own unique address.

return. The 512-bit scratchpad serves to ensure data integrity of transfers to secure memory. A 64-bit factory-lasered ROM provides a unique identity to each DS1991, with an 8-bit family code, a 48-bit serial number, and an 8-bit CRC. The family code for the DS1991 is 02h.

The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1991 to be easily used by human operators. Accessories permit the DS1991 to be mounted on plastic key fobs, photo-ID badges, printed-circuit boards or any smooth surface of an object. Applications include secure access control, debit tokens, work-in-progress tracking, electronic travelers and proprietary data.

OPERATION

The DS1991 is accessed via a single data line using the 1-Wire protocol. The communication sequence has two distinct subsequences: the 1-Wire device selection sequence and the device-specific command sequence. The 1-Wire sequence precedes the device-specific command sequence to identify the particular device on the bus. This protocol is described in detail in the following section, "1-Wire Protocol."

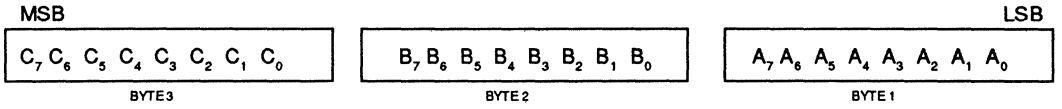
The DS1991 has six device-specific commands: Scratchpad Write, Scratchpad Read, Subkey Write, Subkey Read, Set Password and Move Block.

COMMAND WORD

The DS1991 is controlled through the command word. After the device is selected, the command word is written. The command word is comprised of three fields, each one byte long. The least significant byte is the function code field. This field defines the six commands that can be executed. The second byte is the address field. The first six bits of this field define the starting address of the

command. The last two bits of this field are the subkey address code. The third byte of the command word is a complement of the second byte (Figure 2). Each command in the command word is address-specific

COMMAND WORD STRUCTURE Figure 2



	BYTE 1
A_7-A_0	Command Field:

	BYTE 2
B_7-B_6	Sub-Address: 2 bits specifying which partition is to be accessed 00—SubKey 0 01—SubKey 1 10—SubKey 2 11—Scratchpad
B_5-B_0	Address Field: 6 bits that define the starting byte address in the scratchpad or any subkey

	BYTE 3
C_7-C_6	Partition Identifier Field: bit for bit complement of byte 2
C_5-C_0	Address Field: bit for bit complement of byte 2

COMMAND CONFIGURATIONS Figure 3

	Byte 1	Byte 2	
Command	Valid Commands	Valid Subkeys Address	Valid Addresses
ScratchPad Write	96h	11b	00h-3Fh
ScratchPad Read	69h	11b	00h-3Fh
Subkey Write	99h	00b, 01b, 10b	10h-3Fh
SubKey Read	66h	00b, 01b, 10b	10h-3Fh
Set Password	5Ah	00b, 01b, 10b	00h
Move Block	3Ch	00b, 01b, 10b	00h

NOTE: Byte 3 is complement of byte 2

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and therefore precludes the use of certain subkey codes and starting address locations (Figure 3).

SUBKEY COMMANDS

Each of the subkeys within the DS1991 is accessed individually. Transactions to read and write data to a secured subkey start at the address defined in the command word and proceed until the device is reset or the end of the subkey is reached. The three commands that operate on the secure subkeys are Set Password, Secure Data Write, and Secure Data Read.

Set Password

The Set Password command is used to enter the ID and password of the selected subkey. This command will erase all of the data stored in the secure area as well as over writing the ID and password fields with the new data. The DS1991 has a built-in check to ensure that the proper subkey was selected. The sequence begins by reading the ID field of the selected subkey; the ID of the subkey to be changed is then written into the part. If the IDs do not match, the sequence is terminated. Otherwise, the subkey contents are erased and 64 bits of new ID data are written followed by a new 64-bit password. The command sequence is shown in Figure 4.

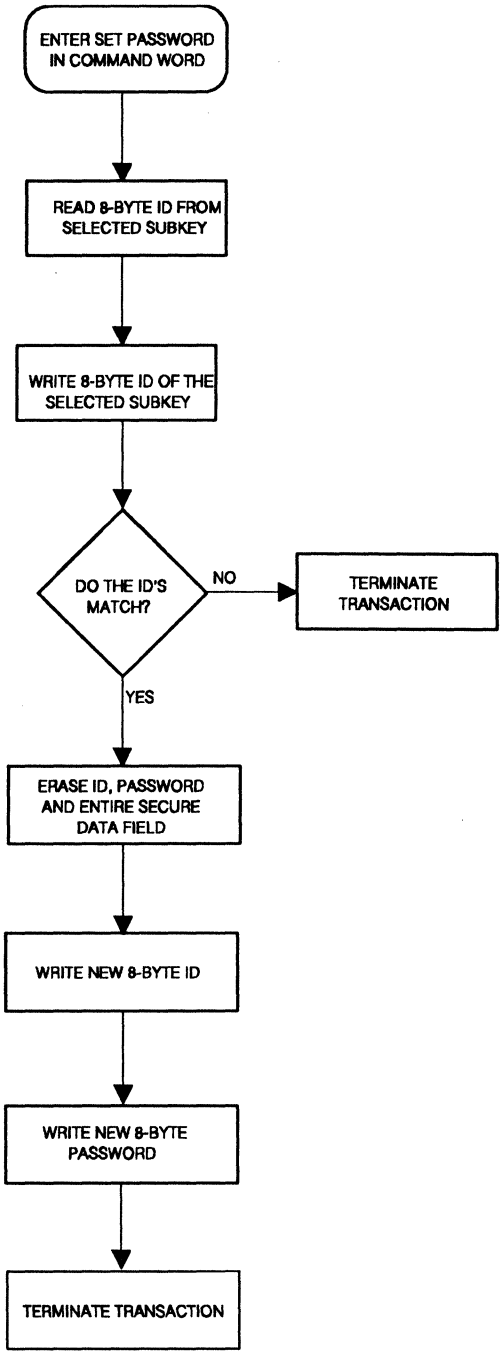
SubKey Write

The Subkey Write command is used to enter data into the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the transaction is terminated. Otherwise, the data following is written into the secure area. The starting address for the write sequence is specified in the command word. Data can be continuously written until the end of the secure subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 5.

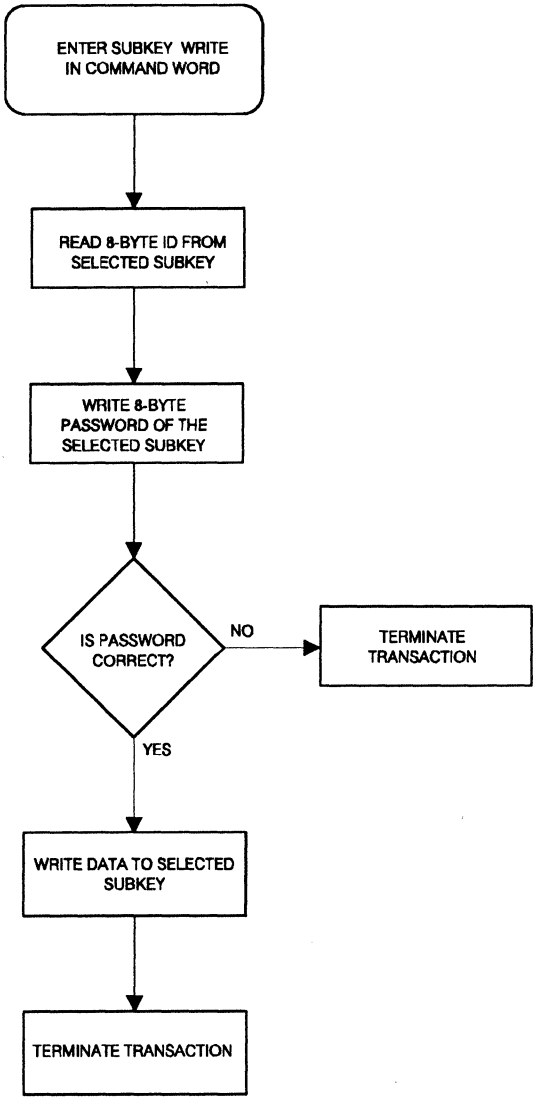
SubKey Read

The Subkey Read command is used to retrieve data from the selected subkey. Since the subkeys are secure, the correct password is required to access them. The sequence begins by reading the ID field; the password is then written back. If the password is incorrect, the DS1991 will transmit random data. Otherwise the data can be read from the subkey. The starting address is specified in the command word. Data can be continuously read until the end of the subkey is reached or until the DS1991 is reset. The command sequence is shown in Figure 6.

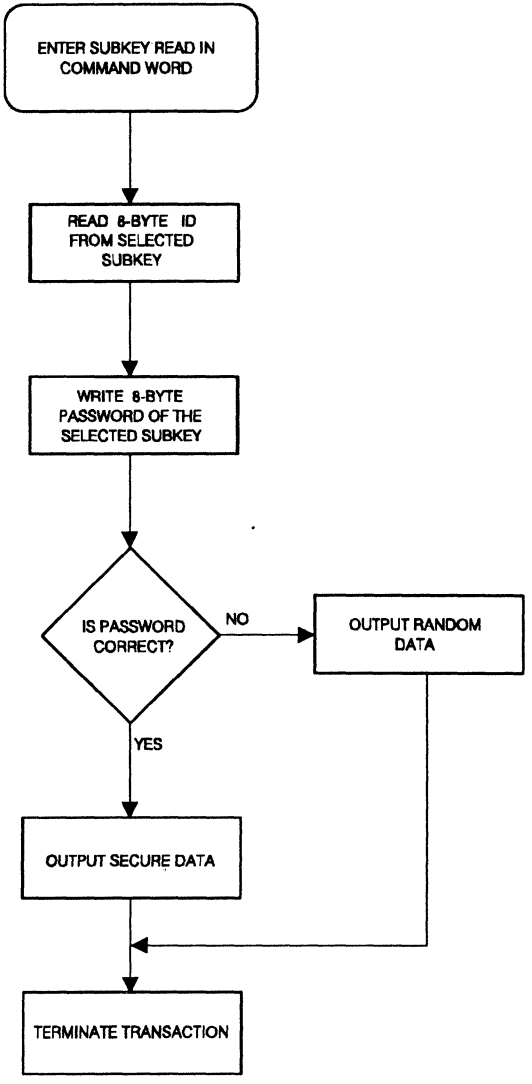
SET PASSWORD Figure 4



SUBKEY WRITE Figure 5



SUBKEY READ Figure 6



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SCRATCHPAD COMMANDS

The 64-byte read/write scratchpad of the DS1991 is not password-protected. The scratchpad can be used to store unsecured data or it can be used to build up a data structure which can be verified and transferred to a secure subkey. The three commands that operate on the scratchpad are Scratchpad Write, Scratchpad Read, and Move Block.

Scratchpad Write

The Scratchpad Write command is used to enter data into the scratchpad. The starting address for the write sequence is specified in the command word. Data can be continuously written until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 7.

Scratch Read

The Scratchpad Read command is used to retrieve data from the scratchpad. The starting address is specified in the command word. Data can be continuously read until the end of the scratchpad is reached or until the DS1991 is reset. The command sequence is shown in Figure 8.

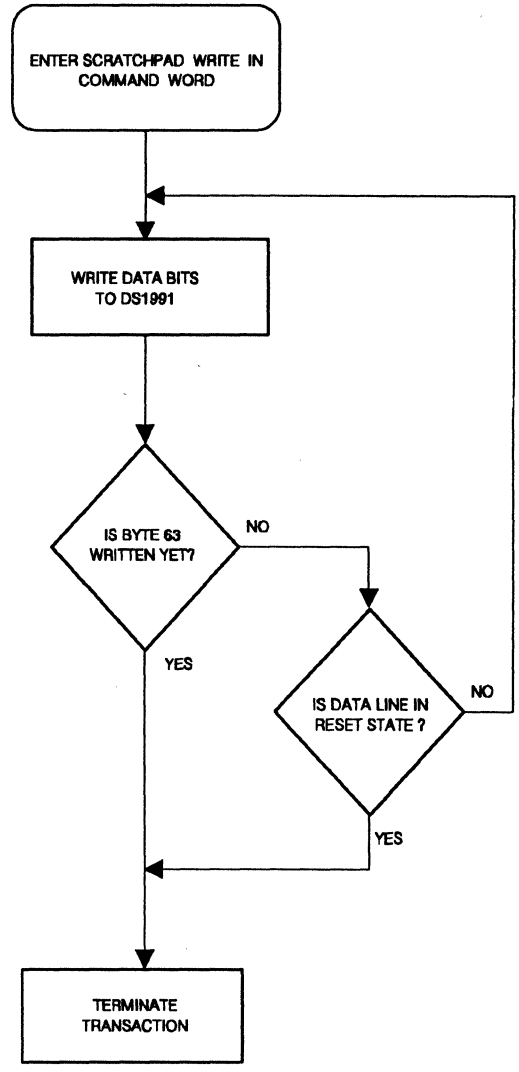
MOVE BLOCK

The Move Block command is used to transfer specified data blocks from the scratchpad to a selected subkey. This command might be used when data verification is required before storage in a secure subkey. Data can be transferred in single 8-byte blocks or a large 64-byte block. There are nine valid block selector codes that are used to specify which block is to be transferred (Figure 9). As a further precaution against accidental erasure of secure data, the 8-byte password of the destination must be entered. If the password does not match, the operation is terminated. After the block of data is transferred to the secure subkey, the original data in the corresponding block of the scratchpad is erased. The command sequence is shown in Figure 10.

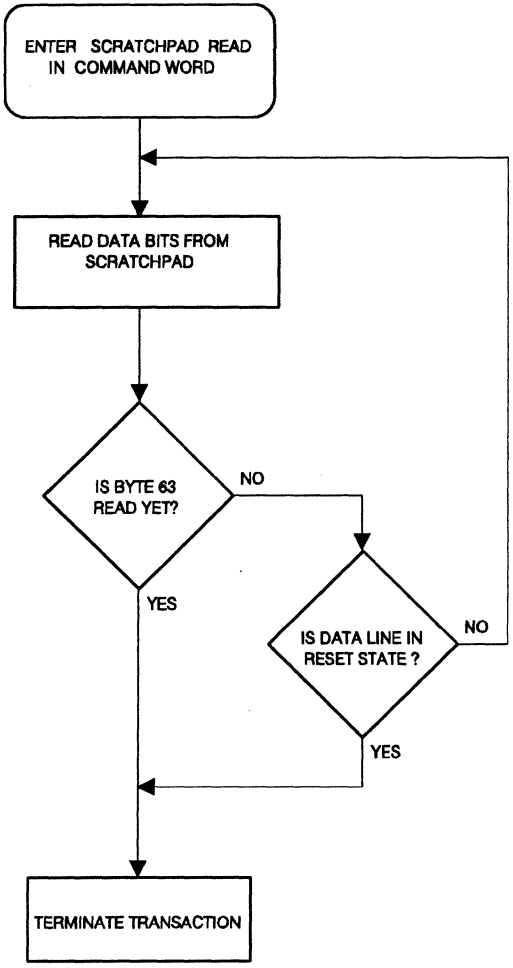
1-WIRE PROTOCOL

The 1-Wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1991 is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence. For a more detailed protocol description, refer to Application Note 23, "Using the 1-Wire Protocol."

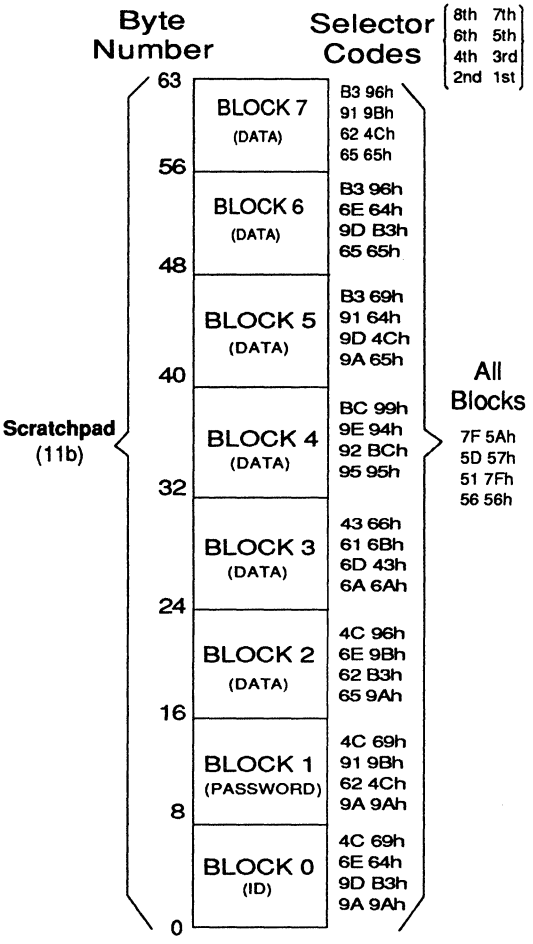
SCRATCHPAD WRITE Figure 7



SCRATCHPAD READ Figure 8



BLOCK MOVE SELECTOR CODES
Figure 9



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Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain connections. The DS1991 is an open drain part with an internal circuit equivalent to that shown in Figure 11. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 12. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur, and the bus is left low for more than 480µS all components on the bus will be reset.

Transaction Sequence

The protocol for accessing the DS1991 is as follows:

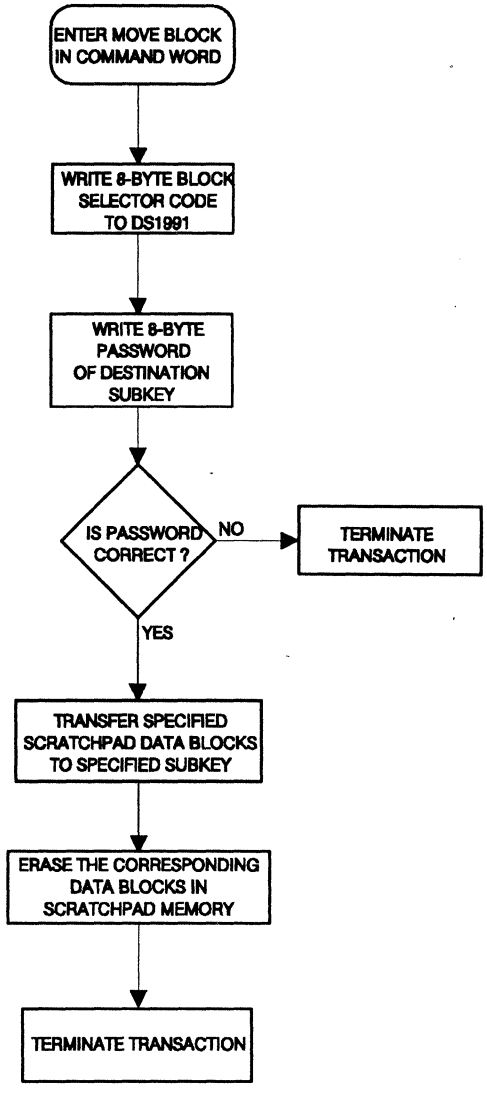
Reset
Presence Detect
1-Wire Command Word
Device Command Word
Transaction/Data
CRC

Reset/Presence Detect - All transactions on the 1-Wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 480µS. The DS1991 is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high; the part is taken out of reset and the part is ready to issue the presence detect.

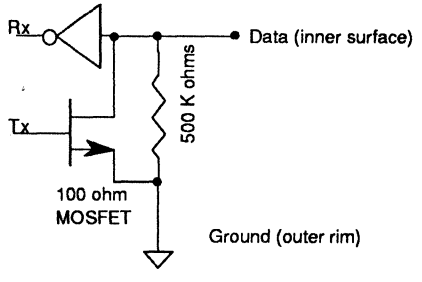
After detecting a high state on the data line, the DS1991 waits 15µS minimum and issues its presence detect. This presence detect is a low-going pulse that lasts a minimum of 60µS. This response to the reset pulse lets the bus master know that the DS1991 is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise, as the DS1991 is taken on and off the bus. Refer to the timing diagram in Figure 13.

After the DS1991 has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1µS. This 1µS interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 13.

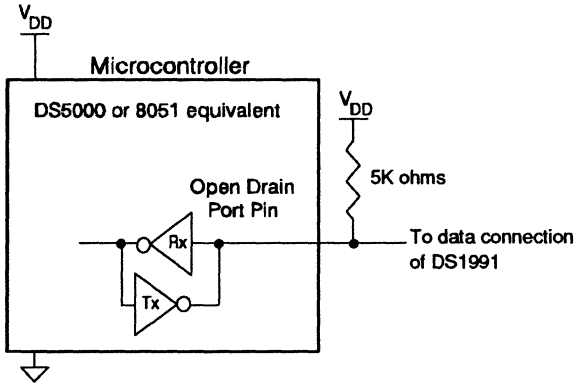
MOVE BLOCK Figure 10



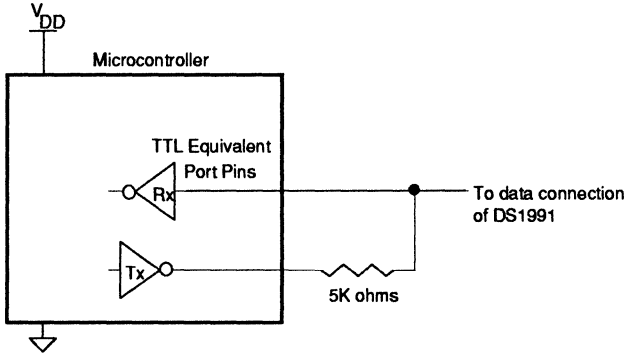
EQUIVALENT CIRCUIT Figure 11



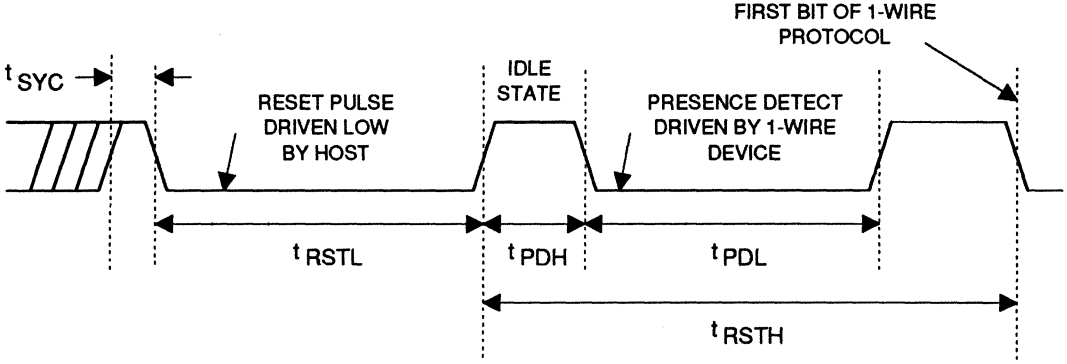
BUS MASTER OPEN DRAIN CIRCUIT Figure 12A



BUS MASTER STANDARD TTL CIRCUIT Figure 12B



RESET/PRESENCE DETECT SEQUENCE Figure 13



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1-Wire Command Word

Once the bus master has detected a presence it can issue one of the four different 1-Wire bus commands. All 1-Wire commands are eight bits long. A list of these commands are as follows:

CCh Pass Thru Mode

This command saves time by allowing direct access to the DS1991 without identifying it by ROM ID number. This command can only be used when there is a single slave on the bus. If more than one device is present there will be bus contention.

33h Read ROM Data

This command allows the bus master to read the DS1991's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1991 on the bus. If more than one is present there will be bus contention.

55h Match ROM Data

This mode allows the bus master to single out a specific DS1991 on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple devices on the bus.

F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the unique ROM data of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple three-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-Wire bus. The ROM data of the four devices is as shown:

ROM1 00110101...
ROM2 10101010...
ROM3 11110101...
ROM4 00010001...

The search process is as follows:

1) The bus master begins by resetting all devices present on the 1-Wire bus.

2) The bus master will then issue the Search ROM Data command on the 1-Wire bus.

3) The bus master will issue a read command to all of the devices on the 1-Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the bus master sees a 0. The bus master issues a second read command. Since the Search ROM data command is being executed, all of the devices on the 1-Wire bus respond to this second read command by placing the complement of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-Wire bus that have a 0 in the first position and others that have a 1.

4) The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-Wire bus.

5) The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6) The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7) The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8) The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9) The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-Wire bus.

10) The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11) The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12) The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13) The bus master starts a new ROM search by repeating steps 1 through 3.

14) The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15) The bus master executes two read time slots and receives two zeros.

16) The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

17) The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18) The bus master starts a new ROM search by repeating steps 13 through 15.

19) The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20) The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-Wire device on each ROM Search operation. The time required to derive the part's unique ID is:

960µS + (8 + (3 + 64)) X 60µS = 12.96mS

The bus master is therefore capable of identifying 77 different 1-Wire devices per second.

Additionally, the data obtained from the two reads of each set of three have the following interpretations:

00 — There are still devices attached which have conflicting bits in this position.
01 — All devices still coupled have a zero bit in this bit position.
10 — All devices still coupled have a one bit in this bit position.
11 — There are no devices active on the 1-Wire bus.

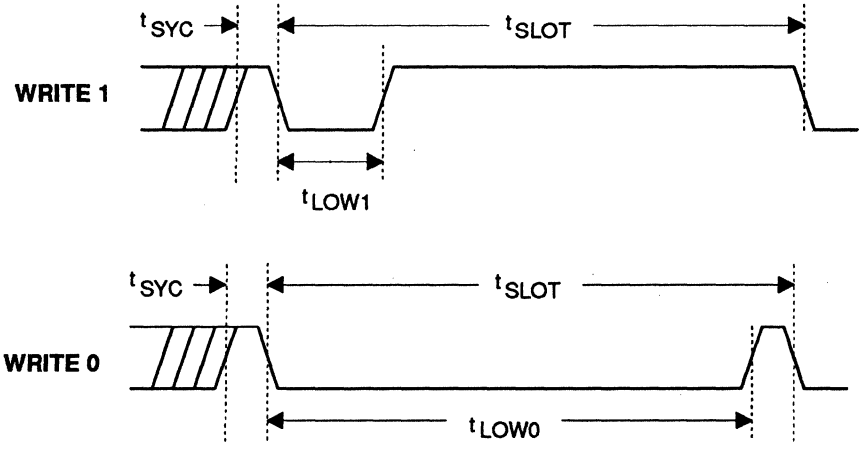
Transmitting/Receiving Data

All communications on the 1-Wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1991 is in the listening mode. The bus master must then transmit the 1-Wire command to the DS1991. To transmit the first bit of the 1-Wire bus command word, the master pulls the bus low for 1µS. This low-going edge informs the DS1991 that the first bit is being sent. After 1µS, the master does one of two things:

1) Holds the line low for an additional 60µS to output a 0 (write a zero) or,

2) Lets the bus go high for an additional 60µS (write a 1).

1-WIRE WRITE TIMING Figure 14



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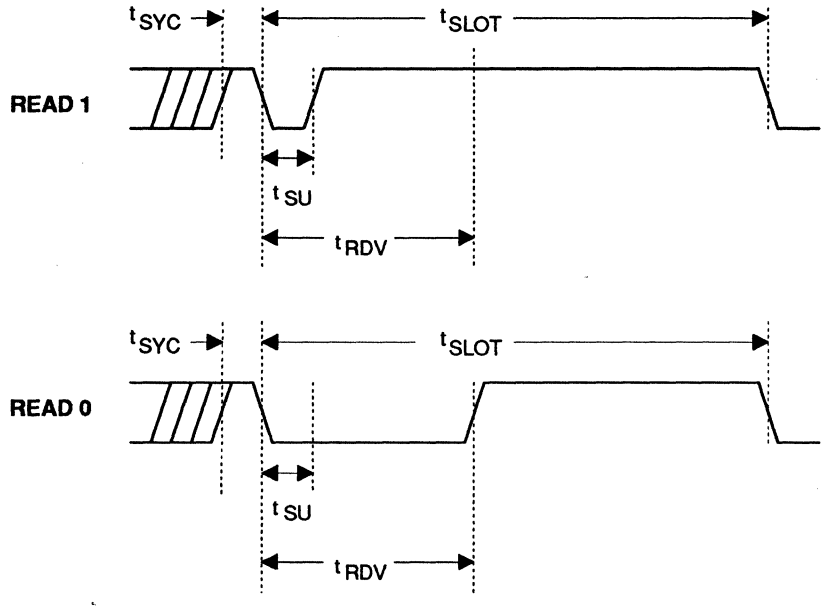
1-WIRE READ TIMING Figure 15



The state of the bus during this 60µS time phase determines the value of the bit. This is the frame sync mentioned earlier. This process is repeated until all the 8 bits are transmitted. Refer to the timing diagram in Figure 14.

The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1µS. This informs the DS1991 that it should have data on the bus no later than the 1µS from the falling edge. After the 1µS, the bus master lets go of the bus and the DS1991 drives the bus. The slave must hold the data on the bus for an additional 14µS minimum (59µS maximum). During the DS1991 holding time, the bus master reads the state of the bus. The bus master should read data from the bus within 15µS after the falling edge. The entire cycle time for one bit lasts a minimum of 60uS (120µS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 15 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1991 must be reset.

CRC Generation

To validate the transmitted data from the DS1991, the bus master generates a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1991. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. If the two CRC values match, the transmission is error-free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the DS5000 Soft Microcontroller. The procedure DO_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. Note that the variable CRC needs to be initialized to zero before the procedure is executed. Each byte of the data is then placed in the accumulator and DO_CRC is called to update the CRC variable. After all the data has been passed to DO_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is:

$$CRC = x^8 + x^5 + x^5 + 1$$

For a detailed explanation of the CRC computation, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

CRC ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC         ; save the accumulator
            PUSH    B           ; save the B register
            PUSH    ACC         ; save bits to be shifted
            MOV     B,#8        ; set shift = 8 bits
                                ;
CRC_LOOP:   XRL     A,CRC       ; calculate CRC
            RRC     A           ; move it to the carry
            MOV     A,CRC       ; get the last CRC value
            JNC     ZERO        ; skip if data = 0
            XRL     A,#18H      ; update the CRC value
                                ;
ZERO:       RRC     A           ; position the new CRC
            MOV     CRC,A       ; store the new CRC
            POP     ACC         ; get the remaining bits
            RR      A           ; position the next bit
            PUSH    ACC         ; save the remaining bits
            DJNZ    B,CRC_LOOP  ; repeat for eight bits
            POP     ACC         ; clean up the stack
            POP     B           ; restore the B register
            POP     ACC         ; restore the accumulator
            RET
```

PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 gms (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	
DS1991L-F5	10 years at 25°C (150 million transactions - see note 4)

Safety The DS1991 contains a small battery which is a lithium type (DS1991L-F5). These parts should never be incinerated or exposed to fire. Contact the appropriate government agency for any special disposal precautions with regard to lithium-powered devices.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-20°C to +70°C
Storage Temperature	-20°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}* = 1.5 to 6.0V, -20° to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.3		0.2	Volts	
Input Logic High	V_{IH}	1.1		6.0	Volts	
Ouput Logic Low @4mA	V_{OL}			0.4	Volts	
Output Logic High	V_{OH}		V_{PUP}	6.0	Volts	1,2
Input Resistance	R_I		500K		Ohms	3

*V_{PUP} = external pull-up voltage

AC ELECTRICAL CHARACTERISTICS

(-20°C to +70°C)

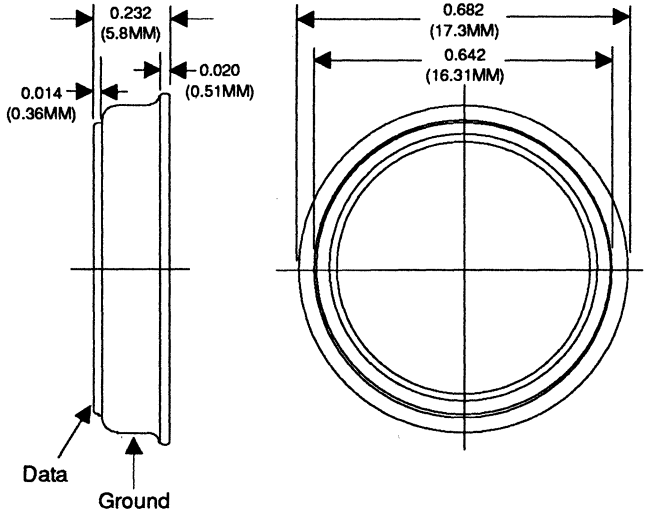
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t_{SLOT}	60		120	µS	
Write 1 Low Time	t_{LOW1}	1		15	µS	
Write 0 Low Time	t_{LOW0}	60		120	µS	
Read Data Valid	t_{RDV}			15	µS	
Read Data Setup	t_{SU}	1			µS	6
Frame Sync	t_{SYC}	1			µS	
Reset Low Time	t_{RSTL}	480			µS	
Reset High Time	t_{RSTH}	480			µS	5
Presence Detect High	t_{PDH}	15		60	µS	
Presence Detect Low	t_{PDL}	60		240	µS	

NOTES

1. All voltages are referenced to ground.
2. V_{PUP}=external pullup voltage to system supply.
3. Input pulldown resistance to ground.
4. A transaction is defined here as reading the entire scratchpad memory.
5. An additional reset or communication sequence cannot begin until the reset high time has expired.
6. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1 µS of this falling edge and will remain valid for 14 µS minimum (15 µS total from falling edge on 1-Wire).

DS1991 TOUCH MULTIKEY

F5 PACKAGE



DALLAS SEMICONDUCTOR

DS1992/DS1993
1K–Bit/4K–Bit Touch Memory
DS1994
4K–Bit Plus Time Touch Memory

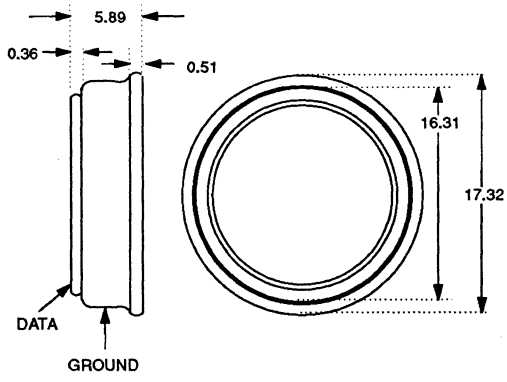
SPECIAL FEATURES

- 4096 bits of read/write nonvolatile memory (DS1993 and DS1994)
- 1024 bits of read/write nonvolatile memory (DS1992)
- 256–bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256–bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Contains real time clock/calendar in binary format (DS1994)
- Interval timer can automatically accumulate time when power is applied (DS1994)
- Programmable cycle counter can accumulate the number of system power–on/off cycles (DS1994)
- Programmable alarms can be set to generate interrupts for interval timer, real time clock, and/or cycle counter (DS1994)
- Write protect feature provides tamper–proof time data (DS1994)
- Programmable expiration date that will limit access to SRAM and timekeeping (DS1994)
- Clock accuracy is better than ±1 minute/month (DS1994)
- Operating temperature range from –20°C to +70°C
- Over 10 years of data retention

COMMON TOUCH MEMORY FEATURES

- Electronic identification by momentary contact
- Chip–based data carrier compactly stores information
- Can be accessed while affixed to object
- Economically communicates to host with a single digital signal at 16.6K bits per second
- Standard 16 mm diameter and 1–wire protocol ensure compatibility with Touch Device family
- Coin shape is self–aligning with mating receptacles
- Durable stainless steel case resists environmental hazards
- Unique, factory–lasered, 48 bit serial number for absolute traceability
- Easily attaches to objects using adhesive backing or snap–in flange, spring clip or magnetic holder
- Presence detect signal announces connection to host

PIN ASSIGNMENT



(All dimensions shown in millimeters)

CONTACTS	
Rim	Ground
Inner Face	Data

ACCESSORIES	
DS9092	Touch Memory Probe, Hand=Grip or Panel Mount
DS9093F	Touch Memory Key Ring Mount
DS9094F	Touch Memory Clip
DS9096	Self–Stick Adhesive Pad
DS9098	Surface Mount Retainer

ORDERING INFORMATION	
DS1992L–F5	10 year data retention, F5 package
DS1993L–F5	10 year data retention, F5 package
DS1994L–F5	10 year data retention, F5 package

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DESCRIPTION

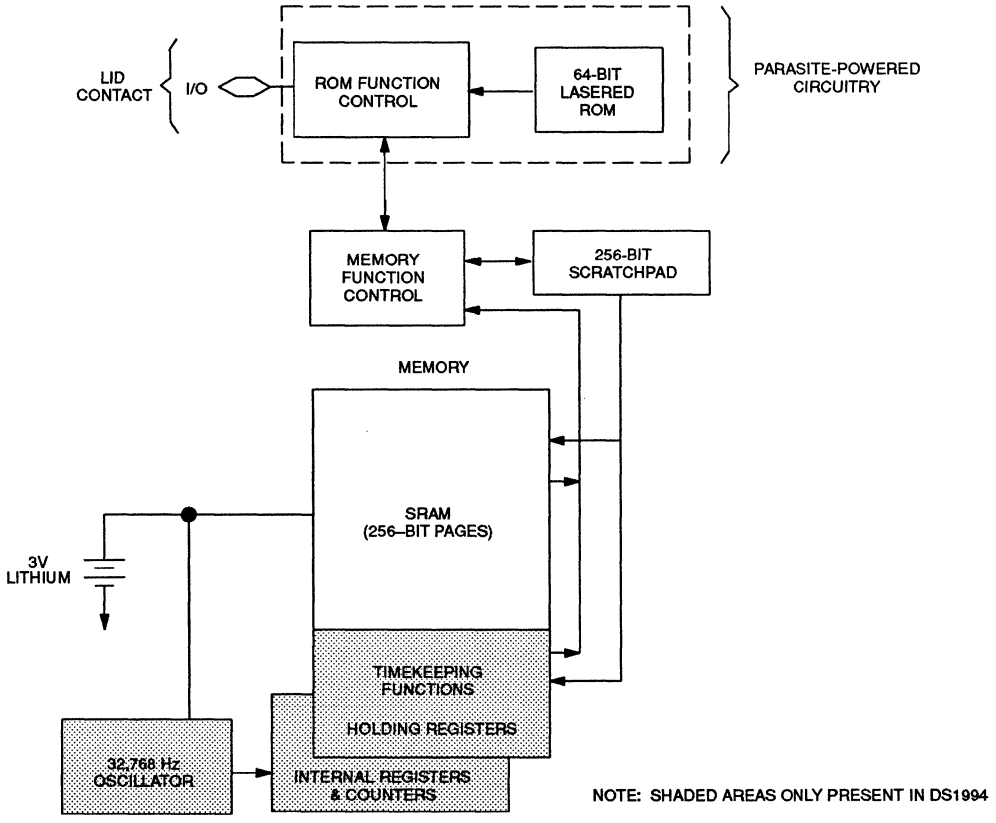
The DS1992/DS1993/DS1994 Touch Memory (hereafter referred to as DS199X) is a rugged read/write data carrier that acts as a localized database that can be easily accessed with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the Touch Memory is attached. Data is transferred serially via the 1–wire protocol which requires only a single data lead and a ground return. The memory is organized into 256–bit pages and data is first written into a page at a time using a 256–bit scratchpad then trasferred to memory for enhanced data integrity. A 48–bit serial number is factory lasered into each DS199X to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin–shaped profile is self–aligning with mating receptacles, allowing the DS199X to be easily used by human operators. Accessories permit the DS199X to be mounted on almost any surface including plastic key fobs, photo–ID badges and printed circuit boards. Applications include access control, work–in–progress tracking, electronic travelers, storage of calibration constants, and debit tokens. With the optional timekeeping functions (DS1994), a real time clock/calendar, interval timer, cycle counter, and programmable interrupts are available in addition to the nonvolatile memory. The internal clock can be programmed to deny memory access based on absolute time/date, total elapsed time, or the number of accesses. These features allow the DS1994 to be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, interval timer, and event scheduler.

OVERVIEW

The DS199X has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 1024–bit (DS1992) or 4096–bit (DS1993 and DS1994) SRAM, and 4) timekeeping registers (DS1994). The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768 kHz crystal. The SRAM and timekeeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions will not be available until the ROM function protocol has been established. This protocol is described in the ROM functions flow chart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master may then provide any one of the four memory function commands (Figure 6).

DS199X BLOCK DIAGRAM Figure 1



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PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for an reason, the ROM may still be read normally.

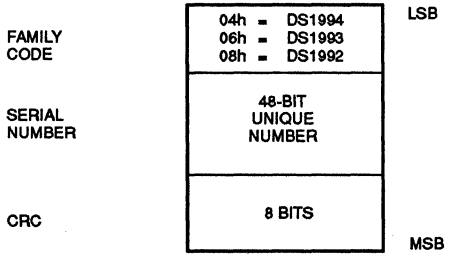
64-BIT LASERED ROM

Each DS199X contains a unique ROM code that is 64 bits long. The first eight bits are a 1-wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 2.)

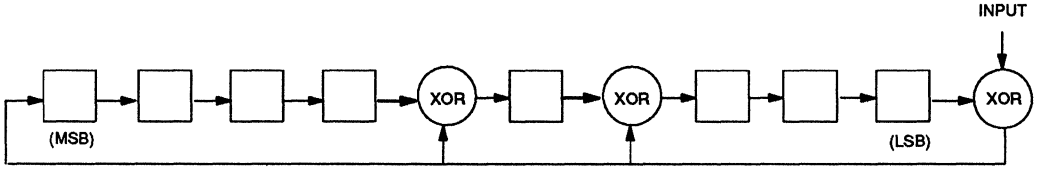
The 1-wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

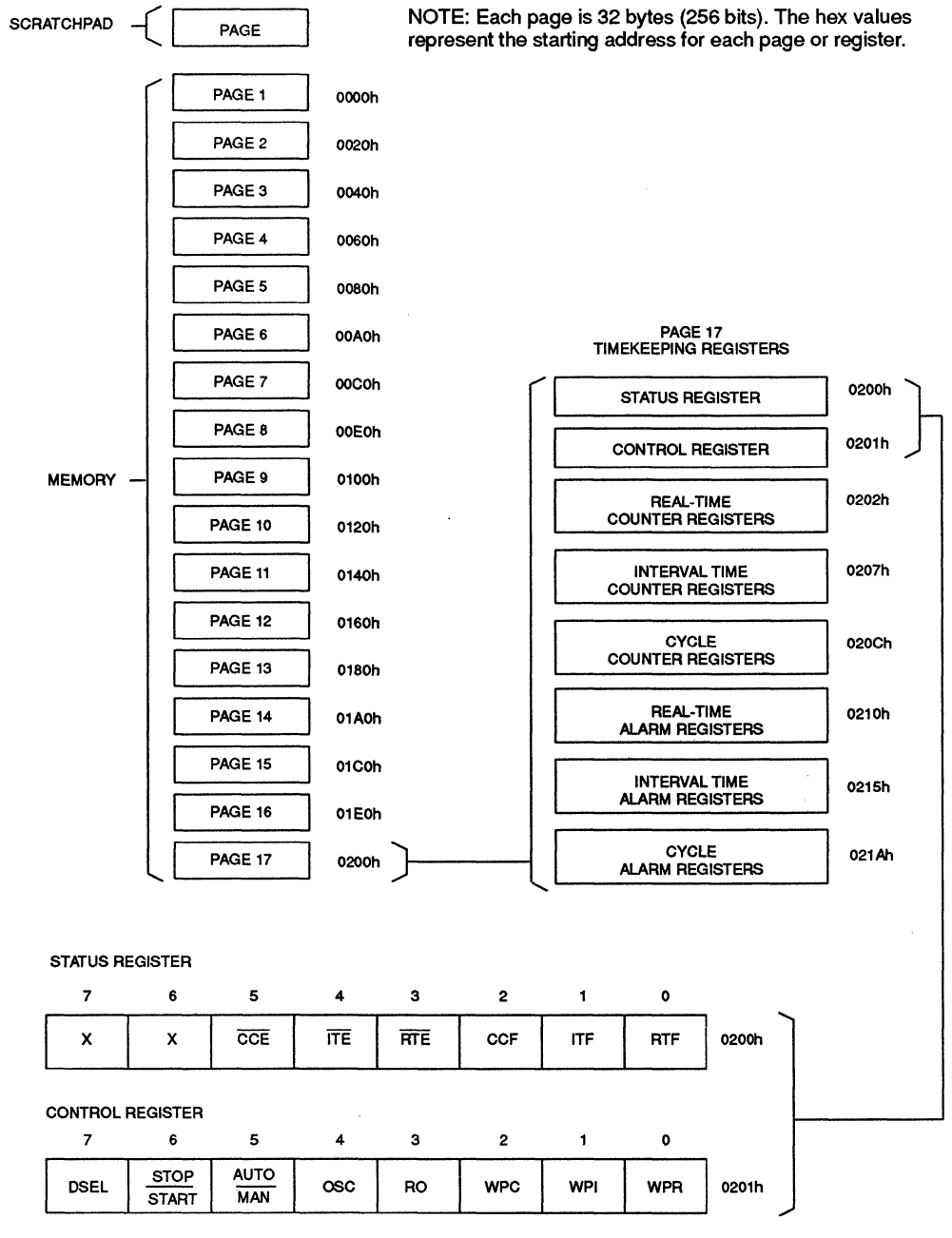
64-BIT LASERED ROM Figure 2



1-WIRE CRC CODE Figure 3



DS1994 MEMORY MAP Figure 4a



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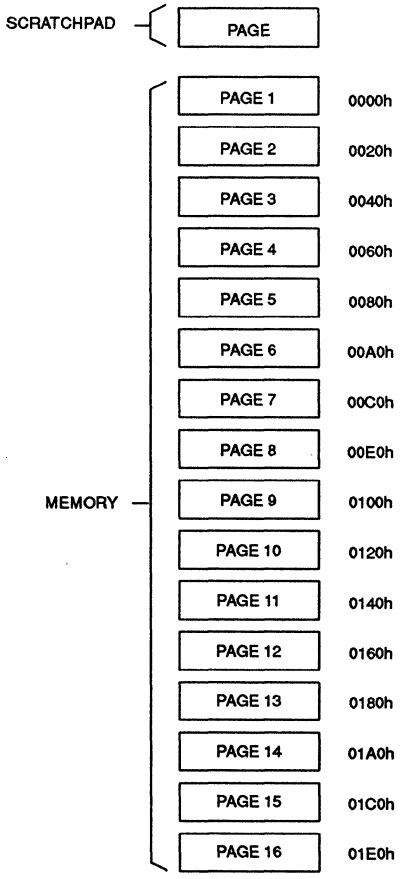
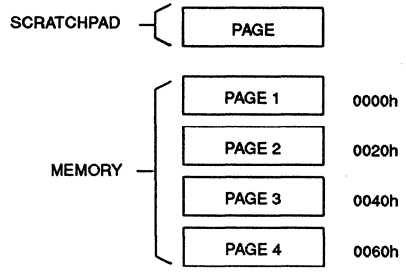
DS1993 MEMORY MAP Figure 4b



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

DS1992 MEMORY MAP Figure 4c



NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

MEMORY

The memory map in Figure 4 shows a 32–byte page called the scratchpad and additional 32–byte pages called memory. The DS1992 contains pages 1 though 4 which make up the 1024–bit SRAM. The DS1993 and DS1994 contain pages 1 through 16 which make up the 4096–bit SRAM. The DS1994 also contains page 17 which has only 30 bytes that contain the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process insures data integrity when modifying the memory.

TIMEKEEPING (DS1994)

A 32,768 Hz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real time clock, interval timer, cycle counter and 1 Hz output to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers which the user accesses. This occurs after the eighth bit of the Read Memory Function command.

Real-Time Clock

The real-time clock is a 5-byte binary counter. It is incremented 256 times per second. The least significant byte is a count of fractional seconds. The upper four bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point which is determined by the user. For example, 12:00A.M., January 1, 1970 could be a reference point.

Interval Timer

The interval timer is a 5-byte binary counter. When enabled, it is incremented 256 times per second. The least significant byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation which are selected by the AUTO/$\overline{\text{MAN}}$ bit in the control register. In the auto mode, the interval timer will begin counting after the I/O line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer will stop counting after the I/O line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/$\overline{\text{START}}$ bit in the control register.

NOTE: For auto mode operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

Cycle Counter

The cycle counter is a 4-byte binary counter. It increments after the falling edge of the I/O line if the appropriate I/O line timing has been met. This timing is selected by the DSEL bit in the control register. (See "Status/Control" section).

NOTE: For cycle counter operation, the high level on the I/O pin must be greater than or equal to 2.1 volts.

Alarm Registers

The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit(s) in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See "Status/Control", "Interrupts", and the "Programmable Expiration" sections.)

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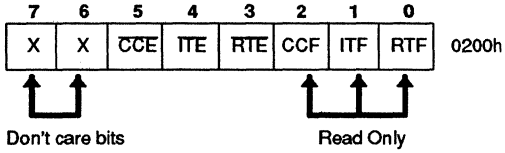
STATUS/CONTROL REGISTERS (DS1994)

The status and control registers are the first two bytes of page 17 (see "Memory Map", Figure 4).

Status Register



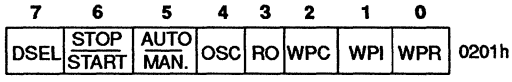
0	RTF	Real-time clock alarm flag
1	ITF	Interval timer alarm flag
2	CCF	Cycle counter alarm flag

When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag(s) is cleared by reading the status register.

3	RTE	Real-time interrupt enable
4	ITE	Interval timer interrupt enable
5	CCE	Cycle counter interrupt enable

Writing any of the interrupt enable bits to a logic 0 will allow an interrupt condition to be generated when its corresponding alarm flag is set (see "Interrupts" section).

Control Register



0	WPR	Write protect real-time clock/alarm registers
1	WPI	Write protect interval timer/alarm registers
2	WPC	Write protect cycle counter/alarm registers

Setting a write protect bit to a logic 1 will permanently write protect the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits can not be written in a normal manner (see "Write Protect/Programmable Expiration" section).

3	RO	Read Only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1992/DS1993/DS1994 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see "Write Protect/Programmable Expiration" section).

4	OSC	Oscillator Enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator will start operation. When the oscillator bit is a logic 0, the oscillator will stop.

5	AUTO/$\overline{\text{MAN}}$	Automatic/$\overline{\text{Manual}}$ Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the I/O line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode the interval timer is enabled by the STOP/$\overline{\text{START}}$ bit.

6	STOP/$\overline{\text{START}}$	Stop/$\overline{\text{Start}}$ (in Manual Mode)

If the interval timer is in manual mode, the interval timer will start counting when this bit is set to a logic 0 and will stop counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7	DSEL	Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the I/O line. When this bit is set to a logic 1, the delay time is 123 ± 2 ms. This delay allows communication on the I/O line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is 3.5 ± 0.5 ms.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers

are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status byte (E/S).

The target address points to a unique byte location in memory. The first five bits of the target address (T4:T0) represent the byte offset within a page. This byte offset points to one of 32 possible byte locations within a given page. For instance, 00000b points to the first byte of a page where as 11111b would point to the last byte of a page.

The third register (E/S) is a read only register. The first five bits (E4: E0) of this register are called the ending offset. The ending offset is a byte offset within a page (1 of 32 bytes). Bit 5 (PF) is the partial byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

ADDRESS REGISTERS Figure 5

	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	OF	PF	E4	E3	E2	E1	E0

Write Scratchpad Command [0Fh]

After issuing the write scratchpad command, the user must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) will be set and the remaining data will be ignored. If the user writes an incomplete byte and an overflow has not occurred, the partial byte flag (PF) will be set.

Read Scratchpad Command [AAh]

This command may be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user may begin reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The user may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [55h]

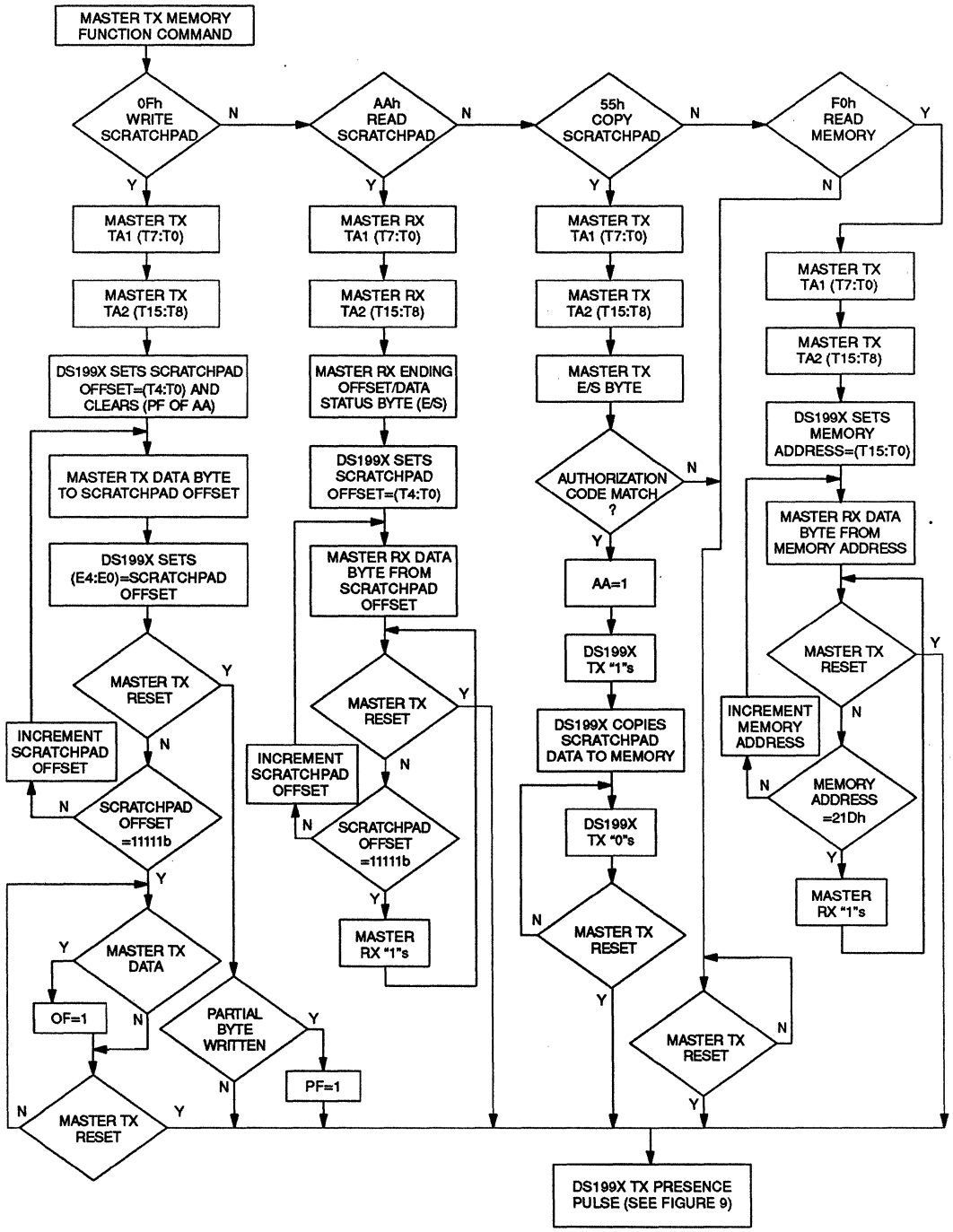
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A logic 0 will be transmitted after the data has been copied until a reset pulse is issued by the user. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 2 to 32 bytes may be copied to memory with this command. Whole bytes are copied even if only partially written. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0h]

The read memory command may be used to read the entire memory. After issuing the command, the user must provide the 2-byte target address. After the two bytes, the user reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

MEMORY FUNCTION FLOW CHART Figure 6



MEMORY FUNCTION EXAMPLES

Example: Write two data bytes to memory locations 0026h and 0027h (the seventh and eighth bytes of page 2). Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	0Fh	Issue "write scratchpad" command
TX	26h	TA1, beginning offset=6
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue "read scratchpad" command
RX	26h	Read TA1, beginning offset=6
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7, flags=0
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	55h	Issue "copy scratchpad" command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	F0h	Issue "read memory" command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<128 bytes (DS1992)> <512 bytes (DS1993)> <542 bytes (DS1994)>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

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WRITE PROTECT/PROGRAMMABLE EXPIRATION (DS1994)

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1994 when an alarm occurs (programmable expiration).

The write protect bits may not be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit will set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command may be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers will continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set.

The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic "0", no memory function commands are available. The ROM functions are always available.

WRITE PROTECT CHART Figure 7

WRITE PROTECT BIT SET:	WPR	WPI	WPC
Data Protected from User Modification:	Real Time Clock Real Time Alarm WPR WPI WPC RO OSC*	Interval Timer Interval Time Alarm WPR WPI WPC RO OSC* STOP/$\overline{\text{START}}$** AUTO/$\overline{\text{MAN}}$	Cycle Counter Cycle Counter Alarm WPR WPI WPC RO OSC* DSEL

* Becomes write "1" only, i.e., once written to a logic "1", may not be written back to a logic "0".
** Forced to a logic "0".

1-WIRE BUS SYSTEM

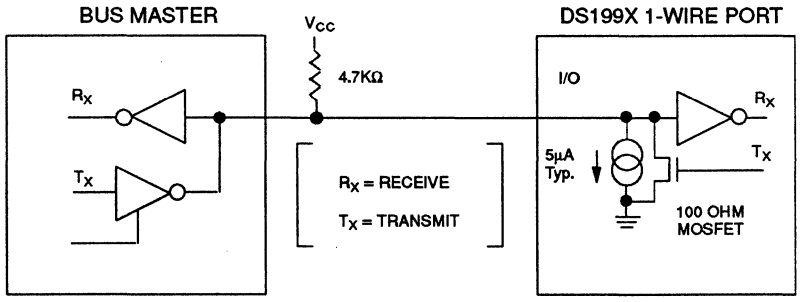
The 1-wire bus is a system which has a single bus master and one or more slaves. In most instances the DS199X behaves as a slave. The exception is when the DS1994 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain or 3–state outputs. The 1-wire port of the DS199X is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1–wire bus with multiple slaves attached. The 1-wire bus has a maximum data rate of 16.6K bits per second and requires a pull-up resistor of approximately 5KΩ.

The idle state for the 1-wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µS, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS199X via the 1-wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS199X is on the bus and is ready to operate. For more details, see the "1-Wire Signalling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33h]

This command allows the bus master to read the DS199X's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS199X on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS199X on a multidrop bus. Only the DS199X that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Example of a ROM Search

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the search ROM command on the 1-wire bus.

3. The bus master reads a bit from the 1–wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1–wire bus. ROM1 and ROM4 will place a 0 onto the 1–wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1–wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the search ROM data command is being executed, all of the devices on the 1–wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1–wire bus. ROM1 and ROM4 will place a 1 onto the 1–wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1–wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1–wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3–step routine have the following interpretations:

   00 - There are still devices attached which have conflicting bits in this position.

   01 - All devices still coupled have a 0 bit in this bit position.

   10 - All devices still coupled have a 1 bit in this bit position.

   11 - There are no devices attached to the 1-wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.

5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.

8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

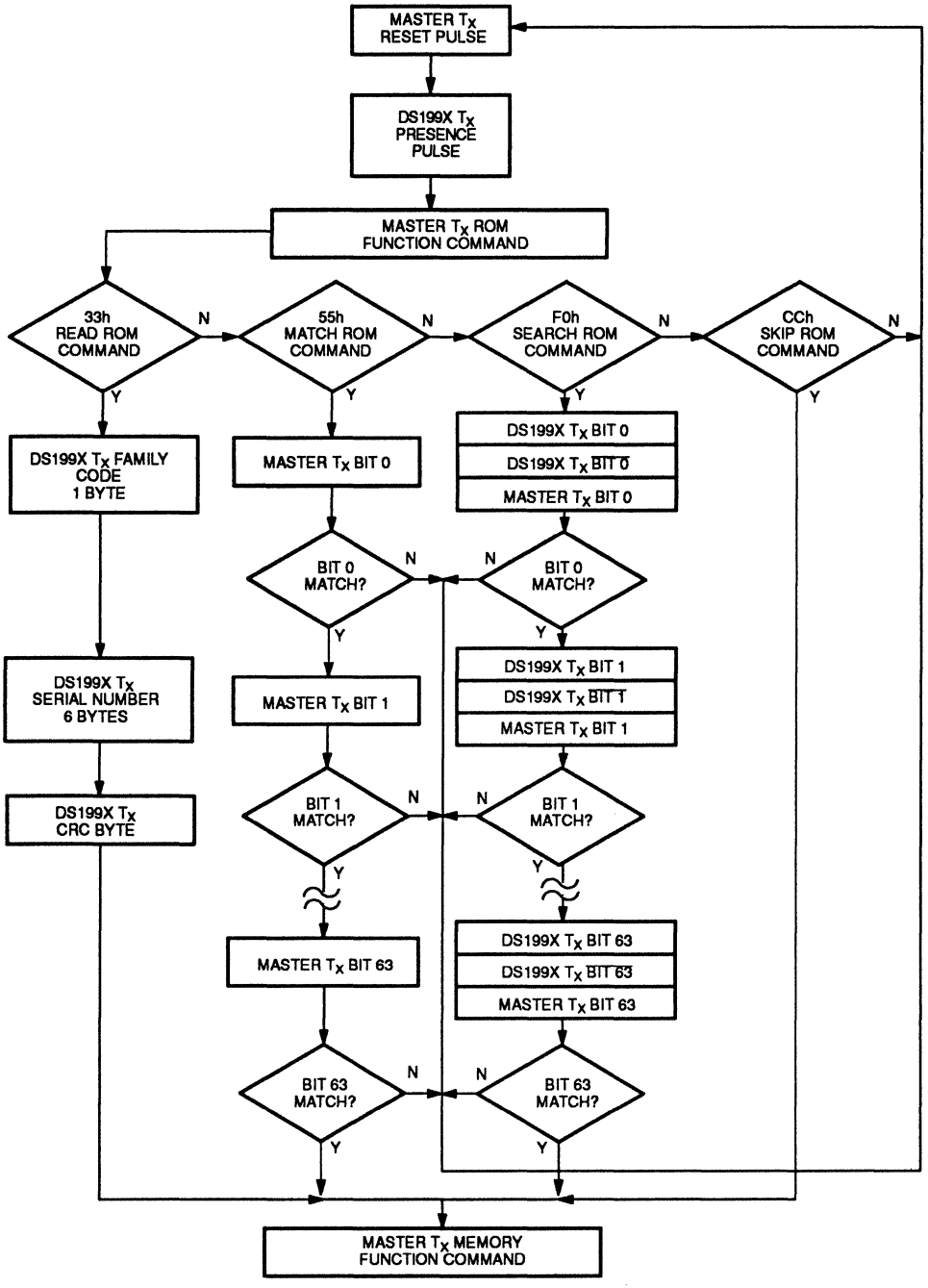
13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two read time slots and receives two zeros.

16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.

ROM FUNCTIONS FLOW CHART Figure 9



(SEE FIGURE 6)

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17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

At this point, the bus master repeats the process described above to determine the ROM code of the remaining devices on the 1-wire bus.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu S + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-wire devices per second.

I/O SIGNALLING

The DS199X requires strict protocols to insure data integrity. The protocol consists of seven types of signalling on one line: reset pulse, presence pulse, write 0, write 1, read 0, read 1, and interrupt pulse (DS1994). All these signals, with the exception of the interrupt pulse, are initiated by the bus master.

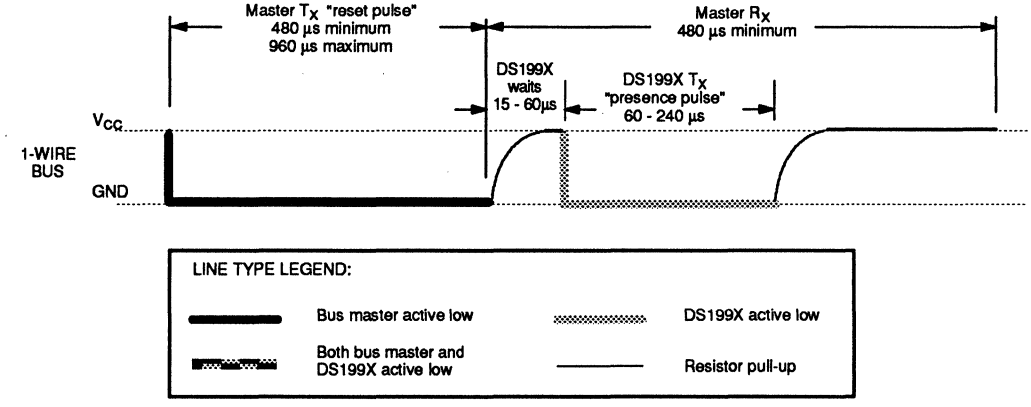
The initialization sequence required to begin any communication with the DS199X is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS199X is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-wire bus is pulled to a high state via the 5K pull-up resistor. After detecting the rising edge on the I/O pin, the DS199X waits 15-60 µs and then transmits the presence pulse (a low signal for 60 - 240 µs). There are special conditions if interrupts are enabled where the bus master must check the state of the 1-wire bus after being in the R_X mode for 480 µs. These conditions will be discussed in the "Interrupt" section.

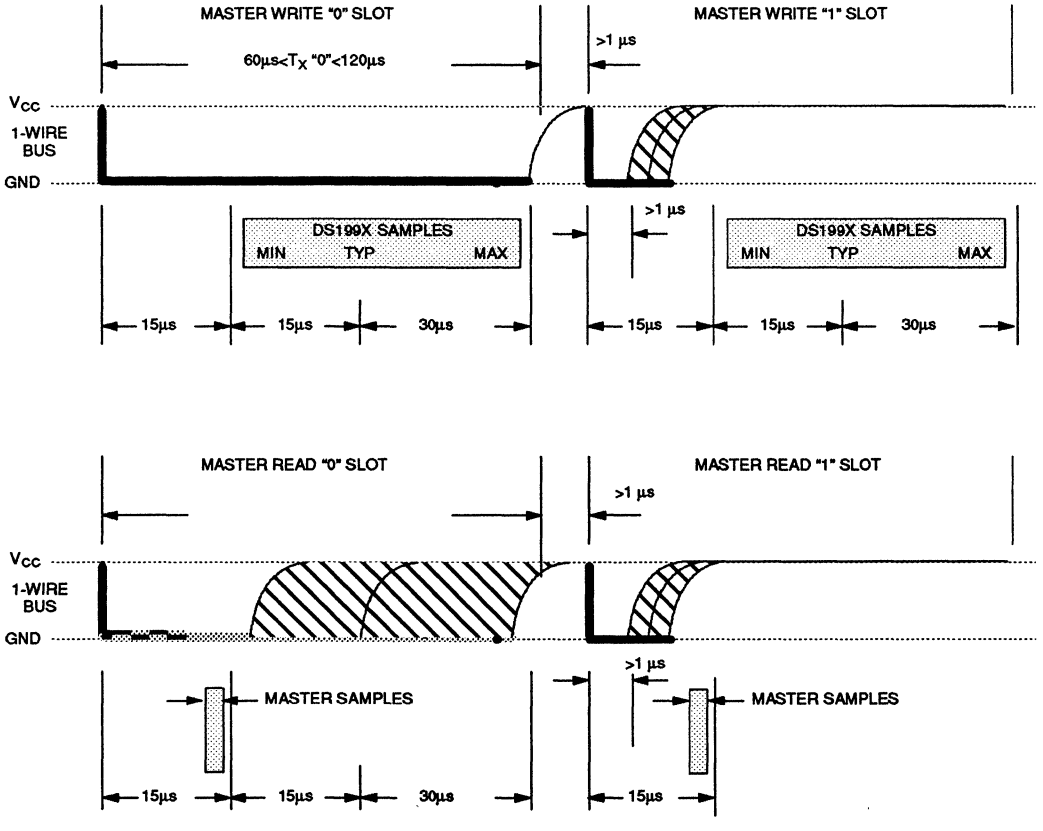
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the I/O line low. The falling edge of the I/O line synchronizes the DS199X to the master by triggering a delay circuit in the DS199X. During write time slots, the delay circuit determines when the DS199X will sample the I/O line. For a "read 0" time slot, the delay circuit determines how long the DS199X will hold the I/O line low.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10



READ/WRITE TIMING DIAGRAM Figure 11



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DETAILED MASTER READ "1" TIMING Figure 12

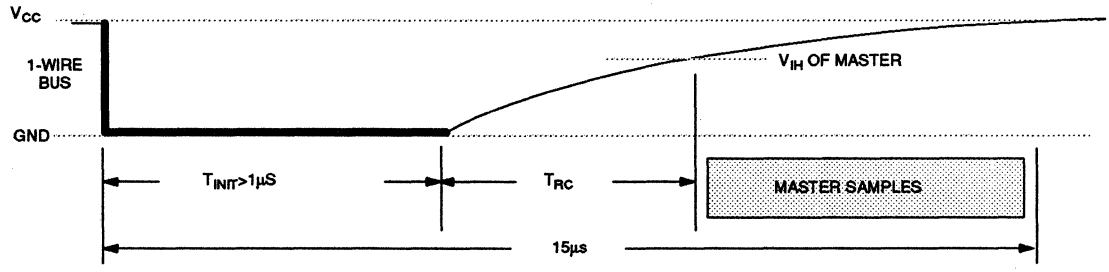
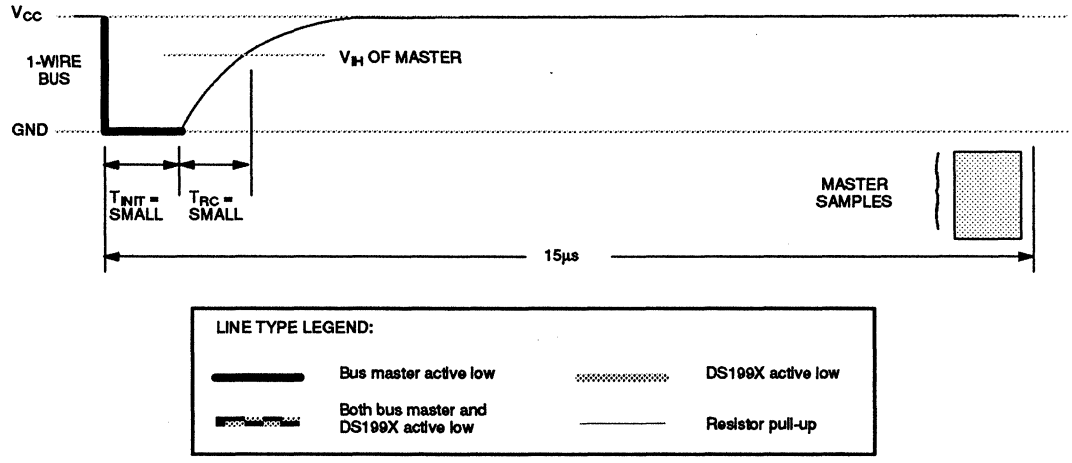


Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs. Figure 13 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15µs period.

RECOMMENDED MASTER READ "1" TIMING Figure 13



Interrupts (DS1994)

An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the flags are read) or if the corresponding interrupt enable bit(s) is disabled.

On the 1-wire port, the DS1994 responds, in general, by driving the I/O pin low for an extended period of time and then releasing. The interrupt condition may produce two types of interrupts on the 1-wire port. A type 1 interrupt (Figure 14) occurs only when I/O is high and there has been no communication (i.e., there has not been a falling edge on I/O since the last presence pulse). If this is the case, I/O is driven low for a period of 960 µs to 3840 µs as soon as an interrupt condition begins. A presence pulse will follow the interrupt pulse.

A type 2 interrupt (Figure 17) occurs if the host issues a reset pulse and an interrupt condition exists when the host releases the reset. If this is the case, I/O is driven low for an additional period of time, extending the reset pulse to a total period of 960 µs to 4800 µs. A presence pulse will follow the interrupt pulse. As long as the interrupt condition exists, the type 2 interrupt will occur with every reset pulse.

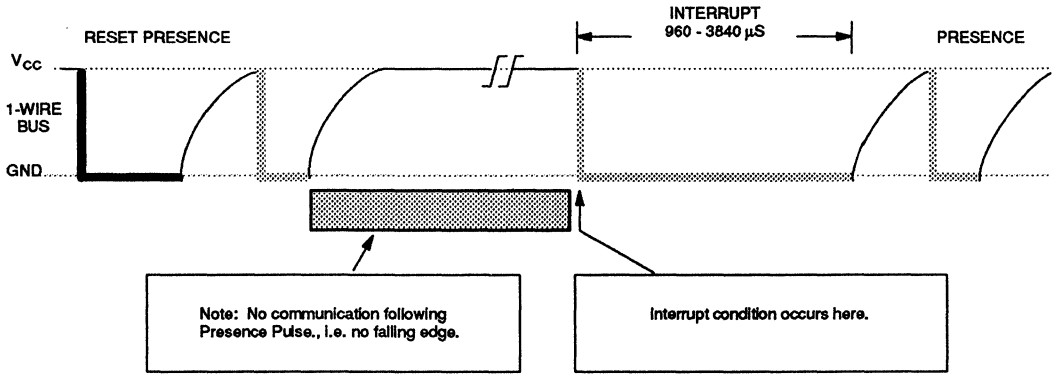
NOTE: If the interrupt condition begins during communication, a type 1 interrupt will not be issued. However, type 2 interrupts will occur during resets as expected.

Special cases exist as follows:

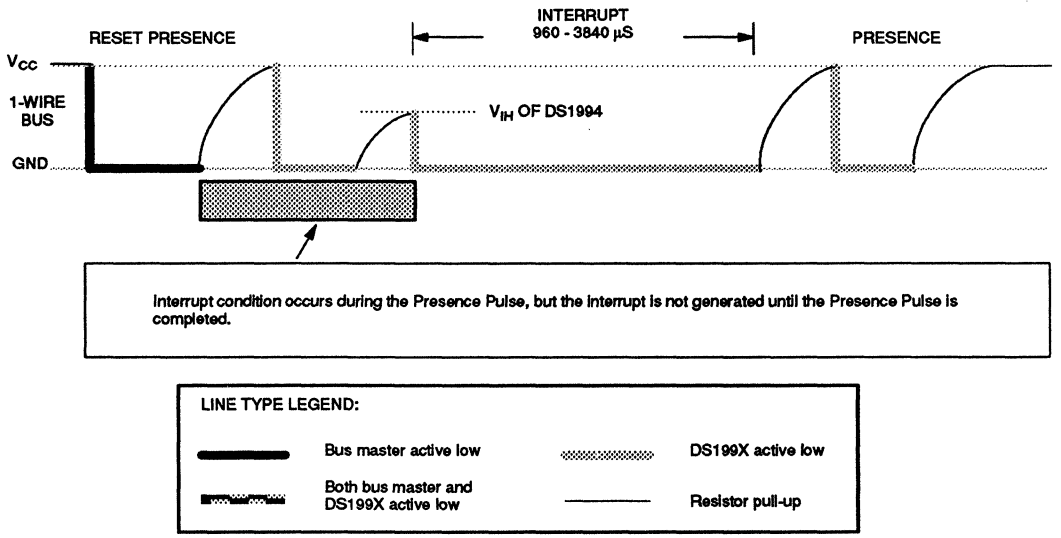
Special Case A (Figure 15): If the interrupt condition begins during a presence pulse, the type 1 interrupt will be postponed until the presence pulse is over and I/O is a logic 1.

Special Case B (Figure 16): If an interrupt condition exists while the parasite-powered circuitry is powered down (i.e., I/O has been low for $\gg$1s), a type 1 interrupt will occur after the first presence pulse following I/O going high, just as in Special Case A.

TYPE 1 INTERRUPT Figure 14



TYPE 1A INTERRUPT (SPECIAL CASE A) Figure 15



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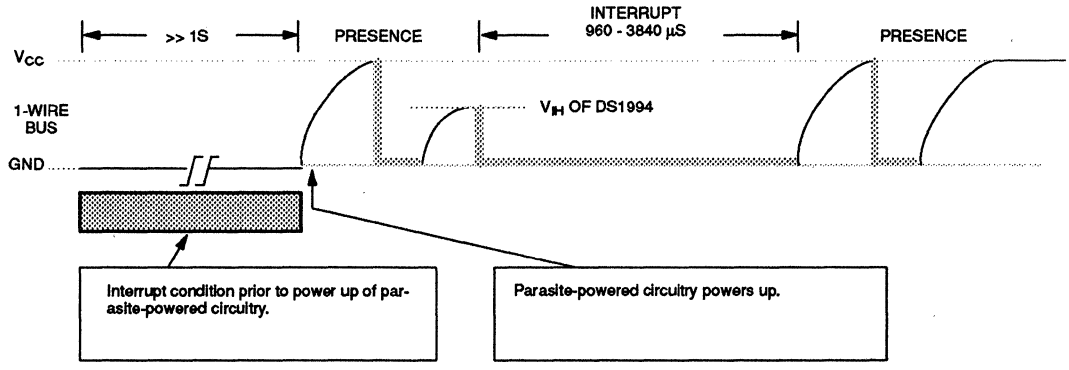
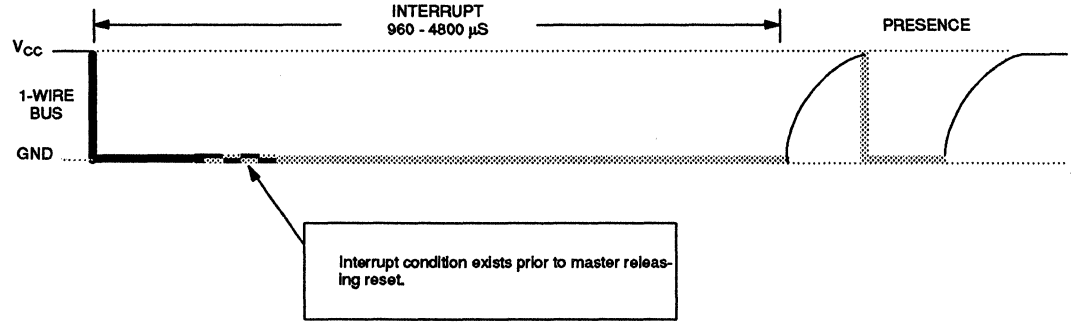
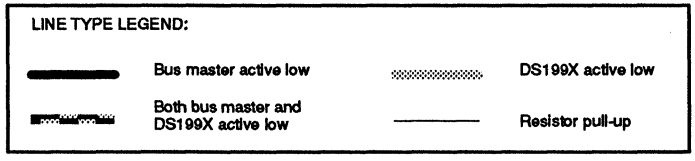
TYPE 1B INTERRUPT (SPECIAL CASE B) Figure 16



TYPE 2 INTERRUPT Figure 17





PHYSICAL SPECIFICATIONS

Size	See mechanical drawing
Weight	3.3 grams (F5 package)
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	The DS199X contains a small battery which is a lithium type. These parts should never be incinerated or exposed to fire. Contact the appropriate Government agency for any special disposal precautions with regard to lithium–powered devices.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	–20°C to 70°C
Storage Temperature	-20°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.8°C to 6.0V, –20°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Output Logic Low @ 1 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	6

AC ELECTRICAL CHARACTERISTICS

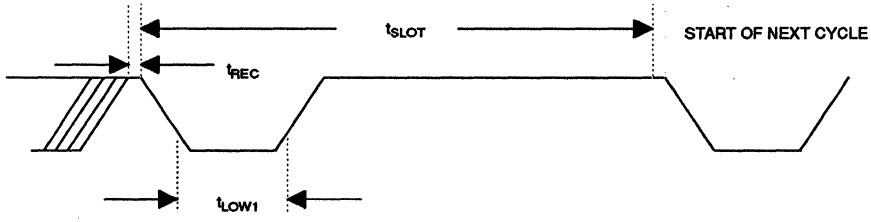
(–20°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}			15	µs	
Read Data Setup	t_{SU}	1			µs	5
Interrupt	t_{INT}	960		4800	µs	8
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

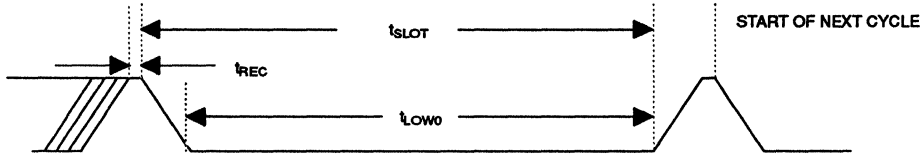
NOTES

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage.
3. Input load is to ground.
4. An additional reset or communication sequence cannot begin until the reset high time has expired.
5. Read data setup time refers to the time the host must pull the 1–wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1–wire bus.)
6. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5K resistor is used to pull-up the I/O line to V_{CC}, 5 µs after power has been applied, the parasite capacitance will not affect normal communications.
7. DS1994 requires a maximum low time for a reset pulse of 960 µs because of the possibility of an interrupt occuring.
8. DS1994 only.

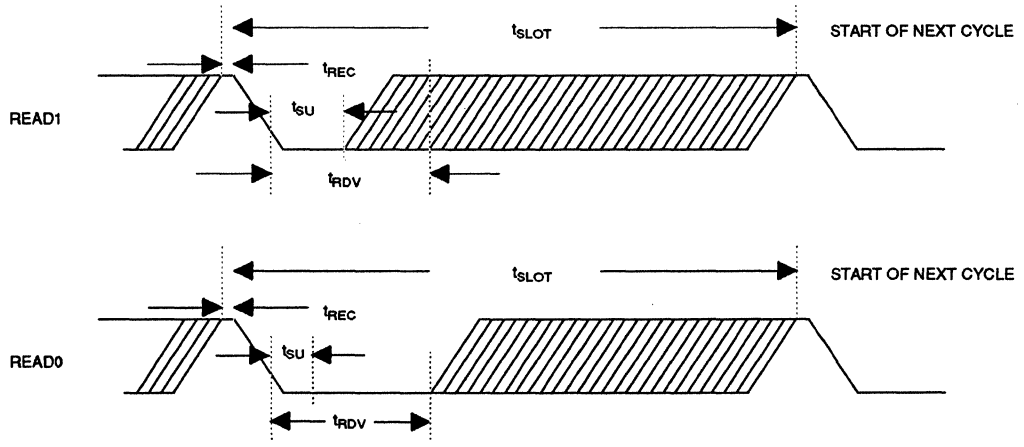
1-WIRE WRITE ONE TIME SLOT Figure 18



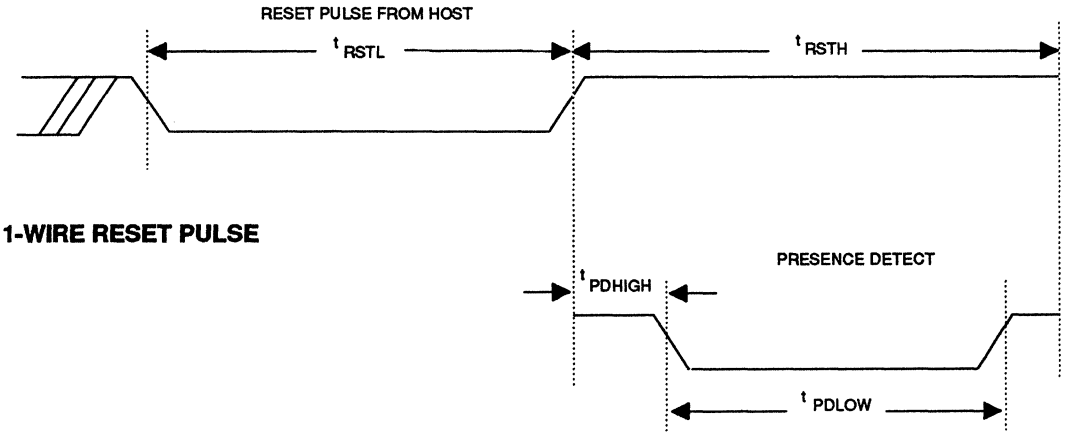
1-WIRE WRITE ZERO TIME SLOT Figure 19



1-WIRE READ TIME SLOTS Figure 20



1-WIRE PRESENCE DETECT Figure 21



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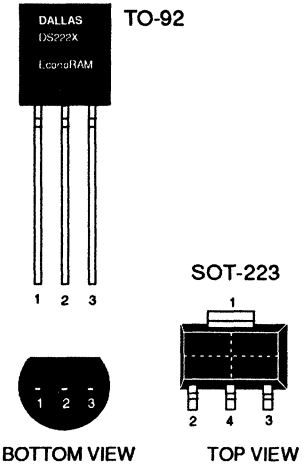
DALLAS SEMICONDUCTOR

DS2223/DS2224
EconoRAM

FEATURES

- Low-cost, general-purpose, 256-bit memory
  - DS2223 has 256-bit SRAM
  - DS2224 has 32-bit ROM, 224-bit SRAM
- Reduces control, address and data interface to a single pin
- Each DS2224 32-bit ROM is factory-lasered with a unique serial number
- Minimal operating power: 45 nanocoulombs per transaction @1.5V typical
- Less than 15nA standby current at 25°C
- Nonvolatile data retention easily achieved via low-cost alkaline batteries or capacitors
- Directly connects to a port pin of popular microcontrollers
- Operation from 1.2 to 5.5 volts
- Popular TO-92 plastic transistor package
- Operates over industrial temperature range -40° to +85°C

PACKAGE OUTLINE



See Mechanical Drawings Section 16, pgs. 18 & 19

PIN CONNECTIONS

Pin 1	GND	- Ground
Pin 2	DQ	- Data In/Out
Pin 3	V_{CC}	- Supply
Pin 4	GND	- Ground

ORDERING INFORMATION

DS2223	256-bit SRAM - TO-92 Package
DS2223Z	256-bit SRAM - SOT-223 Package
DS2223T	1000 piece tape-and-reel of DS2223
DS2223Y	2500 piece tape-and-reel of DS2223Z
DS2224	32-bit serial number (ROM), 224-bit SRAM - TO-92 Package
DS2224Z	32-bit serial number (ROM), 224-bit SRAM - SOT-223 Package
DS2224T	1000 piece tape-and-reel of DS2224
DS2224Y	2500 piece tape-and-reel of DS2224Z
DS2224-XXX	Portion of ROM code has a custom code -TO-92 Package
DS2224Z-XXX	Portion of ROM code has a custom code-SOT-223 Package
DS2224T-XXX	1000 piece tape-and-reel of DS2224-XXX
DS2224Y-XXX	2500 piece tape-and-reel of DS2224Z-XXX

DESCRIPTION

The DS2223 and DS2224 EconoRAMs are fully static, micro-powered, read/write memories in low-cost TO-92 packages. The DS2223 is organized as a serial 256 x 1 bit static read/write memory. The DS2224's first 32 bits are lasered in with a unique ID code at the time of manufacture; the remaining 224 bits are static read/write memory. Signaling necessary for reading or writing is reduced to just one interface lead.

OPERATION

All communications to and from the EconoRAM are accomplished via a single interface lead. EconoRAM data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction. **Note that once a specific transaction has been initiated, either a read or a write, it must be completed for all memory locations before another transaction can be started.**

WRITE TIME SLOTS

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one-microsecond recovery time between individual write cycles.

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot. (See Figure 1.)

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot. (See Figure 2.)

READ TIME SLOTS

The host generates read time slots when data is to be read from the EconoRAM. A read time slot is initiated when the host pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the EconoRAM is then valid for the next 14 microseconds minimum. The host therefore must stop driving the DQ pin to read its state one to 15 microseconds from the start of the read slot (see Figure 3). At some point between 15 and 60 microseconds into the read time slot, the DQ pin will pull back high via the external pullup resistor (30 microseconds typically). All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

COMMAND WORD

The command word consists of 8 bits that are transmitted LSB first from the host to the EconoRAM with write time slots (see Figure 4). The first bit of the command word is set to a logic 1 level. This indicates to the EconoRAM that a command word is being written. The next two bits are the select bits which denote the physical address of the EconoRAM that is to be accessed (set to 00 currently). The remaining five bits determine whether a read or a write operation is to follow. If a write operation is to be performed, all five bits are set to a logic 1 level. If a read operation is to be performed, any or all of these bits are set to a logic 0 level. All eight bits of the command word are transmitted to the EconoRAM with a separate time slot for each bit.

READ OR WRITE TRANSACTION

Read or write transactions are performed by initializing the EconoRAM to a known state, issuing a command word, and then generating the time slots to either read EconoRAM contents or write new data. Each transaction consists of 264 transaction time slots. Eight are for the command word and 256 are for the data bits being transferred. (See Figure 5.) Once a transaction is started, it must be completed for all memory bits before another transaction can begin.

To initially set the EconoRAM into a known state, 264 Write Zero time slots must be sent to it. These Write Zero time slots will not corrupt the data in the EconoRAM since a command word has not been written. This operation will increment the address pointer internal to the EconoRAM to its maximum count value. Upon reaching this maximum value, the EconoRAM will ignore all additional Write Zero time slots issued to it and the internal address pointer will remain locked at the top count value. This condition is removed by the reception of a Write One time slot, typically the first bit of a command word.

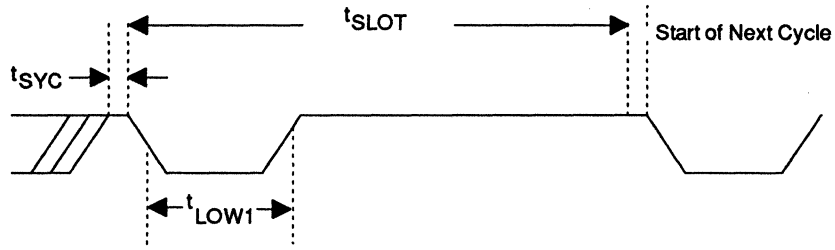
Once the EconoRAM has been set into a known state, the command word is transmitted to the EconoRAM with eight write time slots. This resets the address pointer internal to the EconoRAM and prepares it for the appropriate operation, either a read or a write.

After the command word has been received by the EconoRAM, the host initiates the appropriate data transfer operation. In the case of a read transaction, the host issues 256 read time slots. In the case of a write transaction, the host issues 256 write time slots. As stated previously, these time slots, either read or write, cannot be intermixed within the same transaction cycle.

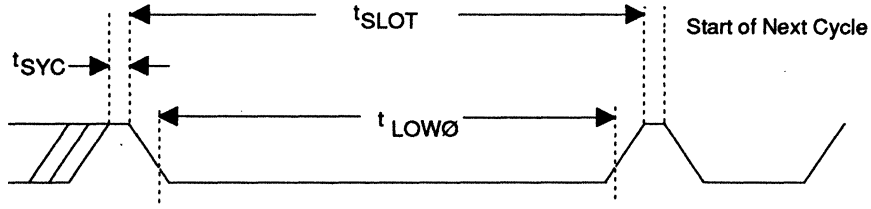
HOST SYSTEM INTERFACE

The host system must have an open drain driver with a pull-up resistor of approximately 5K ohms to system V_{cc} on the data signal line. The EconoRAM has an internal open-drain driver with a 500K ohm pull-down resistor to ground (see Figure 8). **The open-drain driver allows the EconoRAM to be powered by a small standby energy source, such as a single 1.5 volt alkaline battery, and still have the ability to produce CMOS/TTL output levels.** The pulldown resistor holds the DQ pin at ground when the EconoRAM is not connected to the host.

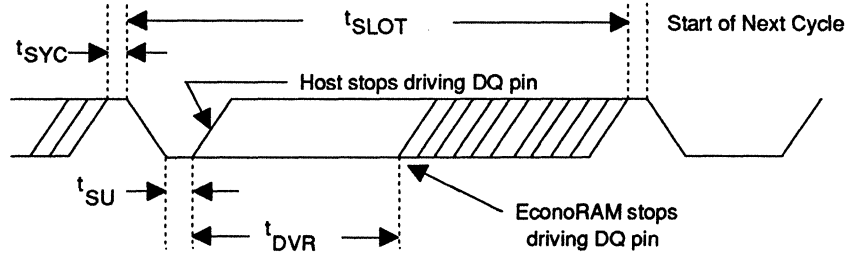
WRITE ONE TIME SLOT Figure 1



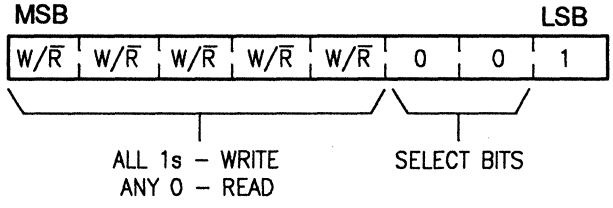
WRITE ZERO TIME SLOT Figure 2



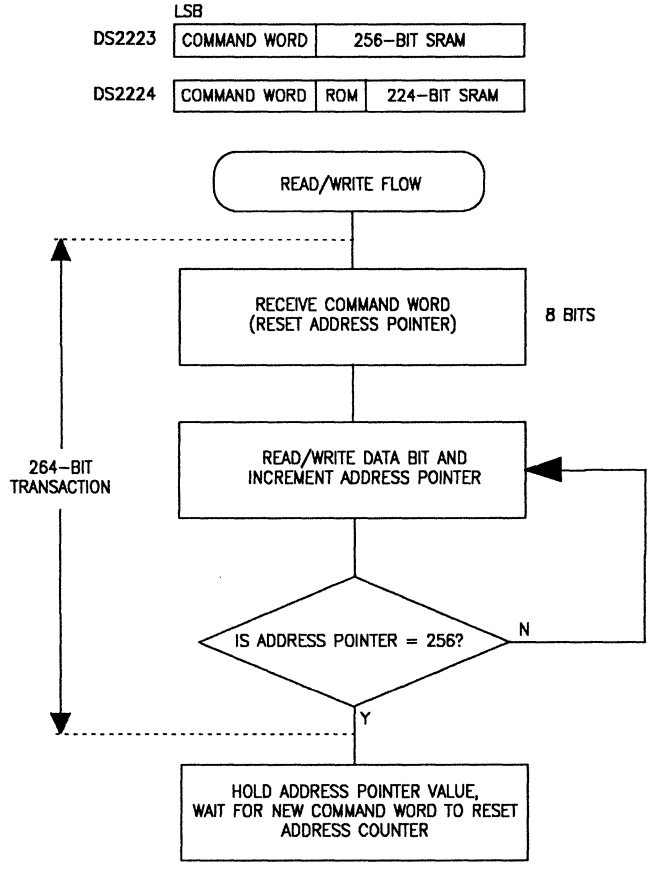
READ DATA TIME SLOTS Figure 3



COMMAND WORD Figure 4



READ/WRITE TRANSACTION Figure 5



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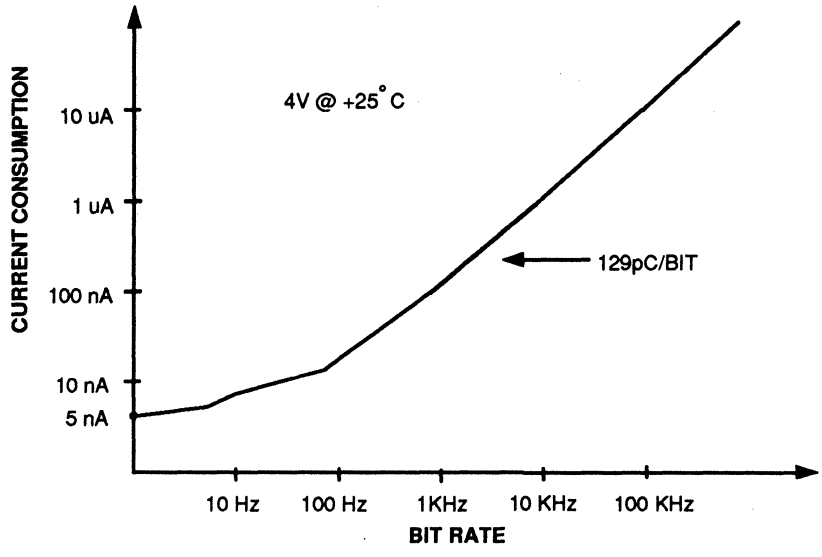
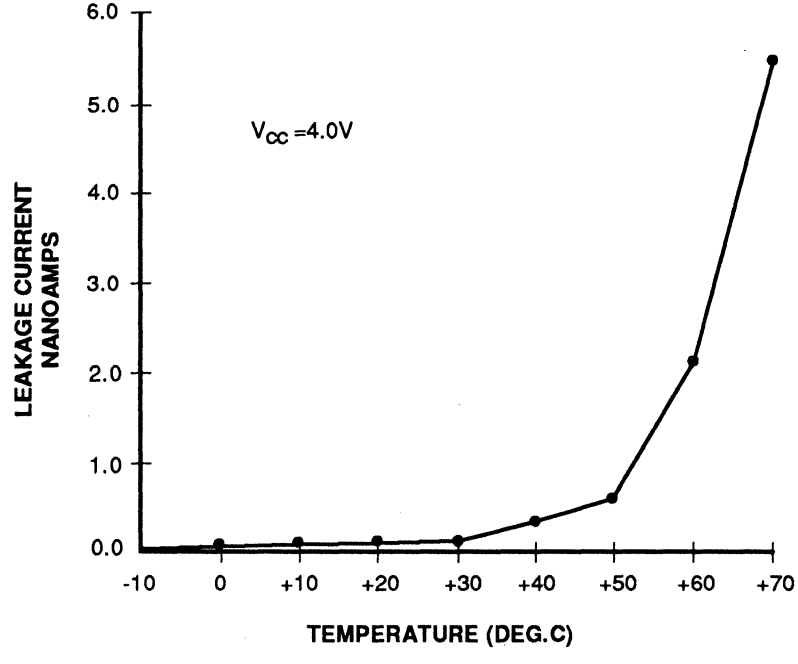
TYPICAL CURRENT CONSUMPTION VS. BIT RATE Figure 6



TYPICAL LEAKAGE CURRENT VS. TEMPERATURE Figure 7



ABSOLUTE MAXIMUM RATINGS

Voltage On Any Pin Relative to Ground	-0.5 to +6.5 Volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

RECOMMENDED DC OPERATING CONDITIONS (DS2223/DS2224 -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Pin	DQ	-0.5		6.0	Volts	1
Supply Voltage	V_{CC}	1.2		5.5	Volts	1

DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V_{CC} = 2.0 - 5.5V, -40° to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5	0.4	0.8	Volts	1
Input Logic High	V_{IH}	V_{CC}-0.5		6.0	Volts	1
Sink Current	I_L	1	2		mA	4
Output Logic Low	V_{OL}			0.4	Volts	1
Output Logic High	V_{OH}	V_{PUP}		5.5	Volts	1,2
Input Resistance	I_R		500K		Ohms	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		0.2	15	nA	6

DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V_{CC} = 1.4V ± 10%, -40° to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5		0.2	Volts	1
Input Logic High	V_{IH}	1.0		6.0	Volts	1
Sink Current	I_L	1	2		mA	7
Output Logic Low	V_{OL}			0.4	Volts	4
Output Logic High	V_{OH}	V_{PUP}		5.5	Volts	1,2
Input Resistance	I_R		500K		Ohms	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		12	25	nA	6

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.4V ± 10%, -40°to 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	70			µS	
Data Valid Read	t_{DVR}	1		15	µS	
Data Valid Write 1	t_{LOW1}	1		15	µS	
Data Valid Write Ø	$t_{LOWØ}$	60		15	µS	
Data Setup Time	t_{SU}	1		14	µS	
Frame Sync Time	t_{SYC}	1			µS	

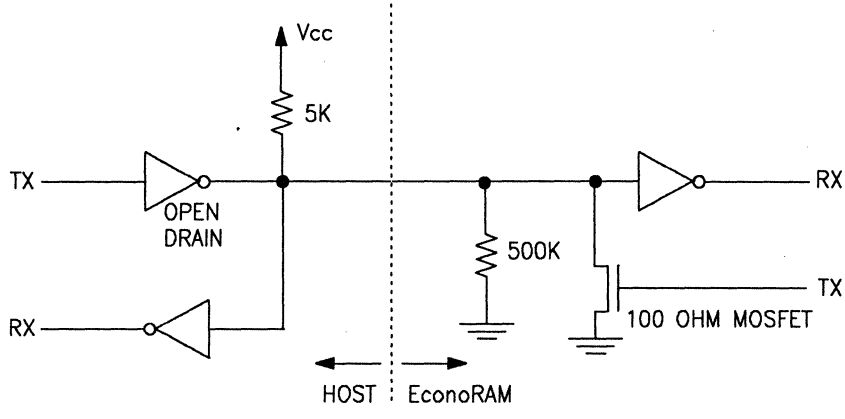
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, -40° to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60			µS	
Data Valid Read	t_{DVR}	1		15	µS	
Data Valid Write 1	t_{LOW1}	1		15	µS	
Data Valid Write Ø	$t_{LOWØ}$	60		15	µS	
Data Setup Time	t_{SU}	1		14	µS	
Frame Sync Time	t_{SYC}	1			µS	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull-up voltage to system supply.
3. Input pull-down resistance to ground.
4. @ V_{OL} = 0.4V.
5. 36 nanocoulombs per 264 time slots @ 1.5V (see Figure 6).
6. See Figure 7 for typical values over temperature.
7. @ V_{OL}= 0.2 V.

HOST TO EconoRAM INTERFACE Figure 8



APPLICATION EXAMPLES

Using Backup Capacitors

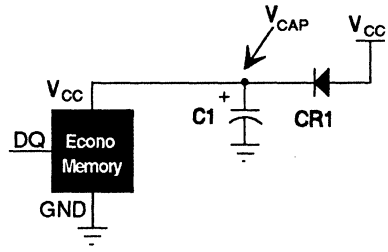
EconoRAMs are extremely conservative with power. Data can be retained in these small memories for as long as a month using the energy stored in a capacitor. Data is retained as long as the voltage on the V_{CC} pin of the EconoRAM (V_{CAP}) is at least 1.2 volts. A typical circuit is shown in Figure 9.

When V_{CC} is applied, capacitor C1 is charged and the EconoRAM receives power directly from V_{CC}. After power is removed, the diode CR1 prevents current from leaking back into the system, keeping the capacitor charged.

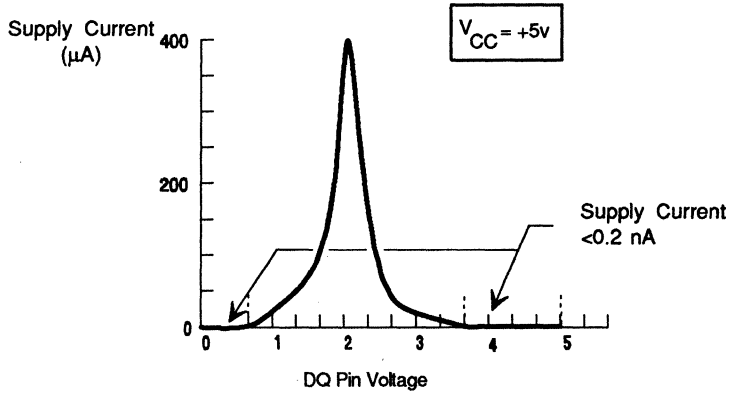
In the standby mode, the EconoRAM typically consumes only 12nA at 25°C. However, the power-down process of the system can cause a slightly higher current drain. This is due to the fact that as system power ramps down, the signal attached to the DQ pin of the EconoRAM transitions slowly through the linear region, while the V_{CAP} voltage remains at its initial value. While in this region, the part draws more current as a function of the DQ pin voltage (see Figure 10).

The data retention time can be estimated with the aid of Figure 11. In this figure, the vertical axis represents the value of the capacitor C1; the horizontal axis is the data retention time in hours. The two curves represent initial V_{CAP} voltages of 3 and 5 volts. These curves are based on the assumption that the time the DQ pin is in the linear region is less than 100 mS.

SUGGESTED CIRCUIT Figure 9

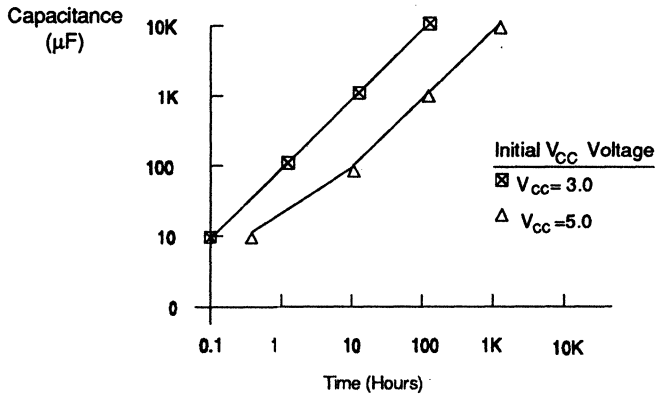


ICC VS. DQ VOLTAGE Figure 10



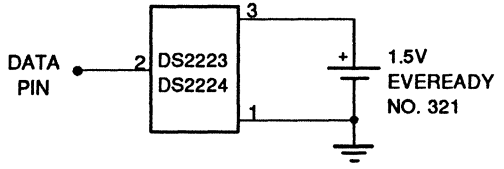
12

DATA RETENTION TIME VS. CAPACITANCE Figure 11



Using Battery Backup

14mA-Hr => 144 million transactions



DALLAS SEMICONDUCTOR

DS2400
Silicon Serial Number

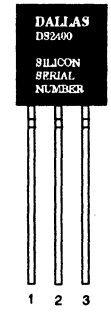
FEATURES

- Unique 48-bit silicon serial number gives 10^{14} combinations
- Factory lasered and tested, no two parts alike
- 8-bit cyclic redundancy check ensures error-free reading
- 8-bit model number references DS2400 communications requirements to system
- Presence detect indicates to the system when first contact is made
- Low-cost TO-92 package and optional surface mount option
- Reduces control, address, and data to a single pin
- Zero standby power required
- Directly connects to one port pin for microprocessor interface
- Pulse width measurement determines 1's or 0's
- Power derived from data line
- Applications
  - PCB Identification
  - Local Area Network I.D.
  - Software Protection
- Operates over industrial temperature range -40° to +85°C

DESCRIPTION

The DS2400 Silicon Serial Number contains an 8-bit family code, a unique 48-bit serial number, and an 8-bit cyclic redundancy check value embedded in silicon. Signaling necessary for reading or writing is reduced to just one interface lead. The familiar TO-92 package provides a small, low-cost enclosure. Power for reading and writing is derived from the data line itself with no need for an external power source.

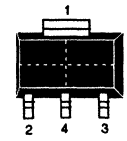
PIN DESCRIPTION



TO-92

BOTTOM VIEW

SOT-223



TOP VIEW

See Mechanical Drawings Section 16, pgs. 18 & 19

PIN NAMES

Pin 1	Ground
Pin 2	Data (DQ)
Pin 3	No Connect
Pin 4	Ground

ORDERING INFORMATION

DS2400	TO-92 Package
DS2400Z	SOT-223 Surface Mount Package
DS2400T	1000 piece tape-and-reel of DS2400
DS2400Y	2500 piece tape-and-reel of DS2400Z
DS2400-XXX	Portion of serial number has a custom code-TO-92 Package
DS2400Z-XXX	Portion of serial number has a custom code -SOT 223 Package
DS2400T-XXX	1000 piece tape-and-reel of DS2400-XXX
DS2400Y-XXX	2500 piece tape-and-reel of DS2400Z-XXX

OPERATION

All communication to and from the DS2400 Silicon Serial Number is accomplished via a single interface lead. Data contained within the DS2400 is accessed through the use of time slots and a 1-Wire protocol. Power to the part is derived from the high going pulse at the beginning of a write or read time slot.

WRITE TIME SLOTS

A write time slot is initiated when the system pulls the data line from a high logic level to a low logic level. There are two types of write time slots: write one and write zero. All write slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond sync pulse between individual write cycles.

For the system to generate a write one time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (see Figure 1).

For the system to generate a write zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (see Figure 2).

READ TIME SLOTS

The system generates read time slots when data is to be read from the DS2400. A read time slot is initiated when the system pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of 1 microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the DS2400 data must be read by the system within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (see Figure 3). All read time slots must be a minimum of 60 microseconds in duration and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond sync pulse between individual read time slots.

1-WIRE PROTOCOL

To communicate with the DS2400 a specific protocol is utilized. The 1-Wire protocol consists of four separate states which are used to reset the device, issue a command word, read the type identifier number, and read the unique silicon serial number and CRC byte (see Figure 4).

To initially set the DS2400 into a known state, a reset pulse must be sent to it. The reset pulse is a logic low generated by the system which must remain low for a minimum of 480 microseconds and then be followed by a 480 microsecond logic high level (see Figure 5). During this 480 microsecond high time the DS2400 will assert a presence detect signal. This signal is generated by the DS2400 and consists of a logic low level which is held for a maximum of 240 microseconds and minimum of 60 microseconds. This signal can be used to detect that a DS2400 is attached to the 1-wire interface after the issuance of a reset command.

Once the DS2400 has been set into a known state, the command word is transmitted to the DS2400 with eight write time slots. The command word for the DS2400 is a hexadecimal **0F**.

Upon recognition of the command word, the DS2400 is ready to respond to the next eight read time slots with the type identifier number. This number is a hexadecimal **01**.

After the system receives the type identifier number, the DS2400 is ready to output the unique 48-bit serial number contained within the device. The system must issue 48 read time slots to retrieve this number. Following the 48-bit serial number is an 8-bit cyclic redundancy check value. This CRC value has been calculated over the type identifier and serial number (56 bits) and is lasered into the part at the time of manufacture. To read the CRC value the system must issue eight read time slots. To stop reading at any time the system can issue a reset pulse.

CRC GENERATION

To validate that the transmitted data from the DS2400 has been received correctly by the system, a comparison of the system-generated CRC and the received DS2400 CRC must be made. If the two CRC values match, the transmission was error-free. An example of how to generate the CRC using software is shown in Table 1. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure **DO_CRC** given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and **DO_CRC** is called to update the CRC variable. After all the data has been passed to **DO_CRC**, the variable CRC will contain the result. For a detailed explanation of the CRC computation, see Application Note #27, "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

RECOMMENDED SYSTEM INTERFACE

The system must have an open drain driver with a pullup resistor of approximately 5K ohms to Vcc on the data signal line. The DS2400 has an internal open drain driver with a 500K ohm pulldown resistor to ground. The pulldown resistor holds the data input pin at ground potential when the DS2400 is not connected to a 1-Wire interface (see Figure 6).

CUSTOM DS2400

The DS2400 is available with portions of the 48-bit serial number defined by the customer. These special parts are designated DS2400-XXX. The custom 48-bit number has three specific subfields of which Dallas Semiconductor will assign a customer ID number in the most significant 12 bits. The next most significant 20 bits are selectable by the customer as a starting value, and the least significant 16 bits are non-selectable and will increment by one, starting at 0000h. Certain quantities and conditions apply, contact your Dallas Semiconductor sales representative for more information.

ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC             ; save the accumulator
            PUSH    B               ; save the B register
            PUSH    ACC             ; save bits to be shifted
            MOV     B,#8            ; set shift = 8 bits
                                    ;
CRC_LOOP:   XRL     A,CRC           ; calculate CRC
            RRC     A               ; move it to the carry
            MOV     A,CRC           ; get the last CRC value
            JNC     ZERO            ; skip if data = 0
            XRL     A,#18H          ; update the CRC value
                                    ;
ZERO:       RRC     A               ; position the new CRC
            MOV     CRC,A           ; store the new CRC
            POP     ACC             ; get the remaining bits
            RR      A               ; position the next bit
            PUSH    ACC             ; save the remaining bits
            DJNZ    B,CRC_LOOP      ; repeat for eight bits
            POP     ACC             ; clean up the stack
            POP     B               ; restore the B register
            POP     ACC             ; restore the accumulator
            RET
```

1-WIRE WRITE TIMING Figure 1

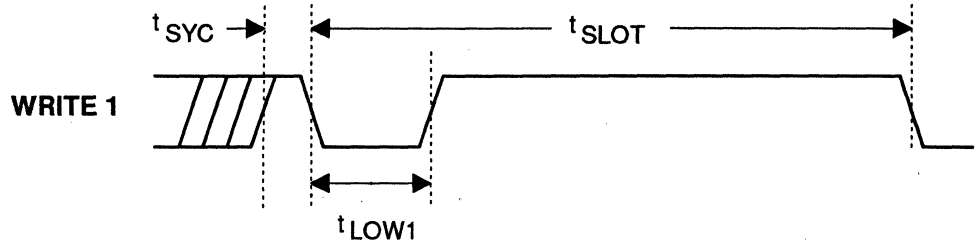
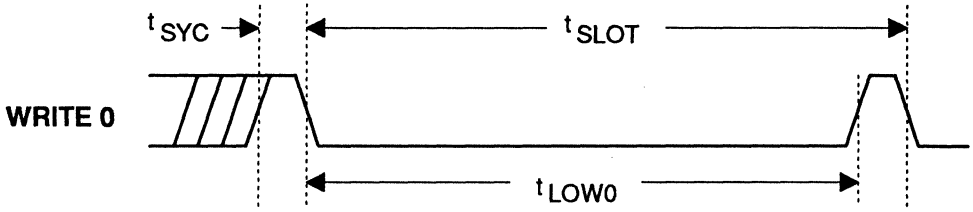


Figure 2



1-WIRE READ TIMING Figure 3A

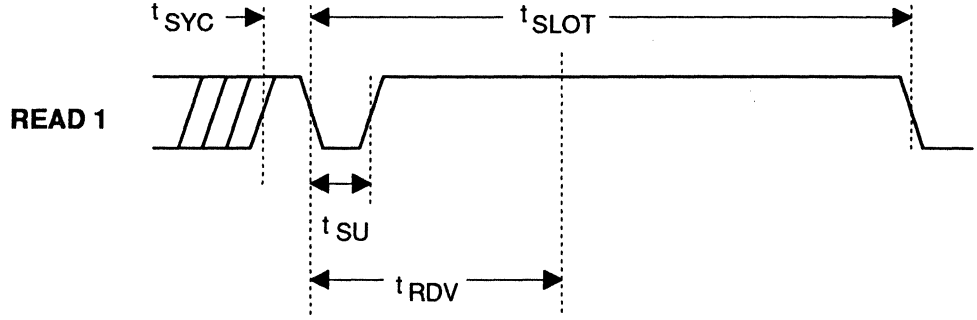
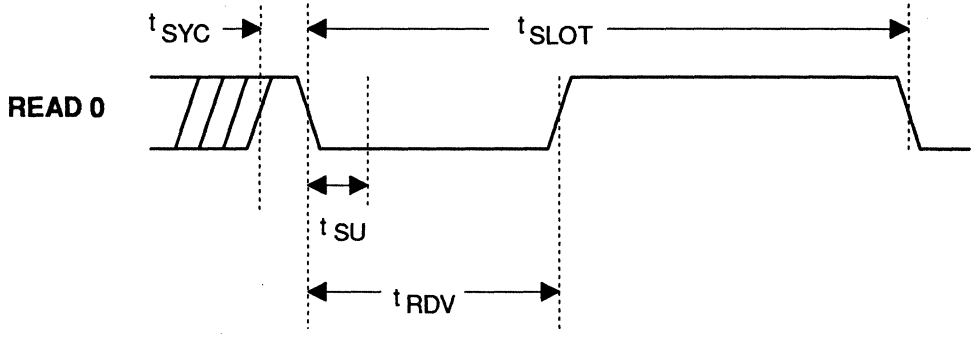
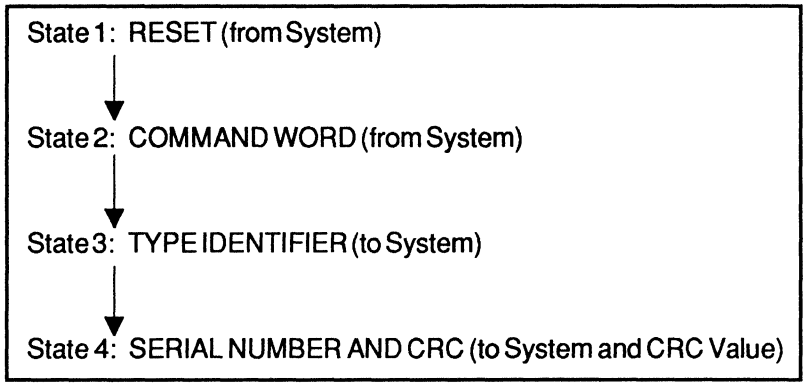


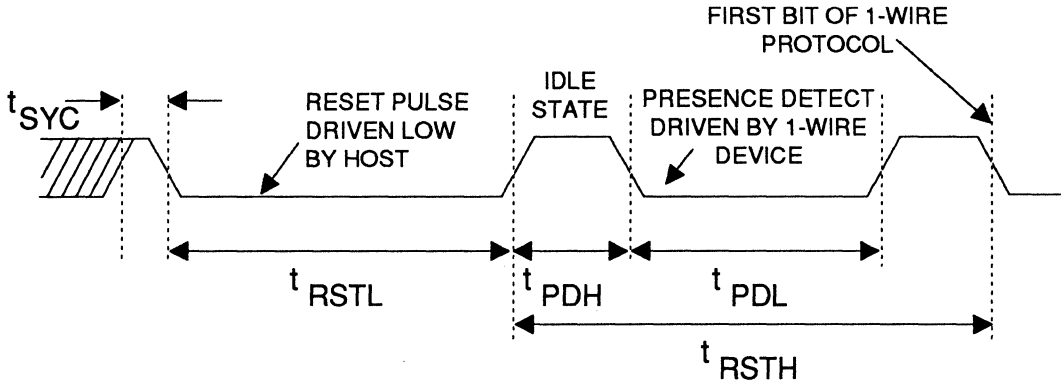
Figure 3B



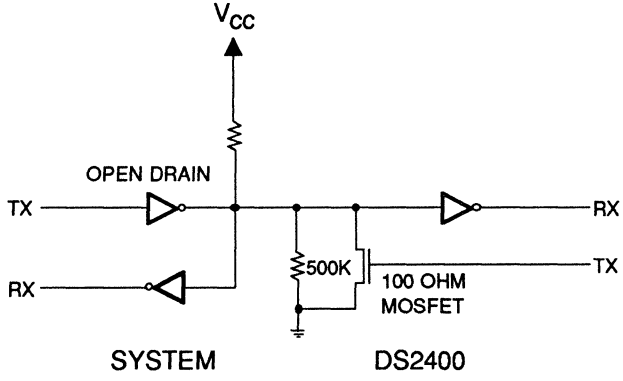
1-WIRE PROTOCOL Figure 4



RESET PULSE/PRESENCE DETECT Figure 5



RECOMMENDED SYSTEM TO DS2400 INTERFACE Figure 6



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ABSOLUTE MAXIMUM RATINGS*

Voltage On Data Pin Relative to Ground	-0.5 to +7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5		5.5	Volts	1
External Pullup Voltage	V_{CC}	4.5		5.5	Volts	

DC ELECTRICAL CHARACTERISTICS

(V_{PUP} = 5V ± 10%, -40°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5		0.4	Volts	1,6
Input Logic High	V_{IH}	3.0	5.0	5.5	Volts	1,6,7
Sink Current	I_L	-1.0			mA	4,6
Output Logic Low	V_{OL}			0.4	Volts	3,6
Output Logic High	V_{OH}			5.5	Volts	3,6
Input Resistance	I_R		500K			2
Operating Charge	I_{OP}			30	nC	5,6

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C, V_{PUP} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot Period	t_{SLOT}	60		120	µS	
Write 1 Low Time	t_{LOW1}	1		15	µS	
Write 0 Low Time	t_{LOW0}	60		120	µS	
Read Data Valid	t_{RDV}			15	µS	
Read Data Setup	t_{SU}	1			µS	8
Frame Sync	t_{SYC}	1			µS	
Reset Low Time	t_{RSTL}	480			µS	
Reset High Time	t_{RSTH}	480			µS	
Presence Detect High	t_{PDH}	15		60	µS	
Presence Detect Low	t_{PDL}	60		240	µS	

NOTES:

1. All voltages are referenced to ground.
2. Input is pulled to ground.
3. @1 mA.
4. @ V_{OUT} = 0.4V.
5. 30 nanocoulombs per 72 time slots @ 5.0V.
6. @V_{CC} = 5.0 volts with a 5K pullup to V_{CC} and a maximum time slot of 120 µs.
7. V_{IH} is a function of the external pullup resistor and the V_{CC} supply.
8. Read data setup time refers to the time the host must pull the 1-Wire pin low to read a bit. Data is guaranteed to be valid within 1µS of this falling edge and will remain valid for 14µS minimum (15µS total from falling edge on 1-Wire).

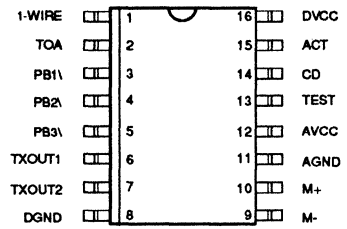
DALLAS SEMICONDUCTOR

DS2569S
Touch/Proximtiy Memory Chip

FEATURES

- Identification by touch contact or wireless link
- 512-bit read/write data memory
- 1-Wire touch pin for programming and reading all configuration and data memory
- Low-level input signal automatically trips a self-clocked output pin for modulating a wireless transmitting device (150-19,200 Hz)
- 3 pushbutton input pins manually trip the output pin to send different partitions of data memory
- Data transmissions are time-slotted to allow multiple devices to be read in the same field
- Laser-trimmed input receiver processes signals as small as 10 mVp-p
- Less than 2 µA of standby current enables long battery life
- 64-bit ROM provides a unique, unalterable serial number via the 1-Wire pin
- Chip architecture is compatible with Dallas Semiconductor 1-Wire Touch Protocol

PIN DESCRIPTION



16-PIN SOIC
(300 MIL)

See Mechanical Drawings
Section 16, pg. 6

PIN NAMES

1-WIRE	1-Wire interface port
TOA	Time out adjust
PB1-3\	Pushbutton inputs; active low
TXOUT1	Transmit data output 1
TXOUT2	Transmit data output 2
M+, M-	Differential receiver input
ACT	Device activity output
CD	Carrier detect; active high
TEST	Test function; leave this pin open
DGND	Digital ground
DVCC	Digital supply
AVCC	Analog supply
AGND	Analog ground

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DESCRIPTION

The DS2569S is a 512-bit serial memory intended for 1-Wire touch or wireless identification applications. Data transmissions are triggered either by a low-level input signal sensed by an on-chip receiver or by a logic low on any of the pushbutton inputs. The memory is organized as three128-bit minor partitions and one 512-bit major partition which can overlap the other three. The length of each partition may specified to be any value less than the maximum. Data is clocked out of the major partition onto the TXOUT1 pin using either the input signal or an on-chip clock source. The three minor partitions clock data out with the internally generated clock onto the TXOUT1/TXOUT2 pins when the proper levels are presented to PB1\, PB2\ or PB3\. The configuration options and data memory can be programmed and read using the 1-Wire interface pin.

MEMORY ORGANIZATION

The DS2569S contains a serial read/write memory that is organized into 4 sections: a major partition up to 512 bits and three separate minor partitions, each up to 128 bits long. The exact length of each memory is programmed by control bits in the configuration register which is accessed through the 1-WIRE pin. The major partition data is transmitted out the TXOUT1 pin when triggered by reception of a low-level signal at M+ and M- as described later. Data in a minor partition is transmitted when a corresponding pushbuttion input pin (PB1-3\) is pulled to a logic low. The lengths of the major and minor partitions are completely independent from each. Any or all minor partitions may overlap the major partition, although the minor partitions are completely separate from each other (see Figure 2).

WIRELESS TRANSMITTER OPERATION - CW MODE

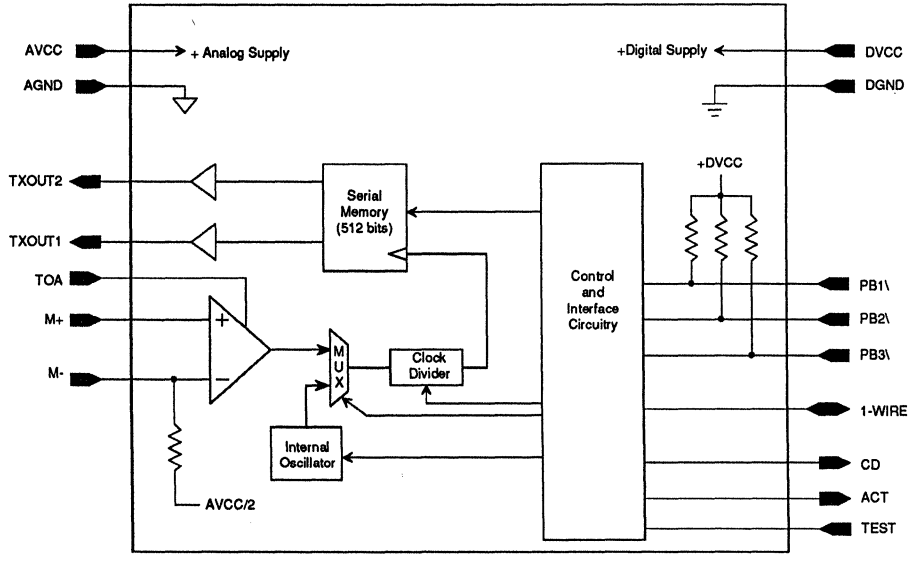
If the DS2569S is configured in the continuous wave (CW) mode, data in the major partition is clocked out the TXOUT1 pin using the input signal present at M+ and M-. Data in all cases is transmitted in the NRZ data format (i.e., data in valid for the entire clock period) and LSB first. A clock edge occurs on every positive signal transition of M+ relative to M-. This clock signal is fed to a programmable divider (N=1-512) whose output is used to clock major partition data. The DS2569S will cycle through the major partition 1 time and then will pause for a pseudo-random number (4 to 11) of partition cycles before restarting the data output. This random timeout scheme allows multiple devices to be read even though they are both in close proximity to each other. After 5 seconds from being triggered, the data output is disabled for a minimum of 30 seconds. When the 30 seconds have expired, the DS2569S can be retriggered for a new transaction only if the input signal at M+, M- has gone away for more than 250 usec, although this time can be increased by attaching an external capacitor on the TOA pin according to the following equation:

Time out period = $C/(1.5 \times 10^{-7})$
where the period is in Seconds and C is in Farads

WIRELESS TRANSMITTER OPERATION - SS MODE

When the DS2569S is configured in single-shot (SS) mode and at least one cycle is presented to M+ and M-, data is output onto the TXOUT1 pin using the internally generated clock. This clock is configurable over a range of frequencies from 150Hz to 19200Hz as shown in Table 3. The DS2569S will cycle through the major partition one time and then pause for a pseudo-random number (4 to 11) of partition cycles. If a signal is detected during the 4-11 pause time, the DS2569S will transmit another 1 on, 4-11 off pattern. This operation continues until the input signal disappears or the 5 second timeout expires as in the CW mode (with the resultant 30 second transmit disable). The input signal must also disappear for at least 250 usec to be retriggered, adjustable via the TOA pin.

DS2569S BLOCK DIAGRAM Figure 1



PUSHBUTTON OPERATION

When any of the pushbutton inputs (PB1-3\) are pulled to a logic 0, data in a minor partition is output onto the TXOUT1 pin using the internally generated clock, irregardless of the CW/SS selection. The entire data of a minor partition is transmitted 4 times; the DS2569S then waits for that input to return high. When the pushbutton input is returned high, the minor partition data will be transmitted 4 more times, except that the data will be complemented. This positive-edge detection is buffered and may occur during the initial 4 passes through the partition. Additionally, the next low/high sequence is buffered to allow for "double clicking" of the push button. The push button inputs are debounced which requires that successive negative edges be separated by at least 80 usec. Pushbutton operation takes precedence over any data transmission triggered by a signal at M+ and M-. Each pushbutton input activates a specific partition as shown in Table 1.

TXOUT1/2 CLOCK SOURCE Table 1

PB3\	PB2\	PB1\	PARTITION	MODE	TXOUT1/TXOUT2 CLOCK
1	1	1	MAJOR	CW	Derived from received signal
1	1	1	MAJOR	SS	Internal
X	X	0	MINOR 1	CW/SS	Internal
X	0	1	MINOR 2	CW/SS	Internal
0	1	1	MINOR 3	CW/SS	Internal

MAJOR PARTITION LASERABLE BITS

The first 96 bits (bits 0-95) of the major partition serial memory can be optionally programmed by the laser at the factory. Contact the marketing department for details about custom programming services. Otherwise, these bits will behave as normal read/write static memory.

TXOUT2 OUTPUT

The DS2569S offers a second data output called TXOUT2. The TXOUT2 transmits the same data as TXOUT1 at the start of a transmission; however TXOUT2 only cycles through the active partition for 4 times. TXOUT2 goes then to an inactive state (low) until retriggered by a new signal at M+, M- or any of the pushbutton inputs.

CARRIER DETECTION

When a valid signal is present at the M+ and M- receiver inputs, the CD (Carrier Detect) pin will transition high. The CD pin will remain high until the input signal disappears. Internal filtering integrates the input signal over several cycles before activating CD.

ACTIVITY PIN

The activity pin goes high whenever the any of the memory partitions are being cycled.

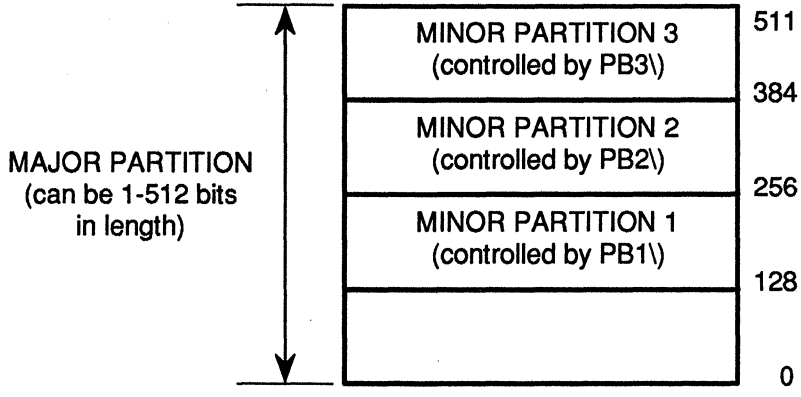
FRESHNESS SEAL

The DS2569 can be placed into a very-low power mode by using the freshness seal bit in the configuration register. If this bit is set to a 1, the internal power supply to the input receive opamp is disconnected, minimizing current consumption (all other circuitry remains powered). Clearing the freshness seal bit to a 0 reactivates the comparator. This feature is intended to conserve battery power when a part using the DS2569S is not in actual use (i.e., stored in inventory).

1-WIRE INTERFACE

The DS2569S has a 1-Wire communication port through which the memory may be accessed and the configuration options programmed and read. This port uses a pulse-width modulation technique for communication. Similiar to Morse code, a host system drives the input pin to a low state for varying periods of time to send a logic 0, a logic 1, a reset signal or to receive data from the DS2569S. All operations through this port are preceded by the logic and timing operations as detailed by Application Note 23, "Using the 1-Wire Protocol". Once the 1-Wire protocol has been satisfied, communications with the DS2569S's memory are initiated by sending a 24-bit command word. The 8-bit family code for the DS2569S (required by the 1-wire protocol) is **69** Hex.

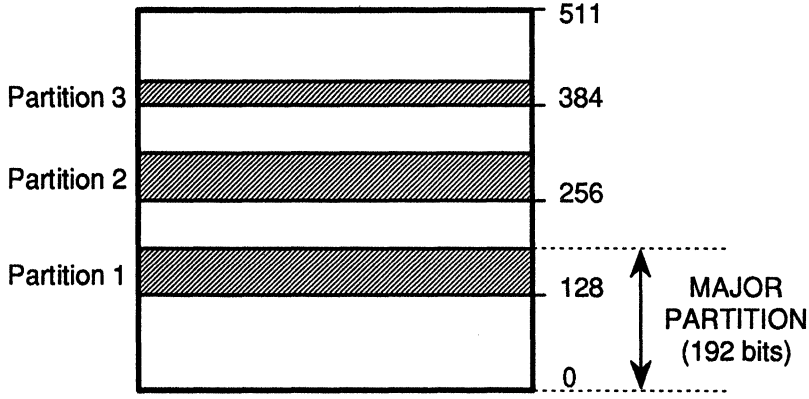
MEMORY ORGANIZATION Figure 2



MINOR PARTITION 1 BEGINS AT BIT POSITION 128
MINOR PARTITION 2 BEGINS AT BIT POSITION 256
MINOR PARTITION 3 BEGINS AT BIT POSITION 384

EXAMPLE:

Minor partitions 1 and 2 have been programmed to be 64 bits long, minor partition 3 to be 32 bits long and the major partition programmed to be 192 bits long.



COMMAND WORD

The command word is a 24-bit sequence of logic 0's and 1's which specify the operation to be performed by the device. There are six possible operations: Read Data, Write Data, Lock Data, Set Configuration, Verify Configuration or Lock Configuration. The bit sequences are detailed in Table 2.

READ DATA

If the command word issued to the DS2569S specifies a Read Data operation then the device will output the entire 512-bit memory in a serial fashion. A single read cycle consists of the host driving the input pin from a high to low state, holding it there for a period of 1uS, and then releasing the pin so the DS2569S may drive data. If a logic zero is being driven the low state will be retained on the pin for 15-70 usec after the falling edge was input. A logic 1 will return the pin to high state in a period of time after release determined by the external pullup resistor (typically, about 2 usec).

WRITE DATA

The Write Data command allows the entire 512 bit data memory to be written in a serial fashion. The data is input after the command word using the same convention for sending logic 0's and 1's as the command word.

LOCK DATA

Once issued, the Lock Data command prevents any further Write Data operations to the memory. This command is a one time only command and its effect cannot be reversed unless the power supply is removed from the part and reattached.

SET CONFIGURATION

The Set Configuration allows those registers which determine the user defined options to be set. The data is written to all registers serially according to Table 3.

VERIFY CONFIGURATION

The Verify Configuration command allows the configuration registers to be read in serial fashion in the same manner as the Read Data operation. Refer to Table 3 for the specific bit locations.

LOCK CONFIGURATION

Once issued, the Lock Configuration command prevents any further modification of the configuration registers. This command is a one-time only command and its effect cannot be reversed unless the power supply is removed and reattached.

COMMAND WORDS Table 2

COMMAND	UPPER	MIDDLE	LOWER
READ DATA	AA	AA	A3
WRITE DATA	AA	AA	5C
LOCK DATA	50	50	AF
READ CONFIG	AA	AA	AC
WRITE CONFIG	AA	AA	53
LOCK CONFIG	50	50	50

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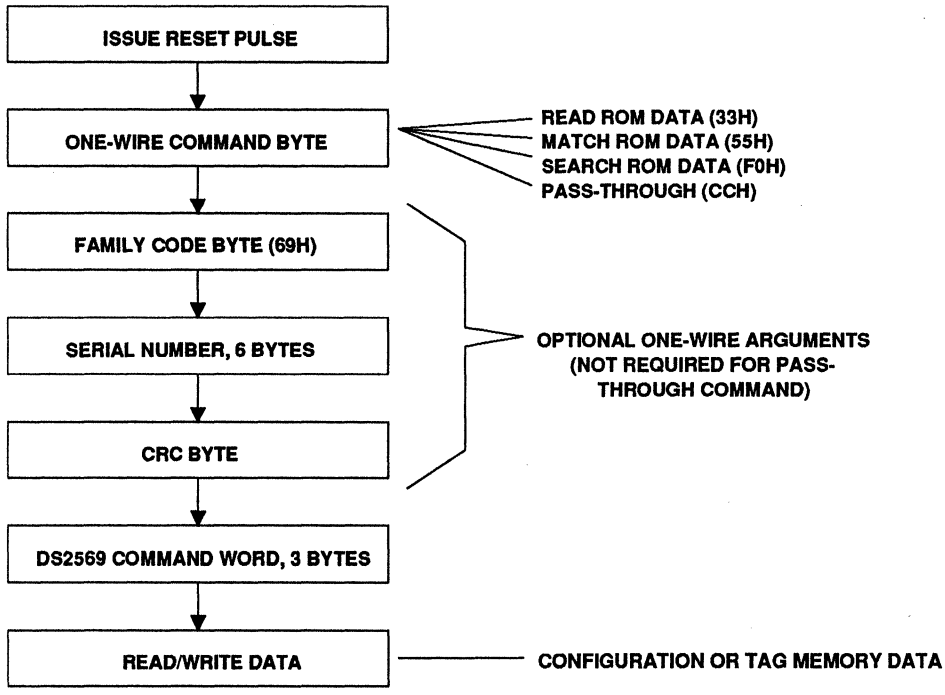
1-WIRE COMMAND SEQUENCE Figure 3



CONFIGURATION REGISTER Table 3

BIT(DEC) FUNCTION

00 CW/SS Mode (1=CW; 0=SS)

01-09 MAJOR PARTITION LENGTH (1 - 512 bits); BIT 01 = LSB

MSB LSB	PARTITION LENGTH
000000000 =	1 bit long
000000001 =	2 bits long
000000010 =	3 bits long, etc.

10-16 These bits should be programmed to 0000000.

17-23 PARTITION 1 LENGTH (1 - 128 bits); BIT 17 = LSB

24-30 PARTITION 2 LENGTH (1 - 128 bits); BIT 24 = LSB

31-37 PARTITION 3 LENGTH (1 - 128 bits); BIT 31 = LSB

MSB LSB	PARTITION LENGTH
00000000 =	1 bit long
00000001 =	2 bits long
00000010 =	3 bits long, etc.

38-40 PUSHBUTTON/SINGLE SHOT MODE BAUD RATE

BIT 40	BIT39	BIT38	BAUD RATE (Hz)
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1,200
1	0	1	2,400
1	1	0	4,800
1	1	1	9,600
0	0	0	19,200

41 FRESHNESS SEAL (1=on; 0=off)

42-50 DIFFERENTIAL CLOCK DIVIDER RATIO

BIT50 BIT42	DIVIDER RATIO
000000000	= Divide by 1
000000001	= Divide by 2
● ● ●	● ● ●
111111111	= Divide by 512

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to 7.0V
Operating Temperature	-40°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply input	DVCC, AVCC	2.5		6.5	Volts	
Input Logic 1 DVCC> 3.4V	V_{IH1}	2.2			Volts	
Input Logic 1 DVCC< 3.4V	V_{IH2}	DVCC-1.2V			Volts	
Input Logic 0	V_{IL}	-0.3		0.8	Volts	

DC ELECTRICAL CHARACTERISTICS

(-40°C to 70°C, AVCC=DVCC= 2.5 to 6.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage Cur.	I_{IL}	-1.0		+1.0	uA	
Output Current High	I_{OH1}	-1.0			mA	V_{OH}= DVCC-0.5 V
Output Current High (TXOUT1/2 only)	I_{OH2}	-10.0			mA	V_{OH}= DVCC-0.5 V
Output Current Low	I_{OL1}			+4.0	mA	V_{OL}= 0.4V
Output Current Low (TXOUT1/2 only)	I_{OL2}			+10.0	mA	V_{OL}= 0.4V
Comparator Sensitivity (M+, M-)	C_{SEN}	10			mVp-p	1
Comparator Frequency (M+, M-)	C_{FREQ}	40		250	Khz	
Comparator Input Resistance	C_{IR}	1			Mohm	
Input Capacitance	C_{IO}			5	pF	
Operating Current	I_{CC1}		100	150	µA	2
Standby Current	I_{CC2}			2.0	µA	3
Standby Current	I_{CC3}			100	µA	Freshness bit = 1

NOTES:

1. Measured with 133 KHz sine wave at M+, M-.
2. M+, M- fed with 250 KHz sine wave at 100 mV p-p (a-c coupled).
3. M+, M- both shorted together; 1-WIRE pin = GND.

1-WIRE AC CHARACTERISTICS

(-40°C to 70°C, DVCC=2.5 TO 6.5 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot Period	t_{SLOT}	60		120	msec	
Write 1 Low Time	t_{LOW1}	1		15	msec	
Write 0 Low Time	t_{LOW0}	60		120	msec	
Read Data Valid	t_{RDV}	15			µsec	
Read Data Setup	t_{SU}	1			µsec	1
Frame Sync	t_{SYC}	1			µsec	
Reset Low Time	t_{RSTL}	480			µsec	
Reset High Time	t_{RSTH}	480			µsec	
Presence Detect High	t_{PDH}	15		60	µsec	
Presence Detect Low	t_{PDL}	60		240	µsec	

AC ELECTRICAL CHARACTERISTICS

(-40°C to 70°C, DVCC=2.5 TO 6.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Retrigger Time Out Tolerance	t_{RTT}	-20		+20	%	
Retrigger Time Out	t_{RTO}	200	250	300	µsec	2
Transmission Time before Squelch	t_{TTS}	3.8	4.3	5.0	sec	3
Squelch Time	t_{SQU}	30.0	37.5	40.0	sec	4
Internal Clock Accuracy	t_{ICA}	-10		+10	%	5
Carrier Detect Delay	t_{CDD}		2.5		µsec	6
Debounce Time	t_{DT}	80	100		µsec	7

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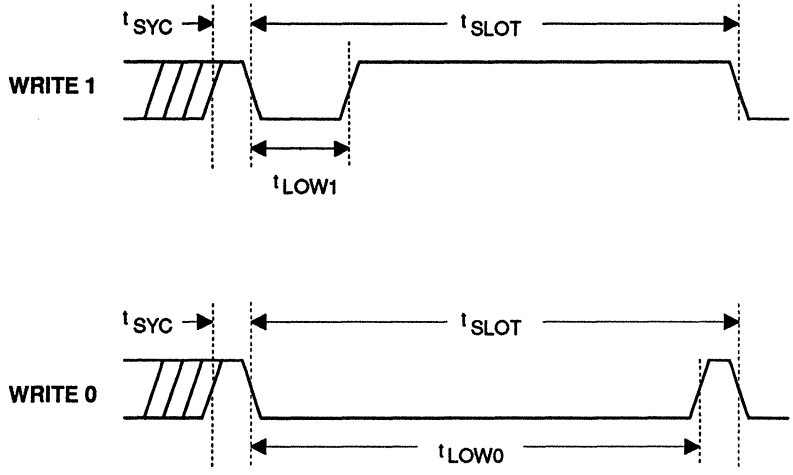
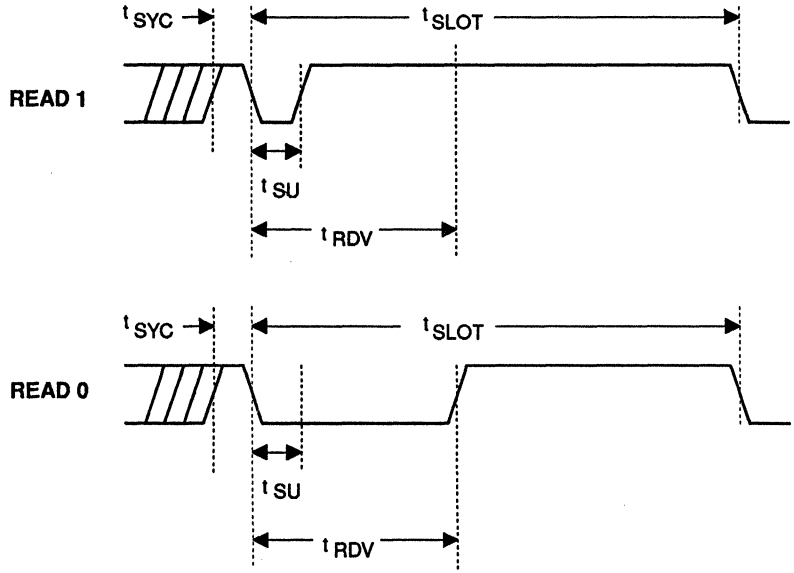
NOTES:

1. Read data setup time refers to the time the host must pull the 1-WIRE pin low to read a bit. Data is guaranteed to be valid within 1 usec of this falling edge and will remain valid for 14 usec minimum (15 msec total from falling edge presented to 1-WIRE pin).
2. This specification refers to the time that the input receiver must be quiet before the DS2569S can be retrigered for a data transmission. The TOA pin is assumed to be open.
3. This specification refers to the maximum continuous data transmission time for TXOUT1/2 outputs before being automatically squelched.
4. This specification refers to the length of the automatic squelch time in which TXOUT1/2 are disabled.
5. Refers to the internal clock frequency used in the SS mode and for pushbutton operation.
6. Delay from beginning of signal at M+, M- to rising edge at CD pin.
7. Minimum debounce time for PB1\, PB2\ and PB3\ pushbutton inputs.

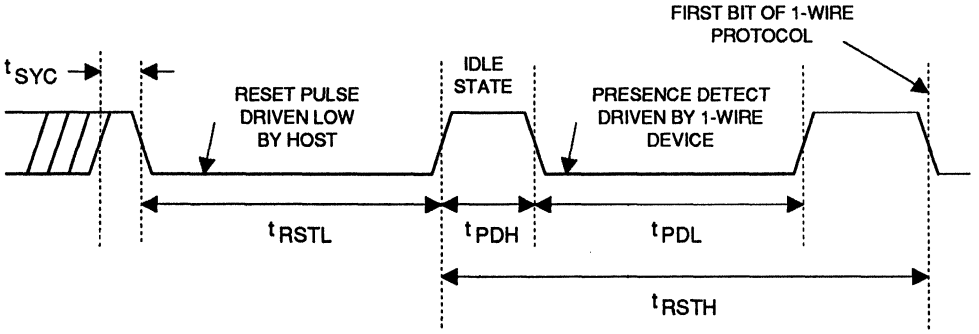
1-WIRE WRITE TIMING Figure 4



1-WIRE READ TIMING Figure 5



1-WIRE RESET/PRESENCE DETECT TIMING Figure 6



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DALLAS SEMICONDUCTOR

DS9092
Touch Memory Probe

FEATURES
- Simple, low-cost metal stampings form a read/write probe for the Touch Memory family
- Probe guides the entry of the Touch Memory
- Touch Memory slides over the surface to self-clean contacts
- Accessible shallow probe cavity simplifies removal of debris such as mud
- Flexible design supports panel mount or hand-grip mount with optional tactile feedback
- Bright tarnish-resistant metal surface provides millions of operations
- Panel-mount probe, pre-wired for easy installation
- Hand-grip probe mates to RJ-11 jack for quick installation

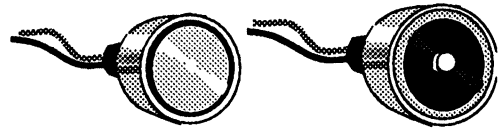
DESCRIPTION
The DS9092 Touch Memory Probe provides the electrical contact necessary for the transfer of data to and from the DS199x family of Touch Memories. The round probe shape provides a self-aligning interface that readily matches the circular rim of the Touch Memory MicroCan. Metal contacts resist wear and are easy to keep clean.

The DS9092 is available with a flat face plate (standard) or with optional tactile feedback. The center contact of the standard reader has no moving parts, making this a more rugged interface for harsh environments. This type of probe is best suited for designs where the Touch Memory is brought into contact with the reader. The tactile feedback probe is ideal for situations where the Touch Memory is stationary and the movable reader is brought in contact with it.

Both types of probes are available in a panel-mount version. The tactile feedback probe is also available in a grip-mount version. The panel-mount probes are fastened with a rear-locking clip ring.

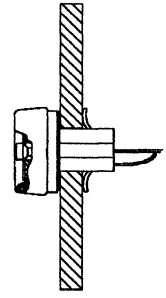
Two 6-inch 22AWG wires are provided for easy connection to the system microcontroller. The hand-grip mount probe comes attached to a 4-inch handle and one-meter cable which is terminated with an RJ11 jack.

PACKAGE DESCRIPTIONS



Standard
DS9092

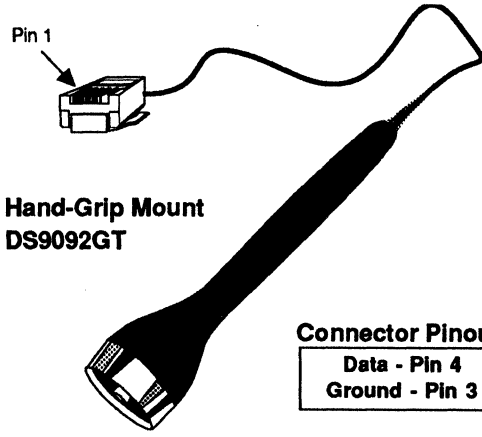
Tactile Feedback
DS9092T



Wire Code

Data - Gray
Ground - Black

Panel Mounting



Hand-Grip Mount
DS9092GT

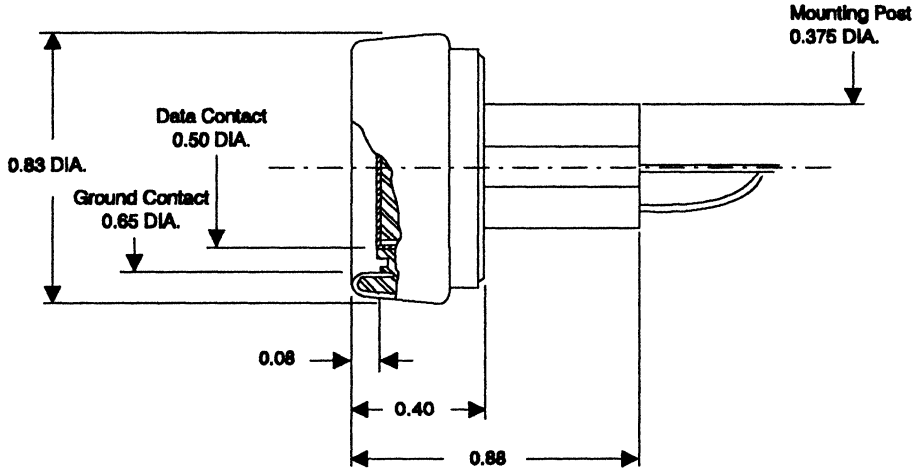
Connector Pinout

Data - Pin 4
Ground - Pin 3

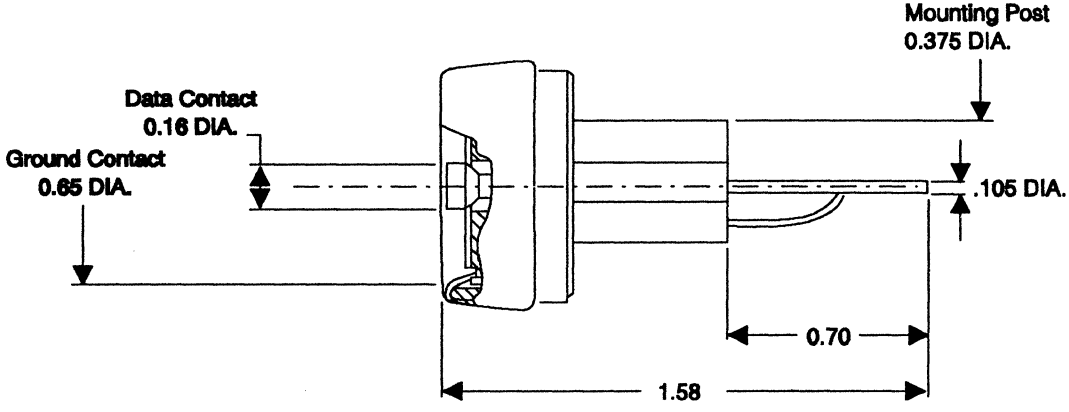
ORDERING INFORMATION

DS9092	- Panel-mount probe, solid face
DS9092T	- Panel-mount probe with tactile feedback
DS9092GT	- Hand-grip mount with tactile feedback

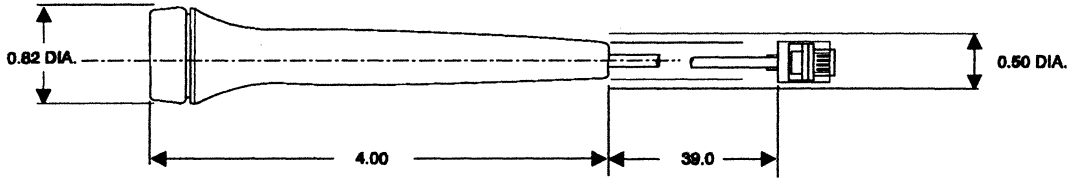
STANDARD TOUCH PROBE Figure 1



OPTIONAL TACTILE FEEDBACK Figure 2

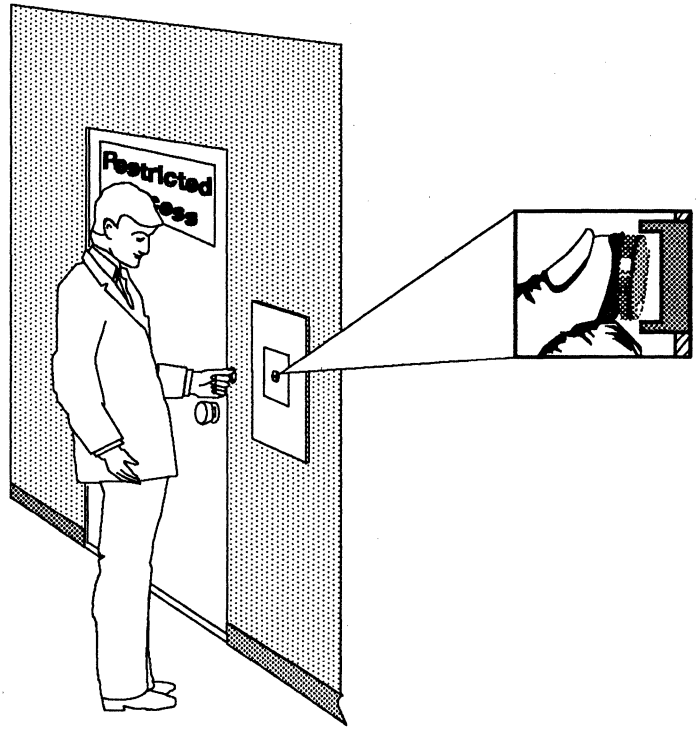


OPTIONAL HAND-HELD WAND Figure 3

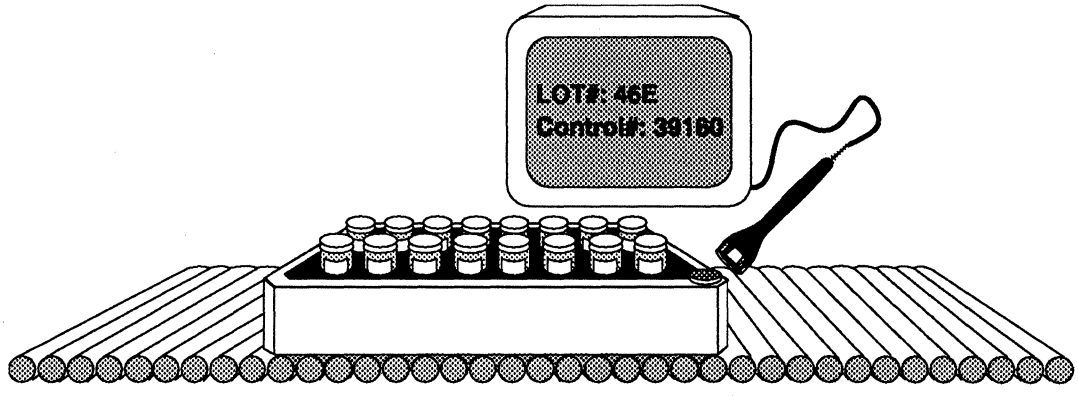


NOTE:
All dimensions are in inches.

TOUCH APPLICATIONS



Door Access Figure 4a



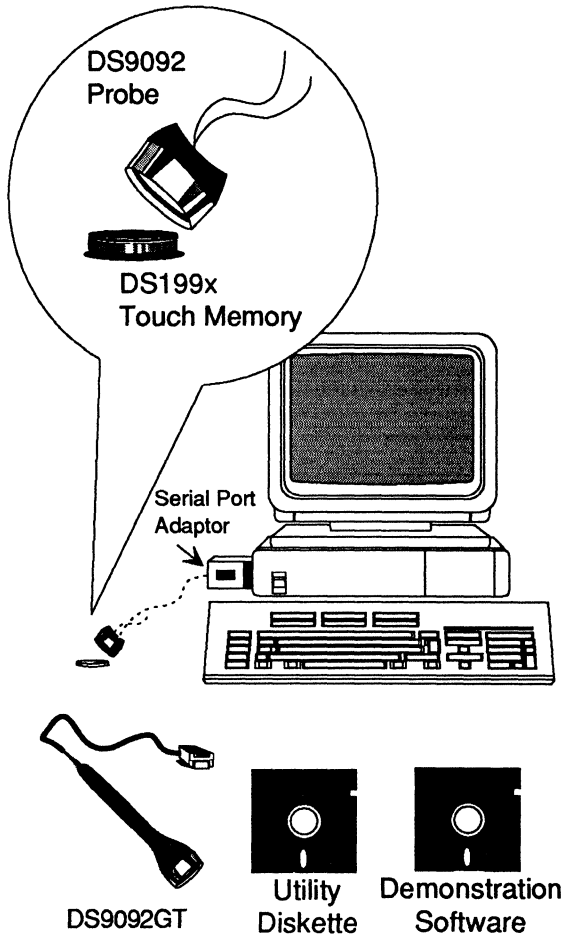
Inventory Control Figure 4b

DALLAS SEMICONDUCTOR

DS9092K
Touch Memory Starter Kit

FEATURES

- Evaluation kit for accessing DS199x Touch Memories from an IBM PC-compatible computer
- Two DS1990 Touch Serial Numbers, one DS1991 Touch Multikey, one DS1993 4K-bit Touch Memory, one DS1994 4K-bit Touch Memory Plus Time
- DS9092 Touch Memory Probe
- DS9092GT Touch Memory Probe with Hand-grip
- Assortment of Touch Memory attachment accessories; DS9093, DS9093F, DS9093S, DS9094F, DS9096
- DS9097 PC serial port adaptor
- PC demonstration software on 5 1/4" diskette
- 5 1/4" diskette of utility functions and source code
- Data sheets and application notes



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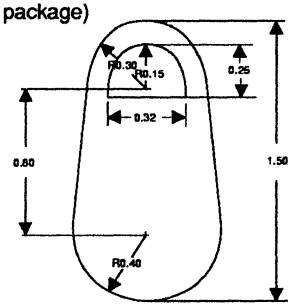
DESCRIPTION

The DS9092K Touch Memory Starter Kit provides hardware and software for quick evaluation of any of Dallas Semiconductor's Touch Memory family using a PC-compatible DOS computer. Included in the kit are 5 Touch Memory devices, a DS9092 and DS9092GT Touch Probe, a PC serial port adaptor, an assortment of Touch Memory attachment accessories, demonstration software and utility programs. The demonstration programs can be executed to read or write a Touch Memory device through a serial port via a 25-pin adaptor which connects to the DS9092 probe. The utility disk allows the user to quickly develop his own Touch Memory programs from the code provided.

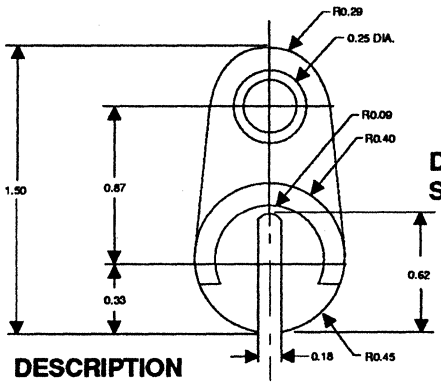
DALLAS SEMICONDUCTOR

DS9093
Touch Memory Mount

FEATURES
- Two keyring mount versions:
  - DS9093 flat fob for peel and stick mounting of rounded rim MicroCan (R3 package)
  - DS9093F snap-in fob for use with flanged MicroCan (F5 package)
- Two permanent mount versions:
  - DS9093S allows a Touch Memory to be easily and permanently attached to an object using screws or rivets. (F5 package)
  - DS9093P has a locating pin and a single mounting hole for permanent attachment. (5F package)

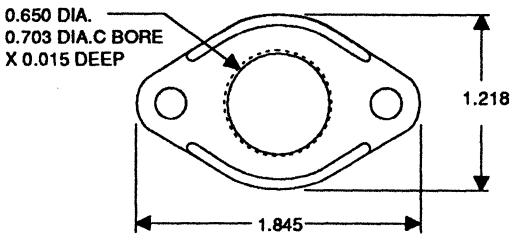


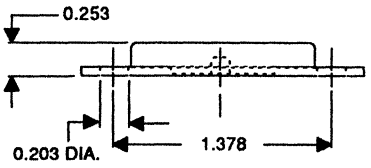
DS9093



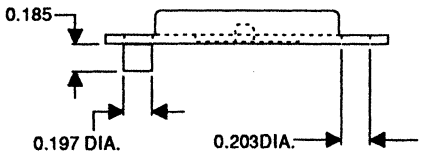
DS9093F
Snap-In

DIMENSIONS





DS9093S



DS9093P

DESCRIPTION

The DS9093 Touch Memory Mount offers the user a low-cost plastic fixture that holds a Touch Memory for thumbpad applications or permanent attachment to an object.

The DS9093 flat fob offers the simplest way to mount a Touch Memory for applications that require only momentary contact. The DS9093F snap-in fob is more versatile and works in captive reader applications where extended communication with the Touch Memory is required. Both fobs can be attached to a keyring for carrying.

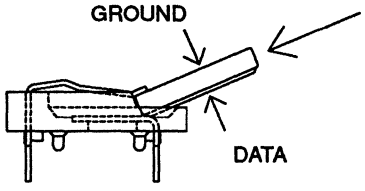
The DS9093S and DS9093P allows the user to permanently attach a Touch Memory to an object with one or two screws, rivets, etc. The plastic plate is designed with an inset that accommodates the flange on the F5 package and allows for flush mounting. A protective wall is provided along the sides of the plate to reduce incidental damage to the Touch Memory.

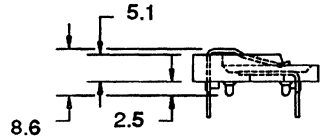
DALLAS SEMICONDUCTOR

DS9094
MicroCan Clip

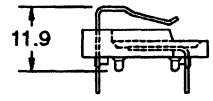
FEATURES

- Low cost holder for 16.3mm MicroCan
- Printed circuit board mount
- MicroCan contacts are 302 spring stainless steel
- Flammability rating: UL94V-O
- Three versions:
  - DS9094 for R3 MicroCan (round rim, 3.2 mm high)
  - DS9094F for F5 MicroCan (flanged rim, 5.8 mm high)
  - DS9094FS for surface mounting F5 MicroCan (flanged rim, 5.8 mm high)
- Printed circuit contacts are selectively tin-lead plated for improved solderability

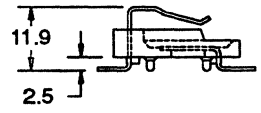




DS9094

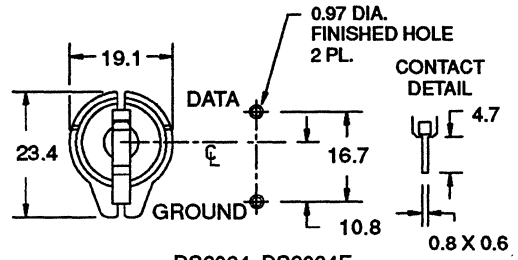


DS9094F



DS9094FS

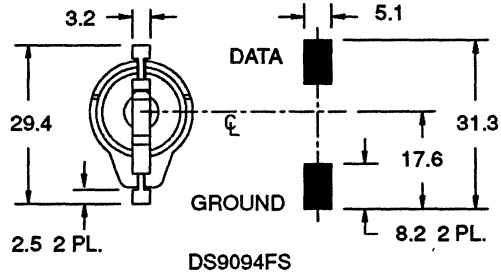
PC BOARD MOUNTING DETAILS



DS9094, DS9094F
RECOMMENDED HOLE SIZE

DESCRIPTION

The DS9094 Clip holds a MicroCan and connects to a printed circuit board. By deflecting the spring clip in the molded housing, a MicroCan can be inserted and extracted without special tools. If reverse insertion is attempted, the beveled edge on the housing prevents contact. The DS9094's low profile minimizes the clearance height above the printed circuit board.



DS9094FS
RECOMMENDED PAD SIZE

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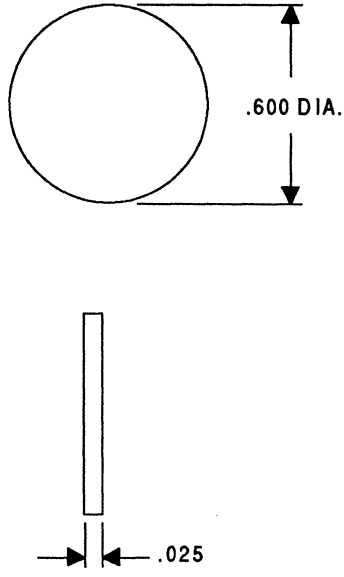
DALLAS SEMICONDUCTOR

DS9096
Touch Memory Adhesive Pads

FEATURES

- Low-cost attachment method for DS199x Touch Memory family
- Readily attaches Touch Memory to DS9093 or other smooth surface
- Two adhesion strengths
  - DS9096 for semi-permanent attachment requirements
  - DS9096P for permanent attachment
- Available in die-cut rolls of 500/roll

PACKAGE DESCRIPTION



(All measurements shown in inches)

DESCRIPTION

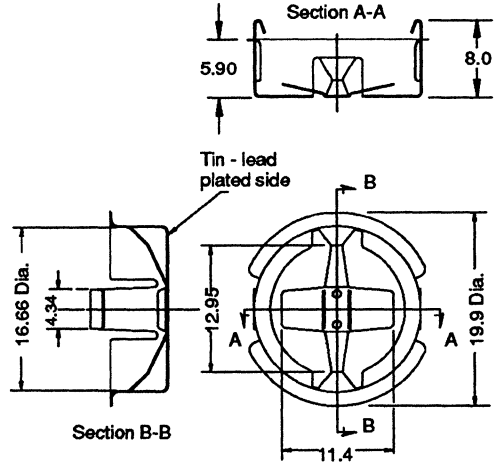
The DS9096 Touch Memory adhesive pad is a double-sided pad that is die-cut to match the diameter of the Touch Memory devices. The pads allow Touch Memories to be attached to virtually any smooth surface. The DS9096 allows for semipermanent attachment, but can be removed if necessary. The DS9096P offers a very permanent attachment method that is not intended to be removed. The pads are ideal for use in conjunction with the DS9093 keyring mount.

DALLAS SEMICONDUCTOR

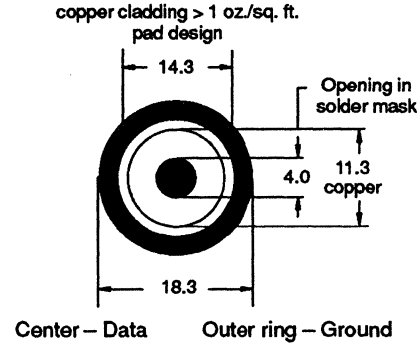
DS9098
MicroCan Retainer

FEATURES

- Compact single-piece, all-metal receptacle for MicroCan mounting
- Retainer withstands high temperatures required for surface mounting
- Center contact is permanently separated at first insertion of MicroCan
- Material is stainless steel with selective tin-lead plating for optimal solderability to printed circuit board
- Retainer to MicroCan connection is stainless steel to stainless steel
- Quadruple redundancy of contacts (4 plus 4)
- Contact force exceeds 200 grams for reliable connection
- At insertion, MicroCan is latched for retention
- Pops up for removal when latch is released
- >100 insertion/withdrawal cycles with no performance degradation
- Compatible with standard pick and place equipment; insensitive to angular orientation
- Cleaning fluids drain freely for quick clean up
- Available in tube packaging (DS9098) or in 32mm wide tape and reel (DS9098T)



Recommended Printed Circuit Layout Pads



All dimensions are in millimeters

DESCRIPTION

The DS9098 MicroCan Retainer is a low-cost, surface mount device that retains a 16.3mm x 5.8mm MicroCan on a printed circuit board. The slender design secures the MicroCan for a compact printed circuit board mount. The retainer latches the flange of the MicroCan and prevents reversed insertion.

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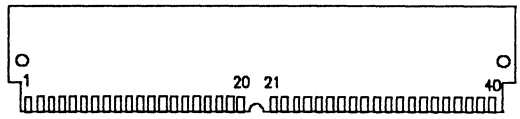
FULL DATA SHEET AVAILABLE — CALL 214-450-3836

DALLAS SEMICONDUCTOR

DS2250(T)
Soft Micro Stik

FEATURES
- Compatible with industry standard 8051 instruction set
- Nonvolatile SRAM for program and/or data
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip, full-duplex serial port
- Adjustable partition between program and data memory
- Completely crashproof: program/data RAM and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power-up/down
- Program and data memory secure, with a tamper-proof, on-chip encryptor
- DS2250T: Permanently powered clock/calendar
- 40-position SIMM connection scheme

PACKAGE OUTLINE



40-Pin SIMM

ORDERING INFORMATION

DS2250 XX—XX Soft Micro Stik
DS2250(T) XX—XX Soft Micro Stik

SPEED GRADE

8	8MHz
12	12MHz
16	16MHz

PROGRAM/DATA RAM

8	8 Kbytes
32	32 Kbytes
64	64 Kbytes

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DESCRIPTION
The DS2250 Soft Micro Stik and DS2250T Time Micro Stik are the functional equivalents of the DS5000 Soft Microcontroller and DS5000T Time Microcontroller, respectively, with the exception that both devices are available with 64 Kbytes of nonvolatile memory. The pinout and instruction set of both products match the industry standard 8051 microcontroller. The DS2250 and DS2250T each plug into a SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

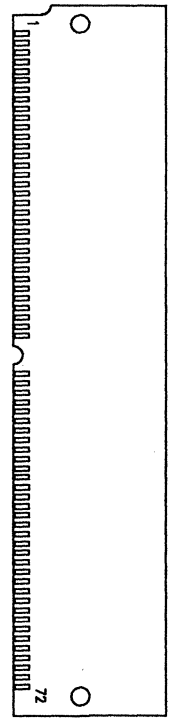
DALLAS SEMICONDUCTOR

DS2251(T)
128K Micro Stik

FEATURES

- 100% compatible with 8051 instruction set
- Up to 128K of nonvolatile SRAM onboard for program and data memory
- Bytewide address and data bus leaves port pins available
- Two peripheral chip enables access external devices via the bytewide bus
- Reprogrammable peripheral controller (RPC mode) emulates 8042 for PC bus applications
- Optional DS1283 Watchdog Timekeeper Chip allows wake-up from idle or stop mode (DS2251T)
- Flexible program loading from serial port or RPC mode peripheral bus
- Based on the DS5001FP Micro Chip
- 72-pin SIMM connection scheme

PACKAGE OUTLINE



72-Pin Stik

DESCRIPTION

The DS2251 128K Micro Stik is a complete 8051-compatible microcontroller system based on the DS5001FP 128K Micro Chip. The DS2251 supports all of the improved features that the DS5001FP offers over its DS5000 predecessor. These include expanded onboard memory and additional I/O functions.

The DS2251 incorporates up to 128K of nonvolatile SRAM onboard, accessed by the DS5001FP's bytewide address and data bus. This bus is added to a standard 8051 architecture and is available at the connector for user applications. The four standard 8051-compatible ports are also available and can be used without interference from memory access. Additional I/O circuits can also be memory mapped onto the bytewide bus by using the two decoded peripheral enable signals.

A Reprogrammable Peripheral Controller mode (RPC) brings the benefits of up to 128K nonvolatile RAM to the design of intelligent and flexible peripheral controllers through hardware emulation of the popular 8042 slave interface. This interface allows the DS2251 to reside as a peripheral on the bus of a more powerful processor.

A permanently powered timekeeping function, the DS1283 Watchdog Timekeeper, is incorporated into the DS2251T. This real time clock is driven by an onboard quartz crystal and keeps time to a hundredth of a second. In addition, the date is automatically adjusted at the end of the month, including those months with fewer than 31 days. Leap year compensation is also performed automatically. Access to the timekeeping function is performed entirely using the DS5001FP's bytewide bus.

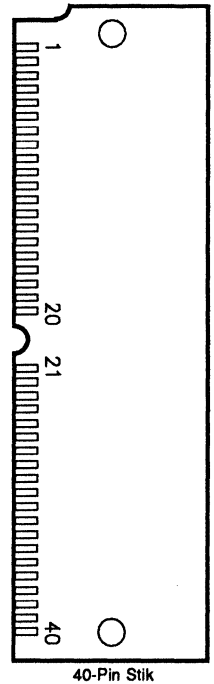
DALLAS SEMICONDUCTOR

DS2252(T)
Secure Micro Stik

FEATURES

- Enhanced firmware security
  - Stronger address/data encryptor
  - 64-bit internal encryption key
  - Automatic random key generation
  - SDI self-destruct input
  - Top-coating on die defeats microprobe
  - Customer-specific encryption available
- 100% compatible with 8051 instruction set
- Up to 128K of nonvolatile SRAM onboard for program and data memory
- Crashproof computer
  - Power-fail reset
  - Early-warning power-fail interrupt
  - Watchdog timer
- Optional DS1283 Watchdog Timekeeper Chip DS2252T
  - Permanently powered timekeeping
  - Programmable time of day interrupt
  - Programmable interval timer
- Hardware slave interface emulates 8042
- Flexible program loading from serial port or slave interface bus
- Based on the DS5002FP Secure Micro Chip
- 40-pin SIMM connection scheme

PACKAGE OUTLINE



40-Pin Stik

DESCRIPTION

The DS2252 Secure Micro Stik is a complete 8051-compatible microcontroller system based on the DS5002FP Secure Micro Chip. It combines the Micro Chip with up to 128K bytes of nonvolatile SRAM memory for program and data, and an optional real-time clock. Onboard program and data memory are accessed by the DS5002FP's bytewide secure memory bus, which is encrypted using an internal security key. Thus, the memory is secure against observation. This leaves the four 8051-type ports for user I/O, while still using the full memory map of the 8051. All security provisions of the DS5002FP chip are available in the DS2252. This includes memory encryption, random 64-bit encryption-key generation and self-destruct input for tamper protection. The details of these security functions are discussed in the DS5002FP data sheet, which is available under a nondisclosure agreement.

A permanently powered timekeeping function, the DS1283 Watchdog Timekeeper, is included in the DS2252T. This real-time clock is driven by an onboard 32 KHz crystal and keeps time to a hundredth of a second. Date is automatically adjusted at the end of the month, and leap year compensation is also performed. Access to the timekeeping function is performed entirely on the DS5002FP's memory bus.

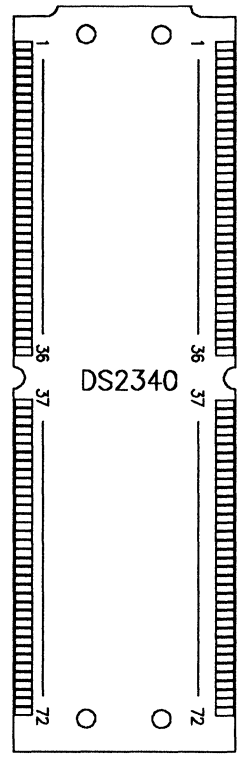
DALLAS SEMICONDUCTOR

DS2340(T)
Soft V40 Flip Stik

FEATURES

- V40-based embedded control system adapts to task-at-hand:
  - Up to 256K bytes of lithium-backed NV SRAM for program/data storage
  - Serial bootstrap loading of software
  - Code can be changed in end use
- Incorporates V40 family processor:
  - Executes industry-standard 8086 instruction set
  - On-chip timers, serial I/O, DMA, and interrupt control
  - Allows code development in native instruction set of IBM PC
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports
- DS2340T provides DS1283 Watchdog Timekeeper Chip
- Dual 72-pin SIMM connection scheme supports single-board or expanded operation

PACKAGE OUTLINE



72-Pin SIMM Double-edge Connector

DESCRIPTION

The DS2340 and DS2340T Soft V40 Flip Stiks are complete, 8086-compatible microcontroller systems that provide the benefits of adaptability, crashproof operation, and powerful I/O capabilities for embedded control applications in an extremely small form factor. These unique features are made possible by the incorporation of the DS5340 V40 Softener Chip. In addition, the DS2340(T) executes the native instruction set of the IBM PC, so that the PC can serve as a development platform for the Soft V40 Flip Stiks. As a result, a wide variety of high-level language compilers, assemblers, and debugging tools are available to support system designs based on the DS2340.

The DS2340(T) offers two SIMM card-edges to support single-board and expanded operations. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support the selected operation. Connector A supports single-board operation. This card edge provides a total of three 8-bit parallel I/O ports. One of these ports allows each pin to serve as an interrupt input. The other two ports can be configured as a high-speed interface to allow the DS2340(T) to act as a peripheral controller to a host microprocessor system.

FULL DATA SHEET AVAILABLE — CALL 214-450-3836

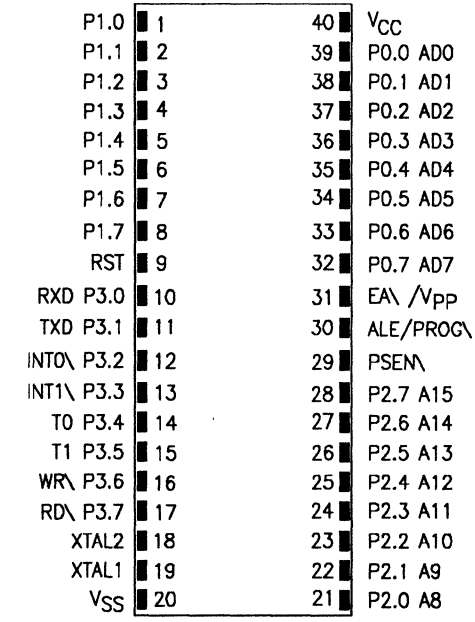
DALLAS SEMICONDUCTOR

DS5000
Soft Microcontroller

FEATURES

- 8-bit uC adapts to task-at-hand:
  - 8 or 32 Kbytes of high performance nonvolatile RAM for program and/or data memory storage
  - Initial downloading of software in end system via on-chip serial port
  - Capable of modifying its own program and/or data memory in end use
  - 128 internal nonvolatile registers for variable retention
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{cc}
  - Orchestrates orderly shutdown and automatic restart on power up/down
  - Automatic restart on detection of errant software execution
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip, full-duplex serial I/O ports
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout

PIN CONNECTIONS



40-Pin Encapsulated Package

ORDERING INFORMATION

DS5000 XX - XX

MAX. Clock Frequency
- 08 8Mhz
- 12 12Mhz
- 16 16MHz

Program/Data RAM
- 08 8 Kbytes
- 32 32 Kbytes

DESCRIPTION

The DS5000 Soft Microcontroller is a high performance 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{cc}. The entire program/data memory space is implemented using high speed, nonvolatile static CMOS RAM. Two memory size versions are available which offer either 8 Kbytes or 32 Kbytes of NV RAM for program/data storage. Furthermore, internal data registers and key configuration registers are also nonvolatile.

A major benefit resulting from its nonvolatility is that the Soft Microcontroller allows program memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the program and data memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution.

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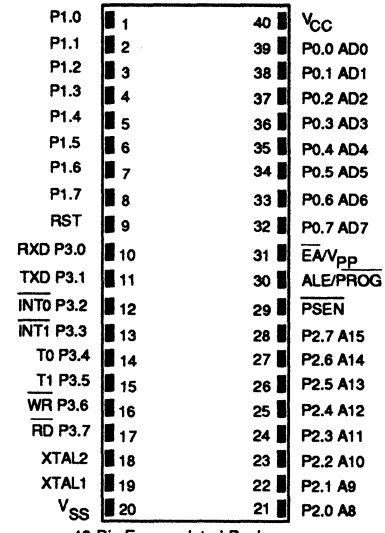
DALLAS SEMICONDUCTOR

DS5000T
Time Microcontroller

FEATURES

- DS5000 Soft Microcontroller with embedded clock/calendar
- Internal lithium cell preserves clock function in the absence of V_{CC}
- Permits logging of events with time and date stamp
- 8 or 32 Kbytes of embedded nonvolatile program/data RAM
- Program loading via on-chip full-duplex serial port
- User-selectable program/data memory partition
- All 4 ports available for system control
- Resident encryptor protects program from piracy
- Power sequencer and watchdog timer help ensure crashproof operation
- Compatible with industry standard 8051 instruction set and pinout
- Clock accuracy is better than 2 min/month @25°C

PIN CONNECTIONS



40-Pin Encapsulated Package

ORDERING INFORMATION

DS5000T YY - XX

Program/Data RAM
- 08 8Kbytes
- 32 32 Kbytes

MAX. Clock Frequency
- 08 8 MHz
- 12 12 MHz
- 16 16 MHz

DESCRIPTION

The DS5000T Time Microcontroller offers all the features of the DS5000 Soft Microcontroller with the added benefit of an embedded real-time clock/calendar function. The clock function itself is accessed as though it were a part of the embedded data RAM so that the 32 I/O pins are free for the application use. With this feature, new and existing microcontroller systems can now log events, schedule activities, and time operations. The combination of DS5000T's soft features together with a real-time clock/calendar provides a powerful controller that adapts to the needs of time-driven applications.

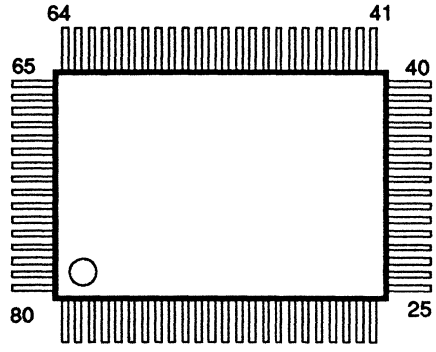
DALLAS SEMICONDUCTOR

DS5000FP
Micro Chip

FEATURES

- Offers the microcontroller die used in the DS5000 Soft Microcontroller DIP packaged in an 80-pin Quad Flat Pack (QFP)
- Provides access to bytewide address/data bus, not available on the DS5000 DIP
- Bytewide address/data bus frees up port pins for I/O use
- Direct interface to bytewide memories
- Supports up to 64 Kbytes of program/data memory
- Incorporates battery switching/monitoring circuitry for powering external memory devices in the absence of V_{cc}
- Ultra-low standby current—less than 75 nA
- Watchdog timer ensures program control
- Fully compatible with 8051 instruction set

PACKAGE DESCRIPTION



80-Pin Quad Flat Pack

ORDERING INFORMATION

DS5000FP-XX	-08	08 MHz
	-12	12 MHz
	-16	16MHz

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DESCRIPTION

The DS5000FP Micro Chip is an 80-pin Quad Flat Pack (QFP) containing a standalone DS5000 Soft Microcontroller die which normally resides in a 40-pin DS5000 DIP package. It retains all the hardware features of a DS5000 DIP and can be used much like ROM-less versions of the 8051, except that all four ports of the DS5000FP are freed up for general-purpose I/O. An external lithium energy cell can be attached to this chip to power external SRAM(s) in the absence of V_{cc}. This gives the user the flexibility of using his own lithium cells and memories to implement a nonvolatile microcontroller solution with the soft features inherent in the DS5000 DIP. EPROM devices can be used for program memory in applications not requiring reloadable software.

Of the 80 pins on the package, only 68 are actually tied to pads on the die. The rest of the pins are no-connects. 40 pins of the 68 signal pins are identical in function to the 40 pins of a standard DS5000. The other 28 pins are normally used to interface to the embedded RAM and the lithium source on the standard DS5000 DIP products.

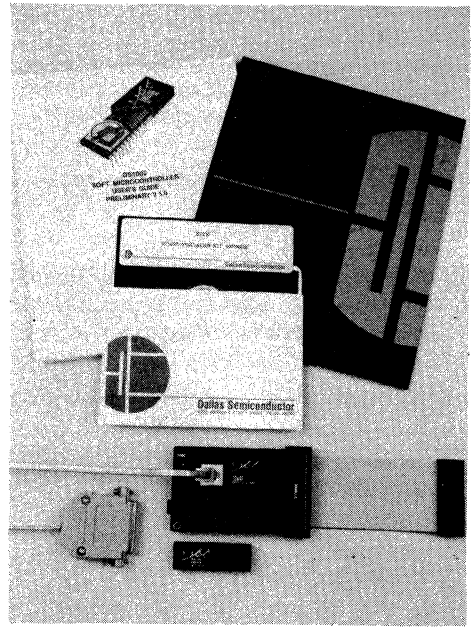
FULL DATA SHEET AVAILABLE — CALL 214-450-3836

DALLAS SEMICONDUCTOR

DS5000TK
Time Micro Evaluation Kit

FEATURES

- Allows immediate evaluation of DS5000T Time Microcontroller or DS5000 Soft Microcontroller in an existing application
- Supplied with DS5000T32, software diskette, DS5000 User's Guide, and In-System Loader hardware
- Supports in-system serial downloading of DS5000(T) from an IBM PC host
- DS5000T supports all functions of DS5000 with addition of real-time clock
- Downloads/verifies Intel Hex absolute object files residing on IBM PC
- User-friendly software prompts user for required system configuration information
- Supports serial download rates up to 19200 bps
- Requires no support circuit overhead on target system



DESCRIPTION

The DS5000TK Time Micro Evaluation Kit is a development support system which is designed to allow immediate evaluation of the DS5000T Time Microcontroller in a system application. Since the DS5000T performs all of the functions associated with the DS5000 Soft Microcontroller, it can also be used for evaluation of any of the versions of a DS5000 for a new or existing design.

Materials provided with the kit include a DS5000T with 32 Kbytes of RAM, full documentation on the DS5000(T), In-System Loader serial download hardware, and software for the IBM PC (KIT5K). Using the Evaluation Kit, the user can quickly configure the DS5000(T) for operation in the target system. This configuration can be performed without detailed knowledge of the operation of the DS5000's Serial Load Mode. The DS5000TK Evaluation Kit not only serves as a first-time evaluation system for the DS5000 or the DS5000T, but also performs the equivalent function of an EPROM programming system throughout the prototyping phase of the design cycle.

Adaptors are available for development with the DS2250 Soft Micro Stik and the DS2250T Time Micro Stik. For information on these see the DS907x data sheet.

The Evaluation Kit's In System Loader hardware allows application software to be loaded into the DS5000(T) while it is connected to the target system, eliminating the need for removal of the device when reprogramming is required. The In System Loader hardware consists of an RS232 cable that connects to the RS232 Fixture which houses the appropriate interface circuitry and provides a 40-pin Zero-Insertion-Force socket for the either the DS5000 or DS5000T. The fixture in turn attaches to the 40-pin target cable which connects to the microcontroller socket in the target system. The hardware provides the mechanism for the KIT5K software to take control of the DS5000(T) via the RS232 cable, place the device in its Serial Program Load Mode, and transmit new software to the device.

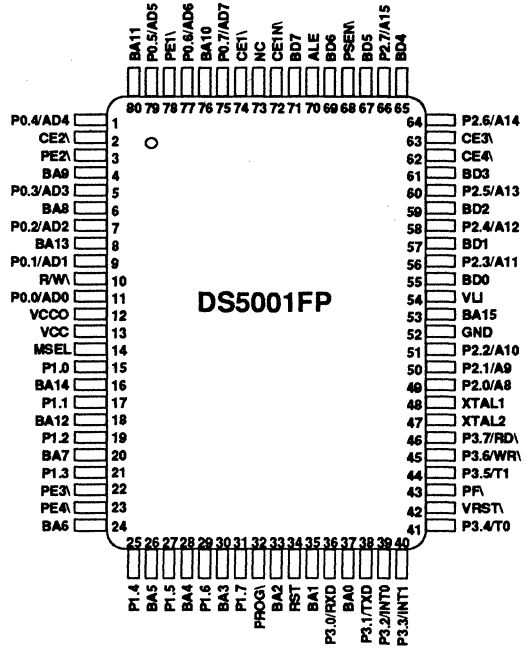
DALLAS SEMICONDUCTOR

DS5001FP
128K Micro Chip

FEATURES

- Enhanced CMOS microcontroller addresses up to 128K of NV SRAM for program/data
- Bytewide address/data bus leaves port pins for general-purpose I/O
- Multiple chip select outputs for memory mapping of peripheral devices
- Crashproof circuitry converts CMOS SRAM into nonvolatile storage
- Reprogrammable Peripheral Controller (RPC) mode emulates 8042 for PC bus applications
- Increased flexibility in program loading
- Optional CRC-16 check of NV program/data RAM area on power-up or watchdog reset
- Bandgap reference provides tight power supply monitoring
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface mount package

PIN CONNECTIONS



80-Pin Quad Flat Pack

DESCRIPTION

The DS5001FP 128K Micro Chip is an enhanced version of the DS5000FP Micro Chip. The DS5001FP is designed for systems with large nonvolatile SRAM and I/O requirements; its separate bytewide address/data bus accesses up to 128K bytes of nonvolatile SRAM for program/data storage. In addition, four peripheral enables allow additional I/O devices to be memory-mapped onto the bytewide bus without the need for external logic. Thus, even in the most complex systems, the 8051-compatible ports are free for general-purpose I/O. When combined with an appropriate external lithium energy cell, the DS5001FP's crashproof circuitry retains programs and data in external SRAM for 10 years in the absence of V_{CC}.

Compared to its predecessor, the DS5000 Soft Microcontroller, the DS5001FP incorporates memory capacity and flexibility enhancements, additional I/O resources, and new software loading features. Memory improvements include the ability to address 128K bytes of NV SRAM on the bytewide bus, multiple memory architectures for optimum implementation, and a peripheral memory map. Substantial flexibility in memory selection is provided by the DS5001FP's unique architecture, which allows the most cost-effective memory selection to be used.

I/O flexibility is provided by the Reprogrammable Peripheral Controller (RPC). This is an 8042 hardware emulation mode that allows the DS5001FP to act as a slaved peripheral controller for PC bus applications. When the RPC is not in use, port I/O which is fully compatible with the 80C51 remains available. Additional I/O flexibility results from the ability to address external peripheral devices on the bytewide bus, which allows the ports to be used for other functions.

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FULL DATA SHEET AVAILABLE — CALL 214-450-3836

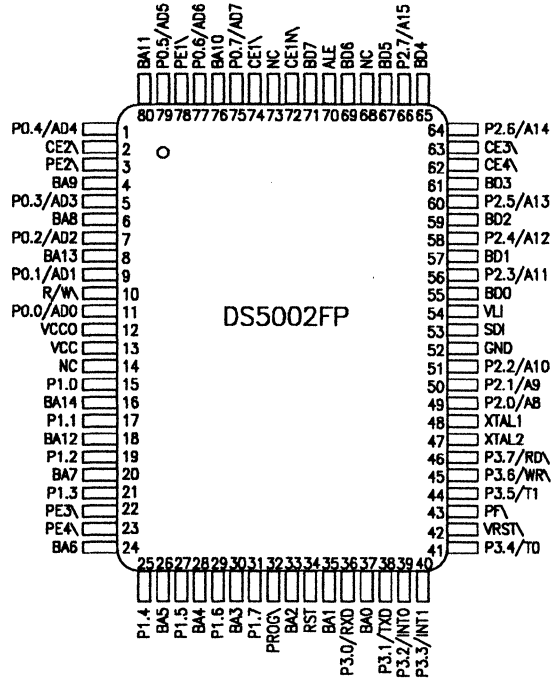
DALLAS SEMICONDUCTOR

DS5002FP
Secure Micro Chip

FEATURES

- Enhanced security features:
  - Stronger address/data encryptor
  - 64-bit encryption key word
  - Automatic true random key generation
  - SDI (Self-Destruct Input)
  - Top coating defeats microprobe attack
- Customer-specific encryption versions available
- Incorporates enhanced memory and I/O features of DS5001FP 128K Micro Chip.
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface-mount package

PACKAGE OUTLINE



DESCRIPTION

The DS5002FP Secure Micro Chip is a secure version of the DS5001FP 128K Micro Chip. In addition to the memory and I/O enhancements of the DS5001FP, the Secure Micro Chip incorporates the most sophisticated security features available in any microcontroller. The security features of the DS5002FP include an array of mechanisms which are designed to resist all levels of threat, including observation, analysis, and physical attack. As a result, a massive effort would be required to obtain any information about memory contents. Furthermore, the soft nature of the DS5002FP allows frequent modification of the secure information, thereby minimizing the value of any secure information obtained at any given time by such a massive effort.

The DS5002FP implements a security system that is an improved version of its predecessor, the DS5000 Soft Microcontroller. Like the DS5000, the DS5002FP loads and executes application software in encrypted form in up to 128K x 8 bytes of standard SRAM on its bytewide bus. This RAM is converted by the DS5002FP into lithium-backed nonvolatile storage for programs and data. As a result, the contents of the RAM and the execution of the software appear unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected key. Any attempt to discover the key value results in its erasure, rendering the encrypted contents of the RAM useless.

The Secure Micro Chip offers a number of major enhancements to the software security implemented in the previous generation of the DS5000 Soft Microcontroller. A full data sheet is available under non-disclosure agreement. Contact the factory for details.

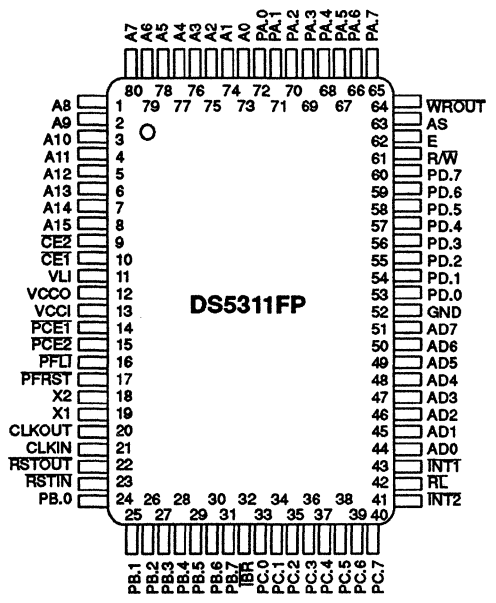
DALLAS SEMICONDUCTOR

DS5311FP
68HC11 Softener Chip

FEATURES

- Softens 68HC11-based systems
  - Converts up to 64K bytes of CMOS RAM into lithium-backed NV program/data storage
  - Serial bootstrap loading
  - In-system program changes adapt HC11 to task at hand
- Crashproof operation during transient conditions
  - NV storage for 10 years with no V_{CC}
  - Orderly shutdown/restart on power-up/down
  - Watchdog timer
  - CRC of memory on power-up
  - Call for Help via Modem
- Enhanced I/O
  - Provides four 8-bit parallel I/O ports to HC11
  - Dual port register file for Host bus interface
  - 4 decoded chip enables with write protection
  - Mates to HC11 Address/Data Bus

PACKAGE OUTLINE



DESCRIPTION

The DS5311FP 68HC11 Softener Chip is a member of the Softener family that is designed to provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Softener Family User's Guide, for systems based on the popular Motorola MC68HC11 microprocessor. The DS5311FP interfaces directly to the HC11's address/data bus and control signals, and converts up to 64K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the 68HC11, DS5311FP Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered DS1283 Watchdog Timekeeper Chip, can be added to the system without the need for additional glue logic.

Also available from Dallas Semiconductor is the DS2311 Soft HC11 Stik, a complete implementation of the embedded control system described above. The Stik is implemented on a SIMM module that plugs into the industry-standard 72-pin SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2311 can be used as a high-level building block in a system design, resulting in a quick time to market for a Softener-based HC11 system. Alternatively, it can be used for fast prototyping of a system that will ultimately incorporate the DS5311FP HC11 Softener Chip. The designer should consult the DS2311 data sheet for information on this application of the DS5311.

13

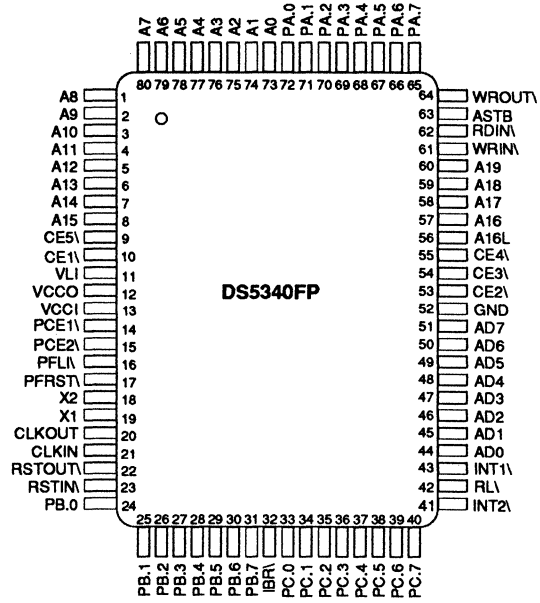
DALLAS SEMICONDUCTOR

DS5340FP
V40 Softener Chip

FEATURES

- Provides softness for V40-based systems:
- Adapts to task-at-hand:
  - Converts up to 672K bytes of CMOS SRAM into lithium-backed NV program/data storage
  - Serial bootstrap loading
  - Code can be changed in end use
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports

PIN DESCRIPTION



80-Pin Quad Flat Pack

DESCRIPTION

The DS5340 V40 Softener, a member of the Softener family, provides the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities as discussed in the *DS53XX User's Guide* for systems based on the popular 8088-compatible NEC V40 microprocessor. The DS5340 interfaces directly to the V40's address/data bus and control signals and converts up to 672K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the V40, DS5340 V40 Softener, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered clock/calendar function (using the DS1283 Watchdog Timekeeper Chip) can be added to the system without the need for additional glue logic. Because the V40 is code-compatible with the 8086, application code can be developed on a PC in its native instruction set. As a result, a multitude of high-level language compilers, assemblers, and debugging packages are available to support development for a V40/DS5340-based embedded control system.

Also available from Dallas Semiconductor is the DS2340 V40 Soft Stik, which is a complete implementation of the embedded control system described above. The DS2340 is implemented as a small daughterboard that plugs into the industry-standard 72-pin SIMM connector scheme, which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2340 can be used as a high-level building block in a system design resulting in a quick time to market for a Softener-based V40 system. Alternatively, it can be used for fast prototyping of a system which will ultimately incorporate the DS5340 V40 Softener itself. The designer should consult the DS2340 product preview for information on this application of the DS5340.

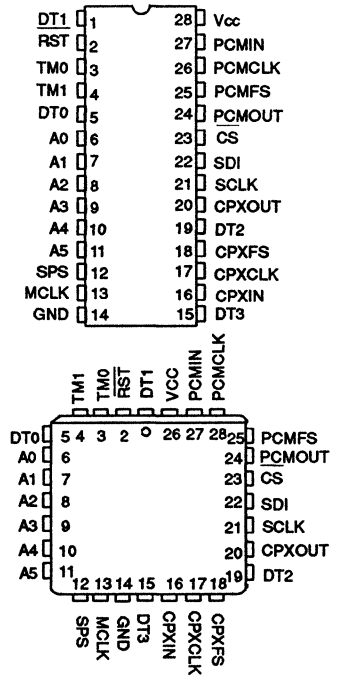
DALLAS SEMICONDUCTOR

DS2130Q
Voice Messaging Processor

FEATURES

- Per-channel voice messaging processor for digitized voice storage and retrieval
- High fidelity speech recording and playback at 8, 12, 16, 24 and 32 Kbits/sec
- Integral DTMF transceiver for remote touch-tone control and dialing
- Connects to popular PCM codec/filters for analog interfacing
- Direct PCM serial data bus interfaces to any of 32 possible TDM time slots
- Monitors and reports audio energy levels for call progress and voice detection
- Selectable beep generator for sound prompts
- 3-wire synchronous serial control port
- 28-pin DIP or PLCC (DS2130Q) packages

PIN CONNECTIONS



DESCRIPTION

The DS2130 Voice Messaging Processor is a CMOS DSP processor that serves as a voice messaging engine for digitized voice storage and retrieval applications. It offers half-duplex speech compression or expansion at either 8, 12, 16, 24 or 32 Kbits/sec. The advanced speech compression algorithm maintains excellent audio clarity even at low bit rates. The algorithm also incorporates a DTMF transceiver for decoding or generating touch-tone signals for remote control and automatic dialing. The tone generator can be used to create single-tone beeps used in popular answering machines. Voice and call progress detection can be easily implemented using the energy threshold detect outputs.

The DS2130 can be used together with a low-cost codec/filter device for analog interfacing in standalone applications such as answering machines or feature phones. It can also interface directly to a serial PCM bus on any of up to 32 possible time slots using an internal software-selectable time slot assigner circuit (TSAC). This configuration can be used in digital switching systems for adding voice messaging services to existing backplane designs.

Applications include digital answering machines, embedded voice response, speech annunciators, voice mail, key telephone systems and automatic operator services.

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FULL DATA SHEET AVAILABLE – CALL 214-450-3836

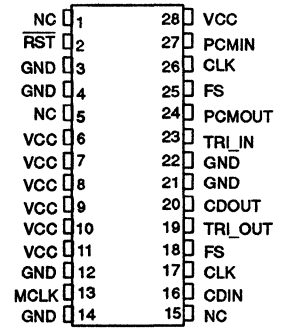
DALLAS SEMICONDUCTOR

DS2132/Q
Digital Answering Machine Processor

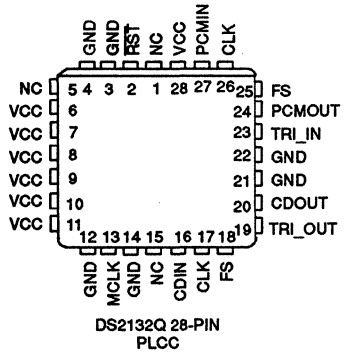
FEATURES

- Two high quality speech compression algorithms permit either 7 or 14 minutes of speech storage in a single 4 Mbit DRAM
- Economical three-wire data/control/status port frees up microcontroller port pins.
- Detects and generates the 12 standard DTMF tones plus the A/B/C/D tones.
- Detects CCITT T.30 FAX calling tone (1100 Hz)
- Generates musical tones which allow "melodies-on-hold" or customizable prompts
- Echo cancellation for improved DTMF receiver performance
- Precise signal level detection capability
- Record/Playback gain control
- 28-pin DIP or PLCC (DS2132Q) packages

PIN ASSIGNMENT



DS2132 28-PIN DIP
600 MIL



DS2132Q 28-PIN
PLCC

DESCRIPTION

The DS2132 Digital Answering Machine Processor is a Digital Signal Processor (DSP) optimized for the compression/expansion of PCM coded voice to/from an extremely low bit rate. The DS2132 contains two advanced speech compression algorithms that offer outstanding fidelity. The Standard Record/Playback algorithm compresses speech to 9.8Kbps and the Extended Record/Playback algorithm compresses speech to 4.9Kbps.

The DS2132 is ideal for embedded applications such as digital answering machines, voice mail, voice annunciators, and any other device that needs to maximize speech storage in a limited memory space. A simple three wire interface to the embedded microcontroller frees up valuable controller port pins for other uses and simplifies the software needed to transfer speech data, issue commands, and receive DTMF/energy level/status information. The DS2132 detects and generates all 16 DTMF tones and can also generate a wide variety of call progress tones. In addition, the DS2132 provides CCITT Rec. T.30 FAX calling tone detection which enables the answering machine to determine if the incoming call is a voice or FAX transmission. The energy level detector allows the microcontroller to perform call progress detection and automatic gain control functions.

FULL DATA SHEET AVAILABLE – CALL – 214-450-3836

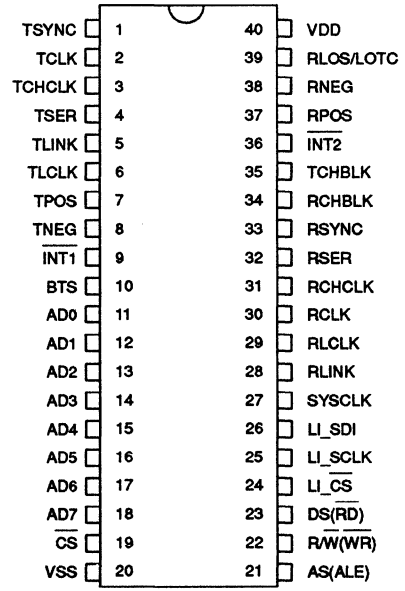
DALLAS SEMICONDUCTOR

DS2141
T1 Controller

FEATURES

- DS1 transceiver
- Parallel Control Port
- Frames to D4, ESF, and SLC–96^{R} formats
- Onboard two frame elastic store slip buffer
- Extracts and inserts robbed bit signaling
- Programmable output clocks
- Supports both FDL standards, ANSI T1.403–1989 and AT&T TR54016
- 5V supply; low power CMOS
- Available in 40 pin DIP and 44 pin PLCC

PIN ASSIGNMENT



40 PIN DIP

DESCRIPTION

The DS2141 is a comprehensive, software-driven T1 framer. It is meant to act as a slave or co-processor to a microcontroller or microprocessor. Quick access via the parallel control port allows a single micro to handle many T1 lines. The DS2141 is very flexible and can be configured into numerous orientations via software. The software orientation of the device allows the user to modify their design to conform to future T1 specification changes. The controller contains a set of 62 eight-bit internal registers which the user can access. These internal registers are used to configure the device and obtain information from the T1 link. The device fully meets all of the latest T1 specifications including ANSI T1.403-1989, AT&T TR 62411 (12-90), and CCITT G.704 and G.706.

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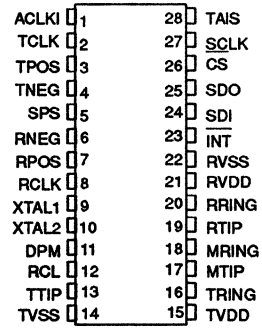
DALLAS SEMICONDUCTOR

DS2145/DS2146
T1/CEPT Medium Haul PCM Line Interface

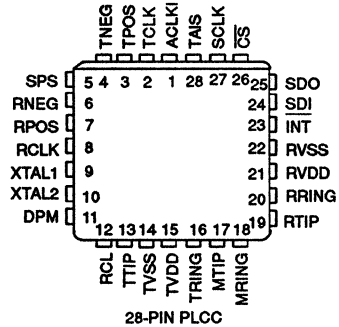
FEATURES

- T1 (1.544 Mbps) and CEPT (2.048 Mbps) PCM line interface transceiver
- Pin compatible with the CS61574(A)/75/35(A) and LXT300/304A/305(A)
- Receiver sensitivity of –18 dB will recover data off of lines up to 3300 feet (1 km) in length
- Onboard 128 bit jitter attenuator which can be disabled
- DS2145 contains a receive side jitter attenuator DS2146 contains a transmit side jitter attenuator
- Compatible with Dallas Semiconductor's complete line of framers including the DS2180A, DS2181A, and DS2141
- Available in 28 pin DIP and PLCC
- Single +5V supply

PIN ASSIGNMENT



28-PIN DIP (600 MIL)



28-PIN PLCC

DESCRIPTION

The DS2145 and DS2146 are monolithic CMOS T1 (1.544 Mbps) and CEPT (2.048 Mbps) line interface transceivers. They couple directly to the T1 or CEPT lines via a transformer and will recover both clock and data from lines as long as 3300 feet (1 km). These devices contain a digital clock recovery system which is very tolerant to incoming jitter and its on–board 128 bit jitter attenuator allows it to smooth wide excursions that can appear in T1 and CEPT data streams. The DS2145 and DS2146 contain a receive only monitor mode in which the transmitter can be disabled to lower the power consumption and the receive side reconstruction filter can also be disabled and replaced with straight resistive gains of 12 dB, 18 dB, or 24 dB. These devices met or exceed the applicable sections of AT&T TR62411 (Dec. 90), ANSI T1.403–1989, and the CCITT Blue book Recommendations G.703, G.823, and G.735.

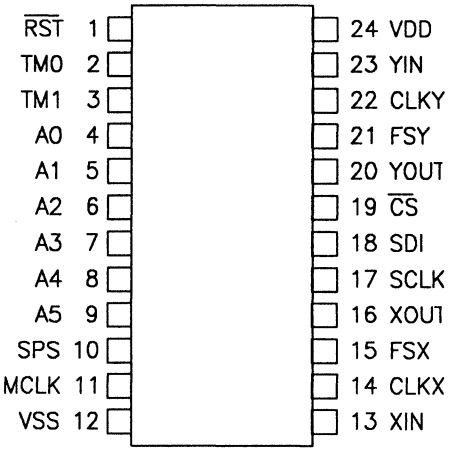
DALLAS SEMICONDUCTOR

DS2165
16/24/32Kbps ADPCM Processor Chip

FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps
- Dual fully independent channel architecture; device can be programmed to perform either:
  - two expansions
  - two compressions
  - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375 us
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports channel associated signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2167 ADPCM Processor Chip
- Single +3 to +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

PIN DESCRIPTION



DS2165 24-Pin DIP

DESCRIPTION

The DS2165 ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression to 32Kbps follows the algorithm specified by CCITT Recommendation G.721 (July 1986) and ANSI document T1.301 (April 1987). The compression to 24Kbps follows ANSI document T1.303. The compression to 16Kbps follows a proprietary algorithm developed by Dallas Semiconductor. The DS2165 can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

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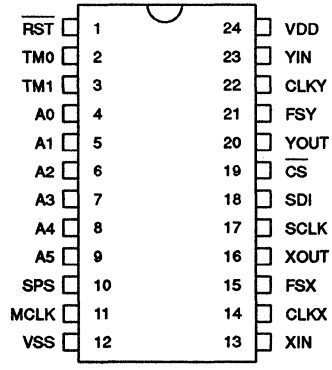
DALLAS SEMICONDUCTOR

DS2167/DS2168
ADPCM Processor

FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture – device may be programmed to perform full duplex, 2–channel expansions, or 2–channel compressions
- Interconnects directly with u–law or A–law combo–codec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On–chip channel counters identify input and output time slots in TDM–based systems
  - Unique addressing scheme simplifies device control; 3–wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for standalone use
  - No host processor required
  - Ideal for voice mail applications
- 28–pin surface mount package available, designated DS2167Q/DS2168Q

PIN ASSIGNMENT



24 PIN DIP (600 mil)

DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM–based telephony networks.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

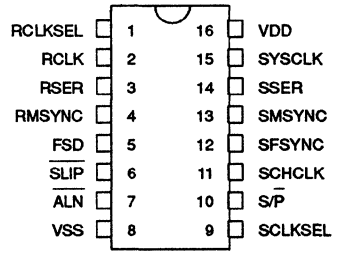
DALLAS SEMICONDUCTOR

DS2175
T1/CEPT Elastic Store

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop–timed and system–timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on–chip "slip" control logic
  - Slip occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A, DS2181 CEPT Transceivers
- Industrial temperature range of –40°C to +85°C available, designated DS2175N

PIN ASSIGNMENT



16–PIN DIP (300 MIL)

DESCRIPTION

The DS2175 is a low–power CMOS elastic–store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1–1.544 MHz) and European (CEPT–2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross–connects (DACS), private network equipment and PABX–to–computer interfaces such as DMI and CPI.

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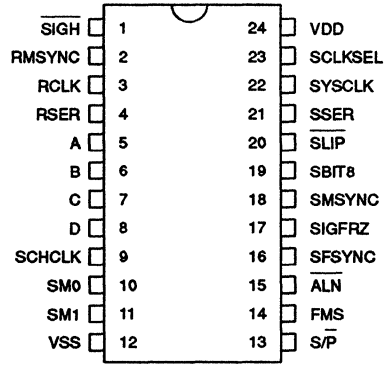
DALLAS SEMICONDUCTOR

DS2176
T1 Receive Buffer

FEATURES

- Synchronizes loop–timed and system–timed T1 data streams
- Two frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed–bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of –40°C to +85°C available, designated DS2176N

PIN ASSIGNMENT



24 PIN DIP (600 mil)

DESCRIPTION

The DS2176 is a low–power CMOS device specifically designed for synchronizing receive side loop–timed T–carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24–lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross–connects (DACS), private network equipment and PABX–to–computer interfaces such as DMI and CPI.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

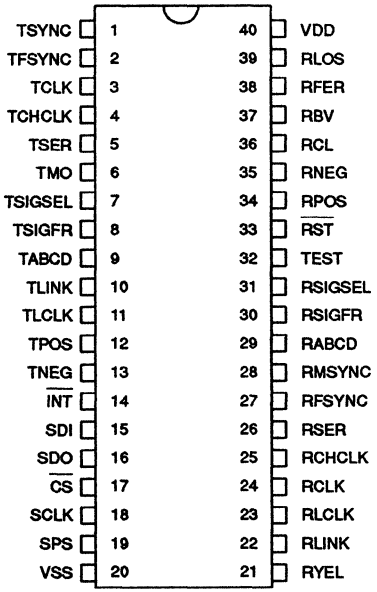
DALLAS SEMICONDUCTOR

DS2180A
T1 Transceiver

FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for standalone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non–clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of –40°C to +85°C available, designated DS2180AN or DS2180AQN

PIN ASSIGNMENT



40 PIN DIP

DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T–carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

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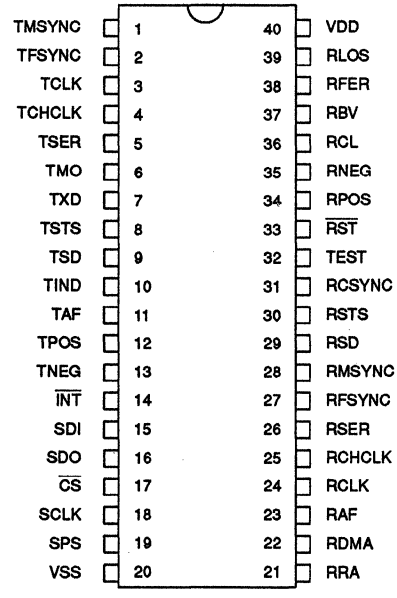
DALLAS SEMICONDUCTOR

DS2181
CEPT Primary Rate Transceiver

FEATURES

- Single chip primary rate transceiver meets CCITT standards G.704, G.706, and G.732
- Supports new CRC4-based framing standards and CAS and CCS signalling standards
- Simples serial interface used for device configuration and control in processor mode
- Hardware mode requires no host processor; intended for stand-alone applications
- Comprehensive, on-chip alarm generation, alarm detection, and error logging logic
- Shares footprint with DS2180A T1 Transceiver
- Companion to dS2175 Transmit/Receive Elastic Store
- 5V supply; low-power CMOS technology

PIN ASSIGNMENT



40 PIN DIP

DESCRIPTION

The DS2181A is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704, G.706, and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signalling data, and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features such as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

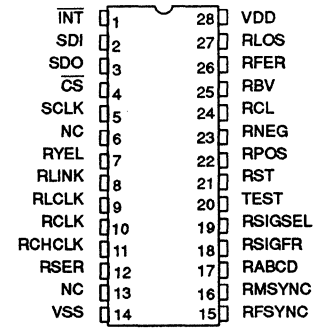
DALLAS SEMICONDUCTOR

DS2182
T1 Line Monitor Chip

FEATURES

- Performs framing and monitoring functions
- Supports Superframe and Extended Superframe formats
- Designed to fulfill the requirements outlined in TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit) and TR-TSY-000194 (ESF Interface Specification)
- Four onboard error counters
  - 16-bit bipolar violation
  - 8-bit CRC
  - 8-bit OOF
  - 8-bit frame bit error
- Indication of the following
  - yellow and blue alarms
  - incoming B8ZS code words
  - 8 and 16 zero strings
  - change of frame alignment
  - loss of sync
  - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allows quick access to counters for status updates
- Automatic counter reset feature
- Single 5V supply; low-power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC

PIN ASSIGNMENT



28-PIN DIP

DESCRIPTION

The DS2182 T1 Line Monitor Chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182 frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large onboard counters allow the accumulation of errors for extended periods, which permit a single CPU to monitor a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signalling bits, and channel data.

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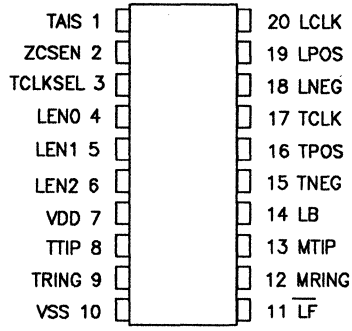
FULL DATA SHEET AVAILABLE - CALL 214-450-3836

DALLAS SEMICONDUCTOR

DS2186
T1/CEPT Transmit Line Interface Chip

FEATURES
- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip transmit LBO (line build out) and line drivers eliminate external components
- Programmable output pulse shape supports short-and long-loop applications
- Supports bipolar and unipolar input data formats
- Transparent B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



DS2186 20-Pin DIP

DESCRIPTION
The DS2186 T1/CEPT Transmit Line Interface Chip interfaces user equipment to North American (T1-1.544MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable wave-shaping circuitry, line drivers, remote loopback, and zero suppression logic. A line-coupling transformer is the only external component required.

Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI. The DS2186 supports ISDN -PRI (Primary Rate Interface) specifications.

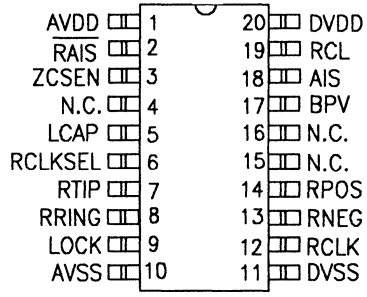
FULL DATA SHEET AVAILABLE - CALL 214-450-3836

DALLAS SEMICONDUCTOR

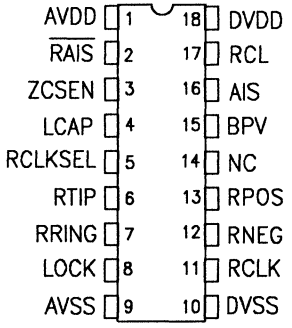
DS2187
T1/CEPT Receive Line Interface Chip

FEATURES
- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411, and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank -- no tuning required
- Decodes AMI, B8ZS, and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1/ISDN Primary Rate and DS2181 CEPT Transceivers
- Companion to the DS2186 T1/CEPT Transmit Line Interface Chip
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



DS2187 20-Plin SOIC



DS2187 18-Pin DIP

14

DESCRIPTION
The DS2187 T1/CEPT Receive Line Interface Chip interfaces user equipment to North American (T1 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI.

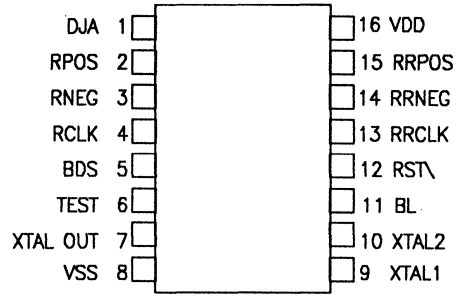
DALLAS SEMICONDUCTOR

DS2188
T1/CEPT Jitter Attenuator Chip

FEATURES

- Attenuates clock and data jitter present in T1 or CEPT lines
- Meets the jitter attenuation templates outlined in TR62411, TR-TSY-000170, G.735, and G.742
- Only one external component required; either a 6.176MHz (T1) or 8.192MHz (CEPT) crystal
- Selectable buffer size of 128 or 32 bits
- Jitter attenuation is easily disabled
- Single +5V supply; low-power CMOS technology
- Available in 16-pin DIP and 16-pin SOIC

PIN DESCRIPTION



DS2188 16-Pin DIP

DESCRIPTION

The DS2188 T1/CEPT Jitter Attenuator Chip contains a 128 X 2-bit buffer which, in conjuction with an external 4X crystal, is used to attenuate the incoming jitter present in clock and data. The device meets all of the latest applicable specifications including those outlined in TR 62411(ACCUNET* T1.5 Service Description and Interface Specifications, December 1988), TR-TSY-000170 (Digital Cross-Connect System Requirements and Objectives, November 1985), and the CCITT Recommendations G.735 and G.742. The DS2188 is compatible with the DS2180A T1/ISDN Primary Rate Transceiver and DS2181 CEPT Transceiver and it is the companion to the DS2187 T1/CEPT Receive Line Interface and DS2186 T1/CEPT Transmit Line Interface. It can also be used in conjunction with the DS2190 T1 Network Interface Unit.

FULL DATA SHEET AVAILABLE - CALL 214-450-3836

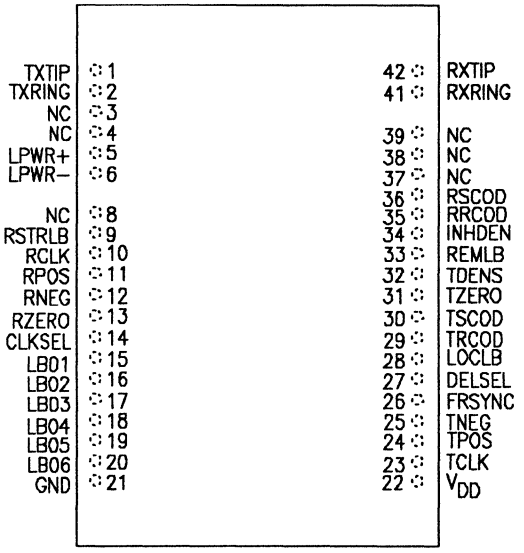
DALLAS SEMICONDUCTOR

DS2190-003
T1 Network Interface Unit (NIU)

FEATURES

- Modularized network interface for 1.544 Mbps T1 services
- Network side connects directly to T1 line
- Compatible with DS2180A T1/ISDN Primary Rate Transceiver
- Small size--approximately six square inches--permits integration onto line cards
- Compatible with AT&T publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data with no external components or tuning
- Detects and generates in-band loopback codes
- Assures proper ones density to network
- Powered by a local +5 volt supply

PIN CONNECTIONS



DESCRIPTION

The DS2190 T1 Network Interface Unit is a small sealed module designed to meet the recommendations of AT&T Publication 62411 for interfacing to T1 1.544 Mbps services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

*Service marks of AT&T Communications

052490 1/1

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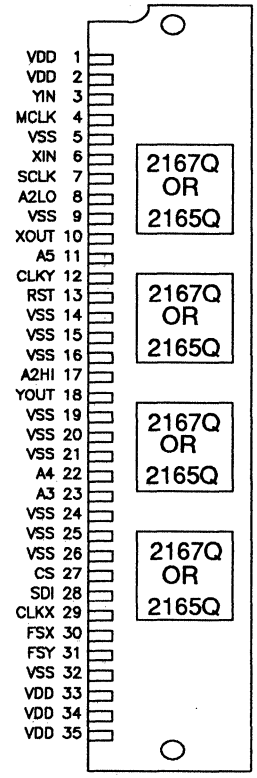
DALLAS SEMICONDUCTOR

DS2264
DS2268
ADPCM Stik

FEATURES

- Provides four channels (DS2264) or eight channels (DS2268) of parallel full-duplex ADPCM processing in a pre-fabricated, snap-in module
- Based on the DS2167Q or DS2165Q ADPCM Processor Chip which implements the T1.301 and CCITT G.721 recommendations
- Occupies only 2 square inches of board space
- Conforms to popular JEDEC standard 35 position single in-line connector
- Easily cascadable up to 64 full-duplex channels in multiples of four or eight
- Both A-law and U-law compatible
- Utilizes serial interface port for microprocessor control of timeslot assignments
- Includes onboard buffers for all critical signals

PIN DESCRIPTION



(actual size)

ORDERING INFORMATION

4 channels with DS2167Q	DS2264
8 channels with DS2167Q	DS2268
4 channels with DS2165Q	DS2264 - EXP
8 channels with DS2165Q	DS2268 - EXP

DESCRIPTION

The DS2264 and DS2268 ADPCM Stiks are complete, pre-fabricated cards that perform either four or eight channels of full-duplex ADPCM processing. The ADPCM algorithm compresses 64Kbps voice data to either 32Kbps, 24Kbps, or 16Kbps. The DS2264 is only populated on one side and offers four channels while the DS2268 is populated on both sides of the Stik and offers eight channels. Control of the Stiks is handled by an external microcontroller via a serial port. Both Stiks are based on the DS2167Q or DS2165Q ADPCM Processor Chips. Specific details on the DS2167Q and DS2165Q can be found in their respective data sheets.

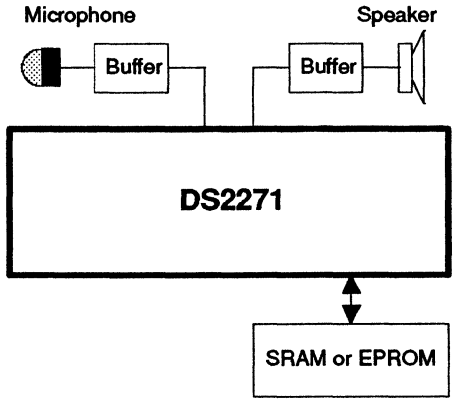
DALLAS SEMICONDUCTOR

DS2271
Speech Stik

FEATURES

- Adds speech recording and playback to any system without any moving parts
- Any sound can be recorded and recreated
- Words can easily be concatenated to form sentences, which lowers the cost of storing the recorded speech
- Telephone-grade speech can be recorded at rates as low as 8Kbps
  - recording capacity of over 8 minutes with external memory
  - 14 seconds of capacity with on-Stik memory
- Can be controlled via switch closures (hardware mode) or via an external controller (software mode)
- New words can be downloaded into the Stik via software
- A kit designed to aid in speech development is available (DS2271DK)

EVALUATION BOARD



DESCRIPTION

The DS2271 Speech Stik is a complete solid-state audio recording/reproducing subsystem that replaces mechanical tape-based recording for embedded applications. With the Speech Stik, equipment can coach novice users on its operation or it can inform nontechnical users of malfunctions. The DS2271 Speech Stik digitizes speech and automatically stores the speech in external memory. With external EPROM, the DS2271 becomes a voice annunciator. With external SRAM, the DS2271 becomes a voice recorder with the ability to both record and play back speech. The DS2271 has been designed to allow the user to easily integrate it into existing systems. The Stik has the unique ability to allow the user to customize each unit with different words and phrases. With the separate speech development kit (DS2271DK), the user has the ability to "edit" the recorded speech to create smooth sounding sentences out of discrete words.

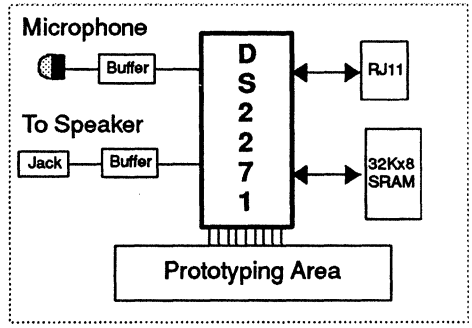
DALLAS SEMICONDUCTOR

DS2271DK
Speech Stik Design Kit

FEATURES

- Facilitates development of prototype systems
- Interfaces directly to IBM PC/XT/AT and compatibles
- Concatenates and trims messages
- Converts speech data to Intel Hex format
- Kit components include:
  - DS2271 Speech Stik
  - DS2271DK Development Software
  - Printed circuit board
  - Interface cable for PC
  - DS1230AB-200 32K x 8 NV SRAM
  - Microphone, speaker jack, and interface circuitry
  - RS-232C Port

EVALUATION BOARD



DESCRIPTION

The DS2271DK Design Kit provides a convenient and flexible platform for prototyping the wide array of possible DS2271 applications. The evaluation board comes with a DS2271 and the interface circuitry necessary for common applications including a microphone, a speaker jack, and an RS-232 port. By connecting the provided cable between a PC and the evaluation board's RS-232 port, the design kit control software can be used to issue DS2271 commands and build compound messages from smaller recorded messages. Prospective compound messages can be previewed by using the MPLAY command and, if desired, converted to Intel Hex format for mask programming.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

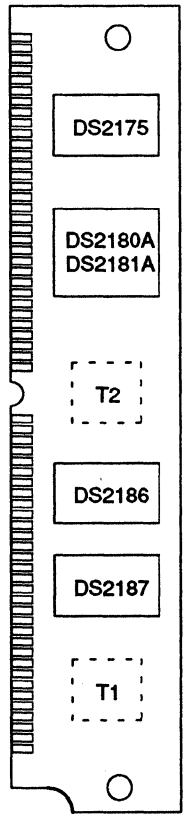
DALLAS SEMICONDUCTOR

DS2280/DS2281
T1 Line Card Stik
CEPT Line Card Stik

FEATURES

- Pretested, Snap-In T1 or CEPT line card
- DS2280 T1 Line Card
  DS2281-075 75 ohm CEPT Line Card
  DS2281-120 120 ohm CEPT Line Card
- Consumes only 2 square inches of board space
- Performs four functions:
  - line interface
  - framing
  - monitoring
  - buffering
- DS2280 and DS2281 share the same pinout
- Includes line interface transformers and termination resistors
- Connects to both 1.544 MHz and 2.048 MHz backplanes
- Operates off a single +5V supply

PIN ASSIGNMENT



DESCRIPTION

The DS2280 and DS2281 are T1 and CEPT line cards that consume only two square inches of printed circuit board space. The cards are designed to plug into standard 68-pin Single In-line connectors. They have been arranged for maximum flexibility and contain all the necessary hardware to connect directly to either T1 or CEPT 75 ohm lines, or CEPT 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The monitoring and framing functions are performed by the DS2180A on the DS2280 and by the DS2181 on the DS2281. The buffering function is handled by the DS2175. The DS2280 and DS2281 provide all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). They also provide indication of frame errors, CRC-6 or CRC-4 errors, and bipolar violations.

DALLAS SEMICONDUCTOR

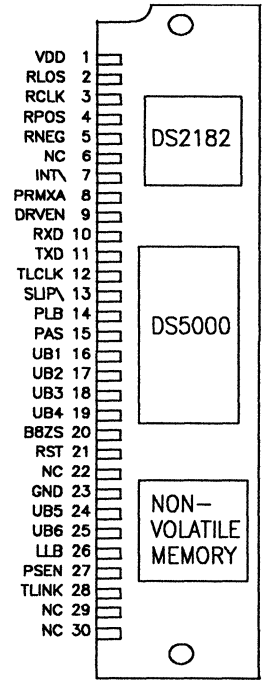
DS2282
T1 FDL Controller/ Monitor Stik

FEATURES

- Fully implements the FDL message format as described in the ANSI document T1.403-1989
- Fully implements the maintenance message protocol described in AT&T TR 54016 (1989)
- Provides high-level monitor counts, namely:
  - Errored Seconds
  - Severely Errored Seconds
  - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2283 T1 Enhanced Line Card Stik or DS2180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin Single In-Line connector
- Single +5V supply

(actual size)

Stik LAYOUT



DESCRIPTION

The DS2282 T1 FDL Controller/Monitor Stik completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000194 (Extended Superframe Format Interface Specification, December 1987) and the ANSI document T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). It also implements the protocol that is described in the AT&T publication TR 54016 (Requirements for Interfacing DTE to Services Employing ESF - September 1989). In addition, it provides a number of important performance parameters involved in monitoring T1 lines such as Errored Seconds, Severly Errored Second, and Unavailable Seconds.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

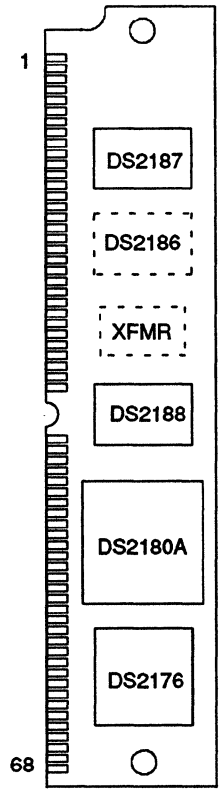
DALLAS SEMICONDUCTOR

DS2283
Enhanced T1 Line Card Stik

FEATURES

- Pre-tested, snap-in T1 line card
- Consumes only 2 square inches of board space
- Performs six functions:
  - line interface
  - clock recovery/dejittering
  - framing
  - monitoring
  - buffering
  - robbed–bit signaling extraction
- Includes line interface transformers and termination resistors
- Three separate loopback modes: payload, line, and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- Fully CMOS for low power consumption
- Operates off a single +5V supply

PIN ASSIGNMENT



DESCRIPTION

The DS2283 is a T1 line card that consumes only two square inches of printed circuit board space. The card is designed to plug into standard 68-pin, single in-line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to T1 DSX-1 twisted pair lines. The line interface function is performed by the DS2187 Receive Line Interface and DS2186 Transmit Line Interface. The dejittering of the clock and data is performed by the DS2188 T1/CEPT Jitter Attenuator. The monitoring and framing functions are performed by the DS2180A T1/ISDN Primary Rate Transceiver. The buffering and robbed-bit signaling extraction functions are handled by the DS2176 Elastic Store with Signalling Buffer. The DS2283 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC-6 errors, and bipolar violations.

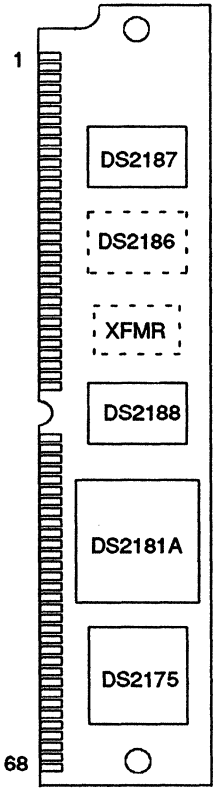
DALLAS SEMICONDUCTOR

DS2284
Enhanced CEPT Line Card Stik

FEATURES

- Pretested, Snap-In CEPT (E1) line card
- Consumes only 2 square inches of board space
- Performs five functions:
  - line interface
  - clock and data dejittering
  - framing
  - monitoring
  - buffering
- Includes line interface transformers and termination resistors
- Pin compatible with the DS2283 Enhanced T1 Line Card Stik
- Two separate loopback modes: line and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- User programmable for either 75 ohm or 120 ohm interfaces
- Fully CMOS for low power consumption
- Operates off a single +5V supply

PIN ASSIGNMENT



DESCRIPTION

The DS2284 is a CEPT (E1) line card that consumes only 2 square inches of printed circuit board space. The card is designed to plug into standard 68-pin Single In-Line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to either CEPT 2.048Mbps 75 or 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The dejittering of the clock and data is performed by the DS2188. The monitoring and framing functions are performed by the DS2181A. The buffering function is handled by the DS2175. The DS2284 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC errors, and bipolar violations.

FULL DATA SHEET AVAILABLE - CALL 214-450-3836

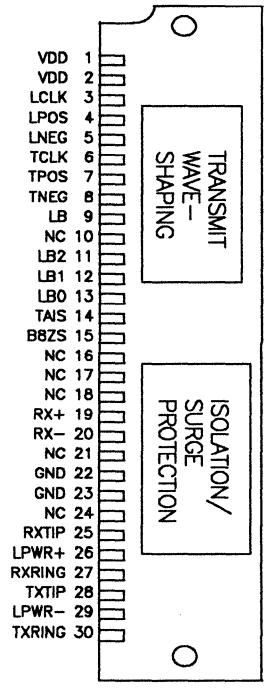
DALLAS SEMICONDUCTOR

DS2290
T1 Isolation Stik

FEATURES

- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403-1989 for transmit pulse characteristics
- Line build outs of 0dB, -7.5dB, and -15dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION

The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre-registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping circuitry that creates transmit pulses meeting the latest T1 specifications including TR 62411 (Accunet* T1.5 Service Description and Interface Specifications, - December 1988) and T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

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* Service mark of AT&T Communications

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

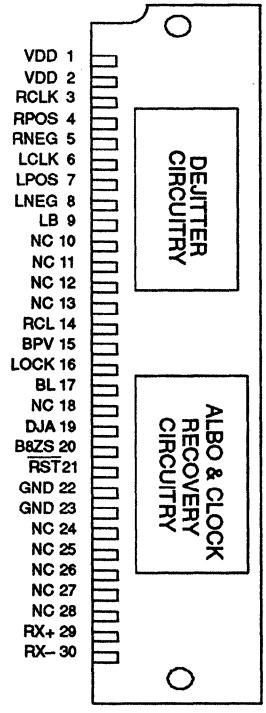
DALLAS SEMICONDUCTOR

DS2291
T1 Long Loop Stik

FEATURES

- Recovers clock and data off of T1 lines from 0 to 6,000 feet in length
- +0 to -30dBSX receiver sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- Dejitters the recovered clock and data
- Meets TR 62411 for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

STIK LAYOUT



(ACTUAL SIZE)

DESCRIPTION

The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data off a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6,000 feet. It also will dejitter the recovered clock and data according the jitter attenuation curves outlined in AT&T Communications Document TR 52411 (Accunet* T1.5 Service Description and Interface specification – December 1988). Applications area include Channel Service Units (CSU), T1 monitoring equipment, and T1 test equipment.

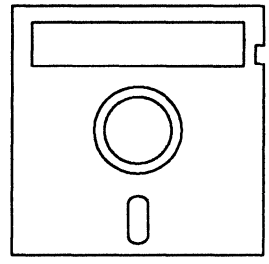
FULL DATA SHEET AVAILABLE – CALL 214-450-3836

DALLAS SEMICONDUCTOR

DS0065
TeleMicro Interface System Software

FEATURES

- Modem control software for the DS2244T TeleMicro Stik
- Multi-tasking between application code and modem control code
- Frees the user from understanding complex modem protocols
- Speeds system development
- Compact assembly language uses minimal memory
- Entire library requires 7K bytes of program memory
- Optional routines may be omitted from memory
- Simplified user interface–one system call
- Easily modifiable source code allows customization
- Allows DS2244T to be reloaded by phone
- C-callable routines
- Library of functions includes:
  - Multitasking system executive routine
  - Software UART routine
  - Originate only routine
  - Answer only routine
  - Remote reloader routine
  - Hang-up routine
  - DTMF decode routine
  - Phantom DAA operations
  - Test modes routine
- Supports numerous user-selectable parameters
- Provides complete status reporting
- Phantom DAA (DS2249PH) support



DESCRIPTION

The DS0065 TeleMicro Interface System is a library of software subroutines and parameter structures that can be combined with user application software in the DS2244T TeleMicro Stik. The DS2244T is an 8-bit microcontroller that incorporates 32K of nonvolatile RAM, a real-time clock, DTMF decoding and modem features. This device allows the user to execute specialized application software and to incorporate data communications by telephone. Embedded systems using the DS2244T can benefit from its integral modem when performing a variety of tasks such as data logging (including time stamp and date) with telephone reporting, remote control by telephone, and embedded control with telephone status reporting. Interaction of the user's application software with the outside world is conducted via the onboard modem. The DS0065 package is designed to simplify this interface, freeing the user from learning the intricacies of modem communication and minimizing the time required to incorporate modem communication into the embedded control realm. The DS0065 allows system designers to concentrate on the application design. A simple software interface is provided with one entry point. However, the library is designed to handle the majority of tasks concerning data communication from intitialization of modem parameters to terminating the telephone call. The multitasking system included as part of the DS0065 provides an orderly means of switching between modem control tasks and application code with minimal disruption.

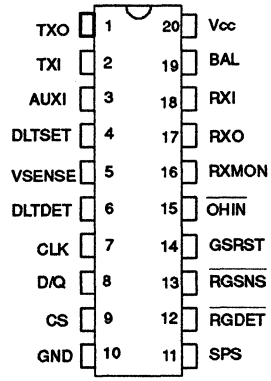
DALLAS SEMICONDUCTOR

DS1360
Phantom DAA Chip

FEATURES

- Single-chip DAA controller for:
  - Modems
  - Speech interfaces
- Phantom operation reports loop current changes back to host
- Allows the DAA to use an existing phone line unobtrusively
- Transmit/receive interface connects directly to 600 ohm phone-line coupling transformers
- On-chip electronic 2- to 4-wire converter
- Integrates FCC Part–68 DAA requirements:
  - Ring detection
  - 2-second billing delay
  - Transmit power limiter
- Onboard, low-pass filtering of transmit and receive signals
- Replaces up to 20 discrete components
- Voice/data switching
- Software-controlled receive gain
- 3-wire serial control port
- +5 Volt single-supply operation
- DS1360S surface mount version available

PIN ASSIGNMENT



DS1360 20–Pin DIP
(300 MIL)

DESCRIPTION

The DS1360 Phantom DAA Chip is a CMOS device that integrates FCC requirements for interfacing data and voice to the telephone network. The DS1360 meets FCC Part-68 specifications such as 2-second billing delay, transmit signal power limiting, and ringing detection. It also offers programmable transmit and receive gains and an on-chip 2- to 4-wire converter (hybrid). By adding a coupling transformer, a relay, and an optocoupler, a complete DAA circuit can be quickly designed.

A unique feature of the DS1360 is its ability to sense loop current using an on-chip, 8-bit A/D converter. By using an external optocoupler (for proper isolation), the phone loop current can be digitized and monitored through the serial port by a host processor. The DS1360 can also be programmed by external resistors to report when the current has changed by a certain percentage. Loop current sensing is important for monitoring the activity of extension phones or for determining loop length for cable compensation.

DALLAS SEMICONDUCTOR

DS2244T
TeleMicro Stik

FEATURES

- 8-bit microcontroller system with integral modem
  - Fully user-programmable
  - 32K x 8 NV RAM for program/data memory
  - 24 general-purpose port pins for user I/O
  - 10 year data retention without V_{CC}
  - Based on standard 8051 instruction set
- Integral modem provides outside data access
  - Supports Bell 212A/103 & CCITT V.22bis/V.22/V.21
  - 1200 or 2400 bps modem versions available
  - Transfers data from connector or uC memory
- DS0065 software support library available
- Permanently powered real-time clock/calendar
  - Time of day interrupt alarm
  - Periodic interrupt alarm
- DTMF generation and detection
- Low-power +5V only operation
- Standard 30-pin SIMM connection scheme

PIN NAMES

1	P3.5 (T1)	16	P3.6 ($\overline{WR}$)
2	P3.1 (TXD)	17	ALE
3	P1.4 ($\overline{OH}$)	18	P3.0 (RXD)
4	P1.5 ($\overline{RI}$)	19	P3.2
5	P2.0	20	P0.0
6	P2.1	21	AIN
7	P2.2	22	P0.1
8	P2.3	23	P0.2
9	P2.4	24	P0.3
10	P2.5	25	P0.4
11	P2.6	26	P0.5
12	VCC	27	P0.6
13	P2.7 (RXCLK)	28	AOUT
14	GND	29	P0.7
15	P3.7 ($\overline{RD}$)	30	$\overline{PROG}$

DESCRIPTION

The DS2244T TeleMicro Stik is an 8-bit, 8051-compatible microcontroller system that is based on nonvolatile RAM and that incorporates an integral modem and DTMF decoder. 32K x 8 of nonvolatile SRAM is available for program and data memory storage. The DS2244T also includes a permanently powered real-time clock/calendar (RTC). Twenty-four port pins are available for user-defined I/O. The nonvolatile memory and permanently powered clock/calendar allow data to be recorded, logged to nonvolatile memory with time stamp and date, and reported via the phone line at a later time. Using the alarm capabilities of the integral timekeeper, the DS2244T can originate a telephone call report at a predetermined time and date. Date and time of day will be retained by lithium-backed circuitry in the absence of power for at least 10 years at 25° C. The DS2244T can serve a wide range of functions from a diagnostic processor with automatic reporting to a specialized modem by providing a full-function, user-programmable microcontroller coupled to an integral modem. The user's application software can access any feature of the DS2244T with few restrictions. However, interaction with the on board modem can be greatly simplified using the DS0065 TeleMicro Interface System software. This package provides a multi-tasking environment that controls the modem and performs other user-requested tasks. More detail is available in the DS0065 TeleMicro Interface System data sheet.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

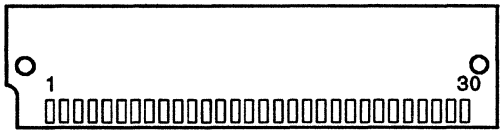
DALLAS SEMICONDUCTOR

DS2245
Soft Modem Stik

FEATURES

- Bell 212A/103 and CCITT V.22bis/V.22/V.21
- Full-duplex operation at 2400, 1200 and 300 bps
- Familiar AT command set
- FCC Part-68 pre-certified when used w/DS2249 DAA
- Teleservicing mode allows reloading/monitoring of DS2250 Soft microcontroller Stik
- Provides remote software updates without host cooperation
- Generates and interprets DTMF tones
- Auto-answer and Originate modes
- Parallel interface connects to PC or other bus
- Reprogrammable with firmware upgrades
- +5V operation
- Low power operation consumes under 400 mW
- Extremely small form factor
- 30-pin SIMM connection scheme

PIN ASSIGNMENT



ORDERING INFORMATION

DS2245-12U	1200 BPS U.S. ONLY
DS2245-24	2400 BPS INT'L.

PIN NAMES

1	CP.2	16	D7
2	CP.1	17	D6
3	$\overline{OH}$	18	$\overline{WR}$
4	$\overline{RI}$	19	D5
5	SPEN	20	$\overline{RD}$
6	CP.3	21	AIN
7	CP.0	22	NC
8	D4	23	A2
9	D3	24	A1
10	D2	25	A0
11	D1	26	$\overline{OUT1}$
12	VCC	27	UR
13	D0	28	AOUT
14	GND	29	INT
15	$\overline{CS}$	30	$\overline{PROG}$

DESCRIPTION

The DS2245 Soft Modem Stik is a data communication subsystem which forms a complete 2400/1200/300 bps modem when combined with the DS2249 DAA. The DS2245-24 supports V.22bis, V.22, V.21 as well as Bell 212A and 103. The DS2245-12U supports the latter Bell standards only. In addition to industry-standard, AT-type commands, the DS2245 provides decoding of incoming DTMF tones. This allows a host system to accept commands from a remote site where a modem is not available. A unique Teleservicing mode allows a central location to dial up a remote system and examine, edit, or reload the program/data memory contents of that system. The DS2245 is designed for embedded applications that benefit from communication with the outside world, and for which a familiar AT command set is desired.

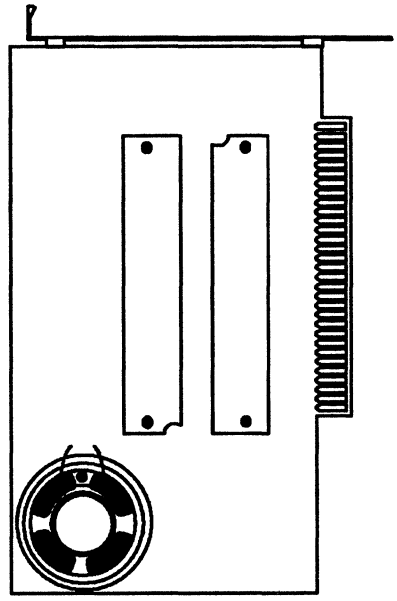
FULL DATA SHEET AVAILABLE – CALL 214-450-3836

DALLAS SEMICONDUCTOR

DS2245K
Soft Modem PC Evaluation Kit

FEATURES

- PC evaluation kit for DS2249 DAA and DS2245 Soft Modem
- For use in PC XT/AT-compatible computers
- Terminal emulation software included
- Provides reprogramming fixture for DS2245 family
- Selectable COM1 or COM2
- AT command set-compatible
- DTMF detection
- Call progress detection
- Speaker for audio monitoring
- FCC Part 68 approved



DESCRIPTION

The DS2245K is an evaluation kit and programming fixture for the DS2245 family of modem Stiks. It includes a DS2245-24 modem and DS2249 DAA. The evaluation kit slides into a normal XT/AT 8-bit expansion slot and acts as either a COM1 or COM2 serial port. Software that is included with the kit provides communication control and allows reprogramming of DS2245 series Stiks. The PC card also incorporates a high quality speaker for monitoring of a call connection. The DS2245K provides a convenient platform for evaluation of the DS2245 and DS2249 family, as well as providing a convenient fixture for loading program upgrades into the modems. New modem control programs can be loaded directly into the DS2245 from a diskette.

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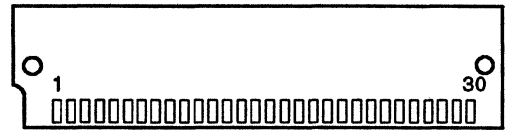
DALLAS SEMICONDUCTOR

DS2245M
Soft Modem w/MNP

FEATURES
- Bell 212A/103 and CCITT V.22bis/V.22/V.21
- Full-duplex operation 2400, 1200, 300 bps
- MNP-5 error correction/data compression
- Error-free transmission on noisy lines
- Up to 200% throughput enhancement from data compression
- Speed matching with flow control
- DTE speed up to 9600 bps
- Optimized AT command interpreter
- Automatic call for help
- Reprograms Dallas Semiconductor Softeners
- Generates and interprets DTMF tones
- Auto-answer and originate modes
- Parallel interface connects to PC or other bus
- +5V only operation
- Low-power operation consumes under 400 mW
- Extremely small form-factor
- Pin-compatible with DS2245
- 30-pin SIMM connection scheme

PIN ASSIGNMENTS



ORDERING INFORMATION

DS2245M-24	2400 bps MNP modem
DS2245ML-24	2400 bps MNP modem, w/no DTMF detection

PIN NAMES

1	CP.2	16	D7
2	CP.1	17	D6
3	$\overline{OH}$	18	$\overline{WR}$
4	$\overline{RI}$	19	D5
5	SPEN	20	$\overline{RD}$
6	CP.3	21	AIN
7	CP.0	22	NC
8	D4	23	A2
9	D3	24	A1
10	D2	25	A0
11	D1	26	$\overline{OUT1}$
12	VCC	27	UR
13	D0	28	AOUT
14	GND	29	INT
15	$\overline{CS}$	30	$\overline{PROG}$

DESCRIPTION

The DS2245M Soft Modem with MNP is a data communications subsystem which forms a complete 2400/1200/300 bps modem when combined with the DS2249 DAA. Embedded software in the DS2245M is capable of sophisticated error correction and data compression using MNP level 5. This software allows the DS2245M to negotiate with the remote modem in order to determine the highest level of protocol that is mutually supported. The DS2245M supports V.22bis, V.22/V.21 and Bell 212A/103 standards. In addition to industry-standard commands and MNP-5, the Soft Modem provides decoding of incoming DTMF tones. This allows a host system to accept commands from a remote site where a modem is not available. The DS2245M is optimized for embedded applications that require reliable communication and for which an AT command set is desired. A unique Teleservicing mode allows a central location to dial up the remote system and examine, edit, or reload the program/data memory contents of that system. The DS2245M is also capable of initiating a call for help when using a Dallas Semiconductor Softener and reloading the soft processor by phone.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

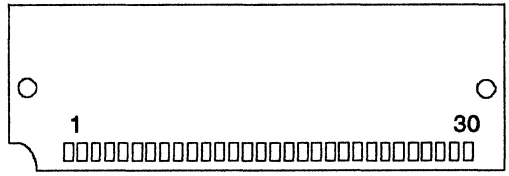
DALLAS SEMICONDUCTOR

DS2249
Data Access Arrangement (DAA) Stik

FEATURES

- Direct connection to the public switched telephone network
- FCC Part-68 compatible with 1000 volts isolation
- User-transferable FCC registration when used with DS2245 Soft Modem Stik
- Single +5 volt supply
- Ring detection
- 2- to 4-wire converter
- Audio monitor output
- 30-pin SIMM connection scheme

PIN ASSIGNMENT



30-PIN SIMM

PIN NAMES

PIN #	PIN NAME
1	$\overline{OH}$
2	AUDIO
3	TXA
4	RXA
5-9	NC
10	VCC
11	GND
12	$\overline{RI}$
13-26	NC
27	RINGO
28	TIPO
29	RING
30	TIP

DESCRIPTION

The DS2249 Data Access Arrangement (DAA) Stik is designed to provide direct connection to the public switched telephone network through an appropriate connector such as an RJ-11. The DS2249 DAA carries a user-transferable, FCC Part-68 registration when used with the DS2245 modem. It is easily registrable with any other data/voice communication circuitry, provided that this circuitry performs output power limiting and billing delay. Included in the DS2249 is a ring detection output, a 2- to 4- wire converter for use with modems such as the DS2245, and an audio output for connection to speaker circuitry. It operates from a single +5 volt source.

Applications include laptop computers, remote data collection, or any application which can benefit from data or voice communication by telephone.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

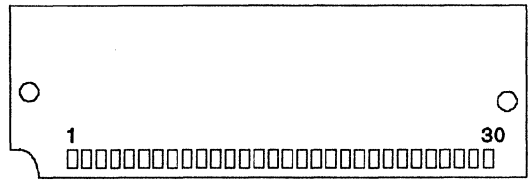
DALLAS SEMICONDUCTOR

DS2249PH/EU
Phantom/European DAA Stik

FEATURES

- Interfaces voice/data to the public switched telephone network
- DS2249PH
  - FCC Part 68-DP registered
  - 1000 Vrms isolation
- DS2249EU
  - 3750 Vrms isolation
  - Meets most European requirements
- Single +5 volt supply operation
- Phantom feature monitors DC loop current
  - Reports changes to host
  - Allows unobtrusive access to existing phone lines
- Ring detection
- 2- to 4-wire converter
- Audio output monitor
- System monitoring and control
  - power up equipment on ring detect
  - Early warning $\overline{NMI}$ to uP
  - uP reset when V_{CC} is out of tolerance
  - Watchdog timer
  - Wink detection (DS2249PH only)
- 30-pin SIMM connection scheme

PIN ASSIGNMENT



PIN NAMES

1	$\overline{OH}$	16	$\overline{ST}$
2	AUDIO	17	$\overline{PSI}$
3	TXA	18	PSO
4	RXA	19	V_{BAT}
5	AUXI	20	RINGDIS
6	SCLK	21	$\overline{RST}$
7	D/Q	22	IN
8	CS	23	$\overline{NMI}$
9	SPS	24	WINK (DS2249PH ONLY)
10	V_{CC}	25	NC
11	GND	26	NC
12	$\overline{RI}$	27	RINGO
13	BAL	28	TIPO
14	GSRST	29	RING
15	DLTDET	30	TIP

DESCRIPTION

The DS2249PH Data Access Arrangement (DAA) Stik provides data communication equipment (modem) with direct connection to the public switched phone network and has been registered by the FCC under Part 68-DP. This user-transferable registration includes isolation and protection, billing delay, and power limiting so that no further certification is required under Part-68. The DS2249PH also features extensive system monitoring and control capability which had been previously unavailable in a DAA. The DS2249PH has been tailored to embedded systems by providing these additional capabilities while saving power and space.

FULL DATA SHEET AVAILABLE – CALL 214-450-3836

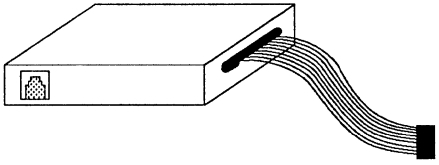
DALLAS SEMICONDUCTOR

DS6071A TeleMemory System
DS6071K TeleMemory Evaluation Kit

FEATURES

- Teleservicing retrofit system
- Connects to a standard 28-pin, bytewide RAM socket through a ribbon cable
- Uploads memory contents from any remote system
- Allows remote examination/editing of data memory
- Distributes new embedded application software by telephone
- MNP Level 5 error correction guarantees accurate data transmission
- Data compression minimizes phone line charges
- FCC Part-68 registered for immediate connection to phone line
- Multiple connecting options via modem
  - Modem connects at 2400 or 1200 bps
  - V.22bis, V.22, & Bell212
  - Answers on a programmable number of rings
  - Varies the number of rings with time of day
- Holds host processor in reset allowing program code updates
- No additional engineering required
- Eurocard box includes three Teleservicing Stiks:
  - DS2249 DAA
  - DS2244T Modem (with TeleMemory software)
  - DS2230T Dual Port NVRAM
- Evaluation kit (DS6071K) includes DS0020 Service Coordinator software for the PC
- Direct RJ11 connection to phone line
- +5V operation, powered from ribbon cable

PACKAGE OUTLINE



ORDERING INFORMATION

DS6071A	TeleMemory System
DS6071K	TeleMemory Evaluation Kit (includes DS0020 software)

PIN NAMES

1	A14 (or V_{PP})	15	DQ3
2	A12	16	DQ4
3	A7	17	DQ5
4	A6	18	DQ6
6	A4	20	$\overline{CE}$
7	A3	21	A10
8	A2	22	$\overline{OE}$
9	A1	23	A11
10	A0	24	A9
11	DQ0	25	A8
12	DQ1	26	A13
13	DQ2	27	$\overline{WE}$ (or A14)
14	GND	28	V_{CC}

*Alternate functions shown in parentheses ( ) are used in retrofitting EPROM applications.

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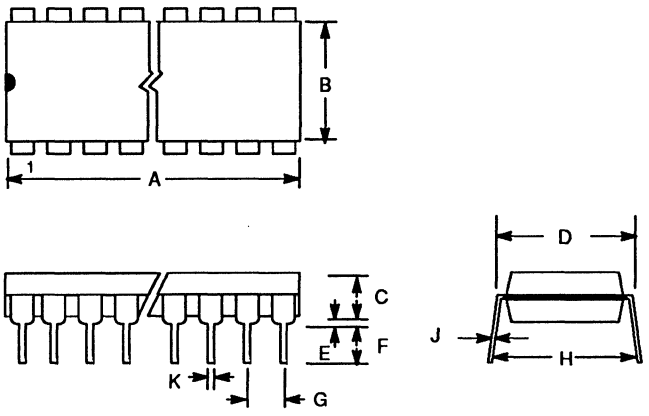
8- TO 28-PIN DIP (300 MIL)



Includes:

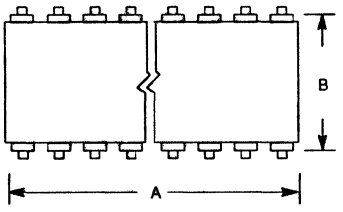
DS1000	DS1215	DS1291
DS1000M	DS1218	DS1293
DS1003	DS1221	DS1336
DS1003M	DS1222	DS1385
DS1005	DS1228	DS1602
DS1005M	DS1229	DS1610
DS1007	DS1231	DS1632
DS1010	DS1232	DS1640
DS1012M	DS1232LP	DS1651
DS1013	DS1234	DS1652B
DS1013M	DS1236	DS1653
DS1020	DS1237	DS1669
DS1040M	DS1238	DS2009D
DS1200	DS1239	DS2010D
DS1206	DS1259	DS2011D
DS1210	DS1267	DS2013D
DS1211	DS1275	

PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.O4	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

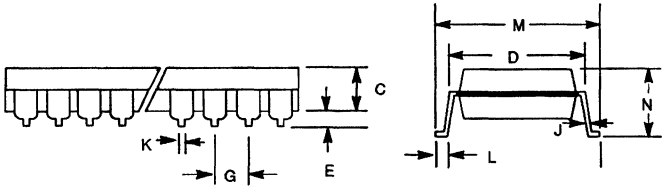
Continued on following page.

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	1.020	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	25.91	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.260	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.10	6.60	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
MM	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56

8- TO 20-PIN GULLWING (300 MIL)

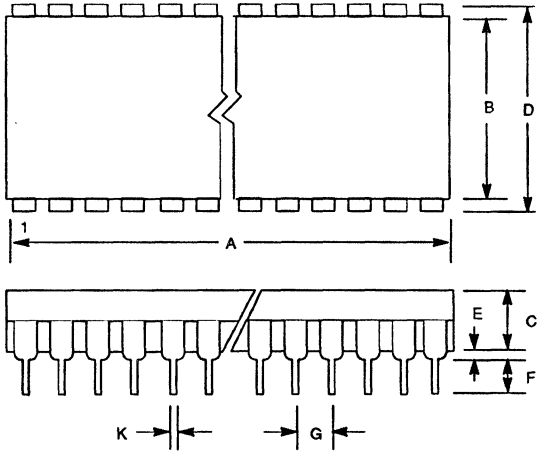


Includes:
DS1000G
DS1000H
DS1003G
DS1003H
DS1005G
DS1005H
DS1010G
DS1013G
DS1013H
DS1040H



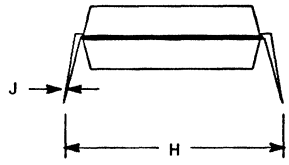
PKG	8-PIN		14-PIN		16-PIN		20-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.345	0.400	0.740	0.780	0.740	0.780	0.960	1.040
MM	8.76	10.16	12.19	13.20	18.79	9.81	24.38	26.41
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53
L IN.	0.030	0.050	0.030	0.050	0.030	0.050	0.030	0.050
MM	0.76	1.27	0.76	1.27	0.76	1.27	0.76	1.27
M IN.	0.370	0.420	0.370	0.420	0.370	0.420	0.370	0.420
MM	9.40	10.67	9.40	10.67	9.40	10.67	9.40	10.67
N IN.	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
MM	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57

24- TO 40-PIN DIP (600 MIL)



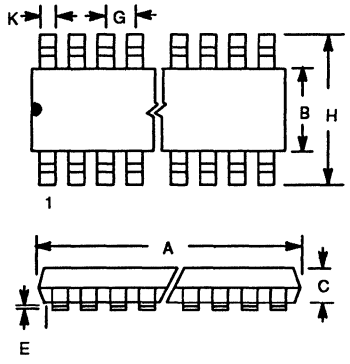
Includes:

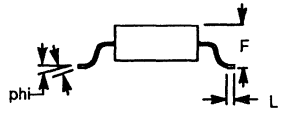
DS1212	DS2010
DS1262	DS2011
DS1277	DS2012
DS1284	DS2013
DS1380	DS2016
DS1485	DS2064
DS1609	DS2257
DS2009	



PKG	24-PIN		28-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	1.245	1.270	1.445	1.470	2.050	2.075
MM	31.62	32.25	36.70	37.34	52.07	52.71
B IN.	0.530	0.550	0.530	0.550	0.530	0.550
MM	13.46	13.97	13.46	13.97	13.46	13.97
C IN.	0.140	0.160	0.140	0.160	0.140	0.160
MM	3.56	4.06	3.56	4.06	3.56	4.06
D IN.	0.600	0.625	0.600	0.625	0.600	0.625
MM	15.24	15.88	15.24	15.88	15.24	15.88
E IN.	0.015	0.050	0.015	0.040	0.015	0.040
MM	0.380	1.27	0.380	1.02	0.380	1.02
F IN.	0.120	0.145	0.120	0.145	0.120	0.145
MM	3.05	3.68	3.05	3.68	3.05	3.68
G IN.	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.625	0.675	0.625	0.675	0.625	0.675
MM	15.88	17.15	15.88	17.15	15.88	17.15
J IN	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.022	0.015	0.022	0.015	0.022
MM	0.38	0.56	0.38	0.56	0.38	.56

8-PIN SOIC (150 MIL AND 200 MIL)



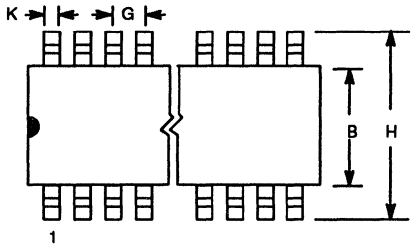


150 mil Includes:
DS1000Z
DS1003Z
DS1012Z
DS1040Z
DS1218D
DS1203S-B1

200 mil Includes:
DS1232S-2
DS1232LPS-2
DS1602S
DS1651S
DS1652S
DS1669S

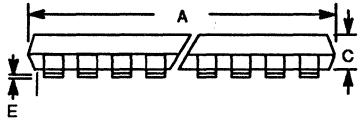
PKG	8-PIN (150 MIL)		8-PIN (200 MIL)	
DIM	MIN	MAX	MIN	MAX
A IN.	0.188	0.196	0.203	0.213
MM	4.78	4.98	5.16	5.41
B IN.	0.150	0.158	0.203	0.213
MM	3.81	4.01	5.16	5.41
C IN.	0.052	0.062	0.070	0.074
MM	1.32	1.57	1.78	1.88
E IN.	0.004	0.010	0.004	0.010
MM	0.10	0.25	0.10	0.25
F IN.	0.058	0.068	.074	.084
MM	1.47	1.73	1.88	2.13
G IN.	.050 BSC			
MM	1.27 BSC			
H IN	0.230	0.244	0.302	0.318
MM	5.84	6.20	7.67	8.07
J IN	0.007	0.010	0.006	0.010
MM	0.17	0.25	0.15	0.25
K IN.	0.013	0.019	0.013	0.020
MM	0.33	0.49	0.33	0.51
L IN.	.016	.035	.019	.030
MM	.40	.89	0.48	.76
phi	0°	8°	0°	8°

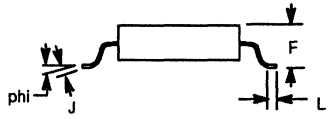
16-, 20-, AND 24-PIN SOIC (300 MIL)



Includes:

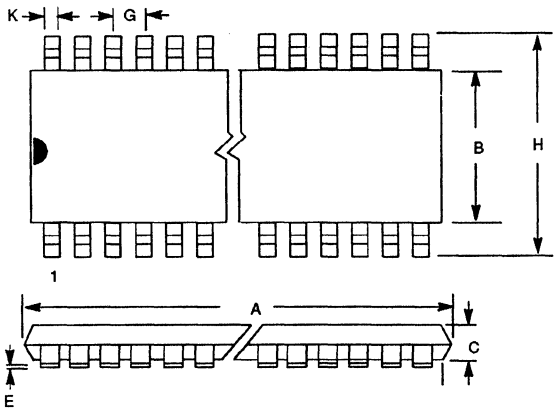
DS1000S	DS1221S	DS1259SDS
DS1005S	DS1222S	1267S
DS1007S	DS1227S	DS1336S
DS1010S	DS1231S	DS1359S
DS1013S	DS1228S	DS1380S
DS1020S	DS1229S	DS1609S
DS1200S	DS1232S	DS1610S
DS1205S	DS1232LPS	DS1632S
DS1206	DS1234S	DS1640S
DS1209S-B1	DS1236S	DS1652BS
DS1210S	DS1237S	DS1653S
DS1211S	DS1238S	DS2107S
DS1215S	DS1239S	

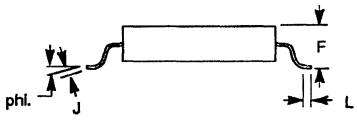




PKG	16-PIN		20-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.402	0.412	0.500	0.511	0.602	0.612
MM	10.21	10.46	12.70	12.99	15.29	15.54
B IN.	0.290	0.300	0.290	0.300	0.290	0.300
MM	7.37	7.65	7.37	7.65	7.37	7.65
C IN.	0.089	0.095	0.089	0.095	0.089	0.095
MM	2.26	2.41	2.26	2.41	2.26	2.41
E IN.	0.004	0.012	0.004	0.012	0.004	0.012
MM	0.102	0.30	0.102	0.30	0.102	0.30
F IN.	0.094	0.105	0.094	0.105	0.094	0.105
MM	2.38	2.68	2.38	2.68	2.38	2.68
G IN.	.050 BSC					
MM	1.27 BSC					
H IN	0.398	0.416	0.398	0.416	0.398	0.416
MM	10.11	10.57	10.11	10.57	10.11	10.57
J IN	0.009	0.013	0.009	0.013	0.009	0.013
MM	0.229	0.33	0.229	0.33	0.229	0.33
K IN.	0.013	0.019	0.013	0.019	0.013	0.019
MM	0.33	0.48	0.33	0.48	0.33	0.48
L IN	.016	.040	.016	.040	.016	.040
MM	.40	1.02	.406	1.20	.40	1.02
phi	0°	8°	0°	8°	0°	8°

24- AND 28-PIN 330 MIL SOIC

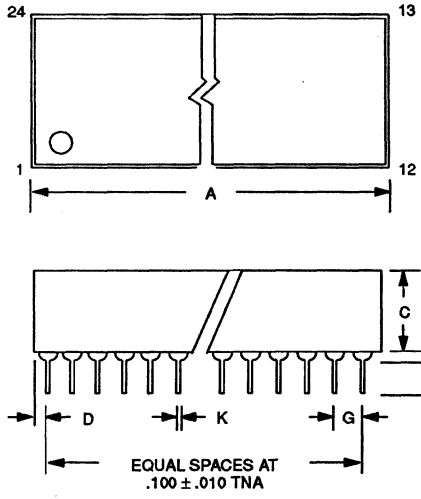




330 Mil Package Includes:	350 Mil Package Includes:
DS2016S	DS1385S
DS2064S	DS1485S
DS2257S	DS1262S

PKG	330 MIL BODY				350 MIL BODY	
	24-PIN		28-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	.594	.602	0.697	0.705	0.706	0.728
MM	15.10	15.30	17.7	17.9	17.93	18.49
B IN.	.327	.335	0.327	0.335	0.338	0.350
MM	8.30	8.50	8.3	8.5	8.58	8.89
C IN.	.0925	.104	0.093	0.104	0.086	0.110
MM	2.35	2.65	2.35	2.65	2.18	2.79
E IN.	.007	.008	0.007	0.008	0.002	0.014
MM	.19	.21	0.19	0.21	0.051	0.356
F IN.	.106 TYP.				0.090	0.124
MM	2.7				2.29	3.15
G IN.	.050 BSC				0.050 BSC	
MM	1.27				1.27	
H IN	0.452	.477	0.452	0.477	0.460	0.480
MM	11.5	12.1	11.5	12.1	11.68	12.19
J IN	.004	.008	0.004	0.008	0.006	0.013
MM	.10	0.20	0.10	0.20	0.152	0.32
K IN.	.012	0.20	0.012	0.020	0.014	0.020
MM	.30	0.50	0.30	0.50	0.36	0.51
L IN.	0.039 TYP		0.039 TYP		0.020	0.050
MM	1.0		1.0		0.51	1.27
phl	0°	8°	0°	8°	0°	8°

16- AND 24- PIN ENCAPSULATED PACKAGE (FLUSH BOTTOM – 450 MIL.)

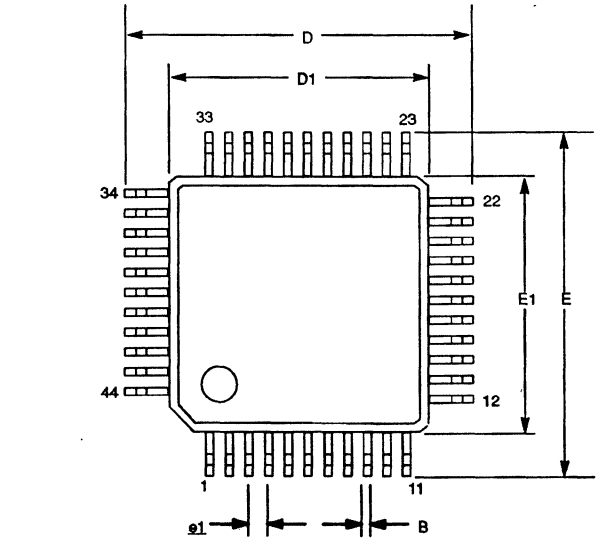


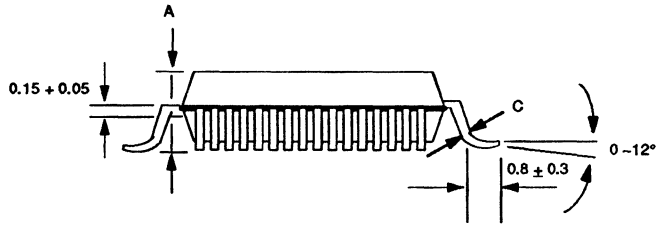
Includes:
DS1290
DS1292

PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.820	0.840	1.310	1.330
MM	20.83	21.34	33.27	33.78
B IN.	0.440	0.460	0.440	0.460
MM	11.18	11.68	11.18	11.68
C IN.	0.330	0.370	0.330	0.370
MM	8.38	9.40	8.38	9.40
D IN.	0.180	0.210	0.215	0.245
MM	4.57	5.33	5.46	6.22
E IN.	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02
F IN.	0.110	0.140	0.110	0.140
MM	2.79	3.56	2.79	3.56
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN	0.330	0.380	0.330	0.380
MM	8.38	9.65	8.38	9.65
J IN	0.008	0.012	0.008	0.012
MM	0.20	0.31	0.20	0.31
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53

NOTE: On 16-pin package, pins 1 and 16 are missing by design. On 24-pin package, pins 1 and 24 are missing by design.

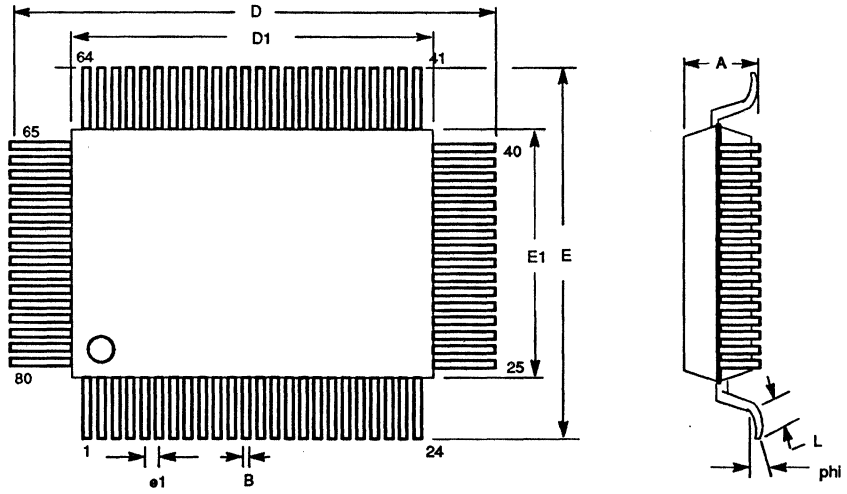
44-PIN QUAD FLAT PACK (PRELIMINARY)





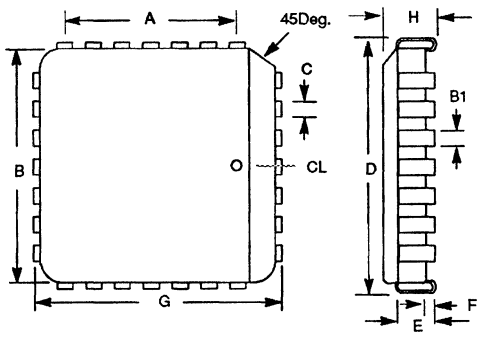
PKG	10 X 10 BODY		14 X 14 BODY	
DIM	MIN	MAX	MIN	MAX
A MM	–	2.45	–	3.4
B MM	0.30	0.45	0.20	0.50
C MM	0.13	0.23	0.10	0.20
D MM	13.65	14.35	16.95	18.00
E MM	13.65	14.35	16.95	18.00
D1MM	9.90	10.10	13.80	14.20
E1MM	9.90	10.10	13.80	14.20
L MM	0.65	0.95	0.50	1.10
e1 IN MM	0.315 0.80 BSC		0.039 1.00 BSC	

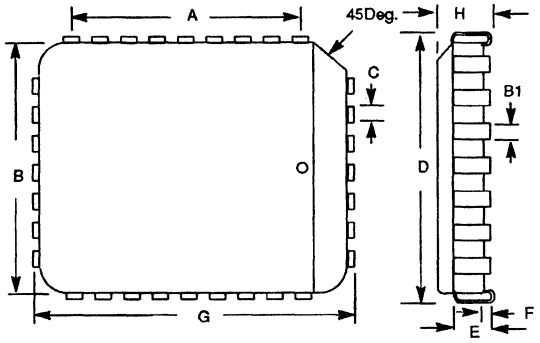
80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)



PKG	80-PIN	
DIM	MIN	MAX
A IN.	0.11	0.128
MM	2.80	3.25
B IN.	0.010	0.020
MM	0.25	0.45
e1 IN.	0.031	BSC
MM	0.80	BSC
D1 IN.	0.781	0.793
MM	19.85	20.15
E1 IN.	0.545	0.557
MM	13.85	14.15
E IN.	0.688	0.720
MM	17.50	18.30
D IN.	0.921	0.953
MM	23.40	24.20
L IN	0.025	0.038
MM	0.65	0.95
phi	0°	8°

28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)

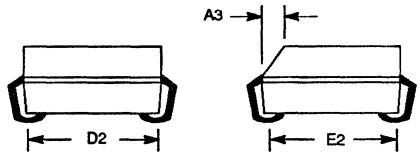




28- Pin Includes:
DS1212Q
DS1284Q
DS1285Q
DS12885Q

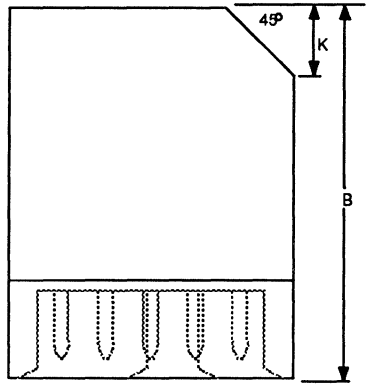
32-Pin Includes:
DS2009Q
DS2010Q
DS2011Q
DS2012Q

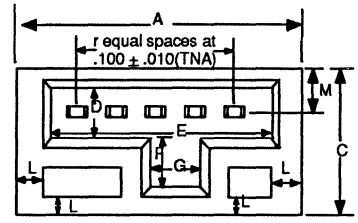
PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.300 BSC		0.400 BSC	
MM	7.62		10.16	
B IN.	0.445	0.460	0.442	0.460
MM	11.30	11.68	11.30	11.68
B1 IN	0.013	0.021	0.013	0.021
MM	0.33	0.53	0.33	0.53
C IN	0.027	0.33	0.027	0.33
MM	0.68	0.84	0.68	0.84
D IN.	0.480	0.500	0.480	0.500
MM	12.19	12.70	12.19	12.70
D2IN.	0.390	0.430	0.390	0.430
MM	9.91	10.92	9.91	10.92
E IN.	0.090	0.120	0.060	0.095
MM	2.29	3.05	1.52	2.41
E2IN.	0.390	0.430	0.490	0.530
MM	9.91	10.92	12.45	13.46
F IN.	0.020		0.015	
MM	0.51		0.38	
G IN	0.480	0.500	0.580	0.600
MM	12.19	12.70	14.7	15.24
H IN	0.165	0.180	0.100	0.140
MM	4.19	4.57	2.54	3.56

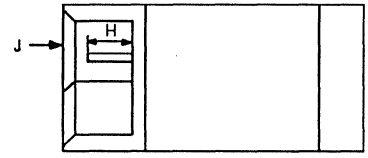


ELECTRONIC KEY/TAG

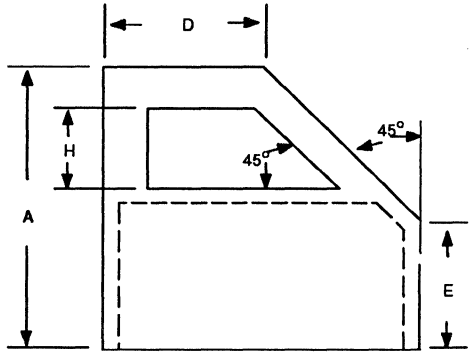
Includes:
DS1201
DS1204U
DS1205U
DS1207

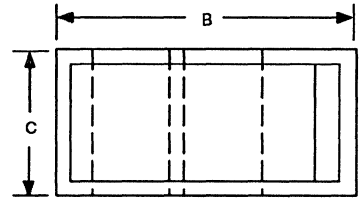






KEY/TAG CAP

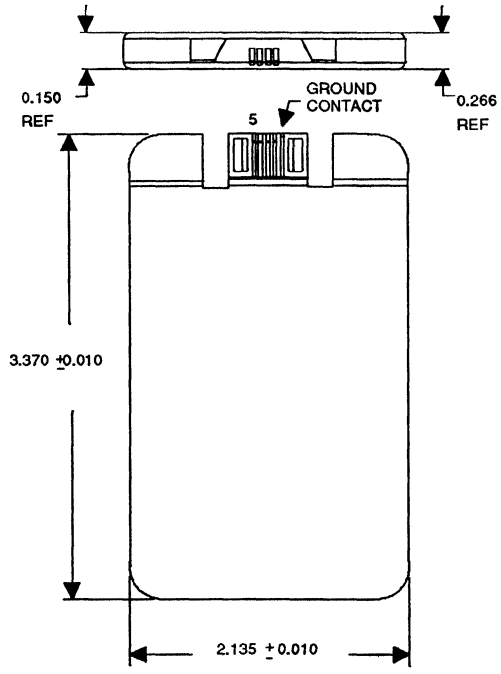


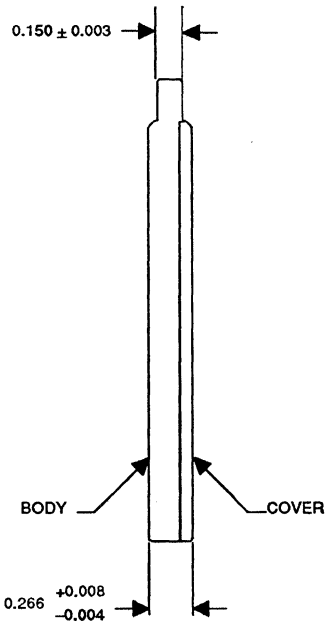


PKG	ELECTRONIC KEY/TAG		KEY/TAG CAP	
DIM	MIN	MAX	MIN	MAX
A IN.	0.610	0.650	0.790	0.810
MM	15.50	16.51	20.07	20.57
B IN.	0.740	0.760	0.680	0.700
MM	18.80	19.30	17.27	17.78
C IN.	0.310	0.355	0.405	0.425
MM	7.87	9.02	10.29	10.80
D IN.	0.100	0.110	0.290	0.310
MM	2.54	2.79	7.37	7.87
E IN.	0.505	0.515	0.410	0.430
MM	12.83	13.08	10.41	10.92
F IN.	0.100	0.110		
MM	2.54	2.79		

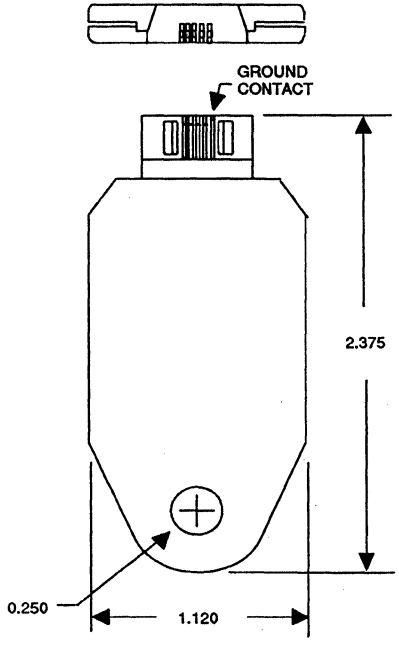
PKG	ELECTRONIC KEY/TAG		KEY/TAG CAP	
DIM	MIN	MAX	MIN	MAX
G IN.	0.100	0.110		
MM	2.54	2.79		
H IN	0.100	0.130		
MM	2.54	3.30		
J IN	0.030	0.060		
MM	0.76	1.52		
K IN.	0.045	0.055		
MM	1.14	1.40		
L IN.	0.045	0.055		
MM	1.14	1.40		
M IN.	0.100	0.110		
MM	2.54	3.30		

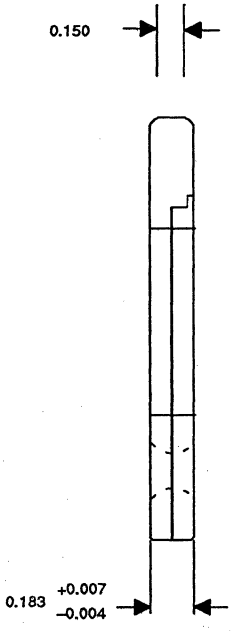
CYBERCARD PACKAGE





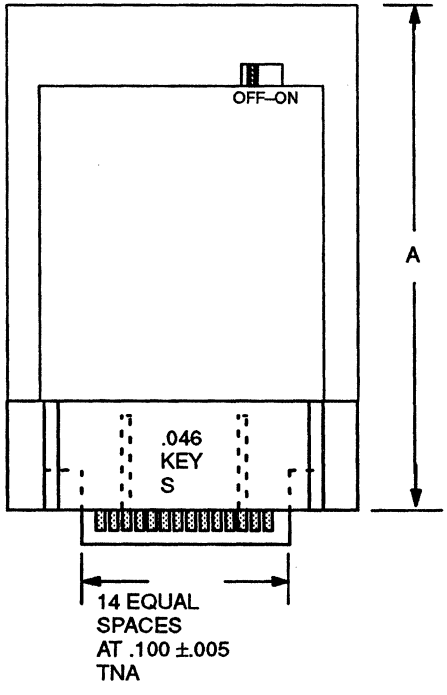
CYBERKEY PACKAGE



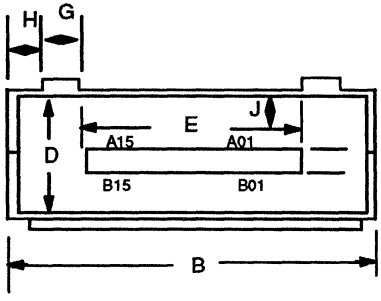


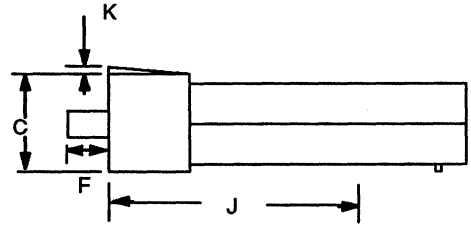
16

NON-VOLATILE READ/WRITE CARTRIDGE

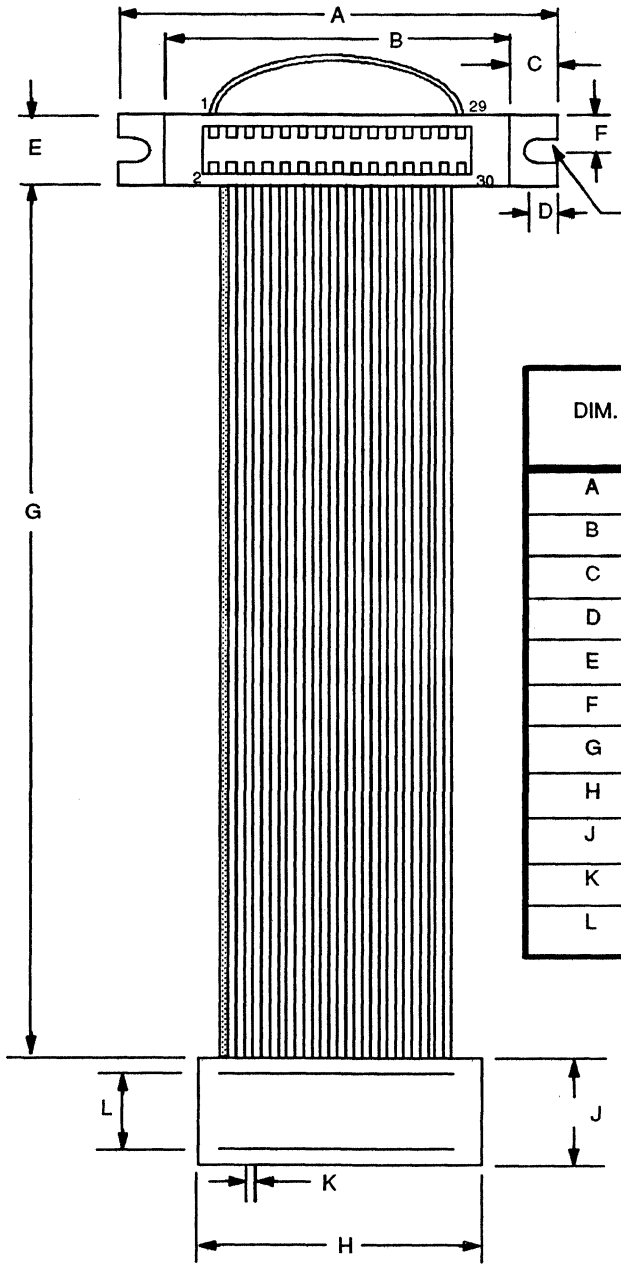


DIM	INCHES MIN	MAX
A	3.020	3.040
B	2.275	2.295
C	0.600	0.630
D	0.440	0.460
E	1.590	1.607
F	0.115	0.135
G	0.115	0.135
H	0.140	0.160
J	1.760	1.790
K	0.040	0.060





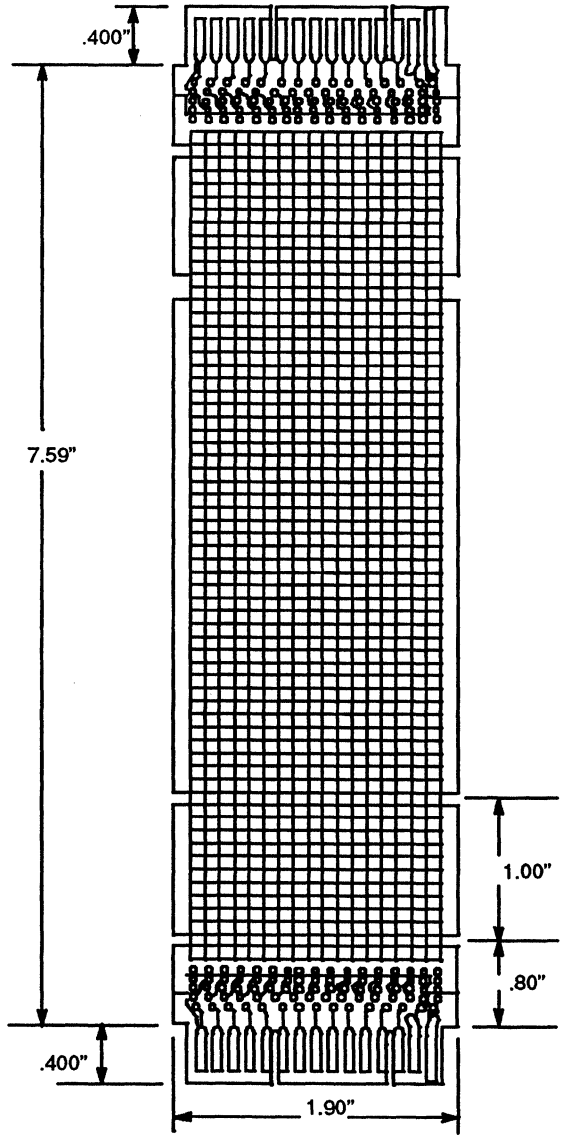
BYTEWIDE CABLE HARNESS



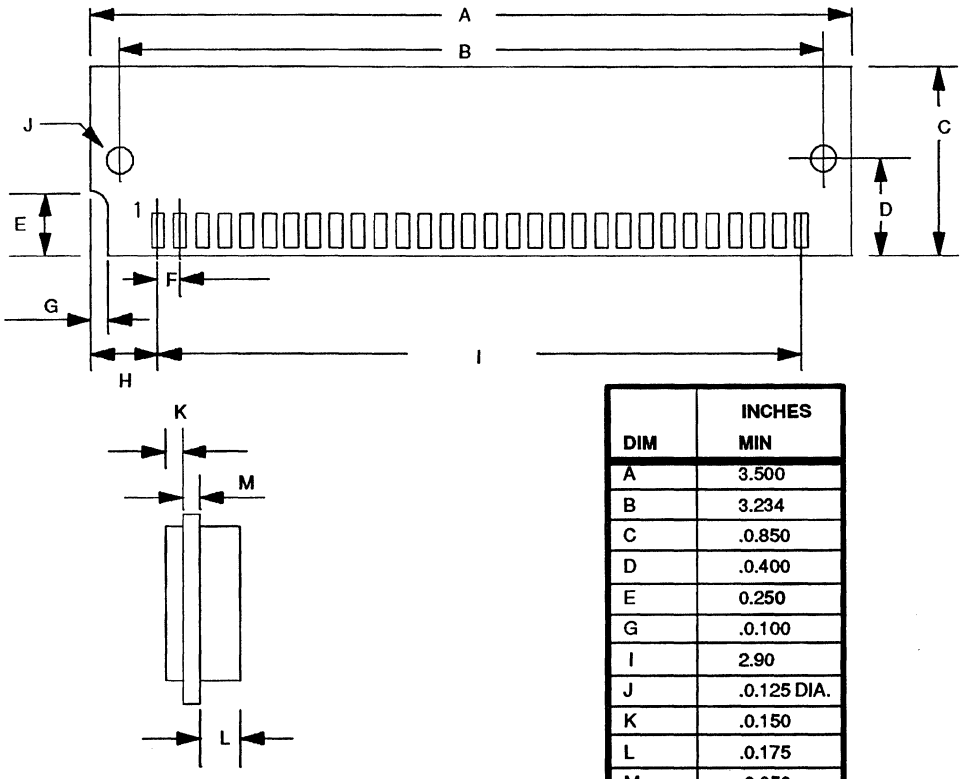
DIM.	INCHES	
	MIN.	MAX.
A	2.480	2.520
B	1.940	1.980
C	.260	.280
D	.160	.175
E	.395	.415
F	.195	.205
G	5.25	5.65
H	1.470	1.500
J	.715	.735
K	.090	.110
L	.590	.610

NOTES: COLOR STRIPE INDICATES PIN 1
END ON 28-PIN PULG.
DIMENSION L IS CENTER TO CENTER

DS9003
CARTRIDGE PROTO
BOARD



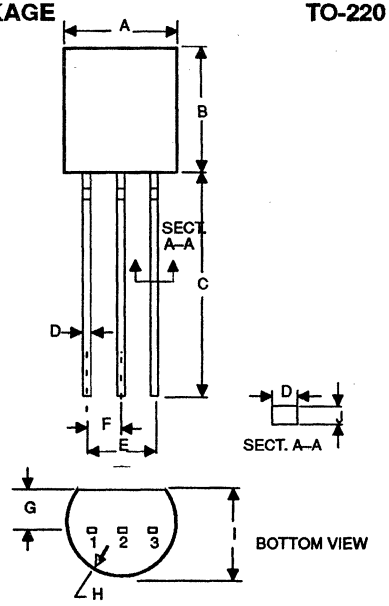
SIPSTIK (30-PIN)



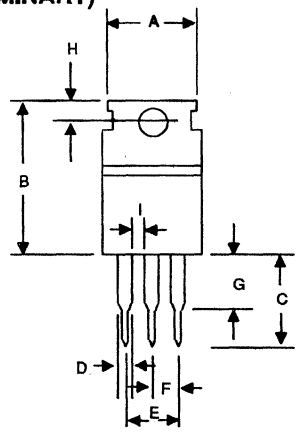
DIM	INCHES MIN
A	3.500
B	3.234
C	.0.850
D	.0.400
E	0.250
G	.0.100
I	2.90
J	.0.125 DIA.
K	.0.150
L	.0.175
M	.0.050

MECHANICAL DRAWINGS

TO-92 PACKAGE

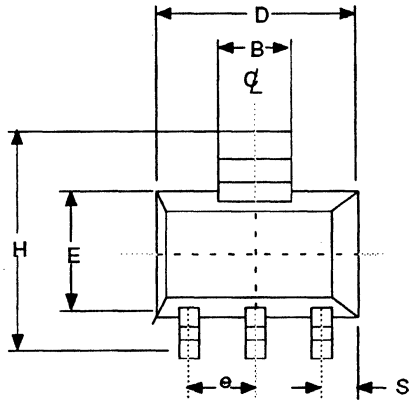


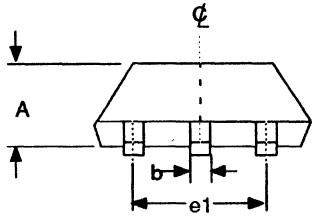
TO-220 PACKAGE (PRELIMINARY)

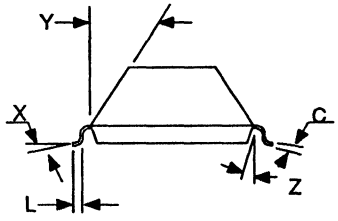


PKG	TO-92		TO-220	
DIM	MIN	MAX	MIN	MAX
A IN.	.175	.195	.380	.420
MM	4.45	4.96	9.66	10.66
B IN.	.170	.195	.560	.600
MM	4.32	4.96	14.23	14.99
C IN.	.500	.610	.510	.550
MM	12.70	15.49	12.95	13.97
D IN.	.016	.022	.045	.060
MM	.406	.559	1.14	1.52
E IN.	.095	.105	.190	.210
MM	2.41	2.67	4.83	5.33
F IN.	.045	.060	.090	.110
MM	1.14	1.52	2.29	5.33
G IN.	0.45	.060	.200	.280
MM	1.14	1.52	5.08	7.11
H IN	.085	.095	.100	.120
MM	2.16	2.41	2.54	3.04
I IN	.130	.155	.040	–
MM	3.30	3.94	1.01	–
J IN	.014	.020		
MM	.35	.51		

SOT–223 PACKAGE

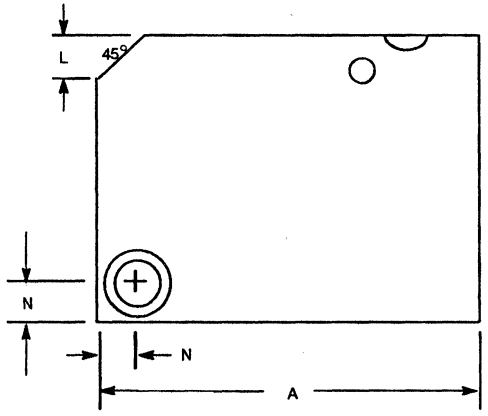




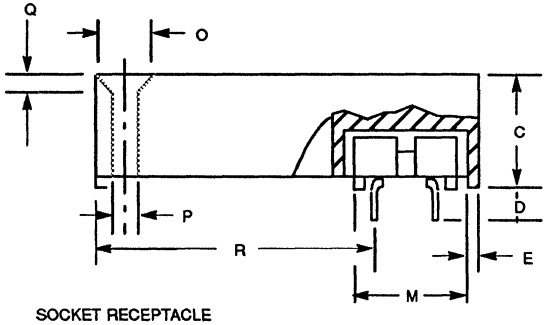


DIM	INCHES	
	MIN	MAX
A	–	.067
b	.025	.033
B	.116	.124
C	.009	.013
D	.248	.263
e	.0905 typ.	
e1	.181 typ.	
E	.130	.145
H	.264	.287
L	.016	.036
S	.033	.041
X	10° MAX	
Y	10°	20°
Z	10°	20°

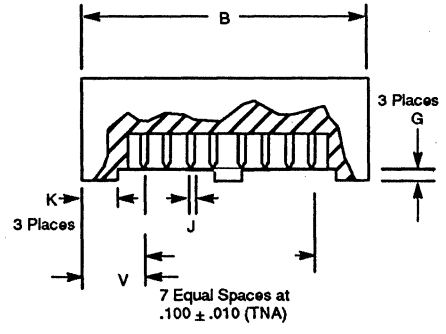
DS1260 SMART BATTERY



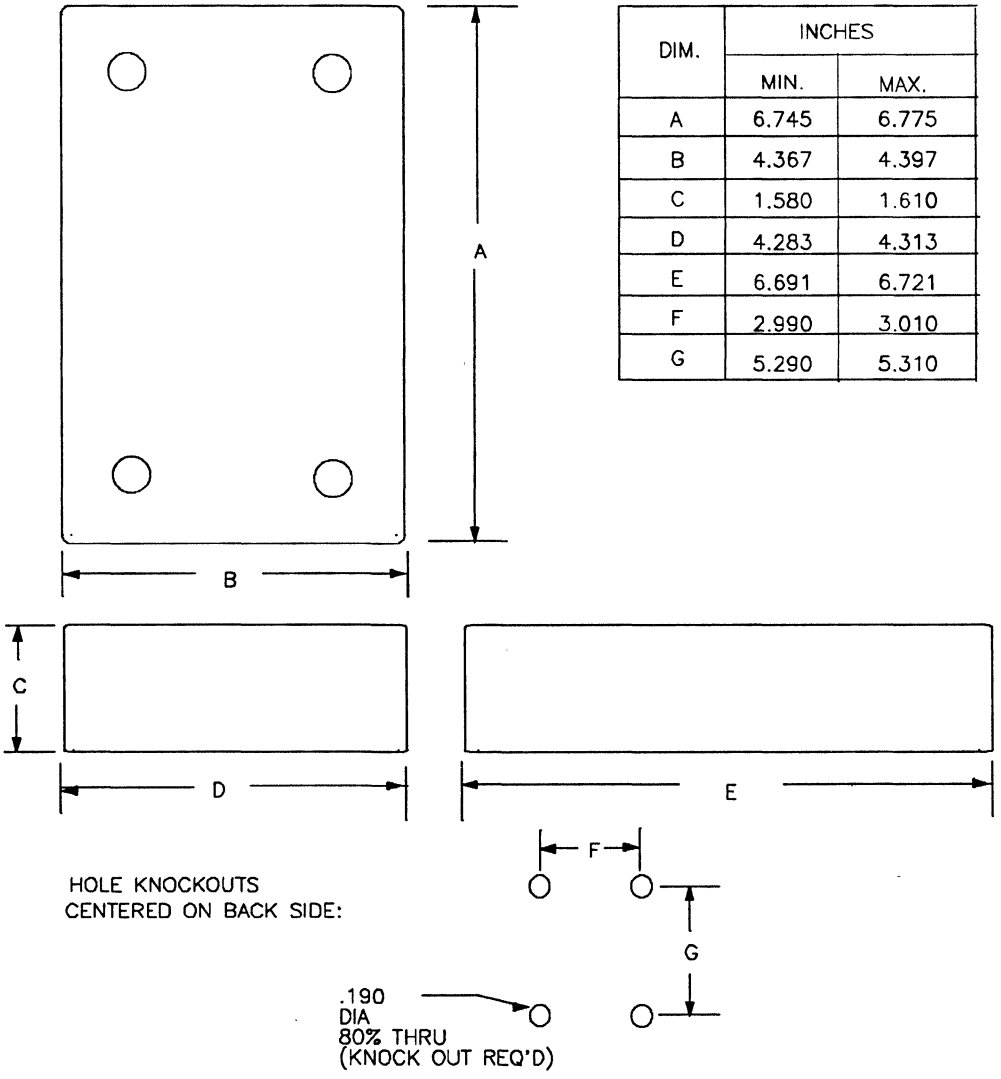
DIM	INCHES MIN	MAX
A	1.480	1.500
B	1.030	1.050
C	.390	.415
D	.120	.140
E	.020	.040
G	.020	.040
J	.022	.026
K	.090	.110
L	.240	.260
M	.420	.440
N	.165	.175
O	.800	.810
P	.160	.180
Q	.098	.109
R	.165	.175
S	.115	.125
T	.052	.058
U	.980	1.000
v	.055	.075



SOCKET RECEPTACLE
WILL ALLOW CONNECTION
WITH A STANDARD
16-DIP SOCKET.
BURDY DILB16P.-11T
SUPPLIED WITH EACH ORDER.



DS9005 EUROCARD ENCLOSURE

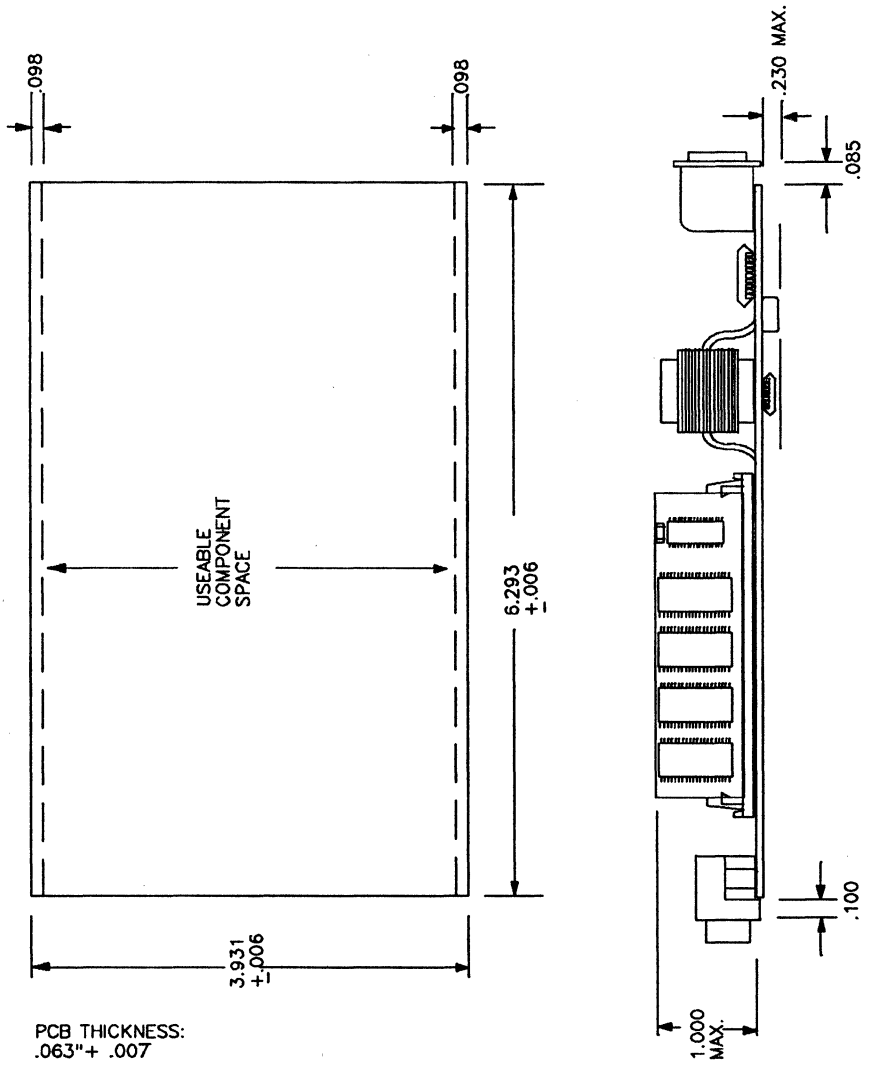


DIM.	INCHES	
	MIN.	MAX.
A	6.745	6.775
B	4.367	4.397
C	1.580	1.610
D	4.283	4.313
E	6.691	6.721
F	2.990	3.010
G	5.290	5.310

DS9006 SIP STIK™ MOTHERBOARD

ALL DIMENSIONS IN INCHES

TYPICAL LAYOUT FOR
DS9005 ENCLOSURE



PCB THICKNESS:
.063"+ .007

SUGGESTED CONNECTOR

PART NUMBERS:

RJ45– AMP #520252–4
9–PIN D–SUB FEMALE– AMP.#745781–1
DIN–64 POS. FEMALE AMP# 531796–2

DALLAS SEMICONDUCTOR

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Telephone: 214-450-0448
FAX: 214-450-0470