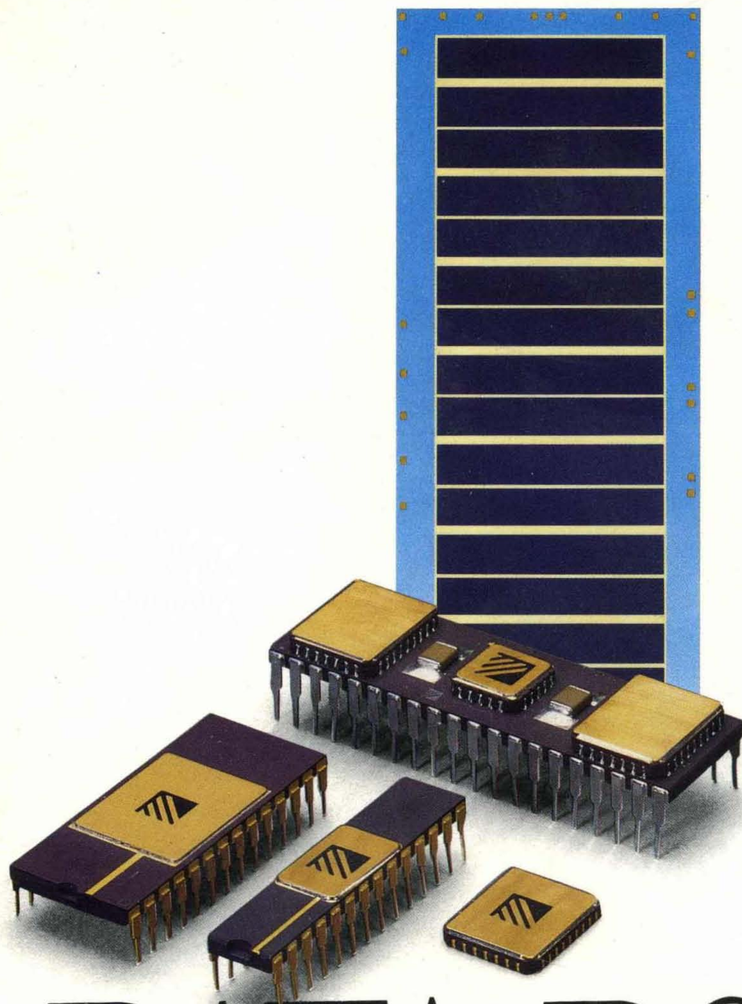
CMOS Static RAM



DATA BOOK

EDI

The future . . . today.

EDI

CMOS Static RAM DATA BOOK

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Additional copies of this Data Book, as well as other EDI literature, may be ordered from:

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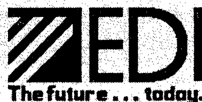

Thank you for taking the time to review our new CMOS Static RAM Data Book.

EDI is one of the top three suppliers of CMOS Static RAMs to the hi-rel market. We are very proud to say that we were the first manufacturer to ship high performance, MIL-STD-883 compliant 256Kx1 and 64Kx4 SRAMs in production volume in 1988. We are also the leading supplier of 8Kx8 and 32Kx8 Static RAMs to the military market.

Our strategy is to continue to be first to market with leading edge, high density, high performance CMOS Static RAMs for the industry's most demanding applications in the future. We plan to be among the first with megabit density MIL-STD-883 monolithic SRAMs, beginning with the 128Kx8 in 1989, followed closely with 256Kx4 and 1Megx1 organizations in 1990.

We are committed to the hi-rel market and are continuing to invest significant resources to maintain the high quality standards mandated by our customers.

You will find EDI able to support your most stringent performance requirements. We have a knowledgable and energetic support staff of sales, marketing, customer service, and engineering people ready to handle any questions.

I hope you will consider EDI for your high performance, low power CMOS Static RAM needs.

Sincerely,

Hans Olsen,
President

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256K	32Kx8	EDI8833C35/45CB/LB/QB	28
288K	32Kx9	EDI8932C45/55CB/LB	29
1M	1Mx1	EDI811024C35/45/55/70TB	30
1M	256Kx4	EDI84256C35/45/55/70TB	31
1M	128Kx8	EDI88130C55/70/90/100CB	32

  Preliminary/Final Data

Density	Org	Part No.	Page
64K	8Kx8	EDI8808CA35/45/55/70CB/LB/QB	33-38
72K	8Kx9	EDI8908C35/45/55L28B/QB	39-44
256K	256Kx1	EDI81256C/P35/45/55LB/QB	45-50
256K	64Kx4	EDI8464C/P35/45/55LB	51-56
256K	64Kx4	EDI8465C/P35/45/55QB	57-62
256K	32Kx8	EDI8832C/P55/70/85/100/120/150CB/LB/QB	63-68

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Advance Information

Density	Org	Part No.	Page
1M	256Kx4	EDI8M4257C35/45/55/70CB/CC	70
2M	512Kx4	EDI8M4512C45/55/70/CB/CC	71
2M	256Kx8	EDI8M8257C90/100/120/150CB/CC	72
4M	512Kx8	EDI8M8512C90/100/120/150CB/CC	73
4M	256Kx16	EDI8M16256C35/45/55/70CB/CC	74

Preliminary/Final Data

Density	Org	Part No.	Page
256K	16Kx16	EDH816H16C-25/35/45CC-Z/CMHR-Z	75-79
512K	64Kx8	EDI8M864C50/60/70/80CB/CC	80-85
512K	64Kx8	EDI8M864C90/100/120/150CB/CC	86-91
1M	128Kx8	EDI8M8128C50/60/70/80CB/CC	92-97
1M	128Kx8	EDI8M8128C/P90/100/120/150CB/CC	98-103
1M	128Kx8	EDI8M8128C100/120/150PC	104-108
1M	128Kx8	EDI8M8130C50/60/70/80CB/CC	109-114
1M	128Kx8	EDI8M8130C/P90/100/120/150CB/CC	115-120
1M	64Kx16	EDH816H64C-35/45/55/70CC/CMHR	121-126
1M	64Kx16	EDI8F1664C100/120/150PC	127-131
1M	64Kx16	EDI8M1664C50/60/70/85/100CB/CC	132-137
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Established CMOS SRAM Leader

In an industry where the primary objective of the major semiconductor manufacturers is high volume production of devices for the vast commercial market, Electronoic Designs Incorporated has focused on the needs of the specialized, high-reliability and military equipment manufacturers.

Through its expertise in value-added design and manufacturing techniques, EDI has time and again proved itself to be the first to market with CMOS Static RAMs providing the highest level in advanced techology for the most demanding high-performance applications.

EDI's current volume parts employ 1.2µ design rules. Recently introduced high speed monolithic 256Kx1 and 64Kx4 devices feature 1.0µ technology. And, a 128Kx8 monolithic, scheduled for introduction late in 1989, will be EDI's first submicron product, featuring 0.8µ geometries.

Since the introduction of its first monolithic CMOS Static RAM products in 1986, EDI has become the leading supplier of bytewide (8Kx8 and 32Kx8) devices for Military applications. The acceptance of these products in the Military marketplace is continuing to fuel exceptional growth for the Company.

DESC Listed

EDI is listed on the Defense Electronics Supply Center (DESC) Standard Military Drawings for microcircuits as an approved source for its 64K density (8Kx8 and 8Kx9) and its complete family of high performance, high speed 256K density (32Kx8, 64Kx4 and 256Kx1) devices.

Not only has EDI been first to market with the latest technology, the company has consistently been first to offer these devices in advanced packaging configurations including surface mount packages which are also used in its megabit density modules.

SRAM Modules

The Company's first SRAM Module, the EDH8808C introduced in 1983, was also the industry's first Military 64K density Static RAM. In 1985 the Company made the decision to focus its product line on high-performance and high-reliability Static RAMs.

In addition to proprietary designs with unique performance characteristics, modules provide today's designers with pin for pin compatibility to the next generation of monolithic technology. The megabit density 128Kx8 Static RAM module (EDI8M8128C), available since 1986, is a market leader.

EDI develops modules from the products in their monolithic product line to provide the same high performance characteristics, in megabit densities. The most recent addition to this line is a 64Kx16 CMOS Static RAM device in a 40 pin package with the same pinout and footprint as the future monolithic device.

Capabilities

EDI is able to be first to provide leading edge technology through its exclusive strategic partnerships and licensing agreements with the industry's leading semiconductor foundries, worldwide. EDI's value-added design approach adapts state-of-the-art technology to product development and manufacturing which employ a combination of stringent processing, advanced packaging techniques, and exhaustive testing, both environmental and electrical.

EDI's applications and service orientation comes naturally from its roots in the computer industry in the high technology region of Massachusetts. EDI's headquarters facility is located in Hopkinton, Massachusetts, near the starting line of the world famous Boston Marathon, just 26 miles west of Boston. The headquarters facility houses R&D, Engineering, Module Assembly, Final Test, Administration, and Sales & Marketing.

New Products

Many new products scheduled for introduction at press time are included in the Advance Data pages of this Data Book. These products include three megabit density monolithics and modules with densities to 4 megabits, all offering exceptional performance characteristics.

Surface Mount Pioneer

Surface mount devices (SMD) allow the designer to take full advantage of the low power feature of CMOS and to obtain the greatest board space savings. Most integrated circuits, however are still packaged in the traditional dual-in-line package (DIP) configuration and there is a large manufacturing support industry to handle thru-hole board assembly.

High Density Modules

EDI was the first manufacturer to provide memory products incorporating surface mount technology for exceptional space savings into a finished device for use in standard through-hole manufacturing applications.These products are comprised of a multi-layered substrate (either co-fired ceramic or glass filled epoxy FR-4) with dual-in-line (DIP) or single-in-line (SIP) pin configurations.

As a surface mount pioneer in the early 1980's, EDI encountered many of the technical issues now facing the military/hi-rel market place. These issues included solving the coefficient of thermal expansion (CTE) mismatch, shear stress, and thermal management problems.

In addressing the CTE problem, EDI performed a comprehensive evaluation of board materials and surface mount packages. The results of this extensive research and development led EDI to select CTE matched leadless ceramic chip carriers with ceramic motherboards to manufacture the industry's first high density memory modules for military applications. An advanced infrared reflow surface mount technology was developed after extensive evaluation proved infra-red reflow to be the most efficient method of heat transfer to produce reliable solder connections.

The result of the combining of high-speed and high-performance monolithic integrated circuits are products providing high performance with exceptionally high density. EDI modules provide customers the density advantages of surface mount technology with the convenience of standard manufacturing techniques.

New Monolithic Packaging

As EDI entered the monolithic marketplace, it recognized an opportunity to bring its surface mount experience to the aid of the military and hi-rel system houses. Shear stresses reaching thousands of pounds per square inch (psi) can build up inside of a surface mount solder joint during thermal cycling due to differences in the CTE of the board material and the package, and out-of-plane warping, causing solder joint failures.

EDI has recently introduced two new surface mount package options to manage the CTE and shear stress problems facing military system designers; leaded ceramic chip carriers and flatpacks. These packages provide the advantages of lead compliancy, shear stress relief, and solder joint inspection capability.

EDI provides its customers with the highest performance and highest density military Static RAMs available in the marketplace, in the most desirable package configurations.

Quality Assurance Policy

The Quality Standard at Electronic Designs Incorporated (EDI) is defect free work. No other standard is acceptable.

This policy is reflected in the attention given to the design, manufacture, and test of all of our products. All procedures are designed to meet or exceed the requirements of our customers, and the strict requirements and procedures dictated by Military Standards.

Maintaining the highest standards of quality demands a continous committment from each individual, throughout the company. EDI conducts a comprehensive training program for all employees which stresses the importance of each individual to the final objective of satisfied customers through defect free products and workmanship.

EDI's operating procedures have been developed to establish and maintain a single standard of manufacturing methodology. The Quality system has been designed to be in compliance with:

1. MIL-M 38510 General Specifications for Microcircuits
2. MIL-STD 45662 Calibration System Requirements
3. MIL-Q-9858 Quality Program Requirements
4. MIL-STD-883

MIL-STD-883C Compliance

EDI's hermetic Military grade monolithic CMOS SRAMs are in full compliance with the product flow and test procedures of paragraph 1.2.1 of MIL-STD-883.

The products are processed to the standardized screening flow, Method 5004 of MIL-STD-883C. Periodic inspections, per Method 5005 of MIL-STD-883C are performed to ensure adequate screening. The purpose of Methods 5004 and 5005 is given below.

1. Screen infant mortality.
2. Produce highly reliable product.

In addition, EDI performs extended life tests on all released products. Devices are tested at +125°C for 1000 hours. Failures are rigorously analyzed to identify failure mechanisms. Finally, corrective actions are implemented to preclude failure recurrence. This closed loop system ensures that reliability is "designed in" rather than "tested in."

With this information, EDI can:

1. Predict failure rates
2. Assess impact of design, process or material change.
3. Determine useful product life.

EDI DESC-SMD Program

EDI is a leading supplier of hi-rel (military), high-performance CMOS Static RAMs and high density CMOS Static RAM modular subsystems products which complement each other to provide high speed CMOS solutions for a wide range of military applications and systems. The product line includes devices which are fully compliant to the latest revision of MIL-STD-883.

EDI is actively involved with the Defense Electronic Supply Center (DESC) in their Standard Military Drawing (SMD) program. The SMD program allows standardization fo militarized products and reduction of the proliferation of non-standard source control drawings. Products listed on DESC Drawings at the time of printing this book are listed below. Users should contact either EDI or DESC for current status of products in the SMD program.

DESC Standard Military Drawing Program

Description	Drawing No.
8Kx8	5962-85525
8Kx9, Low Power*	5962-88683
32Kx8	5962-88662
32Kx8, Low Power	5962-88552
64Kx4	5962-88681
64Kx4, Low Power	5962-88545
256Kx1	5962-88725
256Kx1, Low Power	5962-88544

*Listing Approval Pending at Press time

EDI CMOS Static RAM Selector Guide

Monolithic, Advance Information

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
			Max Current Consum			Packaging Information				

256K Density

32Kx8

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8833C35CB	35	MIL	95	1.5	600	8	DIP	28	1.49x.620x.232	28
EDI8833C45CB	45	MIL	95	1.5	600	8	DIP	28	1.49x.620x.232	28
EDI8833C35LB	35	MIL	95	1.5	600	12	LCC	32	.560x.458x.120	28
EDI8833C45LB	45	MIL	95	1.5	600	12	LCC	32	.560x.458x.120	28
EDI8833C35QB	35	MIL	95	1.5	600	2	DIP	28	1.49x.320x.200	28
EDI8833C45QB	45	MIL	95	1.5	600	2	DIP	28	1.49x.320x.200	28

32Kx9

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8932C45CB	45	MIL	TBD	TBD	TBD	8	DIP	28	1.49x.620x.232	29
EDI8932C55CB	55	MIL	TBD	TBD	TBD	8	DIP	28	1.49x.620x.232	29
EDI8932C45LB	45	MIL	TBD	TBD	TBD	12	LCC	32	.560x.458x.120	29
EDI8932C55LB	55	MIL	TBD	TBD	TBD	12	LCC	32	.560x.458x.120	29

1 Megabit Density

1Mx1

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI811024C35TB	35	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	30
EDI811024C45TB	45	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	30
EDI811024C55TB	55	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	30
EDI811024C70TB	70	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	30

256Kx4

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI84256C35TB	35	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	31
EDI84256C45TB	45	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	31
EDI84256C55TB	55	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	31
EDI84256C70TB	70	MIL	140	5	TBD	101	DIP	28	1.40x.400x.180	31

128Kx8

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI88130C55CB	55	MIL	120	1	TBD	9	DIP	32	1.60x.600x.180	32
EDI88130C70CB	70	MIL	120	1	TBD	9	DIP	32	1.60x.600x.180	32
EDI88130C90CB	90	MIL	120	1	TBD	9	DIP	32	1.60x.600x.180	32
EDI88130C100CB	100	MIL	120	1	TBD	9	DIP	32	1.60x.600x.180	32
EDI88130C55LB	55	MIL	120	1	TBD	100	LCC	32	.800x.450x.090	32
EDI88130C70LB	70	MIL	120	1	TBD	100	LCC	32	.800x.450x.090	32
EDI88130C90LB	90	MIL	120	1	TBD	100	LCC	32	.800x.450x.090	32
EDI88130C100LB	100	MIL	120	1	TBD	100	LCC	32	.800x.450x.090	32

Monolithic

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Packaging Information Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
64K Density										
8Kx8, High Speed										
EDI8808CA35DB	35	MIL	140	1	200	70	CERDIP	28	1.49x.620x.232	33-38
EDI8808CA45DB	45	MIL	140	1	200	70	CERDIP	28	1.49x.620x.232	33-38
EDI8808CA55DB	55	MIL	140	1	200	70	CERDIP	28	1.49x.620x.232	33-38
EDI8808CA70DB	70	MIL	140	1	200	70	CERDIP	28	1.49x.620x.232	33-38
EDI8808CA35LB	35	MIL	140	1	200	12	LCC	32	.560x.458x.120	33-38
EDI8808CA45LB	45	MIL	140	1	200	12	LCC	32	.560x.458x.120	33-38
EDI8808CA55LB	55	MIL	140	1	200	12	LCC	32	.560x.458x.120	33-38
EDI8808CA70LB	70	MIL	140	1	200	12	LCC	32	.560x.458x.120	33-38
EDI8808CA35QB	35	MIL	140	1	200	2	DIP	28	1.49x.320x.200	33-38
EDI8808CA45QB	45	MIL	140	1	200	2	DIP	28	1.49x.320x.200	33-38
EDI8808CA55QB	55	MIL	140	1	200	2	DIP	28	1.49x.320x.200	33-38
EDI8808CA70QB	70	MIL	140	1	200	2	DIP	28	1.49x.320x.200	33-38
8KX9										
EDI8908C35L28B	35	MIL	140	1	200	14	LCC	28	.560x.358x.120	39-44
EDI8908C45L28B	45	MIL	140	1	200	14	LCC	28	.560x.358x.120	39-44
EDI8908C55L28B	55	MIL	140	1	200	14	LCC	28	.560x.358x.120	39-44
EDI8908C35QB	35	MIL	140	1	200	2	DIP	28	1.49x.320x.200	39-44
EDI8908C45QB	45	MIL	140	1	200	2	DIP	28	1.49x.320x.200	39-44
EDI8908C55QB	55	MIL	140	1	200	2	DIP	28	1.49x.320x.200	39-44

EDI CMOS Static RAM Selector Guide
Monolithic, Preliminary/Final Data

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Packaging Information Type	Pins	Dimensions LxWxH (in)	Page
256K Density										
256Kx1										
EDI81256C35LB	35	MIL	120	10	—	14	LCC	28	.560x.358x.120	45-50
EDI81256C45LB	45	MIL	120	10	—	14	LCC	28	.560x.358x.120	45-50
EDI81256C55LB	55	MIL	120	10	—	14	LCC	28	.560x.358x.120	45-50
EDI81256C35QB	35	MIL	120	10	—	3	DIP	24	1.28x.320x.200	45-50
EDI81256C45QB	45	MIL	120	10	—	3	DIP	24	1.28x.320x.200	45-50
EDI81256C55QB	55	MIL	120	10	—	3	DIP	24	1.28x.320x.200	45-50
256Kx1, Low Power										
EDI81256P35LB	35	MIL	120	3	500	14	LCC	28	.560x.358x.120	45-50
EDI81256P45LB	45	MIL	120	3	500	14	LCC	28	.560x.358x.120	45-50
EDI81256P55LB	55	MIL	120	3	500	14	LCC	28	.560x.358x.120	45-50
EDI81256P35QB	35	MIL	120	3	500	3	DIP	24	1.28x.320x.200	45-50
EDI81256P45QB	45	MIL	120	3	500	3	DIP	24	1.28x.320x.200	45-50
EDI81256P55QB	55	MIL	120	3	500	3	DIP	24	1.28x.320x.200	45-50
64Kx4										
EDI8464C35LB	35	MIL	120	10	—	14	LCC	28	.560x.358x.120	51-56
EDI8464C45LB	45	MIL	120	10	—	14	LCC	28	.560x.358x.120	51-56
EDI8464C55LB	55	MIL	120	10	—	14	LCC	28	.560x.358x.120	51-56
EDI8465C35QB	35	MIL	120	10	—	3	DIP	24	1.28x.320x.200	57-62
EDI8465C45QB	45	MIL	120	10	—	3	DIP	24	1.28x.320x.200	57-62
EDI8465C55QB	55	MIL	120	10	—	3	DIP	24	1.28x.320x.200	57-62
64Kx4, Low Power										
EDI8464P35LB	35	MIL	120	3	500	14	LCC	28	.560x.358x.120	51-56
EDI8464P45LB	45	MIL	120	3	500	14	LCC	28	.560x.358x.120	51-56
EDI8464P55LB	55	MIL	120	3	500	14	LCC	28	.560x.358x.120	51-56
EDI8465P35QB	35	MIL	120	3	500	3	DIP	24	1.28x.320x.200	57-62
EDI8465P45QB	45	MIL	120	3	500	3	DIP	24	1.28x.320x.200	57-62
EDI8465P55QB	55	MIL	120	3	500	3	DIP	24	1.28x.320x.200	57-62

Monolithic

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Packaging Information Type	Pins	Dimensions LxWxH (in)	Page
256K Density, Continued										
32KX8										
EDI8832C55CB	55	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C70CB	70	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C85CB	85	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C100CB	100	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C120CB	120	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C150CB	150	MIL	95	1	—	8	DIP	28	1.49x.620x.232	63-68
EDI8832C55LB	55	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C70LB	70	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C85LB	85	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C100LB	100	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C120LB	120	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C150LB	150	MIL	95	1	—	12	LCC	32	.560x.458x.120	63-68
EDI8832C55QB	55	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
EDI8832C70QB	70	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
EDI8832C85QB	85	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
EDI8832C100QB	100	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
EDI8832C120QB	120	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
EDI8832C150QB	150	MIL	95	1	—	2	DIP	28	1.49x.320x.200	63-68
32KX8, Low Power										
EDI8832P55CB	55	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P70CB	70	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P85CB	85	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P100CB	100	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P120CB	120	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P150CB	150	MIL	95	1	500	8	DIP	28	1.49x.620x.232	63-68
EDI8832P55LB	55	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P70LB	70	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P85LB	85	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P100LB	100	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P120LB	120	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P150LB	150	MIL	95	1	500	12	LCC	32	.560x.458x.120	63-68
EDI8832P55QB	55	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68
EDI8832P70QB	70	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68
EDI8832P85QB	85	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68
EDI8832P100QB	100	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68
EDI8832P120QB	120	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68
EDI8832P150QB	150	MIL	95	1	500	2	DIP	28	1.49x.320x.200	63-68

EDI CMOS Static RAM Selector Guide

Modules, Advance Information

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Packaging Information Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
1 Megabit Density										
256Kx4										
EDI8M4257C35TB	35	MIL	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C45TB	45	MIL	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C55TB	55	MIL	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C70TB	70	MIL	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C35TC	35	COM	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C45TC	45	COM	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C55TC	55	COM	480	40	--	104	DIP	28	1.40x.435x.275	70
EDI8M4257C70TC	70	COM	480	40	--	104	DIP	28	1.40x.435x.275	70
2 Megabits Density										
512Kx4										
EDI8M4512C45CB	45	MIL	150	50	--	103	DIP	32	1.60x.600x.275	71
EDI8M4512C55CB	55	MIL	150	50	--	103	DIP	32	1.60x.600x.275	71
EDI8M4512C70CB	70	MIL	150	50	--	103	DIP	32	1.60x.600x.275	71
EDI8M4512C45CC	45	COM	150	50	--	103	DIP	32	1.60x.600x.275	71
EDI8M4512C55CC	55	COM	150	50	--	103	DIP	32	1.60x.600x.275	71
EDI8M4512C70CC	70	COM	150	50	--	103	DIP	32	1.60x.600x.275	71
256Kx8										
EDI8M8257C90CB	90	MIL	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C100CB	100	MIL	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C120CB	120	MIL	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C150CB	150	MIL	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C90CC	90	COM	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C100CC	100	COM	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C120CC	120	COM	120	5	TBD	105	DIP	32	1.60x.600x.230	72
EDI8M8257C150CC	150	COM	120	5	TBD	105	DIP	32	1.60x.600x.230	72

Modules, Advance Information

4 Megabits Density

512Kx8

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Packaging Information Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8M8512C90CB	90	MIL	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C100CB	100	MIL	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C120CB	120	MIL	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C150CB	150	MIL	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C90CC	90	COM	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C100CC	100	COM	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C120CC	120	COM	120	10	TBD	106	DIP	32	1.60x.600x.275	73
EDI8M8512C150CC	150	COM	120	10	TBD	106	DIP	32	1.60x.600x.275	73
256Kx16										
EDI8M16256C35CB	35	MIL	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C45CB	45	MIL	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C55CB	55	MIL	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C70CB	70	MIL	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C35CC	35	COM	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C45CC	45	COM	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C55CC	55	COM	2112	175	--	109	DIP	48	2.37x.900x.300	74
EDI8M16256C70CC	70	COM	2112	175	--	109	DIP	48	2.37x.900x.300	74

EDI CMOS Static RAM Selector Guide

Modules

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Packaging Information Type	Pins	Dimensions LxWxH (in)	Page
256K Density										
16Kx16										
EDH816H16C-25CC-Z	25	COM	440	65	--	19	DIP	36	1.80x.292x.500	75-79
EDH816H16C-35CC-Z	35	COM	440	65	--	19	DIP	36	1.80x.292x.500	75-79
EDH816H16C-45CC-Z	45	COM	440	65	--	19	DIP	36	1.80x.292x.500	75-79
EDH816H16C-25CMHR-Z	25	MIL	440	65	--	19	DIP	36	1.80x.292x.500	75-79
EDH816H16C-35CMHR-Z	35	MIL	440	65	--	19	DIP	36	1.80x.292x.500	75-79
EDH816H16C-45CMHR-Z	45	MIL	440	65	--	19	DIP	36	1.80x.292x.500	75-79
512K Density										
64Kx8										
EDI8M864C50CB	50	MIL	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C60CB	60	MIL	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C70CB	70	MIL	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C80CB	80	MIL	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C90CB	90	MIL	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C100CB	100	MIL	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C120CB	120	MIL	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C150CB	150	MIL	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C50CC	50	COM	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C60CC	60	COM	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C70CC	70	COM	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C80CC	80	COM	120	5	1200	50	DIP	32	1.60x.600x.230	80-85
EDI8M864C90CC	90	COM	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C100CC	100	COM	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C120CC	120	COM	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91
EDI8M864C150CC	150	COM	95	1.5	750	50	DIP	32	1.60x.600x.230	86-91

Modules

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Packaging Information Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page

1 Megabit Density

128Kx8

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8M8128C50CB	50	MIL	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C60CB	60	MIL	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C70CB	70	MIL	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C80CB	80	MIL	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C90CB	90	MIL	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C100CB	100	MIL	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C120CB	120	MIL	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C150CB	150	MIL	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C50CC	50	COM	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C60CC	60	COM	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C70CC	70	COM	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C80CC	80	COM	120	10	--	51	DIP	32	1.60x.600x.275	92-97
EDI8M8128C90CC	90	COM	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C100CC	100	COM	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C120CC	120	COM	95	3	--	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128C150CC	150	COM	95	3	--	51	DIP	32	1.60x.600x.275	98-103

128Kx8 Plastic SOP/ Ceramic Package

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8M8128C100PC	100	COM	95	3	--	108	DIP	32	1.60x.600x.350	104-108
EDI8M8128C120PC	120	COM	95	3	--	108	DIP	32	1.60x.600x.350	104-108
EDI8M8128C150PC	150	COM	95	3	--	108	DIP	32	1.60x.600x.350	104-108

128Kx8, Low Power

EDI Part Number	Speed ns	Temp Range	ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
EDI8M8128P90CB	90	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128P100CB	100	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128P120CB	120	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	98-103
EDI8M8128P150CB	150	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	98-103

Modules

1 Megabit Density, Continued

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Dwg. No.	Packaging Information Type	Pins	Dimensions LxWxH (in)	Page
128Kx8, Dual Chip Enable										
EDI8M8130C50CB	50	MIL	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C60CB	60	MIL	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C70CB	70	MIL	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C80CB	80	MIL	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C90CB	90	MIL	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C100CB	100	MIL	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C120CB	120	MIL	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C150CB	150	MIL	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C50CC	50	COM	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C60CC	60	COM	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C70CC	70	COM	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C80CC	80	COM	125	10	--	51	DIP	32	1.60x.600x.275	109-114
EDI8M8130C90CC	90	COM	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C100CC	100	COM	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C120CC	120	COM	95	3	--	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130C150CC	150	COM	95	3	--	51	DIP	32	1.60x.600x.275	115-120
128Kx8, Dual Chip Enable, Low Power										
EDI8M8130P90CB	90	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130P100CB	100	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130P120CB	120	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	115-120
EDI8M8130P150CB	150	MIL	95	0.9	500	51	DIP	32	1.60x.600x.275	115-120

Modules

EDI Part Number	Speed ns	Temp Range	Max Current Consum ICC1 mA	ICC3 mA	IDR µA	Packaging Information Dwg. No.	Type	Pins	Dimensions LxWxH (in)	Page
1 Megabit Density, Continued										
64Kx16, High Speed, Programmable										
EDH816H64C-35CC	35	COM	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-45CC	45	COM	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-55CC	55	COM	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-70CC	70	COM	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-35CMHR	35	MIL	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-45CMHR	45	MIL	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-55CMHR	55	MIL	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
EDH816H64C-70CMHR	70	MIL	1380	250	--	31	DIP	40	2.20x.900x.270	121-126
64Kx16, JEDEC Pinout, Plastic/FR4 Package										
EDI8F1664C100PC	100	COM	195	3	--	111	DIP	40	2.00x.700x.275	127-131
EDI8F1664C120PC	120	COM	195	3	--	111	DIP	40	2.00x.700x.275	127-131
EDI8F1664C150PC	150	COM	195	3	--	111	DIP	40	2.00x.700x.275	127-131
64Kx16, JEDEC Pinout										
EDI8M1664C50CB	50	MIL	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C60CB	60	MIL	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C70CB	70	MIL	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C85CB	85	MIL	195	3	1500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C100CB	100	MIL	195	3	1500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C50CC	50	COM	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C60CC	60	COM	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C70CC	70	COM	240	3	2500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C85CC	85	COM	195	3	1500	66	DIP	40	2.00x.600x.275	132-137
EDI8M1664C100CC	100	COM	195	3	1500	66	DIP	40	2.00x.600x.275	132-137
2 Megabits Density										
256Kx8										
EDI8M8256C70PC	70	COM	100	20	--	107	DIP	32	1.66x.660x.265	138-142
EDI8M8256C100PC	100	COM	100	20	--	107	DIP	32	1.66x.660x.265	138-142
EDI8M8256C120PC	120	COM	100	20	--	107	DIP	32	1.66x.660x.265	138-142

8Kx8

AMD	EDI
AM99C88-70DMB	EDI8808CA70DB
AM99C88-70LMB	EDI8808CA70LB
CYPRESS	**EDI**
CY7C185-35DMB	EDI8808CA35QB
CY7C185-45DMB	EDI8808CA45QB
CY7C185-55DMB	EDI8808CA55QB
CY7C185-35LMB	EDI8808CA35LB
CY7C185-45LMB	EDI8808CA45LB
CY7C185-55LMB	EDI8808CA55LB
CY7C186-35DMB	EDI8808CA35DB
CY7C186-45DMB	EDI8808CA45DB
CY7C186-55DMB	EDI8808CA55DB
IDT	**EDI**
IDT7164S35DB	EDI8808CA35DB
IDT7164S45DB	EDI8808CA45DB
IDT7164S55DB	EDI8808CA55DB
IDT7164S70DB	EDI8808CA70DB
IDT7164S35TCB	EDI8808CA35QB
IDT7164S45TCB	EDI8808CA45QB
IDT7164S55TCB	EDI8808CA55QB
IDT7164S70TCB	EDI8808CA70QB
IDT7164S35L32B	EDI8808CA35LB
IDT7164S45L32B	EDI8808CA45LB
IDT7164S55L32B	EDI8808CA55LB
IDT7164S70L32B	EDI8808CA70LB
MICRON	**EDI**
MT5C6408-35	EDI8808CA35QB
MT5C6408-45	EDI8808CA45QB
MT5C6408CW-35	EDI8808CA35DB
MT5C6408CW-45	EDI8808CA45DB
MT5C6408EC-35	EDI8808CA35LB
MT5C6408EC-45	EDI8808CA45LB

8Kx9

PERFORMANCE	EDI
P4C163-35CMB	EDI8908C35CB
P4C163-45CMB	EDI8908C45CB
P4C163-55CMB	EDI8908C55CB
P4C163-35LMB	EDI8908C35LB
P4C163-45LMB	EDI8908C45LB
P4C163-55LMB	EDI8908C55LB

256Kx1

CYPRESS	EDI
CY7C197-35DMB	EDI81256C35QB
CY7C197-45DMB	EDI81256C45QB
CY7C197-55DMB	EDI81256C55QB
CY7C197-35LMB	EDI81256C35LB
CY7C197-45LMB	EDI81256C45LB
CY7C197-55LMB	EDI81256C55LB
IDT	**EDI**
IDT71257S35CB	EDI81256C35QB
IDT71257S45CB	EDI81256C45QB
IDT71257S55CB	EDI81256C55QB
IDT71257S70CB	EDI81256C70QB
IDT71257L35CB	EDI81256P35QB
IDT71257L45CB	EDI81256P45QB
IDT71257L55CB	EDI81256P55QB
MICRON	**EDI**
MT5C2561C-35	EDI81256C35QB
MT5C2561C-45	EDI81256C45QB
MT5C2561C-55	EDI81256C55QB
MT5C2561EC-35	EDI81256C35LB
MT5C2561EC-45	EDI81256C45LB
MT5C2561EC-55	EDI81256C55LB
PERFORMANCE	**EDI**
P4C1257-35CMB	EDI81256C35QB
P4C1257-45CMB	EDI81256C45QB
P4C1257-55CMB	EDI81256C55QB
P4C1257-35LMB	EDI81256C35LB
P4C1257-45LMB	EDI81256C45LB
P4C1257-55LMB	EDI81256C55LB

64Kx4

CYPRESS	EDI
CY7C194-35DMB	EDI8465C35QB
CY7C194-45DMB	EDI8465C45QB
CY7C194-55DMB	EDI8465C55QB
CY7C194-35LMB	EDI8464C35LB
CY7C194-45LMB	EDI8464C45LB
CY7C194-55LMB	EDI8464C55LB
IDT	**EDI**
IDT71258S35CB	EDI8465C35QB
IDT71258S45CB	EDI8465C45QB
IDT71258S55CB	EDI8465C55QB
IDT71258L35CB	EDI8465P35QB
IDT71258L45CB	EDI8465P45QB
IDT71258L55CB	EDI8465P55QB

64Kx4 Con't..

MICRON	EDI
MT5C2564C-35	EDI8465C35QB
MT5C2564C-45	EDI8465C45QB
MT5C2564C-55	EDI8465C55QB
MT5C2564EC-35	EDI8464C35LB
MT5C2564EC-45	EDI8464C45LB
MT5C2564EC-55	EDI8464C55LB

PERFORMANCE	EDI
P4C1258-35CMB	EDI8465C35QB
P4C1258-45CMB	EDI8465C45QB
P4C1258-55CMB	EDI8465C55QB
P4C1258-35LMB	EDI8464C35LB
P4C1258-45LMB	EDI8464C45LB
P4C1258-55LMB	EDI8464C55LB

32Kx8

CYPRESS	EDI
CY7C198-35DMB	EDI8833C35CB
CY7C198-45DMB	EDI8833C45CB
CY7C198-55DMB	EDI8832C55CB
CY7C199-35DMB	EDI8833C35QB
CY7C199-45DMB	EDI8833C45QB
CY7C199-55DMB	EDI8832C55QB
CY7C199-35LMB	EDI8833C35LB
CY7C199-45LMB	EDI8833C45LB
CY7C199-55LMB	EDI8832C55LB

IDT	EDI
IDT71256S35DB	EDI8833C35CB
IDT71256S45DB	EDI8833C45CB
IDT71256C55DB	EDI8832C55CB
IDT71256S70DB	EDI8832C70CB
IDT71256S85DB	EDI8832C85CB
IDT71256S35L32B	EDI8833C35LB
IDT71256S45L32B	EDI8833C45LB
IDT71256S55L32B	EDI8832C55LB
IDT71256S70L32B	EDI8832C70LB
IDT71256S85L32B	EDI8832C85LB

INOVA	EDI
S32K8-45MC	EDI8833C45CB
S32K8-55MC	EDI8832C55CB
S32K8-70MC	EDI8832C70CB
S32K8-85MC	EDI8832C85CB
S32K8-100MC	EDI8832C100CB

MICRON	EDI
MT5C2568CW-35	EDI8833C35CB
MT5C2568CW-45	EDI8833C45CB
MT5C2568CW-55	EDI8832C55CB
MT5C2568C-35	EDI8833C35QB
MT5C2568C-45	EDI8833C45QB
MT5C2568C-55	EDI8832C55QB
MT5C2568ECW-35	EDI8833C35LB
MT5C2568ECW-45	EDI8833C45LB
MT5C2568ECW-55	EDI8832C55LB

PERFORMANCE	EDI
P4C12567-35CMB600	EDI8833C35CB
P4C12567-45CMB600	EDI8833C45CB
P4C12567-55CMB600	EDI8832C55CB
P4C12567-35LMB	EDI8833C35LB
P4C12567-45LMB	EDI8833C45LB
P4C12567-55LMB	EDI8832C55LB

1MEG x1

IDT	EDI
IDT71027S45CB	EDI811024C45TB
IDT71027S55CB	EDI811204C55TB
IDT71027S70CB	EDI811024C70TB
IDT71027L45CB	EDI811024P45TB
IDT71027L55CB	EDI811024P55TB
IDT71027L70CB	EDI811024P70TB

256Kx4

IDT	EDI
IDT71028S45CB	EDI84257C45TB
IDT71028S55CB	EDI84257C55TB
IDT71028S70CB	EDI84257C70TB
IDT71028L45CB	EDI84257P45TB
IDT71028L55CB	EDI84257P55TB
IDT71028L70CB	EDI84257P70TB

128K X 8

IDT	EDI
IDT71024S55DB	EDI88130C55CB
IDT71024S70DB	EDI88130C70CB
IDT71024S90DB	EDI88130C90CB
IDT71024L55DB	EDI88130P55CB
IDT71024L70DB	EDI88130P70CB
IDT71024L90DB	EDI88130P90CB

128K X 8

IDT	EDI
IDT71024S55DB	EDI88130C55CB
IDT71024S70DB	EDI88130C70CB
IDT71024S90DB	EDI88130C90CB
IDT71024L55DB	EDI88130P55CB
IDT71024L70DB	EDI88130P70CB
IDT71024L90DB	EDI88130P90CB

64Kx16

CYPRESS	EDI
CYM1620HD-55C	EDI8M1664C50CC
CYM1621HD-35C	EDH816H64C-35CC
CYM1621HD-45C	EDH816H64C-45CC
CYM1621HD-35MB	EDH816H64C-35CMHR
CYM1621HD-45MB	EDH816H64C-45CMHR
CYM1623HD-70C	EDI8M1664C70CC
CYM1623HD-85C	EDI8M1664C85CC
CYM1623HD-70100C	EDI8M1664C100CC
CYM1623HD-70M	EDI8M1664C70CB
CYM1623HD-85M	EDI8M1664C85CB
CYM1623HD-100M	EDI8M1664C100CB
IDT	***EDI***
IDT7M624S35CC	EDH816H64C-35CC
IDT7M624S45CC	EDH816H64C-45CC
IDT7M624S55CC	EDH816H64C-55CC
IDT7M624S35CB	EDH816H64C-35CMHR
IDT7M624S45CB	EDH816H64C-45CMHR
IDT7M624S55CB	EDH816H64C-55CMHR
IDT7M624S85CB	EDH816H64C-70CMHR
IDT8M624S60CC	EDI8M1664C60CC
IDT8M624S70CC	EDI8M1664C70CC
IDT8M624S70CB	EDI8M1664C70CB
IDT8M624S85CB	EDI8M1664C85CB
IDT8M624S100CB	EDI8M1664C100CB

128Kx8

IDT	EDI
IDT8M824S60CC	EDI8M8128C60CC
IDT8M824S70CC	EDI8M8128C70CC
IDT8M824S70CB	EDI8M8128C70CB
IDT8M824S85CB	EDI8M8128C80CB
IDT8M824S100CB	EDI8M8128C100CB
INOVA	***EDI***
S128K8-70CC	EDI8M8128C70CC
S128K8-85CC	EDI8M8128C80CC
S128K8-100CC	EDI8M8128C100CC
S128K8-120CC	EDI8M8128C120CC
S128K8-70MC	EDI8M8128C70CB
S128K8-85MC	EDI8M8128C80CB
S128K8-100MC	EDI8M8128C100CB
S128K8-120MC	EDI8M8128C120CB

256Kx16

IDT	EDI
IDT7M4016S35CB	EDI8M16256C35CB
IDT7M4016S45CB	EDI8M16256C45CB
IDT7M4016S55CB	EDI8M16256C55CB

EDI Product Upgrade

8K x 8 Monolithic Static RAMs

Original Part No.	New Device
EDH8808AC-70LPJMHR	EDI8808CA70LB
EDH8808AC-70LPKMHR	EDI8808CA70DB
EDH8808ACL-70JMHR	EDI8808CA70LB
EDH8808ACL-70KMHR	EDI8808CA70DB
EDI8808C35CB	EDI8808CA35DB
EDI8808C45CB	EDI8808CA45DB
EDI8808C55CB	EDI8808CA55DB
EDI8808C35LB	EDI8808CA35LB
EDI8808C45LB	EDI8808CA45LB
EDI8808C55LB	EDI8808CA55LB
EDI8808C35QB	EDI8808CA35QB
EDI8808C45QB	EDI8808CA45QB
EDI8808C55QB	EDI8808CA55QB

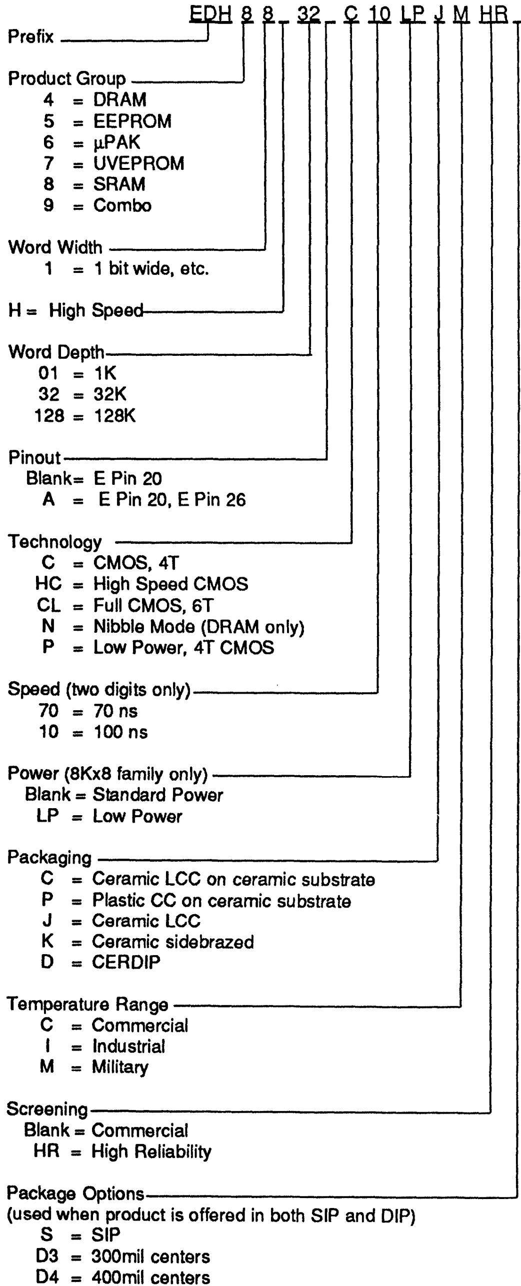
32K x 8 Monolithic Static RAMs

Original Part No.	New Device
EDH8832C-70JMHR	EDI8832C70LB
EDH8832C-70KMHR	EDI8832C70CB
EDH8832C-85JMHR	EDI8832C85LB
EDH8832C-85KMHR	EDI8832C85CB
EDH8832C-100JMHR	EDI8832C100LB
EDH8832C-100KMHR	EDI8832C100CB
EDH8832C-120JMHR	EDI8832C120LB
EDH8832C-120KMHR	EDI8832C120CB
EDH8832C-150JMHR	EDI8832C150LB
EDH8832C-150KMHR	EDI8832C150CB

EDI Part Numbers

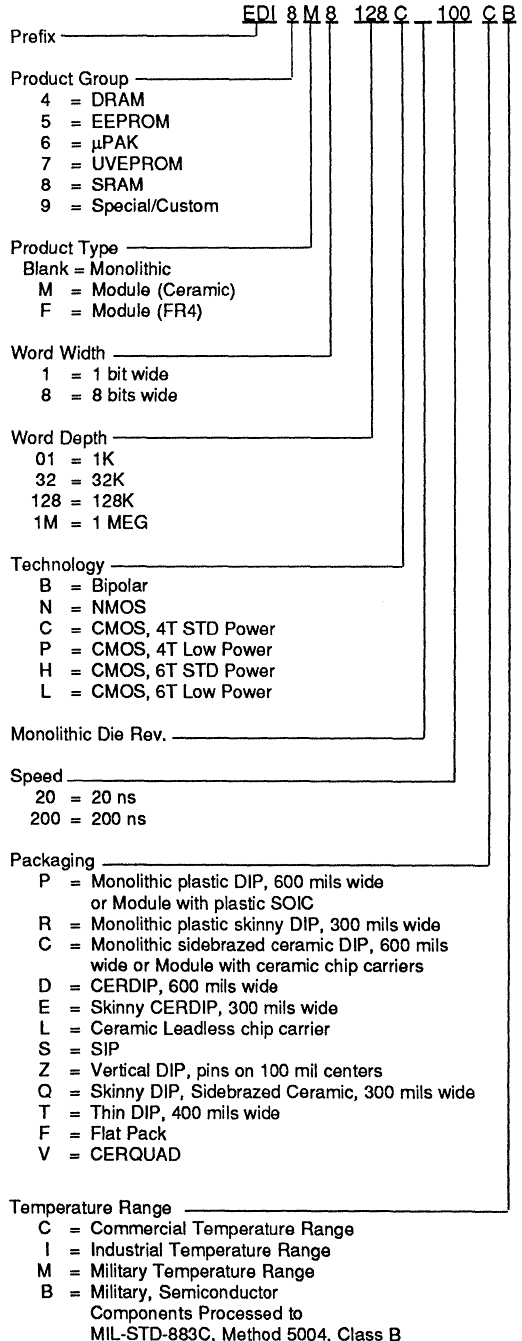
Original Numbering System

(Products introduced prior to 1/87)



Revised Numbering System

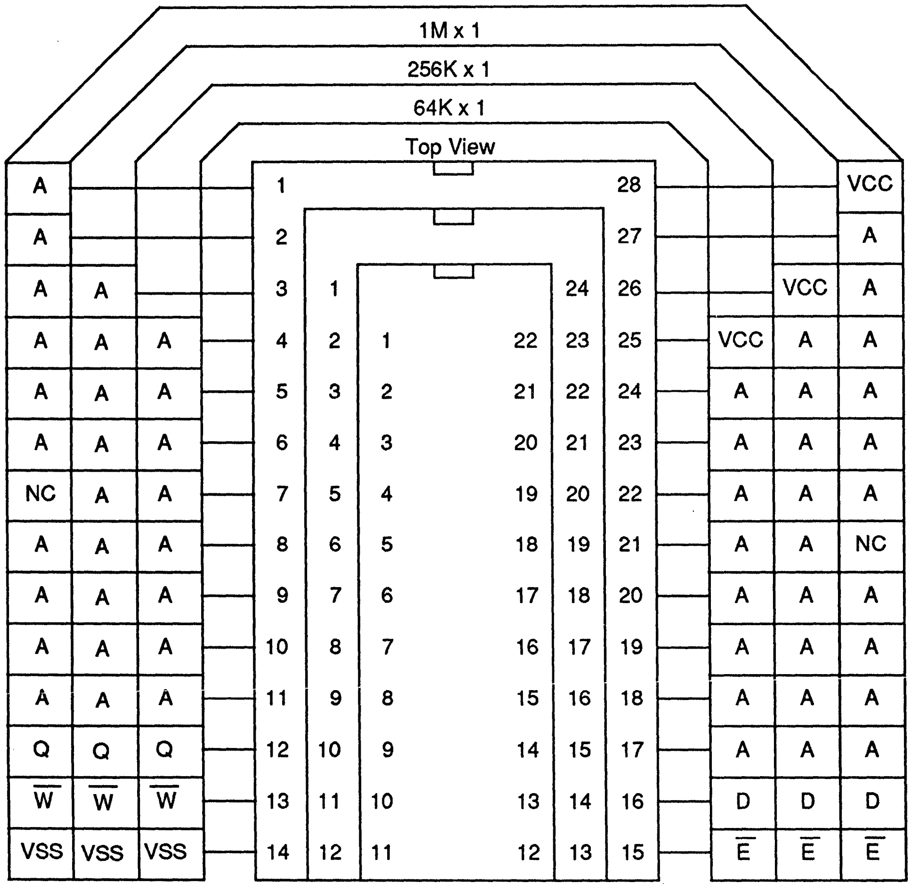
(Products introduced after 1/87)



JEDEC Standard Pinouts

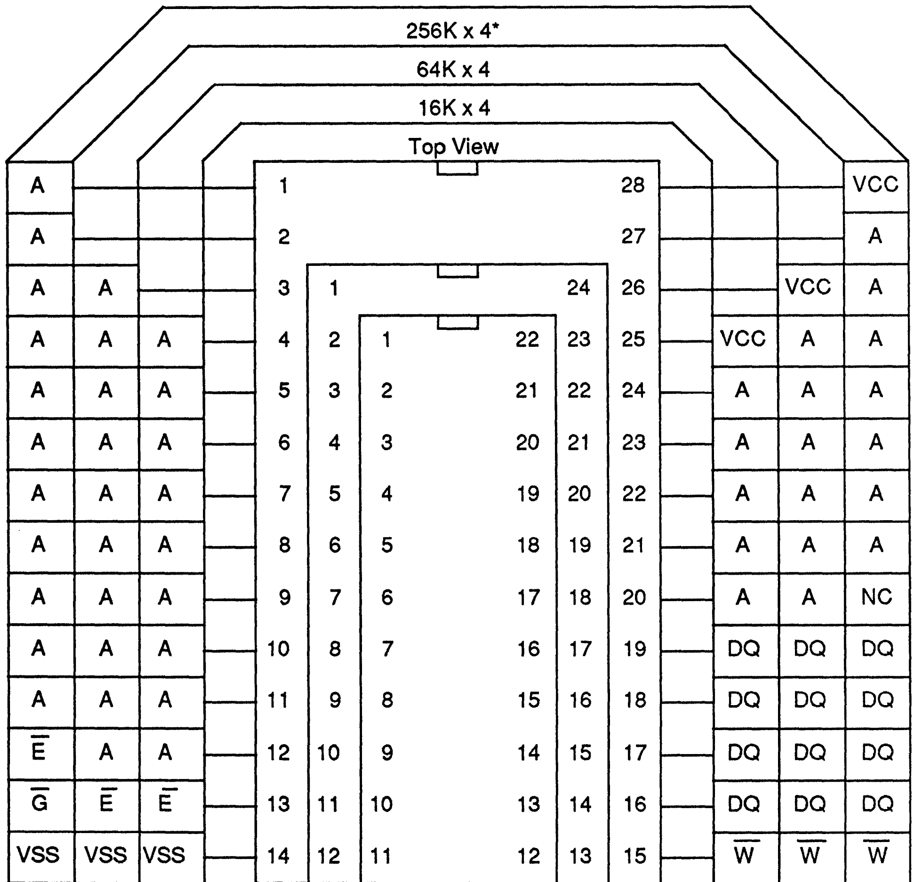
x1 Static RAM Organizations

EDI standard Static RAM devices are designed to conform to JEDEC standard pinouts in all cases, unless the device is a proprietary design offering exceptional performance features and no JEDEC standard has been established.



JEDEC Standard Pinouts

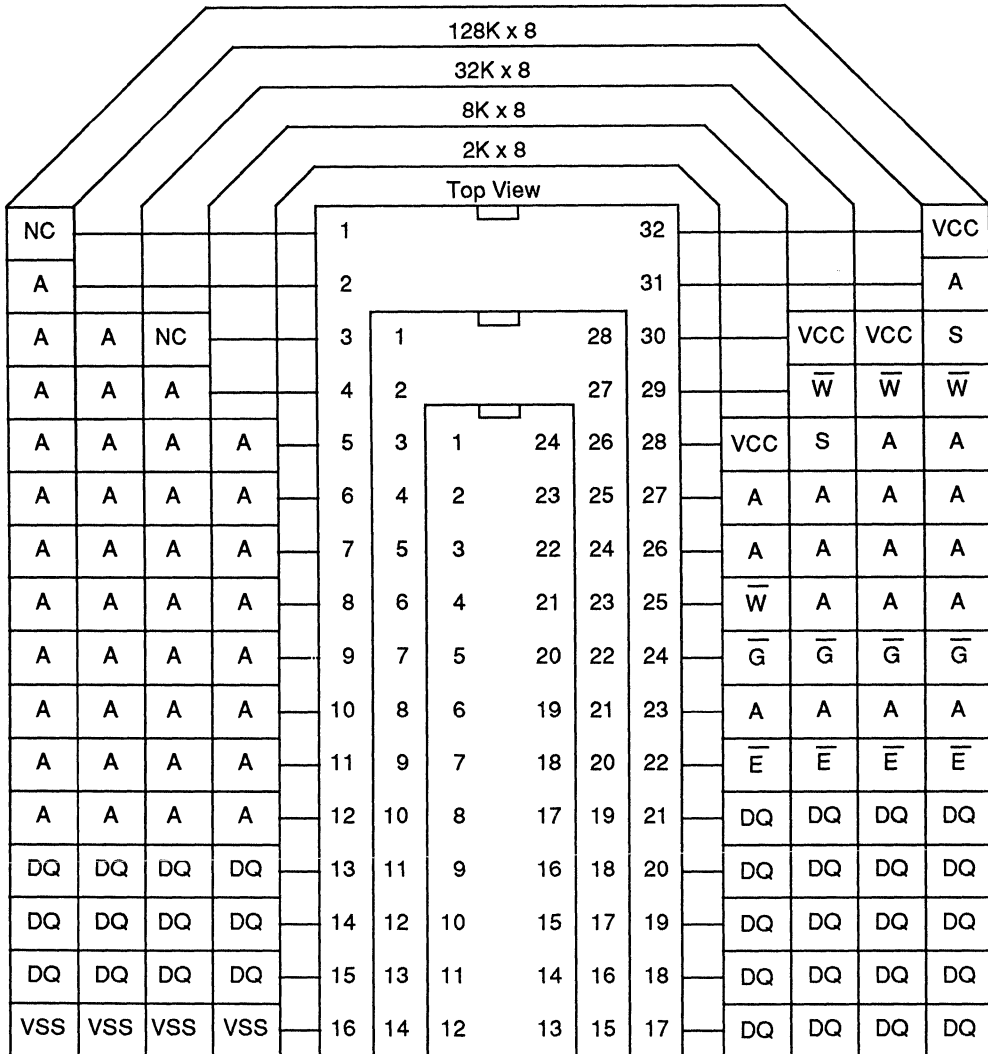
x4 Static RAM Organizations

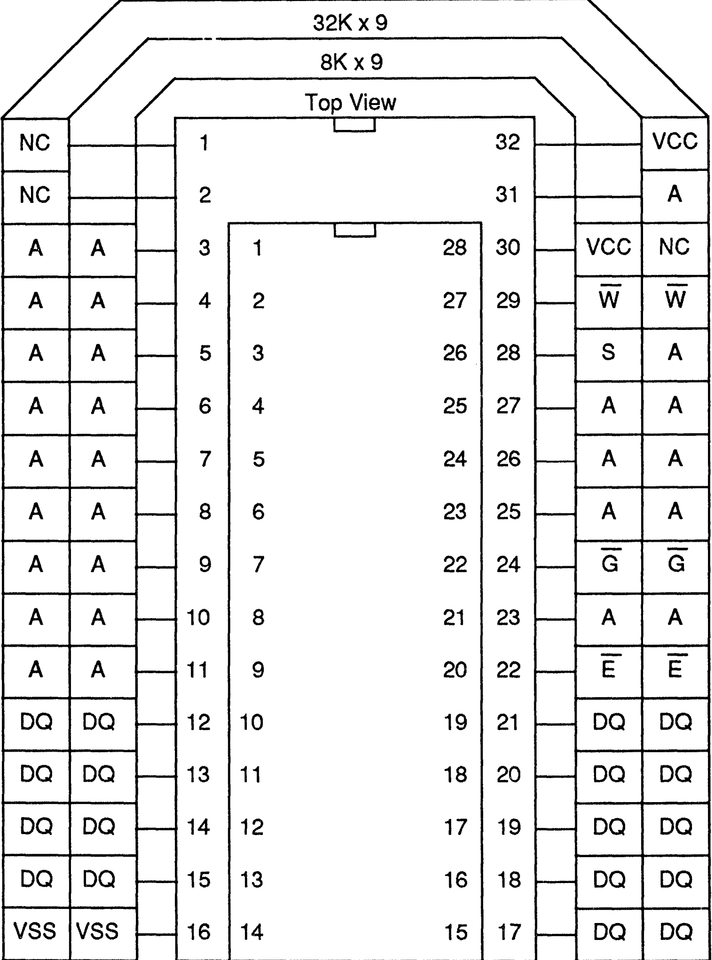


*JEDEC Approval Pending

JEDEC Standard Pinouts

x8 Static RAM Organizations





32K x 9
8K x 9
Top View
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NC
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DQ
VSS
VCC
NC
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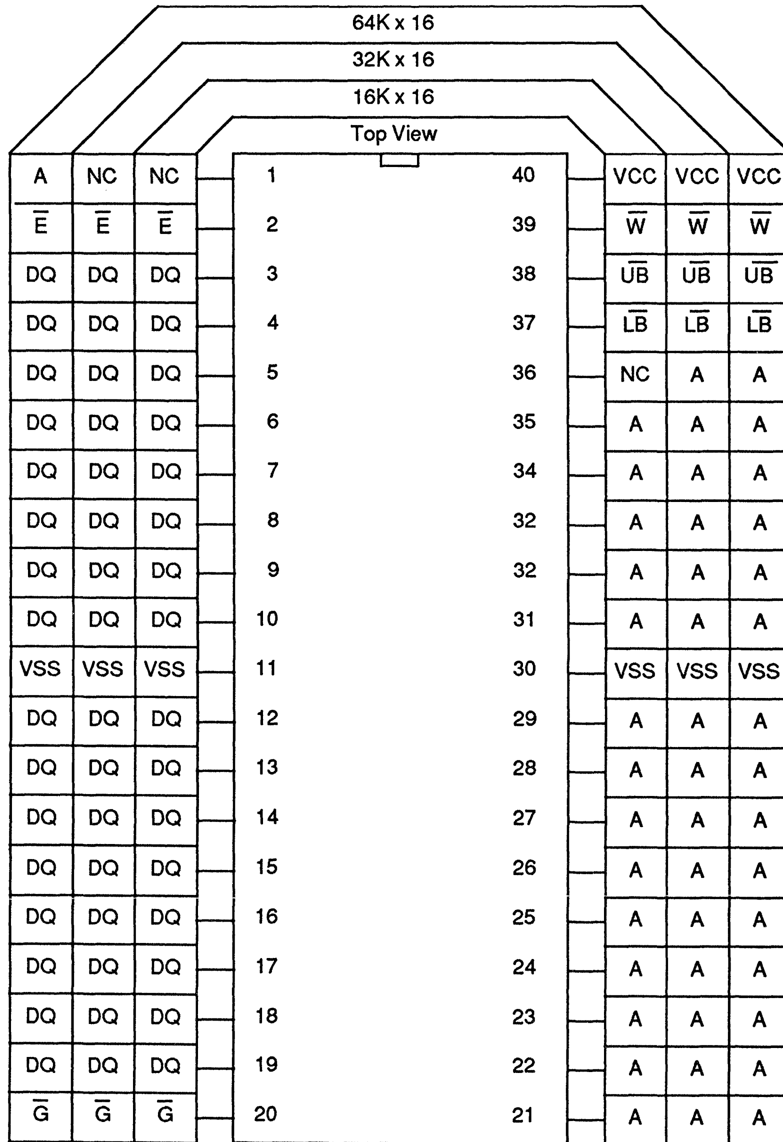
JEDEC Standard Pinouts
x16 Static RAM Organizations



Monolithic CMOS Static RAMs

Electronic Designs Incorporated is a leading supplier of high performance, low power CMOS Static Random Access Memories to the Hi-rel Market. EDI incorporates leading-edge CMOS process technology and advanced design techniques to supply Hi-rel customers with production volumes of the industry's highest performance SRAMs. EDI is committed to providing customers with a wide selection of 64K and 256K CMOS SRAMs including x1, x4, x8, and x9 organizations. EDI is currently the only hi-rel supplier of 256K density devices in all configurations (256Kx1, 64Kx4 and 32Kx8).

Within the next 24 months the EDI line will be expanded to include megabit density monolithics in x1, x4, and x8 organizations.

EDI SRAMs are currently available in a variety of the most popular standard packages, including DIPs and LCCs. We are also expanding our product packaging offering to include flatpack and CERQUAD packages during the coming year.

EDI's military devices are manufactured and processed in strict conformance to all administrative processing and performance requirements of MIL-STD-883. EDI is also listed on Defense Electronic Supply Center Standard Military Drawings for microcircuits as an approved source for 8Kx8, 8Kx9, 32Kx8, 64Kx4, and 256Kx1 devices, in both standard and low power versions.

Monolithic Static RAMs

Advance Information

Density	Org.	Part Numbers	Page
256K	32Kx8	EDI8833C35/45CB/LB/QB	28
288K	32Kx9	EDI8932C35/45CB/LB	29
1M	1Mx1	EDI811024C35/45/55/70TB	30
1M	256Kx4	EDI84256C35/45/55/70TB	31
1M	128Kx8	EDI88130C55/70/90/100CB	32

Preliminary/Final Data

Density	Org.	Part Numbers	Page
64K	8Kx8	EDI8808CA35/45/55/70DB/LB/QB	33-38
72K	8Kx9	EDI8908C35/45/55L28B/QB	39-44
256K	256Kx1	EDI81256C/P35/45/55LB/QB	45-50
256K	64Kx4	EDI8464C/P35/45/55LB	51-56
256K	64Kx4	EDI8465C/P35/45/55QB	57-62
256K	32Kx8	EDI8832C/P55/70/85/100/120/150CB/LB/QB	63-68

EDI
The future . . . today.

EDI8833C
35/45
Monolithic

ADVANCE INFORMATION

32Kx8 SRAM
CMOS, High Speed
Monolithic

The EDI8833C is a high performance, low power, high speed CMOS Static RAM organized as 32,768 words by 8 bits each. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The EDI8833C offers battery back-up data retention capability at VDD equal to 2V and operates from a 5V supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

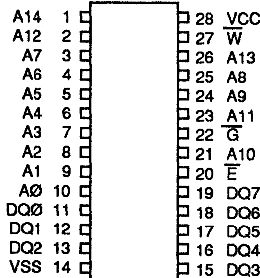
Features

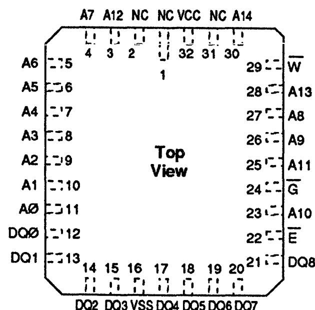
32,768x8 bit Monolithic CMOS
Static Random Access Memory
- Fast Access Times of 35 and 45ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

JEDEC Approved Packages
- 28 Pin Ceramic DIP (C)
- 32 pin Ceramic LCC (L)

Single +5V (±10%) Supply Operation

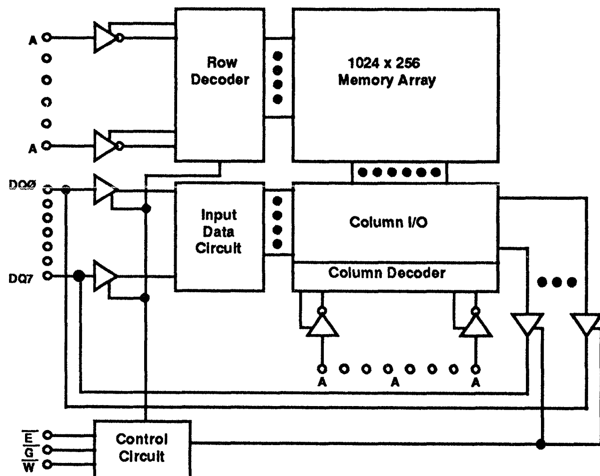
Pin Configurations and Block Diagram





Pin Names

AØ-A14	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



EDI8932C
45/55
Monolithic

ADVANCE INFORMATION

32Kx9 SRAM
CMOS, High Speed
Monolithic

The EDI8932C is a high performance, low power, high speed CMOS Static RAM organized as 32,768 words by 9 bits each. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The EDI8932C offers battery back-up data retention capability at VDD equal to 2V and operates from a 5V supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

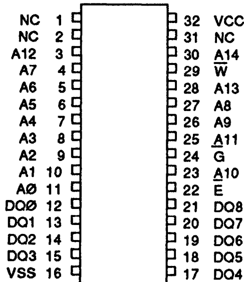
Features

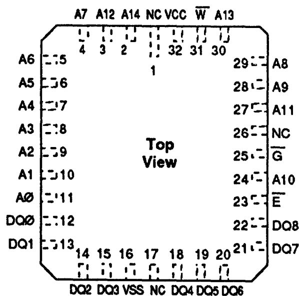
32,768x9 bit Monolithic CMOS Static Random Access Memory
- Fast Access Times of 45 and 55ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

JEDEC Approved Packages
- 28 Pin Ceramic DIP (C)
- 32 pin Ceramic LCC (L)

Single +5V (±10%) Supply Operation

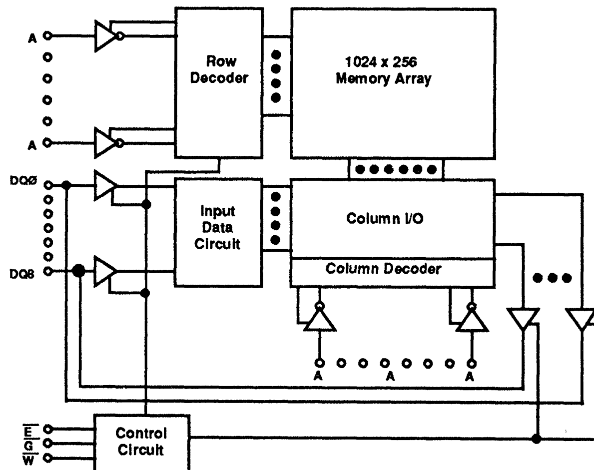
Pin Configurations and Block Diagram





Pin Names

AØ-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ8	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



EDI811024C
35/45/55/70
Monolithic

ADVANCE INFORMATION

1024Kx1 SRAM
CMOS, High Speed
Monolithic

The EDI811024C is an extremely high density, 1024Kx1 bit, high speed Static RAM designed for use in systems where fast computation, low power and board density are the main requirements.

The EDI811024C has separate input and output lines to provide fast read and write access to all memory locations.

An automatic power down feature, controlled by $\overline{E}$, permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

The 28 pin sidebrazed dual-in-line package on 400 mil centers adheres to JEDEC standards for megabit monolithics.

All inputs and outputs of the EDI811024C are TTL compatible and operate from a single five volt supply, simplifying system design.

Military grade product is manufactured to the specifications set forth in the latest revision of MIL-STD-883C, Class B.

Features

1024Kx1 bit Monolithic CMOS
Static Random Access Memory
- One Megabit Density
- Fast Access Times of 35, 45, 55, and 70ns
- Low Power Consumption
  Active: 500mW (typ.)
  Standby: 150µW (typ.)
- Battery Back-up Operation,
  2V Data Retention
- TTL Compatible

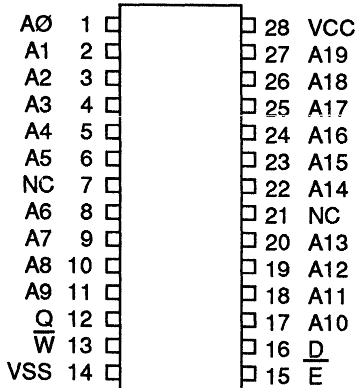
JEDEC Approved Package
- 28 Pin DIP, 400 mil Centers

Single +5V (±10%) Supply Operation

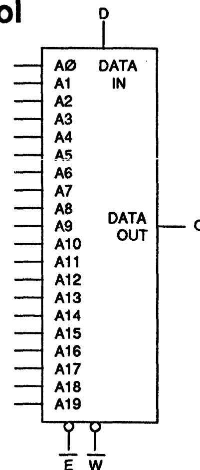
Pin Names

AØ-A19	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration



Logic Symbol



EDI84256C
35/45/55/70
Monolithic

ADVANCE INFORMATION

256K x 4 SRAM
CMOS, High Speed
Monolithic

The EDI84256C is an extremely high density, 256Kx4 bit high speed Static RAM designed for use in systems where fast computation, low power and board density are the main requirements.

The EDI84256C has four bi-directional input-output lines to provide simultaneous access to all bits in a word and has a high speed (35ns) Address Access time to achieve a considerable throughput advantage.

An automatic power down feature, controlled by E, permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

The 28 pin sidebrazed dual-in-line package on 400 mil centers adheres to JEDEC standards for megabit monolithics.

All inputs and outputs of the EDI84256C are TTL compatible and operate from a single five volt supply.

Military grade product is manufactured to the specifications set forth in the latest revision of MIL-STD-883C, Class B.

Features

256Kx4 bit Monolithic CMOS Static Random Access Memory
- One Megabit Density
- Fast Access Times of 35, 45, 55, and 70ns
- Low Power Consumption
  Active: 500mW (typ.)
  Standby: 150μW (typ.)
- Battery Back-up Operation, 2V Data Retention
- TTL Compatible

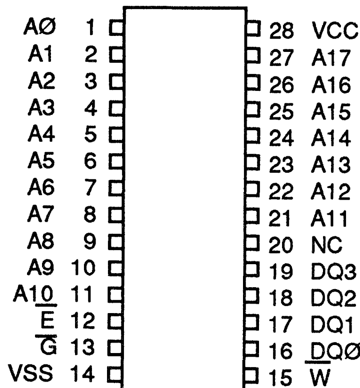
JEDEC Approved Package
- 28 Pin DIP, 400 mil Centers

Single +5V(±10%) Supply Operation

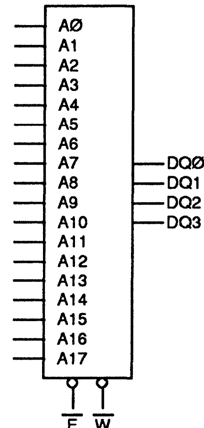
Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ3	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration



Logic Symbol



EDI88130C
55/70/90/100
Monolithic

ADVANCE INFORMATION

128K x 8 SRAM
CMOS, High Speed
Monolithic

The EDI88130C is an extremely high density 128Kx8 bit high speed Static RAM designed for use in systems where fast computation, low power and board density are the main requirements.

The EDI88130C has eight bi-directional input-output lines to provide simultaneous access to all bits in a word and has an output enable (G) pin. An automatic power down feature permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

The 32 pin sidebrazed dual-in-line package on 600 mil centers adheres to JEDEC standards for megabit monolithics.

All inputs and outputs of the EDI88130C are TTL compatible and operate from a single five volt supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

Military grade product is manufactured to the specifications set forth in the latest revision of MIL-STD-883C, Class B.

Features

128K x 8 bits Monolithic CMOS Static Random Access Memory
- One Megabit Density
- Fast Access Times of 55/70/90/100ns
- Dual Chip Selects
- Output Enable Function
- Battery Back-up Operation, 2V Data Retention
- TTL Compatible

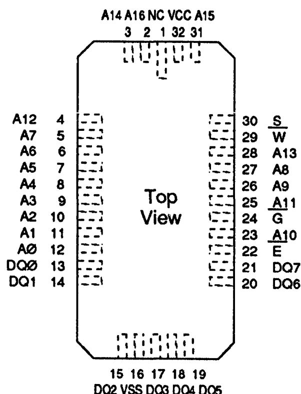
JEDEC Approved Packages
- 32 Pin DIP, 600 mil Centers
- 32 Pin LCC (Approval Pending)

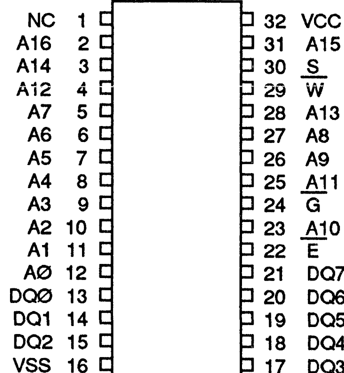
Single +5V (±10%) Supply Operation

Pin Names

AØ-A16	Address Inputs
E, S	Chip Enables
W	Write Enable
G	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configurations





8Kx8 Static RAM
CMOS, High Speed
Monolithic

The EDI8808CA is a high performance, low power CMOS Static RAM organized as 8192 words by 8 bits each. In addition to 13 address inputs, and 8 common data inputs and outputs, the device contains 4 control lines. The $\overline{E}$ and S lines perform chip enable functions and automatically power down the device when proper logic levels are applied. The $\overline{G}$ and $\overline{W}$ lines facilitate read and write operations.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

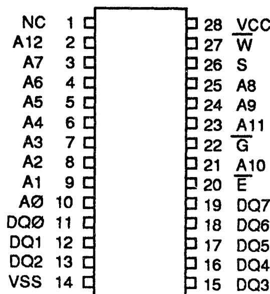
Features

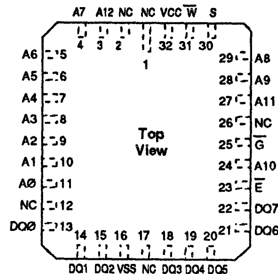
64K bit CMOS Static
Random Access Memory
- Access Times 35, 45, 55, and 70ns
- $\overline{E}$, S, and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Low Power Operation
- Inputs and Outputs Directly TTL Compatible

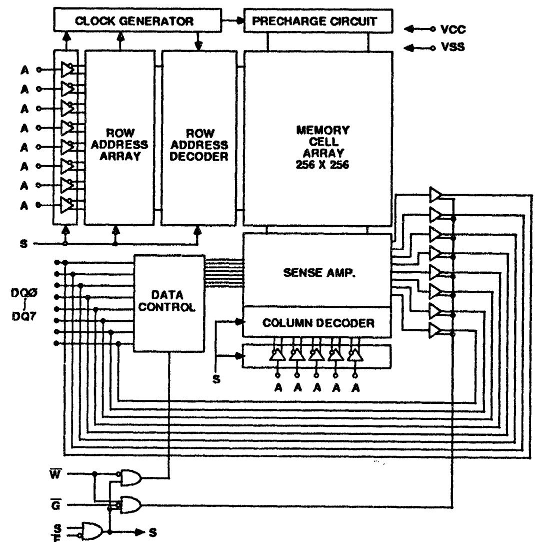
Jedec Approved Pinouts
- 28 Pin Ceramic Dual-in-line Packages
  600 mils Wide (C)
  300 mils Wide (Q)
- 32 Pin Ceramic LCC (L)

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram







Pin Names

AØ-A12	Address Inputs
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial....................................-40°C to +85°C
Military....................................-55°C to +125°C
Storage Temperature (Ambient/Ceramic).-65°C to +150°C
Power Dissipation.. 1 Watt
Output Current.. 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times... 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load..1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle S = VIH, Min Cycle	--	50	140	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH	--	2	30	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	0.1	1	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±5	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	pF

These parameters are sampled, not 100% tested.

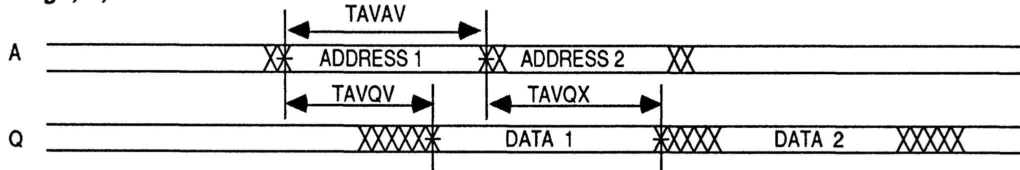
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

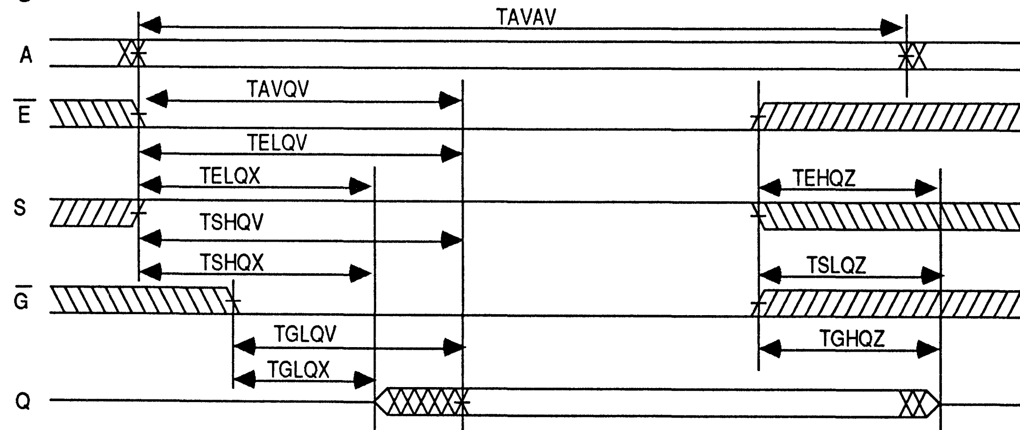
Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		35		45		55		70		ns
Address Access Time	TAVQV			35		45		55		70	ns
Chip Enable Access Time	TELQV	$\overline{E}$		35		45		55		70	ns
	TSHQV	S		35		45		55		55	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$	5		5		5		5		ns
	TSHQX	S	5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$	0	20	0	20	0	20	0	30	ns
	TSLQZ	S	0	20	0	20	0	20	0	30	ns
Output Hold from Address Change	TAVQX		5		5		5		5		ns
Output Enable to Output Valid	TGLQV			15		20		25		35	ns
Output Enable to Output in Low Z (1)	TGLQX		5		5		5		5		ns
Output Disable to Output in High Z (1)	TGHQZ			20		20		20		30	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High



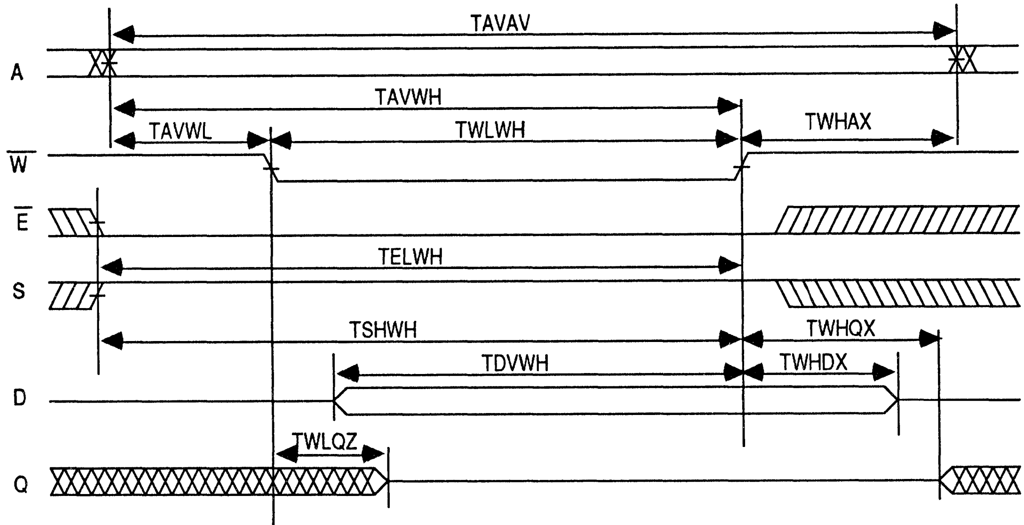
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

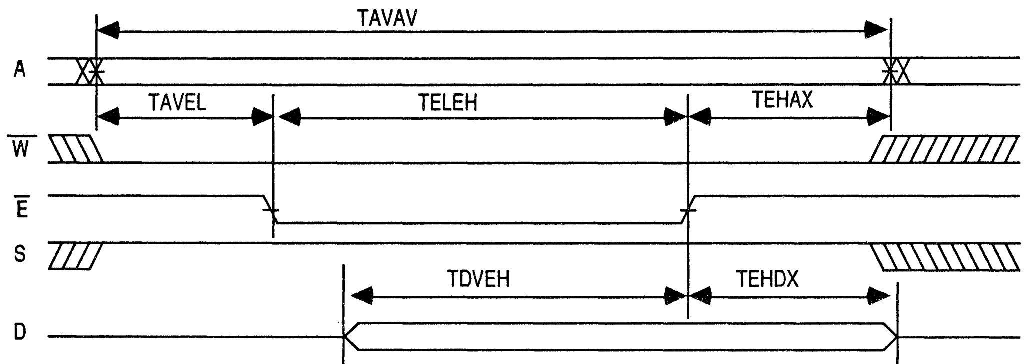
Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		70		ns
Chip Enable to	TELWH	$\overline{E}$	30		35		40		45		ns
End of Write	TSHWH	S	30		35		40		45		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		5		ns
	TAVEL	$\overline{E}$	0		0		0		5		ns
	TAVSH	S	0		0		0		5		ns
Address Valid to End of Write	TAVWH		30		35		50		65		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		30		35		45		ns
	TELEH	$\overline{E}$	25		30		35		45		ns
	TSHSL	S	25		30		45		45		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		ns
	TSLAX	S	0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		0		ns
	TSLDX	S	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ			15		20		25		30	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		25		30		ns
	TDVEH	$\overline{E}$	15		20		25		30		ns
	TDVSL	S	15		20		25		30		ns
Output Active from End of Write (1)	TWHQX		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

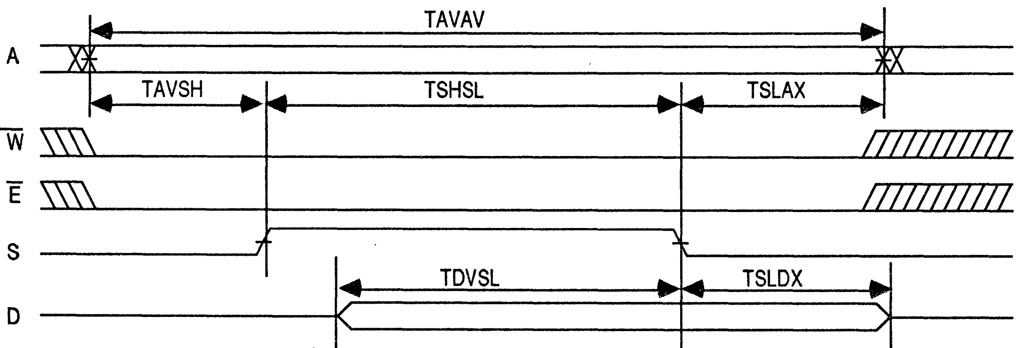
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



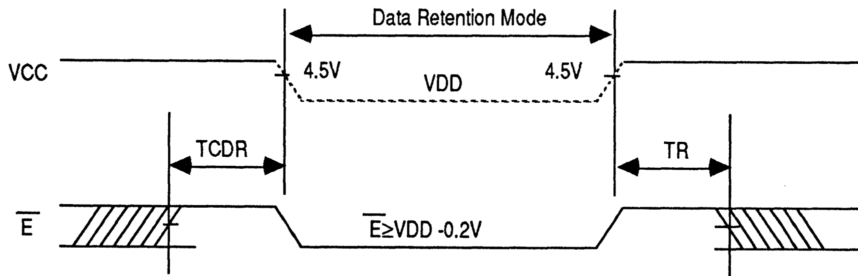
Data Retention Characteristics

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ≥ VDD -0.2V	--	20	200	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



8Kx9 Static RAM CMOS, High Speed Monolithic

The EDI8908C is a high performance, low power CMOS Static RAM organized as 8192 words by 9 bits each. In addition to 13 address inputs, and 9 common data inputs and outputs, the device contains 4 control lines. The $\overline{E}$ and S lines perform chip enable functions and automatically power down the device when proper logic levels are applied. The $\overline{G}$ and $\overline{W}$ lines facilitate read and write operations.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

Features

64K bit CMOS Static Random Access Memory

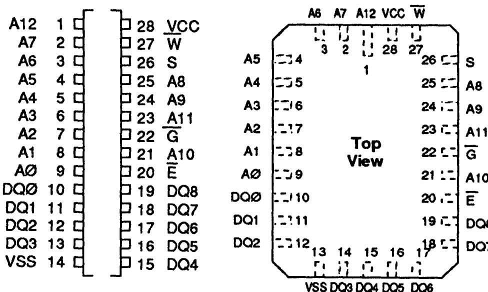
- Access Times 35, 45, and 55ns
- $\overline{E}$, S, and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Low Power Operation
- Inputs and Outputs Directly TTL Compatible

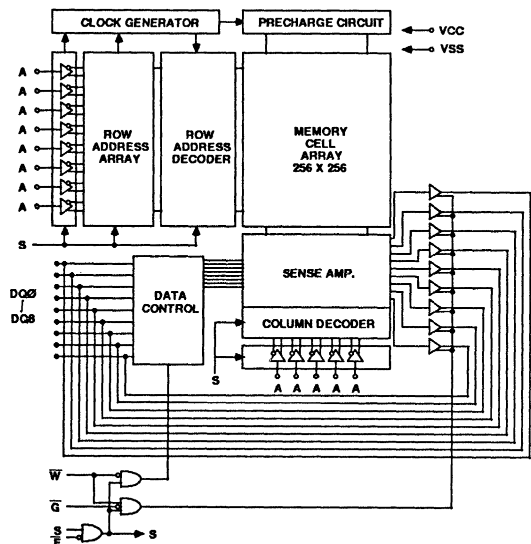
Jedec Approved Pinouts

- 28 Pin Ceramic Dual-in-line Packages 300 mils Wide (Q)
- 28 Pin Ceramic LCC (L28) Non-Jedec

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A12	Address Inputs
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ8	Data Input / Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial....................................-40°C to +85°C
Military.................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 1 Watt
Output Current... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times... 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load...1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle S = VIH, Min Cycle	--	50	140	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH	--	2	30	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	0.1	1	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	pF

These parameters are sampled, not 100% tested.

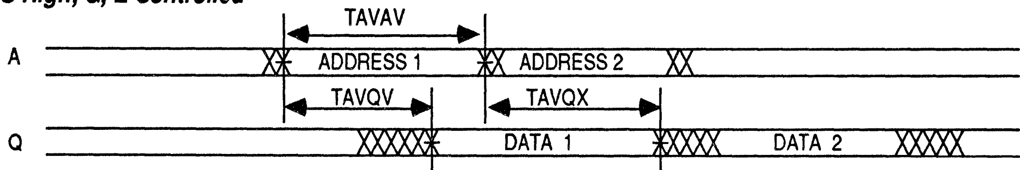
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

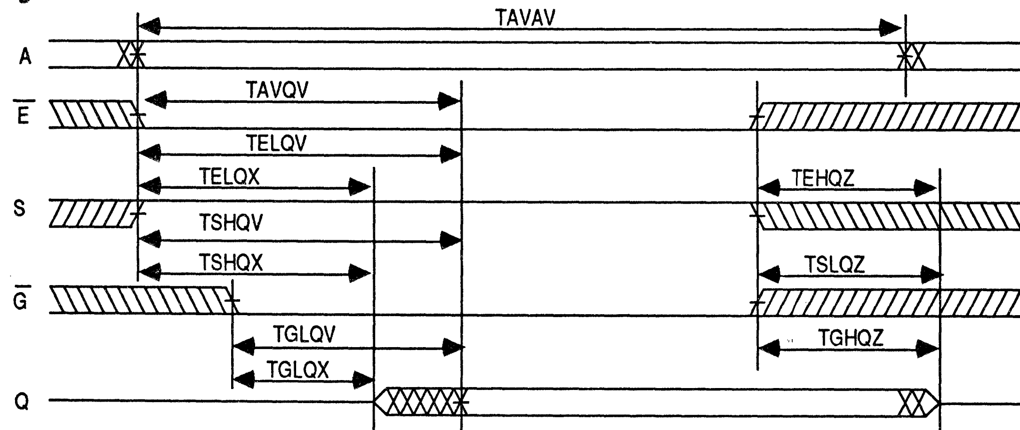
Parameter	Symbol			35ns		45ns		55ns		Units
				Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV			35		45		55		ns
Address Access Time	TAVQV				35		45		55	ns
Chip Enable Access Time	TELQV	$\overline{E}$			35		45		55	ns
	TSHQV	S			20		25		30	ns
Chip Enable to Output Low Z (1)	TELQX	$\overline{E}$		5		5		5		ns
	TSHQX	S		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$			20	0	25	0	35	ns
	TSLQZ	S			20	0	25	0	35	ns
Output Hold from Address Change	TAVQX			5		5		5		ns
Output Enable to Output Valid	TGLQV				20		25		30	ns
Output Enable to Output in Low Z (1)	TGLQX			5		5		5		ns
Output Disable to Output in High Z (1)	TGHQZ				20		25		30	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High



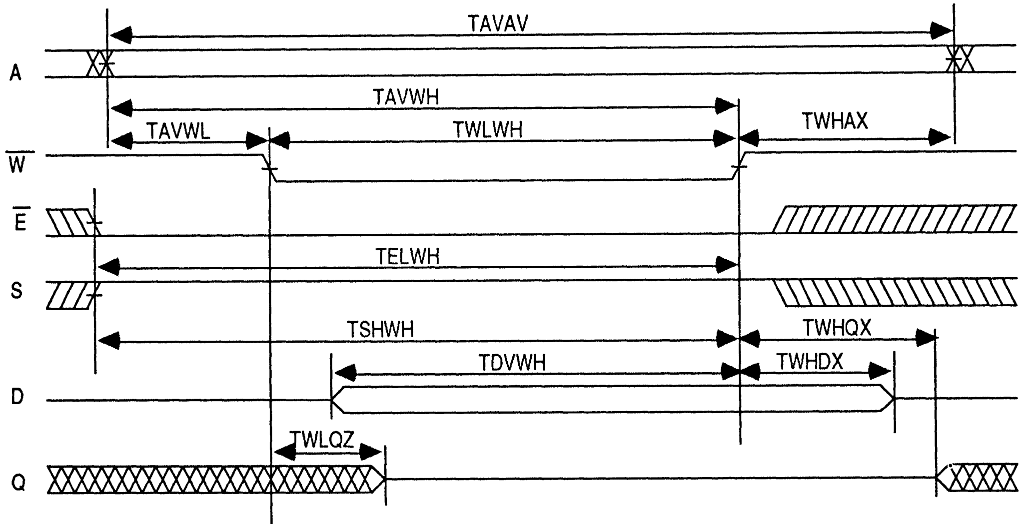
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

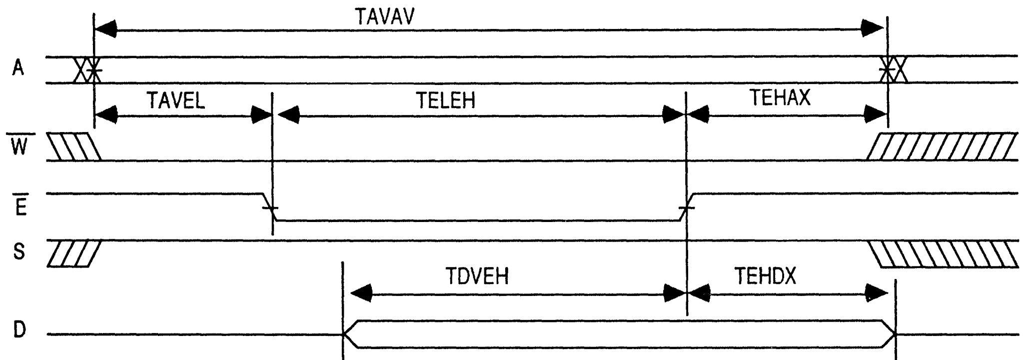
				35ns		45ns		55ns		
Parameter	**Symbol**			**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV			35		45		55		ns
Chip Enable to	TELWH	$\overline{E}$		30		40		45		ns
End of Write	TSHWH	S		20		25		30		ns
Address Setup Time	TAVWL	$\overline{W}$		5		5		5		ns
	TAVEL	$\overline{E}$		5		5		5		ns
	TAVSH	S		5		5		5		ns
Address Valid to End of Write	TAVWH			30		35		50		ns
Write Pulse Width	TWLWH	$\overline{W}$		20		25		30		ns
	TELEH	$\overline{E}$		30		40		45		ns
	TSHSL	S		20		25		30		ns
Write Recovery Time	TWHAX	$\overline{W}$		5		5		5		ns
	TEHAX	$\overline{E}$		5		5		5		ns
	TSLAX	S		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$		5		5		5		ns
	TEHDX	$\overline{E}$		5		5		5		ns
	TSLDX	S		5		5		5		ns
Write to Output in High Z (1)	TWLQZ				15		20		25	ns
Data to Write Time	TDVWH	$\overline{W}$		15		20		30		ns
	TDVEH	$\overline{E}$		15		20		30		ns
	TDVSL	S		15		20		30		ns
Output Active from End of Write (1)	TWHQX			5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

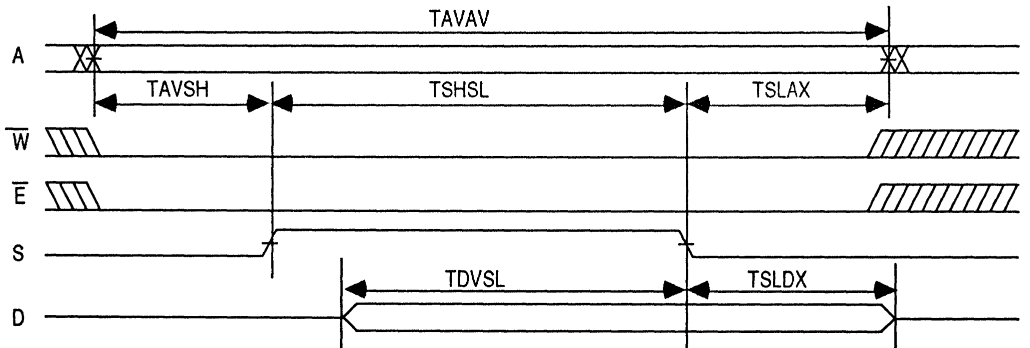
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



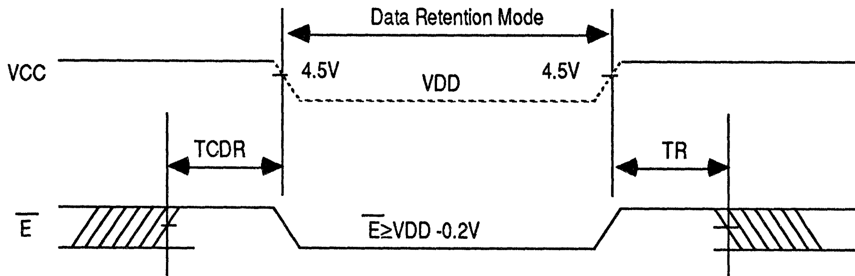
Data Retention Characteristics

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	2	600	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled



256Kx1 Static RAM CMOS, High Speed Monolithic

The EDI81256C/P is a 262,144 bit high performance, low power CMOS Static RAM organized as 256Kx1. It is available in Standard (C) and Low Power (P) versions.

Fully asynchronous, the EDI81256C/P requires no clocks or refreshing for operation.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

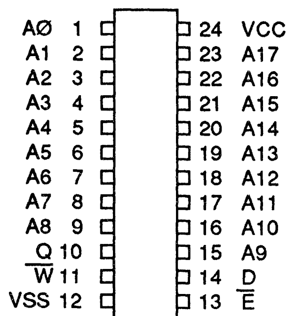
Features

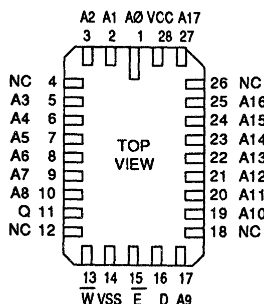
256Kx1 bit CMOS Static Random Access Memory
- Access Times 35, 45, and 55ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Data Retention Function on EDI81256P

Jedec Approved Pinouts
- 24 Pin Ceramic DIP (Q)
- 28 Pin Ceramic LCC (L)

Single +5V (±10%) Supply Operation

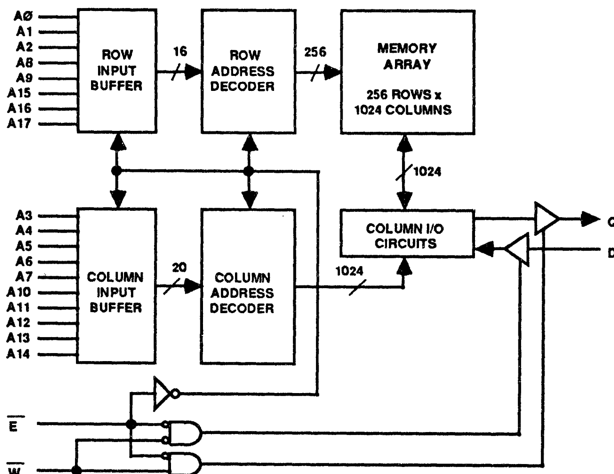
Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial.....................................-40°C to +85°C
Military..................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation... 1 Watt
Output Current.. 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times... 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load..1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	C	--	80	120	mA
			P	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	2	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V	C	--	1	10	mA
		VIN ≥VCC-0.2V or VIN≤0.2V	P	--	0.5	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±5	µA
Output High Voltage	VOH	IOH= -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	pF

These parameters are sampled, not 100% tested.

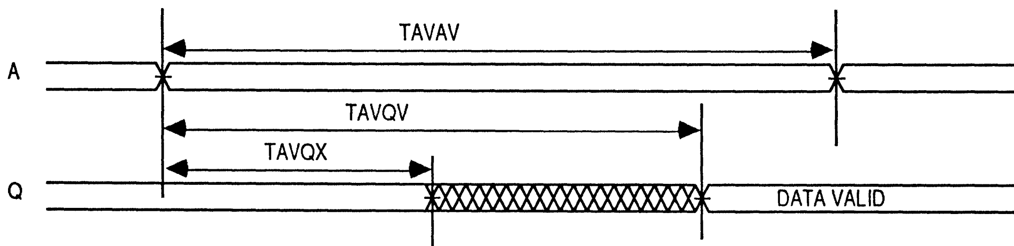
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

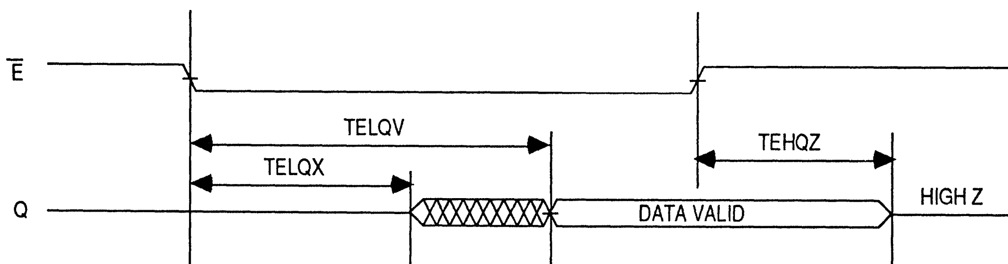
Parameter	Symbol	35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	20	0	20	0	20	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

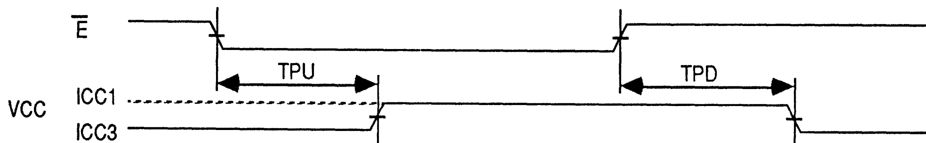
Read Cycle 1
W̄ High (continuously selected, Ē Low)



Read Cycle 2
Ē Low, W̄ High



Ē Power Down Function



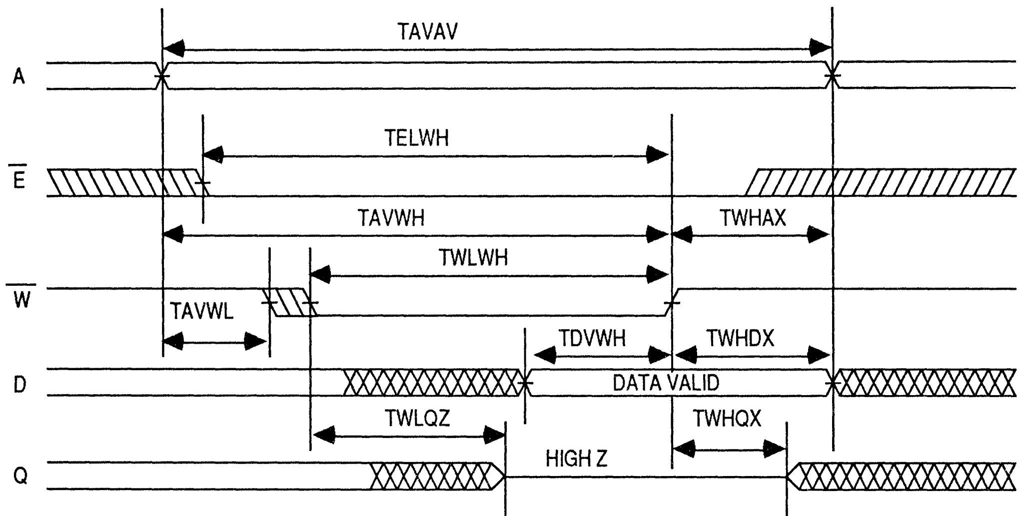
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

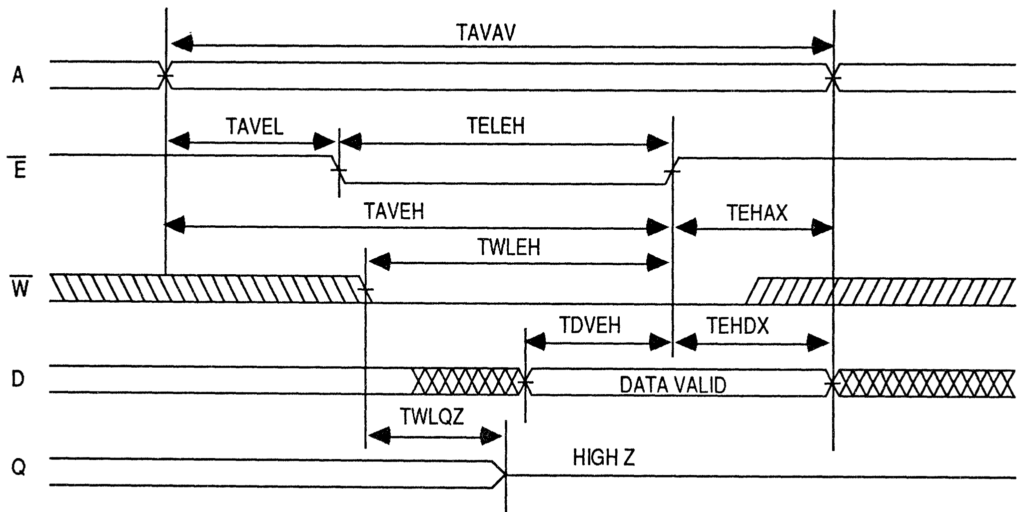
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		35		40		ns
End of Write	TWLEH	$\overline{E}$	30		35		40		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		25		30		ns
	TELEH	$\overline{E}$	25		25		30		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	15	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	20		25		25		ns
	TDVEH	$\overline{E}$	20		25		25		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



(1)

Data Retention Characteristics

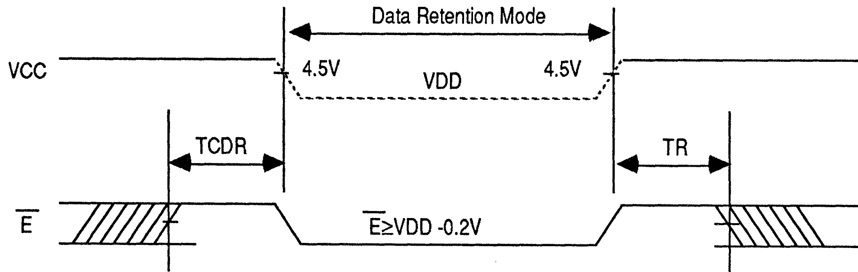
Low Power (EDI81256P Version Only)

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	50	500	μA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



64Kx4 Static RAM CMOS, High Speed Monolithic

The EDI8464C/P is a high performance CMOS Static RAM organized as 64Kx4 and available in both standard power (C) and low power (P) versions. Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

The EDI8464C/P is packaged in a 28 Pin LCC, which provides excellent board level packing densities. (For a 64Kx4 in a 24 Pin DIP package refer to EDI8465C/P.)

Military product is available 100% screened to MIL-STD-883C, Class B.

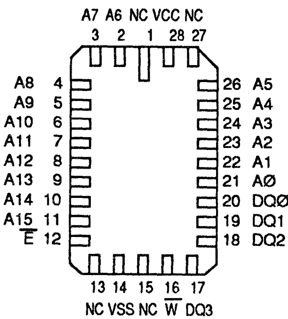
Features

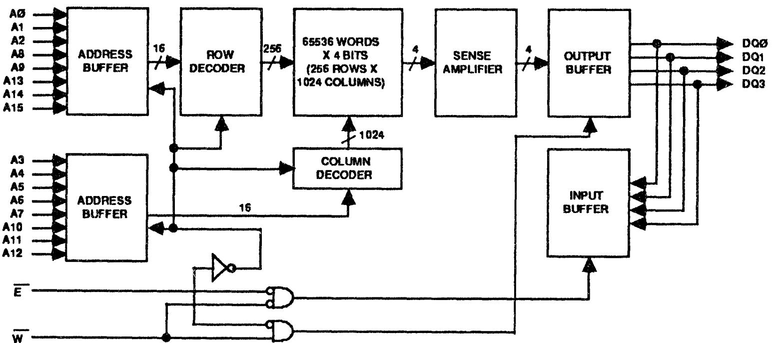
64Kx4 bit CMOS Static Random Access Memory
- Access Times 35, 45 and 55 ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Data Retention Function on EDI8464P

Jedec Approved Pinouts
- 28 Pin Ceramic LCC (L)
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
DQØ/DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial....................................-40°C to +85°C
Military.................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 1 Watt
Output Current.. 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times.. 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load...1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	C	--	80	120	mA
			P	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	2	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	C	--	1	10	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	P		0.5	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±5	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	6	pF
Capacitance Control (DQ Pins)	CD/Q	8	pF

These parameters are sampled, not 100% tested.

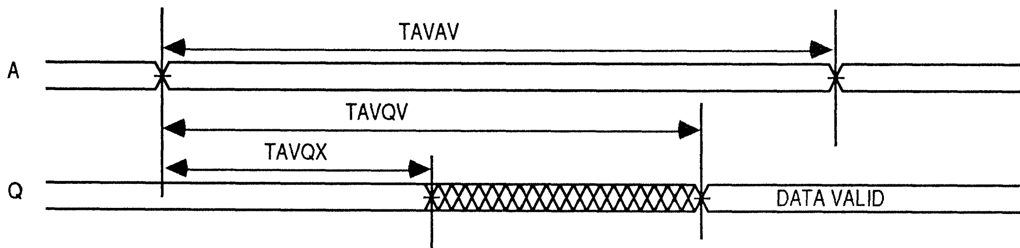
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

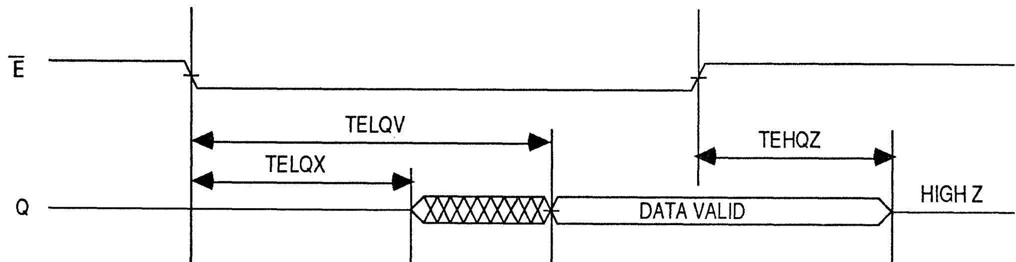
Parameter	Symbol	35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	15	0	20	0	25	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W̄ High (continuously selected, Ē Low)



Read Cycle 2
Ē Low, W̄ High



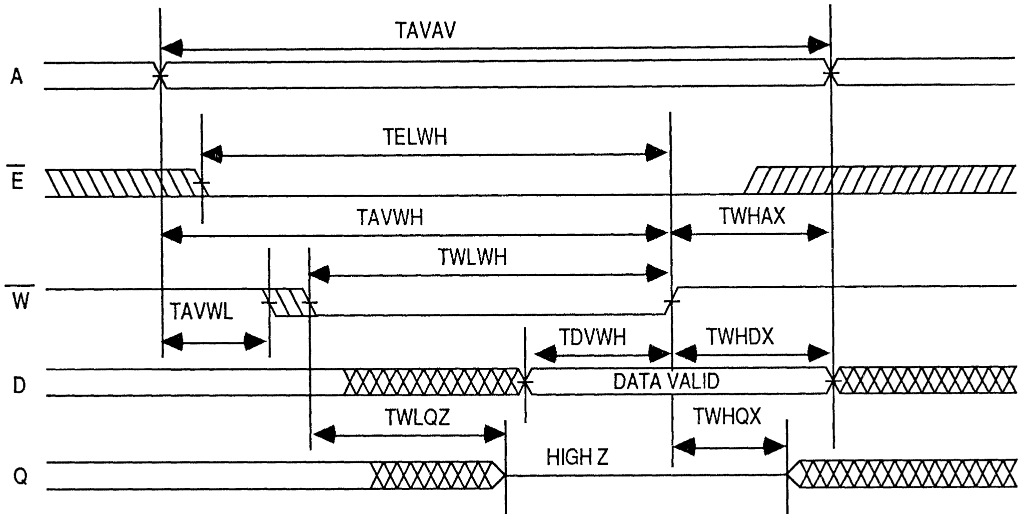
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

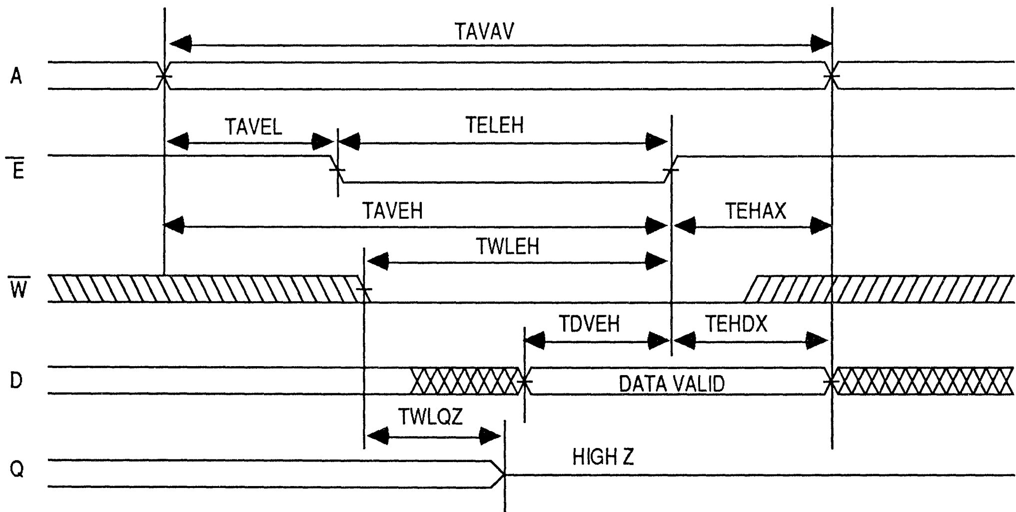
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	30		35		40		ns
	TELEH	$\overline{E}$	30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		20		ns
	TDVEH	$\overline{E}$	15		20		20		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



(1)

Data Retention Characteristics

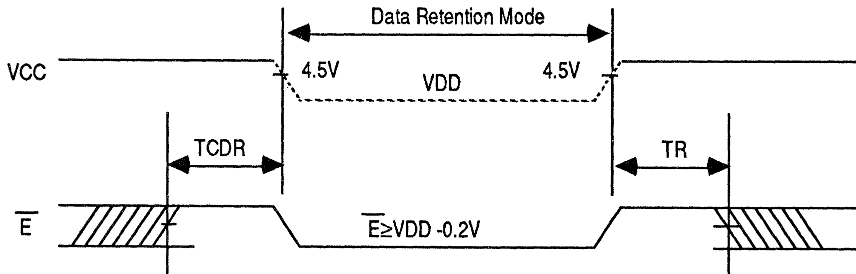
(TA =-55°C to +125°C)

Low Power (EDI8464P) Version Only

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	50	500	μA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



64Kx4 Static RAM CMOS, High Speed Monolithic

The EDI8465C/P is a high performance CMOS Static RAM organized as 64Kx4 and available in both standard power (C) and low power (P) versions. Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

The EDI8465C/P is packaged in a 300 mil wide, 24 pin DIP, which provides excellent board level packing densities.

Military product is available 100% screened to MIL-STD-883C, Class B.

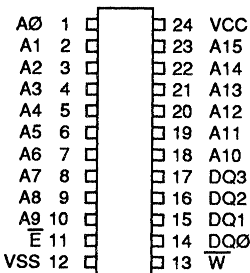
Features

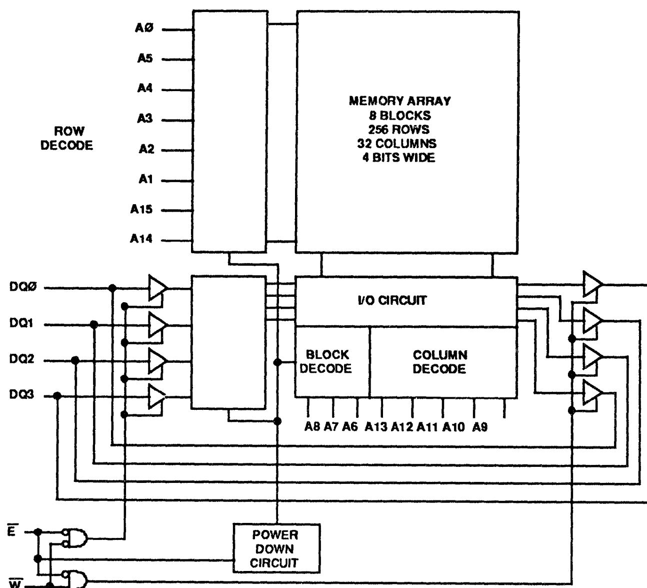
64Kx4 bit CMOS Static Random Access Memory
- Access Times 35, 45, and 55ns
- Fully Static, No Clocks
- Data Retention Function on EDI8465P
- Battery Back-up Capability
- TTL Compatilbe I/O

Jedec Approved Pinout
- 24 Pin Ceramic DIP, 300 mils wide (Q)
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
DQØ-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial....................................-40°C to +85°C
Military.................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 1 Watt
Output Current.. 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times.. 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load..1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	C	--	80	120	mA
			P	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	2	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	C	--	1	10	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	P	--	0.5	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±5	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	10	pF
Capacitance Control (DQ Pins)	CD/Q	12	pF

These parameters are sampled, not 100% tested.

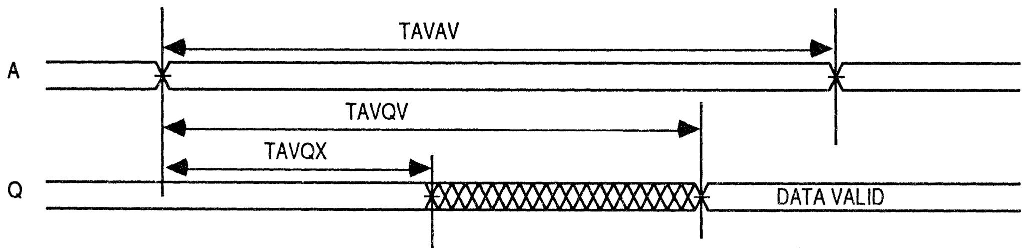
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

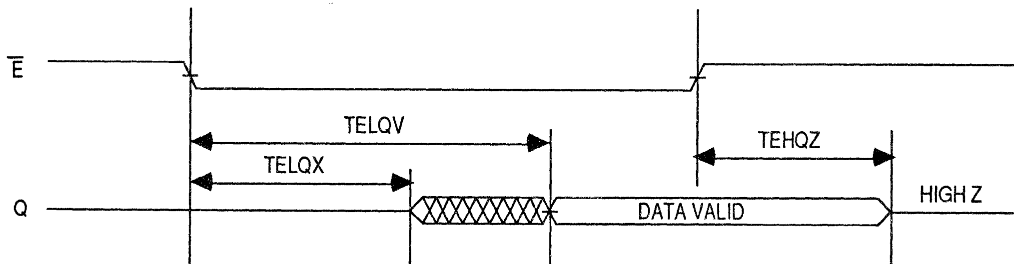
Parameter	Symbol	45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	15	0	20	0	25	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

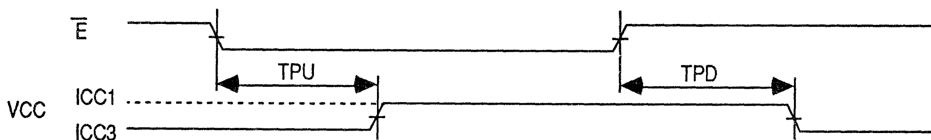
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



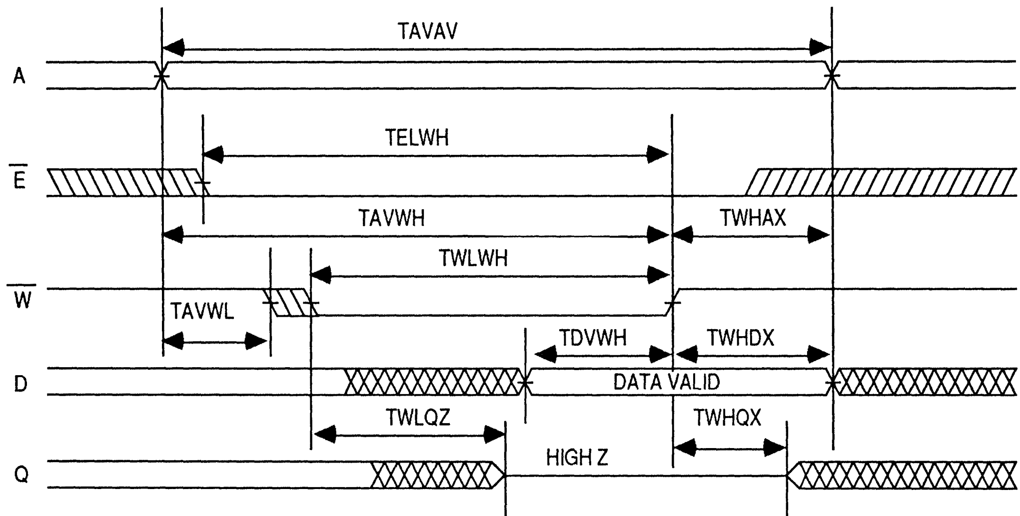
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

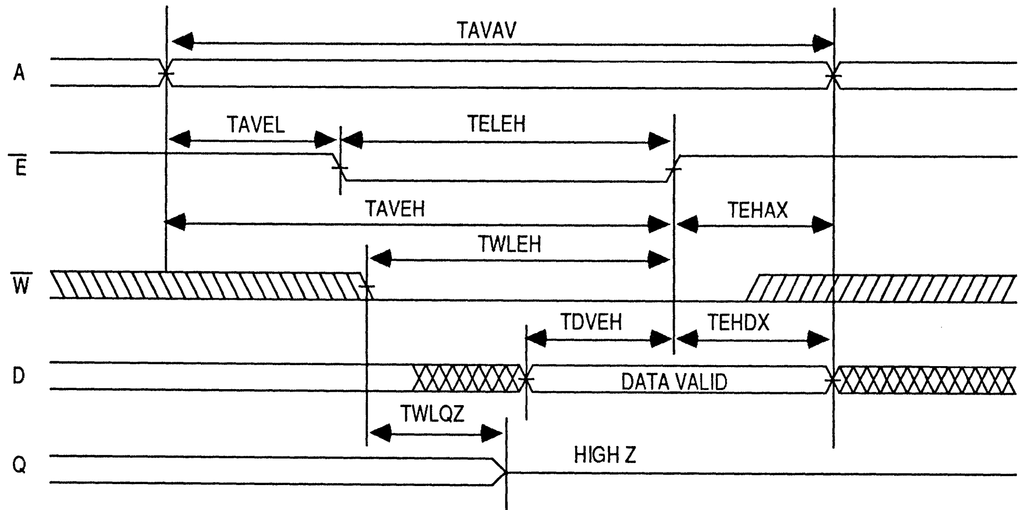
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	30		35		40		ns
	TELEH	$\overline{E}$	30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		20		ns
	TDVEH	$\overline{E}$	15		20		20		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



(1)

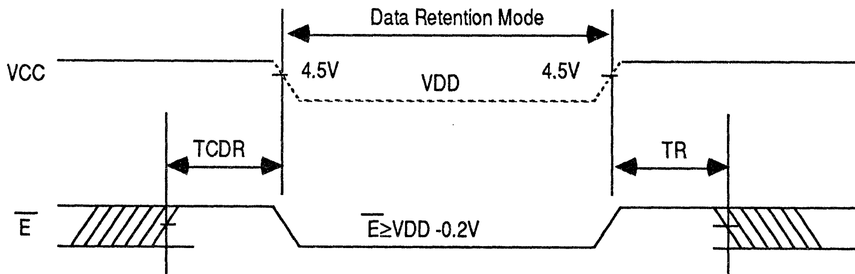
Data Retention Characteristics — *Low Power (P) Version Only*

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	50	500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



32Kx8 Static RAM
CMOS, Monolithic

The EDI8832C/P is a high performance, low power CMOS Static RAM organized as 32,768 words by 8 bits each. It is available in both standard power (C) and low power (P) versions.

Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The EDI8832C/P offers battery back-up data retention capability at VDD equal to 2V and operates from a 5 volt supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

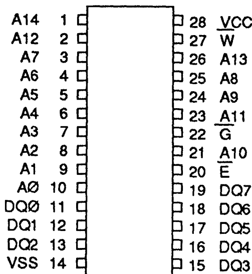
Features

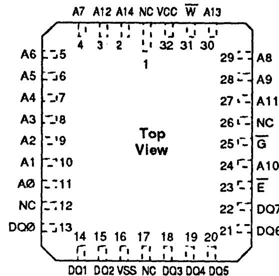
32Kx8 bit CMOS Static Random Access Memory
- Access Times 55,70, 85, 100, 120, and 150ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

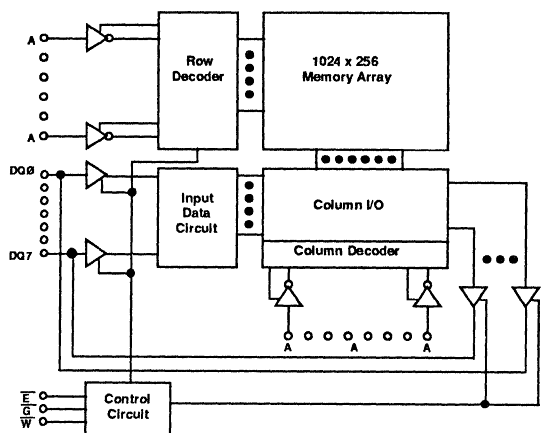
Jedec Approved Pinouts
- 28 Pin Ceramic DIP, 300 mils wide (Q)
- 28 Pin Ceramic DIP, 600 mils wide (C)
- 32 Pad Ceramic LCC (L)

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram







Pin Names

AØ-A14	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial....................................-40°C to +85°C
Military..................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 1 Watt
Output Current.. 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times.. 5ns
Input and Output Timing Levels....................................... 1.5V
Output Load.: 55/70ns.................................. 1TTL, CL =30pF
85/150ns............................ 1TTL, CL = 100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	W̄, Ē = VIL, II/O = 0mA, Min Cycle		--	60	95	mA
Standby (TTL) Power Supply Current	ICC2	Ē ≥ VIH		--	1	3	mA
Full Standby Power Supply Current	ICC3	Ē ≥ VCC-0.2V	C	--	200	1000	µA
		VIN ≥VCC-0.2V or VIN≤0.2V	P	--	20	250	µA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±5	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 4.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

Ḡ	Ē	W̄	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	pF

These parameters are sampled, not 100% tested.

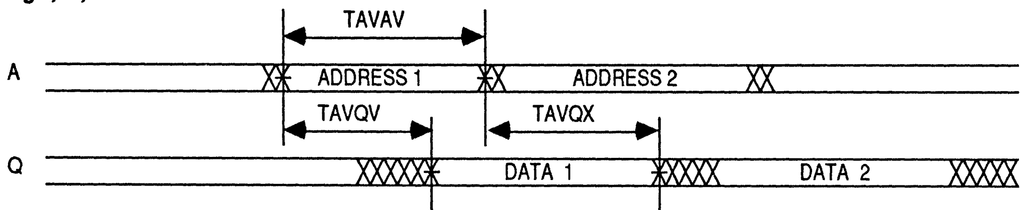
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

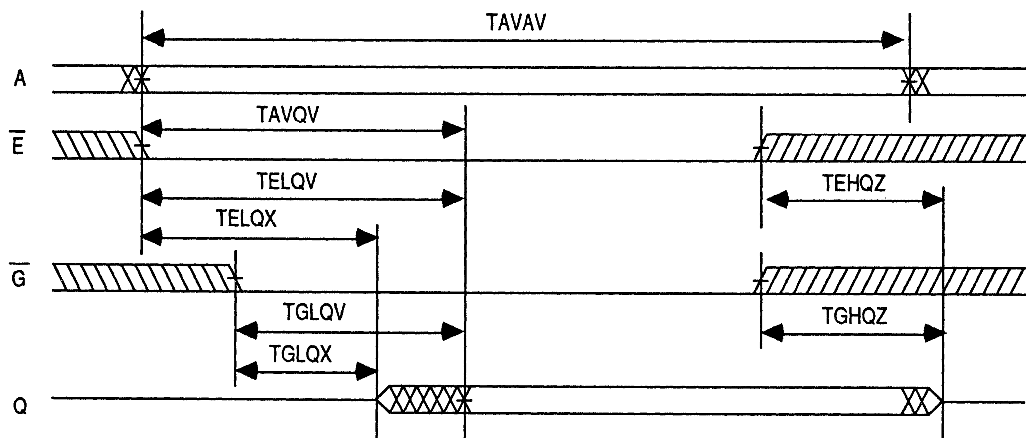
Parameter	Symbol	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	120ns Min	120ns Max	150ns Min	150ns Max	Units
Read Cycle Time	TAVAV	55		70		85		100		120		150		ns
Address Access Time	TAVQV		55		70		85		100		120		150	ns
Chip Enable Access Time	TELQV		55		70		85		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	3		3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV		30		35		35		60		60		75	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		0		0		0		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	30	0	35	0	35	0	35	0	40	0	45	ns
Output Enable to Output in High Z (1)	TGHQZ	0	30	0	35	0	35	0	35	0	40	0	45	ns
Output Hold from Address Change	TAVQX	3		3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



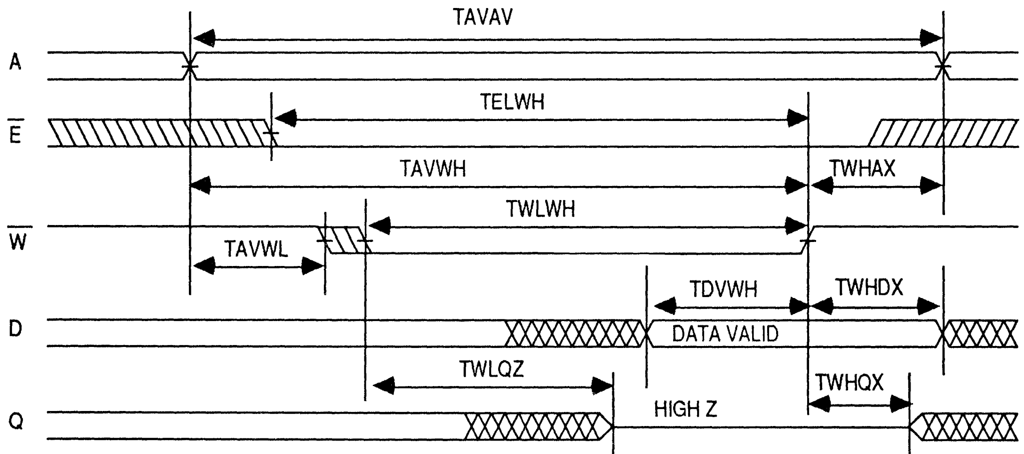
AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

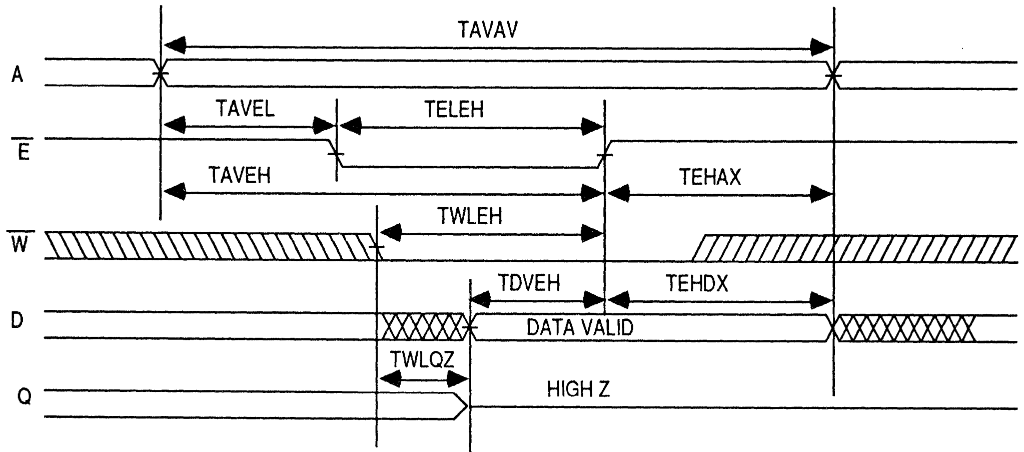
Parameter	Symbol		55ns		70ns		85ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		55		70		85		100		120		150		ns
Chip Enable to	TELWH	$\overline{W}$	45		60		70		80		85		90		ns
End of Write	TWLEH	$\overline{E}$	50		65		65		80		85		90		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	45		60		70		80		85		90		ns
End of Write	TAVEH	$\overline{E}$	45		60		70		80		85		90		ns
Write Pulse Width	TWLWH	$\overline{W}$	35		45		55		70		70		80		ns
	TELEH	$\overline{E}$	35		45		55		70		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	3		3		3		3		3		3		ns
	TEHDX	$\overline{E}$	3		3		3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ		0	30	0	40	0	45	0	50	0	50	0	50	ns
Data to Write Time	TDVWH	$\overline{W}$	25		30		35		35		40		50		ns
	TDVEH	$\overline{E}$	25		30		35		35		40		50		ns
Output Active from End of Write (1)	TWHQX		3		3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



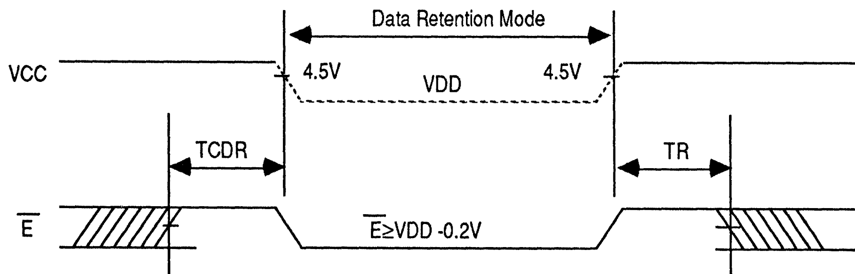
Data Retention Characteristics

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min		Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2		--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}\geq$ VDD -0.2V	C	--	100	500	µA
		VIN ≥VDD -0.2V	P	--	10	150	µA
Chip Disable to Data Retention Time	TCDR	or VIN ≤0.2V	0		--	--	ns
Operation Recovery Time	TR		TAVAV*		--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



CMOS Static RAM Modules

EDI maintains a complete, self contained, U.S.-based assembly operation for all hi-rel and high performance modules. Modules provide today's system designers with the highest possible density and performance characteristics in the smallest possible space. They also shorten design time and allow for ease of manufacturing.

High performance CMOS products in surface mounted packages, combined with thermally matched substrates produce very dense and highly reliable subsystems. Conventional pins sidebrazed to the substrate allow the device to be assembled on circuit board using conventional through-hole manufacturing techniques.

EDI has pioneered module technology and was able to provide the military market its first 64K density Static RAM in 1983, and is continuing its leadership role in the production of Static RAMs in one to four megabit densities, with devices up to 16 megabits planned for the coming year. Modules, with standard JEDEC pin-outs, can provide designers with performance capabilities several years before the available technology can produce a comparable monolithic device. In addition, modules can be used to produce application specific devices that cannot be produced cost effectively from a single piece of silicon.

ASIC modules can include error detection, parity, address latching or buffering, and wide word (x16 and x32) systems.

Complete memory systems (ie: high speed cache, buffered inputs/latched outputs) can be configured in a single module. This provides the system designer with a complete CMOS SRAM solution with the benefits of space-saving surface mount technology.

Static RAM Modules

Advance Information

Density	Org.	Part Numbers	Page
1M	256Kx4	EDI8M4257C35/45/55/70CB/CC	70
2M	512Kx4	EDI8M4512C45/55/70CB/CC	71
2M	256Kx8	EDI8M8257C90/100/120/150CB/CC	72
4M	512Kx8	EDI8M8512C90/100/120/150CB/CC	73
4M	256Kx16	EDI8M16256C35/45/55/70CB/CC	74

Preliminary/Final Data

Density	Org.	Part Numbers	Page
256K	16Kx16	EDH816H16C-25/35/45CC-Z/CMHR-Z	75-79
512K	64Kx8	EDI8M864C50/60/70/80CB/CC	80-85
512K	64Kx8	EDI8M864C90/100/120/150CB/CC	86-91
1M	128Kx8	EDI8M8128C/P50/60/70/80CB/CC	92-97
1M	128Kx8	EDI8M8128C/P90/100/120/150CB/CC	98-103
1M	128Kx8	EDI8M8128C100/120/150PC	104-108
1M	128Kx8	EDI8M8130C50/60/70/80CB/CC	109-114
1M	128Kx8	EDI8M8130C/P90/100/120/150CB/CC	115-120
1M	64Kx16	EDH816H64C-35/45/55/70CC/CMHR	121-126
1M	64Kx16	EDI8F1664C100/120/150PC	127-131
1M	64Kx16	EDI8M1664C50/60/70/85/100CB/CC	132-137
2M	256Kx8	EDI8M8256C70/100/120PC	138-142

EDI8M4257C
35/45/55
Module

ADVANCE INFORMATION

256Kx4 SRAM
CMOS, High Speed
Module

The EDI8M4257C is a Megabit (256Kx4-bit) High Speed Static RAM Module with four bi-directional input/output lines. The module is constructed of four 256Kx1 Static RAMs in leadless chip carriers surface mounted on a multi-layered ceramic substrate. Extremely high speeds are achievable by the use of EDI81256C high performance, high reliability Static RAMs. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest one Megabit module available.

All inputs and outputs of the EDI8M4257C are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

EDI military grade modules are constructed with semiconductor components which are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

Features

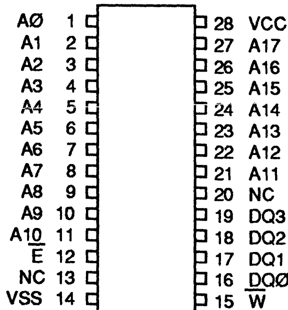
256Kx4 bit, Megabit Density CMOS Static Random Access Memory Module
- Fast Access Times of 35, 45, and 55ns
- Low power consumption:
  - Active: 1600mW (typ)
  - Standby: 40mW (typ)
- Common I/O lines
- TTL-compatible inputs and outputs

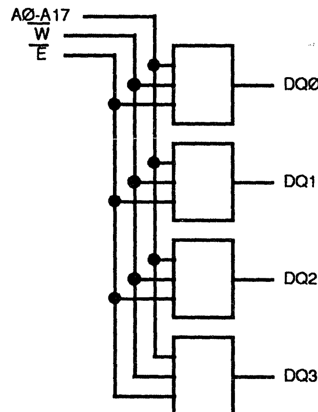
28 pin DIP, 400 mil centers
Single +5V (±10%) Supply Operation

Pin Names

AØ-A17	Address Inputs
E̅	Chip Enables
W̅	Write Enable
DQØ-DQ3	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





EDI8M4512C
45/55/70
Module

ADVANCE INFORMATION

512Kx4 SRAM
CMOS, High Speed
Module

The EDI8M4512C is a Two Megabit (512Kx4-bit) High Speed Static RAM Module with four bi-directional input/output lines. The module is constructed of eight 64Kx4 Static RAMs in leadless chip carriers surface mounted on a multi-layered ceramic substrate.

All inputs and outputs of the EDI8M4512C are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

EDI military grade modules are constructed with semiconductor components which are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

Features

512Kx4 bit, Two Megabit Density CMOS Static Random Access Memory Module

- Fast Access Times of 45, 55, and 70ns
- Low power consumption
- Common I/O lines
- TTL-compatible inputs and outputs

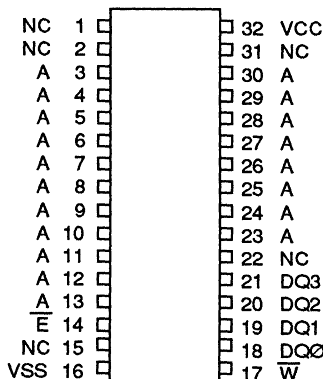
32 pin DIP, 600 mil centers

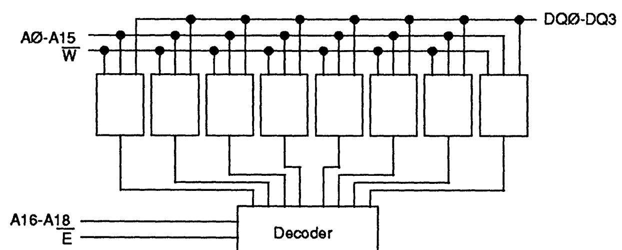
Single +5V (±10%) Supply Operation

Pin Names

AØ-A18	Address Inputs
E̅	Chip Enables
W̅	Write Enable
DQØ-DQ3	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





EDI8M8257C

90/100/120/150 Module

ADVANCE INFORMATION

256Kx8 SRAM CMOS, High Speed Module

The EDI8M8257C is a 2048K (256Kx8 bit) High Speed Static RAM module constructed using two EDI88128C (128Kx8) Static RAMs in leadless chip carriers on a multi-layered ceramic substrate. Functional equivalence to proposed monolithic (Two Megabit Static RAM) is achieved by utilization of an on-board decoder that interprets the higher order address (A17) to select one of the two 128Kx8 RAMs.

The EDI8M8257C is offered in a 32-pin, side-brazed DIP on 600 mil centers, adhering to JEDEC standards for Two Megabit pinout.

All inputs and outputs of the EDI8M8257C are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

Semiconductor components used in EDI military modules are processed to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

Features

256Kx8 bit, Two Megabit Density CMOS Static Random Access Memory Module
- Fast Access Times of 90, 100, 120, and 150ns
- Fully Static, No Clocks
- Data Retention Function
- TTL-Compatible Inputs and Outputs

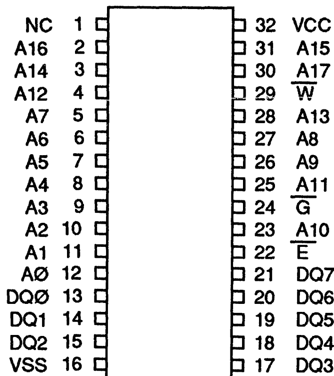
32 pin DIP, 600 mil Centers
- JEDEC Approved Pinout

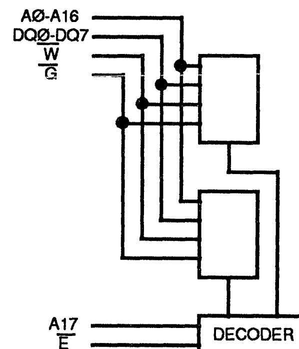
Single +5V (±10%) Supply Operation

Pin Names

AØ-A17	Address Inputs
$\overline{E}$	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





EDI8M8512C
90/100/120/150
Module

ADVANCE INFORMATION

512Kx8 SRAM
CMOS, High Speed
Module

The EDI8M8512C is a 4096K (512Kx8 bit) High Speed Static RAM module constructed using four EDI88128C (128Kx8) Static RAMs in leadless chip carriers on a multi-layered ceramic substrate. Functional equivalence to proposed monolithic Four Megabit Static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A17 and A18 to select one of the four 128Kx8 RAMs.

The EDI8M8512C is offered in a 32-pin, side-brazed DIP on 600 mil centers, adhering to JEDEC standards for the Four Megabit pinout, allowing for compaitibility with future monolithics.

All inputs and outputs of the EDI8M8512C are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

Semiconductor components used in EDI military modules are processed to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

Features

512Kx8 bit, Four Megabit Density CMOS Static Random Access Memory Module
- Fast Access Times of 90, 100, 120, and 150ns
- Fully Static, No Clocks
- Data Retention Function
- TTL-compatible inputs and outputs

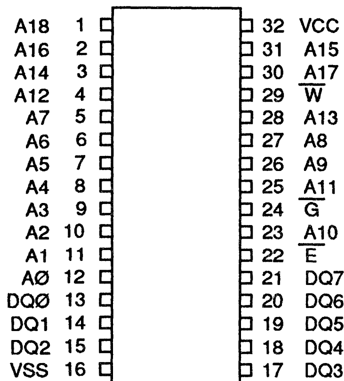
32 pin DIP, 600 mil centers
- JEDEC Approved Pinout

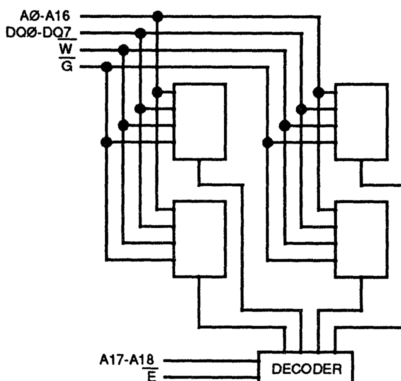
Single +5V (±10%) Supply Operation

Pin Names

AØ-A18	Address Inputs
$\overline{E}$	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





The future . . . today.

EDI8M16256C
35/45/55/70
Module

ADVANCE INFORMATION

256Kx16 SRAM
CMOS, High Speed
Module

The EDI8M16256C is a 4096K (256Kx16bit) High Speed Static RAM module constructed using sixteen EDI81256C (256Kx1) Static RAMs in leadless chip carriers on a multi-layered ceramic substrate. The EDI8M16256C is an upgrade from the EDI816H64C (1024K RAM module). Four chip select lines (one for each group of four RAMs) allow the user to configure the memory into a 256Kx16, 512Kx8 or 1024Kx4 organization.

The EDI8M16256C is offered in a 48-pin, 900 mil center sidebraze DIP to take advantage of the compact leadless chip carriers. This enables Four Megabits of Static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the EDI8M16256C are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

Semiconductor components used in EDI military modules are processed to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

Features

256Kx16 bit, Four Megabit Density CMOS Static Random Access Memory Module
- Fast Access Times of 35, 45, 55, and 70ns
- Customer Configured Memory as 256Kx16, 512Kx8, or 1024Kx4
- Fully Static, No Clocks
- TTL-Compatible Inputs and Outputs

48 pin Dual-in-line Package
- Multiple Power Pins for Maximum Noise Immunity

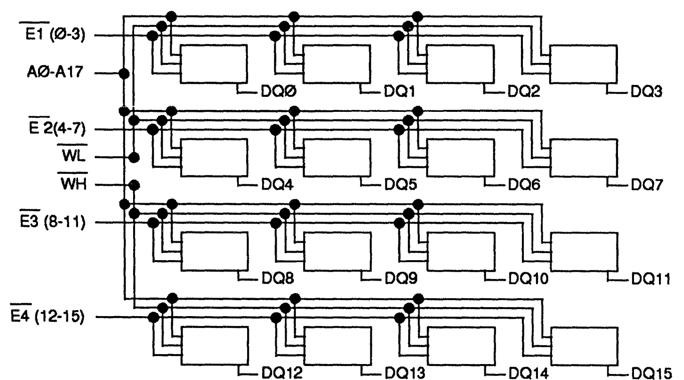
Single +5V (±10%) Supply Operation

Pin Names

AØ-A17	Address Inputs
E1-E4	Chip Enables
WL-WH	Write Enables
DQØ-DQ15	Data Input/Output
VCC	Power (+5V+10%)
VSS	Ground

Pin Configuration and Block Diagram

Name	Pin	Pin	Name
VSS	1	48	VCC
NC	2	47	DQØ
AØ	3	46	DQ1
A1	4	45	DQ2
A2	5	44	DQ3
WL	6	43	E1(0-3)
E2(4-7)	7	42	A3
DQ4	8	41	A4
DQ5	9	40	A5
DQ6	10	39	A6
DQ7	11	38	A7
VSS	12	37	A8
A9	13	36	VCC
A10	14	35	DQ8
A11	15	34	DQ9
A12	16	33	DQ10
A13	17	32	DQ11
WH	18	31	E3(8-11)
E4(12-15)	19	30	A14
DQ12	20	29	A15
DQ13	21	28	A16
DQ14	22	27	A17
DQ15	23	26	NC
VCC	24	25	VSS



16Kx16 Static RAM CMOS, High Speed Module

The EDH816H16C is a 256K bit high speed CMOS Static RAM module based on four 16Kx4 Static RAMs in leadless chip carriers, mounted on a multilayered ceramic substrate.

The 36 pin vertical dual-in-line package (100 mil centers) provides high density in addition to fast access times of 25, 35, and 45 ns.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

EDI Military Modules are constructed using semiconductor components which have been 100% screened to the test methods of MIL-STD-883C, Class B.

Features

16Kx16 bit CMOS Static Random Access Memory Module

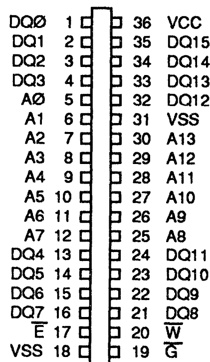
- Access Times 25, 35, and 45ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- 36 Pin Vertical Dual-in-line Package, 100 mil centers

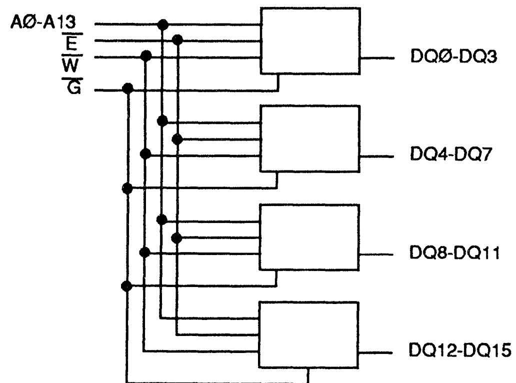
Ideal for:

- Bit Slice Micro Code
- Cache Memory
- Long Word Applications

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A13	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ15	Data Input/ Data Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .... -0.3V to 7.0V
Operating Temperature TA (Ambient)
Commercial .... 0°C to +70°C
Military .... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation .... 2 Watts
Output Current. .... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels .... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load .... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA	--	240	440	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH	--	40	65	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	μA
Output Leakage Current	IOL	V I/O = 0V to VCC, $\overline{E}$=VIH	--	--	10	μA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	Output Deselect	HIGH Z	ICC1
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance	CI	50	pF
Input Capacitance Control Lines	CC	35	pF
Output Capacitance	CO	25	pF

These parameters are sampled, not 100% tested.

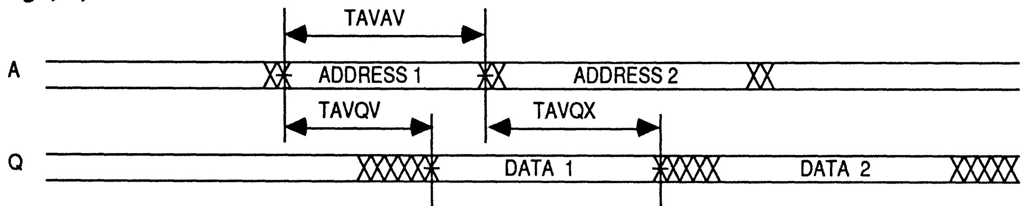
AC Characteristics
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

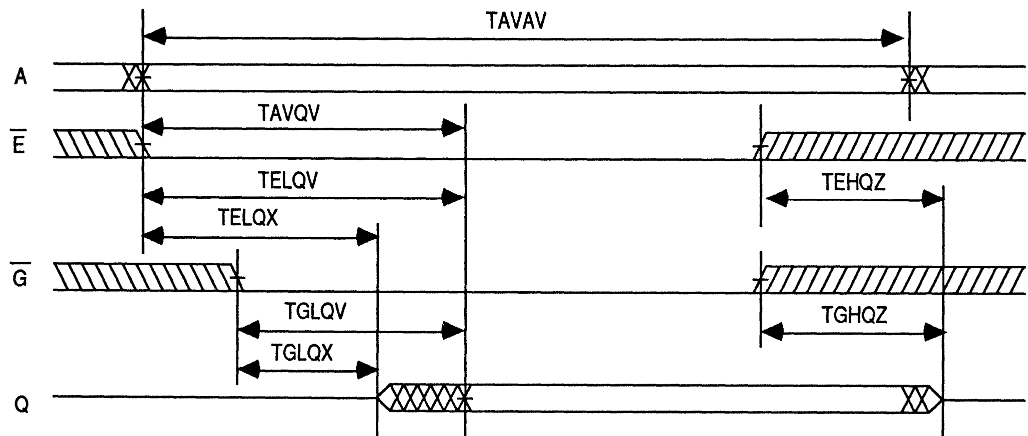
Parameter	Symbol	25ns		35ns		45ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	25		35		45		ns
Address Access Time	TAVQV		25		35		45	ns
Chip Enable Access Time	TELQV		25		35		45	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Output Enable to Output Valid	TGLQV		15		20		25	ns
Output Enable to Output in Low Z	TGLQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ		10		15		15	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		25		35		45	ns

Note 1: Parameter guaranteed, but not tested.

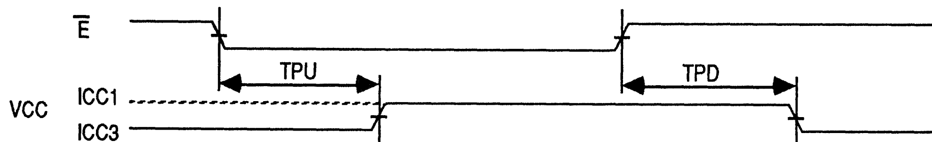
Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



$\overline{E}$ Power Down Function



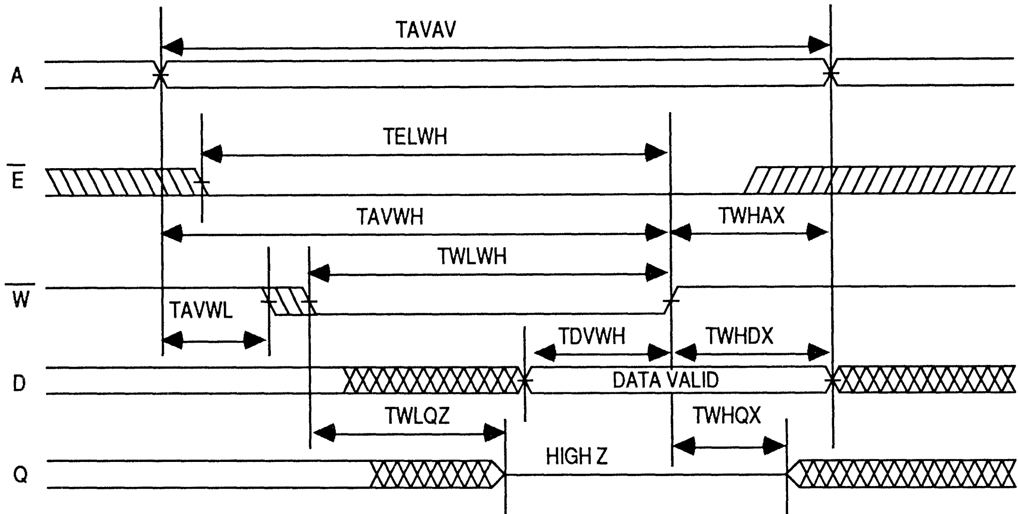
AC Characteristics
Write Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

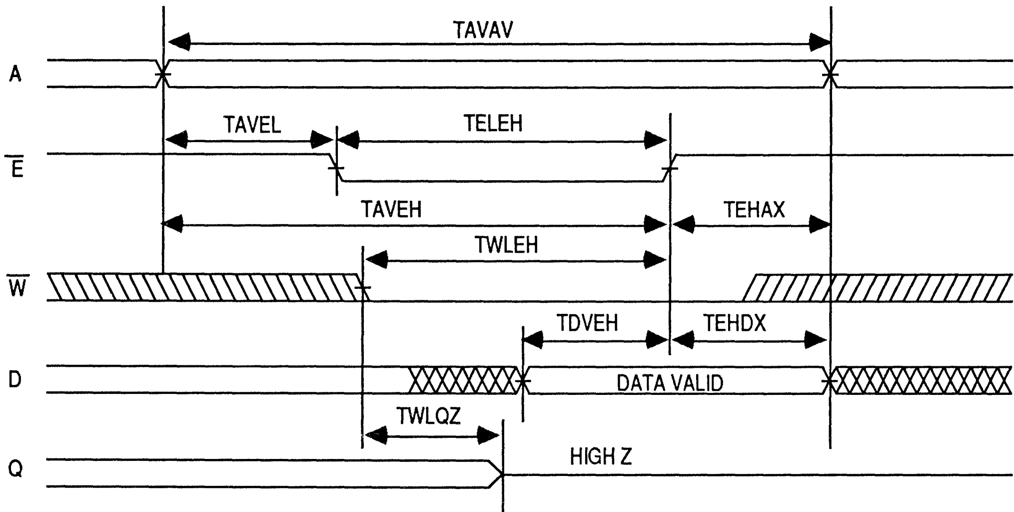
Parameter	Symbol		25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	Units
Write Cycle Time	TAVAV		25		35		45		ns
Chip Enable to	TELWH	$\overline{W}$	20		30		40		ns
End of Write	TWLEH	$\overline{E}$	20		30		40		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	20		25		35		ns
End of Write	TAVEH	$\overline{E}$	20		25		35		ns
Write Pulse Width	TWLWH	$\overline{W}$	20		25		35		ns
	TELEH	$\overline{E}$	20		25		35		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ			10		10		15	ns
Data to Write Time	TDVWH	$\overline{W}$	15		15		20		ns
	TDVEH	$\overline{E}$	15		15		20		ns
Output Active from End of Write (1)	TWHQX		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



64Kx8 Static RAM CMOS, Module

The EDI8M864C is a 512K bit CMOS Static RAM based on two 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate. The EDI8M864C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M864C requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C,Class B., making them ideally suited to applications demanding the highest level of performance and reliability.

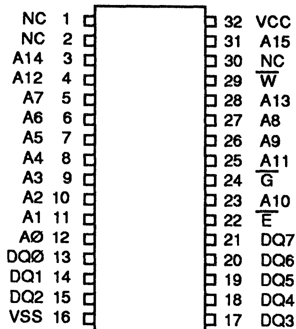
Features

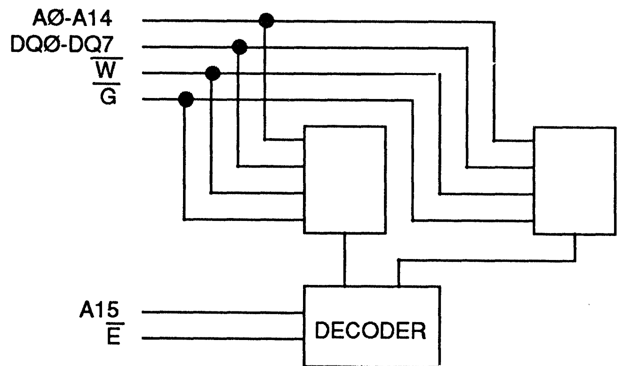
64Kx8 bit CMOS Static Random Access Memory
- Access Times 50, 60, 70, and 80ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial .... 0°C to +70°C
Military .... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation .... 1 Watt
Output Current. .... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. ....VSS to 3.0V
Input Rise and Fall Times.. ....5ns
Input and Output Timing Levels...................................... ....1.5V
Output Load.: ....1TTL, CL = 30pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	70	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH	--	15	40	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V VIN ≥VCC-0.2V or VIN≤0.2V	--	1	5	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH= -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

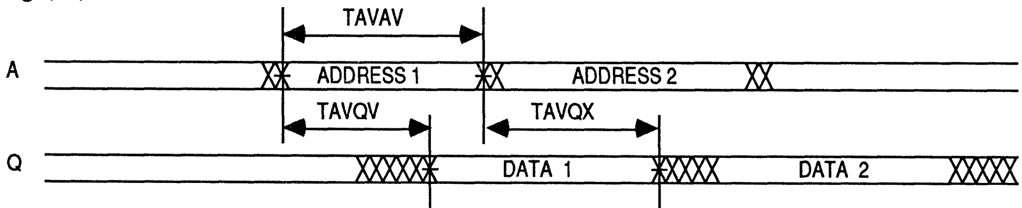
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol	50ns*		60ns		70ns		80ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	50		60		70		80		ns
Address Access Time	TAVQV		50		60		70		80	ns
Chip Enable Access Time	TELQV		50		60		70		80	ns
Chip Enable to Output in Low Z (1)	TELQX	30		30		30		30		ns
Output Enable to Output Valid	TGLQV		40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		25		25		25		30	ns
Output Enable to Output in High Z (1)	TGHQZ		25		25		25		30	ns
Output Hold from Address Change	TAVQX	10		10		10		10		ns

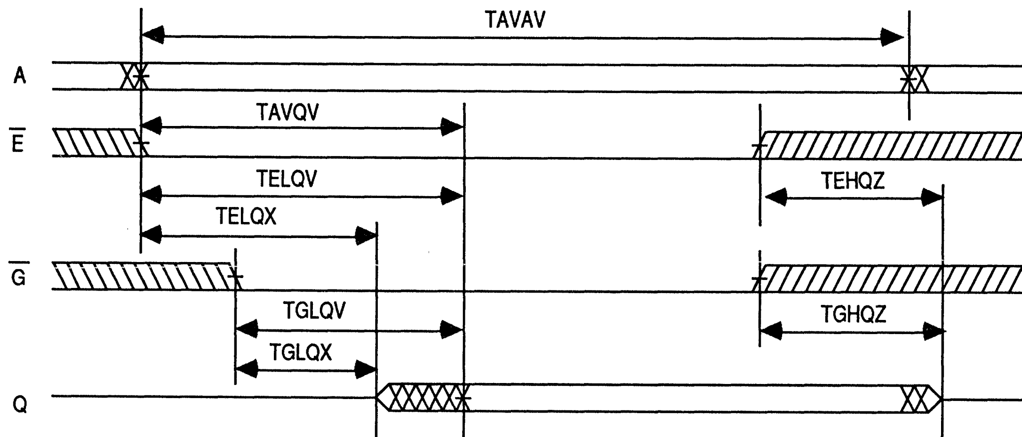
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

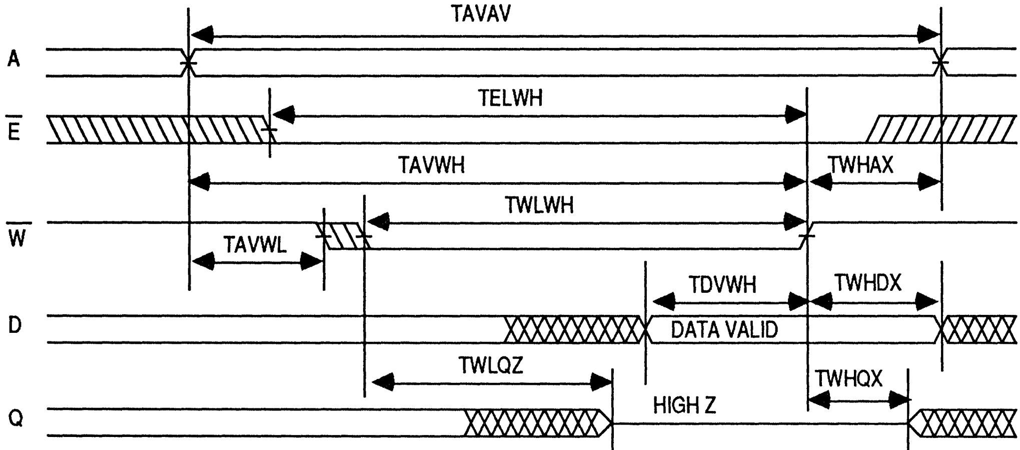
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		80		ns
Chip Enable to	TELWH	$\overline{W}$	45		55		60		70		ns
End of Write	TWLEH	$\overline{E}$	45		55		60		70		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	45		55		60		70		ns
End of Write	TAVEH	$\overline{E}$	45		55		60		70		ns
Write Pulse Width	TWLWH	$\overline{W}$	40		50		55		60		ns
	TELEH	$\overline{E}$	40		50		55		60		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	25	0	30	0	35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

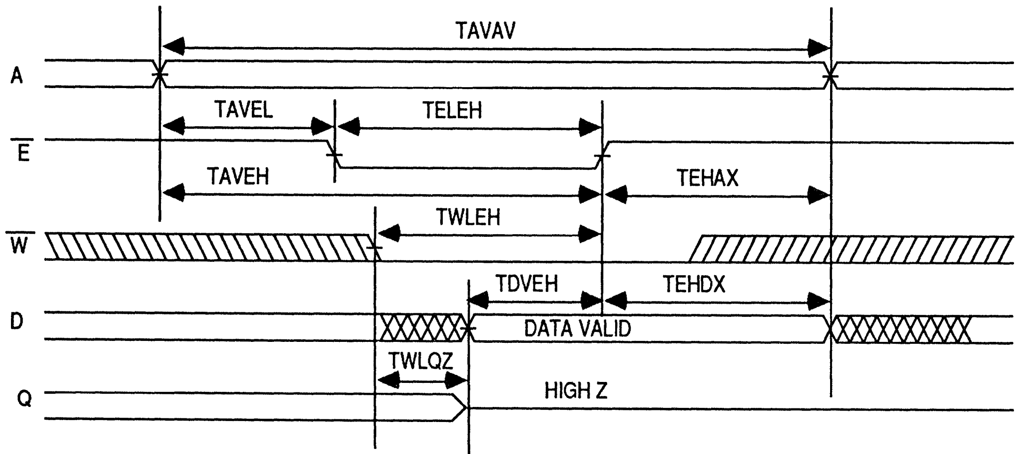
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



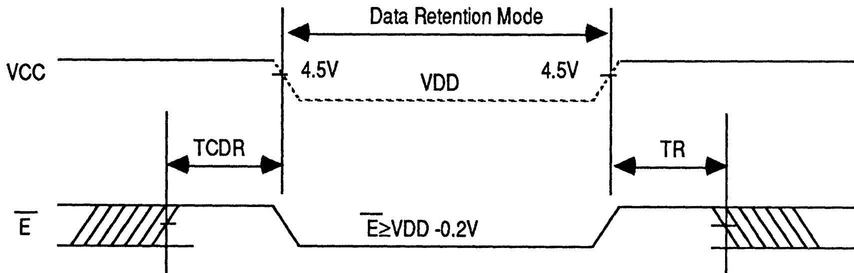
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	--	300	1200	µA
Chip to Data Retention Time	TCDR	VIN ≥VDD-0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled



64Kx8 Static RAM CMOS, Module

The EDI8M864C is a 512K bit CMOS Static RAM based on two 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The EDI8M864C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and out puts are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M864C requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

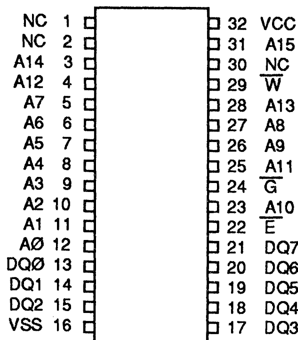
Features

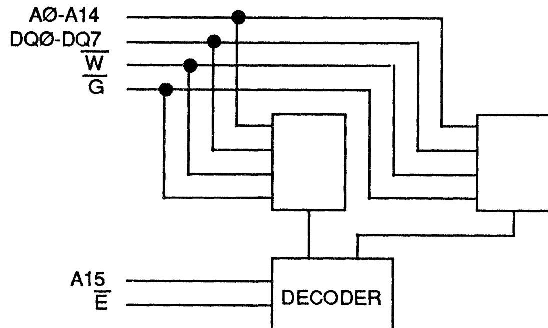
64Kx8 bit CMOS Static Random Access Memory
- Access Times 90, 100, 120, and 150ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial .... 0°C to +70°C
Military.....................................-55°C to +125°C
Storage Temperature (Ambient/Ceramic) . -65°C to +150°C
Power Dissipation .... 1 Watt
Output Current. ....20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ....VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ....1TTL, CL =100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55° to + 125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	70	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH	--	5	15	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	0.5	1.5	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH= -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

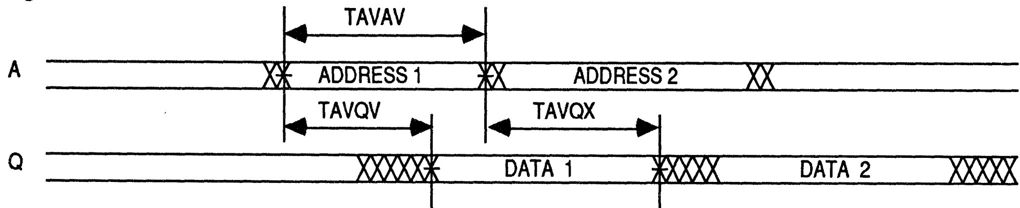
AC Characteristics
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

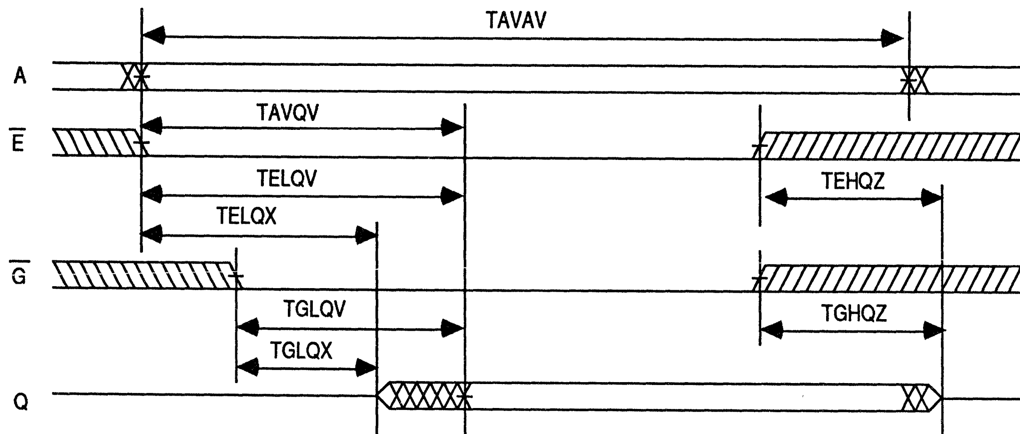
Parameter	Symbol	90ns		100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	90		100		120		150		ns
Address Access Time	TAVQV		90		100		120		150	ns
Chip Enable Access Time	TELQV		90		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	30		30		30		30		ns
Output Enable to Output Valid	TGLQV		50		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		30		30		40		50	ns
Output Enable to Output in High Z(1)	TGHQZ		30		30		40		50	ns
Output Hold from Address Change	TAVQX	10		10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W̄ High; Ḡ, Ē Low



Read Cycle 2
W̄ High



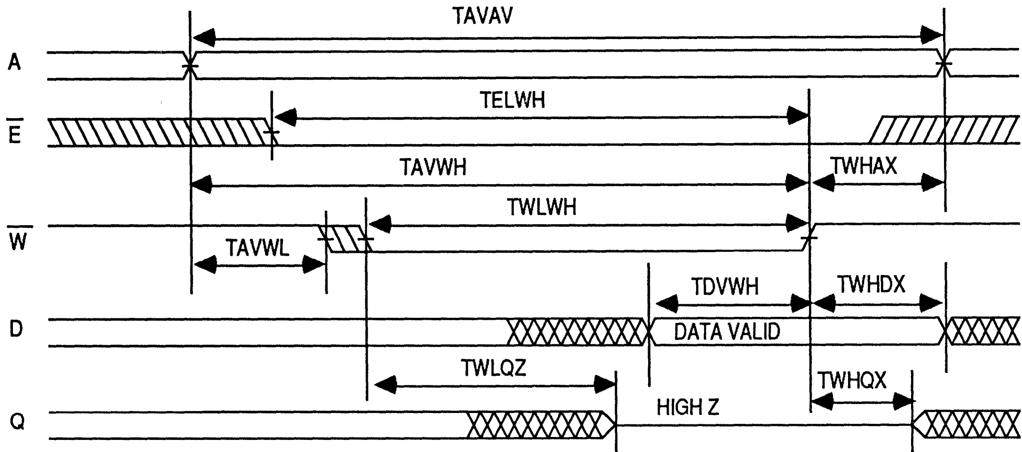
AC Characteristics
Write Cycle

(TA = 0°C to +70°C or -55C to +125°C; VCC = 5.0V ±10%)

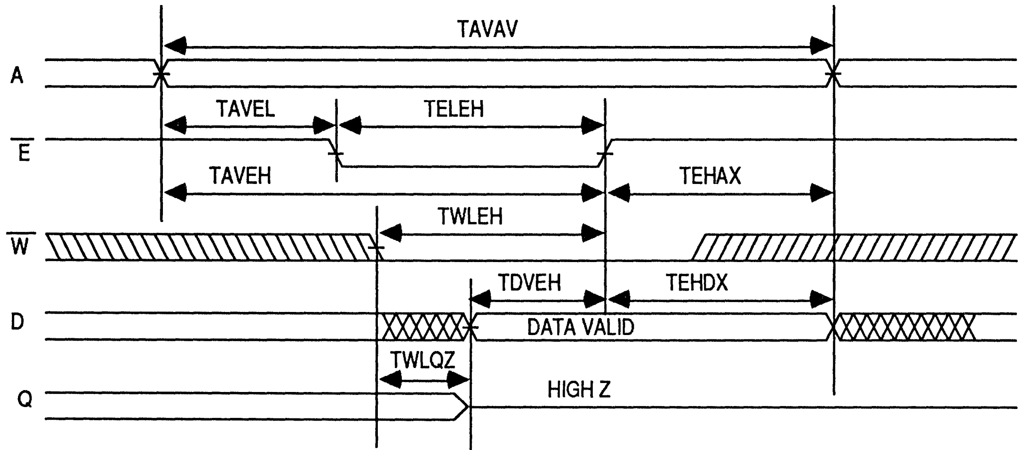
Parameter	Symbol		90ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		90		100		120		150		ns
Chip Enable to End of Write	TELWH	$\overline{W}$	80		80		90		110		ns
	TWLEH	$\overline{E}$	80		80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to End of Write	TAVWH	$\overline{W}$	80		80		90		110		ns
	TAVEH	$\overline{E}$	80		80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	60		60		70		80		ns
	TELEH	$\overline{E}$	60		60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	20		20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	20		20		20		20		ns
Write to Output in High Z (1)	TWLQZ		0	35	0	35	0	35	0	45	ns
Data to Write Time	TDVWH	$\overline{W}$	35		35		40		50		ns
	TDVEH	$\overline{E}$	35		35		40		50		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



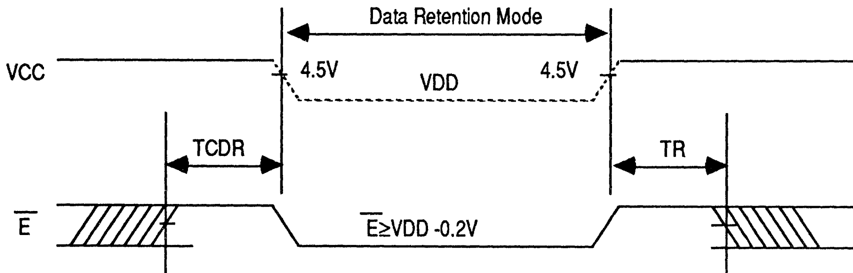
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ≥ VDD -0.2V	--	300	750	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥ VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤ 0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



128Kx8 Static RAM CMOS, Module

The EDI8M8128C is a 1024K bit CMOS Static RAM based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate. The EDI8M8128C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8128C requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

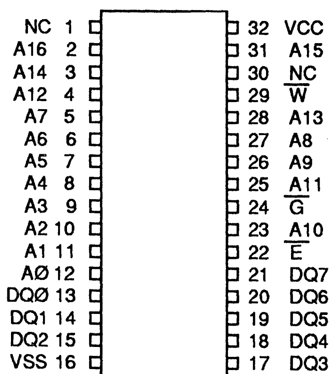
Features

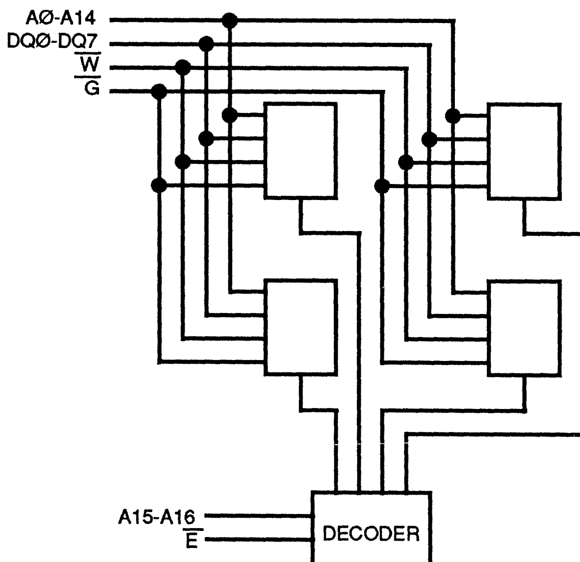
128Kx8 bit CMOS Static Random Access Memory
- Access Times 50, 60, 70, and 80ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A16	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS..................-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial................................. 0°C to +70°C
Military.....................................-55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..1 Watt
Output Current...20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels. ....VSS to 3.0V
Input Rise and Fall Times..5ns
Input and Output Timing Levels..1.5V
Output Load ....1TTL, CL = 30pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or-55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	70	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH	--	20	75	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	4	10	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

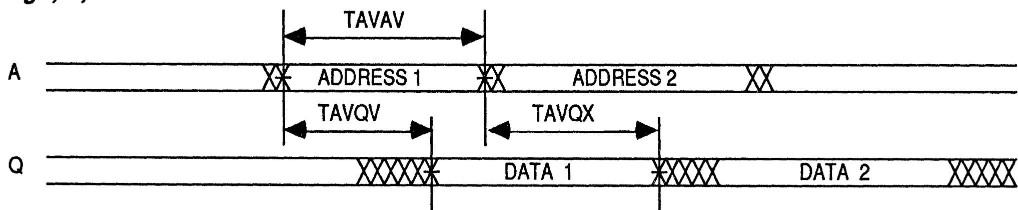
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol	50ns*		60ns		70ns		80ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	50		60		70		80		ns
Address Access Time	TAVQV		50		60		70		80	ns
Chip Enable Access Time	TELQV		50		60		70		80	ns
Chip Enable to Output in Low Z (1)	TELQX	30		30		30		30		ns
Output Enable to Output Valid	TGLQV		40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		25		25		25		30	ns
Output Enable to Output in High Z (1)	TGHQZ		25		25		25		30	ns
Output Hold from Address Change	TAVQX	10		10		10		10		ns

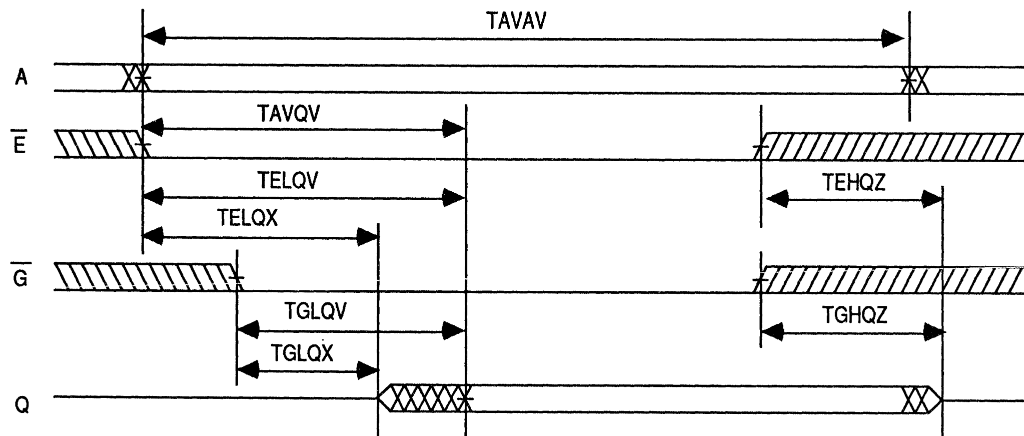
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

Read Cycle 1
W High; G, E Low



Read Cycle 2
W High



AC Characteristics
Write Cycle

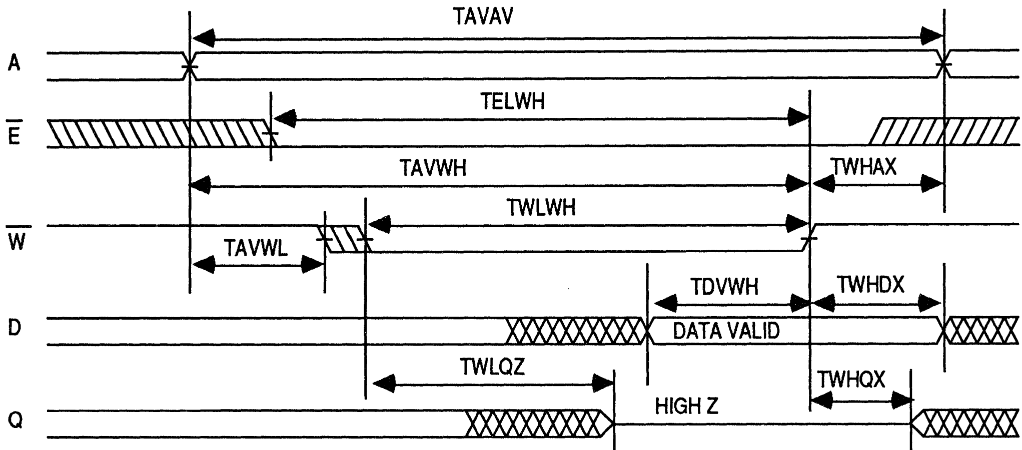
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		80		ns
Chip Enable to	TELWH	$\overline{W}$	45		55		60		70		ns
End of Write	TWLEH	$\overline{E}$	45		55		60		70		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	45		55		60		70		ns
End of Write	TAVEH	$\overline{E}$	45		55		60		70		ns
Write Pulse Width	TWLWH	$\overline{W}$	40		50		55		60		ns
	TELEH	$\overline{E}$	40		50		55		60		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	25	0	30	0	35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		ns
Output Active from 0 End of Write (1)	TWHQX				0		0		0		ns

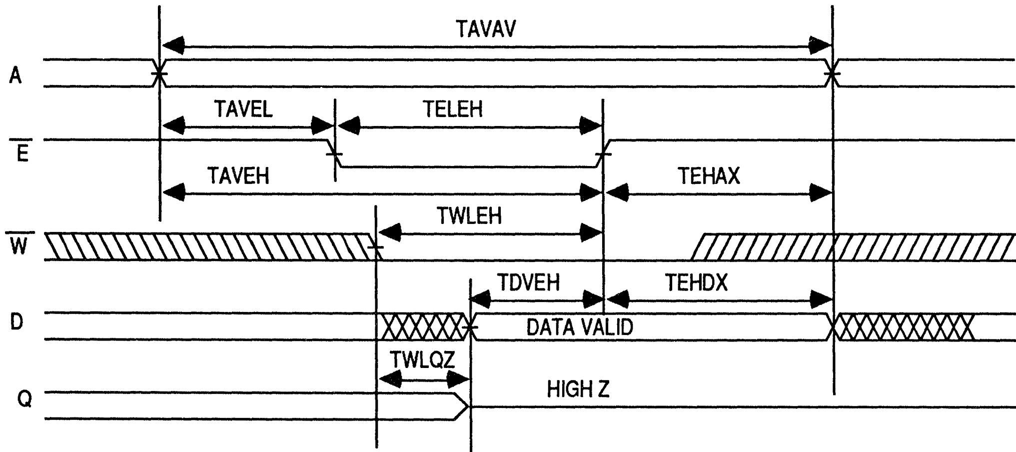
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



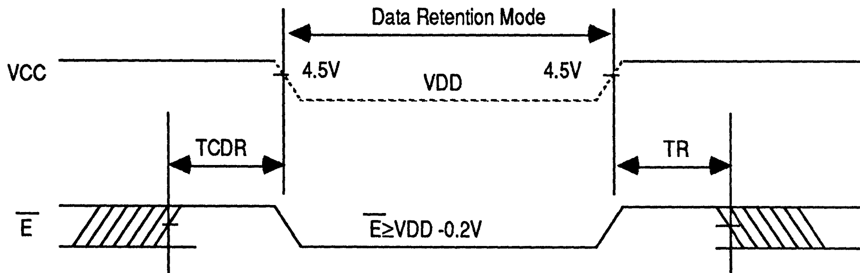
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	900	2500	μA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD-0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention
$\overline{E}$ Controlled



![EDI logo] EDI

EDI8M8128C/P90/100/120/150

High Performance Megabit SRAM Module

128Kx8 Static RAM CMOS, Module

The EDI8M8128C/P is a 1024K bit CMOS Static RAM based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The Military screened product is available in both Standard (C) and Low Power (P) versions.

The EDI8M8128C/P has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and out puts are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8128C/P requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

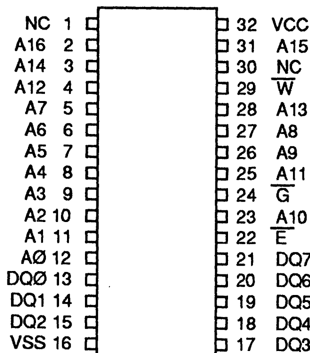
Features

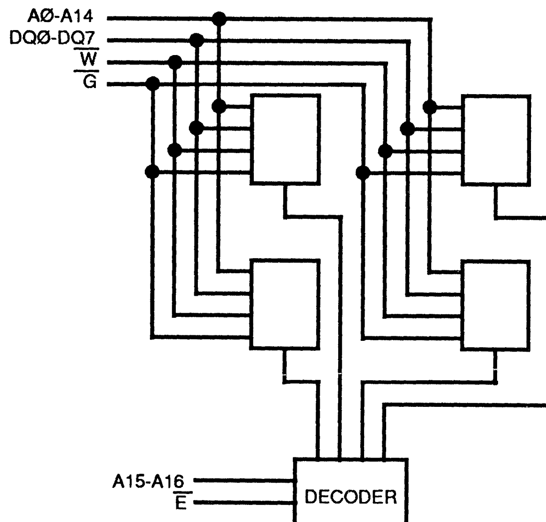
128Kx8 bit CMOS Static Random Access Memory
- Access Times 90, 100, 120, and 150ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A16	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

*Absolute Maximum Ratings**

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ....0°C to +70°C
Military ....-55°C to +125°C
Storage Temperature(Ambient/Ceramic) ..-65°C to +150°C
Power Dissipation ....1 Watt
Output Current. ....20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ....VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ....1TTL, CL =100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to + 125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		--	70	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH		--	10	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	C	--	1	3	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	P	--	50	900	µA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

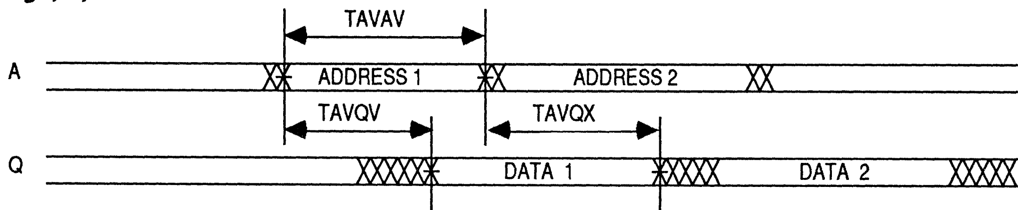
AC Characteristics
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

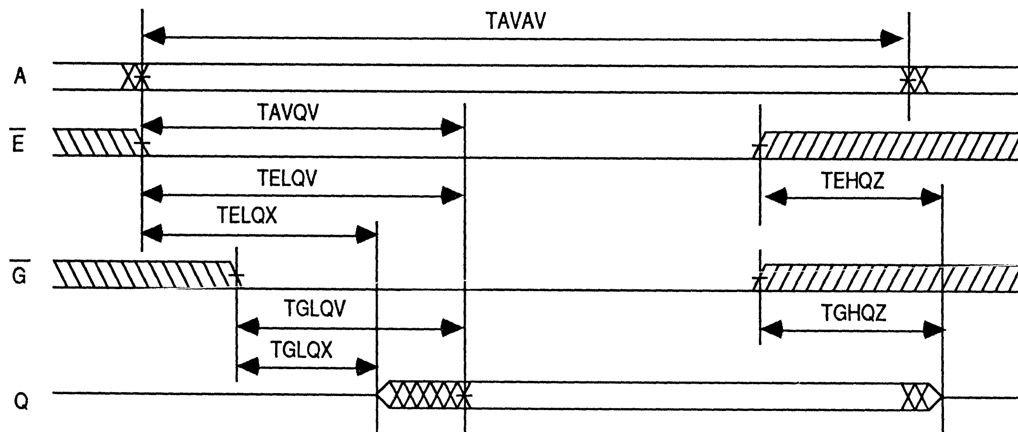
Parameter	Symbol	90ns		100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	90		100		120		150		ns
Address Access Time	TAVQV		90		100		120		150	ns
Chip Enable Access Time	TELQV		90		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	30		30		30		30		ns
Output Enable to Output Valid	TGLQV		50		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		30		30		40		50	ns
Output Enable to Output in High Z(1)	TGHQZ		30		30		40		50	ns
Output Hold from Address Change	TAVQX	10		10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High; G, E Low



Read Cycle 2
W High



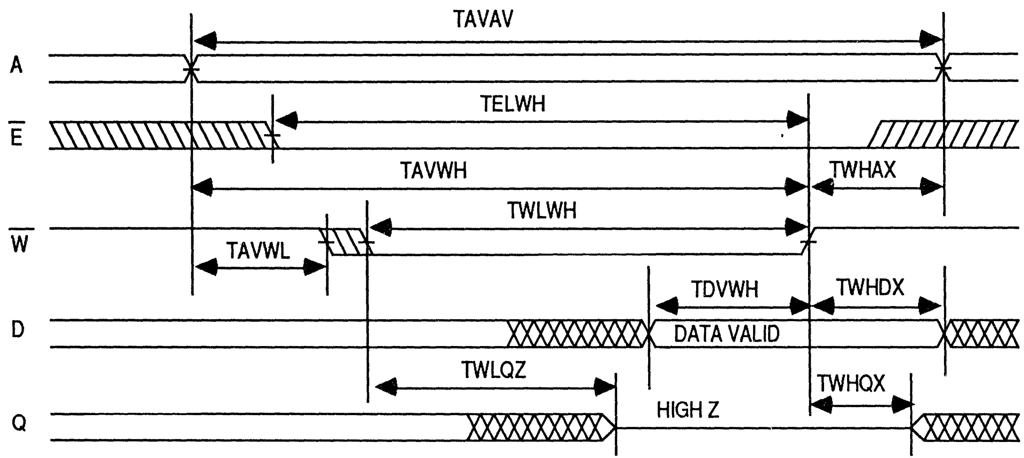
AC Characteristics
Write Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

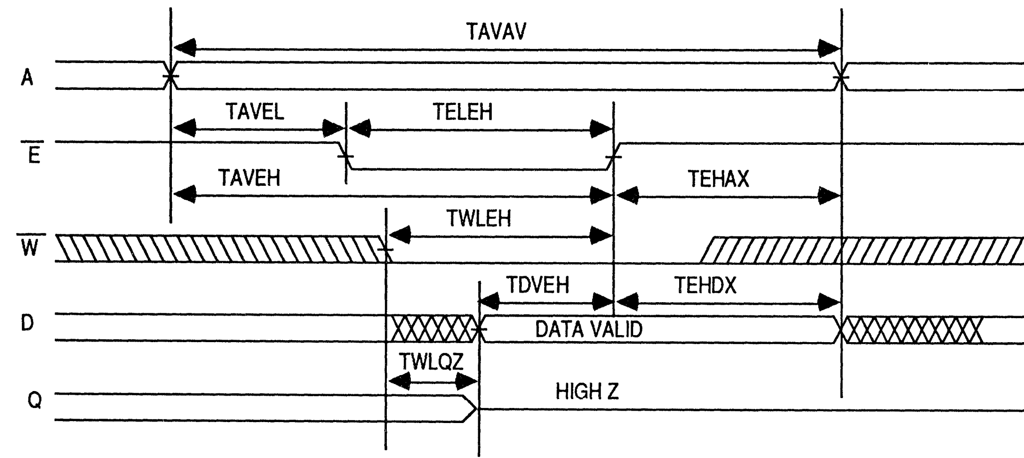
Parameter	Symbol		90ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		90		100		120		150		ns
Chip Enable to	TELWH	$\overline{W}$	80		80		90		110		ns
End of Write	TWLEH	$\overline{E}$	80		80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	80		80		90		110		ns
End of Write	TAVEH	$\overline{E}$	80		80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	60		60		70		80		ns
	TELEH	$\overline{E}$	60		60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	20		20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	20		20		20		20		ns
Write to Output in High Z (1)	TWLQZ		0	35	0	35	0	35	0	45	ns
Data to Write Time	TDVWH	$\overline{W}$	35		35		40		50		ns
	TDVEH	$\overline{E}$	35		35		40		50		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



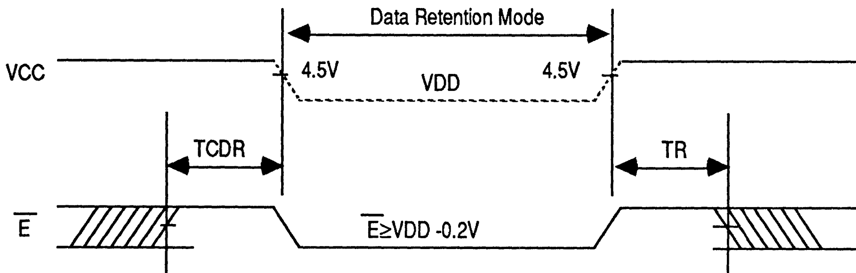
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min		Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2		--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ≥ VDD -0.2V	C	--	500	1500	µA
		VIN ≥VDD -0.2V	P	--	100	500	µA
Chip Disable to Data Retention Time	TCDR	or VIN ≤0.2V	0		--	--	ns
Operation Recovery Time	TR		TAVAV*		--	--	ns

*Read Cycle Time

Data Retention
$\overline{E}$ Controlled



128Kx8 Static RAM CMOS, Module

The EDI8M8128C is a 1024K bit CMOS Static RAM based on four 32Kx8 Static RAMs in economical plastic small outline packages (SOP) mounted on a multi-layered ceramic substrate.

The EDI8M8128C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and out puts are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8128C requires no clocks or refreshing for operation.

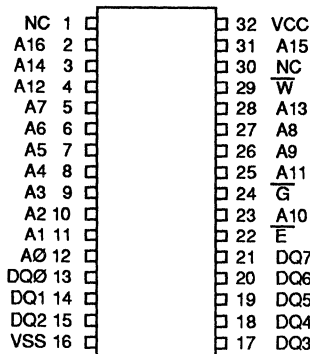
Features

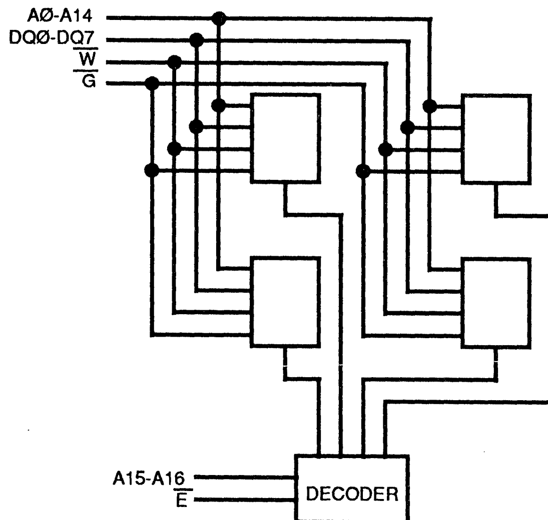
128Kx8 bit CMOS Static Random Access Memory
- Access Times 100, 120, and 150ns
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A16	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ....0°C to +70°C
Storage Temperature (Ambient/Ceramic).-65°C to +150°C
Power Dissipation ....1 Watt
Output Current. ....20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ....VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels...1.5V
Output Load ....1TTL, CL =100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	70	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH	--	10	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

These parameters are sampled, not 100% tested.

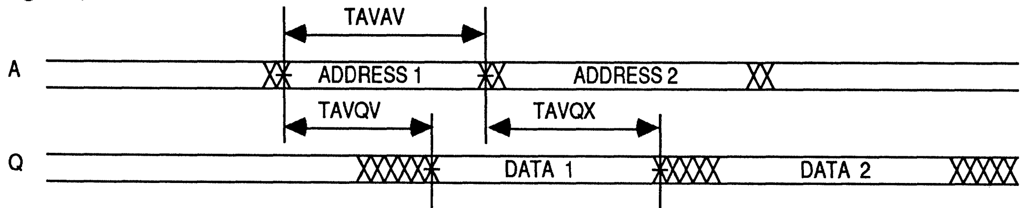
AC Characteristics
Read Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

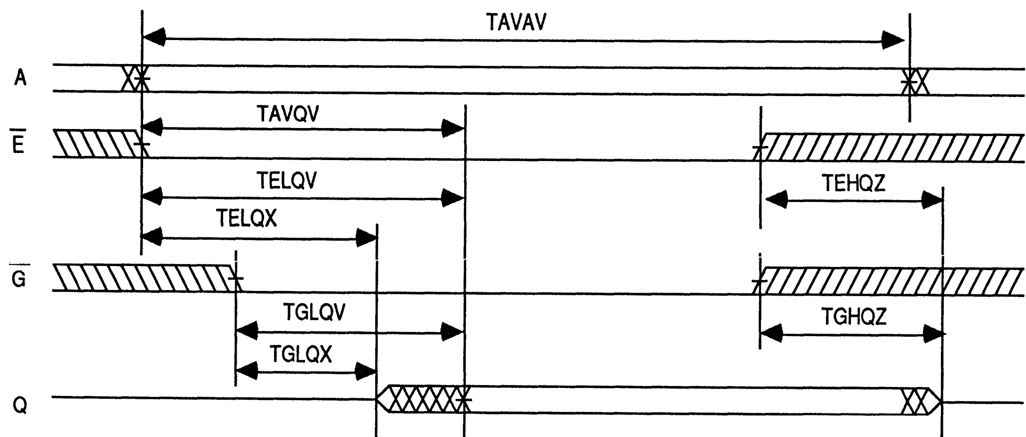
Parameter	Symbol	100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	100		120		150		ns
Address Access Time	TAVQV		100		120		150	ns
Chip Enable Access Time	TELQV		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	30		30		30		ns
Output Enable to Output Valid	TGLQV		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		30		40		50	ns
Output Enable to Output in High Z(1)	TGHQZ		30		40		50	ns
Output Hold from Address Change	TAVQX	10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High; G, E Low



Read Cycle 2
W High



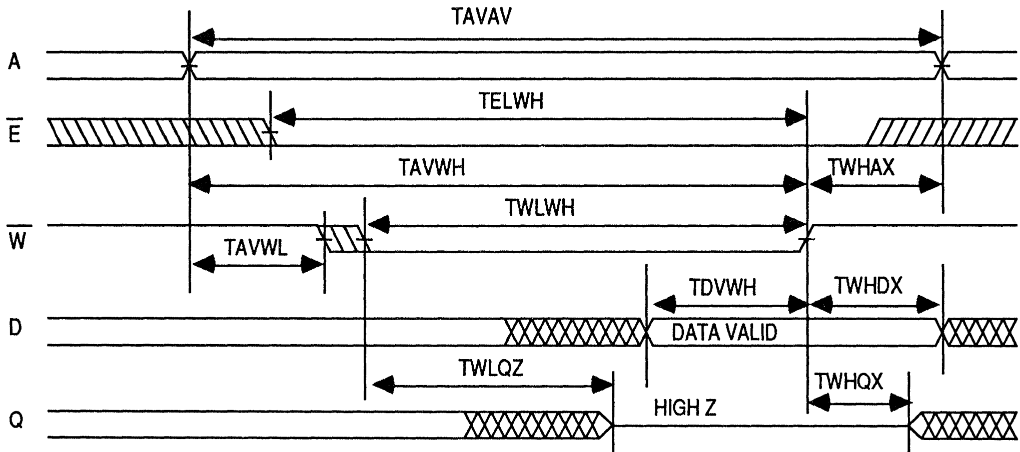
AC Characteristics
Write Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

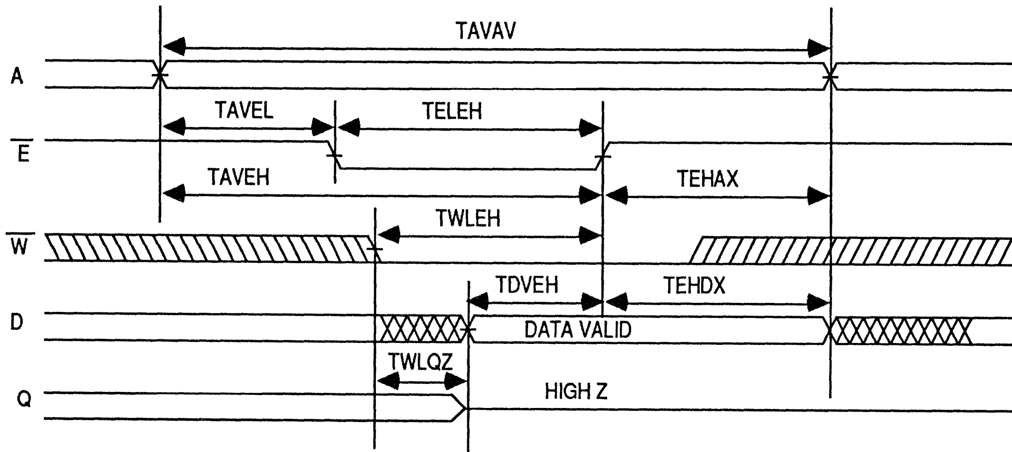
Parameter	Symbol		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		100		120		150		ns
Chip Enable to	TELWH	$\overline{W}$	80		90		110		ns
End of Write	TWLEH	$\overline{E}$	80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	80		90		110		ns
End of Write	TAVEH	$\overline{E}$	80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	60		70		80		ns
	TELEH	$\overline{E}$	60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		ns
	TEHAX	$\overline{E}$	20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	20		20		20		ns
Write to Output in High Z (1)	TWLQZ		0	35	0	35	0	45	ns
Data to Write Time	TDVWH	$\overline{W}$	35		40		50		ns
	TDVEH	$\overline{E}$	35		40		50		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



128Kx8 Static RAM CMOS, Module

The EDI8M8130C is a 1024K bit CMOS Static RAM Module based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The EDI8M8130C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. The E̅ and S lines perform the chip enable functions that automatically power down the device when proper logic levels are applied.

All inputs and outputs are TTL compatible and operate from a 5V supply. Fully asynchronous, the EDI8M8130C requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

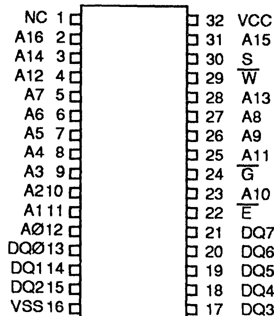
Features

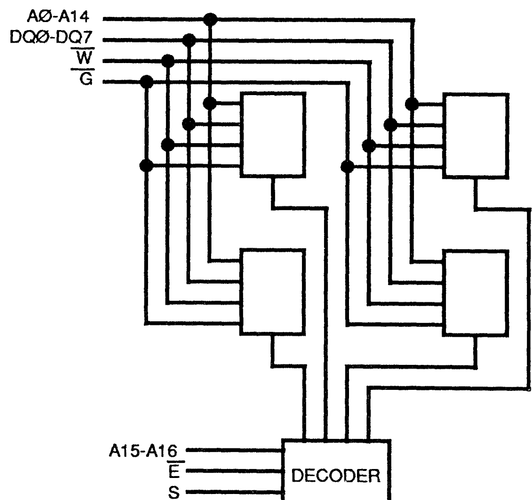
128Kx8 bit CMOS Static Random Access Memory
- Access Times 50, 60, 70, and 80ns
- E̅, S, and G̅ Functions for Bus Control
- Data Retention Function
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Ceramic Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A16	Address Inputs
E̅	Chip Enable
S	Chip Select
W̅	Write Enable
G̅	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial .... 0°C to +70°C
Military .... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation .... 1 Watt
Output Current. .... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels .... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load. .... 1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle S = VIH, Min Cycle	--	70	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or S ≤ VIL	--	20	75	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V or S ≤ 0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	4	10	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC; $\overline{E}$, $\overline{G}$ = VIH or S = VIL	--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$, S)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

Note: These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

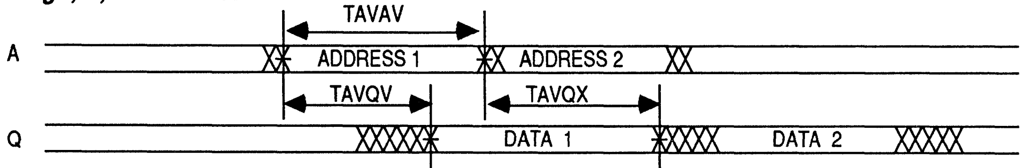
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		50		60		70		80		ns
Address Access Time	TAVQV			50		60		70		80	ns
Chip Enable Access Time	TELQV	$\overline{E}$		50		60		70		80	ns
	TSHQV	S		50		60		70		80	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$	30		30		30		30		ns
	TSHQX	S	30		30		30		30		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$		25		25		25		30	ns
	TSLQZ	S		25		25		25		30	ns
Output Hold from Address Change	TAVQX		10		10		10		10		ns
Output Enable to Output Valid	TGLQV			40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		10		10		ns
Output Disable to Output in High Z (1)	TGHQZ			25		25		25		30	ns

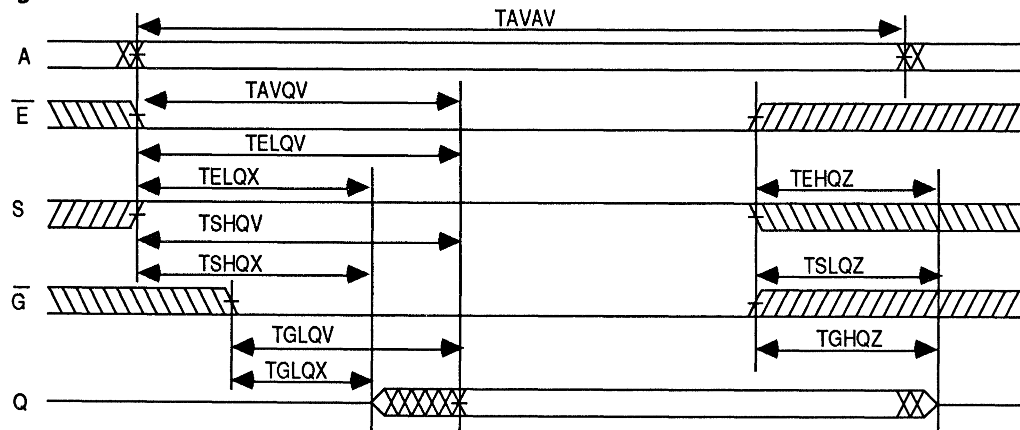
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

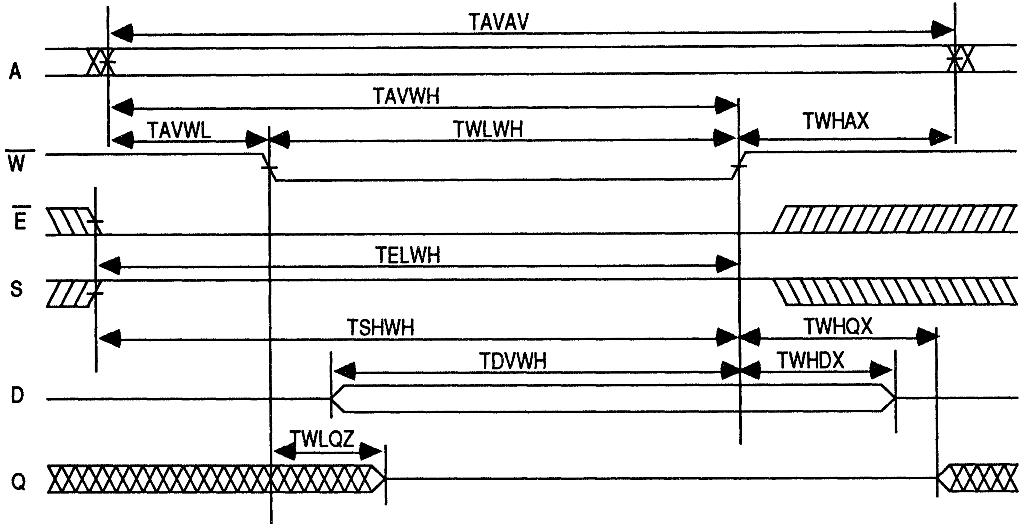
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		80		ns
Chip Enable to	TELWH	$\overline{E}$	45		55		60		70		ns
End of Write	TSHWH	S	45		55		60		70		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
	TAVSH	S	0		0		0		0		ns
Address Valid to End of Write	TAVWH		45		55		60		70		ns
Write Pulse Width	TWLWH	$\overline{W}$	40		50		55		60		ns
	TELEH	$\overline{E}$	40		50		55		60		ns
	TSHSL	S	40		50		55		60		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
	TSLAX	S	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
	TSLDX	S	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ			25		25		30		35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		ns
	TDVSL	S	25		25		30		35		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

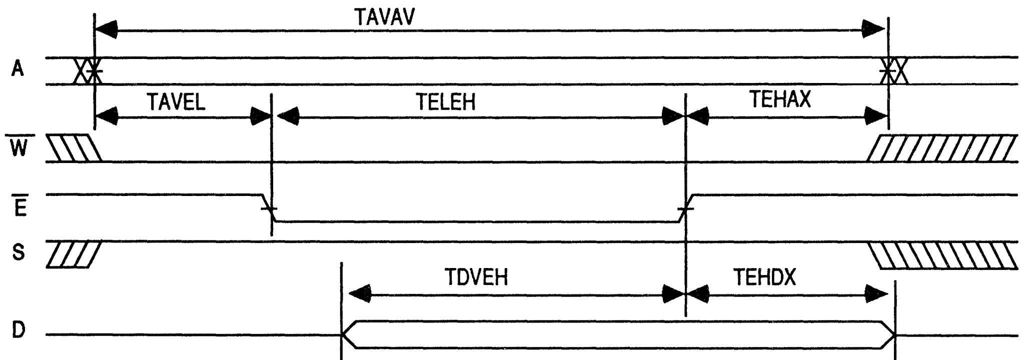
Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

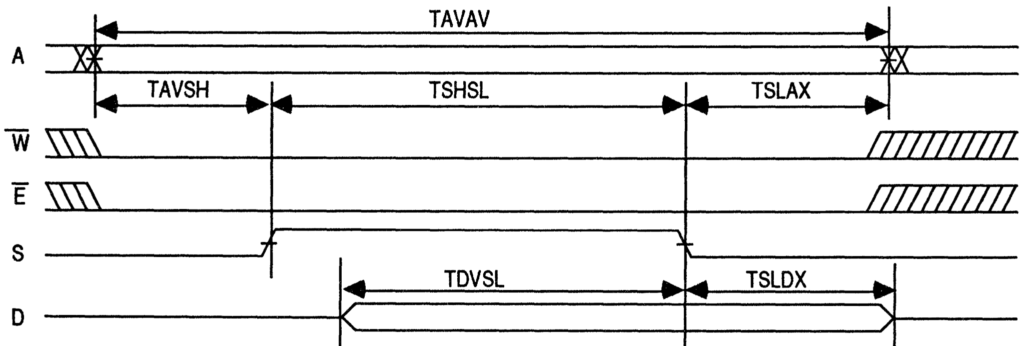
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



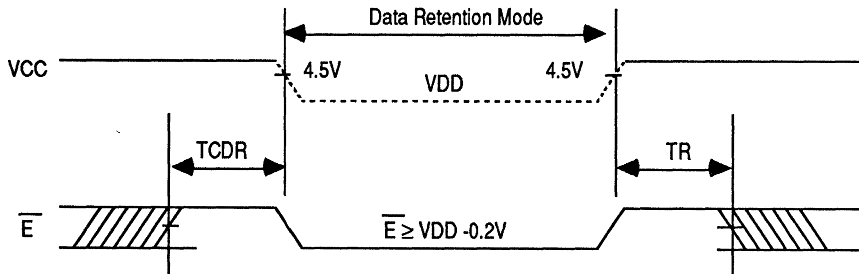
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

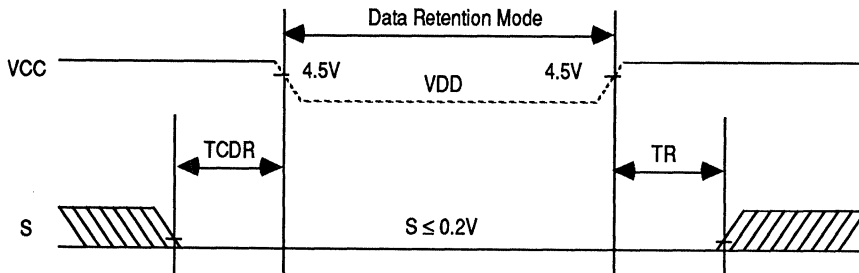
Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V; S ≤ 0.2V	--	900	2500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled



Data Retention S Controlled



128Kx8 Static RAM CMOS, Module

The EDI8M8130C/P is a 1024K bit CMOS Static RAM Module based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The Military screened product is available in both Standard (C) and Low Power (P) versions.

The EDI8M8130C/P has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. The $\overline{E}$ and S lines perform the chip enable functions that automatically power down the device when proper logic levels are applied.

All inputs and outputs are TTL compatible and operate from a 5V supply. Fully asynchronous, the EDI8M8130C/P requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

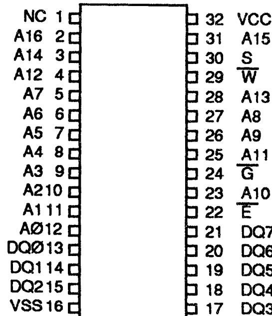
Features

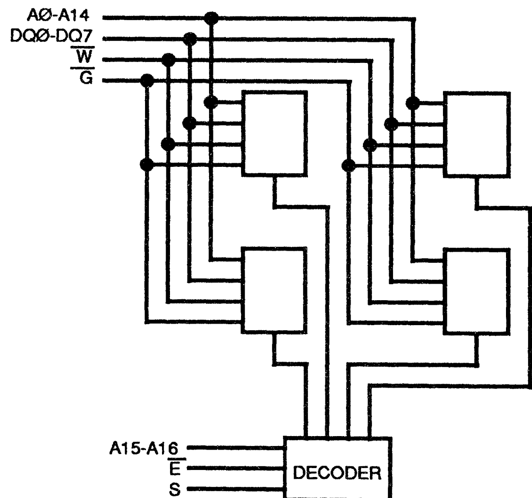
128Kx8 bit CMOS Static Random Access Memory
- Access Times 90, 100, 120 and 150ns
- $\overline{E}$, S, and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Jedec Approved Pinout
- 32 Pin Ceramic Dual-in-line Package

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A16	Address Inputs
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial .... 0°C to +70°C
Military .... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation .... 1 Watt
Output Current. .... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels .... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load. .... 1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle S = VIH, Min Cycle		--	70	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or S ≤ VIL		--	10	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V or S ≤ 0.2V	C	--	1	3	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	P	--	50	900	µA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC; $\overline{E}$, $\overline{G}$ = VIH or S = VIL		--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}$, S)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

Note: These parameters are sampled, not 100% tested.

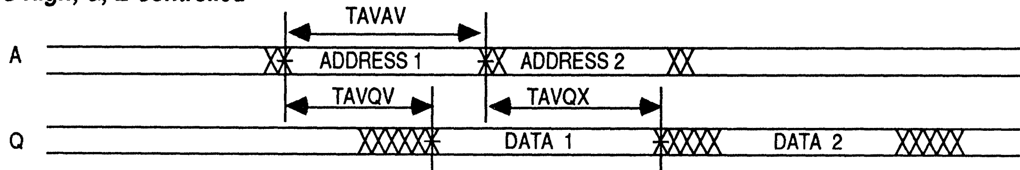
AC Characteristics
Read Cycle

(TA =0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

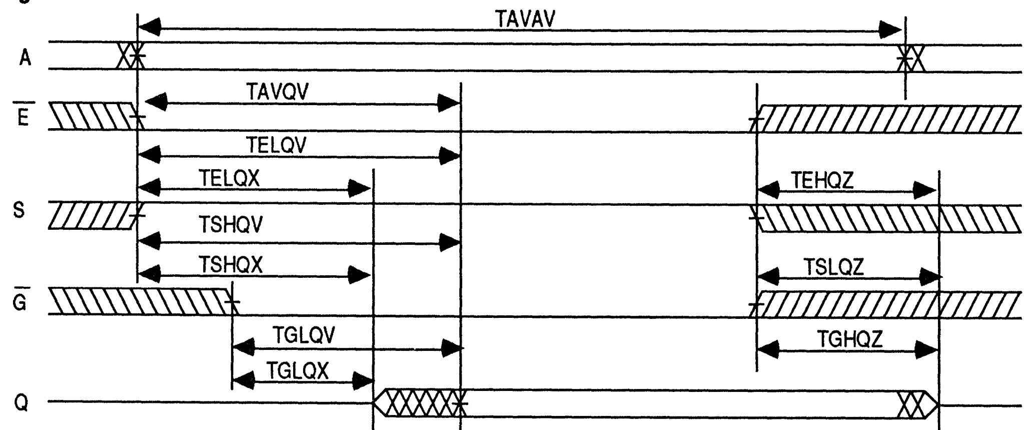
Parameter	Symbol		90ns Min	90ns Max	100ns Min	100ns Max	120ns Min	120ns Max	150ns Min	150ns Max	Units
Read Cycle Time	TAVAV		90		100		120		150		ns
Address Access Time	TAVQV			90		100		120		150	ns
Chip Enable Access Time	TELQV	$\overline{E}$		90		100		120		150	ns
	TSHQV	S		90		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$	30		30		30		30		ns
	TSHQX	S	30		30		30		30		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$		30		30		40		50	ns
	TSLQZ	S		30		30		40		50	ns
Output Hold from Address Change	TAVQX		10		10		10		10		ns
Output Enable to Output Valid	TGLQV			50		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		10		10		ns
Output Disable to Output in High Z (1)	TGHQZ			30		30		40		50	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High



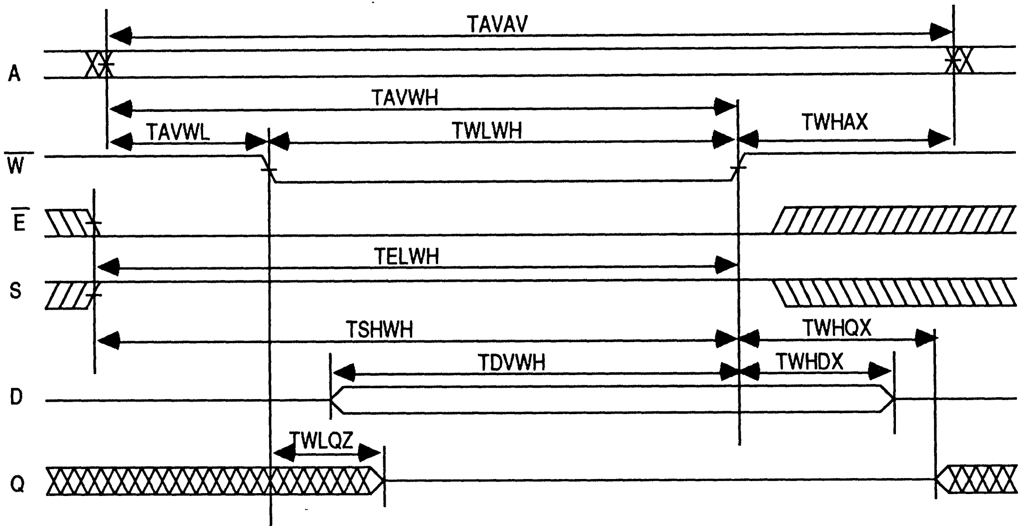
AC Characteristics
Write Cycle

(TA =0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

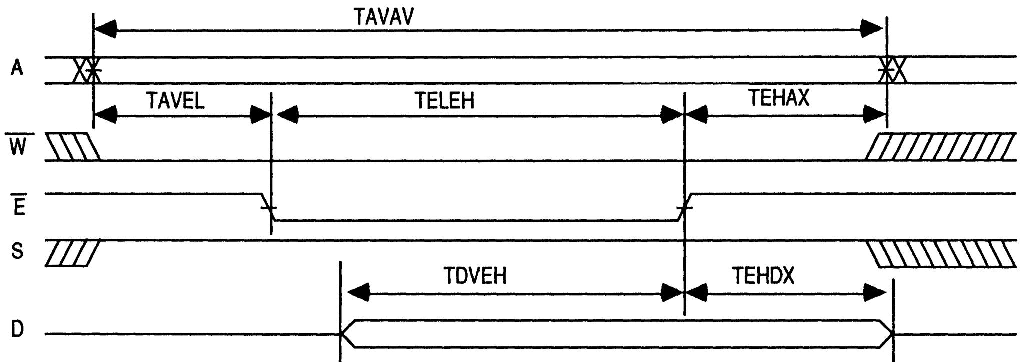
Parameter	**Symbol**		**90ns**		**100ns**		**120ns**		**150ns**		**Units**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	TAVAV		90		100		120		150		ns
Chip Enable to	TELWH	$\overline{E}$	80		80		90		110		ns
End of Write	TSHWH	S	80		80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
	TAVSH	S	0		0		0		0		ns
Address Valid to End of Write	TAVWH		80		80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	60		60		70		80		ns
	TELEH	$\overline{E}$	60		60		70		80		ns
	TSHSL	S	60		60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	20		20		20		20		ns
	TSLAX	S	20		20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	20		20		20		20		ns
	TSLDX	S	20		20		20		20		ns
Write to Output in High Z (1)	TWLQZ		0	35	0	35	0	35	0	45	ns
Data to Write Time	TDVWH	$\overline{W}$	35		35		40		50		ns
	TDVEH	$\overline{E}$	35		35		40		50		ns
	TDVSL	S	35		35		40		50		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

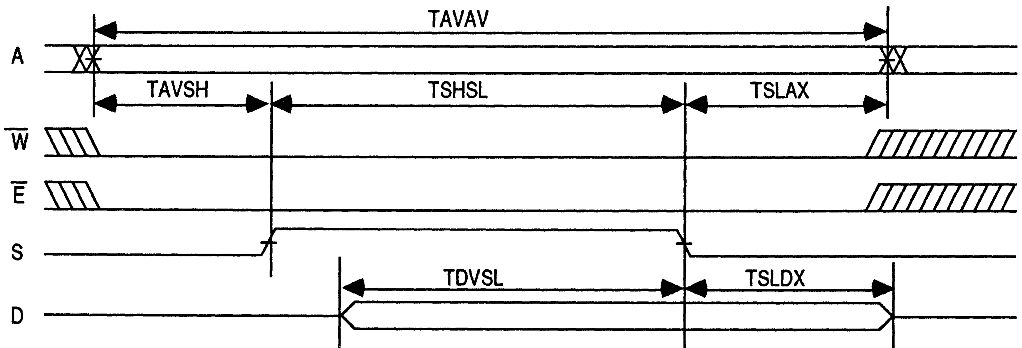
Write Cycle 1
Late Write, W̄ Controlled



Write Cycle 2
Early Write, Ē Controlled



Write Cycle 3
Early Write, S Controlled



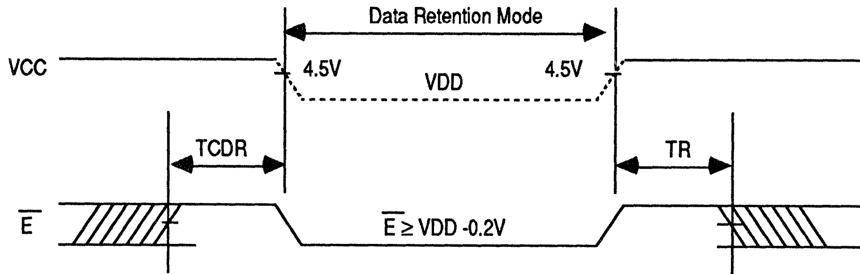
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

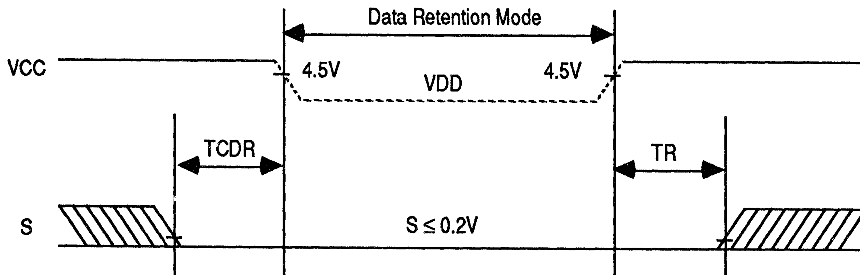
Characteristic	Sym	Test Conditions		Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V		2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ≥ VDD -0.2V	C	--	500	1500	μA
		S ≤ 0.2V	P	--	100	500	μA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V		0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V		TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled



Data Retention S Controlled



64Kx16 CMOS, High Speed Programmable, Static RAM Module

The EDH816H64C is a 1024K-bit high speed CMOS Static RAM Module consisting of sixteen (16) 64Kx1 Static RAMs in leadless chip carriers surface-mounted onto a multilayered ceramic substrate. Four Chip Select lines are provided (one for each 64Kx4 array) allowing the user to configure the memory into a 64Kx16, 128Kx8 or 256Kx4 organizations.

The EDH816H64C is available with access times as fast as 35ns. The module is a high density, 40 pin sidebrazed DIP on 900 mil centers.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Dual ground pins are provided for maximum noise immunity.

Fully asynchronous circuitry requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

Features

High Density 1024K-bit CMOS Static Random Access Memory Module
- Access Times 35, 45, 55, and 70ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Customer Configured Memory, as 64Kx16, 128Kx8 or 256Kx4

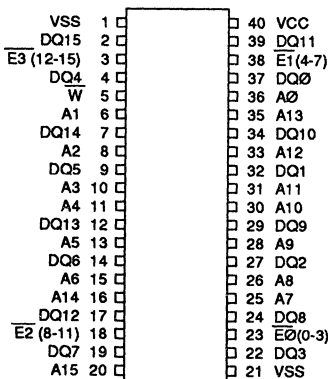
40 Pin Dual-in-line Package
- Dual Ground Pins for Maximum Noise Immunity

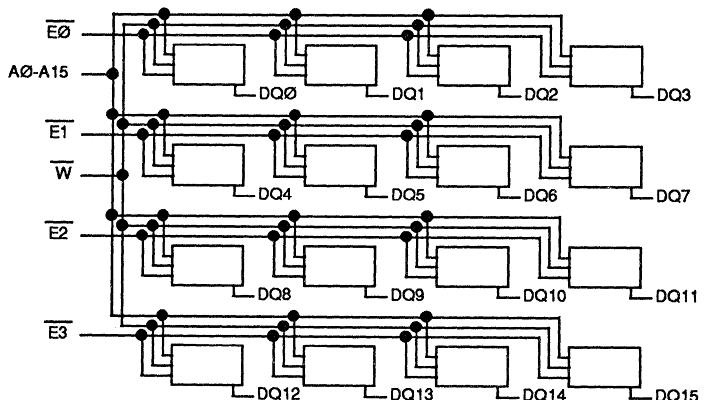
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
EØ-E3	Chip Enables
W	Write Enable
DQØ-DQ15	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial.................................. 0°C to+70°C
Military.................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 8 Watts
Output Current... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times... 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load..1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Mode	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	x16	--	1120	1380	
			x8	--	690	830	mA
			x4	--	445	555	
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	200	475	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		--	40	250	mA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	50	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	50	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Input Capacitance (Address, $\overline{W}$)	Ci	120	pF
Input Capacitance Enable Line ($\overline{E}$)	CE	40	pF
Output Capacitance	CO	12	pF

These parameters are sampled, not 100% tested.

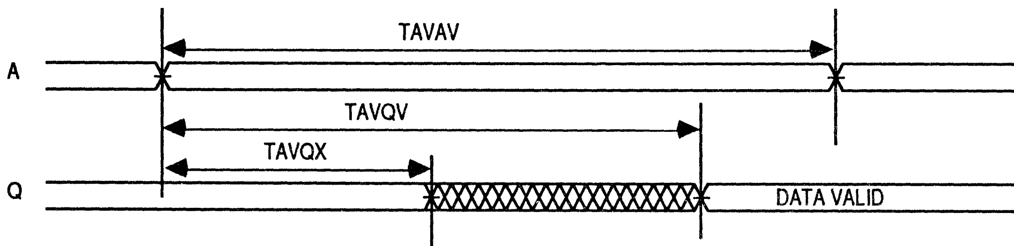
AC Characteristics
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

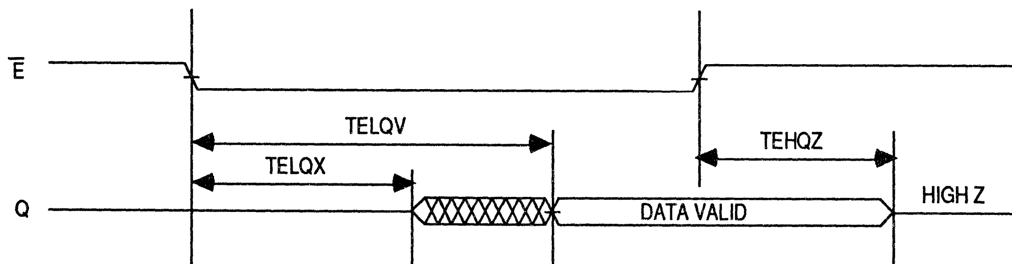
Parameter	Symbol	35ns		45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		70		ns
Address Access Time	TAVQV		35		45		55		70	ns
Chip Enable Access Time	TELQV		35		45		55		70	ns
Chip Enable to Output Low Z (1)	TELQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	25	0	30	0	30	0	30	ns
Output Hold from Address Change	TAVQX	5		5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		0		ns
Chip Disable to Power Down (1)	TPD	0	30	0	35	0	50	0	55	ns

Note 1: Parameter guaranteed, but not tested.

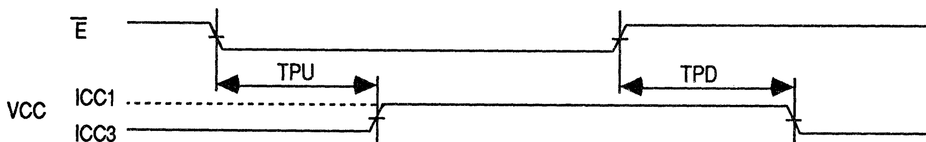
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



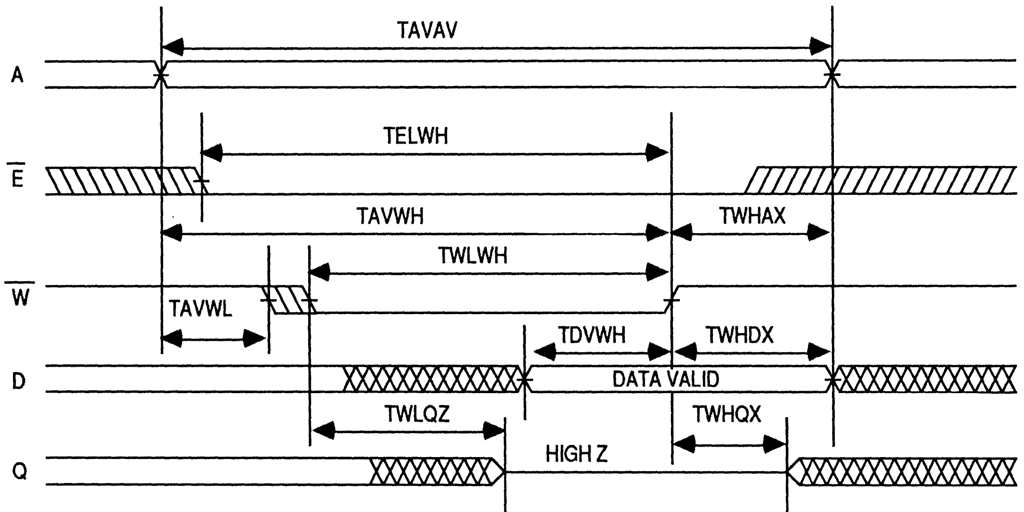
AC Characteristics
Write Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

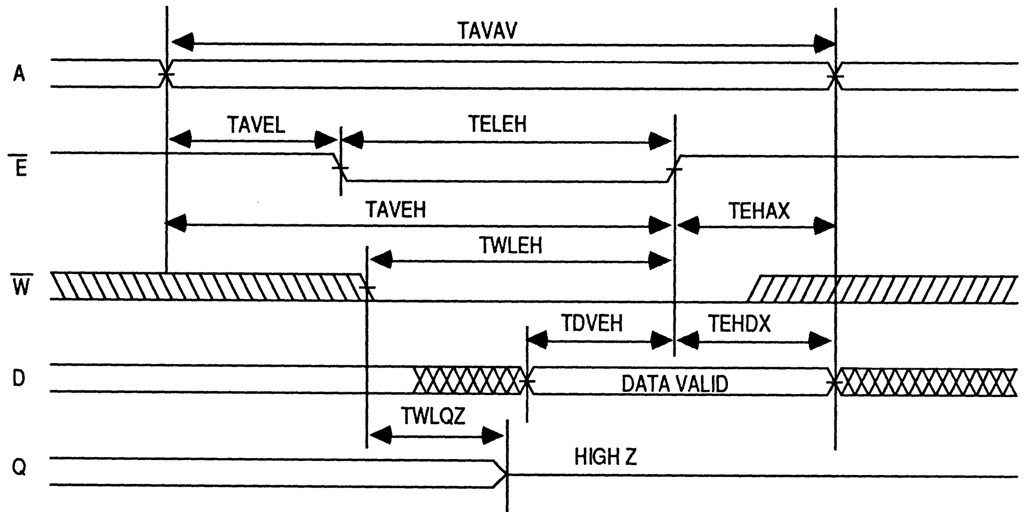
Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		70		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		65		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		65		ns
Address Setup Time	TAVWL	$\overline{W}$	10		10		10		10		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		40		50		65		ns
End of Write	TAVEH	$\overline{E}$	30		40		50		65		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		30		35		40		ns
	TELEH	$\overline{E}$	25		30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	30	0	30	0	35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		30		35		35		ns
	TDVEH	$\overline{E}$	25		30		35		35		ns
Output Active from End of Write (1)	TWHQX		0	20	0	25	0	30	0	40	ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W̄ Controlled

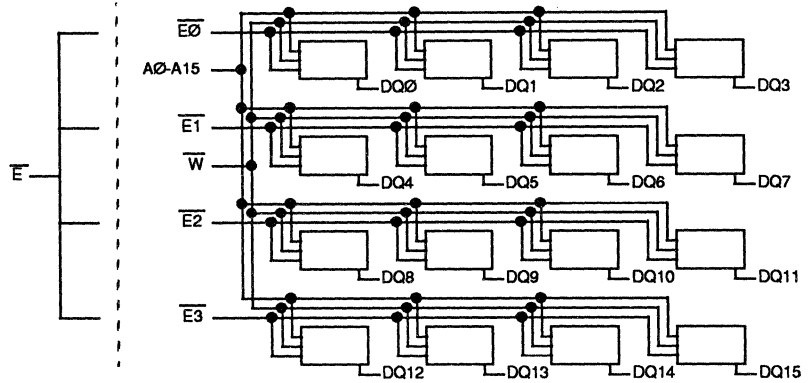


Write Cycle 2
Ē Controlled

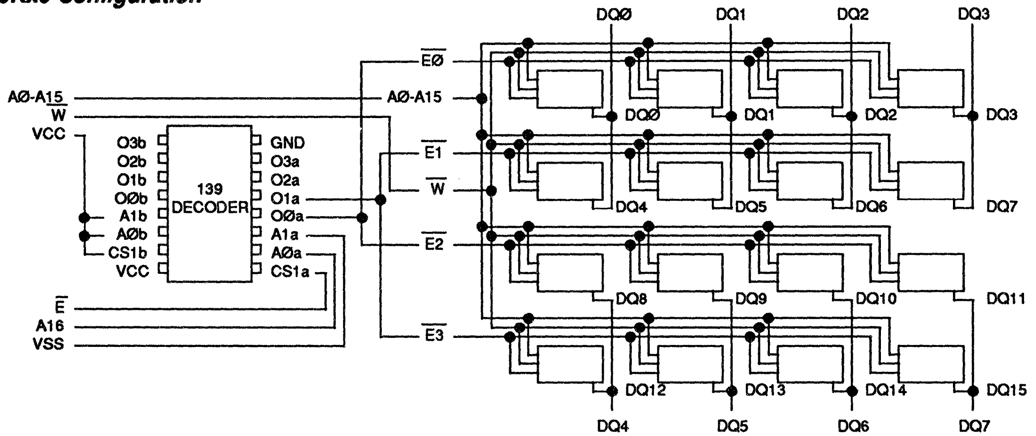


Device Configurations for 139 Decoder Applications

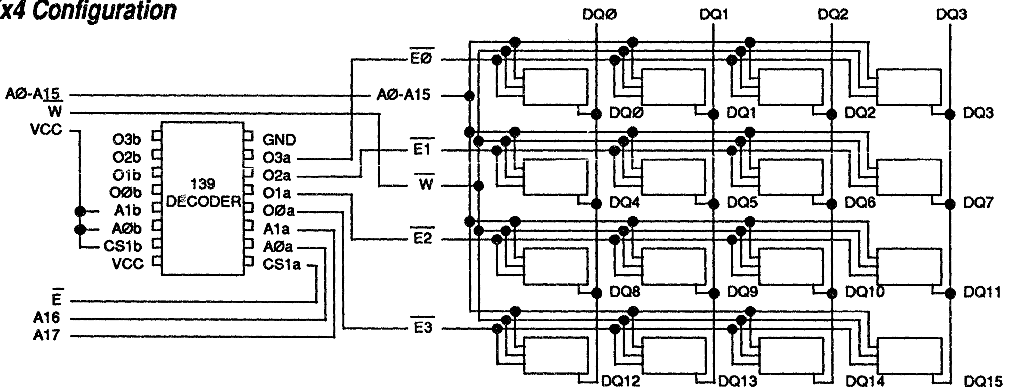
64Kx16 Configuration



128Kx8 Configuration



256Kx4 Configuration



EDI

EDI8F1664C100/120/150

Megabit SRAM Module, JEDEC Pinout

64Kx16 Static RAM CMOS, Module

The EDI8F1664C is a high speed 64Kx16 CMOS Static RAM Module. The module consists of four (4) 32Kx8 CMOS Static RAMs in plastic small outline packages, surface mounted onto an epoxy laminate (FR-4) substrate. The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to proposed monolithic megabit Static RAMs is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using LB and UB as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

EDI uses surface mount technology to produce high density modules which provide a cost effective solution for systems with minimal board spacing.

The EDI8F1664C is available with access times as fast as 100ns. All outputs and inputs are TTL-compatible and operate from a +5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

Features

64Kx16 bit CMOS Static Random Access Memory Module
- Access Times 100, 120, and 150ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible

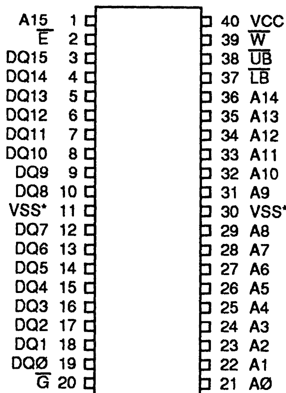
Jedec Approved Pinout
- 40 Pin Dual-in-line Package

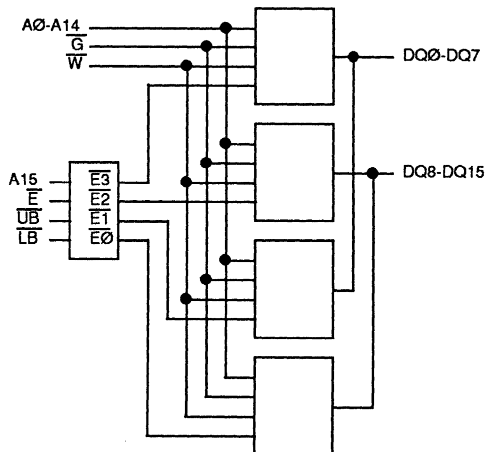
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ15	Data Input/Output
UB	Upper Byte Control
LB	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





*Note: Both ground pins (VSS) need to be grounded for proper operations.

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial.............................. 0°C to +70°C.
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..4 Watts
Output Current... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels.. VSS to 3.0V
Input Rise and Fall Times.. 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load.: 1TTL, CL = 100pF
(Note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, II/O = 0mA, Min Cycle	--	170	195	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{W}$, $\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; II/O = 0mA, Min Cycle	--	115	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or $\overline{LB}$ & $\overline{UB}$ ≥ VIH	--	50	75	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V or $\overline{LB}$ & $\overline{UB}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	UB Write	DIN(8-15)	ICC1
L	H	L	L	X	LB Write	DIN(0-7)	ICC1
L	L	L	L	X	Standby	DIN(0-15)	ICC1
L	L	H	H	L	Standby	DOUT(8-15)	ICC1
L	H	L	H	L	Standby	DOUT(0-7)	ICC1
L	L	L	H	L	Standby	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	G,A	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	30	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	30	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	50	pF

These parameters are sampled, not 100% tested.

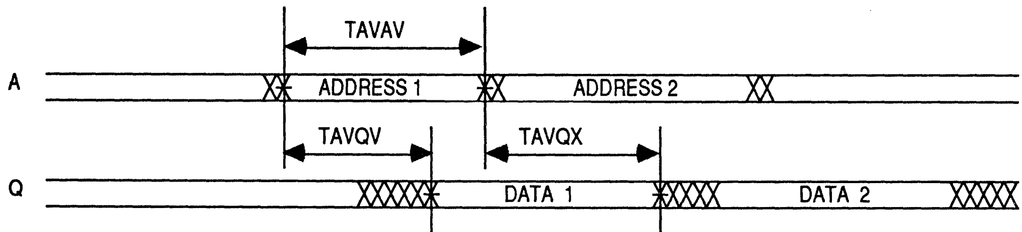
AC Characteristics
Read Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

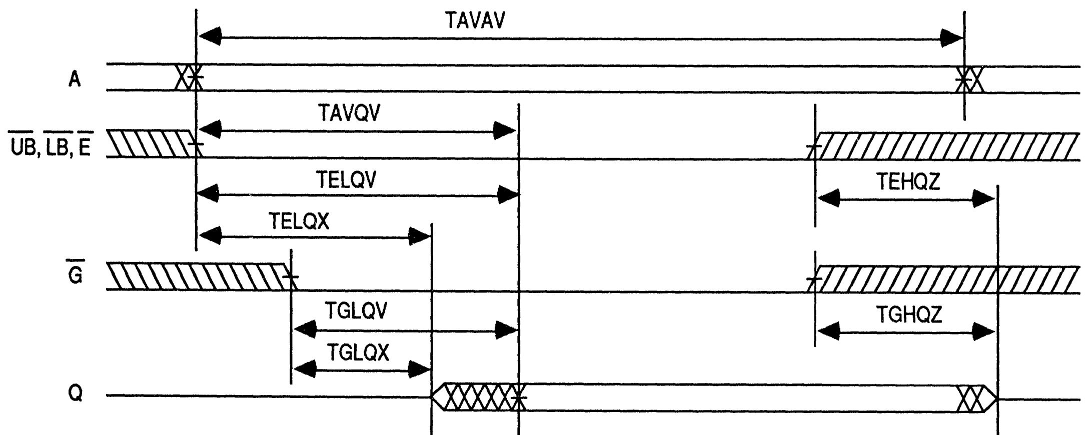
Parameter	Symbol			100ns		120ns		150ns		Units
				Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV			100		120		150		ns
Address Access Time	TAVQV				100		120		150	ns
Chip EnableAccess Time	TELQV	$\overline{E}$			100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$		30		30		30		ns
Output Enable to Output Valid	TGLQV				50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX			10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ	$\overline{E}$			30		40		50	ns
Output Enable to Output in High Z (1)	TGHQZ				30		40		50	ns
Output Hold from Address Change	TAVQX			10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



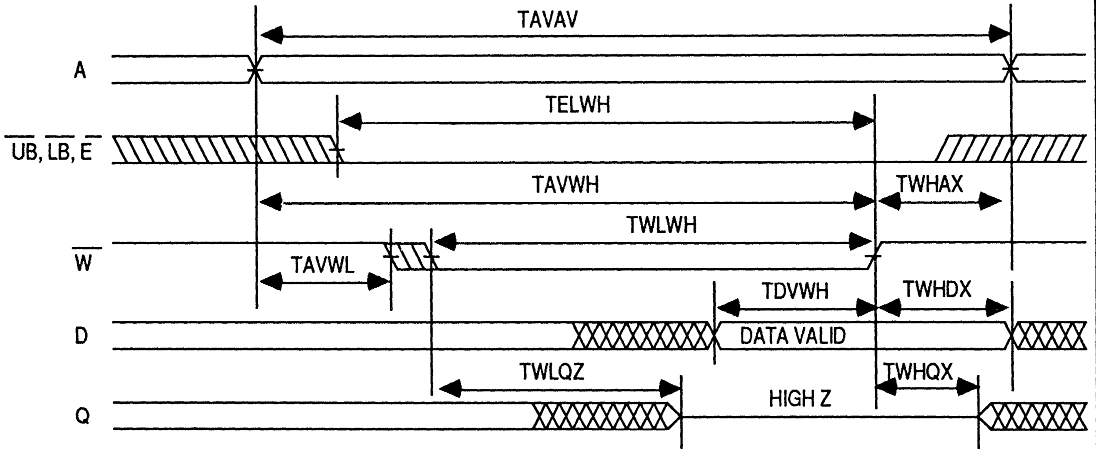
AC Characteristics
Write Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

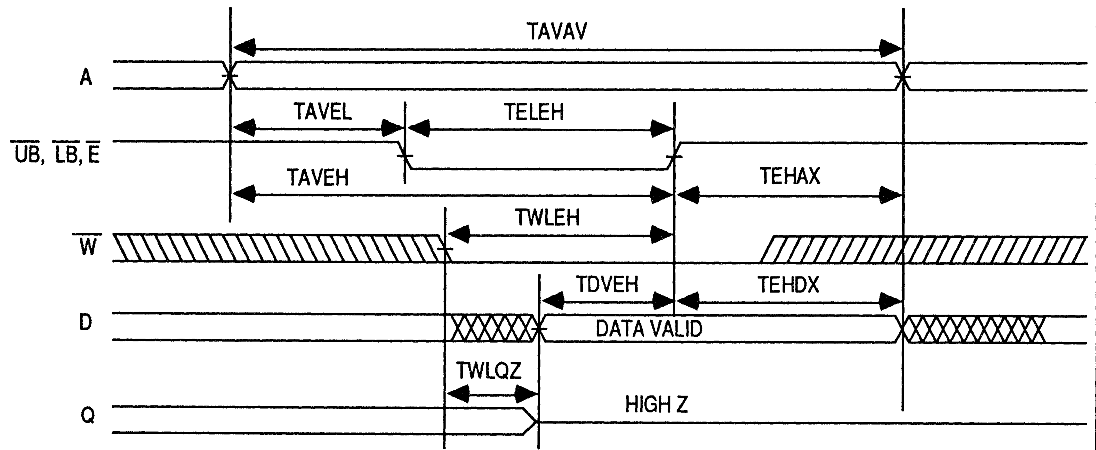
Parameter	Symbol			100ns		120ns		150ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			100		120		150		ns
Chip Enable to	TWLWH	$\overline{W}$		80		90		110		ns
End of Write	TWLEH	$\overline{E}$		80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$		20		20		20		ns
	TAVEL	$\overline{E}$		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$		80		90		110		ns
End of Write	TAVEH	$\overline{E}$		80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$		60		70		80		ns
	TELEH	$\overline{E}$		60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		0		ns
	TEHAX	$\overline{E}$		20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		20		20		20		ns
Write to Output in High Z (1)	TWLQZ			0	35	0	35		45	ns
Data to Write Time	TDVWH	$\overline{W}$		35		40		50		ns
	TDVEH	$\overline{E}$		35		40		50		ns
Output Active from End of Write (1)	TWHQX			0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



EDI

EDI8M1664C50/60/70/85/100

Megabit SRAM Module, JEDEC Pinout

64Kx16 Static RAM CMOS, Module

The EDI8M1664C is a high speed 64Kx16 CMOS Static RAM Module consisting of four (4) 32Kx8 CMOS Static RAMs in leadless chip carriers, surface mounted onto a multi-layered ceramic substrate. The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to proposed monolithic megabit Static RAMs is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using LB and UB as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

The EDI8M81664C is available with access times as fast as 50ns.

Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B., making them ideally suited to applications demanding the highest level of performance and reliability.

Features

64Kx16 bit CMOS Static Random Access Memory Module

- Access Times 50, 60, 70, 85, and 100ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Data Retention Function

Jedec Approved Pinout

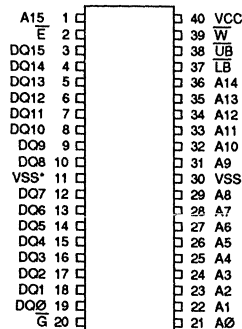
- 40 Pin Ceramic Dual-in-line Package

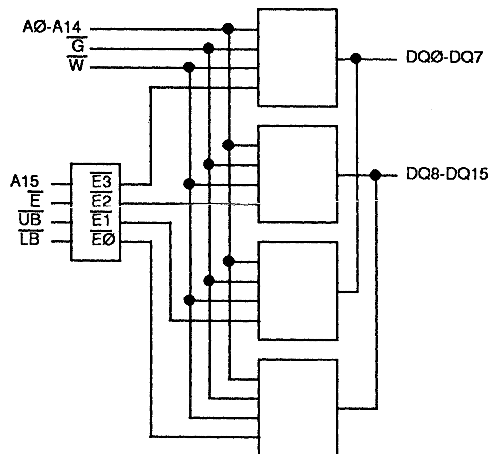
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ15	Data Input/ Output
UB	Upper Byte Control
LB	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





*Note: Both ground pins (VSS) need to be grounded for proper operation.

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial............................... 0°C to +70°C.
Industrial...................................-40°C to +85°C
Military................................... -55°C to +125°C
Storage Temperature (Ambient/Ceramic).-65°C to +150°C
Power Dissipation...4 Watts
Output Current... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels. ....VSS to 3.0V
Input Rise and Fall Times. 5ns
Input and Output Timing Levels 1.5V
Output Load.: 50/70ns. ....1TTL, CL = 30pF
85/100ns.....................................1TTL, CL = 100pF
(Note: For TEHQZ, TGHQZ, and TWLQZ, CL = 5pF.)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max		Units
					50/70	85/100	
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, II/O = 0mA, Min Cycle	--	170	240	195	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; II/O = 0mA, Min Cycle	--	115	160	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or $\overline{LB}$ & $\overline{UB}$ ≥ VIL	--	50	95	75	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ ≥ VCC- 0.2V or $\overline{LB}$ & $\overline{UB}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	10	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±10		µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±10		µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--		V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4		V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	$\overline{UB}$ Write	DIN(8-15)	ICC1
L	H	L	L	X	$\overline{LB}$ Write	DIN(0-7)	ICC1
L	L	L	L	X	Write	DIN(0-15)	ICC1
L	L	H	H	L	$\overline{UB}$ Read	DOUT(8-15)	ICC1
L	H	L	H	L	$\overline{LB}$ Read	DOUT(0-7)	ICC1
L	L	L	H	L	Read	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	$\overline{G}$,A	CI	60	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	30	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	30	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

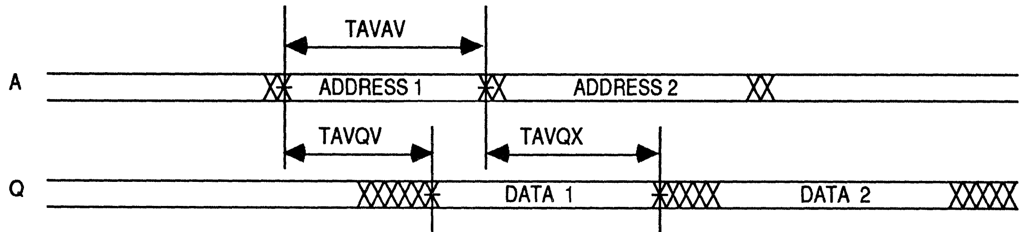
(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		85ns		100ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		50		60		70		85		100		ns
Address Access Time	TAVQV			50		60		70		85		100	ns
Chip EnableAccess Time	TELQV	$\overline{E}$		50		60		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$	30		30		30		30		30		ns
Output Enable to Output Valid	TGLQV			30		35		40		50		60	ns
Output Enable to Output in Low Z (1)	TGLQX		5		5		5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	$\overline{E}$		35		35		35		40		45	ns
Output Enable to Output in High Z (1)	TGHQZ			35		35		35		40		40	ns
Output Hold from Address Change	TAVQX		10		10		10		10		10		ns

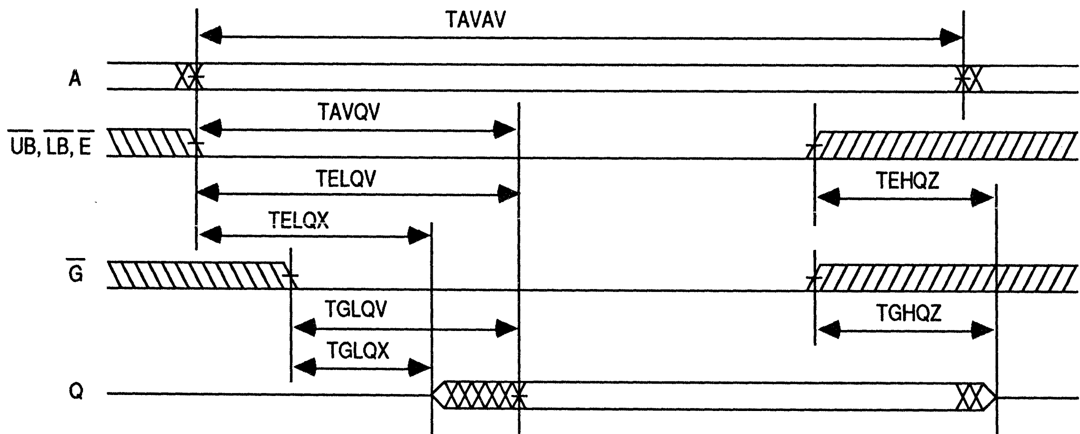
Note 1: Parameter guaranteed, but not tested.

*Preliminary data.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

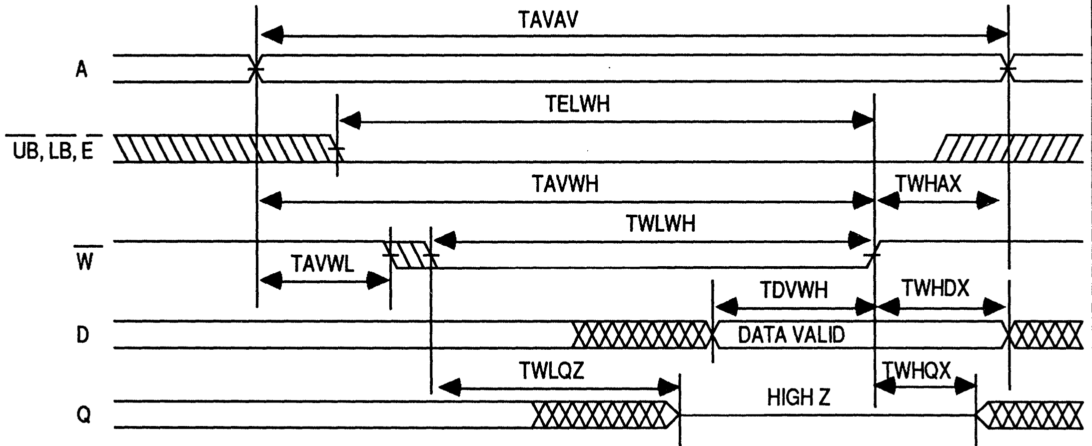
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		85ns		100ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		85		100		ns
Chip Enable to	TELWH	$\overline{W}$	45		50		65		70		80		ns
End of Write	TWLEH	$\overline{E}$	45		50		65		70		80		ns
Address Setup Time	TAVWL	$\overline{W}$	10		10		10		10		10		ns
	TAVEL	$\overline{E}$	10		10		10		10		10		ns
Address Valid to	TAVWH	$\overline{W}$	40		50		65		70		80		ns
End of Write	TAVEH	$\overline{E}$	40		50		65		70		80		ns
Write Pulse Width	TWLWH	$\overline{W}$	35		45		55		55		70		ns
	TELEH	$\overline{E}$	35		45		55		55		70		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	25	0	30	0	45	0	50	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		35		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		0		ns

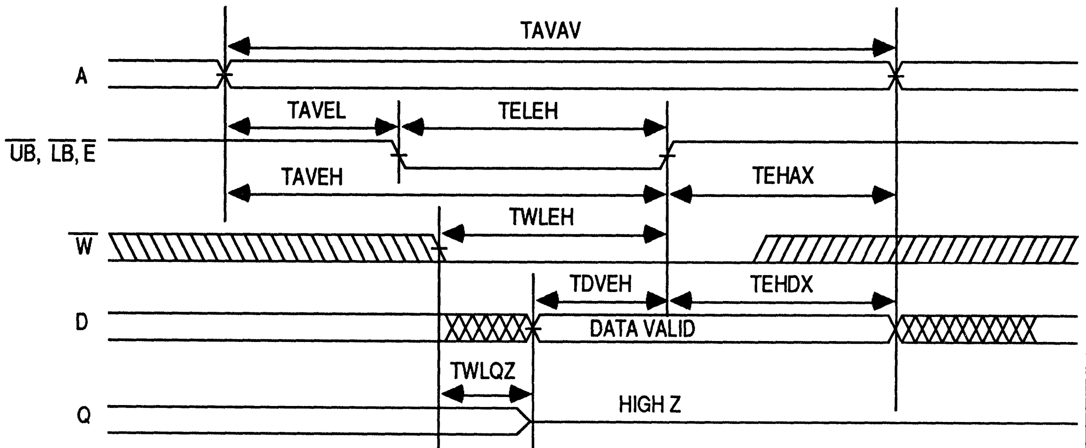
Note 1: Parameter guaranteed, but not tested.

*Preliminary data.

Write Cycle 1
W Controlled



Write Cycle 2
E Controlled



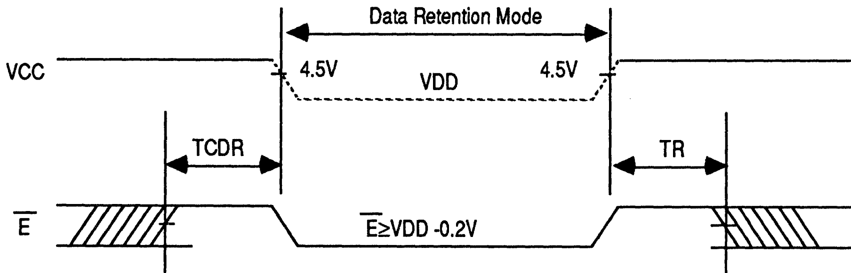
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max		Unit
					50/70	85/100	
Data Retention Voltage	VDD	VDD = 2.0V	2.0	--	--		V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	300	2500	1500	μA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	--	ns

*Read Cycle Time

Data Retention *$\overline{E}$ Controlled*



256Kx8 Static RAM CMOS, Module

PRELIMINARY

The EDI8M8256C is a 2048K bit CMOS Static RAM module.

It is based on eight 32Kx8 Static RAMs in plastic VSOP packages mounted on a multi-layered ceramic substrate. The EDI8M8256C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8256C requires no clocks or refreshing for operation.

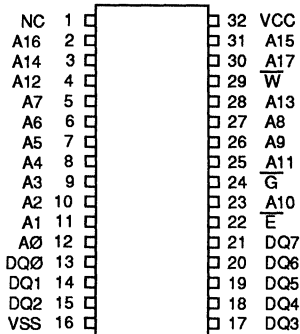
Features

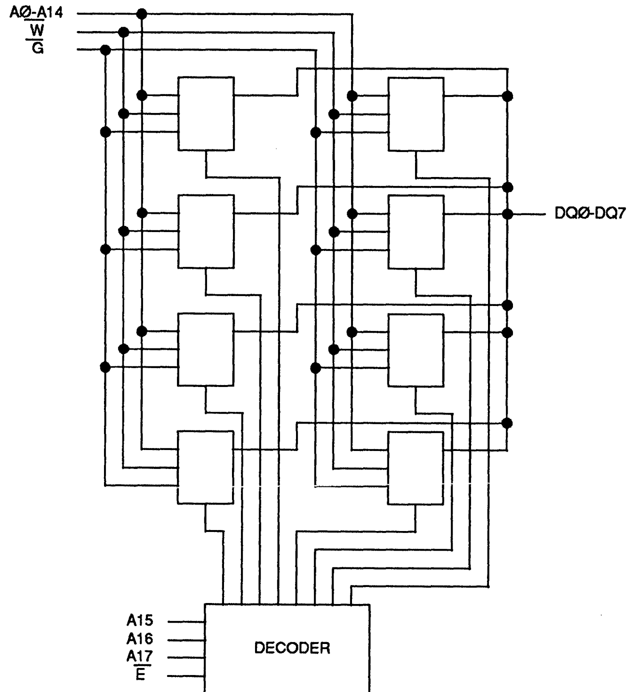
256Kx8 bit CMOS Static
Random Access Memory Module
- Access Times 70, 100, and 120ns
- Fully Static, No Clocks
- TTL Compatible Inputs and Outputs

32 Pin Dual-in-line Package (P)
- JEDEC Approved Pinout

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial...................................0°C to +70°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.. 1 Watt
Output Current... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels..VSS to 3.0V
Input Rise and Fall Times.. 5ns
Input and Output Timing Levels...................................... 1.5V
Output Load... 1TTL, CL = 100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	W̄, Ē = VIL, II/O = 0mA, Min Cycle	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	Ē≥ VIH	--		65	mA
Full Standby Power Supply Current	ICC3	Ē≥ VCC-0.2V VIN ≥VCC-0.2V or VIN≤0.2V	--		20	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

Ḡ	Ē	W̄	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	55	pF
Capacitance Control (DQ Pins)	CD/Q	42	pF
Input Capacitance Control Lines	CC	16	pF
Input Capacitance W̄ Line	CW	48	pF

These parameters are sampled, not 100% tested.

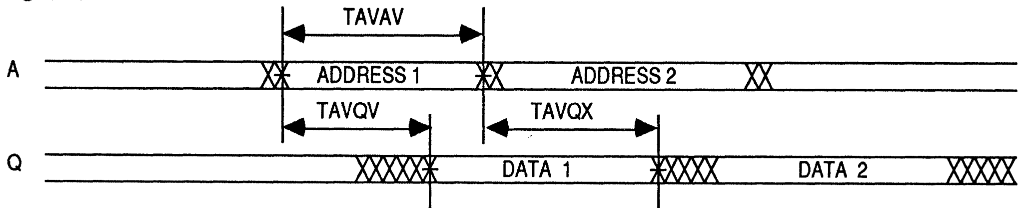
AC Characteristics
Read Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

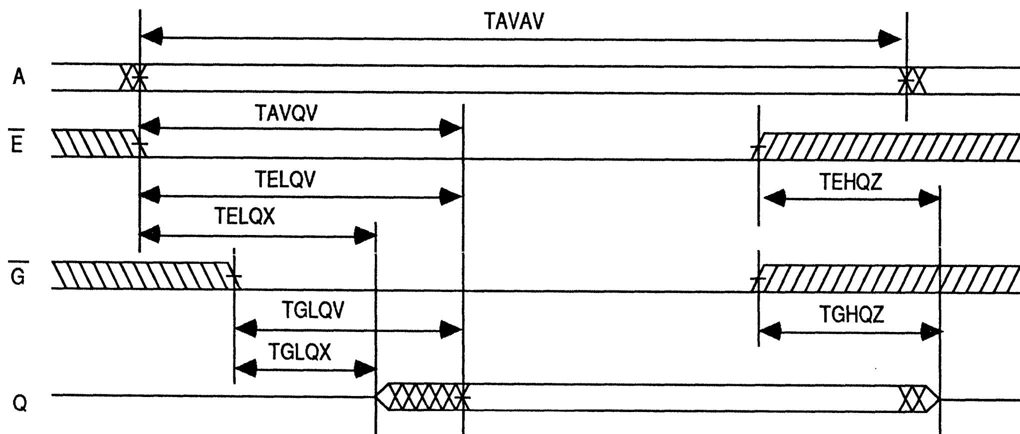
Parameter	Symbol		70ns Min	70ns Max	100ns Min	100ns Max	120ns Min	120ns Max	Units
Read Cycle Time	TAVAV		70		100		120		ns
Address Access Time	TAVQV			70		100		120	ns
Chip Enable Access Time	TELQV			70		100		120	ns
Chip Enable to Output in Low Z (1)	TELQX		30		30		30		ns
Output Enable to Output Valid	TGLQV			35		50		60	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		0	30	0	30	0	40	ns
Output Enable to Output in High Z (1)	TGHQZ		0	30	0	30	0	40	ns
Output Hold from Address Change	TAVQX		10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

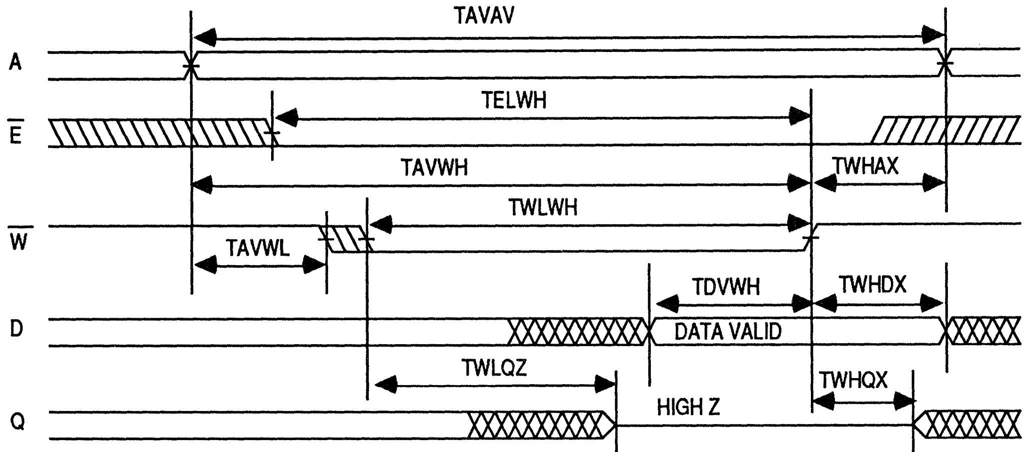


AC Characteristics
Write Cycle
(TA = 0°C to +70°C; VCC = 5.0V ±10%)

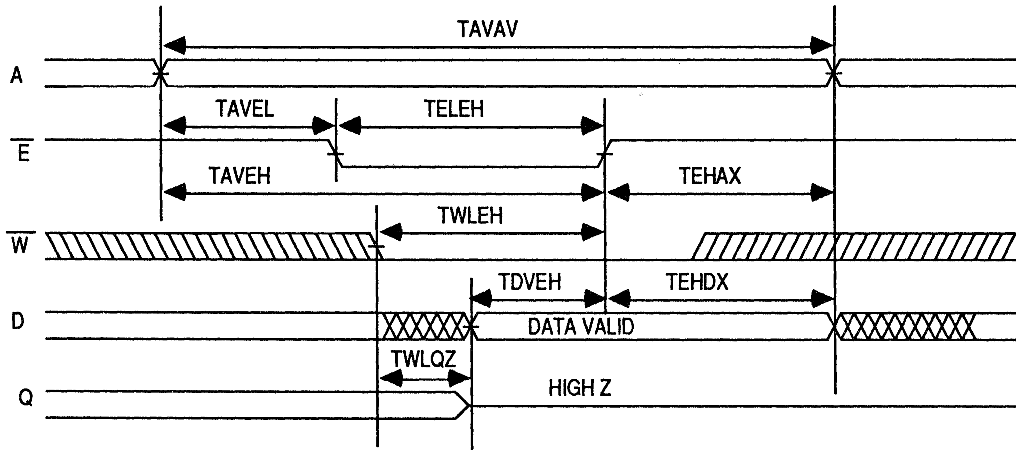
Parameter	Symbol		70ns Min	70ns Max	100ns Min	100ns Max	120ns Min	120ns Max	Units
Write Cycle Time	TAVAV		70		100		120		ns
Chip Enable to End of Write	TELWH	$\overline{W}$	65		80		90		ns
	TWLEH	$\overline{E}$	65		80		90		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to End of Write	TAVWH	$\overline{W}$	60		80		90		ns
	TAVEH	$\overline{E}$	60		80		90		ns
Write Pulse Width	TWLWH	$\overline{W}$	55		60		70		ns
	TELEH	$\overline{E}$	55		60		70		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	30	0	35	0	40	ns
Data to Write Time	TDVWH	$\overline{W}$	30		35		40		ns
	TDVEH	$\overline{E}$	30		35		40		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W Controlled



Write Cycle 2
E Controlled



Quality Assurance Policy

The Quality Standard at Electronic Designs Incorporated (EDI) is defect free work. No other standard is acceptable.

This policy is refelcted in the attention given to the design, manufacture, and test of all of our products. All procedures are designed to meet or exceed the requirements of our customers, and the strict requirements and procedures dictated by Military Standards.

Maintaining the highest standards of quality demands a continous committment fromeach individual, through out the company. EDI conducts a comprehensive training program for all employees which stresses the importance of each individual to the final objetive of satisfied customers through defect free products and workmanship.

MIL-STD-883C Compliance

EDI's hermetic Military grade monolithic CMOS SRAMs are in full compliance with the product flow and test procedures of paragraph 1.2.1 of MIL-STD-883.

The products are processed to the standardized screening flow, Method 5004 of MIL-STD-883C. Periodic inspections, per Method 5005 of MIL-STD-883C are performed to ensure adequate screening. The purpose of Methods 5004 and 5005 is given below.

1. Screen infant mortality.
2. Produce highly reliable product.

In addition, EDI performs extended life tests on all released products. Devices are tested at +125°C for 1000 hours. Failures are rigorously analyzed to identify failure mechanisms. Finally, corrective actions are implemented to preclude failure recurrence. This closed loop system ensures that reliability is "designed in" rather than "tested in."

With this information, EDI can:

1. Predict failure rates
2. Assess impact of design. process or material change.
3. Determine useful product life.

EDI Quality Conformance Inspections

Military Monolithic Devices and Modules

Quality Conformance Inspection (QCI) for monolithic memories, including those used on memory modules, is designed to conform to all of the requirements of MIL–STD–883, Method 5005. QCI for memory modules is also designed to follow the basic requirements of MIL–STD–883, Method 5005, with modifications as described below.

Group Testing

Group A testing on monolithic devices includes a one hundred sixteen (116) piece sample, taken at random from each inspection lot after all assembly screening has been completed, is subjected to the applicable subgroups, dependant upon the test temperature selected. For Modules a lot verification is done by QA per MIL-STD-883C, Method 5008.

Group B tests for monolithics are per Method 5005. Module Group B is the same, except subgroup five (5) is omitted. Samples are taken from each inspection lot as directed and allowed by Method 5005 after all assembly screening has been completed.

Group C tests for monolithic devices are performed on die produced each quarter. A forty–five (45) piece sample from each die family is taken from a representative inspection lot after all screening has been completed. The lot is then subjected to 1000 hours of life testing at 125 degrees centigrade or the equivalent, as allowed by Method 1005, Table 1. Group C tests for modules are performed once annually. A forty five (45) piece sample from each module family is taken from a representative inspection lot after all screening has been completed. the lot is then subjected to 1000 hours of life testing at 125 degrees centigrade or the equivalent, as allowed by Method 1005, Table 1.

Group D tests for monolithic devices are performed once every six months. Samples from each package family are taken from a representative inspection lot after all screening has been completed. Monolithic devices are subjected to the tests per Method 5005. Group D tests for modules are performed once annually on one complex module type for a representative inspection after all other screening has been completed.. Modules are subjected to a modified 5005 screening. Seal tests and subgroups six (6) and eight (8) are omitted.

Military Process Flow

EDI's Military products are assembled and tested to the MIL–STD–883, Rev C. Class B, Method 5004/5005. Component modules are assembled with MIL–STD–883, Rev C compliant monolithic memory devices and processed to the latest recommendations of the JC–13 Task Group on Modules.

Monolithic, MIL-STD-883C, Class B Assembly Flow: Sidebrazed and LCC

- ❑ Receive Wafers, Bases and Lids @ EDI
- ❍ Wafer and Piece Part Incoming Acceptance
- ❑ Ship Wafers and Piece Parts to Subcontractor
- ❍ Incoming Inspection for Wire and Preform, Functional Test for Piece Parts
- ❑ Release to Assembly for Production
- ❑ Wafer Saw 100% Saw-Thru
- ❑ Die Separation and Placement
- ▲ Second Optical Inspection, Method 2010
- ❍ Second Optical QA Gate
- ❑ Eutectic Die Attach
- ❍ Die Shear and Die "Flick" Monitor
- ❑ Ultrasonic Wire Bond
- ❍ Wire Bond Strength Test
- ▲ Third Optical Inspection, Method 2010, Class B
- ❍ Third Optical QA Gate
- ❑ Lid Placement
- ❑ Seal
- ❑ Back Mark
- ❑ Temperature Cycle, Method 1010, Cond. C
- ❑ Centrifuge, Method 2001C, Cond. E
- ❑ Fine Leak, Method 1014
- ❑ Gross Leak, Method 1014, Cond. C
- ❑ Lead Shear (Sidebrazed Only)
- ▲ Final Visual Inspection, Method 2009
- ❍ Final Visual QA Gate
- ❑ Ship to EDI

❑	Production
❍	QA Inspection
▲	Production Inspection

Monolithic, MIL-STD-883C, Class B Assembly Flow: CERDIP

- ❑ Receive Wafers, Bases, Frames and Caps
- ❍ Wafer and Piece Part Incoming Acceptance
- ❑ Ship Wafers and Piece Parts to Subcontractor
- ❍ Incoming Inspection for Wire, Preform, and Jumper Chip Functional Test for Piece Parts
- ❑ Release to Assembly for Production
- ❑ Frame Attach
- ▲ Frame Attach Inspection
- ❑ Wafer Saw 100% Saw-Thru
- ❑ Die Separation and Placement
- ▲ Second Optical Inspection, Method 2010
- ❍ Second Optical QA Gate
- ❑ Eutectic Die Attach on Frame Attached Base
- ❍ Die Shear and Die "Flick" Monitor
- ❑ Ultrasonic Wire Bond
- ❍ Wire Bond Strength Test
- ▲ Third Optical Inspection, Method 2010, Class B
- ❍ Third Optical QA Gate
- ❑ Lid Placement
- ❑ Seal
- ❑ Seal Monitor
- ❑ Back Mark
- ❑ Temperature Cycle, Method 1010, Cond. C
- ❑ Centrifuge Method 2001Cond. E
- ❑ Lead Shear
- ❑ Solder Dip
- ❑ Fine Leak, Method 1014
- ❑ Gross Leak, Method 1014, Cond. C
- ▲ Final Visual Inspection, Method 2009
- ❍ Final Visual QA Gate
- ❑ Ship to EDI

Component Module Assembly Flow

(All Module Semiconductor Components are MIL–STD–883C, Class B Processed)

- ❑ Receive Substrates and Solder @ EDI Substrates and Solder Incoming Inspection
- ❍ Pull components for Module Build to Bill of Materials
- ❑ Release to Assembly for Production
- ❑ Component Prep
  - Mark Removal
  - Solder Dip of Components (as required)
- ❑ Solder Dispense, Bottom
- ❑ Component Placement
- ❑ IR Reflow
- ❑ Solvent Clean
- ❑ Solder Screen Printing,Top
- ❑ Component Placement
- ❑ IR Reflow
- ❑ Solvent Clean
- ❑ Lead Shear
- ▲ Final Assembly Visual Inspection
- ❑ Final Optical QA Gate
- ❑ Move to Test
- ❑ Test @ Room (25°C)
- ❑ Temperature Cycle, Method 1010, Cond. C
- ❑ Test @ Cold (-55°C)
- ❑ Test @ Hot for Speed Sort (125°C)
- ❑ Mark
- ▲ Final Visual Inspection
- ❍ Final Visual QA Sample Gate
- ❍ Group A (In–Line Option)
- ❍ Group B (Mark Perm, Solderability)
  - ❍ Periodic Group C & D
- ❑ Ship

Monolithic Test Flow

- ❑ Receive at EDI from Subcontractor
- ❑ Incoming Inspection
- ❑ Release to Test
- ❑ Room Test (25°C)
- ❑ Burn in, 160 hours @ 125°C or Equivalent
- ❑ Room Test (25°C)
- ❑ PDA Calculation
- ❑ Test @ Cold (-55°C)
- ❑ Test @ Hot for Speed Sort (125°C)
- ▲ Final Visual Inspection
- ❍ Final Visual QA Sample Gate
- ❍ Group A (In–Line Option)
- ❍ Group B
  - ❍ Periodic Group C & D
- ❑ Ship

Test Patterns

Selecting the appropriate patterns to test semiconductor RAM devices can be a long, drawn-out process. A great deal of effort has been spent on finding the perfect pattern, a pattern that could detect all memory faults. It has become apparent, however, that no single pattern could exercize a RAM thoroughly enough to detect all its failure modes. It has therefore become a practice in the semiconductor industry to choose sets of memory test patterns, in the hope that most device faults will be discovered in the shortest time.

Limiting test time, especially in the production environment, has become the most important consideration when choosing test patterns. Test times have increased as memory device densities have increased. In some cases additional test time is directly proportional to the number of memory cells. For some test patterns, the increase in test time follows the square of the number of memory cells. As memory sizes con-

tinue to grow, there is an important trade off between test time and the type and number of test patterns executed.

Extensive testing in the form of characterization is performed on all new products, and in the case of a design or wafer change. Long test patterns are executed with the intent of fully stressing the RAM to guarantee its reliability. It is not feasible to run these long patterns in a production mode, however. By sampling product on a lot by lot basis under the characterization set up, any potential problems which may occur during production testing will be indicated.

The following is a list of test patterns used in normal production testing, followed by a list of characterization patterns. They were chosen on the basis of their ability to find the optimal number of functional problems while keeping production test time to a minimum.

AC Parametric

1. Checkerboard & Inverted Checkerboard:

Functional testing is performed at voltages of 5.5V and 4.5V, with a Checkerboard & Inverted Checkerboard written to the entire memory. Checkerboard & Inverted Checkerboard patterns are used to check that every cell can be forced to a one (1) of a zero (Ø). This pattern also checks the susceptibility of every cell to noise, as each cell is surrounded by it's complement..

2. March:

A background of zeros (Ø) is written into memory. Then a one (1) is written into each sequential cell until the end of memory is reached. Each cell is tested and changed back to zero (Ø) in reverse order until the first address is reached. The same sequence is repeated by loading a background of ones (1).

March patterns will find cell opens and shorts as well as address uniqueness faults.

3. Masest:

This is an alternating multiple-address selection test which writes a background pattern of zeros to the DUT at the min address, then max, then min+1,then max-1, etc., then reads all DUT cells in the same manner, then writes a complimentary background pattern of ones and repeats the same steps.

This test will find any open address decode lines internal to the device.

4. Galdiag:

This is a galloping diagonal pattern test. A diagonal of ones is written to a background of zeros. All memory cells are read and the diagonal is shifted horizontally. This pattern is read and the shifting continues until the diagonal has been shifted throughout the memory. This sequence is then repeated using complemented data.

The Galdiag pattern finds unsatisfactory address transitions between each cell and the positions in the cell's diagonal. It also finds slow sense amplifier recovery and destruction stored data due to noise coupling among cells in a column.

Characterization

In a characterization mode extra patterns are used to further test the functionality of the RAM. The following is a list of patterns which require exceptionally long execution time.

1. Walking:

Into a background of zeros, the first cell is complemented and then all other cells are read sequentially. The first cell is then and restored to zero, the next cell is complemented, and all other cells are read sequentially. This continues for all memory cells. The pattern is then repeated using complemented data.

2. Galpat:

Into a background of zeros, the first cell is complemented and then read alternately with every other cell in memory. This sequence is continual and every memory cell eventually becomes the test cell. The same sequence is then executed using complemented data.

Certificate of Compliance

Customer

Part Number | Quantity

Date/Lote Code | Purchase Order Number

EDI certifies that our Hi-Rel/MIL-STD-883C product meets or exceeds the requirements of our data sheets and complies to MIL-STD-883 Paragraph 1.2.1.

Documentary evidence, in the form of test and inspection reports, is on file and available for review.

QA Representative | Date

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
TELEX 948004 (508)435-2341 FAX(508)4356302

Certificate of Compliance

Customer

Part Number | Quantity

Date/Lote Code | Purchase Order Number

This is to certify that the material furnished according to the purchase order referenced above has been manufactured, tested, and/or inspected in accordance with your purchase order and any applicable specifications.

Documentary evidence, in the form of test and inspection reports, is on file and available for review at Electronic Designs.

QA Representative | Date

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508)435-6302

Certificate of Conformance for Method 5004, Class B Screening

Class B Screen Tests	MIL-STD-883 Method*	Acc.	Rej.
Internal VIsual	2010B		
Stabilization Bake	1008C, 24 hrs. @+150°C		
Temperature Cycling	1010C, 10 Cycles -65°C / +150°C		
Constant Acceleration	2001E, Y1 orientation		
External Visual	2009		
Fine Leak	1014A, 5x10-8 Atm cc/sec.		
Gross Leak	1014C		
Interim Electrical 25°C (Pre-Burn-in)	DC and Functional tests per applicable device specification		
Burn-in	1015, 160 hrs @ +125°C		
Electrical 25°C (Post Burn-in)	DC and Functional tests per applicable device specification		
Final Electrical Tests (125°C and -55°C)	DC and Functional tests per applicable device specification		
External Visual	2009		

*All methods performed to current MIL-STD-883 revision level.

This is to certify that all EDI products supplied to your purchase order have been screened per the above methods of MIL-STD-883. All Test and Certification Data is on file at our facility.

Customer ____________________
Part Number ____________________
PO Number ____________________
Date Code(s) ____________________
Lot Number(s) ____________________
Quantity ____________________

____
Date

____
QA Representative

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508) 435-6302

Certificate of Conformance for Group A Attribute Data

Test (See Note 1)	Temp.	Sample Size	Accept	Reject
Subgroup 1, 4, 7, 9 Static, Dynamic, Functional and Switching Tests:	25°C			
Subgroup 2, 5, 8, 10 Static, Dynamic, Functional and Switching Tests:	125°C			
Subgroup 3, 6, 8, 11 Static, Dynamic, Functional and Switching Tests:	-55°C			

*Note 1. The specific parameters to be included for testing in each subgroup shall be as specified in the EDI Data Sheet or as specified on Purchase Order.

This is to certify that all EDI products supplied to your purchase order have been screened per the above methods of MIL-STD-883. All Test and Certification Data is on file at our facility.

Customer ________________
Part Number ________________
PO Number ________________
Date Code(s) ________________
Lot Number(s) ________________
Quantity ________________

____
Date

____
QA Representative

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508)435-6302

Qualification and Quality Conformance Report
Group B

Part Number / Description: ______________________

Lot Number: ______________ Date Code: ________ Quantity: ________

This hereby certifies that the above listed devices have been subjected to the reliability screening sequences as indicated below.

Test	MIL-STD-883		Quantity	
	Method	Condition	Accept	Reject
Subgroup 2 (a) Resistance to Solvents	2015			
Subgroup 3 (a) Solderability	2003	Soldering Temperature of +245° ±5°C		
Subgroup 5 (a) Bond Strength	2011	Test Condition D		

Quality Assurance Engineer ______________________ Date ____________

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508) 435-6302

Qualification and Quality Conformance Report
Group C

Part Number / Description: ______________________

Lot Number: ______________ Date Code: ________ Quantity: ________

This hereby certifies that the above listed devices have been subjected to the reliability screening sequences as indicated below.

Test	MIL-STD-883		Quantity	
	Method	Condition	Accept	Reject
Subgroup 1				
(a) Steady State Life Test	1005	1000 Hours @125°C or Equivalent		
(b) End-point Electrical Test		Per EDI Specification		

______________________ ______________
Quality Assurance Engineer Date

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508)435-6302

Qualification and Quality Conformance Report
Group D

Part Number / Description: ____________________
Lot Number: ____________ Date Code: ________ Quantity: ________

This hereby certifies that the above listed devices have been subjected to the reliability screening sequences as indicated below.

Test	MIL-STD-883		Quantity	
	Method	Condition	Acc	Rej
Subgroup 1				
(a) Physical Dimensions	2016			
Subgroup 2				
(a) Lead Integrity	2004	B2 for Leaded, D for LCC		
(b) Seal	1014	As Applicable		
(1) Fine				
(2) Gross				
Subgroup 3				
(a) Thermal Shock	1011	15 Cycles, Condition B, Min.		
(b) Temperature Cycling	1010	100 Cycles, Condition C, Min.		
(c) Moisture Resistance	1004			
(d) Seal	1014	As Applicable		
(1) Fine				
(2) Gross				
(e) Visual Examination		Per Visual Criteria/Methods 1004 & 1010		
(f) End Point Electrical Test		Per EDI Part Specification		
Subgroup 4				
(a) Mechanical Shock	2002	Condition B, Min.		
(b) Vibration Variable Freq.	2007	Condition A, Min.		
(c) Constant Acceleration	2001	Condition E, Min, Y1 Orientation only		
(d) Seal	1014	As Applicable		
(1) Fine				
(2) Gross				
(e) Visual Examination		Per Visual Criteria / Methods 1004 &1010		
(f) End Point Electrical Test		Per EDI Part Specification		
Subgroup 5				
(a) Salt Atmosphere	1009	Condition A, Min.		
(d) Seal	1014	As Applicable		
(1) Fine				
(2) Gross				
(e) Visual Examination		Per Criteria Method 1009		
Subgroup 6				
(a) Internal Water Vapor Content	1018	5,000 ppm. water content at 100°C		
Subgroup 7				
(a) Adhesion of Lead Finish	2025			
Subgroup 8				
(a) Lid Torque	2024			

Quality Assurance Engineer ____________ Date ____________

Electronic Designs Incorporated
42 South Street, Hopkinton, MA 01748 USA
Telex 948004 (508) 435-2341 Fax (508) 435-6302

Reliability Program

Radiation Program

An increased need for radiation survivability has been expressed throughout the defense industry. This need has prompted EDI to dedicate resources to the understanding of radiation effects on its Static RAM products. Our efforts are focused on gaining a better understanding of the various radiation environments and the effects of those environments on silicon.

There are two major radiation environments 1] space, 2] a nuclear event in the battlefield, each presenting unique requirements.

In a space application, a design engineer needs to consider the high energy cosmic ray penetration on the semiconductor. Hence, engineers will most likely impose a total dose and or cell requirement on space bound semiconductors.

In a nuclear battlefield application, a design engineer must consider the several types of radiation from a nuclear detonation. These include gamma, photon, and neutron radiation. Typically, a design engineer will impose a total dose neutron and a dose rate requirement. The graph shown here summarizes the various radiation environments and CMOS Static RAM effects.

Several external specialized test labs are performing radiation tests for EDI. Please consult the factory for the most recent radiation test data.

Radiation Test	*Primary Particle*	*Possible Source*	*Effect on SRAMs*
Total Dose	GAMMA	Space or Nuclear Event	Permanent functional failures due to memory cell failures
Dose Rate	Photons	Nuclear Event	Temporary upset of logic states causing "soft errors" and/or CMOS Latch-up
Single Event Upset (SEU)	Cosmic Rays	Space	Temporary upset of Logic states causing "soft errors"
Neutron	Neutrons	Nuclear Event	Silicon lattice damage

MTBF Prediction Techniques

Techniques exist for computing a components failure rate based on probability mathematics. The term failure rate, represented by the greek letter lambda (λ), is used to represent the number of failures per million hours. The reciprocal of the failure rate is called the mean time between failures (MTBF).

Monolithic MTBF Calculation

EDI has implemented a PC based program to calculate the MTBF for its Military Monolithic SRAMs. This program utilizes the failure rate prediction model found in MIL-HDBK-217E page 5.1.2.4-1. MTBF Calculations can be made available on request. In addition, calculations can be tailored to better emulate your application

Module MTBF

EDI's Military Grade CMOS SRAM Modules are fully compliant with the test and product flow procedures required by MIL-STD-883 for module assemblies. All semiconductor components used on EDI Military grade modules are processed to MIL-STD-883C, Class B prior to module assembly.

A fundamental approach for determining a module's failure rate is to calculate the sum of the individual failure rates of devices that form the sub assembly. However, special attention should be given to modules with more than one memory device. Depending on the decoding technique, one SRAM may be ON while others are Powered Down. Since EDI's SRAMs have extremely low current levels in full CMOS Standby mode, low power dissipation can be acheived. Hence, a Static RAM's power disssipation is dependent on its mode of operation, dynamic or standby.

Power Dissipation versus the mode of operation is expressed as follows:

Dynamic Mode, $P_D = V_{CC}\ I_{CC1}$

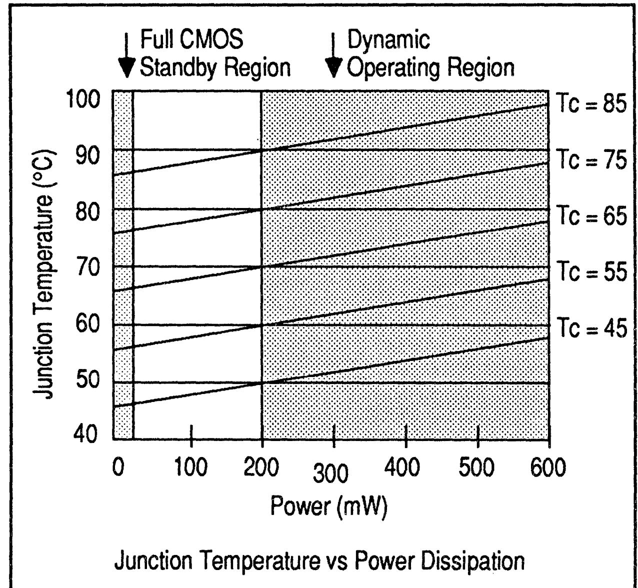
Standby Mode, $P_S = V_{CC}\ I_{CC3}$

Typically, ICC1 (Dynamic Current) and ICC3 (Full Standby Current) will vary by a factor of ten. This corresponds to a 10x increase in Dynamic Power (P_D) versus Standby Power (P_S) dissipation.

A component's failure rate is dependent on junction temperature(T_J):

$T_J = T_C = P\ (\Theta_{JC})$

T_J is a function of the case temperature (T_C), power dissipation (P), and junction to case thermal resistance (Θ_{JC}). The junction to case thermal resistance is a constant and solely dependent on the material of the die and package. Likewise, case temperature can be assumed constant and dependent upon the environment of the application. Thus, power dissipation is the only variable and it is dependent on the Static RAM's mode of operation. The graph shown here illustrates the relationship between T_J and power dissipation. Note that the junction temperature in Standby Mode is significantly lower than in Dynamic Mode.



Junction Temperature vs Power Dissipation

A lower junction temperature would correspond to a lower failure rate. Thus, a module's failure rate can improve, if you consider the standby operation of its Static RAMs. This is a suggested prediction technique for failure rate improvement.

This application note describes the basic characteristics of CMOS Static RAM devices and how they relate to the environment in which they operate. Subjects discussed range from the operation of fundamental inverter circuit, through CMOS threshold levels, and latch-up immunity, to the comparison of Static RAM storage cells.

Later on, data sheet specifications and parameters are looked at with practical applications in mind.

Basic CMOS Characteristics

Inverter Circuit

The basic building block of all CMOS circuitry is the inverter. This simple gate is used in various configurations to form the necessary functions required. The key to the low power consumption of CMOS devices is the operation of this element. Figure 1 is the schematic diagram of a CMOS inverter. It consists of a PMOS and NMOS device with common gate input and drain outputs.

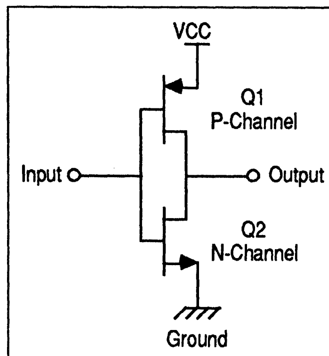


Figure 1. CMOS Inverter

Raising the input high will turn Q2 ON, coincidentally turning Q1 OFF. Similarly, returning the input level to Ground(Vss) will turn Q1 ON again and switch Q2 OFF. This has the effect of producing an output waveform that is the inverse of the applied input. The threshold of the P and N-type transistors is controlled during fabrication of the wafer to control the vertical current flow as the input signal passes from Vss to Vcc and vice-versa.

It can be seen that, while the input remains in a high or low state, no current flow occurs through the vertical path and, moreover, the amount of power consumed will depend upon the time taken to make the transition, and the number of transitions made.

If the rise and fall time of the input is relatively constant, the circuit's current consumption is almost entirely frequency dependant, doubling the switching rate will double the current consumption.

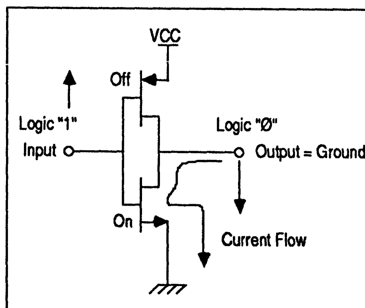


Figure 2A.

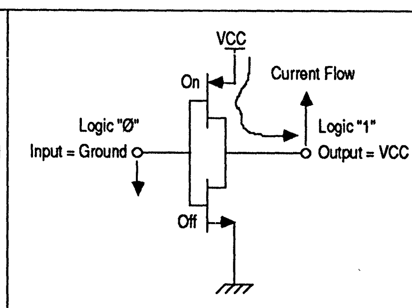


Figure 2B.

Figures 2A & 2B illustrate the direction of current flow according to the input voltage level.

As previously explained, vertical current flow from Vcc to Vss only occurs during the switching transition.

The characteristics of this current flow in relation to the input voltage is depicted in Figure 3. It will be noted that, due to the non-identical threshold levels of the P-type and N-type transistors, that the current flow is not symmetrical around the mid-input voltage level (2.5 volts) and is shifted towards the low voltage level.

Threshold Levels

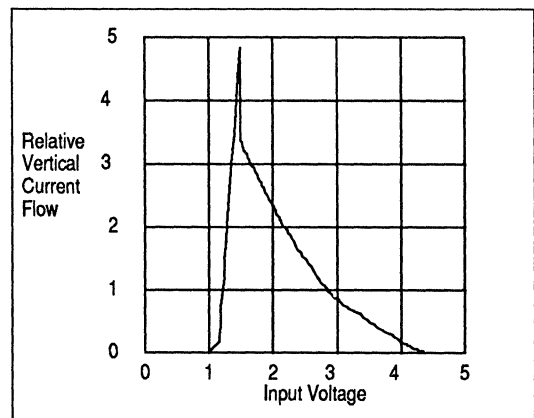


Figure 3. Input Voltage versus Current Flow for a CMOS Inverter

The characteristics of the P-type and N-type transistors define the inverter output levels for a defined input level. CMOS operates over a range of operating voltages - generally about +3 to +18 volts - and switches at a nominal 30% and 70% of VCC. If a 5 volt TTL supply is used the input must be between 0 and 1.5 volts or 3.5 to 5 volts to guarantee logic '1' and '0' respectively. This is not absolutely compatible with a TTL environment that may present the inverter with an input level as low as 2.2 volts, and require a logic '0' output to be maintained. Figure 4 demonstrates the

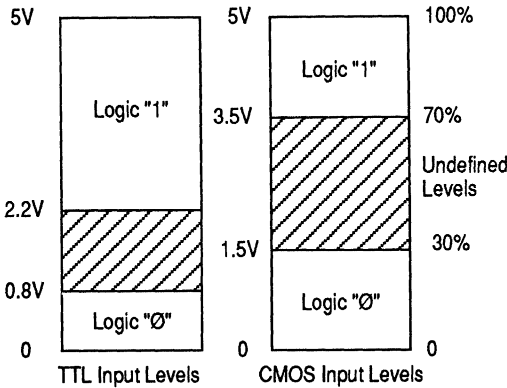


Figure 4..

problem. At below 3.5 volts, the CMOS input enters an area of uncertainty.

Fortunately, this scenario can be overcome with the careful design of input buffer threshold levels by tight control of dopants and gate geometry. The addition of an extra N-type transistor in parallel allows greater drive and lower resistance, thereby extending the guaranteed '1' input level to below 70% of the input voltage

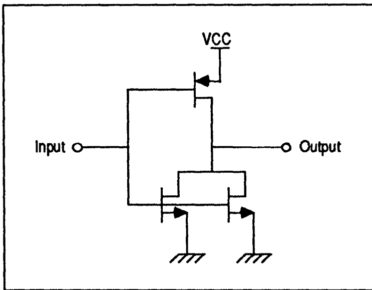


Figure 5. Input TTL to CMOS Inverter

Although we can now successfully interface TTL level signals with CMOS products, the control of the input levels has a substantial effect upon the performance of the device, especially upon the D.C. operating specifications.

Latch-up Susceptibility

Early CMOS devices had an unfortunate habit of latching-up as, inherent to the CMOS fabrication process, parasitic thyristor circuits are produced at the inputs and outputs. Worse still is the fact that thyristing action is triggered by excessive positive or negative transitions of the terminal pins.

These can occur through voltage overshoot or undershoot caused by circuit ringing or noise.

Figure 6 shows a cross section through a CMOS inverter detailing the various parasitic Bipolar transistors that are formed. In Figure 7, the equivalent schematic diagrams of the thyristor action are shown for excessive positive or negative terminal voltage.

In Figure 7A, if positive voltage, either an A.C. noise spike or a D.C. condition, is applied to the output pin, Q3 will turn ON as result of the bias voltage produced between the transistor's base

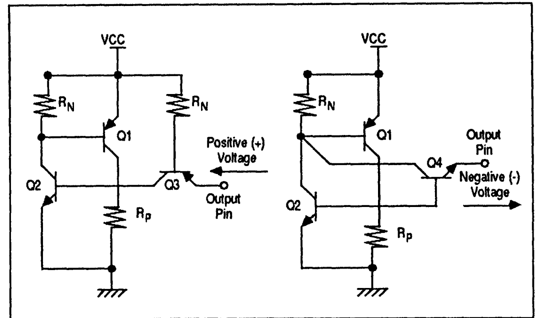


Figure 7A. Figure 7B.
Equivalent Circuits for Positive and Negative Voltage Latched Thyristors

and emitter. This will produce a current flow through the base resistance of Q2, shown as RP, to ground. This then causes Q2 to conduct, which in turn switches Q1 ON. The action of Q1 turning ON maintains base current to Q2 forming a closed loop circuit of Q1 and Q2. Current then flows from VCC to VSS for as long as the supply is maintained. The transient input pulse is no longer required to maintain current flow conditions and the circuit is latched.

Figure 7B shows the position in the case of a negative input condition. In this case Q4 conducts, enabling base current of Q1 to flow and resulting in the conduction of Q1. This leads to Q2 being turned ON, maintaining base current to Q1, stabilizing the conduction path between VCC and VSS.

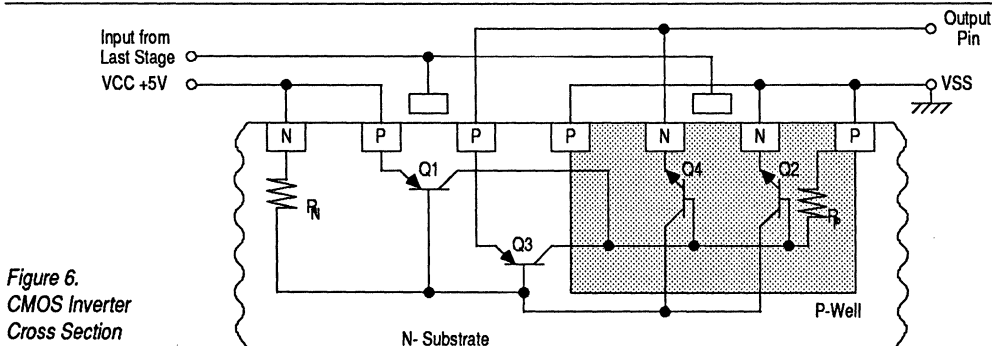


Figure 6. CMOS Inverter Cross Section

Fortunately the tendency for devices to latch-up, which could, in some cases, lead to the destruction of the part, has largely been eliminated. Figure 8 illustrates the latch-up immunity characteristics typical of EDI devices.

EDI products include a number of features that are designed to prevent latch-up under normal operating conditions.

These features include:

- Increased separation between the VCC N-well and N-diffusion layer.
- Careful design of input circuits using diffused polysilicon resistors and protection diodes to VCC and VSS.
- Increased current sink capability to VSS.
- Diffused guard bands on all inputs and outputs to prevent substrate current flow occurring.

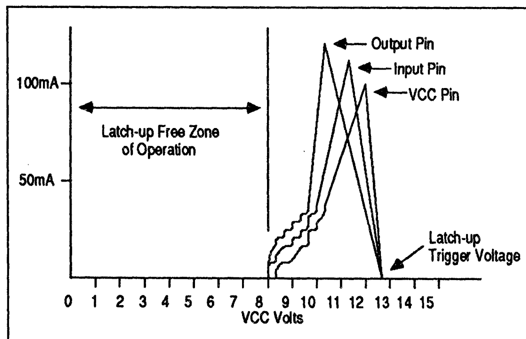


Figure 8. SRAM Latch-up.

As noise and current spikes are a realistic part of every digital circuit, a generous margin on recommended operation conditions is specified to virtually eliminate the possibly of latch-up.

For instance, EDI's 256K x 1 SRAM, EDI81256, has the following specification:

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCC	Supply voltage	-3.5* to 7	V
VI	Input voltage	-3.5* to 7	V
VO	Output voltage	-3.5* to 7	V

*-3.5 Volt input is permissible for maximum pulse width of 20ns. The D.C. steady state voltage condition is -0.5 volts.

As long as the engineer maintains good equipment design practice, and operates devices within these limits, no problems will occur with parts latching-up. Careful consideration should be a applied to power regulation, power distribution, device decoupling and bus terminations to prevent excessive ringing. It is recommended that one ceramic or tantalum de-coupling capacitor with a value of between 10-100nF is used for every device where all devices are accessed at once, i.e. in designs using x1 organizations, or for every two or three devices when x8 parts are used.

Power supply lines VCC and VSS should run as close as possible to the device to ensure the lowest impedance. Thicker copper tracking should be used for the power rails than for signal lines. In large arrays, or where many devices are accessed in parallel, the use of additional copper strips mounted vertically on the upper side of the printed circuit board and connected along the length of the power supply tracking, should be considered to reduce power supply noise and impedance. Wherever possible, all signal lines should run at right angles to the power tracks to minimize any R.F. coupling effects.

Noise generated in signal lines can usually be traced to an unstable VSS reference voltage. The use of a 50Ω series resistor in the signal path will often cure the problem if the power supply is found not to be at fault.

CMOS SRAM Cell Design

The basic Static RAM cell consists of a flip-flop circuit with additional transistors to enable the storage and retrieval of data to and from the cell.

Memory devices have highly orthogonal layouts, with the data storage cells occupying from 40% to 60% of the silicon area. Not only will the cell design contribute significantly to the memory access time, but it will also be the major factor in determining the operational and standby power consumption, data retention performance, and, not least, the cost of the device.

All Static RAM devices today use one of two cell configurations to produce the required characteristics. One of these is commonly known as the 4 transistor or NMOS cell device that uses full CMOS peripheral circuitry to reduce operational power consumption and is usually referred to as a MIX-MOS part. The other is the FULL-CMOS or 6 transistor design that utilizes CMOS fabrication in the construction of the data storage cell and peripheral functions.

Although the characteristics of the memory cells differ somewhat, the basic operation is the same.

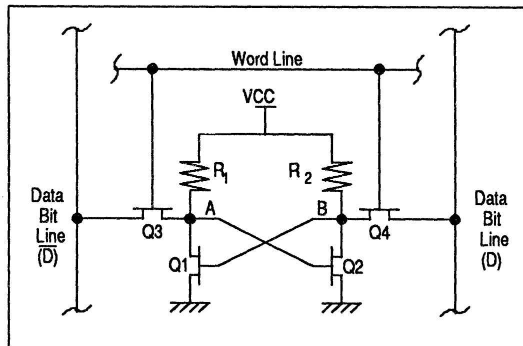


Figure 9. 4T+2R Memory Cell Operation.

Figure 9 is the schematic diagram of a 4 transistor memory cell. This is the cell type that is used in the majority of Static RAM devices available today. It operates as follows: The address decoders select a unique address within the memory array that, depending upon the word width of the device, activates one, four, eight, or sometimes nine memory cells. Two data bit lines correspond with each cell. One for true and one for inverse of the data bit value. When writing to a cell, the word line is raised in order to turn on both transistors Q3 and Q4. The voltage levels at points A and B will always complement each other, with node B representing the true logic level to be stored in the cell. If data line D is high

when the word line turns Q4 ON, a high level will appear at node B. At the same time, a corresponding low level will be applied to node A through Q3. Whatever the state of the memory cell prior to this, it will now reflect the voltage levels at points A and B. Q1 will now be in a state of conduction, which assists the low level at point A and turns Q2 OFF, allowing point B to rise to VCC. Lowering or de-selecting the word line will turn off Q3 and Q4, leaving the cell in a stable state reflecting the data most recently applied. Reading back the data is again initiated by making Q3 and Q4 conduct by raising the word line, only on this occasion the bit lines are high impedance inputs to the sense amplifiers. The sense amplifier inputs are now fed with appropriate data from points A and B.

Resistors R1 and R2 provide the loads for transistors Q1 and Q2 respectively. In the FULL CMOS cell structure, the load is provided by P-type transistors. The relative merits of these cell configurations are summarized in the following table:

Comparison of Static Ram Memory Cell Structures

	4T+2R NMOS Cell	6T CMOS Cell
Relative Area	1	1.5
ICC1: Operating Current	Medium to High 80-105mA	Low to Medium 50-100mA
ICC3: Standby Current	Medium 10-30mA	Low to Medium 5-25mA
IDR: Data Retention Current	Low to Medium 100-500µA	Very Low 10-50µA
Access Times	Fast to Medium 25 to 150ns	Medium to Slow 70 to 250 ns

Relative Area

As previously mentioned, the memory cell array can consume between 40% and 60% of the total area of a device. A relatively small saving then, will result in a considerable reduction in overall die size. As the number of devices that can be fabricated onto a given wafer size increase, the cost per die falls. This is one of the prime reasons for designing with 4T+2R cell configuration.

For instance, if a comparison is made of 256K SRAM with 4T+2R or 6T cell structure we find the following:

Cell Structure Area

	4T+2R	6T	Unit
Cell Area	90	135	sq. µm
Peripheral Area	25	25	sq. mm
Total Cell Area	23	35	sq. mm
Total Die Area	48	60	sq. mm
% Cell Area of Die	48	58	%
Increase in Die Size	0	25	%
No. per 6" Wafer	380	304	

The effective number of die per wafer is decreased by 20% if a 6 transistor cell structure is used.

As memory density increases from the 256K bit level up to and through the 1M to 4M bit densities, the die size becomes an increasingly important factor. Line widths and minimum feature dimensions must be reduced to compensate for the quadruplingof the number of memory cells. This tends to favor the 4T+2R device for future designs as the percentage of die area consumed by the memory cells will increase up to 85 to 90% of the total. At this point, the die area increases almost identically to that of the individual cell. With manufacturers continually trying to squeeze higher density into smaller packages, it is unlikely that the full CMOS cell will survive the course.

Operating Current

Since the dynamic operation of the two memory cells is similar, the variation of operating current is mainly attributable to the optimization of one or more features. Generally, 6T devices are designed for low standby and data retention currents, and speed is compromised. On the other hand, 4T designs are usually aimed at producing a faster part with acceptable data retention figures.

Like the basic CMOS inverter circuit, maximum current is consumed during operations. Similarly, as the frequency of reading and writing increases, the current required increase in direct proportion.

Comparisons of operating current must be made at the same operating frequency with identical data patterns. Reading or writing of data, which consume different amounts of power, must also be considered.

If a comparison is made between the two cell design types, with devices using similar fabrication process and with similar access times, the operating current consumption will not vary greatly.

Standby Current

Standby current is usually defined at specific input voltage levels relating to CMOS and TTL logic conditions.

When in standby, the memory cell retains the most recently written data. All peripheral chip functions have ceased and the only current consumed is made up from leakage and the current flow required to maintain the memory array state. In the 6 Transistor configuration, and referring to Figure 10B, one pair of diagonal P and N type transistors will be conducting, the other pair will be turned off.

Because there is no direct path from VCC to ground for current to flow, the standby current consumption of this cell is caused by thermally generated carriers and increases with temperature. Although very small, the leakage current per cell must be multiplied by the memory density to arrive at the memory cell array consumption.

For the 4 Transistor design, data is maintained with one of the two cross coupled N Type transistors ON, and the other one OFF. Looking at Figure 10A, if Q1 is OFF, node A will be very close to VCC. Current flow through resistor R1 would be practically zero. However, Q2 will be conducting, pulling point B to ground and dissipating power in R2. This current flow through one of the cell's load resistors contributes to the main current consumption of this cell type in standby. The current through the load resistor need only be sufficient to compensate for the leakage current drain from nodes A and B to Vss. This is usually in the order of picoamps. The polysilicon resistors can therefore be in the region of several GΩ. It is only in the past few years that the ability to fabricate resistors of uniform high resistance has been developed, enabling design-

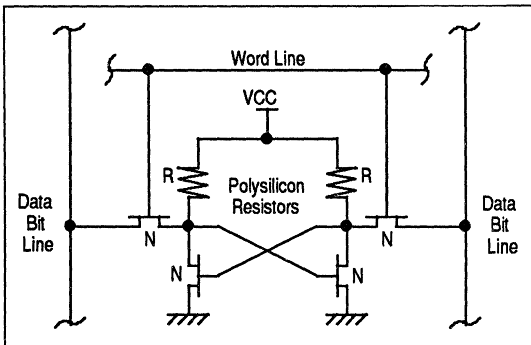


Figure 10A. 4T+2R Cell

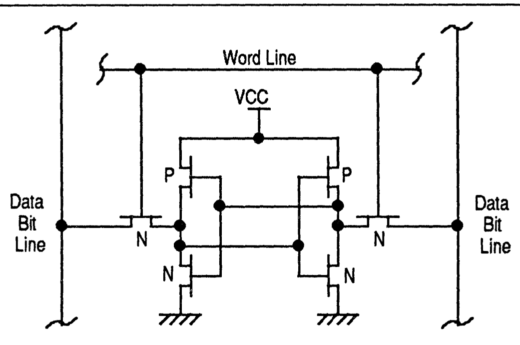


Figure 10B. 6T Cell

ers to realize high density memory arrays with 4 Transistor cell structures and low power consumption.

While the load resistor values stay around the 10GΩ region, the current consumption of the two cell designs is very similar. However, polysilicon has a negative temperature coefficient of resistance such that as things warm up, a significant increase in current through the resistor results. At anything below 70° to 85°C the standby current consumption curves of the cell designs are similar. Above this point, the rate of increase in current consumption of the 4T cell is far greater than the 6T. Typical curves are given later.

The cell array current consumption can become a small proportion of the total under certain conditions. These conditions relate to the control of the input level voltage while in standby. The reason for this is explained later in the data sheet characteristics section.

Data Retention Current

Data retention is usually specified at 2 volts VCC with all inputs at CMOS logic levels.

This presents the device with the best electrical conditions in order to consume minimum currents. Data retention mode is a low voltage version of the standby mode. The current consumption characteristics are similar to the standby condition, although the difference in the cell structure is more apparent as the ratio in current demonstrates. The memory array consumption now becomes the dominant element in the overall figure.

Access Time

Static RAMs are usually optimized for low current consumption or fast access time. The feature sizes of the elements that make up the cell size will determine some of the access time characteristics. A larger transistor area, for instance, will have a greater electron storage effect and will require longer to switch condition. Conversely, this will also determine the maximum rate of current change as the two N-type transistors connecting the memory core to the bit lines must supply the initial charge to alter the memory state, if required. The peripheral circuit functions such as address buffers, decoders, memory array drivers, sense amplifiers and output buffers can all be designed with low power or high speed in mind. A full CMOS 6T memory cell structure consumes a larger silicon area than a 4T part and access times are greater due to increased signal propagation delays. In general, 6T designs are used where low power consumption is needed and access times are not important..

Data Sheet Characteristics

Operating Power Supply Current, ICC1

ICC1 is the absolute maximum current consumption of the device measured at the worst case over the entire operating temperature range (usually -55°C to +125°C) at the highest speed for the fastest part included in the data sheet.

SInce this part will have the minimum cycle time, it will require the greatest current assumption.

All address and data inputs will be toggling at the minimum cycle time as patterns of address and data are written to, and read from, the device.

The Chip enable pin will be held at the maximum TTL logic low voltage level (0.8 volts) as this also consumes the maximum power in the buffer input stages.

No additional current drain from the output buffers of the part is considered. In a circuit, current will be taken from the output buffers by the input stages of the devices being driven. This current will depend very much on the type of input; CMOS devices will present a mainly capacitive load with instantaneous current requirements, while a TTL input will draw a continuous current.

A typical current is also specified. This is derived from characterization data and represent what can be expected if the part is used at room temperature with a 5 volt supply. Again, this will be for the fastest device on the data sheet.Figure 11 illustrates operating power supply current consumption variation with temperature. It can be seen that the device has a negative coefficient and would consume the maximum current at the minimum temperature. This should be considered when the system power supply unit is specified.

Standby (TTL Level) Power Supply Current, ICC2

Raising the Chip Enable pin (E bar) to a minimum of 2.2 volts will guarantee that the device enters the standby mode. Under this condition, the device becomes inactive, tristating all outputs, and will not respond to control input commands on the Write Enable or Output Enable pins. Data is preserved for as long as VCC is

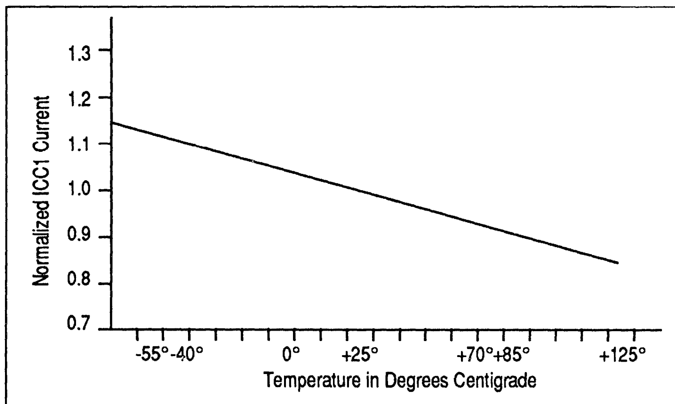


Figure 11. Operating Power Supply Current versus Temperature

present. The design of the address and data input buffers will have a profound effect upon the standby current variation with the input voltage levels, and the level of the Chip Enable pin. If we assume that the device is used in parallel with other parts, maybe EPROM or an I/O device, and one of the other devices on the Address and Data Bus is being accessed, the SRAM will be subjected to the same input switching waveforms as the selected device. It will be recalled that the basic inverter circuit consumes current in direct proportion to the frequency of input transition. The first stage of address input buffering on the SRAM would be an inverter. Consequently, the device would consume power in its input buffers due to being exercised on the address and data buses. A solution to this power waste is the "gated input". Additional NMOS and PMOS transistors are inserted in series and parallel respectively with the inverter transistors. The gates of these devices are coupled together and are controlled from the Chip Enable pin via an inverter.

When the SRAM is enabled, CE will be low, inputting a high voltage onto the gate of transistor Q1, switching it ON, and allowing the address input inverter circuit to operate. Meanwhile Q1, is switched OFF and does not interfere. As soon as CE is taken high, Q1 turns OFF, thus denying a vertical current path for the input inverter, and Q2 conducts, presenting the next input stage with a clean logic 1. This circuit will avoid any variation of standby current with the alteration of input frequency or voltage level. Depending upon the anticipated application of a device, it may or may not have this feature. The second variation of standby current is attributed to the actual voltage level of the CE pin. At 2.2 volts, the SRAM is just disabled, however due to input level characteristics of the input buffers and tri-state control a small vertical current flow through the CMOS inverter elements will exist as one of the complementary NMOS and PMOS transistors in each element will not be driven completely OFF. This is true for the entire CMOS peripheral circuitry that surrounds the memory array.

As CE is pulled further towards VCC, the TTL Standby power supply current will decrease and begin to approximate the CMOS Standby power supply current specification. From a designer's standpoint, little can be done to avoid toggling the address and data buses as this will be software/application defined. However, devices with input gating will remove this variable from the Standby current composition. Steps can be taken to ensure that the CE control is driven to as near VCC as possible. The extra power dissipated through a high value Chip Enable pull-up resistor during device operation will usually be compensated by the reduction in Standby current, if Chip Deselect voltages are only marginally above 2.2 volts. Figure 13 illustrates typical characteristics of a 32K x 8 SRAM for Standby and Data Retention modes.

Standby (CMOS Level) Power Supply Current, ICC3

ICC3 differs from ICC2 by specifying the following:

- Chip Enable is at VCC minus 0.2 volts minimum. i.e. 4.8V
- All Inputs are below 0.2 volts or above 4.8 volts.

In other words, all inputs are optimized for operation in a CMOS environment where waveforms are switched at over 85% of the rail voltage. The Standby condition ICC3 defines that Chip Enable control is driven hard OFF, and that there is no activity on the address and data buses. The effect of this definition is represented in Figure 13 where ICC2 and ICC3 can be compared. The

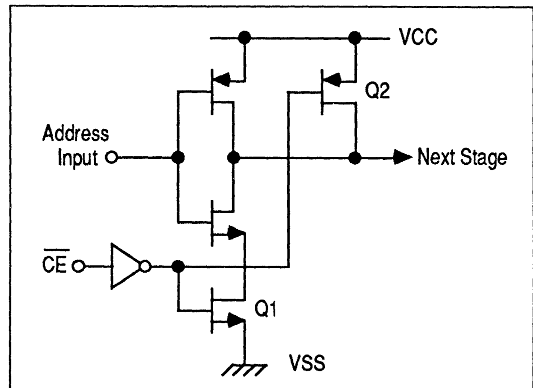


Figure 12. Gated Input Address Buffer

logarithmic scale diminishes the apparent difference between the two modes, but at room temperature ICC2 has a value approximately 1000 times that of ICC3. For ICC2, the dominant power consumer is the peripheral circuitry around the memory array. Only above +85°C does the effect of the negative temperature coefficient pull-up resistors of the 4T memory cell become apparent, with a slight increase at +125°C. This is in contrast to the ICC3 plot, where the peripheral circuitry will consume almost no current, and logarithmicpower consumption isattributabel to the memory array pull-up resistors in each cell.

It goes without saying that for the best characteristics power characteristics the designer should try to approach those condi-

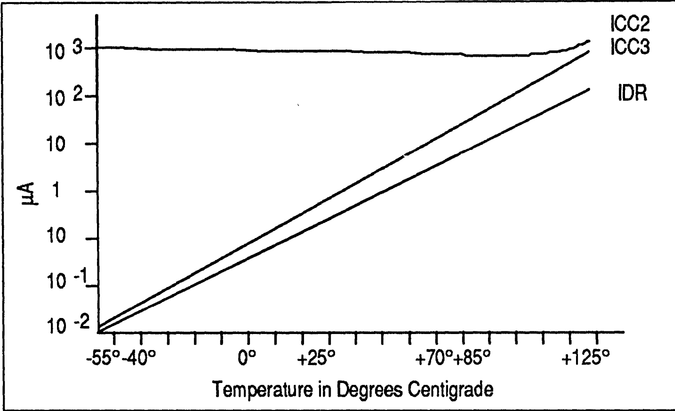


Figure 13. Standby and Data Retention Characteristics, 32Kx8

tions specified in ICC3 to keep power consumption to a minimum.

Data Retention Current, IDR

The Data Retention or Battery Backup Mode is a condition similar to ICC3, but running on a reduced VCC level of 2.0 volts. In this condition the SRAM will maintain the data most recently Written, but must not be enabled at this voltage as data corruption will result. Figure 13 includes the plot of IDR over the full military temperature range. As expected, it has a similar characteristic to ICC3. Special note should be taken when using SRAMs at elevated temperature in Data Retention Mode. The current drain is fairly insignificant up to +70°C, often only consuming 10μA or less. However, above this point the current drain rises quickly to, perhaps, 100μA at +125°C. It is therefore most important that the internal temperature characteristics of the equipment are known as accurately as possible to avoid excessive battery specifications or loss of data. The entry to and exit from the Data Retention mode must be carefully executed to ensure that the device is fully deselected before joint into Data Retention by reduction of the VCC voltage. Full VCC voltage must be restored before the device is re-selected again. Particular attention must be paid to timings TCDR and TR as defined in Figure 14. The specifications are given in product data sheets and are usually equivalent to the device Write Cycle time.

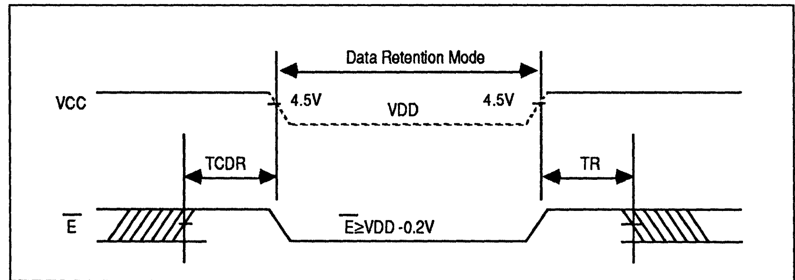


Figure 14. Data Retention Mode

High Speed and Low Power

EDI's Military High Speed CMOS Static RAMs are among the lowest power devices in the industry. The following information demonstrates these superior performance characteristics with actual test data.

High Speed

EDI offers the 256Kx1 and 64Kx4 CMOS SRAMs in High Speeds, from 25ns to 70ns.

All of these parts are available screened to full MIL-STD 883, Class B. EDI is also listed as an approved source on DESC-SMD drawings for 256Kx1 and 64Kx4 devices, both standard and low power.

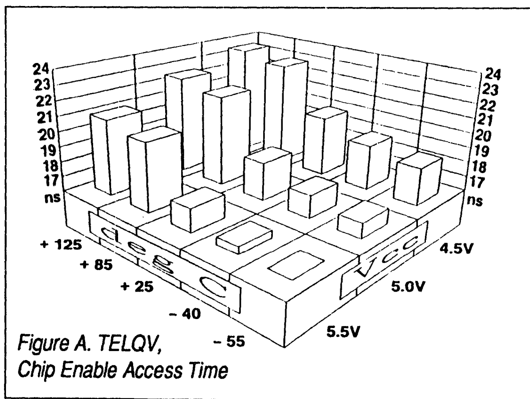


Figure A. TELQV, Chip Enable Access Time

Figure A shows a Military 256Kx1 device operating at sub-25ns range.

The scope pictures, Figures B and C, show test results from a typical 35ns, 256Kx1 device at room temperature with a standard test load of 30pF.

Low Power Consumption Regions

CMOS RAMs have five regions of operation, with a different power consumption for each region. These regions are designated in our data sheets as follows:

- DC Operating Current Region,
- Dynamic Operating Current Region, ICC1,
- Standby or TTL Current Region, ICC2,
- CMOS Full Standby Current Region, ICC3,
- Battery Back-up Standby or Data Retention Region, IDR.

The RAM is Enabled in the DC Operating Region, but not cycling. Its address, data and control inputs do not change.

In the Dynamic Operating Region the RAM is Reading and Writing at speeds up to its minimum rated read/write cycle time.

In TTL Standby the RAM is Disabled with address, data and control inputs at TTL levels, either static or cycling at the rated cycle time.

In CMOS Standby the RAM is Disabled and all inputs are at CMOS level (i.e., within 0.2 volt of VSS (ground) or VCC (power).

Battery Backup Standby is similar to CMOS Standby region, with a reduced power supply voltage of 2.0 or 3.0 volts rather than a the normal 5.0 volts.

Standard and Low Power Options

EDI RAM chips are divided into two types, standard (C) and low power (P). These part types are power dissipation test selections from a single product, similar to speed grade selections. The low power part is selected for low power standby operation and fully specified for the battery backup mode. The standard power part has relaxed power specifications in the form of higher limits on all ICC specifications, particularly in the standby power modes, and it is not specified for battery backup operation.

Because of its relaxed specifications, the standard power part

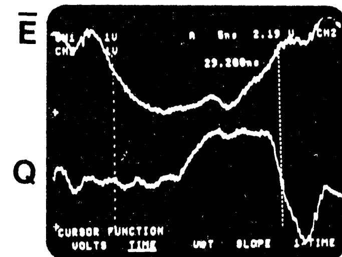


Figure B. Chip Enable Controlled Read Cycle

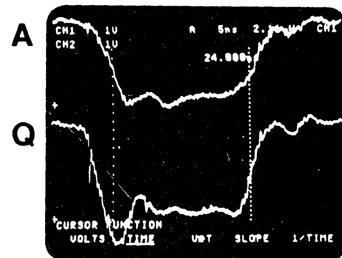
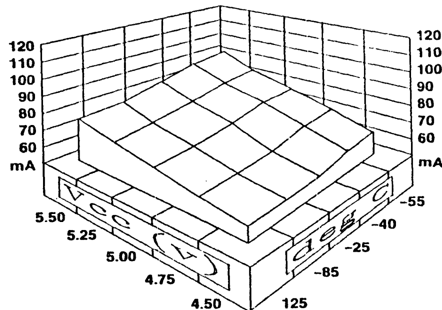


Figure C. Address Controlled Read Cycle



ICC1, Dynamic Operating Current
Figure D. 256Kx1

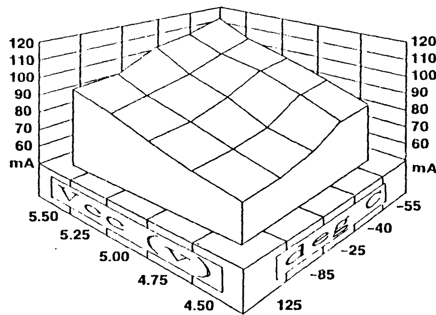


Figure E. 64Kx4

is used where very low standby power is not required, such as applications where the part is continually enabled.

Low Dynamic Operating Current

The Dynamic Operating Current, ICC1 specification applies when the RAM is cycling at its specified access time. Figures D and E illustrate a 256Kx1 and a 64Kx4, respectively, operating at 35ns against variables of VCC (power) and case temperature. Graphs for both the x1 and x4 devices are shown since the x4 output draws more current during Read cycles than the x1 device.

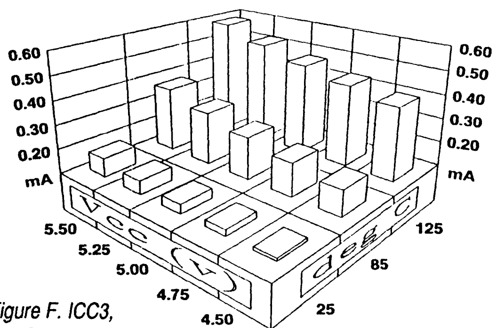


Figure F. ICC3, Full Standby Current

Standby Current

The CMOS Standby Current, ICC3, specification applies when the chip and all its inputs are static (i.e. Non-changing) at CMOS levels within 0.20 volts of VSS (Ground). In this state, only the RAM Array and leakage currents are drawn. The RAM array current is relatively independent of temperature, while the diode leakage is strongly temperature dependent, rising dramatically with temperature. Figure F illustrates Standby Operating Current consumption (ICC3) against variables of supply voltage and case temperature.

Battery Backup

Data Retention Characteristics, or Battery Backed Standby Currents, IDR, are specified for the Low Power, P Versions, of the 64Kx4 and 256Kx1 devices. Because of their low standby power these parts are often used as permanent memory where a battery is used to supply power to maintain data in the RAM when the system power is off. The Data Retention specification applies when the chip is disabled and all inputs are at CMOS levels (i.e., within 0.20 volts of VCC.) In battery backed up applications, the battery supplies a low voltage of 2 to 3 volts rather than the 5 volts of normal operation. This lower voltage allows use of a smaller battery, both because of the lower voltage for the same ampere per hour rating and because the RAM draws less current at the lower voltage.

When VCC is reduced to 2 or 3 volts the RAM is guaranteed to retain data stored at 5.0 volts, but may not function. In other words,

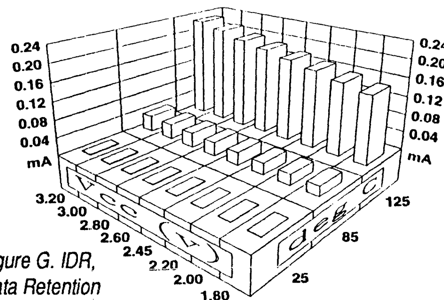


Figure G. IDR, Data Retention

it may or may not read or write reliably at these voltages. For this reason the chip is kept disabled while VCC is below 5.0 volts. When VCC is restored to 5.0 volts, full functional operation is restored and data will remain as it was before VCC was reduced.

The Low Power 256Kx1 and 64Kx4 devices are specified at a Data Retention Current of 500µA. Figure G shows Data Retention Current (IDR) against supply voltage and case temperature.

Military designers are taking advantage of new, higher density circuits to increase system performance. However, these new developments in increased circuit density and the elevated power requirements of advanced integrated circuits are creating demands for new hermetic package designs.

Initially, military component package designers were able to take advantage of the packaging developments used for commercial parts. When the commercial world moved to plastic packaging, however, the military world was left on its own to find solutions to their special requirements for hermeticity and operation across a wide temperature range.

Surface Mount Technology

With the advent of Surface Mount Technology in the early 1980s, a number of technical issues needed to be resolved. The first problem encountered was coefficient of thermal expansion (CTE) mismatch between leadless chip carriers (LCC) and printed circuit boards (PCB).

System designers could utilize two different approaches to solve the thermal cycling problem. First, PCB material which matched LCC/CTE was utilized; copper-invar-copper was a leading solution. However, this approach invariably adds excessive weight and cost to the system.

The second approach involved adding J-wire compliant leads to finished LCC devices. Static RAMs in 28 and 32 lead LCCs with lead lengths of at least 0.06 in. were found to be especially tolerant to temperature cycling tests. Again, the cost of adding leads, especially to devices with increasingly higher pin counts, and performing additional tests was often cost prohibitive. And, large, high pin count leadless chip carriers typically do not survive thermal cycling over the -55°C to +125°C temperature range specified by MIL-STD-883 when mounted directly onto printed circuits boards.

EDI was the first manufacturer to provide miltary customers with the density advantages of surface mount packaging with ceramic multichip modules; hermetic ceramic LCCs surface mounted onto a ceramic substrate provide a solution to the thermal coefficient mismatch problem. Modules also provide ease in manufacturing since the finished module is handled in the same manner as a standard DIP.

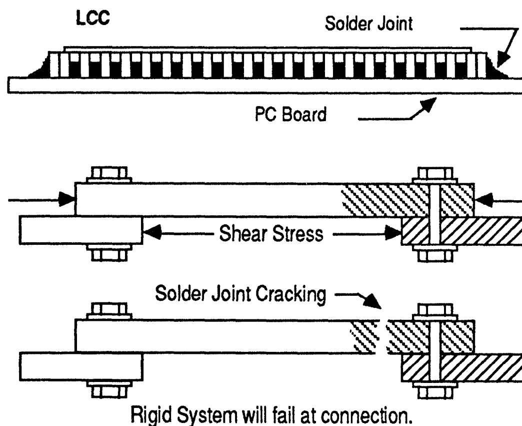
Further developments in packaging are needed, however. Board density and weight savings are just as crucial as high circuit density in many military applications, thus mandating a means of packaging that will further enhance the real estate and weight saving advantages of this technology.

Shear Stress Management

The shear stresses that build up inside of a solder joint during thermal cycling can reach thousands of pounds per square inch (psi) due to differences in the thermal coefficients of expansion between the board material and the package substrate as well as out-of-plane warping. Environmental shock and vibration can also increase not only shear stress, but z-axis stress in dense solder joints. These phenomena are often present in airborne systems that are subject to high G-forces and ground based systems that may be deployed in a variety of mission environments.

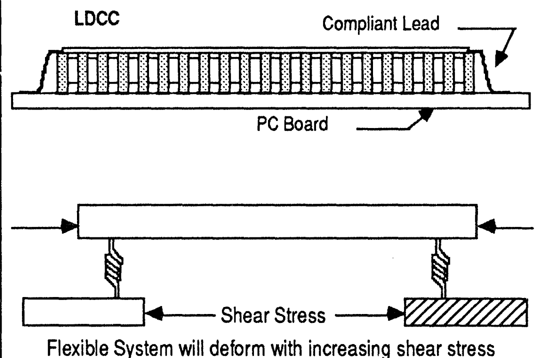
Small, rigid solder joints, like the ones holding leadless chip carriers (LCCs) to a printed circuit board (PCB), can be simply modelled as bolts mounting a beam between two supports. *(Figure A.)* As increased shearing force is applied to the beam, the concentrated load at the bolts will soon cause the beam to fall.

Figure A.



Rigid System will fail at connection.

Figure B.



Flexible System will deform with increasing shear stress

Consider the same beam mounted to the supports with coil springs. *(Figure B.)* The shear that causes failure in the rigid system merely cause the beam too be displaced, but not disconnected. In a similar manner, the leads in a compliant leaded device distribute what would be solder joint fracturing stress for an LCC into lead deformation energy, thus reducing the possibility of solder joint related component failure.

Thermal Management

Efficient thermal management may mean the difference between reliable operation and premature circuit failure due to heat related effects. An increasing number of military systems are being designed under a conduction cooling only restriction. A package with a cavity up die configuration allows the heat generated during operation to be directed downward through the package substrate.

Thermal management has recently been aided by employing advanced CAD layout techniques to properly thermally map a PCB layout. These techniques are utilized to avoid concentration of power dissipation in one area of the PCB.

Power dissipation imbalance can be reduced in memory subsystem design by incorporating EDI's multichip ceramic modules which contain EDI's low power CMOS SRAMs.

Real Estate Gains

Real estate savings of 16:1 have been realized by SMT against standard plated through hole (PTH) technology. By reducing profile height and double siding the printed circuit board, the total number of boards required to perform a systems function is reduced. The weight and space savings may them be utilized for other on board systems.

With the advent of submicron technology, smaller die sizes are allowing the use of skinny (300 mil) and thin (400 mil) DIPs. In addition, many different package types have been developed in the transition from through-hole to surface mount technology.

As shown below in Table 1, there are six basic package types used in the military hi-rel marketplace. SMT devices in the form of LCC and flatpack for low I/O packages, LCCs and LDCCs for the mid-I/Os and LLCCs and CGAs for high I/O Devices.

Table 1:

Package Type	Advantages	Disadvantages
LCC (Leadless Chip Carrier)	space, weight, low profile capacitance, induction performance	CTE mismatch, shear stress shock and vibration liabilities
Leaded Chip Carriers	lead compliant , space dimensions compatible with PLCC footprint compatible LCC	height
Flatpacks	CTE resolved, shear stress relief solder joint inspection	lead coplanarity, non-standard handling no standard lead form, (J bend vs gull wing) height vs LCC
CGA (Ceramic Grid Array)	high density, number of pins	solder joint inspection, cost
CERDIP	lower package cost , ease of handling	smaller cavity than sidebrazed
Sidebrazed DIP	larger cavity, ease of handling	higher package cost than CERDIP

The proliferation of packages is a result of the many issues that are being addressed.

For instance, surface mount technology is being used in airborne applications in an attempt to achieve smaller, lighter, compact systems. Some military and hi-rel applications have experienced problems in utilizing LCCs, however, due to problems associated with thermal coefficients of expansion mismatch, shear stress, and thermal management.

Attempts to overcome these issues have resulted in variety of solutions being employed including:

Table 2:

Solution	Advantages	Disadvantages
Solder Columns	height (Z Axis), density	non-standard manufacturing, lead coplanarity, maintenance
TCE matched boards (Cu-In-Cu, Kevlar, Ceramic)	fewer TCE problems	cost, weight
Edge clips or compliant lead attach via thermal companion board	lead compliancy, height (Z Axis) shear stress relief, solder joint inspection, high density	non-standard manufacturing flow, castellation uniformity required, lead coplanarity

As a supplier of both modules and monolithic devices over a wide range of densities, EDI is uniquely positioned to satisfy a variety of military/hi-rel packaging requirements. EDI's modules combine the density advantages of LCCs with the ease of use and cost benefits of DIPs. In addition, as SRAM monolithic device densities go beyond 1 megabit, EDI will be there with package offerings that are consistent with emerging industry standards to meet the changing needs of our customers.

Thermal Characteristics
Military CMOS SRAM Packaging

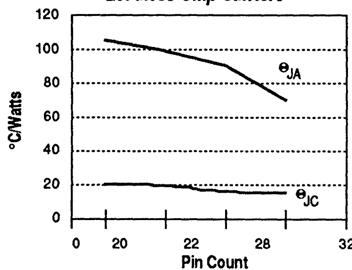
Power dissipation requirements have risen dramatically with the advent of high density VLSI devices. The mean time between failure of these devices has been shown to be exponentially related to the device operating temperature thus, thermal management on a package level is increasing in importance to military system designers. Effective thermal management requires extensive planning in the board layout stage of system level design. Specific, actual heat transfer characteristics of the packages in a system need to be known in advance of system design. In response to this demand for adequate and accurate engineering data to support thermal management on a board level EDI has taken extensive measurements of Θ_{JA} and Θ_{JC} on its DIP and LCC packages.

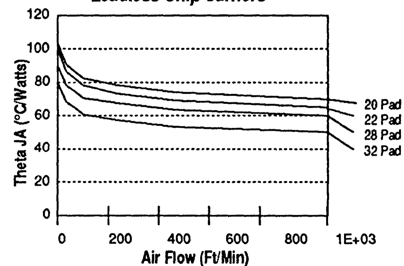
The thermal characterization technique used to measure thermal resistance utilizes the linear voltage drop vs. temperature change across a P-N junction of a semiconductor. Theta JC, resistance from junction to case, and Theta JA, resistance from junction to ambient, were measured in degrees Celsius per Watt (°C/W). This value determines the ability of a mechanical structure to transfer heat from a semiconductor device to the surrounding environment. Θ_{JR} is defined as the difference between the junction temperature and a reference point, ie. case or ambient, divided by the the power dissipation. the formula is expressed as :

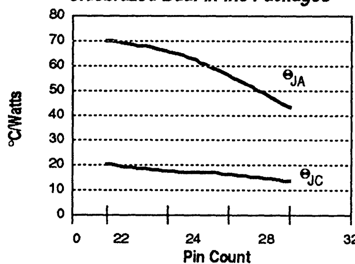
$$\Theta_{JR} = \frac{T_J - T_R}{P}$$

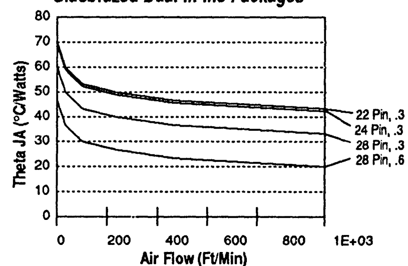
Θ_{JR} = Thermal Resistance, Junction to Reference Point in °C/W
T_J = Junction Temperature in °C
T_R = Reference Temperature in °C (ie. ambient or case)
P = Power Dissipation

The following figures graphically depict the thermal values of EDI's package families. The graphs illustrates the the results of thermal testing of various package types and variables, ie. pin counts, cavity sizes, die sizes. Actual test procedure is outlined in Appendix A.









Appendix A.

The technique used to measure thermal resistance takes advantage of the linear voltage drop versus temperature change across a P-N junction of a semiconductor. Thermal test die were used for our research. They have several sets of diode pairs to measure the temperature change of the die, and a resistor to dissipate power (simulating the power dissipation and heating characteristics of an actual die.) The following is a brief description of the procedure used for thermal resistance measurement:

1. The voltage drop of the sensing element (diode pairs) is calibrated. This is done by measuring the voltage drop at several temperatures with no power dissipated by the test die.
2. Measure voltage drop and thus temperature change) under various conditions with power applied to the dissipation resistor. For Θ_{JC} the measurement is taken while the part is immersed in a constant temperature bath. For Θ_{JA} the measurement is taken while the part is subjected to various air flow rates.
3. Thermal resistance is calculated as follows:

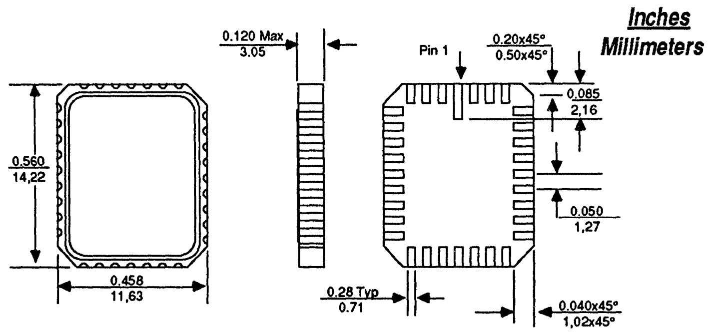
$$\Theta_{JC} = \frac{T_J - T_C}{P} \qquad \Theta_{JA} = \frac{T_J - T_A}{P}$$

Packaging Detail

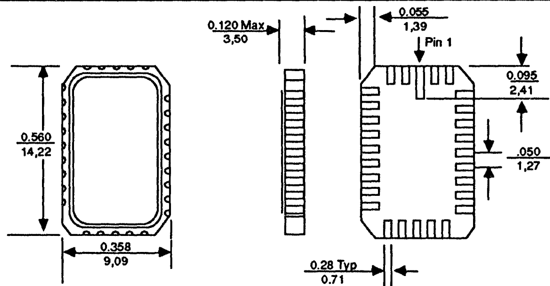
Monolithic LCC and CERDIP

Inches
Millimeters

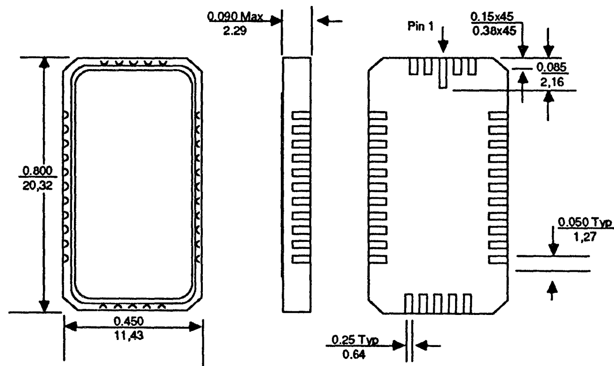
Package J or L, No. 12
(Package configuration in accordance with Mil-M-38510, Appendix C, No. D-12)
32 Pad Ceramic Leadless Chip Carrier



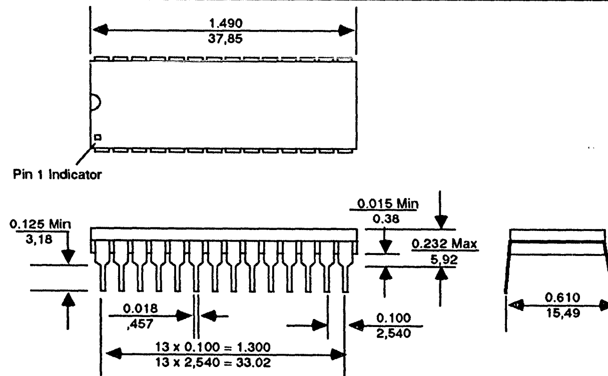
Package L, No. 14
(Package configuration in accordance with Mil-M-38510, Appendix C, No. D-11)
28 Pad Ceramic Leadless Chip Carrier



Package L, No. 100
32 Pad Ceramic Leadless Chip Carrier
(Preliminary)



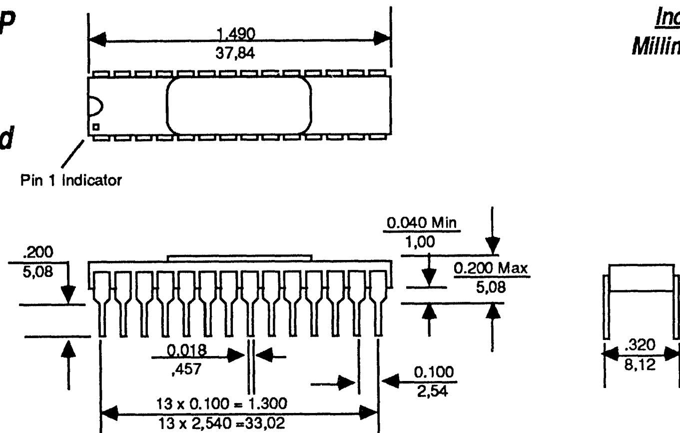
Monolithic DIPs
Package D, No. 70
(Package configuration in accordance with Mil-M-38510, Appendix C, No. D-10)
28 Pin CERDIP



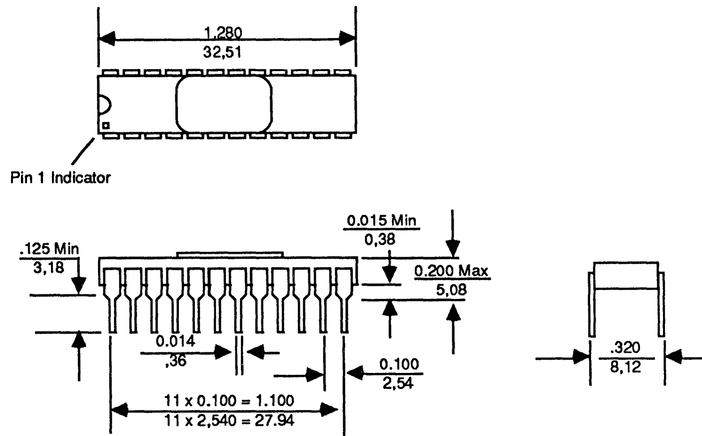
Inches
Millimeters

Monolithic, Sidebrazed DIP

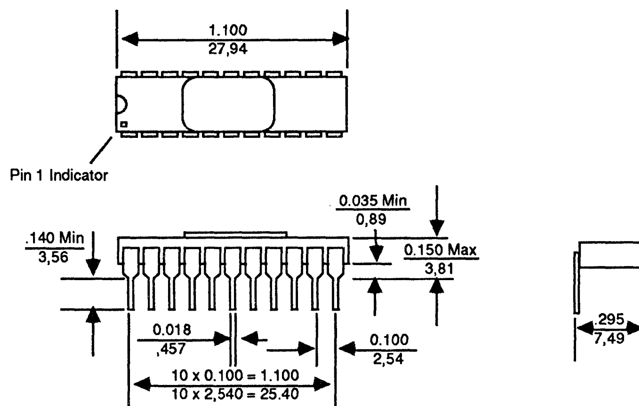
Package Q, No. 2
28 Pin Ceramic Sidebrazed Dual-in-line Package 300 mils Wide



Package Q, No. 3
(Package configuration in accordance with Mil-M-38510, Appendix C, No. D-9)
24 Pin Ceramic Sidebrazed Dual-in-line Package 300 mils Wide



Package Q, No. 6
22 Pin Ceramic Sidebrazed Dual-in-line Package 300 mils Wide



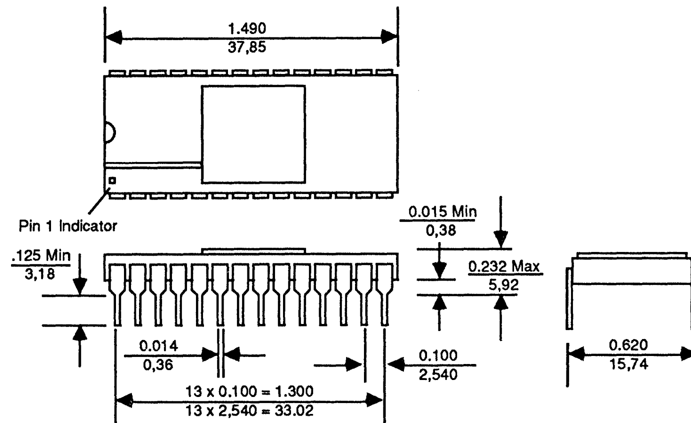
Packaging Detail

Monolithic Sidebrazed DIPs

Inches
Millimeters

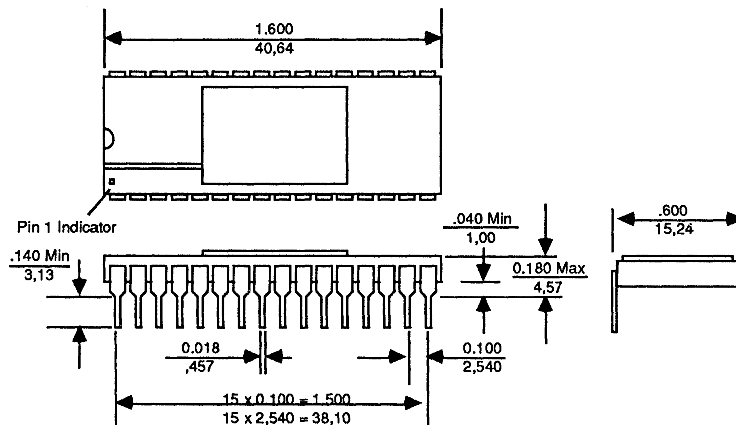
Package C or K, No. 8

(Package configuration in accordance with Mil-M-38510, Appendix C, No. D-10)
28 Pin Ceramic Sidebrazed Dual-in-line Package 600 mils Wide



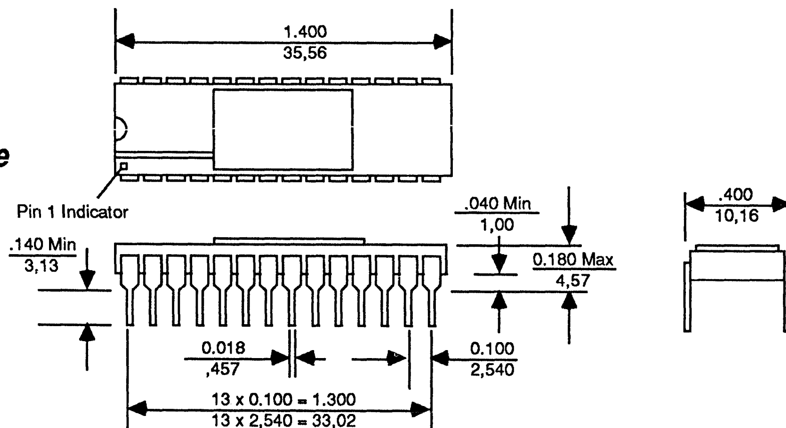
Package C, No. 9

32 Pin Ceramic Sidebrazed Dual-in-line Package 600 mils Wide



Package T, No. 101

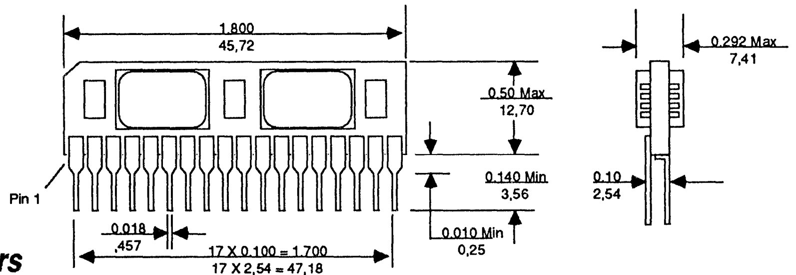
28 Pin Ceramic Sidebrazed Dual-in-line Package 400 mils Wide



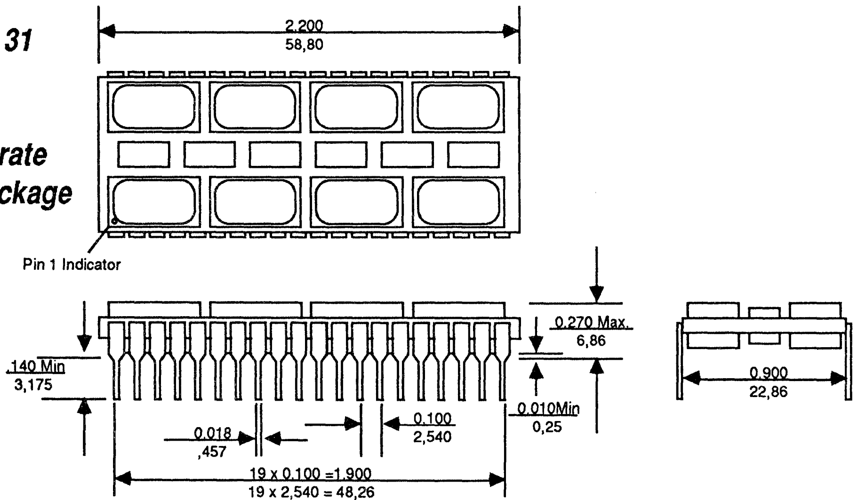
Ceramic Modules

Inches
Millimeters

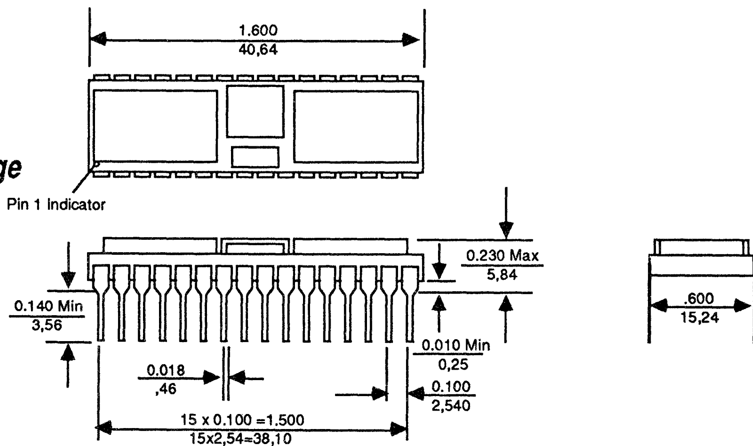
Package C, No. 19
36 Pin ZIP Module
Ceramic LCCs
Vertical
Ceramic Substrate
Dual-in-line Package
Pins on100 mil Centers



Package C, No. 31
40 Pin Module
Ceramic LCCs
Ceramic Substrate
Dual-in-line Package
900 mils Wide



Package C, No. 50
32 Pin Module
Ceramic LCCs
Ceramic Substrate
Dual-in-line Package
600 mils Wide

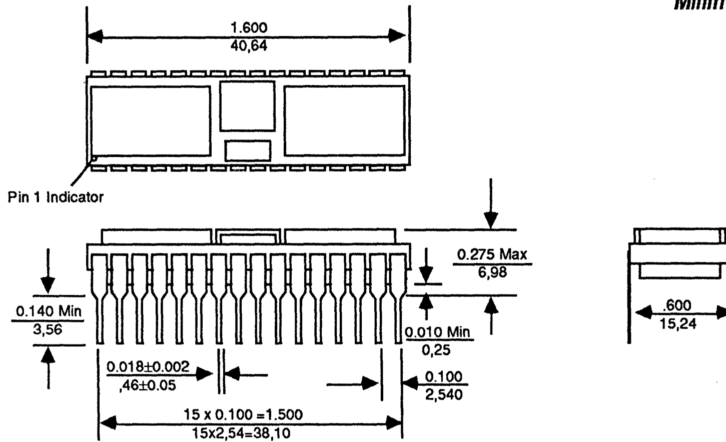


Packaging Detail

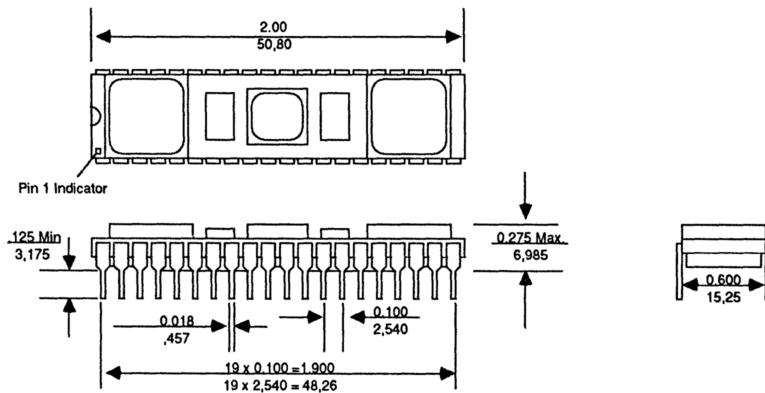
Ceramic Modules

Inches
Millimeters

Package C, No. 51
32 Pin Module
Ceramic LCCs
Ceramic Substrate
Dual-in-line Package
600 mils Wide



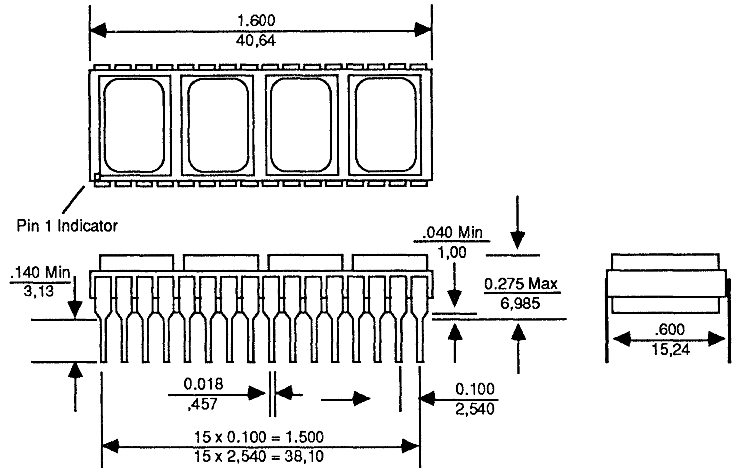
Package C, No. 66
40 Pin Module
Ceramic LCCs
Ceramic Substrate
Dual-in-line Package
600 mils Wide



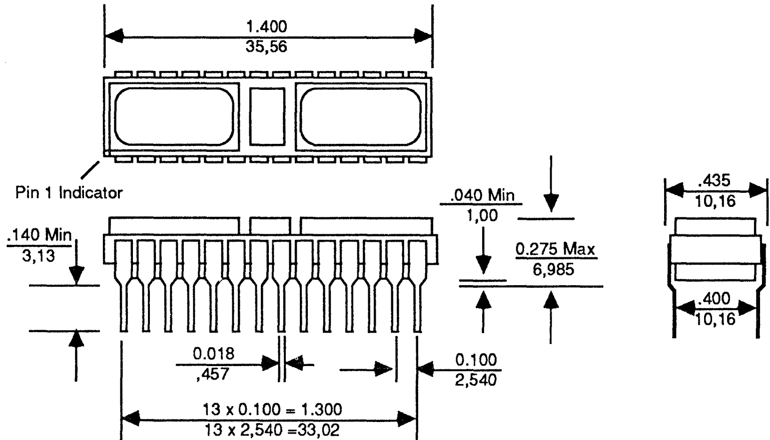
Ceramic Modules

Inches
Millimeters

Package C, No. 103
32 Pin Module
Ceramic LCCs
Sidebrazed Ceramic
Substrate
Dual-in-line Package
600 mils Wide



Package C, No. 104
28 Pin Module
Ceramic LCCs
Sidebrazed Ceramic
Substrate
Dual-in-line Package
on 400 mil Centers

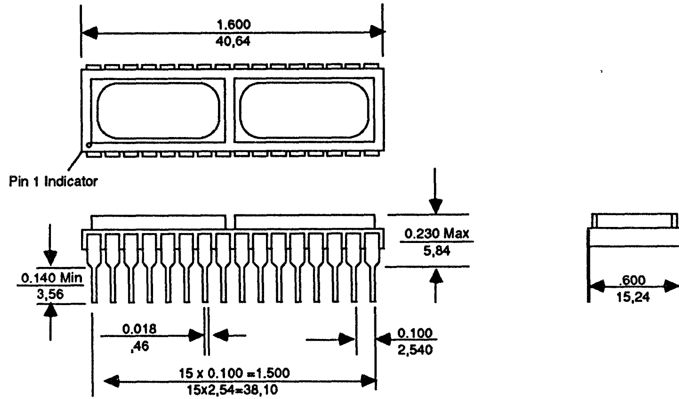


Packaging Detail

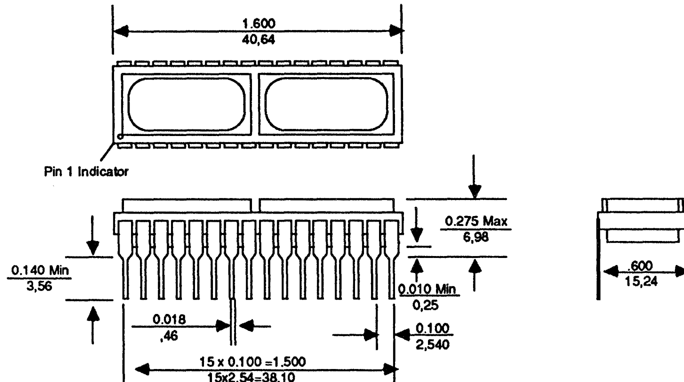
Ceramic Modules

Inches
Millimeters

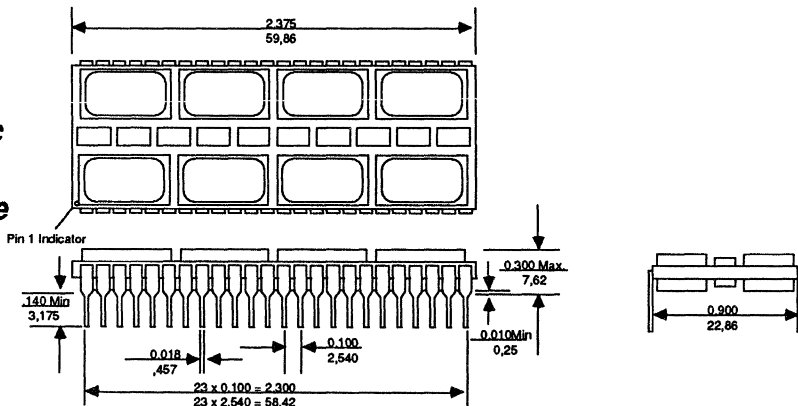
Package C, No. 105
32 Pin Module
Ceramic LCCs
Sidebrazed Ceramic
Substrate
Dual-in-line Package
600 mils Wide



Package C, No. 106
32 Pin Module
Ceramic LCCs
Sidebrazed Ceramic
Substrate
Dual-in-line Package
600 mils Wide



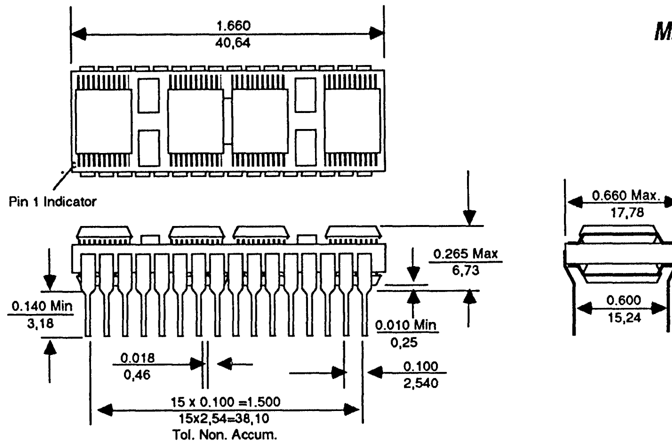
Package C, No. 109
48 Pin Module
Ceramic LCCs
Sidebrazed Ceramic
Substrate
Dual-in-line Package
900 mils Wide



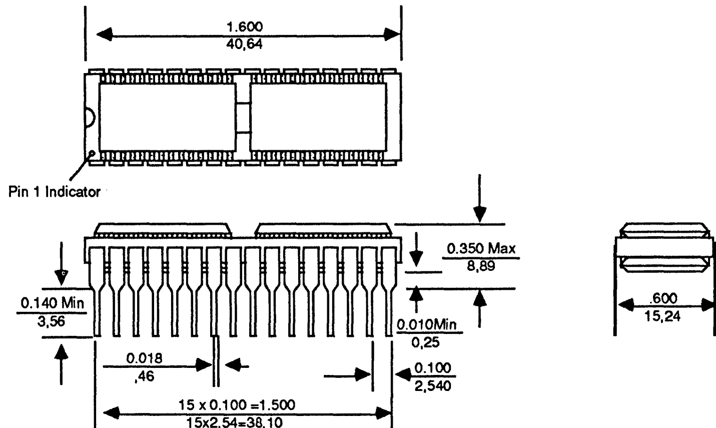
Inches
Millimeters

Plastic Modules

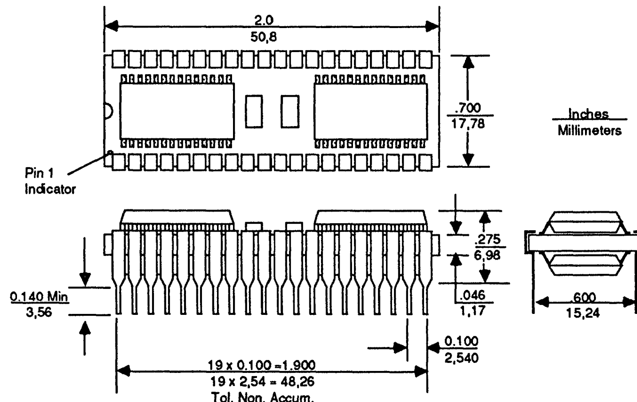
Package P, No 107
32 Pin Module
Plastic VSOP
Ceramic Substrate
Dual-in-line Package
600 mils Wide



Package P, No. 108
32 Pin Module
Plastic SOP
Ceramic Substrate
Dual-in-line Package
600 mils Wide



Package P, No. 111
40 Pin Module
Plastic SOP
FR4 Substrate
Dual-in-line Package
600 mils Wide



Packaging Detail

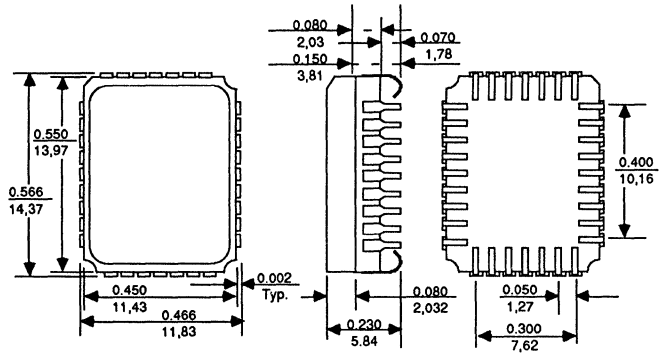
Advanced Packaging

Inches
Millimeters

Package V, No. 75

(Package configuration in accordance with Mil-M-38510, Appendix C, No. JC-11)

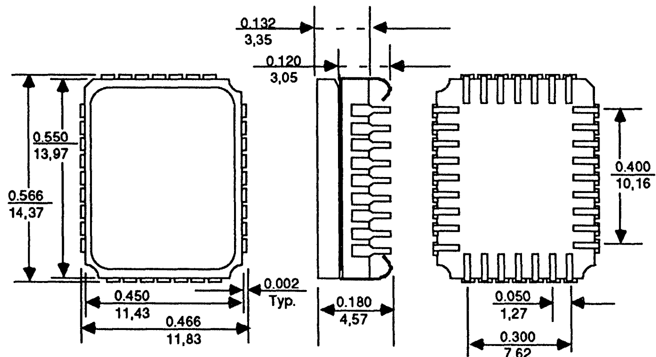
32 Pin (J-Lead) Ceramic Multilayered Chip Carrier



Package V, No. 78

(Package configuration in accordance with Mil-M-38510, Appendix C, No. JC-11)

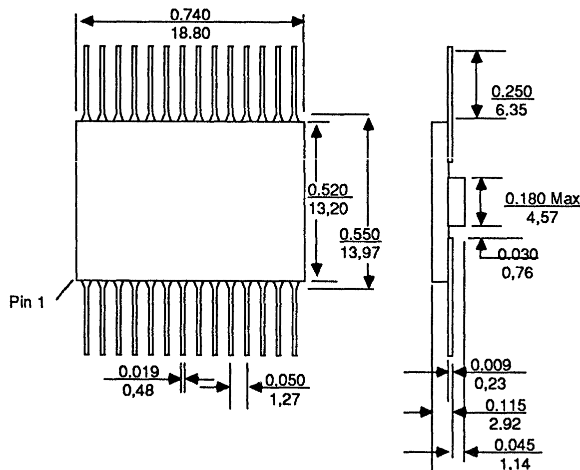
32 Pin (J-Lead) Cerquad



Package F, No. 79

(Package configuration in accordance with Mil-M-38510, Appendix C, No. F11-A)

28 Pin Flatpack



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