EPSON

SPC7223F2E

ATA Packet Interface & CD-ROM Decoder

- ●ATA Packet Interface for CD-ROMs SFF-8020
- ●Host data transfer rate supporting the PIO mode 4
- ●20-times CD-ROM decoding operation

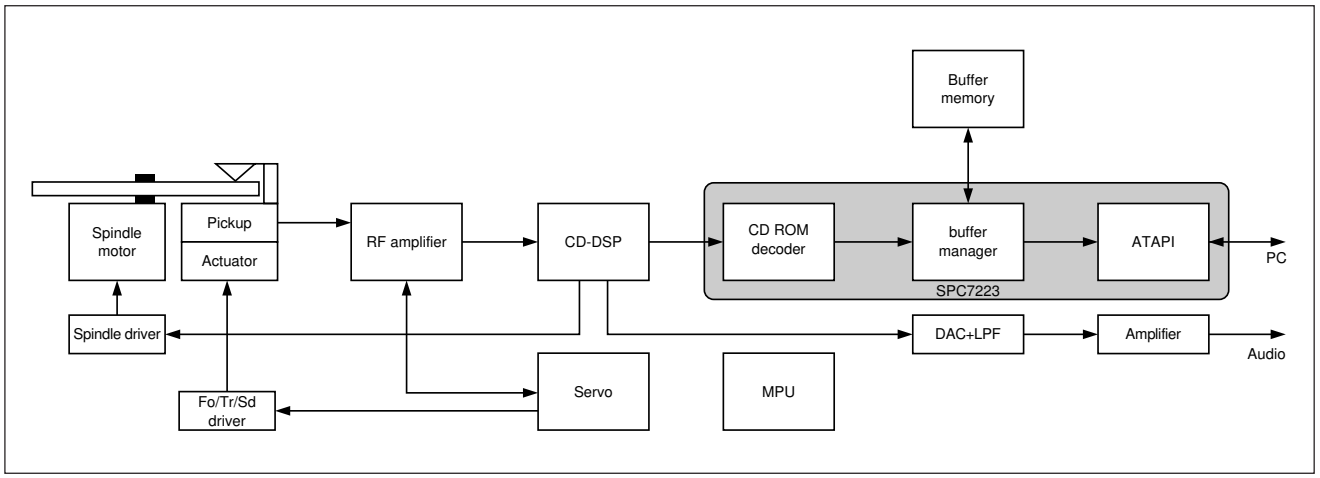
■ OUTLINE

SPC7223F2E are LSIs of CD-ROM decoder and host interface. These support decoding of 20-times speed and ATA packet interface function. These are supporting CD-ROM media conforming to CD-DA, CD-ROM and CD-ROM XA format.

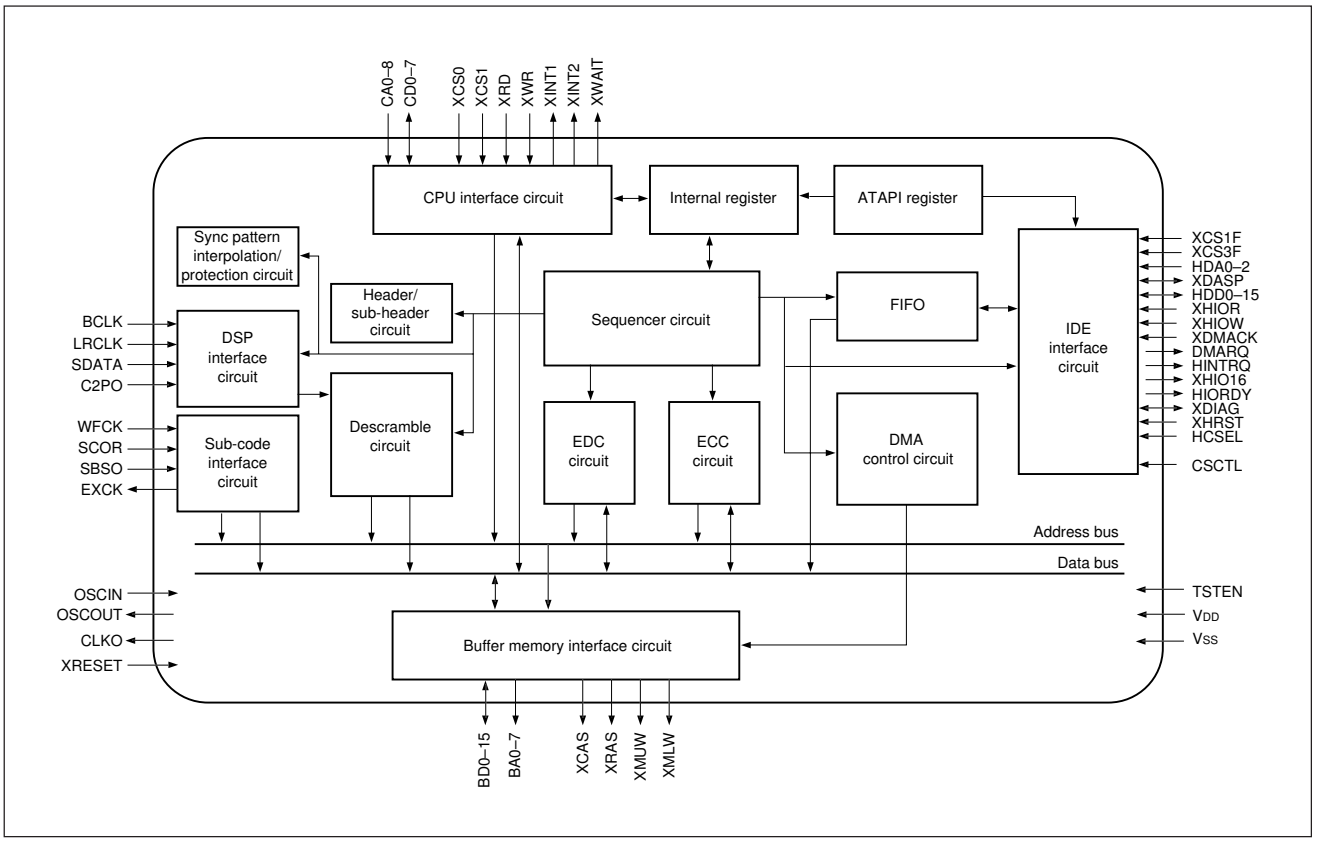
■ FEATURES

- ● Fully compatible with ATA Packet Interface specification SFF-8020i.
- ● Host data transfer rate of up to 16.6Mbyte/s.
  Supporting PIO mode 0-4, Single-word DMA mode 0-2, Multi-word DMA mode 0-2.
- ● 20-times speed decoding operations.
- ● Realtime CD-ROM ECC P-1word, Q-1word
- ● Supporting subcode data P-W interface
- ● Supporting various CD-DSP device interface
- ● Supporting high speed 8bit MPU interface
- ● Direct addressing 64Kword × 16 bit DRAM
- ● Built-in oscillation circuit 33.8688MHz
- ● Supply voltage 5.0V ± 10%
- ● Package QFP5-128pin

■ BLOCK DIAGRAM (CD-ROM driver)

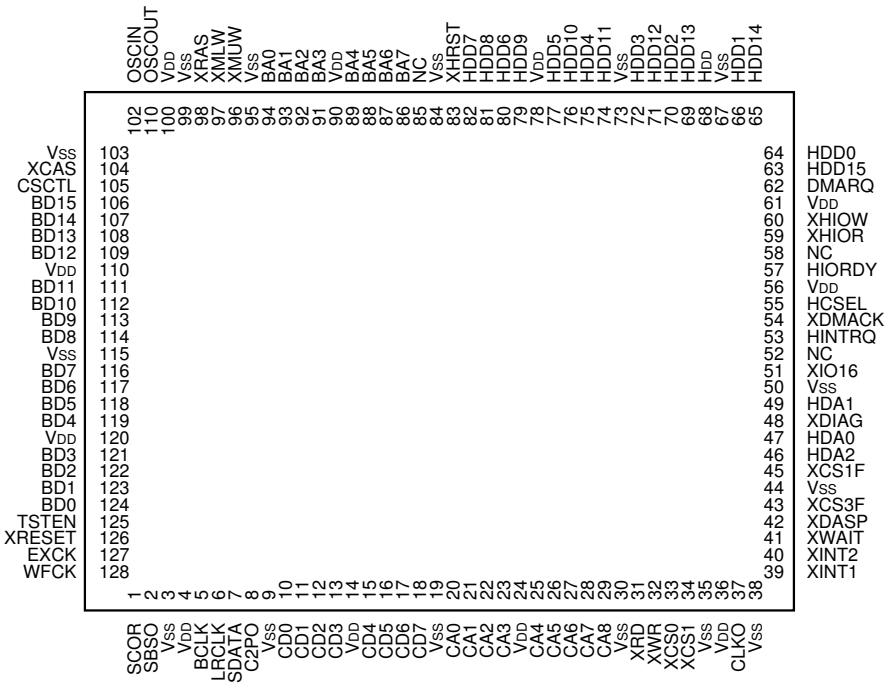


■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP5-128pin-S1



■ PIN ARRANGEMENT

"X" preceding a pin name indicates that the control signal is low active.

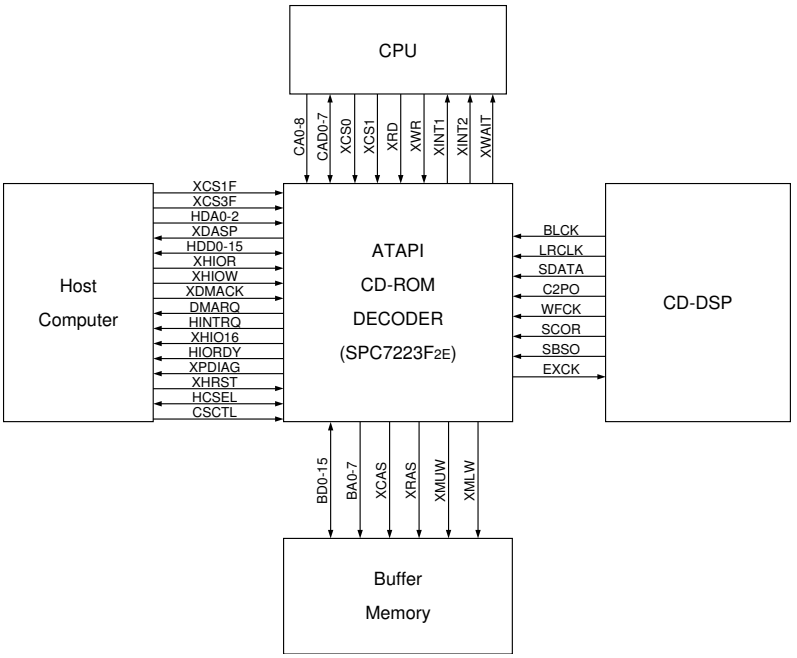
Pin No.	Pin names	I/O	Function
1	SCOR	O	Subcode sync S0+S1 input
2	SBSO	O	Subcode data serial input
3	VSS	P	GND pin
4	VDD	P	Power supply pin
5	BCLK	I	Bit clock input for SDATA signal strobe
6	LRCLK	I	LR channel clock
7	SDATA	I	Serial data input from DSP
8	C2PO	I	SDATA C2 pointer signal
9	VSS	P	GND pin
10	CD0	Ipu/O	CPU data buses
11	CD1	Ipu/O	(CD7 is MSB and CD0 is LSB)
12	CD2	Ipu/O	
13	CD3	Ipu/O	
14	VDD	P	Power supply pin
15	CD4	Ipu/O	CPU data buses
16	CD5	Ipu/O	
17	CD6	Ipu/O	
18	CD7	Ipu/O	
19	VSS	P	GND pin
20	CA0	I	CPU address buses
21	CA1	I	(CA8 is the MSB and CA0 is the LSB)
22	CA2	I	
23	CA3	I	
24	VDD	P	Power supply pin
25	CA4	I	CPU address buses
26	CA5	I	
27	CA6	I	
28	CA7	I	
29	CA8	I	
30	VSS	P	GND pin
31	XRD	I	CPU read strobe signal
32	XWR	I	CPU write strobe signal
33	XCS0	I	Chip select signal to access CPU register
34	XCS1	I	Chip select signal to access CPU buffer memory
35	VSS	P	GND pin
36	VDD	P	Power supply pin
37	CLKO	O	Clock output (33.8699 MHz/16.9344 MHz)
38	VSS	P	GND pin
39	XINT1	O	CPU interrupt request signal
40	XINT2	O	CPU interrupt request signal
41	XWAIT	Ood	CPU wait signal
42	XDASP	I/Ood	Drive active/drive 1 connection signal
43	XCS3F	Ipu	Control block register access Chip select signal
44	VSS	P	GND pin
45	XCS1F	Ipu	Command block register access Chip select signal

Pin No.	Pin names	I/O	Function
46	HDA2	Ipu	ATAPI register access address bus
47	HDA0	Ipu	ATAPI register access address bus
48	XDIAG	I/Ood	Diagnostics end signal
49	HDAI	Ipu	ATAPI register access address bus
50	VSS	P	GND pin
51	XIO16	Ood	Host computer 16 bits transfer enable signal
52	(N.C.)		
53	HINTRQ	Ots	Host computer interrupt request signal
54	XDMACK	Ipu	DMA transfer acknowledge signal from host computer
55	HCSEL	Ipu	Master/slave selection signal
56	VDD	P	Power supply pin
57	HIORDY	Ood	Host computer transfer cycle expansion signal
58	(N.C.)		
59	XHIOR	Ipu	Host computer read strobe signal
60	XHIOW	Ipu	Host computer write strobe signal
61	VDD	P	Power supply pin
62	DMARQ	Ots	Host computer DMA transfer request signal
63	HDD15	I/O	Host computer data buses (HDD15 is the SB and HDD0 is the LSB)
64	HDD0	I/O	
65	HDD14	I/O	
66	HDD1	I/O	
67	VSS	P	GND pin
68	VDD	P	Power supply pin
69	HDD13	I/O	Host computer data buses
70	HDD2	I/O	
71	HDD12	I/O	
72	HDD3	I/O	
73	VSS	P	GND pin
74	HDD11	I/O	Host computer data buses
75	HDD4	I/O	
76	HDD10	I/O	
77	HDD5	I/O	
78	VDD	P	Power supply pin
79	HDD9	I/O	Host computer data buses
80	HDD6	I/O	
81	HDD8	I/O	
82	HDD7	I/O	
83	XHRST	Ipu	Reset signal from host computer
84	VSS	P	GND pin
85	(N.C.)	O	
86	BA7	O	Buffer memory address buses (BA8 is the MSB and BA0 is the LSB)
87	BA6	O	
88	BA5	O	
89	BA4	O	
90	VDD	P	Power supply pin

Pin No.	Pin names	I/O	Function
91	BA3	O	Buffer memory address buses
92	BA2	O	
93	BA1	O	
94	BA0	O	
95	VSS	P	GND pin
96	XMUW	O	Buffer memory write strobe signal (high-order byte)
97	XMLW	O	Buffer memory write strobe signal (low-order byte)
98	XRAS	O	Buffer memory low address strobe signal
99	VSS	P	GND pin
100	VDD	P	Power supply pin
101	OSCOUT	O	Built-in oscillation circuit output pin
102	OSCIN	I	Built-in oscillation circuit input pin
103	VSS	P	Power supply pin
104	XCAS	O	Buffer memory column address strobe signal
105	CSCTL	Ipu	
106	BD15	Ipu/O	Buffer memory data buses
107	BD14	Ipu/O	(BD15 is the MSB and BD0 is the LSB)
108	BD13	Ipu/O	
109	BD12	Ipu/O	
110	VDD	P	Power supply pin
111	BD11	Ipu/O	Buffer memory data buses
112	BD10	Ipu/O	
113	BD9	Ipu/O	
114	BD8	Ipu/O	
115	VSS	P	GND pin
116	BD7	Ipu/O	Buffer memory data buses
117	BD6	Ipu/O	
118	BD5	Ipu/O	
119	BD4	Ipu/O	
120	VDD	P	Power supply pin
121	BD3	Ipu/O	Buffer memory data buses
122	BD2	Ipu/O	
123	BD1	Ipu/O	
124	BD0	Ipu/O	
125	TSTEN	Ipd	Test pin (Normally, this pin should be connected to GND pin)
126	XRESET	I	Reset signal
127	EXCK	O	Subcode read clock output
128	WFCK	O	Write frame clock input

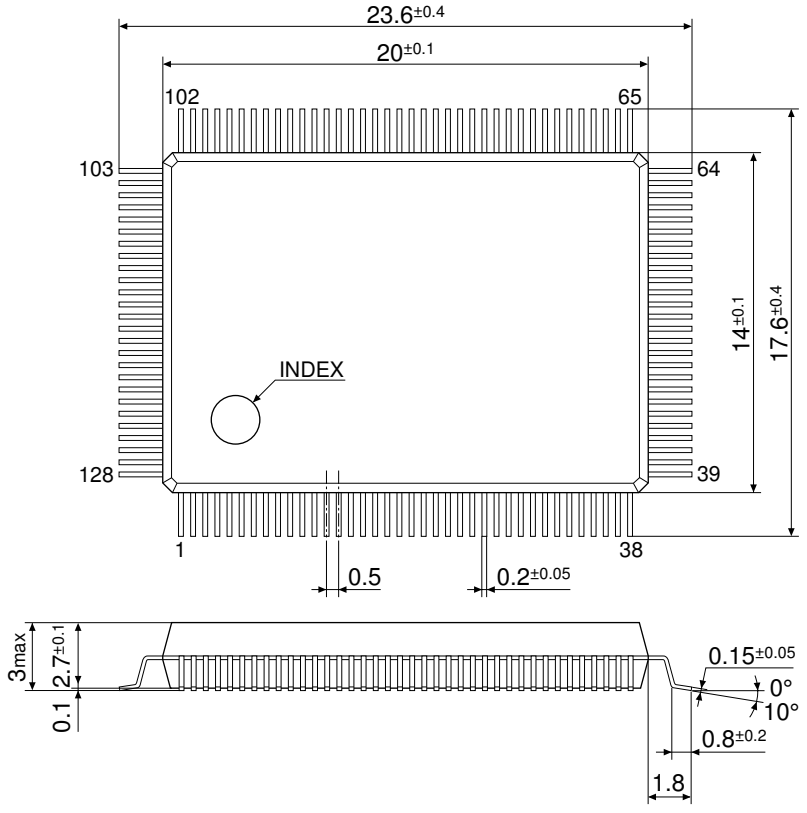
Note: I : Input
Ipu : Pull-up input
Ipd : Pull-down input
O : Output
Ood : Open drain output
Ots : 3-state output

■ EXAMPLE OF APPLICATION



■ PACKAGE DIMENTION

Plastic QFP5-128pin



Unit: mm

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