# CMOS Channeled Gate Arrays

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FÚJITSU

CMOS Channeled Gate Arrays

1989 Data Book



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> 3350 Scott Boulevard #24 Santa Clara, CA 95054

(408) 727-7707

FAX (408) 986-1947

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Design	Information
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UHB Series Unit Cell Library

AV Series Unit Cell Library

Sales Information

# **CMOS Channeled Gate Arrays** -

# 1989 Data Book

# Fujitsu Microelectronics, Inc. Integrated Circuits Division

3545 North First Street, San Jose, CA 95134-1804

Tel:

(408) 922-9000 FAX: (408) 432-9044 Telex: 910-320

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#### Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art electronic products.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

#### Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc., with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, Fujitsu Microelectronics has grown to include one R&D division, two marketing divisions, two manufacturing divisions and a subsidiary. Fujitsu Microelectronics offers a complete array of semiconductor products for its customers.

The R&D Division, APD (Advanced Products Division), using U.S.-based engineering, has jointly developed RISC for Sun Microsystems and Ethernet®, a chip set used in local area networks. APD also markets AFP, an adaptive filter processor, and EtherStar®, the first VLSI device to integrate both StarLAN® and Ethernet protocols into one device.

The Microwave and Optoelectronics Division markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors. The second marketing division, and the largest FMI division, is ICD (Integrated Circuits Division).

Memory and programmable devices marketed by ICD include DRAMs, EPROMs, EEPROMs, NOVRAMs, CMOS masked ROMs, bipolar PROMs, CMOS SRAMs, ECL RAMs, STRAMs (the first self-timed RAM), high speed ECL Logic, linear ICs and transistors.

ASIC products offered by ICD include bipolar gate arrays, CMOS gate arrays, and standard cells. Customer support and customer CAE training for ASIC designs is available through FMI's five design centers: San Jose, Dallas, Atlanta, Chicago, and Boston, with additional design centers planned for Gresham, Oregon and Irvine, California.

Microcomputer and communications products offered by ICD include 4-bit MCUs, 8- and 16-bit MPUs, SCSI and controllers, DSPs, prescalers, and PLLs.

Fujitsu Microelectronics' manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, FMI opened the Gresham Manufacturing Division to manufacture ASIC products. This facility has one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

#### Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a totally owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Western Europe. The wide range of IC products, LSI memories and, in particular, gate arrays are noted throughout Western Europe for design excellence and unmatched reliability. Five branch offices to support Fujitsu's semiconductor operations are located in Munich, London, Paris, Stockholm, and Milan.

#### Fujitsu Microelectronics Ireland, Ltd. (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME supplies 64K/256K DRAMs, 64K CMOS/NMOS EPROMs, 256K EPROMs, and other LSI memory products.

#### Fujitsu Microelectronics, Ltd. (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with a highly sophisticated CAD system to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

#### Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Center)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

- ® Ethernet is a registered trademark of Xerox Corporation.
- EtherStar is a trademark of Fuiltsu Microelectronics, Inc.
- StarLAN is a trademark of AT&T.

#### **Preface**

Fujitsu Microelectronics introduced its first commercially available gate array, a bipolar chip called the B200, in 1974 (Fujitsu had been making them for internal use since 1972). Over the years it has been so popular that it is regarded as the world's most widely implemented gate array. Since that first array, Fujitsu has produced over 9000 successful bipolar and CMOS custom designs.

Fujitsu designs are successful because they are implemented using the most advanced design verification CAD systems available, allowing the production of chips with 90% cell utilization (more functional logic per chip than the industry standard) and one of the highest performance records in the industry.

This data book provides you with information necessary to choose an application specific IC (ASIC) design using one of Fujitsu's advanced CMOS channeled gate array technologies (AV, AVB, AVL, AVM, and UHB). The data book describes Fujitsu's CMOS channeled gate array technologies, explains the benefits and specifications applicable to each, and outlines the process by which logic and circuit designers create a chip. Except where noted, the material presented in this data book is common to all of Fujitsu's CMOS channeled technologies. The device (unit cell) libraries for these channeled gate array technologies are included at the end of this volume. The second volume in this series provides the same information for Fujitsu's channel-less or sea-of-gates ASIC technologies.

Fujitsu has pioneered and maintained a technological lead in the production of bipolar as well as CMOS ASIC devices; data books describing Fujitsu's other ASIC product families, as well as any other technical or sales-related information, may be obtained from any Fujitsu Technical Resource Center or Sales Office listed at the end of this book or by calling or writing Fujitsu Microelectronics Inc., 3545 North First Street, San Jose, CA 94135–1804, (408) 922–9000.

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#### **Fujitsu ASIC Products Listing**

#### **CMOS Channeled Gate Arrays Data Book**

#### UHB Series High Drive Gate Arrays — 1.5μ, 0.9 ns typical delay

Description	Name	Device Part Number
336 Gates, 58 I/O	C330UHB	MB625xxx
530 Gates, 64 I/O	C530UHB	MB624xxx
830 Gates, 74 I/O	C830UHB	MB623xxx
1,233 Gates. 88 I/O	C1200UHB	MB622xxx
1,724 Gates, 102 I/O	C1700UHB	MB621xxx
2,220 Gates, 115 I/O	C2200UHB	MB620xxx
3,066 Gates, 140 I/O	C3000UHB	MB606xxx
4,174 Gates, 155 I/O	C4100UHB	MB605xxx
6,000 Gates, 155 I/O	C6000UHB	MB604xxx
8,768 Gates, 188 I/O	C8700UHB	MB603xxx
12.734 Gates, 220 I/O	C12000UHB	MB602xxx

#### AV Series CMOS Gate Arrays — $1.8\mu$ , 1.4 ns typical delay

#### AV Series High Speed Gate Arrays

Description	Name	Device Part Number
2,640 Gates, 106 I/O	C2600AV	MB654xxx
3,900 Gates, 127 I/O	C3900AV	MB653xxx
5,022 Gates, 127 I/O	C5000AV	MB652xxx
6,664 Gates, 160 I/O	C6600AV	MB651xxx
8,000 Gates, 160 I/O	C8000AV	MB650xxx

#### AVB Series High Drive Gate Arrays

Description	Name	Device Part Number
357 Gates, 38 I/O	C350AVB	MB675xxx
549 Gates, 48 I/O	C540AVB	MB674xxx
852 Gates, 58 I/O	C850AVB	MB673xxx
1,245 Gates, 68 I/O	C1200AVB	MB672xxx
1,674 Gates, 74 I/O	C1600AVB	MB671xxx
2,052 Gates, 88 I/O	C2000AVB	MB670xxx

#### AVL Series Low Power Gate Arrays — 2.3 $\mu$ , 2.9 ns typical delay at 3V

Description	Name	Device Part Number
357 Gates, 38 I/O, 3 Volt Operation	C350AVL	MB685xxx
549 Gates, 48 I/O, 3 Volt Operation	C540AVL	MB684xxx
852 Gates, 58 I/O, 3 Volt Operation	C850AVL	MB683xxx
1,245 Gates, 68 I/O, 3 Volt Operation	C1200AVL	MB682xxx
1,674 Gates, 74 I/O, 3 Volt Operation	C1600AVL	MB681xxx
2,052 Gates, 88 I/O, 3 Volt Operation	C2000AVL	MB680xxx

#### AVM Series Gate Arrays with Memory

Description	Name	Device Part Numb
1,564 Gates with 4.6K ROM or 2.3K RAM, 107 I/O	C1502AVM	MB662xxx
2,375 Gates with 2K ROM or 1K RAM, 117 I/O	C2301AVM	MB661xxx
4,087 Gates with 4.6K ROM or 2.3K RAM, 120 I/O	C4002AVM	MB660xxx

#### **CMOS Channelless Gate Arrays Data Book**

#### AU Series CMOS Series Gate Arrays $-1.2\mu$ , 0.6 ns typical delay

Name	Device Part Number
C10KAU	MB637xxx
C15KAU	MB636xxx
C20KAU	MB635xxx
C30KAU	MB634xxx
C40KAU	MB633xxx
C50KAU	MB632xxx
C75KAU	MB631xxx
C100KAU	MB630xxx
	C10KAU C15KAU C20KAU C30KAU C40KAU C50KAU C75KAU

#### **BiCMOS Gate Arrays Data Book**

#### BC Series BiCMOS Gate Arrays - 1.5μ/1.4μ, 0.65 ns typical delay

Description	Name	Device Part Number
645 Gates, 52 I/O	BC400	MB211xxx
1,218 Gates, 72 I/O	BC800	MB212xxx
1,872 Gates, 96 I/O	BC1200	MB213xxx
3,240 Gates, 112 I/O	BC2000	MB214xxx

#### BC-H Series BiCMOS Gate Arrays — $1.0\mu/0.5\mu$ , 0.45 ns typical delay

4.312 Gates, 96 I/O	BC4000H	MB221xxx
8,160 Gates, 128 I/O	BC8000H	MB222xxx
11,968 Gates, 160 I/o	BC12000H	MB223xxx
16 720 Gates 200 I/O	BC16000H	MR224xxx

#### **ECL Gate Arrays Data Book**

#### ET Series ECL Gate Arrays — $1.0\mu$ , 220 ps typical delay

Description	Name	Device Part Number
1,056 Gates, 64 I/O	ET750	MB121Kxxx
2,112 Gates, 88 I/O	ET1500	MB123Kxxx
4,224 Gates, 120 I/O	ET3000	MB125Kxxx
6,160 Gates, 120 I/O	ET4500	MB128Kxxx
2,640 Gates, 120 I/O with 4.6 Kb RAM	ET2004M	MB181/191xxx
2,640 Gates, 136 I/O, with 9.2 Kb RAM	ET2009M	MB182/192xxx
3.960 Gates, 136 I/O, with 4.6 Kb RAM	ET3004M	MB183/193xxx

#### H Series ECL Gate Arrays $-0.5\mu$ , 100 ps typical delay

9,856 Gates, 200 I/O	ET10000H	MB147/157xxx
9,856 Gates, 300 I/O	E10000H	MB148/158xxx
4,928 Gates, 200 I/O, with 5.1Kb RAM	ET5005HM	MB185/195xxx
128 Gates, 23 /I/O	E128H	MB1800
32 Gates, 13 I/O	E32	MB1700
128 Gates 16 I/O	E128	MB1600

#### **CMOS Standard Cell Data Book**

AU Series Standard Cells —  $1.2\mu$ , 0.6 ns typical delay

# Section 1

# Design Information

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#### Chapter 1 - Fujitsu CMOS Products

#### Contents of This Chapter

- 1.1 Introduction
- 1.2 CMOS Technology for ASICs
- 1.3 CMOS Gate Array Structure
- 1.4 Fujitsu's CMOS Channeled Gate Array Technologies: UHB and AV Data Sheets

#### 1.1 Introduction

This section of the data book gives an overview of CMOS technology and introduces the CMOS channeled gate array technology families developed by Fujitsu to implement ASIC designs.

#### 1.2 CMOS Technology for ASICs

ASICs (Application Specific Integrated Circuits) are large scale integrated circuits that provide customers with made-to-order functions. These ICs implement the unique value designed into customer products by producing custom semiconductor designs that allow customers to take advantage of perceived market opportunities in a timely manner. The customized solutions offered by ASICs combine the power of personalized electronics and the advantage of increased system efficiency.

CMOS technology has long been chosen for ASIC applications because of its low power and high density characteristics. Advancing process technology and new production and fabrication techniques have now allowed device speed to increase to the point where it is competitive with bipolar devices. Fujitsu CMOS gate arrays are manufactured using advanced silicon gate technology utilizing two-layer and three-layer metal. This fabrication process yields parts that:

- a) require very low power dissipation (typically less than 500 mW per channeled array)
- b) operate at speeds equaling existing bipolar technologies
- c) feature higher gate densities than competing bipolar devices
- d) use a single power supply of 5 volts or less
- e) provide top-grade noise immunity and programmable logic levels compatible with TTL and CMOS logic families

#### 1.3 CMOS Gate Array Structure

Fujitsu CMOS gate arrays are configured in a matrix of basic cells in the center of the chip with input-output (I/O) cells on the device periphery. One basic cell is equivalent to a two-input NAND gate. The custom logic function is realized by interconnecting basic cells with double-layer metalization (or triple-layer metalization for the largest arrays). Fujitsu's gate array products are fabricated using a twin-tub polysilicon CMOS process to produce high-speed, high-density arrays consisting of 300 to 100,000 basic cells.

#### 1.3.1 The Basic Cell

The basic cell of Fujitsu's CMOS gate array is a common building block consisting of one pair of P-channel and one pair of N-channel MOS transistors interconnected as shown in Figure 1-1.

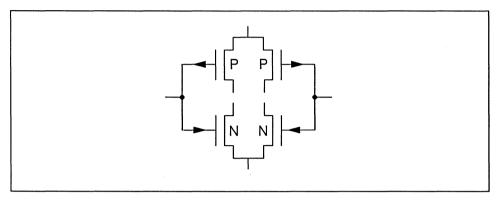


Figure 1-1. The Basic Cell

Since this is a "generic" basic cell, no connections are shown to the power supply (+5 volts), to ground, or to the two common control gate terminals of the circuit. These connections are made as required during the metalization phase of the manufacturing process. All CMOS gate arrays are built up of basic cells.

Figure 1-2 shows a schematic representation of the basic cell with the addition of the custom metalization required to convert the generic basic cell into a two-input NAND gate.

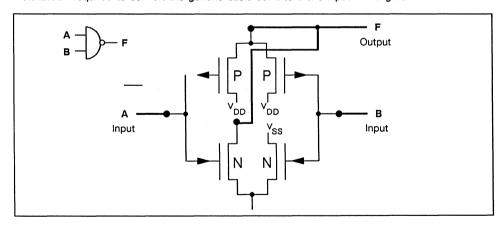


Figure 1-2. The Basic Cell as a 2-Input NAND Gate

#### 1.3.2 Basic Cell Construction

Basic cell construction varies somewhat among Fujitsu's CMOS technologies; however, an explanation based on AV technology provides a good model of how a basic cell is fabricated in any

of the CMOS families. In AV, the basic cell is constructed from an N-type silicon substrate upon which a P-well is deposited. The surface of the substrate is then covered with a thin layer of silicon dioxide (glass) and two strips of polysilicon are deposited perpendicular to the P-well and geometrically parallel. (Polysilicon is a silicon-based compound chemically altered so that it has good electrical conduction properties.) The polysilicon strips serve as the gate control elements of the basic cell and also as the two electrical interconnections between the sources of the P and N transistor pairs. See Figure 1-3.

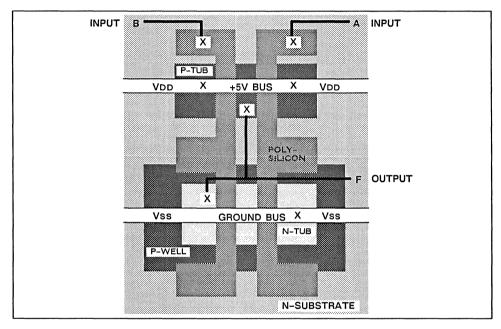


Figure 1-3. Physical Construction of the Unit Cell NAND Gate

The silicon dioxide layer is then stripped away from all areas of the substrate not protected by polysilicon. In two separate steps, the N-type and the P-type material of the twin tubs is diffused onto the substrate.

For the next step, N-type material is diffused or implanted into the P-well that was previously laid down. It straddles the two strips of polysilicon close to their ends. The polysilicon resists the diffusion, which results in the formation of three pads of N-type material separated by the two strips of polysilicon (self-aligned processing). The center pad of N-type material serves as a common drain terminal for both N-channel transistors. The outer pads are the separate source elements.

Then the P-type material is deposited on the the N-type substrate straddling the two polysilicon strips. Similarly the center pad of P-type material forms the common source connection for both P-channel transistors. The basic cell is then converted to a unit cell by application of a custom metalization pattern that connects (or wires) various points of the basic cell, or a number of basic cells, together. Figure 1–3 shows the structure of a basic cell configured as a NAND gate after metalization (represented by the solid bold line connections) has been laid down.

Some unit cells require two or even three layers of metal to be applied. Such layers are separated by an insulating layer of silicon dioxide. Interconnections between the metal layers are made by means of "vias" passing through the glass.

#### 1.3.3 Structure of the Chip

The arrangement of the basic cells on the chip differs according to the technology. The fundamental chip layout is a matrix of basic cells surrounded by a perimeter of I/O cells. Basic cells can be arranged in single columns, with the channels between the columns used for routing unit cell interconnections, as in AV, AVB, AVL, and AVM technologies, or in double columns as in UHB technology. See Figure 1–4. The sea-of-gates technologies are constructed with no wiring channels between the double columns, allowing the wiring to go over the cells, rather than between the cells. See Figure 1–5. The channel-less or sea-of-gates technologies are covered in a separate data book.

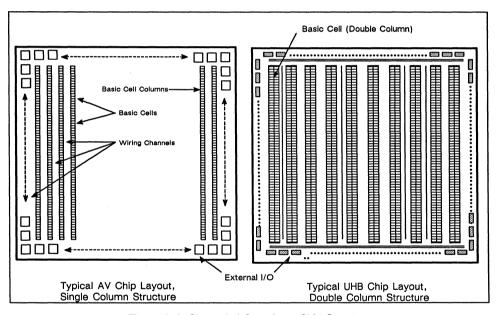


Figure 1-4. Channeled Gate Array Chip Structure

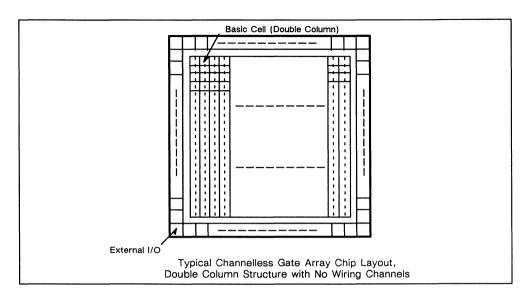


Figure 1-5. Channelless Gate Array Chip Structure

Larger gate arrays depart from the fundamental layout scheme by partitioning the basic cell matrix into four blocks. In some instances the designer may define the size of each block within certain limitations, while in other cases the block size is fixed. The purpose of chip partitioning is to improve speed performance by controlling wire length. Each block can be looked at as a small gate array, with four such gate arrays inside one package. (Smaller arrays exhibit less delay than larger ones.) In some technologies, AVM, for example, a block can be devoted to RAM or ROM for special applications requiring memory.

#### 1.3.4 Basic Cell Arrangement

Basic cells can be arranged in any of the following configurations:

- (a) Fundamental logic function units called unit cells (e.g. NAND gate, flip-flop, etc.).
- (b) User macros, which are composed of unit cells to form higher level logic block functions (e.g., shift register or decoder). Such blocks are user-defined and may contain any unit cell configuration.
- (c) RAM macros, which are available in seven basic configurations.

#### 1.3.5 I/O Cells

I/O cells are input/output buffer cells located on the periphery of the basic cell matrix (and memory block, if one is present). I/O cells are usually not included in the basic cell count. These buffer cells convert external voltage levels into internal CMOS levels. The output buffers provide a sufficient voltage level to drive TTL components but the input buffers must convert TTL levels to CMOS levels when appropriate.

#### 1.3.6 Macros

Different macros are available for each technology group. For a list of available macros for each technology, contact any of the Fujitsu Technical Resource Centers listed in the back of this volume.

#### 1.4 Fujitsu's CMOS Channeled Gate Array Technologies

Fujitsu offers over 50 different CMOS gate array devices, fabricated with advanced silicon gate technology. Fujitsu's channeled CMOS gate arrays include the technology options described in detail in the data sheets that follow:

- UHB Series CMOS Gate Arrays
- AV Series CMOS Gate Arrays (including AVB, AVL, and AVM)

Complete information on Fujitsu's channel-less CMOS gate array families is provided in a separate data book.

All offer the same fast turnaround on design, simplified customer interface, full support by Fujitsu ViewCAD system design software if requested, full design support of other major CAE workstations, and a wide variety of packaging options.

Fujitsu's newest channeled gate array technology, QCL (Quickly Customized Logic) offers the UHB cell library and UHB compatibility using AU technology with one level of metalization to provide ASIC designers with a product proven reliability with an especially fast turnaround.

The number of gates in relationship to the processing speed of each new CMOS technology is shown in Figure 1–6. Figure 1–7 shows in tabular form the equivalent gate count for each technology family.

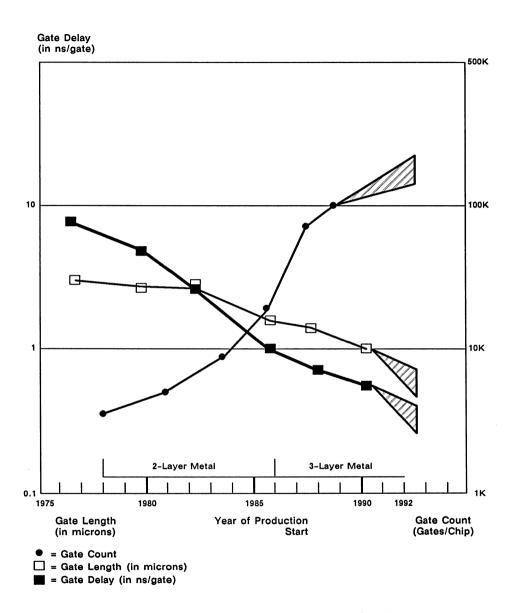


Figure 1-6. Equivalent Gate Count vs. Processing Speed, Fujitsu CMOS Gate Array Technologies

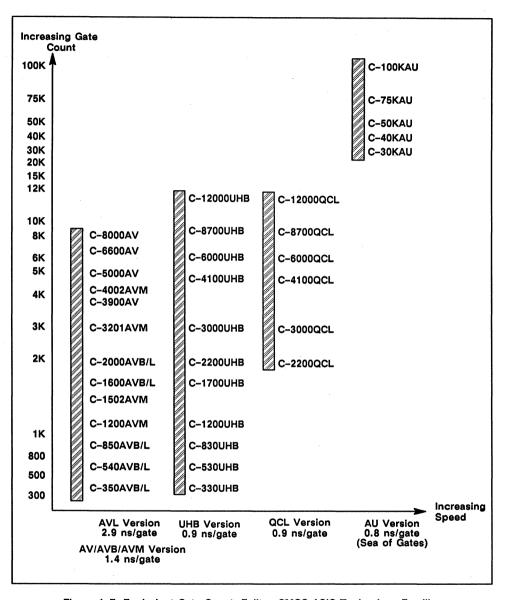


Figure 1-7. Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families



# UHB SERIES 1.5 $\mu$ CMOS GATE ARRAYS

#### MB62XXXX MB60XXXX

September 1988 Edition 1.1

#### DESCRIPTION

The UHB series of 1.5-micron CMOS gate arrays is a highly integrated low-power, ultra high-speed product family that derives its enhanced performance and increased user flexibility from the use of a system-proven, dual-column gate structure and 2-layer metal interconnect technology. The unique dual-column gate structure increases density and speed performance, as well as gate utilization

Internal high-drive clock buffers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic underneath the routing channels. The high-drive output buffers provide highly symmetrical output waveforms.

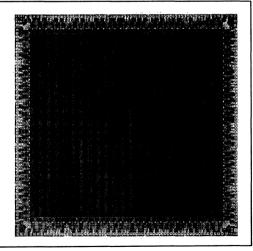
#### **FEATURES**

- High-density silicon gate CMOS technology
  - 330 to 12,000 usable gates
  - 90% maximum utilization fully autorouted
- Ultra high speed
  - typical 0.9 ns gate delay
  - narrow delay variation
- High sink current capability
  - 3.2 mA, 8 mA, 12 mA, and 24 mA options
  - selectable edge rate control
- Low-skew clock signal distribution
  - High-performance clock drivers
  - Hierarchical clock distribution
  - Frequency-dependent clock routing

- · Automatic test pattern generation for 6K gates and up
  - complete family of scan design macros available
- 2-column gate structure enhances macro performance
- High-performance internal 3-state bus
  - burled cells within the routing channels ensure high density and reliable performance
- Proven 1.5-micron 2-layer metal technology
- Highest pin-to-gate count commercially available
  - 60 logic I/O for 336 gates
  - 222 logic I/O for 1200 gates
- Input buffers incorporating pull-up/pull-down resistance
- Bullt-in feedback resistors for oscillators
- User-defined hierarchy-driven placement

Device Name	Utilizable Gates <sup>1</sup>	Maximum Signal Pins <sup>2</sup>
C-330UHB	336 gates	60
C-530UHB	530 gates	66
C-830UHB	830 gates	76
C-1200UHB	1233 gates	92
C-1700UHB	1724 gates	108
C-2200UHB	2220 gates	123
C-3000UHB	3066 gates	148
C-4100UHB	4174 gates	163
C-6000UHB	6000 gates	163
C-8700UHB	8768 gates	188
C-12000UHB	12734 gates	220

- 1. Gates available for logic (exclusive of I/O usage).
- Maximum signal pin numbers depend on the output drive requirements and the package selected.



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#### MB62xxxx **FUJITSU** MB60xxxx

#### PRODUCT FAMILY DESCRIPTIONS

Device Name	Part Number	2-Input Gate Equivalent Complexity	Maximum Signal Pins	Total Number of Basic Cells on Chip
C-330UHB	MB625xxx	336 gates	60	610 gates
C-530UHB	MB624xxx	530 gates	66	840 gates
C-830UHB	MB623xxx	830 gates	76	1176 gates
C-1200UHB	MB622xxx	1233 gates	92	1680 gates
C-1700UHB	MB621xxx	1724 gates	108	2232 gates
C-2200UHB	MB620xxx	2220 gates	123	2800 gates
C-3000UHB	MB606xxx	3066 gates	148	3744 gates
C-4100UHB	MB605xxx	4174 gates	163	4888 gates
C-6000UHB	MB604xxx	6000 gates	163	6976 gates
C-8700UHB	MB603xxx	8768 gates	188	9720 gates
C-12000UHB	MB602xxx	12734 gates	220	13728 gates

Typical device gate speed, with F/O=2, for a 2-input NAND gate, is 0.9 ns. A basic cell is equivalent to a 2-input gate.
Basic cells on chip are also used for I/O buffer function. Notes: 1.

The maximum signal pin numbers depend on the output drive requirements and the package selection.

#### **AC CHARACTERISTICS**

#### BEST/WORST CASE MULTIPLIERS FOR PROPAGATION DELAYS

Propagation delays characteristic of a gate array are a function of several factors, including operating temperature, supply voltage, fanout loading, interconnection routing metal, process variation, input transition time, and input signal polarity. Temperature and supply voltage factors affecting propagation delays in the UHB CMOS family of gate arrays are given in the table below.

		Pre-Layou	t Simulation	ו	Post-Layout Simulation				
Temperature Range	V <sub>DD</sub> =	$_{D} = 5V \pm 5\%$ $V_{DD} = 5V \pm 10\%$ $V_{I}$		V <sub>DD</sub> = 5V± 5%		V <sub>DD</sub> = 5V±10%			
	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	
1. 0 - 70°C	0.35	1.65	0.30	1.75	0.40	1.60	0.35	1.70	
220 - 70°C	0.35	1.65	0.25	1.75	0.35	1.60	0.30	1.70	
340 - 70°C	0.25	1.65	0.20	1.75	0.30	1.60	0.25	1.70	
440 - 85°C	0.25	1.75	0.20	1.85	0.30	1.70	0.25	1.80	

- 1. = commercial temperature range
- 4. = industrial temperature range

Constants for calculating the delays due to process variation, fanout loading, interconnection routing metal, transition time, and signal polarity are given for each unit cell in the UHB Unit Cell Library. Delays using these factors are calculated for a representative selection of unit cells and are shown in the Propagation Delays table on the following page.



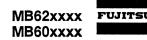
#### REPRESENTATIVE PROPAGATION DELAYS

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array).

Typical values are indicated. Worst case multipliers are applied to typical values. Smaller arrays can exhibit significantly greater speed.

	T			Propagation Delays (in ns)						
Unit Cell Function	Unit Cell Name	Equivalent Gate Count		NDI (Fan-out)						
				1	2	4	8	16	32	
Inverter	V1N	1	t PLH, t PHL	0.86 0.67	1.51 1.04	2.36 1.52	3.53 2.18	5.19 3.11	8.09 4.74	
Power 2-Input NAND	N2K	2	t PLH, t PHL	0.66 0.68	.99 .97	1.41 1.34	1.99 1.85	2.83 2.58	4.27 3.85	
Power 16-Input NAND	NGB	11	t PLH, t PHL	1.82 3.69	2.15 3.93	2.57 4.25	3.15 4.69	3.99 5.31	5.43 6.40	
Power 2-Input NOR	R2K	2	t PLH, t PHL	0.95 0.67	1.53 0.91	2.27 1.23	3.29 1.67	4.75 2.29	7.28 3.38	
Power Exclusive OR	X2B	4	t PLH, t PHL	1.72 1.82	2.05 2.03	2.47 2.29	3.05 2.66	3.89 3.18	5.33 4.08	
3-wide 2-AND 6-Input AND-OR Inverter (A→Y)	D36	3	t PLH, t PHL	1.78 1.22	2.93 1.80	4.41 2.54	6.45 3.56	9.37 5.02	4.43 7.55	
2-wide 2-OR 4-input OR-AND-inverter (A→X)	G24	2	t PLH, t PHL	1.54 1.20	2.73 1.78	4.27 2.52	6.39 3.54	9.40 5.00	14.65 7.53	
Power 2-AND 8-Wide Multiplexer (A→X)	T28	11	t PLH, t PHL	2.41 1.66	2.74 1.83	3.16 2.04	3.74 2.33	4.58 2.75	6.02 3.47	
Power Clock Buffer	K2B	3	t PLH, t PHL	1.30 1.38	1.57 1.58	1.90 1.83	2.30 2.13	2.81 2.51	3.61 3.11	
Scan 8-bit D FF with Clock inhibit and 2:1 Data Multiplexer (CK,IH→Q)	SHK	88	t PLH, t PHL	5.22 4.92	5.87 5.29	6.72 5.77	7.89 6.43	9.55 7.36	12.45 8.99	
Non-Scan D FF with Reset (CK→Q)	FDO	7	t PLH, t PHL	2.51 2.14	3.16 2.55	4.01 3.08	5.18 3.81	6.84 4.85	9.74 6.66	
Non-Scan Power D FF with Clear (CK→Q)	FD5	8	t PLH, t PHL	2.17 1.89	2.50 2.10	2.92 2.36	3.50 2.73	4.34 3.25	5.78 4.15	
Non-Scan 4-bit Binary Synchronous Up Counter (CI→CO)	C43	48	t PLH, t PHL	2.18 1.10	2.83 1.43	3.68 1.85	4.85 2.43	6.51 3.27	9.41 4.71	
Non-Scan 4-bit Binary Synchronous Up Counter (CI→CO)	C45	48	t PLH, t PHL	2.52 1.68	3.22 2.05	4.12 2.53	5.36 3.19	7.13 4.12	10.21 5.75	

Note: Delays for inter-block wiring are not included



#### REPRESENTATIVE PROPAGATION DELAYS (Continued)

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array). Typical values are indicated. Worst case multipliers are applied to typical values.

				Propagation Delays (in na				ns)	
Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition	NDI (Fan-out)					
runction	Name	Gate Count	iransition	1	2	4	8	16	32
Non-Scan 4-bit Binary Synchronous Up/Down Counter (DU→CO)	C47	68	t PLH, t PHL	2.87 3.30	3.32 3.63	3.90 4.05	4.70 4.63	5.85 5.47	7.84 6.91
4-bit Binary Full Adder with Fast Carry (Cl→S1)	A4H	48	t PLH, t PHL	1.97 2.13	2.87 2.71	4.04 3.45	5.65 4.47	7.93 5.93	11.92 8.46
4:1 Selector (S5→X)	T5A	5	t PLH, t PHL	1.39 1.12	2.33 1.77	3.55 2.62	5.23 3.79	7.62 5.45	11.79 8.35
4-bit Shift Register with Synchronous Load	FS2	30	t PLH, t PHL	2.90 3.46	3.55 3.83	4.40 4.31	5.57 4.97	7.23 5.90	10.13 7.53
9-bit Odd Parity Generator/Checker	PO9	22	t PLH, t PHL	5.78 6.00	6.43 6.33	7.28 6.75	8.45 7.33	10.11 8.17	13.01 9.61
4-wide 2:1 Data Selector (A→X)	P24	12	t PLH, t PHL	1.24 0.97	1.57 1.14	1.99 1.35	2.57 1.64	3.41 2.06	4.85 2.78
4-bit Magnitude Comparator (IS→OG)	MC4	42	t PLH, t PHL	3.17 2.60	4.36 2.93	5.90 3.35	8.02 3.93	11.03 4.77	16.28 6.21
4-bit Bus Driver (A→X)	B41	9	t PLH, t PHL	1.99 1.87	2.48 2.29	3.05 2.78	3.76 3.39	4.64 4.14	6.04 5.34
Input Buffer (Inverter)	I1B	5	t PLH, t PHL	1.84 1.78	2.11 2.05	2.44 2.38	2.84 2.78	3.35 3.29	4.15 4.09
Clock Input Buffer (Inverter)	IKB	4	t PLH, t PHL	2.49 1.94	2.63 2.08	2.79 2.24	2.99 2.44	3.24 2.69	3.64 3.09
				Output Buffer Load in pF					
				12	25	50	100	200	400
Output Buffer (True)	O2B	2	t PLH, t PHL	2.37 3.24	3.10 4.85	4.50 7.95	7.30 14.15	12.90 26.55	24.10 51.35
Power Output Buffer (True)	O2L	2	t PLH, t <sub>PHI</sub>	2.53 2.47	3.02 3.01	3.94 4.03	5.79 6.08	9.49 10.18	16.89 18.38
3-State Output Buffer (True)	O4T	4	t PLH, t PHL	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.52	13.62 28.52	24.82 54.52
Power 3-State Output Buffer (True)	O4W	4	t PLH, t PHL	3.48 4.68	3/97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92
3-State Output and Input Buffer (True)	Н6Т	8	t PLH, t PHL	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.57	13.62 28.52	24.82 54.52
Power 3-State Output and Input Buffer (True)	H6W	8	t PLH, t PHL	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92

Note: Delays for Inter-block wiring are not included



#### DC CHARACTERISTICS

#### ABSOLUTE MAXIMUM RATINGS1

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V <sub>DD</sub>	V <sub>SS</sub> <sup>2</sup> -0.5	6.0	>
Input Voltage		٧	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD</sub> +0.5	٧
Output Voltage		v <sub>o</sub>	V <sub>SS</sub> <sup>2</sup> -0.5	V <sub>DD+</sub> 0.5	٧
	I <sub>OL</sub> =3.2mA	los	-40	+40	
Output Current <sup>3</sup>	I <sub>OL</sub> =8mA		-40	+80	
Output Current	I <sub>OL</sub> =12mA		-60	+120	mA
	l <sub>OL</sub> =24mA		-90	+180	
Storage Temperature	Ceramic Plastic	T <sub>stg</sub>	-65 -40	+150 +125	°c
Temperature Under Blas	Ceramic Plastic	T <sub>bias</sub>	-40 -25	+125 +85	°C

Notes: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Vss = 0V.

3. Only one output at a time may be shorted for more than one second.

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	VDD	4.75	5.0	5.25	٧
Input High Voltage for TTL Input	VIН	2.2	-	-	٧
input Low Voltage for TTL input	VIL		-	0.8	V
Input High Voltage for CMOS Input	VIH	V <sub>DD</sub> x 0.7	_	-	V
Input Low Voltage for CMOS Input	VIL	-	-	V <sub>DD</sub> x 0.3	· V
Operating Temperature	TA	0	-	70	°C

#### **CAPACITANCE** $(T_A = 25^{\circ}C, V_{DD} = V_I = 0V, f = 1 \text{ MHz})$

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C <sub>IN</sub>	-	-	16	pF
Output Pin Capacitance (I <sub>OL</sub> =3.2mA, 8mA or 12mA)	C <sub>OUT</sub>	-	-	16	pF
Output Pin Capacitance (I <sub>OL</sub> =24mA)	COUT	-	-	18	pF
I/O Pin Capacitance (I <sub>OL</sub> =3.2mA, 8mA or 12mA)	c <sub>I/O</sub>	-	_	16	pF
I/O Pin Capacitance (I <sub>OL</sub> =24mA)	c <sub>I/O</sub>	-	-	23	pF

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	IDDS	Steady State <sup>1</sup>	0	_	100	μА
Output High Voltage for Normal Output (IOL =3.2mA)	V <sub>OH</sub>	I <sub>OH</sub> = -2mA	4.0		v <sub>DD</sub>	V
Output High Voltage for Driver Output (IOL =8mA)	v <sub>oH</sub>	I <sub>OH</sub> = -2mA	4.0	· <u> </u>	V <sub>DD</sub>	٧
Output High Voltage for Driver Output (IOL =12mA)	v <sub>oh</sub>	I <sub>OH</sub> = -4mA	4.0	_	v <sub>DD</sub>	٧
Output High Voltage for Driver Output (IOL =24mA)	V <sub>OH</sub>	I <sub>OH</sub> = -8mA	4.0	_	v <sub>DD</sub>	٧
Output Low Voltage <sup>2</sup> for Normal Output (IOL= 3.2mA)	V <sub>OL</sub>	I <sub>OL</sub> = 3.2mA	v <sub>ss</sub>	_	0.4	V
Output Low Voltage <sup>2</sup> for Driver Output (IOL= 8mA)	v <sub>oL</sub>	IOL = 8mA	v <sub>ss</sub>	_	0.4	0∨
Output Low Voltage <sup>2</sup> for Driver Output (IOL= 12mA)	V <sub>OL</sub>	I <sub>OL</sub> = 12mA	v <sub>ss</sub>	_	0.4	0∨
Output Low Voltage <sup>2</sup> for Driver Output (IOL= 24mA)	V <sub>OL</sub>	I <sub>OL</sub> = 24mA	v <sub>ss</sub>		0.4	0V
Input High Voltage for TTL Input	V <sub>IH</sub>	_	2.2	_	_	V
Input Low Voltage for TTL Input	V <sub>IL</sub>	_		_	0.8	V
Input High Voltage for CMOS Input	VIH	<del>-</del>	V <sub>DD</sub> x 0.7		_	V
Input Low Voltage for CMOS Input	V <sub>IL</sub>		_	_	V <sub>DD</sub> x 0.3	V
Schmitt Trigger CMOS Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> - V <sub>T-</sub>	- V <sub>IL</sub> to V <sub>IH</sub> V <sub>IH</sub> to V <sub>IL</sub>	2.5 0.7 1.1	3.3 1.4 1.9	4.0 2.0 2.7	* *
Schmitt Trigger TTL Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> - V <sub>T-</sub>	  Уј to Ујн Ујн to Уј	1.4 0.8 0.4	1.9 1.3 0.6	2.5 1.8 0.7	V V
Input Pull-up/Pull-down Resistor	RP	VIH = V <sub>DD</sub> VIL = V <sub>SS</sub>	25	50	100	kΩ
Input Leakage Current	I <sub>LI</sub>	V <sub>I</sub> = 0 - V <sub>DD</sub>	-10		10	μА
Input Leakage Current (3-state)	lLZ	VI = 0 - V <sub>DD</sub>	-10	_	10	μА

Notes: 1.VIH = VDD, VIL = VSS 2.With certain restrictions on pin assignment 3.These values for reference only

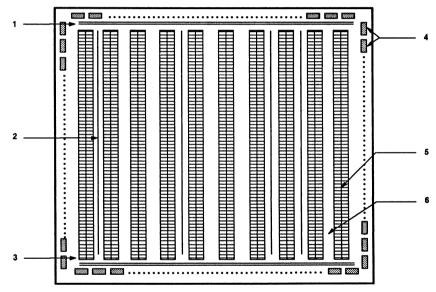


#### ARRAY ARCHITECTURE

The typical UHB chip is composed of double columns of CMOS gates (basic cells) separated by dedicated wiring channels. A basic cell consists of a pair of N-channel and a pair of P-channel transistors interconnected by polysilicon gate control terminals. Groups of basic cells are interconnected by custom metalization into unit cells. Fujitsu unit cells provide a wide range of standard logic functions such as exclusive OR gates, flip-flops, buffers, and counters. The UHB Series CMOS Gate Array family includes over 250 different unit cells. These unit cells are the building blocks from which complex designs are constructed.

The spaces between the double columns of basic cells are occupied by channels for custom metalization. Nearly half of these wiring channels contain transmission gates that implement internal 3-state buses. Bus terminators located at the ends of the double columns of cells maintain the last value to be sent through the bus to ensure proper operation under all conditions.

The I/O cells around the perimeter of the matrix of cells are composed of internal cells with input protection networks and the potential to be configured as input buffers, clock input buffers, output buffers, power output buffers, or bidirectional buffers.



Typical Chip Layout, Double Column Structure

- 1. Dedicated Clock Network for high frequency clocks
- 2. 3-state Bus Logic located in wiring channels
- 3. Bus Terminators prevent floating state on buses
- 4. Driver Transistors and I/O Protection Networks provide high I/O count
- 5. Double Columns for optional macro utilization and speed
- 6. Wiring Channel Area for metalization between unit cells

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#### **DESIGN COMPONENTS**

#### DESIGNING WITH THE UHB PRODUCT FAMILY

To implement logic functions, the designer builds up the elements of the circuit from unit cells. Simple unit cells are used hierarchically to build higher level functions until the logic is completely defined. Fujitsu offers a complete line of standard logic functions in the unit cell library.

Soft macros are used to implement large super-cell functions such as expandable ALU's and multipliers.

#### I/O BUFFERS

Each UHB I/O buffer around the perimeter of the array consists of an input protection network and large N-channel and P-channel transistors capable of supplying the standard 3.2-mA, 8-mA, and 12-mA output currents. Two of these large transistor pairs may be connected in parallel, using high-output-current macros, to obtain 24-mA drive. One of the I/O pads whose output transistors have been used for the 24-mA high-current option may still be used as an input.

Input I/O buffers convert external TTL levels to internal CMOS levels or may receive CMOS level signals directly. Output I/O buffers are totem pole and may drive either CMOS and TTL levels, depending on their AC and DC loads. Any of the pins except the dedicated power and ground pads can be designed to be an input buffer, an input buffer with pull-up/pull-down resistance, a clock input buffer, an output buffer, a high-drive output buffer, an output buffer with noise limiting resistance, a 3-state output buffer, a bi-directional buffer, or a Schmitt trigger input buffer. There are some restrictions on the location of 24-mA buffers.

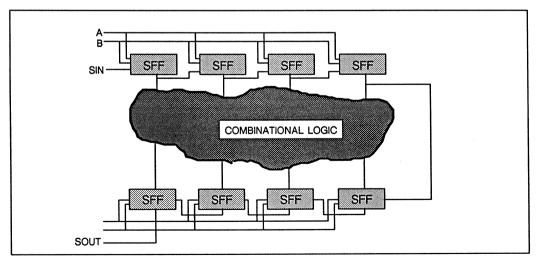
#### INPUT CLOCK DRIVERS

The large output I/O transistor pair is used in a high-drive input clock driver for high fanout applications within the array. This allows the designer to fully utilize the high speed capabilities of the UHB technology.

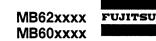
#### **TESTING UHB DEVICES**

Two options are available for testing UHB designs: (1) the standard designer-supplied test patterns and test vectors (in Fujitsu's FTDL format) and (2) the use of scan cells combined with Automatic Test Generation (ATG) performed by Fujitsu computers for additional diagnostic test patterns. If the designer has designed with scan cells and other scan logic elements, Fujitsu will complete the scan test program generation.

Regardless of the selected test option, it is the responsibility of the designer to furnish Fujitsu with enough test patterns to guarantee that the submitted design completely performs its intended logic functions. These patterns include the designer's test function of each I/O pin.



Diagramatic Representation of Design Structure for Scan Testing



#### VDD and VSS REQUIREMENTS

Each UHB Series gate array device has two options for each package type, both supporting a different number of power and ground pins. The number of power and ground pins required depends on the number of simultaneously switching outputs used in the design. Simultaneously switching outputs (SSOs) are output signals that change from H to L or L to H or from Z to H or Z to L within a 20-ns window (including possible skew).

Multiple outputs that switch at the same time can cause noise on VDD and Vss lines and affect the performance of a device. Therefore, to achieve maximum reliability, Fujitsu limits the number of SSOs per VDD pin according to the table below. The maximum number of SSOs per pin is determined by a representative value specified for the driving capability of each type of output. The total representative value of all SSOs used in a design must not exceed 80 per Vss pin. For example, 11 normal 3.2-mA outputs with edge rate control, four 12-mA outputs, or three 24-mA outputs per Vss pin may be SSOs.

Output Drive Type	Representative Value per Output			
Normal (3.2 mA)	10			
High Drive (12 mA)	20			
Normal (3.2 mA) with Edge Rate Control	7			
High Drive (12 mA) with Edge Rate Control	14			
High Drive (24 mA) with Edge Rate Control	26			



#### ESTIMATION OF POWER DISSIPATION

In order to select a sultable ASIC package and determine system cooling requirements and system power supply requirements, the designer needs to estimate the power dissipation of the circuit.

Power dissipation calculation in CMOS technologies is complicated by the fact that transient currents involved in charging and discharging capacitances dominate the total power dissipation.

Fujitsu has simplified the calculation of power dissipation by studying a long history of designs to determine what typical circuit activity constitutes, and by observing the power dissipation characteristics of individual gates as they operate. These parameters are summarized below and are incorporated into the worksheet that follows.

```
0.073mW/MHz
Pd(in)
_d(out)
                     0.025mW/pF
pd(seq)
                     0.20mW/MHz
pd(comb)
                    0.033mW/MHz
C<sup>V</sup>(5V<sup>±</sup>5%)
                    1.11
```

The example below assumes a system clock frequency (f) of 25 MHz for a circuit of 2700 gates with 90 inputs and 50 outputs, all outputs loaded at 20 pF. The circuit activity, that is, the maximum number of internal gates, inputs, and outputs that are simultaneously active, is 20%. The mix of sequential to combinational gates is 1:5 (20%).

Note: P is in units of mW/MHz, except  $P_{d(out)}$ , which is in mW/MHz/pF.

- 1.0 I/O AC POWER CALCULATION
- 1 1 Number of inputs  $90 \times \text{freq}$   $25/2 \times PD(in) \times 20\% = 16.43 \text{ mW}$
- 1.2 Number of outputs  $\underline{50}$  x freq<sup>1</sup>  $\underline{25/4}$  x load  $\underline{20F}$  x PD(out) x 20% =  $\underline{31.25}$  mW
- 1.3 Total I/O AC (transient) Power ..... PAC = 47.68 mW
- 2.0 I/O DC POWER CALCULATION
- 2.1 Number of 3.2 mA outputs<sup>2</sup>  $34 \times (0.15 \times (loL + loH)) =$ 26.52 mW
- 2.2 Number of 8 mA outputs 16 x (0.15 (IOL + IOH)) = 24 mW
- Number of 12 mA outputs  $0 \times (0.15 \text{ (IOL} + \text{IOH)}) =$ \_\_0\_ mW 2.3
- 2.4 Number of 24 mA outputs  $0 \times (0.15 \times (10L + 10H)) = 0 \text{ mW}$
- 2.5 Total I/O DC (steady state) Power ...... PDC = 50.52 mW
- 3.0 INTERNAL GATE POWER CALCULATION
- 3.1 Number of used gates 2700 x % seq. 20% x freq 25/8 X PD(seq) = 337.5 mW
- Number of used gates 2700 x % comb. 80% x freq3 25/20 X PD(comb) = 89.1 mW 3.2
- Total Internal Gate Transient Power ...... PINT = \_\_426.6 \_\_mW 33
- 4.0 TOTAL CHIP ESTIMATED POWER DISSIPATION
- 4.1 Pt (typical) = PAC 47.68 mW + PDC 50.52 mW + PINT 426.6 mW = 524.8 mW
- 4.2 PD(worst case) = Pt = 524.8 mW x CV 1.11 = 582.5 mW = .6W W
- Notes: 1. It is assumed that outputs will toggle at one fourth the frequency of the system clock on the average.

  2. The (IoL + IoH) term assumes outputs are symmetrically high and low

  3. It is assumed that only 20% of the combinational gates are simultaneously active, and at a frequency of one fourth the clock frequency.

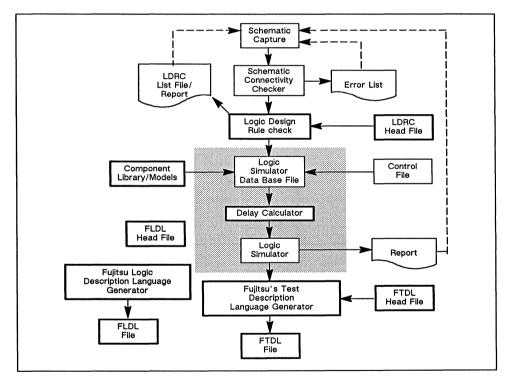
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#### WORKSTATION DESIGN FLOW

Fujitsu ASICs customers have a choice of four popular CAE design packages (Dalsy, Mentor, Valid, and HP 9000) plus Fujitsu's own new Sun-based workstation software (ViewCAD) for schematic capture and design implementation. The design flow process is summarized in the diagram below. The boxes outlined in bold indicate Fujitsu-supplied software that integrates with standard CAE software to produce the data files necessary to implement a design. The design process flowchart is somewhat simpler for the Fulltsu (ViewCAD) software because ViewCAD was written specifically for Fulltsu's high-reliability design process.

A design logic file and a test data file, known as Fujitsu Logic Design Language (FTDL) and Fujitsu Test Design Language (FTDL), are the ultimate result of the workstation design process.



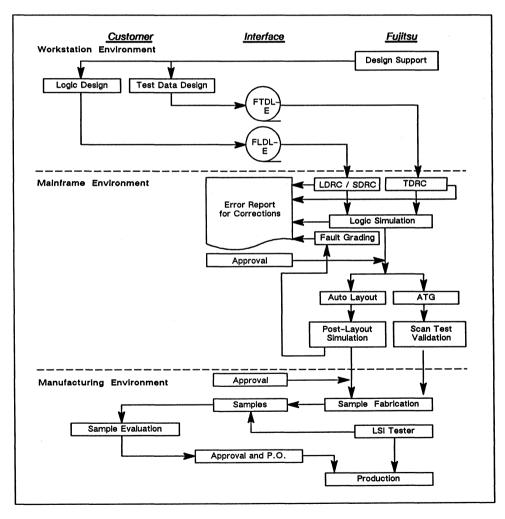
Workstation Design Process



# **DESIGN IMPLEMENTATION FLOW**

After the workstation design process is complete, the FLDL and FTDL files are transferred to the mainframe environment at one of Fulltsu's Technical Resource Centers. There, the FLDL file is checked by the Logic Design Rule Check (LDRC) and a pre-layout simulation is made using the test data generated in FTDL. Then, after automated layout takes place, simulation is run to validate the LSI function.

When the design data is validated, the design files are sent to the prototype manufacturing area where mask sets are fabricated and engineering sample devices are manufactured for test and approval. After the engineering samples are fully tested and signed off, full production can begin.



**Post-Design Process** 



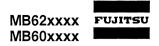
# **FUNCTIONAL INDEX OF UNIT CELL LIBRARY**

Note: The load unit ( $\ell_{\mathbf{u}}$ ) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

Inverter and Buffer	Family				
Unit Cell			T T		
Name	Description		Basic Cells	Drive (lu)	Polarity
V1N	Inverter		1	18	Neg
V2B	Power Inverter		1	36	Neg
V1L	Double Power Inverter		2	55	Neg
B1N	True Buffer		1	18	Pos
BD3	True Delay Buffer	(> 5ns)	5	18	Pos
BD4	Delay Cell	(> 4ns)	4	6	Pos
BD5	Delay Cell	(>10ns)	9	18	Pos
BD6	Delay Cell	(>22ns)	17	18	Pos
Clock Buffer Family					
Unit Cell Name	Description		Basic Cells	Drive (/u)	Polarity
K1B	True Clock Buffer	***************************************	2	36	Pos
K2B	Power Clock Buffer		3	55	Pos
КЗВ	Gated Clock (AND) Bu	ffer	2	36	Pos
K4B	Gated Clock (OR) Buff	er	2	36	Pos
K5B	Gated Clock (NAND) B	uffer	3	36	Neg
KAB	Block Clock (OR) Buffer		3	55	Pos
KBB	Block Clock (OR x 10) Buffer		30	55	Pos
NAND Family					
Unit Cell Name	Description		Basic Cells	Drive ( <i>l</i> u)	
N2N	2-input NAND		1	18	
N2B	Power 2-Input NAND		3	36	
N2K	Fast Power 2-Input NA	ND	2	36	
N3N	3-Input NAND		2	14	
N3B	Power 3-Input NAND		3	36	
N4N	4-input NAND		2	10	
N4B	Power 4-input NAND		4	36	
N6B	Power 6-input NAND		5	36	
N8B	Power 8-input NAND		6	36	
N9B	Power 9-input NAND		8	36	
NCB	Power 12-input NAND		10	36	
NGB	Power 16-input NAND		11	36	
N3K	Fast Power 3-input NA	.ND	3	36	
N4K	Fast Power 4-input NA	ND	4	36	



NOR Family				
Unit Cell				
Name	Description	Basic Cells	Drive (ℓu)	
R2N	2-input NOR	1	14	
R2B	Power 2-input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-input NOR	2	10	
R3B	Power 3-input NOR	3	36	
R3K	Power 3-input NOR	3	36	
R4N	4-input NOR	2	6	
R4B	Power 4-input NOR	4	36	
R4K	Power 4-input NOR	4	36	
R6B	Power 6-input NOR	5	36	
R8B	Power 8-input NOR	6	36	
R9B	Power 9-input NOR	. 8	36	
RCB	Power 12-input NOR	10	36	
RGB	Power 16-input NOR	11	36	
AND Family				
Unit Cell	1			
Name	Description	Basic Cells	Drive (ℓu)	
N2P	Power 2-input AND	2	36	<del></del>
N3P	Power 3-Input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	
OR Family				
Unit Cell				
Name	Description	Basic Cells	Drive ( $\ell_{u}$ )	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	
Exclusive NOR/OR	Family (EXOR/EXNOR)			
Unit Cell				
Name	Description	Basic Cells	Drive ( <sub>lu</sub> )	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
X3B	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR	6	36	Pos



Jnit Cell Name	Description	Basic Cells	Dri∨e (ℓu)	
D23	2 AND Into 2 NOR AOI	2	14	
014	3 AND into 2 NOR AOI	2	14	
D24	2, 2 AND into 2 NOR AOI	2	14	
D34	2 AND into 3 NOR AOI	2	10	
D36	3, 2 AND into 3 NOR AOI	3	10	
D44	2 OR into 2 AND into 2 NOR AOI	2	10	
Note: AND-OR-	-Invert unit cells are useful in implementing sum-of-p	products (SOP) expression	ins.	

Unit Cell Name	Description	Basic Cells	Drive ( <sub>ℓu</sub> )	
G23	2 OR into 2 NAND OAI	2	18	
G14	3 OR into 2 NAND OAI	2	10	
G24	2, 2 OR into 2 NAND OAI	2	10	
G34	2 OR into 3 NAND OAI	2	10	
G44	2 AND into 2 OR into 2 NAND OAI	2	14	

Note: OR-AND-Invert unit cells are useful in implementing product-of-sums (POS) expressions.

# Multiplexer Family

Unit Cell Name	Туре	Description	Basic Cells	Drive ( $\ell$ u)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	. 9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS



Jnit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	s, xs	Q	4
T2E	2:1	Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	s, xs	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	8	9	s, xs	XQ	11
V3A*	1:2	Selector	2	14	s, xs	XQ	11
V3B*	1:2	Selector	4	14	s, xs	XQ	2

\* These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

# Decoders

Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Active Level Outputs	Enable	
DE2	2:4	Decoder	5	18	Low		
DE3	3:8	Decoder	15	14	Low		
DE4	2:4	Decoder	8	14	Low	Low	
DE6	3:8	Decoder	30	18	Low	1 High 2 Low	

# Internal Bus Unit Cells

Unit Cell Name	Type Description	Basic Cells	Drive (lu)	Bus Size	Enable	
B41	4-bit Bus Driver	9	36	4 bits	Low	

Notes: 1 The number of B41s used is limited by the chosen array series, as shown in the table below.

 On-chip buses (managing more than one bus source and/or a bi-directional bus) may be implemented with either multiplexer-type unit cells or bus drivers. While bus drivers impose certain design restrictions, the optimum choice is dictated by the specific design.

Device Name	Maximum B41s
C-330UHB	4
C-530UHB	5
C-830UHB	6
C-1200UHB	8
C-1700UHB	12
C-2200UHB	16
C-3000UHB	21
C-4100UHB	26
C-6000UHB	50



Unit Cell Name	Description	Basic Cells	Drive (lu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	_
YL4	Data Latch with TM	14	36	High	4	Q	_
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	_

Scan Fli	o-Flop Family (Positive-Edg	e Triggered)						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH*	Scan D FF with 2:1 Multiplex	14	36	1	Q, XQ	Async	_	Yes
SDJ*	Scan D FF with 4:1 Multiplex	15	36	1	Q, XQ	Async	_	Yes
SDK*	Scan D FF with 3:1 Multiplex	16	36	1	Q, XQ	Async	_	Yes
SJH	Scan J-K FF	16	36	1	Q, XQ	Async	_	Yes
SDD*	Scan DFF with 2:1 Multiplex	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D FF	12	36	1	Q, XQ	_	_	Yes
SDB	Scan 1-input D FF	42	36	4	Q, XQ	_	_	Yes
SHA	Scan 1-input D FF	68	18	8	Q, XQ			Yes
SHB	Scan 1-input D FF	62	18	8	Q		_	Yes
SHC	Scan 1-input D FF	62	18	8	XQ		_	Yes
SH.I*	Scan D FF with 2:1 Multipley	78	18	8	0. 0			Vee

Note: \* Indicates D Flip-Flop with multiplexed inputs.

Scan D FF with 3:1 Multiplex

SHK\*



11-14				1				
Unit Celi Name	Description	Basic Cells	Drive (lu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D FF with Set	7	18	1	Q, XQ	_	Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	_		Pos
FDO	Non-Scan D FF with Reset	7	18	1	Q, XQ	Async	_	Pos
FDP	Non-Scan D FF with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D FF	21	18	4	Q		_	Neg
FDR	Non-Scan D FF with Clear	26	18	4	Q	Async	_	Pos
FDS	Non-Scan D FF	20	18	4	Q	_	_	Pos
FD2	Non-Scan Power D FF	7	36	1	Q, XQ		_	Neg
FD3	Non-Scan Power D FF with Preset	8	36	1	Q, XQ	_	Async	Neg
FD4	Non-Scan Power D FF with Clear							
	and Preset	9	36	1	Q, XQ	Async	Async	Neg
FD5	Non-Scan Power D FF with Clear	8	36	1	Q, XQ	Async	_	Neg
FJD	Non-Scan Positive Edge Clocked							
	Power J-K FF with Clear	12	36	1 1	Q, XQ	Async	_	Pos

Note: Synchronous filp-flops my be constructed by adding a simple AND gate (such as N2P) to the input of a filp-flop to create a synchronous clear.

Binary	Counter Family									
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down
SC72	Scan 4-bit Synchronous Binary				Q, XQ,					
	Up Counter with Parallel Load	62	36	4	CO (S)	Sync	_	Low	High	Up
SC8 <sup>2</sup>	Scan 4-bit Synchronous Binary				Q, XQ,				,	
	Down Counter with Parallel Load	66	36	4	CO (S)	Sync	_	High	Low	Down
C113	Non-Scan Flip-Flop for Counter	11	18	Ι –	Q, XQ	_	_	_		_
C41	Non-Scan 4-bit Binary									
	Asynchronous Counter	24	18	4	Q, (A)	_	Async	_	_	Up
C42	Non-Scan 4-bit Binary									
	Synchronous Counter	32	18	4	Q	_	Async	_	_	Up
C43	Non-Scan 4-bit Binary									
	Synchronous Up Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous									
	Up Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous									
	I	1		1 .	l	i .	1	I .	1 .	I

Up/Down Counter 68 18 4 Q, CO Async — Low Low Up/Down Notes: 1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous.

- 2. Scan counters include clock inhibit and high drive (CDR = 36  $\ell$ u). For non-Scan counters CDR = 18  $\ell$ u.
- 3. C11 may by used for purposes other than counters.



Shift Regis	ster Family									
Unit Cell Name	Description	Basic Cells	Dri∨e (ℓu)	Bit Width	Load	3	Outputs	Clock Polarity		
FS1	Serial-in Parallel-out Shift									
	Register	18	16	4	Serial-lı	n only	Q-Parallel	Neg		
FS2	Shift Register with									
	Synchronous Load	30	16	4	Sync-H	igh	Q-Parallel	Neg		
FS3	Shift Register with									
	Asynchronous Load	18	4	Async-	Low	Q-Parallel	Pos			
SR1	Serial-in Parallel-out Shift				ł					
	Register with Scan	36	36	4	Serial-li	n only	Q-Parallel	Pos		
Datapath (	Dperators (Adder, ALU, Pari	ty)		1	1					
Unit Cell Name	Description	Basic Cells	Drive ( <sub>lu</sub> )	Bit Width		Outputs	Carry In			
MC4	Magnitude Comparator		42	18(=) 10(<,>)	4	A>B	, A=B, A <b< td=""><td>A&gt;B,A=B,ALB</td></b<>	A>B,A=B,ALB		
A1A	1-bit Half Adder		5	36	1	S, C	0	_		
A1N	1-bit Full Adder		8	18	1	S, C	0	CI		
A2N	2-bit Full Adder		16	14	2	S, C	0	CI		
A4H	4-bit Binary Full Adder w/Fast C	arry	48	18(CO) 14(S)	4	s, c	0	CI		
PE5	Even Parity Generator/Checker		12	36	5	EVE	N, ODD	_		
PO5	Odd Parity Generator/Checker		12	36	5	ODD	, EVEN	_		
PE8	Even Parity Generator/Checker		18	18	8	EVE	N, ODD			
PO8	Odd Parity Generator/Checker		18	18	8	ODD	, EVEN	_		
PE9	Even Parity Generator/Checker		22	18	9	EVE	N, ODD			
PO9	Odd Parity Generator/Checker		22	18	9	ODE	, EVEN	_		
Miscellane	ous Cells		<b>,</b>							
Unit Cell			Basic							
Name	Description		Cells	Function						
Z00	0 Clip	0	Tie to Vss							
Z01	1 Clip		0	Tie to VDD						

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# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Input B	uffer Family					
Unit Celi Name	Description	Basic Cells	Drive (/u)	Logic Level	Туре	input/ Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signai	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
12CU	I2C with Pull-up Resistance	4	36	смоѕ	Signal	True
12CD	I2C with Pull-down Resistance	4	36	смоѕ	Signal	True
IIS	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
IISU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
I2S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	6	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	6	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	6	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True
12RD		8	18	1	Schmitt	

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of  $50 \text{K}\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.



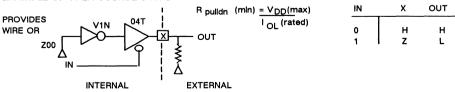


Output	Buffer Family						
Unit Cell Name	Description	Basic Cells	Drive (IOL)	Logic² Level	Туре	Edge Rate Control	input/ Output Polarity
O1B	Output Buffer	3	3.2mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12mA	TTL/CMOS	Standard	Yes	True
O4T¹	Output Buffer	4	3.2mA	TTL/CMOS	3-state	No	True
O4W¹	Power 3-state Output Buffer	4	12mA	TTL/CMOS	3-state	No	True
O4S1	Power 3-state Output Buffer	5	12mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2mA	TTL/CMOS	Standard	Yes	True
O4R <sup>1</sup>	Output Buffer	5	3.2mA	TTL/CMOS	3-state	Yes	True
O2S2	High Power Output Buffer	6	24mA	TTL/CMOS	Standard	Yes	True
O4S21	High Power Output Buffer	7	24mA	TTL/CMOS	3-state	Yes	True
O1BF	Output Buffer	3	8mA	TTL/CMOS	Standard	No	invert
O1RF	Output Buffer	5	8mA	TTL/CMOS	Standard	Yes	Invert
O2BF	Output Buffer	2	8mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8mA	TTL/CMOS	3-state	No	True

Note: 1. While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

# **EXAMPLE OF OPEN DRAIN OUTPUT**

# **EXAMPLE OF OPEN SOURCE OUTPUT**



Note: 2. Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

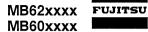
# MB62xxxx MB60xxxx



# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirect	ional I/O Buffers (Buses)					
Unit Cell Name	Description	Basic Cells	Drive (IOL)	Logic Level	Edge Rate Control	Input/ Output Polarity
нет	3-state Output and Input Buffer	8	3.2mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2mA	TTL	No	True
H6W	Power 3-state Output and Input					
	Buffer	8	12mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12mA	TTL	No	True
H6C	3-state Output and CMOS					
	Interface Input Buffer	8	3.2mA	смоѕ	No	True
H6CU	H6C with Pull-up Resistance	8	3.2mA	смоѕ	No	True
H6CD	H6C with Pull-down Resistance	8	3.2mA	смоѕ	No	True
H6E	Power 3-state Output and CMOS					
	Interface Input Buffer	8	12mA	смоѕ	No	True
H6EU	H6E with Pull-up Resistance	8	12mA	смоѕ	No	True
H6ED	H6E with Pull-down Resistance	8	12mA	смоѕ	No	True
H6S	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2mA	смоѕ	No	True
H6SU	H6S with Pull-up Resistance	12	3.2mA	смоѕ	No	True
H6SD	H6S with Pull-down Resistance	12	3.2mA	CMOS	No	True
H6R	3-state Output and Schmitt					
	Trigger input Buffer	12	3.2mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2mA	TTL	No	True
н8Т	3-state Output and Input Buffer	9	3.2mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2mA	TTL	Yes	True
H8W	Power 3-state Output and Input					
	Buffer	9	12mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12mA	TTL	Yes	True
H8W2	High Power 3-state Output and Input					
	Buffer	11	24mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	11	24mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	11	24mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS			<b> </b>		
	Interface Input Buffer	9	3.2mA	смоѕ	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2mA	смоѕ	Yes	True
	•	9	3.2mA	CMOS	Yes	True

Note: A "U" suffixed tol the name of a bidirectional buffer indicates a pull-up resistance of  $50\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.





Bidirect	ional I/O Buffers (Buses) continu	ed				
Unit Cell Name	Description	Basic Cells	Drive (IOL)	input Logic Level	Edge Rate Control	Input/ Output Polarity
H8E	Power 3-state Output Buffer and					
	Interface Input Buffer	9	12mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12mA	CMOS	Yes	True
H8E2	High Power 3-state Output and Input					
	Buffer	11	24mA	CMOS	Yes	True
H8E1	H8E2 with Pull-up Resistance	11	24mA	CMOS	Yes	True
H8E0	H8E2 with Pull-down Resistance	11	24mA	CMOS	Yes	True
H8S	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2mA	CMOS	Yes	True
H8R	3-state Output and Schmitt					
	Trigger Input Buffer	13	3.2mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2mA	TTL	Yes	True
H6TF	3-state Output and Schmitt					
	Trigger Input Buffer	8	8mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8mA	CMOS	Yes	True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

# Oscillator Circuits

Unit			Input
Cell Name	Description	Basic Cells	Logic Level
нос	Output Buffer for Oscillator and		
	Input Buffer	8	CMOS
HOCS	Output Buffer for Oscillator and		
	Schmitt Trigger Input Buffer	8	TTL
HOCR	Output Buffer for Oscillator with		
	feedback Resistance	8	CMOS
IT1O	Input Buffer for Oscillator	0	_

# MB62xxxx Fujitsu MB60xxxx

# **Availability Characteristics of UHB Gate Array Packages**

Dual In-line P	ackages (Standard	DIP)			
Pinout Code	Package	Code	Number	Number	Available Number of
	Plastic	Ceramic	of Vdd	of Vss	Signal Pins
DIP-16	DIP-16P-MO2	DIP-16C-C03	1	2	13
	DIP-16P-MO4				
DIP-18	DIP-18P-MO1	DIP-18C-CO1			
	DIP-18P-MO2				
DIP-20	DIP-20P-MO2	DIP-20C-CO2	1	2	17
DIP-20U			1	1	18
DIP-22	DIP-22P-MO2	DIP-22C-C02	2	2	18
	DIP-22P-MO3				
DIP-22U			1	1	20
DIP-24	DIP24P-MO1	DIP-24C-C01	2	2	20
	DIP24P-MO2				
DIP-24U			1	1	22
DIP-28	DIP-28P-M02	DIP-28C-C02	2	2	24
	DIP-28P-M03				
DIP-28U			1	1	26
DIP-40	DIP-40P-M01	DIP-40C-A01	2	4	34
		DIP-40C-A02			
DIP-40U		<u> </u>	1	1	38
DIP-42	DIP-42P-MO1	DIP-42C-A01	2	4	36
	DIP-42P-MO2	<del> </del>			
DIP-42U			1	1	40
DIP-48	DIP-48P-MO1	DIP-48C-A01	2	4	42
	DIP-48P-MO2				
DIP-48U			1	1	46
Dual In-line P	ackages (Shrink Dif	P. 70 mil Pin Pitcl	1)		
	Package		l		Available
Pinout Code	Plastic	Ceramic	Number of Vdd	Number of Vss	Number of Signal Pins
DIP-28SH			2	2	24
DIP-28SHU			1	1	26
DIP-42SH			2	4	36
DIP-42SHU			1	1	40
DIP-48SH			2	4	36
DIP-48SHU			1	. 1	46
DIP-64SH			2	4	58
DIP-64SHU			2	2	60

# MB62xxxx MB60xxxx



# **Availability Characteristics of UHB Gate Array Packages**

Dual In-line P	ackages (Skinny DIP, :	300mil Body W	idth)		
Pinout Code	Package Cod Plastic		Number of Vdd	Number of Vss	Available Number of Signal Pins
DIP-22SK			2	2	18
DIP-22SKU	· · · · · · · · · · · · · · · · · · ·		1	1	20
DIP-24SK			2	2	20
DIP-24SKU			1	1	22
DIP-28SK			2	2	24
DIP-28SKU			1	1	26
Flatpack Pack	ages (Dual-Leaded)				
Pinout Code	Package Co	de	Number	Number	Available Number of
Finout Code	Plastic	Ceramic	of Vdd	of Vss	Signal Pins
FPT-16	FPT-16P-MO3		1	2	13
FPT-16U			1	1	14
FPT-20	FPT-20P-MO2		1	2	17
FPT-20U			1	1	18
FPT-24	FPT-24-MO2		2	2	20
FPT-24U			1	1	22
FPT-28	FPT-28P-MO1		2	2	24
FPT-28U			1	1	26
Flatpack Pack	ages (Quad-Leaded)				
•	Package Co	40			Available
Pinout Code	Plastic	Ceramic	Number of Vdd	Number of Vss	Number of Signal Pins
FPT-44			2	4	36
FPT-44U	***************************************		2	2	40
FPT-48	FPT-48P-MO2		2	4	42
FPT-48U			2	2	44
FPT-48 *			2	4	42
FPT-48U *			2	2	44
FPT-64*	FPT-64P-MO1		2	4	58
FPT-64U	FPT-70P-MO1		1	1	62
FPT-80	FPT-80P-MO1		2	6	72
FPT-80U			2	4	74
FPT-100	FPT-100P-MO1		4	8	88
FPT-100U			4	4	92
FPT-120			6	12	102
FPT-120U			4	8	108
FPT-160			8	14	138
FPT-160U			6	12	142

<sup>\*</sup> Small body size.

# MB62xxxx FUJITSU MB60xxxx

# **Availability Characteristics of UHB Gate Array Packages**

Pin Grid Array	rs (PGA, Thru-Hole, 1	00mil Pin Pitch	)		
Pinout Code	Package C Plastic	ode Ceramic	Number # Vdd	Number # Vss	Available Number of Signal Pins
PGA-64		PGA-64C-A02	2	4	58
PGA-64U		1	2	2	60
PGA-88		PGA-88C-A01	4	6	78
PGA-88U		<b>-</b>	4	4	80
PGA-135		<u> </u>	8	12	115
PGA-135U	···		4	8 .	127
PGA-179			8	16	155
PGA-179U			8	8	163
PGA-208			12	18	178
PGA-256			16	20	220
Flatpack Pack	ages (Dual-Leaded)				
Pinout Code	Package C	ode I Ceramic	Number of Vdd	Number of Vss	Available Number of Signal Pins
LCC-28	Flastic	LCC-28C-A02	2	2	Signal Fins
LCC-28U		LCC-28C-AU2	1	1	26
LCC-280		LCC-48C-A01	2	4	42
LCC-48U	,	LCC-48C-AU1	1	2	45
LCC-64		LCC-64C-A01	2	4	58
LCC-64U		LCC-04C-A01	2	2	60
LCC-68	·	-	2	4	62
LCC-68U		- <del> </del>	2	2	64
LCC-84			4	6	74
LCC-84U			3	4	77
	d Chip Carriers (PLC)	S 50mil Pitch)	<u> </u>	7	
	Package C				Available
Pinout Code	Plastic	Ceramic	Number of Vdd	Number of Vss	Number of Signal Pins
PLCC-28	LCC-28P-M01	The state of the s	2	2	24
PLCC-28U			1	1	26
PLCC-44	LCC-44P-MO1		2	4	38
PLCC-44U		<del> </del>	1	2	41
PLCC-68	LCC-68P-M01	1	2	4	62
PLCC-68U			2	2	64
PLCC-84	LCC-84P-M01	<b>†</b>	4	6	74

Subject to Change

# MB62xxxx FUJITSU MB60xxxx

# PACKAGE AVAILABILITY

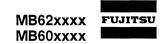
DACKACE ODTIONS

PACKAGE	OPT	<u> 101</u>	IS																				
		C-3	330 HB		530 HB	όΞ	830 HB	C-1 UI	200 HB	C-1 UI	700 -IB	C-2 UH	200 1B	C-3 Uł	000 1B	C-4 Uh	100 IB	C-6	000 HB	C-8 UI		C-12 UF	2000 HB
		C	Р	С	Р	C	Р	С	Р	С	Р	С	Р	O	Р	C	Ω	O	Р	O	Р	C	Р
DIP	16 18 20 22 24 28 40 42 48	• • • •	• • • • • • •	•	• • • • • •	••••	• • • • •	•	•	•	•	•	•	••	••••		••••		•••				
SDIP (SHRINK)	28 42 48 64	•	:	•		•		•		•		•	:		•		:		:				
SKDIP (SKINNY)	22 24 28		•		•																		
FPT with leads on two sides of the package	16 20 24 28		:		:		:		:														
FPT with leads on four sides of the package	44 48 48* 64 80 100 120 160		:		•	•	•	•	•		••••		•		•	•		•	•	0 0 •	•	0 0	0 0
PLCC	28 44 68 84		:		:		:		:		:		:		:		:		:				
PGA	64 88 135 179 208 256	•	•	•	•	:	:	:	:	:	:	:	:	•	:	:	:	:	:	•	:	0	
rcc	28 48 64 68 84	•		•		:		•		:		•		•		•		•		•			

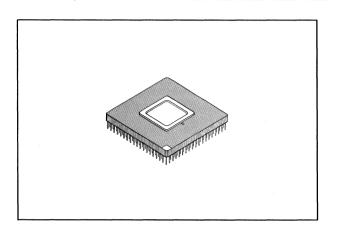
C = Ceramic P = Plastic

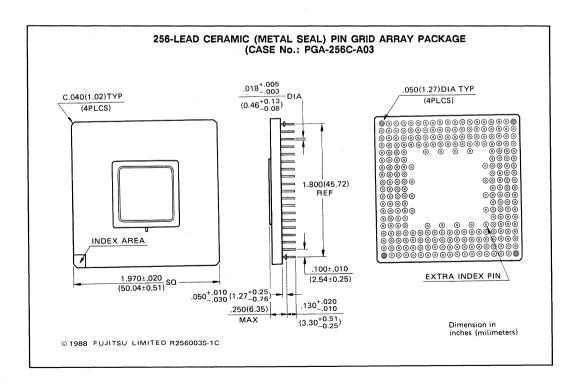
<sup>•:</sup> available now
•: under development

<sup>\* = 48-</sup>pin FPT, smaller than the other 48 FPT



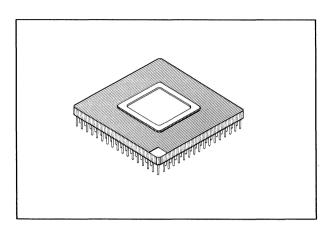
# **PACKAGE DEMENSIONS**

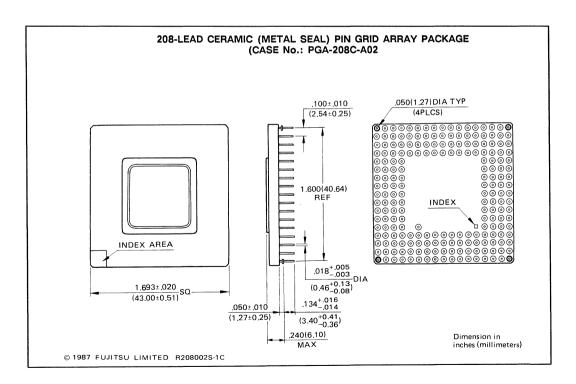




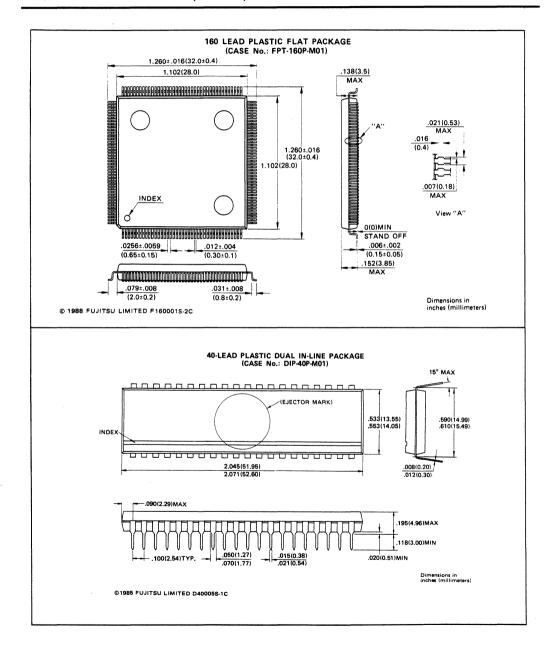


# PACKAGE DEMENSIONS (Continued)





# PACKAGE DEMENSIONS (Continued)





# AV CMOS SERIES GATE ARRAYS

MB65xxxx MB66xxxx MB67xxxx

> June 1986 Edition 2.0

# DESCRIPTION

The Fujitsu MB65xxxx/MB66xxxx/MB67xxxx family are a series of high performance CMOS gate arrays designed to provide high density, low power, and operating speeds that are comparable to standard bipolar logic. The AV (MB65xxxx) series is an ideal choice for LSI and VLSI applications that require up to 8000 gates, 2304 bits of RAM, 4608 bits of ROM or for bus interface circuits with high-drive requirements. The AVB (MB67xxxx) series include optional 10 mA buffered outputs and input pull-up/pull-down resistors for easy interfacing with bus organized logic. The AVM (MB66xxxx) series of memory arrays include, in addition to the 1.5K, 2.3K, and 4K gates of logic, two basic sizes of static registered memories:

The C4002 and C1502 have up to 2304 bits of RAM organized in an optional by-nine memory configuration that is system compatible with most modern designs. The 2301 has 1024 bits of RAM that may be configured into any by-four multiple from 256-by-4 to 32-by-32.

The AVM memories contain duplicate decoder and address register logic so that they may be split and used as two independent memories without borrowing any of the unit cells.

All AV, AVB and AVM arrays use the same basic internal cell structure and common logic Macros.

### **FEATURES**

- 1.4 ns gate delay typical. (2-input NAND gate, F.O.=2)
- Static RAM or ROM on chip.
- Silicon-gate 1.8 micron dual metal.
- 100% automatic placement and routing with guaranteed 90% cell utilization.
- Three-state and bidirectional outputs available.
- High-drive output.

Buffers, I OL = 10.0 mA, available.

- Pull-up/pull-down input buffers available.
- Single 5V power supply.
- TTL compatible I/O, CMOS input and Schmitt trigger input.
- Popular CAE workstations supported.
- Over 100 unit cells available for design.
- Predesigned software macros available. (F-Macros).
- Fast turnaround: 5 weeks after final validation.
- Evaluation samples available.
- Extended temperature range available.

AV-CMOS SERIES	Device	Part No.	Gates	1/0	Gate Spe	ed Features	
	C2600AV	MB654xxx	2640	106	1.4 ns	High Density	
	C3900AV	MB653xxx	3900	127	1.4 ns	High Density	
	C5000AV	MB652xxx	5022	127	1.4 ns	High Density	
	C6600AV	MB651xxx	6664	160	1.4 ns	High Density	
	C8000AV	MB650xxx	MB650xxx	8000	160	1.4 ns	High Density
AVB-CMOS SERIES	C350AVB	MB675xxx	357	38 (42) <sup>1</sup>	1.4 ns	High-Drive	
[	C540AVB	MB674xxx	549	48 (50) <sup>1</sup>	1.4 ns	High-Drive	
	C850AVB	MB673xxx	852	58 (60) <sup>1</sup>	1.4 ns	High-Drive	
	C1200AVB	MB672xxx	1245	68 (68) <sup>1</sup>	1.4 ns	High-Drive	
	C1600AVB	MB671xxx	1674	74 (76) <sup>1</sup>	1.4 ns	High-Drive	
	C2000AVB	MB670xxx	2052	88 (92) <sup>1</sup>	1.4 ns	High-Drive	
AVM-CMOS SERIES	C1502AVM	MB662xxx	1564	107 (109) <sup>2</sup>	1.4 ns	4K ROM/2K RAM <sup>3</sup>	
	C2301AVM	MB661xxx	2375 117 (119) <sup>2</sup> 1.4 ns		1.4 ns	2K ROM/1K RAM <sup>3</sup>	
Notes:	C4002AVM	MB660xxx	4087	120 (122) <sup>2</sup>	1.4 ns	4K ROM/2K RAM 3	

- 1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.
- 2. When ROM is provided.
- 3. Available options.

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# **ELECTRICAL CHARACTERISTICS**

# ABSOLUTE MAXIMUM RATINGS 1

 $(V_{ss} = 0V.)$ 

Rating	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V <sub>DD</sub>	V <sub>ss</sub> - 0.5	- 1	6.0	volts
Input Voltage	Vı	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	volts
Output Voltage	V <sub>o</sub>	V <sub>SS</sub> - 0.5		V <sub>DD</sub> + 0.5	volts
Output Current 2 AVB	Ios	-80	-	140	mA
Output Current 2AV, AVM	Ios	-40	- 1	70	mA
Storage Temperature	T <sub>STG</sub>	-65 Ceramic	-	150 Ceramic	°c
	isia	-40 Plastic	-	125 Plastic	°c
Bias Temperature	T <sub>bias</sub>	-40 Ceramic	_	125 Ceramic	°c
	· bias	-25 Plastic	_	85 Plastic	°c

### Notes:

- 1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions of recommended operation. Exposure to absolute maximum ratings for extended periods may affect device reliability.
- 2. No more than one output can be shorted at a time and no output can be shorted for more than one second.

# RECOMMENDED OPERATING CONDITIONS

 $(V_{ss} = 0V.)$ 

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V <sub>DD</sub>	4.75	5.0	5.25	volts
Input High Voltage	V <sub>IH</sub>	2.2	-	-	volts
for CMOS Inputs	V <sub>IH</sub>	V <sub>DD</sub> x 0.7	-	-	volts
Input Low Voltage	V <sub>IL</sub>	<del>-</del> · .	-	0.8	volts
for CMOS Inputs	V <sub>IL</sub>	-	-	V <sub>DD</sub> x 0.3	volts
Ambient Temperature	TA	0 .	-	70	°c

AV, AVM SERIES CAPACITANCE (Ta = 25 °C, V<sub>DD</sub>= V<sub>I</sub> = 0 volts, f = 1 MHz.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	CIN	-	-	9	pF
Output Capacitance	C <sub>OUT</sub>	-	-	9	pF
I/O Pin Capacitance	C <sub>1/O</sub>	_	-	11	pF

# **AVB SERIES CAPACITANCE**

 $(Ta = 25 \, ^{\circ}C, \, V_{DD} = V_{I} = 0 \, \text{volts}, \, f = 1 \, \text{MHz.})$ 

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	CIN	_	_	8	pF
Output Capacitance	C <sub>OUT</sub>	-	_	16	pF
I/O Pin Capacitance	G <sub>1/0</sub>	_	-	21	pF

# DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Current (Steady state, V <sub>I</sub> = 0V or V <sub>DD</sub> )	I <sub>DDS</sub>	-	-	100	μА
Output High Voltage (I <sub>OH</sub> = -0.4 mA)	V <sub>OH</sub>	4.2	-	V <sub>DD</sub>	volts
for Driver Output (I <sub>OH</sub> = -0.4 mA)	V <sub>OH</sub>	4.2	-	V <sub>DD</sub>	volts
Output Low Voltage (I <sub>OL</sub> = 3.2 mA)	V <sub>OL</sub>	V <sub>SS</sub>	-	0.4	volts
for Driver Output (I <sub>OL</sub> = 10.0 mA)	V <sub>OL</sub>	V <sub>SS</sub>	-	0.5	volts
Input High Voltage	Vн	2.2	-	-	volts
for CMOS Input	V <sub>IH</sub>	V <sub>DD</sub> x 0.7	-	-	volts
Input Low Voltage	V <sub>IL</sub>	_	-	0.8	volts
for CMOS Input	V <sub>IL</sub>	-	-	V <sub>DD</sub> x 0.3	volts
Input Leakage Current (V <sub>I</sub> = 0 - V <sub>DD</sub> )	I <sub>LI</sub>	-10	-	10	μА
Input Leakage Current (3-state, V <sub>I</sub> = 0 - V <sub>DD</sub> )	I <sub>LZ</sub>	-10	_	10	μА
Input Pull-Up/Down Resistor (Pull up: V <sub>IL</sub> = 0V, Pull down V <sub>IH</sub> = V <sub>DD</sub> )	RP	25	50	100	kΩ

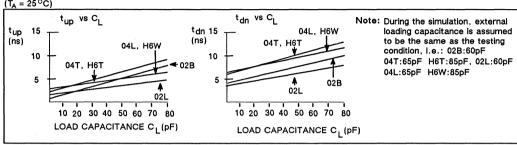
# AC CHARACTERISTICS DELAY MULTIPLIERS FOR PRE-LAYOUT SIMULATION

(See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Propagation Delay	t <sub>pd</sub>				
Enable Time	t <sub>PZL</sub> /t <sub>PZH</sub>				
Disable Time	t <sub>PLZ</sub> /t <sub>PHZ</sub>	Typ x 0.45		Typ x 1.6	ns
Set-up Time	t <sub>SD</sub>				
Hold Time	t <sub>HD</sub>				
Pulse Width	t <sub>cw</sub>				

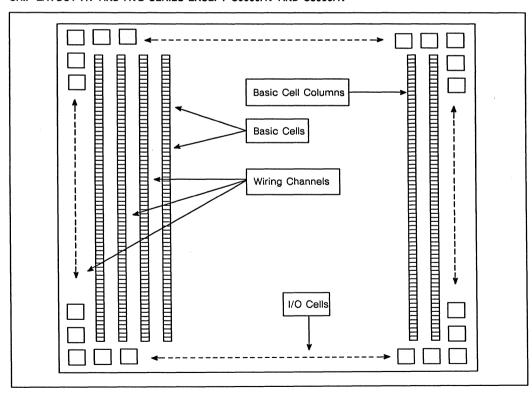
# AC CHARACTERISTICS DELAY MULTIPLIERS FOR POST-LAYOUT SIMULATION (See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
_	_	Typ x 0.50	-	Typ x 1.55	ns



# AV AND AVB-CMOS GATE ARRAY CHIP LAYOUT AND ORGANIZATION

### CHIP LAYOUT AV AND AVB SERIES EXCEPT C6600AV AND C8000AV



# AV AND AVB ORGANIZATION

Device	Total Basic Cells	Columns	Basic Cells per Column	Total I/O Cells
C350AVB	357	7	`51	38 (42) <sup>1</sup>
C540AVB	549	9	61	48 (50) <sup>1</sup>
C850AVB	852	12	. 71	58 (60) <sup>1</sup>
C1200AVB	1245	. 15	83	68 (68) <sup>1</sup>
C1600AVB	1674	18	93	74 (76) <sup>1</sup>
C2000AVB	2052	18	114	88 (92) <sup>1</sup>
C2600AV	2640	22	120	106
C3900AV	3900	25	156	127
C5000AV	5022	27	186	127

### Note:

# C6600AV, C8000AV AND AVM GATE ARRAY CHIP LAYOUT AND ORGANIZATION

# C6600AV, C8000AV CHIP LAYOUT

For C6600AV each block may vary from 1000 to 2000 basic cells.  For C8000AV each block is fixed at 2000 basic cells.	
For automatic placement and routing, the maximum basic cells used for each block should not exceed 90% of the total available in that block.	

# C6600AV, C8000AV ORGANIZATION

Device	Total Basic Cells	Blocks	BC/Block	Rows/Block	Columns/Block	Total I/O Cells
C6600AV	6664	4	1000 - 2000	-	Variable	160
C8000AV	8000	4	2000	100	20	160

<sup>1.</sup> I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.

# C1502AVM, C2301AVM CHIP LAYOUT

The maximum basic cells used for the basic cell block		
should not exceed 90% of		
the total available.		
The block is configurable for		····
either 1024 or 2304 total bits	LUIIIIIIII PAGIG GELL	Pi cor
organized from 2-bits per	BASIC CELL	BLOCK
word to 32-bits per word, or		
9-bits per word to 36-bits		
per word.	[11111111111111111111111111111111111111	111111111111111111111111111111111111111
8-bit word sizes and larger		
(for C2301AVM) or 18-bit	1 111111111111111111111111	
word sizes and larger (for		
C1502AVM) allow division of		<del>''''''</del> ''''
the RAM block into two	RAM or RO	M BLOCK
separate RAMSs.		mmm);;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
ROM can be provided in		
place of RAM. The ROM		
block is configurable for		
either 2048 or 4608 total		
bits.		

# C4002AVM CHIP LAYOUT

For automatic placement and routing the maximum basic cells should not exceed 90% of the total available.

The RAM block is configurable for 2304 total bits organized from 9 bits per word to 36 bits per word.

18-bit word sizes and larger allow division of the RAM block into two separate RAMs.

ROM can be provided in place of RAM. The ROM block is configured for 4608 total bits.

# C1502AVM, C2301AVM, C4002AVM ORGANIZATION

Device	Total Basic Cells	Columns	BC/Column	RAM Size	Total I/O Cells
C1502AVM	1564	23	68	2K, 9-bit to 36-bit	107 (109) <sup>1</sup>
C2301AVM	2375	25	95	1K, 4-bit to 32-bit	117 (119) <sup>1</sup>
C4002AVM	4087	6 25	202 115	2K, 9-bit to 36-bit	120 (122) 1

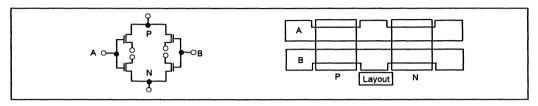
# Note:

<sup>1.</sup> When ROM is provided.

# **DESIGN COMPONENTS**

# BASIC CELL

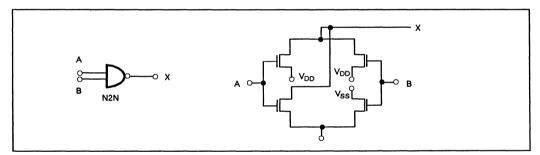
An unprogrammed gate array is an array of basic cells. Thus the "gates" in a gate array are actually the basic cells which will make up final logic. Fulltsu's basic cell contains enough transistors to form a two-input NAND gate.



Unprogrammmed Basic Cell

### **UNIT CELL**

A design is implemented in a gate array by logicially combining unit cells from the Fujitsu unit cell library to form the logic. Fujitsu provides unit cells to perform most common logic functions and the designer need only name the unit cells required to form the higher level logic functions of his design.

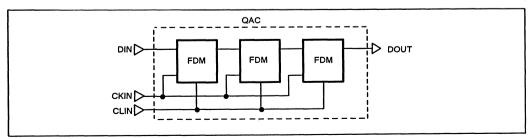


Two-Input NAND Gate Unit Cell (One Basic Cell)

A two-input NAND gate requires only one basic cell to implement. Other unit cells may require as many as 60 or more basic cells. (C47, a counter, requires 68.) Over 100 unit cells are available for design with AV/AVB/AVM-CMOS arrays.

### **USER MACROS**

User Macros are groups of unit cells which perform an identifiable function within the design. It is a user macro because it is defined by the designer. The primary utility of a user macro is that it allows the designer to compose a macro function from unit cells once, then use it any number of times simply by calling it by name.



User Macro QAC is Composed of Three FDM Unit Cells

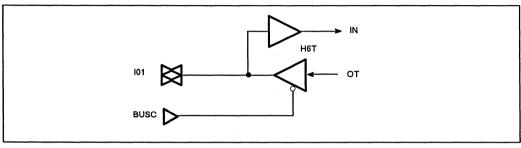
MB65xxxx MB66xxxx MB67xxxx

# F-MACROS

F-Macros are created and offered by Fujitsu to emulate the function of popular industry-standard TTL devices. They are identical in application to user macros. Using F-Macros, a designer may convert an existing design directly into gate array. For example, the 74LS191 function is emulated by the Fujitsu F191 F-Macro.

### I/O Cells

The I/O cells located on the periphery of the gate array chip are programmable to any of the input or output buffers available. The actual location of an I/O buffer on the chip is determined by the location on the chip of the associated circuitry and any pin location requirements that may be in effect.



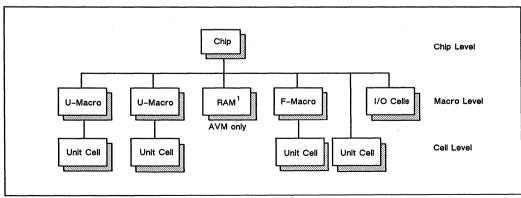
**Bidirectional Buffer** 

# **DESIGN DESCRIPTION**

### **DESIGN DESCRIPTION**

Fujitsu requires only two basic inputs to complete a gate array design: A Logic Description and a Test Description. The logic description defines the logical function of the circuit to be implemented in the array. The test description defines the electrical operation required.

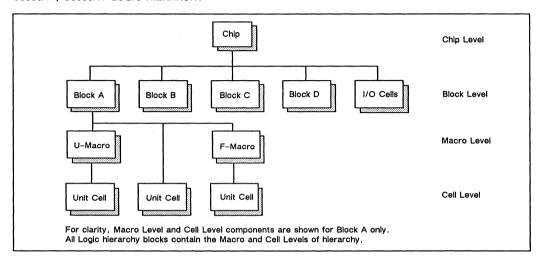
# AV, AVB AND AVM LOGIC HIERARCHY



# Note:

1. ROM can be made available in place of RAM.

### C6600AV, C8000AV LOGIC HIERARCHY



### LOGIC DESCRIPTION

The Logic Description, sometimes called a "netlist," calls out the unit cells utilized and their interconnection to form the designer's circuit. Fujitsu uses a proprietary description language, the Fujitsu Logic Description Language (FLDL), to enter the logic description language into the design flow to produce the array design. Designers may prepare their logic description using FLDL or use other description media which Fujitsu will convert to FLDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. In all cases, the design description must follow the fundamental design description structure provided by the logic hierarchy. In many cases Fujitsu will provide turnkey design services.

### LOGIC HIERARCHY

The Logic Description is organized into a hierarchy of design components. The logic hierarchy provides the fundamental structure for all logic description inputs and allows a designer to divide his logic into major macro functions and follow a step-by-step approach in describing their interconnection. User Macros may be created to allow repeating the same logic function many times in the design without describing the entire function each time. Fujitsu provides predefined macros (F-Macros) which duplicate the function of many popular industry-standard TTL devices and RAM macros which provide from 1K to 2K of single-port static RAM on chip. Also, ROM macros can be provided. The C6600AV and C8000AV are further divided into "blocks" of cells to ease the layout operations.

### CHIP LEVEL

The Chip Level of the logic description defines the interconnection of the design components to each other and the I/O cells. For most AY-CMOS family devices, all types of design components including user macros, F-Macros, RAM macros, ROM macros, and unit cells may be interconnected with each other and the I/O cells to form the chip level logic provided the basic cells total required does not exceed 90% of the basic cell total on the array. For the C6600AV and C8000AV, the same basic cells total restriction applies; the chip level of hierarchy describes only the interconnection of the blocks with the I/O cells to form the chip level logic.

### **BLOCK LEVEL**

The Block Level of the logic description defines the interconnection of design components to form each block of the logic description. C6600AV and C8000AV allow up to 90% of the available basic cells to be utilized for each block. Designers may utilize any of the available design components, including user macros, F-Macros and unit cells for interconnection within the blocks provided the basic cell total required to implement the block design does not exceed the maximum allowed for the block. C6600AV provides a flexible block arrangement, allowing block sizes to range between 1000 and 2000 basic cells provided the total does not exceed 90% of the total available on the array.

### MACRO LEVEL

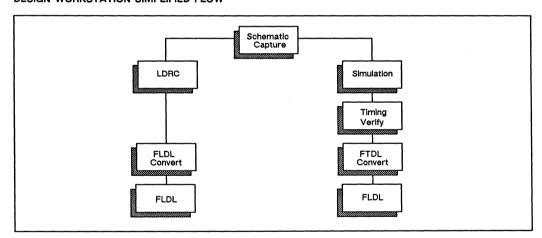
The Macro Level of the logic description defines the interconnection of unit cells to form user macros. F-Macros may not be used to form user macros. Nor may user macros be nested to form other user macros. The total number of basic cells included in one User Macro can be larger than the total number of basic cells available in one column of the array provided the number of BCs in any of the Unit Cells used in the User Macro does not exceed the total number of basic cells available in one column of the array.

### **TEST DESCRIPTION**

The Test Description defines the electrical performance required of the finished array. Test descriptions are used for all simulation operations and are ultimately converted into final test programs for prototype and production testing. Fujitsu utilizes the proprietary Fujitsu Test Data Description Language (FTDL) for all test description inputs to the design operation. As with the logic description, designers may submit test descriptions utilizing other media and Fujitsu will convert to FTDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. Turnkey services may be available. A complete test description will include D.C. testing and functional testing. Delay testing may be performed under some conditions.

### DESIGN DEVELOPMENT FLOW

### DESIGN WORKSTATION SIMPLIFIED FLOW



### WORKSTATION DESIGN

Fujitsu provides workstation support software free of charge to designers using workstations manufactured by Dalsy, Valid or Mentor. This software includes a complete design library of unit cells, I/O cells, and memory macros for AV-CMOS gate arrays and conversion programs which generate the logic and test descriptions in the FLDL and FTDL languages required for design input to Fujitsu.

### FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY

Fujitsu accepts a variety of design input media but all media must be converted to logic and test descriptions using the FLDL and FTDL description languages. Fujitsu may request additional engineering fees for conversion. Logic and test descriptions are collected into data files for access by the Fujitsu CAD system. The test data file provides the basic information used to conduct simulations and generate the final test program.

### LDRC

The Logic Design Rule Check conducts a verification that no design rule violations for interconnect, hierarchy or design description language syntax have occurred, and that the description is complete. Fujitsu will work with the designer to resolve any discrepancies before proceeding with the design development.

1

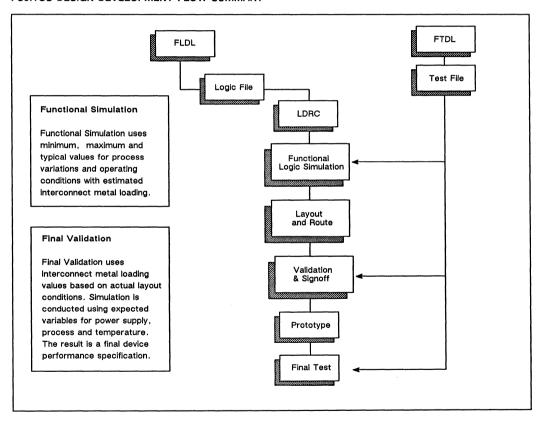
### SIMULATION

The Functional Logic Simulation is conducted using minimum, maximum and typical values for process, power supply and temperature conditions, with estimated interconnect metal loading. The functional logic simulation must successfully demonstrate device operation according to the designer's test description before any layout operations are attempted.

### FINAL VALIDATION

Final Validation is conducted to produce the device operating specification for approval and signoff by the designer. The simulation is conducted using values for interconnect metal loading based on the actual layout. Full range values for process, temperature and power supply variation are also used. A final operating specification is presented to the designer which defines the parameters which will be guaranteed by Fujitsu in the prototype and production devices.

### FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY



# **PROTOTYPES**

At the completion of the design development Fujitsu provides the designer with prototypes for on-site design evaluation. Ten prototype devices (Five for C8000AV) are provided with the development fee. Additional prototypes may be provided for an additional fee.

# UNIT CELL LIBRARY

	Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
INVERTER, CLOCK	V1N	Inverter	1	КЗВ	Gated Clock Buffer (AND)	3
BUFFER FAMILY	V2B	Power Inverter	1	K4B	Gated Clock Buffer (OR)	3
	K1B	Clock Buffer	2	ксв	Block Clock Buffer	11
	K2B	Power Clock Buffer	3	-	-	-
NAND FAMILY	N2N	2-input NAND	1	N6B	6-input Power NAND	5
	N3N	3-input NAND	2	N8B	8-input Power NAND	6
	N4N	4-input NAND	2	N9B	9-input Power NAND	7
	N2B	2-input Power NAND	3	NCB	12-input Power NAND	9
	N3B	3-input Power NAND	3	NGB	16-input Power NAND	11
	N4B	4-input Power NAND	. 4	-	-	
AND FAMILY	N2P	2-input Power AND	2	N4P	4-input Power AND	3
	N3P	3-input Power AND	3	-	=	- 1
		1				
NOR FAMILY	R2N	2-input NOR	1	R6B	6-input Power NOR	5
	R3N	3-input NOR	2	R8B	8-input Power NOR	6
	R4N	4-input NOR	2	R9B	9-input Power NOR	7
	R2B	2-input Power NOR	3	RCB	12-input Power NOR	9
	R3B	3-input Power NOR	3	RGB	16-input Power NOR	11
	R4B	4-input Power NOR	4	-	-	_
OR FAMILY	R2P	2-input Power OR	2	R4P	4-input Power OR	3
	R3P	3-input Power OR	3	-	-	-
ENOR/EOR	X1B	Power ENOR	4	X2B	Power EOR	4
	L		<b>.</b>			
AND-NOR FAMILY	D14	2-wide 3-AND 4-input AND-OR invert	2	D34	3-wide 2-AND 4-input AND-OR invert	2
	D23	2-wide 2-AND 3-input AND-OR Invert	2	D44	2-wide 2-OR 2 AND 4-input AND-OR invert	2
	D24	2-wide 2-AND 4-input AND-OR Invert	2	_	-	-
OR-NAND FAMILY	G14	2-wide 3-OR 4-input OR-AND Invert	2	G34	3-wide 2-OR 4-input OR-AND invert	2
	G23	2-wide 2-OR 3-input OR-AND Invert	2	G44	2-wide 2-AND 2-OR 4-input OR-AND invert	2
	G24	2-wide 2-OR 4-input OR-AND invert	2	-	-	-

**UNIT CELL LIBRARY** 

Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
T24	Power 2-AND 4-wide	6	U24	Power 2-OR 4-wide	6
T26	Power 2-AND 6-wide	9	U26	Power 2-OR 6-wide	9
T28	Power 2-AND 8-wide	11	U28	Power 2-OR 8-wide	11
T32	Power 3-AND 2-wide	5	U32	Power 3-OR 2-wide	5
T33	Power 3-AND 3-wide	7	U33	Power 3-OR 3-wide	7
T34	Power 3-AND 4-wide	9	U34	Power 3-OR 4-wide	9
T42	Power 4-AND 2-wide	6	U42	Power 4-OR 2-wide	6
T43	Power 4-AND 3-wide	9	U43	Power 4-OR 3-wide	9
T44	Power 4-AND 4-wide	11	U44	Power 4-OR 4-wide	11

# FLIP-FLOP FAMILY

FD2	Power DFF	8	FDD	Positive Edge Power DFF with Clear/Preset	11
FD3	Power DFF with Preset	9	FDE	Positive Edge Power DFF with Clear	10
FD4	Power DFF with Clear/ Preset	10	FDG	Positive Edge with Clear	9
FD5	Power DFF with Clear	9	FJD	Positive Edge Power JKFF with Clear	12
FD6	DFF	7	FJ4	Power JKFF with Clear	11
FD7	DFF with Clear	8	FJ5	Power JKFF with Clear/ Preset	12
FD8	DFF with Latch	9	-	-	-

FLIP-FLOP FAMILY USING TRANSMISSION GATES

FDM	DFF	6	FDP	DFF with Set/Reset	8
FDN	DFF with Set	7	FDQ	4-bit DFF	21
FDO	DFF with Reset	7	FDR	4-bit DFF with Clear	26
FDS	4-Bit DFF	20	-	_	_

# LATCH FAMILY

LT1	SET-RESET with Clear	4	LT3	4-bit Data Latch	15
LT2	1-bit Data Latch	4	LT4	4-bit Data Latch	13
LTK	Data Latch	4	LTL	Data Latch with Clear	5
LTM	4-Bit Data Latch with Clear	15	-	-	-

# SHIFT REGISTER FAMILY

FS1	4-bit S <sub>in</sub> -P <sub>out</sub>	18	FS3	4-bit with Async Load	34
FS2	4 bit S <sub>in</sub> -P <sub>out</sub> with Sync Load	30	-	-	-

DECODER FAMILY

DE2	2:4 Decoder	5	DE3	3:8 Decoder	15
	<del></del>				

# **COUNTER FAMILY**

1	C11	Flip-Flop for Counter	11	C43	4-bit Sync UP with Clear	48
1	C41	4-bit Async	24	C45	4-bit Sync UP	48
1	C42	4-bit Sync	32	C47 <sup>1</sup>	4-bit Sync UP/DOWN	68

# Note:

<sup>1.</sup> C47 is not available for C-350AVB and C540AVB.

# **UNIT CELL LIBRARY**

	Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
SELECTOR FAMILY	T2B	2:1 Selector	2	V3A	1:2 Selector	2
	T2C	Dual 2:1 Selector	4	V3B	Dual 1:2 Selector	3
	T2D	2:1 Selector	2	T5A	4:1 Selector	5

# **COMPARATOR**

MC4	4-bit Magnitude Comparator	42	-	_	-
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# ADDER FAMILY

A1N	1-bit Full Adder	8	A4H	4-bit Fuli Adder	50
A2N	2-bit Full Adder	16	_		_

# SCHMITT TRIGGER

# SM1 Schmitt Trigger 8 SM2 Schmitt Trigger 7

# DELAY UNIT

ſ	BD3	Buffer (Delay Cell)	5	BD6	Buffer (Delay Cell)	17
ſ	BD5	Buffer (Delay Cell)	9	-	_	-

# I/O CELL FAMILY

I2B	Input Buffer	0	IKB	Clocked Input Buffer(Inverting)	. 0
12BU <sup>2</sup>	I2B with Input Pull-up	0	IKBU <sup>2</sup>	IKB with Input Pull-up	0
I2BD <sup>2</sup>	I2B with Input Pull-down	0	IKBD <sup>2</sup>	IKB with Input Pull-down	0
ILB	Clocked Input Buffer	0	12C	CMOS Interface Input Buffer	0
ILBU <sup>2</sup>	ILB with Input Pull-up	0	120	(True & Inverter)	
ILBD <sup>2</sup>	ILB with Input Pull-down	0	I2CU <sup>2</sup>	I2C with Input Pull-up	0
IT1	Input Buffer for Schmitt-	0	I2CD <sup>2</sup>	I2C with Input Pull-down	0
	Trigger Input		Н6Т	Tri-state Output & Input Buffer	0
IT1U <sup>2</sup>	IT1 with Input Pull-up	0	H6TU <sup>2</sup>	H6T with Input Pull-up	0
IT1D <sup>2</sup>	IT1 with Input Pull-down	0	H6TD <sup>2</sup>	H6T with Input Pull-down	0
O2B	Output Buffer	0	O4T	Tri-state Output Buffer	0
02L <sup>2</sup>	Power Output Buffer (True)	0	O4W <sup>2</sup>	Power Tri-state Output Buffer	0
H6W <sup>2</sup>	Power Tri-state Output and	0	0,,,	(True)	
ПОТ	Input Buffer (True)		H6C <sup>2</sup>	Tri-state Output and CMOS	0
H6WU <sup>2</sup>	H6W with Input Pull-up	0		Interface input Buffer (True)	
H6WD <sup>2</sup>	H6W with Input Pull-down	0	H6CU <sup>2</sup>	H6C with Input Pull-up	0
	Power Tri-state Output and	0	H6CD <sup>2</sup>	H6C with Input Pull-down	0
H6E <sup>2</sup>	CMOS Interface Input Buffer	U	H6EU <sup>2</sup>	H6E with Input Pull-up	0
	(True)		H6ED <sup>2</sup>	H6E with Input Pull-down	0

# Note:

- 1. SM1 and SM2 must not be used together in one chip.
- 2. Available only for AVB.

# F-MACRO LIBRARY

# F-MACRO FUNCTION

Fujitsu's F-Macros are direct software macro implementations of popular industry-standard TTL functions. They may be used in the design exactly the same as user macros. Designers's converting existing TTL designs to gate array will find the F-Macro a particularly useful implementation.

F-MACROS AVAILABLE TO REPLACE THESE TTL DEVICES

Device	Basic Cells	Device	Basic Cells	Device	Basic Cells
7400		7498	36	74176	76
7402		7499		74177	72
7404		74100 60 74178		74178	63
7408		74101		74179	71
7410		74102		74180	33
7411		74103		74181	
7420		74106		74182	49
7421		74107		74183	36
7425		74108		74190	106
7427		74109		74191	73 <sup>1</sup>
7430		74112		74192	92
7432		74113		74193	82
7442	32	74114		74194	78
7443	32	74116	82	74195	51
7444	32	74120	34	74198	132
7451	7	74135		74199	98
7454	9	74137	48	74260	1
7455	6	74138	28	74261	107
7456		74139	26	74273	
7457		74147	49	74278	46
7464	9	74148	53	74279	18
7468	89	74150	112	74280	57
7469	79	74151	54	74283	50
7473		74152	29	74290	45
7474		74153	24	74293	33
7475	32	74154	96	74298	36
7476		74155	29	74352	28
7477	18	74157	23	74375	18
7478		74158	23	74377	71
7482	16	74160	82	74378	55
7483	50	74161	48	74379	39
7485	42	74162	83	74381	192
7486		74163	48	74382	201
7487	1	74164	70	74386	
7490	41	74165	73	74390	82
7491	43	74166	80	74393	52
7492	64	74168	111	74396	60
7493	33	74169	74 <sup>1</sup>	74398	37
7494	47	74171		74399	37
7495	42	74174	46		
7496	56	74175	32		
7497					

Note:
1. These F-Macros utilize complex unit cells and may not be available for smaller arrays.

# RAM MACRO LIBRARY

# C2301AVM

32-W	ORD
RAM	<b>MACROS</b>

RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration
R51	32-word x 32-bit	-
R51A	32-word x 28-bit	32-word x 4-bit
R51B	32-word x 24-bit	32-word x 8-bit
R51C	32-word x 20-bit	32-word x 12-bit
R51D	32-word x 16-bit	32-word x 16-bit

# 64-WORD RAM MACROS

R61	64-word x 16-bit	_
R61A	64-word x 12-bit	64-word x 4-bit
R61B	64-word x 8-bit	64-word x 8-bit

# 128-WORD RAM MACROS

R71	128-word x 8-bit	_
R71A	128-word x 4-bit	128-word x 4-bit

# 256-WORD RAM MACROS

R83	256-word x 4-bit	_		
R83A	256-word x 2-bit	256-word x 2-bit		

# C1502AVM/C4002AVM

64-WORD RAM MACROS

RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration		
R610	64-word x 36-bit	<del>-</del>		
R611	64-word x 20-bit	64-word x 16-bit		

128-WORD RAM MACROS

R711	128-word x 18-bit	-
R712	128-word x 9-bit	128-word x 9-bit

256-WORD RAM MACROS

R87	256-word x 9-bit	-

# **ROM MACRO LIBRARY**

# C2301AVM

256-WORD ROM MACROS

ROM Macro Name	Configuration	
YRn	256-word x 8-bit	-

Note:

Contact nearest Fujitsu Design Center for additional ROM data.

# PACKAGE AVAILABILITY MATRIX

DUAL IN-LINE PACKAGES, PLASTIC SHRINK TYPE (SH-DIP)

DUAL IN-LINE PACKAGES
PLASTIC SKINNY TYPE (SK-DIP)

### DUAL IN-LINE PACKAGES, PLASTIC (PDIP)

	PACKAGE PRODUCT		PDIP- 18	PDIP- 20	PDIP- 22	PDIP- 24	PDIP- 28	PDIP- 40	PDIP- 42	PDIP- 48
CMOS	350AVB	•	•	•	•	•	•	•	•	
	540AVB	٠	٠	•	•	•	•	•	•	
	850AVB			•	•	•	•	•	•	
	1200AVB				•	•	•	•	•	•
	1502AVM					•	•	•	•	
	1600AVB				•	•	•	•	•	•
	2000AVB					•	•	•	•	•
	2301AVM					•		•	•	
	2600AV					•	•	•	•	•
	3900AV					•		•	•	
	4002AVM									
	5000AV							•		
	6600AV									
	8000AV									

PACKAGE PRODUCT	DIP- 28SH SHRINK	DIP- 42SH SHRINK	DIP- 48SH SHRINK	DIP- 64SH SHRINK	DIP- 24SK SKINNY
350AVB	•	•	•		
540AVB	•	•	•	•	
850AVB	•	•	•	•	
1200AVB	•	•	•	•	
1502AVM		•	•	•	
1600AVB	•	٠	•	•	
2000AVB		•	•	•	
2301AVM			•	•	
2600AV		•	•	•	
3900AV			•	•	
4002AVM					
5000AV					
6600AV					
8000AV		1		ļ	

# PLASTIC LEADED CHIP CARRIERS (PLCC)

11100001	20	"	"	04
350AVB	٠	•		
540AVB	•	•		
850AVB	•	•		
1200AVB	•	•		
1502AVM		•	•	•
1600AVB	•	•	•	
2000AVB		•	•	
2301AVM		•	•	•
2600AV	•	•	•	•
3900AV		•	•	•
4002AVM				

PACKAGE PLCC- PLCC- PLCC- PLCC- PLCC- PRODUCT 28 44 68 84

### FLAT PACKS, PLASTIC (FPT)

TEAT FACILITY										
PACKAGE PRODUCT	FPT- 16	FPT- 20	FPT- 24	FPT- 28	FPT- 48	FPT- 64	FPT- 80	FPT- 100	FPT- 120	FPT- 160
350AVB	•	•	•	•	•		,			
540AVB	•	•	•	•	•	•				
850AVB			•	•	•	•				
1200AVB			•	•	•	•	•			
1502AVM					•	•	•	•		
1600AVB					•	•	•			
2000AVB					•	•	•	•		
2301AVM					•	•	•	•		
2600AV					•	•	•	•		
3900AV					•	•	•	•		
4002AVM										
5000AV							•	•		
6600AV										
8000AV										

- - QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW
- ☐- PACKAGE COMBINATION UNDER DEVELOPMENT

5000AV 6600AV 8000AV

**CMOS** 

Note:
Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions. Plastic PGA packages (64, 88, 135, 179-pln) are now under development.

# А

## PACKAGE AVAILABILITY MATRIX

## **DUAL IN-LINE PACKAGES, CERAMIC (CDIP)**

## смоѕ

PACKAGE PRODUCT		CDIP- 18	CDIP- 20	CDIP- 22	CDIP- 24	CDIP- 28	CDIP- 40	CDIP- 42	CDIP- 48
350AVB	•	•	•	•	•	•	•		
540AVB	•	•	•	•	•	•	•		
850AVB				•	•	•	•		
1200AVB				•	•	•	•	•	•
1502AVM							•	•	•
1600AVB				•	•	•	•	•	•
2000AVB						•	•	•	•
2301AVM							•	•	•
2600AV						•	•	•	•
3900AV							•	•	•
4002AVM									
5000AV									
6600AV									
8000AV									

CERAMIC LEADLESS CHIP CARRIERS (LCC) CERAMIC J-LEADED CHIP CARRIERS (JLCC) CERAMIC PIN GRID ARRAY (PGA)

## CMOS

PACKAGE PRODUCT	LCC- 28	LCC-	LCC- 64	LCC-	JLCC- 68	JLCC- 84	PGA- 64	PGA- 88	PGA- 135	PGA- 179	PGA- 256
350AVB	•	•			-				750		
540AVB	•	•	•				•				
850AVB	•	•	•				•				
1200AVB	•	•	•				•				
1502AVM		•	•				•	•	•		
1600AVB	•	•	•				•	•			
2000AVB		•	•				•	•			
2301AVM		•	•				•	•	•		
2600AV		•	•				•	•	•		
3900AV		•	•				•	•	•		
4002AVM			•	•			•	•	•		
5000AV		•	•				•	•	•		
6600AV			•				•	•	•	•	
8000AV			•				•	•	•	•	

• - QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW

 $\square$  - PACKAGE COMBINATION UNDER DEVELOPMENT

## Note:

Ote:

Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions.

## Chapter 2 - Steps Toward Design

#### Contents of This Chapter

- 2.1 Introduction
- 2.2 Choosing Fujitsu as your ASIC Manufacturer
- 2.3 Choosing a Device
- 2.4 Choosing a Package
- 2.5 Technical Review
- 2.6 Design Interface Options

#### 2.1 Introduction

This section of the data book takes a look at the issues that must be considered before a design is ready to be entered on a computer-aided engineering (CAE) workstation.

## 2.2 Choosing Fujitsu as Your ASIC Manufacturer

The first step in implementing a given ASIC design is to choose the manufacturer that offers semiconductor processes capable of actualizing the performance requirements of the IC. The manufacturer should also offer consistent and easily accessible customer support, timely transfer of the design into silicon, and a highly reliable end product.

The data sheets and supplementary information in Chapter 1 enable customers to determine whether their requirements fall within the broad range of Fujitsu's technical capability.

The second step is to discuss the design requirements with one of Fujitsu's Field Applications Engineers at either a Regional Sales Office or a Technical Resource Center. Regional Sales Office and Technical Resource Center addresses and telephone numbers are listed at the back of this volume. Fujitsu's Field Applications Engineers work with each customer to determine which technology would be most suitable for a given design, taking into account the factors outlined in more detail below.

Fujitsu's highly developed software tools, high-capacity manufacturing facilities (the largest in the world) and long history of excellence in the field (Fujitsu has been producing custom gate arrays commercially since 1974) enable customers to turn designs into highly reliable products in a cost-effective time frame.

## 2.3 Choosing A Device

Speed is usually the deciding factor in choosing the technology for a design, but sometimes special requirements such as package availability, on-chip memory (available in the AU and AVM technology), or the necessity for battery power (a feature of the AVL technology) influence the final decision.

Usually the device type is a requirement of the design and is chosen before the package size is determined. The size of the package will depend on array size, partitioning, the number of power

and ground pins required by the SSOs (simultaneously switching outputs) used in the design, and the high power drive buffers and clock inputs used in the design.

To determine the most suitable device within a given technology, the designer must determine the gate count and pinout requirements from the schematic diagram of the design to be implemented.

The functions in the schematic or logic block diagram may be described using standard logic functions, programmable logic, or Fujitsu's Unit Cell Library.

Gate counts are calculated in terms of how many basic cells make up each component function (unit cell). This number is given for each unit cell in the unit cell library for each technology. By adding up the number of basic cells used in each logic element in a design, a designer can arrive at a good first estimate of the design complexity.

In technologies in which the basic cells are arranged in single columns (AV/AVB/AVL/AVM), unit cells may not bridge two basic cell columns, and therefore, there may not be more unit cells requiring the majority of cells in a column than there are columns. In the double-column technologies (UHB and AU), unit cells take up parts of two adjacent columns. It is recommended that no more than 90% of the basic cells in a channeled array be used. Respecting this limitation facilitates fully automated layout.

#### 2.4 Choosing a Package

Before the final choice of an array can be made, however, the choice of a package must be considered. The intended use of the IC generally determines the type of package used: packaging issues are discussed in detail in the application note "Choosing the Best Package for Your ASIC Design" included in Chapter 8 of this data book. The types of packages available for Fujitsu's ASIC products are shown in Table 2–1. The number of pins per package for each device is shown on the data sheets in Section 1.

Table 2-1. Fujitsu CMOS ASIC Package Options

Package Type	Package Options
Standard DIP (100 mil)	16 – 64 pins, Ceramic 16 – 48 pins, Plastic
Shrink DIP (70 mil )	28 – 42 pins, Ceramic 28 – 64 pins, Plastic
Skinny DIP (300 mil row space)	22 - 28 pins, Plastic
PLCC	22 - 28 pins, Plastic
LCC	28 - 64 pins, Ceramic
Flat Package	16 - 160 pins, Plastic 48 - 260 pins, Ceramic
Pin Grid Array	64 - 401 pins, Ceramic 64 - 135 pins, Plastic

The size of the package chosen is regulated by the number of inputs and outputs required, the number of Vss and VDD pins required, and the number of simultaneously switching outputs (SSOs) included in the design.

## Package Size vs. SSOs

The number of SSOs can influence the size of the package chosen because additional ground pins are sometimes required in a design that has more simultaneously switching outputs than is acceptable for a given package type. Simultaneously switching outputs are those that switch from a logic low or a high impedance (Z) to a logic high or from a logic high or Z state to a logic low within 20 nanoseconds of each other.

A general rule is to use one ground pin for each group of 10 simultaneously switching low power outputs or for 20 non-simultaneous outputs. For the actual restrictions for each technology and situation, the design manual must be consulted.

Although the VSS and VDD pins are preassigned in each package and cannot be changed, alternate packages are available offering varying numbers of power and ground pins.

#### 2.5 Technical Review

When the CMOS technology, the device, and the package have been decided upon, the customer and Fujitsu's Field Applications Engineer hold a technical review to ensure that all the information necessary to implement the design is available and to allow Fujitsu to derive a schedule and price. Often, especially for new customers, a technical review form, such as the one reproduced below and on the following pages as Figure 2–1, is used.

Technical Resource Center Engineer : Field Applications Engineer :								
Technical Review Form Fujitsu Microelectronics Incorporated ASIC Products								
	RFQ #							
	Quote #							
Company:								
Prepared by:								
Customer Design Engineer:								
Designer's Phone Number:								
Customer Engineering Manager:								
Design City/State:								
Production City/State:								
Reviewed by:								
The purpose of this form is to compile data that will impact or affect the cost and delivery of Custom/Semicustom products. Any price or delivery quotation will be based solely on the information provided in this document.  Customer Part Number:								
Customer Program Name:								
Customer Program Name:  If Member of a Set, Set Name:								

Figure 2-1a. Sample Technical Review Form

1.0	General Information						
1.1	Device Technology (specify exact technology and size)						
1.2	Design .	Approach	n:				
	Gate Ar	ray		S	standard Cell		
1.3	Number	of hierar	chical lev	els in desigr	1;		
1.4	Logic Cell Count:						
	Basic C	ell Count		(non-hier	archical) without	memory	
	If hierar	chical,	Block A	Block B	Block C	Block D	
		4	Block E	Block F	Block G	Block H	
1.5	Memory	Requirer	ments				
	1.5.1	RAM		ROM	None	(Circle to indicate)	
	1.5.2	Size:					
	1.5.3	Size: Organiza	ation:				
		Size: Organiza Number	ation: of Ports:				
	1.5.3	Size: Organiza Number 1.5.4.1	ation: of Ports: Reads: _	-			
	1.5.3	Size: Organiza Number 1.5.4.1 1.5.4.2	of Ports:  Reads: _  Writes: _				
	1.5.3 1.5.4	Organiza Number 1.5.4.1 1.5.4.2 State the	of Ports: Reads: _ Writes: _ e custom	RAM cell or	ganization		
1.6	1.5.3 1.5.4 1.5.5 1.5.6	Size: Organiza Number 1.5.4.1 1.5.4.2 State the Memory	ation: of Ports: Reads: _ Writes: _ e custom Cell Cou	RAM cell or	ganization		
	1.5.3 1.5.4 1.5.5 1.5.6 Special	Size:Organiza Number 1.5.4.1 1.5.4.2 State the Memory	of Ports: Reads: _ Writes: _ e custom Cell Cou	RAM cell or	ganization		
1.7	1.5.3 1.5.4 1.5.5 1.5.6 Special	Size:Organiza Number 1.5.4.1 1.5.4.2 State the Memory F-macro e Type (6)	ation: of Ports: Reads: _ Writes: _ e custom Cell Cou Requirem e.g. DIP-2	RAM cell or int	ganization		
1.7 1.8	1.5.3 1.5.4 1.5.5 1.5.6 Special Package Special	Size:Organiza Number 1.5.4.1 1.5.4.2 State the Memory F-macro Type (e) Heatsink:	ation: of Ports: Reads: _ Writes: _ e custom Cell Cou Requirem e.g. DIP-2	RAM cell or int	ganization		
1.7 1.8 1.9	1.5.3 1.5.4 1.5.5 1.5.6 Special Package Special Special	Size:Organiza Number 1.5.4.1 1.5.4.2 State the Memory F-macro Type (e) Heatsink: Carrier:	ation: of Ports: Reads: _ Writes: _ e custom Cell Cou Requirem e.g. DIP-2	RAM cell or intnents:	ganization		

Figure 2-1b. Sample Technical Review Form

1.1	.11 Number of Input Pi			is:						
	CMO	S	TT	L	-	Sch	ımitt Trig	ger		
1.12	tput Pins:	CMOS_			TTL					
1.13	3 Numb	per of Bidi	irectional	Pins: Cl	MOS		TTL			
. 1.1	4 Comp	position of	i Simultar	neously :	Switche	d Output	Groups:			
	( <u>+</u> 10	ns of eac	h other)							
	1.14.	1 Indicate	the num	ber of b	uffer ty	pes conta	ained wit	hin eac	h group.	
			O	utput But	ffer Typ	e .				
Group Number	3.2mA	6.4mA	8.0mA	10mA	12mA	12mA w/NLR	24mA w/NLR	Other	Total lou per Group	
1										
2										
3										
4										
5										
6										
Total IoL per Buffer Type										
	1.14.2	2 Other Sp	pecial Gr	oup(s)	<u> </u>	(Consul	It a TRC	Design	Engineer)	
		Group	) #		: #-		- @		-mA	
Group # : # @						-mA				
1.19	5 Total	l Number	of Groun	ıd Pins F	Required	d:				
1.10	6 Total	l Number	of Power	r Pins Re	equired:					
1.1		ts Fujitsu lo, consult					No			

Figure 2-1c. Sample Technical Review Form

	1.18	Attach a completed photocopy of the chosen pin assignment table from the Design Manual (e.g., for a C-4002AVM, LCC-68, attach Table 24).							
	Note:	The standard placement for the power supply and special purpose pins are shown in the Pin Assignment Tables. Any variation from the standard is subject to approval by Fujitsu.							
	1.19	Complete the Attached "I/O Pin Specification/Special Requirement" Form When Requesting Package Variances.							
	1.20	Maximum Output Frequency:MHz into pF Load							
		Buffer Type: CMOS TTL (Circle to indicate)							
	1.21	Maximum Input Frequency:MHz	z						
	1.22	Maximum Toggle Frequency:MHz	z						
	1.23	Crystal Oscillator Requirements:							
		On-chip Resistor Required: Yes No							
		Pin Numbers Frequency	_						
	1.24	Power Supply Requirements (Referenced to ground):							
		PS Volts <u>+</u> %							
	1.25	Customer Maximum Power Dissipation Limit:	_						
	1.26	Customer Maximum Temperature Range/Variation:							
		Min°C Max°C							
2.0	Desig	n Input Format: (Circle or Complete)							
	2.1	Logic Data: FLDL Other	_						
			_						
	2.2	Test Data: FTDL Other	_						
			_						
	2.3	Input Media: Mag Tape (IBM Standard or Non Label)							
		Diskette (Daisy, Valid, Mentor, Other)							
		File Transfer (Kermit and Telebit or Hayes Modem)							
	2.4	Workstation Used	_						
			_						

Figure 2-1d. Sample Technical Review Form

3.0	Test	Data:		-	:	-				
	3.1	Descript	ion of the FTDL							
		No. Of T	Test Blocks	Cycle Time	No. Of Test Patterns					
		Function	l:							
		2-functio	on:	*	·					
		DC:		1000ns						
(Optio	onal)	AC:								
		Other:	·							
	3.2	For an additional fee, the customer requests Fujitsu to perform fault grading on the design and provide results. Yes No								
	3.3	For an additional fee, the customer requests Fujitsu to provide a copy the test tape in the following format:								
		Sentry		Advantest	(Circle one)					
4.0	Critic	al Path P	ropagation De	lay Estimation:						
	4.1	all critic	elay calculation form, descri kimum or minimum delay re- as many sheets as neces-	-						
	4.2	Critical I	Path Description	n:						
		4.2.1	Critical Path	Name/Number:	_					
		4.2.2	Delay Require	ed:	MinMa	x				
		4.2.3	Logic Diagrai	m Drawing:						

Figure 2-1e. Sample Technical Review Form

## 2.6 Design Interface Options

The next step is to determine which computer-aided engineering (CAE) workstation will be used to enter the design. The desired result of entering the design on a CAE workstation is the generation of a successful Fujitsu Logic Description Language (FLDL) file and Fujitsu Test Description Language (FTDL) file. These two files (which may be generated on any of several different CAE workstation systems) enable Fujitsu's host mainframe to perform automated layout and rigorous test and simulation of the design.

Four popular dedicated CAE workstation systems (Valid, Mentor, Daisy, and the HP 9000) as well as several hardware-independent CAE packages support Fujitsu's design software. In addition, Fujitsu now offers design support on ViewCAD®, a computer-aided engineering system originated by Fujitsu for ASIC designs.

ViewCAD is written in the C programming language and runs on any UNIX® platform that supports the XWindow System® (such as the Sun 3 or 4 series of workstations). It includes in one package all of the necessary functions for the design, simulation, and analysis of an ASIC design. ViewCAD makes use of a graphics-oriented interface that allows visual examination of all circuits, circuit test data, and simulation results. Its final product is the logic and test data description files (FLDL and FTDL) that are required by the host mainframe computer to process a design.

Through long experience, Fujitsu has found that by far the most efficient way to achieve a trouble-free end product is for customers to implement the design on a workstation themselves. This can be done:

- (a) on CAD equipment that the customer is already using (Fujitsu provides cell library information files and the expertise to help write a conversion program to produce the FLDL and FTDL files if necessary)
- (b) on one of the design systems that specifically support Fujitsu software (Daisy, Mentor, Valid, HP 9000) either at the customer's workplace or in one of the Technical Resource Centers
- (c) on ViewCAD either on the customer's own Sun equipment or at a Technical Resource Center.

# Chapter 3 - Design Procedures

#### Contents of This Chapter

- 3.1 Introduction
- 3.2 ViewCAD Design Procedures
- 3.3 Generic Workstation Design Procedures
- 3.4 Post-Design Process

## 3.1 Introduction

This section of the data book explains the steps necessary to implement an ASIC design in one of Fujitsu's CMOS technologies using a CAE (computer-aided engineering) workstation. Designs can be implemented with Fujitsu's ViewCAD design software or with one of the CAE systems or software applications that support Fujitsu designs.

#### 3.2 ViewCAD Design Procedures

Fujitsu developed the ViewCAD design software to complement a wide range of customer third party design tools. It includes:

- A Schematic Capture Module utilizing the XWindow System
- A Logic Design Rule Check Module that screens for design violations in the areas of fanout and drive, gate count, I/O requirements, etc.
- A Test Data or Waveform Entry Module for test vector entry
- An Interactive Simulation Module that replicates the Fujitsu mainframe for both functional and timing simulation
- Conversion Modules to define the net list and test vectors in the FLDL (Fujitsu Logic
  Description Language) and FTDL (Fujitsu Test Data Description Language) formats required
  by Fujitsu's host mainframe.

Figure 3–1 shows the ASIC design flow using ViewCAD. This design flow includes the use of schematic capture and test data generated on other workstations as well as on ViewCAD. The numbers on the left side of Figure 3–1 correspond to the numbers of the paragraphs below that explain the corresponding portion of the figure.

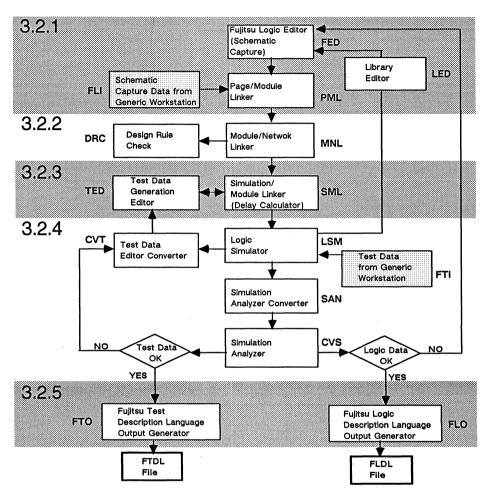


Figure 3-1. ASIC Design Flow with ViewCAD

## 3.2.1 Schematic Capture

ViewCAD users accomplish logic circuit entry (schematic capture) through the Fujitsu Schematic Editor (FED) module. After running a setup utility requiring the entry of the design name, technology series, and package type, users can insert unit cells and connect them to create circuit diagrams and see a graphic representation of the resulting schematic. The Schematic Editor also provides a basic verification routine. If the schematic has already been entered in another CAE system, it can be converted to ViewCAD-compatible data by the FLDL-to-ViewCAD translator (FLI) module. A Library Editor (LED) module is available to specify design hierarchies, create user macros, and implement blocks in partitioned arrays. ViewCAD allows the user to go back and forth between LED and FED to facilitate the development of complex hierarchical designs.

The designer then uses a Page/Module Linker (PML) module to link pages, ensuring connectivity between the pages of the schematic.

#### 3.2.2 Logic Design Rule Check

DRC, ViewCAD's Design Rule Check module, examines the data files produced by the editor and page linker modules for conformity to the design rules of the CMOS technology in which the design is executed.

Subsequently a Module/Network Linker (MNL) is run on the PML file to expand macros and link the levels of the design hierarchy to prepare the data for the logic simulator.

## 3.2.3 Circuit Test Data Entry

The designer then provides the Test Data Editor (TED) with test signals for the simulator. Like the schematic capture module, the test data generator displays the data graphically. It allows the user to create and modify signal data and to prepare the data for the simulator module by saving it in a format that the simulator understands. If test data has already been prepared on another CAE system, it can be converted to data usable to the Test Data Editor.

The Simulation Module Linker (SML), which takes the output of the Module/Network Linker and generates the delay estimates for the logic simulator, is run before the logic simulator can be executed.

#### 3.2.4 Simulation and Analysis

The Logic Simulator Module (LSM) reads the data created by SML and combines it with the test information in the TED file to run a simulation of the design.

The Test Data Editor Converter (CVT) then converts the output of the simulation module (LSM) back into a TED file. It provides the path from the simulator back to TED so that output that was previously given an undefined value of "X" can be assigned actual simulated values.

The Simulation Analyzer Converter (CVS) translates the output of the logic simulator (LSM) into an acceptable format for the simulation analyzer.

The Simulation Analyzer Module (SAN) analyzes the output from the simulator to determine whether it performs as it was intended to. SAN allows the user to display the simulation output and manipulate the display to help the user analyze the output.

## 3.2.5 Data Conversion for Mainframe Interface

The last step in the implementation of an ASIC design on ViewCAD is the generation of the all-important FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) files.

After any design errors that may have been found by simulation and analysis have been corrected in the schematic capture module, the designer runs the Fujitsu Logic Language Output Generator (FLO) module to convert the schematic data into an FLDL file for use on Fujitsu's host mainframe.

If any errors in test data are discovered during the simulation analysis process, the test data can be sent back to the Test Data Editor Converter Module to be reconverted into a form that the test Data Editor understands (since the errors must be corrected in the Test Data Editor module). After

error correction or if no errors are found, the designer sends the test data file to the Fujitsu Test Description Language Output Generator (FTO) module for conversion into an FTDL file for use on the mainframe.

## 3.3 Generic Workstation Design Procedures

Fujitsu provides ASIC Design Software Kits for designers using some of the popular design tools on generic workstations. The kits offer support for Daisy, Mentor, Valid, and HP9000 and include:

- Fujitsu Symbol Model Libraries for the CAE system's schematic capture module
- A Logic Design Rule Check module
- · Fujitsu Timing Model Libraries for the system's simulator
- A Delay Calculator module
- Conversion Modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) formats required by host mainframe computer.

These Fujitsu-supplied software modules are shown in boldface boxes in the diagram in Figure 3-2.

In addition, Fujitsu now offers FAME (Fujitsu's ASIC Management Environment), a menu-driven design management program that enables the user to select the technology, the approximate gate count and I/O, pinout, and the package requirements, and to create a design database that is referenced by the other modules to assure correct-by-construction design. FAME includes a test vector module that creates test vectors automatically for complex functions, assists in defining test groupings, cycle times, and strobe settings, and checks created test files against restrictions.

Fujitsu designs are also supported by several high-performance third party CAE tools. These include:

- Verilog-XL<sup>®</sup> (Gateway Design Automation) mixed-mode system simulator
- LASAR Version 6 (Teradyne) design simulator and test program generator with fault simulation
- HILO-3<sup>®</sup> (GenRad) design verification, fault simulation, and test generation tools
- IKOS® 800 logic validation hardware accelerator
- Synopsys Design Compiler interactive behavioral/logic synthesizer

Figure 3–2 shows a flowchart of the generic workstation-based design process. Because the function and file names used by each different CAE system may differ, generalized names for each operation are used rather than system-specific names in the following list of steps.

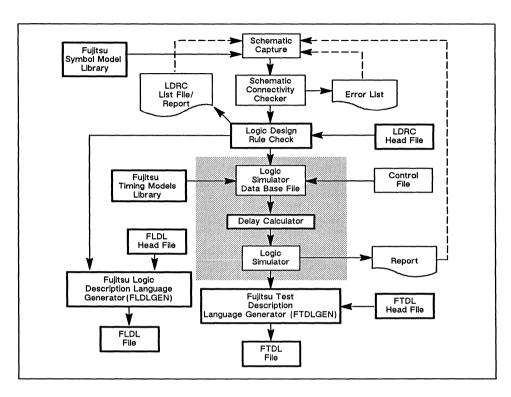


Figure 3-2. Generic Workstation Design Flow

#### 3.3.1 Schematic Capture

Logic circuit entry (schematic capture) is the first step in the generic design automation process. The designer uses the drawing editor program of the applicable workstation software and Fujitsu-supplied symbol model libraries for schematic capture. In most of the Fujitsu-compatible CAE applications, as in ViewCAD, circuits can be defined as macros, for use as sub-parts of other circuits.

## 3.3.2 Schematic Connectivity Checker/Page Compiler.

After the schematic has been entered, it is scrutinized for violation of design rules by the connectivity checking program of the applicable software. The connectivity check produces a list file of the schematic and an error report. The error report lists common violations of design rules of the technology being used, such as unit cells having unconnected inputs and/or outputs, unnamed signals, and signals having multiple names. Errors detected at this level can be easily corrected by going back into the schematic drawing editor program in which schematic capture was performed.

## 3.3.3 Logic Design Rule Check

The Logic Design Rule Check (LDRC) module is Fujitsu software, written specifically for each technology to check gate array designs. This program is run before simulation because it catches

errors that, undetected under normal workstation design rules, often cannot be tolerated in a Fujitsu gate array. Even a seemingly small design flaw undetected prior to simulation may be severe enough to invalidate the functional simulation of the design and any test signal data that may be generated from as a result. LDRC checks that the design conforms to the logic design rules applicable to all Fujitsu designs, to those unique to a technology and to those required by the chosen package type. When hierarchy is used, LDRC checks for hierarchy violations.

In order to tailor the LDRC to a particular technology, device, and package, the customer enters required information via an LDRC Head File, which supplies the device and package name and sets the LDRC to output information in the form of a report either on all nets or on only nets that contain errors.

#### LDRC Report

When the LDRC is finished running, it produces a report containing the following information:

- (a) errors, alarms, and warnings of detected violations
- (b) chip information such as:
  - number of basic cells used vs. cells available number of unit cells and of different unit cell types total number of unit cell terminals vs. number of connected unit cell terminals total number of nets total number of external input, output, and bus terminals package name signal pins used and maximum number of signal pins available
- (c) loading unit check list (a list of the load units associated with each input and output signal)

Errors detected during LDRC can now be corrected before the Logic Simulation Program is run.

## 3.3.4 Logic Simulation

The steps that make up the logic simulation process vary between workstations. For some workstations, logic simulation is all one step (see the shaded box in Figure 3-2), while for others it is three separate steps:

- (a) logic simulator data base file compilation
- (b) delay calculation
- (c) logic simulation

#### Logic Simulator Data Base File

The logic simulator data base file uses a Fujitsu-supplied library to apply behavioral characteristics such as component functions, delay parameters, loading factors, and minimum pulse width, set-up time, and hold time for flip-flops. These values are supplied by the Fujitsu libraries for the appropriate technology. Input stimulus to the circuit is supplied by the designer in the form of the Control File.

#### **Delay Calculator**

Fujitsu provides the program for performing the delay timing calculations. The execution of the program calculates the delay times unique to each net in accordance with the loading condition

(fan-out and hierarchy) in the schematic data file. These calculated delays are representative of pre-layout loading conditions.

The calculations for metal loading are based on the same look-up tables and load equations used in the Design Manual. These loads are subject to change after layout, reflecting the actual metal loads experienced.

#### Logic Simulator

The event-driven logic simulator evaluates the outputs of each gate as a function of its inputs and displays the results as either a waveform drawing or as a data file. Workstation simulations performed under the influence of the Delay Calculator are vitally important to verification of design functionality and to the creation of successful test vectors. Using in-circuit application stimulus from the Logic Simulator Data Base File, simulations are executed in minimum, nominal, and maximum modes, with timing checks enabled, to ensure that the design is responding as expected and is stable under all conditions. The results are written to a print-on-change file, which is a list of the signals that changed state, their new state, and the time at which they changed.

## 3.3.5 FLDL Generator

Any errors found by the logic simulation process can be corrected at this point before Fujitsu's Logic Design Language generator (FLDLGEN) program is run on the schematic data file to create the FLDL file. The purpose of the FLDL file is to provide information to the host mainframe for automatic layout and logic simulation. An FLDL head file must be created by the customer containing the customer's name, the workstation type, the revision, the date, and the designer. The FLDLGEN program receives input from the FLDL Head File and the schematic data base file created at schematic capture and amended if necessary according to the results of the LDRC and Logic Simulation. The FLDLGEN program can then create a Logic Description (FLDL) file that describes the customer's design for the mainframe software.

## 3.3.6 FTDL Generator

The FTDL Generator (FTDLGEN) is a conversion program that translates the Logic Simulator's output file into Fujitsu's Test Description Language. In the process of doing this, it applies Fujitsu tester restrictions to the simulator results. If any signal or timing violations are detected, the operator is informed so that the necessary changes can be made to the data file. The final output file of the FTDL Generator becomes the FTDL File, that is, the test vectors for the mainframe simulator as well as for the LSI tester.

## 3.4 Post-Design Process

At this point, the customer has gone as far as possible in designing a CMOS gate array on a CAE workstation. Now the design is transferred to the mainframe environment at one of the Technical Resource Centers for mainframe simulation on a Fujitsu M780 35 mips computer. This process is described in more detail in Chapter 6.

## Chapter 4 - Design Considerations

#### Contents of This Chapter

- 4.1 Introduction
- 4.2 Logic Design Considerations
- 4.3 Designing for Reliability and Testability
- 4.4 Designing for Speed
- 4.5 Bus Circuit Design
- 4.6 I/O Design
- 4.7 Designing for Scan Test Technology

#### 4.1 Introduction

This section of the data book gives an overview of the logic and I/O design considerations that must be kept in mind to implement a successful design is one of Fujitsu's CMOS technologies. Specific design recommendations for each technology can be found in the Design Manual for that technology.

## 4.2 Logic Design Considerations

In order to benefit from fully automated layout, a designer may use no more than 90% of the actual cell count of an AV or UHB gate array. The actual cell count is the number of basic cells used in the device. It is important to note, however, that this percentage may vary with device type as well as technology.

In Fujitsu's channeled CMOS technologies, the unit cells are grouped in single or double columns alternating with wiring channels. Within the columnar architectures, unit cells are always constructed on one single or double column, i.e., a unit cell cannot bridge the wiring channel between two basic cell columns. This limits the number and complexity of unit cells that can be placed on a double or single column.

The number of inputs and outputs and therefore input and output buffers required also limit the number of basic cells available for logic design in most technologies.

#### 4.3 Designing for Reliability and Testability

The following considerations must be made to ensure maximum testability and therefore reliability of a design:

- (a) External signal paths must be interfaced to the array by an I/O buffer.
- (b) The outputs of a unit cell other than 3-state bus macros may not be wire-ANDed. Generally, if output functions must be tied together, they must be combined through a logic function.
- (c) Only one I/O buffer cell can be connected to an external terminal.
- (d) Inputs to the same cell may not be tied together.
- (e) Unused inputs must be tied high or low, never left floating.

- (f) At least one output of a unit cell must be connected.
- (g) Functions such as one-shots and other monostable or astable circuits cannot be incorporated into a Fujitsu CMOS gate array. All logic state changes detected at the output of the array must be predictable for the purpose of test, and as such, be the direct result of changes of input stimulus. Series inverters must not be used for the purpose of creating a delay.
- (h) Circuits incorporating sequential devices (for instance, flip-flops, counters, shift registers, and so on) must have a traceable method of initialization designed into the circuit, independent of feedback loops.
- (i) No logic function should be incorporated within the array if it cannot be directly or indirectly set or initialized from a primary input.

Designers have two choices for initialization:

- (1) Supply an external signal (for CLEAR, LOAD, etc.).
- (2) Supply known inputs and allow time for them to propagate through the circuit. If the propagation method is used, UNKNOWN ("X" state) must be an acceptable output state until the initialization is completed.

#### 4.4 Designing for Speed

In general, signal delays are caused by the signal having to travel through more gates or over longer distances, especially to enter a different block in gate arrays having block architecture (partitioned arrays). Delay is proportional to length of interconnection metal along which the signal must travel. The following recommendations are therefore made to optimize overall design speed by minimizing the interconnect metal length.

#### 4.4.1 Interblock Connections

Devices that are not physically partitioned do not allow the designer to control relative path lengths. It is highly recommended, therefore, to design hierarchically, dividing the cell into blocks and the blocks into sub-blocks so that functional groups of unit cells are laid out in close proximity and signals have less far to travel. When it becomes necessary to link blocks, the use of high-power "high-drive" unit cells is recommended to drive signals in the inter-block metal.

## 4.4.2 Clock Line Design

A clock network is a circuit used for the efficient distribution of an external clock input to internal sequential and combinatorial unit cells clock. Clock skew is the differential delay of a clock signal as it proceeds through a system; it is determined by the types and relative positions of the gates and blocks within the array. Clock networks must be optimized to minimize skews for both internal and inter-chip clock distribution to assure high-speed operation.

Optimization of clock networks is made possible by using dedicated input buffers called clock input buffers and dedicated unit cells called clock distribution buffers.

Clocks must enter the array through the clock input buffers. They should be further distributed via the clock distribution buffers. Proper use of clock buffers to boost signal strength and balance loads reduces the problems of clock skew and clock pulse variation. The locations of clock input buffers for signals with frequencies greater than 5 MHz are limited to paths on two sides of the die; the number of such buffers is limited depending on the CMOS technology used.

External clock signals must be wired in parallel with chips; once inside the chip, clock signals must be wired in parallel with logic blocks.

## 4.4.3 Delay Unit Cells

Fujitsu supplies delay unit cells to assist the designer in solving timing problems such as set-up and hold time requirements. The designer should not, however, use delay cells to construct asynchronous circuits (one-shots or glitch generators).

#### 4.5 Bus Circuit Design

The AV (AV, AVB, AVL, and AVM) Gate Array family has no 3-state buses internal to the array. As a result, busing is accomplished through one-way multiplex networks. The UHB technology has special provisions for implementing high-performance internal 3-state buses. The internal 3-state bus can be implemented on the chip using bus driver cells and bus terminators, which maintain the last logic level on each bus line when all bus drivers switch to their high impedance state. The bus terminator maintains this logic level until any bus driver begins to drive the bus line. The bus terminator is invisible to a logic designer; it will be connected to each of the bus lines automatically by the mainframe CAD system. It uses only one basic cell per bus line.

The number of internal 3-state buses permitted depends on the technology and on the size of the gate array and the bus width (number of bits per bus) required.

## 4.6 I/O Design

#### 4.6.1 Pin Assignment Guidelines

The following parameters apply to the assignment of I/O pins:

- (a) All Vss pins must be tied to ground.
- (b) All VDD pins must be tied to 5 volts.
- (c) Voltage and ground pins are predetermined by the package type and cannot be altered.
- (d) Pins designated "No Connection" cannot be used.
- (e) Additional Vss and VDD pins may not be assigned by the designer without first negotiating this deviation with Fuiltsu.
- (f) Fujitsu recommends that the designer assign the pin numbers to the circuit in the \*ASSIGN or \*OPTION section of FLDL or submit the complete pin assignment table with the design. It is also possible to allow the Technical Resource Center to do the assignment automatically on the mainframe or manually from a customer-supplied form.

#### 4.6.2 Simultaneously Switching Outputs (SSOs)

Outputs are defined as switching simultaneously when they switch from a logic low (or a high impedance state) to a logic high or switch from a logic high (or high impedance state) to a logic low within 20 nanoseconds of each other.

When a number of outputs switch from high to low simultaneously, a problem condition may arise when the ground potential is momentarily pulled up from 0 volts to a more positive level. This momentary tug on ground can appear as noise spikes or ringing. It is possible, with insufficient Vss pins, for the ground plane to be pulled up to a point where the threshold limit for VIH is violated.

When the ground level is raised by the noise, the input threshold (VIH) of the gates is also raised, relatively, for the duration of the impulse, as illustrated in Figure 4-1. This could cause logic high outputs close to the VIH (minimum) threshold to momentarily change to logic low.

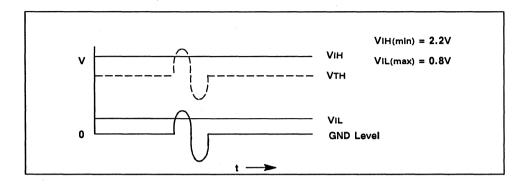


Figure 4-1. SSO-Generated Noise

The intensity of the effect of SSOs is determined by:

the number of SSOs the density and distribution of SSOs in the package the size of the load (capacitance) being driven

To prevent their interference with the signals on other outputs, SSOs must be grouped around ground pins. The number of SSOs allowed in a package is restricted by the number of ground pins available, their location on the package, and the drive capability of the output buffers.

Different CMOS technologies have different rules and guidelines regarding number of SSOs per ground pin. A general rule is to use one ground pin for each group of ten simultaneously switching low power outputs or 30 non-simultaneous outputs. For example, in a package with two Vss pins, a maximum of 20 low power outputs may switch simultaneously.

Asynchronous inputs such as clock, clear, and preset should be physically isolated from SSOs. It is better to place these inputs near a ground pin (if one is available) away from the SSOs. Asynchronous inputs should not be placed on the corners of the packages, especially when the chip is packaged in DIP. Corner DIP pins have the longest lead lengths and therefore the greatest inductance. Outputs to be used as clock, preset, and clear for other devices should be similarly physically isolated. In partitioned chips, pins should be grouped by internal blocks to keep internal interconnect wiring as short as possible.

#### 4.6.3 Test Pins

To facilitate testing, external pins should be provided whenever conditions warrant. The addition of supplementary test pins often allows the reduction of the overall test complexity for a circuit, thus reducing the number of test patterns required and the time necessary to determine functionality of the circuit.

## 4.7 Designing for Scan Test Technology

Scan testing is a special technique that supplements the customer's submitted test patterns to achieve greater fault coverage, thus assuring both Fujitsu and the customer of a highly reliable gate array. Scan testing is implemented by constructing a circuit that allows Fujitsu ATG (automatic test generation) software to automatically generate the scan test patterns (both applied input stimulus and expected outputs). Scan testing is optional and is offered by Fujitsu for the partitioned arrays of the UHB technology.

The unit cells in a device designed for scan testing are arbitrarily connected by the designer to form an enormous shift register. This shift register can contain up to 3000 stages and is formed by connecting the Q-output of one state to the dedicated scan input (SI) of the next. To implement scan testing, designers use special scan-compatible unit cells for all sequential logic functions. With the use of the serial scan method, the difficult problem of testing a logic circuit containing both combinatorial and sequential logic is simplified to testing combinatorial logic and a shift register.

The scan chain can be considered a data carrier with the ability to carry test input stimulus deep into the design and to apply it to the unit cell(s) under test. Once a unit cell has been tested, its output (test result) may, if necessary, be stored in the scan data chain and be carried out of the design for comparison to that which was expected. To the designer, scan unit cells perform exactly the same as non-scan cells, the only difference being the provision of additional basic cells to facilitate the scan test.

#### 4.7.1 Scan Test Modes

Scan testing consists of two modes of operation: SISO (Scan Input/Scan Output test) mode and TC (Test Clock) mode. Sequential logic is primarily addressed by SISO and combinatorial logic is addressed by TC; the two modes are alternated during the scan test.

## 4.7.2 Scan Test Signals

Scan test implementation requires the assignment of up to seven dedicated package pins, six of which are in predefined package locations:

XACK - for the SISO A-clock signal

BCK - for the SISO B-clock signal

XSM - for the SISO mode signal

XTCK - for the TC mode clock signal

SDI – for the serial data input to the first device of the scan path from outside the chip. This is the only one of the scan pins that can serve a dual purpose. It may also be used as a principal input during regular operation.

- SDO for the serial data output from the last device of the scan-configured shift register to the "outside world." The location of the SDO pin is not fixed, and may be placed by the designer at any convenient location.
- XTST for the scan test signal. XTST is used only if the isolation of asynchronous functions or non-scan cells is required during scan testing. If no circuit isolation is required, then XTST is not required and is not provided for.
- XMM for the signal that sets up the compiled cell for test. The pin location of XMM is user defined. This pin is used only in AU series channel-less gate arrays and provided only if compiled cells (RAM or ROM) are a part of the design.
- XTWE for data to be written into RAM in the TC mode. The pin location of XTWE is user defined. This pin is used only in AU series channel-less gate arrays and provided only if RAM cells are a part of the design.

To implement scan path testing in a device, a designer must use specially designed scan components for all sequential (storage) functions such as flip-flops, latches, and shift registers. The scan test feature cannot be implemented for a gate array employing any non-scan sequential unit cell in any portion of the design, with the exception of certain test mode data latches described for each technology in the appropriate Design Manual. Non-scan sequential functions constructed with combinatorial logic (e.g., NAND-gate flip-flops, NOR-gate flip-flops, etc.) are permitted. If, however, non-scan sequential functions constructed with combinatorial logic are used, then the customer-generated function test will be the only means to exercise the nodes in the associated circuits.

# **Chapter 5 – Delay Estimation Principles**

## Contents of This Chapter

- 5.1 Introduction
- 5.2 Choosing Critical Paths
- 5.3 Load Units and Loading Guidelines
- 5.4 The Delay Equation
- 5.5 Estimating Gate Delay
- 5.6 Estimating Total Circuit Delay
- 5.7 Delay Calculations when Load Exceeds CDR
- 5.8 Delay Calculations and the Operating Environment
- 5.9 Clock Loading

#### 5.1 Introduction

This section of the data book gives an overview of the engineering considerations important to the design of an ASIC using Fujitsu's CMOS technologies. Included are the loading rules for CMOS gate arrays and a demonstration of how to estimate the delay through a circuit. In addition to the basic delay equation, this chapter also considers the loading limitations for clock signals and the effects of the operating environment on typical delay figures.

## 5.2 Choosing Critical Paths

A critical path is a logic path whose timing requirements must be satisfied to ensure proper system function. In an ordinary synchronous circuit, data propagates from one register through combinatorial logic into another register. For the circuit to function properly, the sum of the clock-to-Q delay of the source register, the propagation delay through the logic, and the set-up time on the target register must be less than the worst-case system clock period. Correct timing of the signal along the critical path guarantees that this condition is met.

Usually, the critical path is the one with the greatest number of gate levels. However, if such a path is speeded up by redesign, another, less complex path may become the new critical path.

For example, in a design in which a path has eight levels of gating, the designer may determine upon inspection that two groups of NAND-NAND structures can be changed to AND-OR inverters, an efficient CMOS implementation that noticeably increases the speed of the path. In this case, after applying DeMorgan's theorem and reducing the result, the designer finds that another path is now the critical path.

Since each logic state sensitizes different branches, logic paths must be analyzed using the inputs (rising or falling) that will actually be applied to them (since rising and falling delays are not equal) to determine the longest path that will be sensitized and ensure that it meets critical path requirements.

The path delay calculation worked through in this section shows how a designer can analyze each element of a Fujitsu CMOS circuit to make sure the design meets critical path requirements. In this case, the effect of a rising input on the sample circuit is calculated as it would be if this were a critical path and the rising input were forcing the transition of interest.

#### 5.3 Load Units and Loading Guidelines

The Fujitsu CMOS load unit (lu) is the input capacitance of an inverter used as the basic unit for measurement and calculation of capacitive loads presented to unit cells within the gate array. Both the output drive factor of a unit cell and its input load factor are defined in terms of load units. Both factors are listed for each unit cell in the unit cell library for the appropriate technology.

#### 5.3.1 Output Drive Factor

The output drive factor (CDR) is a parameter expressing the load driving capability of a unit cell. Unit cells can drive loads greater than the output drive factor. The performance of CMOS circuits degrades exponentially with increased loading; if too great a load is driven, an exaggerated increase in delay through the unit cell may be experienced.

It is permissible for the load to exceed CDR if the associated additional delays are anticipated and tolerable. Additional calculation factors are required to estimate delays of loads greater than CDR. Figure 5–1 indicates the delays that may be generated when the load exceeds these guidelines.

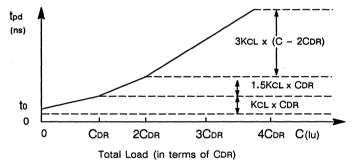


Figure 5-1. Delay Time vs. Loading Factor

## 5.3.2 Input Load Factor

The input load factor of a unit cell is used to estimate the propagation delay of a critical path in a design. The total propagation delay of a path is defined as the sum of the delay factor of each of the unit cells in the path.

## 5.3.3 Delay Factor

The delay factor of each unit cell is made up of two types of capacitive loading:

- (a) Load capacitance inherent in the input of each cell (the input loading factor)
- (b) Load capacitance due to the metal interconnection of unit cells (CL)

The total load (C) presented by a unit cell is estimated by adding the total cell input load or NF/O (the input loading factors of all other cells connected to the output network of the cell in question) to the total metal load (CL),

or C = NF/O + CL

## 5.4 The Delay Equation

The basic delay equation combines the AC parameters of a cell and its associated capacitive loads to estimate the delay time through the cell. The rise and fall time of a unit cell may not be

symmetrical due to differences in the transconductivity of the N and P transistors as well as to differences in the arrangement of the transistors to form unit cells. The same equation is used with different variables for positive-going and negative-going signals at the unit cell output. These signal polarity variables must be considered separately.

tup = t0up + KCLup(NF/O + CL)

tdn = t0dn + KCLdn(NF/O + CL)

#### where:

t0xx is the circuit delay through the unit cell under no-load conditions (a value given in ns for each cell in the unit cell library).

KCLxx is the load derating constant or delay time per loading unit conversion factor (ns/pF) defined for each unit cell.

NF/O is the sum total of the input loads of all unit cells driven on the net (expressed in load units).

CL is the amount of loading, in load units, on the unit cell output due to interconnect metal (metal load).

The term "net" refers to the network of metal wiring connecting all the unit cells driven by a specified unit cell. Interconnect metal refers to the metal wiring, also called routing metal, that makes up each net.

#### 5.5 Estimating Gate Delay

Figure 5-2 shows a sample circuit for the purposes of demonstrating how the total accumulated delay (tpd) through a short path is estimated.

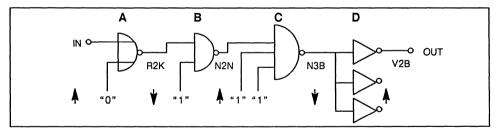


Figure 5-2. Delay Path Sample Circuit

Ordinarily a designer looks up the the specifications of each unit cell in the unit cell library of the applicable technology. For this example, however, all of the necessary specifications have been assembled in Table 5-1, using the values for UHB technology.

Table 5-1. AC Parameters of Unit Cells

Cell	Cell	Basic	Input	Output	Propagation Delay Time				
Function	Name	Cells	Load	Drive	tı	1b	tdn		
		Used	Factor	Factor	to	KCL	to	KcL	
2-Input NOR	R2K*	2	2	36	0.45	0.14	0.45	0.06	
2-Input NAND	N2N	1	1	18	0.37	0.16	0.56	0.14	
3-Input NAND	N3B*	3	1	36	1.28	0.08	1.70	0.04	
Inverter	V2B	1	2	36	0.25	0.08	0.25	0.05	

<sup>\*</sup> These are high drive cells that operate faster than their low drive equivalents under these circumstances.

The delays for rising (tup) and falling (tdn) edges of a pulse can differ widely. Digital pulses are either lengthened or shortened while passing through a unit cell. It is therefore important to calculate the pulse width variations along the entire signal path to verify that pulse width is sufficient to pass through each gate.

In the example that follows, based on Figure 5-2, calculations are based on a rising pulse entering the input of unit cell A and changing state several times as it proceeds through the sample circuit. To find the total delay for the circuit, it would be necessary to calculate the values resulting from the opposite case, in which a falling pulse enters the circuit at unit cell A.

## 5.5.1 Delay Parameter for Rising Edge (tup)

The unit cell library shows that the delay time (t0) for an upward transitioning signal at the unit cell output (tup) for R2K, a 2-input NOR, is 0.45. It shows that the load/delay conversion factor for an upward transitioning signal (KCLup) for R2K is 0.14.

#### 5.5.2 Number of Fan-outs (NF/O)

The sample schematic in Figure 5-2 shows that the NF/O, the number of cells that the R2K must drive, is one (an N2N). The unit cell library shows that the N2N has an input load factor of 1 lu.

## 5.5.3 Number of Driven Inputs (NDI) and Metal Load (CL)

The value for CL is based on the number of inputs the cell in question must drive and is derived from the Estimation Tables for Metal Loading at the beginning of the unit cell library. Table 5–2 is a sample metal load table; each technology and device has unique load/delay characteristics. Since the number of driven inputs (or NDI) for R2K, N2N, and V2B in Figure 5–2 is one, the amount of loading due to metalization (L) is 1.0 lu. The NDI for N3B in Figure 5–2 is three; therefore the CL is 3.0.

Table 5-2. NDI vs. CL\*

NDI	CL (lu)
1	1.0
2	2.2
3	3.0
4	3.5
5	3.9
6	4.2
7	4.6
8	4.8
9	4.9
10	5.0

The value given for CL in the Estimation Tables for Metal Loading is an estimate of the loading effect of the metalization capacitance on the output based on Fujitsu's careful statistical analysis of typical designs. Actual metal loading is based on the effect of the routing and therefore may vary from these estimates. To compensate for this uncertainty, Fujitsu incorporates a  $\pm$  5% variation into the prelayout delay multipliers. After routing, another set of simulations is run to verify the effect of the actual metal routing.

NOTE: In an array partitioned into blocks, if the interconnected unit cells are located in different blocks, the loading is greatly increased. The designer can avoid this worst-case situation by using the hierarchical approach during the schematic capture process to confine circuits to one block whenever path delay is critical.

#### 5.6 Estimating Total Circuit Delay

Based on the values from Tables 5-1 and 5-2, the propagation delay for R2K in the sample circuit is:

The propagation delay for N2N, found by following the same procedure, is:

```
tup (B) = t0up + KCLup (NF/O + CL)

tup = 0.37 + 0.16 (1 +1.0)

tup = 0.37 + 0.16 (2.0)

tup = 0.37 + 0.32

tup = 0.69

tup (B) = 0.7 (rounded up to the next 0.1 ns)
```

The propagation delay for N3B, found by following the same procedure, is:

<sup>\*</sup> For a 330UHB gate array.

The propagation delay for V2B, found by following the same procedure, is:

```
tup (D) = toup + KCLup(NF/O + CL)

tup = 0.25 + 0.08 (1 +1.0)

tup = 0.25 + 0.08 (2.0)

tup = 0.25 + 0.16

tup = 0.41

tup (D) = 0.5 (rounded up to the next 0.1 ns)
```

Therefore, the total delay for the sample circuit shown in Figure 5-2 is:

```
tpd = tdn (A) + tup (B) + tdn (C) + tup (D)

tpd = 0.6 + 0.7 + 2.0 + 0.5

tpd = 3.8 ns
```

## 5.7 Delay Calculations when Loads Exceed CDR

Fujitsu CMOS gate arrays are capable of driving loads beyond their published Output Drive Factor (CDR). It must be emphasized, however, that the delays that result from this practice are considerably increased. Unit cells may be loaded beyond their CDRs provided that the increased delay is acceptable.

Anticipation of the effects of loading beyond the published CDR requires recalculation of delay. Different delay equations must be used depending on the technology being used and the amount that the loading exceeds CDR.

The general formula for loading beyond CDR are listed below; different delay equations must be used depending on the degree that the loading exceeds CDR.

NOTE: All degrees of loading shown below are not necessarily permitted in all technologies and certain technologies may further modify the equations to reflect different characteristics.

```
When C is CDR or less:

tpd = t0 + (KCL x C) where C = NF/O + CL

When C is between CDR and 2CDR:

tpd = t0 + (KCL x CDR) + 1.5 KCL(C - CDR)

When C is between 2CDR and 4CDR:

tpd = t0 + (KCL x CDR) + 1.5 (KCL x CDR) + 3KCL(C - 2CDR)

When C is greater than 4CDR:

FORBIDDEN
```

NOTE: Clock networks are never loaded beyond CDR because clock timing is critical to the proper functioning of the gate array. (See Section 5.9)

#### 5.8 Delay Calculations and the Operating Environment

The operating environment of the array can cause variations from the calculated typical delay figures. Influencing factors include ambient temperature, applied voltage, and variations in the manufacturing processes. Figure 5–3 shows how supply voltage and temperature affect the performance of a sample array. It is necessary, therefore, to simulate worst-case conditions during test. Revised estimates of delay under these harsher circumstances may be arrived at by multiplying the typical delay figures by delay multipliers when temperature or supply voltage varies beyond the operating condition specifications published for each technology. The actual multipliers used depend on the device technology and/or the device type.

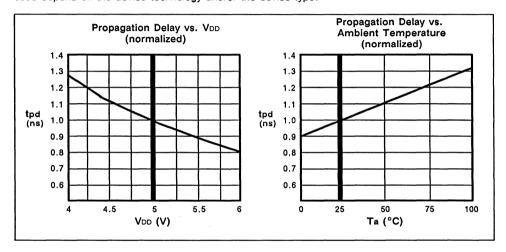


Figure 5-3. Factors Influencing Delay

#### 5.8.1 Minimum/Maximum Delay Multipliers

The minimum delay multiplier and the maximum delay multiplier for typical Fujitsu CMOS technologies given below incorporate process, power supply, and temperature variation.

	Minimum Delay	Maximum Delay		
	Multiplier (0° C, 2.5V)	Multiplier (70° C, 4.75V)		
UHB Technology	0.35	1.65		
AV Technology	0.45	1.60		

These delay multipliers are applied in one of two different ways, depending upon whether they are to be used for the optional delay test calculations or for the other tests performed on the mainframe using the information in the FTDL (Fujitsu Test Description Language) file, such as DC test, function test, or high impedance test. More information on the testing process is included in the following section, Chapter 6.

## 5.8.2 Delay Calculations for Delay Test (AC Test)

The min/max delays for the delay test are determined by taking the sum of the typical delays and multiplying it by the appropriate minimum or maximum delay factor. The maximum delay figure

must be rounded up to the next highest 0.1 ns, while the minimum delay figure must be rounded down to the next lowest 0.1 ns. The result of the equation shown for delay calculation is repeated here and also shown in its modified form. The delay factors used are those for UHB technology.

Typical delay:

tpd = 
$$0.6 + 0.7 + 2.0 + 0.5 = 3.8$$
 ns  
Maximum delay (rounded up to 0.1 ns):  
tpd =  $(0.6 + 0.7 + 2.0 + 0.5) \times 1.65 = 6.27 = 6.3$  ns  
Minimum delay (rounded down to 0.1 ns):  
tpd =  $(0.6 + 0.7 + 2.0 + 0.5) \times 0.35 = 1.33 = 1.3$  ns

## 5.8.3 Delay Calculations for DC Test, Function Test, and High Impedance Test

The minimum and maximum delays for these tests are determined by multiplying the typical delays for each cell individually by the delay factors. The resulting figures for both maximum and minimum delays are rounded up to the next 0.1 ns for each cell. The final figures for each unit cell of the path are totaled. The delay calculation used earlier is repeated here and is also shown calculated for the DC, Function and High Impedance tests. The delay factors used are those for UHB technology.

Typical delay (rounded up to 0.1 ns):

$$tpd = 0.6 + 0.7 + 2.0 + 0.5 = 3.8 \text{ ns}$$

Maximum delay (delay for each gate rounded up to the next 0.1 ns):

tpd = 
$$(0.6 \times 1.65) + (0.7 \times 1.65) + (2.0 \times 1.65) + (0.5 \times 1.65) =$$
  
 $0.99 + 1.155 + 3.3 + 0.825 =$   
 $1.0 + 1.2 + 3.3 + 0.9 = 6.4$  ns

Minimum delay (delay for each gate rounded up to the next 0.1 ns):

tpd = 
$$(0.6 \times 0.35) + (0.7 \times 0.35) + (2.0 \times 0.35) + (0.5 \times 0.35) =$$
  
 $0.21 + 0.245 + 0.7 + 0.175 =$   
 $0.3 + 0.3 + 0.7 + 0.2 = 1.5$  ns

Minimum/maximum delays are also calculated this way for minimum clock pulse width, minimum data set-up time, minimum data hold time, preset timing, and clear timing. The values of the maximum and minimum delay multipliers shown above apply to pre-layout calculations only; different factors, specific to each technology, are used for post-layout analysis.

## 5.9 Clock Loading

It is acceptable, though not a recommended design practice, to load the output of a unit cell that does not carry a clock signal beyond its Output Drive Factor (CDR). To ensure maximum clock accuracy, however, unit cells that output clock signals must never be loaded beyond CDR. These different loading limitations for clock and non-clock unit cells can lead to "race conditions," in which the clock signal arrives at a flip-flop before the data signal set-up time has elapsed. It is therefore most important, when loading a unit cell beyond CDR, to modify the fundamental delay equation using the extra delay factors explained in Section 5.7.

# Chapter 6 - Simulation and Test

## Contents of This Chapter

- 6.1 Introduction
- 6.2 Post-Design Simulation and Test
- 6.3 Engineering Sample Testing
- 6.4 ATG Testing and Scan Design

## 6.1 Introduction

This section of the data book explains the simulation and testing processes performed by Fujitsu after the customer completes the CMOS gate array design process on a CAE workstation. These simulation and test processes are carried out using the Fujitsu mainframe software at a Technical Resource Center. Simulation and testing ensure that the data collected in the FLDL (Fujitsu Logic Design Language) file and the FTDL (Fujitsu Test Design Language) file result in an error-free layout and a successful ASIC design. Figure 6–1 describes the post-design process in flowchart form.

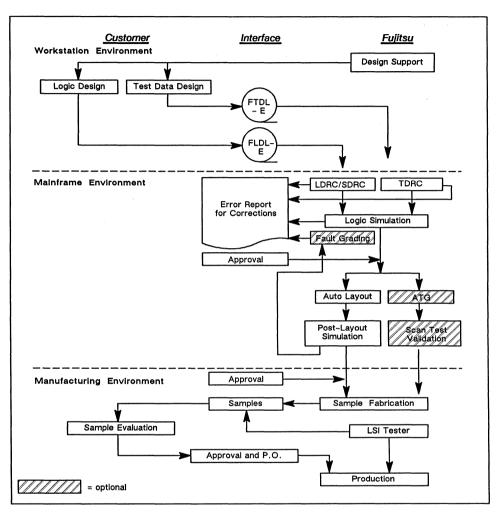


Figure 6-1. Post-Workstation Design Process

## 6.2 Post-Design Simulation and Test

## 6.2.1 LDRC and TDRC

The FLDL and FTDL files are provided to a Technical Resource Center usually in the form of magnetic tape or floppy disk. On the mainframe, the FLDL is checked by the mainframe's Logic Design Rule Check (LDRC) to confirm the validity of the logic data and for formatting errors, unconnected inputs and outputs, loading conditions, etc. The FTDL file is checked by a similar mainframe program called the Test Data Rule Check (TDRC), which flags any violations of the published test data restrictions.

#### 6.2.2 Pre-layout Simulation

After the LDRC and TDRC have been run successfully on the FLDL and FTDL, the mainframe pre-layout simulation can be performed. This is a logic simulation run at nominal, minimum, and maximum propagation delay times using estimated metalization capacitance values. If there is no discrepancy between simulation results and the expected outputs, the design is presumed to be correct. One of two simulators, LBS6 or ViewCAD, runs functional simulations and timing verification including the checking of set-up and hold time, pulse width, and removal times.

#### 6.2.3 Automatic Layout

After a successful pre-layout simulation has taken place and customer approval has been obtained, a proprietary Fujitsu mainframe application performs automatic placement and metal interconnection routing.

## 6.2.4 Fault Grading

After pre-layout simulation is completed, customers have the option of requesting that Fujitsu subject the test data to a process called "fault grading." This CPU-intensive process analyzes the customer's circuit and test data to calculate the percentage of fault coverage. The input test data is analyzed to determine the adequacy of the stimulus patterns to detect any "stuck" (malfunctioning) nodes. The result, a report of all nodes not tested by the stimulus provided, is given to the customer. The customer then has the option of either changing the test vectors or acknowledging that the untested nodes are acceptable.

#### 6.2. 5 Post-Layout Simulation

Post-layout simulation, also known as final validation, is again performed at nominal, minimum, and maximum propagation delay times, but using actual calculated capacitance based on the metal interconnection routing resulting from automatic layout.

#### 6.2.6 Sample Fabrication

After a successful post-layout fabrication has been performed and customer approval has again been obtained, engineering samples of the array are fabricated for customer evaluation.

## 6.3 Engineering Sample Testing

### 6.3.1 LSI Tester

Once sample chips have been fabricated, they are tested on the LSI Tester, a test instrument located at the manufacturing facility. Sample chips are tested with input test patterns and expected outputs obtained from the FTDL file.

One of the most important tasks of post-layout simulation is to validate the test vectors for later use on the LSI Tester. For this reason, simulation is executed under conditions adhering as closely as possible to the conditions imposed by the tester. A device that passes all phases of simulation is likely to pass the LSI tester.

The limitations of the LSI Tester places various restrictions upon test data. These restrictions must be respected when preparing the test data pattern and when creating the (stimulus) Control file for running workstation simulations.

A "Summary of Test Data Restrictions" is published for each CMOS Gate Array technology and is included in the design manual for the specific technology.

Test data restrictions involve such issues at the numbers of test patterns acceptable for each test type, the minimum test cycle length, input signal timing, output strobe timing, bidirectional buffer simulation, input and output cycle timing, tester skew, and the treatment of data signals.

Tests performed on the LSI Tester include the function test, the delay test, the DC test, and the high impedance ("Z function") test. Specific data (given in the Design Manual for each technology) must be included in FTDL to perform each of these tests.

#### 6.3.2 Function Test

The function test guarantees the designed function of the gate array by exercising as many of the internal nodes as possible and detecting functional failures. Fujitsu requires the function test because it is the primary means of determining if an ASIC is functioning properly as it comes from manufacturing.

In the course of the function test, input signals are applied in accordance with customer timing specifications, using worst-case input voltage at a clock frequency not to exceed 16 MHz (a period of 63 ns). The dynamic performance of this test also partially verifies the AC characteristics of the device.

The function test may be run in multiple units (blocks), allowing changes to be made in the test vectors to assure thorough testing of the device. The transition from one block to the next requires that the device be powered off, adjustments made to the tester and pins regrouped as required. After all changes have been made, the test is restarted.

The test vectors used in the function test originate with the Print on Change file (the output results of the workstation simulation) and the FTDL head file created by the user. The Print on Change file is a list of the signals sampled and a history of the transitions in a given test block with the actual times that the transitions occurred. The FTDL head file adds the parameters needed to qualify the test data in the Print on Change File: definition of the test cycle time, signal delays, pulse types and pulse widths, and output strobes.

#### 6.3.3 Z-Function Test

The Z-Function test is administered in the last block(s) of the function test. Its purpose is limited to the verification of the high-impedance function of 3-state and bidirectional output buffers. The Z-function test is necessary only when there are two or more logic combinations that can generate the high-impedance state for a given I/O cell. The test can verify all these logic combinations. If only one logic combination generates the high-impedance condition, then the DC test is adequate.

## 6.3.4 DC Test

The DC test, as its name implies, verifies the DC characteristics of the array. It is not intended to check circuit functionality, but is can be used as a function test of 3-state circuits having only one signal path that generates the high-impedance condition.

The designer supplies the sequence of input signals and expected outputs in the FTDL. These test patterns must generate every possible output state for every type of output and input buffer being used (high, low, and high-impedance).

The DC test applies the specified inputs to measure the following DC parameters:

- (a) Steady State Power Supply Current (IDDS)
- (b) Output High Voltage (VOH)
- (c) Output Low Voltage (VOL)
- (d) Input Leakage Current (ILI)
- (e) High-Impedance Output Leakage Current (ILZ)

## 6.3.5 Delay Test

The delay test is optional. It is used to verify critical paths or as a means to characterize the device by performing this test on a small number of paths. The purpose of the test is to check that signal paths from various inputs of the chip to their respective outputs meet the customer's standards for minimum and/or maximum delay times. The paths may be sequential and/or combinatorial but only the propagation delay, not the toggle frequency, is measured.

## 6.4 ATG Testing and Scan Design

ATG testing is a special technique that supplements the customer's submitted test patterns (FTDL) to assure both Fujitsu and the customer of a highly reliable gate array by achieving a high degree of fault coverage. ATG testing is implemented by using scan design techniques described in Section 4.7. Scan test patterns (both applied input stimulus and expected outputs) are automatically generated by Fujitsu's Automatic Test Generator (ATG) software. ATG is offered by Fujitsu for partitioned arrays of the UHB technology and for all arrays in the channel-less gate array technologies.

1

# Chapter 7 - Quality and Reliability

## Contents of This Chapter

- 7.1 Introduction
- 7.2 Engineering Testing
- 7.3 In-process Inspection and Quality Control
- 7.4 Reliability Testing
- 7.5 Test Methods and Criteria
- 7.6 Reliability Theory

#### 7.1 Introduction

This section explains Fujitsu's approach to quality and reliability. A single-minded emphasis on quality and a dedication to providing components to meet exacting requirements is the reason Fujitsu integrated circuits are known for their exemplary performance.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. (See Figure 7-1) Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end on the Fujitsu factory floor. It extends to a policy of meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use Fujitsu products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The QC process begins with incoming inspection of all raw materials and ends with shipping tests and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

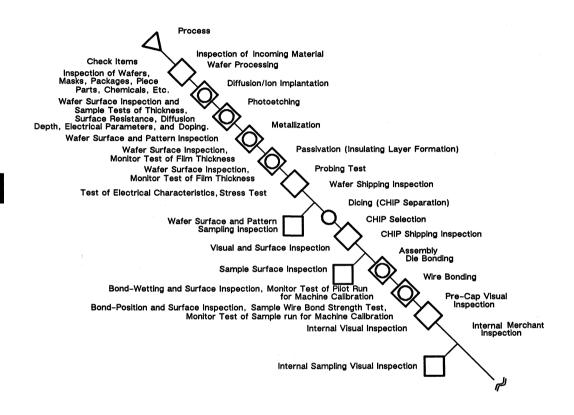


Figure 7-1. Quality Control Flowchart

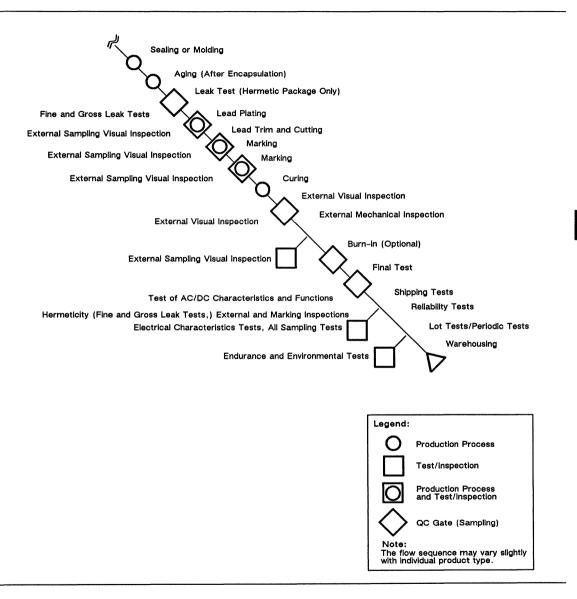


Figure 7-1. Quality Control Flowchart (Continued)

## 7.2 Engineering Testing

Engineering testing is the heart of reliability and quality control. The reliability engineering department plans and performs most engineering testing. Whenever a device is developed, it must undergo engineering approval tests. After the device passes these tests, production engineering approval tests are performed on a representative sample of the device. All factors that could influence production of the device are examined. Only if all conditions are favorable and the device passes thorough testing, can the new device go into production.

Table 7-1 shows a sampling plan for engineering testing. These tests are in compliance with MIL STD 883, Class B, as indicated in Table 7-1a. When a change in production (e.g., a material change) is needed, engineering tests are performed on specific items for the change.

Since the representative samples tested must accurately reflect the reliability of the device, the following conditions must also be satisfied: the functions performed by the same basic circuit; the same processing techniques, materials, parts and packages used; and the same processing followed at the same factory.

Table 7-1a. Sampling Plan for Engineering Testing: Endurance Test

Test items	MIL-STD -883	LTPD* (%)	Acceptance number**	Note
High-temperature storage 150°C	1008 C	7	1	
High-temperature continuous operation 150°C or 125°C	1005 D	7	. 1	
High-temperature continuous operation 125°C	1055 D	5	2	
Low-temperature continuous operation -55°C	(1055 C or D)	7	1	As applicable
High-temperature high-humidity storage 85°C, 85% RH	_	7	1	Plastic package only
High-temperature high-humidity continuous operation 85°C, 85°RH	(1005 C or D)	7	1	Plastic package only

Lot test percent defects

<sup>\*\*</sup> Number of failures permitted per lot

Table 7-1b. Sampling Plan for Engineering Testing: Environmental and Mechanical Test

Test Items	MIL-STD -883	LTPD (%)	Acceptance number	Note
External visual inspection	2009	15	1	Same sample
Physical dimensions	2016	15	1	•
Radiophotography	2012	3 devices	0	
Internal visual inspection	2013	15	0	
Lead integrity: Tension Bending stress Lead fatigue	2004 A B1 B 1	15 15 15 15	0 0 0	Devices which failed in electrical characteristics test are acceptable to this test. Each test is performed on one third of the leads of each sample.
Resistance to soldering heat	_		7	Same sample
Temperature cycling	1010 C	7	1	
Thermal shock	1011 A	7	1	
Vibration, variable-frequency	2007 A	·		
Mechanical shock	2002 B	1 10	1	
Constant acceleration	2001 D	1	·	
Seal: (Fine and gross leak checks)	1014 A1 C	7 7	1 1	Hermetic package only
Resistance to solvents	2015	40 devices	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (260°C)	2003	15	1	Devices which falled in electrical characteristics test are acceptable to this test.
Solderability (230°C)	_	15	1	Devices which falled in electrical characteristics test are acceptable to this test.
Internal water-vapor content	1018	3 devices	0	Hermetic package only
Electrostatic discharge sensitivity	3015 A	15	1	1
Pressure-Temperature-Humidity Storage (PTHS) 121°C, 2 atm.	_	15	1	Plastic package only

The following tests are performed only when required or when requested by the customer.

Table 7-1c. Sampling Plan for Engineering Testing: Optional Environmental Mechanical Test

Test items	MIL-STD -883	LTPD (%)	Acceptance number	Note
Bond strength	2011 D(orC)	15	2 wires	34 wires/4 devices
Die shear strength	2019	3 devices	0	Hermetic package only
Moisture resistance	1004	15	0	
Salt atmosphere (corrosion)	1009 A	15	0	
Vibration fatigue	2005	15	0	
Immersion	1002 B	15	0	
SEM inspection of metalization	2018	3 devices	0	
Particle impact noise detection (PIND) test	2020 B	15	1	Hermetic package only
Lid torque	2024			Frit sealed package only, as applicable
Adhesion of lead finish	2025			As applicable

Table 7-1d. Sampling Plan for Engineering Testing: Continuity Test

Test items	MIL-STD -883	LTPD (%)	Acceptance number	Note
Continuity check	_	5	2	Plastic package only

#### 7.3 In-Process Inspection and Quality Control

Every department involved in the manufacturing process is responsible for the quality-control inspection in its sphere of operation. In-process checks, sampling tests, and other inspections are assigned so that each department has certain allotted tasks for which it takes full responsibility. This total control system has rationalized overall operations dramatically.

## 7.3.1 In-Process Checks (Including screening)

In-process checks are performed after each key step that is critical to the next process in wafer processing and assembly. Defective or substandard products are weeded out at an early stage. Testing falls into three categories:

- (a) Probe testing, chip selection, and final testing. These are defined for each process.
- (b) Voluntary-checks. These include inspection of the wafer surface after window opening (before the diffusion process) and inspection of the wafer surface after the metalization.
- (c) 100% screening. This includes the aging and visual inspection that are performed during wafer processing and assembly.

#### 7.3.2 In-Process Sampling Test

The in-process sampling test is performed as a part of process quality control. The Manufacturing and QC departments check randomly drawn samples at key points in the manufacturing process to check process and facility conditions. This helps in maintaining product quality at the customary high level. The following items are checked in these sampling inspections or monitoring:

(a) Surface resistance after diffusion, film thickness, evaporated or sputtered electrode thickness, and device characteristics.

- (b) Product quality (checked by visual inspection of the chip surface).
- (c) Bonding machine calibration, visual inspection and bond strength after wire bonding, product appearance, marking permanency tests.

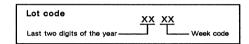
### 7.3.3 In-Process Inspection

The Manufacturing and QC departments perform stringent quality checks between major processes to ensure the highest quality. Four types of inspections are performed:

- (a) Inspection of incoming materials, parts, and chemicals
- (b) Wafer shipping inspection
- (c) Chip shipping inspection
- (d) Shipping test

## 7.3.4 Lot Configuration

A "lot" consists of the same devices produced over a stated period, having the same design and using the same processing techniques, materials, and production line. In addition to the Fujitsu logo, part number and others, each IC is marked with a lot code as shown below.



## 7.4 Reliability Testing

Reliability testing includes three types of tests—lot tests, periodic tests, and "occasional" tests. This section explains the details of each test in turn.

#### 7.4.1 Lot Tests

There are two types of lot tests, called Group A tests and Group B tests. Group A tests and Group B tests are performed on items that are tested regularly, usually every week. Table 7–2 lists the specific lot tests.

Details of individual tests vary with the product under test, but all samples are selected at random from every weekly lot. Tests are not performed in any particular order unless specified, but are performed for each device type.

Note that the high-temperature storage and continuous-operation tests usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. No-good samples and samples that have undergone destructive testing are destroyed.

### 7.4.2 Periodic Tests

Particulars of the periodic tests are also listed in Table 7-2. There are two types of periodic tests: Group C tests and Group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability tests and very long life tests. The Group D tests are usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified, but are performed for each device type. Note that the high-temperature storage and continuous operation tests for Group C take 1000 hours and those for Group D take 3000 hours.

Table 7-2. Sampling Plan for Reliability Testing

0	S	Device c	lassification	De	vice group 1	D	evice group 2	
Group	Subgroup	Test	items	Sampling plan				
	A1	External visual inspection		100% test of sampled devices (All sampled devices				
	A2		Function test		LTPD 5%	Ac=0		
Α	A3	Electrical	Static Characteristics		LTPD 5%	Ac=0		
	A4	Characteristics	Dynamic/Switching characteristics		LTPD 5%	Ac=0		
				Sample size	Acceptance number	Sample size	Acceptance number	
	B1	Physical dimens	sions	9	1	6	1	
	B2	Environmental	Resistance to solvent + Temp-cycling	9	18	9	18	
		tests	Thermal shock test	9	18	9	18	
	B3		Mechanical environmental test	9	1	9	1	
	B4-I	Solderability (2:	30°C, 5s) 1	9	1	3	1	
	B4-II	Solderability (2)	50°C, 5s) 1	9	1	3	1	
В	B5	Lead integrity1		9	1	3	1	
		Pressure-temp storage <sup>2</sup>	erature-humidity	9	13	3	13	
	В6	Pressure-temp	erature-humidity-	9	17	3	17	
	B7		High-temperature storage	14	14	7	14	
	B8		Continuous operation	24	14	11	14	
	B9		High-humidity storage 85°C, 85% RH <sup>2</sup>	24	14	11	14	
	C1		High-temperature storage	14	15	7	15	
С	C2		Continuous operation	24	16	11	15	
	C3	Endurance test	High-humidity storage 85°C, 85% RH <sup>2</sup>	24	15	11	15	
	D1		High-temperature storages	14		7		
D	D2		Continuous operation <sup>6</sup>	24		11	_	
	D3	]	High-humidity storage 85°C, 85% RH <sup>2</sup> <sup>8</sup>	24		11	_	

Test cycle: Group A and B for every weekly lot, Group C every 13 weeks, Group D every 26 weeks

- Electrical reject devices can be used in this test.
   These tests are performed on resin-sealed devices.
- 3: This test takes 96 hours.
- 4: These tests normally take 500 hours. But if no defects are found in the first 168 hours, the lot can be passed and the test may be terminated.
  5: These tests take 1000 hours.
- These tests take 3000 hours.
- 7: This test takes 48 hours.
- These tests take 100 cycles.

## 7.4.3 Occasional Tests

Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Division according to the purpose of the test.

#### 7.5 Test Methods and Criteria

The reliability of Fujitsu ICs is assured by severe environmental and endurance testing. Test methods are usually based on Japan Industrial Standards (JIS), the standards of the Electronic Industrial Association of Japan (EIAJ), and MIL standards.

Reliability tests are performed for two reasons. Firstly, they check or guarantee the reliability of a type or a lot according to specified standards. Secondly, they are used to determine the failure rate or mode. The most appropriate test method is chosen for each test, and test results are processed in the most suitable manner. Fujitsu usually performs the tests listed in Tables 7–3, 7–4, and 7–5.

Table 7-3. Example of Reliability Testing

Test items	MIL-STD-883	Condition
Resistance to soldering heat		260°C, 10s
Temperature cycling	1010 C	-65°C (30 min.) to 150°C (30 min.), 100 cycles
Thermal shock	1011 A	0°C (5 min.) to 100°C (5 min.), 100 cycles
Vibration, variable-frequency	2007 A	20 to 2,000Hz, 20G
Mechanical shock	2002 B	1,500G, 0.5ms
Constant acceleration	2001 E	30,000G, 1 min, Y1 only
Final leak <sup>1</sup>	1014 A1	Using compressed helium 99.5 psig, 4 hrs.
Gross leak <sup>1</sup>	1014 C	Using fluorocarbon 75 psig., 1 hr., 125°C
0-1d		230°C, 5s
Solderability	2003	260°C, 5s
Lead fatigue	2004 B2	0.25kgf, 90°, twice
PTHS/PTHB <sup>2</sup>	_	121°C, 2 atm
High-temperature storage	1008 C	150°C, 1,000 hrs.
Continuous operation	1005 A to D	125°C, 1,000 hrs.
High-humidity storage <sup>2</sup>	_	85°C,85%RH, 1,000 hrs.

Notes: 1 Applies to hermetic packages.

2 Applies to hermetic packages.

Table 7-4. Example of Electrical Testing

Circuit classification	Characteristics	Bipolar	моѕ		
Gates	DC AC	Voн, Vol, liн, lil, lcc (lee) Function	VOH, VOL, IIH, IIL, IDD (Isub) Function		
Flip-flops	DC AC	Voн, Vol, liн, lil, loн, lcc (IEE) Function	VOH, VOL, IIH, IIL, IDD (Isub) Function		
Shift registers	DC AC	Voн, Vol, liн, lil, loн, lcc (IEE) Function	VOH, VOL, IIH, IIL, IDD (Isub) Function		
Memories	DC AC	VOH, VOL, IIH, IIL, ICC (IEE) Function	VOH, VOL, IIH, IIL, (IOH), (IOL.)		
Random-logic devices	DC AC	Voн, Vol, liн, lil, loc (IEE) Function	VOH, VOL, IIH, IIL, (IOH), (IOL.) IDD (Isub) Function		
Analog devices	DC AC	Vio, Iio, Ii, Vom, Voh, Vol, Av, Kf2, Nf	_		

Table 7-5. Example of Electrical Criteria

Parameter	Limit value (in multiples of the absolute value)						
Parameter	Upper	Lower					
Vон		Lx0.9					
Vol	U x 1.1	-					
Iн	U x 2 (No leak: U x 1.1)	_					
liL	U x 1.1 (Leak: U x 2)	_					
IOH ICC (IEE) ICC (Isub)	U x 1.1 (Leak: U x 2)	_					

"U" and "L" stand for the upper and lower limits

## 7.6 Reliability Theory

## 7.6.1 Estimating the Failure Rate

The graph of a component failure distribution is usually a downward-bowed curve, what is called the bathtub curve (Figure 7-2). Since semiconductors do not wear out physically, the distribution reflects the initial failure rates. Life tests show that the instantaneous failure rate decreases with time and graphs as a straight line on a Weibull probability sheet. Shape parameter m, which shows the instantaneous failure rate, is between 0.3 and 0.7. (In an exponential distribution, the instantaneous failure rate does not change and m=1. As m=1 becomes smaller than 1, the instantaneous failure rate decreases with time.)

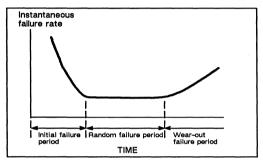


Figure 7-2. Distribution of Component Failure

Usually, the failure rates during the initial and random failure periods are the most important for semiconductors. Figure 7-3 shows an example of life test data graphed on a Weibull probability chart.

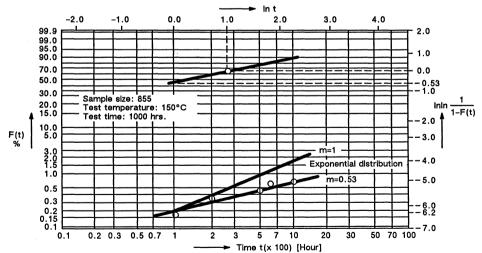


Figure 7-3. Example of High-temperature Storage on MOS IC

#### 7.6.2 Accelerated Life Test

Modern applications require an extremely low failure rate for semiconductors. To guarantee such strict quality, Fujitsu uses an accelerated life test. There is no fixed acceleration rate for semiconductors but, since semiconductor failure is usually caused by physical and chemical changes in materials, an acceleration rate can be calculated from the Arrhenius equation for the progress speed of physical and chemical phenomena (assuming the R is proportional to the degradation speed):

 $R = A \exp(-E_a/kT)$ 

R: Reaction rate

A: Proportionally constant

Ea: Activation energy

K: Boltzmann constant

T: Absolute temperature

The proportionality constant A corresponds to the component reliability. The activation energy, E, depends on the component's materials and their combination, but it ranges from 0.3 to 1.35 eV for semiconductors. This equation does not fit the data perfectly because it assumes that the failure rate is affected only by temperature when, in fact, there are many contributing factors. However, the equation does give a good rough fit. Using the equation on data from the accelerated life test, engineers can estimate and guarantee the field failure rate with reasonable accuracy.

The calculation method for the field failure rate is given below for Fujitsu semiconductor products. Although this method is not generally accepted yet, it has been found to be useful.

- (1) Calculate the junction temperature (Tj(op)) for actual use from the temperature rise (Tj) and the ambient temperature (Ta) under an average load (do not use the worst-case load), Tj(op) =  $\Delta$ Tj + Ta.
- (2) Calculate the junction temperature(Tjt) for a life test. For a high-temperature storage test, Tjt equals Ta (the storage temperature). For a continuous operation test, the temperature rise under load plus the ambient temperature (25°C except for high-temperature operation) for an operating temperature, Tjt =  $\Delta$ Tj + Ta.
- (3) Calculate the acceleration rate ( $\alpha$ ) from the difference of Tj(op) and Tjt using Figure 7-3.

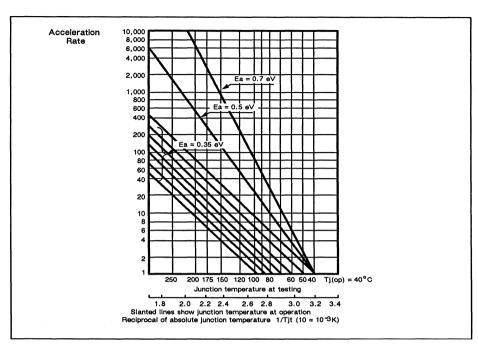


Figure 7-4. Acceleration Rate lpha vs. Junction Temperature

(4) If planning reliability testing or calculating reliability in the field from data obtained in steps (1) to (3), determine the coefficient γ for the 60% confidence level in Table 7-6 from the number of defective units allowed or from the total number of failures found in the test.

Reliability =  $\frac{n}{\alpha NT}$  x Y x 109 [FIT] where:

N: Number of samples T: Total test time (hrs)

n: Number of failed samples in test

Table 7-6. Determination of coefficient

No. of failures	Confidence level					
1101 01 141141 00	60%	90%				
0	(0.92)	(2.30)				
1	2.02	3.89				
2	1.55	2.66				
3	1.39	2.23				
4	1.31	2.00				
5	1.26	1.85				
6	1.22	1.76				
7	1.20	1.68				
8	1.18	1.62				
9	1.16	1.58				
10	1.15	1.54				

The above equation applies only when n/N is equal to or less than 10% for the total test time, T. If n/N exceeds 10%, use the following method of calculation: divide the total test duration time, T, into subsections,  $\Delta ti$  (i = 1,2, . . . , m), so that for each  $\Delta ti$  the failure rate,  $(n_{i+1}-n)/(N-n_i)$  (where ni is the cumulative number of failed samples for  $\Delta ti$ ), does not exceed 10%. Calculate  $(N-n_i)$   $\Delta ti$  for each time section  $\Delta ti$ . Calculate the summation  $\sum (N-n_i)$   $\Delta ti$  for all the time sections in T. The summation  $\sum (N-n_i)$   $\Delta ti$  must then be substituted for NT in the above equation.

#### 7.6.3 Failure and Causes

Circuit format differences, package types, and operating environments can change the mechanisms of IC failures, so it is difficult to foresee which factor will be the most important in a failure mechanism. Figure 7–5 shows specific electrical failures for ICs, their most common causes, and general corrective actions. Causes of IC failures are largely the same as for planar transistor failures, but the following problems are more common or specific to ICs:

- (a) Surface degradation
- (b) Flaws in an evaporated or sputtered metal film
- (c) Contact failures due to an increased number of wire bondings per package
- (d) Package failures due to an increased number of external leads

Table 7-7 lists failures with their most common causes, and Table 7-8 shows the relationship between operating environments and failure causes. Test items can be listed only if the failure cause can be pinpointed by the test.

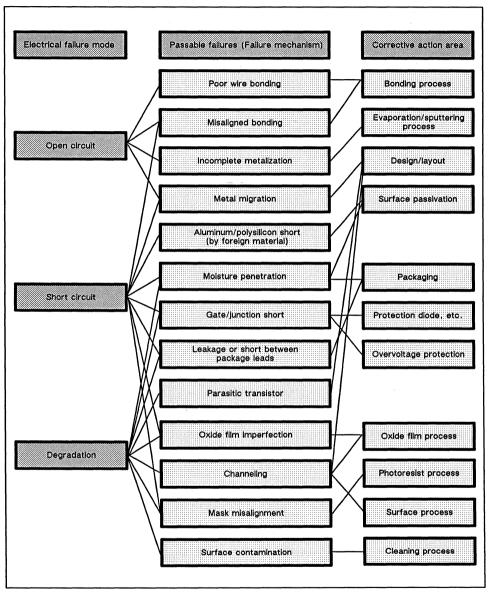


Figure 7-5. Digital IC Failures and Corrective Actions

Table 7-7. Process Defects Analysis

Defect Area	Defect mechanism	Frequency		Source	9		
			Design	Factory Process Control	Manuf. Tech.	Opera- tor Skill	User Applica- tion
Junction	Junction failure due to current crowding	High	•				•
(Internal)	Metal migration	Low	•	•	•	•	
Junction	Oxide film imperfection (Pinhole, crack, void, etc.)	Medium		•		•	
(Surface)	Impurity contamination	High	•	•		•	
	Metal peeling	Medium		•	•	•	
	Mask misalignment	Medium				•	
	Incomplete metalization	Medium		•	•	•	
inter- connection	Improper metalization	Medium					
COMINECTION	Metal over-stress	High					•
	Aluminum corrosion	Medium		•	•	•	
	Aluminum migration	Medium	•			•	
	Bonding peel	High			•	•	
Wire	Purple plague	Medium	•		•	•	
wire	Wire over-stress	High				•	•
	Particle/wire short	Low				•	
	Leakage	Medium			•	•	
	Die bond failure	Low	•		•	•	
Package	Lead breakage	Medium			•		•
	Package corrosion	Medium	•	•	•		•
	Chip crack	Medium			•	•	•
Others	Seal contamination	Low		•		•	

Table 7-8. Relationship between Failure Causes and Analytical Test Methods

						Test						
Failure Cause	Solder- ability (2003.2)	Tempera ture Cycling (1010.2)	Thermal shock (1011.2)	Constant Accelera- tion (2001.2)	Mechani- cal shock (2002.2)	Vibration, variable frequency (2007.1)	Lead fatigue (2004.2)	Baro- metric pressure reduced (1001)	Moisture resistance (1004.2)	Salt atmos- phere (1009.2)	Vibration fatigue (2005.1)	Vibration noise (2006.1)
Bond integrity (Chip or wire)		•	•	•	•	•					•	•
Cracked chip		•	•		•							•
Internal structural defect					•	•						
Contamination-/ contact-induced short		•		•	•	•					•	•
Wire or chip breakage				•	•	•						
Glass crack	•	•	•		•		•	•				
Lead fatigue  Contamination of junction (Surface)		•					•					•
Thermal fatigue		•										
Seal integrity		•										
Seal contamination				•	•	•	i					•
Leakage		•	•				•	•	•	•		
Package/material integrity		•	•						•	•		

# Chapter 8 - Application Notes

#### Contents of This Chapter

A8 Developing Test Patterns with Consideration of the Physical Tester

8B Selecting the Best Package for Your ASIC Design

8A. Developing Test Patterns that Work with the Physical Tester

#### 1.0 Introduction

This application note briefly describes the process of developing test patterns simulation and test of Fujitsu CMOS ASIC designs. This information supplements testing information found in the Design Manual for the appropriate Fujitsu CMOS ASIC technology.

## 2.0 Tests to be Created

Fujitsu supports five types of test:

- 1. DC test
- 2. Dvnamic function test
- 3. High impedance test (Z-function test)
- 4. Delay test (AC test)
- 5. Scan test (optional for certain Fujitsu technologies)

The DC test measures DC characteristics such as loos, VoH, VoL, ILI, and ILZ, while the function test screens for manufacturing faults (metal and transistor faults, principally). The Z-function test augments the DC test and is required for circuits in which one or more enable signals from a 3-state buffer can be generated by logic deeper than one gate of complexity within the ASIC device. The delay test may be used to verify critical timing paths that are necessary for proper system operation. Scan test methods may be used to simplify the process of testing for the manufacturing defects traditionally uncovered by the function test. Automatic test generation (ATG) is supported in conjunction with scan testing in the UH, UHB, and AU technologies as an option.

#### 3.0 Overview of Test Vector Creation

For each set of test patterns defined as a test block, the customer must specify input states and output states (in either a vector or wave format), and the timing of inputs and outputs (with bidirectionals being considered both an input and an output). Many designers rely on one of the Fujitsu-supported CAE workstations when generating test vectors, easing the burden of test pattern development. In these cases, the customer creates input stimuli for the workstation simulator, which then generates a print-on-change file containing the resulting output response and the associated input stimulus previously defined by the designer. The print-on-change file is converted by Fujitsu's workstation software into FTDL (Fujitsu Test Description Language), which is the accepted test pattern description format regardless of the method by which patterns are created.

#### 4.0 Developing the Tester Timing Information

Whether or not the patterns are generated on the CAE workstation, it is necessary for the customer to generate in the FTDL file a Common Block file, containing administrative information and the test type, and a Test Block file, containing the timing information for all chip inputs and outputs by group (discussed further in the Design Manual). The definition of this overall timing is critical to the success of the test program itself. For example, input timing defines when input signals will transition, while output timing defines when outputs will be compared with their expected values or measured at a transition point.

The designer is responsible for specifying the following timing parameters for the Test Block, depending on the specific type of test:

- 1. Test Cycle
- 2. Grouping of inputs and, if necessary, outputs and bidirectionals
- 3. DT (Delay to Transition) time for each input group of NRZ (non-return to zero) signals
- tp and Wp (delay-to-transition and pulsewidth) times for the positive-going and negativegoing pulses (PP and NP) for each input group of RTZ (return to zero) signals
- 5.\* STB (delay-to-strobe time) point for each output group
- 6.\* DT and STB times for bidirectionals
- 7.\*\* T time in the SPATH statement for AC tests
- \*Specified in DC, function and Z-function tests
- \*\*Applicable only to AC tests.

This timing is established for the entire test block and is invariant until another test block is invoked. Therefore, test pattern timing is periodic, that is, a group of inputs may only transition at the time specified in the Test Block, which is relative to the beginning of the test cycle. This delay to transition time for inputs is programmed for each input group with the tp parameter in the FTDL INTIM or BUSTIM statement.

Similarly, common output groups are strobed, or sampled, periodically at a time determined by the test cycle and the delay-to-strobe time specified in the OUTTIM or BUSTIM statement, or the T parameter in the FTDL SPATH statement in the case of an AC test.

## 5.0 Determining Input and Output Timing Parameters

During the function test, outputs should stabilize before being strobed. Therefore, the minimum permissible test cycle programmed by the TIMING statement in the Test Block should be set with consideration of the maximum propagation delay from any input to any output, and the respective DT and STB times for those groups should be set far enough apart in time to assure that the outputs are stable under maximum conditions. Similarly, if the output is strobed before the transition, it must be stable under minimum delay conditions.

Test patterns are required to be invariant over minimum and maximum delay conditions. This is verified in simulation by scaling the typical delays by multipliers representing process, temperature, and power supply variations. Similarly, the strobed or expected output states must be identical under typical, maximum, and minimum conditions. If a propagation delay from input to output is greater than the test cycle defined, output states may not fulfill this requirement (see Figure 8A–1). Furthermore, designers should be careful that glitches or short pulses do not occur anywhere within this minimum/maximum window (see Figure 8A–2).

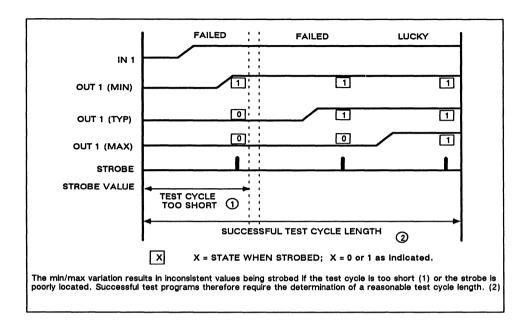


Figure 8A-1. Determining a Successful Test Cycle Length

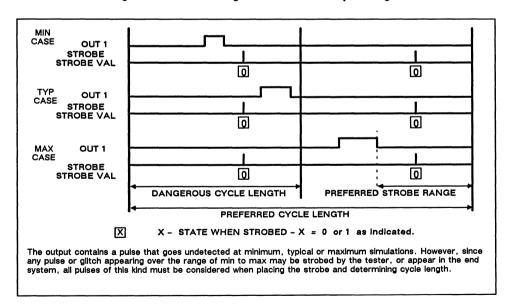


Figure 8A-2. Determining Preferred Cycle Length

## 6.0 Generating Functional Input Stimulus Given Test Pattern Timing

Issues that must be considered when determining test pattern timing are the relationship between input signals, such as clock/data pairs, which must satisfy set-up and hold times. Other considerations guiding the timing definition are dependent on the particular circuit being tested, and on restrictions imposed by the tester. These restrictions are published in the Summary of Test Data Restriction section of Fujitsu's Design Manuals.

## 7.0 Tester Skew and its Compensation of Test Timing

The designer must pay particular attention to the issue of tester skew when determining input and output timing for Test Blocks: otherwise, the timing will not correctly represent the behavior of the device under test. Tester skew, specified for each technology in the Summary of Test Data Restrictions, is a result of the variation in the time at which a given signal generator triggers a transition or a comparator measures an output state. Several timings are affected by this skew.

#### 7.1 Input-to-Input Skew

For the purpose of estimating the skew between two signal generators, (one driving data and the other driving its clock, for example), the driver skew, linearity of clocks, clock-to-clock skew, and jitter are collectively called driver accuracy, denoted tDSKEW.

In the case of data/clock pairs, the clocked data may either fail a set-up or hold time, depending on the direction of the skew. Therefore, when determining DT and tp for data/clock pairs, the designer should adjust times to satisfy the following relationships (see Figure 8A-3):

Set-up Time Criteria for Testing: (tp(CLOCK) - DT(DATA)) >= ts(MIN) + 2 \* tDSKEWHold Time Criteria for Testing: (DT(DATA) - tp(CLOCK)) >= th(MIN) + 2 \* tDSKEW

Where ts(MIN) and tH(MIN) are the worst case set-up and hold times, respectively, sensitized from the internal circuit to the inputs, tDSKEW is not directly specified in the Summary of Test Data Restrictions; however, TACC, the overall system timing accuracy, is specified and can be substituted for tDSKEW (see Section 7.2).

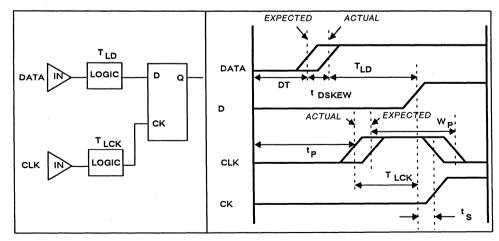


Figure 8A-3. Input-to-Input Skew

### 7.2 Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual comparators, and the driver-to-comparator timing error. All factors are considered in the overall system timing accuracy, tACC, which in turn affects output timing as shown in Figure 8A-4.

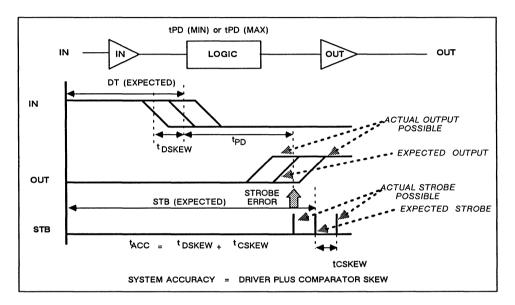


Figure 8A-4. Input-to-Output Skew

## 7.3 Skew Effect on Input/Output Pairs - Minimum Delay Case

The STB (or T parameter in the SPATH statement) should expect an output transition at a time relative to the stimulated input transition dictated by:

where STB is the strobe point of the output under consideration, DT is the DT time of the stimulating input of interest, and tPD(MIN) is the minimum propagation delay from this input to the strobed (or measured) output. In the case of the AC test, the quantity (STB - DT) should be replaced by the minimum T parameter in the SPATH statement. Note that if the path delay spans a test cycle boundary, STB should be set to STB plus the test cycle period.

## 7.4 Skew Effect on Input/Output Pairs - Maximum Delay Case

The complementary case occurs for maximum delay measurements, as described by:

Note that these guidelines regarding the specification of test data timing as affected by tester skew apply to DC and Z-function tests as well. In these cases, the same rules apply as for the function test.

Again, for the specific values of tACC, and tDSKEW, please refer to the Summary of Test Data Restrictions in the Fujitsu Design Manual for the appropriate technology. A designer interested in a methodical approach to the generation and verification of a good set of test vectors must consider the tester hardware on which it is running. Fujitsu has simplified designer responsibility by providing this information as part of the Test Block Information.

However, a lack of implementation and careful analysis of the timing characteristics of the circuit may result in a poor or unfeasible test, resulting in schedule delays or reduced device yield. Therefore, plan a test approach early, design for testability, and consider the effect and operation of the physical tester.

## 8B. Selecting the Best Package for Your ASIC Design

#### 1.0 Introduction

The widely varying degrees of complexity (gate count) of Fujitsu's CMOS and BiCMOS devices and the flexibility of their I/O configurations combine to produce devices that can be accommodated in a wide variety of package implementations. With the equally broad selection of packages available from Fujitsu, however, the requirements for package selection go far beyond pin count as the sole determinant of the best package. Selection issues include surface mount versus through-hole, plastic versus ceramic, and exotic versus conventional packaging. In fact, Fujitsu offers over 100 packages and 1000 package-die combinations from which to choose. Compounding the selection problem is the effect of increasingly faster outputs coupled with higher drive and wider bus structures, resulting in greater numbers of simultaneously switching outputs (and thus greater amounts of noise).

The result is that designers are finding ASIC design packaging implementation to be an increasingly complex task. This application note provides information about ASIC packaging that is meant to simplify the designer's task. It provides designers with a review of the various Fujitsu packages and their electrical, thermal, and mechanical characteristics, as well as some problem-solving strategies for their use. The first part (Sections 2.0 and 3.0) addresses system requirements and package availability; the second part (Sections 4.0 and 5.0) discusses noise and thermal issues.

## 2.0 How System Requirements Affect Package Choice

Section 2.0 presents considerations involved in the selection of packages from a system designer's perspective. Figure 8B-1 lists issues a designer must consider when determining the optimal packaging for an ASIC design.

Manufacturing and Cost-Related Issues	Speed Requirement Issues				
Board Integration	Package and Interconnect Delays				
Double-sided Component Mounting	The Effect of Package on Noise				
Number of Packages	Thermal Considerations				
Package Outline Area					
Power Density Limitations					
Producibility Issues	<b>Quality Considerations</b>				
Board Layout	Package Quality and Reliability				
Package Construction	Number of Devices				
Packaging Complexity	Noise				
Manufacturing Flow	Thermal Considerations				

Figure 8B-1. Considerations for Package Selection

## 2.1 Manufacturing and Cost-Related Requirements

The manufacturing-related factors discussed below, although not directly related to the design of the device or the number of power and ground pins it requires, are nonetheless important in the choice of an ASIC package.

#### 2.1.1 Board Area

One of the most important issues is the board area consumed by a circuit. Some of the factors affecting overall board density are:

Integration (gates per square inch of board)

Double-sided mounting capability (integration)

Number of packages

Package outline area

Additional board space required (for spacing, resistors, capacitors, probe areas, etc.)

Power density area (discussed in Section 5.0)

The critical issue in board area reduction, however, is overall integration. For example, surface mount devices (SMDs) can be densely mounted on both sides of the board, making them ideal for systems demanding high package integration. But a large design integrated into a few very large Sea-of-Gates arrays, even if packaged in large, through-hole packages, may well consume less board space than the same design using surface mount PLCCs. The PLCC version would require more space because the PLCCs, although small in outline, cannot house as large a die and therefore require the design to be partitioned into a greater number of devices.

Figure 8B-2 illustrates the board area taken up by the outline of each kind of package Fujitsu offers, excluding any area around the package necessary for spacing, decoupling capacitors, series damping resistors, or solder pads.

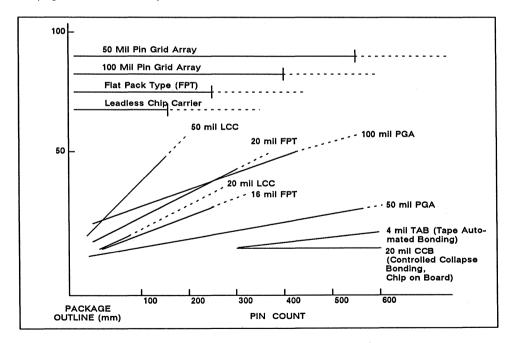


Figure 8B-2. Package Size vs. Pin Count

#### 2.1.2 Board Layout

Restrictions in board layout or construction must be identified and resolved early in the design process. For example, a design containing large buses (16 bits or 32 bits or more) must be split up to comply with SSO restrictions (to maintain proximity to ground pins). Splitting up the buses, however, may result in variations in signal trace length and require extra care in routing. Similarly, flatpacks, a form of SMDs, are a convenient way to support high pin counts in relatively inexpensive plastic packages. However, with pin pitches as narrow as 15 mils (1\1000 of an inch), they demand extremely accurate positioning of solder pads. Dense PGAs, on the other hand, provide a spacious 100-mil pin separation, but because of the number of rows of pins, normally require a large number of board layers.

## 2.1.3 Producibility

Though some unusual packages may appear to promise ultra-high speed or dense integration or minimized component/board cost, the designer must always keep manufacturability in mind. The cost of a system is only partially dependent on materials and labor costs per unit; it is also highly dependent on the manufacturing yield of the end product. Therefore, design and production engineering must consider the choice of package jointly in order to guarantee that the chosen package conforms to existing (or purchasable) manufacturing equipment and that the manufacturing process can meet yield goals.

## 2.2 Speed Requirements

The speed requirements of a system strongly affect package choice. If the interconnect lengths in the system (both inter- and intra-board) can be reduced, system speed may be increased. Reducing interconnect lengths may involve reducing the required number of packages, choosing packages with smaller outlines, changing to double-sided, modular, or piggy-backed mounting, using small form factors, reorganizing boards, and even changing the number of metal routing layers of the board. See Figure 8B-3.

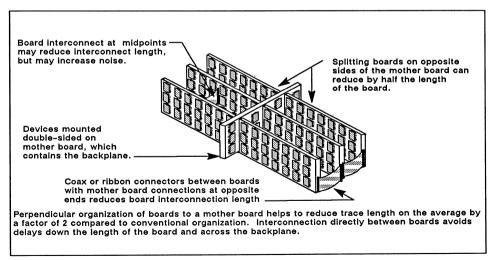


Figure 8B-3. Minimizing Interconnect Length

## 2.2.1 The Effect of Noise on Speed

There are various sources of noise that can affect an IC, each with its own effect; all forms of noise influence signal speed, quality, and consequently, system reliability. Certain types of noise arise between a chip I/O and ground or power, while other forms of noise are coupled to the power rails and influence system power and ground lines, propagating the noise throughout the entire system. Noise appears to an input buffer (receiver) relative to the receiver's ground. Any noise on this referenced signal is superimposed onto the incoming signal itself, as shown in Figure 8B-4. The VIH or input threshold level of the receiver indicates when the input will switch, if the signal is stable at that level. Therefore, although the input voltage ordinarily would switch 4 ns after the driver switches, when the signal first crosses the threshold, the designer must assume it will not switch until it is stable; in this case at 8 ns, producing a loss of 4 ns due to noise.

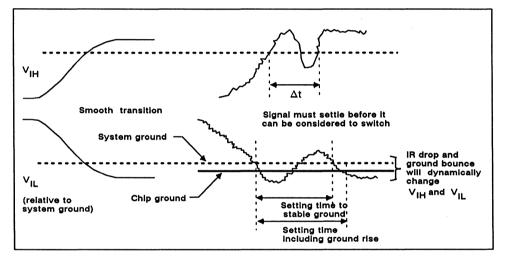


Figure 8B-4. Impact of Noise on Speed

## 2.2.2 Controlling Noise through Package Selection

Each form of noise is dependent not only on current or its first derivative with respect to time, but also on the real and imaginary components of impedance: resistance (R), inductance (L), and capacitance (C). One solution to noise can be to minimize the package L and R and to locate high drive pins where they will minimize L and R.

## 2.2.3 The Effect of Thermal Characteristics on Speed

The speed performance of a CMOS or BiCMOS circuit degrades with temperature rise. Therefore, in very high speed systems, it is sometimes necessary to reduce the junction temperature (Tj) or die temperature as a way to improve speed. Certain packages offer better cooling properties than others, making them more suitable for high speed systems. Thermal issues are discussed in Section 5.0.

## 2.3 Quality and Reliability Requirements

Reliability refers to the defects or failures that appear during the lifetime of a device. Quality, on the other hand, refers to the frequency of occurrence of defects or faults in a device as a result

of the manufacturing process. Quality defects are revealed by testing immediately after manufacturing, while reliability defects are revealed by special long-term or intensive test sequences or by time.

## 2.3.1 How Package Type Affects Quality Testing

Conventional (through-hole) packages lend themselves to simplified testing because it is easy to access the leads in order to force a state (1 or 0) at a node and/or to observe the state of the node. These tests are performed with board-level in-circuit or functional testers. Such tests facilitate the manufacture of high-quality systems by ensuring proper connectivity and function.

Surface mount devices, however, generally provide poor probe access, and are known to occasionally possess faulty joints that make temporary connections during probe. Through-hole packages also have occasional bad solder joints, although their node access is fairly good.

## 2.3.2 How Device Integration Affects Reliability

Total system reliability is related to the reliability of the individual devices and to their configurations. Systems may be configured as a series in which all devices are interdependent, in which case any one failure will cause overall system failure, or they may be configured in parallel, in which case all devices must fail for the system to fail. Parallel configuration is used in redundant or fault-tolerant systems.

The reliability of a system also depends on the reliability of the devices that comprise the system. The long-term reliability of a single device is defined as an inverse natural log function in a variable lambda, which is the failure rate of the device in the region of lifetime operation characterized by a constant failure rate. In the first hours of a device's life (the infant mortality period), the failure rate declines. The majority of a device's life is characterized by random failures (expressed as lambda), and the end of a device's life exhibits an increasing failure rate. Today's ICs, however, are designed so that wearout does not even begin to occur for at least several hundred years, and can be considered never to occur. To understand how the partitioning of a system into circuits can affect the reliability of a system, consider a system in which N components are configured in series. Although the density of ASIC devices has increased by two orders of magnitude in the last decade, the reliability of the devices has remained roughly constant. Therefore, it can be assumed that the failure rate of each of the components is constant. The reliability of systems and subsystems in which components are series-dependent is the product of the individual reliability terms for each component. The reliability function of the system just described is therefore:

$$R(t)sys = R(t)1 * R(t)2 * ...R(t)N$$

where R(t)N = e - Nit, t is the independent variable time, and I is lambda, the failure rate.

Since all components have the same failure rate, the reliability function of the system is:

$$R(t)svs = e - Nlt$$

Because the number of packages affects the reliability more than the integration factor does, a designer's goal in constructing a reliable system should be to maximize integration and thereby reduce part count.

The disadvantage is that increased integration may in turn increase the package pin count, requiring a more complex package, which usually costs more than a simpler, smaller package. Additionally, the larger die sizes cost slightly more per gate than the smaller ones, although the total NRE (non-recurring engineering charges) would typically be lower.

## 2.3.3 How Noise Affects Reliability

Even when Schmitt trigger input buffers are used to receive clock signals, noise may go beyond the hysteresis value of the input buffer and cause a counter to be incorrectly clocked or other circuit malfunction. Noise is in this sense a threat to reliability as well to speed and must be considered in the choice of package as well.

## 2.3.4 How Thermal Issues Affect Reliability

While the junction temperature of a device affects its speed, it also affects reliability expressed as MTBF (mean time between failures) or the mean time a device will operate in a given environment before failure occurs. Figure 7-4 in the previous chapter, Quality and Reliability, illustrates this concept by plotting life test failures as a function of junction temperature. System reliability goals, then, restrict the desired maximum junction temperature in a manner that affects the choice of package according to its thermal characteristics, the chosen type of system thermal management (cooling), and the maximum allowable device power dissipation.

## 2.3.5 How Package Material Affects Reliability

The different materials used in package construction each have distinct thermal and mechanical properties. The most common materials and their characteristics are listed in the table in Figure 8B-5 below.

Package Type	Body Material	TCE (ppm/ °C)	Thermal Conductivity (W/m * °C)	Dielectric Constant (K)
Ceramic	Al <sub>2</sub> O <sub>3</sub> (Alumina)	7.0	20	10
Plastic PGAs	Epoxy Fiberglass	14 – 18	0.16	4.5 - 5.0
Other plastic packages (DIP, PLCC, Flatpack)	Polyimide Epoxy	15 – 18	0.38	4.5 - 5.0

Figure 8B-5. Package and Material Characteristics

To better understand the different characteristics of plastic and ceramic packages, it is helpful to know something about the way they are constructed. Packages provide electrical connection from the IC to the system and isolate the device from destructive elements of the environment. The choice of materials and construction of a package affect its final dimensions, thermal characteristics, and electrical characteristics, as well as device reliability. Fujitsu carefully determines the most appropriate manufacturing methods for a given package and then performs extensive qualification tests to determine its success.

The largest part of the package is the body, which houses the die. The die may be affixed to a lead frame, which physically supports the die and provides the leads that electrically connect the die to the system by means of bonding wires or tab leads. Alternatively, the die may be supported by a cavity on the body of the package or attached to the bottom of the body by a chip carrier.

The die is attached to the surface of the lead frame or to the metallized surface of the cavity or carrier with gold or silver paste, or eutectic. After the die is attached to the lead frame, cavity, or carrier and the bonding pads are bonded to the leads, the assembly is encapsulated. In plastic packages, an epoxy resin is molded around the assembly. In ceramic packages, a cap is sealed

onto the lower part of the body or carrier using a frit glass or metal seal (the metal seal has a higher melting temperature than the glass). A solder seal can be used if the cap is metal.

To ensure that the device is completely isolated from its environment, the surface of the die is then coated with glass (SiO2) and then polyimide or other coating that prevents gas and moisture from coming in contact with the surface of the die. Figure 8B-6 shows a frontal cross section of the structure of a PLCC package; Figure 8B-7 provides a top view.

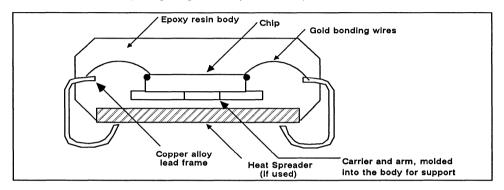


Figure 8B-6. PLCC Package Construction (Front View)

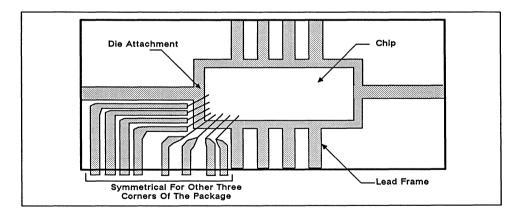


Figure 8B-7. PLCC Lead Frame Construction (Top View)

Each of the various packaging methods has its advantages and disadvantages; for instance each body type and each type of seal has a different maximum case temperature. While plastic packages can tolerate temperatures to up 125°C and high humidity levels with outstanding reliability, ceramic packages are the most reliable for harsh extremes of cold.

Each package type also responds differently to the thermal environment of the board to which the device is attached. Heat can cause thermal stress on the device when different materials expand at different rates, a particularly important factor when surface mount packages are involved.

Different packages also exhibit different electrical characteristics. As the speed and gate densities of CMOS devices rise, the avoidance of electrical parasitics in the form of package delays and noise become increasingly important factors in choosing a package type.

Fujitsu's plastic PGA provides a good example of the tradeoffs involved in package construction. In 1986, Fujitsu introduced the plastic version of its ceramic PGA. The plastic configuration proved to have several advantages over the ceramic version. The body is formed from glass epoxy (VG-10) with an aluminum cap and an epoxy resin sealer. This combination of materials has the same rate of expansion as the PC boards onto which it is mounted; it is also less expensive than ceramic.

Ceramic PGAs have a hermetic seal of solder between the metal lid and the cavity, but plastic PGAs are sealed by filling the cavity with epoxy resin to form an inner seal, then placing a resin sheet over the inner seal to form an outer seal, and then securing an aluminum cap over the outer seal. The aluminum cap provides the necessary rigidity to support the fragile glass epoxy, as well as improving the thermal conductivity of the package.

Connections from the bonding wires to the pins are provided by copper traces designed to minimize mutual and self inductance. Because the plastic PGA is a large package, however, and generally houses a large die, the thermal coefficient of expansion (TCE) difference between the die and the cavity can exert stress on the bonding wires and the die attach. Figure 8B-8 lists the package types discussed in this section and the materials used to construct each type.

Package Type	Lead frame/ Metallization	Lead/Pad	Lead Finish	Cap Material	Body Material	Seal Material
Plastic DIP	le-Ni or Cu Alloy Lead frame	Same	Solder Dipped		Resin	Resin
Ceramic DIP	Tungsten Metallization	Kovar or Fe-Ni	Au/Sn Plated	Metal or Aluminum	Laminated Alumina	Solder, Glass Frit
CERDIP	Fe-Ni Alloy Lead frame	Fe-Ni	Sn Plated	Alumina	Alumina	Glass Frit
Plastic Flatpack	Fe-Ni Alloy Lead frame	Same	Sn Plated		Resin	Resin
Ceramic Flatpack	Fe-Ni or Kovar Lead frame	Same	Au Plated	Metal or Aluminum	Laminated Alumina	Solder or Glass Frit
Cerpack	Fe-Ni Alloy Lead frame	Same	Sn Plated & Solder Dipped	Alumina	Alumina	Glass Frit
Plastic PGA	Cu Conductor on Epoxy glass	Kovar	Ni Plated & Solder Dipped	Aluminum	Epoxy Glass	Resin
Ceramic PGA	Tungsten Metallization	Kovar	Au Plated & Solder Dipped	Metal or Alumina	Laminated Alumina	Glass Frit
Plastic LCC	Cu Alloy Lead frame	Same	Solder Plated		Resin	Resin
Ceramic LCC	Tungsten Metallization	Tungsten Metal, Pad	Au Plated	Metal or Alumina	Laminated Alumina	Solder, Glass Frit

NOTES: All above packages are hermetic. Alumina is a ceramic. Solder is PbSn. Fe-Ni is ferrous (iron) nickel. Kovar is an alloy. Bonding wires are gold in the case of molded packages (epoxy resin PLCCs, DIPs, Flatpacks) and gold or aluminum for the other cases. Cerpack is the ceramic flatpack equivalent of CERDIP.

Figure 8B-8. Fujitsu Package Types

## 2.3.6 Package Qualification to Ensure Reliability

Fujitsu performs extensive six-month minimum qualification tests for every package-die combination. After such qualification is performed, the package die-combination is added to a package matrix that is supplied in the Design Manual for the appropriate technology. The designer can be assured that Fujitsu has considered the issues presented here, as well as others, when releasing an approved package-die combination.

## 3.0 Package Types

VLSI ASICs are supported by a wide variety of packages, of both surface mount and through-hole types. Through-hole devices, including dual in-line packages (DIPs), and pin grid arrays (PGAs), are a proven technology and are supported by widely available production equipment. The pins of these devices are inserted though holes in the PC board to form electrical contact with traces (usually copper) which are embedded in the board or applied to the surface and are routed to drilled pin holes. Solder applied by reflow or wave technique then completes the connection.

#### 3.1 Through-hole Packages

### 3.1.1 Dual In-line Package (DIPs)

DIPs have two rows of pins spaced 300 mils to 900 mils apart, with a pin spacing of 70 to 100 mils. Since the length of the package increases as each pair of pins is added, the size of a DIP tends to be unmanageable over 64 pins. The lead width and length of a DIP varies widely, causing variation in the input and output response of the device and thus, skew. Also, due to their high pin inductance, DIPs tend to be noisy, the degree of noise being a function of the location of outputs and sensitive inputs.

The DIP is relatively simple for manufacturing to support, thanks to a large installed base of well-proven equipment and is one of the least expensive packages available. Furthermore, DIPs, being well established, come in many JEDEC-approved options (see JEDEC Standard 95), and are available in both ceramic and plastic cases.

## 3.1.2 Pin Grid Arrays (PGAs)

Although PGAs are usually through-hole (Fujitsu also offers SMD versions), they differ from DIPs in that pins are arranged in rows on all four sides. While the pin spacing is usually the same as for DIPs (70 to 100 mils), nesting the pins in rows permits a larger number of pins to be contained within a smaller area allowing PGAs to support high pin counts of more than 300 pins. See Figure 8B–9 for a list of Fujitsu PGAs.

Package	Type	Construction	Number of Pins
PGA - 64C, 64P	Through-hole	Ceramic/Plastic	64
PGA - 88C, 88P	Through-hole	Ceramic/Plastic	88
PGA - 135C, 135P	Through-hole	Ceramic/Plastic	135
PGA - 179C, 179P	Through-hole	Ceramic/Plastic	179
PGA - 208C	Through-hole	Ceramic	208
PGA - 256C	Through-hole	Ceramic	256
PGA - 256C	Surface	Ceramic	256
PGA - 299C	Through-hole	Ceramic	299
PGA - 321C	Staggered	Ceramic	321
PGA - 361C	Staggered	Ceramic	361
PGA - 401C	Staggered	Ceramic	401

Through-hole = 100 mil through-hole Surface = 50 mil surface mount PGA Staggered = 71 mil staggered PGA

Figure 8B-9. PGAs Available from Fujitsu for CMOS

Although PGAs are generally easy to support from a manufacturing standpoint, they may also raise problems. The PC board designer may find it difficult to route signals to and from the inner rows of the PGA, since it has only 100 mils spacing between pins. Additionally, the large cluster of pins confined to a small area tends to create trace congestion and may require boards of up to six layers to be used to support the PGAs. Manufacturing engineers find the solder joints for the pins of inner rows are difficult to inspect, forcing them to rely on the results of "bed-of-nails" in-circuit testers, or sophisticated inspection techniques such as x-ray or infrared.

Although more expensive than DIPs, PGAs have come down in cost with the introduction of plastic PGAs (previous PGAs were usually ceramic). These plastic PGAs are generally constructed of G-10 glass-type epoxy with the traces routed through the epoxy the way they are routed on a typical PC board. (The electrical characteristics are, or course, tightly controlled). Although the reliability of plastic PGAs was initially in question, Fujitsu built them using special construction techniques employing metal lids and heat spreaders to provide rigidity and heat dissipation. Their excellent reliability history up to this point seem to indicate that plastic PGAs will continue to be popular. The widely-used epoxy thick-film substrate, once a quality and reliability concern, has the same thermal coefficient of expansion (TCE) as the most common PC boards, and reduces the stress of expansion and contraction that is typically a concern with larger packages. (The distance of expansion per unit change in temperature increases with the size of the package).

## 3.1.3 Advances in Through-hole Packaging at Fujitsu

The demand for high pin-count plastic packages cannot be satisfied by merely increasing the number of pins a package supports. As size increases, so do the problems inherent in these lower-cost packages. These problems include greater lead inductance and thermal expansion mismatch between die and package. Ceramic flatpacks can support more pins than plastic packages, but they require special manufacturing capabilities, and are difficult to work with since they may have pin pitches down to 10 mils. Surface mount PGAs (discussed in Section 3.2) can support a large number of pins, but require difficult manufacturing processes.

Fujitsu's answer to these problems, for the customer who wants high levels of integration without the need for exotic manufacturing methods, is the staggered PGA, shown in Figure 8B-10.

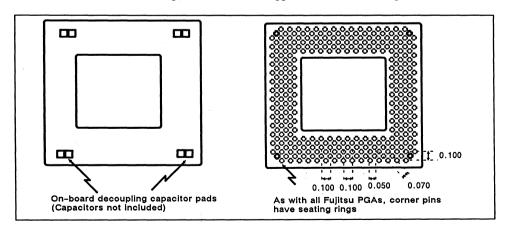


Figure 8B-10. 321-Pin Ceramic Pin Grid Array

Figure 8B-11 illustrates the footprint of the staggered PGA and the method for routing traces through the leads. Note that the routing is oblique, with the traces offset 45 degrees compared to traditional routing. At this angle, the lead spacing is 71 mils, providing the trace density available with standard through-hole devices, while reducing the package outline by approximately 40%.

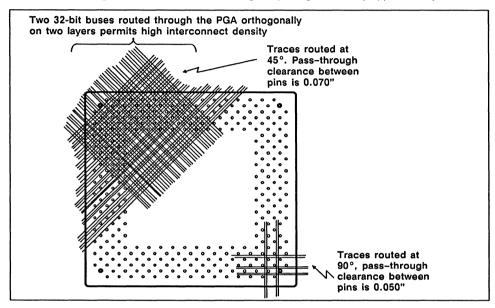


Figure 8B-11. Staggered Pin Grid Array Routing

The lead configuration of a package affects the pin assignment of the ASIC device. For example, Figure 8B–12 shows a situation in which a 32-bit address bus and a 32-bit data bus are routed through the device, with one offset 90 degrees from the other. If you assign consecutive bit significance to the bus, you will notice that the resulting pinout is quite different from an equivalent circuit packaged in a traditional orthogonal PGA. High drive buses can still be distributed around the ground pins, but the associated pads are not concentrated in one specific area of the die, reducing the concentration of simultaneously switching outputs, thereby reducing signal noise.

#### 3.2 Surface Mount Devices (SMDs)

The demands of military applications, space-constrained systems and boards containing large numbers of memory devices were initially responsible for the development of surface mount technology (SMT). However, the accelerated push for physically reduced systems, the appearance of higher pin count ASICs, and the cost of pin grid arrays have forced many more designers to consider surface mount options. Easing the strain of the migration to SMT is the broader availability of pick and place, vapor phase soldering, and other necessary SMT equipment, as well as the availability of SMDs for an increasing percentage of devices on the boards. SMT for VLSI is gaining momentum due to the smaller board area consumption, smaller profile, and proven reliability.

#### 3.2.1 Flatpacks

Plastic flatpacks have been popular for years with manufacturers of peripherals in which the board area is constrained and height is restricted. And recently, the low cost of flatpacks (in plastic) has

made them an attractive alternate to PGAs and even to DIPs in cases of higher pin count. As the following figures show, flatpacks come in several lead type and location configurations. Figure 8B–12a illustrates a SOIC (small outline integrated circuit), with gullwing leads on two sides, Figure 8B–12b illustrates a quad flatpack (QFPT) with gullwing leads on four sides. Flatpacks with axial leads require special assembly, and are generally used only for ECL circuits in which leads may have to be trimmed and formed to tune impedance.

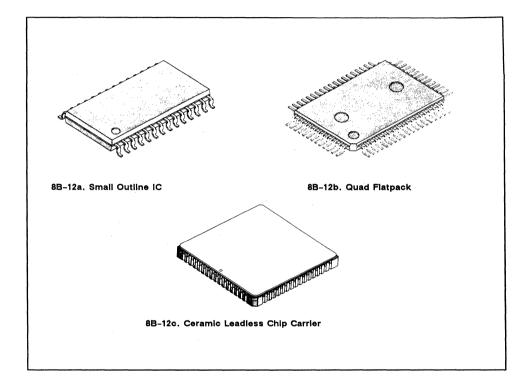


Figure 8B-12. Flatpack Configurations

Because flatpacks feature pin pitches (pin spacing from center to center) down to 10 mils, they can support high pin counts within a small board area. However, the narrow pin spacing means that accuracy in device placement, pad size and placement, and solder paste application tolerance are all more critical. PCB designers also need to determine whether the true package dimensions are in metric or English dimensions, and, when converting between the systems of measure, ensure that enough precision is maintained so that pins on the end of large packages won't roll off due to inaccuracies in pad location.

Probing devices with fine pin pitches can be difficult because the pins do not pierce the bottom of the board, and if probes are attached to the leads, they can easily slip off and short adjacent leads.

#### 3.2.2 Leadless Chip Carriers (LCCs)

Ceramic leadless chip carriers (CLCCs), such as the example shown in Figure 8B-12c, have a long history in surface mount packaging. Ceramic packages perform well in high temperature environments, explaining their popularity in military applications. The term "chip carrier" comes from the process of mounting the die directly to a thick-film chip carrier, which also has pads for external connection on the opposite side of the substrate. This configuration differs from that of the PGA, in which the die is housed in the cavity of the package, or the flatpack, in which the die is held by the lead frame and molded with the package. CLCCs are available in pad counts ranging from 28 to 84 and beyond.

Pads, not leads, are located on the bottom of the carrier and are generally spaced at a 40-mil pitch (standard). Solder paste is applied to the pads on the board to which the device will be mounted, usually by screen printing, and the board is then vapor phase or infrared reflow soldered. Because the pads are located beneath the package, they are typically very difficult to probe and are subject to manufacturing defects such as solder voiding (gas bubbles in solder formed during reflow).

The most challenging problem inherent to LCC devices relates to thermal coefficient of expansion (TCE) mismatch between the chip carrier and the board to which it is mounted. As the temperature of boards and packages rises, the materials expand at different rates. This difference translates to mechanical shear force at the solder joint. This force temporarily deforms the leads of PLCCs and flatpacks, but CLCCs have no leads. Consequently, the force is directed at the solder joint, tending to promote thermal fractures, (shown in Figure 8B–13).

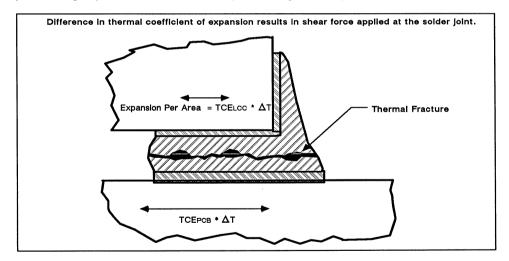


Figure 8B-13. Defect Caused by Difference in Thermal Coefficient of Expansion

Even though CLCC SMDs cost more than equivalent plastic packages, their resistance to high temperatures, availability in hermetically sealed (moisture resistant) packages, and low profile of the CLCC SMDs make them very useful for applications in extreme environments. The TCE mismatch problem affecting LCCs is less severe when they are mounted to ceramic hybrids or PC boards, making their disadvantages acceptable in many circumstances.

#### 3.2.3 Leaded Chip Carriers (PLCCs)

If cost and TCE mismatch are a significant deterrent to the use of LCCs, leaded chip carriers may be more attractive. Though the chip is still mounted on a carrier (see Figure 8B-15), the electrical connections of PLCCs are through pins that deform to absorb the TCE-induced thermal stress. Furthermore, while solvents used in the post-soldering cleaning process may be retained beneath the low profile of the CLCC and flatpack, the board offset of the PLCC permits it to remain free of these contaminants. In addition, the LCC in a plastic package costs less than the equivalent CLCC. This package is termed an SOJ (small outline J-lead) when its bent leads are located on only two sides (Figure 8B-14). The leads are bent into the form of a J in order to permit it to be placed on top of the solder pad.

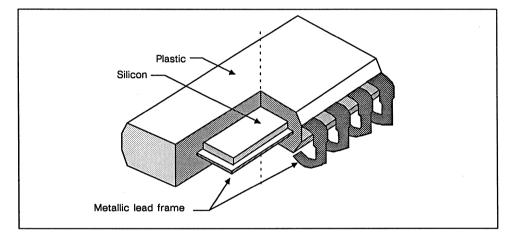


Figure 8B-14. Cross-Section of a Plastic Small-Outline Package

When more pins are necessary (in the 44-, 68-, 84- pin packages necessary for ASICs), the LCC is called a PLCC (shown in Figure 8B-15). It is also available in a ceramic body version; both are available in pin counts of 28 to 84 and beyond.

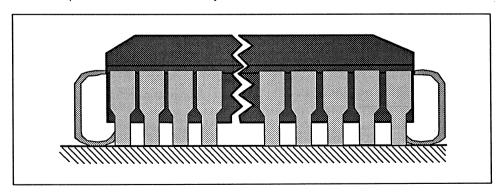


Figure 8B-15. PLCC Package

On the list of drawbacks of the PLCC is its limited ability to withstand high case temperatures, and its unavailability as a hermetic package. It is nevertheless very well suited for industrial and commercial environments. With a 50-mil pin pitch and only slightly greater height and width, the profile of the PLCC is nearly equivalent to the corresponding CLCC.

#### 3.2.4 Advances in Surface Mounted Packages

While smaller process geometries themselves have few disadvantages, the associated increase in integration, speed, power, and particularly pin count place heavy burdens on packaging. The greatest challenges CMOS faces is supporting pin counts in excess of 300 in packages with low lead inductance, capacitance, and resistance.

To respond to these demands, Fujitsu has developed a clever solution in packaging to obtain the highest average pin density per board area yet achieved. This is accomplished with surface mount PGAs, which rely on narrow pin pitch (50 and even 25 mils) in a dense grid of multiple rows of pins. Since through-hole packages cannot effectively support pin pitches narrower than 70 mils, these PGAs must be surface mounted, though they still possess pins (see Figure 8B-16).

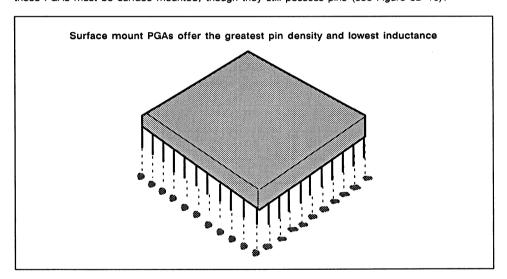


Figure 8B-16. Surface Mount PGA

The surface mount technology also permits traces to run beneath the package leads, increasing available trace density. Figure 8B-17 shows the solder pad design required by these high-pin-density packages.

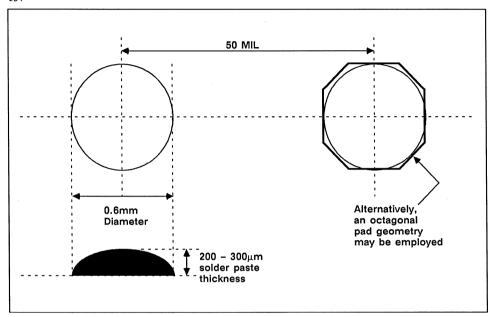


Figure 8B-17. Solder Pad Design for Surface Mount Pin Grid Arrays

The table in Figure 8B-18 provides an item-for-item comparison between PGAs, surface mount PGAs, and flatpacks of similar pin counts.

PACKAGE	TYPE	PIN PITCH	OUTLINE (MAX)	PIN DENSITY (Pins Per Sq. Inch)
FPT - 160	Surface	25 mil	1.276" x 1.276" (1.63 sq ln)	98
PGA - 256	Through	100 mil	2" x 2" (4 sq ln)	64
PGA - 256	Surface	50 mil	1" x 1" (1 sq ln)	256
PGA - 321	Staggered	71 mil	1.72" x 1.72" (2,96 sq ln)	109
PGA - 401	Staggered	71 mil	1.922" x 1.922" (3.69 sq ln)	109

Figure 8B-18. Comparison of Critical Features

The numerous electrical and mechanical advantages of surface-mount PGAs would seem to out-weigh their disadvantages. However, the general state of high volume manufacturing has not kept pace with the rapid advances in semiconductor packaging. This is partly due to the requirement for state-of-the-art manufacturing equipment, which is quite expensive, and also to the need to maintain board yields with such complex devices. Therefore, in order to establish these packages as an attractive alternative, Fujitsu has instituted a program with which to assist customers in the mounting and inspecting of these highly complex packages.

#### 3.3 A Comparison of Through-hole and Surface Mount Devices

SMDs provide improved electrical performance and reduced system size and costs. Furthermore, with plastic flatpacks of up to 160 pins and beyond available, SMDs show promise in supporting the rapidly advancing gate size complexities and high pin count of today's ASIC products at a substantially lower cost than the large ceramic PGAs. However, as the manufacturing complexities that have just been reviewed indicate, surface mounting large ASIC devices may be difficult and risky, and the designer should be cautious in their use.

If board space constraints are not critical, if the economic impact of scaling down the end system is not great, if optimal electrical characteristics in packaging are not a critical concern, then through-hole packaging may be the best solution. On the other hand, if speed and integration requirements dictate the use of very dense gate arrays, PGAs or SMT PGAs provide both through-hole and surface mount alternatives.

#### 3.3.1 Socketing Surface Mount Devices

Some benefits of SMDs are available to manufacturers employing through-hole packages through the use of sockets for SMDs. Sockets are available for QFPTs, SOPs (small outline packages), CLCCs and PLCCs; however, the use of QFPT and SOP sockets is normally restricted to prototyping and burn-in, while low-cost, reliable production sockets are more commonly available for PLCCs and CLCCs. These production sockets house the SMD (they are tightly tailored to the specific package) in one of two ways. Flatpacks and LCCs use low/zero insertion force with a lid that closes down on the package. PLCCs use pressured socket contacts that drive a pin into the underside of the socket. Socket pins are arranged like those of PGAs: they are through-hole, they have 100-mil spacing (generally), and they are most commonly oriented in a grid of two rows.

One advantage of these sockets is that in applications where through-hole packaging is required and the choice of through-hole packages is limited to PGAs, a plastic SM package plus the production socket will cost less than the through-hole PGA. The scenario typically occurs when the required number of pins is between 40 and 84 for PLCCs and LCCs and up to 160 or more for the flatpacks.

Another significant reason to socket SMDs results from the manufacturing difficulties of SMDs that were presented earlier. ASIC devices are usually among the largest in the system, and the most vital and expensive. For the purpose of field maintenance, many companies feel it is more economical and reliable not to risk running an ASIC device through wave or reflow solder and risking stress fractures or other damage. Furthermore, the test probing difficulties alluded to earlier are alleviated with sockets, which usually provide easy access to the contacts. Often, once reliability of the system is proven, the boards are re-laid out with surface mount devices. Therefore, simply because a manufacturing facility isn't geared up for SMT does not mean that SMT devices cannot be used there.

#### 3.3.2 Noise Problems With Sockets

Sockets for SMDs are convenient for manufacturers not yet ready to go to SMT, or for initial prototyping where the device may frequently be removed. Socketing permits the user to gain many of the benefits of SMDs, such as reduced profile and support of high pin counts in plastic, while avoiding the drawbacks, such as special manufacturing equipment and lead probing difficulties. Unfortunately a major electrical advantage of SMDs, low pin inductance, is compromised when sockets are used. The primary result is greatly increased noise, which, adversely affects overall speed and signal quality. In fact, a socketed SMD generally has a higher lead inductance then an equivalent through-hole PGA.

#### 3.4 Summary of the Packaging Alternatives

Having reviewed the package selection alternatives presented in Section 2.0 and the various tradeoffs between the packages discussed in this section and summarized in the table in Figure 8B-19 below, the designer can weigh the benefits and limitations of the various packages and arrive at an optimal packaging scheme.

# PINS: Pin Pitch: Body Length: Body Width:  # PINS: Pin Pitch: Body Length: Outline Width:  # PINS: Pin Pitch: Body Width:	.300" to .700"  16 to 28 10 mils 50 to 70 mils .300" to .400"	R: Medium L: High C: Low R: Medium L: Medium C: Low	Ceramic/Plastic θJA <sup>2</sup> : 70 - 40/ 120 - 80 Ceramic/Plastic θJA: 110 - 80/ 130 - 105	Up to 17K gates Up to 6500 gates	1
Pin Pitch: Body Length: Outline Width:  # PINS: Pin Pitch:	10 mils 50 to 70 mils .300" to .400"	L: Medium C: Low R: Medium	θJA: 110 - 80/ 130 - 105		1
Pin Pitch:	10 mils				
	.65" to 1.7"	L: Medium C: Low	θJA: 95 - 60	Up to 17K gates	1
# PINS: Pin Pitch: Body Width:	28 to 84 40 to 50 mils .45" to .97"	R: Medium L: Medium C:Medium	Ceramic θJA: 70 -45	Up to 25K gates	5
# PINS: Pin Pitch: Body Width:	28 to 84 50 mils .49" to 1.19"	R: Medium L: Medium C: Low	Plastic θJA <sup>2</sup> : 65 - 50	Up to 17K gates	1.05
# PINS: Pin Pitch: Body Width:	64 to 299 .100 mlls, 70 mlls 1.033" to 1.7"	Ceramic/Plastic R: Low Low L: Low Low C: High Low	Ceramic/Plastic θJA: 40 - 19/ 46 - 38	Up to 75K gates	Ceramic/Plastic
i	Pin Pitch: Body Width:  # PINS: Pin Pitch: Body Width:  # PINS: Pin Pitch: Body Width:	# PINS: 28 to 84 Pin Pitch: 50 mils Body Width: .45" to .97"  # PINS: 28 to 84 Pin Pitch: 50 mils Body Width: .49" to 1.19"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"	# PINS: 28 to 84 Pin Pitch: 50 mils Body Width: .45" to .97"  # PINS: 28 to 84 Pin Pitch: 50 mils Body Width: .49" to 1.19"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # Ceramic/Plastic R: Low Low L: Low Low C: High Low	# PINS: 28 to 84	# PINS: 28 to 84 Pin Pitch: 40 to 50 mils Body Width: .45" to .97"  # PINS: 28 to 84 Pin Pitch: 50 mils Body Width: .49" to 1.19"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"  # PINS: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: .100 mils

Figure 8B-19. ASIC CMOS Package Types and their Characteristics

<sup>(2)</sup> R = Resistance, L = Inductance, C = Capacitance (3) Utilizable gates

#### 4.0 Electrical Considerations for the Assignment of Signal, Power, and Ground Pins

Driven by the continual demand for high speed systems, CMOS ASICs are now being developed that exhibit output drive levels, rise and fall times, and propagation delays comparable to yesterday's ECL circuits. Consequently, the problems intrinsic to ECL design (even thermal management) are now appearing in CMOS designs. These problems, based on noise and its effect on the device, are introduced in this section and possible solutions are discussed.

#### 4.1 Sources and Magnitude of Noise

CMOS circuits operate by charging and discharging node capacitances through pull-up or pull-down transistor networks constructed of P channel and N channel enhancement mode (normally off) MOSFET transistors. As a result, these circuits generate noise when switching. The following review of basic CMOS circuits and how they work explains this phenomenon in greater depth.

#### 4.1.1 Basic CMOS Circuits

Figure 8B-20 shows a CMOS totem pole output buffer, the typical implementation for CMOS circuits, while Figure 8B-21 illustrates a CMOS-compatible input buffer, and Figure 8B-22 depicts a CMOS input buffer configured to be TTL compatible.

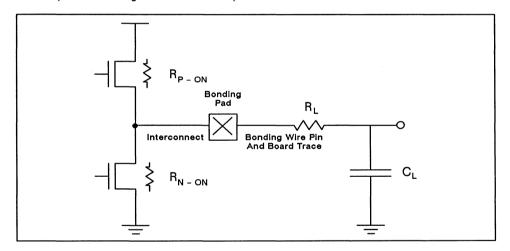


Figure 8B-20. CMOS Output Buffer Model (Totem Pole)

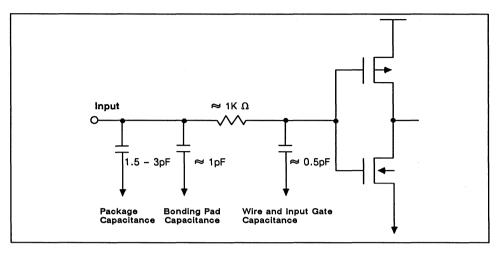


Figure 8B-21. I/O Model, CMOS Input

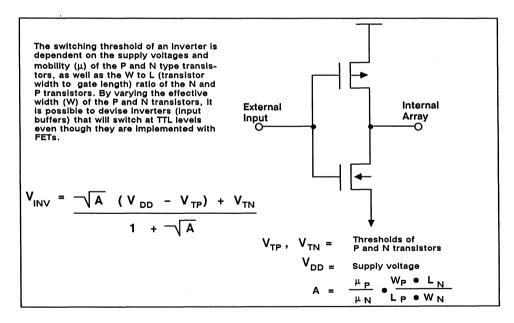


Figure 8B-22. I/O Model, TTL Input

Internal CMOS circuits, such as the NAND gate shown in Figure 8B-23 are typical of CMOS logic designs, which can be represented as a pull-up network and a pull-down network, each with its own logic and analog characteristics.

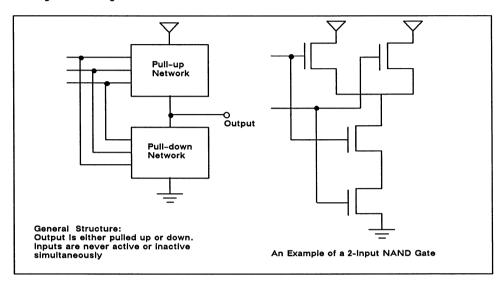


Figure 8B-23. CMOS Basic Gate Structure: The Pull-up/Pull-down Network

The other type of element used in CMOS circuits is the transmission gate, or T-gate, which is useful for the efficient construction of multiplexers and sequential circuits (D-flops, latches, etc.) as shown in Figure 8B-24.

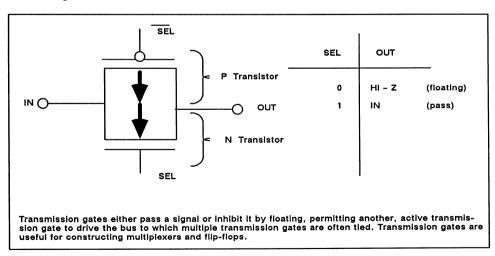


Figure 8B-24. CMOS Basic Gate Structure: The Transmission Gate

#### 4.1.2 Output Switching Noise and Simultaneous Switching Outputs (SSOs)

The greatest source of noise in a CMOS circuit is the result of an output switching either high to low or low to high, particularly into or out of a high capacitive load. CMOS outputs drive two types of loads, either CMOS loads, which are high in capacitance (C) but low in leakage current, or TTL loads, which are lower in capacitance but higher in leakage current. Therefore, the AC and DC currents that the buffers see when they switch depend greatly on the type of driven load and its capacitance. When this load discharges through the N-type transistor of the totem pole output, as illustrated in Figure 8B-22, the effect is that of a capacitor discharging through resistance (R). Consequently, the initial current is high and decreases over time as the output node capacitance becomes charged. Similar currents may be observed when charging the node capacitance, as in the case of a low-to-high transition.

Figure 8B-25 shows the characteristic resistance and capacitance of various parts of the output of an ASIC device.

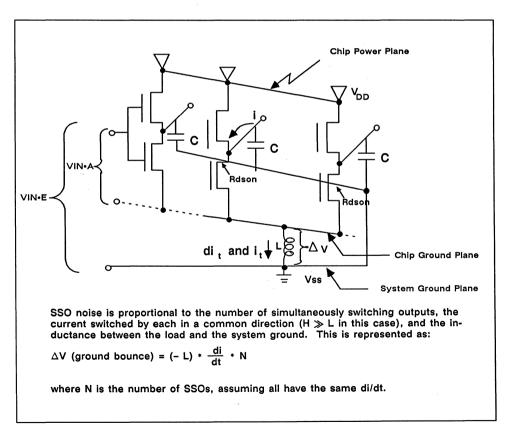


Figure 8B-25. Electrical Model of Simultaneously Switching Outputs

Although small, the total inductance becomes a critical factor when discharging or charging output capacitance, since the instantaneous current (i) is high. Recall that the self-induced voltage in an inductance. (L) is expressed by:

$$\Delta VINDUCED = \frac{L * dl}{dt}$$

where t is time and d is rate of change.

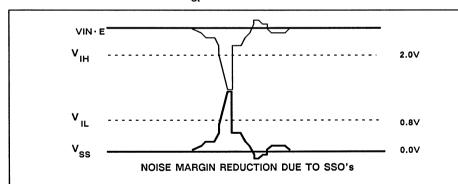
In a high-drive CMOS device driving high loads, such as 200pF, through a voltage swing approaching 5 volts with a rise/fall time of < 2ns, the instantaneous current may be:

i = C \* 
$$\frac{dv}{dt} \approx C * \frac{\Delta v}{\Delta t}$$
 (average over rise and fall time)

This induced voltage appears as noise on the receiving end of the signal as referenced to the ground. The current on a high-to-low transition is sunk into ground, causing the current to "bounce" or rise relative to other signals referenced to it. This ground bounce phenomenon may also apply to power on low-to-high transitions, yielding a similar noise problem.

Noise on signals may cause false triggering on the input buffer(s) being driven, or at least create a window of ambiguity in the time at which the driven input should switch (see Figure 8B-26). Therefore, noise may result in degradation in speed resulting from adding settling time to a delay and may even result in functional effects if false triggering occurs. Furthermore, if N multiple outputs under this condition switch simultaneously, the induced voltage is increased as a multiple of the number of outputs:

$$\Delta V = N * L * \frac{di}{dt}$$



- In this example, outputs switching H ≫ L result in a ground bounce or rise in the chip ground relative to system ground.
- The rise appears as if the input signal voltage levels are reduced proportionally.
   If the bounce is too great, the input voltage is below Vih causing false triggering.
- In the L ≫ H case, it is the low input levels (V<sub>IL</sub>) that are affected.

Figure 8B-26. Effect of SSO Noise on Thresholds

Not only inductance but also characteristic resistance can create noise problems. The following paragraphs summarize the types of noise that exist in CMOS systems and explain how packaging impacts this noise.

#### 4.1.3 Self-Induced Noise

Self-induced noise results when high-speed, high-drive outputs switch and introduce a spike on the signal relative to ground. The SSO effect, discussed above, is an example of the level of self-induced noise that can occur. It is predicted by:

$$\Delta VSI = L \frac{\Delta i}{\Delta t}$$

where L is the inductance between the pin and ground as well as the trace inductance.  $\Delta i$  is the instantaneous current and  $\Delta t$  is the fall/rise time.

#### 4.1.4 Mutually Induced Noise

A form of crosstalk, this noise occurs when a signal trace running parallel to another for some distance switches, inducing a voltage into the adjacent wire. Since both inductive and capacitive coupling occur only during signal transition and propagation, the effect is additive, as the signal propagates down the trace. Resultant noise propagates in both the forward and backward directions down the line. The forward crosstalk has a pulse duration equal to the rise and fall of the signal, with an amplitude equal to the difference between the capacitive and inductive coupling. Backward crosstalk has a pulse duration equal to the transition time down the trace and an amplitude dependent on the sum of the inductive and capacitive coupling as well as the trace length.

#### 4.1.5 Capacitive Coupled Noise

Another form of crosstalk resulting from mutual signal coupling, this noise occurs in proportion to the dielectric constant of the board, the distance of trace separation, and the trace length and width. Acting as two thin parallel plates, these traces couple switching current as integrated over time.

#### 4.1.6 Ringing on Signals

From basic circuit theory, the designer will recall that if the signal line impedance does not match the output impedance of the buffer, then the signal is not naturally dampened. If the impedance of the load is less than that of the buffer, the signal is over-damped and will have a slow rise/fall time. However, if the buffer possesses lower impedance, then the signal is under-damped and may ring, as illustrated by Figure 8B-4 of Section 2. Typically, signal line impedances are in the range of 50 to 250 ohms, while in the past buffers possessed "on" resistances of 500 ohms to 2 Kohms. However, due to the need for higher current sourcing/sinking and faster switching speeds, "on" resistances of output buffers have come down to the 10- to 50-ohm range, requiring the use of special termination techniques, discussed in the Fujitsu Application Note "Interfacing CMOS and BiCMOS VLSIs."

#### 4.1.7 iR Drop

Up to this point, the sources of noise discussed have depended on inductance or capacitance. The familiar voltage drop across a resistor as current passes through it is also a source of noise, since the DC current that a ground pin may sink, or that a power supply pin may source can be significant. This iR drop is the phenomenon that a limits the sum of source and sink currents through power and ground pins respectively. Ohm's Law describes the effect of this noise source, as expressed in the equation below where:

R is the output pin-to-ground (sink) resistance or power pin return-loop (source) resistance (including the "on" resistance of the respective N or P channel device) and

in is the current through the nth output pin connected to this common ground or power pin.

Given these parameters, the voltage rise or drop due to iR effects is:

$$\Delta V = R + \sum_{n=0}^{N-1} i_n$$

#### 4.1.8 Current Spiking or "Crowbar Noise"

As Figure 8B-22 illustrated, a CMOS output buffer is constructed as totem pole in which the output is taken from the common source (P type) and drain (N type) with the drain of the P type connected to power and the source of the N type connected to ground. When the input to the totem pole, or the P and N gates, switch, the Miller capacitance of the gate causes the gates to charge or discharge at some specified time constant. It is possible that both transistors can be on, one in saturation and the other passing through the linear region, creating a current path between power and ground that can damage the device. This is less a concern for internal transistors than it is for the "beefy" transistors at the I/O. This current spiking can not only introduce noise on the power and ground planes, but may damage the device as well. For this reason, Fujitsu has taken precautions in the design of the CMOS output buffers to prevent this problem from occurring.

#### 4.2 Recommended Strategy for Pin Assignment

The assignment of Clock, Scan, and other signals, as well as power and ground, to specific pins on the package affects electrical behavior (speed, noise, reliability, etc.), board manufacturing requirements, and device reliability. Therefore, optimal pin assignment strategies should consider the variables over which the user has control (placement of non-scan inputs, outputs and bi-directionals) and the variables over which the vendor has control (power, ground and scan signal placement). Out of these relationships a method of placement can be developed, using the following approach:

- a) Prioritize the signals whose placement is most critical.
- Establish guidelines for the location of these signals, both in absolute position and relative to other signals.

#### 4.2.1 Prioritization of Signals for Placement

Noise minimization is used to establish signal prioritization. All of the various forms of noise discussed in the last section are dependent on either i or di/dt, and L, M, R, or C. The signals affect i and di/dt, while the package pin location affects L, R and C. Figure 8B-27 provides an illustration of how electrical characteristics vary by pin position.

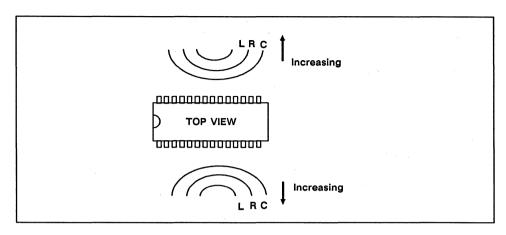


Figure 8B-27. Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position

In general, the further a pin's external contact is from the die connection, the greater its resistance, impedance, and capacitance. Therefore, signal prioritization is established according to current or its time derivative, while location is guided by package pin characteristics. Input signals are classified by their noise sensitivity. If a spike on an input could be disastrous (as with a clock), that signal should be carefully located. Figure 8B-28 classifies signal type by electrical characteristics.

Signal Type	Current Characteristics (General)						
Ground	Highest i, DC and di/dt						
Power	High i, DC and di/dt						
High drive outputs	High di/dt						
Clocks	Highest noise sensitivity						
Low drive outputs	Large di/dt						
Other Signals							

Figure 8B-28. Electrical Characteristics of Each Signal Type

#### 4.2.2 Characteristics of Package Pins by Location

The inductance, capacitance, and resistance, all of which are critical to minimizing noise, are related not only to board construction, but also to the pin position on given packages, and the circuit to which the pins are bonded. The pin, lead frame, bonding wires, pads and buffer (input, output or bi-directional) all influence the characteristic L, R, and C of the line. See Figure 8B-29.

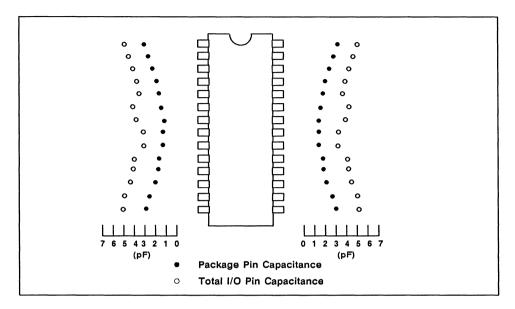


Figure 8B-29. Measured Pin Capacitance by Package Position

#### 4.2.3 Relating Signal Type to Package Location

Since power and ground pins demand a large DC current (i), iR drops are the greatest concern, and so Fujitsu assigns power and ground to pins with the minimum resistance (and inductance as well). High-drive outputs exhibit a large di/dt, resulting from high capacitive loading, on power or high-power outputs. Since L di/dt and M di/dt noise is their greatest enemy, the best pins for these signals are those of minimum inductance. Furthermore, adjacent pins possess the greatest M, and thus couple the most M di/dt noise. This means that noise-sensitive inputs, such as clocks, should be isolated from signals with a high di/dt, namely high-drive outputs.

#### 4.2.4 Minimizing iR Drops on Power and Ground Pins

Since noise on ground affects the voltage level of all signals referenced to it, placement of the ground pins is most critical. For this reason, Fujitsu has preassigned the power (Vdd) and ground (Vss) signals for all packages in a given gate array family according to the electrically optimal locations. Fujitsu also took into consideration manufacturing issues such as adjacent pin shorting due to probes and package rotation. Preassigning power pins also permits Fujitsu to develop load boards (which interface the packaged device to the tester) advanced enough to carry out high-speed functional testing of devices with high I/O count and to drive devices with relatively low noise. The predefined power and ground assignments for Fujitsu devices are found in the Package Pin Assignment Guide in the Design Manual for the appropriate gate array family, and are used in conjunction with the Package Matrix to determine pin assignment.

#### 4.2.5 Minimizing the Self-Inductance of a Signal

Fujitsu believes that an ASIC designer concerned about designing a mini-computer, PC, main-frame or other complex system should not have to be concerned with determining specific on-chip noise issues, particularly since board-level noise issues are demanding enough. Therefore, Fujitsu

developed a straightforward grouping scheme for the placement of various types of signals relative to their distance from the nearest power and ground pins. As Figure 8B-30 shows, the self-inductance associated with a given signal is a function of the length of wire between it and its nearest ground (for a falling transition) or power (for a rising transition).

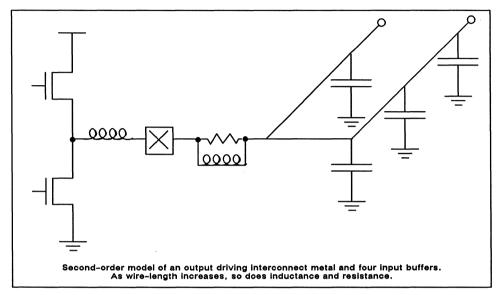


Figure 8B-30. Self-inductance in a Circuit

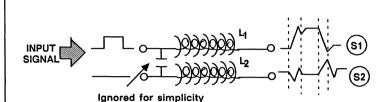
Since di/dt can vary greatly for outputs within a group, there are some general restrictions relating simultaneously switching outputs (SSOs) and their total current to the number of grounds on the chip. This is done by summing representative values like those shown in the UHB Data Sheet, which are weighed depending on the IOL of the given output buffer. Notice that, if the output buffer employs noise limiting circuitry (edge rate grading) then di/dt is less and the representative value is also less, meaning more of these outputs can be supported per ground pin.

In summary, to ensure that the iR drops and the ground bounce effect (L di/dt) are within reasonable limitations, Fujitsu has established guidelines for determining the number of necessary grounds and defining the pinout.

#### 4.2.6 Placement of Clocks and Asynchronous Clear/Presets

In addition to causing the ground bounce and iR drops that can deteriorate an output signal's quality and alter the ground reference, output switching can also couple noise into adjacent sensitive inputs by mutual inductance, as shown in Figure 8B-31. For that reason, the designer should ensure that clocks and asynchronous clear and preset signals are not placed near outputs, particularly high drive outputs. To further isolate inputs from noise, the designer should minimize the inductance (length) of the return loop from the input buffer to ground by placing this type of input near a ground pin. The mutual inductance of the input buffer itself can be minimized if it, and any outputs nearby, are not assigned to high inductance pins. As discussed in Section 4.2.1, the center pins of a DIP, flatpack, or PLCC possess the lowest L and R, as do the inner rows of PGAs,

making them most suitable for Vdd, Vss and high drive outputs. But the edges of the package, while suitable for data signals, should be avoided when placing clocks and other sensitive signals, as they exhibit a high mutual inductance and large iR drop.



Noise is introduced on the adjacent lead S2 as S1 is driven in a manner described by Michael Faraday as:

$$V_{S2} = -M \frac{di_{S1}}{dt}$$

where M is the mutual inductance between the adjacent leads.

If S2 is also being driven, then the mutually induced noise is superimposed on the self induced noise already present, as described by:

$$V_{S2} = -M \frac{di_{S1}}{dt} + L_2 \frac{di_{S2}}{dt}$$

Figure 8B-31. Crosstalk and What Promotes It.

#### 4.3 Summary: Choosing the Package and Assigning the Pins

This discussion of noise as related to packaging and its effect on pinout should help the designer appreciate the care Fujitsu has taken to ensure that noise margins within the device are restricted to maximize system reliability. It should also provide the designer with a basis for establishing optimum pin assignments. This section will now conclude with a step-by-step procedure to choose an optimal package, and assign pins to it.

#### 4.4 Package Selection Checklist

When selecting the package for an ASIC device, the designer should consider the following points:

- Define a subset of the Fujitsu packages that can be supported by your company's manufacturing capabilities.
- 2. Estimate, as closely as possible, the gate and I/O counts of the circuit(s).
- 3. Determine the number of power and ground pins required by considering the following:
  - a) Representative value limitations for SSOs.
  - b) Limitation of the sum of the sink current (IOL) per ground pin.
  - Limitation of instantaneous current per ground pin to satisfy metal migration restrictions.

- Using the package and pin assignment section of the Design Manual, determine the packages that satisfy the signal, power, and ground pin requirements of the circuit.
- Make sure that the electrical, mechanical, and thermal properties of the chosen packages are suitable for the application.
- 6. Check the mechanical dimensions in Fujitsu's ASIC Package Catalog and the power and ground pin assignment tables and grouping charts in the appropriate package and pin assignment tables for the chosen technology. Please contact Fujitsu regarding pricing trade-offs when evaluating packages or partitioning the system.

#### 4.5 Pin Assignment Checklist

- Follow Fujitsu's pin assignments in the Package and Pin Assignment section of the Design Manuals. Although multiple pinouts of the same package may be offered in some cases, all power and ground signals indicated on the chosen package must be connected on the board.
- Assign input pins (in excess of 5 MHz) and high power output buffers (IOL = 24mA) according to the appropriate pin assignment table.
- Place all high-drive (power and high power) outputs near ground pins; the higher the drive, the closer they should be placed. SSOs should be placed particularly close to ground pins.
- 4. Place SSOs in groups belonging to given ground pins.
- 5. Distance noise-sensitive signals such as clocks and asynchronous clears and presets away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near a ground, if one is available away from SSOs or highdrive outputs.
- Place SSOs on low inductance pins, such as those located on the inner rows and middle position of the PGAs.

Following these guidelines should assist the designer in choosing the best package for the application, one that results in a device with reliable and predictable electrical performance and without harmful DC and AC effects on the system. There are other system interface issues such as device decoupling and termination that should be considered during design. These are discussed in Fujitsu's application note "Interfacing CMOS and BiCMOS VLSIs."

#### 5.0 Thermal Issues in CMOS ASIC Packaging

CMOS has traditionally been associated with low power, one of the classic advantages it has over ECL. While ECL continually draws high current to supply its internal differential amplifiers and emitter-follower circuits, CMOS draws current primarily when it is switching. The total power dissipation of a CMOS device is dependent on the number of gates, the switching frequency, and the loading on the output of the gates. The revolution in CMOS technology that has resulted in gate densities of 100K gates has been accompanied by increases in all of these factors influencing power dissipation. Prior to 1985, when Fujitsu introduced the world's first 20,000 gate array, the C20000UH, CMOS gate arrays were not of sufficient integration density to warrant concerns about thermal control. But advancing CMOS technologies have forced this issue to the surface.

Power dissipation is important in defining the necessary power supply currents, since power is the product of current and voltage. However, the propagation delays and the reliability of a device are also dependent on the temperature at which the die operates, as discussed in Sections 2.2.3 and 2.3.4. To ensure that speed and reliability requirements are satisfied, it is necessary to estimate

the power dissipation of the device and, from this information, choose appropriate packages and system cooling techniques.

#### 5.1 Estimation of Power Dissipation in CMOS Circuits

There are two constituent factors in the power dissipation of a semiconductor device: the DC power, which is dependent on the steady-state (quiescent) current, and the AC or dynamic power.

#### 5.1.1 Estimation of Dynamic (AC) Power Dissipation

CMOS circuits are constructed of FETs, which possess very small leakage currents. Therefore, CMOS possesses a low quiescent or steady-state current. CMOS dissipates power primarily while it is charging or discharging node capacitance, or drawing switching current, which occurs as a gate changes state. This can be modeled as the familiar pull-up/pull-down circuit discussed in Section 4.1, charging and discharging a node capacitance, CL (shown in Figure 8B-25). This model holds true whether the node is internal or off-chip.

The switching current is a result of charging and discharging the node capacitance which, for periodic signals, occurs twice a cycle: once while charging the capacitance, and once while discharging it. The energy involved in charging or discharging a capacitance is  $1/2(CL * V^2)$ . The power is the energy divided by the period of time between successive changes (the clock period, T), multiplied by the two transitions that occur per cycle. Therefore, the dynamic or switching current of a CMOS circuit is defined as:

$$Pd-dyn = 2 * \frac{(CL * V^2)}{2 * T} = (CL * V^2) * f$$

where V is the supply voltage and f is the frequency of the given signal.

This is the power calculation for a single gate. The power dissipation for entire chip, however is much more complicated, since not all gates are simultaneously active. The degree of switching activity varies greatly within a circuit and depends on the nature of the circuits (synchronous sequential gates tend to switch concurrently, while combinational gates switch more randomly), the input stimulus (whether the circuit is stimulated at a periodic interval or asynchronously) and other design-dependent issues. Based on Fujitsu's experience, gate activity is on the average about 20%. This same figure is applied to the power estimation for output and input buffers.

#### 5.1.2 Estimation of Quiescent (DC) Power Dissipation

There are two sources/sinks of DC current in a CMOS ASIC: the leakage current of the gates (gate leakage) and the DC current that flows through output and bidirectional buffers in output mode. The gate leakage in CMOS devices, even dense ones, is in the range of tens of microamperes, and is negligible. The DC current of the output buffers is the current that the buffer sources or sinks in steady state. This current level depends on the leakage currents of the driven loads, but for simplicity will be assumed to be equivalent to the IOL and IOH rating of the buffers. The DC power can be estimated for each output buffer by analyzing:

- the product of source current times the voltage difference from the power rail (Vdd-VOH), and
- (2) the sink current times the low-level voltage (VOL).

This calculation is valid provided the duty cycle, or the portion of the cycle that the output is low versus the portion of the cycle that the output is high, weighs the sum of the two components. The total DC power may be determined by extending this method to each output and bidirectional buffer.

#### 5.1.3 Estimation of Total Power Dissipation

The total power dissipation of a circuit is the sum of the DC and AC components. I/O buffers dissipate both DC and AC power when switching, while internal gates may be considered for the sake of simplicity, to dissipate only AC. The theory behind CMOS power dissipation is simple; however, the task of calculating the power dissipation can be tedious and prone to error. Therefore, Fujitsu has devised methods for estimating the power dissipation for each CMOS technology. These methods are presented in the Design Manual for the appropriate technology, available through the Field Applications Engineers at local Fujitsu Sales Offices or Technical Resource Centers.

#### 5.2 The Relationship Between Power Dissipation and Temperature

A device draws current through the power supply pins and the I/O buffers. As it does so, it dissipates thermal energy proportional to the power dissipated in the device. Assuming that the power dissipation of a device has been estimated as Pd, using the method described in Section 5.1.1, how can one relate this power to the temperature of the die and the package, and also determine the warming effect on the surrounding environment?

The answer lies with two principles of heat transfer: conduction and convection. When an object is in a state of thermal equilibrium it is isothermal, seeing a constant temperature across its body. As the temperature of one end of the object is raised by the introduction of energy, it is no longer in equilibrium; heat begins to flow from the warmer region to the cooler region through the process of conduction.

When a lake in winter is filled with water at a constant temperature, just above 32°F, it may still freeze. It will freeze at the surface, however, not the bottom. This is because heat is drawn from the water into the air through convection, the act of cooling by a gas.

These same mechanisms, conduction and convection, act upon a packaged semiconductor device and determine its junction temperature, the package or case temperature, and the warming effect on the surroundings.

#### 5.2.1 Determining the Junction Temperature of a Device

Figure 8B-32 shows the paths through which heat flows in a packaged device. Each interface of materials with different properties of thermal conduction must be considered when determining the flow of heat from the die to the surroundings. The back side of the die is attached to a lead frame or slug, usually by means of a eutectic bond (material heat bonded with some conductive material, such as silver). Heat flows through this path from the die to the package, then from the package to the surrounding air.

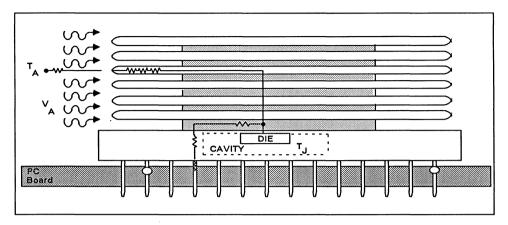


Figure 8B-32. Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink

From the die junction to the package, there is some associated thermal impedance (or resistance to the flow of heat). This impedance can be calculated, but may also be estimated in the following way. Operate a device and determine its power dissipation. Then, using some mechanism such as a thermal diode, whose forward bias voltage tracks linearly with temperature, determine the junction temperature. Then, after measuring the case temperature, determine the thermal impedance along the path from the die junction to the case (package body) using the following equation:

$$\Theta jc = \frac{(Tc - Tj)}{Pd}$$

where To and Tj are the case and junction temperatures, respectively.

A similar procedure is followed when determining the thermal impedance between the junction and the ambient environment, except that the case temperature is replaced by the measurement of the ambient temperature:

$$\Theta ja = \frac{(Ta - Tj)}{Pd}$$

While  $\Theta$  ic relies on conduction as its cooling mechanism,  $\Theta$  ia reflects convective cooling. Therefore,  $\Theta$  ia varies with airflow and is specified at a given airflow, or as static (= 0).

Since thermal impedance depends on the heat conduction path between the die and some other interface, it can be modeled the same way as current flowing through real impedance or resistance. Therefore, as in circuit theory, when multiple interfaces are oriented in parallel, the thermal impedance is lowered. However, the situation is different from circuit theory in that when a very low impedance interface such as a heat sink is placed in the conduction path the flow capacity is increased, with the heat sink pulling heat out at a faster rate, lowering the thermal impedance.

#### 5.2.2 Using Thermal Impedance Data

Thermal impedance information and power dissipation information are used to estimate junction temperature and ambient temperature rise. Which impedance figure to use is based on how the

device is to be cooled. If the device is air cooled (convective), then  $\Theta$ ja should be applied, while  $\Theta$ jc should be used if conductive techniques such as heat pipes or cold plates are employed. For example, the junction temperature may be obtained by multiplying the power dissipation of the device by the appropriate  $\Theta$ ja and adding the ambient temperature. It is not surprising that this indicates that a small thermal impedance is desirable to achieve a low junction temperature.

Junction temperature is used to determine worst case delay multipliers and the package options for Fujitsu's CMOS AU (Sea-of-Gates) family. The junction temperature also indicates whether reliability goals are being met. The designer can trade off packages (which exhibit varying thermal impedances) with cooling techniques (such as varying the amount of airflow in a system) to achieve the desired junction temperature and consequently, worst case delay multiplier and reliability targets.

#### 5.3 Summary of Thermal Issues

Although thermal considerations in CMOS have not previously been of great concern, since the frequency and density of the devices have not required such concern, current generations of CMOS devices are stimulating an awareness of these matters. This section has surveyed some of the issues involved in applying thermal analysis to CMOS devices and using the information gained from such analysis to determine the appropriate packaging and cooling techniques.

#### 6.0 Summary of the Note

As VLSI circuits increase in complexity, pin count and die size increase as well, placing greater demands on packaging, board layout, and manufacturing. Fujitsu has addressed these problems with more exotic forms of packaging such as the surface mount PGA and the staggered PGA, while also stressing the importance of other surface mount packages. But simply making these packages available is not sufficient; Fujitsu must also provide the support and information necessary to ensure that these packages can successfully be accommodated by our customers in an efficient manner. Field Applications support in the local sales offices, technical information such as this Application Note, and centralized package specialists at Fujitsu's San Jose headquarters have all been established to provide this support.

#### References

John C. Mather, "A Status Report on Multilayer Circuit Boards"; Proceedings, 30th Electronic Components Conference, 1980, pp 302-306.

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## Section 2

# UHB Series CMOS Gate Array Unit Cell Library

#### **Contents** 2-2 Unit Cell Specification Information 2-5 Inverter and Buffer Family 2-15 NAND Family 2-31 NOR Family 2-47 AND Family 2-53 **OR Family** 2-59 EXNOR/EXOR Family 2-69 AND-OR-Inverter Family 2-77 **OR-AND-Inverter Family** 2-85 Multiplexer Family 2-107 Clock Buffer Family Scan Flip-Flop (Positive Edge Type) Family 2-117 2-157 Non-Scan Flip-Flop Family 2-185 Binary Counter Family 2-217 Adder Family 2-225 Data Latch Family 2-243 Shift Register Family 2-255 Parity Generator/Selector/Decoder Family 2-283 **Bus Driver** 2-287 Clip Cells 2-293 I/O Buffer Family 2-403 Appendix A: General AC Specifications 2-405 Appendix B: Hierarchical Structure 2-407 Appendix C: Estimation Tables for Metal Loading 2-413 Appendix D: Available Package Types 2-415 Appendis E: TTL 7400 Function Conversion Table 2-419 Appendix F: Alphanumeric Index of Unit Cells

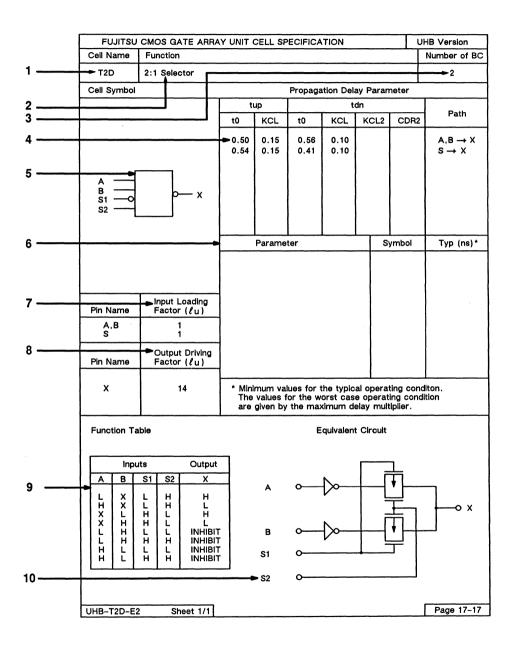
### **Unit Cell Specification Information**

This section contains specifications for all the unit cells available for the UHB Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors.

#### How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the UHB Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit cell name appears in the upper left corner of the page.
- 2. The unit cell function is given on the same line as the unit cell name.
- The number of basic cells (BC) or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t0) is given in ns. KCL, the delay constant for the cell (delay time per load unit) is given in ns/pF. KCL2 and CDR2 are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (CDR).
- 5. The cell (logic) symbol is shown in the top left box under the cell name.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
- 7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- The output drive factor is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function (truth) table, if applicable, is shown in a box at the lower left side of the page.
- 10. The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.



2

# Inverter and Buffer Family

	Unit Cell			Basic
Page	Name	Function		Cells
2-7	V1N	Inverter		1
2–8	V2B	Power Inverter		1
2-9	V1L	Double Power Inverter		2
2-10	B1N	True Buffer		1
2-11	BD3	True Delay Buffer	(> 5ns)	5
2-12	BD4	Delay Cell	(> 4ns)	4
2-13	BD5	Delay Cell	(>10ns)	9
2-14	BD6	Delay Cell	(>22ns)	17

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N N		l "UHI	B" Version
	Function			1011110	···		I N	Number of BC
V1N	Inverter							1
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		0.28	0.16	0.35	0.09	0.12	4	$A \rightarrow X$
								1
	\_							
Α —	>>─— х							
•								
								<u> </u>
		Parame	ter			S	ymbol	Typ(ns)*
						ł		
						1		
						- 1		
D: 11	Input Loading					-		
Pin Name	Factor (lu)					1		
A	1					- 1		
						1		
						-		
	Out Delete					1		
Din Nama	Output Driving							
Pin Name X	Factor (lu)							
Λ	10							
		* Mini	miim 1707	ues for	the tw	nical o	norati	ng condition.
		The	majnec	for the	worst	picai o	peratin	g condition
		370	values civen h	tor the m	aximum	dalaw m	ultinl	ier
	L	916	OTAGII D	, one m	~~~mum	actay m		
UHB-V1N-E1	Sheet 1/1							Page 1-1

FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U.	HB" Version Number of BC
V2B						***************************************		
Cell Symbol	Power Inverter		Prop	agation	Delay	Paramet	er	1
			up		td	n		
		t0 0.25	KCL 0.08	t0 0.25	0.05	KCL2 0.08	CDR2	Path A → X
		0.23	0.00	0.25	0.05	0.00	,	A
	,							
	4							
Α	x							
A	<b>A</b>							
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	2							
Pin Name	Output Driving Factor (lu)					ļ		
X	36							
		4 10 1	-		. 1			
		" Mini	mum vai values	ues for for the	tne ty worst	pical o case or	perat erati	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
UHB-V2B-E1	Sheet 1/1							Page 1-2

FILITSII	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		] WIII	HB" Version
Cell Name	Function	000	0.1001.	LIGHTIU				Number of BC
V1L	Inverting Clock	Buffer	n		D-1	D		2
Cell Symbol		+	up Prop	agation	Delay td	n n	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.35	0.04	0.67	0.03			A + X
								1
								1 1
Α	> х							
A	^ ^					l	İ	1 1
		Paran			l	l ,	ymbol	T::::()+
		Parame	rei			<del>-   °</del>	ушоот	Typ(ns)*
						1		
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						ł		
						1		
	Input Loading							
Pin Name	Factor (lu)					ł		
A	4					1		
	Output Driving							
Pin Name X	Factor (lu)							
Λ								
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	1	are	given b	y the m	aximum	delay m	ultip	lier.
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l								
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UHB-V1L-E2	Sheet 1/1							Page 1-3
		2.0						

FUJITSU Cell Name	CMOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N		וט" ו	HB" Niii	Version	n BC
B1N Cell Symbol	True Buffer		Prop	agation	Delay	Paramet	er		1	
			up		td	n		$\exists$		
		t0 0.58	KCL 0.16	t0 0.68	KCL 0.08	KCL2	CDR2	-	$\frac{\text{Path}}{\text{A} \rightarrow \text{X}}$	ζ
		0.50	0.10	0.00	0.00					-
Α	x									
								-		
								-		
								$\perp$	T (	74
		Parame	ter				ymbol	+	Typ(ns	s) <b>"</b>
						c				
	Input Loading					Ì		l		
Pin Name	Factor (lu)					İ				
A	1					l				
						İ		-		
	Output Driving									
Pin Name	Factor (lu)					-				
X	18									
		* Mini	mum val	ues for	the ty	pical c	perat	ing	condi	tion.
		The	values given b	for the	worst aximum	case op	erati:	ng lie	condit:	ion
		aro	STACH D	y che in	<u>uximum</u>	uciay n	штетр	110		
UHB-B1N-E1	Sheet 1/1								Page	1-4

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHB	" Version
Cell Name	Function						N	umber of BC
BD3	Delay Cell							5
Cell Symbol			Prop	agation	Delay :	Paramet -	er	
	!	t0	up KCL	t0	KCL	KCL2	CDR2	Path
		5.33	0.16	4.71	0.12	0.13	4	Path A → X
1								
Α —	<u> </u>							
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name A	Factor (lu)							
	_							
Pin Name	Output Driving Factor (lu)							
X	18							
		* Mini The	mum val values	ues for for the	the ty worst	pical o	perating erating	ng condition. g condition
	l	are	given b	y the m	aximum	delay m	ultipl	ier.
UHB-BD3-E1	Sheet 1/1							Page 1-5

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	IB" Version
Cell Name	Function							Number of BC
BD4	Delay Cell						I	4
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td		CDDO	-l l
		t0 3.56	KCL	t0 4.10	KCL	KCL2 0.36	CDR2	Path A → X
		3.30	0.57	4.10	0.31	0.30	4	A → A
	_							
Α	<b>→</b> x							
		Parame	ter			S	ymbol	Typ(ns)*
						- 1		į į
						ı		
						l		
	Input Loading					l		
Pin Name	Factor (lu)					- 1		
A	4					j		1
	'							
	!							
	Output Driving	1						
Pin Name	Factor (lu)							
X	6	<del> </del>						
		* Mini	mum val	ues for	the tu	nical o	nerati	ing condition.
		The	values	for the	worst	case or	erati	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
Hun nn/ no	Chart 1/1							Dana 1-6
UHB-BD4-E2	Sheet 1/1							Page 1-6

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" וו	HB" Version
Cell Name	Function							Number of BC
BD5	Delay Cell							9
Cell Symbol				agation	Delay	Paramet	er	
		t0 t	up KCL	t0	td KCL	n KCL2	CDR2	- Both
		10.92	0.16	10.35	0.10	0.15	4	Path A → X
A —	<b>&gt;</b> —x							
"	- "							
		Parame	ter			S	ymbol	Typ(ns)*
i								
	Input Loading					1		
Pin Name	Factor (lu)					ļ		
A	1							
						1		
	Output Driving							
Pin Name	Factor (lu)							
Х	18							
1		* Mini	mum val	ues for	the tv	nical c	perat	ing condition.
		The	values	for the	worst	case on	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.
UHB-BD5-E1	Sheet 1/1							Page 1-7

FUJITSU	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	v v		T"UH	B" Version
Cell Name	Function							Number of BC
,								
BD6	Delay Cell							17
Cell Symbol	- 5		Prop	agation			er	- <del></del>
			up		td			╣
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		22.00	0.17	21.82	0.09	0.14	4	A + X
								1
								1
Λ	x			. 1				
Α ——	^							
								1
		Parame	ter	L		S	ymbol	Typ(ns)*
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	*					ŀ		
						ł		1
						İ		
	Input Loading							
Pin Name	Factor (lu)							
A	1					1		
						}		
	Output Driving					1		
Pin Name	Factor (lu)					1		
Х	18							
			_	_				••••
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	urtipi	ier.
1								
UHB-BD6-E1	Sheet 1/1							Page 1-8

## **NAND Family**

Unit Cell Name	Function	Basic Cells
N2N	2-input NAND	1
N2B	Power 2-input NAND	3
N2K	Fast Power 2-input NAND	2
N3N	3-input NAND	2
N3B	Power 3-input NAND	3
N4N	4-input NAND	- 2
N4B	Power 4-input NAND	4
N6B	Power 6-input NAND	5
N8B	Power 8-input NAND	6
N9B	Power 9-input NAND	8
NCB	Power 12-input NAND	10
NGB	Power 16-input NAND	11
N3K	Fast Power 3-input NAND	3
N4K	Fast Power 4-input NAND	4
	Name N2N N2B N2K N3N N3B N4N N4B N6B N8B N9B NCB NGB N3K	Name Function  N2N 2-input NAND  N2B Power 2-input NAND  N2K Fast Power 2-input NAND  N3N 3-input NAND  N3B Power 3-input NAND  N4N 4-input NAND  N4B Power 4-input NAND  N6B Power 6-input NAND  N8B Power 8-input NAND  N9B Power 9-input NAND  NCB Power 12-input NAND  NGB Power 16-input NAND  NGB Power 3-input NAND  NGB Power 16-input NAND  NGB Power 3-input NAND

FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version Number of BC
N2N	2-input NAND							1
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.37	0.16	0.56	0.14			$A \rightarrow X$
								1
								1
A1 ——								
	] )> x						1	
A2								
		Parame	ter			I S	ymbol	Typ(ns)*
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								1
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	Input Loading							
Pin Name	Factor (lu)							1
A A	1					1		
A	1							
		}						
	10.1.1.					1		1
D4- M	Output Driving							
Pin Name	Factor (lu)							
Х	18							
			1		41 4			
		" mini	mum vai	ues for	the ty	picai c	perati	ng condition.
		Ine	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipi	ler.
UHB-N2N-E2	Shoot 1/1							Page 2-1
UNDENZINEEZ	1 311881 1/11							1 * 400

FILITAGILO	MOS GATE ARRAY U	NIT CET	I. SPECT	FICATIO	Ŋ		ппп	B" Version
Cell Name	Function	MII CEL	n orect	TOWITO	14		I OH	Number of BC
COLL Name	1 0110 0 1 0 11							TOURSEL OF BO
N2B	Power 2-input N	AND						3
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.10	0.08	1.42	0.04			A → X
								1
							i	
A1 ——								
A2 -	)> x							ĺ
AZ [								1
		Barrer	+			- T A	umb = 1	Tum (ma) th
		Parame	rer				ymbol	Typ(ns)*
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		]				- 1		
		1				ļ		1
						1		1
	Input Loading	1						
Pin Name	Factor (lu)	1						
A	1							
		l				1		
		l						
	Output Driving	ł						
Pin Name	Factor (lu)	ļ						
Pin Name X	Factor (lu)	1						
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
*		The	values	for the	worst	case or	eratir	ng condition
		are	given b	y the m	aximum	delay n	ultipl	ier.
UHB-N2B-E2	Sheet 1/1							Page 2-2

THITTEGH O	WOO O. W. A. A. A. A. A. A. A. A. A. A. A. A. A.	NITT OFF	CDECT	DICAMIC			11777	ml II
	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version Number of BC
CEIT NAME	r miccion						<del></del>	TIGHTHET OF DC
N2K	Power 2-input N	AND						2
Cell Symbol			Prop	agation	Delav	Paramet	er	-
		t	up		td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.37	0.08	0.43	0.07	0.09	7	A → X
								İ
A1 ——								
A2	р <u> —                                   </u>							
AZ						•		
	,							
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		Parame	ter			S	ymbol	Typ(ns)*
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n	Input Loading							
Pin Name	Factor (lu)							İ
A	2					1		
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		]				į.		
	Output Driving	ł				- 1		
Pin Name	Factor (lu)	l						
X X	36	ł						1
Α.	1	<del></del>	···········					_1
		* Mini	mum val	ues for	the ty	mical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	v the m	aximum	delay n	ultip	lier.
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IND NOV TO	Chart 1/1							Page 2-3
UHB-N2K-E2	Sheet 1/1							11050 23

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version
Cell Name	Function							Number of BC
N3N	3-input NAND							2
Cell Symbol				agation	Delay		ter	
	44		up		td		Lanna	
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
	,	0.52	0.16	0.69	0.19			A → A
								]
A1	<b>₽</b>							
A2	b x						1	
A3	$\cup$						1	]
							1	[ ]
						L		
		Parame	ter				Symbol	Typ(ns)*
						1		
						1		
						1		
<del></del>	Input Loading					İ		
Pin Name	Factor (lu)							
A	1							
						l		
	Output Driving							
Pin Name	Factor (lu)					.		
X	14							
		. يىرىد	1	6				tina aanditian
		" Mini	.wum val	ues IOI	. une ty	hicai	operat	ting condition. ing condition
		ine	varues given b	TOT THE	avimum	delaw	multi.	olier.
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UHB-N3N-E2	Sheet 1/1							Page 2-4

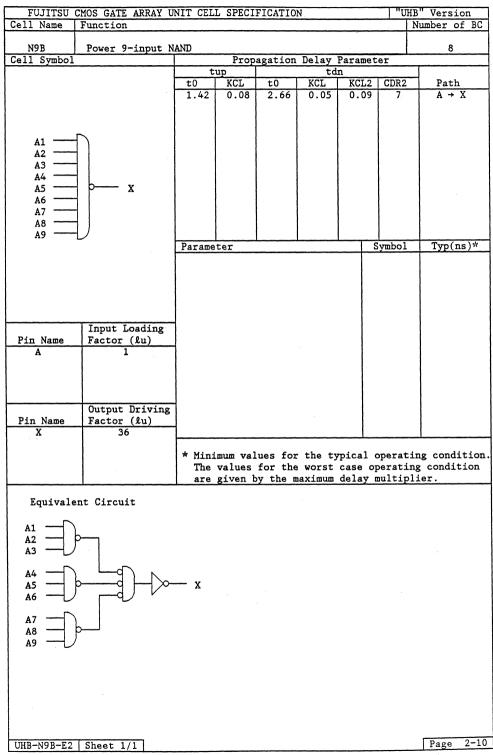
FILITSIL	MOS GATE ARRAY U	NIT CEL	T SDECT	アイクトでもつ	N		עודויי ו	B" Version
	Function	1111 051	L OFECT.	LICALIO	14		I Un	Number of BC
N3B Cell Symbol	Power 3-input N	AND	P===	agatic=	Dolar	Daramat		3
Cell Symbol		t.	up Prop	agation	Delay td		er	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.28	0.08	1.70	0.04			A -> X
.,								
A1 ————————————————————————————————————	р—— х							
A3	<i></i>							
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		Parame	ter	L	1	l s	ymbol	Typ(ns)*
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		]						
						- 1		
	Input Loading	1						
Pin Name	Factor (lu)							
A	1							
	<u> </u>	1						
Pin Name	Output Driving Factor (lu)							
X X	36	1						
					_			
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		are	values given h	or the m	worst maximum	delav m	eratii ultipl	ng condition lier.
	1	l are	021011	, 5116 11			<u></u>	
UHB-N3B-E2	Sheet 1/1							Page 2-5

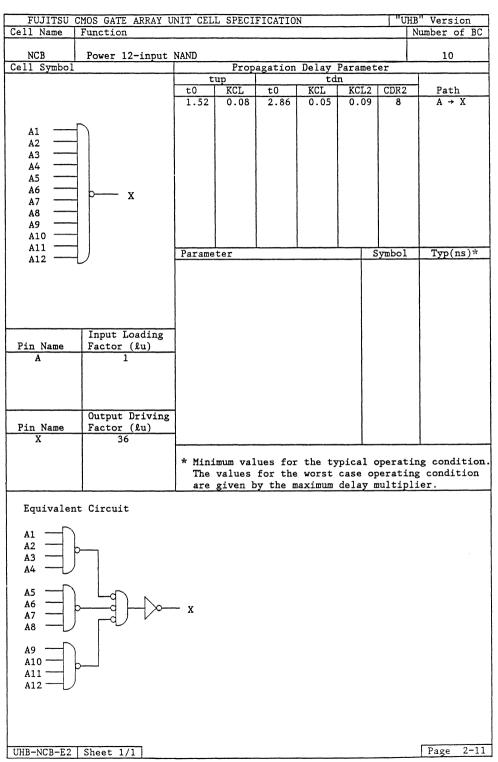
FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		יט" ו	HB" Version Number of BC
		<del></del>						
N4N Cell Symbol	4-input NAND		Prop	agation	Delav	Paramet	er	2
			ıp		td	n		
		t0 0.62	KCL 0.16	t0 0.74	KCL 0.24	KCL2	CDR2	Path A → X
		0.02	0.10	0.,-	0.24			
				İ				
	_							
A1 ————————————————————————————————————	] ]							
АЗ ——	р— х							
A4								
		Paramet	er			S	ymbol	Typ(ns)*
	Input Loading					į		
Pin Name	Factor (lu)					1		
A	1					1		
	Output Driving							
Pin Name X	Factor (lu)							
		# W:-:						
		The	num vai values	ues for for	tne ty worst	pical c case op	perat: erati:	ing condition. ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.
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UHB-N4N-E2	Sheet 1/1							Page 2-6

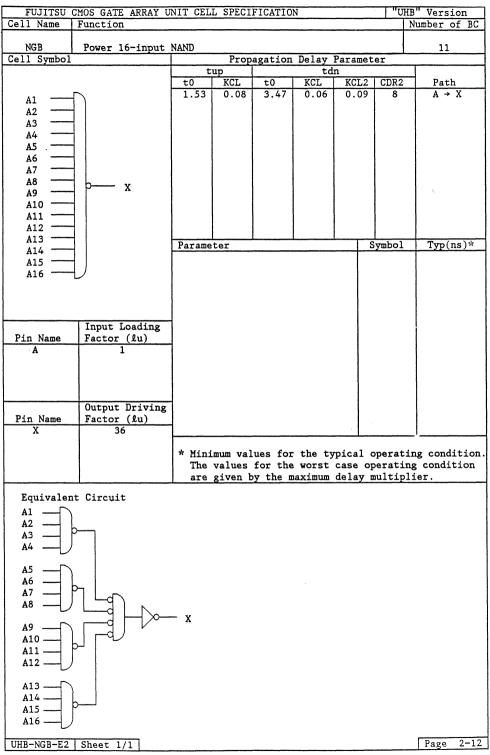
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		"UHB	" Version
	Function						N	umber of BC
		IANTO						
N4B Cell Symbol	Power 4-input N	IAND	Prop	agation	Delay	Paramet	er	4
Jell Dymbol		t	up	agacion	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.38	0.08	1.90	0.04			A + X
	_							
A1 ———	] )							
A3	р—— х							
A4	Ð							
							<u></u>	m ( ) di
		Parame	ter			<u>_</u>	ymbol	Typ(ns)*
	Input Loading	1						
Pin Name	Factor (lu)							
A	1							
	Output Driving	-						
Pin Name	Factor (lu)							
X	36							
		* Mini	mum 1701	ues for	the tw	mical o	meratir	ng condition.
		The	values	for the	worst	case of	perating	condition
		are	given b	y the m	aximum	delay n	nultipli	er.
								[ Dana 2 7
UHB-N4B-E2	Sheet 1/1							Page 2-7

Cell Name	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		וט" ו	HB" Version Number of BC
Sell Mame								Trumper Of BC
N6B	Power 6-input N	AND						5
Cell Symbol				agation			er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		1.37	0.08	2.02	0.04	0.07	7	Path A → X
					İ			
A1								
A2 -								
A3	р <del></del>							
A4 ————————————————————————————————————								
A6								1
		Parame	ter			S	ymbol	Typ(ns)*
						l		Ì
	Input Loading							
Pin Name	Factor (lu)							
A	1	1						
						j		
Din Nama	Output Driving							
Pin Name X	Factor (lu)							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
	,	are	varues given b	y the m	aximum	delav n	nultio	ng condition lier.
			8					
Equivalen	t Circuit							
A1 —								
A2	<del></del>							
A3 —								
A4 —		X						
A5								
A6 —								
UHB-N6B-E2	Sheet 1/1		24					Page 2-8

PHILIPON (	TWO CAME ADDAY I	NIT CEL	CDECT	CTCATTO	·		117777	B" Version
Cell Name	CMOS GATE ARRAY U Function	NII CEL	n officia	TUALIU	IA			Number of BC
N8B	Power 8-input N	AND						66
Cell Symbol			Propa up	agation	Delay td		er	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.44	0.08	2.21	0.04	0.07	7	A + X
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							Ì	
A1 ————————————————————————————————————							1	
A3 —								
A4	v						İ	
A5	р— х				ļ			
A6							1	
A7 ————————————————————————————————————								
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		Parame	rer				ymbol	Typ(ns)*
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						1		
		1						
l	Input Loading	1						
Pin Name	Factor (lu)							
A	1							
		1						
	Output Driving							
Pin Name X	Factor (lu)	1						
Α	30							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
	1	are	given b	y the m	naximum	delay n	ultipl	ier.
Equivalen	t Circuit							
A1 —	<del>-</del>							
A1 — )								
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A4 —	La N							
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A6								
A7 — 5								
A8 —								
UHB-N8B-E2	Sheet 1/1							Page 2-9
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FULLTSU	CMOS GATE ARRAY U	NIT CEL	SPECT	FICATIO	NI		1171	HB" Version
	Function	NII OLL	o biboi	TICKTIO	IN .		ij	Number of BC
NOW	D 2 '' '	AND						
N3K Cell Symbol	Power 3-input N	AND	Prop	agation	Delav	Paramet	er	3
		tı	up	-8401011	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.48	0.07	0.65	0.08			A -> X
A1	<u>)</u> .							
A2 ————————————————————————————————————	р х							
A3 [								
		<u> </u>				L	L	
		Parame	cer				ymbol	Typ(ns)*
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	2							
	İ							
	Output Driving							
Pin Name	Factor (lu)							
X	28							
		sk Mini	num *** 1:	ues for	the tu	mical o	norat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
UHB-N3K-E1	Sheet 1/1							Page 2-13

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
N4K	Power 4-input N	AND						4
Cell Symbol			Prop	agation	Delay		er	
			up		td		,	
		t0	KCL	t0	KCL	KCL2	CDR2	Path   A → X
		0.56	0.07	0.76	0.10			$A \rightarrow X$
							ľ	
A1	$\cap$							
A2								
A3	P x							
A4	)							
ДЧ							1	
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							<u> </u>	
		Parame	ter			S	ymbol	Typ(ns)*
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	<del></del>					ł		
5	Input Loading							
Pin Name	Factor (lu)					1		
A	2					1		
						1		
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	0 4 4 5 1 1	ł						
Dia Nama	Output Driving							
Pin Name X	Factor (lu)							
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		w Mini	m.,m1	fa-	. +ha +			
		The	.mum vai	for the	voret	pical c	perati	ng condition. g condition
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	1	are	given L	y the h	aximum	delay i	urcipi	Ter.
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1								
UHB-N4K-E1	Sheet 1/1							Page 2-14

## **NOR Family**

Page	Unit Cell Name	Function	Basic Cells
2-33	R2N	2-input NOR	1
2-34	R2B	Power 2-input NOR	3
2-35	R2K	Power 2-input NOR	2
2-36	R3N	3-input NOR	2
2-37	R3B	Power 3-input NOR	3
2-38	R4N	4-input NOR	2
2-39	R4B	Power 4-input NOR	4
2-40	R6B	Power 6-input NOR	5
2-41	R8B	Power 8-input NOR	6
2-42	R9B	Power 9-input NOR	8
2-43	RCB	Power 12-input NOR	10
2-44	RGB	Power 16-input NOR	11
2-45	R3K	Power 3-input NOR	3
2-46	R4K	Power 4-input NOR	4

FUITTSU C	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N N		111111	IB" Version
Cell Name	Function	NII CLL	D DILOI.	FICALIO	IN .	·		Number of BC
R2N	2-input NOR							11
Cell Symbol		+-	Prop.	agation	Delay td	Paramet -	er	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.40	0.29	0.44	0.08	0.11	4	A + X
A1	$\rightarrow$							
A2 —	_p x							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						į		
						l		
	Output Driving							
Pin Name	Factor (lu)							
X	14					<u> </u>		
		* Mini	mm ***a1	ues for	+ ho + n	mical c	nerati	ing condition.
		The	mum vai values	for the	worst	case or	erati	ng condition
		are	given b	y the m	naximum	delay m	ultip	lier.
								1
								ļ
								İ
UHB-R2N-E2	Sheet 1/1							Page 3-1

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N			B" Version
Cell Name	Function							Number of BC
Dan	Davies 2 3 37	OΒ					1	,
R2B Cell Symbol	Power 2-input N	υĸ	Pron	agation	Delaw	Parame+	ar I	3
Sell Symbol		tı	up	agacion	td	n arawet	CT	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.36	0.08	1.25	0.04			Path A → X
							l	
							l	
								1
A1 ——— A2 ———	x							
AZ								
		Parame	ter	L		1 8	ymbol	Typ(ns)*
			·					
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						l		
								1
	Output Driving					- 1		
Pin Name	Factor (lu)					1		
Х	36							
			_	_	_			
		* Mini	mum val	ues for	the ty	pical o	operat:	ing condition.
		The	values	for the m	WOTST	delaw r	perati	ng condition
	<del></del>	are	given i	y the h	IAXIIIUII	delay i	питетр	iiei.
1								
1								
UHB-R2B-E2	Sheet 1/1							Page 3-2

EUTEROU C	WOO CAME ADDAY II	NITE OFF	CDECT	ETGIETO	.,		1 11 77777	11 ++
Cell Name	MOS GATE ARRAY U	NII CEL	L SPECI.	FICALIO	N		I UHI	B" Version Number of BC
CELL MAINE	1 4110 0 1 0 11							remper or po
R2K	Power 2-input N	OR						2
Cell Symbol			Prop	agation	Delay	Paramet	er	
	, egilet	ti	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	, in the second second	0.45	0.14	0.45	0.06			$A \rightarrow X$
	'							
	A *							
	. *							
_	_							
A1	x							
A2			l					
	3.							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						-		
	Inputoading					1		
Pin Name	Factor (lu)							1
A	2							
	6							
						1		
						l		
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
		* Mini	mum val	nes for	the tv	pical o	perati	ng condition.
		The	values	for the	worst	case or	erating	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
	7,							
	1.24							
	19116 - T							
	<b>4</b> 4							
	4.5							
	4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1							
UHB-R2K-E2	Sheet 1/1							Page 3-3
			35					

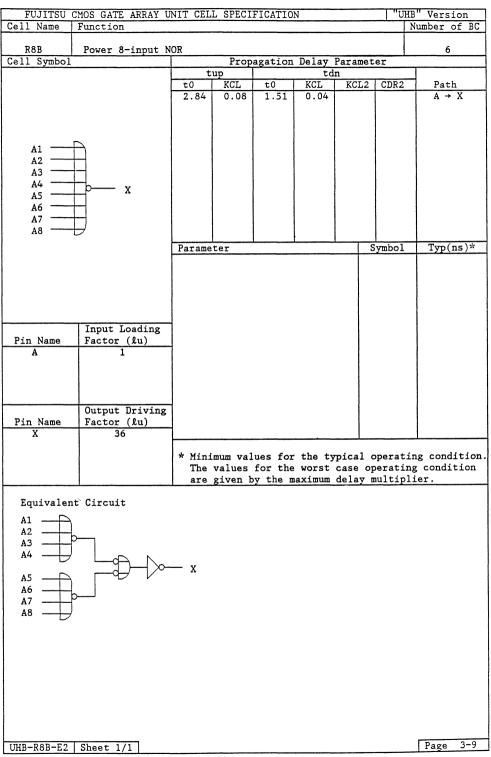
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Versio	n
Cell Name	Function							Number of	BC
זאפת	2-i-mu+ NOD						1	•	
R3N Cell Symbol	3-input NOR		Prop	agation	Delay	Paramet	er	2	
JOIL DYMDOI		t	up IIOp	-6401011	td		~1		
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.84	0.41	0.46	0.09	0.12	4	A → X	
A1	<u> </u>								
A2 ————————————————————————————————————	x								
AJ									
							L	<del>  </del>	<u> </u>
		Parame	ter			S	ymbol	Typ(ns	)"
	Input Loading					- 1			
Pin Name	Factor (lu)								
A	1								
		ļ							
	Output Driving								
Pin Name	Factor (lu)								
X	10								
		* Mini	mum 1721	ues for	the to	mical c	nerati	ng condit	ion
		The	walues	for the	worst	case or	eratin	ng conditi	on.
		are	given b	y the m	aximum	delay n	ultipl	ier.	
UHB-R3N-E2	Sheet 1/1							Page	3-4

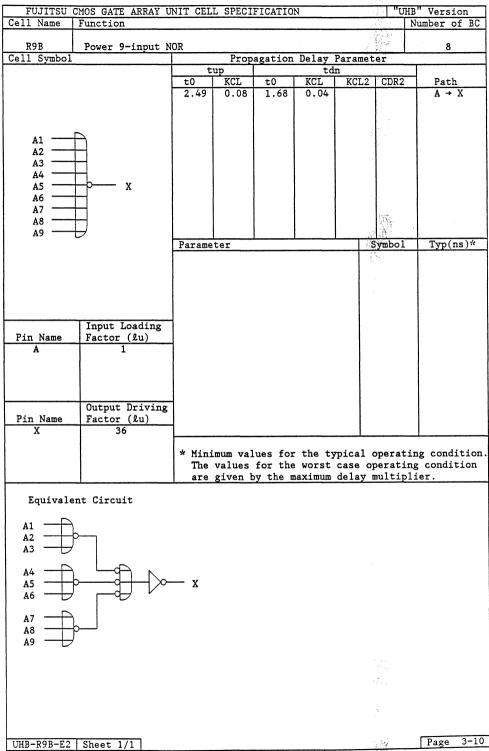
EUTTTOU	CMOC CAMP ADDAY I	NITT CEL	CDECT	ETCARTO	N7		117777	B" Version
	CMOS GATE ARRAY ( Function	NII CEL	L SPECI	FICATIO	N		l on	Number of BC
	-							
R3B	Power 3-input N	IOR						3
Cell Symbol				agation	Delay		er	_
		t0	up KCL	t0	td: KCL	KCL2	CDR2	Path
		1.99	0.08	1.37	0.04			Path A → X
	_							
A1	<u> </u>							
A2 ———	х							
AS								
				<u> </u>		L	1 1	T()*
		Parame	ter			-S	ymbol	Typ(ns)*
						İ		
						1		
	Input Loading	1						
Pin Name	Factor (lu)							
A	1	1						
		1						
	Output Driving	1				l		
Pin Name X	Factor (lu)	4				1		
^	36							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
İ								
İ								
UHB-R3B-E2	Sheet 1/1							Page 3-5
	4							

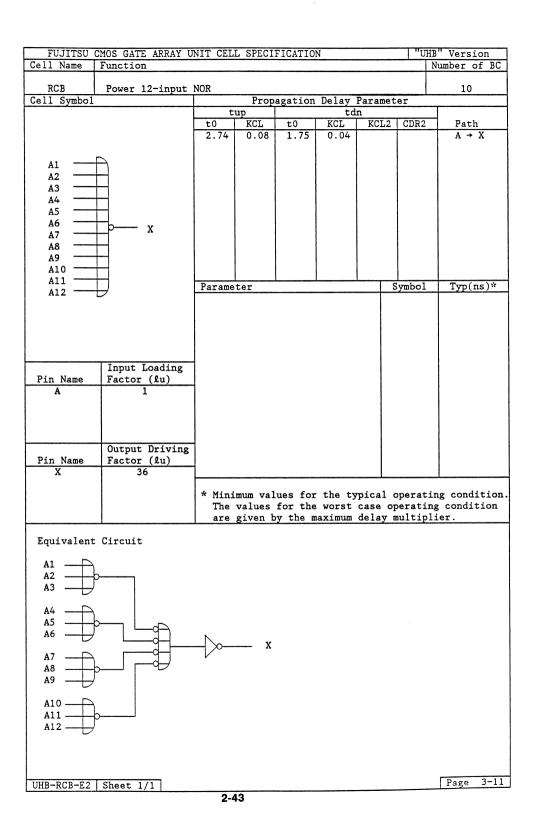
FULITSU C	MOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	J.		1 "171	IB" Version
Cell Name	Function	WII ODD	D DI BOI	1011110			T J	Number of BC
R4N Cell Symbol	4-input NOR	Γ	Prop	agation	Dolor	Damamat		2
Cell Symbol		t	up Flop	agacion	td		er	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.24	0.54	0.46	0.09	0.13	4	Path A → X
A1	7							
A2								
A3	_p x			·				
A4 —	7							
		Parame	ter			S	ymbol	Typ(ns)*
		1						
		1						
		]				1		
	Input Loading	1						
Pin Name	Factor (lu)	1						
A	1					l		ł
		]						
D	Output Driving							
Pin Name X	Factor (lu)	-				1		
•								
	,	* Mini	mum val	ues for	the ty	pical o	perat:	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay n	ultip.	lier.
1								
1								
1								
UHB-R4N-E2	Sheet 1/1							Page 3-6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION   "UHB" Version Cell Name Function   Number of BC    R4B   Power 4-input NOR   4    Cell Symbol   Tup   to   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup	FILITTEIL (	TMOS CATE ADDAY I	DITT CEL	CDECT	ETCATIO	N		1777	ID" Voncion
R4B   Power 4-input NOR	Cell Name		MATI CEP	u ofect.	FICALIO	IN		1 01	Number of BC
Propagation Delay Parameter   tup   tdn									
Tup		Power 4-input N	OR	D		D-1 3	Dame		4
Parameter    To   KCL   to   KCL   KCL2   CDR2   Path	cerr symbol		+		agation			er	
A1 A2 A3 A4 Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  A 1  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition				KCL				CDR2	Path
Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Discrepance of the typical operating condition The values for the worst case operating condition			2.50	0.08	1.34	0.04			A → X
Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Discrepance of the typical operating condition The values for the worst case operating condition									
Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Discrepance of the typical operating condition The values for the worst case operating condition								İ	
Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Discrepance of the typical operating condition The values for the worst case operating condition									
Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Discrepance of the typical operating condition The values for the worst case operating condition									
Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  A 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition	A1	A							
Parameter Symbol Typ(ns)*  Pin Name Factor (Lu)  A 1  Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition		├ x							
Parameter Symbol Typ(ns)*  Pin Name Factor (Lu)  A 1  Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition		<u> </u>							
Pin Name Factor (£u)  A 1  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition	A4					ļ j			
Pin Name Factor (£u)  A 1  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (£u)  A 1  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition			Parame	ter	l	L	l s	ymbol	Typ(ns)*
Pin Name Factor (Lu)  A 1  Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (Lu)  A 1  Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (Lu)  A 1  Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (Lu)  A 1  Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (Lu)  A 1  Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition			1				1		
A 1  Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition	Din Nama	Input Loading							
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition			1				-		
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition		1							
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition							1		
Pin Name Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition		Output Driving	1						
X 36  * Minimum values for the typical operating condition The values for the worst case operating condition									
The values for the worst case operating condition									
The values for the worst case operating condition			* Mini	mum Test	ues for	the tw	nical c	nerat	ing condition
are given by the maximum delay multiplier.			The	values	for the	worst	case or	erati	ng condition
		<u> </u>	are	given b	y the m	aximum	delay n	ultip	lier.
UHB-R4B-E2   Sheet 1/1   Page 3-7									

C CULTEROU O	MOC CAPT ADDAY II	NITE OFF	CDECT	CTOAMTO			111777	
Cell Name	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	N		1 0	HB" Version Number of BC
- Joseph Manne						<del></del>		
R6B	Power 6-input N	OR						5
Cell Symbol				agation			er	
		t0	up KCL	t0	KCL KCL	n KCL2	CDR2	Path
	,	2.25	0.08	1.48	0.04	ROBE	ODICE	A + X
A	_							
A1 A2								
A3 -								
A4	_р х							
A5								
A6 —	7							
		Decree				<u> </u>	rmh - 1	Tum (ma) th
		Parame	rei			<del> -</del>	Symbol	Typ(ns)*
						-		
	Input Loading					l		
Pin Name	Factor (lu)							
A	1							
	l							
Din Nama	Output Driving Factor (lu)							
Pin Name X	36	i						
		* Mini	mum val	ues for	the ty	pical o	operat	ing condition.
		are	values given b	or the m	aximum	delav	perati nultip	ng condition
		1 410	<u> </u>	<i>y</i> 0110 11		uciu,	<u> </u>	
Equivalent	t Circuit							
A1								
A1 ————————————————————————————————————	<b></b>							
A3 —								
		X						
A4 -								
A5 A6								
(TITE DATE TO THE	G1 1 /							Page 3-8
UHB-R6B-E2	Sheet 1/1		40					Tage 5 0







FULTERIA	WOO CATTE ADDAY II	NITE CEL	CDECT	CICATIO	· ·		1 117 777	ID!! W
	MOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	N		I OH	B" Version Number of BC
					***************************************			
RGB	Power 16-input	NOR	D		D-1	D +		11
Cell Symbol		+	up up	agation	Delay td		er	7
1		t0	KCL	t0	KCL	KCL2	CDR2	Path
A1	$\Rightarrow$	3.43	0.08	1.82	0.04			Path A → X
A2 -	-							
A3 -								
A4 A5								
A6 -	-							
A7								
A8 A9	x							
A10 -								
A11 -								
A12								
A13 A14		Parame	ter			S	ymbol	Typ(ns)*
A15	_							
A16 —	<b>ブ</b>							
<b> </b>	Input Loading							
Pin Name	Factor (lu)							
A	1							
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
		* Mini	mum val	ues for	the tv	nical o	perati	ng condition.
		The	walues	for the	worst	case op	eratin	ng condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
Equivalent	Circuit							
A1 —								
A2								
A3 ————————————————————————————————————								
A5 —								
A6 A7	7   _							
A8	1 -97							
		- x						
A9 A10								
A11	<u> </u>							
A12 —								
A13 —								
A14								
A15	<del></del>							
A16 —								
UHB-RGB-E2	Sheet 1/1							Page 3-12
	·	2	-44			<del></del>		

THITTON (	ONOG GAME ADDAY U	NITE CELL	CDECT	CTCATTO	\T		1 1177	m" w
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	N			HB" Version Number of BC
R3K Cell Symbol	Power 3-input N	OR	P		Do 1 1	Dama		3
Cell Symbol		t.:	up Prop	agation	Delay td		er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.66	0.17	0.32	0.04	0.07	7	Path A → X
,								
A1	A							
A2	— — х							
A3	$\forall$							
		Parame	ter			S	ymbol	Typ(ns)*
						l		
	Input Loading							
Pin Name	Factor (lu)					Ì		
A	2							
						İ		
Pin Name	Output Driving Factor (lu)	ł						
X	20							
		* Mini	mum val values	ues tor for the	the ty	pical c	perat	ing condition. ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
								<u> </u>
UHB-R3K-E1	Sheet 1/1	2	45					Page 3-13

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION						"បា	HB" Version		
Cell Name	Function						Number of BC		
<b>5</b> /						,			
R4K	Power 4-input NOR 4								
Cell Symbol		+	Propagation Delay Parameter tup tdn						
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		1.08	0.23	0.35	0.03	0.05	7	A → X	
							İ		
				· ·					
							1		
A1	A								
A2	х								
A3	<b>↑</b>				,		l		
A4	$\Theta$								
,		Parame	ter			S	ymbo1	Typ(ns)*	
	•					T			
						1			
	Input Loading	i							
Pin Name	Factor (lu)					İ			
A	2	1				1			
						-			
						Ī			
	Output Driving	ł				ŀ			
Pin Name	Factor (lu)								
X	12	1							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.	
1	* Minimum values for the typical operating condition The values for the worst case operating condition						ng condition		
	are given by the maximum delay multiplier.						lier.		
1									
1									
1									
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UHB-R4K-E1	Sheet 1/1							Page 3-14	

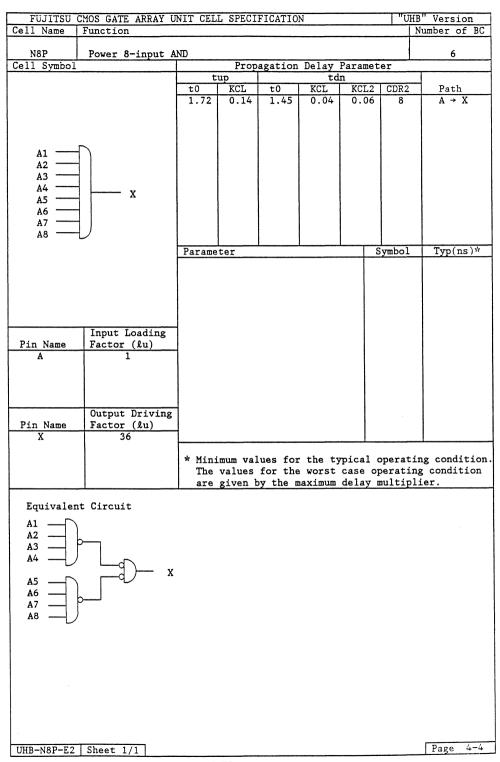
## **AND Family**

Page	Unit Cell Name	Function	Basic Cells
2-49	N2P	Power 2-input AND	2
2-50	N3P	Power 3-input AND	3
2-51	N4P	Power 4-input AND	3
2-52	N8P	Power 8-input AND	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U Cell Name   Function						10	HB" Version Number of BC	
Cell Name Function							Tramber of bo	
N2P								2
Cell Symbol	Cell Symbol Propagation Delay Parameter							
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		1.01	0.08	0.86	0.04	0.06		A + X
						ĺ		
A1	·						Ì	
A2	x	l						
							-	
		Pariti			l	L.,,,,,	 	T ()*
		Parame	rer				Symbol	Typ(ns)*
		1						
		1				1		
	Input Loading	1						
Pin Name	Factor (lu)	1						
A	1	l				- 1		
		j						
Pin Name	Output Driving Factor (lu)							
X	36	1						
		* Minimum values for the typical operating condition.						
		The values for the worst case operating condition are given by the maximum delay multiplier.						
	are given by the maximum delay multiplier.							
1								
								ļ
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UHB-N2P-E2	Sheet 1/1							Page 4-1

EUTTTCU C	MOC CATE ADDAY II	NITT CET	CDECT	ETCATTO	NT.		117777	B" Version
Cell Name	MOS GATE ARRAY U Function	NII CEL	L SPECI.	FICALIO	IN .		1 UH	Number of BC
N3P	Power 3-input A	ND						3
Cell Symbol				agation	Delay	Paramet	er	
			up		td		<u> </u>	
		t0 1.32	KCL 0.08	t0 1.07	KCL 0.04	KCL2 0.06	CDR2	Path A → X
		1.32	0.08	1.07	0.04	0.06	,	AAA
	_							
A1								
A2	x							
A3								
		Parame	ter		L	l s	ymbol	Typ(ns)*
						<del></del>	, <b>_</b>	//
	<del></del>					İ		
D4 17	Input Loading							
Pin Name	Factor (lu)					1		
A	1					1		
						1		
	Output Driving							1
Pin Name	Factor (lu)							
X	36							
			_					
		" Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		Ine	values	ior the	worst aximum	delaw -	eratin	g condition
		are	graen p	y the m	IAXIIIUIII	deray I	iar erbr	161 .
UHB-N3P-E2	Sheet 1/1							Page 4-2
UNB-NSP-E2	PHEEF I/I							11050 7 2

EU TERCU	3V00 0488 4554V IV	NITE CET	CDECT	DI O AMITO	.,		1 117777	70 17
Cell Name	CMOS GATE ARRAY U Function	NIT CEL	L SPECI.	FICATIO	N			B" Version Number of BC
COLL MAINE	1 mice TOIL							TOWNET OF DO
N4P	Power 4-input A	ND					l	3
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.58	0.08	1.19	0.04	0.06	8	A - X
		1						
						ľ		
A1	$\Gamma$							
A2								1
A3	х х							
A4								
	_				}			j .
		Parame	ter	L	<u> </u>	1 6	ymbol	Typ(ns)*
		1 ar ame	CET				, m.o.i	139(113)
		1						
		1				İ		
		1				1		
		1						
	Input Loading	1				1		
Pin Name	Factor (lu)					l		
A	1	1						
						1		
Dia N	Output Driving	İ						
Pin Name X	Factor (lu)	-				j		j
^	36							
		* Mini	mum 17a1	ues for	the tw	mical c	narati	ng condition.
		The	walnes	for the	worst	case or	eratir	ng condition
		are	given b	v the m	aximum	delav m	ultipl	ier.
		<u> </u>	0					
UHB-N4P-E2	Sheet 1/1							Page 4-3
			E 4					



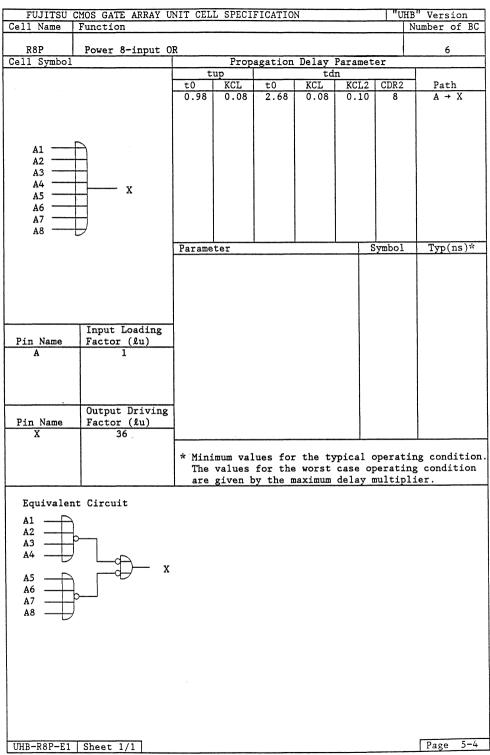
# **OR Family**

	Unit Cell		Basic
Page	Name	Function	Cells
2-55	R2P	Power 2-input OR	2
2-56	R3P	Power 3-input OR	3
2-57	R4P	Power 4-input OR	3
2-58	R8P	Power 8-input OR	6

FILITSH	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		וווויי	B" Version
	Function	.111 0111	. 01501	LICALIU	17		1	Number of BC
		_			***************************************			
R2P Cell Symbol	Power 2-input 0	R	Dean	+	Delem	Damanat		2
Cell Symbol		t	up	agation	Delay td		er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.78	0.08	1.14	0.05	0.07	8	A + X
	_							
A1	x	ĺ						
A2	7							
		Parame	ter	I	I	S	ymbol	Typ(ns)*
						-		
Din Mana	Input Loading	}						
Pin Name A	Factor (lu)	1						
••	1					l		
						ł		
								}
	Output Driving	1				1		
Pin Name	Factor (lu)							
Х	36							
		* Mini	mum 1701	ues for	+ + he + v	mical c	nerati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	naximum	delay n	ultipl	ier.
UHB-R2P-E2	Sheet 1/1							Page 5-1
			EE					

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version
Cell Name	Function							Number of BC
R3P	Power 3-input 0	R						3
Cell Symbol		4	Prop up	agation	Delay td	Paramet	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	•	0.90	0.08	1.84	0.06	0.08	8	A → X
A1	$\supset$							
A2	x							
A3 —	$\exists$							
								1
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1							
	Output Driving							
Pin Name	Factor (lu)					1		
Х	36					l		
		* Mini	mum val	ues for	the tw	roical o	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	<u> </u>	are	given b	y the m	naximum	delay n	ultip	lier.
UHB-R3P-E2	Sheet 1/1							Page 5-2

FILITZEI C	MOS GATE ARRAY U	NITT CELL	CDECT	ETCATTO	NT.		מעודייו	" Version
	Function	NII CELI	J SFECT.	FICATIO	IN		I ONB	umber of BC
							— † <u>`</u> `	
R4P	Power 4-input 0	R						3
Cell Symbol				agation	Delay	Paramet	er	
		t0 t	KCL KCL	t0	td KCL	n KCL2	CDR2	Path
	•	0.90	0.08	2.52	0.07	0.10	8 8	A → X
		0.70	0.00	2.52	0.07	0.10		n · n
		j						
A1	$\rightarrow$							
A2 -								
A3	x							
A4 —	eg							
		Parame	ter			S	ymbol	Typ(ns)*
						1		1
	Input Loading	1						
Pin Name	Factor (lu)							
A	1	l						
		]						
						Ì		
	0	1						
Din Name	Output Driving Factor (lu)					ļ		
Pin Name X	36	ł						
••								· · · · · · · · · · · · · · · · · · ·
		* Mini	mum val	ues for	the ty	pical o	peratir	g condition.
		The	values	for the	worst	case or	erating	condition
		are	given b	y the m	aximum	delay m	ultipli	er.
1010 D/D 50 1	G1 4 7 7 1							Page 5-3
UHB-R4P-E2	Sheet 1/1							leage 2 2



## **EXNOR/EXOR Family**

Page	Unit Cell Name	Function	Basic Cells
2-61	X1N	Exclusive NOR	3
2-62	X1B	Power Exclusive NOR	4
2-63	X2N	Exclusive OR	3
2-64	X2B	Power Exclusive OR	4
2-65	X3N	3-input Exclusive NOR	5
2-66	X3B	Power 3-input Exclusive NOR	6
2-67	X4N	3-input Exclusive OR	5
2-68	X4B	Power 3-input Exclusive OR	6

2

בווזדדפון כ	MOS GATE ARRAY U	NIT CEL	C C C C C C C C C C C C C C C C C C C	ETCATTO	NT		1177	IB" Version
	Function	111 01111	DI DI LOI.	FICATIO			- 1	Number of BC
X1N Cell Symbol	Exclusive NOR		Pron		Dalam	Paramete		3
Cell Symbol		tı	up	agation	td	n n	÷ I	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.16	0.29	0.96	0.13	0.16	4	A → X
					:			
A1 —	`> x					ŀ		
A2 ———	<b>→</b>							
		Parame	ter			S	ymbol	Typ(ns)*
D: 17	Input Loading							
Pin Name A	Factor (lu)							
n	-							
	Output Driving							
Pin Name	Factor (lu)							
X	18							
		* Wini		nas for	the tu	mical o	na=a+:	ing condition.
		The	wam var values	for the	worst	case op	erati:	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
Equivalent	Circuit							
ndararem	. 0110410							
A1	h							
A2 -	~	_						
L		) <del></del>	— x					
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	_							
*								
UHB-X1N-E2	Sheet 1/1							Page 6-1
4,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,								

FILITSILO	MOS GATE ARRAY U	NIT CEL	T. SPECT	FICATIO	N		ועוזיי	B" Version
Cell Name	Function	IVII OLL	L SIECI.	FICALLO	IN .		1 1	Number of BC
							<del></del>	
X1B	Power Exclusive	NOR						4
Cell Symbol				agation	Delay td	Paramet	er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		1.49	0.08	1.77	0.05	0.09	7	Path A → X
A1 ———	_							
A2	_)> x							
, AZ 1								
į								
		Parame	ter		·	S	ymbol	Typ(ns)*
						1		
						ľ		
						- 1		
	Input Loading							
Pin Name	Factor (lu)							
A	2					1		
1								Į.
	Output Driving	1						
Pin Name	Factor (lu)	1						
X	36	<u> </u>						
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	naximum	delay n	ultipl	ier.
1								
Equivalen	t Circuit							
	<del></del>							
A1 A2	) <del></del>							
M2   TTD		A. N	\_					
			<u> </u>	X				
		Γ ΄						
UHB-X1B-E2	Sheet 1/1							Page 6-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION	"UHB" Vers Number	of BC
X2N	3	
Cell Symbol         Propagation Delay Parameter           tup         tdn           t0         KCL         t0         KCL         KCL         KCL		i
tup tdn t0 KCL t0 KCL KCL2 C		
tO   KCL   tO   KCL   KCL2   C		
	DR2 Pat	
1.11 0.29 1.17 0.13 0.16	4 A →	X
		I
	1	1
	1	
A1 — X		
A2 - X	1	
Parameter Sym	bol Typ(	ns)*
rarameter	Lyp(	
Input Loading		
Pin Name   Factor (lu)		
A 2		
	i	
Output Driving		
Pin Name Factor (lu) X 14		
A 1-7		
* Minimum values for the typical ope	rating cond	lition.
The values for the worst case open	ating condi	tion.
are given by the maximum delay mu	tipiler.	
Equivalent Circuit		
A1		
A1 A2		
x		
UHB-X2N-E2   Sheet 1/1	Page	6-3

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	<u> </u>		UHB.	" Version
Cell Name	Function	000	5 51 501.	1 1011110	· <u>'</u>		N	umber of BC
X2B	Power Exclusive	OR						4
Cell Symbol	·	<u></u>	Prop	agation	Delay	Paramet	er	
			up YOT	+0	td		anna	70.45
		t0	0.08	t0 1.64	KCL 0.05	KCL2 0.07	CDR2	Path A → X
		1.43	0.08	1.64	0.05	0.07	,	$A \rightarrow X$
	·							
4.4	_							
A1 —	x							
A2	<del></del>							
		Parame	ter			S	ymbo1	Typ(ns)*
		1						
	Input Loading							
Pin Name	Factor (lu)							
A	2	Ì						
						ì		
	Detect Being	1						
D. 11	Output Driving							
Pin Name	Factor (lu)					i		
Х	36	<u> </u>						<u> </u>
		# Mini	mum *** 1	nos for	+ho +v	mical c	noratio	g condition.
		The	walnee	for the	worst	PICAL C	perating	condition
		are	values given h	y the m	avimim	delay n	niltinli	er.
		are	given i	y che i	ax z m cm	ucia, a	.ururpii	
,								
Equivalen	t Circuit							
-1								
A1	b							
A2 + 1								
		p—1,	<b>&gt;&gt;</b>	X				
-			, -					
1								
1								
1								
UHB-X2B-E2	Sheet 1/1							Page 6-4

							1 11	
	MOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N		1 "U	HB" Version Number of BC
JOZZ Mame	1 410 01011							
X3N	3-input Exclusi	ve NOR				_	1	5
Cell Symbol		t	up Prop	agation	Delay td		ter	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.72	0.29	2.32	0.13	0.16	4	A → X
A1	$\rightarrow$							
A2	— <del>р</del> — х							
A3 —   1	$\overline{\mathcal{I}}$							
				<u> </u>				
		Parame	ter				Symbol	Typ(ns)*
						- 1		
D	Input Loading							
Pin Name A	Factor (lu)							
	_							
		Į						
	Output Driving	İ						
Pin Name	Factor (lu)							
Х	18							
		* Mini	mum val	ues for	the ty	pical	operat	ing condition.
		The	values	for the	worst	case c	perati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay	multip	lier.
Equivalen	t Circuit							
A2 -								
A3								
	<u> </u> х							
A1								
	_							
UHB-X3N-E2	Sheet 1/1							Page 6-5

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Vers	ion
Cell Name	Function							Number o	of BC
V05			NOD				]		:
X3B	Power 3-input E	xclusiv	e NOR		D-1	D · · ·		6	
Cell Symbol				agation	Delay	Paramet	er	<del></del>	
		t0	up KCL	t0	td KCL	KCL2	CDR2	- Bant	
		2.64	0.08	3.39	0.05	0.09	7	Patl	<u>v</u>
		2.04	0.00	3.39	0.03	0.09	'	A -	Λ
								İ	
								1	
							1		
A1	A								
A2 -									
A3 -	<del>                                     </del>								
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l		Parame	ter				ymbol	Typ(:	ns)*
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		}				1			
1						1			
	Input Loading					1		-	
Pin Name	Factor (lu)								
A	2								
1						- 1		1	
						l			
İ									
						1			
	Output Driving					ı			
Pin Name	Factor (lu)					1		1	
Х	36								
		+ w:-:	rra 1	was for	+ ha +=	mical d	noreti	ing cond	ition
		The	.mum vai	for the	worst	PICAL (	operati	ng condi	tion.
		ine	given b	TOT LITE	avimum	delaw i	miltini	ig Conui Lior	CIOII
		l are	grven r	y the n	IOYTHIUM	ueray I	mar erb:		
Equivaler	nt Circuit								
Edutater	ic official								
A2	Δ								
A3	L)¬ ,¬ .								
1	~ <del>-                                     </del>	х							
A1	$\overline{}$								
1									
	<del></del>							[ D	6-6
UHB-X3B-E2	Sheet 1/1							Page	6-6

THE TERMS OF		NITE OF	CDDGT	DIG LETTO			1 117-77	T
	MOS GATE ARRAY U	NIT CEL	L SPECI.	FICATIO	N			B" Version
Cell Name	Function							Number of BC
X4N	3-input Exclusi	TA OR					1	5
Cell Symbol	C Impac Excidsi	TE OIL	Prop	agation	Delay	Paramet	er	
3011 0,0001		t.	up	-6401011	td		<u></u>	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.82	0.29	2.53	0.13	0.16	4	A -> X
	'							
1								
Į.								
A1 -	7							
A2	<del>                                     </del>							
A3 ——	$\overline{\mathcal{I}}$							
}						L	<u> </u>	
1		Parame	ter			s	ymbol	Typ(ns)*
								1
1		1						
1		ł						
Ì								
						1		
D/- V	Input Loading							
Pin Name	Factor (lu)							
A	2	ļ						
		į						
	Output Driving	}						
Pin Name	Factor (lu)							
X	14	ł				i		
-								
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		The	values	for the	worst	case or	eratin	ng condition
		are	given b	y the m	aximum	delay m	ultipl	lier.
	*					<del></del>		
Equivalent	: Circuit							
]								
A2 -								
1 !! -	٦							
A3	110							ļ
	<del></del>							
A1	x							
A1								
UHB-X4N-E2	Sheet 1/1							Page 6-7
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FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UI	dB" Version
	Function							Number of BC
								_
X4B	Power 3-input E	xclusiv	e OR				1	6
Cell Symbol				agation			er	
			up VOT		td		CDDO	I
		t0 2.47	KCL 0.08	t0	KCL	KCL2 0.07	CDR2	Path A → X
		2.4/	0.08	3.13	0.05	0.07	7	$A \rightarrow X$
A1	A I						l	1
A2	<del>                                     </del>							
A3 -	<del>-</del> -							
		Parame	ter			S	ymbo1	Typ(ns)*
								]
	Input Loading							
Pin Name	Factor (lu)	}						
A	2	}						
		1				į.		
						1		
	Outsuch Budadas					- 1		
Din Name	Output Driving					1		
Pin Name X	Factor (lu)					- 1		-
^	30							
		* Mini	mum 1721	ues for	the tw	mical o	nerat	ing condition.
		The	walnes	for the	worst	case or	perati	ng condition
		are	oiven h	y the m	aximum	delay n	miltip	lier.
			9	, "				
Equivalen	t Circuit							
	_							
A2 ———	<del>_</del>							
A3 ————————————————————————————————————								
A1	$\sim$	х						
	, 0							
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	i .							
1								
UHB-X4B-E2	Sheet 1/1							Page 6-8

## AND-OR-Inverter Family (AOI)

Page	Unit Cell Name	Function	Basic Cells
2-71	D23	2 AND into 2 NOR AOI	2
2-72	D14	3 AND into 2 NOR AOI	2
2-73	D24	2, 2 ANDS into 2 NOR AOI	2
2-74	D34	2 AND into 3 NOR AOI	2
2-75	D36	3, 2 ANDS into 3 NOR AOI	3
2-76	D44	2 OR into 2 AND inot 2 NOR AOI	2

FILITTEIL C	MOS CATE ADDAY II	NIT CEL	T CDECT	EICATIO	NI .		11111	HB" Version
	MOS GATE ARRAY U	NII CEL	L SPEUL	LICHILO	7.4		1 1	Number of BC
D23 Cell Symbol	2-wide 2-AND 3-	input A	OI		Do 1	Dame		2
Cell Symbol		t	up Prop	agation	Delay td		er	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.73	0.29	0.68	0.14			A → X
		0.37	0.22	0.37	0.09	0.12	4	B → X
A1 -	7							
A2	х							
В								
					,			
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1							
В	1							
	Output Driving							
Pin Name X	Factor (lu)							
^	14							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati:	ng condition
	I	are	given b	y the m	aximum	deray n	urcip	iler.
İ								
								!
UHB-D23-E1	Sheet 1/1							Page 7-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			HB" Version
Cell Name	Function				.,			Number of BC
D1/		•	0.7					
D14 Cell Symbol	2-wide 3-AND 4-	input A	UI P===	agation	Doler	Darer +		2
CETT SAMPOT		+	up	agation	td		<u>e1</u>	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.90	0.29	0.70	0.19	0.21	4	$A \rightarrow X$
		0.32	0.20	0.36	0.09	0.12	4	B → X
_								
A1 -							ŀ	1
A2	<u> </u>							
A3 ———————————————————————————————————								
В	о—_ х							
В							İ	
}								
		Parame				١	ymbol	Typ(ns)*
		rarame	CET			<del></del>	2 mbOI	Typ(IIS)
		1				1		
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						1		
		1				1		
	Input Loading	1						
Pin Name	Factor (lu)	l						
A	1	i						
В	1							
	Output Driving	-						
Pin Name	Factor (lu)							
X	14	1						
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati:	ng condition
ļ	1	are	given b	y the m	aximum	delay n	ultip	lier.
1								
1								
UHB-D14-E1	Sheet 1/1							Page 7-2
OUD_DIA_FI	SHEEL 1/1					<del></del>		11450 / 4

TILITERIA CI	VOG GARTE ADDAY IT	NITT OFF	CDECT	CT CAMTO	N.T.		117.77	IDII II
	MOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		101	HB" Version Number of BC
CETT MAINE	Function							TAUMDET OF BC
D24	2-wide 2-AND 4-	input A	DI				- 1	2
Cell Symbol			Prop	agation	Delay	Paramet	er	
		tı	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.54	0.22	0.62	0.14			A → X
		0.67	0.22	0.83	0.14			B → X
_								
A1 -	_							
A2 ——								
_	x							
B1							ļ	
B2 —								
		Parame	ter			S	ymbol	Typ(ns)*
	Tours Tours					ł		
Pin Name	Input Loading Factor (lu)							1
A A	factor (ku)							
B	1							
	•	ł						
	Output Driving					ŀ		
Pin Name	Factor (lu)							
X	14							
				6-				ina nonditia
		The The	wum vai	tor +ha	tne ty	bicar c	perat:	ing condition. ng condition
		are	oiven h	A the w	aximum	delaw n	mltin	lier.
	L	arc	OTACH D	, 0116 11				
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1								
UHB-D24-E2	Sheet 1/1							Page 7-3
	Chast 1/1/							1 Page /-3

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UF	IB" Version
Cell Name	Function							Number of BC
D34	3-wide 2-AND 4-	input A	ОТ				l	2
Cell Symbol	5 W145 2 11KB 4		Prop	agation	Delay	Paramet	er	
			up		td	n.		
		t0 1.15	KCL 0.41	t0 0.73	KCL 0.15	KCL2	CDR2	$\begin{array}{c c} Path \\ A \rightarrow X \end{array}$
		0.62	0.41	0.73	0.13	0.12	4	$B \rightarrow X$
		0.02	0.05		0.07		·	
I								1
A1	7							
	4							1.
B1	x							
B2								
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						-		
Pin Name	Input Loading Factor (lu)							
A	1	ĺ						
В -	1					1		
						1		
	Output Driving	ł						
Pin Name	Factor (lu)							
Х	10							
		* Mini	mum 17a1	ues for	the tw	mical c	nerat	ing condition.
1	i	The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
IIID DOV DO	Ch 1 /1 1							Page 7-4
UHB-D34-E2	Sheet 1/1							Page 7-4

FULLTELL	MOC CATE ADDAY II	NIT CEL	CDECT	CTCATTO	NT.		111111111111111111111111111111111111111	" Version
	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO.	N		I UNB	umber of BC
							<del></del>	
D36	3-wide 2-AND 6-	input A	01					3
Cell Symbol		<del></del>		agation		Paramet	er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		0.77	0.28	0.72	0.14	RODZ	ODILE	$A \rightarrow X$
		0.98	0.28	0.87	0.14			$B \rightarrow X$
		1.17	0.28	1.02	0.14			C → X
A1								
A2 ——								
	4							
B1 D	———— x							
B2 U								
C1 —								
C2 —								
		Parame	ter		L	l S	ymbol	Typ(ns)*
							,	-35 \/
						ļ		
						- 1		
	Input Loading					1		
Pin Name	Factor (lu)	ł				İ		
A	1							
В	1							
С	1							
	Output Driving	1						
Pin Name	Factor (lu)							
X	10							
			_	_				
		* Mini	mum val	ues for	the ty	pical o	peratir	g condition.
		ine	values	or the m	e WOIST	delay m	erating ultipli	condition er
	<u> </u>	are	given b	y the n	aximum	deray m	di cipii	
ļ								
UHB-D36-E1	Sheet 1/1							Page 7-5

PILITECTI C	MOC CATTE ADDAY II	NITT CET	CDECT	PTCATTO	NT.		11777	IB" Version
	MOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	N		l On	Number of BC
D44	2-wide 2-OR 2-A	ND 4-in	put AOI					2
Cell Symbol				agation	Delay		er	
			up		td		6555	-
	•	t0 1.04	KCL 0.41	t0 0.78	KCL 0.14	KCL2	CDR2	$\begin{array}{c c} & \text{Path} \\ \hline & A \rightarrow X \end{array}$
		1.03	0.41	0.76	0.14			$B \rightarrow X$
		0.99	0.29	0.48	0.09	0.11	4	$C \rightarrow X$
	•							
A1	7							
A2	1 )							
B	<u> </u>							
C	. D							
		Parame	ter			2	ymbol	Typ(ns)*
	Input Loading							1
Pin Name	Factor (lu)							
A	1							
В	1					1		
С	1							
	Output Driving							
Pin Name	Factor (lu)					İ		
X	10							
		* Mini	mum val	ues for	the ty	pical o	perati	ing condition.
		The	values	for the	worst	case or	peratio	ng condition
	L	are	given b	y the m	aximum	delay r	mutip.	lier.
1								
1								
UHB-D44-E1	Sheet 1/1							Page 7-6

## OR-AND-Inverter Family (OAI)

Page	Unit Cell Name	Function	Basic Cells
2–79	G23	2 OR into 2 NAND OAI	2
2-80	G14	3 OR into 2 NAND OAI	2
2-81	G24	2, 2 OR into 2 NAND OAI	2
2-82	G34	2 OR into 3 NAND OAI	2
2-83	G44	2 AND into 2 OR into 2 NAND OAI	2

FILTTEIL C	MOS GATE ARRAY U	NIT CELL	SDECT	ETCATTO	N		ועוזיי	B" Version
	Function	NII CELI	J DI LOI	TICATIO.	IN .		1 1	Number of BC
			_					
G23 Cell Symbol	2-wide 2-OR 3-i	nput OAl	Pron	agatio-	Delay 1	Darame+	AT.	2
OETT DAMPOT		tı		agation	tdi		- <u>CT</u>	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.72	0.29	0.55	0.14			A → X
		0.28	0.16	0.55	0.14			B → X
_								
A1	7.0							
A2	x	1					1	
В —								
							1	
		Paramet	er			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1					1		
В	1							
	Output Driving							
Pin Name X	Factor (lu) 18							
^	10							
		* Minim	num val	ues for	the ty	pical c	perati:	ng condition.
		The v	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	deray n	ultlpl	TEL.
								İ
								[D 0 1
UHB-G23-E1	Sheet 1/1							Page 8-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N	£.,	"UHI	B" Version
	Function							Number of BC
G14 Cell Symbol	2-wide 3-OR 4-i	nput OA	I Prop	agation	Delay	Paramet	er	2
			up		td	n		T
		t0 1.20	KCL 0.42	t0 0.65	KCL 0.14	KCL2	CDR2	Path   A → X
		0.25	0.16	0.65	0.14			$B \to X$
			İ				l	
_								
A1 A2	~~							
A3 —								
В	х							
В								
						L		( ) W
		Parame	ter			— <del>  S</del>	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1							
В	1							
	Output Driving	1						-
Pin Name	Factor (lu)							
Х	10							1
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst aximum	case or	peratin	g condition
	L	are	given b	y the i	aximum	delay i	uururpi	iei.
IIIIP_C1/- E1	Chast 1/1							Page 8-2
UHB-G14-E1	Sheet 1/1							rage 0-2

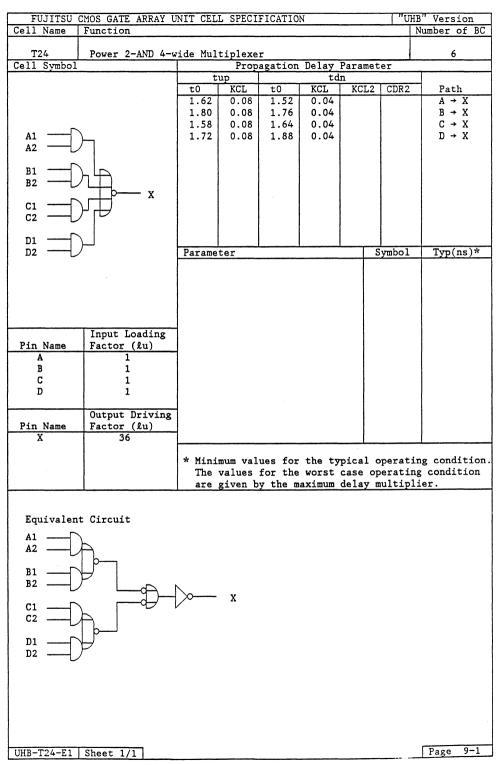
FILITCH C	MOS GATE ARRAY U	NITE CELL	CDECT	ETCATTO	NI .		i "i mur	B" Version	
	Function	NII CEL	L SPECI	FICALIO	N		I One	Number of BC	
				<del>-</del>					
G24	2-wide 2-OR 4-i	nput OA	<u> </u>					2	
Cell Symbol				agation	Delay		er		
		t0	KCL KCL	t0	KCL KCL	KCL2	CDR2	Path	
		0.50	0.29	0.70	0.14	KOLL	ODKZ	A + X	
		0.90	0.29	0.60	0.14			$B \rightarrow X$	
A1 —									
A2	7		į		1				
_	x								
B1									
B2 —									
		Parame	ter		<u></u>	S	ymbol	Typ(ns)*	
						ļ			
	Input Loading					ı			
Pin Name	Factor (lu)								
A B	1 1								
Д	1					1			
<b></b>	Output Driving								
Pin Name X	Factor (lu)					-			
Λ	10								
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.	
		The values for the worst case operating condition							
	<u> </u>	are given by the maximum delay multiplier.							
								,	
								,	
UHB-G24-E2	Sheet 1/1							Page 8-3	

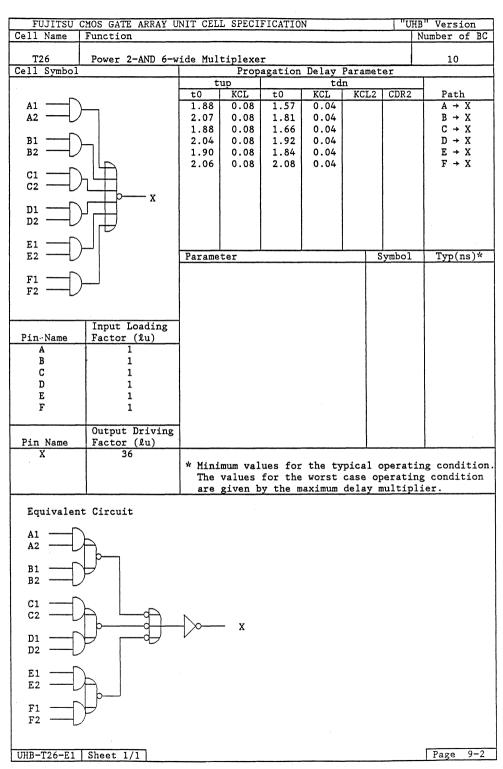
FUJITSU CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		"UH	B" Version
Cell Name   Function				``			Number of BC
G34 3-wide 2-OR 4-i	nnut 04	т					2
G34 3-wide 2-OR 4-i Cell Symbol	nput OA.	Prop	agation	Delav	Paramet	er	
		up		td	n		
	0.95	KCL	t0	KCL	KCL2	CDR2	Path   A → X
	0.93	0.29 0.19	0.70 0.45	0.19 0.16			$B \to X$
	••••						
							1.
A1 —							
A2							
1 - 42 -							
B1 B2 X							
"2"							
	Parame	tor		<u> </u>	٠	Symbol	Typ(ns)*
	Tarame	rer				ушоот	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1					1		
	j				l		
Input Loading Pin Name Factor (lu)							
Pin Name Factor (lu) A 1					1		
B 1					Ì		
Output Driving	1						
Pin Name Factor (lu)	4						
X 10	<b></b>						
	* Mini	mum val	ues for	the ty	pical o	operati	ng condition.
	The	values	for the	worst	case of	peratin	g condition
	are	given r	y the m	aximum	delay	nuitipi	ier.
UHB-G34-E2   Sheet 1/1							Page 8-4

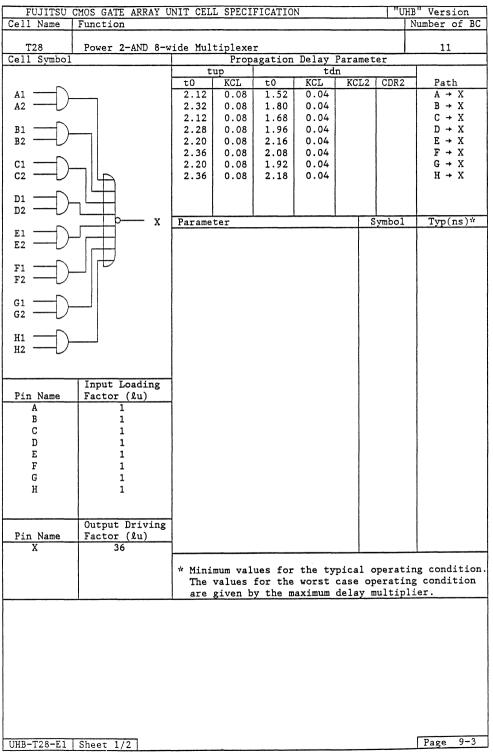
FUJITSU C	MOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		"UHB	" Version	
Cell Name	Function						N	lumber of BC	
G44	2-wide 2-AND 2-	OR 4-in	out_OAI		2				
Cell Symbol			Prop	er					
	•	t0 t	KCL KCL	t0	td KCL	n KCL2	CDR2	Path	
		0.73	0.29	0.86	0.19			A -> X	
		0.43	0.29	0.62	0.19 0.14			$\begin{array}{c} B \rightarrow X \\ C \rightarrow X \end{array}$	
		0.30	0.16	0.52	0.14				
A1 —									
A1	A								
В —	₩ x								
c	——U "								
					L	<u> </u>		T ()*	
		Parame	ter			<del>-   s</del>	ymbol	Typ(ns)*	
						1			
						1			
								1	
Pin Name	Input Loading Factor (lu)								
A	1								
В	1								
С	1								
Dia Nama	Output Driving							1	
Pin Name X	Factor (lu)								
			_	_				1	
		* Minimum values for the typical operating condition.  The values for the worst case operating condition							
		are given by the maximum delay multiplier.							
								-	
								The same	
UHB-G44-E1	Sheet 1/1		***************************************					Page 8-5	

## **Multiplexer Family**

Page	Unit Cell Name	Function	Basic Cells
2-87	T24	4:1 Power 4, 2 ANDs into 4 NOR Multiplexer	6
2-88	T26	6:1 Power 6, 2 ANDs into 6 NOR Multiplexer	10
2-89	T28	8:1 Power 8, 2 ANDs into 8 NOR Multiplexer	11
2-91	T32	2:1 Power 2, 3 ANDs into 2 NOR Multiplexer	5
2-92	T33	3:1 Power 3, 3 ANDs into 3 NOR Multiplexer	7
2-93	T34	4:1 Power 4, 3 AND into 4 NOR Multiplexer	9
2-94	T42	2:1 Power 2, 4 ANDs into 2 NOR Multiplexer	6
2-95	T43	3:1 Power 3, 4 ANDs into 3 NOR Multiplexer	10
2-96	T44	4:1 Power 4, 4 ANDs into 4 NOR Multiplexer	11
2-97	T54	4:1 Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10
2-98	U24	4:1 Power 4, 2 OR into 4 NAND Multiplexer	6
2-99	U26	6:1 Power 6, 2 OR into 6 NAND Multiplexer	9
2-100	U28	8:1 Power 8, 2 OR into 8 NAND Multiplexer	11
2-101	U32	2:1 Power 2, 3 OR into 2 NAND Multiplexer	5
2-102	U33	3:1 Power 3, 3 OR into 3 NAND Multiplexer	7
2-103	U34	4:1 Power 4, 3 OR into 4 NAND Multiplexer	9
2-104	U42	2:1 Power 2, 4 OR into 4 NAND Multiplexer	6
2-105	U43	3:1 Power 3, 4 OR into 3 NAND Multiplexer	9
2-106	U44	4:1 Power 4, 4 OR into 4 NAND Multiplexer	11







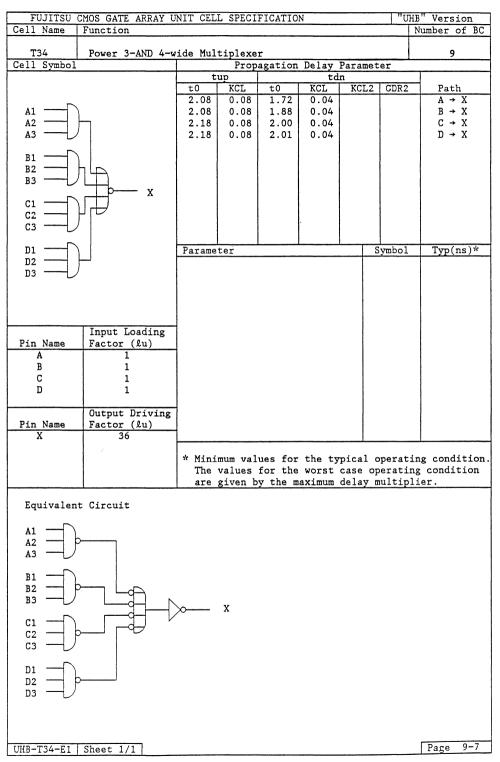
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name T28 Equivalent Circuit A1 -A2 -B1 -B2 -C1 -C2 -D1 -D2 -E1 -E2 -F1 -F2 -G1 -G2 -H1 -H2 -

UHB-T28-E1 | Sheet 2/2

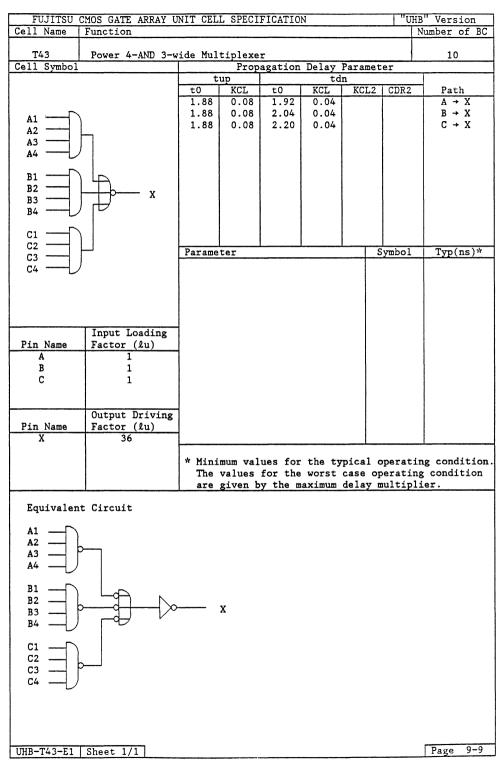
Page 9-4

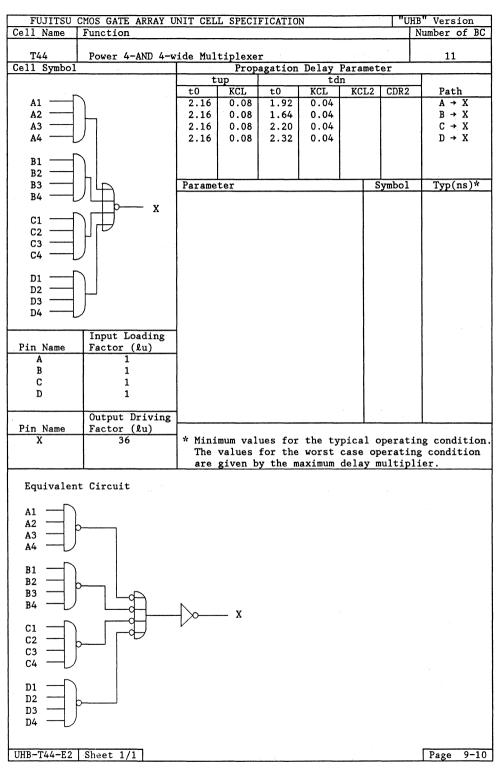
TILIT TOUR				n	.,		1 112	
	MOS GATE ARRAY U Function	NIT CEL	L SPECI.	FICATIO	N		11	IB" Version Number of BC
JOIL HAME								
T32	Power 3-AND 2-w	ide Mul	tiplexe	r				5
Cell Symbol				agation	Delay td		er	
		t0	KCL KCL	t0	KCL	n KCL2	CDR2	Path
		1.52	0.08	1.68	0.04	RODE	322	A + X
		1.52	0.08	1.80	0.04			B → X
A1 -	)							
A2	h							
A3 —	′ Ъ⊶ х							
В1 —	^							
В2 —	<del>                                     </del>						l	
В3 —	/							
		Parame	ter		L	<u> </u>	ymbol	Typ(ns)*
		101000					,	-55()
						ĺ		
Pin Name	Input Loading Factor (lu)							
A B	1 1							
ע	1							
	0-1					}		
Pin Name	Output Driving Factor (lu)							
X	36							
			_		. 1			, ,,,,
		* Mini	mum val values	ues for	the ty	pical o	operati neratir	ing condition. ng condition
		are	given b	y the m	aximum	delay r	nultip	lier.
	**************************************	·		-				
Equivalent	Circuit							
A1 —								
A2	<del></del>							
A3 —								
D1		<b>&gt;&gt;</b>	X					
B1 B2								
B3								
UHB-T32-E1	Sheet 1/1							Page 9-5
011D 105 D1	D11060 1/1							

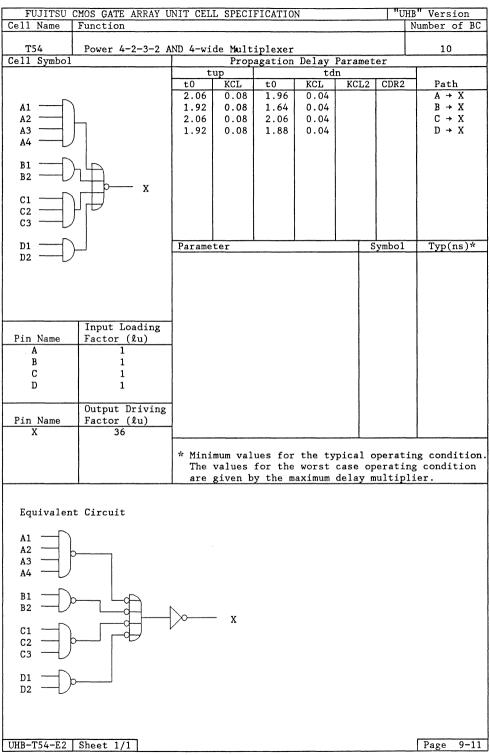
FULL COL	WOO CAME ADDAY U	NITE CEL	CDECT	ETCATTO			1 117.77	TD !!
	MOS GATE ARRAY U	NII CEL	L SPECI	FICATIO	N		1 01	HB" Version Number of BC
JOZZ MAINE								DCI OI DC
T33	Power 3-AND 3-w	ide Mul	tiplexe	r				7
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up KCL	t0	KCL KCL		CDD2	- B-+1
		t0 1.75	0.08	1.66	0.04	KCL2	CDR2	Path A → X
		1.75	0.08	1.78	0.04			B → X
		1.75	0.08	1.95	0.04			C → X
A1								
A2 A3								
l as								
B1 —	4							
B2	——— x							
B3 —								
C1 —								
C2								
C3 —		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)							
A	1							
В	1							
С	1							
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
	1	* Mini	mum val	ues for	the tv	pical o	perati	ing condition.
		The	values	for the	worst	case op	eratir	ng condition
		are	given b	y the m	aximum	delay m	ultipl	lier.
1								
INID TOO DE T	Ch - + 1/1							Page 9-6
UHB-T33-E1	Sheet 1/1							Page 9-6



	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version Number of BC
CEIT Mame	ruiccion							Od 10 redumer
T42	Power 4-AND 2-w	ide Mul	tiplexe	r				6
Cell Symbol				agation			er	·
		t0	up KCL	t0	KCL KCL	n KCL2	CDR2	Path
		1.60	0.08	1.88	0.04	RODE	OBAL	A + X
		1.60	0.08	2.00	0.04			B → X
A1	\							
A2 -								
A3	П							
A4 —	/ <del>L</del>				,			
B1 —	x — x						1	
B2								
В3 —								1
B4 —	)	D	<u> </u>			L	\h_1	T ()*
		Parame	rer			-   -	Symbol	Typ(ns)*
İ						l		
1								-
	Input Loading					1		1
Pin Name	Factor (lu)							
A	1					J		
В	1					1		
						1		
Din Nama	Output Driving							
Pin Name X	Factor (lu)	1						
		<b> </b>						
		* Mini	mum val	ues for	the ty	pical o	operati	ng condition.
		The	values	for the	worst	case of	peratin	g condition
	<u> </u>	ı are	given b	y the m	aximum	deray i	nurcipi	Tel.
Equivalent	Circuit							
_								
A1 -								
A2 — Þ								
A4 —								
		<del></del>	X					
B1 -								
B2 D								
B3 -								
UHB-T42-E1	Sheet 1/1							Page 9-8

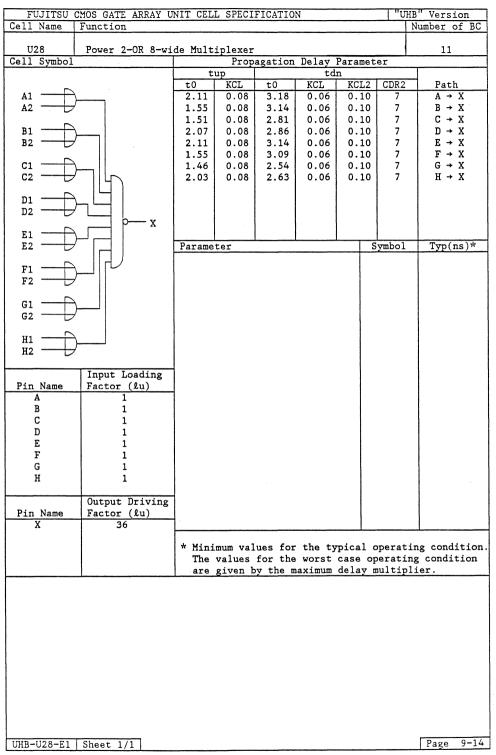






DULTEROU C	WOO CAME ADDAY II	NITT CET	T CDECT	CTCAMTO	,		1 11777	ITD II II
	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	N		1 01	HB" Version Number of BC
				······································				
U24	Power 2-OR 4-wi	de Mult	iplexer				İ	6
Cell Symbol			Prop	agation	Delay :	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.00	0.08	1.80 1.75	0.05 0.05	0.08 0.08	7 7	$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		1.44	0.08	1.78	0.05	0.08	7	$C \to X$
A1 —		1.38	0.08	1.70	0.05	0.08	7	$D \rightarrow X$
A2	$\vdash$	1.30	0.00	1.70	0.05	0.00	'	1 2
В1 —	۲ [							
B2 -	<b>′</b> Ц ).							
	→ x						1	
C1	$\forall AJ$						ł	
C2 —								
D1	\							
D2 -	<del>)</del>	Parame	ter			l s	ymbol	Typ(ns)*
	T==== T == 3.5 =	1						
Pin Name	Input Loading Factor (lu)							
A	1							
В В	i							
C	1							
ם	1							
	Output Driving							
Pin Name	Factor (lu)	-						
Х	36							
		* Mini	mum val	nes for	the tv	nical d	perat	ing condition
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
		<del>-</del>						
1								
1								
1777 VO / 75	(1)							Dags 0 12
UHB-U24-E1	Sheet 1/1							Page 9-12

FULLWAY CHOC CATE ADDAY I	NIT CEL	CDECT	CTC ATTO	NT.		1177	IID II Wanadan
FUJITSU CMOS GATE ARRAY U Cell Name   Function	NII CEL.	L SPECI.	FICATIO	N		1 0	HB" Version Number of BC
U26 Power 2-OR 6-wi	de Mult	Prop	agation	Delay	Paramet	<u> </u>	9
Gell Symbol	t	up	agacion	td		e1	
	t0	KCL	t0	KCL	KCL2	CDR2	
A1 A2	2.00 1.55	0.08	2.34 2.26	0.05	0.08	7	$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
	2.04	0.08	2.40	0.05	0.08	7	$C \rightarrow X$
B1	1.58	0.08	2.40	0.05	0.08	7	D → X
B2	1.64 2.10	0.08	2.58 2.58	0.05	0.08	7	$\begin{array}{c c} E \rightarrow X \\ F \rightarrow X \end{array}$
	2.10	0.00	2.30	0.05	0.00		
C2 — — — — — — — — — — — — — — — — — — —							
D1 — X							
E1 E2	Parame	ter		l	L .	ymbol	Typ(ns)*
			·				-,,,,,,,,
F1 F2							
F2 0							
Input Loading							
Pin Name   Factor (lu)							
A 1					1		
B 1 1							
D 1					- 1		
E 1							
F 1							
Output Driving							
Pin Name Factor (lu) X 36					- 1		
X 36							
							ing condition.
	The are	values given b	tor the v the m	aximum	case op delav m	eratı ultip	ng condition
<u> </u>		<u> </u>					
							1
							D 0.10
UHB-U26-E1   Sheet 1/1							Page 9-13



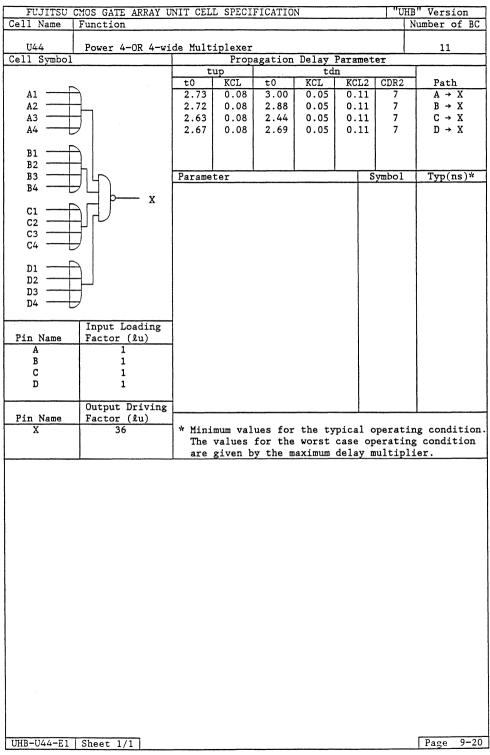
FILTER: C	MOC CAME ADDAY I	DITT CET	CDECT	CTC LETO	17		1 117.777	B" Version
Cell Name	MOS GATE ARRAY T	JNII CEL	L SPECI.	FICATIO	N		I UH	Number of BC
CELL MAME	I MICCIOII							tramper of bo
U32	Power 3-0R 2-w:	ide Mult	iplexer				1	5
Cell Symbol		T	Prop	agation	Delay	Paramet	er	
		t	up		td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.15	0.08	1.66	0.05	0.08	7	A → X
		2.11	0.08	1.63	0.05	0.08	7	$B \rightarrow X$
		1						
_		1 1						
A1 —								
A2	7							
A3 —	<u>[</u>	1 1						
_	x				i			
B1 —								
B2								1
В3 —								
		1 1						1
		Parame	ter			S	ymbol	Typ(ns)*
								1 1
						1		
						1		
		4						
D/- V	Input Loading					ł		
Pin Name	Factor (lu)	4						1
A B	1							
Д								
	Output Driving	1						
Pin Name	Factor (lu)							
X	36	1						
		* Mini	mum val	ues for	the tv	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	v the m	aximum	delav m	ultipl	ier.
	·····	<u> </u>	<u> </u>	<del>*************************************</del>				
								•
UHB-U32-E1	Sheet 1/1							Page 9-15

EUTTEU (	TWOC CATE ADDAY I	NITT CELL C	DECTE	TCATTO	,	<del></del>	1 17111	iB" Versi	
	MOS GATE ARRAY U	NII CELL S	PECIF	ICATIO	<u> </u>		I UI	Number o	of BC
U33	Power 3-OR 3-wi	de Multipl	exer					7	
Cell Symbol			Propa.	gation	Delay:		eI	<del></del>	
		tup t0 F	CL	t0	KCL	KCL2	CDR2	Path	,
			0.08	2.28	0.05	0.11	7	A +	
			80.0	2.38	0.05	0.11	7	B →	
		2.31	0.08	2.52	0.05	0.10	7	C →	Χ .
A1 A2	<u> </u>	1							
A3 —				l					
			1	ļ					
B1 -	147								
B2	р—— х			1					
В3	P	1		1					
C1 —	.			l					
C2 -	H								
C3 —		Parameter				S	ymbol	Typ(r	ıs)*
		1							
	T								
Pin Name	Input Loading Factor (lu)					'			
A	1					ļ			
В	1							-	
C	1	l							
								l	
	Output Driving	1				.			
Pin Name	Factor (lu)					1.			
Х	36								
:		* Minimur	1	f	+1			d.	
-		The va	n valu lues f	or the	worst	case or	perat. erati:	ng condi	tion
					aximum				
									*
	Sheet 1/1							Page	9-16

EUITTCU C	MOC CATE ADDAY II	NITT CEL	CDECT	CICATIO	NT .		1 117711	D" Vonedon
	MOS GATE ARRAY U	NII CEL	u areul	LICALIO	IN		1 OH	B" Version Number of BC
U34	Power 3-OR 4-wi	de Mult	iplexer					9
Cell Symbol				agation		<b>Parame</b> t	EI	
		t0 t	up KCL	t0	td KCL	n KCL2	CDR2	Path
		2.11	0.08	2.98	0.06	0.10	7	$A \rightarrow X$
		2.13	0.08	3.00	0.06	0.10	7	B + X
A1 —		1.92	0.08	2.44	0.06	0.10	7	C → X
A2 -		2.11	0.08	2.69	0.06	0.10	7	D + X
A3								
В1 —								
B2								
В3 —								
_	_ р— х							
C1	J d J							
C2 C3	- -							
		Parame	ter		Ŀ	l s	ymbol	Typ(ns)*
D1 -							<u> </u>	- · · · · · · · · · · · · · · · · · ·
D2 -								
D3 ———								
						1		
	Input Loading					- 1		
Pin Name	Factor (lu)							
A	1							
В	1					l		
C D	1							
, b	1							
	Output Driving							
Pin Name	Factor (lu)					1		
X	36							
		- w	1					
		The	monnas Monnas	ues ior for the	the ty	DICAT C	perati	ng condition.  ng condition
		are	given b	v the m	aximum	delay m	ultipl	ier.
	<u> </u>		8				-	
1								
								;
								D. 0.13
UHB-U34-E1	Sheet 1/1							Page 9-17

FUJITSU C	MOS GATE ARRAY U	NIT CELL SPE	CIFICATIO	N		l "UHB	" Version
	Function					N	umber of BC
· U42	Power 4-OR 2-wi	de Multiplas	er			1	6
Cell Symbol	TOWEL 4-OR Z-WI	Pr	opagation	Delay F	aramete	er	U
		tup		tdr	1		
		t0 KCI 2.60 0.0		0.05	KCL2 0.08	CDR2	$\begin{array}{c c} Path \\ A \rightarrow X \end{array}$
		2.53 0.0		0.05	0.08	7	$B \rightarrow X$
					]		*
					l		
A1	4				1		
A2	<b>├</b> ,						
A3 A4	7 1 _	Parameter			S	ymbol	Typ(ns)*
A4 U	´ ⅓)> x						
B1 -	1 [						
B2 B3	구						
В4 —	)						
	Input Loading						
Pin Name	Factor (lu)						
A	1						
В	1						
							ļ
Pin Name	Output Driving Factor (lu)						<u> </u>
X	36	* Minimum v	alues for	the typ	oical o	peratin	g condition
		The value	s for the	worst o	ase op	erating	condition
	1	are giver	by the m	aximum o	петау ш	urtipii	er.
		-, -					
UHB-U42-E1	Sheet 1/1						Page 9-18

FULLTCU	CHOC CATE ADDAY I	NITE CELL	CDECT	ETCATTO	<del>.,</del>		1777	un" u
Cell Name	CMOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	N		1 0	HB" Version Number of BC
			. ,					
U43 Cell Symbol	Power 4-OR 3-wi	de Mult:	iplexer	ocation	Delay 1	Paramat		9
Cell Symbol		tı	up riop	agation	tdi		eı	- <del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.57	0.08	2.13	0.06	0.08	7	A + X
A1 ——	$\rightarrow$	2.62	0.08	2.26 2.39	0.06	0.08	7	$\begin{array}{c} B \rightarrow X \\ C \rightarrow X \end{array}$
A2		2.,,	0.00	2.37	0.00	0.00	,	, ,
A3								
A4 —	7							
В1 ——	7 In	Parame	ter		1	T S	ymbol	Typ(ns)*
B2 -	<del></del>							-3.5 \/
В3	$\exists \exists \exists x$							
B4 ——		1						
C1 —	7							
C2								1
C3 —	7							
U- L	/							
								1
	Input Loading	1				l		
Pin Name	Factor (lu)					ļ		1
A	1							
B C	1 1							
J	1							
Die Name	Output Driving							
Pin Name X	Factor (lu)	* Mini	num val	ues for	the tv	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati:	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.
UHB-U43-E1	Sheet 1/1							Page 9-19
UND-U43-E1	Direct 1/1							11050 7 17



## **Clock Buffer Family**

Page	Unit Cell Name	Function	Basic Cells
2-109	K1B	True Clock Buffer	2
2-110	K2B	Power Clock Buffer	3
2-111	К3В	Gated Clock (AND) Buffer	36
2-112	K4B	Gated Clock (OR) Buffer	36
2-113	K4B	Gated Clock (NAND) Buffer	3
2-114	KAB	Block Clock (OR) Buffer	55
2-115	KBB	Block Clock (OR x 10) Buffer	30

2

		RAY UNIT CELL SPECIFICATION "UH							
Cell Name	Function							Number of BC	
K1B	True Clock Buff	er	P		Do 1	Darc		2	
Cell Symbol		t.1	up Prop	agation	Delay td		er		
		t0	KCL	t0	KCL	KCL2	CDR2		
		0.72	0.08	0.86	0.04			A → X	
								!	
	<b>N</b>								
Α	x								
	V								
		Parame	ter			S	ymbol	Typ(ns)*	
						-			
Die Name	Input Loading								
Pin Name A	Factor (lu)					1			
	-								
	Output Driving								
Pin Name	Factor (lu)					l			
Х	36								
		* Mini	miim ***a1	use for	the tw	nical o	norat	ing condition.	
		The	mum vai values	for the	worst	case or	erati	ng condition	
		are	given b	y the m	aximum	delay m	ultip	lier.	
F	-+ Cii+								
	nt Circuit								
A>	x								
	V								
UHB-K1B-E1	Sheet 1/1							Page 10-1	

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
Won.	D 011- D0							•
K2B Cell Symbol	Power Clock Buf	rer	Pron	agation	Dolay	Paramet	er l	3
OCII Bymboi		t	up	agacion	td	n	61	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.20	0.03			A → X
							1	
1								
	N							
Α	x							
		Parame	ter			S	ymbol	Typ(ns)*
	T							
Pin Name	Input Loading Factor (lu)							
A	1							
						1		
		}				ĺ		
	Output Driving	1						
Pin Name	Factor (lu)					İ		
Х	55							
			_	_				
}		* Mini	mum val	ues for	the ty	pical c	perati	ng condition. g condition
		are	values given b	v the m	aximum	delay m	mltipl	g condition
		, 410	0	, 11				===:
Equivalen	t Circuit							
A — >	x							
	V							
UHB-K2B-E1	Sheet 1/1							Page 10-2

FILITTEIL C	MOS GATE ARRAY U	NIT CEL	CDECT	ETCATTO:	NI.		"IIIII	B" Version
	Function	NII CEL	L SPECI	FICALIO	I.A.		1 011	Number of BC
COLL Hame	1 0110 0 1 011				, CLIDCE OI DO			
кзв	Gated Clock (AN	D) Buff	er				1	2
Cell Symbol			Prop	agation	Delay	Paramet	er	
		tı	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.00	0.08	1.00	0.04			A + X
4.4 F	_							i i
A1 —	)—— x							
A2	) <del>"</del>							
		Parame	ter	لـــــــــــا		7 9	ymbol	Typ(ns)*
		rarame					J. III.O. I	1,50(5)
						1		1
						l		
						1		
	T							1
<b>5.</b>	Input Loading					ı		
Pin Name	Factor (lu)							1
A	1 1					[		
	]					1		
						1		
	Output Driving							
Pin Name	Factor (lu)							
X	36							<u> </u>
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl.	ier.
Equivalent	: Circuit							
A1 —	N							
	→ x							
A2 —	V							
UHB-K3B-E2	Sheet 1/1						-	Page 10-3

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"ਪਸ	B" Version
Cell Name	Function							Number of BC
K4B Gated Clock (OR) Buffer						2		
Cell Symbol Propagation Delay Parameter						ter		
		t	up	-8	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.78	0.08	1.14	0.05	0.07		A → X
	,							1
							-	
							1	
							1	
A1 ————————————————————————————————————	x							
A2			•					
							İ	
			<u> </u>			L		
		Parame	ter				Symbol	Typ(ns)*
						l		
						l		
						ı		
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1							
								]
	Output Driving							
Pin Name	Factor (lu)							
X	36							<u> </u>
		" Mini	mum vai	tor the	the ty	bicar	operati	ng condition. g condition
1		are	varues viven h	v the m	aximum	delav	multipl	ier.
			811011	y 0110 L		4014)		
}								
Equivalent	t Circuit							
A1 —	~ x							
A2	~ \\ \ \ \ \ \							
1								
								(B) 10 /
UHB-K4B-E1	Sheet 1/1							Page 10-4

FILITSII	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		"ITH	B" Version
Cell Name	Function	IVII ODD	D DI DOI	1100110	.,			Number of BC
K5B	Gated Clock (NA	ND) Buf	fer				1	3
Cell Symbol				agation			er	- <del></del>
			up		td		anna	
		t0	KCL	t0	KCL	KCL2	CDR2	Path   A → X
		1.14	0.08	1.48	0.04			$A \rightarrow X$
								1
								1
	_							
A1	) <del></del> х							
A2	^							
		Parame	ter	L	L	l s	ymbol	Typ(ns)*
		1 ar ame					,	1 275(22)
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)	1						
A	1	1						
								1
	Output Driving					.		
Pin Name	Factor (lu)					ļ		
Х	36							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case of	eratin	g condition
	1	are	given b	y the m	aximum	delay m	ultipl	ier.
F								
Equivalen	t Circuit							
A1	~ / / <sub>~</sub>							
A2 —		— х						
	•							
UHB-K5B-E2	Sheet 1/1							Page 10-5

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		UH	B" Version Number of BC
Cell Mame					Number of BC			
KAB Coll Symbol								3
Cell Symbol		tı	up Prop	agation	Delay td	raramet n	er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.08	0.04	1.85	0.03			A → X
							ļ	
A1	$\triangle$							
A2	x						Ì	
	1						]	T ()*
		Parame	ter			<del></del>	ymbol	Typ(ns)*
Pin Name	Input Loading Factor (lu)							
A	1							
								ŀ
	Output Driving					- 1		
Pin Name X	Factor (lu)	}				İ		
•								<del></del>
		* Mini	mum val	ues for	the ty	pical o	perati	ing condition.
		are	values given h	or the m	aximum	delav n	peration	ng condition
			821011	,				
Equivalen	t Circuit							
A1 ——								
A2	р——d>—— х							
	·							
1								
UHB-KAB-E2	Sheet 1/1							Page 10-6

FILITTSIL	CMOS GATE ARRAY U	NIT CELL SPECT	FICATIO	N	Т	"UHB" Version
	Function	HII ODDI DIECI	I IOAI IO.			Number of BC
		(OD 15)				
KBB Cell Symbol	Block Clock Buf	rer (UK X 10)	agation	Delav	Parameter	30
JOIL DYMESOL		tup		td		
	:	tO KCL	t0	KCL	KCL2 CI	DR2 Path
		1.34 0.04 1.08 0.04	2.08 1.85	0.03		CK → X IH → X
Γ		1.00	1.03	0.05		1
CK -						
IHO —	xo					
IH1	x1					
IH2	X2					
IH3 IH4	X3 X4					
IH5	x5					
IH6	X6					
IH7 IH8	X7 X8	Parameter			Syml	bol Typ(ns)*
IH9	X8	1 al ametel			- J Symi	тур(па)
L						
	<b>.</b>					
Pin Name	Input Loading Factor (lu)					
CK	10					
IH	1					
	Output Driving					
Pin Name X	Factor (lu)					
Α.						
		* Minimum val	ues for	the ty	pical ope	rating condition.
		are given b	for the m	aximum	delav mul	ating condition
		<u>ure 811011 2</u>	<i>y</i> <b>0</b> 110 11			327222
	······································					<u> </u>
UHB-KBB-E1	Sheet 1/2					Page 10-7

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name KBB Equivalent Circuit CK IHO - xo IH1 -IH2 IH3 . IH4 -IH5 -IH6 IH7 -IH8 IH9 Page 10-8 UHB-KBB-E1 | Sheet 2/2

## Scan Flip-Flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basic Cells
2–119	SDH	Scan D FF with 2:1 Multiplex with Clear and Clock Inhibit	14
2–122	SDJ	Scan D FF with 4:1 Multiplex with Clear and Clock Inhibit	15
2–125	SDK	Scan D FF with 3:1 Multiplex with Clear and Clock Inhibit	16
2-128	SJH	Scan J-K F with Clear and Clock Inhibit	36
2–131	SDD	Scan D FF with 2:1 Multiplex, Preset Clear, and Clock Inhibit	16
2-135	SDA	Scan 1-input D FF with Clock Inhibit	12
2-138	SDB	Scan 1-input D FF with Clock Inhibit	42
2-142	SHA	Scan 1-input D FF with Clock Inhibit	68
2–145	SHB	Scan 1-input D FF with Clock Inhibit and Q Output	62
2–148	SHC	Scan 1-input D FF with Clock Inhibit and XQ Output	62
2–151	SHJ	Scan D FF with 2:1 Multiplex and Clock Inhibit	78
2–154	SHK	Scan D FF with 3:1 Multiplex and Clock Inhibit	88

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N .		<b>"</b> U	HB" Version
Cell Name	Function							Number of BC
SDH	SCAN 2-input DF	F with						14
Cell Symbol				agation			ter	····
			up		td		T === :	
		t0	KCL	t0	KCL	KCL2		
		3.72	0.08	2.98	0.04	0.08		CK, IH → Q
		2.35	0.08	2.15	0.06	0.12		CK,IH → XQ
		3.79	0.08	1.07	0.04	0.08	7	CL → Q,
A1							Ì	XQ
A2								
CK	Q						i	
1							į	
IH —							1	1
GT							l	
SI	vo						1	
A ——	р—— xq	Parame				ــــــ	Svmbol	T ()*
				2 4 4 14			tCW	Typ(ns)* 5.4
	Y	Clock Pulse Width Clock Pause Time					tCWH	4.5
		Clock rause lime					CCWII	+
	CL	Data Setup Time					tSD	3.7
	OH	Data Hold Time					tHD	1.0
		Data II	010 111		<del></del>			
		Clear	Pulse W	idth			tLW	4.5
			Release				tREM	3.0
	Input Loading		Hold Ti				tINH	1.5
Pin Name	Factor (lu)						<u> </u>	
A1,A2	1							ŀ
CK	ī							
IH	ī					i		
CL	3	1						
SI	i	1						
A,B	2	1				- 1		
		1						
		1				1		1
		1				1		
	Output Driving	1				1		
Pin Name	Factor (lu)							
Q	36	* Mini	mum val	ues for	the ty	pical	operat	ing condition.
xQ	36							ng condition
,				y the m				
			0					

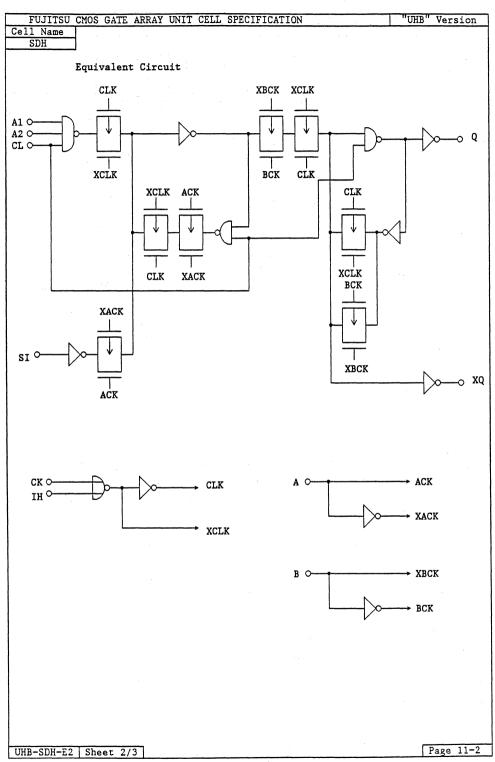
## Function Table

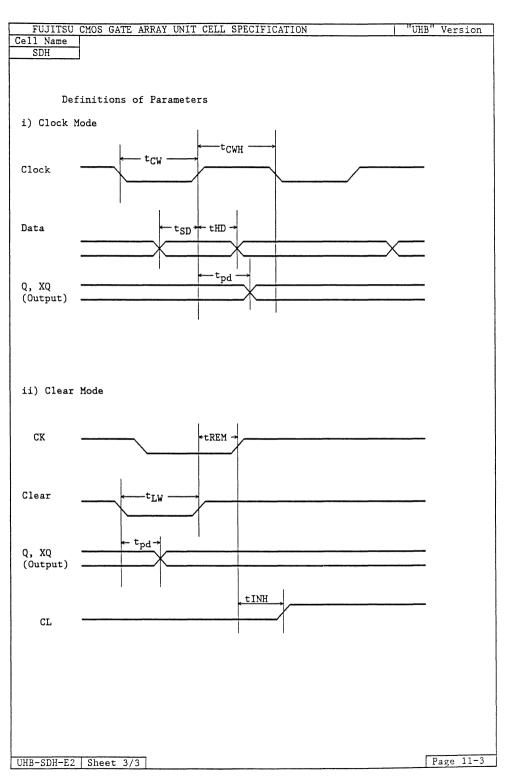
UHB-SDH-E2 | Sheet 1/3

MODE			IN	PUT			ou.	rput -
	CLK	CL	D	A	В	SI	Q	ΧQ
CLEAR	х	L	Х	х	х	x	L	н
CLOCK	L→H	Н	Di	L	L	х	Di	Di
	н	Н	x	L	L	X	Q <sub>0</sub>	$XQ_0$
SCAN	н	н	X	L→H→L	Н	Si	Q <sub>0</sub>	XQ.
	Н	Н	Х	L	H→L→H	Х	Si	Si

Note : CLK = CK + IH  $D = A1 \times A2$ 

Page 11-1





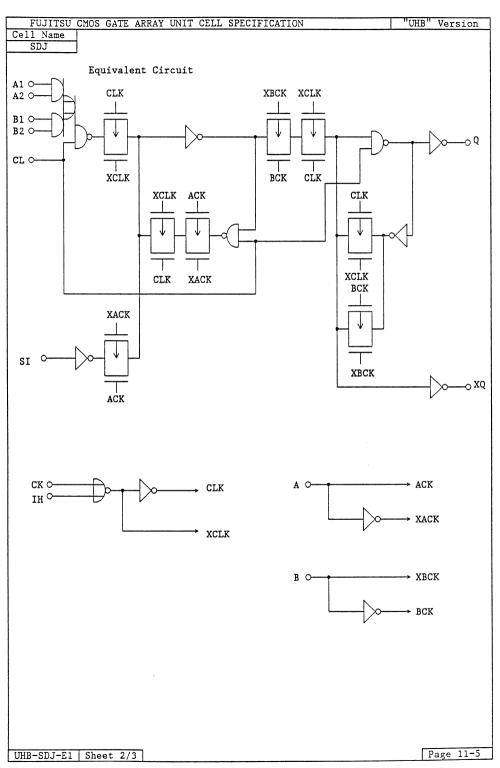
FUJITS	U CMOS	GATE A	RRAY I	INIT CEI	LL SPEC	IFICATION	ON.		<del></del>	'UHB'	Version
Cell Name	Func			02.	0120						umber of BC
SDJ	SCA	N 4-in	put DI	FF with	Clear	& Clock	-Inhibi	t			15
Cell Symb				1		pagation			meter		
				1	tup			dn			
1				t0	KCL	t0	KCL	KC	L2   CDR	₹2	Path
l				2.75	0.08	3.02	0.04	0.	08 7	7	CK, IH → Q
				2.36	0.08				12 7	,	CK, IH → XQ
		_		3.74	0.08	,		,	,		CL → Q,
A1				3.74	"."	1.00	"."	"	"		XQ XQ
A2		1		l	İ					- 1	nq
B1			Ġ.	1	1			1			
I		1	Q	i	İ	1				1	
B2								1			
CK -				1			i	1	ı		
IH —	1			1	1		į.				
		L		1							
si —		p—	XQ		<u> </u>						
A	1			Parame					Symbo	)1	Typ(ns)*
В —	1			Clock	Pulse	Width			tCW		5.4
	<del>-                                    </del>			Clock	Pause	Time			tCWH	I	4.5
ł											
				Data	Setup T	ime			tSD		4.4
	$\mathtt{CL}$			Data 1	Hold Ti	me			tHD		0.8
1				Clear	Pulse	Width			tLW		4.5
					Releas				tREM	1	3.0
	Inp	ut Loa	ding		Hold T				tINH		1.5
Pin Name		tor (l									
A1,A2	- 1.00	1		1						- 1	
B1,B2		ī									
CK	1	ī		l							
IH		i									
CL	Į.	3								- 1	
SI	į.	1		1						- 1	
		2									
A,B		2		1							
				]						1	
ļ		D-		-						1	
Din Name		put Dr									
Pin Name	Fac	tor (l	.u)	- w		1 6.			1		
Q	1	36		" min	ımum va	lues Io	r the t	ypica	1 opera	tin	g condition.
XQ		36		Ine	values	IOT th	e worst	case	operat	ing	condition
ļ				are	given	by the	maximum	dela	y multi	rbire	er.
Function	n Tabla										
Tunctio	n labie										
									٦		
MODE			IN	PUT			OUT	PUT			
									7		
	CLK	CL	D	A	В	SI	Q	XQ			
									7		
CLEAR	X	L	X	X	X	X	L	H			
									7		
CLOCK	L→H	H	Di	L	L	X	Di	Di	_1		
									1		
	Н	Н	Х	L	L	X	Q <sub>0</sub>	$XQ_{o}$	1		
							<u> </u>		4		
SCAN	Н	Н	Х	$L\rightarrow H\rightarrow L$	Н	Si	Q <sub>0</sub>	$XQ_{o}$	1		
			-						4		
	н	Н	Х	L	H→L→H	Х	Si	Si			
					***************************************						

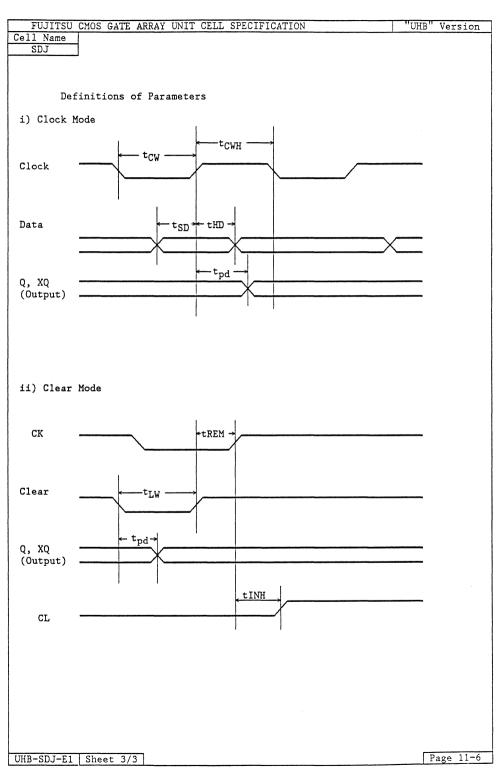
UHB-SDJ-E1 | Sheet 1/3

Note : CLK = CK + IH

D = (A1 x A2) + (B1 x B2)

Page 11-4





FILITTEIL	CMOS GATE ARRAY U	NITT CEL	T CDECT	EICATIO	NT.			11 11	IB" Version
Cell Name	Function	NII CEL	L BIECI	FICATIO	IN .			<del>- 1</del>	Number of BC
3011	1 4110 0 1 0 11							$\dashv$	Number of be
SDK	SCAN 6-input DF	F with	Clear &	Clock-	Inhibit				16
Cell Symbol			Prop	agation	Delay	Paran	neter		
			up		td				
		t0	KCL	t0	KCL	KCI			Path
		3.70	0.08	3.00	0.04	0.0		7	CK,IH → Q
		2.32	0.08	2.16	0.06	0.1		7	CK, IH → XQ
A1 -		3.74	0.08	1.02	0.04	0.0	08	7	CL → Q,
A2 -									XQ
B1 -							1		
B2	- Q								
C1 -									
C2									
CK -									
IH —	vo								
sı —	р—— хо	Parana			Cromb	-1	Typ(ns)*		
A -		Parameter Clock Pulse Width					Symbol tCW		5.4
B ——		Clock Pause Time					tCW		4.5
		OTOCK TRUBE TIME							<del>                                     </del>
	Ĭ	Data Setup Time							5.0
		Data Hold Time							0.5
	CL				******				
		Clear	Pulse W	idth			tLW		4.5
			Release				tRE		3.0
	Input Loading	Clear	Hold Ti	me			tIN	H	1.5
Pin Name	Factor (lu)								
A1,A2	1	1							
B1,B2	1								
C1,C2	1								
CK	1								
IH	1								
CL	3								
SI	1 2								
A,B	2								
	Output Driving	ł							
Pin Name	Factor (lu)								
Q	36	* Mini	mum val	ues for	the tv	pica:	loper	ati	ng condition.
XQ	36								ng condition
	are given by the maximum delay multiplier.								

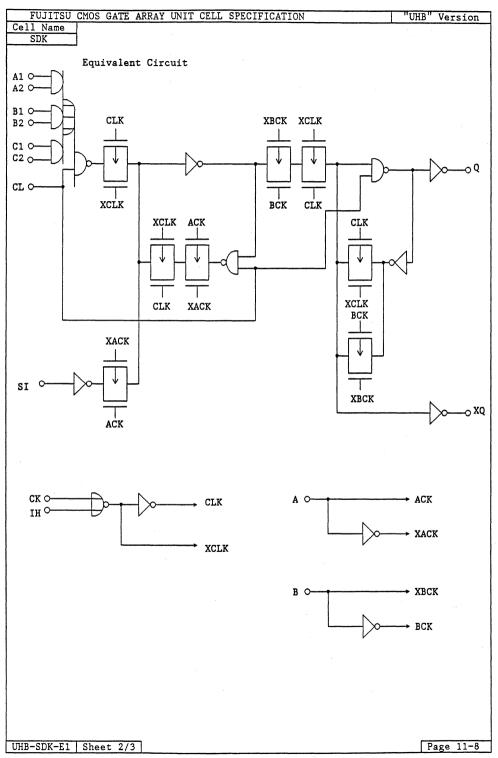
MODE			IN	PUT			OU.	rpur
	CLK	CL	D	A	В	SI	Q	ХQ
CLEAR	х	L	Х	Х	Х	X	L	Н
CLOCK	L→H	н	Di	L	L	X	Di	Di
	Н	Н	х	L	L	X	Q.	$XQ_0$
SCAN	Н	Н	Х	L→H→L	Н	Si	Q <sub>0</sub>	XQ₀
	Н	Н	Х	L	H→L→H	Х	Si	Si

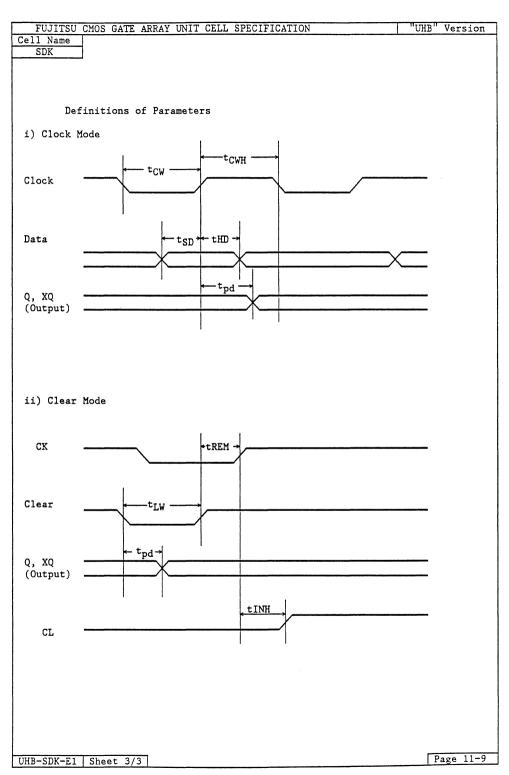
Note : CLK = CK + IH

D = (A1 x A2) + (B1 x B2) + (C1 x C2)

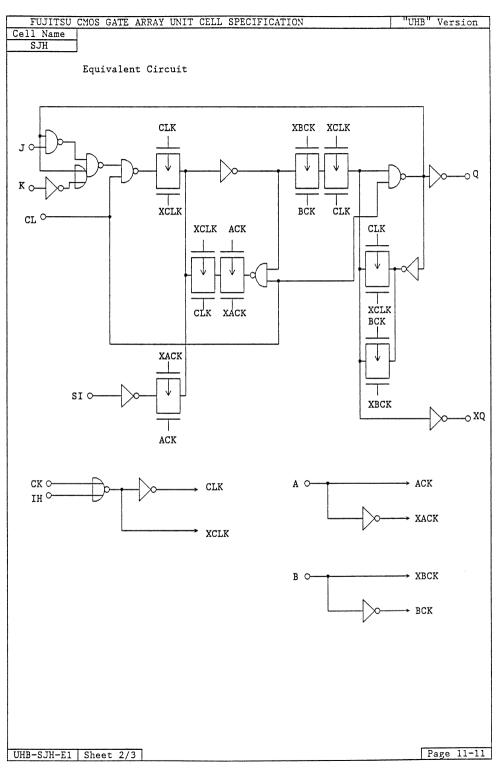
Page 11-7

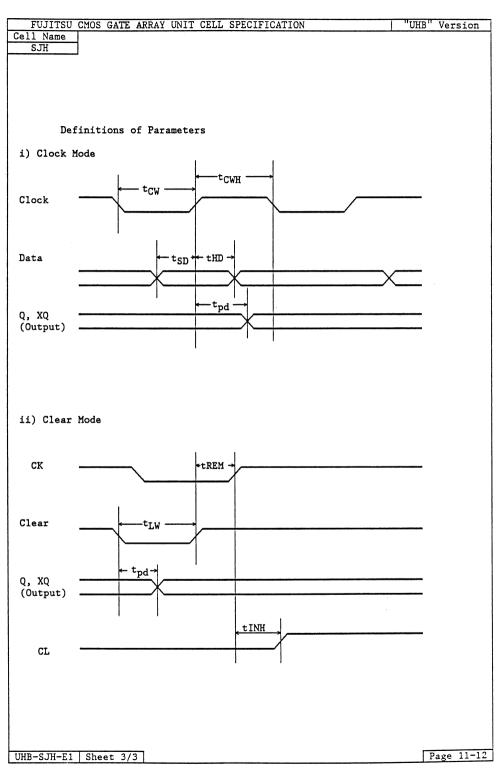
UHB-SDK-E1 | Sheet 1/3





FUJITS	J CMOS	GATE A	RRAY U	NIT CE	LL SPEC	CIFICA'	TION				'UH	B" Version	
Cell Name	Func	tion										Number of BC	
SJH	SCA	N J-K	FF wit	h Clea	r & Clc	ock-Inl	hibi	t				16	
Cell Symbo					Pro			Delay		neter			
				+0	tup   KCL	+		td KCL		0   CDI	22	D.+1	
				t0 4.24		t0		0.04	KCI 0.0		7	Path CK,IH → Q	
				2.36			16	0.06	0.1		7	CK, IH → XQ	
				3.76	0.08	3 1.3	39	0.04	0.0	08   7	7	CL → Q,	
J												XQ	
ck —			Q	Param	eter				<u> </u>	Symbo	1	Typ(ns)*	
IH —					Pulse	Width	-			tCW		5.4	
				Clock	Pause	Time				tCWI	ĭ	4.5	
SI —		b	XQ	Data	Setup 7	Cimo (	J)			tSD		4.4	
В —			ΛŲ		Setup 1					tSD		4.8	
	- γ			Data Hold Time (J,K) tHD								0.5	
				C1	D11-5	13:24-1-				<b>±</b> ₹₹?		/ -	
	CL			Clear Pulse Width tLW Clear Release Time tREM							1	3.0	
					Clear Hold Time tINH 1.5								
	T 7	T	31						İ				
Pin Name		ut Loa tor (l							1				
J,K	1.00	1		1					1				
CK		1											
IH CL		1 3							l				
SI		1											
A,B		2											
	Out	put Dr	iving										
Pin Name	Fac	tor (l	u)			_	_	_					
Q XQ		36 36										ng condition. g condition	
					given								
Function	n Table												
				INPUT				T	OU.	TPUT .			
MODE	CLK	CL	J	К	A	В	SI		Q	XQ			
CLEAR	Х	L	X	Х	Х	x	X		L	Н			
	L→H	Н	L	L	L	L	X		L	Н	1		
	L→H	H	Н	Н	L	L	х		Н	L	1		
CLOCK	L→H	Н	L	н	L	L	X		Q <sub>0</sub>	XQ.			
	L→H	Н	 Н	 L		 L	X		XQ <sub>0</sub>	Q <sub>0</sub>	1		
	Н	H	X	X	L	L	X		Q <sub>0</sub>	XQ.	1		
SCAN	Н	Н	X	X	L→H→L	Н	Si		Q <sub>0</sub>	XQ <sub>o</sub>	1		
	Н	Н	X	Х	L 1	H→L→H	Х		Si	Si			
			,		Note	e : CL	к =	CK + I	H			D - 11 10	
UHB-SJH-E	1   Shee	t 1/3	l									Page 11-10	





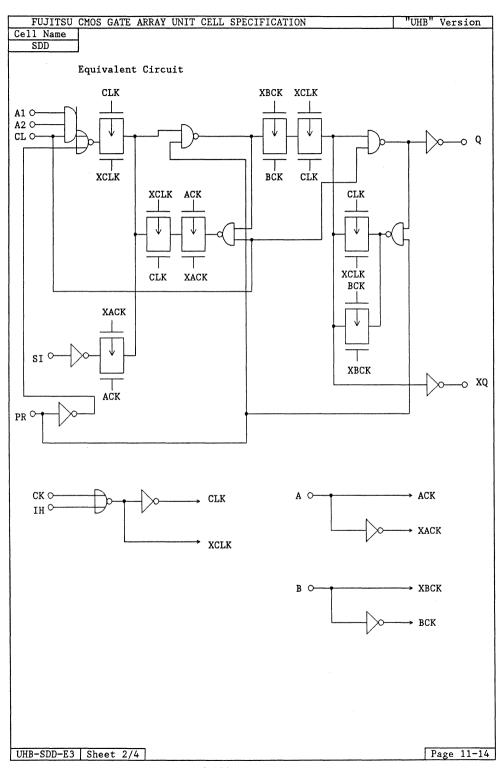
	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N				B" Version
Cell Name	Function								Number of BC
SDD	SCAN 2-input DF	Tth	Closs	Drocot	s. Clook	_Tnh	164+		16
Cell Symbol	BOAN 2-Input Dr	r with		agation					10
Cell Symbol		+	up	agation	td		neter		T
	PR	t0	KCL	t0	KCL	KCI	.2   CD	R2	Path
	I	3.70	0.08	3.22	0.04	0.0		7	CK, IH → Q
		2.65	0.08		0.04	0.:		7	CK, IH → XQ
	Ţ	4.50	0.08	1.02	0.04	0.0		7	$CL \rightarrow Q$
	<del></del>	7.50	0.00	1.02	0.04	0.1	"	•	XQ,
A1 -		3.84	0.08	2.35	0.06	0.3	, ,	7	$PR \rightarrow Q$
A2	Q	3.04	0.00	2.55	0.00	0	12	′	XQ,
CK -							1		AQ
IH —							- 1		
		Parame	ter			—т	Symb	01	Typ(ns)*
sı —			Pulse W	idth			tCW		5.4
Α	р xq		Pause T				tCW		4.5
в — ф		OTOCK	Tause 1	TIME			2011	111	<del> </del>
_	<u> </u>		Data Setup Time					)	5.4
	Ĭ		Data Hold Time					)	1.0
	l	Dava II	014 11						1
	CL	Clear	Pulse W	idth			tLW	1	5.0
			Release				tRE	:M	3.0
	Input Loading		Hold Ti				tIN		1.5
Pin Name	Factor (lu)	01001							
A1,A2	1	Preset	Pulse	Width			tPW	1	6.8
CK	1	Preset	Releas	e Time			tRE	M	3.7
IH	1		Hold T				tIN	IH.	1.0
CL	3			·					
PR	3					l			
SI	1					l			
A,B	2					1			
·									
						1			
	Output Driving								1
Pin Name	Factor (lu)								
Q	36	* Mini	mum val	ues for	the ty	pica:	l oper	ati	ng condition.
XQ	36	The	values	for the	worst	case	opera	ting	g condition
		are	given b	y the m	aximum	delay	y mult	ipl:	ier.

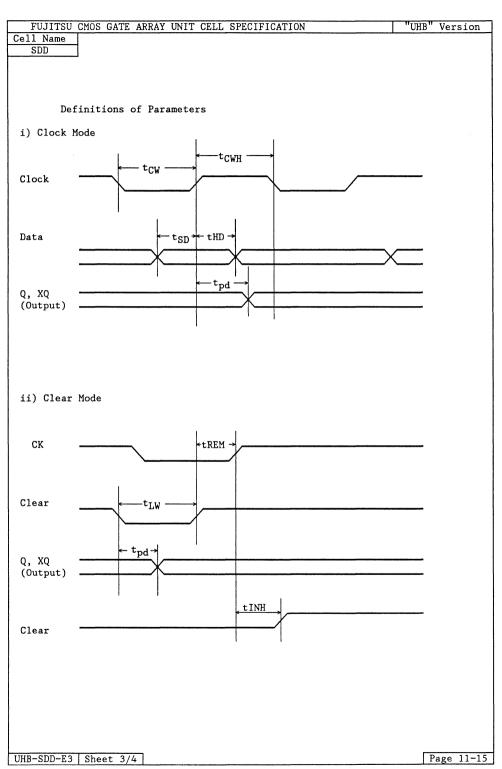
MODE				INPU	T			OU	rput
	CLK	CL	PR	D	A	В	sı	Q	XQ
CLEAR	Х	L	н	Х	Х	Х	Х	L	н
PRESET	х	Н	L	Х	х	Х	Х	Н	L
CLOCK	L→H	н	н	Di	L	L	х	Di	Di
	Н	Н	Н	х	L	L	х	Qo	ΧQο
SCAN	Н	Н	Н	Х	L→H→L	Н	Si	Q <sub>0</sub>	XQ <sub>0</sub>
	Н	Н	Н	Х	L	H→L→H	Х	Si	Si
CL/PR	х	L	L	Х	Х	Х	X	Proh	ibited

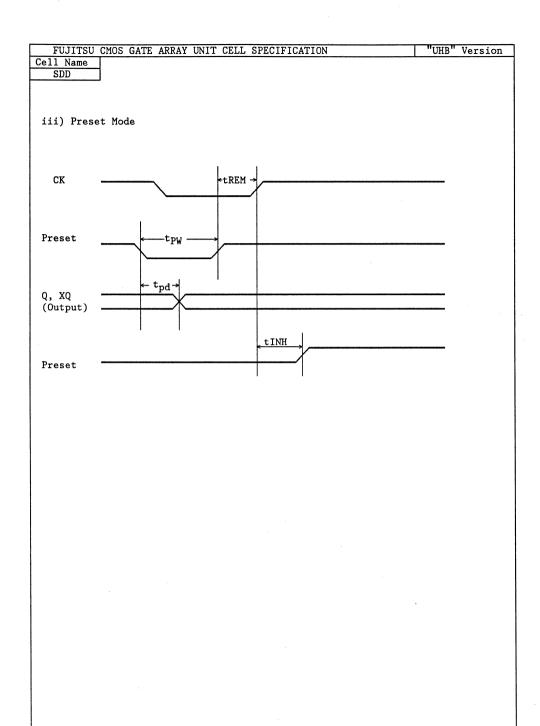
Note : CLK = CK + IH

 $D = A1 \times A2$ 

UHB-SDD-E3 Sheet 1/4







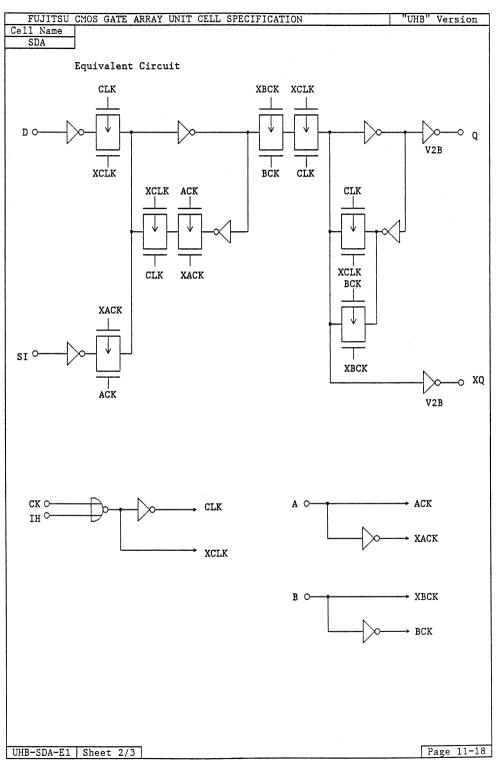
UHB-SDD-E3 | Sheet 4/4

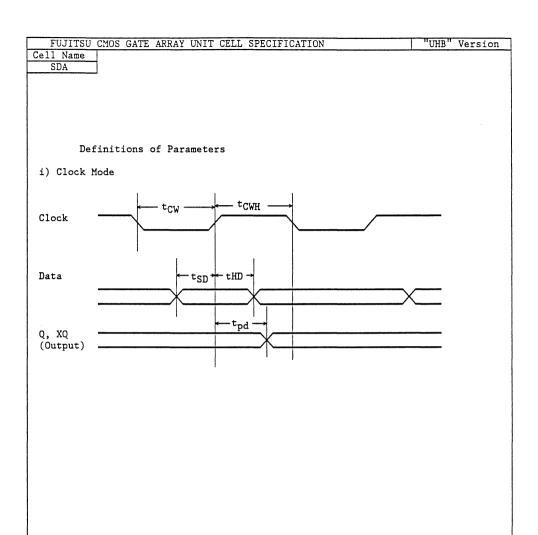
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		"[]	HB" Version
Cell Name	Function	1111 000	<u>D OIDOI</u>	1 1011110	· <u>'</u>			Number of BC
SDA	SCAN 1-input DF	F with						12
Cell Symbol				agation	Delay		eter	
			up		td			
		t0	KCL	t0	KCL	KCL:		
		3.18	0.08	3.00 2.17	0.04	0.0		CK, IH → Q
D CK IH SI	→ Q Q	2.33	0.08	2.17	0.06	0.1:	2 7	CK,IH → XQ
A ————————————————————————————————————		Parame	ter				Symbol	Typ(ns)*
-			Pulse W				tCW	5.4
		Clock	Pause T	ime			tCWH	4.5
			etup Ti old Tim				tSD tHD	3.5
		Data II	OIQ IIII	5			CIID	1.7
Pin Name	Input Loading Factor (lu)							
D D	ractor (Lu)							
cĸ	i							
IH	ī	1						
SI	1					į		
A,B	2							1
	Output Driving	ļ						
Pin Name	Factor (lu)			_				
Q	36							ing condition.
XQ	36							ng condition
	<u> </u>	are	given b	у спе ш	aximum	deray	шитстр	TTEL.

MODE			INPUT			OU.	rpur
	CLK	D	A	В	SI	Q	ХQ
CLOCK	L→H	Di	L	L	X	Di	Di
	н	x	L	L	x	Q.	XQ <sub>o</sub>
SCAN	Н	Х	L→H→L	Н	Si	Q.	XQ <sub>o</sub>
	Н	Х	L	H→L→H	Х	Si	Si

Note : CLK = CK + IH

UHB-SDA-E1 | Sheet 1/3





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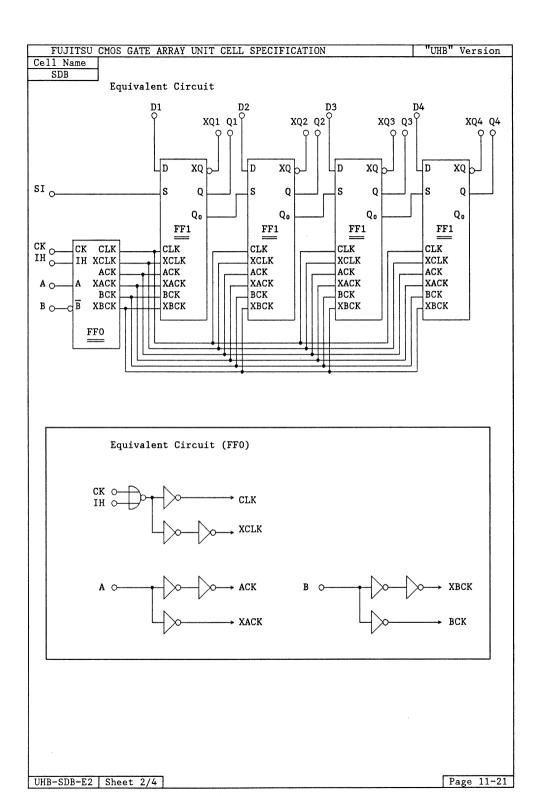
UHB-SDA-E1 | Sheet 3/3

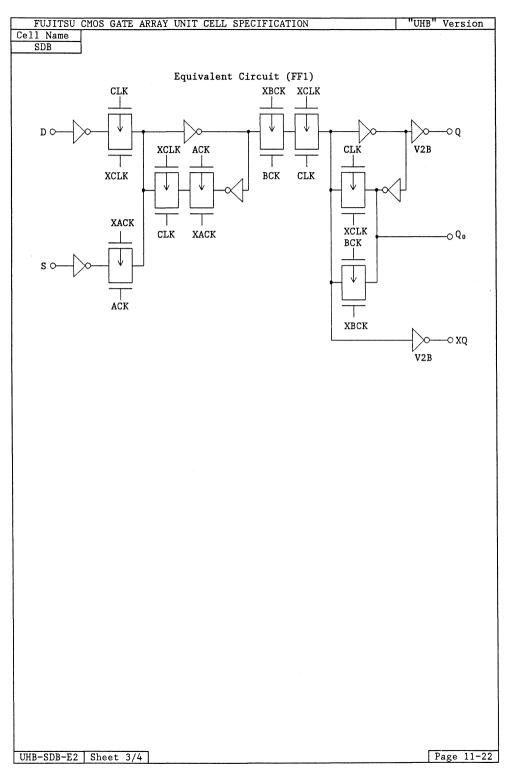
FILITCII	CMOS GATE ARRAY U	NIT CEI	T CDECT	EICATIO	NI :		— ги	IIID	" Version	
Cell Name	Function	NII CEL	L SPECI	FICATIO	IN				umber of	
GOII Name	Tunction		···					+*`	umber or	<u> </u>
SDB	SCAN 1-input 4-	bit DFF	with C	lock-In	hibit			1	42	
Cell Symbol	Joint L Lingue V	1			Delay	Param	eter			
		t	up	28401011	td		0001			
ĺ		t0	KCL	t0	KCL	KCL	2 CDR	2	Path	
1		4.24	0.08	3.94	0.04	0.0			CK,IH →	0
		3.25	0.08	3.32	0.06	0.1	2 7		CK,IH →	
	•								,	•
	4									
D1	Q1									
D2	þ— xQ1									
D3 —	Q2							- 1		
D4	þ xQ2									
ск —	—— Q3									
IH —	р <del></del> хоз									
si —	Q4	Parame					Symbo	1	Typ(ns)	*
A	р—— xQ4	Clock Pulse Width					tCW		6.8	
<b>В</b> — а		Clock Pause Time t					tCWH		5.0	
~ L										
			etup Ti				tSD		2.2	
		Data H	old Tim	e			tHD		3.3	
						- 1				
	т									
<b>.</b>	Input Loading									
Pin Name	Factor (lu)							l		
D	1									
CK	1									
IH	1	l								
SI	1									
A,B	2									
1		l						- 1		
	Output Driving	ł				i				
Pin Name	Factor (lu)	<b> </b>							L	
Q Q	36	* Mi==	miim 1701	ues for	the to	nice1	oners	+15	g conditi	00
xQ	36								conditio	
1 24	30		varues given b							11
ļ	1	are	Proen D	y cire ii	antillulli	ueray	muici	$\nu_{11}$	cr.	

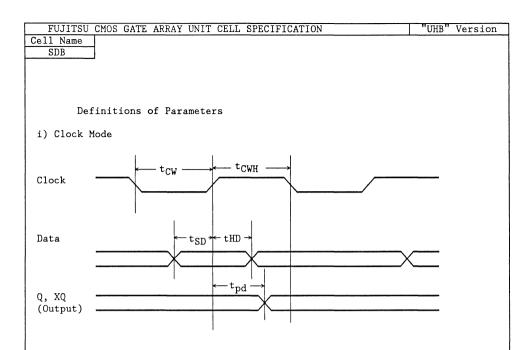
MODE			INPUT			OUT	PUT
	CLK	Dn	·A	В	SI,Qn-1	Qn	XQn
CLOCK	L→H	Di	L	L	X	Di	Di
	Н	x	L	L	х	Qn∘	XQn∘
SCAN	Н	Х	L→H→L	Н	Si	Qn∘	XQn∘
	Н	Х	L	H→L→H	Х	Si	Si

Note : CLK = CK + IH  $n = 1 \sim 4$ 

UHB-SDB-E2 | Sheet 1/4

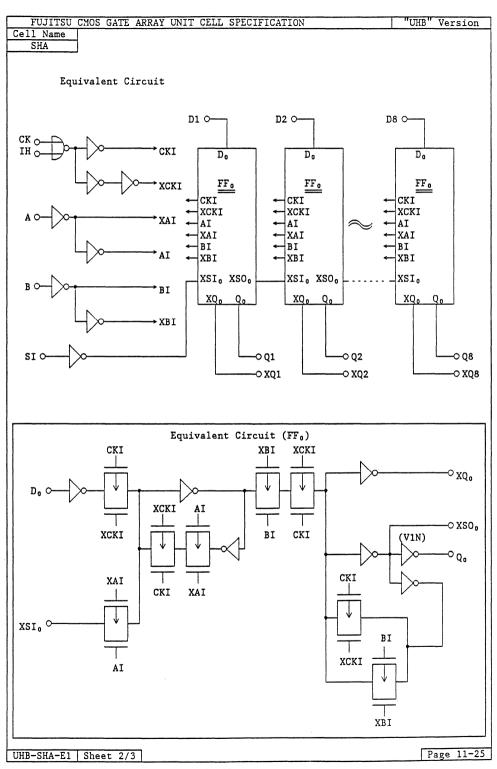


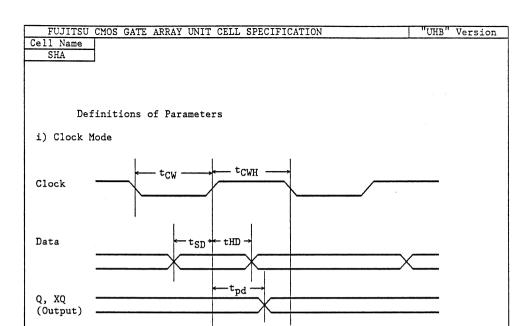




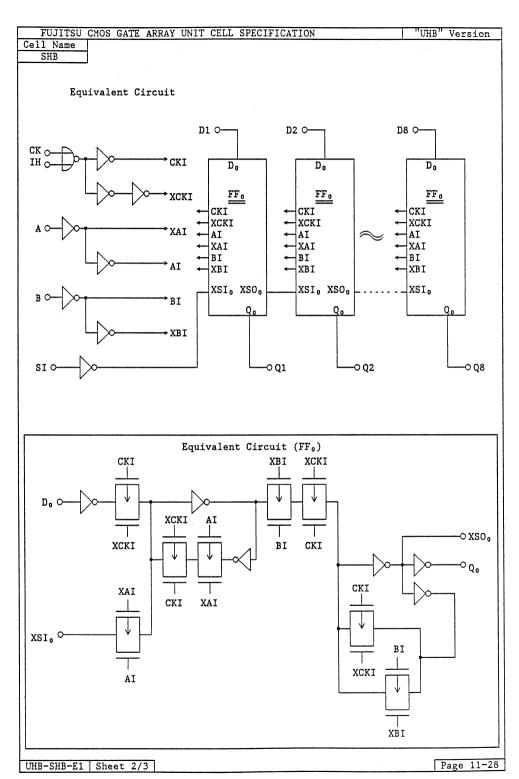
UHB-SDB-E2 | Sheet 4/4

FULLTSU C	MOS GATE ARRAY U	NIT CELL SPE	CIFICATIO	)N		"пн	B" Version
	Function	0000 010					Number of BC
SHA	SCAN 1	hi+ DEE+L	Clock-T-	h4h4+			68
Cell Symbol	SCAN 1-input 8-		opagation		Parame	ter	00
		tup		td	n		
		tO KCL		KCL	KCL2		Path
D1	Q1	4.72 0.1 4.12 0.1		0.09	0.10		CK,IH → Q CK,IH → XQ
D2	р—— XQ1	4.12 0.1	4.00	0.13	0.10	-	ok,in · zq
D3	Q2						
D4	р—— XQ2						
D5 ———	Q3 — XQ3			Ì		ļ	
D7	— Q4						
D8	р xq4						
	Q5 Q5 XQ5						
	Q6						
ск —	þ—— xQ6	Parameter				Symbol	Typ(ns)*
IH —	Q7	Clock Pulse	Width			tCW	7.2
SI	D—— XQ7 —— Q8	Clock Pause	ттше			tCWH	5.5
В —	<b>├</b>	Data Setup	Time			tSD	1.8
_		Data Hold T	ime			tHD	3.3
	Input Loading						
Pin Name	Factor (lu)						
D	1						
CK IH	1 1						
SI	i						
A	1						
В	1				- 1		
	Output Driving				1		l
Pin Name	Factor (lu)						
Q XQ	18 18	* Minimum	alues for	the to	mical	onerati	ng condition.
	10	The value	s for the	worst	case o	peratin	g condition
	<u> </u>	are giver	by the m	naximum	delay	multipl	ier.
UHB-SHA-E1	Sheet 1/3						Page 11-24





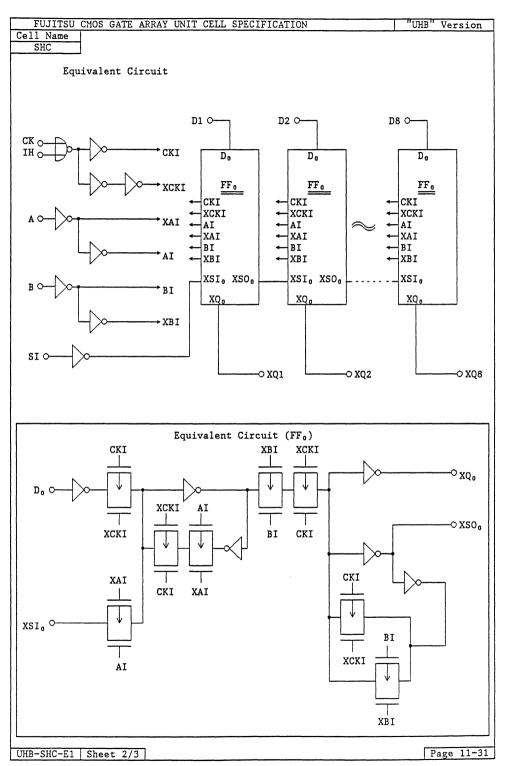
FILITSILC	MOS GATE ARRAY U	NIT CEL	T. SPECI	FICATIO	N		"ITH	B" Version
	Function	5.VII OBB	<u> </u>	1 1011110				Number of BC
		Lit Down		11- *	L:L:+ *	D 0:		
SHB Cell Symbol	SCAN 1-input 8-	-bit DFF	Prop	agation	Delay	Paramet	er	62
0011 0,0001		t	up		td			
		t0	KCL	t0	KCL	KCL2		Path
		4.32	0.16	4.42	0.09	0.10	4	CK,IH → Q
D1 -	Q1							
D2	Q2	1						
D3	Q3							
D4	Q4							
D6	Q5 Q6							Ì
D7	Q7	1						
D8	Q8							
ck —								
IH		Parame	ter	L		S	ymbol	Typ(ns)*
A —		Clock	Pulse W				tCW	7.2
<u>в</u> — ф		Clock	Pause T	ime			tCWH	5.5
Ĺ		Data S	etup Ti	me			tSD	1.9
		Data H	old Tim	е			tHD	3.3
	T T : 11							
Pin Name	Input Loading Factor (lu)					l		
D	1	1						
CK	1	1						
IH SI	1 1	1						
A	1							
В	1							
	Outros Dedesino	4						
Pin Name	Output Driving Factor (lu)							
Q	18							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		are	values given b	ror the m	worst	delav m	meratin	g condition
	J		82.0	<i>y</i>				

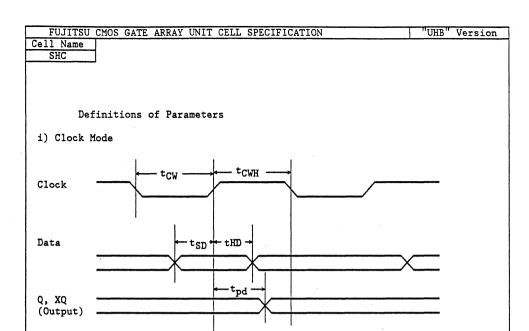


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name SHB Definitions of Parameters i) Clock Mode - t<sub>CWH</sub> t<sub>CW</sub> Clock tHD Data tSD\* -t<sub>pd</sub> -Q, XQ (Output)

UHB-SHB-E1 | Sheet 3/3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB"	Version					
Cell Name   Function   Nu	mber of BC					
SHC SCAN 1-input 8-bit DFF with Clock-Inhibit & XQ Output	62					
Cell Symbol Propagation Delay Parameter tup tdn						
t0 KCL t0 KCL KCL2 CDR2	Path					
4.18 0.16 4.10 0.13 0.18 4	CK, IH → XQ					
D1 — 0— XQ1						
D2 — XQ2						
D4 p xQ4						
D5						
D6 —						
D7 —						
D8 —— XQ8						
CK —						
IH Parameter Symbol	Typ(ns)*					
Clock Pulse Width	7.2					
B ——c Clock Pause Time tCWH	5.5					
Data Setup Time tSD	1.9					
Data Hold Time tHD	3.3					
Input Loading Pin Name Factor (lu)						
D 1						
CK 1						
IH 1   1						
SI 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1						
B 1 1						
Output Driving						
Pin Name Factor (lu) XQ 18						
* Minimum values for the typical operating	g condition.					
The values for the worst case operating	condition					
are given by the maximum delay multiplie	er.					

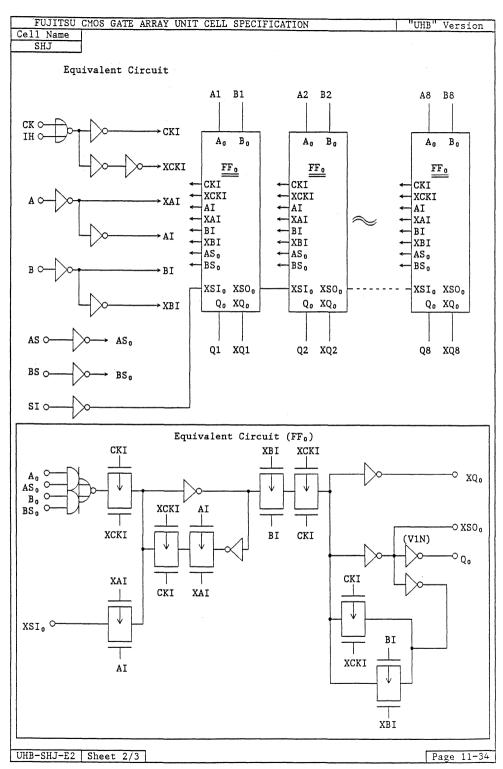


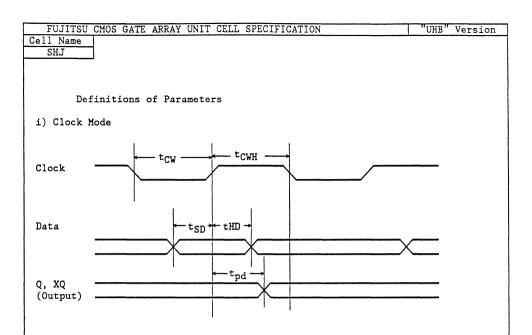


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UHB-SHC-E1 | Sheet 3/3

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"UH	3" Version
Cell Name	Function						N	Number of BC
		with Clock-Inhibit						
SHJ Cell Symbol	& 2-to-1 Data M	ultiple			Dalam	Damamad		78
Cell Symbol		Propagation Delay Parameter tup tdn					T	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.82	0.16	4.84	0.08	0.12	4	CK,IH → Q
		4.12	0.16	4.00	0.11	0.20	4	CK, IH → XQ
A1 ————————————————————————————————————	P—— Q1 P—— XQ1							
A2	Q2						ļ	
В2 —	þ— xq₂							
A3	Q3						1	
B3	о—— xqз				1		1	
A4 ————————————————————————————————————	Q4 P XQ4							
A5	Q5						1	
В5 —	þ xQ5							
A6	Q6							1
B6	2 XQ6						1	
A7	—— Q7 ○—— XQ7				i		İ	
A8	Q8							1
B8	⊳—— x̂Q8						1	
AS —						]		
BS ——								
CK —						•		1
IH —		}						1
SI		Parame	ter		<u> </u>		Symbol .	Typ(ns)*
A ————————————————————————————————————			Pulse W				tCW	7.2
<u> </u>		Clock	Pause T	ime			tCWH	5.5
		Data S	etup Ti	me			tSD	3.0
			old Tim				tHD	3.1
	I Tarab Tarabar							
Pin Name	Input Loading Factor (lu)	i						
An, Bn	1					1		
(n=1~8)								
AS,BS	1							
CK	1							
IH SI	1 1							
A,B	1							
D/- 11	Output Driving							
Pin Name Q	Factor (lu)	<del> </del>						<del></del>
χQ	18	* Mini	mum val	ues for	the ty	pical (	operati	ng condition.
1		The	values	for the	worst	case o	peratin	g condition
	1	are	given b	y the m	naximum	delay	multipl	ier.
1								
IND CUT ES	Ch 1 /0							Page 11-33
UHB-SHJ-E2	Sheet 1/3							Trage II 33

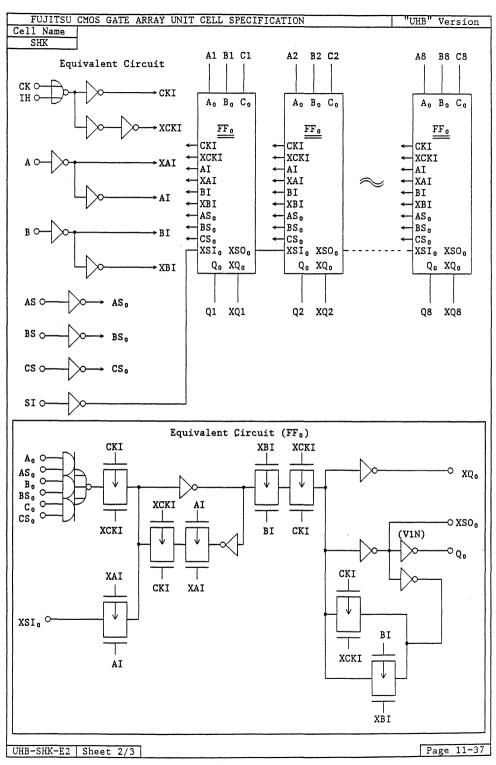


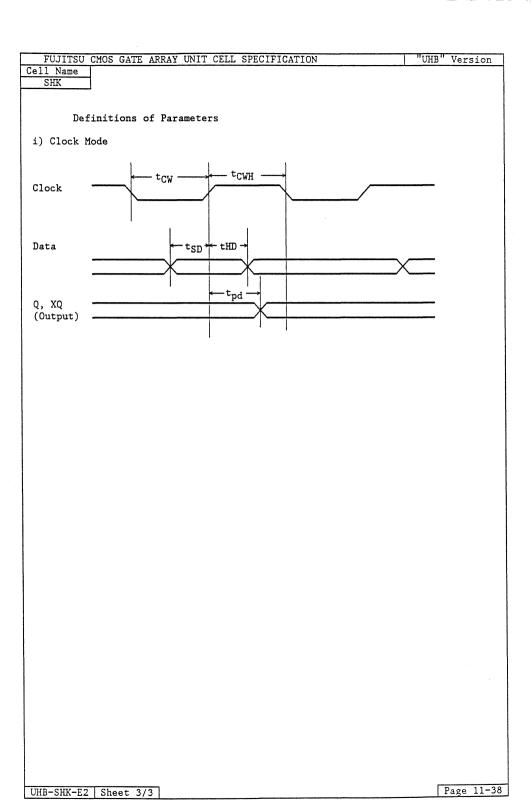


2-153

UHB-SHJ-E2 | Sheet 3/3

FUJITSU CNOS GATE ARRAY UNIT CELL SPECIFICATION	FULLTSU	MOS GATE ARRAY III	NIT CEL	T. SPECT	FICATIO	N	<del></del>	l III	HB" Version
SIAK   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six   Six	Cell Name		NII OLL	n biller	TIGATIO	14			
Propagation   Pelay Parameter   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Path   Pat		SCAN 8-bit DFF with Clock-Inhibit							
Tup		& 3-to-1 Data M	to-1 Data Multiplexer 88					88	
Cl	Cell Symbol								
## A1					+0			Lanna	- n
Bi	Δ1 Γ								
C1		├ O1							
A2		1 1	7.00	0.10	7.00	0.13	0.10	-	on, in and
C2		γ— xq1						1	
A3		Q2						1	
R3		b x02						1	
C3								1	
A4		1							
B4		р—— xqз							
C4		Q4							
Data Setup Time   Symbol   Typ(ns)*		1						1	
C5		1							
A6		Q5							
B6		₽ xQ5							
C6		├── 06					1		
R7		1							
C7		1							
A8		Q7							
R8		р <b>х</b> Q7							
Name		08							
AS — C		1						1	
Parameter   Symbol   Typ(ns)*		XQ8						1	
Parameter   Symbol   Typ(ns)*	1 -!								
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 7.2  Clock Pause Time tCWH 5.5  Data Setup Time tSD 3.8  Data Hold Time tHD 2.9  Pin Name Factor (\$\textit{ku}\$)  An,Bn,Cn (n=1~8)  AS,BS,CS 1  CK 1  IH 1  SI 1  SI 1  A,B 1  Output Driving Factor (\$\textit{ku}\$)  Q 18  XQ 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Parameter   Symbol   Typ(ns)*									
Clock Pulse Width   tCW   7.2	1		Parame	ter	L	L	<del>'                                    </del>	Symbol	Typ(ns)*
B — C Data Setup Time tSD 3.8  Data Hold Time tHD 2.9  Pin Name Factor (Ru)  An,Bn,Cn (n=1~8) AS,BS,CS 1 CK 1 IH 1 SI 1 A,B 1  Pin Name Factor (Ru)  Q 18  XQ 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1		Clock	Pulse W	idth				
Data Setup Time tSD 3.8 Data Hold Time tHD 2.9  Pin Name Factor (fu)  An,Bn,Cn (n=1~8) AS,BS,CS 1 CK 1 IH 1 1 SI 1 1 A,B 1  Q 18 XQ 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Clock Pause Time					tCWH	5.5
Pin Name Factor (fu)  An,Bn,Cn (n=1~8) AS,BS,CS 1 CK 1 IH 1 1 SI 1 1 A,B 1  Q 18 XQ 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	В — 9								
Pin Name   Input Loading   Factor (£u)   An,Bn,Cn	_								
Pin Name Factor (Lu)  An,Bn,Cn			Data Hold Time					CUD	4.9
Pin Name Factor (Lu)  An,Bn,Cn		Input Loading	1						
(n=1~8) AS,BS,CS 1 CK 1 IH 1 SI 1 A,B 1  Output Driving Factor (lu)  Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	Pin Name								
AS,BS,CS  CK  IH  IH  SI  A,B  Output Driving  Pin Name  Q  18  XQ  18  XQ  18  * Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.		1					İ		1
CK 1 IH 1 SI 1 A,B 1  Output Driving Factor (Lu)  Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1 '	1	1						[
IH 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1							
SI 1 1 1		1							
Pin Name Output Driving Factor (lu)  Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1	1							
Pin Name Factor (lu)  Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	A,B	1							1
Pin Name Factor (lu)  Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	ļ	1	1						
Q 18 XQ 18 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	Pin Nama								
XQ 18 * Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.									
The values for the worst case operating condition are given by the maximum delay multiplier.		I	* Mini	mum val	ues for	the ty	pical	operat	ing condition.
are given by the maximum delay multiplier.			The	values	for the	worst	case o	perati	ng condition
UHB-SHK-E2   Sheet 1/3   Page 11-36			are	given b	y the m	naximum	delay	multip	olier.
UHB-SHK-E2   Sheet 1/3   Page 11-36									
UHB-SHK-E2   Sheet 1/3   Page 11-36									
UHB-SHK-E2   Sheet 1/3   Page 11-36									
	UHB-SHK-E2	Sheet 1/3							Page 11-36





# Non Scan Flip-Flop Family

Page	Unit Cell Name	Function	Basic Cells
2-159	FDM	Non-Scan D FF	6
2-161	FDN	Non-Scan D FF with Set	7
2-163	FDO	Non-Scan D FF with Reset	7
2-165	FDP	Non-Scan D FF with Set and Reset	8
2-168	FDQ	Non-Scan D FF	21
2-170	FDR	Non-Scan D FF with Clear	26
2-173	FDS	Non-Scan D FF	20
2-175	FD2	Non-Scan Power D FF	7
2-177	FD3	Non-Scan Power D FF with Preset	8
2-179	FD4	Non-Scan Power D FF with Clear and Preset	9
2-181	FD5	Non-Scan Power D FF with Clear	8
2–183	FJD	Non-Scan Positive Edge Clocked Power J-K FF with Clear	12

Cell Name	CMOS GATE ARRAY U	NII CEL	L SPECI	FICALIU.	N		1 0	HB" Version Number of B
ell Name	Function							Number of B
FDM	Non-SCAN DFF							6
Cell Symbol			Prop	agation	Delay 1	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.75	0.16	1.80	0.09			CK → Q
		2.16	0.16	2.36	0.09			CK → XQ
D ——	— Q —— хQ							
			Pulse W				ymbol tCW tCWH	Typ(ns)* 4.0 4.0
		Clock	Pause T	ıme			ECWH	4.0
		Doto S	etup Ti	mo			tSD	2.1
			old Tim				tHD	1.5
Pin Name D CK	Input Loading Factor (£u)  2 1							
Pin Name Q	Output Driving Factor (lu)							
хQ	18	The	mum val values given b	for the	worst	case or	erati	ing condition g condition lier.

Inputs	Outputs
D CK	Q XQ
H ↑ L ↑	H L L H

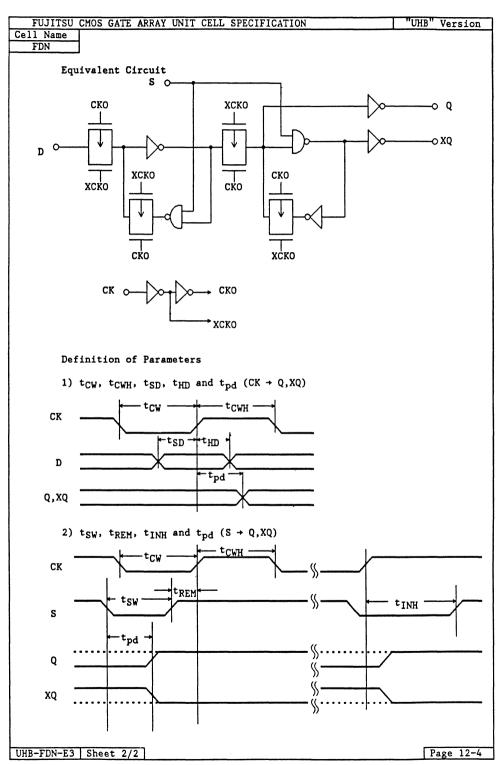
UHB-FDM-E2 | Sheet 1/2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION
Cell Name 'UHB" Version FDM Equivalent Circuit CLK XCLK o XQ XCLK CLK XCLK CLK XCLK \*XCLK Definition of Parameters t<sub>CWH</sub> CK tSD D - t<sub>pd</sub>-Q,XQ Page 12-2 UHB-FDM-E2 | Sheet 2/2

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version
Cell Name	Function						Number of BC	
FDN	Non-SCAN DFF with SET						7	
Cell Symbol				agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.80	0.16	1.75	0.09	0.12	4	CK + Q
		2.46	0.16	2.42	0.08			CK → XQ
	S	2.24	0.16	1.07	0.08			$s \rightarrow q, xq$
	Ţ						l	
Г							l	
D —	Q						İ	
ск —							l	
- CK							1	
İ	р—— <b>х</b> Q						l	
L						ļ	l	
							Ì	
		Parame				S	ymbol	Typ(ns)*
		Clock	Pulse W	idth			tCW	4.0
		Clock	Pause T	ime			tCWH	4.0
		Data S	etup Ti	me			tSD	2.1
		Data H	old Tim	e			tHD	1.5
	Input Loading	Set Pu	lse Wid	th			tSW	4.0
Pin Name	Factor (lu)	Set Re	lease T	ime (S)			tREM	0.3
D	2	Set Ho	ld Time				tINH	3.8
S	2							
CK	1	l				l		
		1						
	Output Driving	1						
Pin Name	Factor (lu)							
Q	18	1						
χQ	18							
• • •		* Mini	mum val	ues for	the tv	pical c	perat	ing condition
								ng condition
				y the m				
	<del>•</del>		<u> </u>					

Ir	put	s	Out	tputs
S	D	CK	Q	XQ
L H H	X H L	X †	H H L	L L H

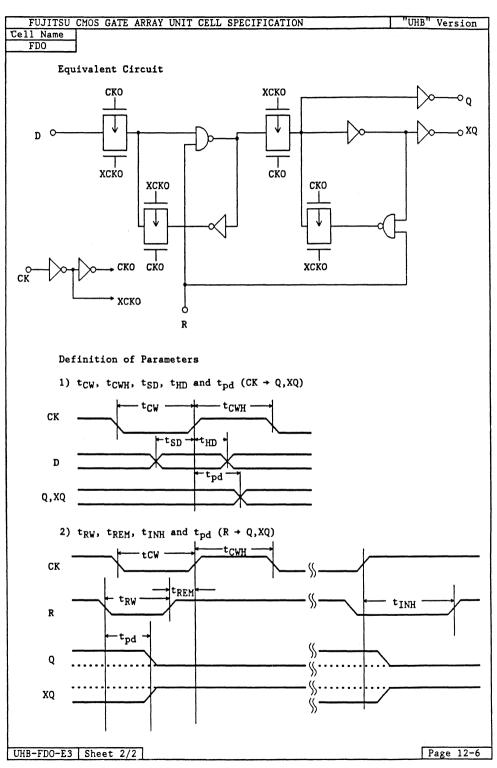
UHB-FDN-E3 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version
Cell Name	Function						Number of BC	
FDO	Non-SCAN DFF wi	th RESE						7
Cell Symbol				agation	Delay		er	
			up		td		T	
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.93	0.16	1.78	0.10		ļ	CK → Q
		2.16	0.16	2.58	0.09			CK → XQ
		2.00	0.16	1.64	0.10			$R \rightarrow Q, XQ$
							ļ	
D ——CK	Q		ter Pulse W Pause T				Symbol tCW tCWH	Typ(ns)* 4.0 4.0
		Data S	etup Ti	me			tSD	2.1
			old Tim				tHD	1.5
	Input Loading	Reset	Pulse W	idth			tRW	4.0
Pin Name	Factor (lu)		Release		R)		tREM	0.9
D	2						tINH	3.3
R CK	2 1	Reset Hold Time tINF						
	Output Driving	1				l		
Pin Name	Factor (lu)					l		
Q	18	1						
хQ	18	<b></b>						
		The	values	for the		case o	perati	ing condition ng condition lier.

Iı	nput	s	Ou-	tputs
R	D	CK	Q	XQ
L H H	X H L	X †	L H L	H L H

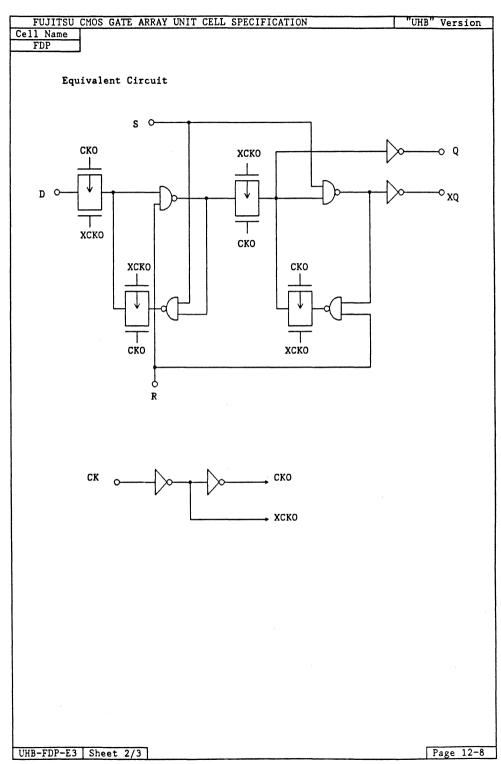
UHB-FDO-E3 Sheet 1/2

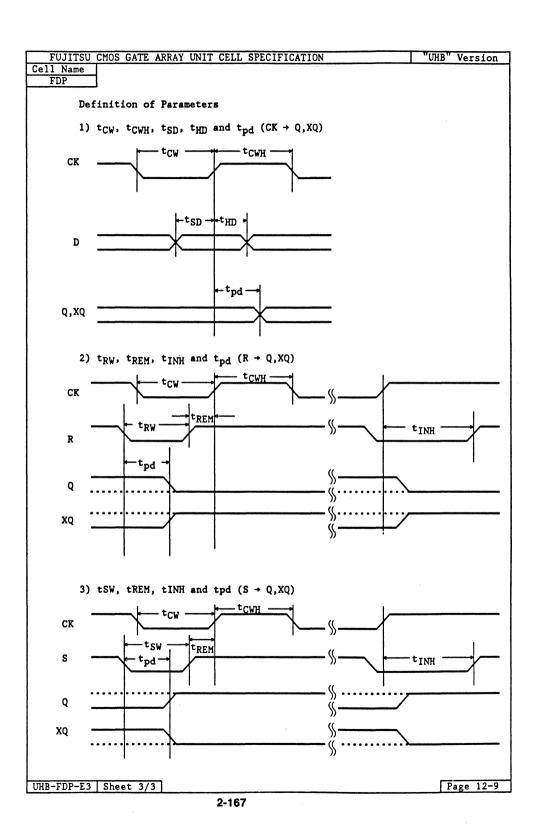


FULLTSU	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		1"11	HB" Version
Cell Name	Function	MIT ODD	D DI DOI	11011110	**			Number of BC
FDP	Non-SCAN DFF wi	th Set	and Res	et				8
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.96	0.16	1.76	0.10		l	CK → Q
	_	2.45			0.09			CK → XQ
	S	2.24		1.59	0.10			$R \rightarrow Q, XQ$
İ		2.54	0.16	1.01	0.09		l	$s \rightarrow Q, xQ$
_							Ì	
D —	o							
	٧						İ	1
CK —								
1	þ xQ							
l L								
1	Ĭ							
l	į.						1	
	R	Parame	ter		<del></del>	S	ymbo1	Typ(ns)*
		Clock	Pulse W	idth			tCW	4.0
		Clock	Pause T	ime			tCWH	4.0
1			etup Ti				tSD	2.1
		Data H	old Tim	e			tHD	1.5
l	Input Loading		lse Wid				tSW	4.0
Pin Name	Factor (lu)			ime (S)			tREM	0.3
D	2	Set Ho	ld Time				tINH	3.8
S R	2 2	Panat	Pulse W	1 d+ h			tRW	4.0
CK	1			Time (	D)		tREM	0.9
	1		Hold Ti		м)		tINH	3.3
<u> </u>	Output Driving	Weser	noru II	me.			CIMI	<del>-                                     </del>
Pin Name	Factor (lu)							
Q	18	1						
χQ	18	<b>———</b>						
"		* Mini	mum val	ues for	the tv	pical c	perat	ing condition.
								ng condition
1					aximum			

	Inpi	ıts		Outputs
S	R	D	CK	q xq
H L L H	L H L H	X X X H L	X X X †	L H H L Inhibited H L L H

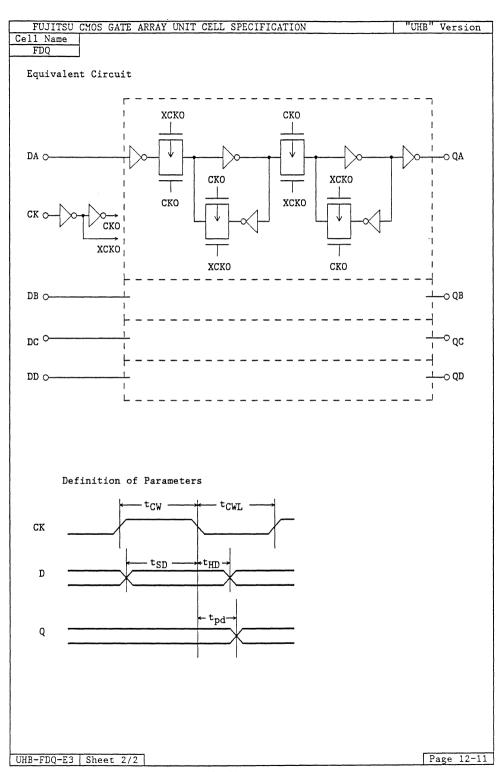
UHB-FDP-E3 Sheet 1/3





	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version
Cell Name	Function	tion						Number of BC
FDQ	Non-SCAN 4-bit	DFF		21				
Cell Symbol				agation	Delay :		er	
			up		td			_
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.37	0.16	2.74	0.08			CK → Q
							1	
DA								
, Di	β DD						1	
							1	
							1	
	—— QA						1	
	QB QB						ł	
ск ——	- QC	ļ					ł	
	QD							
	цу							
							1	
		Parame	ter				ymbol	Typ(ns)*
		Clock	Pulse W	idth			tCW	4.0
		Clock	Pause T	ime			tCWL	4.0
		Data S	etup Ti	me			tSD	1.1
		Data H	old Tim	е			tHD	2.8
	Input Loading	1				ł		
Pin Name	Factor (lu)	1				l		1
D	1	]						1
CK	1					- 1		
						-		
						- 1		
						- 1		]
	Output Driving	1						
Pin Name	Factor (lu)					l		
Q	18	1				1		1
•								
		* Mini	mum val	ues for	the tv	pical o	perati	ing condition
								ng condition
					aximum			
		1 476	0-1011	,				

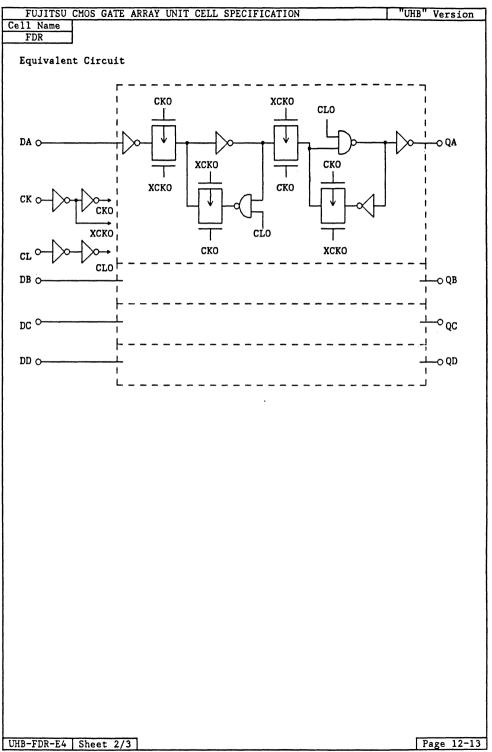
Inpi	ut	Output
CK	D	Q
<b>+</b>	H L	H L



FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N	<u> </u>	<b>"</b> U	HB" Version
Cell Name	Function							Number of BC
FDR	FDR Non-SCAN 4-bit DFF with CLEAR						26	
Cell Symbol				agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
j		2.64	0.16	3.62	0.08			CK → Q
		-	-	2.18	0.08			CL → Q
CK —								
1 .	cL	Parame					ymbol	
1	<b>7</b> 0		Pulse W				tCW	4.0
		Clock	Pause T	'ime			tCWH	4.0
		ļ						
			etup Ti				tSD	1.1
		Data H	old Tim	e			tHD	2.8
ļ	Input Loading	Class	Pulse W	11 d+h			tLW	4.0
Pin Name	Factor (lu)		Release				tREM	1.5
D D	ractor (£u)		Hold Ti				tINH	4.5
ck	i	Uleal .	11010 11	.ше		-+	CIMI	<del></del>
CL	l i	[						
Ch.	•							
	Output Driving	1						
Pin Name	Factor (lu)	1						}
Q	18	1				1		
		* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.						

I	nputs	Output	
CK	D	CL	Q
X †	X L H	L H H	L L H

UHB-FDR-E4 | Sheet 1/3



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version
Cell Name
FDR

Definition of Parameters

QA~QD

1) t<sub>CW</sub>, t<sub>CWH</sub>, t<sub>SD</sub>, t<sub>HD</sub>, and t<sub>pd</sub> (CK+QA~QD)

CK

t<sub>CW</sub>

t<sub>CW</sub>

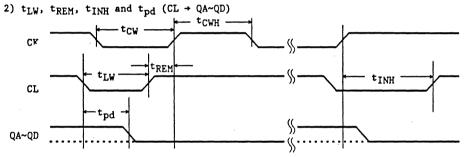
t<sub>CW</sub>

t<sub>CW</sub>

t<sub>CW</sub>

t<sub>CW</sub>

t<sub>CWH</sub>

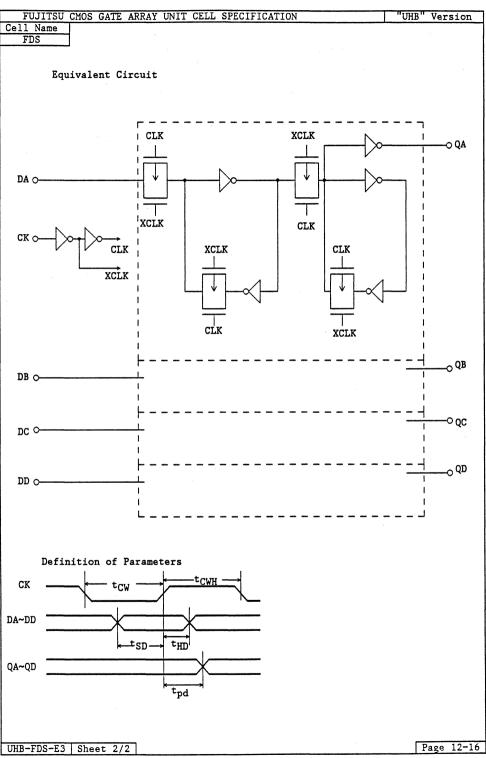


UHB-FDR-E4 | Sheet 3/3

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט"ו	HB" Version
	Function							Number of BC
FDS	Non-SCAN 4-bit	DFF						20
Cell Symbol				agation	Delay		er	
			up		td		anna	
		t0 3.03	KCL 0.16	t0 2.45	KCL 0.09	KCL2	CDR2	Path CK → Q
		3.03	0.16	2.45	0.09			CX + Q
DA D	B DC DD							
1 -								
	QA QB							
ck —	☐ ģc				:			İ
	QD			· ·				
		Parame					ymbol	Typ(ns)*
			Pulse W				tCW	4.0
		Clock	Pause T	ime			tCWH	4.0
		Data C	etup Ti				tSD	1.1
			old Tim				tHD	2.5
		Data II	Old III				CILD .	+
	Input Loading	1						
Pin Name	Factor (lu)							
D	2	1						
CK	1	1						
<b> </b>	Output Driving	1						
Pin Name	Factor (lu)	1						
Q	18	1						
1								
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati:	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.

Inp	uts	Outputs		
CK	מ	Q		
<b>†</b>	L H	L H		

UHB-FDS-E3 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"U	HB" Version
Cell Name	Function							Number of BC
FD2	Non-SCAN Power	DFF						7
Cell Symbol			Prop	agation			er	
		t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.65	0.08	1.72	0.05	0.10	7	CK → Q
		2.55	0.08	2.34	0.04	0.07	7	CK → XQ
D ——	Q							The (a) W
		Parame				-   8	Symbol	
		Clock Pulse Width tCW						4.0
		Clock Pause Time tCW						4.0
			etup Ti				tSD	1.1
		Data H	old Tim	е			tHD	2.4
Pin Name D CK	Input Loading Factor (lu) 2 1							
Pin Name	Output Driving Factor (lu)							
Q XQ	36	The	values		worst	- case o <u>r</u>	perati	ing condition ng condition lier.

Inp	uts	Outputs			
CK	D	Q	XQ		
<b>→</b> →	H L	H L	L H		

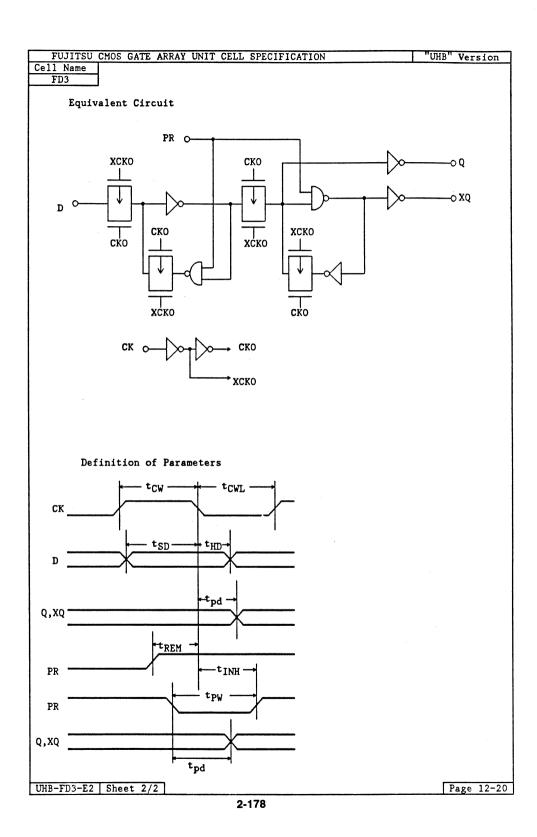
UHB-FD2-E3 | Sheet 1/2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name FD2 Equivalent Circuit CKO XCKO XCKO CKO XCKO CKO cko XCKO > CKO Definition of Parameters tCWL CK tSD D t<sub>pd</sub>-Q,XQ Page 12-18 UHB-FD2-E3 | Sheet 2/2

FILITSILO	MOS GATE ARRAY U	NIT CEL	I CDECT	FICATIO	NJ .		1 1711	THB" Version
	Function	NII OLD	D BILCI	FICHIO				Number of BC
						·····		
FD3	Non-SCAN Power	DFF wit						8
Cell Symbol				agation			er	
			up		td			
ĺ		t0	KCL	t0	KCL	KCL2	CDR2	
_		1.71	0.06	1.73	0.04	0.10	7	CK → Q
F	PR	2.80	0.06	2.50	0.04	0.07		CK → XQ
		2.39	0.06	0.91	0.04	0.07	7	PR → Q,XQ
	<u></u>						İ	
D	P Q							
ск-—ф								
	<b>├</b> ── x0						1	
	^						ł	
							1	
							l	
		Parame	ter	L			ymbo1	. Typ(ns)*
		Clock Pulse Width					tCW	4.0
		Clock Pause Time					tCWL	4.0
			etup Ti			tSD	2.1	
		Data H	old Tim	е		tHD	1.5	
	•							
	Input Loading		Pulse				tPW	4.0
Pin Name	Factor (lu)		Releas				tREM	0.3
D	2	Preset	Hold T	ime			tINH	3.8
CK	1	ŀ				- 1		
PR	2					1		
						l		
	Output Driving	ł				ı		
Pin Name	Factor (lu)					ı		
Q	36	1				1		
χο	36							
"``		* Mini	mum val	ues for	the tv	pical o	perat	ing condition.
	1							ng condition
				y the m				
	<del></del>							

	Inputs	Outputs		
PR	CK	D	Q	XQ
L H H	X +	X H L	H H L	L L H

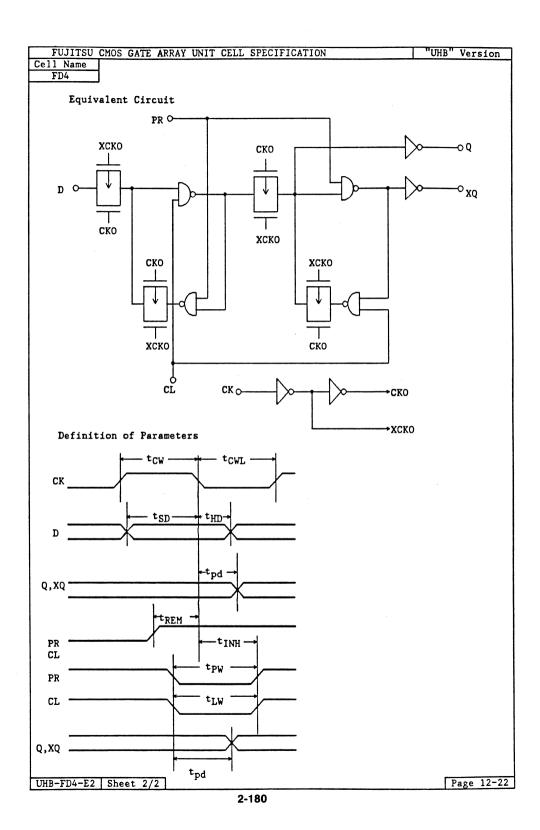
UHB-FD3-E2 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" [	HB" Version
Cell Name	Function							Number of BC
FD4	Non-SCAN Power	DFF wit	h Clear	and Pr	eset			9
Cell Symbol				agation			er	
			up	10	td KCL		CDR2	┥ 。
		t0	KCL 0.07	t0 1.72	0.05	0.10		
	PR	1.90 2.81			0.03	0.10		CK → Q CK → XQ
r	T.	2.61				0.10		CL + Q,XQ
		2.49	0.00	0.92	0.03	0.10	1 7	$PR \rightarrow Q, XQ$
	۵	2.49	0.07	0.32	0.04	0.07	′	11. 4 Q, AQ
р —	├ Q						l	
							ł	
ск							1	
	⊳—— xQ						]	
<u> </u>	<del></del>						1	
							1	
C	:L						į .	
							<u> </u>	
		Parameter Symbo						
		Clock Pulse Width					tCW	4.0
		Clock Pause Time					tCWL	4.0
		Dete S	etun Ti	me			tSD	2.1
		Data Setup Time Data Hold Time					tHD	1.5
		2000 11	010 111				<u> </u>	1
	Input Loading	Preset	Pulse	Width			tPW	4.0
Pin Name	Factor (lu)		Releas				tREM	0.3
D	2	Preset	Hold T	ime			tINH	3.8
CK	1							
CL	2		Palse W				tLW	4.0
PR	2		Release				tREM	0.9
		Clear Hold Time				tINH	3.3	
	Output Driving							
Pin Name	Factor (lu)					ł		
Q	36							
XQ	36	1						
								ing condition
								ng condition
		are	given b	y the m	aximum	deray t	ultip	lier.

	Inp	Out	puts		
PR	CL	CK	D	Q	XQ
L H H	H H H	X X +	X X H L	H H L	L H L H

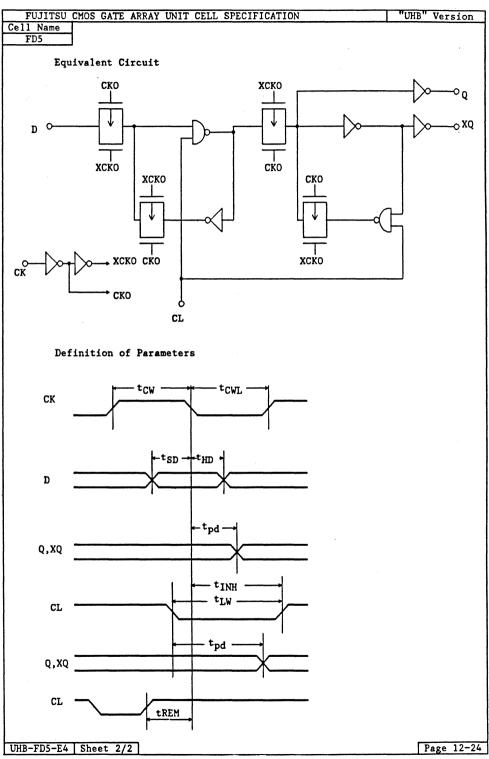
UHB-FD4-E2 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version
	Function							Number of BC
FD5	Non-SCAN Power	DFF wit						8
Cell Symbol				agation			ter	
			up	·	td		1	
		t0	KCL	t0	KCL	KCL2		
		1.88	0.08	1.71	0.05	0.10		CK → Q
		2.57	0.08	2.57	0.04	0.07		CK → XQ
		2.36	0.08	1.52	0.05	0.10	' '	CL → Q,XQ
р ——	Q XQ	Parame					Symbol	
		Clock Pulse Width					tCW	4.0
		Clock Pause Time					tCWL	4.0
ĺ								
			etup Ti				tSD	1.1
		Data H	old Tim	e			tHD	2.4
ļ	Tonut Tondino	Class	Pulse W	2.34%			tLW	4.0
Pin Name	Input Loading Factor (lu)		Release			-+	tREM	1.5
D D	Pactor (ku)		Hold Ti			-+	tINH	4.5
СК	1	Oleal	noru II	ше		-+	CIM	+
CL	2					1		
C.D								
<b>.</b>	Output Driving					i		
Pin Name	Factor (lu)	l				- 1		
Q VO	36 36	<b></b>						1
XQ	36	* Minimum values for the typical operating conditions The values for the worst case operating conditions are given by the maximum delay multiplier.					ng condition	

	Input	Outputs		
CL	CK	D	Q	XQ
L H H	X ↓	X H L	L H L	H L H

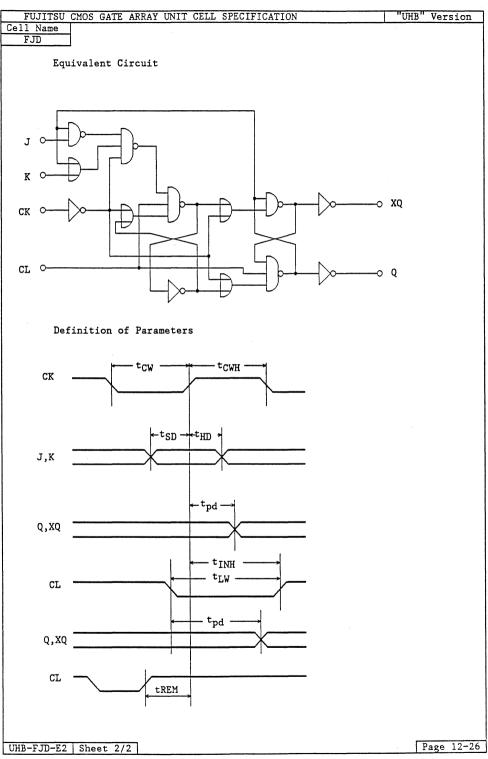
UHB-FD5-E4 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N .		l "U	HB" Version
Cell Name	Function		2 01 201		···			Number of BC
				************				
FJD	Non-SCAN Positi	ve edge	clocke	d Power	JKFF w	ith Cle	ar	12
Cell Symbol				agation				
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.40	0.08	2.96	0.05	0.08	7	CK → Q
		4.43	0.08	2.48	0.05	0.08	7	CK → XQ
		2.40	0.08	1.29	0.05	0.08	7	CL → Q,XQ
							İ	1 "
								1
							1	
J —	├ q		1					
		<b>\</b>	]				1	
ск —							1	
к —	b xo		1				ł	
. L								
	Y						1	
	1	·					1	
	CL	Parame	ter				Symbol	Typ(ns)*
		Clock Pulse Width					tCW	5.6
		Clock Pause Time					tCWH	5.6
		J.K Se	tup Tim	e			tSD	2.5
			ld Time				tHD	1.2
		<del> </del>						
	Input Loading	Clear	Pulse W	idth			tLW	4.0
Pin Name	Factor (lu)		Release				tREM	2.5
CL	2	Clear	Hold Ti	me			tINH	4.5
J	1							
K	1	İ				- 1		
CK	1	İ				l		
	1	I				1		
	Output Driving	1				Î		
Pin Name	Factor (lu)					i		
Q	36	1						
χQ	36							
•	1	* Mini	mum val	ues for	the tv	pical o	perat	ing condition.
								ng condition
				y the m				
			D	, 111			Р	

	Inpi	ıts	Outputs	
CL	CK	J	K	Q XQ
L	X	x	x	L H
H	<b>†</b>	L	L	Q <sub>o</sub> XQ <sub>o</sub> L H
H	•	L	H	L H
Н	<b>†</b>	H	L	H L
H	<b>†</b>	Н	H	XQ. Q.

UHB-FJD-E3 | Sheet 1/2

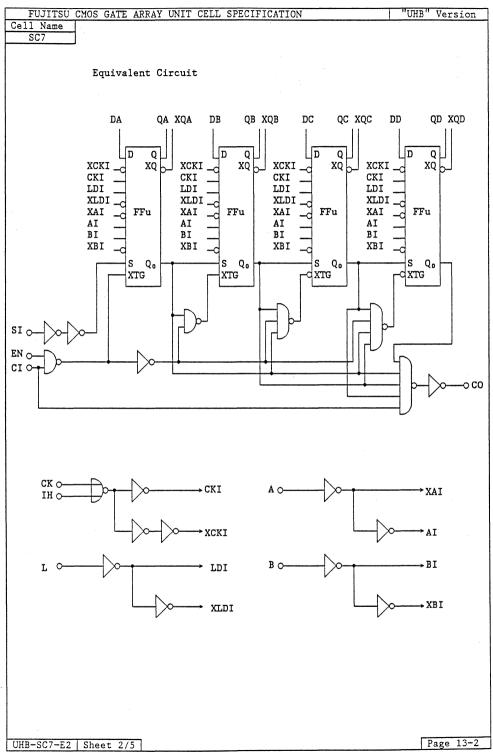


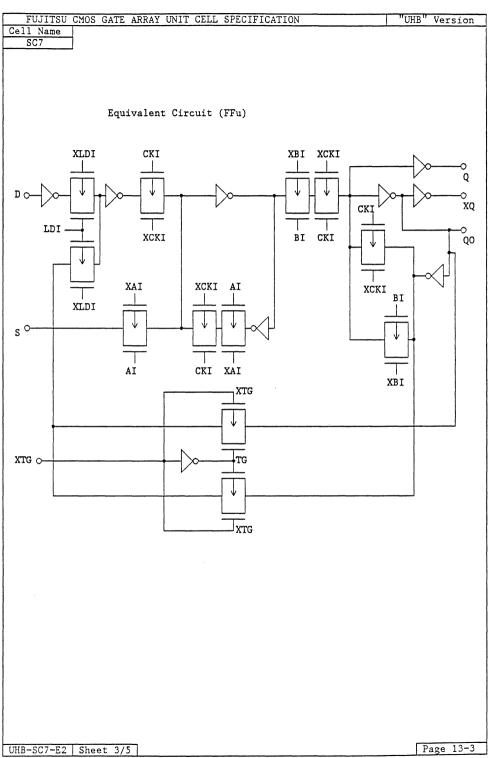
# **Binary Counter Family**

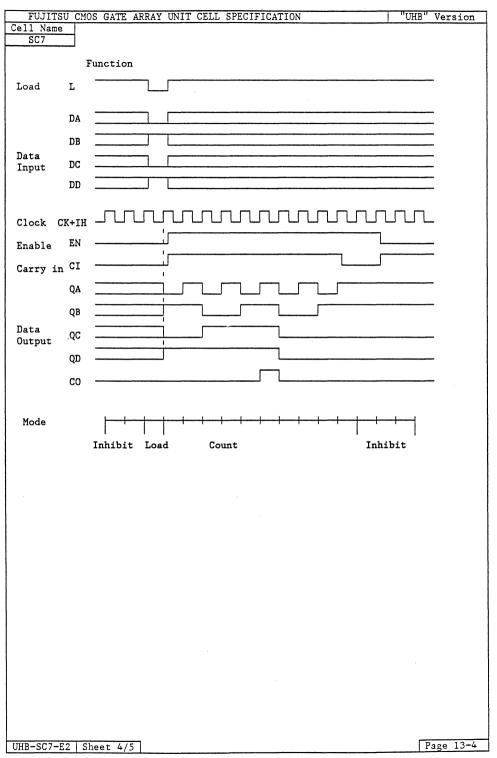
Page	Unit Cell Name	Function	Basic Cells
2-187	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
2–192	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
2-197	C11	Non-Scan Flip-Flop for Counter	11
2-199	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
2-202	C42	Non-Scan 4-bit Binary Synchronous Counter	32
2-205	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
2-209	C45	Non-Scan Binary Synchronous Up Counter	48
2-213	C47	Non-Scan Binary Synchronous Up/Down Counter	68

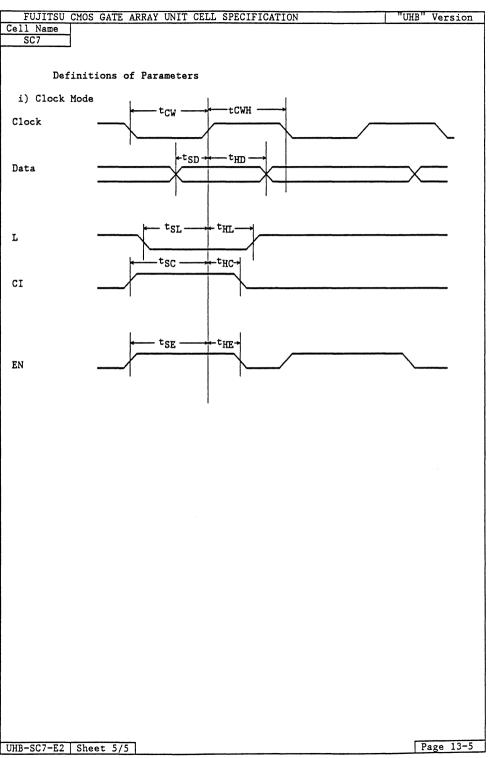
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FILITCII (	CMOS CATE ADDAY II	NIT CEL	CDECT	ETCATTO	NT.			I TUD II	Version
								mber of BC	
SCAN 4-bit Synchronous Binary						1			
SC7	Up Counter with		el Load						62
Cell Symbol				agation	Delay		neter		
		tup tdn						D 11	
		t0 3.30	KCL 0.08	t0 3.05	KCL 0.06	0.1			Path CK,IH → Q
		5.78	0.08	5.34	0.06	0.3	l l		$CK,IH \rightarrow Q$
		7.80	0.08	5.23	0.04	_	-	. [	CK,IH → CO
DA		2.00	0.08	1.00	0.04	_	-	.   `	CI → CO
DB —	QA VOA							- 1	
DC -	D—— XQA —— QB							į	
	р—— хов						- 1	l	
ck —	— QC						- 1	į	
IH —	p xQC							l	
г —	QD QD	Parame	ter		نــــنـــــــا	ш-,	Symbo	,	Typ(ns)*
CI	р ХОД		Pulse W	idth			tCW	_	7.2
EN	co		Pause T				tCWH		7.2
A									
в —			etup Ti				tSD		2.0
L		Data H	old Tim	<u>e</u>			tHD		3.3
		Load C	etun Ti	mo.	<del></del>		tSL		6.3
	Load Setup Time Load Hold Time				tHL		3.6		
				<u> </u>					
	Input Loading		up Time				tSC		7.2
Pin Name	Factor (lu)	CI Hol	d Time				tHC		2.7
D CK	1 1	EN Cat	TP/				tSE		7 2
IH	1	EN Hol	up Time				tHE	-	7.2
L	1	LIV IIOI	u iime						
CI	2					- 1			
EN	1								
SI	1					- 1			
A,B	1								
	Output Driving							1	
Pin Name	Factor (lu)							1	
Q	36					1		- 1	
XQ	36								
CO	36	* Minimum values for the typical operating condition.							
		The values for the worst case operating condition are given by the maximum delay multiplier.							
	J	are	given b	y the m	aximum	dela	y multi	pile	r.
UHB-SC7-E2	Sheet 1/5								Page 13-1

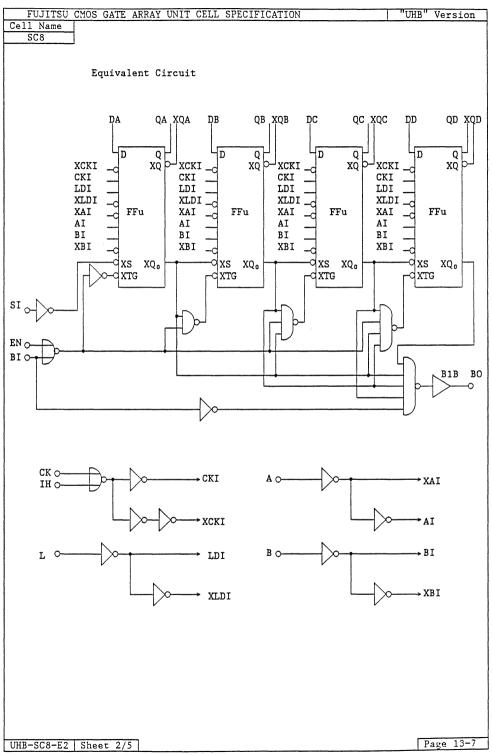


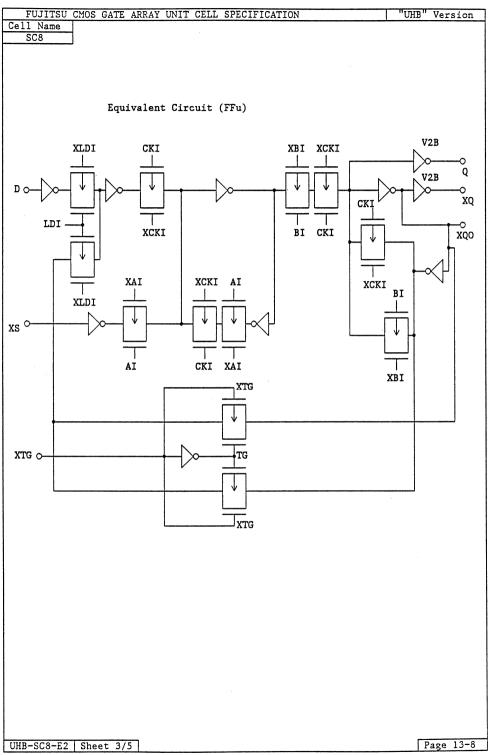


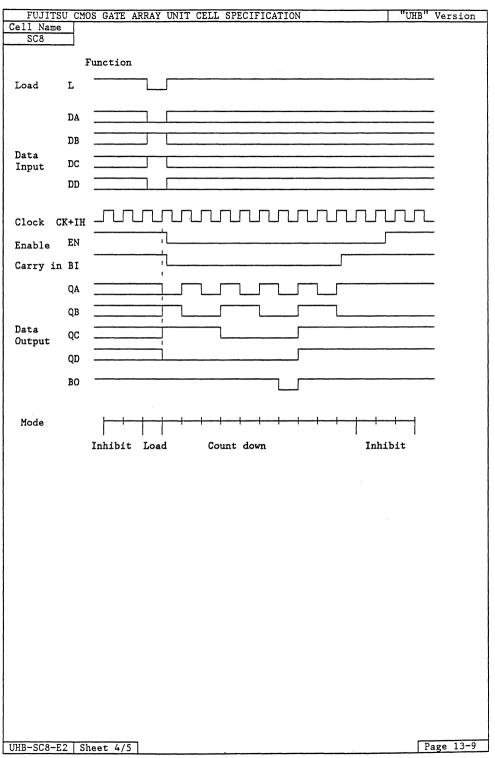


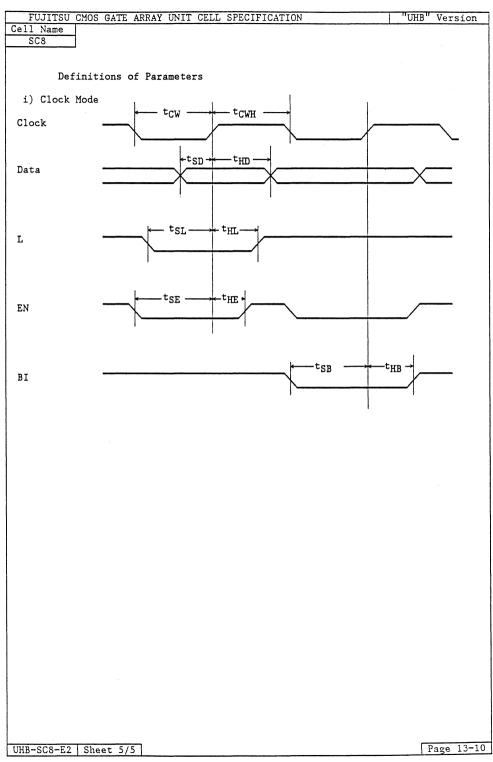


FULLTER	OMOG CAME ADDAY II	NITT CET	T CDECT	TICATIO	V.		1111	17D    17	
Cell Name							] "0.	HB" Version Number of BC	
OCII Name	SCAN 4-bit Sync	hronous	Binary					Number of BC	
SC8	th Para	llel Lo	ad			- (	66		
Cell Symbol	1 1 1 1 1 1	Prop	agation	Delav	Paramet	er			
, , , , , , , , , , , , , , , , , , , ,	Propagation Delay Parameter tup tdn								
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		3.37	0.07	3.18	0.06	0.13	7	CK, IH → Q	
		4.40	0.06	4.32	0.04			CK, IH → XQ	
F		6.41	0.08	8.37	0.04			CK, IH → BO	
DA	QA	1.49	0.08	2.27	0.04			BI → BO	
DB —	b XQA								
DC -	QB QB								
DD -	р—— хов			* 1					
ск —	QC								
IH —	þ xoc								
r —o	QD						٠,,		
ві — с	р—— <u>хо</u> д	Parame		7.1.1			ymbol		
EN —			Pulse W				tCW	6.8	
si —	р <del></del> во	CTOCK	Pause T	ıme			tCWH	6.8	
Α		Data S	etup Ti			-+	tSD	2.0	
в — ф		Data B	old Tim	ше			tHD	3.3	
		рака п	OIG III	-			עונט	<del>  ,,,</del>	
		Load S	etun Ti	mo			tSL	6.3	
		Load Setup Time Load Hold Time					tHL	3.6	
		Doau II	OIG III					1 3.0	
	Input Loading	EN Set	up Time				tSE	8.1	
Pin Name	Factor (lu)	EN Hol					tHE	1.8	
D	1								
CK	1	BI Setup Time					tSB	8.1	
IH	1	BI Hold Time					tHB	1.8	
L	1								
BI	2								
EN	1								
SI	1								
A,B	1								
		}							
	Output Driving								
Pin Name	Factor (lu)								
Q	36								
XQ	36	4. 10			. 41 4				
ВО	36	* Minimum values for the typical operating condition.							
		The values for the worst case operating condition are given by the maximum delay multiplier.							
		are	given b	y the m	aximum	deray n	urcip	1161.	
1									
1									
UHB-SC8-E2	Sheet 1/5							Page 13-6	
UND-300-E2	Differ 1/3							11050 10 0	





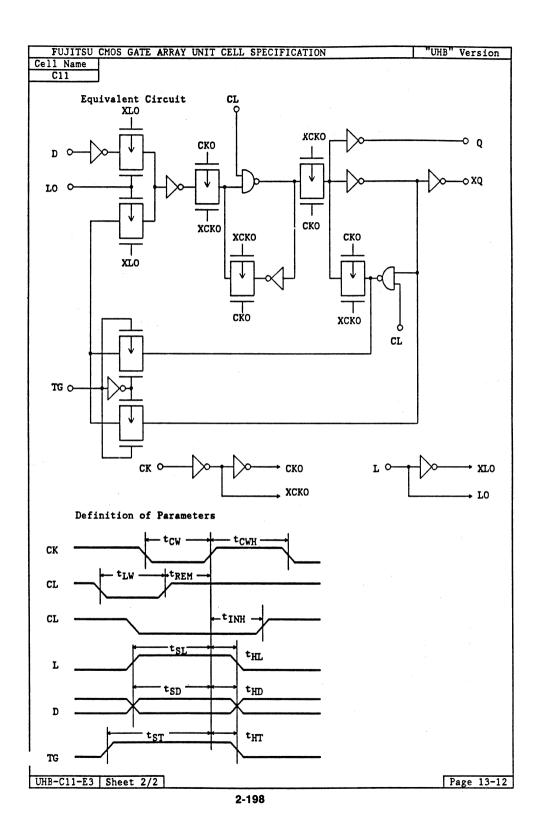




FILTER	TSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
Cell Name	Function	NII CEL	L SPECI	FICATIO	'N		1 0	Number of BC	
Cell Name	runction							Number of BC	
C11	Non-SCAN Flip-F	lop for	Counte	r				11	
Cell Symbol	······································	Propagation Delay Parameter							
		t	tup tdn						
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		1.90	0.16	1.75	0.10			CK → Q	
İ		2.53	0.16	2.97	0.10			CK → XQ	
		2.62	0.16	1.73	0.10			CL → Q,XQ	
D									
L	Q								
ск —									
TG -	<b>р—— х</b> о								
L		Parame	ter	l	1	l s	ymbol	Typ(ns)*	
ĺ	Ĭ	Clock Pulse Width					tCW	4.0	
	07	Clock Pause Time					tCWH	4.2	
j	CL								
		Clear Pulse Width					tLW	4.0	
]			Release				tREM	1.0	
		Clear	Hold Ti	me			tINH	0.5	
	Input Loading								
Pin Name	Factor (lu)		etup Ti		CK)		tSL	2.3	
L	2	Load H	old Tim	ie (	CK)		tHL	0.5	
TG CL	2 2	Data C	atus Ti		CK)		tSD	2.5	
D,CK	1		etup Ti		CK)		t HD	0.5	
D, CK	1	раса п	010 110	(	UK)		LUD	- 0.5	
	Output Driving	TG Set	up Time		CK)	-+-	tST	2.9	
Pin Name	Factor (lu)		d Time		CK)		tHT	0.0	
Q	18				/			<b>—</b>	
ΧQ	18								
		* Mini	mum val	ues for	the tv	pical o	perat	ing condition.	
	* Minimum values for the typical operating condit.  The values for the worst case operating condit.						ng condition		
					naximum				

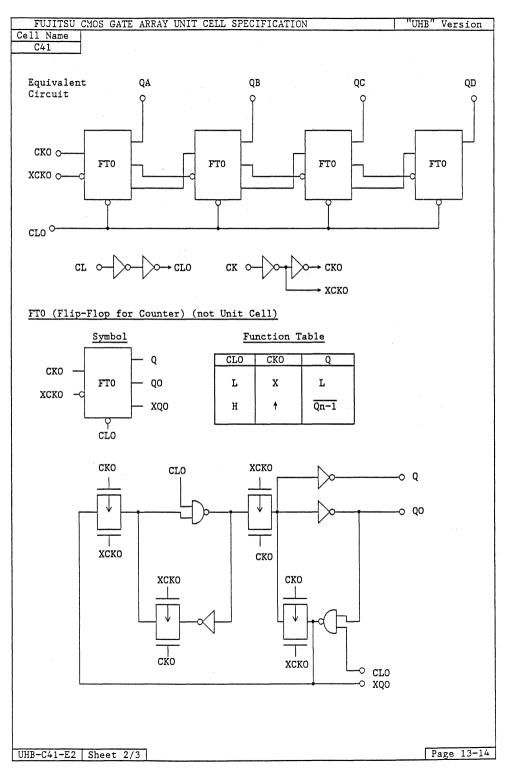
L	D	TG	CL	СК	Q(Q <sub>0</sub> )
х	Х	Х	L	х	L
Н	Н	х	н	1	н
н	L	х	н	+	L
L	х	L	н	+	Q(Q <sub>0</sub> )
L	х	н	н	+	$\overline{\mathbb{Q}}(\overline{\mathbb{Q}_0})$
	X H H	х х н н ц х	х х х н н х т х т	X X X L H  H L X H  L X H	X X X L X H H X H † H L X H †

UHB-C11-E3 Sheet 1/2



FULTER	CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version							
Cell Name	Function	.,,,	D DI DOL	TONITO	.,			Number of BC
C41	Non-SCAN 4-bit	Rinary	Asynchr	onous C	ounter			24
Cell Symbol	NOI DOMY + DIC	Dinary			Delay	Paramet	PT	
GOLL DYMEST		t	up	46441011	td		,,,,,	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.00	0.14	1.86	0.10	_	_	CK → QA
		3.67	0.14	3.28	0.10	-	-	CK → QB
		5.13	0.14	4.75	0.10	-	-	CK → QC
		6.60	0.14	6.20	0.10	-	-	CK → QD
l . г		-	-	4.19	0.10	-	-	CL → Q
ск	——— QA ——— QB ——— QD							
L		Parame	ter			1 5	vmbol	Typ(ns)*
	Ĭ	Clock Pulse Width					tCW	4.3
	1	Clock Pause Time					tCWH	4.6
	CL							
		Clear	Pulse W	idth			tLW	3.9
		Clear	Release	Time			tREM	2.1
	Input Loading	Clear	Hold Ti	me			tINH	6.7
Pin Name	Factor (lu)							
CK	1							
CL	1							1
ĺ		1						
j	1							1
	<u> </u>							
l	Output Driving							
Pin Name	Factor (lu)					- 1		
Q	18							
	* Minimum values for the typical operating cond The values for the worst case operating condi are given by the maximum delay multiplier.						ng condition	

Inp	uts	Outputs				
CL	CK	Q				
H L	† X	Count up L				



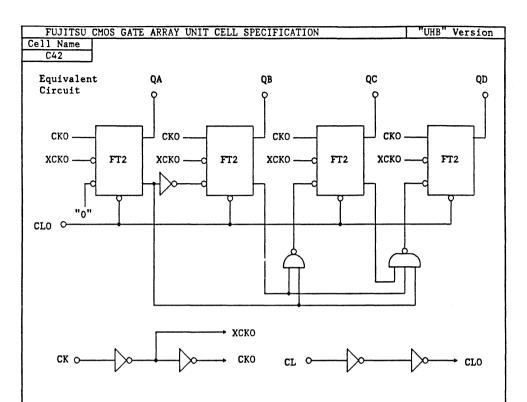
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name C41 Definition of Parameters tCWH -CK t<sub>REM→</sub>  $t_{INH}$ 

UHB-C41-E2 | Sheet 3/3

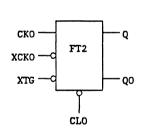
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" [	HB" Version
	Function							Number of BC
C42 Cell Symbol	Non-SCAN 4-bit	Binary	Synchro	nous Co agation	unter	Daramot	0.5	32
cell Symbol		+	up up	agation	td		er	<del></del>
		to	KCL	t0	KCL	KCL2	CDR2	Path
		3.18	0.14	2.34	0.09	0.12	4	CK → Q
				3.36	0.09	0.12	4	CL + Q
ск —	QA QB QC QD		ter Pulse W Pause T	lidth	0.03	S	ymbol tCW	
	CL							
			Pulse W Release				tLW tREM	4.0
	Input Loading		<u>Kelease</u> Hold Ti				tINH	6.7
Pin Name	Factor (lu)	Cleal	noru II	me			CIM	<del></del>
CL CK	1							
	Output Driving	1						
Pin Name	Factor (lu)							
Q	18	1						
	* Minimum values for the typical operating condi The values for the worst case operating condit are given by the maximum delay multiplier.							ng condition

Inp	uts	Outputs				
CL	CK	Q				
H L	† X	Count up L				

UHB-C42-E3 | Sheet 1/3



FT2 (Flip-Flop for Counter) (not Unit Cell)

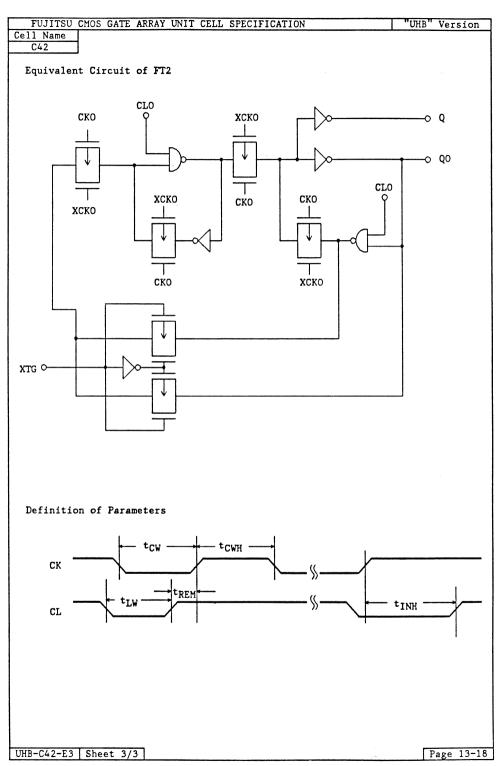


Symbol

Function Table

	Inputs CLO XTG CKO							
CLO	XTG	Q(Q0)						
L	x	x	L					
н	н	<b>†</b>	Qn-1					
н	L	+	Qn-1					

UHB-C42-E3 | Sheet 2/3

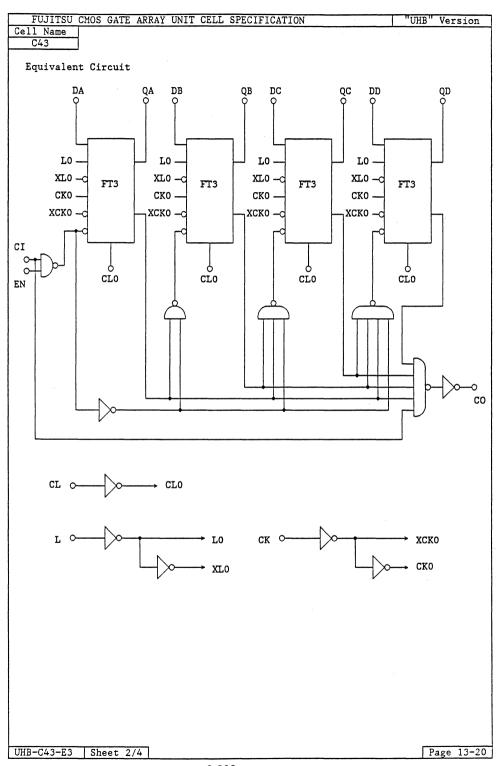


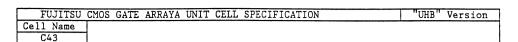
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version
Cell Name	Function							Number of BC
7/0					_			
C43	Non-SCAN 4-bit	Binary						48
Cell Symbol	·			agation	Delay		er	
		tup tdn						_
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.96	0.16	2.40	0.09			CK → Q
		5.60	0.16	3.56	0.08			CK → CO
		1.60	0.16					CI → CO
		-	-	3.88	0.09			CL → Q
Г		-	-	2.64	0.08			CT → CO
DA -	QA							
DB —	—— QB							
DC -	— QC							
DD	<u></u> qp							
l r—d								
CK -								
EN -								
CI -	со							
_	<del></del>	Parameter					ymbol	Typ(ns)*
İ		Clock Pulse Width						4.7
	CL	Clock	Pause T	ime		tCWH	6.7	
	CL	Data S	etup Ti	me		tSD	2.6	
		Data Hold Time						2.9
		Load S	etup Ti	me			tSL	4.4
	Input Loading		old Tim				tHL	1.3
Pin Name	Factor (lu)		up Time				tSC	4.3
D	1		d Time				tHC	0.9
L,EN	1		up Time				tSE	4.3
CK,CL	1		d Time				tHE	0.9
CI	2		Pulse W				tLW	5.6
			Release				tREM	1.9
	Output Driving	Clear	Hold Ti	me			tINH	8.3
Pin Name	Factor (lu)							
Q	18							
CO	18							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
ļ		The values for the worst case operating condition					ng condition	
	1	are	given b	y the m	aximum	delay m	ultip	lier.
	are given by the maximum delay multiplier.							

		Outputs				
CI	L	D	EN	CI	CK	Q
L H H H	X L H H	X H L X X	X X X X L H	X X X L X H	X † X X	L H L No Counting No Counting Count up

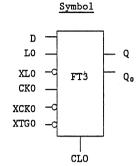
Note: The CO output produces a high level output data when the counter overflows.

UHB-C43-E3 Sheet 1/4



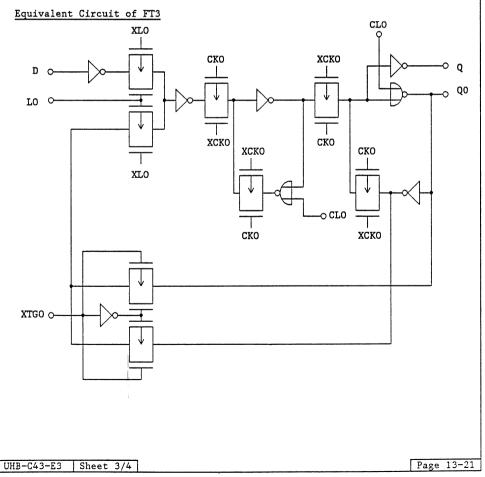


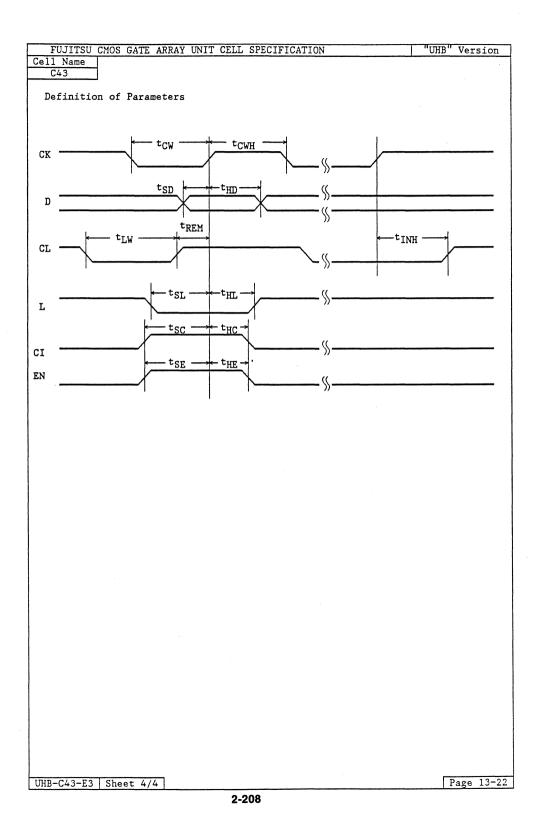
· FT3 (Flip-Flop for Counter)(not Unit Cell)



Function Table

LO	D	XTG0	CLO	CK	Q(Q0)
X H H L	X H L X X	T X X X	H L L	X ^ ^	L H L Q(Q0) Q(Q0)



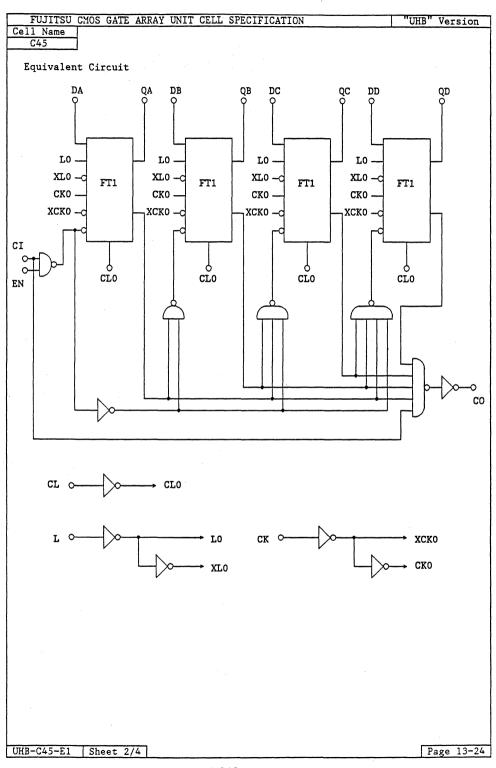


FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			HB" Version
	Function						<u> </u>	Number of BC
C45	Non-SCAN 4-bit	Binarv	Synchro	nous Up	Counte	r	4	48
Cell Symbol		Propagation Delay Parameter						
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.67	0.14	1.87	0.09	0.13	4	CK → Q
		5.07	0.17	2.82	0.09			CK → CO
		1.91	0.17	1.36	0.09			CI → CO
-								
DA	QA						j	į į
DB —	— QB							
DC —								
DD —	├── ḡn							1
L	_							ŀ
CK -								
EN -								
CI —	co						l	
	<del></del>	Parame	ter			1 5	ymbol	Typ(ns)*
	Ĭ		Pulse W	idth			tCW	4.0
		Clock Pause Time					tCWH	4.6
	CL	Data Setup Time					tSD	3.8
1		Data Hold Time					tHD	2.1
		Load S	etup Ti	me			tSL	5.0
	Input Loading		old Tim				tHL	2.1
Pin Name	Factor (lu)	CI Set	up Time				tSC	6.6
D	1		d Time	***************************************			tHC	1.9
L,EN	1	EN Set	up Time				tSE	6.6
CK,CL	1		d Time				tHE	1.9
CI	2	Clear	Setup T	'ime			tSR	3.8
		Clear	Hold Ti	me			tHR	2.0
	Output Driving							
Pin Name	Factor (lu)							
Q	18							
co	18							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
1								ng condition
	are given by the maximum delay multiplier.							

		Outputs				
CL	L	D	EN	CI	CK	Q
L H H H H	X L L H H	X H L X X	X X X L H	X X X L X H	† † X X	L H L No Counting No Counting Count up

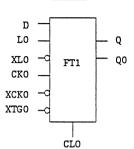
Note : The CO output produces a high level output data when the counter overflows.

UHB-C45-E1 | Sheet 1/4





· FT1 (Flip-Flop for Counter)(not Unit Cell)

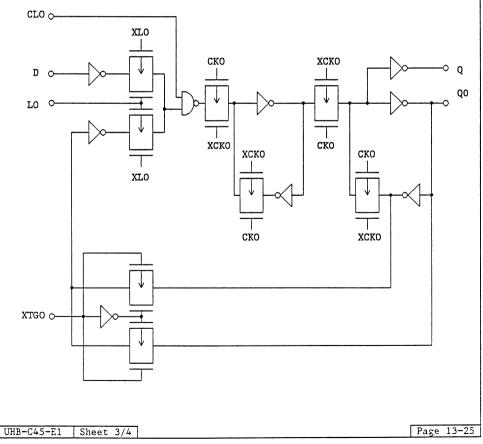


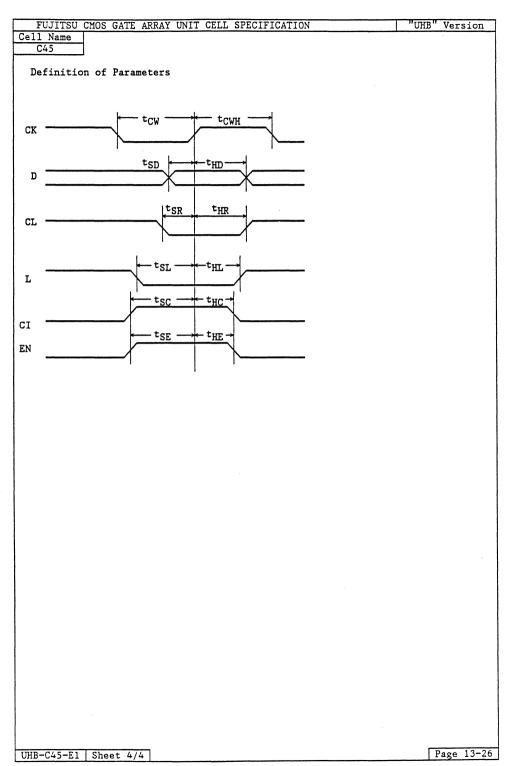
Symbol

# Function Table

LO	D	XTG0	CL0	CK	Q(Q0)
L H H L	X H L X	X X H L	H L L L	++++	L H L Q(Q0) Q(Q0)

### Equivalent Circuit of FT3



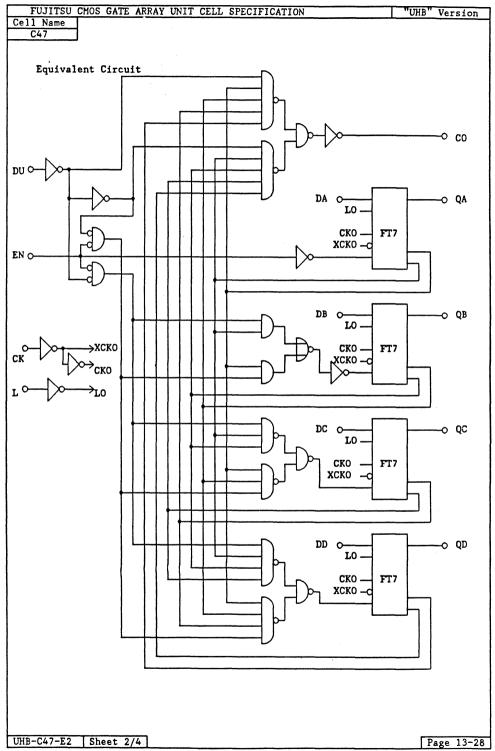


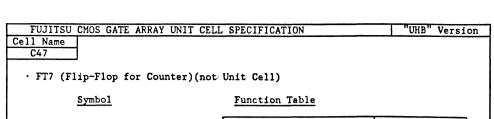
FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version	
Cell Name	Function							Number of BC	
C47	Non-SCAN 4-bit	Binary	Synchro	nous Up	/Down C	ounter		68	
Cell Symbol				agation			er		
		t0	tup tdn t0 KCL t0 KCL KCL				CDR2	<b>-</b>	
		3.99	0.16	t0 3.59	KCL 0.16	KCL2 0.25	4		
		5.41	0.10		0.18	0.23	*	CK → Q CK → CO	
		5.01	0.11		0.08	0.25	4	L + Q	
		2.47	0.10	3.01	0.18	0.23	•	DU → CO	
_		2.47	0.11	3.01	0.08		1	1 20 4 60	
DA ————————————————————————————————————	QA QB QC QD								
<b>-</b>		Parame			*****	-   5	Symbol		
			Pulse W				tCW	5.6	
		Clock	Pause T	ime			tCWH	8.9	
			etup Ti				tSD tHD	0.7	
	T	Data Hold Time tl						1.8	
Pin Name	Input Loading Factor (lu)	DIL Cot	up Time				tSU	5.3	
D D	ractor (ku)		d Time				tHU	0.8	
L L	2	וסוו טע	u iime				LIIU	- 0.8	
ממ	1	EN Set	up Time				tSE	5.0	
CK	i							1.2	
EN	3	21, 1.01	- Alme			-+-	tHE	<del></del>	
		Clear	Release	Time		tREM	2.3		
	Output Driving		Hold Ti				tINH	11.1	
Pin Name	Factor (lu)								
Q	18	Load P	ulse Wi	dth			tLW	4.6	
co	18	The	values		worst	case or	erati	ing condition ng condition lier.	

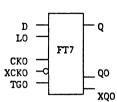
			Inp	uts		Outputs
	₹	L	EN	DU -	CK	Q
) )		L L H H	X H L	X X X L H	X X † †	H L No Counting Count Up Count Down

Note: The CO output produces a low level output pulse when the counter overflows or underflows.

UHB-C47-E2 | Sheet 1/4

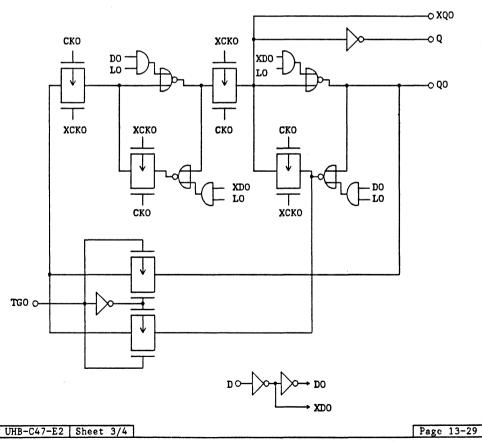


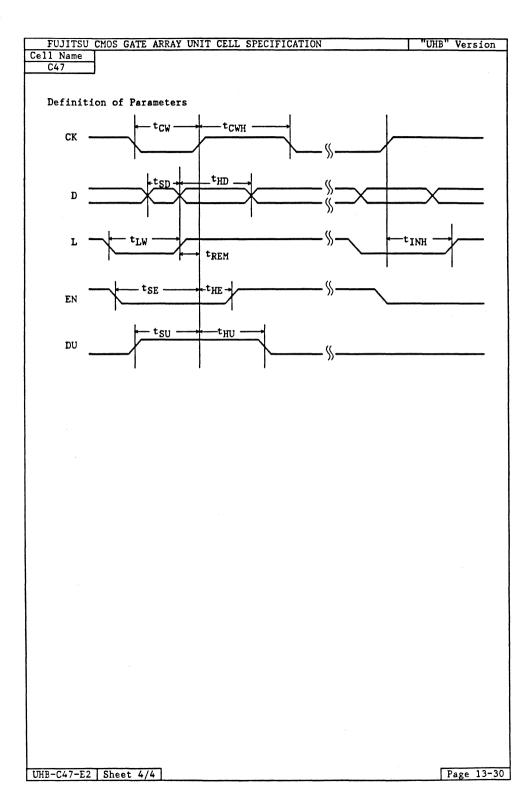




	Inp		Outputs			
LO	D	TGO	CKO	Q0(Q)	<u>Q</u> (Q0)	
H	н	x	x	н	L	
н	L	х	х	L	н	
L	x	L	<b>+</b>	Qn-1	Qn−1	
L	х	н	†	Qn−1	Qn-1	

# Equivalent Circuit of FT7





# **Adder Family**

F	Page	Unit Cell Name	Function	Basic Cells
2	2-219	A1A	1-bit Half Adder	5
2	2–220	A1N	1-bit Full Adder	8
2	2-221	A2N	2-bit Full Adder	16
2	2-223	A4H	4-bit Binary Full Adder with Fast Carry	48

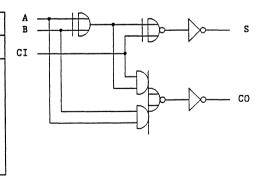
	CMOS GATE ARR Function	AY UNIT C	ELL SPECI	FICATIO	N			B" Version Number of BC		
CEII Name	Tanceron							TOWNET OF BO		
AlA	1-bit Half	Adder						5		
Cell Symbol			Propagation Delay Parameter							
		t0	KCL	to	KCL KCL	n KCL2	CDR2	- Bath		
		1.2		1.44	0.04	KULZ	CDRZ	Path A → S		
		1.09			•		1	B → S		
		1.13		1.25				A → CO		
		1.2	7 0.08	1.15	0.04			B → CO		
			1	1			1			
			1					İ		
В	со			1	1		1			
Α —	s				ł					
		İ		1		1	1			
_						1				
				ļ						
		Darra	reter	L	L	<del></del>	Symbol	Typ(ns)*		
		rarai	meter				оушоот	TAb(H2)		
						1				
						1				
						1				
						1				
	Input Loadi	<del></del>								
Pin Name	Factor (lu)									
A	2					ı				
В	2	-				Ì				
	İ					ı				
		į				1				
	Output Driv	100								
Pin Name	Factor (lu)	ing				İ				
CO	36									
s	36									
		* M1:	nimum val	lues for	the ty	pical	operati	ng condition.		
		The	e values e given l	for the	worst	case o	peratin	ng condition		
	1	ar	e given i	by the n	aximum	delay	multipi	.ier.		
Function	Table			Equival	ent Cir	cuit				
_			A -			-A				
A	в со	S	В –		1	Н,	b-1>	o— s		
L	L L	L				T	/ V	<del>-</del>		
		H								
	i li	н			15	_	N	<b>^</b>		
		L				D-+	$ \vee$	○ со		
							•			
UHB-A1A-E2	Sheet 1/1							Page 14-1		

FILITTEIL	CMOS GATE ARRAY U	NIT CEL	I SPECT	FICATIO	N		1 1111	HB" Version	
Cell Name	Function	NII OLD	D BILCI	FICATIO	N		<del>- 1 - 1</del>	Number of BC	
JOIL NAME	1 411001011							THE POLICE OF BO	
A1N	1-bit Full Adde	r						8	
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t	up		td				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		2.64	0.16	3.15	0.08			A,B → S	
		1.25	0.16	1.35	0.08			CI → S	
		2.98	0.16	2.38	0.08			A,B → CO	
		1.02	0.16	1.17	0.08			CI → CO	
В	co								
A -	s								
_									
	CI								
	CI	Parame	<u></u>				ymbol	Typ(ns)*	
		rarame	rer				ymbor	Typ(IIS)	
						- 1			
						į			
		}							
						ì			
	Input Loading	İ						ĺ	
Pin Name	Factor (lu)	İ				1			
A	3	1				1			
В	3					j			
CI	3							1	
	Output Driving	1				- 1		1	
Pin Name	Factor (lu)	l							
CO	18	1							
S	18								
								ing condition	
	The values for the worst case operating condition								
		are	given b	y the m	aximum	delay m	ultip	lier.	

UHB-A1N-E2 | Sheet 1/1

	Input	s	Out	outs
A	В	CI	s	СО
L H L H L H	L H H L H	L L L H H	L H L H L L	L L H L H

# Equivalent Circuit



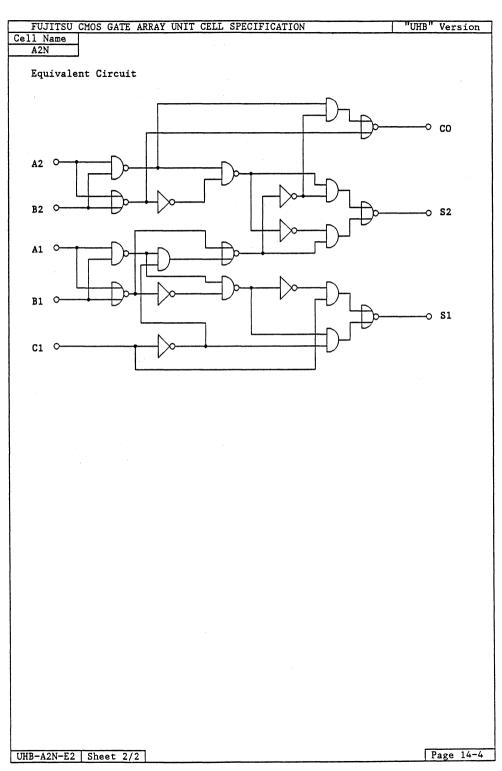
Page 14-2

FUJITSU CMOS GATE ARRAY	UNIT CEL	L SPECI	FICATIO	N		"UH	IB" Version	
Cell Name   Function							Number of BC	
A2N 2-bit Full Add	er						16	
Cell Symbol			agation	Delay		er		
		up		td			<b>-</b>	
	t0	KCL	t0	KCL	KCL2	CDR2	Path	
	2.85	0.29	2.81	0.14			A1 → CO	
	2.74	0.29	2.87	0.14			B1 → CO	
	1.58	0.29	1.36	0.09	0.12	4	A2 → C0	
	1.47	0.29	1.36	0.09	0.12	4	B2 → C0	
70 - 70	2.79	0.29	2.58	0.14			CI → CO	
B2 CO	2.97	0.22	2.75	0.14			A1 → S1 B1 → S1	
B1 S2		0.22		0.14 0.14			B1 → S1   CI → S1	
A1 - S1	1.18	0.22	1.19	0.14			A1 → S2	
A1 51	3.11	0.22	2.75	0.14			$\begin{array}{c} A1 \rightarrow 32 \\ A2 \rightarrow S2 \end{array}$	
	2.71	0.22	2.81	0.14			B1 → S2	
	3.11	0.22	2.95	0.14			B2 → S2	
l ci	2.76	0.22	2.52	0.14			CI → S2	
		V.22		0121				
	Parame	ter		· · · · · · · · · · · · · · · · · · ·	S	ymbol	Typ(ns)*	
					Ì			
Input Loading					ļ			
Pin Name Factor (lu)								
A,B 2					l			
CI 2					l			
					l			
					l			
Output Driving	+				-			
Pin Name Factor (lu)					l			
S 14	+				1			
CO 14								
	* Mini	mum val	ues for	the tv	pical o	perati	ng condition.	
	* Minimum values for the typical operating condition.  The values for the worst case operating condition							
				aximum				

	Inpu	ıts				Out	puts			
				(	I = I		CI = H			
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO	
L	L	L	L	L	L	L	H	L	L	
H	L	L	L	H	L	L	L	H	L	
L	H	L	L	H	L	L	L	H	L	
Н	H	L	L	L	H	L	H	H	L	
L	L	H	L	L	H	L	H	H	L	
H	L	H	L	H	H	L	L	L	H	
L	H	H	L	H	H	L	L	L	H	
H	H	H	L	L	L	H	H	L	H	
L	L	L	H	L	H	L	H	H	L	
H	L	L	H	H	H	L	L	L	H	
L	H	L	H	H	H	L	L	L	H	
Н	H	L	H	L	L	H	H	L	H	
L	L	H	H	L	L	H	H	L	H	
Н	L	H	H	Н	L	H	L	H	H	
L	Н	H	Н	Н	L	H	L	H	H	
H	H	H	H	L	H	H	Н	H	H	

UHB-A2N-E2 | Sheet 1/2

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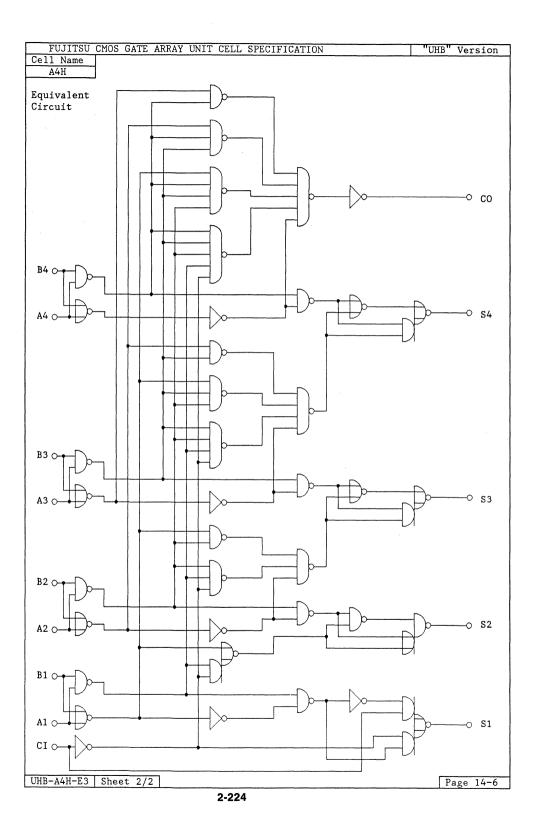
THE TAX ASSESSMENT OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY OF THE PARTY							1 11	
	MOS GATE ARRAY U	NIT CEL	L SPECI.	F1CATIO	N			" Version
Cell Name	Function						1	Number of BC
A4H	A-bit Dinama En	11 444		East Ca				48
Cell Symbol	4-bit Binary Fu	II Adde	Prop	agation	Dolon	Damamat		40
Cell Symbol		+		agation	td		er	T
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		1.18	0.22	1.63	0.14	RODZ	ODKZ	CI → S1
		2.65	0.22	3.07	0.14			CI → S2
		3.03	0.29	2.98	0.14			CI → S3
В4	co	3.14	0.29	3.54	0.14			CI → S4
A4 —	s4	2.87	0.16	3.21	0.08			CI → CO
ВЗ —		2.07	0.10	J.21	0.00			01 00
A3 -	s3	3.81	0.22	3.39	0.14			A1,B1 → S1
B2		3.17	0.29	3.08	0.14			A1,B1 → S2
A2	S2	3.42	0.29	3.85	0.14			A1,B1 → S3
B1		3.75	0.29	3.92	0.14			A1,B1 → S4
A1	s1	3.30	0.16	3.78	0.08			A1,B1 → CO
								,
		3.09	0.29	3.37	0.14			A2,B2 → S2
	i	3.66	0.29	3.60	0.14			A2,B2 → S3
	CI	3.74	0.29	4.05	0.14			$A2,B2 \rightarrow S4$
		3.87	0.16	3.83	0.08			A2,B2 → CO
	Input Loading	2.81	0.29	2.85	0.14			A3,B3 → S3
Pin Name	Factor (lu)	3.84	0.29	4.04	0.14			A3,B3 → S4
A	2	3.80	0.16	3.82	0.08			A3,B3 → CO
В	2							
CI	2	2.90	0.22	3.01	0.09	0.12	4	$A4,B4 \rightarrow S4$
		3.66	0.16	3.51	0.08			A4,B4 → CO
	Output Driving							
Pin Name	Factor (lu)						Ì	
CO	18						L	J
\$1,83,84	14							
S2	18							
	I	L						

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					OUTPUT						
A1         B1         A2         B2         B4         B3         S4         B4         B3         S2         C2         S1         S2         C2           L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L		INP	UT		CI	= <u>I</u>	:		= }	<u> </u>	
A3         B3         A4         B4         S3         S4         CO         S3         S4         CO           L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L <td< td=""><td></td><td></td><td>4.0</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>			4.0								
L L L L L L L L H L L H L L H L L H L L H L L H L L H L L H L L H L L H L L H L L H L L H L L L H L L L H L L L H L L L H L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L L H L L L L L H L L L L L H L L L L L H L L L L L H L L L L L L H L L L L L L H L L L L L L L H L L L L L L L L L H L L L L L L L L L L L L L L L L L L L L				<u> </u>	$-\frac{S1}{}$		<u>C2</u>	<u> </u>	. <u>52</u> _		
H L L L H L L L H L L H L L H L L L H L H H L L L H L H	A3	В3	A4	B4	S3	S4	CO	S3	S4	CO	
H L L L H L L L H L L H L L H L L L H L H H L L L H L H	_	_	_	_	۱ _	_	_		_	_	
L H L L H L L H L L H L L H H L L L H H L L H H L L H H L H L H H L H L H H L H L H H L H L H H L H L H H L H L H H L H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H H L H H H L H H H L H H H L H H H L H H H H H H H H H H H H H H H H H H H H					i .			L			
H H L L L L H L H H L L L H L H L H H L H L H L	H	L	L	L	Н	L	L	L	H	L	
L L H L H L H H L H H L H L H L H L H L	L	H	L	$\mathbf{L}$	H	$\mathbf{L}$	L	L	H	L	
H L H L H H L L L H L H H L H H L L L H H H L L L H H L H L L L H L H	H	H	$\mathbf{L}$	L	L	H	L	Н	H	L	
L H H L H H L L L H H L H L H L H L H L	L	L	H	L	L	H	L	Н	H	L	
L H H L H H L L L H H L H L H L H L H L	Н	L	H	L	н	H	L	L	L	H	
H H H L L L H H L H L L L H L H L H L L L H L H	L	Н	Н		н	Н		L	L	H	
L L L H L H L H L L H L H L L H L L H L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L H L L L L H L L L H L L L L H L L L L H L L L L H L L L L H L L L L H L L L L L H L L L L L H L L L L L L L L L L L L L L L L L L L L	Н	Н	Н	L	L	L	H	н	L	Н	
H L L H H H L L L H H H L H H L L L H H H L H L								1			
L H L H H H L L L H H L L L H H L H L H								1			
H H L H L L H H L H L L H H L H H L H H L H L								i .			
L L H H L L H H L H H L H H L H H L H H L H H L H H L H H L H H L H H								I			
					5						
								1			
l l					l						
					l .			1			
	H	H	H	H	L	Н	H	H	H	H	

#### Note:

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Page 14-5



# **Data Latch Family**

Page	Unit Cell Name	Function	Basic Cells
2-227	YL2	Data Latch with TM	5
2-229	YL4	Data Latch with TM	14
2-231	LTK	Data Latch	4
2-233	LTL	Data Latch with Clear	5
2-235	LTM	Data Latch with Clear	16
2-238	LT1	S-R Latch with Clear	4
2-240	LT4	Data Latch	14

2

FUJITSU CMOS GATE ARRAY UN Cell Name Function  YL2 1-bit Data Latch Cell Symbol  D — Q CK — C IH — TM — C	with	TM	agation t0 2.81 1.28				B" Version Number of BC  5  Path CK,IH + Q D + Q
D — Q СК — С IH —	t0 2.73	Propug up KCL 0.08	t0 2.81	KCL 0.04	n		Path CK,IH → Q
р — Q ск — с IH —	t0 2.73	WCL 0.08	t0 2.81	KCL 0.04	n		CK,IH → Q
ск — с ін —	t0 2.73	KCL 0.08	2.81	KCL 0.04		CDR2	CK,IH → Q
ск — с ін —	2.73	0.08	2.81	0.04	KCL2	CDR2	CK,IH → Q
ск — с ін —							
ск — с ін —	1.10	0.00	1.20	0.04			1 2 , 4
ск — с ін —						1	
	Parameter					ymbol	Typ(ns)*
	Clock Pulse Width					tCW	6.8
<del> </del>	Clock Pulse width					LUW	1 0.0
	Data Setup Time					tSD	3.2
	Data Hold Time					tHD	2.5
Input Loading							ļ
Pin Name Factor (Lu) D 2							1
CK 1 1					i		
I IH I I							
TM 1							
Output Driving							
Pin Name Factor (Lu)					1		1
Q 36					1		1
`	* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.						

# Note:

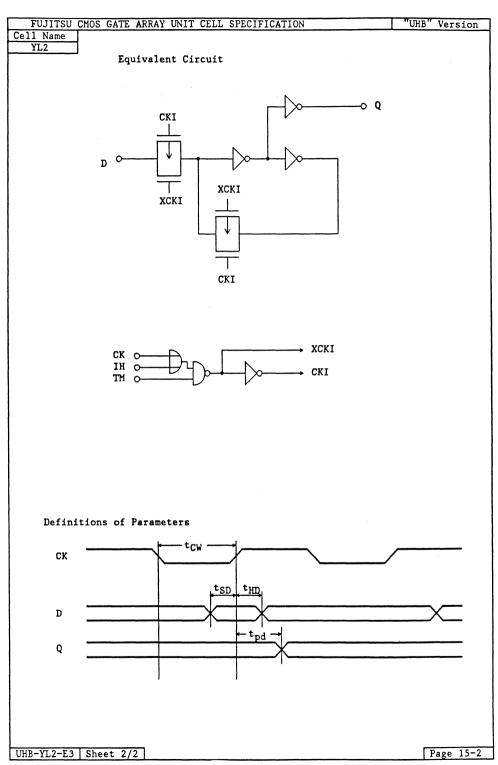
The TM terminal must be kept LOW during the SCAN Mode.

### Function Table

	Inp	ut		Output	Mode		
TM	IH	CK	D	Q	node		
L	X	X	D	D	SCAN		
H	H	X	X	Q <sub>0</sub>			
H	X	Н	X	l Q₀ l	LATCH		
Н	L	L	D	D			

UHB-YL2-E3 | Sheet 1/2

Page 15-1



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
	11 Name   Function   Number of BO							Number of BC
YL4	4-bit Data Late	h with			D. 1	D 4 -		14
Cell Symbol				agation	Delay td	Paramete	er	
Ì	t0	up KCL	t0	KCL	KCL2	CDR2	Path	
	3.33	0.08	3.43	0.04	KOBL	ODKZ	CK,IH → Q	
		1.10	0.08	1.29	0.04	l		$D \rightarrow Q$
D1 — D2 — D3 — D4 — CK — C IH — TM — C	— Q1 — Q2 — Q3 — Q4		ter Pulse W		(CK	) 1	ymbol cCW	Typ(ns)* 7.2
	Data Hold Time (D)					HD	4.0	
Pin Name D CK IH TM	Input Loading Factor (lu)  2 1 1 1							
Pin Name	Output Driving Factor (lu)							
*		The	values :	for the	worst		eratin	ing condition.  ag condition  ier.

#### Note:

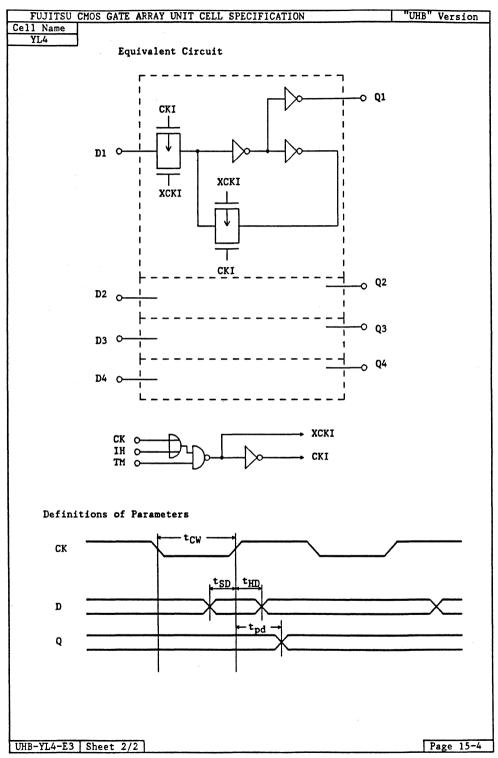
The TM terminal must be kept LOW during the SCAN Mode.

### Function Table

	Inp	ut		Output	Mode			
TM	IH	CK	Dn	Qn	node			
L	X	X	D	D	SCAN			
H	Н	X	X	Qno				
H	X	Н	Х	Qno	LATCH			
Н	L	L	D	D				
n = 1 ~ 4								

UHB-YL4-E3 | Sheet 1/2

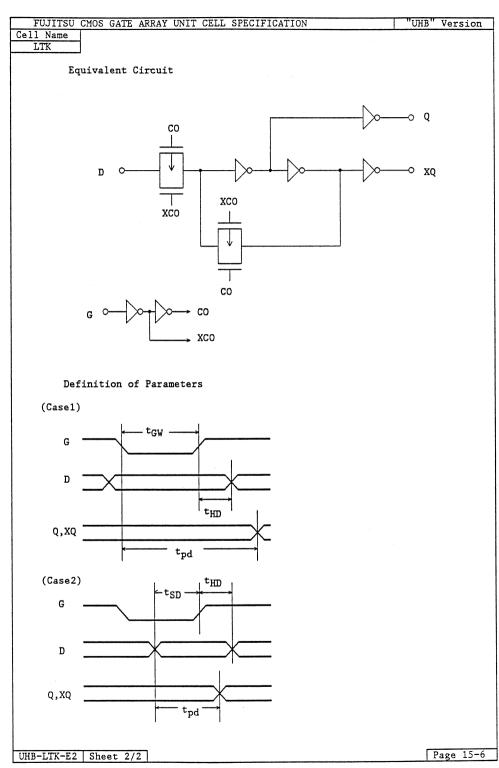
Page 15-3



FULITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		1"[]	THB" Version
Cell Name	Function	1111 000	0.001	1 1 0 1 1 1 1 0	••			Number of BC
LTK	Data Latch							4
Cell Symbol								
			up		td		anna	<b>-</b>
		t0	KCL 0.16	t0 1.15	KCL 0.08	KCL2	CDR2	Path D → Q
		1.03						$D \rightarrow Q$ $D \rightarrow XQ$
		1.75	0.16		0.08			$G \rightarrow Q$
		2.12	0.16	2.34	0.08			G → XQ
			0.10	2.54	0.00			1
-	<del></del>							
D —	—— Q							
G —d								
1 1								
1	p xq							
_								
		Parame	tor		l		ymbol	. Typ(ns)*
			G Input Pulse Width tGW					4.0
		0 11100 11100 11100						
		Data Setup Time tSD					tSD	1.6
		Data H	old Tim	e			tHD	2.3
	1							
Din Nama	Input Loading							
Pin Name D	Factor (lu)							
G	1							
"	1							
1								
	Output Driving					1		
Pin Name	Factor (lu)					.		
Q	18							
XQ	18	l	_	_				
								ing condition.
								ing condition
		are	given p	y the m	aximum	deray m	ultil	TITEL.

Ing	outs	Outputs				
D	G	Q	ХQ			
X H L	H L L	Q <sub>o</sub> H L	XQ <sub>o</sub> L H			

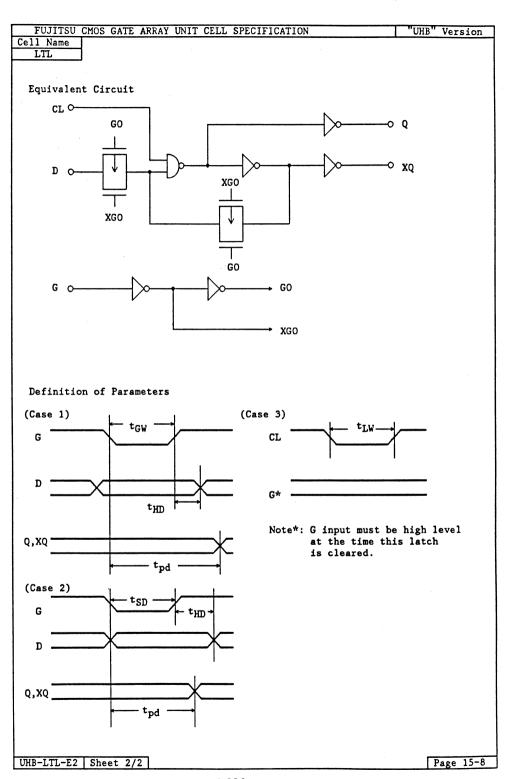
UHB-LTK-E2 | Sheet 1/2 | Page 15-5



FILTER	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function	NII CEL	L SPECI	FICATIO.	N			Number of BC			
DETT Name	runction							Number of BC			
LTL	1-bit Data Lato	h with	Clear					5			
Cell Symbol				agation	Delay	Paramet	er				
		t	up		td						
İ		t0	KCL	t0	KCL	KCL2	LD2				
		1.39	0.16	0.85	0.09			CL → Q,XQ			
		1.18	0.16	1.22	0.09			$D \rightarrow Q$			
		1.52	0.16	1.71	0.09			$D \rightarrow XQ$			
		1.96	0.16	1.92	0.09			G → Q			
	<del></del>	2.22	0.16	2.51	0.09		l	G → XQ			
D	├─ Q						1				
G		1					1				
							i				
	р—— <b>х</b> q	1									
	9						l				
		1 1					1	1 1			
	CL										
	OD	Parame					ymbol				
1		G Input Pulse Width					tGW	4.0			
		D + C + Ti									
		Data Setup Time					tSD tHD	1.3			
		Data Hold Time tH					(III)	1 0.3			
		Clear	Pulse W	idth			tLW	4.0			
	Input Loading										
Pin Name	Factor (lu)	1				- 1		[			
D	2	1									
G	1	]				1					
CL	1										
						1		1			
ļ	ļ	ļ									
D/- V	Output Driving					1					
Pin Name	Factor (lu)	ł									
Q XQ	18										
AQ	18										
	* Minimum values for the typical operating condition.  The values for the worst case operating condition										
	are given by the maximum delay multiplier.										

Iı	nput	Outputs			
CL	D	G	Q	XQ	
L H H	X X H L	H H L	L Q. H L	H XQ. L H	

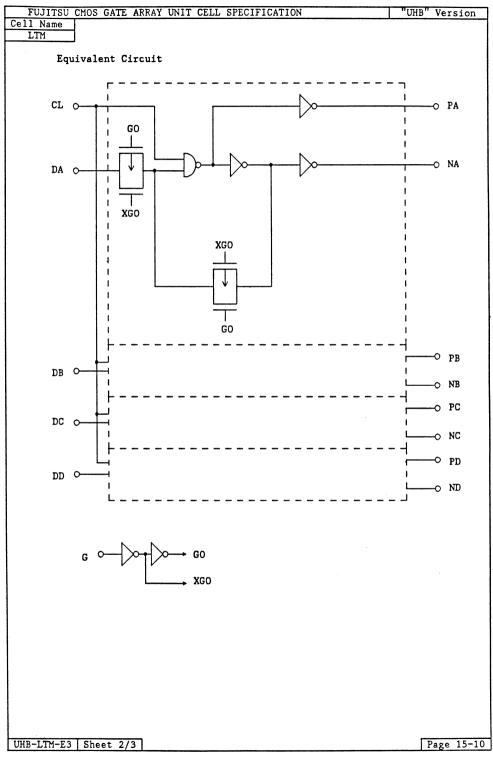
UHB-LTL-E2 | Sheet 1/2



FILITSII (	CMOS GATE ARRAY U	NIT CEL	T. SPECT	FICATIO	N N		1 "11	HB" Version
Cell Name	Function	NII CEL	D BILCI.	r TORTTO				Number of BC
LTM	4-bit Data Late	h with	Clear					16
Cell Symbol		I		agation	Delay	Paramet	er	
		t	up		td	n		
		t0	KCL	tO·	KCL	KCL2	CDR2	
		1.54	0.16	0.97	0.08			CL → P,N
ļ		1.22	0.16	1.29	0.08			$D \rightarrow P$
		1.60	0 16	1.79	0.08			$D \rightarrow N$
		2.61	0.16		0.08			G → P
DA -	PA	2.73	0 16	3.15	0.08			G → N
DB —	P— NA							
DC -	PB	1						1
DD -	р— ив	1 1						
G	PC						l	
1	PD NC						ĺ	
1	р— ND						ł	
	N						1	
	Y	Parame	ter			1 8	ymbol	Typ(ns)*
	1	G Input Pulse Width					tGW	4.0
	CL							
		Clear Pulse Width t					tLW	4.0
		Data Setup Time tS					tSD	1.6
							tHD	2.3
		1				1		
1	Input Loading	1				i		
Pin Name	Factor (lu)	ł						
D G	1							
CL	4					- 1		
02	1	Ì				- 1		
}								
<del> </del>	Output Driving	1				i		
Pin Name	Factor (lu)					l		
P	18	1						
N	18	<u> </u>						
1		* Mini	mum val	ues for	the tv	pical c	perat	ing condition.
	* Minimum values for the typical operating condition The values for the worst case operating condition							
				y the m				
<del></del>								

Ir	put	Outputs			
CL	D	G	P	N	
L H H	X X H L	H H L	L P <sub>0</sub> H L	H No L H	

UHB-LTM-E3 Sheet 1/3

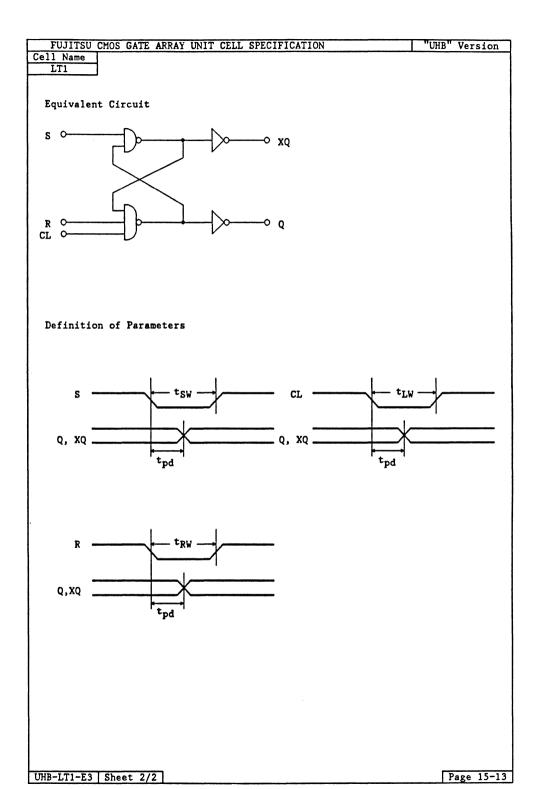


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name LTM Definition of Parameters (Case1) -t<sub>GW</sub> -G D P,N (Case2) G D  $t_{SD}$  $\mathsf{t}_{\text{HD}}$ P,N (Case3) CL **∗**G P,N Note \*: G input must be high level at the time this latch is cleared. Page 15-11 UHB-LTM-E3 | Sheet 3/3

FUJITSU	CMOS GATE ARRAY I	NIT CEL	L SPECI	FICATIO	N		l "U	HB" Version	
Cell Name	Function							Number of BC	
LT1	S-R Latch with	CIFAD						4	
Cell Symbol	B K Datell With	T	Prop	agation	Delay	Parame	eter		
Jell Dymbol		t	up	agacion	td			1	
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		1.76	0.16	0.88	0.08			$S \rightarrow Q, XC$	
		1.56	0.16	1.04	0.08	1	1	$R \rightarrow Q, XC$	
		1.44	0.16	0.92	0.08		1	CL → Q,XC	
						l		,,,,,,	
г						1		1	
s — q	├─ <b>-</b> Q					l	1		
ļ							l		
_	L					l			
<b>г</b> — q	р— xq					Ì	1		
<b>-</b>	<del>-</del>		· '			1	1	I	
								1	
	1	1					1		
	CL	Parame	<u> </u>	<u> </u>	<u> </u>	<del></del>	Symbol	T()+	
			lse Wid	+ h			tSW	Typ(ns)* 4.0	
		Set Fu	ise wid			<del></del>	LOW	+	
		Reset	Pulse W	idth			tRW	4.0	
		Clear	Pulse W	idth			tLW	4.0	
		4							
D/- N	Input Loading								
Pin Name S	Factor (lu)	4				- 1			
R R	1 1								
CL	1 1	1				1			
OL	1	1				1			
						į			
	Output Driving	1				1		1	
Pin Name	Factor (lu)	1				1			
Q	18	1				- 1			
ΧQ	18								
·		* Mini	mum val	ues for	the ty	pical	operat	ing condition	
		The	values	for the	worst	case	operati	ng condition	
		are	given b	y the m	naximum	delay	multip	lier.	
_									
Function	Table								
Inputs		4							
CL S	R Q XQ	-							
ь н	H L H								
н н	H Q XQ	1							
н н	L L H	1							
H L	HHL								
1		I							

Ir	puts	Outputs				
CL	S	R	Q	XQ		
L H H H	H H H L	H H L H L	L Q <sub>0</sub> L H Inh	H XQ <sub>o</sub> H L Lbited		

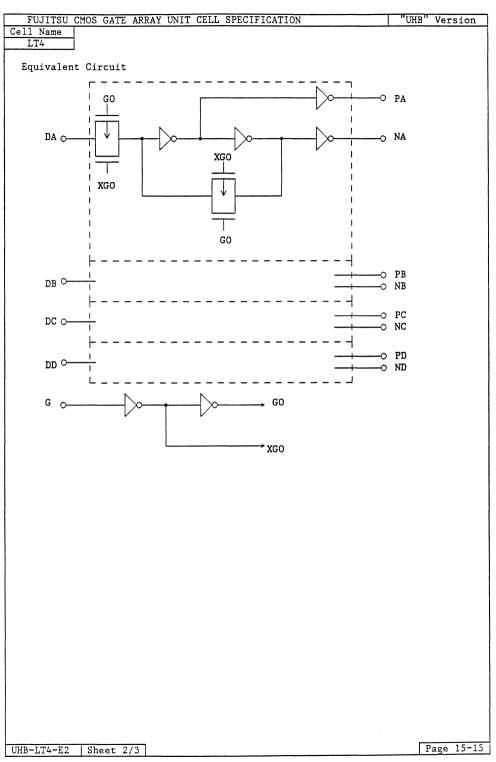
UHB-LT1-E3 | Sheet 1/2

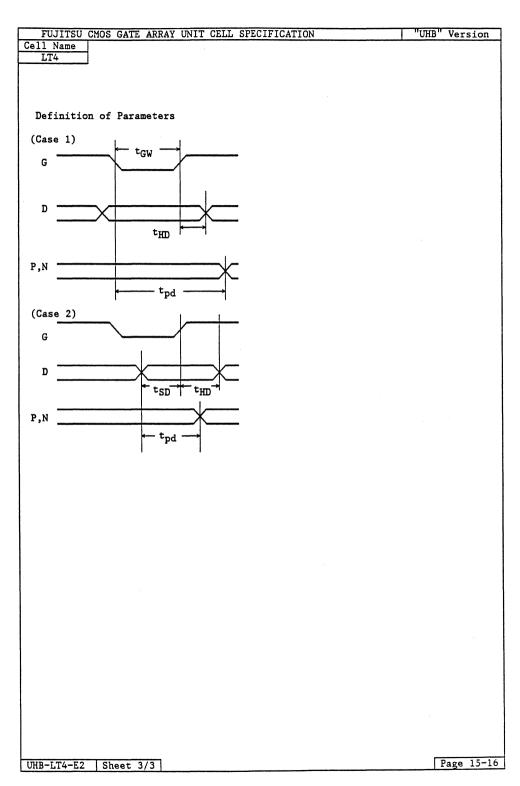


THE TENOUS OF	MOS GATE ARRAY U	NITT CET	CDECT	CTC ATTO			1 1177	TID!! TT
	MUS GATE ARRAY U	NII CEL	L SPECI.	FICALIO.	N		1 0	HB" Version Number of BC
Cell Name	Function							Number of BC
LT4	4-bit Data Latc	h						14
Cell Symbol			Prop	agation	Delay 1	Paramet	er	1
		t	ир		tdi	n.		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.50	0.16	2.28	0.08			G → P
		2.50	0.16	3.05	0.08			G → N
		1.05	0 16	1.18	0.08		l	$D \rightarrow P$
		1.40	0.16	1.60	0.08			$D \rightarrow N$
DA -	PA							
DB —	р— NA						1	
DC —	PB							
מם —	р <del>—</del> мв						l	
<b>G</b> —d	PC							
"	р— ис							
1	PD							
	р— <b>и</b> д							
							1	
1 .		Parame				S	ymbol	
		G Inpu	t Pulse	Width			tGW	4.0
							tSD	1.6
		Data Hold Time tHD					2.3	
						İ		
						- 1		
		ŀ						
	Input Loading					1		
Pin Name	Factor (lu)					1		
D	2							
G	1	1						
								1
	Output Driving							
Pin Name	Factor (lu)							
P	18							
N	18							
1		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
The values for the worst case operating condition are given by the maximum delay multiplier.								
i								

Ing	outs	Outputs				
D	G	P	N			
H L H L	H H L	Po Po H L	No No L H			

UHB-LT4-E2 | Sheet 1/3





# **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
2-245	FS1	Serial-in Parallel-out Shift Register	18
2-247	FS2	Shift Register with Synchronous Load	30
2-249	FS3	Shift Register with Asynchronous Load	34
2-252	SR1	Serial-in Parallel-out Shift Register with Scan	36

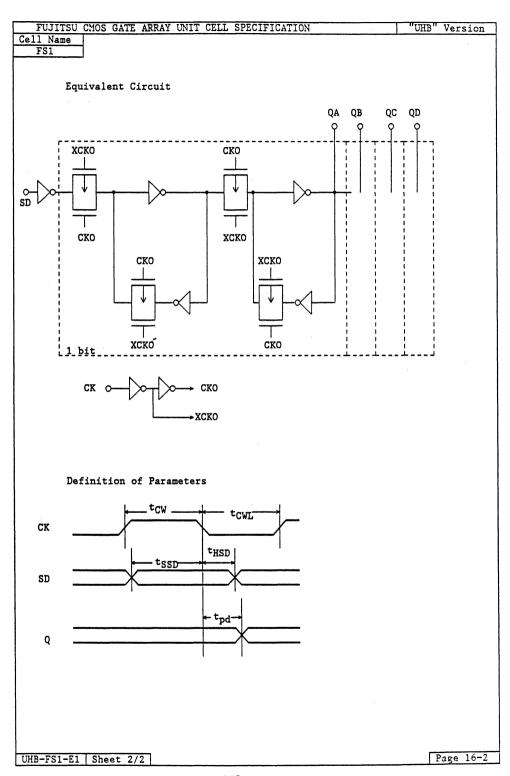
FILITSUC	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
	Function	MII ODD	<u> </u>	TIONITO	11			Number of BC	
FS1	4-bit Serial-in	Parall	el-out	Shift R	egister			18	
Cell Symbol				agation			ter		
		t	up		td				
	•	t0	KCL	t0	KCL	KCL2	CDR2		
		2.42	0.16	3.14	0.09	0.12	4	CK → Q	
SD —c CK —c	QA QB QC QD		Parameter Symb Clock Pulse Width tCW					Typ(ns)* 4.0	
		SD Setup Time					tSSD	0.6	
			d Time				tHSD	0.0	
		101	~ 11me				01100	· · · -	
		Clock		C ≤ 1	6 lu		tCWL*	* 5.8	
	Input Loading	Pause	16	< C ≦ 3			tCWL*	* 8.4	
Pin Name	Factor (lu)	Time	32	< C ≦ 4	8 lu		tCWL*	* 10.9	
SD CK	1 1	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							
Pin Name Q	Output Driving Factor (lu)								

1	Inp	uts		Outp	uts	
	SD	CK	QA	QB	QC	QD
	SD	+	SD	QAn	QBn	QCn

Note:  $\cdot$ SD = H or L

'QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

UHB-FS1-E1 | Sheet 1/2



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECII	FICATIO	N		"U	HB" Version	
Cell Name	Function							Number of BC	
FS2	4-bit Shift Regi	ster wi	th Syncl	hronous	Load			30	
Cell Symbol				agation	Delay		ter		
			up		td		T ====		
		t0	KCL	t0	KCL	KCL2			
		2.32	0.16	3.14	0.09	0.12	4	CK → Q	
							1	1	
							1		
PA —	QA						1		
PB —	QB						1		
PC -	Qc		1						
PD —	do do		1						
								i i	
SD —		1 1					1		
ск ——									
L —		Parameter					Symbol Symbol	Typ(ns)*	
		Clock Pulse Width					tCW	4.0	
		SD Setup Time					tSSD	2.8	
		SD Hold Time					tHSD	1.2	
		DD NOTE TIME					CHOD	1.2	
		Load Setup Time					tSL	4.3	
		Load Hold Time					tHL	0.5	
		P Setup Time					tSP	3.6	
		P Hold	Time			tHP	1.5		
D. 13	Input Loading	-			<i>-</i>		. 01 17 -1-		
Pin Name CK	Factor (lu)	Clock Pause	16	C ≦ 1 < C ≤ 3			tCWL*		
SD	1	Time		< C ≦ 3 < C ≦ 4			tCWL*		
L	1	TIME	1 22	· U = 4	U	L	50#II	1 11.0	
P	i	* Min	imum va	lues fo	r the t	voical	opera	ting con-	
	_							ase operating	
	Output Driving	con	dition a						
Pin Name	Factor (lu)	mul	tiplier		-				
Q	16	]							
			value						
		connected to the output terminals, QA, QB, QC and							
		QD.							
1	1	I							

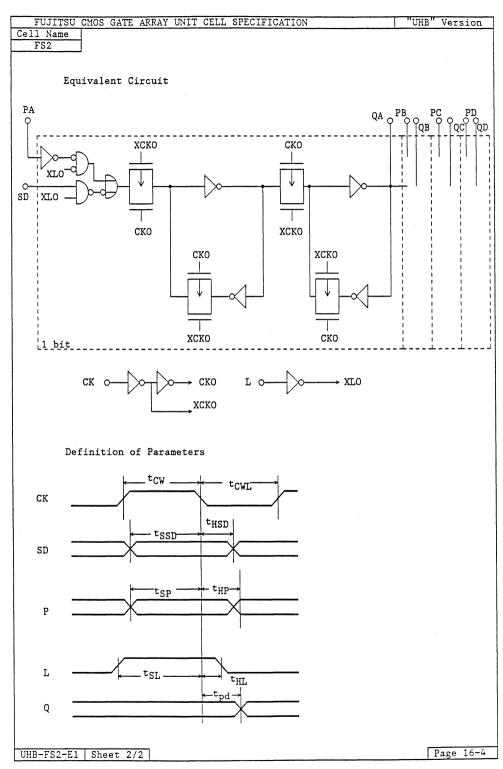
Г	Inp	uts		Outputs					
SD	L	P	CK	QA	QB	QC	QD		
SD	L	Х	<b>↓</b>	SD	QAn	QBn	QCn		
х	н	P	<b>+</b>	PA	PB	PC	PD		

Note:  $\cdot$ SD = H or L

·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

 $\cdot P$  represents PA, PB, PC and PD.

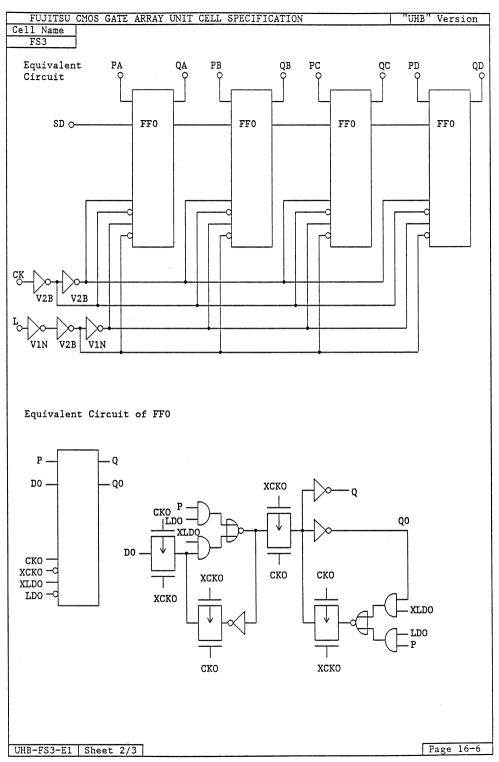
UHB-FS2-E1 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		"U	HB" Version
Cell Name	Function							Number of BC
FS3	4-bit Shift Regi	ster wi						34
Cell Symbol				agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
1		2.28	0.17	2.12	0.11			CK → Q
		4.64	0.17		0.11			$L \rightarrow Q$
		2.03	0.17	3.02	0.11			P → Q
PA — PB — PC — PD — SD — CK — C	Clock	ter Pulse W Pause T	ime			ymbol tCW tCWH	Typ(ns)* 4.0 4.0 6.2	
		Load F	uise wi	<u>utn</u>			CLW	0.2
		SD Set	up Time				tSSD	1.0
			d Time				tHSD	1.7
	Input Loading	P Setup Time					tSP	0.3
Pin Name	Factor (lu)	P Hold	Time				tHP	2.3
CK SD L P	2 2 1 2							
Pin Name Q	Output Driving Factor (Lu)							
ų,	10	The	values		worst	case op	erati	ing condition. ng condition lier.

	Inp	Output		
L	P	SD	CK	Q
L L H H	L H X X	X X L H	X X †	L H L H

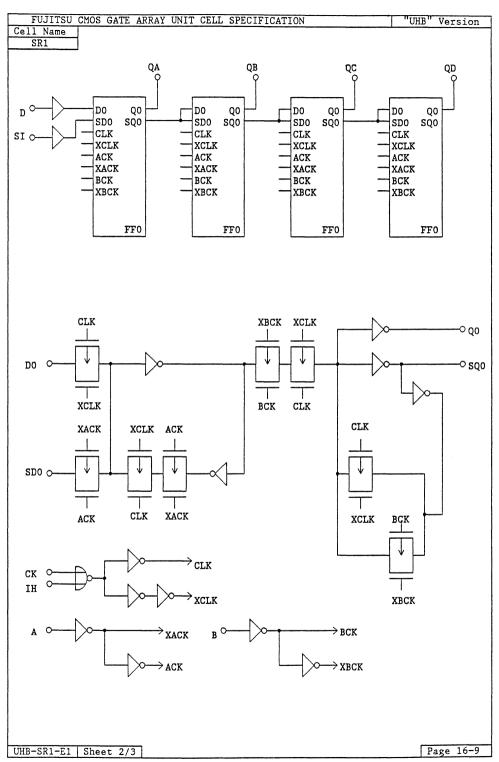
UHB-FS3-E1 | Sheet 1/3



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name FS3 Definition of Parameters CK SD \_t<sub>LW</sub> -L Page 16-7

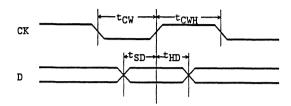
UHB-FS3-E1 | Sheet 3/3

FUJITSU C	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version
Cell Name	Function							Number of BC
SR1	4-bit Serial-in	<u>Parall</u> e	1-out S	hift Re	gister '	with S	CAN	36
Cell Symbol			Prop	agation	Delay	Parame	ter	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.27	0.09	3.37	0.07			CK → Q
		2.58	0.09	2.90	0.07	0.11		$B \rightarrow Q$
								,
		1				,	1	
						ł		
l r							1	
D —	— QA					l		İ
arr _	— QB							
CK -	— QC						1	
IH —	— QD							
si —								
Α —								
в ф								
-							1	
		Parame	ter				Symbol	Typ(ns)*
		Clock	Pulse W	idth			tCW	5.5
		Clock	Pause T	Ime			tCWH	5.6
		Data S	etup Ti	me			tSD	3.3
		Data H	old Tim	e			tHD	1.5
		1						
	Input Loading	i				1		
Pin Name	Factor (lu)					1		
D D	1	1				1		
cĸ	1					1		
IH	1							
ľ	1							
SI	1							
A,B	1	4				l		
1	Output Driving							
Pin Name	Factor (lu)	1						
Q	36							
		١	_	_				
		* Mini	.mum val	ues for	the ty	pical	operati	ing condition.
		The	values	for the	worst	case o	peratir	ng condition
		are	given b	y the m	aximum	delay	multip.	lier.
	_							
UHB-SR1-E1	Sheet 1/3							Page 16-8



"UHB" Version

Definitions of Parameters

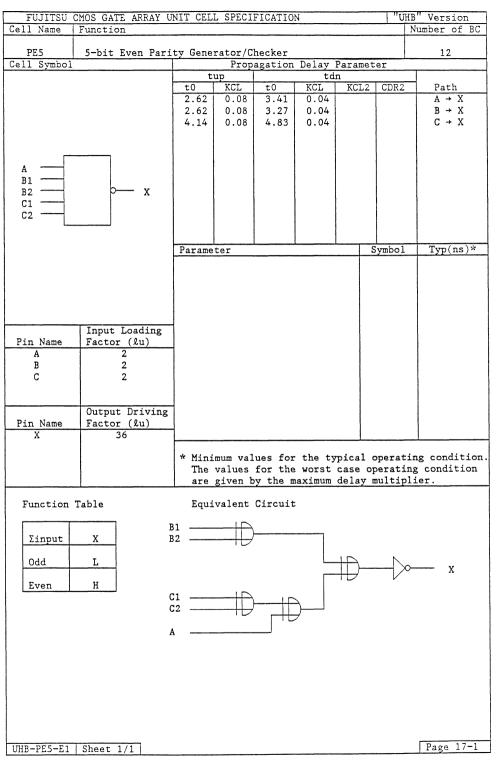


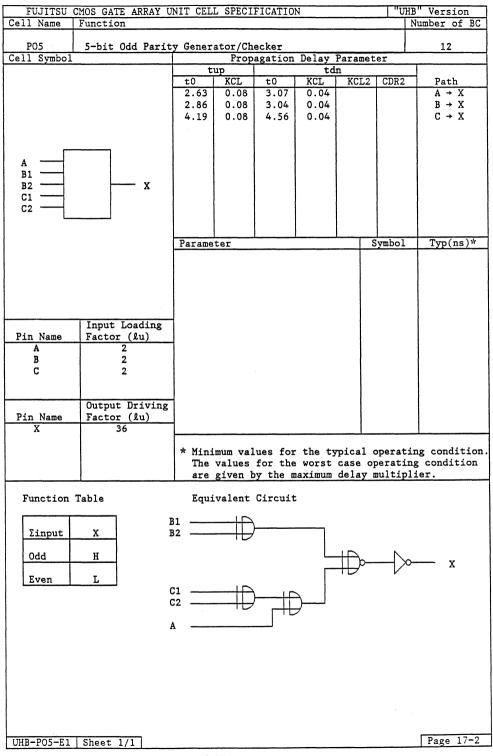
2

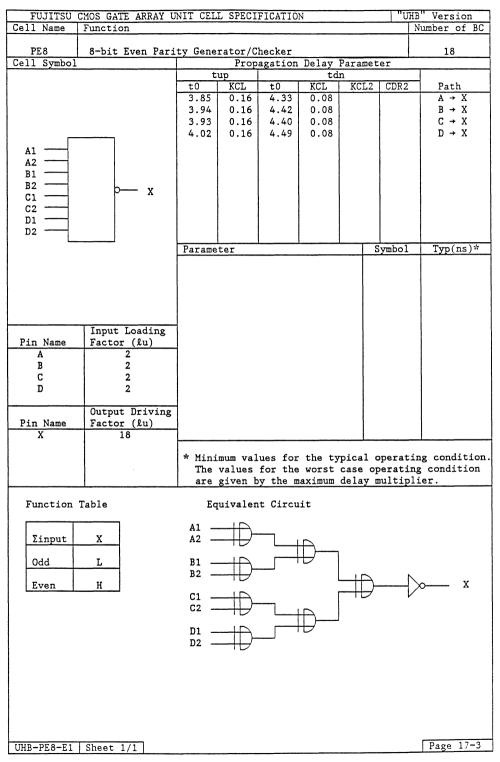
UHB-SR1-E1 | Sheet 3/3

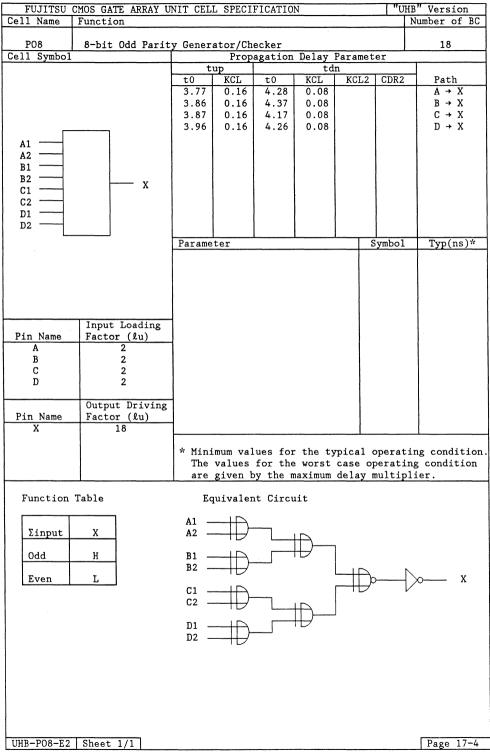
# Parity Generator/Selector/Decoder Family

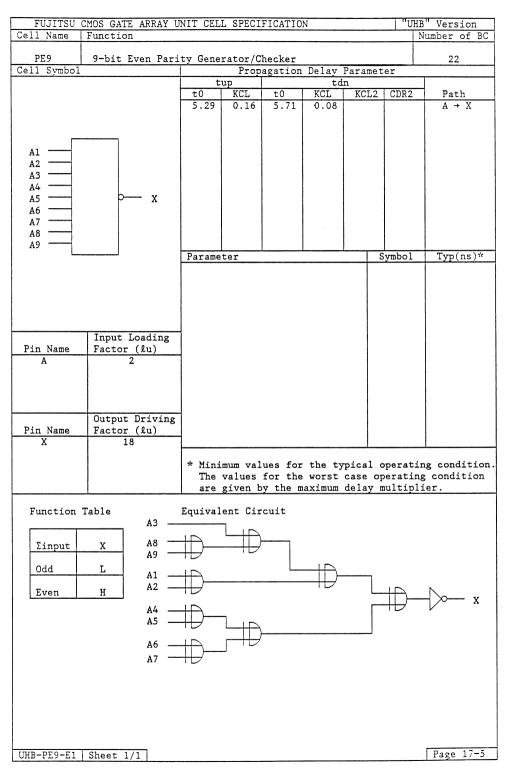
Page	Unit Cell Name	Function	Basic Cells
Parity Ge	nerators/Ch	eckers	
2–257	PE5	Even Parity Generator/Checker	12
2-258	PO5	Odd Parity Generator/Checker	12
2-259	PE8	Even Parity Generator/Checker	18
2-260	PO8	Odd Parity Generator/Checker	18
2-261	PE9	Even Parity Generator/Checker	22
2-262	PO9	Odd Parity Generator/Checker	22
Data Sele	ector		
2-263	P24	2:1 Data Selector	12
Decoder	8		
2-264	DE2	2:4 Decoder	5
2-265	DE3	3:8 Decoder	15
2-267	DE4	2:4 Decoder	8
2-268	DE6	3:8 Decoder	30
Selector	8		
2-270	T2B	2:1 Selector	2
2-272	T2C	2:1 Selector	4
2-273	T2D	2:1 Selector	2
2-274	T2E	2:1 Selector	5
2-275	T2F	2:1 Selector	8
2-277	T5A	4:1 Selector	4
2-279	V3A	1:2 Selector	2
2-280	V3B	1:2 Selector	4
Magnitud	de Compara	tor	
2-281	MC4	Magnitude Comparator	42

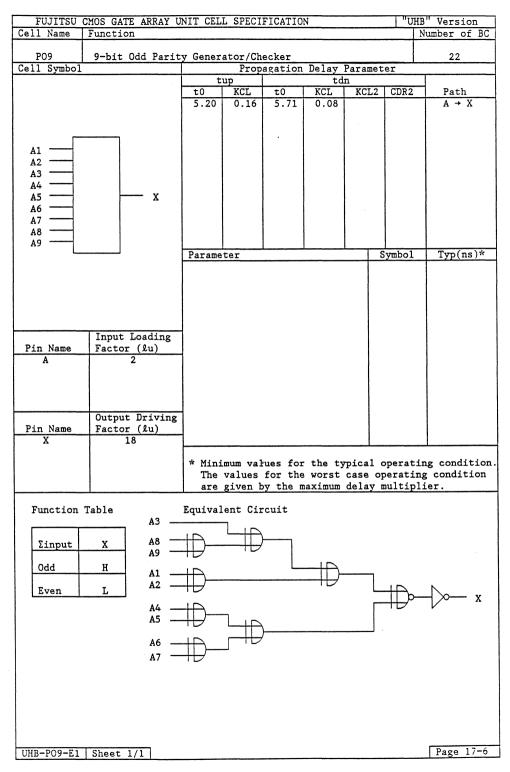


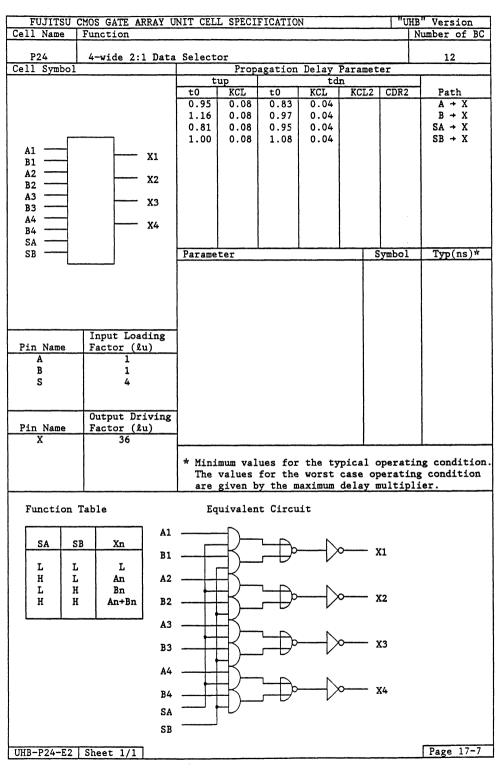


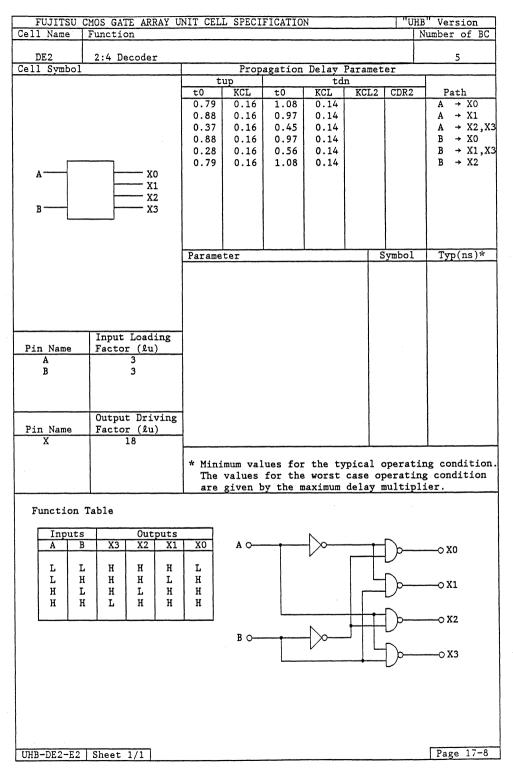












Number of BC   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symb	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Symbol												
Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup		3:8 Decoder							15			
To   KCL   to   KCL   CDR2   Path	Cell Symbol				agation			er				
1.44								1 4556	┥ 。			
2.44							KCL2	CDR2				
1.33												
Name												
A — X0 — X1 — X2 — X3 — X4 — X5 — X6 — X7 — X7 — X7 — X7 — X7 — X8 — X6 — X7 — X7 — X8 — X6 — X7 — X7 — X8 — X6 — X7 — X8 — X6 — X7 — X8 — X8 — X8 — X8 — X8 — X8 — X8									1 1			
X1		xo										
B — X3 X4 — X5 — X6 — X7  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  A 1	A					0.19			C → X4~X7			
Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A 1 B 1 C 1  Output Driving Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition.												
C — X4 — X5 — X6 — X7  Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  A 1 B 1 C 1  Output Driving Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition	В —							1				
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Pin Name Factor (lu)  A 1 B 1 C 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition.												
Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (lu)  A 1 B 1 C 1  Output Driving Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition.												
Parameter Symbol Typ(ns)*    Parameter   Symbol Typ(ns)*												
Pin Name   Input Loading Factor (lu)   A		Δ/										
Pin Name   Input Loading Factor (lu)   A			Parameter   Symbol					Typ(ns)*				
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition	1											
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition												
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition.												
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition			ļ				Į.					
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition			į				ł					
Pin Name Factor (lu)  A 1 B 1 C 1  Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition		Input Loading					ļ		1			
A 1 B 1 C 1  Output Driving Factor (2u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition	Pin Name											
C 1  Pin Name Factor (Lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition			1				-					
Pin Name Factor (£u)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition		1					l					
Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition	C	1	}				1					
Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition							l					
Pin Name Factor (lu)  X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition		1	}									
X 14  * Minimum values for the typical operating condition. The values for the worst case operating condition	Dia Man	Output Driving										
* Minimum values for the typical operating condition. The values for the worst case operating condition		ractor (xu)	1				1					
The values for the worst case operating condition	^	14	<b></b>									
The values for the worst case operating condition		perat	ing condition.									
are given by the maximum delay multiplier.												
			are	given b	y the m	aximum	delay n	nultip	olier.			

Г	Ir	puts	3				Outp	uts			
	A	В	С	X0	X1	X2	Х3	X4	X5	Х6	X7
	L L L H H	L H H L L H	L H L H L H	L H H H H H	H L H H H H	H H L H H H	H H H L H H	H H H H L H	H H H H H L H	H H H H H H H	H H H H H H

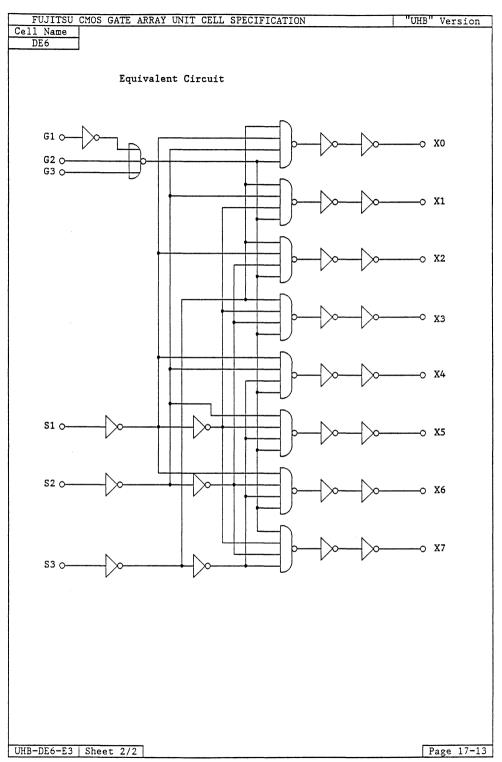
UHB-DE3-E2 | Sheet 1/2

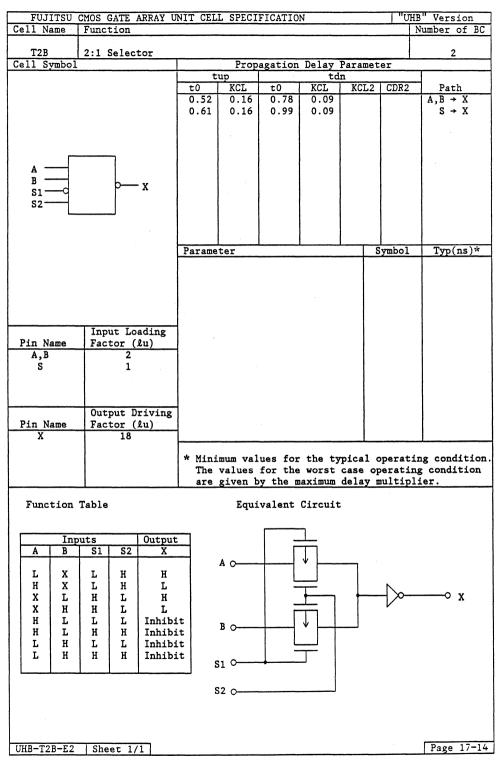
Page 17-9

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name DE3 Equivalent Circuit --> X0 -0 X1 -0 X2 -o X3 -O X4 -⊙ X5 -Q X6 -0 X7 UHB-DE3-E2 | Sheet 2/2 Page 17-10

			MOS GA	ATE AI	RRAY U	NIT (	CELL S	SPECI	FICATI	ON			HB" Version
Cell	Nam	e	Funct:	ion									Number of BC
DE	4		2.4 1	Decod	er wit	h Eps	ahla						8
Cell		bol	۷.4 )	DECOU	or MTP	1112	1016	Prop	agatio	n Delay	Paramet	er	<u> </u>
							tup			td	n		
						t0		KCL	t0	KCL	KCL2	CDR2	Path
						1.1		0.16 0.16	1.46				$G \to X$ $A \to X$
						0.8		0.16	1.11				$B \rightarrow X$
						1.0	"   '	0.10	1.17	0.17			
										}			
										1			
A			b		X0								
В			5		X1 X2								
G		-d	5		X3								
		L											1
							- 1						
						D			l	<u> </u>	ــــــــــــــــــــــــــــــــــــــ	ymbol	Tran()*
						rara	amete:	Ι			-   S	ушро1	Typ(ns)*
											1		
<u> </u>			Innu	t Loa	ding								
Pin	Nam	ne .		or (l							l		
A	7			3							1		
	В 3												
G	;			1									
											1		
<b></b>			Outp	ut Dr	iving						1		
Pin		ne		or (l									
X				14									
1						* M	inim	m 1121	nes fo	r the to	mical o	nerst:	ing condition.
						T	he va	m vai lues	for th	e worst	case on	erati	ng condition
						a	re gi	ven b	y the	maximum	delay m	ultip	lier.
Fun	ıcti	on I	able							Equivale	ent Circ	uit	
-	-1							7		N			
G	;	Α	В	хз	X2	X1	X0		G —	$-\!\!\!\!-\!\!\!\!\!/\!\!\!\!>$		$\neg$	l
							_	7		Ň		H	) <u></u>
H	I I	X	X	H	H	Н	H	1	Α —	$\rightarrow$		++	b x0 │
1	.	L	L	н	н	Н	L						/
I	.	L	Н	H	H	L	H					1	\
I		H	L	Н	L	H	H						b X1
I	i	H	Н	L	H	H	H				+	$+\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!\!$	)
				<u> </u>								1	<u> </u>
													b X2
									В	-	111	4	Γ <del>'''</del>
										V			
												4	\ v <sub>2</sub>
													<b>р</b> —— хз
													/
UHB-D	DE4-	-E2	Sheet	1/1									Page 17-11

	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version														
Cell Name	e Fund	tion												Nı	ımber of BC
DE6		B Deco	der wi	th	Enabl										30 -
Cell Sym	bol			+			ropa	gatio	on D	elay		met	er		
				-	t0	up KC:		t0	Т	KCL		L2	CDR2	-	Path
					3.05	0.	16	5.9	5	0.08					G → X
				İ	2.89	0.	16	3.28	8	0.08				ı	$S \rightarrow X$
	Γ	_					İ								
G1			- X0						1						
G2 —			- X1 - X2												
s1 —		-	- X3												
S2	-		- X4 - X5												
S3	_	-	- X6		·									-	
			- X7				İ								
		_		P	arame	ter					1	S	ymbo1		Typ(ns)*
												T			
				ĺ											
	l In	nut Lo	ading	4											
Pin Nam		tor (		╛								ļ			
G S		1 1										Ì			
8		1													
	011	tout D	riving	+											
Pin Nam		ctor (		`											
Х		18		L											
				*	Mini	mum	valu	es f	or t	he ty	pica	al o	perat	in;	g condition.
					The	valu	es f	or t	he w	orst	case	e op	erati	ing	condition
				L_	are	give	n by	the	max	imum	dela	ay m	ultip	oli	er.
Functi	on Tabl	е													
		·			T								7		
G1	G2+G3	S3	S2 :	31	X7	X6	X5	X4	хз	X2	X1	ΧO			
				_									7		
X	H X	X		K K	H	H H	H H	H H	H H	H H	H H	H H			
H	L	L	L :		H	H	H	H	H			L			
HH	L L	L		H L	H	H H	H H	H H	H H	H L	L H	H H			
н	L	L	H :	H	H	H	H	H	L	H	H	H			
H	L L	H		L H	H	H H	H L	L H	H H	H H	H H	H H			
H	L	Н		L.	H	L	Н	H	H	Н	Н	H			
н	L	Н		H	L	H	H	Н	H	H	H	H			
					1										
UHB-DE6-	E3   She	et 1/2	2												Page 17-12





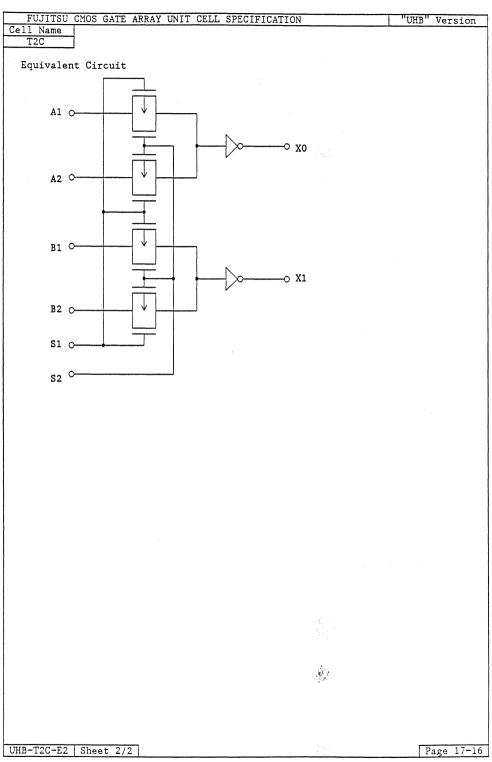
FILITEII (	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		1111	HB" Version
Cell Name	Function	022		1011110	•			Number of BC
T2C	Dual 2:1 Selecto	r						4
Cell Symbol				agation	Delay		er	,.
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.51	0.16	0.77	0.09			$A,B \rightarrow X$ $S \rightarrow X$
61	S2	0.67	0.16	1.03	0.09			5 + X
21	52						ŧ	
لم ا								
A1	b x₀							
A2	Au							1
B1								
B2	⊳— x1							
"-								
		Parame	ter		L	2	ymbol	Typ(ns)*
						l		
						- 1		
						1		
						-		}
		į				1		
	Input Loading					1		
Pin Name	Factor (lu)	1						
A,B	2							
S	2							
						- 1		
	Output Driving	1						
Pin Name	Factor (lu)							
X X	18	1						
^	10							_1
		* Mini	mum val	ues for	the tw	mical o	nerat	ing condition
	1							ng condition
	ł		given b					
	<del></del>		<u> </u>				F	

### Function Table

	Inp	uts			Outputs	
	A1,B1	A2,B2	S1	S2	X0	X1
Г						
	L	Х	L	H	H	H
1	H	X	L	H	L	L
1	X	L	н	L	H	H
1	X	H	н	L	L	L
1	L	H	L	L	Inhibit	Inhibit
ŀ	H	L	L	L	Inhibit	Inhibit
1	L	H	н	H	Inhibit	Inhibit
İ	H	L	н	Н	Inhibit	Inhibit
L						

UHB-T2C-E2 | Sheet 1/2

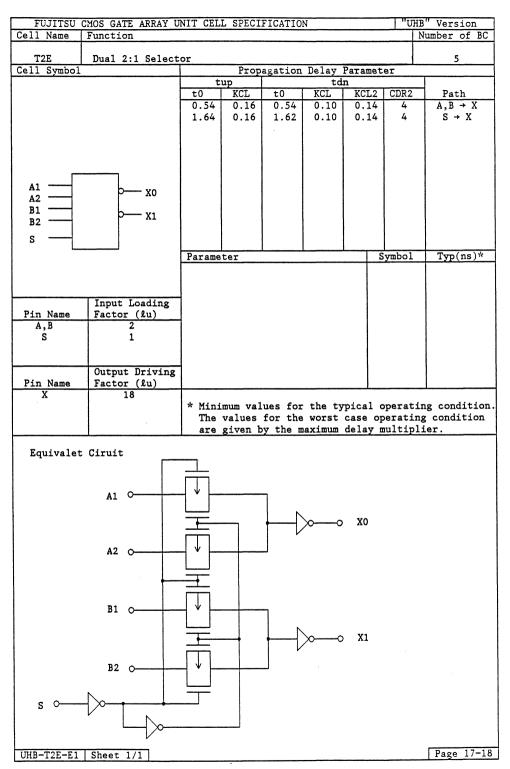
Page 17-15



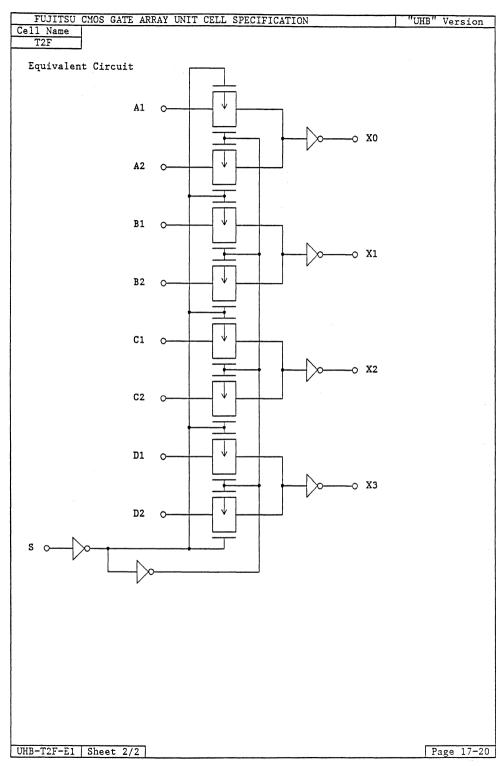
Page 17-17

FUJ:	ITSU C	CMOS (	GATE .	ARRAY U	NIT CEL	L SPECI	FICATIO	N			UHB" Version
Cell Na		Func									Number of BC
T2D	- 1	2.1	Selec	tor							2
Cell Sy	ymbol	4.1	Jerec	101		Prop	agation	Delay	Param	eter	
					t	up		td	n		
					t0	KCL	t0	KCL	KCI	.2 CDR	
					0.62	0.18 0.18	0.70 0.51	0.12			$ \begin{array}{c} A,B \to X \\ S \to X \end{array} $
			_								
А — В —				v							
S1 - S2 -				X							
			_								
					Parame	ter				Symbo	l Typ(ns)*
		Inn	ut Lo	ading							
Pin N	ame		tor (								
A,B S			1 1								
٥			1						1		
		Out	put D	riving					1		
Pin N	ame		tor (								
Х		İ	14								
					The	values	for the	worst	case	operat	ting condition
					are	given i	y the n	naximum	ueray	mult1	hiter.
Func	tion ?	Table				Equi	valent	Circuit	:		
	Inp	uts		Output	$\neg$					<u></u>	
A	В	S1	S2	X			N			П	
_		_				A 0	$\dashv \gg$		┤ ,	<b>/</b>	
L H	X X	L L	H H	H L			V	1	L		
X	L L	H	L	H						<u> </u>	~~~~x
x	н	H	L	L					_		
L	H H	L	L	Inhibi	t	В 0-	-		·	<b>↓</b>	
L H	L	H L	H	Inhibi Inhibi			V				
H	Ĺ	H	Н	Inhibi	t	. ~				厂	
						1 0-					
					S	2 0—					

UHB-T2D-E2 | Sheet 1/1



THE TAX PORT OF	WOO S. 1872 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L. 1772 L.	VITTE OFF	CDECT				l lles	
	MOS GATE ARRAY U Function	NIT CEL	L SPECI.	FICATIO	N		101	HB" Version Number of BC
COLL MAME	7 0000 0 1011							
T2F	2:1 Selector							8
Cell Symbol				agation		Paramet	er	
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
		0.54	0.16	0.54	0.10	0.14	4	A,B,
								$C,D \rightarrow X$
		1.64	0.16	1.62	0.10	0.14	4	S → X
-								
A1 —								
A2	P x0							
B1 -	р—— x1							
B2 C1								
C2 —	P X2							
D1 -	р—— x3							
D2 -	, A3							
s		Parame	ter		L	ا ا	ymbol	Typ(ns)*
<u> </u>		rarame	rer		<del></del>		ушрот	Typ(IIs)
						İ		
	Input Loading							
Pin Name	Factor (lu)							
A,B,C,D	2							
S	1							
		l						
	Output Driving	l						ĺ
Pin Name X	Factor (lu)							1
Δ.	10							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	L	are	given b	y the m	aximum	delay m	ultip	lier.
UHB-T2F-E1	Sheet 1/2							Page 17-19



FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<u>"</u> U	HB" Version
Cell Name	Function							Number of BC
T5A	4:1 Selector							5
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.00	0.23	1.00	0.16			$A,B \rightarrow X$
S1	S2 S3 S4	1.00	0.23	0.84	0.16			S1~4 → X
1	1 1 1	0.56	0.23	0.54	0.16			S5~6 → X
1								
l 1, 1	101							
A1								
B1	р—— х							
B2	Γ ^			:				
""								
م ا								
85	, S6							
		Parame	ter			S	ymbol	Typ(ns)*
		1				1		
								İ
		1						
	Input Loading					- 1		
Pin Name	Factor (lu)	1				i		
A,B S	1 1	1				1		
5	1	1				- 1		
						l		
						1		
<b></b>	Output Driving	†				j		ļ
Pin Name	Factor (lu)							
X	9	1				1		
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.

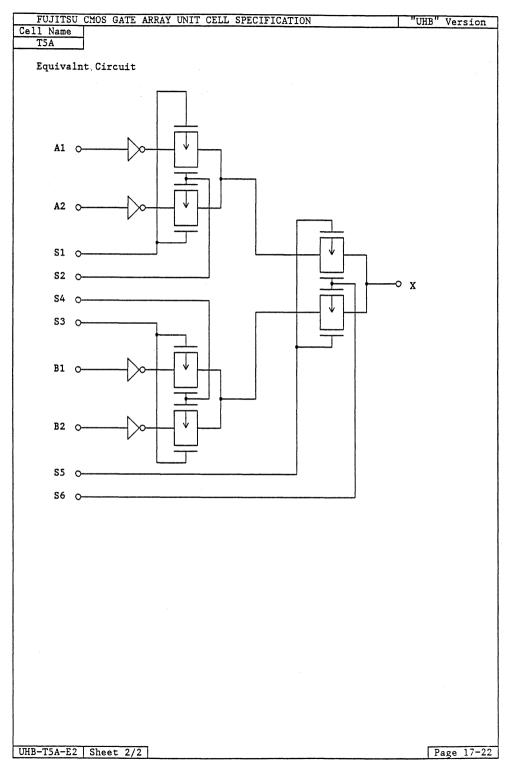
#### Function Table

				Inp	uts					Output
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X
L H	L H	L H	L H	L H H	H H L	L L H H	H H L L	L L L H H	H H H L L L	H L H L H L

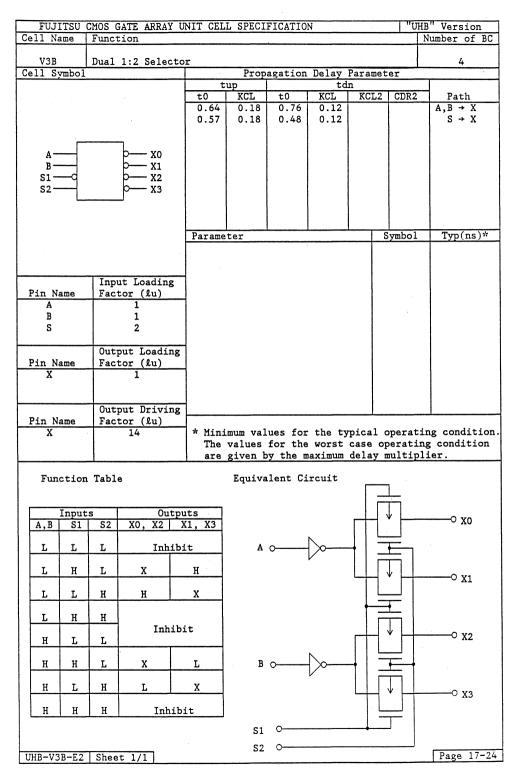
 $A1 = A2 \rightarrow S1 = S2$  or S5=S6 Inhibit  $B1 = B2 \rightarrow S3 = S4$  or S5=S6 Inhibit A1,A2 = B1,B2 or S5=S6 Inhibit

UHB-T5A-E2 | Sheet 1/2

Page 17-21



FUJITSU	J CMOS	GATE ARI	RAY U	NIT CEL	L SPECI	FICATIO	N		T "U	HB" Version
Cell Name	Fun	ction								Number of BC
V3A		Selector								2
Cell Symbo		Selecto		Ι	Prop	agation	Delay	Parame	ter	
				t	ир		td	n		
				t0	KCL	t0	KCL	KCL2	CDR2	
				0.62	0.18 0.18	0.70	0.12		1	$\begin{array}{c} A \rightarrow X \\ S \rightarrow X \end{array}$
				0.55	0.10	0.43	0.12	}		
								1	-	
A		x	,					ĺ		
_		^	,						1	
s1 — 9									1	
S2		p x	L						1	
									1	
										}
							L	L	ل	
				Parame	ter				Symbol	Typ(ns)*
	In	put Load	ing	1						
Pin Name	Fa	ctor (lu	)	4						
A S		1 1								
D/- V		tput Loa								
Pin Name X	ra	ctor (lu 1	)	1						
		_								
	-	4 t . D . /		4						
Pin Name	Fa	tput Dri ctor (lu	ving	ļ						
X		14								ing condition.
										ng condition
				are	given b	y the m	aximum	delay	multip	ller.
Function	on Tab	le			Equiva	lent Ci	rcuit			
Inpi	uts	Output	s				1_			
A S			X1			lг	T			
7 7	,	Tobaba	.			$\Box$	<b>V</b>	○X0		
LLL	L	Inhibi	-		<b>N</b>	_	<del>_</del> _			
L H	L	x	H	A 0-	$-\!\!\!\!/\!\!\!\!>$	<del> </del>				l
,   ,	17	"	.		,	7	$\neg \neg$ $\mid$			
LLL	H	H	X			4	<b>V</b>	-0 X1		
L H	Н	_				L				
,,   -		Inhibi	t		1 0					
H L	L L	+	$\dashv$	2	· <u>·</u>					
н н	L	x	L	S	2 0					
	1									
H L	H	L	X							
н н	н	Inhibi	t_							
UHB-V3A-E	1   She	et 1/1								Page 17-23



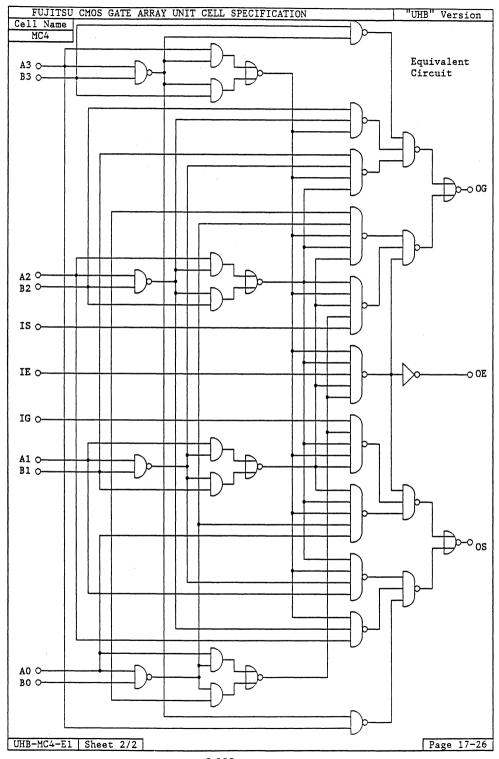
L LOSTION CHOS GA	TE ARRAY UNIT C	ELL SPECI	FICATIO	N		<b>"</b> UI	HB" Version
Cell Name   Function	on						Number of BC
	Magnitude Comp	arator					42
Cell Symbol			agation	Delay		er	
		tup		td			
	t0	KCL	t0	KCL	KCL2	CDR2	Path
}	5.2	1	6.32	0.08	0.11	4	A → OS
	5.3		6.21	0.08	0.11	4	B → OS
	2.3		2.78	0.08	0.11	4	IE → OS
A3 B3	1.9		2.41	0.08	0.11	4	IG → OS
A2 B2	5.1		6.53	0.08	0.11	4	A → OG B → OG
A1 B1	5.2		6.42	0.08	0.11	4	IE → OG
AO BO	2.2		2.99	0.08	0.11	4	IS → OG
	5.6		4.36	0.08	0.11	4	A → OE
IG -	— 0G   5 5				0.12	4	B + OE
IE	OE   2 1		1.43	0.09	0.12	4	IE → OE
IS—	— os   2.1	7   0.10	1.73	0.05	0.12	-	11 / 01
			İ				
	Para	neter			S	ymbol	Typ(ns)*
					1		
	Loading						
Pin Name Factor							
A	3						
B	3				1		
IE IG	1				1		
IS	1						
15	1						
Outpu	t Driving				1		
	r (lu)						
	18						1
1	10						
		nimum val	ues for	the ty	pical o	perat	ing condition.
							ng condition
		e given b					

#### Function Table

	Comparin	g Inputs		Casca	ding In	puts		Outputs	
				IG	IS	IE	OG	OS	OE
A3,B3	A2,B2	A1,B1	AO,BO	(A>B)	(A <b)< td=""><td>(A=B)</td><td>(A&gt;B)</td><td>(A<b)< td=""><td>(A=B)</td></b)<></td></b)<>	(A=B)	(A>B)	(A <b)< td=""><td>(A=B)</td></b)<>	(A=B)
A3>B3	X	X	Х	X	X	X	H	L	L
A3 <b3< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b3<>	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2 <b2< td=""><td>X</td><td>x</td><td>Х</td><td>X</td><td>X</td><td>L</td><td>Н</td><td>L</td></b2<>	X	x	Х	X	X	L	Н	L
A3=B3	A2=B2	A1>B1	Х	X	X	X	н	L	L
A3=B3	A2=B2	A1 <b1< td=""><td>х</td><td>Х</td><td>X</td><td>Х</td><td>L</td><td>Н</td><td>L</td></b1<>	х	Х	X	Х	L	Н	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	н	L	L
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>Х</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b0<>	Х	X	X	L	H	L
A3=B3	A2=B2	A1=B1	AO=BO	X	X	Н	L	L	н
A3=B3	A2=B2	A1=B1	AO=BO	н	L	L	н	L	L
A3=B3	A2=B2	A1=B1	AO=BO	L	Н	L	L	Н	L
A3=B3	A2=B2	A1=B1	AO=BO	н	H	L	L	L	L
A3=B3	A2=B2	A1=B1	AO=BO	L	L	L	Н	Н	L
								1	

UHB-MC4-E1 | Sheet 1/2

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## **Bus Driver**

Page	Unit Cell Name	Function	Basic Cells
2-285	B41	4-hit Rus Driver	Q

	MOS GATE ARRAY U	NIT CEL.	L SPECI	FICATIO	N		"U.	HB" Version
Cell Name	Function							Number of BC
B41	4-bit Bus Drive	r						9
Cell Symbol		<del></del>	Prop	<del></del>				
			up	+0	td		anna	
		t0 1.58	KCL 0.07	t0 1.52	KCL 0.06	KCL2	CDR2	Path A → X
		2.50	0.07	1.90	0.06			$C \rightarrow X$
		2.30	0.07	1.90	0.00			C 7 A
A0	xo							
A1 —	x1							
A2	X2							
A3	хз							
								j
c —q								
1								
								}
		Parame	ter			S	ymbol	Typ(ns)*
	•							
						1		
						- 1		
						1		
Dia Nama	Input Loading							
Pin Name	Factor (lu)					- 1		
A C	1 1					1		
C	1					1		
	Output Loading							
Pin Name	Factor (lu)					1		
X	1							
	_							
	Output Driving							
Pin Name	Factor (lu)					İ		
X	36							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.

## Maximum Number of B41 used in each UHB device

Device Name	Max. B41				
С-330UНВ	4				
C-530UHB	5				
C-830UHB	6				
C-1200UHB	8				
C-1700UHB	12				
C-2200UHB	16				

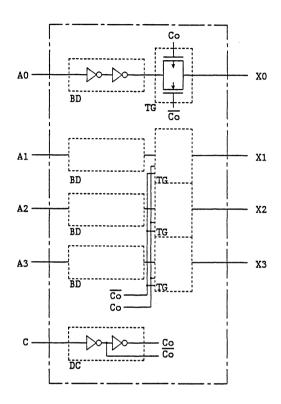
Device Name	Max. B41
С-3000UНВ	21
C-4100UHB	26
C-6000UHB	50
C-8700UHB	70
C-12000UHB	90

UHB-B41-E3 | Sheet 1/2

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B41

Equivalent Circuit



#### Note:

- $\cdot$  TG is configured using the special transmission gates buried in the channel area of the UHB devices.
- $\cdot$  BD and DC use the regular internal baisc cells in the UHB devices.
- · A Bus Terminator is invisible to logic designers and is automatically connected to each Bus line, when B41 is used.

UHB-B41-E3 | Sheet 2/2

Page 18-2

# Clip Cells

Page	Unit Cell Name	Name Function Z00 0 Clip	Basic Cells
2-289	Z00	0 Clip	0
2-290	Z01	1 Clip	0
2-291	KD2	Load Gate (Fan-in = 2)	1

FUJITSU CMOS GATE ARRAY	INIT (	TELL SPEC	TETCATI	ON		יווויי	B" Version
Cell Name Function	ONII	JEED BIEG	IFICALL	OIV		1 1	Number of BC
Z00 0 Clip Cell Symbol		Dro	nacatio	n Delay	Damamat		0
Cell Symbol		tup	pagatio	td		er	T
	t0	KCL	t0	KCL	KCL2	CDR2	Path
		1			1		
				1		ĺ	1
						1	
X			ļ			1	1
			1			İ	
<b>l</b>							1
		1	ļ				
					<u> </u>		
	Para	ameter			T 8	ymbol	Typ(ns)*
							1
Input Loading					•		
Pin Name Factor (Lu)							
	}						
	l				- 1		
	ļ						
	_						
Pin Name Factor (lu)	8						
X 200	-						
				_			
	* M:	inimum va ho valuos	lues fo	r the ty	rpical o	operati Deratin	ng condition. g condition
	a	re given	by the	maximum	delay r	multipl	ier.
UHB-Z00-E1   Sheet 1/1							Page 19-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version	
Cell Name	Function		Number of						
Z01	1 Clip		Propagation Delay Parameter						
Cell Symbol			Prop	agation	Delay td		er	<del></del>	
		t t	—  <sub>թո+ե</sub>						
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
	\ /						1		
	Υ								
							1		
		'							
	X						l		
	= <del>=</del>						1		
		Parame	ter	·	·	S	ymbol	Typ(ns)*	
								1	
	Input Loading	1				-			
Pin Name	Factor (lu)								
		l				- 1			
						- 1			
						1			
	Output Driving	ł				1			
Pin Name	Factor (82)					-			
X	Factor (lu)	ł							
^*	200			<del></del>					
		* Mini	mum val	ues for	the tv	mical o	perat	ing condition.	
		The	values	for the	worst	case or	erati	ng condition	
		are	given b	y the m	naximum	delay t	multip	lier.	
1									
1									
1									
	t								
]									
1									
UHB-Z01-E1	Sheet 1/1							Page 19-2	

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHE	" Version
Cell Name	Function						N	lumber of BC
KD2	Load Gate Fan-i	n = 2						1
Cell Symbol				agation	Delay	Paramet	er	
		t	up		td		T	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
							ŀ	
							İ	1
							l	
A	Λ							
A	$\vee$							
							İ	
			,					
		Parame	ter			<u>s</u>	ymbol	Typ(ns)*
n	Input Loading	1						
Pin Name A	Factor (lu)	-						
, A	2	İ						
		Ì						
Din Nama	Output Driving Factor (lu)					ļ		
Pin Name	Factor (ku)	1						
								<del></del>
		* Mini	.mum val	ues for	the ty	pical c	perati	ng condition.
]	]	The	values	for the	worst	case or	perating	g condition
	1	are	given b	y the m	aximum	delay m	nultipl:	ier.
UHB-KD2-E1	Sheet 1/1							Page 19-3

## I/O Buffer Family

Done	Unit Cell Name	Eurobian	Basic Cells
Page		Function	Cells
Input Buff 2-295 2-296 2-297 2-298 2-299 2-300 2-301 2-302 2-303 2-304 2-305 2-306 2-307 2-310 2-311 2-312 2-313 2-314 2-315 2-316 2-317 2-318 2-318 2-319 2-320 2-321 2-322 2-323	118	Input Buffer I1B with Pull-up Resistance I1B with Pull-down Resistance Input Buffer I2B with Pull-up Resistance I2B with Pull-down Resistance I2B with Pull-down Resistance I2B with Pull-down Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I1C with Pull-up Resistance I1C with Pull-up Resistance I2C with Pull-up Resistance I2C with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance I3B with Pull-up Resistance	5554444446665555444488888866668888
Output Bu			_
2-325 2-326 2-327 2-328 2-329 2-331 2-331 2-332 2-334 2-335 2-336 2-337 2-338 2-340 2-341 2-342 2-343 2-344	01B 01L 01R 01S 02B 02L 02S 02S2 04R 04S2 04T 04W 01BF 02BF 02RF 04RF 04TF	Output Buffer Power Output Buffer Output Buffer Power Output Buffer Output Buffer Power Output Buffer Output Buffer Output Buffer Power Output Buffer High Power Output Buffer Output Buffer Power 3-state Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer 3-state Output Buffer 3-state Output Buffer Output Buffer S-state Output Buffer	33552244655744352454
		fers (Buses)	8
2-345 2-346 2-347	H6T H6TU H6TD	3-state Output and Input Buffer H6T with Pull-up Resistance H6T with Pull-down Resistance	8 8

2-348 2-349 2-350 2-351 2-352 2-353 Output Bu	H6W H6WU H6WD H6C H7CU H6CD	Power 3-state Output and Input Buffer H6W with Pull-up Resistance H6W with Pull-down Resistance 3-state Output and CMOS Interface Input Buffer H6C with Pull-up Resistance H6C with Pull-down Resistance	8 8 8 8 8
2-354 2-355 2-356 2-357 2-358 2-359 2-360 2-361 2-362 2-363 2-364 2-365 2-368 2-371 2-372 2-373 2-376 2-377 2-378 2-379 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380 2-380	HEGES JD LEGENT LOW SAN TO THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE HEGES STORE THE THE HEGES STORE THE THE HEGES STORE THE THE THE THE THE THE THE THE THE TH	Power 3-state Output and CMOS Interface Input Buffer H6E with Pull-up Resistance H6E with Pull-up Resistance 3-state Output and Schmitt Trigger Input Buffer H6S with Pull-up Resistance H6S with Pull-up Resistance H6S with Pull-up Resistance H6R with Pull-up Resistance H6R with Pull-up Resistance H6R with Pull-up Resistance H6R with Pull-up Resistance H8T with Pull-up Resistance H8T with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W2 with Pull-up Resistance H8W2 with Pull-up Resistance H8C with Pull-up Resistance H8C with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E2 with Pull-up Resistance H8E2 with Pull-up Resistance H8E2 with Pull-up Resistance H8E3 with Pull-up Resistance H8E4 with Pull-up Resistance H8E5 with Pull-up Resistance H8E6 with Pull-up Resistance H8E7 with Pull-up Resistance H8E8 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance	8 8 12 12 12 12 12 12 19 9 9 9 9 9 9 9 9 9
Oscillator 2-399 2-400 2-401 2-402	IT10 HOC HOS HOCR	Input Buffer for Oscillator Output Buffer for Oscillator and Input Buffer Output Buffer for Oscillator and Schmitt Trigger Input Buffer Output Buffer for Oscillator	0 8 8

FULITSU C	MOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		l "UH	B" Version
	Function	NII OLL	B DI LOII	TOATTO				Number of BC
			`					
I1B Cell Symbol	Input Buffer (I:	nverter	Prop	agation	Delay	Paramet	er	5
		tı	up	-8	td	n		
		t0	KCL	t0 1.54	KCL	KCL2	CDR2	Path X → IN
		1.60	0.04	1.54	0.04			$X \to IN$
	1							
1	<b>.</b>							
х —	>O— IN							
		Parame	ter		L	l I s	ymbol	Typ(ns)*
		ame					,	-5,5(20)
Pin Name	Input Loading Factor (lu)							
1111 Name	ractor (zu)					-		
						1		
	Output Driving	1						
Pin Name IN	Factor (lu)							
IN	30							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values given b	for the	worst	delaw m	eratin m1+in1	ng condition
	L	ale	given b	y the a	IAXIMUM	deray n	dicipi	161.
i								
								<u></u>
UHB-I1B-E1	Sheet 1/1							Page 20-1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บา	HB" Version
	Function		Nu					
	Input Buffer (I:	nverter)						
I1BU	with Pull-up Res	istance						5
Cell Symbol			Prop	agation	Delay		er	
			up		td		ars:	
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.60	0.04	1.54	0.04			X → IN
		1					]	
								1
							1	
х —	>>— и						1	
	<u>"</u> "							
		Parame	ter			S	ymbol	Typ(ns)*
•								
						1		
	Input Loading							
Pin Name	Factor (lu)							
LIII Mame	ractor (xu)					-		
	Output Driving							
Pin Name	Factor (lu)					1		
IN	36							
			_	_				
		* Mini	mum val	ues for	the ty	rpical o	perat	ing condition.
		The	values	ror the	worst	case of	erati	ng condition
		are	given b	y the m	aximum	петау г	nuitip	iler.
1								
1								
UHB-I1BU-E1	Sheet 1/1							Page 20-2

FILITTOIL	CMOS GATE ARRAY U	NITT CET	SPECT	ETCATTO	NI .		1177	IB" Version
	Function	NII CEL.	L SPECI.	FICATIO	IN .		1 01	Number of BC
	Input Buffer (I	nverter	)			<del></del>		
I1BD	with Pull-down R	esistan	ce					5
Cell Symbol				agation			er	
			up	+0	td		CDDO	J 7
		t0 1.60	KCL 0.04	t0 1.54	KCL 0.04	KCL2	CDR2	Path X → IN
		1.60	0.04	1.54	0.04			A 7 IN
	_							1
х —	>>— IN							
		Parame	ter	L	L	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	ymbol	Typ(ns)*
		raramo					<u> </u>	=7.5(==7
	<del></del>							
<b>.</b> .,	Input Loading							
Pin Name	Factor (lu)					[		
								;
	Output Driving							
Pin Name	Factor (lu)					1		
IN	36							
		* Mini	mum val	ues for	the ty	rpical c	perat	ing condition.
		The	values	for the	worst	case of	erati	ng condition
		are	given b	y the m	aximum	delay i	uitip	lier.
]								
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UHB-I1BD-E1	Sheet 1/1							Page 20-3
OUB-IIRD-FI	I   Sheet 1/1							11450 20 3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								B" Version		
	Function		Number of BC							
I2B										
Cell Symbol		Propagation Delay Parameter								
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		1.06	0.04	1.84	0.04		1	Path X → IN		
х —	IN			·						
^ _	114						1	1		
							l			
1										
	*	Parameter					Symbol Typ(r			
1										
						l				
	Input Loading									
Pin Name	Factor (lu)					l				
						l				
						1				
l						1				
	Output Driving	i								
Pin Name	Factor (lu)	ĺ								
IN	36									
	1	* Mini	mum val	ues for	the ty	pical	operati	ng condition.		
		The	g condition							
	<u> </u>	are	given b	y the n	aximum	delay	multipl	ier.		
TTT Fanis	lent Circuit									
IIL Equiva.	lent Circuit									
	, ,									
1	<del></del>									
1	3 1									
74504	74804					b.				
74LS04	74LS04									
UHB-I2B-E1	Sheet 1/1							Page 20-4		

FUJITSU C	"U	JHB" Version								
Cell Name   Function   Input Buffer (True)								Number of BC		
I2BU	with Pull-up Res	ietanco	4							
Cell Symbol	with full up kes	Istance								
Cell Symbol Propagation Delay Parameter tup tdn										
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		1.06	0.04	1.84	0.04			Path X → IN		
!										
								1		
								1		
x —	IN							1		
" L										
		Parame	ter			S	ymbol	Typ(ns)*		
						1				
						1				
						l				
	Input Loading	1								
Pin Name	Factor (lu)									
İ	į	1								
<b></b>	Output Driving									
Pin Name	Factor (lu)							i		
IN	36	1								
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.		
		The values for the worst case operating condition								
	l	are given by the maximum delay multiplier.								
1										
1										
UHB-I2BU-E1	Sheet 1/1							Page 20-5		
OHD-12BU-EI	I DITECT 1/1							15		

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								"UHB" Version		
	Function	01111.	- 0.101		Number of BC					
COII Hame		rue)			Number OI					
I2BD	with Pull-down R		C B				1	4		
Cell Symbol	#ICH LUII-GOWN K	COTOLAII	Pron	agation	Delay	Parame+	or	7		
Cell Symbol				agation	Delay td	raramet	-eT			
		t0	up KCL	t0	KCL	n KCL2	CDR2	Dath		
			VCT	1.84		NUL2	CDKZ	Path X → IN		
		1.06	0.04	1.84	0.04			X → IN		
							1			
							1			
1										
х —	>— IN									
ا							1			
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		Parame	ter		L	, ,	ymbol	Typ(ns)*		
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						-				
	<del></del>									
	Input Loading									
Pin Name	Factor (lu)					- 1				
						1				
						i		1		
						l				
	Output Driving					1				
Pin Name	Factor (lu)					1		1		
IN	36	1								
		* Mini	mum val	ues for	the ty	pical o	operatin	ng condition.		
		The	values	for the	worst	case of	perating	condition		
		are	given h	v the m	aximum	delav	nultipli	er.		
			<u> </u>	, u						
1										
UHB-I2BD-E1	Sheet 1/1							Page 20-6		

FIITTEII C	MOS GATE ARRAY U	NIT CELL C	DECTETCATIO	NT.		"UHB" Ver			
		Number of BC							
TVD	me   Function   Clock Input Buffer (Inverter)								
IKB Cell Symbol	Clock input Buff		4						
Joseph Symbol		tup	Propagation	td	n				
			CL tO	KCL	KCL2 CI	DR2 Pa	th → CI		
		2.37 0	.02 1.82	0.02		X .	→ C1		
			İ						
x	CT.								
^	>> c1								
		Parameter		I	Symi	ool Typ	(ns)*		
							İ		
	Input Loading								
Pin Name	Factor (lu)								
	Output Driving								
Pin Name	Factor (lu)								
CI	150								
		* Minimum	values for	the ty	pical ope	rating con	dition.		
		* Minimum values for the typical operation.  The values for the worst case operation are given by the maximum delay multip							
	L	are giv	en by the m	naximum	delay mul	tiplier.			
TTL Equival	ent Circuit								
[									
	<b>)</b> :								
	þ <del>. :</del>								
	<i>)</i> :								
1									
74 "1"	S40								
"1"									
					,				
UHB-IKB-E2	Sheet 1/1					Page	20-7		
CILD TKD DZ	Direct 1/1					1 1 450			

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version
Cell Name	Function Clock Input Buff	0= /T-			· · · · · · · · · · · · · · · · · · ·			Number of BC
IKBU	with Pull-up Res	er (IN istance	verter)					4
Cell Symbol			Prop	agation	Delay	Paramet	er	<del>-</del>
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.37	0.02	1.82	0.02			X → CI
١.								
x —	>> cī		'					
- L			:					
						*		
		Parame	ter			l s	ymbol	Typ(ns)*
							,	7 F ()
						1		
	Input Loading							
Pin Name	Factor (lu)							
	Output Driving							
Pin Name	Factor (lu)		*					
CI	150	<b></b>						
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
TTT. Fandres	lent Circuit							
IID EQUIVA	reur Olicale							
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+ -	ノ:							
74	4840							
"1"								
UHB-IKBU-E2	Ch + 1/1							Page 20-8
UNB-IKBU-E2	Sheet 1/1							rage 20-0

TIL TIMOL		VIII CET	CDECT		.,		1 11	
Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		1	HB" Version
Cell Name	Function Clock Input Buff	er (In	verter					Number of BC
IKBD	with Pull-down R							4
Cell Symbol		001000	Prop	agation	Delav	Paramet	er	,
		t	up		td	n		T
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.37	0.02	1.82	0.02			X → CI
į.								
x	>> cī							
1								
1		Parama	+			1 6	ymbol	Typ(ns)*
		Parame	rer				y m DO I	Typ(IIs)"
j								
						1		
	Input Loading							
Pin Name	Factor (lu)							
FIII Name	ractor (xu)					-		
						- 1		
1						- 1		
]								
						ĺ		
	Output Driving							
Pin Name CI	Factor (lu)					- 1		
C1	150							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
	1	The	values	for the	worst	case op	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
TTL Equiva	lent Circuit							
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	n :							
1 -	b							
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"1"	4S40							
"1"								
1								
		`	•					
						•		
UHB-IKBD-E2	Sheet 1/1							Page 20-9
<u> </u>	<del></del>							

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	" Version
	Function						l l	Number of BC
		, <u> </u>						_
ILB	Clock Input Buff	er (Tr	ue)		D-1	D *		6
Cell Symbol		+-	up Prop	agation	Delay td		er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.03	0.02	2.56	0.02	RODZ	ODICE	X → CI
			1112		*****			" "
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								1
x —	cı							
^	tı							
		Parame	ter			S	ymbol	Typ(ns)*
						1		
	Input Loading					į		
Pin Name	Factor (lu)							
						1		
	Output Driving					l		
Pin Name	Factor (lu)							
CI	150							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl:	ier.
UHB-ILB-E2	Sheet 1/1							Page 20-10
PT_GTT	DITEC T							1 5

FULITSU C	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		тин г	B" Version
Cell Name	Function			1 1011110	**			Number of BC
	Clock Input Buff	er (Tr	ue)					
	with Pull-up Res	istance	D		D-1	Damamad		6
Cell Symbol		+	up Prop	agation	Delay td	Paramet	er	r
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.03	0.02	2.56	0.02			X → CI
x —	CI							
l	/ "							
		Parame	ter	L	l	l S	ymbol	Typ(ns)*
								-55 (2027)
						1		
						l		
	Input Loading					•		
Pin Name	Factor (lu)					1		
Pin Name	Output Driving Factor (lu)					l		
CI	150							
								, , , , , , , , , , , , , , , , , , , ,
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		ine	values given h	ror tne	WOIST	case op delay m	erating ultipl	g condition
		are	given b	y the i	ISATMUM	deray m	urcipi.	
TTL Equival	ent Circuit							
I								
1		CI						
74S04 74LS04								
741504								
	<sup>1</sup> 74540							
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UHB-ILBU-E2	Sheet 1/1							Page 20-11

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version
Cell Name	Function							Number of BC
	Clock Input Buff	er (Tr	ue)					
ILBD	with Pull-down R	esistan	ce					6
Cell Symbol			Prop	agation	Delay		ter	
			up		td		T ====	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.03	0.02	2.56	0.02			X → CI
	l							
								]
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х —	' '							
							1	
							1	
		Parame	ter	L	L	<u> </u>	Symbol	Typ(ns)*
		101000					- , 01	-75(110)
						1		
	Input Loading					1		1
Pin Name	Factor (lu)							
	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\					1		1
						1		]
						İ		1
						l		1
						1		
	Output Driving					1		•
Pin Name	Factor (lu)					1		
CI	150							
		* Mini	mum val	ues for	the ty	pical (	operat	ing condition.
		The	values	for the	worst	case of	perati	ng condition
		are	given b	y the m	aximum	delay	multip	lier.
l								
UHB-ILBD-E2	Sheet 1/1							Page 20-12
	, 4/4							

FILTITOU C	MOS CATE APPAY I	NITT CEI	T CDECT	ETCATTO	NT.		1 1177	HB" Version
	MOS GATE ARRAY U	NII CEL	L SPECI	FICALLO	14		1 01	Number of BC
				_	_			
I1C	CMOS Interface I	nput Bu	ffer (	Inverte	r)	D		5
Cell Symbol		+	Prop up	agation	Delay td		eI	
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.32	0.04	1.44	0.04			X → IN
							}	
		į i						
x —	>> IN						1	
[		1						
		Parame	ter		L	l s	ymbol	Typ(ns)*
						l		
						1		
		]				1		
	Input Loading	1						
Pin Name	Factor (lu)	4						
	}					1		
	Output Driving	}						
Pin Name	Factor (lu)							
IN	36							
			1			_/1	<b>.</b>	
		The	mum vai	ues for	the ty	DICAL C	perat	ing condition. ng condition
		are	given b	y the m	naximum	delay n	ultip	lier.
		<del></del>						
IND IIO C1	Chast 1/1							Page 20-13
UHB-I1C-E1	Sheet 1/1							11050 20 13

	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		"U	HB" Version
Cell Name	Function CMOS Interface I	nnut Ru	ffor (	Inverte	<del>-</del> )			Number of BC
I1CU	with Pull-up Res	istance	rrer (	TUAGL CG	<b>.</b> )			5
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0 1.32	KCL 0.04	t0 1.44	KCL 0.04	KCL2	CDR2	Path X → IN
		1.54	0.04	1.44	0.04			V - TH
	_						1	
х —	>>─ IN						ĺ	
			,					
		Parame	ter			8	ymbol	. Typ(ns)*
	1 T T 3:							
Pin Name	Input Loading Factor (lu)							
1 III Name	1 20001 (84)					l		
						-		
	Output Driving	1				1		
Pin Name	Factor (lu)							
IN	36							
		* Mini	mum val	ues for	the to	mical a	perat	ting condition
		The	values	for the	worst	case of	perati	ing condition
		are	given b	y the m	naximum	delay i	nultip	olier.
UHB-I1CU-E1	Sheet 1/1							Page 20-14

DILITECT :	TWO CAME ADDAM IT	NITT CET	T CDECT	DTO ATTO	NT.		II t ti t to	11 57
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI.	r IUATIO	N		I OHB	" Version umber of BC
Cell Name	CMOS Interface I	nnut D.	ffor (	Tarra=+ -	-7		N	umber of RC
TION	UNUS INCETIACE I	ubac pa	riei (	Inverte:	ı)			_
I1CD	with Pull-down R	esistan	ce D		D-1 1	2		5
Cell Symbol			Prop	agation	Delay	raramet	er	
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		t0	KCL	t0	KCL	KCL2	CDR2	Path
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	Input Loading	1						
Pin Name	Factor (lu)	1				1		
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	Output Driving							
Pin Name	Factor (lu)	1						
IN	36							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case or	erating	condition
		are	given h	v the m	aximum	delav n	ultipli	ler.
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	Sheet 1/1							Page 20-15
UHB-I1CD-E1								

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	3" Version
	Function						1	Number of BC
I2C	CMOS Interface I	nput Bu	ffer (T	rue)				4
Cell Symbol				agation	Delay		er	T
		t0	up KCL	t0	td KCL	n KCL2	CDR2	Path
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	Input Loading							
Pin Name	Factor (lu)							
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	Output Driving	1						
Pin Name	Factor (lu)							
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		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
	1	The	values	for the	worst	case or	peratin	g condition
		are	given b	y the m	aximum	delay n	multipl	ier.
UHB-I2C-E2	Sheet 1/1							Page 20-16

PHILTERN CVCC	CAMP ADDAY ??	NITT OFT	CDECT	CTCATTO	NT		117777	17 37
FUJITSU CMOS Cell Name   Func	tion	NII CEL	L SPECI.	r IUATIO	N			Version
CEIT NAME LANG	Interface I	nnut Ru	ffer				—   <sup>1</sup>	Number of BC
	Pull-up Res						1	4
Cell Symbol	Turi up nob		Prop	agation	Delay 1	Paramet	er	
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Pin Name   Fac	tor (ku)					1		
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Out	put Driving	1						
Pin Name Fac	tor (lu)	İ						
IN	36	1						
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case op	erating	g condition
		are	given b	y the m	aximum	delay m	ultipl:	ier.
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UHB-I2CU-E2   She								Page 20-17

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	"UH	B" Version			
Cell Name	Function							Number of BC
	CMOS Interface I:	nput Bu	ffer					
I2CD	with Pull-down R	esistan	ce (Tru	e)				4
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t <sup>.</sup>	up		td			7
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04			X + IN
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	Output Driving					1		
Din Nama	Factor (An)							
Pin Name	Factor (lu)	}				1		
IN	36	ļ						
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		" Mini	.mum val	ues for	the ty	picai c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	naximum	delay n	nultip.	lier.
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UHB-I2CD-E2	Sheet 1/1							Page 20-18

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	<u>N</u>		ן "ט	HB" Version
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1S	(CMOS Type, Inve	rter)						8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
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UHB-I1S-E1	Sheet 1/1							Page 20-19
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	CMOS GATE ARRAY U	NIT CEL	"UH	B" Version						
Cell Name	Function							Number of BC		
	Schmitt Trigger	Input B	uffer							
I1SU	(CMOS Type, Inve	rter) w	ith Pull	1-up Re	sistanc	е		8		
Cell Symbol			Prop	agation	Delay	Paramet	er			
			up		td					
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		3.90	0.16	2.68	0.08			X → IN		
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UHB-I1SU-E	1   Sheet 1/1							Page 20-20		

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "UH	B" Version
	Function						Number of BC	
	Schmitt Trigger	Input B	uffer					
I1SD	(CMOS Type, Inve	rter) w	ith Pul	1-down	Resista	nce		8
Cell Symbol			Prop	agation			er	
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		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
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	Output Driving					- 1		
Pin Name	Factor (lu)	}				l		
IN	18							
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UHB-I1SD-E1	Sheet 1/1							Page 20-21

FILITTELL	CMOS GATE ARRAY U	NIT CET	I SPECT	FICATIO	M		מעוז"	" Version
Cell Name	Function	411 CCL	u orbol.	TONITO	i v		I N	umber of BC
JOIL HAME	Schmitt Trigger	Input R	uffer					amber or no
I2S	(CMOS Type, True							8
Cell Symbol	,	·	Prop	agation	Delav	Paramet	er	
		t	up	<u> </u>	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
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	Output Driving					- 1		
Pin Name	Factor (lu)	ļ				ļ		
IN	18					1		
		* Mini	mum val	ues for	the ty	pical o	peratir	ng condition.
		The	values	for the	worst	case of	perating	g condition
		are	given b	y the m	aximum	delay n	ultipli	ler.
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UHB-I2S-E1	Sheet 1/1							Page 20-22

EILITTELL C	MOC CATE ADDAY II	NITT CET	COECT	ETCATTO	NT.		מעונדויו	" Version
	MOS GATE ARRAY U	MII CEL	n offici	T TCALLO	TA			umber of BC
	Schmitt Trigger	Input B	uffer				· ·	
I2SU	(CMOS Type, True	) with	Pull-up	Resist	ance			8
Cell Symbol			Prop	agation	Delay :	Paramet	er	
		t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
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Pin Name	Factor (lu)	]						
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	Output Driving	1				1		
Pin Name	Factor (lu)	1				1		
IN	18	1						
	1	* Mini	mum val	ues for	the ty	pical o	peratio	ng condition.
		The	values	for the	worst	case or	erating	g condition
		are	given b	y the m	naximum	delay n	nultipli	ier.
UHB-I2SU-E1	Sheet 1/1							Page 20-23
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
	Function	· · · · · · · · · · · · · · · · · · ·	ornor	1 10M110			1 1	Number of BC
- Jaza Mamo	Schmitt Trigger	Input B	uffer					
I2SD	(CMOS Type, True	) with	Pull-do	wn Resi	stance			8
Cell Symbol	, <u>-</u>		Prop	agation	Delay	Paramet	er	
		t	up		td	n.		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.48	0.16	3.08	0.10			Path X → IN
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	Input Loading							İ
Pin Name	Factor (lu)							
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Pin Name	Factor (lu)							1
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		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	nultip	lier.
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UHB-I2SD-E1	Sheet 1/1							Page 20-24

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
	Function	NIT CEL	L SPECI	FICATIO	N		J UH	Number of BC
JOIL Hame	Schmitt Trigger	Input R	uffer				<del></del>	TAUDEL OF BC
I1R	(TTL Type, Inver	ter)					1	8
Cell Symbol			Prop	agation	Delay	Paramet	er	
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Pin Name	Input Loading Factor (lu)	1						
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	Output Driving					l		
Pin Name	Factor (lu)					İ		
IN	18							
		* Mini	mum 31a1	ues for	+ho +v	mical c	noreti	ng condition.
		The	values	for the	worst	CASE OF	eratin	g condition
		are	given b	v the m	aximum	delay n	ultipl	ier.
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UHB-I1R-E2	Sheet 1/1							Page 20-25

FUJITSU (	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION							B" Version
	Function							Number of BC
1	Schmitt Trigger	Input B	uffer					
I1RU	(TTL Type, Inver	ter) wi	th Pull	-up Res	istance		- 1	8
Cell Symbol			Prop	agation	Delay	Paramet	er	
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	Output Driving					- 1		
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IN	18					i		
		* Mini	mum val	ues for	the tv	pical c	perati	ng condition.
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		are	given b	v the m	aximum	delav	ultipl	ier.
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UHB-I1RU-E2	Sheet 1/1							Page 20-26

FUJITSU (	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version							HB" Version
	Function						Ť	Number of BC
	Schmitt Trigger	Input B	uffer					
I1RD	(TTL Type, Inver	ter) wi	th Pull	-down R	esistan	ce		8
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td		anna	┩ │
		t0	KCL	t0	KCL	KCL2	CDR2	Path
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	Input Loading							
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Die Name	Output Driving					j		
Pin Name IN	Factor (lu)							
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UHB-I1RD-E2	Sheet 1/1							Page 20-27

	CMOS GATE ARRAY U	E ARRAY UNIT CELL SPECIFICATION						HB" Version	
Cell Name	Function							Number of BC	
705	Schmitt Trigger	Input B	uffer						
I2R Cell Symbol	(TTL Type, True)		Dean	+i	Dalam	Damama t		8	
Cerr PAMPOI		+-	up Prop	agation	Delay td	n aramet	ET		
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
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Din Nama	Output Driving Factor (lu)								
Pin Name IN	18								
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		The	values	for the	worst	case or	erati	ng condition	
	<u> </u>	are	given b	y the m	aximum	delay n	ultip	lier.	
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UHB-I2R-E1	Sheet 1/1							Page 20-28	
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FUJITSU C	MOS GATE ARRAY U	UNIT CELL SPECIFICATION "UHB" Ver						B" Version
	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I2RU	(TTL Type, True)	with P	ull-up	Resista	nce		-	8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.24	0.16	3.72	0.13			Path X → IN
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	Output Driving					-		
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	İ	* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	ng condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
UHB-I2RU-E1	Sheet 1/1							Page 20-29
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								B" Version		
	Function						1	Number of BC		
	Schmitt Trigger	Input B	uffer							
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Pin Name	Factor (lu)									
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Pin Name	Factor (lu)	1				.   .				
IN	18									
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UHB-I2RD-E1	Sheet 1/1							Page 20-30		

FUJITSU CMOS GATE ARRAY UNIT C	IT CELL SPECIFICATION "UHB" V						
Cell Name   Function						Number of BC	
O1B Output Buffer(IOL=3.2	mA, Inver	ter)				3	
Cell Symbol		pagation			eter	<del></del>	
	tup	ļ	td				
t0	KCL	t0	KCL	KCL	2 CDR2		
1.9		2.24	0.124	1	ł	OT → X	
(5.2	9)	(9.68)			- 1	1	
	ļ				İ		
	l	ł		Ì	ł	ļ	
	į			l	1		
	ı	1					
		ļ.					
0T	İ	1	j				
от — х	1						
	j						
	l						
	1						
Para	meter	Typ(ns)*					
<u> </u>					Symbol	- J.F ()	
				1			
				1			
Input Loading				l			
Pin Name Factor (lu)				1			
OT 2				- 1			
				- 1			
				1			
Output Driving				l		1	
Pin Name Factor (Lu)							
1							
+ W.	námum rol	luos for	+ho +	miss1		ing condition	
						ing condition	

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

		ATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function							Number of BC				
01L	Output Buffer(IO	L=12mA,						3				
Cell Symbol				agation			ter					
			up		td			<b>_</b>				
		t0	KCL	t0	KCL	KCL2	CDR2					
,		2.29	0.037	2.47	0.041			OT → X				
		(4.51)	1	(4.93)		1						
						l	1					
						l	1	· .				
						İ	l					
	<u> </u>					1	1					
-						l	-					
OT —	>>─ x				į							
		i					1					
					į	İ						
							ł					
		Parame	+ 0 =		L	<del></del>	Symbol	Typ(ns)*				
		rarame	tei				Symbol	Typ(IIS)				
		l				- 1						
						ł						
		į				1						
						1						
		l						1				
	Input Loading	1										
Pin Name	Factor (lu)	1				ı						
OT	2	1										
	_	1				1						
						- 1						
		1				1		1				
		1				- 1						
	Output Driving	1				-						
Pin Name	Factor (lu)											
	1	1										
								ing condition				
l												
		The values for the worst case operating condition are given by the maximum delay multiplier.										

Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU	CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name	Function							Number of BC				
	Output Buffer(IO	L=3.2mA	, Inver	ter)								
O1R	with Noise Limit			•				5				
Cell Symbol			Prop	agation :	Delay P	aramete:	r					
		t	up		tdn							
		t0	KCL	t0	KCL	KCL2	CDR2					
		3.30	0.056	5.18	0.13			OT → X				
		(6.66)		(12.98)								
								1				
								1				
от —	> x →											
01	^ ^											
								İ				
		Parame	ter		L	Sv	mbol	Typ(ns)*				
			***************************************					1 7				
						- 1						
						ļ						
						- 1		1				
						l						
<b>.</b>	Input Loading					1		[				
Pin Name	Factor (lu)							j				
OT	1							1				
						ŀ						
						1						
								1				
	Output Driving											
Pin Name	Factor (lu)					- 1		1				
	1											
	1											
								ng condition.				
								g condition				
	1	are	given b	y the ma	ximum d	elay mu	ltipl	ier.				
	are given by the maximum delay multiplier.											

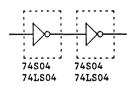
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

TUITTCII C	NOC CATE ADDAY II	NIT CEL	CDECT	TICATION				1 1111	HB" Version	
Cell Name	MOS GATE ARRAY U	NII CEL	L SPECI	FICALIUN				1 0	Number of BC	
Cell Name	Output Buffer(IO	T = 1 2m A	Invert	02)					Mamper of RC	
015	with Noise Limit			elj				- 1	. 5	
Cell Symbol	WICH NOISE BIMIT	Kesise		agation :	Delay P	aran	ete			
		t	up	-6	tdn					
		t0	KCL	t0	KCL	KC	L2	CDR	2 Path	
		4.02	0.038	6.39	0.054				OT → X	
		(6.30)		(9.63)			- 1			
							1			
							ŀ			
							ł			
ı							- 1		1	
от —	>>- x						Ì			
01	^									
							- 1			
							l			
		Parame	ter	<u> </u>			Syı	mbol	Typ(ns)*	
						1			1	
						- 1				
	Input Loading					- 1				
Pin Name	Factor (lu)					- 1				
OT	1									
0.	-									
						- 1				
						- 1				
						- 1				
	Output Driving					- 1				
Pin Name	Factor (lu)					- 1				
		<u></u> .	•							
									ing condition.	
		The values for the worst case operating condition								
	]	are given by the maximum delay multiplier.								

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "U	HB" Version
Cell Name	Function							Number of BC
02B	Output Buffer (I	OL=3.2m						2
Cell Symbol	···	ļ		agation	Delay		er	
		to	up KCL	t0	td KCL	n KCL2	CDR2	Path
		1.70	0.056	1.75		KCD2	CDKZ	OT + X
		(5.09)		(9.19)			l	
				(				
							1	
							i	
					ĺ		ļ	
	$\wedge$							
ОТ	> x							
				·			1	
		Parame	tor	l	l	٠ .	ymbol	Typ(ns)*
		Falame	tel				ymbol	1yp(ns)
		}				ł		•
						ŀ		
						į		
						- 1		
<b> </b>	Input Loading	1						
Pin Name	Factor (lu)							
OT	4	1						
		1				- 1		
		1				ł		
		l				ŀ		
	Output Driving	┨				l		
Pin Name	Factor (lu)							
		1						
					_			
								ting condition.
								ing condition
are given by the maximum delay multiplier.								

## TTL Equivalent Circuit



Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-02B-E4 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version
	Function				· · · · · · · · · · · · · · · · · · ·			Number of BC
O2L	Output Buffer(IO	L=12mA,						2
Cell Symbol				agation			er	
			up	+0	td		CDDO	┥ 。 ┃
		t0 2.09	KCL 0.037	t0 1.98	KCL 0.041	KCL2	.CDR2	Path OT → X
		(4.31)	0.037	(4.44)				01 7 %
		(4.51)		(4.44)				
								1
OT	x							
i								
								1
		Parame	ter			S	ymbol	Typ(ns)*
						İ		
						İ		
								-
	Input Loading							
Pin Name	Factor (lu)							1
OT	4							
						1		
	Output Driving							
Pin Name	Factor (lu)							
. 411 114116	1							
				***************************************				
								ing condition.
	*							ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU (	CMOS GATE ARRAY U	GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function								Number of BC			
	Output Buffer(10							T				
O2R	with Noise Limit	Resist							4			
Cell Symbol				agation :			eter					
			up		tdn							
		t0	KCL	t0	KCL	KC	L2	CDR2	Path			
		2.99	0.056	4.69	0.13		- 1		OT → X			
		(6.35)		(12.49)			ı					
							- 1					
							- 1					
							- 1					
1							J					
от —	> x											
01	^ ^											
1							- 1					
							- 1					
		Parame	ter				Sym	nbol	Typ(ns)*			
						- 1						
						- 1			ł			
						- 1						
Dia Name	Input Loading											
Pin Name OT	Factor (lu)					1						
01	2	ĺ				- 1						
						1			1			
									1			
	Output Driving					1						
Pin Name	Factor (lu)					- 1						
	1					1						
									ng condition.			
									g condition			
	1	are	given b	y the ma	ximum d	elay	mul	ltipl:	ier.			

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N				B" Version
Cell Name	Function								Number of BC
	Output Buffer(IO								_
028	with Noise Limit	Resist						i.	4
Cell Symbol			Prop	agation	Delay	Para	met	er	· ·
		t	up		td				4
		t0	KCL	t0	KCL	KC.	L2	CDR2	Path
		3.71	0.038	5.87	0.054				OT → X
		(5.99)		(9.11)					į
								1	
						ŀ		l	
								l	1
						l		l	1
						1		ŀ	İ
077						1		1	
OT -	x								1
								1	1
						İ		l	
						İ		Ì	
		Parame	tor	L	L	L	- 6	ymbol	Typ(ns)*
		larame	tei					ymbol	Typ(IIs)
									1
	Input Loading								
Pin Name	Factor (lu)								
OT	2								
									1
									1
									1
	Output Driving								
Pin Name	Factor (lu)								1
									ng condition.
									ng condition
		are	given b	y the m	aximum	dela	y m	ultipl	ier.

Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

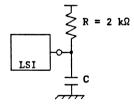
FUJITSU	CMOS GATE ARRAY U	NIT CELL	SPECIF	ICATION			"U	нв"	Version		
Cell Name	Function						٦		mber of BC		
	Output Buffer(IO	L=24mA,	True)								
0252	with Noise Limit						- 1		6		
Cell Symbol			Propa	gation De	lay Par	ameter					
		tu			tdn			Т			
ĺ		t0	KCL	t0	KCL	KCL2	CD	R2	Path		
		5.27	0.032	9.51	0.06			Т	OT → X		
		(7.19)		(13.11)				- 1			
								- 1			
1								1			
									-		
	_							ı			
								ı			
то	x						l		ì		
1								1			
					1		1				
			L		<u> </u>	L	Ļ	-			
		Paramet	er			Sym	bol	+	Typ(ns)*		
						1		ı			
								- 1			
		1				1		- 1			
						1					
Ì											
	Input Loading										
Pin Name	Factor (lu)					1					
OT	2										
"	1										
						1					
	1					1			1		
	Output Driving					1					
Pin Name	Factor (lu)							- 1			
	1							- 1			
		* Minim	um valu	es for th	e tvoic	al ope	rat	ine	g condition.		
1											
	The values for the worst case operating condition are given by the maximum delay multiplier.										
	<del></del>		are given by the maximum delay multiplier.								

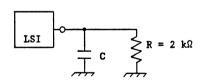
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	I		"ຫ	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output			2mA, Tru	1e)		1	
O4R	with Noise Limit	Resist					i	5
Cell Symbol				agation			r	
		t0	up		tdn			႕
			KCL	t0	KCL	KCL2	CDR	
		3.12	0.056	5.66	0.13			OT → X
		(6.76)		(14.11)	1			
				ł	1			İ
				Ì	]			İ
	$\sim$							
от	x			}	1			1
01	^ *							l
	1							
	C							
					1			į .
			$L \rightarrow 2$	<u>'                                     </u>	L	$Z \rightarrow L$		
		t0		KCL	t0		CL	$ c \rightarrow x$
		2.2	2		6.47	0.	13	
		(13.4	4)	*	(14.92	) [		
		`		1	•	´		1
			1			1		
	Input Loading					l		1
Pin Name	Factor (lu)		1	- 1		ļ		
OT	2							
С	2		H → Z			Z → H		
		t0		KCL	t0		CL	
		3.0			3.20		056	1
	Output Driving	(13.4	4)	*.	(14.92	)		
Pin Name	Factor (lu)	Į		İ		- 1		
				1				
	1							
	1	l	ļ	ļ		1		

\* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

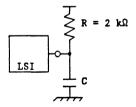
Note: 1. The unit of KCL is ns/pF.

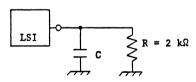
- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-04R-E3 | Sheet 1/1

FILLITSII CMOS GATE APPAY I	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name   Function	WILL OLDE D.	LOII IONIIO			Number of BC							
Tri-state Output	Buffer(IO	L=12mA, Tru	e)									
04S   with Noise Limit			-,		5							
Cell Symbol		Propagation	Delay Par	ameter								
	tup	T I	tdn									
		CL t0		KCL2 CDR								
		7.25		j	OT → X							
	(6.43)	(10.76	기	1								
			1									
1			1 1									
	1		1	ł								
от — х		1	1 1		1							
	i i	ı	1 1									
			1 1									
1	i i	1	1 1									
C			ł									
			_1									
1		+ Z		. → L								
	t0	KCL	t0	KCL	C → X							
	3.65		7.40 (10.91)	0.054	1							
	(17.83)	"	(10.91)	1	1							
	1	1			l l							
Input Loading	1			1	1							
Pin Name Factor (lu)				1								
OT 2	1			1	ł							
C 2	Н	→ Z	2	2 → H								
	t0	KCL	t0	KCL								
	3.75		3.69	0.038	7							
Output Driving	(17.83)	*	(10.91)	1	İ							
Pin Name Factor (Lu)	4				1							
	]			1	1							
1	1	1		1	1							
1	1	1	l	1	ł							

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



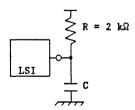


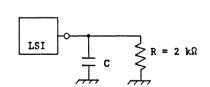
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL is ns/pF.
  - Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-04S-E3 | Sheet 1/1

FILITCII	CHOC CATE ADDAY II	NITE CEL	t cnrc	TTCLTTO	3		I minu	B" Version
Cell Name	CMOS GATE ARRAY U	NII CEL	L SPEC	IT ICATIO	<u> </u>			Number of BC
OCII Name	Tri-state Output	Buffor	( TOT = 2/	mA True	.,			Number of BC
0452	with Noise Limit			·mA, IIu	=)			7
Cell Symbol		VESTE		pagation	Dolar P	aramete	<del>-</del>	/
Cell Symbol		-	up	I	tdn	aramete	<u> </u>	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		5.61	0.032	11.62		RODE	ODKZ	OT + X
		(7.69)		(15.52)			l	01 7 %
		(7.69)		(13.32	ή Ι			
				1	1			
				ì			l	
	<u> </u>						l	
				1	1		ł	
от —	x -			i	1		l	ı
	V	į		1			l	
							l	
			1			ł	İ	
	C							
				<u> </u>				
			L → :			$Z \rightarrow L$		_
		t0		KCL	t0		CL	_ c → x
ı		5.3			11.18		06	
		(19.2	3)	*	(15.08	)		
ı								1
		1				1		
	Input Loading	1		j		1		
Pin Name	Factor (lu)					i		İ
OT	2							
С	2		H → 2	Z		Z → H		7
		t0		KCL	t0	K	CL	
		6.3	7		5.25	0.	032	7
	Output Driving	(19.2	3)	*	(15.08	)		
Pin Name	Factor (lu)				-			
		1	- 1					
		1				1		1
		1						1
	1		- 1			1		1

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



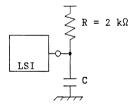


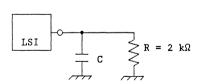
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\text{CL}}$  is ns/pF.
  - Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-04S2-E3 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name	Function						T	Number of BC			
04T	Tri-state Output	Buffer	(IOL=3.	2mA, Tr	ue)			4			
Cell Symbol					Delay P	aramete	r				
			ир		tdn						
		t0	KCL	t0	KCL	KCL2	CDR				
		2.42 (6.06)	0.056	2.52				OT → X			
		(0.00)		(10.57	1						
	$\setminus$			İ							
от —	x			1							
	С										
1				<u> </u>		ليسيا					
		t0	L → 2	KCL	t0	$Z \rightarrow L$	CL	$ C \rightarrow X$			
		2.0	7	KCL	2.55		13	- 0 / 1			
		(12.3	1	*	(11.00						
	Input Loading										
Pin Name	Factor (lu)					-					
ТО	4										
С	2	+6	H → Z		+ 2	$Z \rightarrow H$	OT.	_			
		t0 3.4	1 +-	KCL	t0 2.31		CL 056	-			
	Output Driving	(12.3		*	(11.00)		050				
Pin Name	Factor (lu)	`			, , ,						

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:

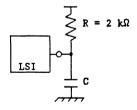


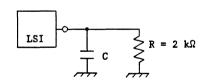


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-04T-E5 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N N	— т	"UHB	" Version
Cell Name	Function							lumber of BC
04W	Tri-state Output	Buffer						4
Cell Symbol				pagation	Delay Par	rameter		
			ıp	ļ,	tdn			
		t0	KCL	t0		KCL2 CI	R2	Path
		3.02	0.038	4.12	0.047	İ		OT → X
		(5.49)		(7.17)		- 1		
					1	- 1		
						- 1		1
ı					ŀ	- 1		
от —	>— x				į į	- 1		
	· "					. 1		
•								
	l			Į į		i		
	C					1		
								}
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0	KCI		] c → x
		2.9	_		3.69	0.04	+7	
		(16.3	5)	*	(6.75)			
	Input Loading		j					
Pin Name	Factor (lu)							
OT	4							
Č	2		H → 2	Z		$Z \rightarrow H$		1
-	_	t0	<u> </u>	KCL	t0	KCI		1
		4.0	3		2.72	0.03	38	1
	Output Driving	(16.3	5)	*	(6.75)			
Pin Name	Factor (lu)							
	i		.					
	<b>1</b>							L





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-04W-E3 | Sheet 1/1

71177mari a							1 11:-	W
	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		U	HB" Version
Cell Name	Function							Number of BC
		<b></b>	_					
O1BF	Output Buffer (I	OL=8mA,	Invert	er)				3
Cell Symbol				agation			ter	<del></del>
			up		td		Lanna	┥
		t0	KCL	t0	KCL	KCL2	CDR2	Path OT → X
		1.96	0.056	2.01	0.063		1	01 - X
		(5.32)		(5.79)				
							1	
							1	1
1							1	
от —	>─ x						1	1
01							ļ	
•								
							1	
							1	
		Parame	ter				Symbol	Typ(ns)*
		1				1		
		ŀ				- 1		
						1		1
	Input Loading							
Pin Name	Factor (lu)					ł		
OT	2							
						- 1		
						- 1		I
	Output Driving	{				- 1		İ
Din Nama	Factor (lu)					- 1		
Pin Name	ractor (Lu)							
		<del></del>						
		* Mini	mum vel	ues for	the to	nical -	operat	ing condition.
								ng condition
	(			y the m				
	<del></del>							

Note: 1. The unit of  $K_{\text{CL}}$  is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

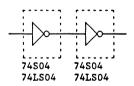
FUJITSU CMOS	GATE ARRAY U	NIT CEL	L SPECI	FICATION			"UH	B" Version	
	ction			·				Number of BC	
Out	put Buffer (I	OL=8mA,	Invert	er)					
	h Noise Limit	Resist						5	
Cell Symbol				agation :			r		
			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2		
		3.39	0.056	5.60	0.063		1	OT + X	
		(6.75)		(9.38)	·		1	İ	
							1		
							l		
							1		
							1		
$\sim$									
от —	>>— x ∣						l		
							1		
							l		
							ł	1	
		لــــــا					ــِـــــ		
		Parame	ter			-   53	mbo1	Typ(ns)*	
						i			
						- 1			
In	put Loading								
	ctor (lu)								
OT	1					- 1			
						1			
<b>\</b>						1			
	Amora Dodonia					1			
	tput Driving ctor (lu)					1			
Pin Name Fa	ctor (ku)					1		1	
		* Mini	mum vel	ues for	the two	ical or	erati	ng condition.	
		The values for the worst case operating condition are given by the maximum delay multiplier.							

Note: 1. The unit of  $K_{CL}$  is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version
Cell Name	Function	on						
O2BF	Output Buffer (I	OL=8mA	True)					2
Cell Symbol	000000000000000000000000000000000000000	<u> </u>	Prop	agation	Delay	Paramet	er	_
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	
ł		1.76	0.056	1.52	0.063			OT → X
		(5.12)		(5.30)			ĺ	
							l	
							l	
1 .	_						}	j
ОТ —	x							
01	, x							
1								
							<u> </u>	
		Parame	ter			<u>s</u>	ymbol	Typ(ns)*
						1		
		1				1		İ
		1						1
Dim Name	Input Loading							
Pin Name OT	Factor (lu)	1				1		1
"	<b>T</b>	1						
1								
1		1						
		1						
Pin Name	Output Driving							
rin Name	Factor (lu)	ł						
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.

TTL Equivalent Circuit



Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

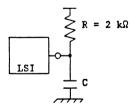
UHB-02BF-E1 | Sheet 1/1

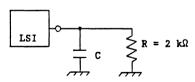
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			<u>"U</u>	HB" Version
Cell Name	Function							Number of BC
	Output Buffer (I						į	_
O2RF	with Noise Limit	Resist						4
Cell Symbol				agation			r	
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		3.08	0.056	5.11	0.063			OT + X
		(6.44)		(8.89)			1	
							1	
							1	
							1	
							1	
,							1	
	\						1	
OT -	x						ł	
							1	
							ı	
						1		
		لـــــــا	Ļ		<u> </u>	L	۲.,	
		Parame	ter			87	mbol	Typ(ns)*
						ł		
						Ì		
						1		1
						ŀ		į
	T 7					ł		
	Input Loading					- 1		
Pin Name	Factor (lu)					ı		
OT	2							İ
						ŀ		1
						- 1		1
						ı		ŀ
	l					- 1		
	Output Driving							
Pin Name	Factor (lu)	l				1		
		ļ						
		رے رہریا	1		AL. A			
								ing condition.
								ng condition
	<u> </u>	are	given b	y the ma	XIDUM C	eray m	uitip	iler.

Note: 1. The unit of  $K_{CL}$  is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU (	CMOS GATE ARRAY U	NIT CELL S	SPECT	FICATION	v ·		T "U	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output	Buffer (	OL=8	mA, True	e)			
O4RF	with Noise Limit	Resistan	ce					5
Cell Symbol			Prop	agation			r	
		tup		ļ	tdn			
			KCL	t0	KCL	KCL2	CDR	
			.056	5.96				OT → X
		(6.85)		(10.51)	)			1
1				1				
								•
	$\sim$			İ				ì
от —	>— x			1				
1	, "			ł	1			
İ				1	1			
	1	1		1	1			
	C	l i						
Į.								
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	c → x
		2.62	ì	.	6.82		070	ł
		(15.89)		*	(11.37	)		
]								1
	T 7 37							
Pin Name	Input Loading Factor (lu)		1					
OT OT	Pactor (£u)							1
C	2		H → 2	,		$Z \rightarrow H$		
"	-	t0		KCL	t0		CL	
	1	3.30	+	NOD .	3.21		056	-
	Output Driving	(15.89)	1	*	(11.37)			
Pin Name	Factor (lu)	(20.00)	1		(==:=,)			ı
	†	1						I
1			1					1
1		1						

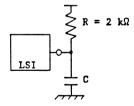


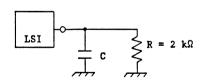


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.
  - Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-04RF-E1 | Sheet 1/1

	MOS GATE ARRAY U	NIT CELL	SPECI	FICATION	N		"UHE	" Version
	Function						IN	umber of BC
04TF	Tri-state Output	Buffer						4
Cell Symbol				agation	Delay Pa	ramete	r	
		tu			tdn		,	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.51 (6.15)	0.056	3.27 (7.37)				OT → X
от —	x							
ĺ			,					
	C				1 1			
	· ·				1 1			
			$L \rightarrow Z$			$Z \rightarrow L$	<b></b>	
		t0		KCL	t0		CL	C → X
		2.29 (14.80		*	3.35 (7.45)		063	
		(14.60	'		(7.43)	'		
						-		
	Input Loading					-		
Pin Name	Factor (lu)					-		1
OT C	4 2		H → Z			$Z \rightarrow H$		1
U		t0		KCL	t0		CL	1
		3.12			2.37		056	1
	Output Driving	(14.80	)	*	(7.45)			1
Pin Name	Factor (lu)				, ,	- 1		1
l			- 1			- 1		
						-		
	1	i	1			1		ı





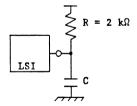
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

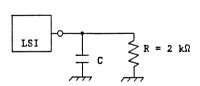
Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-04TF-E1 Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHE	" Version
Cell Name	Function							Number of BC
н6Т	Tri-state Output	(IOL=3.	2mA) &	Input B	uffer (T	rue)		8
Cell Symbol					Delay P		r	
			up		tdn			1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84				X → IN
		2.42	0.056	2.52			ļ	OT → X
	1	(7.18)		(13.57	기			
IN	<b>-</b> < h							1
1	\ \ \ \			ł				
от —	<b>x</b>			1				
01	^							ł
'				1	1			
				1				
	С						1	
				1				
			$L \rightarrow 2$			$Z \rightarrow L$	*	
		t0		KCL	t0		CL	] c → x
		2.0			2.55		13	
		(15.3	5)	*	(13.60	)		İ
			- 1					
	17 7					1		
Din Name	Input Loading Factor (lu)					j		
Pin Name OT	Factor (ku)		- 1			1		
C	2		H → 2	,		Z → H		┧
•	-	t0	<del>-                                    </del>	KCL	t0		CL	1
		3.4	1		2.31		056	1
	Output Driving	(15.3		*	(13.60		_	
Pin Name	Factor (lu)				,			
IN	36		ı					į
		1	- 1					
			ŀ					
	l l	l	- 1			I		1



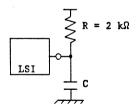


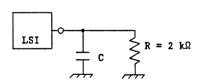
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6T-E4 | Sheet 1/1

UHB" Version FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION Cell Name Function Number of BC Tri-state Output(IOL=3.2mA) & Input Buffer (True) H6TU with Pull-up Resistance 8 Cell Symbol Propagation Delay Parameter KCL KCL KCL2 | CDR2 t0 t0 Path 1.84 0.04 1.06 0.04 X → IN 2.42 0.056 2.52 0.13 OT + X (7.18)(13.57)X L → Z  $Z \rightarrow L$ t0 KCL t0 C → X 2.07 2.55 0.13 (15.35)(13.60)Input Loading Pin Name Factor (lu) OT  $H \rightarrow Z$  $Z \rightarrow H$ С 2 t0 KCL t0 KCL 3.41 2.31 0.056 Output Driving (15.35)(13.60)Pin Name Factor (lu) IN

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:





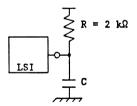
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

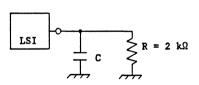
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6TU-E4 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function .							Number of BC
	Tri-state Output	(IOL=3.	2mA) &	Input B	uffer (T	rue)		
H6TD	with Pull-down R	esistan	ce	•				8
Cell Symbol			Prop	agation	Delay P	aramete	r	-,
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X + IN
		2.42	0.056	2.52	0.13		l	OT → X
		(7.18)		(13.57	)		1	
ın							l	
IN	$\sim$						l	
							l	
от ——	→ x				1		l	
	M						1	1
					1			
	l			1			1	1
	С			1	1		Į .	1
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	_ c → x
		2.0			2.55		13	
		(15.3	5)	*	(13.60	)		į
						1		į.
						- 1		l
	Input Loading	l	İ			ı		į
Pin Name	Factor (lu)							
OT	4							j
С	2		H → 2			$Z \rightarrow H$		
		t0		KCL	t0	K	CL	
		3.4			2.31		056	
	Output Driving	(15.3	5)	*	(13.60	)		ļ
Pin Name	Factor (lu)	l	- 1			j		ŀ
IN	36					1		
			Ī					ł
		l						
	1	l	- 1			ı		

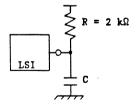


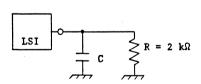


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H	6TD-E4	Sheet	1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version
Cell Name	Function							Number of BC
H6W	Tri-state Output	(IOL=12	mA) & I	nput Bu	ffer (T	rue)		8
Cell Symbol				agation			er	
			up		td		anna	
		t0 1.06	KCL 0.04	t0	KCL 0.04	KCL2	CDR2	Path X → IN
		3.02	0.04	4.12	0.047		1	$0T \rightarrow X$
		(6.25)	0.036	(8.12)			1	01 7 1
		(0.23)		(0.12)				1
IN —								
				İ			1	
OT	√ x						1	
	M							
								1
				1			1	İ
	C							l
			L + 2			$Z \rightarrow I$	L	<del> </del>
		t0		KCL	t0		KCL	$d c \rightarrow x$
		2.9		NOD	3.6		.047	⊢
		(20.2		*	(7.6			
		,	1		`			
	Input Loading		ļ					ļ
Pin Name	Factor (lu)		İ	1		ı		İ
OT	4							_
С	2		H → 2			Z → H		_
		t0 4.0	2	KCL	2.7		KCL .038	4
•	Output Driving	(20.2	- 1	*	(7.6	- 1 -	.036	
Pin Name	Factor (lu)	(20.2	"	**	(7.0	"		1
IN	36	1						
		1						
			1		İ	- 1		

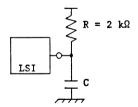


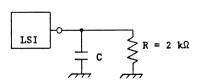


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6W-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"U	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=12	mA) & 1	nout Bu	ffer (T	rue)		
H6WU	with Pull-up Res				(-	,		8
Cell Symbol				pagation	Delay	Paramet	er	
		t	up	T	td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X + IN
		3.02	0.038	4.12	0.047			OT → X
		(6.25)		(8.12)				
		(0.25)		(0.22)				
IN -	$\overline{}$			1				
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \							į
от —	$\rightarrow$ x						1	
01	<b>√</b> "			l				
				1				
	l						l	
	C			1	1		1	
	· ·							İ
			L + 2	7.		Z + I	<u>.                                    </u>	
		t0	<del> </del>	KCL	t0		KCL	$\neg \mid c \rightarrow x$
		2.9	6	1100	3.6		.047	- "
		(20.2		*	(7.6			
		(20.2	"		(,	"		1
						l		
	Input Loading							
Pin Name	Factor (lu)					- 1		
OT	4				l			
C	2		H + 2	7.	<del> </del>	$Z \rightarrow 1$	7	-
		t0	<del></del>	KCL	to		KCL	
		4.0	3		2.7		0.038	
	Output Driving	(20.2		*	(7.6			
Pin Name	Factor (lu)	(20.2	,		(/	"		
IN	36		1					1
	1		1			1.		1
					1	- 1		
	1		- 1		i			
		L			<u> </u>			



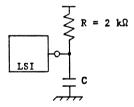


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

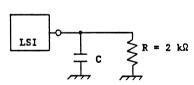
UHB-H6WU-E3 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION UHB" Version Function Cell Name Number of BC Tri-state Output(IOL=12mA) & Input Buffer (True) H6WD with Pull-down Resistance 8 Cell Symbol Propagation Delay Parameter tup tdn KCL KCL2 | CDR2 t0 KCL t0 Path 1.06 0.04 1.84 0.04 X → IN 0.047 OT + X 3.02 0.038 4.12 (6.25)(8.12)IN  $Z \rightarrow L$  $L \rightarrow Z$ KCL t0 KCL  $C \rightarrow X$ tO 2.96 3.69 0.047 (7.69)(20.25)Input Loading Pin Name Factor (lu) OT C 2 H + Z  $Z \rightarrow H$ t0 KCL t0 KCL 4.03 2.72 0.038 Output Driving (20.25)(7.69)Pin Name Factor (lu)

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



IN



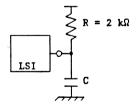
(a) Measurement of tpd at LZ and ZL.

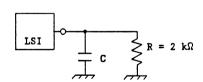
36

- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6WD-E3 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		l "UF	B" Version
	Function	000	<u> </u>		• • • • • • • • • • • • • • • • • • • •		<del>-                                    </del>	Number of BC
	Tri-state Output	(IOL=3.	2mA)					
H6C	& CMOS Interface			(True)			- 1	8
Cell Symbol					Delay P	aramete	r	
		tı	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33				X → IN
		2.42	0.056	2.52				0T → X
	1	(7.18)		(13.57	)			
IN	<b>-</b> <-\h						l	
	, VI						İ	
OT -	<b>x</b>						l	Į
l	Ĭ			1				
	C :			1				
	·						İ	
į		I	L + 2	7.	T	$Z \rightarrow L$	L	<del></del>
	!	t0		KCL	t0		CL	d c → x
		2.0	7		2.55		.13	
		(15.3		*	(13.60	1		
		,	´		,	´		1
	Input Loading		- 1			- 1		
Pin Name	Factor (lu)		- 1					1
OT	4		L					
С	2	$H \rightarrow Z$ $Z \rightarrow H$						
	1	t0		KCL	t0		CL	
		3.4			2.31		056	
	Output Driving	(15.3	5)	*	(13.60	)		
Pin Name	Factor (lu)	l	-					1
IN	36		- 1					
			- 1		l			1
						j		1.
		1	- 1		l	1		1

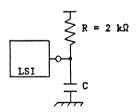


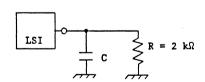


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6C-E4 Sheet 1/1

FILITSIL	MOS GATE ARRAY U	NIT CEL	T. SPF	CII	TCATION	J		111	HR'	Version
	Function	IVII ODD	D DIL	,011	TONITON					umber of BC
	Tri-state Output	(IOL=3.	2mA)	& (	MOS Int	erface				
H6CU	Input Buffer (Tr									8
Cell Symbol			Pr	opa	gation	Delay P	aramet	er		
		t	up	T		tdn			$\neg$	
		t0	KCL	,	t0	KCL	KCL2	CDR	2	Path
		0.92	1		1.33	1		1		$X \rightarrow IN$
		2.42	0.05	6	2.52	0.13		1	- 1	$OT \rightarrow X$
	1	(7.18)		- 1	(13.57)	)}		1	- 1	
IN	<b>-</b> < h ∣			ı						
1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			- 1					١	
от —	<b>x</b>			- 1				İ		
01	^ ^					1		1	-	
·								i	١	
				- 1		1		1	-	
	С					l	ŀ	1	- 1	
l						ł				
			L -	Z		·	$Z \rightarrow L$		$\neg$	
		t0		I	KCL	t0		KCL		$C \rightarrow X$
		2.0			-	2.55		0.13		
		(15.3	5)		*	(13.60	)			
					- 1		1			
	·		- 1		1		ĺ			
	Input Loading		- 1							
Pin Name	Factor (lu)				i					
OT C	4 2		<u>H</u> →	. 7			$Z \rightarrow H$			
١		t0	- H -		KCL	t0		KCL	$\dashv$	
		3.4	<del>,  </del>		VOT	2.31		.056	-	
ļ	Output Driving	(15.3			*	(13.60		. 550		
Pin Name	Factor (lu)	(15.5	٠,		1	(15.00	′			
IN	36						1			
			1		l					
			ł		1					
	1		- 1		l					





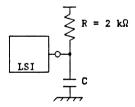
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

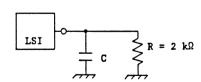
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6CU-E4 | Sheet 1/1

FULLTSU	CMOS GATE ARRAY U	NIT CFL	I. SPECI	FICATIO	N .		T"UH	B" Version
Cell Name	Function	IVII ODD	D DI BOI	11011110				Number of BC
	Tri-state Output	(IOL=3.	2mA) &	CMOS In	terface			
H6CD	Input Buffer (Tr						]	8
Cell Symbol			Prop	agation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33			İ	X → IN
		2.42	0.056	2.52				OT → X
	1	(7.18)		(13.57	)		l	
IN	<b>-</b> < h				1		l	
	7							
OT					1			
OT -	x							
İ								
				ļ			l	
	C							
	· ·							
			$L \rightarrow 2$	!	<u> </u>	$Z \rightarrow L$	1	<del> </del>
		t0		KCL	t0		CL	d c → x
		2.0	7		2.55		.13	
		(15.3	5)	*	(13.60	)		
			·		,			
			- 1					
	Input Loading							
Pin Name	Factor (lu)					- 1		
OT	4							
C	2		H → 2			$Z \rightarrow H$		_
		t0		KCL	t0		CL	
	1	3.4			2.31		056	
١	Output Driving	(15.3	5)	*	(13.60	)		
Pin Name	Factor (lu)		ł			- 1		
IN	36					- 1		
			- 1			1		
			- 1			- 1		
	_l	l						_1

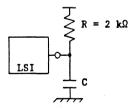


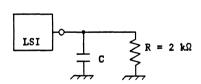


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6CD-E4 | Sheet 1/1

FUJITSU	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UH									
	Function							Number of BC		
	Tri-state Output	(IOL=12	mA) &	CMOS Int	erface					
H6E	Input Buffer (Tr						Ì	8		
Cell Symbol	· · · · · · · · · · · · · · · · · · ·		Pro	pagation	Delay	Paramet	er			
		t	up	7	td					
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		0.92	0.04	1.33	0.04			X + IN		
		3.02	0.038		0.047		l	OT + X		
				(8.12)			1			
		(6.25)					İ			
IN —		l			1	1				
	\					1	1			
от ——	<b>→</b> x		l			1				
	· ·		l			1	1			
			l			l	l	1		
						1	]			
	С		l				1			
			l			l	1			
			L +	2		$Z \rightarrow I$				
		t0	TΤ	KCL	t0		KCL	$\neg c \rightarrow x$		
		2.9	6		3.6		0.047	<b>-</b>		
		(20.2		*	(7.6					
		(20.2	,		('	'				
		1	- 1			I				
	Input Loading	1				1				
Pin Name	Factor (lu)		- 1			1				
OT	4	1	1							
Č	2		H →	7.	<del> </del>	$Z \rightarrow 1$	1	-		
•	1	t0	<del>-i</del> -	KCL	t0		KCL	7		
		4.0	3		2.7		0.038	7		
	Output Driving	(20.2		*	(7.6			1		
Pin Name	Factor (lu)	`==	1		``	1		1		
IN	36	i				- 1		1		
		l	- 1		1	- 1		ł		
	1		- 1			1		1		
	I	l	- 1		I			ı		

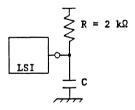


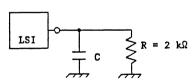


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6E-E3 | Sheet 1/1

FULLIA	MOS GATE ARRAY U	NIT CEL	I. SPEC	TEICATIO	N		"IT	HB" Version
	Function	000	<u> </u>	11.10110.				Number of BC
	Tri-state Output	(IOL=12	mA) &	CMOS Inte	erface			
H6EU	Input Buffer (Tr							8
Cell Symbol				pagation		Paramet	er	
		t	up	1	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04			X → IN
		3.02	0.038		0.047			OT → X
l	_	(6.25)		(8.12)				
IN	<b>-</b> <-			1 1			1	
]	\ \ \			1		1	1	
	\ \ \						1	
OT -	x					1	1	1
	ľ I					1	l	į.
l							Ì	
	Ċ						1	
l	С			1			ł	
			L →	1		$Z \rightarrow I$	<del>!</del>	
		t0		KCL	t0		KCL	$ c \rightarrow x$
		2.9	6	KOD	3.6		0.047	- "
		(20.2		*	(7.6			
l		(20.2	"		(/	"		
						- 1		
	Input Loading							1
Pin Name	Factor (lu)				1	1		
OT	4		- 1					
C	2		H →	Z		$Z \rightarrow I$	ł	
1		t0		KCL	tO		KCL	
		4.0	3		2.7		0.038	
	Output Driving	(20.2	5)	*	(7.6	59)		1
Pin Name	Factor (lu)	}				1		
IN	36		1					
			- 1					1
	Ì		l					
1		ł	1		İ			





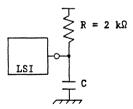
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

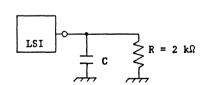
UHB-H6EU-E3 | Sheet 1/1

Cell Name Function Number of BC Tri-state Output(IOL=12mA) & CMOS Interface H6ED Input Buffer (True) with Pull-down Resistance 8 Cell Symbol Propagation Delay Parameter tup tdn KCL KCL t0 KCL2 CDR2 Path 0.92 0.04 1.33 X → IN 3.02 0.038 4.12 0.047  $OT \rightarrow X$ (6.25)(8.12)IN  $L \rightarrow Z$  $Z \rightarrow L$ t0 KCL t0 KCL  $C \rightarrow X$ 3.69 0.047 2.96 (20.25)(7.69)Input Loading Pin Name Factor (lu) OT 2  $H \rightarrow Z$  $Z \rightarrow H$ С t0 KCL t0 KCL 0.038 4.03 2.72 Output Driving (20.25)(7.69)Pin Name Factor (lu) IN 36

\* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

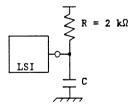


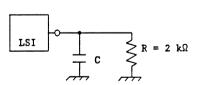


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6ED-E3 | Sheet 1/1

FUJITSÜ	CMOS GATE ARRAY U	10S GATE ARRAY UNIT CELL SPECIFICATION "U									
Cell Name	Function							Number of BC			
	Tri-state Output	(IOL=3.	2mA) &								
H6S	Schmitt Trigger	Input B	uffer(C	MOS Typ	e, True)			12			
Cell Symbol			Prop	pagation	Delay P	aramete	r				
			up		tdn						
		t0	KCL	t0	KCL	KCL2	CDR2				
		2.48	0.16	3.08				X → IN			
		2.42	0.056	2.52			l	OT → X			
	1	(7.18)		(13.57	)		İ				
IN —	─<ਯbr/> h			İ			İ				
	7			1	1		1				
от —	x						l				
"	^						1				
				1			l				
				1	1		l				
1	С										
	_			l			i				
		$L \rightarrow Z$ $Z \rightarrow L$									
		t0		KCL	t0	K	CL	_ c → x			
		2.0	7		2.55		.13				
		(15.3	5)	*	(13.60	)					
			l								
	Input Loading		- 1								
Pin Name	Factor (lu)		1			- 1					
OT	4		H → 2	,		$Z \rightarrow H$		4			
С	2	t0	<u> </u>	KCL	t0		CL	-			
		3.4	<del>.  </del>	VOT	2.31		056	┥			
	Output Driving	(15.3	-	*	(13.60	1	050				
Pin Name	Factor (lu)	(13.3	·		(15.00	<b>′</b>					
IN	18		- 1			- 1		ł			
			ļ					İ			
			-								

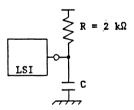


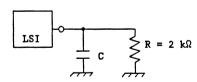


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6S-E2 | Sheet 1/1

FUJITSU	CMUS GATE ARRAY U	10S GATE ARRAY UNIT CELL SPECIFICATION								
Cell Name	Function							Wumber of BC		
	Tri-state Output	(IOL=3.	2mA) 8	Schmitt Schmitt	Trigger					
H6SU	Input Buffer(CMO	S Type,	True)	) with Res	sistance			12		
Cell Symbol			Pro	opagation			r			
	,		up		tdn					
		t0	KCL		KCL	KCL2	CDR2	Path		
		2.48			0.10			X → IN		
		2.42	0.056		0.13		)	OT → X		
		(7.18)		(13.57)	'		1			
IN —	<b></b> <⊅h									
	7				1		l			
от —	x —				1 1					
01	<b>√</b>			1			1	ł		
							l			
	i			1			1	ł		
	С			j				j		
	-							1		
			L →	Z		$Z \rightarrow L$				
		t0		KCL	t0		CL	] c → x		
		2.0			2.55		13	1		
		(15.3	5)	*	(13.60	)				
1			- 1	1						
			- 1	1				1		
1	Input Loading		1			)				
Pin Name OT	Factor (lu)		1	i		l		1		
C	2	ļ	- H →	<del></del>		$Z \rightarrow H$		4		
1	2	t0	_ <del>n →</del>	KCL	t0		CL	-{		
		3.4	<del>,  </del>	YOT	2.31		056	-1		
<b> </b>	Output Driving	(15.3		*	(13.60		. 050	1		
Pin Name	Factor (lu)	\13.5	-,	1	(25.00	<b>'</b> ]				
IN	18		ı							
			1							
				1				1		
		Ì.						İ		

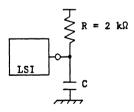


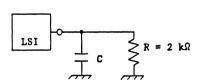


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6SU-E2 | Sheet 1/1

FUJITSU	U CMOS GATE ARRAY UNIT CELL SPECIFICATION "UH									
Cell Name	Function							umber of BC		
	Tri-state Output	(IOL=3.2	2mA) &	Schmitt	Trigger					
H6SD	Input Buffer(CMO	S Type,	True)	with Res	sistance		ł	12		
Cell Symbol			Prop	agation	Delay P	aramete	r			
		tı		T	tdn					
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		2.48	0.16	3.08	0.10			X → IN		
		2.42	0.056	2.52	0.13			OT → X		
	!			(13.57)	)					
	$\overline{\sigma}$				1					
IN ————————————————————————————————————				1			1			
	N 1						l			
от —	→ x						ļ			
		· 1								
							l			
	1									
	C	]					Į.			
	•	1								
			$L \rightarrow Z$			$Z \rightarrow L$	<b></b>			
		t0		KCL	t0	K	CL	C → X		
		2.0	7		2.55	0	.13			
		(15.3	5)	*	(13.60	)				
		`			•	`				
			ı	j		ı				
	Input Loading	1	l							
Pin Name	Factor (lu)		1			1		1		
TO	4	1	- 1			1		1		
С	2		H → Z	2		$Z \rightarrow H$		1		
		t0		KCL	t0	K	CL	1		
		3.4	1		2.31	0.	056	1		
	Output Driving	(15.3	5)	*	(13.60	)		1		
Pin Name	Factor (lu)	'	.		•					
IN	18	1	į			1				
		l	ļ							
		1						1		
		l				- 1		i		

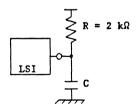


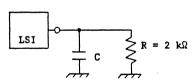


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6SD-E2 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELL :	SPECI	FICATIO	N	MOS GATE ARRAY UNIT CELL SPECIFICATION "U									
Cell Name	Function							HB" Version Number of BC							
	Tri-state Output	(IOL=3.2m	3 (F	Schmitt	Trigger										
H6R	Input Buffer (TT	L Type, T	rue)		-			12							
Cell Symbol	·		Prop	agation	Delay P	aramete	r								
		tup			tdn										
		t0 1	(CL	t0	KCL	KCL2	CDR	2 Path							
			.16	3.72				X → IN							
			. 056	2.52			ĺ	OT → X							
	1	(7.18)		(13.57)	)										
IN —	<i>-&lt;1</i>	1					l								
	, <del>7</del> ]														
	\ \ \			1			1								
OT -	x						1								
	Y				1										
				İ	1										
	_			1			ł								
	С	1		1				į							
		ļ <u>l.</u> .	L → 2	ļ		$Z \rightarrow L$	<u> </u>								
		t0	7 4	KCL	t0		CL	- $+$ $+$ $+$ $+$ $+$ $+$ $+$							
		2.07		VCT	2.55		0.13	⊣ <sup>് 7</sup> ^							
		(15.35)	-	*	(13.60		,,13	1							
		(13.33)	1		(13.00	'		1							
			1												
<del></del>	Input Loading		-			ı									
Pin Name	Factor (lu)		-												
OT	4		- 1												
C	2		H → 2	2		$Z \rightarrow H$									
		t0		KCL	t0		CL								
		3.41	T		2.31	0.	056								
	Output Driving	(15.35)		*	(13.60	)									
Pin Name	Factor (lu)		-			}									
IN	18		-												
ĺ			-												
	1		1			· ·									

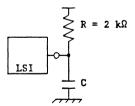


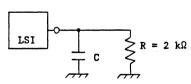


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6R-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SI	PECIFICATION	ON		"UHB	" Version
Cell Name	Function						umber of BC
	Tri-state Output	(IOL=3.2mA)	& Schmitt	Trigger			
H6RU	Input Buffer (TI						12
Cell Symbol		1	Propagation	n Delay P	arameter		
		tup		tdn			
		to K		KCL	KCL2	CDR2	Path
		2.24 0.1					X → IN
			056 2.5		1		OT → X
	1	(7.18)	(13.5	7)	1		i
IN	<i>&lt;</i> ⊅h		1	ŀ			İ
	7			1			
OT	x				1		l
OT -	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		1	1	1		
			1	l	1 1		
			ł	1	1		
	С				1		i
j	· ·	)		1			1
		L	→ Z	T	$Z \rightarrow L$		
		t0	KCL	t0	KC	L	c → x
		2.07		2.55	0.	13	1
		(15.35)	*	(13.60	)		l
			ļ	i			
			1	1			l
	Input Loading		ł	1			
Pin Name	Factor (lu)		i	1			]
OT	4		<u> </u>				1
С	2		→ Z		Z + H		
	}	t0	KCL	t0	KC		Į
	10.1.1.2.1.1	3.41	*	2.31		56	
Din Non-	Output Driving	(15.35)	*	(13.60	וי		i
Pin Name IN	Factor (lu)		l	1			ļ
714	10		l				i
							l
							1
		<u> </u>	<u> </u>				1





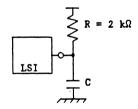
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

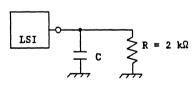
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6RU-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N		"UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output							
H6RD	Input Buffer (TT	L Type,	True)	with Pul	ll-down	Resista	nce	12
Cell Symbol			Prop	agation			r	
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
ı		2.24	0.16	3.72	,			X → IN
		2.42	0.056	2.52			1	OT → X
	1	(7.18)		(13.57)	)		•	1
TN	<i>&lt;1</i> √h						İ	
7:4				i		İ	l	1
	<b> </b> \			l			l	
OT -	x — x						l	
	ΓY							1
							1	
	•						ł	
	С			1				
			L	<u>l</u>	<u> </u>	<u> </u>	<u> </u>	
			$L \rightarrow 2$			$Z \rightarrow L$		┦
		t0		KCL	t0		CL	_ c → x
		2.0			2.55		).13	ļ
		(15.3	5)	*	(13.60	ויי		İ
			l			1		
	· · · · · · · · · · · · · · · · · · ·	1	i	l		1		
D/- 11	Input Loading		- 1					
Pin Name	Factor (lu)		1			1		1
OT C	4		H → 2	,		$Z \rightarrow H$		-
U	2	t0	$n \rightarrow 2$	KCL	t0		CL	-
	}	3.4	<del>,  </del> -	VOT	2.31		056	4
	Output Driving	(15.3	-	*	(13.60		030	
Pin Name	Factor (lu)	(13.3	'3)		(15.00	'		İ
IN IN	18	{	-			1		1
TIN	10	1	1			I		1
		l	1			1		1
		1	1			}		J
		İ			L			

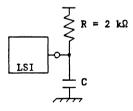


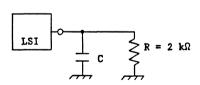


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6RD-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	IB" Version						
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=3.2	mA) wi	th Noise	e Limit	Resista	nce	
H8T	& Input Buffer (	True)						9
Cell Symbol			Prop	agation	Delay P	aramete	r	
		tu			tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X → IN
		3.12	0.056	5.66	0.13		l	OT → X
	_	(7.88)		(16.71)	)		ŀ	1
IN							ļ.	1
IN	$\sim$	1 1					ŀ	
				1	1		1	
от —	<b>→</b> x							
	<b>▶</b> Ŷ	ł			1		l	
		1 1			1		ł	1
	i	1 1					ł	1
	C						ł	
		1 1					1	
			L + Z			$Z \rightarrow L$		
		t0		KCL	t0	K	CL	¬ c → x
		2.22			6.47	0.	13	
		(16.44	) l	*	(17.52	)		
		, ,	´	- 1	•	´		
		{	Į.	i		1		
	Input Loading	1						
Pin Name	Factor (lu)	1						İ
OT	2	1				İ		1
С	2		H + Z			Z + H		7
		t0		KCL	t0	K	CL	
		3.07			3.20	0.	056	7
	Output Driving	(16.44	)	*	(17.52	)		1
Pin Name	Factor (lu)	]						1
IN	36	1						
			1	- 1				Ì
		[						
	1	i	- 1			ı		1

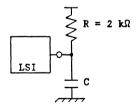


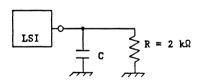


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8T-E3 | Sheet 1/1

							1 11	v
	CMOS GATE ARRAY U	NIT CEL	L SPEC	1F1CAT1ON	<u> </u>			" Version
Cell Name	Function	/TOT 0						umber of BC
******	Tri-state Output						nce	_
H8TU	& Input Buffer (	True) w						9
Cell Symbol				pagation			r	·
	•		up	4	tdn		0000	<b>.</b>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
,		1.06		1.84			1	X → IN
		3.12	0.056		,		l	OT → X
	1	(7.88)		(16.71)	)		l	
IN	<b>-</b> < h			į			1	
	, 기			1			[	1
				ı			1	
от —	x			1			ł	
	νľ			1			l	
				1				
	_			ı			1	
	С		l	ı			1	ļ
			l		1		L	
		t0	L →	KCL	t0	$Z \rightarrow L$	CL	c → x
		2.2	2	KCL	6.47		13	1 0 7 1
		(16.4		*	(17.52	1	13	
		(10.4	۱ (۳		(17.52	'		}
			ļ	1				1
	Input Loading		- 1	l		- 1		1
Pin Name	Factor (lu)		- 1	ļ				1
OT	2		- 1			ı		
C	2	ļ	H →	7		$Z \rightarrow H$		1
Ĭ	_	t0	<del>-                                    </del>	KCL	t0		CL	1
		3.0	7		3,20		056	1
	Output Driving	(16.4		*	(17.52	1 -	-50	
Pin Name	Factor (lu)	\10.7	7		(17.52	<b>'</b>		
IN	36	l	- 1	1		1		
	1	İ						1
	1		- 1	l				1
		1				ı		

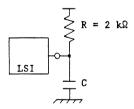


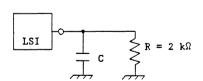


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8TU-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL	SPECI	FICATION	N		"UH	IB" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=3.2	mA) wi	th Nois	e Limit F	Resista		
H8TD	& Input Buffer (	True) wi	th Pul	1-down 1	Resistano	ce		9
Cell Symbol			Prop	agation	Delay Pa	aramete	r	
		tu			tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
			0.04	1.84		i		$X \rightarrow IN$
		3.12	0.056	5.66				OT → X
	1	(7.88)		(16.71	기			1
IN —	<b>-</b> < h '				1	1		
	7							
ОТ	x							
01	^				1 1			
					1			
	İ				1 1	ì		1
	С				1 1			
	· ·				1			1
			L + Z			$Z \rightarrow L$		
		t0		KCL	t0		CL	d c → x l
		2.22			6.47			
		(16.44	•)	*	(17.52)			
		,	1					
		ļ				1		
	Input Loading					- 1		
Pin Name	Factor (lu)		- 1			1		
OT	2							_
С	2		H → Z			Z → H		_
	İ	t0		KCL	t0		CL	_
	<u> </u>	3.07			3.20	3	056	
Dia Nama	Output Driving	(16.44	+)	*	(17.52)	<i>)</i>		
Pin Name IN	Factor (lu)	{						
IN	30		1			1		
		ĺ	ŀ			- 1		
1	1	{	1			1		

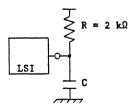


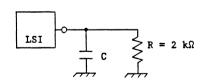


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8TD-E3 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N .			" Version
Cell Name	Function	·					N N	lumber of BO
	Tri-state Output		nA) wit	h Noise	Limit Re	sistan	ce	
H8W	& Input Buffer (	True)						99
Cell Symbol				agation	Delay Pa	ramete	r	
			ир	L	tdn			]
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84			l	X → IN
		3.96	0.038	7.25				OT → X
	4	(7.19)		(11.84)	)		l	
IN —	<b>─</b>				1		l	
111	, \				1			
					1 1			
OT	<b>x</b>				1 1			1
					1 1		ĺ	
	}	1			) )			
	1			]	1			
	C			1	1 1			
					1 1		l	
			$L \rightarrow 2$	2		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	] c → x
		3.6	5		7.40	0.	054	1
		(21.7)	3)	*	(11.99)	)		
		•	1					
								1
	Input Loading					- 1		l
Pin Name	Factor (lu)		1			i		İ
OT	2					l		1
С	2		H + 2	3		$Z \rightarrow H$		1
		t0		KCL	t0	I K	CL	1
		3.7	5		3.69	0.	038	1
	Output Driving	(21.7		*	(11.99			1
Pin Name	Factor (lu)	,						1
IN	36	1				ı		
						1		}
			1					
		l	- 1					1

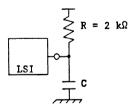


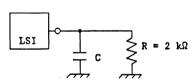


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8W-E2 | Sheet 1/1

PHITTEH (	CMOS GATE ARRAY U	NIT CELL	CDECT	TICATION	,		1 11/11/1	B" Version
Cell Name	Function	NII CELL	SPECI	FICATION	<u> </u>			Number of BC
Cell Name	Tri-state Output	(TOT = 12m	A)+	h Noice	Timit D	cicton		Number of BC
нвwu	& Input Buffer (						ice	9
Cell Symbol	& Input Buller (	liue) wi	Pron	1-up kes	Delay Pa	ramoto		<del></del>
Cell Symbol		tu		agacion	tdn	ar ame ce		T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
			0.04	1.84		RUDZ	CDRZ	X + IN
			0.038	7.25				OT + X
		(7.19)	0.036	(11.84)				01 7 7
	1	(7.19)		(11.04)	1 1		l	
IN —	<b>─</b> < h	i i			1 1		l	
	\						1	
от —	<b>X</b>				1		1	
01	^ *	i					]	1
'		1			1 1		ł	<b> </b>
	1						ł	
	C			1			1	1
	· ·	1		1			ļ	1
		<u> </u>	$L \rightarrow Z$			$Z \rightarrow L$	<u> </u>	<del> </del>
		t0		KCL	t0		CL	d с → х
		3.65			7.40		054	1
		(21.73		*	(11.99	)		1 .
		\	´		•	´		1
				l		- 1		1
	Input Loading							1
Pin Name	Factor (lu)		i			- 1		
OT	2	1				- 1		
C	2		H → Z			Z → H		7
		t0		KCL	t0	1	KCL	7
1		3.75			3.69		.038	7
	Output Driving	(21.73	3)	*	(11.99	)		
Pin Name	Factor (lu)	1		}				
IN	36	1	ŀ	į		1		
	}	}				1		1





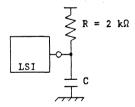
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

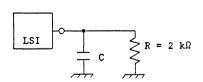
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8WU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	· ·		ט" ד	нв"	Versio	n
Cell Name	Function						1		mber of	
	Tri-state Output	(IOL=12	mA) wit	h Noise	Limit R	esistan	ce			
H8WD	& Input Buffer (	True) w							9	
Cell Symbol				agation			r			
			up		tdn			_		1
		t0	KCL	t0	KCL	KCL2	CDR	2	Path	
		1.06	0.04	1.84	0.04				X → I	
		3.96	0.038	7.25	0.054			- 1	OT → X	
	1	(7.19)		(11.84)	İ			-		
IN	<b>&lt;</b> h ∣							-		
,	/ 7									
от —	x									
51	\\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \\ \forall \forall \\ \forall \forall \\ \forall \forall \forall \\ \forall \forall \forall \forall \\ \forall \forall \forall \forall \forall			]				- 1		
								- 1		
	С			j						
	-									
			L → 2			$Z \rightarrow L$				
		t0		KCL	t0	K	CL		C →	x
		3.6	5		7.40	0.	054			
		(21.7	3)	*	(11.99	)				
				į						
								- 1		
	Input Loading									
Pin Name	Factor (lu)			-		1				
OT	2							_		
С	2		H → Z			$Z \rightarrow H$	<u> </u>	$\dashv$		
		t0		KCL	t0		CL	$\dashv$		
	Output Driving	3.7 (21.7	1	*	3.69 (11.99		038			
Din Nama		(21.7	3)		(11.99	'				
Pin Name IN	Factor (lu)	l						į		
114	]		}					- 1		
			1							
			- 1					1		
		L								

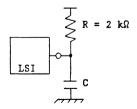


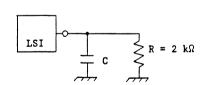


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation}.$

UHB-H8WD-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	N		<b>"</b> U	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=24	mA) w:	ith Noise	Limit R	esistan	ce	
H8W2	& Input Buffer (							11
Cell Symbol		T		opagation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR:	Path .
		1.06	0.04	1.84	0.04			X → IN
1		5.61	0.03	2 11.62	0.06		l	OT → X
	4	(8.33)		(16.72)	)		1	
IN —					1	į	1	
IN	. \			1				
				1				
OT	→ x			1			}	1
	V			1		į		
							l	
		1		1			1	
	С			i			1	
					<u> </u>	<u> </u>		
			L →			$Z \rightarrow L$		
1		t0		KCL	t0		CL	_ c → x
		5.3			11.18		06	
		(23.2	3)	*	(16.28	)		
			1			1		1
			1					
1	Input Loading	ĺ	ı					
Pin Name	Factor (lu)	1				- 1		
OT	2	ļ						4
С	2		Н →			Z → H		4
		t0		KCL	t0		CL	_
	1	6.3			5.25		032	
Dia Nam	Output Driving	(23.2	3)	*	(16.28			1
Pin Name	Factor (lu)	1				- 1		
IN	36							
			- 1	i		-		1
1						1		
	<u></u>	l						





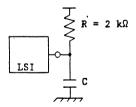
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

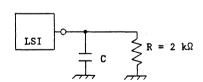
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8W2-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		່ "ບາ	IB" Ve	rsion
Cell Name	Function								r of BC
	Tri-state Output	(IOL=24	mA) wit	h Noise	Limit R	esistan	ce		
H8W1	& Input Buffer (	TTL, Tr	ue) wit	h Pull-u	p Resis	tance	- 1		11
Cell Symbol			Prop	agation	Delay P	aramete	r		
		t	up	i i	tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2 P	ath
j		1.06	0.04	1.84	0.04			X	→ IN
		5.61	0.032	11.62	0.06			TO	' → X
		(8.33)		(16.72)					
		` ′		` '				ı	
IN —								ı	
1	$\setminus$ 1				]			1	
ОТ	> x				]			1	
1				1					
	C .							1	
	•								
İ			$L \rightarrow Z$	<u>'                                    </u>	1	$Z \rightarrow L$			
Ì		t0		KCL	t0		CL	$\dashv$ $\circ$	: → X
		5.3		NOD .	11.18		06	⊢ ~	
		(23.2		*	(16.28		•		
		(23.2	"		(10.20	'		1	
1								1	
	Input Loading			1		- 1		-	
Pin Name	Factor (lu)							1	
OT	2								
C	2		H → Z			Z → H		$\dashv$	
	_	t0		KCL	t0		CL	-	
1		6.3	<del>,   -</del>	NOD	5.25		032	$\dashv$	
	Output Driving	(23.2		*	(16.28		032	1	
Pin Name	Factor (lu)	(23.2	٠,		(10.20	7		1	
IN	36		- 1	ļ				-	
111	30					- 1		1	
1			ı			ı		- 1	
						- 1		-	
	· 1		i						

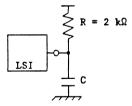


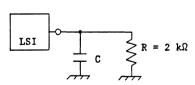


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8W1-E2 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		T"UH	B" Version
	Function	····· ODDI	<u> Di Doi</u>	110110.	· · · · · · · · · · · · · · · · · · ·			Number of BC
	Tri-state Output	(IOL=24m	A) wit	h Noise	Limit R	esistan		
H8WO	& Input Buffer (	TTL, Tru	ne) wit	h Pull-	down Res	istance	.	11
Cell Symbol			Prop	agation	Delay P	aramete	r	
		tu			tdn			
1		t0	KCL	t0	KCL	KCL2	CDR2	
		1.06	0.04	1.84			l	X → IN
		5.61	0.032	11.62			l	OT → X
	1	(8.33)		(16.72	기		ł	
IN —	<b>-</b> < h ∣						1	
1	7						l	
ОТ —	<b>X</b>							
	^ ^							
'		1					l	
	1			]			1	
	С	l i		1			1	
							1	
			L → Z			$Z \rightarrow L$		
		t0		KCL	t0		CL	_ c → x
		5.36	1		11.18		.06	
l		(23.23	3)	*	(16.28	)		
}								
	I Tomas Toods							
Pin Name	Input Loading Factor (lu)		- 1					
OT OT	2		- 1					
l c	2		H → Z			$Z \rightarrow H$		-
	_	t0		KCL	t0		CL	
	1	6.37			5.25		032	7
	Output Driving	(23.23		*	(16.28			
Pin Name	Factor (lu)							
IN	36							
1	1		1					
1	i	ŀ	1			1		

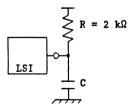


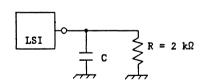


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8W0-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"UF	B" Version
Cell Name	Function							Number of BC
	Tri-state Output				e Limit	Resista	nce	
H8C	& CMOS Interface	Input I	Buffer	(True)				9
Cell Symbol			Prop	agation	Delay P		r	
			ıρ		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33				X → IN
		3.12	0.056	5.66				OT → X
	1	(7.88)		(16.71	기	1		
IN —	<b>-</b> < h ∣				1 1			
	\ \ \ \							
от —	x							
"	^ ^							
					1 1			
	C	1						
		1	L + Z	<u> </u>	J	$Z \rightarrow L$		
		t0		KCL	t0		CL	$\dashv c \rightarrow x$
		2.2			6.47		.13	-
		(16.44		*	(17.52			1
		,			•	´		
1						1		
	Input Loading	İ				- 1		
Pin Name	Factor (lu)					- 1		ł
OT	2							
C	2		H → Z			$Z \rightarrow H$		
		t0		KCL	t0		CL	_
		3.0			3.20		056	1
l	Output Driving	(16.44	4)	*	(17.52	)		
Pin Name	Factor (lu)							ŀ
IN	36		l					
	1	l	- 1					1
			- 1					
L	1	l				1		





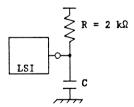
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

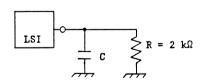
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8C-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> UI	HB" Version	1
Cell Name	Function							Number of	
	Tri-state Output(	IOL=3.2	mA) w/	Noise L	imit Res	istance	&	,	
H8CU	CMOS Interface In	put Buf	fer (Tr	ue) w/ :	Pull-up	Resista	nce	9	
Cell Symbol			Prop	pagation	Delay P	aramete	r		
		t	up	1	tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2 Path	
		0.92	0.04	1.33				X → IN	
		3.12	0.056	5.66	0.13		1	OT → X	
	4	(7.88)		(16.71	)		ļ	I	
in —				İ					
714					1			1	
		I							
OT	-	1		1					
	V			Ì				I	
		İ		ļ			1		
		]	}	1				1	
	C						1		
								_	
			$L \rightarrow 2$			$Z \rightarrow L$			
		t0		KCL	t0		CL	C → 2	X
		2.2			6.47		1.13		
		(16.4	4)	*	(17.52	)		1	
			İ			1		ı	
		1						1	
	Input Loading		- 1						
Pin Name	Factor (lu)					1			
OT	2								
С	2		H → 2			$Z \rightarrow H$			
		t0		KCL	t0		CL	_	
		3.0			3.20		056		
	Output Driving	(16.4	4)	*	(17.52	)			
Pin Name	Factor (lu)	ļ	l						
IN	36		1					1	
			l						
		l	I			- 1			
	1	ı	1			1		1	





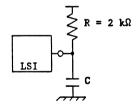
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

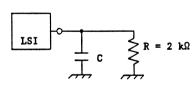
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8CU-E3 | Sheet 1/1

FULLTSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
	Function							Number of BC			
	Tri-state Output(	IOL=3.2	mA) w/	Noise L	lmit Resi	stance	&				
H8CD	CMOS Interface In	put Buf						9			
Cell Symbol			Prop	agation	Delay Pa	ramete	r				
			up		tdn						
		t0	KCL	t0	KCL	KCL2	CDR2	Path			
		0.92	0.04	1.33	0.04			X + IN			
		3.12	0.056	5.66	0.13			OT → X			
l	1	(7.88)		(16.71)	'l l			1			
IN -	<b>&lt;</b> h ∣				1 1						
	7	1									
от —	x -										
"	A *										
					1						
	l				1 1			1			
	С			1	1						
1				•			į				
			L + 2		***************************************	Z + L					
		t0		KCL	t0		CL	] c → x			
ļ		2.2			6.47		.13	]			
l		(16.4	4)	*	(17.52)	)					
1											
1	Input Loading		- 1								
Pin Name	Factor (lu)		- 1								
OT C	2 2	<b></b>	H → 2	, —		$Z \rightarrow H$		-			
	1 2	t0		KCL	t0		CL	-			
		3.0		VOT	3.20		056	-			
	Output Driving	(16.4		*	(17.52)		050				
Pin Name	Factor (lu)	(10.4	<sup>-,</sup>		(17.52)	'					
IN	36	1	l			- 1					
		l	- 1			- 1					
			- 1								
		1	- 1								

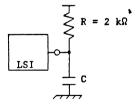


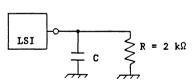


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8CD-E3 | Sheet 1/1

FULLTSU	CMOS GATE ARRAY U	NIT CEL	CDE	CIEICATIO	Ŋ		מאווי	" Version
Cell Name	Function	MII CEL	L SFE	CIFICALIO	<u> </u>			lumber of BC
	Tri-state Output	(IOL=12	mA) w	ith Noise	Limit Res	istance	+	
H8E	& CMOS Interface						1	9
Cell Symbol					Delay Par	ameter		
		t	up	1	tdn			
		t0	KCL	t0	KCL	KCL2 C	DR2	Path
		0.92	0.04					X → IN
		3.96	0.03			1		OT → X
	1	(7.19)		(11.84	)	1		
IN	<b>-</b> <- h ⋅					ļ		
	\ \ \ \					ł		1
от —	x -				1 1			
01	X X				1 1	1		
					1 1	[		
	С			1	1 1	i		
1	Ū				1	1		
	•	L	$L \to Z \qquad \qquad Z \to L$					
		t0		KCL	t0	KCL		1 c → x
l		3.6	5		7.40	0.054		Ì
	,	(21.7	3)	*	(11.99)	,		
								İ
			1					
	Input Loading		- 1					l
Pin Name	Factor (lu)							
TO	2							
C	2	10	H →			Z → H		1
ļ		t0 3.7	-	KCL	t0 3.69	0.038	,	-
<u> </u>	Output Driving	(21.7		*	(11.99)	1 0.030	•	
Pin Name	Factor (lu)	(21./	ا ر	••	(11.99)			
IN	36		1					1
1	""		- 1			1		1
			- 1			1		1
1			- 1					1

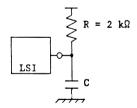


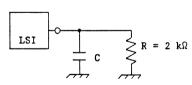


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\text{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			" Version
Cell Name	Function							umber of BC
	Tri-state Output(	IOL=12m	A) with	Noise	Limit Res	istance	&	
H8EU	CMOS Interface In	put Buf	fer (Tr	ue) w/	Pull-up R	esistan	ce	9
Cell Symbo	1		Prop	agation	Delay Pa	rameter		
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33				X → IN
		3.96	0.038	7.25				OT → X
	4	(7.19)		(11.84	)			
IN —								
211	$\sqrt{N}$							
OT -	- x				1 1			
	M							
					1			
				1	1			
	C				1			
			L → Z			Z → L		
		t0		KCL	t0	KC		C → X
		3.6	- 1		7.40	0.0	54	
		(21.7	3)	*	(11.99)			
	Input Loading							
Pin Name	Factor (lu)							
OT	2	ļ						
С	2		H → Z			Z → H		ļ
		t0		KCL	t0	KC		Į
		3.7	-		3.69	0.0	38	
<b>5</b>	Output Driving	(21.7	3)	*	(11.99)			
Pin Name	Factor (lu)	ł				1		l
IN	36	1						
		1						1
	1							
IN	36				·			

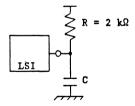


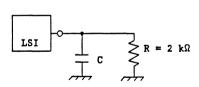


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8EU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N N		"UHB	" Version	
	Function				·			Number of	
	Tri-state Output(	IOL=12m	A) with	Noise	Limit Res	istance			
H8ED	CMOS Interface In							9	
Cell Symbol		Î	Prop	agation	Delay Pa	rameter			
		t	up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.92	0.04	1.33				X - IN	1
		3.96	0.038	7.25	0.054			OT → X	
	4	(7.19)		(11.84	)				
IN -	<b>─</b> < h						l		
2.11							1		
				Ì	1		1		
ОТ —	x +							İ	
	V			l					
					j l		1		
	,			l			1	1	
	С				}			]	
			$L \rightarrow Z$			$Z \rightarrow L$	<u> </u>	<b> </b>	
		t0		KCL	t0	KC	٦.	C → >	,
		3.6		KOL	7.40	0.0		" ' '	•
		(21.7		*	(11.99)	""		]	
		\	,		(22.77)				
		1	1			- 1		1	
	Input Loading	1				1		1	
Pin Name	Factor (lu)	l	1			- 1		]	
OT	2	1				1		1	
C	2		H → Z			$Z \rightarrow H$		1	
		t0		KCL	t0	KC	CL	1	
		3.7			3.69	0.0		1	
	Output Driving	(21.7	3)	*	(11.99)	-			
Pin Name	Factor (lu)	`						1	
IN	36		i	į		-		1	
		l	1			-		1	
		ĺ	İ	i		-		ļ	
		ŀ							

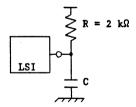


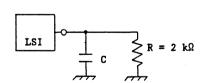


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8ED-E2 | Sheet 1/1

FULL TOOL O	WOO CAME ADDAY II	17. O.T.					W.n.s	W		
Cell Name I	MOS GATE ARRAY U	NII CEL	L SPECI	FICATIO	N			" Versi		
OCII Mame I	Tri-state Output	(101.=24	mΔ) w/	Noise I.	imit Rosis	tance	7	Number	OI BU	
H8E2	& Input Buffer (			MOISC D.	IMIC NESI:	cance	1	11		
Cell Symbol				agation	Delay Par	rameter			***************************************	
		t	up		tdn		-			
		t0	KCL	t0	KCL	KCL2	CDR2	Path	ı	
	•	0.92	0.04	1.33	1 1			X →		
		5.61	0.032	11.62		1		OT →	X	
	4	(8.33)		(16.72	)	1				
IN —	<b>-</b> < h ∣			1						
1	\					1				
от —	<b>x</b>				1	l				
01	, <b>,</b>				1	1				
1										
	1									
	c									
	_				1 1	l				
			L + 2	;		$Z \rightarrow L$				
		t0		KCL	t0	KCL		C →	X	
		5.3			11.18	0.06	,			
		(23.2	.3)	*	(16.28)					
	<del></del>					1				
Pin Name	Input Loading Factor (lu)		- 1							
OT OT	Pactor (Ru)		- 1							
C	2		H + 2	,		$Z \rightarrow H$		l		
	•	t0		KCL	t0	KCL		1		
		6.3	7		5.25	0.03		1		
	Output Driving	(23.2		*	(16.28)			1		
Pin Name	Factor (lu)	'	·		, <i>'</i>					
IN	36							1		
								l		
			- 1			-		l		
l .	t ·				l	1		Į .		





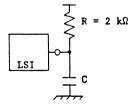
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

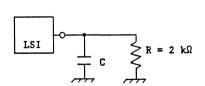
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E2-E2 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version
Cell Name	Function							Number of BC
	Tri-state Output(	IOL=24m	A) w/ h	Noise Li	mit Resis	tance		
H8E1	& Input Buffer(CM	OS, Tru	e) w/ I	ull-up	Resistanc	9		11
Cell Symbo	1		Prop	pagation	Delay Pa:	rameter		
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		0.92	0.04	1.33	0.04			X + IN
		5.61	0.032	11.62	0.06			OT → X
	_			(16.72	)			}
IN ————————————————————————————————————					l		i	1
IN						1		
							l	
от	-  > x			1				
				1				
	•			1	1 1			
	C						1	
			L + 2			Z → L		
		t0		KCL	t0	KC		_ c → x
		5.3	-		11.18	0.0	)6	
		(23.2	3)	*	(16.28)	ł		
			1		ł	1		
	Input Loading		- 1			1		
Pin Name	Factor (lu)		1		1	1		1
OT	2							_
С	2		Η → :			Z → H		_
		t0		KCL	t0	KC		<b></b>
		6.3			5.25	0.0	32	i
	Output Driving	(23.2	3)	*	(16.28)			1
Pin Name	Factor (lu)	1			1	- 1		1
IN	36	İ			1	1		
			1		1	-		
			ı		1			į
	i	ı	1		1	1		1

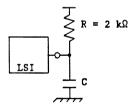


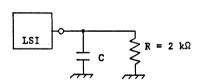


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E1-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			"Version
Cell Name	Function						N	umber of BC
	Tri-state Output(							
H8E0	& Input Buffer(CM	OS, Tru	e) w/ P	ull-dow	n Resistar	ıce		11
Cell Symbo			Prop	agation	Delay Par	ameter		
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33				X → IN
		5.61	0.032	11.62				$OT \rightarrow X$
4		(8.33)		(16.72	)			
IN ————————————————————————————————————								
•••	, 7				1 1			
от —	x +			l				
	V				1 1			
	,				1			
	С				1			
			$L \rightarrow Z$	ļ	,	Z + L	L	
		±0		KCL	t0	KC	T.	c → x
		5.3		NOD _	11.18	0.0		U A
		(23.2	-	*	(16.28)		•	
		(	,		(20,20)			
			1					
	Input Loading							
Pin Name	Factor (lu)		1					
OT	2					1		
С	2		H → Z			Z → H		
		t0		KCL	t0	KC	L	
		6.3	7		5.25	0.0	32	
	Output Driving	(23.2	3)	*	(16.28)			
Pin Name	Factor (lu)					1		
IN	36					1		
						1		
		1				1		
	1	l	- 1			1		

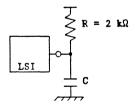


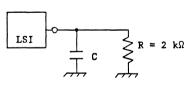


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E0-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function	0000	- 01201					Number of BC
	Tri-state Output	(IOL=3.2	2mA) &	Schmitt	Trigger			Tumber of be
H8S	Input Buffer (CM	OS Type,	True)	w/ Noi	se Limit	Resist	ance	13
Cell Symbol					Delay Pa			
		tu			tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
1			0.16	3.08	1 1			X → IN
1		3.12	0.056	5.66				OT → X
	1	(7.88)		(16.71	기 ]			
IN —	<b></b> <₹h			ĺ	1 1			
	/ 71							
от —	<b>x</b>			1				
1	, ·							
				Í				1
	1			4				1
	C	1 1		ļ	1 1			
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.22			6.47		13	
		(16.44	+)	*	(17.52)	)		
1						1		
	17	1						
Pin Name	Input Loading					l		
OT OT	Factor (lu)	1				- 1		
C	2	ļ	H → 2	,		$Z \rightarrow H$		-
"	1	t0		KCL	t0		CL	-
1		3.07			3.20		056	┪ !
	Output Driving	(16.44		*	(17.52)	1		
Pin Name	Factor (lu)	,			, =			
IN	18	1						
						1		1
1	1	ł	- 1					

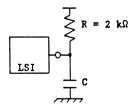


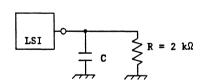


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8S-E2 | Sheet 1/1

THITTON	CMOS GATE ARRAY U	NITT CET	T CDEC	TETCATIO	<u>., </u>	<del></del>	1 11111	ID" U		
Cell Name	Function	NII CEL	L SPEC	IFICATIO	N			IB" Version Number of BC		
Cell Name	Tri-state Output(	TOT = 3 2	2 (Am	Sohmitt '	Tricor			Number of BC		
	Input Buffer (CMOS					cictono	.			
нвsu	w/ Pull-up Resist		rue) w	/ Noise	LIMIT KE	SISCANC		13		
Cell Symbo		ance	Desc		Dalam D	aramata		13		
Cell Symbo	L		Propagation Delay Parameter tup tdn							
		t0	KCL	t0	KCL	KCL2	CDR2	Path		
		2.48	0.16	3.08		RODZ	CDK2	X → IN		
			0.16					OT + X		
		3.12 (7.88)		(16.71				01 7 1		
	(7,00)		(10.71	1 1						
IN -	— ⊬ h</td <td></td> <td></td> <td>1</td> <td></td> <td></td> <td></td> <td></td>			1						
	/ /									
OT — X										
				ł						
	C						1			
	· ·		ł				Ì			
		<b></b>	L →	7		$Z \rightarrow L$	L			
		t0	<del></del> -	KCL	t0		CL	$ c \rightarrow x$		
		2.2	<del>,  </del>	NOD .	6.47		13	⊣		
		(16.4		*	(17.52		13			
j		(20.7	7		(17.52	'				
		l	ļ			- 1				
	Input Loading	l				1		i		
Pin Name	Factor (lu)					- 1				
OT	2	1	ł			1				
c	2		H →	7.		$Z \rightarrow H$		-		
		t0	<del></del>	KCL	t0		CL	7		
		3.0	7		3,20		056	7		
	Output Driving	(16.4		*	(17.52					
Pin Name	Factor (lu)	````	7		(17.52	<b>′</b>				
IN	18	1	1			- 1				
	10	l				- 1				
						- 1				
		l	1			- 1				

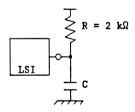


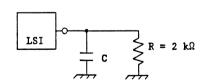


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8SU-E2 Sheet 1/1

FILITSII	CMOS GATE ARRAY U	NIT CEL	I SPEC	TEICATIO	N.		11111	IB" Version
Cell Name	Function	000	L DILLO	11 10A110	1			Number of BC
	Tri-state Output(	IOL=3.2	mA) &	Schmitt '	Trigger			THE MIDEL OF BO
	Input Buffer(CMOS	Type .	True)	w/ Noise	Limit R	esistar	nce	
H8SD	w/ Pull-down Resi			.,				13
Cell Symbo			Pro	pagation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	CDR2	Path			
1		2.48 0.16 3.08 0.10						X → IN
ŀ	*	3.12	0.056				1	OT → X
	4	(7.88)		(16.71	)		1	
"								
от — х								
j								
	С		ļ					
ł								1
}			L +	Z	1	$Z \rightarrow L$		
		t0	T	KCL	t0	I	KCL	d c → x
		2.2	2		6.47	0.	.13	7
		(16.4	4)	*	(17.52	)		
			- 1					1
			- 1					
	Input Loading		1					
Pin Name	Factor (lu)			į				
OT	2							_
C	2		Н →			$Z \rightarrow H$		_
		t0		KCL	t0		KCL	4
	<del>                                     </del>	3.0			3.20		.056	
Dia Name	Output Driving	(16.4	4)	*	(17.52	,		
Pin Name IN	Factor (Lu)							
IN	10		- 1					1
			j					j
			- 1					





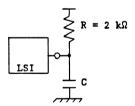
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

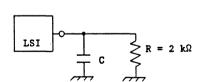
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the  ${\tt simulation}.$

UHB-H8SD-E2 Sheet 1/1

FULLTEU	ONOC CATE ADDAY I	NIT OF	T ODDO	DIGATE O	.,		1 771777	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICALIO	N			" Version Number of BC
Cell Name	Tri-state Output	(TOT - 2	2-4) 5	Cabaitt	Tudasan		-   r	dumber of BC
H8R								13
	Input Buffer (TT	L lype,						13
Cell Symbol				pagation	Delay P		I	Υ
			up	<del>                                     </del>	tdn		CDDO	٠, ا
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.24	0.16	3.72				X + IN
		3.12	0.056	5.66				OT → X
	1	(7.88)		(16.71	ו			
IN —	—<#n			1	1		i	
	\ \ \ \			1				
	\ \ \			1			l	
OT	x -			1	1		l	
	νY			1				
	'			1	1		1	
	С			İ			l	
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0	K	CL	$C \rightarrow X$
		2.2	2		6.47	0.	13	1
		(16.4	4)	*	(17.52	)		
			·	1	•	`		į
			j			ł		l
	Input Loading		1					
Pin Name	Factor (lu)							l
OT	2							
C	2	ļ	H → 2	7.		$Z \rightarrow H$		1
_		t0		KCL	t0		CL	1
		3.0	7		3.20		056	1
	Output Driving	(16.4		*	(17.52			1
Pin Name	Factor (lu)	`	"		(	<b>'</b>		1
IN	18					ı		
			ı					1
			1			1		
	1	l	- 1			1		1

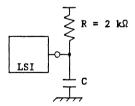


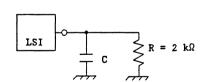


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8R-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	I. SPEC	TEICATIO	N		11111	HB" Version		
Cell Name	Function	000	L DILLO	LITORITO	11		1 1	Number of BC		
	Tri-state Output(	IOL=3.2	mA) &	Schmitt	Trigger			Trumber of bo		
	Input Buffer(TTL					sistano	e			
HBRU	w/ Pull-up Resist			•				13		
Cell Symbo			Pro	pagation	Delay P	aramete	r			
			up		tdn					
		t0	KCL	t0	KCL	KCL2	CDR2			
		2.24 0.16 3.72 0.13					1	X → IN		
			3.12 0.056 5.66 0.13				1	OT → X		
	1	(7.88)		(16.71	7		}	1		
IN -	IN ————————————————————————————————————									
ОТ	$rac{1}{\sqrt{1+rac}}$									
01										
			1							
	1									
	C									
				1						
			L +			$Z \rightarrow L$				
		t0		KCL	t0		CL	c → x		
1		2.2	- 1		6.47		13	1		
		(16.4	4)	*	(17.52	)				
		1						1		
<b>}</b>	Input Loading	1								
Pin Name	Factor (lu)									
OT	2	1								
C	2	<b> </b>	H →	7.		$Z \rightarrow H$		-1		
		to KCL to I				CL	_			
		3.0	7		3.20	0.	056	7		
	Output Driving	(16.4	4)	*	(17.52	)		1		
Pin Name	Factor (lu)				i .			1		
IN	18	1	- 1					1		
1		1	- 1							
i	1	l	- 1		l	l l		ı		

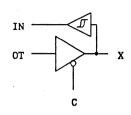




- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

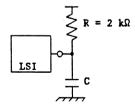
UHB-H8RU-E2 | Sheet 1/1

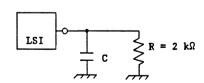
FUJITSU	CMOS GATE ARRAY	JNIT CEL	L SPECI	FICATION			"UH	B" Version	
Cell Name	Function							Number of BC	
H8RD	Tri-state Output(IOL=3.2mA) & Schmitt Trigger Input Buffer(TTL Type, True) w/ Noise Limit Resistance H8RD w/ Pull-down Resistance 13								
Cell Symbo		Stance	Prop	agation	Delay P	aramete	r	13	
		t	up		tdn				
tO   KCL   tO   KCL   KCL2   CDR								Path	



t0	KCL	t0	KCL	KCL2	CDR2	Path
2.24	0.16	3.72	0.13			X → IN
3.12	0.056	5.66	0.13			OT → X
(7.88)		(16.71)	)			
	ł		1			
			]			
		Ì				
		1				
	1	}				
		i				
	l	1				
	<u>L:</u>	<u></u>	L	<u> </u>		
	L +			$Z \rightarrow L$		
t0		KCL ·	t0		CL	C → X
2.2		1	6.47		13	
(16.4	4)	*	(17.52	)		

	Input Loading				
Pin Name	Factor (lu)				
OT	2				
C	2	Н	→ Z	Z	→ H
		t0	KCL	t0	KCL
		3.07		3.20	0.056
	Output Driving	(16.44)	*	(17.52)	
Pin Name	Factor (lu)				
IN	18			1	
	1			1	





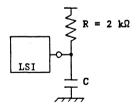
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

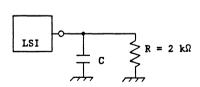
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8RD-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL	SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
н6тғ	Tri-state Output	(IOL=8mA)						8
Cell Symbol				agation	Delay Pa	aramete	r	
		tup			tdn			
			KCL	t0	KCL	KCL2	CDR2	
			.04	1.84				X + IN
			.056	3.27			]	OT → X
	/	(7.27)		(8.63	기			
IN ——	—< h ∣	1			1			
	/ 7						l	
от —	x —						1	
01	√ ".				1		]	
				l			1	
	1			1			ĺ	
	C			İ	1 1		1	
				1		•		
			$L \rightarrow 2$			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.29			3.35		063	
		(18.62)		*	(8.71	)		
			1			- 1		
	T		- 1					
Din Name	Input Loading					- 1		
Pin Name OT	Factor (lu)		1					
C	2		<u> </u>	,		$Z \rightarrow H$		-
U	1	t0	<del></del>	KCL	t0		CL	-
		3.12	$\dashv$	VOD	2.37		056	4
	Output Driving	(18.62)		*	(8.71			
Pin Name	Factor (lu)	(23.32)	- 1		(3.72	´		
IN	36		ı			1		<b>!</b>
			ı			1		
			-			- 1		1
		ŀ	- 1					

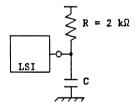


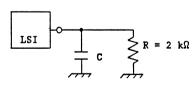


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6TF-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		"บ		" Version
Cell Name	Function							Nı	umber of BC
	Tri-state Output			nput Buf	fer (Tru	e)			
H6TFU	with Pull-up Res	istance							8
Cell Symbol			Pro	pagation	Delay P	aramete	r		
		t	up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		1.06	0.04	1.84					$X \rightarrow IN$
		2.51	0.056	3.27			l	- 1	$OT \rightarrow X$
	_	(7.27)		(8.63)				- 1	
IN —	<b>─</b> < h.							- 1	
2.11				İ			l		
							1		
от —	<b>x</b>			1				i	
	V			1			1		
				1	1		1	- 1	
	<u>'</u>				1				
	C .							- 1	
					1		<u> </u>	_	
	•		L +	KCL	t0	$Z \rightarrow L$	CL	$\dashv$	C → X
		t0 2.2	<del>.  </del>	KCT	3.35		063	$\dashv$	U → X
			-	*	(8.71		003		
		(18.6	2)		(0.71	'		- 1	
								-	
	Input Loading								
Pin Name	Factor (lu)		l						
OT	4								
C	2	ļ	H +	7		$Z \rightarrow H$		-	
J		t0	<del></del>	KCL	t0		CL	-	
		3.1	2		2.37		056	-	
	Output Driving	(18.6		*	(8.71			ı	
Pin Name	Factor (lu)	`	-/		,,,,,,	´			
IN	36	1	- 1						
			1			1			
		1	1			1			
		l	i						

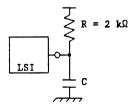


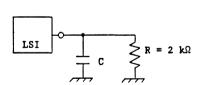


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\text{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6TFU-E1 | Sheet 1/1

FULLTSU (	CMOS GATE ARRAY U	NIT CELL SE	FCIFICATIO	IN .	т	"IIHR	" Version
	Function	MII ODDD DI	BOIL TOWLIG				umber of BC
	Tri-state Output	(IOI.=8mA) 8	Input Buf	fer (True)		<del>-   '</del>	umber or bo
H6TFD	with Pull-down R		Input Dui	101 (1100)		- 1	8
Cell Symbol	WICH IGII GOWN A	F	ropagation	Delay Par	ameter		
0011 03001		tup	Topagation	tdn	uover		
		to KC	L to		KCL2 C	DR2	Path
		1.06 0.0					X + IN
		2.51 0.0					OT → X
		(7.27)	(8.63	1 1	1		
	1	( )	( )	1 1	ł		
IN —					i		
I							
от —	> <b>x</b>		1				
	7		į				
·			{				
	I	i i	1				
	C	1 1	- [				
			į		1		
		L	→ Z	7	: + L		
		t0	KCL	t0	KCL	,	C → X
		2.29		3.35	0.06	3	
		(18.62)	*	(8.71)	ı		
				1			
			1	1			
	Input Loading						į
Pin Name	Factor (lu)			1			
TO	4			L			
C	2		→ Z		: → H		
		t0	KCL	t0	KCI		
		3.12	1 .	2.37	0.05	6	
	Output Driving	(18.62)	*	(8.71)			
Pin Name	Factor (lu)			1			
IN	36		1	1	1		
			i	L	1		

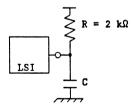


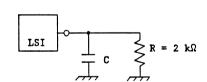


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6TFD-E1 | Sheet 1/1

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1			B" Version
Cell Name	Function							Number of BC
ĺ	Tri-state Output						1	
H6CF	& CMOS Interface	Input						8
Cell Symbol			Propagation Delay Parameter					
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33	0.04		1	X → IN
		2.51	0.056	3.27	0.063			OT → X
	,	(7.27)		(8.63)	)		l	
IN	<b>-</b> ∕						l	
111	$\mathcal{N}$						l	1
					1 1		l	
OT -	<b>X</b>						l	1
Į	7				1		1	
							i	
	C						l	i
				]				
			$L \rightarrow 2$			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.2			3.35		.063	
		(18.6	2)	*	(8.71	)		
						- 1		
			- 1			- 1		
	Input Loading		- 1			- 1		
Pin Name	Factor (lu)							1
OT	4							4
С	2		H → 2			Z → H		4
		t0		KCL	t0		CL	4
	1	3.1		*	2.37		056	1
D4- N	Output Driving	(18.6	2)	*	(8.71	,		1
Pin Name	Factor (lu)		İ			- 1		
IN	36					- 1		
		I		1				
		Į.	- 1	i		- 1		





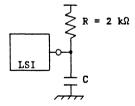
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

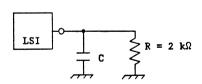
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6CF-E1 | Sheet 1/1 | Page 20-96

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N		"บา	HB" Version
Cell Name	Function			·				Number of BC
	Tri-state Output				rface In	put Buf	fer	
H6CFU	(True) with Pull	-up Res						8
Cell Symbol			Prop	agation	Delay P	aramete	r	
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		0.92	0.04	1.33				X → IN
		2.51	0.056	3.27				OT → X
	1	(7.27)		(8.63	ባ l			
IN	<b>-</b> < h ∣				1 1			1
1	7			l			l	
ОТ —	<b>X</b>							
0.1	<b>^</b>							
•				Ì	1 1			
				<u> </u>				İ
	С	1 1						1
			L → 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	c → x
		2.2			3.35		0.063	
		(18.6	2)	*	(8.71	)		
			1			-		
	1	l				ł		
Pin Name	Input Loading Factor (lu)	l						
OT	Factor (ku)	ł	ŀ			- 1		
C	2		H → 2	,		$Z \rightarrow H$		_
·	1	t0		KCL	t0		CL	
		3.1	2	МОП	2.37		056	-
	Output Driving	(18.6		*	(8.71			
Pin Name	Factor (lu)	`	-´		(3.72	´		
IN	36	1	- 1					
		1						
			- 1			1		1
	I	ŀ	Į.					

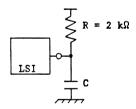


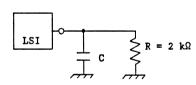


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6CFU-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATION	N		T "U	нв'	'Version
Cell Name	Function								umber of BC
	Tri-state Output	(IOL=8m	A) & Ch	OS Inter	rface In	put Buf	fer		
H6CFD	(True) with Pull				•	•			8
Cell Symbol			Prop	agation	Delay P.	aramete	r		***************************************
		tı	ир	T	tdn			T	
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.92	0.04	1.33	0.04			1	X → IN
		2.51	0.056	3.27	0.063			-	OT → X
		(7.27)		(8.63)				ı	
		1 1		` '				- 1	
IN —									
	$\setminus$ 1				1			- 1	
от —	> x				1		1	- 1	
	√ ·			į			1	1	
					1		1		
				ł	1		l	1	
	С								
	U								
			L + 2	, ,		$Z \rightarrow L$	L	-	
		t0	<u> </u>	KCL	t0		CL	ᅱ	c → x
		2.2	<del>.   -</del>	VOT.	3.35		.063	$\dashv$	C - A
				*	(8.71		.003	'	
		(18.6	<sup>2</sup> )	•	(0.71	'		ı	
						- 1		- 1	
						- 1		- [	
<b>5.</b>	Input Loading							- 1	
Pin Name	Factor (lu)					- 1		- 1	
OT	4							_	
С	2		H → 2			$Z \rightarrow H$		_	
		t0		KCL	t0		CL	_	
		3.1			2.37		056	- 1	
	Output Driving	(18.6	2)	*	(8.71	)			
Pin Name	Factor (lu)		1						
IN	36					- 1			
		ĺ							
			1						
	1	l	- 1	1		1		- 1	





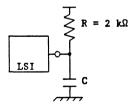
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

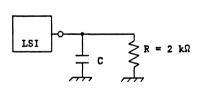
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6CFD-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	N		ี "บ	HB" Version
Cell Name	Function						Ť	Number of BC
	Tri-state Output	(IOL=8m	A) with	h Noise I	Limit Res	sistanc	e	
H8TF	& Input Buffer (							9
Cell Symbol			Pro	pagation	Delay Pa	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	
		1.06	0.04	1.84				X → IN
		3.21	0.056	5.96	0.070			OT + X
	4	(7.97)		(11.91)				ł
IN	<u> </u>						ł	
111	, 7				1 1		1	
							l	
ОТ	<b>→</b> x			1			l	
	Y			1	1 1			
					1 1			
	ı			1	1 1			1
	C			1	1 1		l	
				1				
			L → :			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.6	2		6.82	0.	070	
		(19.7	1)	*	(12.77	)		İ
			1	j				1
			1			1		1
	Input Loading		1					
Pin Name	Factor (lu)					- 1		ı
OT	2							
С	2		H -	Z		Z + H		
		t0		KCL	t0	K	CL	
	<u> </u>	3.3			3.21		056	
	Output Driving	(19.7	1)	*	(12.77	)		1
Pin Name	Factor (lu)							1
IN	36					1		
						- 1		
			- 1			1		
	1	1				- 1		

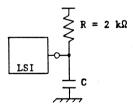


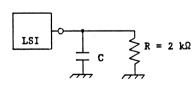


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8TF-E1 | Sheet 1/1

Number   Function   Number   Tri-state Output(IOL=8mA) with Noise Limit Resistance   R8TFU   & Input Buffer (True) with Pull-up Resistance	mber of BC 9 Path
H8TFU & Input Buffer (True) with Pull-up Resistance	
Cell Symbol         Propagation Delay Parameter           tup         tdn         tdn         tdn         tdn         tD         tCL         tCL         CDR2         CDR2           1.06         0.04         1.84         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04         0.04	
tup         tdn           t0         KCL         t0         KCL         KCL2         CDR2           1.06         0.04         1.84         0.04	Path
tup         tdn           t0         KCL         t0         KCL         KCL2         CDR2           1.06         0.04         1.84         0.04	Path
t0 KCL t0 KCL KCL2 CDR2 1.06 0.04 1.84 0.04	Path
1 = 1	Iacii
1 2 21 10 056   5 06 10 070   1	X → IN
3.21   0.030   3.30   0.070	$OT \rightarrow X$
(7.97) (11.91)	
·" , \lambda	
OT — X	
'	
C	
$L \to Z \qquad Z \to L$	
tO KCL tO KCL	$C \rightarrow X$
2.62   6.82   0.070   (12.77)	
(19.71)   * (12.77)	
Input Loading	
OT 2	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	
OT 2 2	
OT 2	
OT 2	
OT 2	

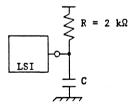


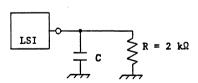


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\text{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8TFU-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N N		T "UH	B" Version
	Function						1 1	Number of BC
	Tri-state Output	(IOL=8m/	A) with	Noise	Limit Res	sistanc	е	
H8TFD	& Input Buffer (						-	9
Cell Symbol					Delay Pa		r	<u> </u>
		tı	ıp	I .	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X → IN
		3.21	0.056	5.96	0.070			OT → X
	4	(7.97)		(11.91	)			1
IN				· .			1	1
IN		1					1	
į		]					1	
OT —	<b>→</b> x							İ
!	$\sim$				1 1		1	1
				ĺ	1 1		l	
	1	1		ļ	1 i		1	1
	C	l i		l	1 1		l	
				<u> </u>			<u> </u>	
			$L \rightarrow Z$			$Z \rightarrow L$		٠
		t0		KCL	t0		CL	c → x
		2.6			6.82		070	
	•	(19.7	1)	*	(12.77)	)		
		1						
	T	1						
<b>5.</b>	Input Loading	l	1					
Pin Name	Factor (lu)	1						
TO	2	ļ						_
С	2		H → 2			Z → H		4
		t0		KCL	t0		CL	4
	1 D 1 1 D 1 1 1	3.3		*	3.21		056	
Die Need	Output Driving	(19.7	1)	*	(12.77)	'		
Pin Name IN	Factor (lu)	ł	1			- 1		
IN	30					- 1		
			- 1			1		
		1				1		
	1	I	- 1		l	ı		

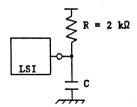


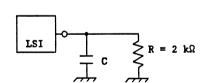


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8TFD-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	Ň		" UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=8m	A) wi	th Noise	Limit Re	sistanc		
H8CF	& CMOS Interface							9
Cell Symbol		I	Pr	opagation	Delay P	aramete	r	***************************************
		t	up	1	tdn			1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04		1	X + IN
		3.21	0.05	6 5.96	0.070		l	OT + X
		(7.97)		(11.91			1.	
		( , , , ,		,	1		l	
IN —	$\overline{}$			I	1	1	1	
	<u> </u>			l	1		l	1
от —	>→ x			1			l	
	<b>√</b> "	l i		ļ			l	1
		1		1			ł	
	1			1			į	
	С			į.	1.	Ì	Ì	
				l	1			
			L →	Z		$Z \rightarrow L$	A	
		t0	_ <u>_</u>	KCL	t0		CL	¬ с + х
Ĭ		2.6	2		6.82		0.070	7
		(19.7		*	(12.77	)		
		,,,,,,,	-'		,	´		
			- 1					
	Input Loading	1						1
Pin Name	Factor (lu)	l	1			l		1
OT	2	1	1			-		1
C	2		H →	Z		$Z \rightarrow H$		
		t0		KCL	t0		CL	7
		3.3	0		3.21	0.	.056	7
	Output Driving	(19.7		*	(12.77	)   <u> </u>		
Pin Name	Factor (lu)	,			•			
IN	36	1	- 1			1		
l			- 1			1		
			- 1			- 1		
l	1		- 1					

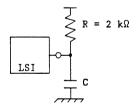


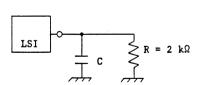


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8CF-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	<u></u>		пп.	B" Version
Cell Name	Function							Number of BC
	Tri-state Output(	IOL=8mA	) w/ No	ise Lim	it Resis	tance &		
H8CFU	CMOS Interface In	put Buf	fer (Tr	ue) w/ 1	Pull-up	Resista	nce	9
Cell Symbo	1				Delay P			
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33	1 :		ļ	X → IN
		3.21	0.056	5.96				OT → X
	1	(7.97)		(11.91)	)			
IN -	<b>─</b> < h			1			i	
1	~ ~			1				
от	- x			1				1
"	^							
								1
	С			1	1			
	-			1				I
			L + 2	2		$Z \rightarrow L$		
		t0		KCL	t0		CL	_ c → x
		2.6			6.82		.070	
		(19.7	1)	*	(12.77	)		
1		1				1		1
			i					
D/- 33	Input Loading					1		
Pin Name OT	Factor (lu)							
C	2 2	<b> </b>	H → Z	,		$Z \rightarrow H$		
١		to	n 7 2	KCL	t0		CL	$\dashv$
1		3.3	${\circ}$	YOT	3.21		056	┥
<del> </del>	Output Driving	(19.7	1	*	(12.77		550	
Pin Name	Factor (lu)	(	-/		(//	<b>′</b>		1
IN	36	1	l					
			Ì					
		(						
	1	1	- 1					1

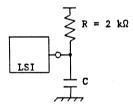


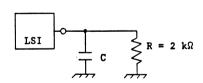


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8CFU-E1 | Sheet 1/1

FILITCII	TSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version							
	Function	WII CLL	J SILC.	ITICATIO	<u> </u>			Number of BC
	Tri-state Output(	TOL=8mA	) w/ No	nise Lim	it Resist	tance &		INTERPORT OF BO
	CMOS Interface In							9
Cell Symbol				pagation				
		tı	up	T	tdn			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
·		0.92	0.04	1.33	0.04			X → IN
		3.21	0.056					OT → X
		(7.97)		(11.91)				
IN —	<b>-</b> √ h — 1							
	, 71 1			1				
				1				
ОТ —	x			l				1
	С			1	1			
							ĺ	
			L +	z I		Z + L		
		t0		KCL	t0	K	CL	c → x
		2.6			6.82		.070	7
		(19.7	1)	*	(12.77	)		
			- 1					
						- 1		
	Input Loading					- 1		
Pin Name	Factor (lu)		- 1			1		
OT C	2 2	ļ	H → 1	,		$Z \rightarrow H$		-
'	2	t0		KCL	t0		CL	-
		3.3	${}$	VOD	3.21		056	-
<del> </del>	Output Driving	(19.7		*	(12.77			
Pin Name	Factor (lu)	(2)./	-/		(	´		
IN	36	1	i			- 1		
1			1			1		1
,		1						
		1						





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8CFD-E1 | Sheet 1/1

	CMOS GATE ARRAY U	TE ARRAY UNIT CELL SPECIFICATION "UHB" Version						
Cell Name	Function							Number of BC
IT10	Input Buffer for	Oscill	ator Ci	rcuit				0
Cell Symbol			Prop	agation	Delay		ter	
			up		td		.,	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0	0	0	0		1	X → IN
							1	
							i	
	_							
х	>— IN							
		'					1	
		Parame	+	L		<u> </u>	Symbol	Typ(ns)*
		rarame	rei				БУШБОТ	Typ(IIS)"
						-		
						l		
						- 1		
	T					- 1		
Dim Nama	Input Loading					1		
Pin Name	Factor (lu)					- [		
						- 1		
						- 1		
	Output Driving					- 1		
Pin Name	Factor (lu)							
		* M:-:	1	,,,, f	. +ho +	mical	anare+	ing condition
								ing condition. ng condition
					aximum			
	_L	1 016	011011 1	, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	·~************************************			

This cell if for the oscillator circuit only. Please refer to the document Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit GATI0281 $\Delta$  for the details.

UHB-IT10-E1 | Sheet 1/1

Cell Name	FUJITSU	CMOS GATE ARRAY U	ATE ARRAY UNIT CELL SPECIFICATION "UHB" Version							
HOC		Function								
Propagation Delay Parameter   tup   tdn   t0   KCL   t0   KCL   CDR2   Path   0.92   0.04   1.33   0.04   X → IN		Output Buffer for	r Oscil	lator						
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		with CMOS Interf	ace Inp							88
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Cell Symbol				agation			eter		
0.92 0.04 1.33 0.04 X → IN  OTX										
INX							KC:	L2	CDR2	
от — х			0.92	0.04	1.33	0.04		- 1		$X \rightarrow 1N$
от — х								- 1		
от — х								- 1		
от — х										
от — х										
	IN	<b>-</b> < h ∣						- 1		
		N 7								
	от —	>∞↓_x						- 1		
								- 1		İ
								- 1		
				}		}		- 1		
Parameter Symbol Typ(ns)*			Parame	ter				Sym	bol	Typ(ns)*
							ı			
		T 7 7 11					- 1			
Input Loading	Dia Nama						j			1
Pin Name Factor (lu)	Pin Name	Factor (ku)					1			
							- 1			}
							ļ			}
Output Driving		Output Driving								
Pin Name Factor (lu)	Pin Name									
IN 36			1				- }			1
* Minimum values for the typical operating condition.			* Mini	mum val	ues for	the typ	ical	ope	rati	ng condition.
The values for the worst case operating condition										
are given by the maximum delay multiplier.			are	given b	y the ma	ximum d	elay	mu1	tipl	ier.

This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281 $\Delta$ )" for the details.

UHB-HOC-E1 | Sheet 1/1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	***************************************			"UHB	" Version
Cell Name	Function								umber of BC
	Output Buffer for							T	
HOS	with Schmitt Tri	gger In							8
Cell Symbol				agation			ter		
			up		tdn		<u> </u>	220	n . 1
		t0	KCL	t0	KCL	KCL	2 C	DR2	Path
		2.48	0.16	3.08	0.10				X → IN
							- 1		
IN	$\pi$						- 1		
IN	~~~\						- 1		
ĺ							-		
от —	>> <del></del>								
			l	1			1		
		Parame	ter	L		$\Box$	Symb	01	Typ(ns)*
						- 1			
						- 1			İ
						1			
<b>5.</b>	Input Loading					- 1			
Pin Name	Factor (lu)								
									1
	Output Driving								
Pin Name	Factor (lu)					- [			1
IN	18					- 1			
									L
		* Mini	mum val	ues for	the tvo	ical	oper	atir	g condition.
		The values for the worst case operating condition are given by the maximum delay multiplier.							
			are given by the maximum delay multiplier.						

This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281 $\Delta$ )" for the details.

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			<u>"U</u>	нв"		on
Cell Name	Function							Nu.	_£ C	of BC
	Output Buffer for									
HOCR	w/ CMOS Interfac	e Input							8	
Cell Symbol			Prop	agation	Delay P	aramete	r			
			up		tdn					
		t0	KCL	t0	KCL	KCL2	CDR	2	Path	
		0.92	0.04	1.33	0.04				X →	IN
			l							
IN —	<b>─</b> < h		1							
	N 1		ļ							
от —	>→ x									
0.			ļ							
					İ					
			<u> </u>		<u> </u>	Ĺ	L			
		Parame	ter			Sy	mbol	_ _	Typ(r	ns)*
						i				
								ļ		
						l				
	1					İ				
<b></b>	Input Loading									
Pin Name	Factor (lu)					- 1				
						- 1				
	1									
								- 1		
	<del> </del>							- 1		
B	Output Driving					- 1				
Pin Name	Factor (lu)	1								
IN	36							L_		
	1	. بيديد		<b>.</b>	41. 4-	1			•	141-
				ues for						
		The values for the worst case operating condition are given by the maximum delay multiplier.								
		are	given t	y the ma	XIMUM C	ielay mu	1111	rier	•	

This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281 $\Delta$ )" for the details.

# **APPENDIX A: General AC Specifications**

Simulation Delay Specifications (Recommended Operating Conditions, Ta = 0 to 70°C, VDD =  $5V\pm5\%$ 

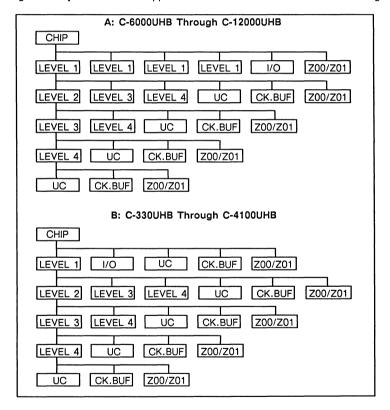
Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	1.65
Post-layout Simulation	0.40	1.60

# **APPENDIX B: Hierarchical Structure**

Hierarchical blocks (or Functional Logic Blocks) within other hierarchical blocks are user-defined groups of cells laid out in close proximity to each other in both X and Y dimensions of the array.

The hierarchical method of design allows circuit sections to be placed within the array at positions relative to each other. This is made possible by the designer's defining and placing functional logic blocks within the hierarchy and thus controlling path lengths.

There are five levels of hierarchy, also referred to as Functional Logic Blocks (FLBs). Certain design rules regarding what may and what must appear at certain levels are condensed in the diagram below.



Use of the hierarchical design method is mandatory for partitioned arrays and optional for non-partitioned arrays. Section A of the figure above addresses partitioned arrays C-6000UHB through C-12000UHB. Section B of the figure above addresses non-partitioned arrays C330UHB through C4100UHB. Immediately below the chip level, four Level 1 (FLB1) blocks must be defined, giving identity to each of the four partitioned quadrants of the array.

# **APPENDIX B: Hierarchical Structure (Continued)**

All I/O buffers and their associated circuitry must be defined immediately beneath the chip level with the FLB1 blocks. Nothing but I/O buffers may be so defined. If pull-up or pull-down cells (A01s or X00s) are required for unused inputs of the I/O buffers, they must also be defined at this level. Unit cells (UC) may be defined at each level.

For optimum delay characteristics, Level 2 blocks should be defined under each of the Level 1 blocks, Level 3 Blocks under Level 2 blocks, and so on. Unit cells should be defined under Level 4.

# **APPENDIX C: Estimation Tables for Metal Loading**

## C-330UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4 5 6 7 8	1.0 2.2 3.0 3.5 3.9 4.2 4.6 4.8 4.9	10 11 12 13 14 15 16–30 31–50 51–75 76–100	5.0 5.1 5.2 5.3 5.3 5.7 6.6 6.7 7.4

## C-530UHB

NDI	CL(ℓu)	NDI	CL(lu)
1 2 3 4 5 6 7 8 9	1.1 2.5 3.4 3.9 4.4 4.7 5.1 5.4 5.5	10 11 12 13 14 15 16–30 31–50 51–75 76–100	5.6 5.7 5.8 5.9 5.9 6.4 7.4 7.5 8.3

#### C-830UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4 5 6 7 8 9	1.3 3.0 4.0 4.7 5.2 5.6 6.1 6.4 6.6	10 11 12 13 14 15 16–30 31–50 51–75 76–100	6.7 6.8 6.9 7.1 7.1 7.7 8.8 9.0 9.9

## C-1200UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4 5 6 7 8 9	1.7 3.6 4.9 5.7 6.3 6.8 7.4 7.8 8.0	10 11 12 13 14 15 16–30 31–50 51–75 76–100	8.2 8.3 8.4 8.6 9.3 10.6 10.9

# C-1700UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4	1.8 3.9 5.3 6.2	10 11 12 13 14	8.8 8.8 9.0 9.1
5 6 7 8 9	6.8 7.4 8.1 8.4 8.6	14 15 16–30 31–50 51–75 76–100	9.3 9.3 10.1 11.5 11.8 13.0
I		1,0,100	1 .0.0

# APPENDIX C: Estimation Tables for Metal Loading (Continued)

#### C-2200UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4 5 6 7 8	2.2 4.7 6.4 7.4 8.2 8.9 9.7 10.1	10 11 12 13 14 15 16–30 31–50 51–75 76–100	10.7 10.7 10.8 10.9 11.2 11.2 12.1 13.9 14.3 15.7

#### C-3000UHB

NDI	CL(ℓu)		IDI	CL(ℓu)
1 2 3 4 5 6 7	2.6 5.7 7.7 9.0 10.0 10.8 11.8	16	10 11 12 13 14 15 3–30	12.9 12.9 13.1 13.2 13.6 13.6 14.7
8 9	12.3 12.6	5	1-50 1-75 3-100	16.8 17.3 19.0

#### C-4100UHB

NDI	CL(ℓu)	NDI	CL(ℓu)
1	3.0	10	14.8
2	6.6	11	14.8
3	8.8	12	15.0
4	10.3	13	15.2
5	11.4	14	15.5
6	12.4	15	15.5
7	13.5	16-30	16.8
8	14.0	31-50	19.3
9	14.4	51-75	19.8
		76–100	21.8

#### C-6000UHB (Within Block)

NDI	CL(ℓu)	NDI	CL(ℓu)
1	1.6	10	7.9
2	3.5	11	7.9
3	4.7	12	8.0
2 3 4	5.5	13	8.2
5	6.1	14	8.4
6	6.6	15	8.4
7	7.2	16-30	9.1
8	7.5	31-50	10.4
9	7.7	51-75	10.6
		76–100	11.7

#### C-6000UHB (Inter-Block)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 2 3 4 5 6 7 8 9	3.5 7.6 10.2 12.0 13.3 14.4 15.7 16.3 16.8	10 11 12 13 14 15 16–3 31–5 51–7 76–1	0 22.4 5 23.0

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

# APPENDIX C: Estimation Tables for Metal Loading (Continued)

#### C-8700UHB (Within Block)

NDI	CL( ℓ u)	NDI	CL( ℓ u)
1 2 3 4 5 6 7 8 9	2.2 4.7 6.4 7.4 8.2 8.9 9.7 10.1	10 11 12 13 14 15 16–30 31–50 51–75 76–100	10.7 10.7 10.8 10.9 11.2 11.2 12.1 13.9 14.3 15.7

#### C-8700UHB (Inter-Block)

NDI	CL(ℓu)		NDI	CL(ℓu)
1	4.2		10	20.8
2	9.2	П	11	20.8
3	12.4	П	12	21.0
4	14.5	H	13	21.3
5	16.0		14	21.8
6	17.3	П	15	21.8
7	18.9	ı	16-30	23.6
8	19.7		31-50	27.1
9	20.2		51-75	27.8
			76–100	30.5

#### C-12000UHB (Within Block)

2.6	CL( lu)	NDI	Г	NDI	CL(ℓu)
	2.6			NO	OL( vu)
7.7 9.0	5.7 7.7 9.0	1 2 3 4		10 11 12 13	12.9 12.9 13.1 13.2 13.6
0.8 1.8 2.3	10.0 10.8 11.8 12.3 12.6	6 7 8 9		15 16–30 31–50 51–75	13.6 13.6 14.7 16.8 17.3
0.8 1.8 2.3	11.8 12.3	7 8		16–30 31–50	13 14 16 17

## C-12000UHB (Inter-Block)

NDI	CL(ℓu)		NDI	CL(ℓu)
1 1	4.9		10	24.3
2	10.8		11	24.3
3	14.5		12	24.6
5	17.0 18.8		13 14	25.0 25.6
6	20.3	П	15	25.6 25.6
7	22.2		16-30	27.7
l à	23.1		31-50	31.7
9	23.7	ľ	51-75	32.6
			76–100	35.8

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

### APPENDIX C: Estimation Tables for Metal Loading for Clock Nets

#### C-330UHB (for CK20, CK40)

NDI	CL(ℓu)		NDI	CL(ℓu)
1 – 2	5.1		11 – 12	12.7
3 – 4	9.5		13 - 15	13.0
5 – 6	11.9	l	16 - 30	13.3
7 – 8	12.2		31 - 50	15.4
9 – 10	12.4		51 - 80	18.1

#### C-330UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	7.0	11 - 12	
3 - 4	13.4	13 - 15	
5 - 6	16.7	16 - 30	
7 - 8	17.0	31 - 50	
9 - 10	17.3	51 - 80	

#### C-530UHB (for CK20, CK40)

NDI	CL(lu)		NDI	CL(ℓu)
1 – 2	5.1		11 - 12	14.9
3 – 4	9.6	П	13 - 15	15.1
5 - 6	14.1		16 - 30	15.4
7 – 8	14.4		31 - 50	17.3
9 - 10	14.6		51 - 80	19.8

#### C-530UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2 3 - 4 5 - 6 7 - 8 9 - 10	7.3 14.0 20.7 20.9 21.2	11 - 12 13 - 15 16 - 30 31 - 50 51 - 80	21.7 21.9

#### C-830UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	5.6	11 - 12	
3 - 4	10.5	13 - 15	
5 - 6	15.4	16 - 30	
7 - 8	18.0	31 - 50	
9 - 10	18.2	51 - 80	

#### C-830UHB (for CK60, CK80)

NDI	CL(lu)	NDI	CL(ℓu)
1 - 2 3 - 4 5 - 6	8.1 15.5 22.9	11 - 12 13 - 15 16 - 30	27.3 27.6 27.8
7 – 8	26.7	31 - 50	30.0
9 - 10	27.0	51 - 80	32.8

#### C-1200UHB (for CK20, CK40)

NDI	CL(ℓu)	ND
1 - 2	6.2	11 -
3 - 4	11.7	13 -
5 - 6	17.2	16 -
7 - 8	22.7	31 -
9 - 10	23.0	51 -

NDI	CL(ℓu)
11 - 12 13 - 15 16 - 30 31 - 50	23.3 23.7 24.0 26.3
51 - 80	29.3

#### C-1200UHB (for CK60, CK80)

NDI	CL(lu)	NDI	CL(ℓu)
1 - 2	9.3	11 - 12	36.0
3 - 4	18.0	13 - 15	36.3
5 - 6	26.7	16 - 30	36.6
7 - 8	35.4	31 - 50	38.9
9 - 10	35.7	51 - 80	41.9

### Estimation Tables for Metal Loading for Clock Nets (Continued)

#### C-1700UHB (for CK20, CK40)

NDI	CL(lu)	NDI	CL(ℓu)
1 - 2	6.6	11 - 12	28.0
3 - 4	12.6	13 - 15	28.3
5 - 6	18.6	16 - 30	28.6
7 – 8	24.5	31 - 50	31.0
9 – 10	27.7	51 - 80	34.2

#### C-1700UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)	
1 – 2	10.3	11 – 12	44.4	l
3 – 4	19.9	13 – 15	44.7	ı
5 – 6	29.5	16 – 30	45.0	l
7 – 8	39.1	31 - 50	47.4	l
9 – 10	44.1	51 - 80	50.6	ı

#### C-2200UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	7.1	11 - 12	33.1
3 - 4	13.5	13 - 15	33.4
5 - 6	19.9	16 - 30	33.8
7 - 8	26.3	31 - 50	36.3
9 - 10	32.8	51 - 80	39.6

#### C-2200UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2 3 - 4 5 - 6	11.2 21.8 32.3	11 - 12 13 - 15 16 - 30	54.1 54.4
7 – 8 9 – 10	42.8 53.4	31 - 50 51 - 80	56.9 60.2

#### C-3000UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 – 2	7.7	11 - 12	43.0
3 – 4	14.8	13 – 15	43.3
5 - 6	21.8	16 - 30	43.7
7 – 8	28.9	31 - 50	46.3
9 – 10	35.9	51 - 80	49.8

#### C-3000UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	12.6	11 - 12	72.1
3 - 4	24.5	13 - 15	72.4
5 - 6	36.4	16 - 30	72.8
7 - 8	48.3	31 - 50	75.4
9 - 10	60.2	51 - 80	78.9

### C-4100UHB (for CK20, CK40)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2	8.4	11 - 12	47.3
3 – 4	16.2	13 - 15	51.4
5 – 6	24.0	16 - 30	51.7
7 – 8	31.7	31 - 50	54.6
9 – 10	39.5	51 - 80	58.4

#### C-4100UHB (for CK60, CK80)

NDI	CL(ℓu)	NDI	CL(ℓu)
1 - 2 3 - 4 5 - 6 7 - 8 9 - 10	14.0 27.4 40.7 54.1 67.4	11 - 12 13 - 15 16 - 30 31 - 50 51 - 80	87.6 88.0

### Estimation Tables for Metal Loading for Clock Nets (Continued)

#### C-6000UHB (for CK20, CK40)

NDI	CL(ℓu)
1	9.9
2	14.9
3	24.1
4	29.2

#### C-6000UHB (for CK60, CK80)

NDI	CL(ℓu)
1	13.2
2	24.8
3	37.3
4	48.9

#### C-8700UHB (for CK20, CK40)

NDI	CL(ℓu)
1	11.8
2	17.8
3	28.9
4	34.9

### C-8700UHB (for CK60, CK80)

NDI	CL(ℓu)
1	15.7
2	29.7
3	44.8
4	58.7

#### C-12000UHB (for CK20, CK40)

NDI	CL(ℓu)
1	13.7
2	20.7
3	33.7
4	40.8

#### C-12000UHB (for CK60, CK80)

NDI	CL(ℓu)
1	18.3
2	34.7
3	52.3
4	68.7

## **APPENDIX D: Available Package Types**

# UHB CMOS Available Package Types Plastic

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-12000 UHB
DIP											
Standard	(100 mil	pin pitc	h)								
16 DIP	•	_		_			_	_		_	_
18 DIP	CH		-	_	_					_	
20 DIP	•	•	_		_	_	_	_	_		
22 DIP 24 DIP	•	:	•	•	•	-	_		_		-
28 DIP	:	:		•		:	•	•	_		_
40 DIP	•	•	•	•	•	•	•	•	•	СН	
42 DIP	•	•	•	•	•	•	•	•	•	СН	-
48 DIP	•	•	•	•	•	•	•	•	•	CH	_
Shrink	(70 mil p	in pitch	)								
28 SHDIP	•	•	•	•	•	_	_	_	_	-	_
42 SHDIP	•	•	•	•	•	•	•	•	•		_
48 SHDIP 64 SHDIP	•	:	:	•	•	•	•	•	•	CH	_
	/200 mil		4	•	•	•	•	•	•	СП	
Skinny	(300 mil	wide bo	uy)								
22 SKDIP 24 SKDIP	СН	СН	_	_		_	_	_	_	_	_
28 SKDIP	NW	NW	_			_	_	_	_	_	_
FPT											
	(leads on				***************************************						
16 FPT	•	СН	СН	СН	_	_	_	-	_	_	-
20 FPT	•	СН	СН	CH	_		_	_		_	_
24 FPT 28 FPT	:	:	:	•				_	_		-
20111	(leads on		oldoo)								
44 FPT	(leads of	all lour	sides)		•	_	_	_		_	
48 FPT	•	•	•	•	•	•	•	_	_	_	_
48 FPT-S*	•	•	•	•	•	_	_				
64 FPT	•	•	•	•	•	•	•	•	•	CH	_
80 FPT		•	•	•	•	•	•	•	•		_
100 FPT	_	_	•	•	•	•	•	•	•	_	_
120 FPT 160 FPT		_		•	•	•	•	•	•	:	
100171	*smaller	than the	other 48	— —pin FP1			•	•	•	•	
PLCC											
28 PLCC	•	•	•	•	•	•	•		_	_	
44 PLCC	•	•	•	•	•	•	•	CH	CH	- CP	
68 PLCC 84 PLCC	•	•	•	•	•	:	:	:	:	CH CH	CH CH
PPGA					•	•	•		•		
FFGA	100 mil p	oin pitch	1)								
64 PGA	•	•	•	•	•	•	•	•	•	•	_
88 PGA	_	•	•	•	•	•	•	•	•	•	_
135 PGA		_		_	_	_	•	•	•	•	
NOTES:											
• : Av	ailable										
	t Available										
	der Develo										
	ewly Availab		nackaca	hae shan	al ban	hecome !!	navailable				
CH : In	ie availabilit	y OI IIIB	package	nas cnan	you, 1.8.,	Decorrie ul	iavallable				
L											

## APPENDIX D: Available Package Types (Continued)

# UHB CMOS Available Package Types Ceramic

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-12000 UHB
DIP											
Standard	(100 mil	pin pitc	h)								
20 DIP	•	_	_	_	_				_		
22 DIP	•	•	•	_			_			_	_
24 DIP	•	•	•	•	-	•	_	_	_		
28 DIP	•	•	•	•	:	•	_	_		_	
40 DIP 42 DIP	•	•	•	:	:	•	•			_	_
48 DIP	_	_	•	•	•	•	•		_	_	_
Shrink	(70 mil p	in pitch	)								
28 SHDIP	•	•	•	_	_	_	_	_		_	_
42 SHDIP	_	_	_	•	•	•	_		_	_	
FPT											
	(leads on	all four	sides)								
48 FPT			•	•	•	•		_			
80 FPT		_			_	_			_	UD	
100 FPT	_	_		_	•	•		-	-	UD	UD
120 FPT	_		_			_		•	•	•	CH
160 FPT			_			<del></del>	<del></del>	<del></del>	_		UD
LCC											
28 LCC	•	•	•	•		_		_	_	_	_
48 LCC	•	•	•	•	•	•	•	•	-	_	
64 LCC	•	•	•	•	•	•	•	•	•	•	CH
68 LCC 84 LCC	_	•	•	<u>.</u>	•	•	•	•	•	•	CH
PGA											
	100 mil p	oin pitch	<u> </u>								
64 PGA	•	•	" •	•	•	•	•	•	•	•	•
88 PGA		СН	•	•	•	•	•	•	•	•	UD
135 PGA				•	•	•	•	•	•	•	•
179 PGA	_		_	_			NW	NW	NW	•	•
208 PGA	_	_	· —			_	•	NW	NW	NW	NW
256 PGA			_		_	_				•	•
NOTES:				,							
	vailable										
	ot Available										
	nder Develo ewly Availab										
	ewiy Avallab ne avallabilit		nackace	has heen	changed	ie beco	me unavai	ilabie			
J.,	urunubiiit	, 51 1116	Package		J. Idingou,						

## Appendix E: TTL 7400 Function Conversion Table

TTL 7400 Series Name	Function	Fujitsu of	umbe Unit ells
400	Quad 2-input NAND	4 x N2N	4
401	Quad 2-input NAND, Open Collector Outputs		6
402		4 x R2N	4
403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
404		6 x VIN	6
405	Hex Inverter, Open Collector Outputs	R6B	5
406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
407	Hex Buffer, Open Collector Outputs	2 x N3N into R2n	5
408		4 x N2P	8
409	Quad 2-input AND, Open Collector Outputs	N8P	6
410	Triple 3-input NAND	3 x N3N	6
411	Triple 3-input AND	3 x N3P	9
412	Triple 3-NAND, Open Collector Outputs	T33	7
413	Dual 4-Input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
414	Hex Schmitt Trigger Inverter	6 x I1R	48
415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
419	Hex Schmitt Trigger Inverter	6 x I1R	48
420	Dual 4-input NAND	2 x N4N	4
421	Dual 4-input AND	2 x N4P	6
422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
424	Quad Schmitt Trigger 2-Input NAND	8 x I2R + 4 x N2N	68
425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
427	Triple 3-input NOR	3 x R3N	6
428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector		
	Outputs	4 x R2N + N4P	7
7434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
437	Quad 2-input NAND Buffer	4 x N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector		
	Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(
442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
7446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2	P 53
7447	BCD to 7-segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N3	2P 53
448	BCD to 7-segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2	
449	BCD to 7-segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2	
450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5
451	AOI	2 x D24 (LS51 = D24 + T32)	41
452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
453	Expandable 4-wide AOI	D36 + D23 into N2P	7
454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
455	2-wide 4-input AOI	T42	6
460	Dual 4-input Expander	2 x N4P	6
7461	Triple 3-input Expander	3 x N3P	6
7462	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4-2-3-2 AOI	T54	10
7465	4-2-3-2 AOI (Open Collector)	T54	10

### TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset		
	and Clear or:	3 x V1N + 2 x N3N + N2N + R2N + FJD FD4 + 2 x N2N + R2N + V1N + R2P + D24(2)	21 17
7471	AND-gated RS M/S FF with Preset and Clear or:	FD4 + 2 x N3N + 2 x D23 + 2 x V1N LT1+ 2 x N4N + N2P	19 10
7472	AND-gated JK M/S FF with Preset and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
7473	or: Dual JK FF with Clear	FD4 + N3P + N3N + V1N + D24 2 x FJD	17 24
7474	Dual positive-edge D-FF with Preset and	2 X 1 3 D	24
	Clear	2 x FDP	16
7475	4-bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4-bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common Clear and Clock	2 x (FJD + N2N + R2N + V1N)	30
7480	Gated Full Adder	A1N	8
7482 7483	2-bit Binary Full Adder 4-bit Binary Full Adder with Fast Carry	A2N A4H	16 48
7484	4-bit Magnitude Comparator	MC4	40
7486	Quad 2-input XOR	4 x X2N	12
7487	4-bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64-bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4	298
	· · · · · · · · · · · · · · · · · · ·	+ 5 x (V2B + T5A) + 10 x V1B	
7490	Decade Counter	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
	(Different Implementation)	4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8-bit Shift Register	2 x FDS + V1N	41
7492	Divide-by-12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25 34
7494	4-bit Shift Register, 2 asynchronous Presets 4-bit Shift Register, 2 asynchronous Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	34 42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6-bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N + 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B	122
		+ R2B + X2N + 5 x X1B.	
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42 30
74100	8-bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101 74102	AO-gated JK Negative-Edge FF, with Preset AND-gated JK Negative-Edge FF with	FD3 + V1N + 3 × D24	15
74102	Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26
14100	or:	2 x (FD5 + D24 + V1N)	22
74106	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data		
l	Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24

### TTL 7400 Function Conversion Table (Continued)

Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	2 x (FD3 + D24 + V1N)	22
74114	Dual JK Negative-Edge FF with Preset and	,	
	Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4-bit Latch with Clear	2 x.LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3-state Output	B41	9
74126	Quad Bus Buffer with 3-state Output	B41 + 4 x V1N	13
74132	Quad 2-input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133	13-input NAND	2 x N4N + N3N + N2N into R4P	10
74134	12-input NAND with 3-state Outputs	NCB + O4R	15
74135	Quad 3-input EXOR/EXNOR	4 x X4N	20
74136	Quad 2-input EXOR with Open-Collector		
	Outputs	4 x X2N + R4N	14
74137	3-line to 8-line Decoder with Address		
	Latch	3 x LTK Into DE6	42
74138	3-line to 8-line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 x DE4	16
74141	BCD-to-Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD-to-decimal Decoder	4 x V1N + 10 x N4N	24
74147	10-line to 4-line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P	36
74440	O Han to O Han Ontal Bulanky Francis	+ 3 x R2N + R4N + 13 x V1N	40
74148	8-line to 3-line Octal Priority Encoder	N9B + 2 × N2N + R2P + R4N + 4 × N3N	40
74150	1 to 16 Multipleyon	+ 2 × N4N + G44 + 12 × V1N DE3 + 2 × U28 + D24 + 2 × V1N	41
74150	1-to-16 Multiplexer 1-to-8 Multiplexer with Strobe	DE3 + 2 x 026 + D24 + 2 x V IN DE3 + U28 + N2N(1) + V1N	28
74151	1-to-8 Multiplexers	DE3 + U28 + N2N(1) + V1N	26 26
74152	Dual 4-line to 1-line Selector/Multiplexer	DE2 + 2 x U24 + 2 x R2N)	19
74154	4-line to 16-line Decoder/Demultiplexer	2 x DE6( + V1N	61
74154	or:	2 x DE4 + N2P + 16 x R2P	50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 × N3N + 2 × R2N + 5 × V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer (Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1-line multiplexer	T2F + 4 x R2N + B1N	13
74157	Quad 2-line to 1-line multiplexer	12F + 4 X HZN + BIN	13
74130	(Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4-line to 16-line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4-bit Counter	4 x C11 + K1B + 2 x V1B + V1N + B1N+	62
74100	(Decimal with Direct Clear)	N2K + 2 x R3N + R4N + 3 x R2N + N2N	02
74161	Synchronous 4-bit Counter (Binary	142K + 2 X 115K + 114K + 5 X 112K + 142K	
74101	with Direct Clear)	C43	48
74162	Synchronous 4-bit Counter	040	
	(Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4-bit Counter (Binary		
, 4100	with Synchronous Clear)	C45	48
74164	8-bit Parallel Output Serial Shift	0.10	
	Register, Asynchronous Clear	2 x FDR + N2P	54
74165	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	71
74166	8-bit Shift Register	2 x FDR + 8 x D24 + 10 x V1N + K4B	80
74168	4-bit Up/Down Synchronous Counter		
	(Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V1B + K1B	85
74169	4-bit Up/Down Synchronous Counter		
	(Binary)	C47	68
74170	4-by-4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
	Quad D-FF with Clear	FDR + 4 x V1N	30
74171			0.40
74171 74172	16-bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 +	348

### TTL 7400 Function Conversion Table (Continued)

Name	Function		mbei Unit
IVAIIIE	Tunction	Dasic Cells Ce	113
74173	4-bit D-type Register	EDD - A - DOM - D44 - A - MAN - KAD - A - D04	
74474	(3-state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
	Hex D-FF (Single Output)	FDR + 2 x FD0	40
	Quad D-FF (with Clear)	FDR + 4 x V1N	30
	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
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		N6B + N4B + 2 × N2N + 2 × N4P	113
74182	Look-ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
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74184	BCD-to-binary Code Converter	These devices are ROM based	
74185	Binary-to-BCD Code Converter	These devices are ROM based	
74105	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N	
. 4100	Cynicii Oproown Counter (BCD)	+ 9 x N2N + 2 x T32 + T43	
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74132	Op/Down Dual Clock Counter (BCD)	+ T32 + T42 + T43	,,
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	(Internal Pull-up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2F	53
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74000	(Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2F	
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# AV Series CMOS Gate Array Unit Cell Library

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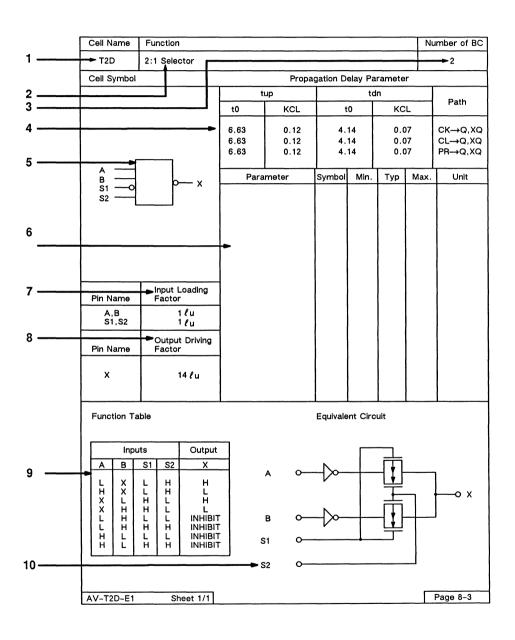
### **Unit Cell Specification Information**

This section contains specifications for all the unit cells available for the AV Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors.

#### How to Read a Unit Cell Specification

The following paragraphs numbered 1-10 explain how the information given in the AV Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit cell name appears in the upper left corner of the page.
- 2. The unit cell Function is given on the same line as the unit cell Name.
- The number of basic cells (BC) or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t0) is given in ns. KCL, the delay constant for the cell (delay time per load unit) is given in ns/pF. KCL2 and CDR2 are a delay constant and an output driving factor provided for some unit cells to calculate delay when a unit cell is loaded beyond its published output driving factor (CDR).
- 5. The cell (logic) symbol is shown in the top left box under the cell name box.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given when applicable in a table directly below the propagation delay parameters.
- 7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- The output driving factor is shown directly under the input loading factor. The output driving factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function (truth) table, if applicable, is shown in a box at the lower left side of the page.
- 10. The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.



## Inverter, Clock Buffer Family

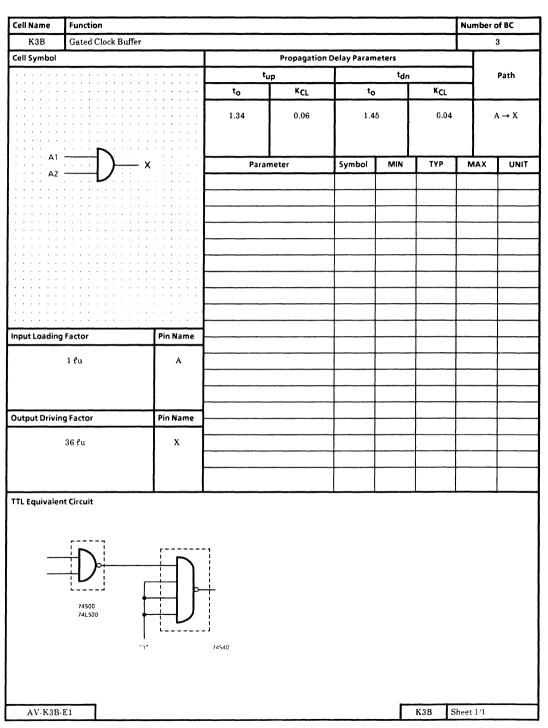
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Cell Name	Function							Number	of BC
VIN	Inverter	•							1
Cell Symbol	<u> </u>		·	Propagation	Delay Param	eters			
			tu	ıρ		tdn			Path
			to	K <sub>CL</sub>	to		KCL		
			0.55	0.25	0.3	0	0.14		A → X
	A	, : : : : <b> -</b>	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
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Output Drivin	g Factor	Pin Name —			-				
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TTL Equivalen	t Circuit								
	745								
	LJ 74L	204							

Cell Name	Function							Number	of BC
V2B	Power Inverter							-	1
Cell Symbol				Propagatio	n Delay Param	eters			
			t	up		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
			0.64	0.12	0.2	4	0.07		$A \rightarrow X$
		: : : : : :				- 1			
A	×	: : : : : <b> </b>	Para	meter	Symbol	MIN	TYP	MAX	UNIT
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Input Loading	g Factor	Pin Name							ļ
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Output Drivir	ng Factor	Pin Name			1		<del> </del>		ļ
	36 ℓu	x					<b>_</b>		<del> </del>
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TTL Equivale	nt Circuit								
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	$\longrightarrow$								
	745	04 504							
AV-V2B	-E1						V2B S	Sheet 1/1	

Cell Name	Function							Number	of BC
K1B	Clock Buffer								2
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>i</sub>	р		<sup>t</sup> dn			Path
			to	KCL	to		KCL		
			1.20	0.12	1.20	6	0.07		$A \rightarrow X$
		}	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
nput Loading	JFactor 1 ℓu	Pin Name			3,1110				
			· · · · · · · · · · · · · · · · · · ·						
Output Drivin	ng Factor	Pin Name —			+		<del> </del>		+
	36 ℓu	х							
TTL Equivaler	74504 74L504	74504 74LS04							
AV-K1B-	-E1						K1B S	Sheet 1/1	

Cell Name	Function							Number	of BC
K2B	Power Clock Buffer								3
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	p .		tdn			Path
			to	K <sub>CL</sub>	to		KCL		
			1.51	0.05	1.8	3	0.04	- 1	$A \rightarrow X$
									<del>,                                     </del>
	× ×		Param	eter	Symbol	MIN	TYP	MAX	UNIT
	:::: <b>/</b> ::::								
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Input Loading	g Factor	Pin Name							<b>†</b>
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Output Drivir	ng Factor	Pin Name -							<b>†</b>
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TTL Equivale	nt Circuit								
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	74504	•							
	74LS04	+ + 1	ノ						
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AV-K2B	-E1						K2B S	Sheet 1/1	



K4B Cell Symbol	Gated Clock (OR) Buff	fer	tup	Propagation	n Delay Param				3
Cell Symbol					Delay Param				
						eters		į	
				•		<sup>t</sup> dn			Path
			to	KCL	to		K <sub>CL</sub>		
	· · · · · · · · · · · · · · · · · · ·		1.39	0.05	3.0	7	0.04		A → X
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		<u> </u>			1		<del> </del>		
Output Driving	y Factor	Pin Name							
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		L1					<u> </u>		
TTL Equivalen	74502								
AV-K4B-	74LS02	L== "1"	J 74\$40			<b> </b> -	К4В S	Sheet 1/1	

Cell Name	Function							Number	of BC
ксв	Block Clock Buffer (No	on-Inv)							11
Cell Symbol				Propagation	n Delay Param	eters			
			tu	р		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
			9.00	0.00	3.3		0.02		A . V
			2.26	0.02	3.3	<b>'</b>	0.02		$A \rightarrow X$
						l			
	$\mathcal{L}$		Paran	notor.	Symbol	MIN	TYP	MAX	UNIT
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nput Loading	g Factor	Pin Name					<del> </del>	-	<del>                                     </del>
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Output Drivin	ng Factor	Pin Name			-		<del> </del>	<b> </b>	<del> </del>
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TTL Equivaler	nt Circuit								
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	74LS04	+ +	リー						
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		"1·	74540						
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AV-KCB	-E1						KCB S	Sheet 1/1	

### **NAND Family**

Page	Unit Cell Name	Function	Basic Cells
3–17	N2N	2-input NAND	1
3-18	N3N	3-input NAND	2
3–19	N4N	4-input NAND	2
3-20	N2B	Power 2-input NAND	3
3-21	N3B	Power 3-input NAND	3
3-22	N4B	Power 4-input NAND	4
3-23	N6B	Power 6-input NAND	5
3-24	N8B	Power 8-input NAND	6
3-25	N9B	Power 9-input NAND	7
3-26	NCB	Power 12-input NAND	9
3-27	NGB	Power 16-input NAND	11

Call Name	Eunction							Number	-4 P.C
								Number	
	Z-Input NAND	T		Oronagation	Dolay Baram	otors		<del> </del>	1
Cell Symbol					T Delay Faran				D-44-
		· · · · · ·			<del></del>				Path
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			0.71	0.27	0.3	4	0.19	ı	$A \rightarrow X$
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	/ <b></b> ×	· · · · · · <b>·</b>	Para	meter	Symbol	MIN	TYP	MAX	UNIT
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Input Loading	Factor	Pin Name —			<u> </u>			<del>                                     </del>	†
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Output Drivin	g Factor	Pin Name —						ļ	
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	74500								
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to KcL to KcL  0.71 0.27 0.34 0.19 A -  Parameter Symbol Miln TYP MAX  Parameter Symbol Miln TYP MAX  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name  18 ℓu X  TTL Equivalent Circuit									
AV-N2N-	E1						N2N	Sheet 1/1	

Cell Name	Function							Number	of BC
N3N	3-input NAND			*****					2
Cell Symbol				Propagation	n Delay Paran	eters			
			t <sub>(</sub>	ıp		tdn			Path
			to	KCL	to		K <sub>CL</sub>		
			0.83	0.27	0.6	2	0.28		A → X
			0.00	0.21	0.0	"	0.20		1 - A
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Input Loading	g ractor	Pin Name —							
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Output Drivir	ng Factor	Pin Name							
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AV-N3N	-E1						N3N S	heet 1/1	

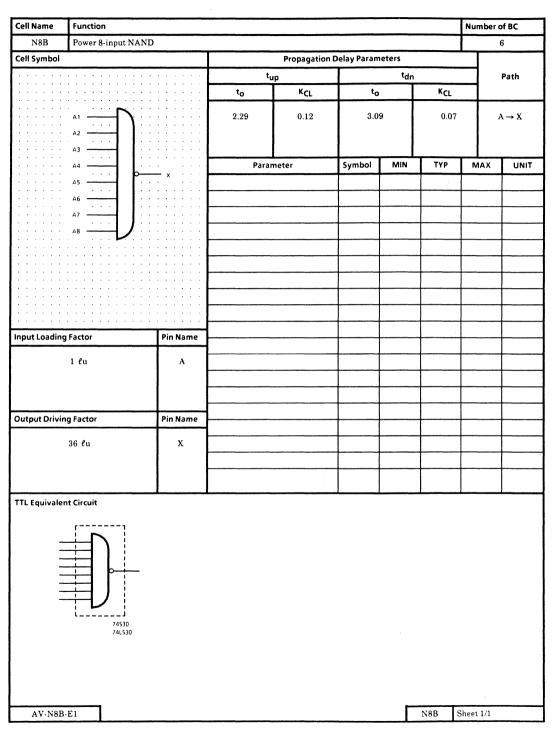
Cell Name	Function							Number o	f BC
N4N	4-input NAND								2
Cell Symbol				Propagation	n Delay Param	eters			
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			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
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			0.50	0.21	0.5		0.00	'	·
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Input Loading	Factor	Pin Name —				wa kuma wasan			
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Output Drivin	g Factor	Pin Name —							
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TTL Equivalen	t Circuit								
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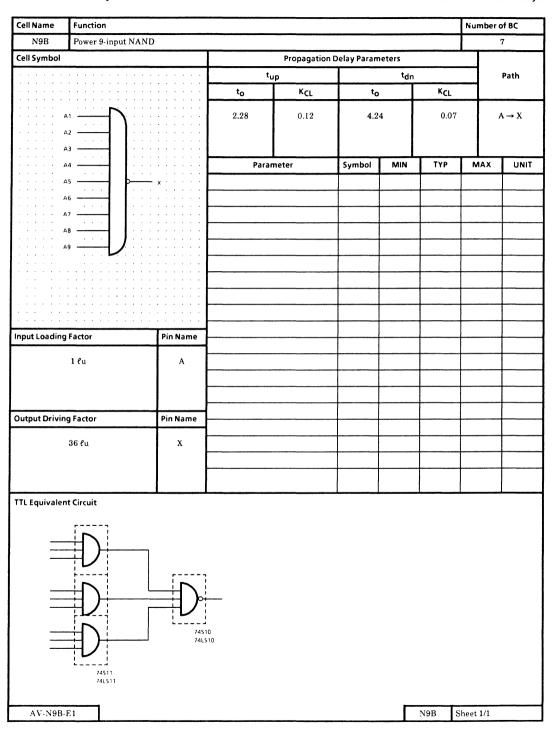
Cell Name	Function							Number	of BC
N2B	Power 2-input NAND								3
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	р		t <sub>dn</sub>			Path
			t <sub>o</sub>	K <sub>CL</sub>	to		KCL		
			2.03	0.12	1.7	,	0.07		A → X
			2.00	0.12	1		0.01	] '	1 -7 A
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	A1	J:::::	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
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Input Loading	g Factor	Pin Name —		<del></del>			<del> </del>		
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Output Drivi	ng Factor	Pin Name					<del>                                     </del>		<u> </u>
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TTL Equivale	nt Circuit								
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	74500 74L500								
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AV-N2B	5-E1						N2B S	Sheet 1/1	

Cell Name	Function							Number	of BC
N3B	Power 3-input NAND	1							3
Cell Symbol				Propagation	n Delay Param	eters			
			tլ	ıp		<sup>t</sup> dn			Path
			to	KCL	to		KCL		
			0.05	0.10	2.0		0.07		
			2.27	0.12	2.0	9	0.07	1	$A \to X$
	A1						T		
	A2 - X		Parar	neter	Symbol	MIN	ТҮР	MAX	UNIT
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Input Loading	Factor	Pin Name —							
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Output Drivin	g Factor	Pin Name					ļ	ļ	
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TTL Equivaler	nt Circuit							<u> </u>	L
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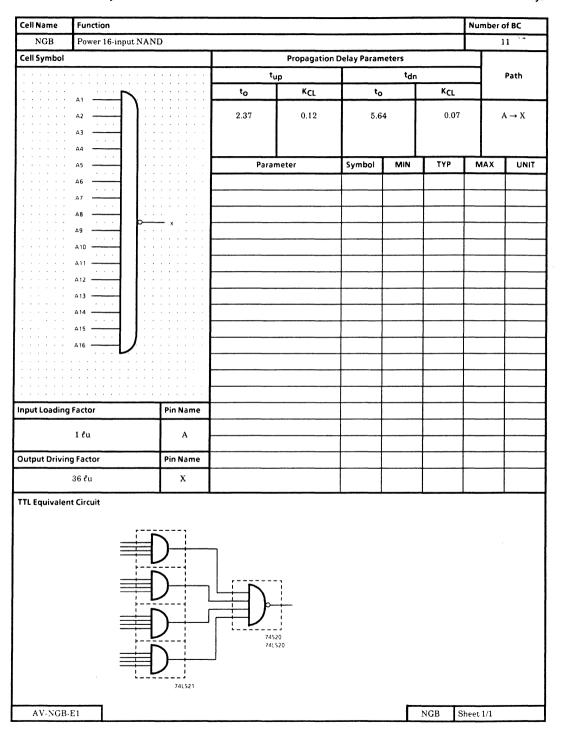
Cell Name	Function							Number o	of BC
N4B	Power 4-input NAND								4
Cell Symbol				Propagation	n Delay Param	eters			
			tլ	ıp		tdn			Path
			to	KCL	to		KCL		
			2.38	0.12	2.3	5	0.07	A	A → X
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	A2	x	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
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Output Drivin	g Factor	Pin Name							
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	74520 74L520								
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Cell Name	Function							Number	of BC
N6B	Power 6-input NANI	D						1	5
Cell Symbol		T		Propagation	n Delay Param	eters		<u> </u>	
			t <sub>t</sub>	ıp		<sup>t</sup> dn			Path
			to	KCL	to		KCL		
			2.18	0.12	2.8	,	0.07		A → X
			2.10	0.12	2,0	, I	0.01		1 <del>7</del> A
A1					1				
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nput Loading	g Factor	Pin Name —					<b> </b>		
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Output Drivir	ng Factor	Pin Name							
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		74L530				<b></b>			
AV-N6B	E1						N6B S	Sheet 1/1	





Cell Name	Function							Number	of BC
NCB	Power 12-input NANI	)	-					!	9
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>i</sub>	ıp		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
	A1		2.26	0.12	5.3		0.07		A → X
	42		2.20	0.12	0.0	°	0.01	'	171
,	43 —					ı			
,	A4	: : : : : <b> </b>	Parai	neter	Symbol	MIN	TYP	MAX	UNIT
	A5	<b> -</b>			3,				
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	A7	^ : : : : : <b> -</b>							<del>                                     </del>
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	A12	::::: <b> </b>							1
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Output Drivin	ig ractor	Pin Name							
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	74L521								



## **AND Family**

Page	Unit Cell Name	Function	Basic Cells
3-31	N2P	Power 2-input AND	2
3-32	N3P	Power 3-input AND	3
3 33	NAD	Power 4 input AND	3

Cell Name	Function							Number	of BC
N2P	Power 2-input AND								2
Cell Symbol				Propagatio	n Delay Param	eters			
			tլ	ıp		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			1.32	0.12	1,4	1	0.07	A → >	
			Parar	neter	Symbol	MIN	ТҮР	MAX	UNIT
A2	—								
nput Loading	Factor	Pin Name —							
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Output Driving	g Factor	Pin Name —							
	36 ℓu	x							
TTL Equivalen	t Circuit	<u>LL</u>		P-107					
	74508								
	74LS08								

Cell Name	Function							Number	of BC
N3P	Power 3-input AND								3
Cell Symbol				Propagation	n Delay Param	eters			
			tı	ıp		<sup>t</sup> dn	ı		Path
		<b>[</b>	to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			1.82	0.12	1.6	1	0.07		A → X
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	A2	`	Parai	neter	Symbol	MIN	TYP	MAX	UNIT
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Input Loading	Factor	Pin Name –			-		<u> </u>		<del> </del>
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Output Drivin	g Factor	Pin Name -			1				<b>†</b>
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TTL Equivaler	r								
	74511 74L511								
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AV-N3P-	E1					Γ	N3P S	Sheet 1/1	

Cell Name	Function							Number	of BC
N4P	Power 4-input AND								3
Cell Symbol		Į.		Propagation	n Delay Param	eters			
			tu	р		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			2.15	0.12	1.7	,	0.07		A → X
			2.10	0.12	1.4	'	0.07		A → A
	A1 —				1				
		-	Parar	notor	Symbol	MIN	TYP	MAX	UNIT
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Output Drivin	g Factor	Pin Name —			-		<del> </del>	<del> </del>	<del> </del>
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AV-N4P-	<del></del>						N4P S	Sheet 1/1	

## **NOR Family**

Page	Unit Cell Name	Function	Basic Cells
2-37	R2N	2-input NOR	1
2-38	R3N	3-input NOR	2
2-39	R4N	4-input NOR	2
2-40	R2B	Power 2-input NOR	3
2-41	R3B	Power 3-input NOR	3
2-42	R4B	Power 4-input NOR	4
2-43	R6B	Power 6-input NOR	5
2-44	R8B	Power 8-input NOR	6
2-45	R9B	Power 9-input NOR	7
2-46	RCB	Power 12-input NOR	9
2-47	RGB	Power 16-input NOR	11

Cell Name	Function							Nur	mber o	f BC
R2N	2-input NOR							T		l
Cell Symbol	<u> </u>			Propagation	Delay Paran	eters				
			t,	ıb		tdr	า			Path
			to	KCL	to		K <sub>CL</sub>			
			0.07	0.46	0.2	2	0.13			<b>A</b> → X
			0.87	0.46	0.2	J	0.13		,	. <del>- </del>
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Input Loading	Factor	Pin Name						_		
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Output Driving	g Factor	Pin Name						+		
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AV-R2N-l	E1					Γ	R2N	Sheet	1/1	

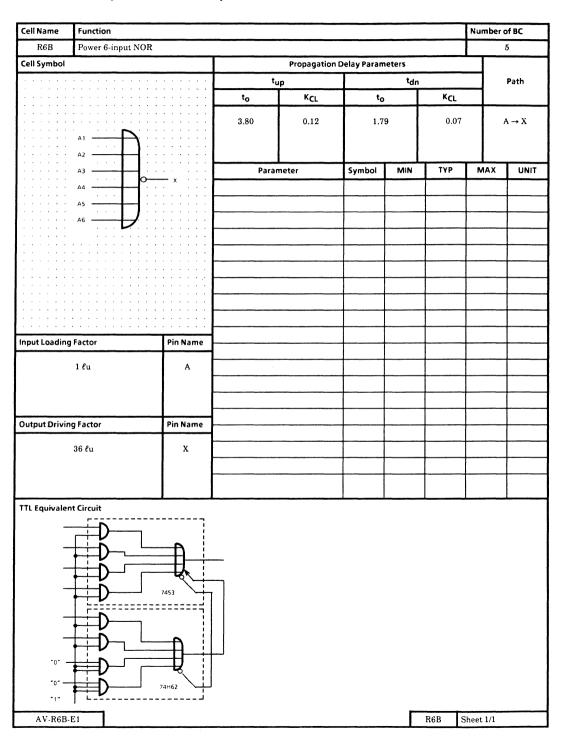
Cell Name	Function				1 4			Number	of BC
R3N	3-input NOR								2
Cell Symbol				Propagation	n Delay Param	eters			
			tլ	ıp		<sup>t</sup> dn			Path
			t <sub>o</sub>	K <sub>CL</sub>	to		KCL		
			1.98	0.60	0.3	1	0.15	I	A → X
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AV-R3N-	E1						R3N S	Sheet 1/1	

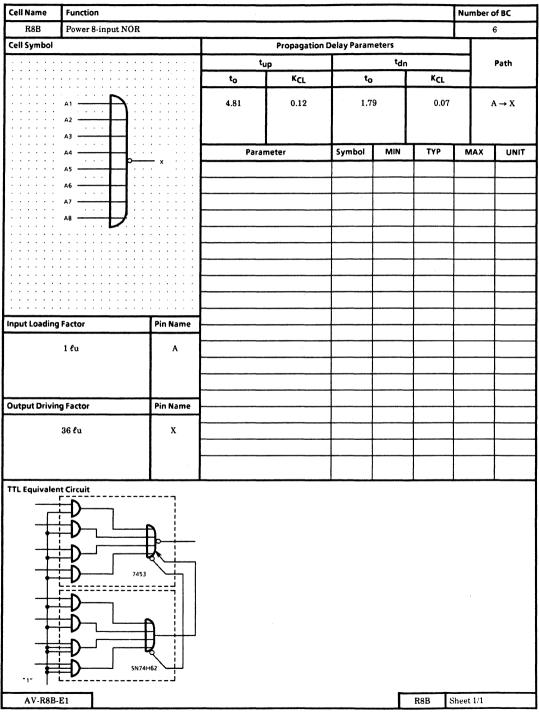
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R4N	4-input NOR								2
Cell Symbol				Propagation	n Delay Param	eters			
			tu	p		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
			0.74	0.76	0.2	,	0.16		
			2.74	0.76	0.3	"	0.16	' l '	$A \to X$
	A1				l	- 1			
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	A3	`	Parar	neter	Symbol	MIN	ТҮР	MAX	UNIT
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Output Drivin	g Factor	Pin Name						<b>_</b>	<u> </u>
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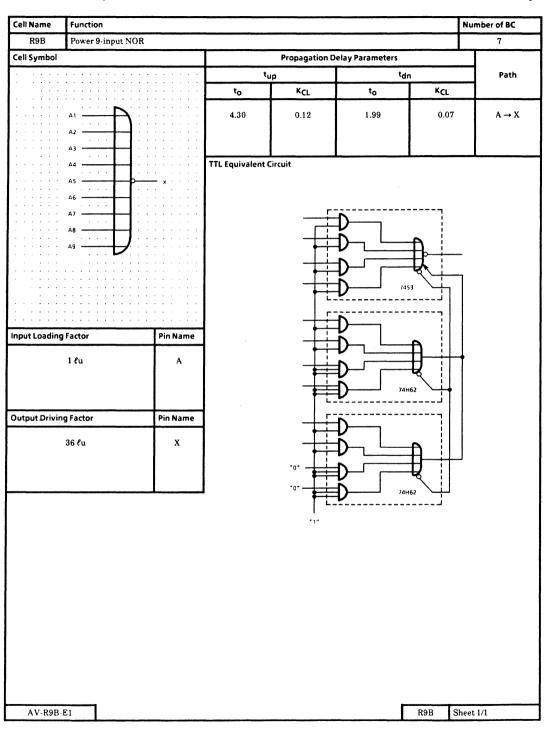
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R2B	Power 2-input NOR								3
Cell Symbol				Propagation	n Delay Param	eters			
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			to	K <sub>CL</sub>	t <sub>o</sub>		KCL		
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			2.00	0.12	"			į	• • • •
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	×		Parar	neter	Symbol	MIN	TYP	MAX	UNIT
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TTL Equivale	nt Circuit								
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AV-R2B	)-E1						R2B	Sheet 1/1	

Cell Name	Function							Number	of BC
R3B	Power 3-input NOR								3
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	ıp		<sup>t</sup> dn			Path
			to	KCL	to		KCL		
		- : : : : : : <b>  -</b>							
			3.65	0.12	1.6	1	0.07	1	$A \to X$
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Output Drivin	g Factor	Pin Name —							
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AV-R3B-									
							R3B S	Sheet 1/1	

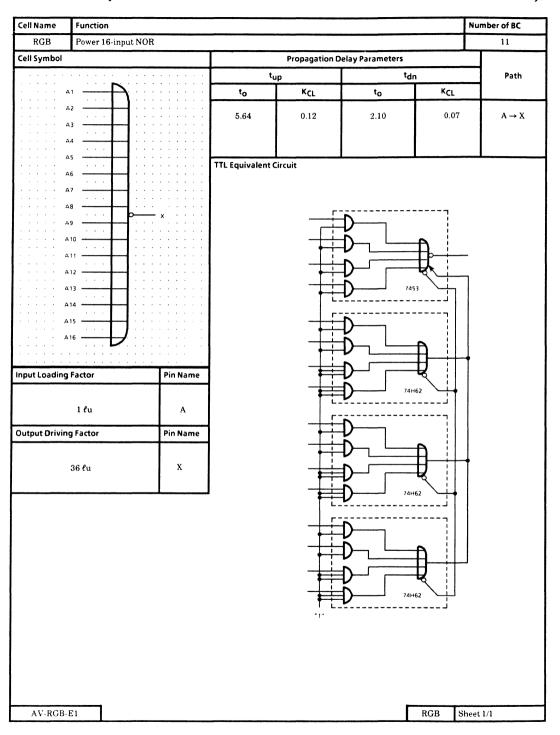
Cell Name	Function							Number	of BC
R4B	Power 4-input NOR								4
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>t</sub>	р		t <sub>dn</sub>			Path
			to	KCL	to		KCL		
			4.66	0.12	1.6	,	0.07		A → X
			4.00	0.12	1.0	·	0.01	-   '	1 <del>7</del>
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Input Loading	Factor	Pin Name							
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Output Drivin	ng Factor	Pin Name							
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RCB         Power 12-input NOR         9           Cell Symbol         Propagation Delay Parameters           tup         tdn         Path           to         KCL         to         KCL           A2         4.63         0.12         2.10         0.07         A → X           A3         A6         A7         A8         A9         A9         A10         A11         A11         A12         A12         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14	RCB         Power 12-input NOR         9           Cell Symbol         Propagation Delay Parameters           tup         tdn         Patl           to         KCL         to         KCL         A →           A3         A4         A63         0.12         2.10         0.07         A →           A5         A6         A7         A8         A9         A10         A11         A12         A12         A12         A14         A14         A14         A14         A15         A16         A17         A17         A18         A19         A19         A10         A11         A11         A12         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14         A14	RCB   Power 12-input NOR   9	9 Path						ne Function	Cell Name
Propagation Delay Parameters   Tup   tdn   Path	Cell Symbol         Propagation Delay Parameters           tup         tdn         Path           to         KCL         to         KCL           4.63         0.12         2.10         0.07         A →           A3         A4         A5         TTL Equivalent Circuit         TTL Equivalent Circuit         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3         A3	Propagation Delay Parameters   tup   tdn   to   KCL   to   KCL     A1   A2   A3   A4   A5   A7   A8   A9   A10   A11   A12   A12   A12   A12   A12   A12   A12   A12   A12   A14   A15   A15   A15   A15   A15   A16   A17   A17   A18   A19   A19   A10   A11   A12   A12   A12   A12   A13   A14   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15   A15	Path					NOR		
tup tdn Path  to KCL to KCL  A2  4.63 0.12 2.10 0.07 A → X  A3  A4  TTL Equivalent Circuit  TTL Equivalent Circuit  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name  36 ℓu X	tup tdn Pati to KCL  4.63 0.12 2.10 0.07 A →  4.63 0.12 2.10 0.07 A →  TTL Equivalent Circuit  1 ℓu A  Output Driving Factor Pin Name	tup tdn   to   KCL   to   KCL		i	elay Parameters	Propagation De				
to KCL to KCL  4.63 0.12 2.10 0.07 A → X  4.63 0.12 2.10 0.07 A → X  TTL Equivalent Circuit  Input Loading Factor Pin Name  1 ℓ u A  Output Driving Factor Pin Name  36 ℓ u X	to KCL to KCL  A2  4.63  0.12  2.10  0.07  A→  A3  A5  TTL Equivalent Circuit  Input Loading Factor  Pin Name  1 ℓu  A  Output Driving Factor  Pin Name	to KCL to KCL  A2  4.63  0.12  2.10  0.07  A  TTL Equivalent Circuit  Input Loading Factor  1 \( \ell \) U  A					t,			
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TTL Equivalent Circuit  A6 A7 A8 A9 A9 A10 A11 A12  Input Loading Factor Pin Name 1 ℓu A  Output Driving Factor Pin Name 36 ℓu X	TTL Equivalent Circuit  A6 A7 A8 A9 A10 A11 A12  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name	TTL Equivalent Circuit  A6  A7  A8  A8  A9  A10  A11  A12  Input Loading Factor Pin Name  1 ℓu A	$A \rightarrow X$	0.07	2.10	0.12	4.63		· · A2	
TTL Equivalent Circuit  A6 A7 A8 A9 A10 A11 A12  Input Loading Factor Pin Name 1 ℓu A  Output Driving Factor Pin Name 36 ℓu X	TTL Equivalent Circuit  A6  A7  A8  A9  A10  A11  A12  Input Loading Factor Pin Name  1 & u A	TTL Equivalent Circuit  A6  A7  A8  A9  A10  A12  Input Loading Factor Pin Name  1 & u A			1				АЗ	
TTL Equivalent Circuit  A6 A7 A8 A9 A10 A11 A12  Input Loading Factor Pin Name 1 ℓu A  Output Driving Factor Pin Name 36 ℓu X	TTL Equivalent Circuit  A6  A7  A8  A9  A10  A11  A12  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name	TTL Equivalent Circuit  A6  A7  A8  A9  A10  A12  Input Loading Factor Pin Name  1 & u A							· · · · · · · · · · · · · · · · · · ·	
A6 A7 A8 A8 A9 A10 A11 A12  Input Loading Factor Pin Name  1 ℓ u A  Output Driving Factor Pin Name  36 ℓ u X	A6 A7 A8 A8 A9 A10 A11 A12  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name	A6				ircuit	TTI Fauivalent			
A7 A8 A8 A9 A10 A11 A12  Input Loading Factor Pin Name 1 ℓu A  Output Driving Factor Pin Name 36 ℓu X	A7 A8 A9 A10 A11 A11 A12  Input Loading Factor  I fu  A  Output Driving Factor  Pin Name	A7				com	TTE Equivalent			
A8 A9 A10 A11 A12  Input Loading Factor Pin Name  1 ℓu A  Output Driving Factor Pin Name  36 ℓu X	A8 A9 A10 A11 A12  Input Loading Factor Pin Name  1 \( \ell u \)  Output Driving Factor Pin Name	Input Loading Factor Pin Name						x	A6	
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name	Input Loading Factor Pin Name							A7	
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor Pin Name  1 \( \ell u \)  Output Driving Factor Pin Name	Input Loading Factor  1 \( \ell u \)  A  A  A  A  A  A  A  A  A  A  A		7	<b>N</b>				А8	
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor  Pin Name  1 \( \ell u \)  Output Driving Factor  Pin Name	Input Loading Factor Pin Name		!		<del>[                                    </del>			А9	
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor  Pin Name  1 \( \ell u \)  Output Driving Factor  Pin Name	Input Loading Factor Pin Name		A !	D-, \				Δ10	
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor  Pin Name  1 lu  A  Output Driving Factor  Pin Name	Input Loading Factor Pin Name		<b>I</b> Þ						
Input Loading Factor Pin Name  1 lu A  Output Driving Factor Pin Name  36 lu X	Input Loading Factor Pin Name  1 fu A  Output Driving Factor Pin Name	Input Loading Factor Pin Name		₩ <u>.</u>	D_	1			A11	
Input Loading Factor Pin Name  1 \( \ell u \)  Output Driving Factor Pin Name  36 \( \ell u \)  X	Input Loading Factor Pin Name  1 du A  Output Driving Factor Pin Name	Input Loading Factor Pin Name		, \	7453				A12	
1 lu A Output Driving Factor Pin Name 36 lu X	1 lu A Output Driving Factor Pin Name	1 eu A			ν 	L				
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Output Driving Factor Pin Name 36 éu X	Output Driving Factor Pin Name				<u> </u>	<del>-   -  </del>		Pin Name	ading Factor	Input Loading
Output Driving Factor Pin Name  36 éu X	Output Driving Factor Pin Name			╆┵┼		•			1.60	
Output Driving Factor Pin Name  36 éu X	Output Driving Factor Pin Name	74H62		₽ :	$\mathcal{D}$			n .	1 tu	
Output Driving Factor Pin Name  36 éu X	Output Driving Factor Pin Name	/4/102			701167	<del>- Li</del>				
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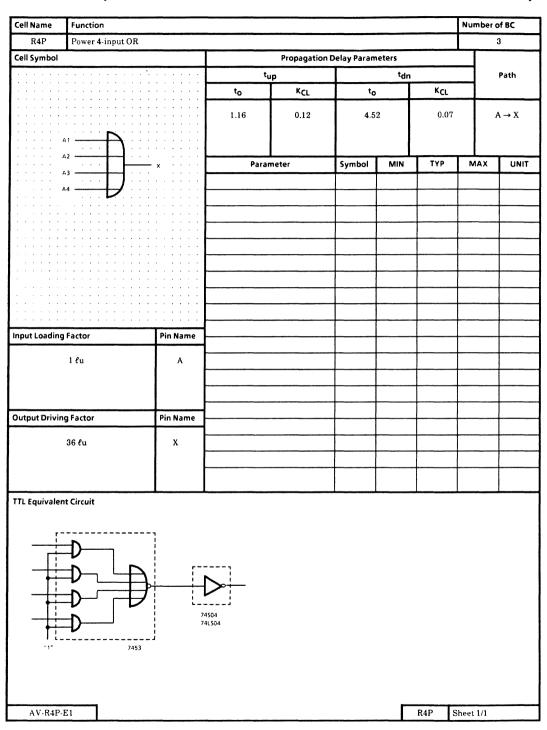


## **OR Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3-51	R2P	Power 2-input OR	2
3-52	R3P	Power 3-input OR	3
3-53	R4P	Power 4-input OR	3

Cell Name	Function							Number	of BC
R2P	Power 2-input OR								2
Cell Symbol				Propagation	Delay Param	eters			
			tu	р		<sup>t</sup> dn			Path
		: : : : : : <b>[</b>	to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			1.08	0.12	1.9	7	0.07	,	$A \to X$
	A1	x	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
nput Loading		Pin Name							
	1 lu	A							
									-
Output Drivin	g Factor	Pin Name							<u> </u>
	36 ℓu	x							
TTL Equivalen	nt Circuit	1					1		L
_	/4532 74L532								
AV-R2P-	E1					Г	R2P S	heet 1/1	

Cell Name	Function							Number	of BC
R3P	Power 3-input OR								3
Cell Symbol				Propagation	Delay Param	eters			
			tլ	ıp		<sup>t</sup> dn	1		Path
		: : : : : <b>[</b>	to	K <sub>CL</sub>	to		KCL		
			1.18	0.12	3.38	,	0.07		$A \rightarrow X$
			1.10	0.12			0.01		•
	A1								
	A2	, <b> </b>	Parai	neter	Symbol	MIN	ТҮР	MAX	UNIT
	A3	Î : : : : : <b> -</b>							
	~	<b> </b> -					<del>- </del>	<del> </del>	<del> </del>
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		<b> -</b>							<b> </b>
		<b> -</b>							
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		: : : : : <b> -</b>					<del> </del>		<b>†</b>
		: : : : : <b> -</b>			+		+		<u> </u>
							<del> </del>	<del>                                     </del>	<b>†</b>
Input Loading	g Factor	Pin Name			+		<u> </u>	<b>†</b>	<del>                                     </del>
	1 <b>l</b> u	A					<u> </u>	<u> </u>	
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									<b>†</b>
								<u> </u>	<b>†</b>
Output Drivir	ng Factor	Pin Name —						<u> </u>	<b> </b>
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		<u>l</u>						<u> </u>	<u> </u>
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	74LS27								
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AV-R3P	-E1						R3P	Sheet 1/1	



## **EXNOR/EXOR Family**

Page	Unit Cell Name	Function	Basic Cells
3-57	X1B	Power EXNOR	4
3-58	X2B	Power FXOR	4

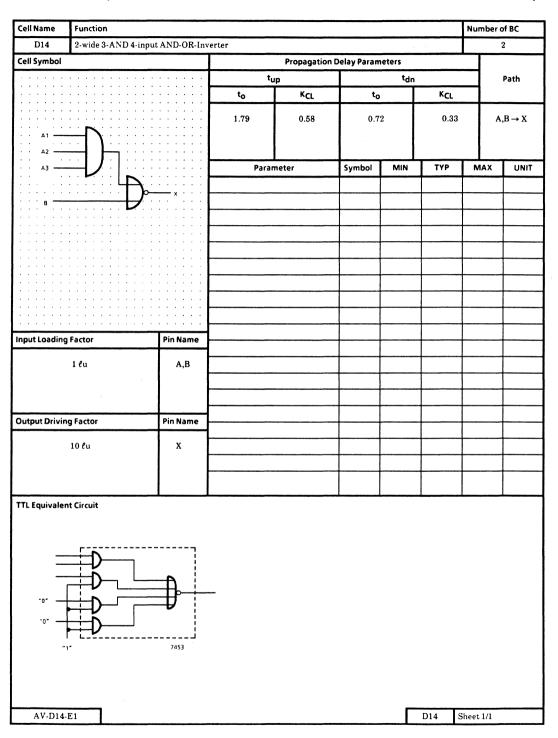
Cell Name	Function							Number	of BC
X1B	Power ENOR								4
Cell Symbol				Propagation	Delay Param	eters			
			t	up		<sup>t</sup> dr	1		Path
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
		: : : : : <b>[</b>	0.41	0.10	1		0.07		. v
			2.41	0.12	3.2	4	0.07	l	$A \rightarrow X$
							i	- 1	
A1	-+	: : : : : <b> </b>		<u> </u>	-	20121	T/0	<del></del>	T
 A2			Para	meter	Symbol	MIN	TYP	MAX	UNIT
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							4	<del> </del>	
Output Driving	g Factor	Pin Name						<del> </del>	-
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TTL Equivalen	t Circuit								
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AV-X1B-I	31					Г	X1B	Sheet 1/1	<del></del>
VA-VID-I							ALD	J.1CCC 1/1	

Cell Name	Function							Number o	of BC
X2B	Power EOR								4
Cell Symbol				Propagation	Delay Param	eters			
			. t <sub>u</sub>	p		t <sub>dn</sub>			Path
			to	KCL	to		K <sub>CL</sub>		
			2.34	0.12	3.5	0	0.07	A	A → X
	A1	: · · · · · · · · · · · · · · · · · · ·	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
Input Loading	Factor	Pin Name							
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	2 tu	\ ^ <b>-</b>							
		-		······································					
					-				
Output Driving	g Factor	Pin Name							
	36 ℓu	x			1				
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		<u> </u>					li		
TTL Equivalen									

## AND-OR-Inverter Family

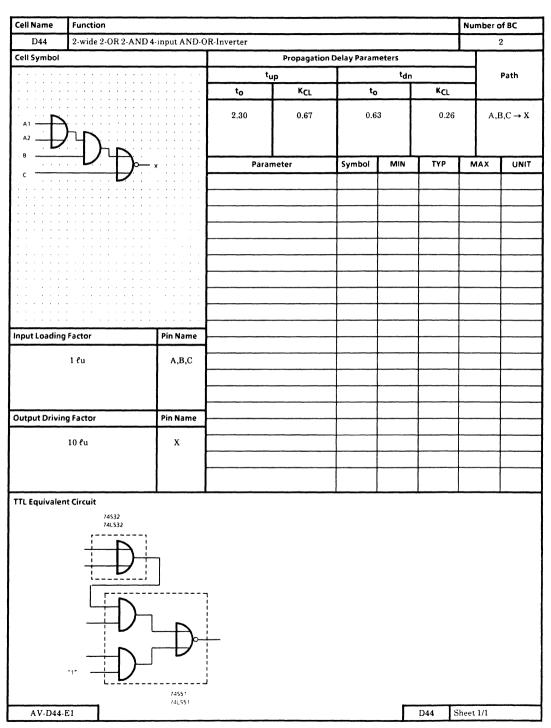
Page	Unit Cell Name	Function	Basic Cells
3-61	D14	2-wide 3-AND 4-input AND-OR inverter	2
3-62	D23	2-wide 2-AND 3-input AND-OR inverter	2
3-63	D24	2-wide 2-AND 4-input AND-OR inverter	2
3-64	D34	3-wide 2-AND 4-input AND-OR inverter	2
3-65	D44	2-wide 2-OR 2-AND 4-input AND-OR inverter	2
3-66	D36	3-input AND-OR Inverter	3

tup         tdn         Path           to         KCL         to         KCL           1.41         0.54         0.48         0.24         A,B → X           Parameter         Symbol         MIN         TYP         MAX         UNIT           Input Loading Factor         Pin Name         If a contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract o	Cell Name	Function							Number	of BC
tup         tdn         Path           to         KCL         to         KCL           1.41         0.54         0.48         0.24         A,B → X           Parameter         Symbol         MIN         TYP         MAX         UNIT           Input Loading Factor         Pin Name         If a contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract of the contract o	D23	2-wide 2-AND 3-inpu	t AND-OR-Inver	ter						2
to KCL to KCL  1.41 0.54 0.48 0.24 A,B→ X  Parameter Symbol MIN TYP MAX UNIT  Symbol MIN TYP MAX UNIT  Parameter Symbol MIN TYP MAX UNIT  ABOUT Loading Factor Pin Name  1 ℓ u A,B  Lutput Driving Factor Pin Name  10 ℓ u X  TI. Equivalent Circuit	Cell Symbol				Propagation	n Delay Param	eters			
1.41 0.54 0.48 0.24 A,B→ X  Parameter Symbol MiN TYP MAX UNIT  Symbol MiN TYP MAX UNIT  Parameter Symbol MiN TYP MAX UNIT  Parameter Symbol MiN TYP MAX UNIT  A,B UNIT  Parameter Symbol MiN TYP MAX UNIT  Parameter Symbol MiN TYP MAX UNIT  Typut Loading Factor Pin Name  10 €u X  TL Equivalent Circuit				tլ	ıp		<sup>t</sup> dn			Path
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Injust Loading Factor Pin Name  1 fu A,B  Sutput Driving Factor Pin Name  10 fu X  TL Equivalent Circuit	· · · · · ·									
input Loading Factor Pin Name  1 \( \ell \) A,B  input Driving Factor Pin Name  10 \( \ell \) X  TL Equivalent Circuit			x · ·	Parai	neter	Symbol	MIN	TYP	MAX	UNIT
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1 fu A,B  Putput Driving Factor Pin Name  10 fu X  TL Equivalent Circuit								-		
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1 fu A,B  Putput Driving Factor Pin Name  10 fu X  TL Equivalent Circuit							·····			ļ
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TL Equivalent Circuit	Input Loading	Factor	Pin Name							-
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74L5S1		L								
AV D22 E1										
AV D92 F1										
AV D22 E1										
	4 V-D22	FI					г	D23 S	heet 1/1	



Cell Name	Function							Number	of BC
D24	2-wide 2-AND 4-input	AND-OR-Inver	ter						2
Cell Symbol				Propagation	Delay Param	eters			
			tu	p		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
A1 ——			1.66	0.61	0.48	3	0.26	А	,B → X
	<u> </u>		Paran	neter	Symbol	MIN	ТҮР	MAX	UNIT
B1 B2 B2 B3 B3 B3	) Factor	Pin Name A,B							
Output Drivir	ng Factor	Pin Name							
	10 lu	х							
TTL Equivaler	74551 74555								
AV-D24-	E1					Г	D24 S	heet 1/1	

Cell Name	Function							Number	of BC
D34	3-wide 2-AND 4-inp	ut AND-OR-Inver	ter						2
Cell Symbol				Propagation	n Delay Param	eters			
			tı	ıp		<sup>t</sup> dn		$\neg$	Path
	3-wide 2-AND 4-input AND-OR ymbol  A1  A2  B1  B2  Loading Factor Pin Nam  1 \( \ell u \) A,B		to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			2.36	0.69	0.4	8	0.27	A	,B → X
			2.00	0.00	1 0.1		0.21	-   "	.,D - A
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	P	<del> </del>	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
B1 —	<del></del>	· · · · × · · ·			-			<b>†</b>	
B2 —	·····/	: : : : : <b> </b>							
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AV-D34	-E1					Г	D34 S	Sheet 1/1	



D36	Number of BC	FUJITSU C	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"A"	V" Version
Propagation Delay Parameter   tup   tdn   t0   KCL   t0   KCL   Path   2.92   0.77   0.72   0.30   A,B,C →	Propagation   Delay Parameter	Cell Name	Function				1	Number of BC
Propagation Delay Parameter   tup   tdn   t0   KCL   t0   KCL   Path   2.92   0.77   0.72   0.30   A,B,C →	Propagation   Delay Parameter	D36	3-input AND-OR-	Inverter				3
tup tdn  t0 KCL t0 KCL Path  2.92 0.77 0.72 0.30 A,B,C →   B1 B2 Parameter Symbol Typ(ns)  Parameter Input Loading  Pin Name Factor (£u)	tup tdn  t0 KCL t0 KCL Path  2.92 0.77 0.72 0.30 A,B,C → X  B1 B2 Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  A, B, C 1  Output Driving Pin Name Factor (£u)		3 Impac and on	P	ropagation	Delay Para	meter	•
Al Al Bl Bl Bl Parameter Symbol Typ(ns)  Parameter Symbol Typ(ns)  Pin Name Factor (&u)	A1 A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u) A, B, C 1  Output Driving Pin Name Factor (£u)				р	t	dn	
Al Al Bl Bl Bl Parameter Symbol Typ(ns)  Parameter Symbol Typ(ns)  Pin Name Factor (&u)	A1 A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u) A, B, C 1  Output Driving Pin Name Factor (£u)				KCL		KCL	Path
A2 B1 B2 C1 C2 Parameter Symbol Typ(ns)  Pin Name Input Loading Factor (£u)	A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)			2.92	0.77	0.72	0.30	$A,B,C \rightarrow X$
A2 B1 B2 C1 C2 Parameter Symbol Typ(ns)  Pin Name Input Loading Factor (£u)	A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)							
B1 B2 C1 C2 Parameter Symbol Typ(ns)  Pin Name Input Loading Factor (£u)	A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)							
A2 B1 B2 C1 C2 Parameter Symbol Typ(ns)  Pin Name   Input Loading Factor (£u)	A2 B1 B2 Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)	A1 —						
Parameter Symbol Typ(ns)  Pin Name Factor (£u)	Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A, B, C 1  Output Driving Factor (lu)  Parameter Symbol Typ(ns)*		7_					
Parameter Symbol Typ(ns)  Pin Name Factor (2u)	Parameter  Symbol Typ(ns)*  Pin Name Factor (lu)  A, B, C 1  Output Driving Factor (lu)  Pin Name Factor (lu)		Д х					
C2 Parameter Symbol Typ(ns)  Pin Name Factor (2u)	C2  Input Loading Pin Name Factor (lu)  A, B, C  Output Driving Pin Name Factor (lu)	B2						
Input Loading Pin Name Factor (lu)	Pin Name   Input Loading   Factor (lu)   A, B, C			Parameter		1	Symbol	Typ(ns)*
Pin Name   Factor (lu)	Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)							
Pin Name   Factor (lu)	Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)						1	
Pin Name   Factor (lu)	Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)							
Pin Name   Factor (lu)	Pin Name Factor (lu) A, B, C 1  Output Driving Pin Name Factor (lu)							
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A, B, C 1	A, B, C 1  Output Driving Pin Name Factor (lu)		Input Loading					
	Pin Name   Factor (lu)	A, B, C						
	Pin Name   Factor (lu)							
	Pin Name   Factor (lu)							
Output Driving			Output Driving					
			Factor (lu)					
* Minimum values for the typical operating conditi	* Minimum values for the typical operating condition			* Minimum	values for	the twoice	al operati	ng condition
The values for the worst case operating condition	The values for the worst case operating condition			The valu	es for the	worst case	e operatin	g condition
are given by the maximum delay multiplier.			L	are give	n by the m	maximum dela	ay multipl	ier.
The values for the worst case operating condition	The values for the worst case operating condition			The valu	es for the	worst case	e operatin	g condition
	are given by the maximum delay multiplier.		A				***************************************	
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.							
	are given by the maximum delay multiplier.	AV-D36-E1	Sheet 1/1	·				Page 5-7

## **OR-AND-Inverter Family**

Page	Unit Cell Name	Function	Basic Cells
3-69	G14	2-wide 3-OR 4-input OR-AND Inverter	2
3-70	G23	2-wide 2-OR 3-input OR-AND Inverter	2
3-71	G24	2-wide 2-OR 4-input OR-AND Inverter	2
3-72	G34	3-wide 2-OR 4-input OR-AND Inverter	2
3_73	GAA	2-wide 2-AND 2-OR 4-input OR-AND Inverter	2

Cell Name	Function							Number	of BC
G14	2-wide 3-OR 4-input	OR-AND-Inverte	r						2
Cell Symbol	<u> </u>			Propagation	n Delay Param	eters		<u>'                                    </u>	
			tu			<sup>t</sup> dn			Path
			to	KCL	to		KCL		
			2.23	0.69	0.54	4	0.27	А	.,B → X
A1 ————————————————————————————————————	2-wide 3-OR 4-input OR-AND-Invocal  Sing Factor Pin Name  1 \( \ell u \)  A,B  iving Factor Pin Name  10 \( \ell u \)  X  alent Circuit		Paran	neter	Symbol	MIN	ТҮР	MAX	UNIT
B B		Pin Name A,B							
Output Drivin	g Factor	Pin Name —							
	10 <b>ℓ</b> u	X							
TTL Equivalen	t Circuit						1		l
	74527	74.504							
AV-G14-I						_	G14 S	heet 1/1	

Cell Name	Function					***		Number	of BC
G23	2-wide 2-OR 3-input (	R-AND-Inverte	r						2
Cell Symbol	· · · · · · · · · · · · · · · · · · ·			Propagation	Delay Param	eters			
			t <sub>u</sub>	p		<sup>t</sup> dn		$\neg$	Path
			to	K <sub>CL</sub>	to		KCL		
			1.41	0.54	0.4	3	0.24	A	,B → X
A1	D-D-		Parar	neter	Symbol	MIN	ТҮР	MAX	UNIT
Input Loading	Factor	Pin Name					<b>-</b>	İ	<del> </del>
	1 eu	A,B							
Output Drivin	ng Factor	Pin Name					-		<del> </del>
	10 ℓu	х							
TTL Equivaler	nt Circuit	<u> </u>						<u> </u>	<u></u>
-	74532 74L532	74500 74L500							
AV-G23	E1					Г	G23 S	Sheet 1/1	

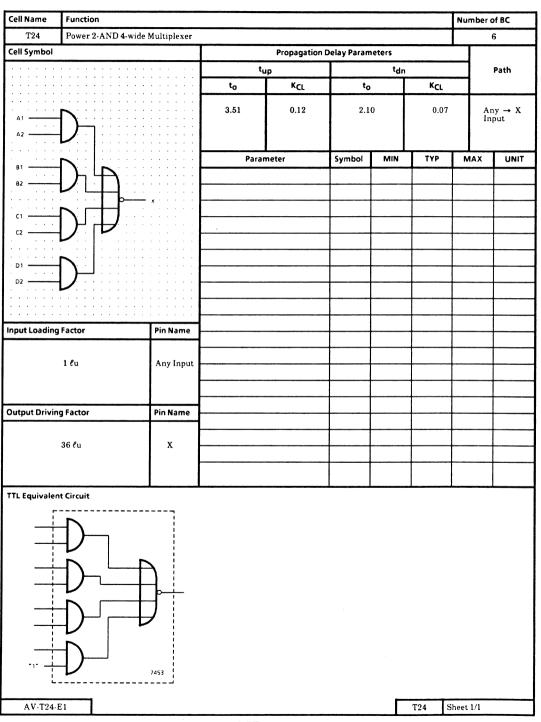
Cell Name	Function							Number	of BC
G24	2-wide 2-OR 4-input O	R-AND-Inverte	r						2
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	р		<sup>t</sup> dn			Path
		: : : : : · <b>[</b>	to	KCL	to		K <sub>CL</sub>		
	2-wide 2-OR 4-input OR-AND-Inbol		1.47	0.57	0.5	4	0.28	А	.,B → X
A2		<del> </del>	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
B1 B2 B2	Factor	Pin Name							
	1 <b>/</b> u	A B	***************************************		-		-		ļ
	7.00	'`.B							<u> </u>
		<del> </del>							
		-							
Output Drivin	g Factor	Pin Name							
	10 ℓu	х							
TTL Equivaler	nt Circuit	LL_					L		L
	74L532 74S32	<b>-</b> 00							
AV-G24-	E1					Г	G24 S	heet 1/1	

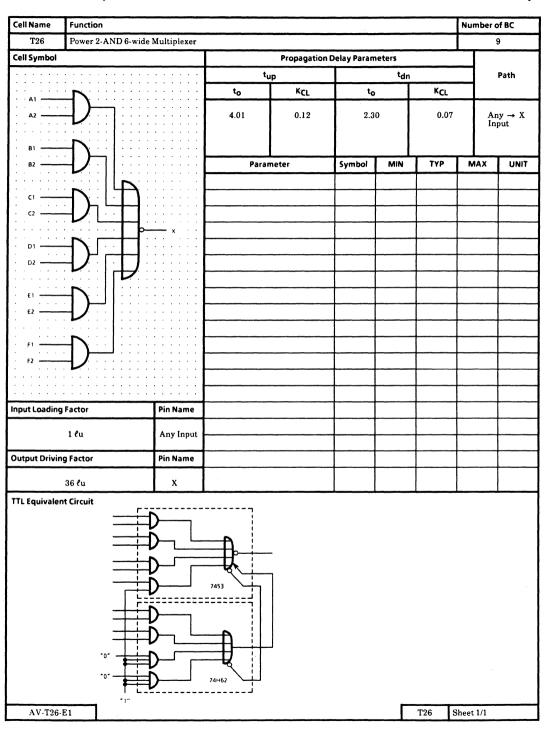
Cell Name	Function							Number	of BC
G34	3-wide 2-OR 4-input O	R-AND-Inverte	er						2
Cell Symbol		· ·		Propagation	n Delay Param	eters			
		: : : : : L	t <sub>u</sub>	р		t <sub>dn</sub>			Path
		: : : : : <b>L</b>	to	KCL	to		KCL		
			1.53	0.57	0.73	2	0.34	A	.,B → X
						- 1			
					Ì				
· · A1		::::: <b>[</b>	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
		: : : : : <b>[</b>							
		_ x							
B2 ——			·				<u> </u>		
		: : : : : <b> </b> _							ļ
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		: : : : : :					<del> </del>	<del> </del>	ļ
		: : : : : <b> </b> _						<del> </del>	ļ
nput Loadin	g Factor	Pin Name —		····	-			<u> </u>	
	1 <i>l</i> u	A,B					<del> </del>	<u> </u>	
		l F						<u> </u>	
Output Drivin	ng Factor	Pin Name							
		<b></b>							
	10 ℓu	х _							ļ
		<u> </u>					ļ	-	
TTL Equivale	ent Circuit								
	****								
	74532 74L532								
		<b>」</b>							
	L.								
		74510 74L510							
AV-G34	-E1						G34	Sheet 1/1	

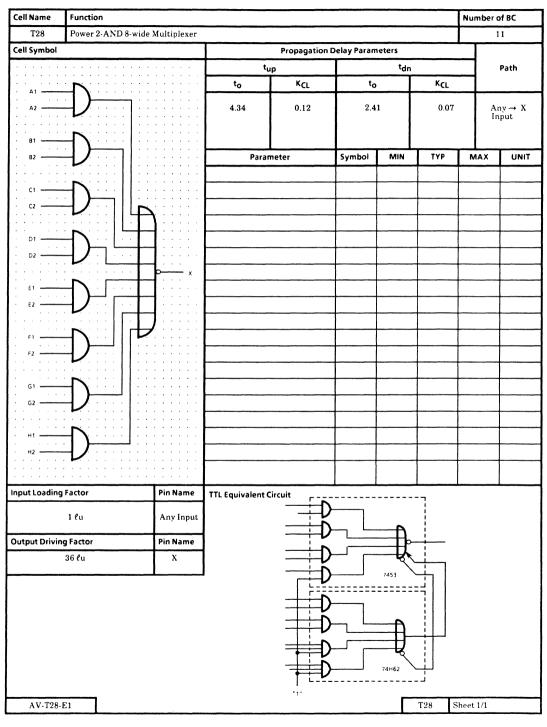
Cell Name	Function							Number	of BC
G44	2-wide 2-AND 2-OR 4	-input OR-AN	D-Inverter						2
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	ıp		<sup>t</sup> dn			Path
			to	KCL	to		KCL		
A1 ———	``````````````````````````````````````	1.72 0.60		0.58		0.35	Α, Ι	$A, B, C \rightarrow X$	
Α2	プ <del>レーニーー</del>		Parar	neter	Symbol	MIN	TYP	MAX	UNIT
C	Factor 1 lu	Pin Name							
							ļ		
Output Drivin	g Factor	Pin Name							
	10 ℓu	х							
TTL Equivaler	74551 74551		74504 74L504 74L500 74L500						

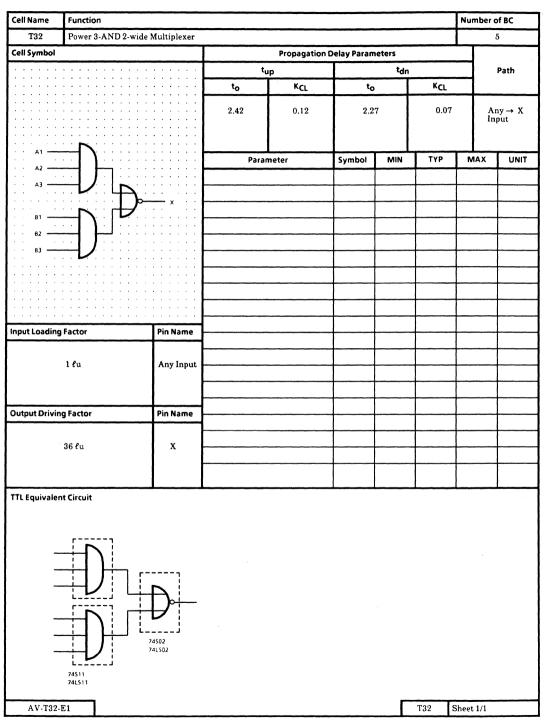
## **Multiplexer Family**

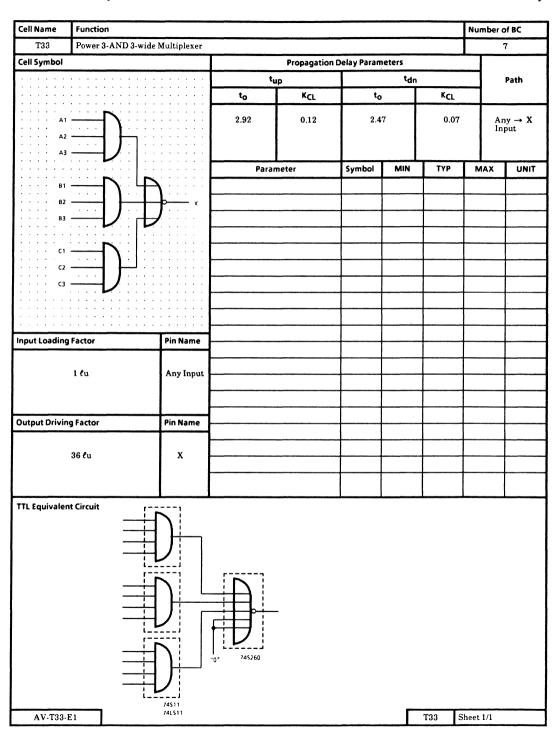
Page	Unit Cell Name	Function	Basic Cells
3-77	T24	Power 2-AND 4-wide Multiplexer	6
3-78	T26	Power 2-AND 6-wide Multiplexer	9
3-79	T28	Power 2-AND 8-wide Multiplexer	11
3-80	T32	Power 3-AND 2-wide Multiplexer	5
3-81	T33	Power 3-AND 3-wide Multiplexer	7
3-82	T34	Power 3-AND 4-wide Multiplexer	9
3-83	T42	Power 4-AND 2-wide Multiplexer	6
3-84	T43	Power 4-AND 3-wide Multiplexer	9
3-85	T44	Power 4-AND 4-wide Multiplexer	11
3-86	U24	Power 2-OR 4-wide Multiplexer	6
3-87	U26	Power 2-OR 6-wide Multiplexer	9
3-88	U28	Power 2-OR 8-wide Multiplexer	11
3-89	U32	Power 3-OR 2-wide Multiplexer	5
3-90	U33	Power 3-OR 3-wide Multiplexer	7
3-91	U34	Power 3-OR 4-wide Multiplexer	9
3-92	U42	Power 4-OR 2-wide Multiplexer	6
3-93	U43	Power 4-OR 3-wide Multiplexer	9
3-94	U44	Power 4-OR 4-wide Multiplexer	11



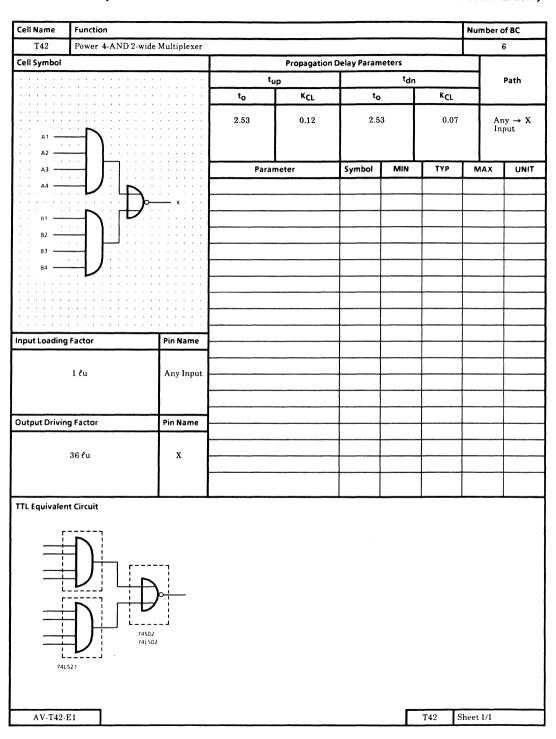


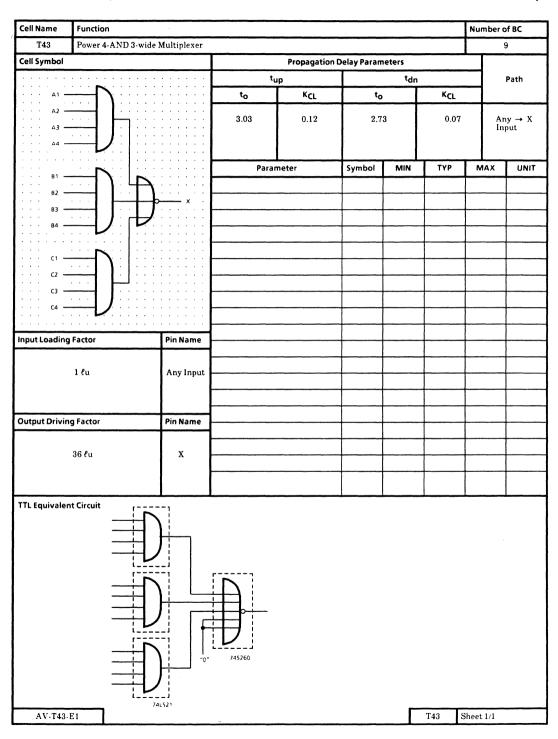


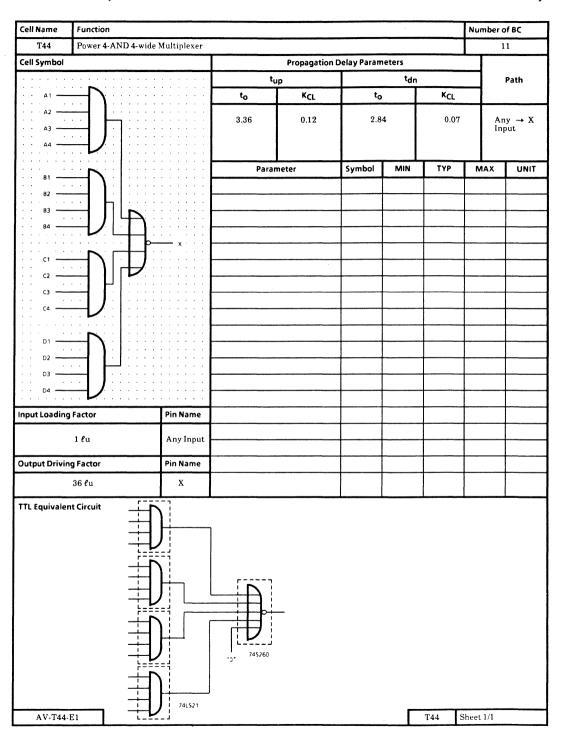


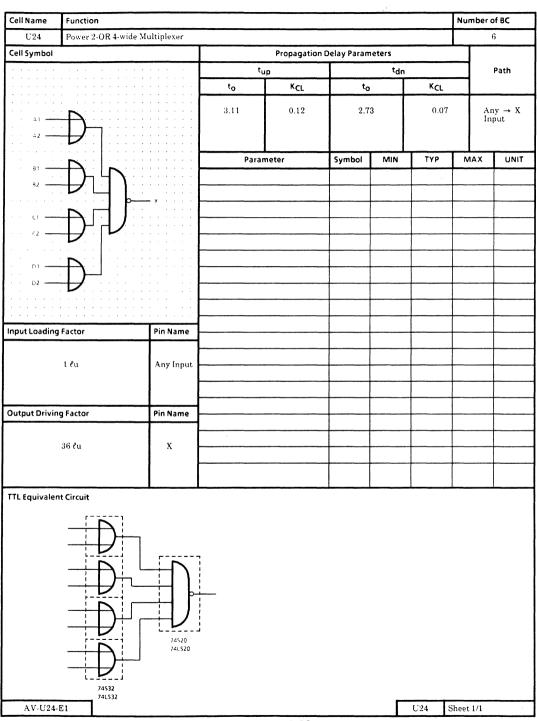


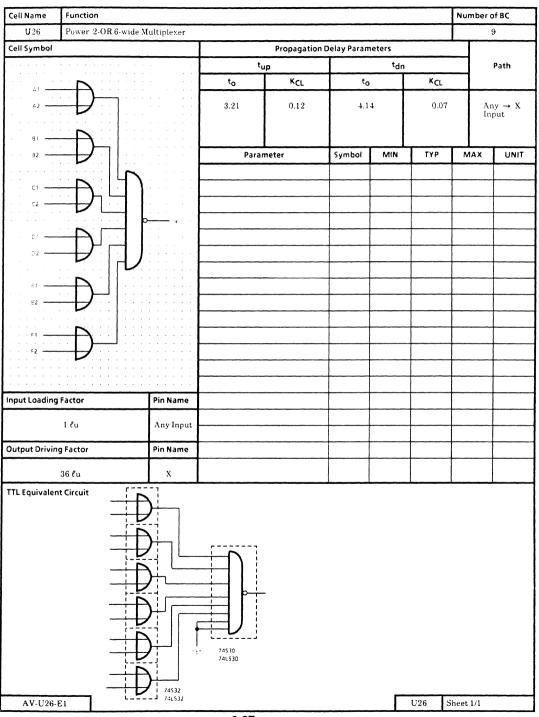
Cell Name	Function							Number	of BC
T34	Power 3-AND 4-wide	Multiplexer							9
Cell Symbol					n Delay Param	eters			
A1			t <sub>t</sub>			<sup>t</sup> dn			Path
A2 —	<u>                                    </u>		t <sub>o</sub>	KCL	to		KCL		
A3 —	<b>一</b> レ		3.25	0.12	2.5	8	0.07	A	ny → X nput
в2 —			Para	neter	Symbol	MIN	TYP	MAX	UNIT
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		×							
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c3 —							+	<b></b>	
D1 —	_				-		+	<del> </del>	+
D2							1		
D3 —	<b></b> ノ								
Input Loading	Factor	Pin Name							
	1 <b>l</b> u	Any Input					+		ļ
		<b>l l</b>					+	-	1
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Output Drivin	ng Factor	Pin Name		·			1		
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TTL Equivaler	nt Circuit r-								
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	<u> </u>	74511 74L511							
AV-T34-	E1	74LS11				Γ	T34 5	Sheet 1/1	

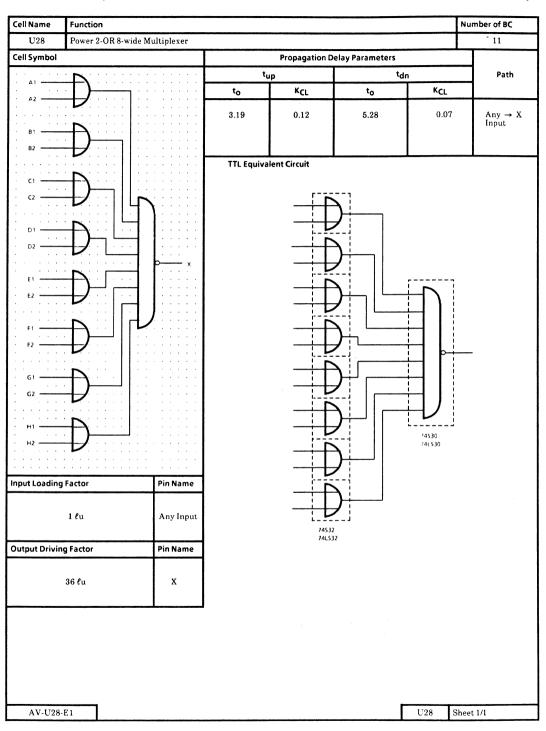






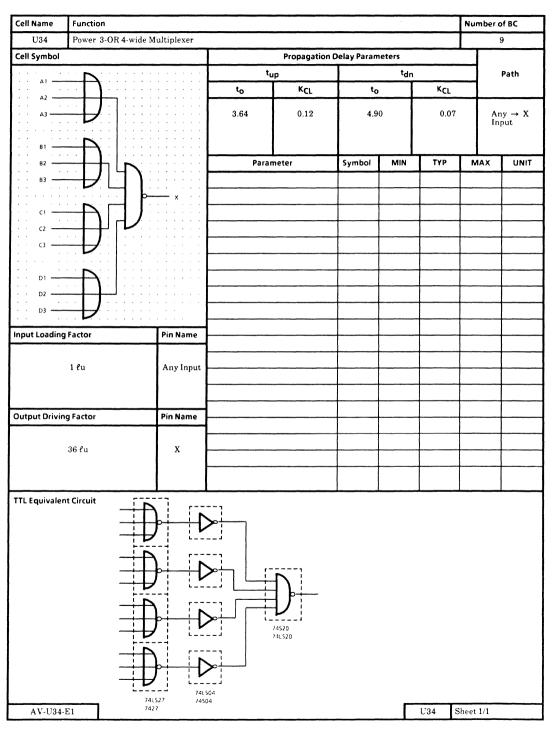


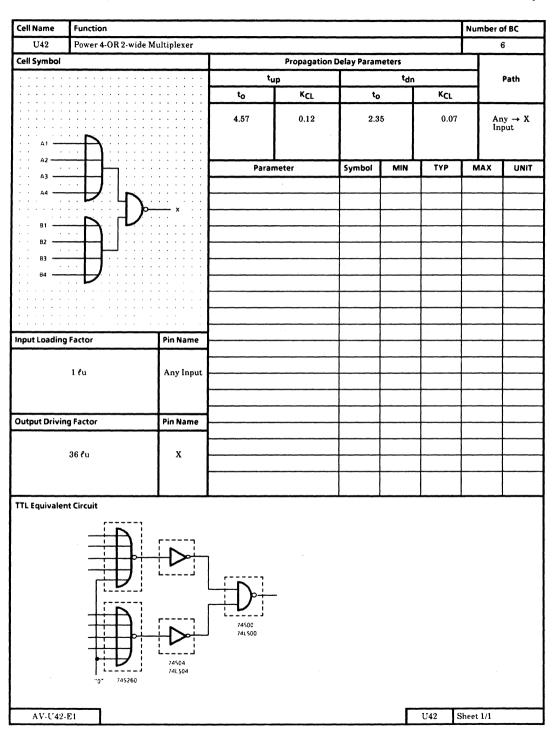


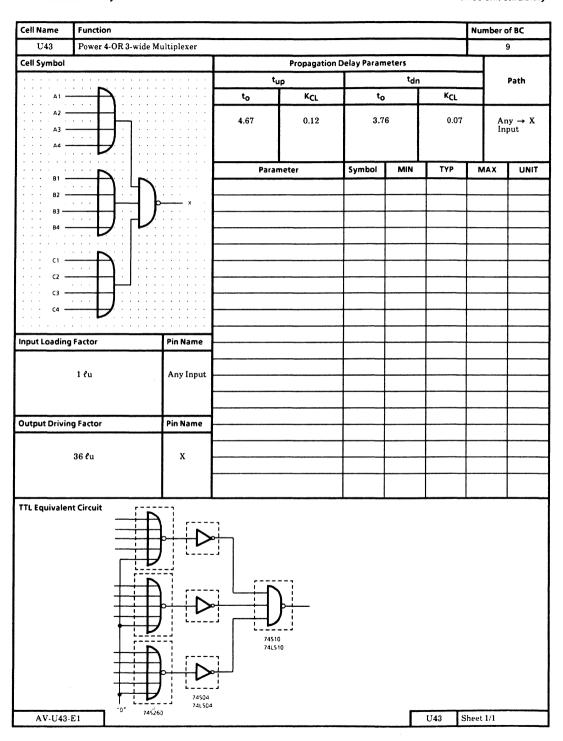


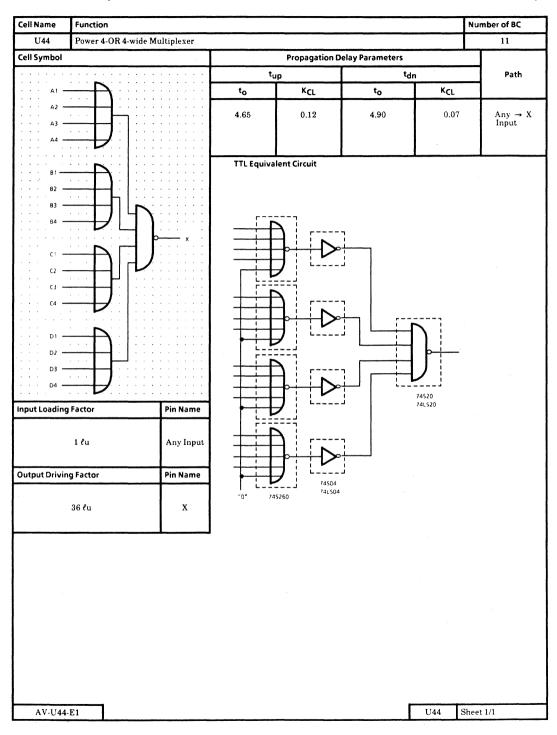
Cell Name	Function							Number	of BC	
U32	Power 3-OR 2-wide Mu	altiplexer							5	
Cell Symbol				Propagation	Delay Param	eters				
			tu	р		<sup>t</sup> dn			Path	
			to	KCL	to		K <sub>CL</sub>			
			3.56	0.12	2.35		0.07	Ai	Any → X Input	
A1 —	<del>                                   </del>	: : : : : <b> </b>	Paran	neter	Symbol	MIN	TYP	MAX	UNIT	
81 ————————————————————————————————————	Factor	Pin Name								
	1 lu	Any Input								
Output Drivin	g Factor	Pin Name –							ļ	
	36 fu	х								
TTL Equivalen	nt Circuit	LL					1		L	
- - - -			74500 741500							
AV-U32-1	E1					Г	U32 S	heet 1/1		

Power 3-OR 3-wide Multiplexer	lame Fu	nction							Number	of BC
tup tdn  to KCL to KCL  3.66 0.12 3.76 0.07  A2 A3 Parameter Symbol MIN TYP MAX  B1 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		wer 3-OR 3-wide Mu	ltiplexer							7
to KCL to KCL  3.66 0.12 3.76 0.07  Parameter Symbol MIN TYP MAX  1 2 2 3 3 3 4 3 4 3 4 3 4 4 4 4 4 4 4 4 4	ymbol				Propagation	n Delay Param	eters			
Input Loading Factor  I fu Any Input  Output Driving Factor  Pin Name  36 fu X  TTL Equivalent Circuit				ŧ, t	р		<sup>t</sup> dn			Path
A2 A3 Parameter Symbol MIN TYP MAX  81 82 83 C1 C2 C3 C3 Input Loading Factor Pin Name 1 ℓu Any Input  Output Driving Factor Pin Name 36 ℓu X  TTL Equivalent Circuit				to	KCL	to		KCL		
Parameter Symbol MiN TYP MAX  81 82 83  Input Loading Factor Pin Name  1 fu Any Input  Output Driving Factor Pin Name  36 fu X	A2				0.12	3.76		0.07	A: In	ny → X put
Input Loading Factor  I du  Any Input  Output Driving Factor  Pin Name  36 du  X		<del>. []</del> : [ : : : :		Parar	neter	Symbol	MIN	TYP	MAX	UNIT
36 lu X  TTL Equivalent Circuit	82	tor								
36 lu X  TTL Equivalent Circuit	It Driving Fac	ctor	Pin Name							
TTL Equivalent Circuit										
	36 €	lu .	Х							
74510 74L510 AV-U33-E1 74L527 74L504 74L504		7427	74	74 /4			-			







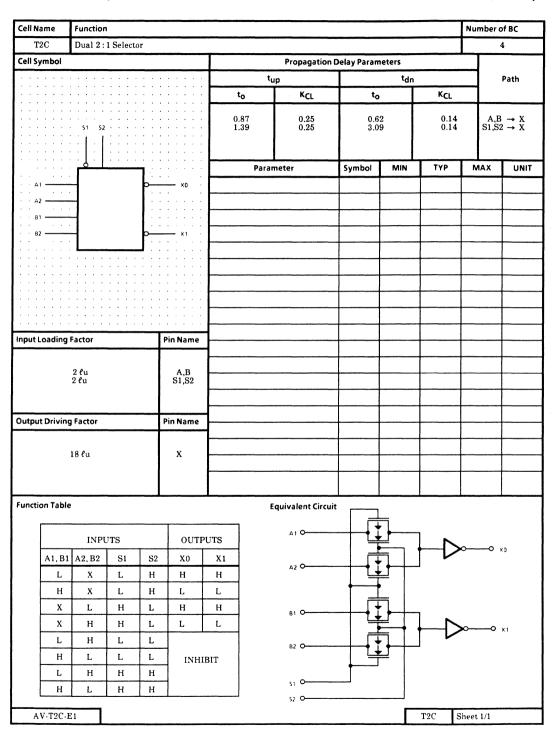


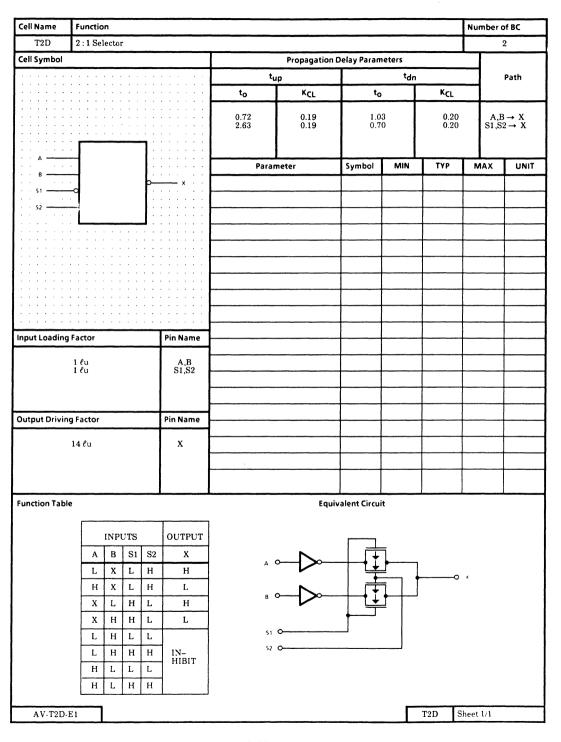
## **Selector Family**

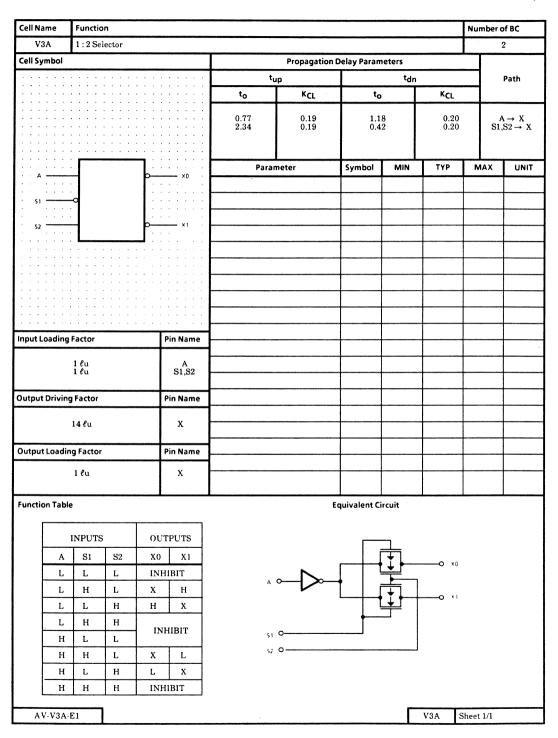
Page	Unit Cell Name	Function	Basic Cells
3-97	T2B	2:1 Selector	2
3-98	T2C	Dual 2:1 Selector	4
3-99	T2D	2:1 Selector	2
3-100	V3A	1:2 Selector	2
3-101	V3B	Dual 1:2 Selector	3
3-102	T5A	4:1 Selector	5

3

Cell Name	Function										Numbe	er of BC
T2B	2:1 Selecti	or										2
Cell Symbol						Propagation Delay Parameters						
						tu	р		<sup>t</sup> dn			Path
					t	0	KCL	to		K <sub>CL</sub>		
					0.1	87	0.25	0.6	2	0.14		Δ R Y
					1.3	39	0.25	3.0	9	0.14	s	$\begin{array}{c} A,B \to X \\ 1,S2 \to X \end{array}$
											- 1	
· · A		1:			-	Parar	neter	Symbol	MIN	ТҮР	MAX	UNIT
в —								1 ,				
· · S1 ———	-9	<b>f</b> :						1.				-
· · s2	-	1:						+		<b>†</b>		
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Input Loading	Factor		Pin	Name	]			-				
					<b>—</b>			-		ļ		
	2 <b>l</b> u 1 lu		Ι.	A,B S1,S2	ļ		· · · · · · · · · · · · · · · · · · ·	<del> </del>				
	1 tu			31,32				-				
					<u> </u>			-				_
Output Drivin	g Factor		Pin	Name								
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	18 ℓu			X				-				
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Function Tabl	e						Equivale	ent Circuit				
		·				7						
		INP	UTS	1	OUTPUT							
		АВ	Sı		X	1			<u>_</u>			
		L X	L	Н	H	1	Δ Ο		· ‡	<b>-</b> .		
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		L H	L	L	НІВІТ		,, 0 —					
		L H	Н	Н								
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AV-T2B-	E1									T2B S	heet 1/1	

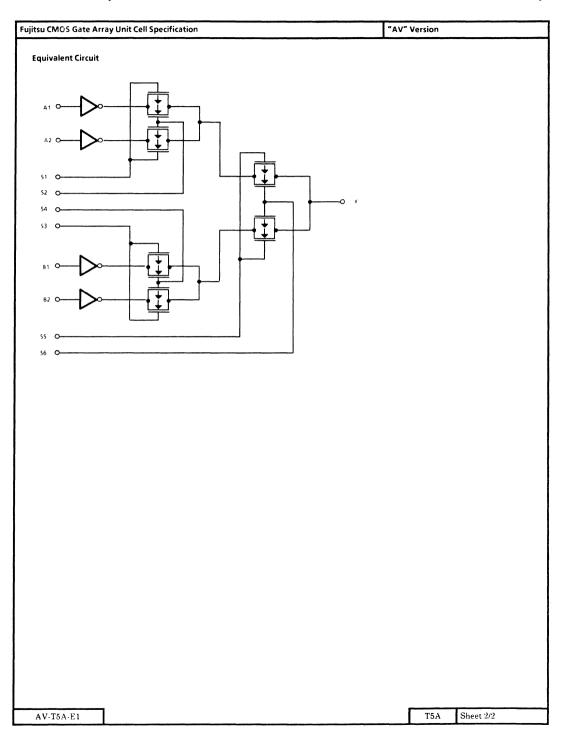






Cell Name	Funct	ion								Number	of BC
V3B	Dual	1 : 2 Sel	ector								3
Cell Symbol	***************************************					Propagation	Delay Paran	eters			
					t <sub>t</sub>	ıp	tdn			Path	
					to	KCL	to		KCL		
					$0.77 \\ 2.34$	0.19 0.19	1.1 0.4	8 2	$0.20 \\ 0.20$	A. S1,	$\begin{array}{c} B \rightarrow X \\ S2 \rightarrow X \end{array}$
							1	1			
			<b>—</b>	: : : : <b>L</b>	Para	neter	Symbol	MIN	TYP	MAX	UNIT
· A	_		þ-	xo ·						*	
В ——	-1		þ-	x1							
51	⊸		þ.	x2							
52 ——			þ	хз							
	: L										
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									-		
nput Loading	Factor			Pin Name —							
	1 <b>l</b> u			A.B							
	1 <b>l</b> u 2 <b>l</b> u			A,B S1,S2							<b></b>
				<u> </u>							
Output Drivin	g Facto	r		Pin Name			+				
										······································	
	14 ℓu			X			<b>+</b>				
Output Loadii	ng Facto	or		Pin Name							
	1ℓu			х			<del> </del>				
Function Tabl	e					Equivalent Circ	uit	1			
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I	NPUTS	,	OUT	PUTS		. N.			O x0		
A,B	S1	S2	X0, X2	X1, X3	Д	<b>─</b> D⊶	1   =				
L	L	L	INH	IBIT					O x1		
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L	L	Н	Н	Х			[		_		
L	Н	Н							O X2		
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L					52	<u> </u>					

Cell Name	1	Functi	on													Number o	of BC
T5A		4:1 S	elector	r													5
Cell Symbo	ol									Propag	ation [	Delay Param	eters				
										tup			td	n		]	Path
	: :								to	Kc	L	to		Kc	L		
								1.	48	0.1	9	1.13			20 20	A,E	$\begin{array}{c} 3 \rightarrow X \\ S4 \rightarrow X \\ S6 \rightarrow X \end{array}$
			52 S3	8 S4				2.	22 63	0.1 0.1	9	1.25 0.70			20	S5 ~	$S6 \rightarrow X$
									Pa	rameter		Symbol	MIN	TYP	Т	MAX	UNIT
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. A2		ł			_	· · · · ·						-		_	+		
. B1 —		1										1		+	$\top$		
B2		1													+		
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		\$5	s6 · ·							****					$\top$		
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nput Loadi	ng ra	actor			_	Pin Nar	ne										
	1	ℓu ℓu				A,B S1 ~	S6										
	•	·u				51											
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Output Driv	ving f	Factor			$\neg$	Pin Nan	ne								$\perp$		
					$\neg$										_		
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Function Ta	ble																
										1	ì						
				INI	PUTS	}				OUTPUT							
A1	A2	Bı	B2	Sı	S2	S0	Sı	S5	S6	x	Δ.	1 ≠ A2 → S	1 = 52 0	r S5 – S6	Inhil	nit	
L				L	Н			L	Н	Н		$1 \neq B2 \rightarrow S$					
н		ļ		L	Н			L	н	L		$1 \neq B2 \rightarrow S6$ $1, A2 \neq B3$					
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			Н	<u> </u>		Н	L	Н	L	L							
			1										r		Tai		
AV-T5	A-E1	l												T5A	She	eet 1/2	



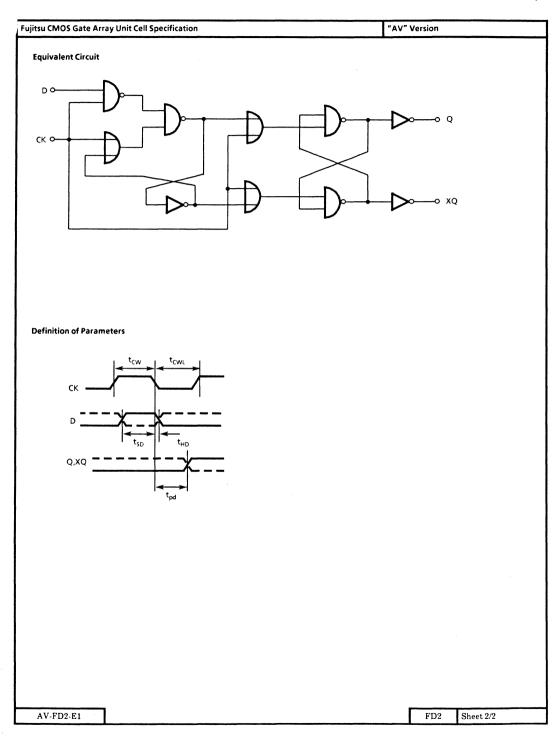
3

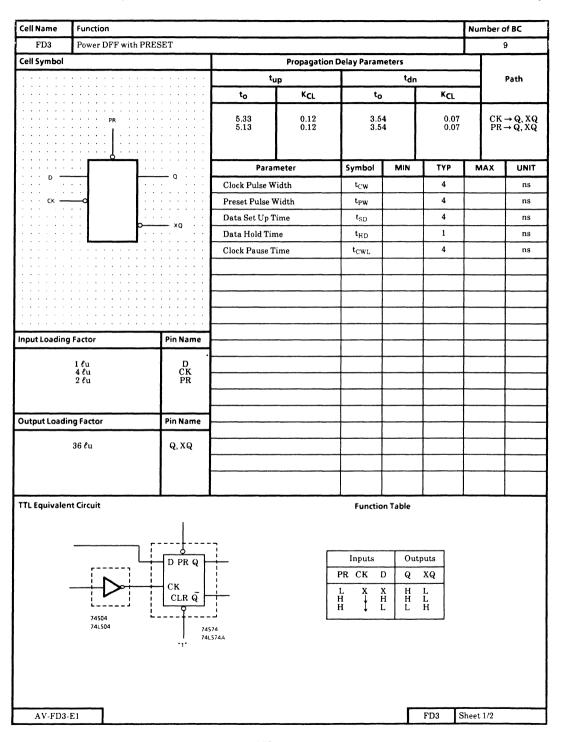
## Flip-Flop Family

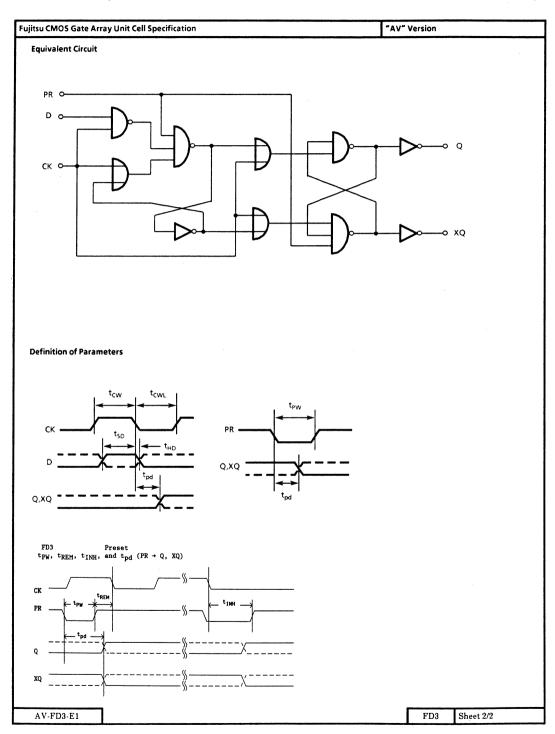
Page	Unit Cell Name	Function	Basic Cells
3-107	FD2	Power D FF	8
3-109	FD3	Power D FF with Preset	9
3-111	FD4	Power D FF with Clear and Preset	10
3-113	FD5	Power D FF with Clear	9
3-115	FD6	D FF	7
3-117	FD7	D FF with Clear	8
3-119	FD8	D FF and Latch	9
3–121	FDD	Positive Edge Clocked Power D FF with Clear and Preset	11
3-123	FDE	Positive Edge Clocked Power D FF with Clear	10
3-125	FDG	Positive Edge Clocked D FF with Clear	9
3-127	FDM	D FF	6
3-129	FDN	D FF with Set	7
3-131	FDO	D FF with Reset	7
3-133	FDP	D FF with Set and Reset	8
3-135	FDQ	4-bit D FF	21
3-137	FDR	4-bit D FF with Clear	26
3-139	FDS	4-bit D FF	20
3-141	FJ4	Power J-K FF with Clear	11
3-143	FJ5	Power J-K FF with Clear and Preset	12
3-145	FJD	Positive Edge Clocked Power J-K FF with Clear	12

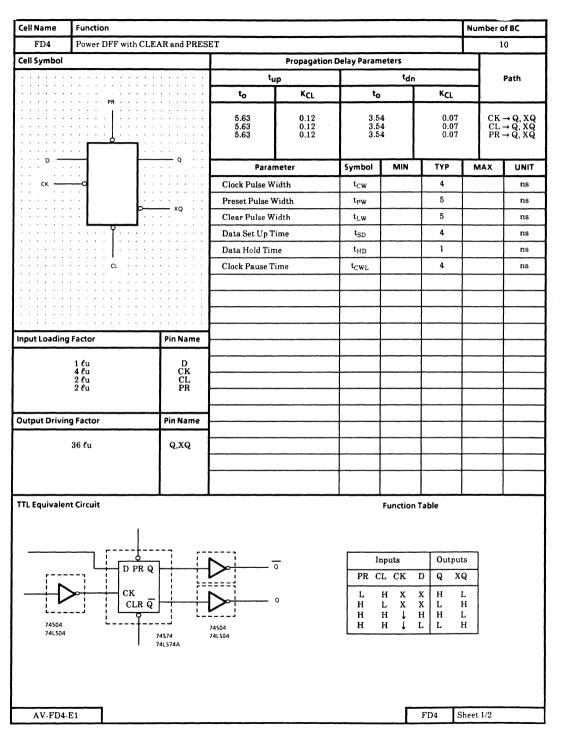
3

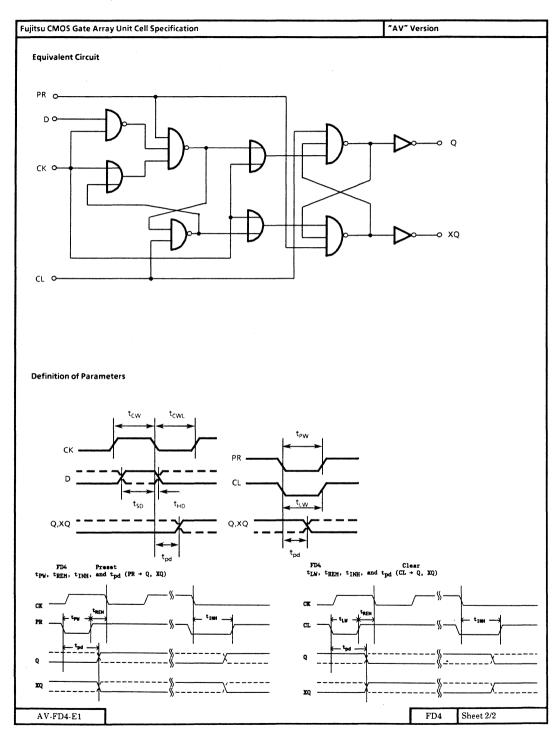
Cell Name	Function							Number	of BC
FD2	Power DFF								8
Cell Symbol				Propagation	Delay Param	eters			
			1	up		<sup>t</sup> dn			Path
			to	KCL	to		K <sub>CL</sub>		
			4.83	0.12	3.2	4	0.07	СК	i → Q, XQ
			Para	meter	Symbol	MIN	TYP	MAX	UNIT
D		— o · · · ·	Clock Pulse V	Width	t <sub>CW</sub>		4		ns
ск —			Data Set Up	Time	$t_{\mathrm{SD}}$		4		ns
			Data Hold Ti	me	t <sub>HD</sub>		1		ns
			Clock Pause	Time	t <sub>CWL</sub>		3		ns
							1		
							ļ		
									ļ
Input Loading	g Factor	Pin Name			ļ				-
					-		<del> </del>		<del> </del>
	1 <b>l</b> u <b>4 l</b> u	D CK			-				-
							<del> </del>	<b> </b>	
					-		<del>                                     </del>		-
Output Loadi	ng Factor	Pin Name					<del> </del>		<del> </del>
	36 ℓu	Q,XQ			1		-		
	0014	4,4			-		+	<del> </del>	<del> </del>
			<del></del>		<del> </del>		+		<u> </u>
TTL Equivale	nt Circuit			Fu	nction Table				
		"1"							
		-};							
		PR		Inp	uts Outp	outs			
	D	Q		CK					
	CI	l i		1 1	H H L L	L H			
		CR CR	-	Ļ					
		1							
		"1"							
	74S04 74LS04	74574 74L574	ıΔ						
		,,							
AV-FD2-	F1					_	FD2 S	heet 1/2	
WA-L D7-	<u> </u>						104		

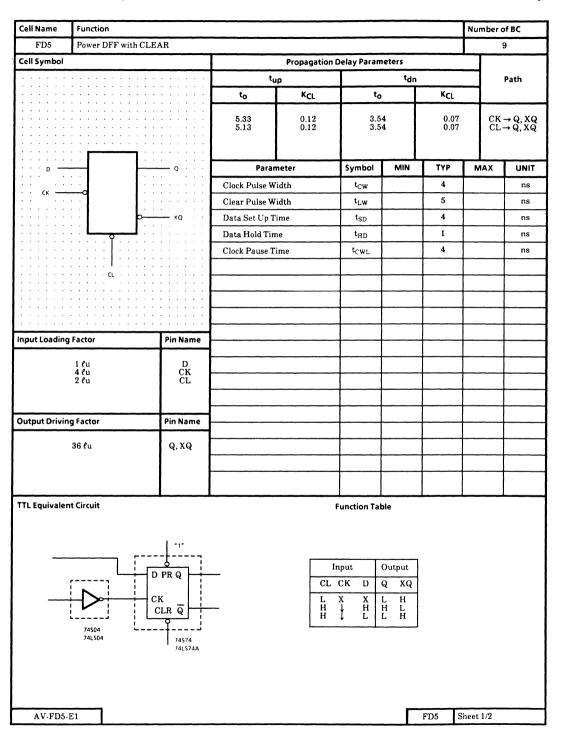


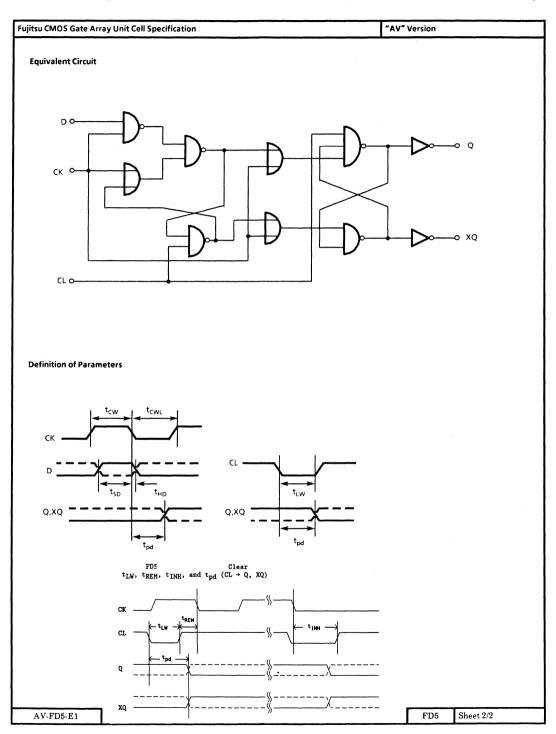




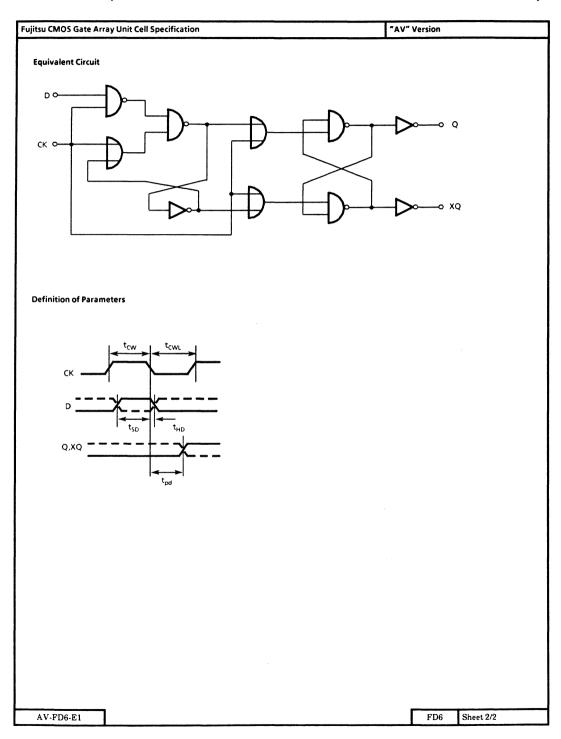


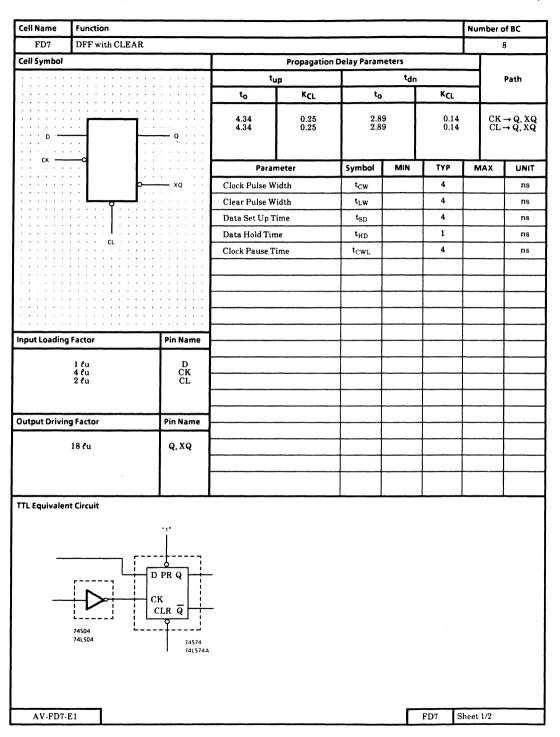


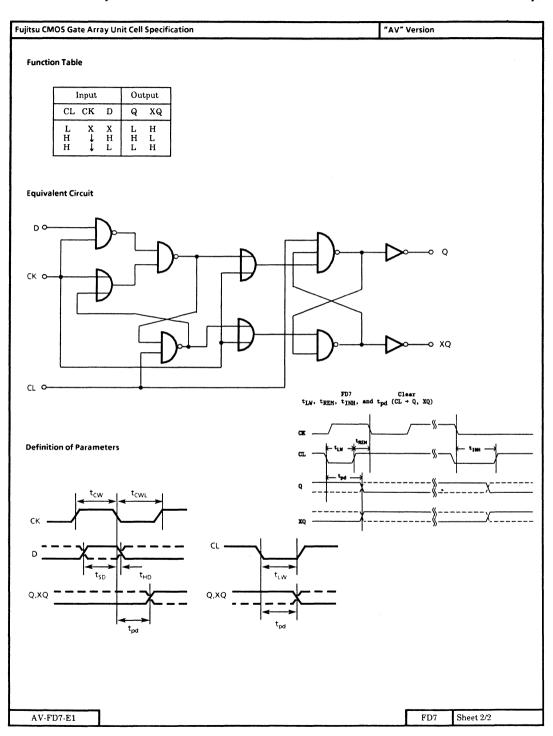


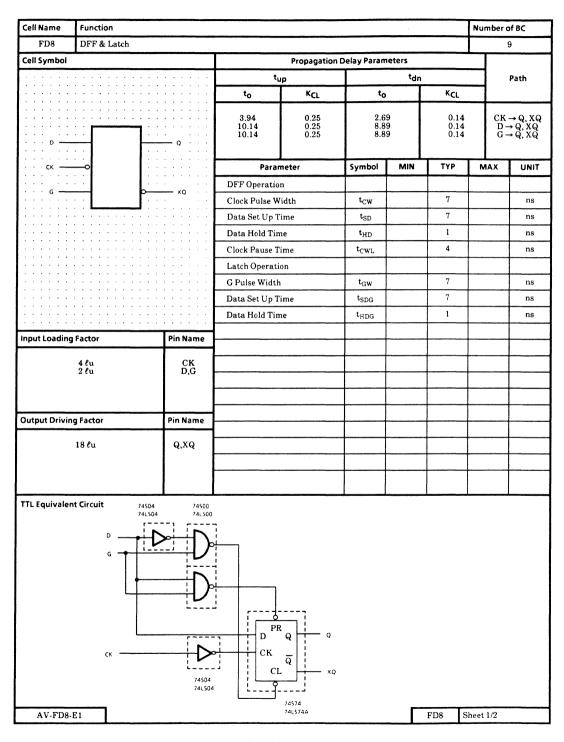


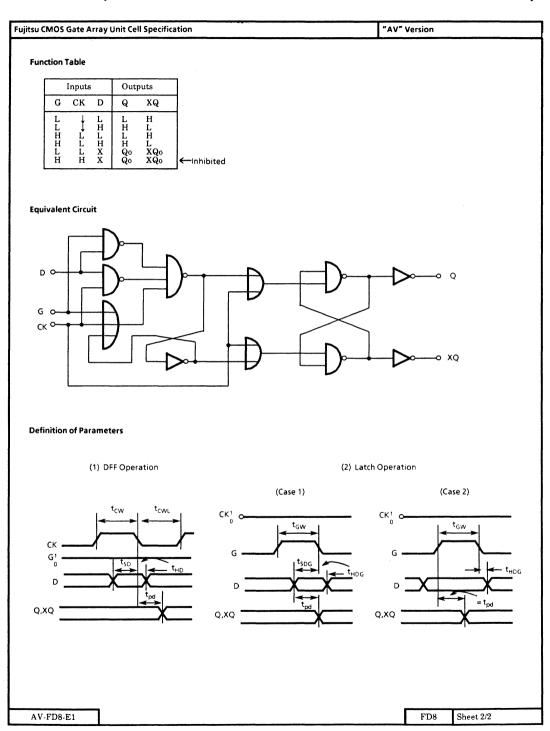
Cell Name	Function				<del></del>			Number	of BC
FD6	DFF								7
Cell Symbol				Propagation	n Delay Param	eters			
			t	up		<sup>t</sup> dr	·		Path
			to	KCL	to		KCL		
			3.94	0.25	2.6		0.14	CV	$C \rightarrow Q, XQ$
			3.34	0.23	2.0		0.14		Q, A.Q
								j	
			Dava	meter	Symbol	MIN	TYP	MAX	UNIT
		_ o · · ·				IVIIN	4	MAA	-
			Clock Pulse V		t <sub>CW</sub>		4	<del>                                     </del>	ns
· · · CK —			Data Set Up		t <sub>SD</sub>				ns
	p	xQ · ·	Data Hold Ti		t <sub>HD</sub>		1		ns
			Clock Pause	l'ime	t <sub>CWL</sub>		3	ļ	ns
							-		-
									<del> </del>
								ļ	<b></b>
nput Loading	Factor	Pin Name							-
	1.0	_					-		ļ
	1 lu 4 lu	D CK						<u> </u>	ļ
							<del></del>		<del> </del>
								ļ	<del> </del>
Output Drivin	g Factor	Pin Name					-		<del> </del>
	10.4	0.40			_				ļ
	18 ℓu	Q,XQ			_		<del> </del>		<del> </del>
					_		-		
TTL Equivaler	nt Circuit				Function	on Table		•	<del></del>
		۱ ",٠							
			7		Γ	Τ			
	1 :	D PR Q	-		Input	Outp			
		1			CK D	QX			
		CK _			↓ H ↓ L	1	L H		
	L	CLR Q	+						
	74S04 74LS04	<u>γ</u>	i						
	<b>b</b> .	745	. <b></b> 74						
		74L	574A						
		″1 <b>″</b>							
	E1						FD6	heet 1/2	

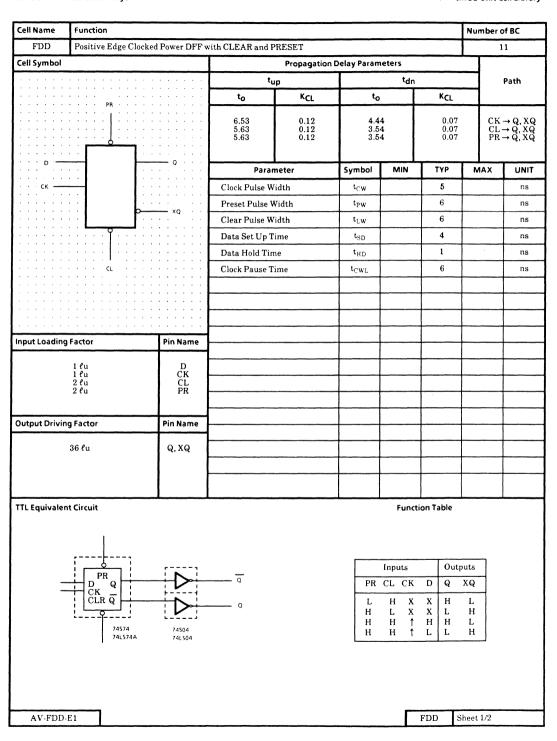


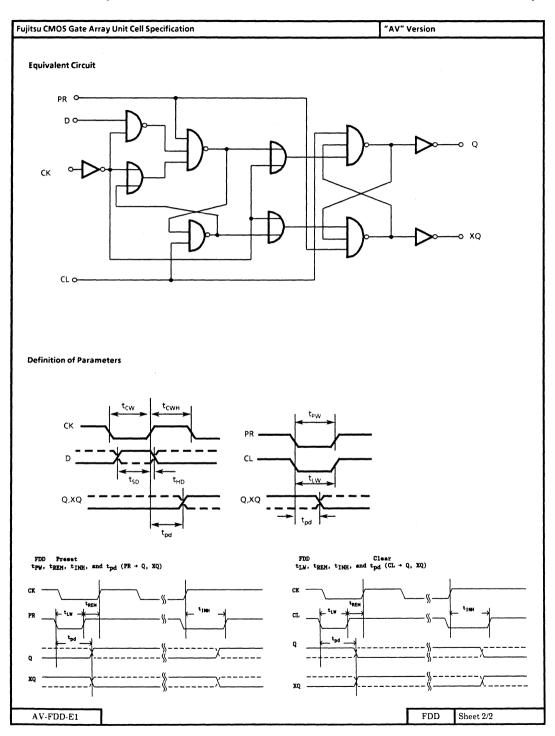


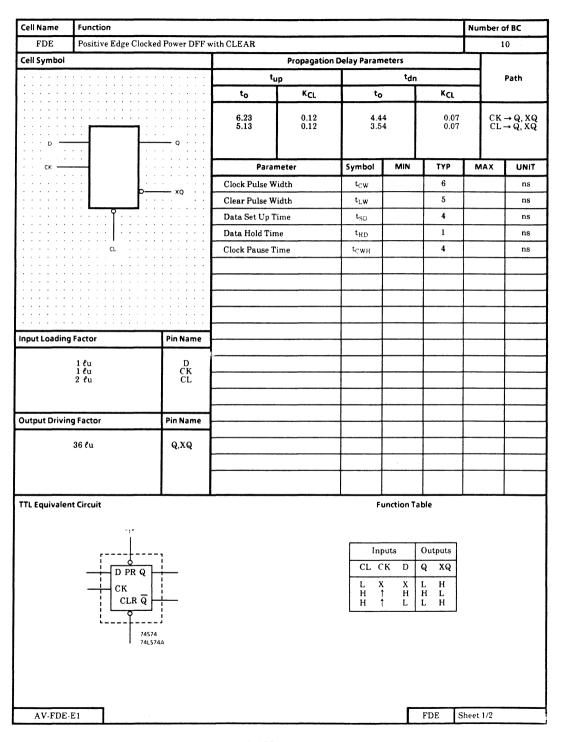


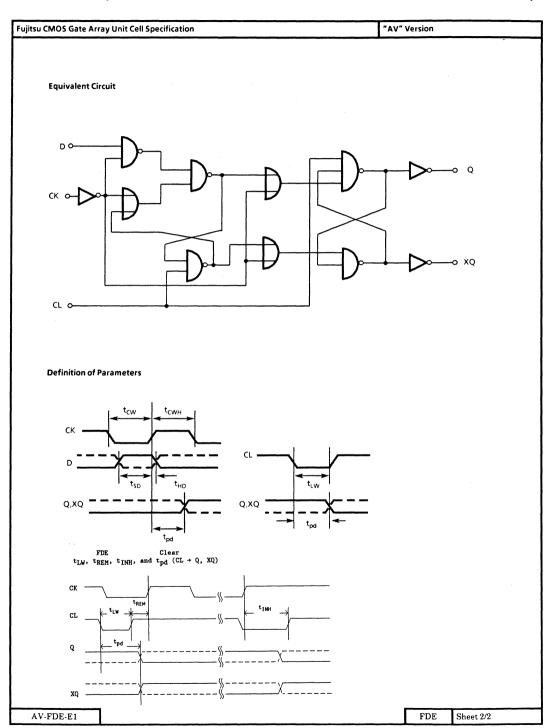




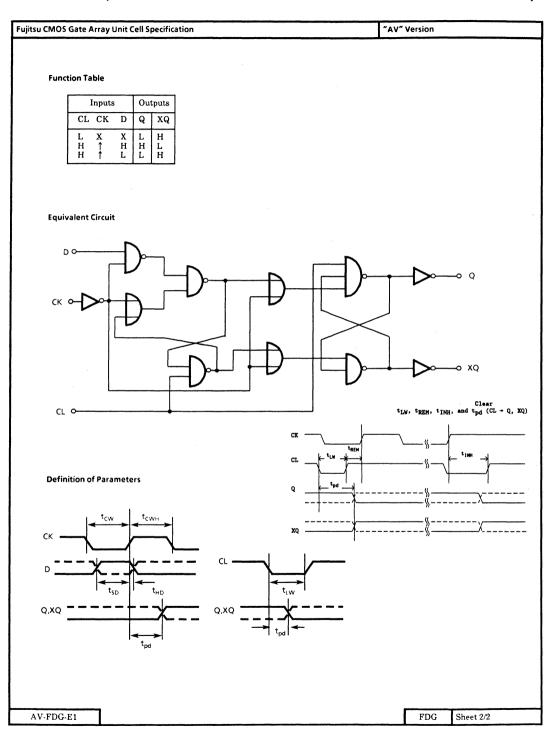


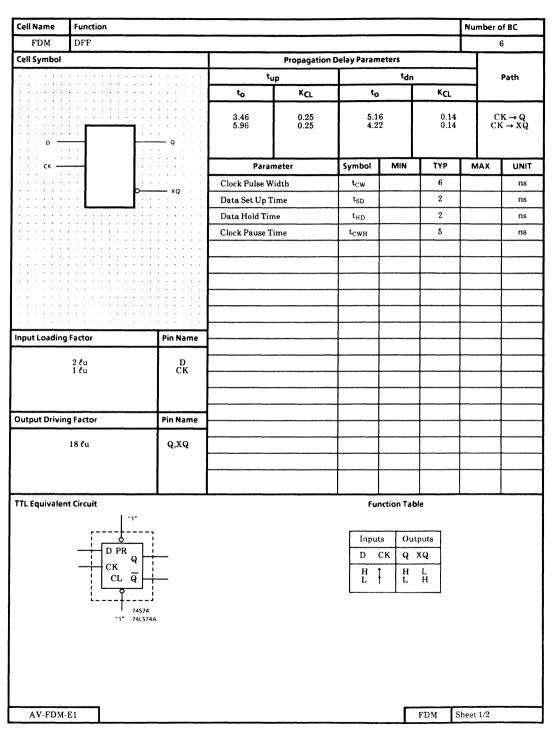


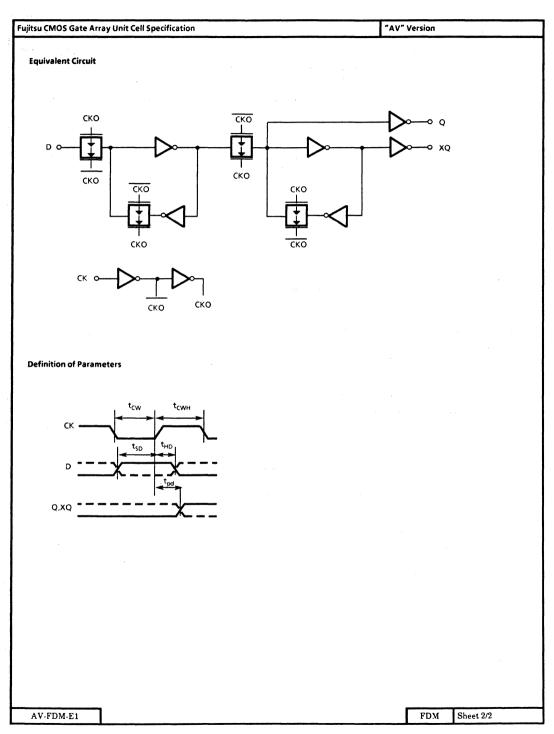




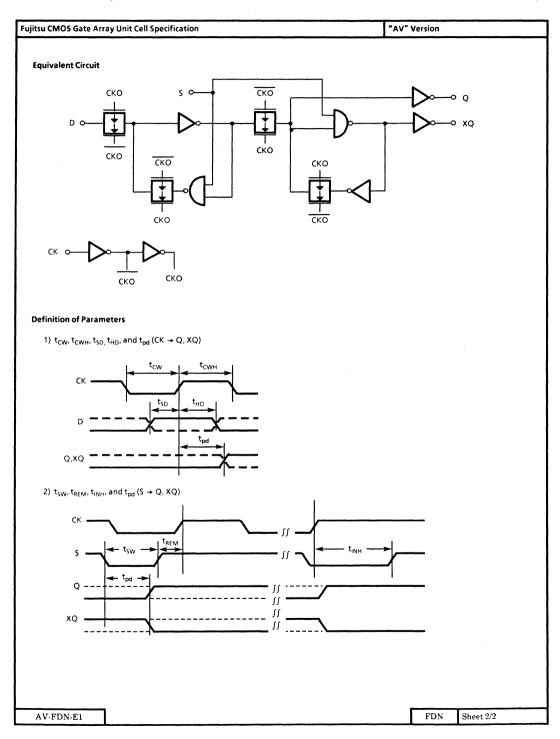
Cell Name	Function							Number	of BC
FDG	Positive Edge Clocked	DFF with CL	EAR	9					
Cell Symbol									
			t,	ıb		<sup>t</sup> dr	)		Path
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
D		— Q	5.24 4.14	0.25 0.25	3.79 2.89	9	0.14 0.14	CK CL	→ Q, XQ → Q, XQ
ск —			Para	meter	Symbol	MIN	TYP	MAX	UNIT
			Clock Pulse V		t <sub>CW</sub>		6		ns
		xQ · ·	Clear Pulse W		t <sub>LW</sub>		4		ns
	· · · · · · · · · · · · · · · · · · ·		Data Set Up 7		t <sub>SD</sub>		4		ns
			Data Hold Tir		t <sub>HD</sub>		1		ns
	CL		Clock Pause T		t <sub>CWH</sub>		4		ns
Input Loading	Factor	Pin Name							
	1 lu 1 lu 2 lu	D							
	2 lu	D CK CL							
Output Drivin	a Factor	Pin Name							
- Catpat Billion	gractor	riii Naiile							
	18 ℓu	Q, XQ				· · · · · · · · · · · · · · · · · · ·			
TTL Equivaler	A Circuit						_1		L
	D PR Q CK CLR Q 74574 74157								
AV-FDG-	E1						FDG S	heet 1/2	



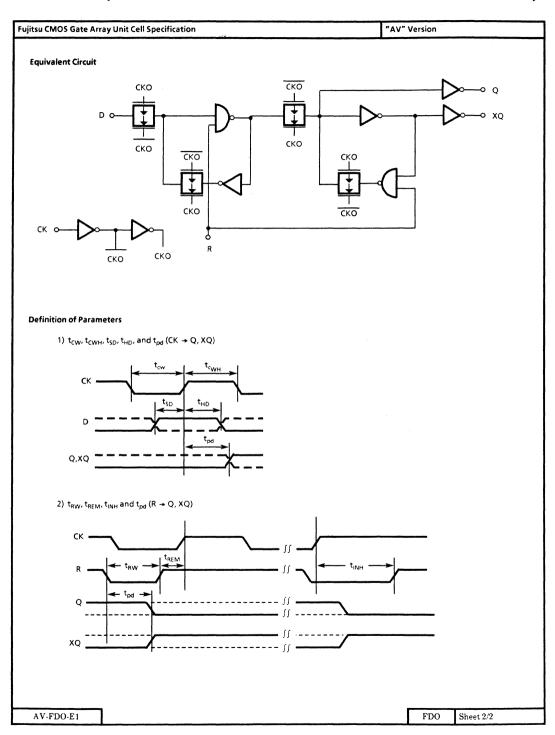


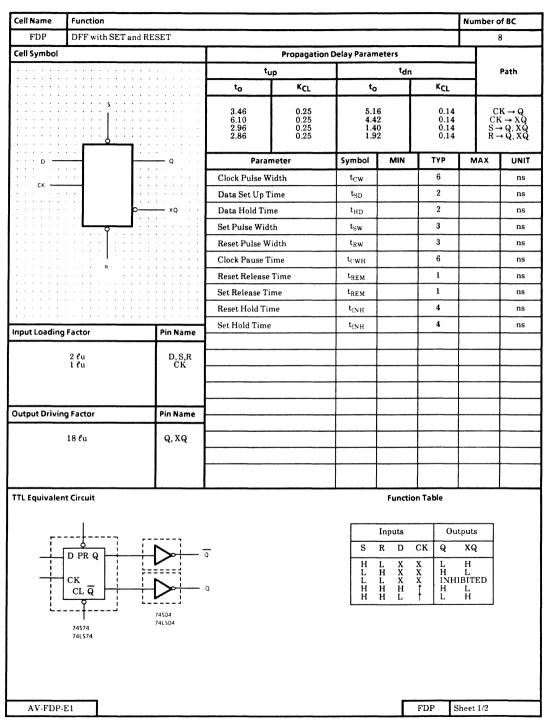


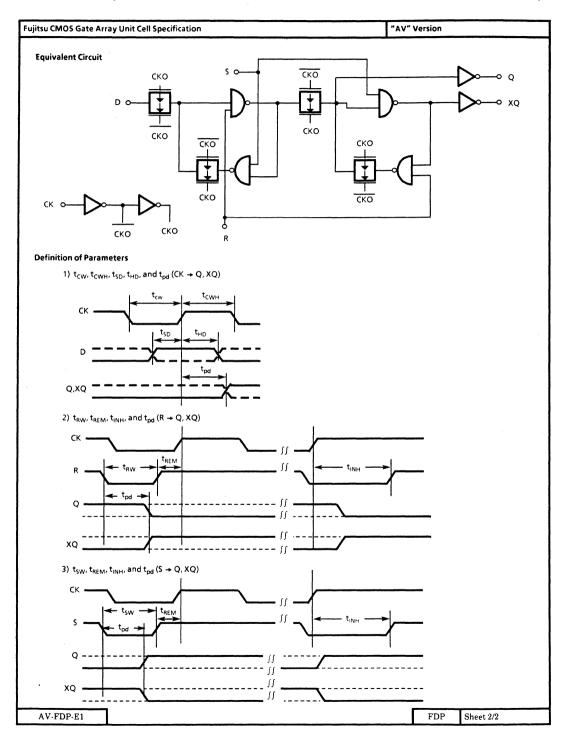
Cell Name	Function							Number	of BC
FDN	DFF with SET								7
Cell Symbol				Propagation	n Delay Paran	neters			
			t <sub>up</sub>			<sup>t</sup> dn			Path
			t <sub>o</sub>	K <sub>CL</sub>	to	,	K <sub>CL</sub>		
	s		3.46 6.10 2.82	0.25 0.25 0.25	5.1 <b>4.</b> 4 1.4	2	0.14 0.14 0.14	CI S-	$K \rightarrow Q$ $K \rightarrow XQ$ $\rightarrow Q, XQ$
<sub>D</sub>	<u> </u>	<u> </u>	Paran	neter	Symbol	MIN	TYP	MAX	UNIT
			Clock Pulse W	idth	t <sub>CW</sub>		6		ns
ск —			Data Set Up Ti	me	t <sub>SD</sub>		2		ns
		×Q	Data Hold Tim	ie	t <sub>HD</sub>		2		ns
			Set Pulse Widt	h	t <sub>SW</sub>		3		ns
			Clock Pause Ti	me	t <sub>CWH</sub>		6		ns
			Set Release Ti	me	t <sub>REM</sub>		1		ns
			Set Hold Time		t <sub>INH</sub>		4		ns
Input Loading	Factor	Pin Name				ļ			ļ
	2 <b>l</b> u	D.S			-		-		<del> </del>
	1 <i>l</i> u	D, S CK					+		<u> </u>
Output Drivin	a Factor	Pin Name							
Output Divini	gracion	rintaine							
	18 <b>ℓ</b> u	Q, XQ							
							-		
TTL Equivalen	nt Circuit				<del></del>	Functio	n Table		<b></b>
								,	
	[					Inputs	Outputs	1	
	D PR Q	<del> </del>			S	D CK		1	
	CK CL Q				L H	X X H ↑ L ↑	H L		
	9				Н	L †	L H		
	7457								
	"1" 74LS	74A							
AV EDN	F1					_	EDN: I di	neet 1/2	
AV-FDN-	E1						FDN SI	ieet 1/2	

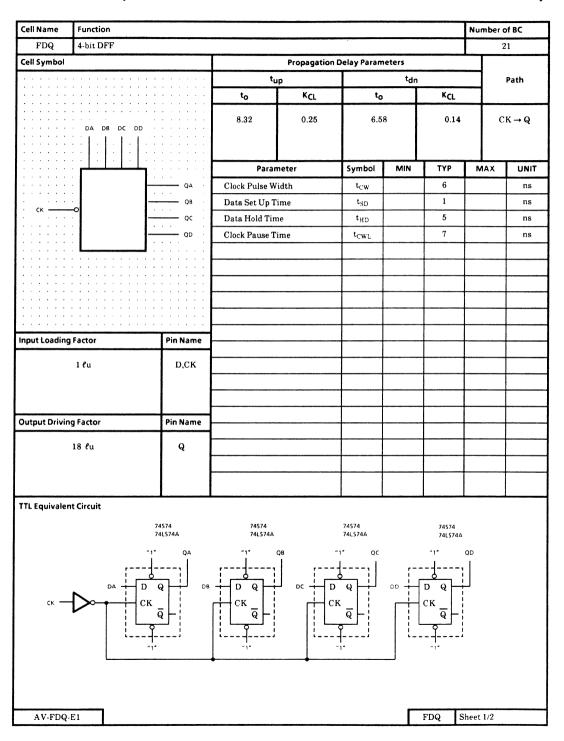


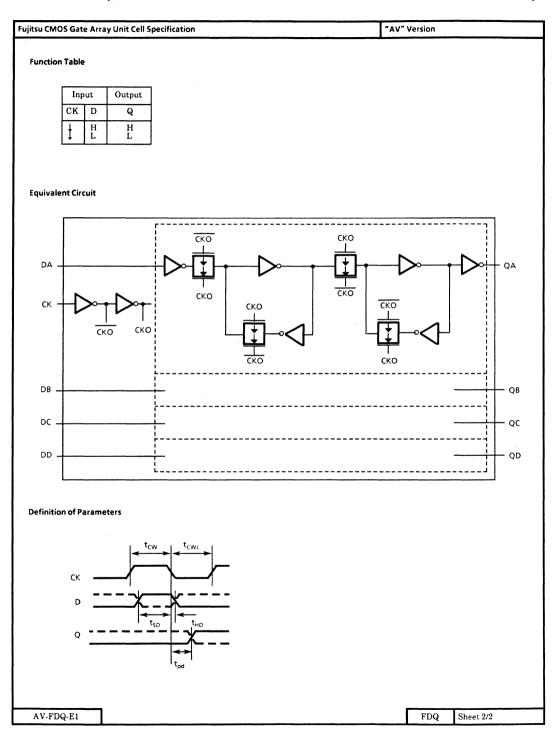
Cell Name	Function							Number	of BC
FDO	DFF with RESET								7
Cell Symbol				Propagation	n Delay Paran	neters			
			tu	)		t <sub>dn</sub>			Path
			to	K <sub>CL</sub>	to	,	K <sub>CL</sub>		
		— Q	3.46 5.96 2.72	0.25 0.25 0.25	5.1 4.2 1.9	2	0.14 0.14 0.14	CI CI R -	K → Q < → XQ → Q, XQ
ск —			Param	eter	Symbol	MIN	ТҮР	MAX	UNIT
			Clock Pulse Wi		t <sub>CW</sub>		6		ns
	::  P <del></del>	xQ · ·	Data Set Up Ti		t <sub>SD</sub>		2	<del></del>	ns
	: : <del></del>		Data Hold Tim		t <sub>HD</sub>		2		ns
			Reset Pulse Wi	dth	t <sub>RW</sub>		3		ns
	R		Clock Pause Ti	me	t <sub>CWH</sub>		6		ns
			Reset Release	Γime	t <sub>REM</sub>		1	***************************************	ns
			Reset Hold Tin	ıe	t <sub>INH</sub>		3		ns
Input Loading	Factor	Pin Name							
	2 / 11	D.P.							
	2 lu 1 lu	D,R CK							
									<u> </u>
Output Drivin	g Factor	Pin Name							
	18 lu	Q,XQ							
TTL Equivalen	t Circuit	LJ				Function	Table		1
	″1°					Inputs	Outputs	1	
_	D PR Q				R	D CK	Q XQ	┨	
	СК				L		L H	1	
	CL Q	-			H	X X H ↑ L ↑	H L L H	İ	
					L			J	
	74574 74L574A								
AV-FDO-	n. 1						FDO SI	neet 1/2	

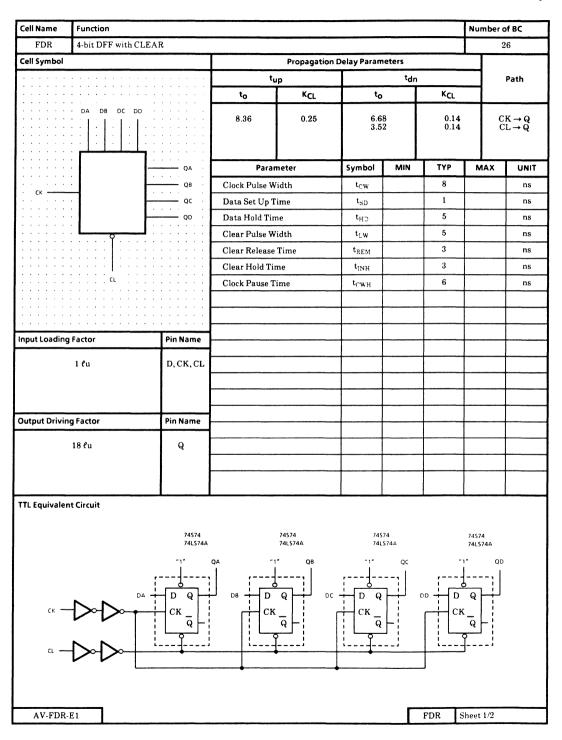


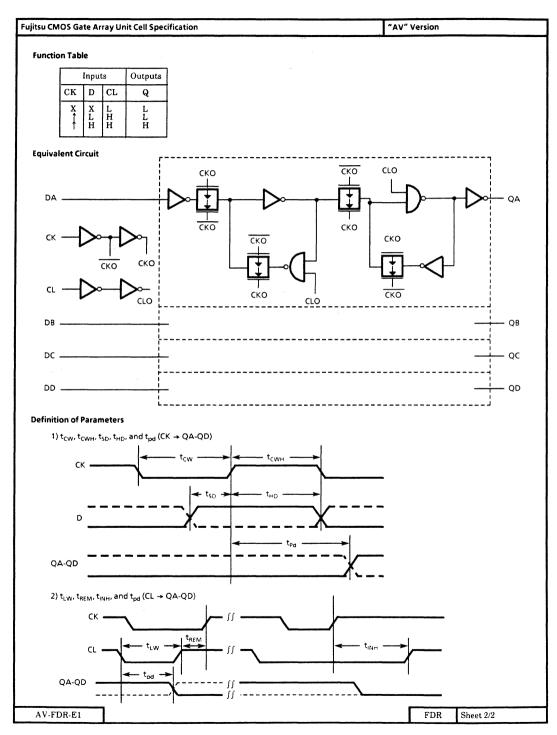




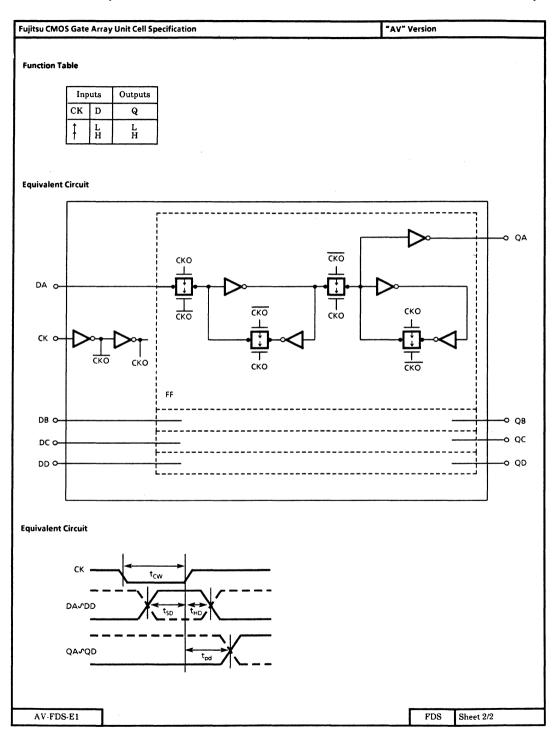








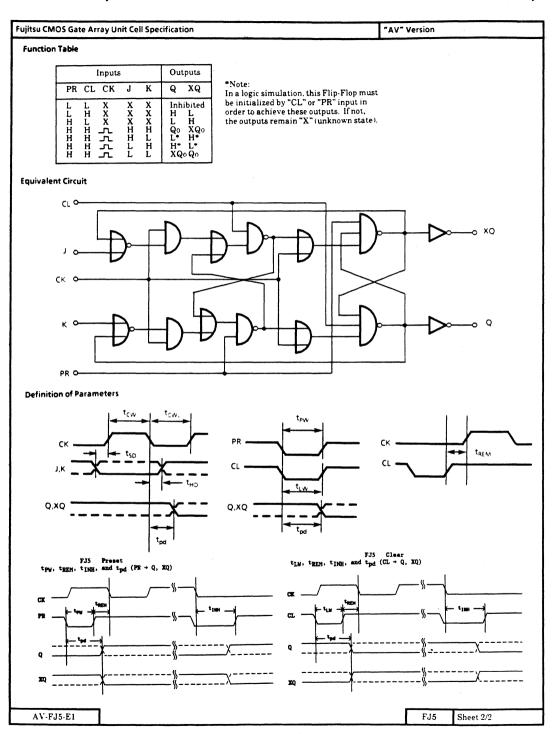
Cell Name	Function							Number of BC	
FDS	Positive Edge Clocked	4-bit DFF			20				
Celi Symbol				Propagation	n Delay Param	eters			
			t <sub>up</sub> t <sub>di</sub>			<sup>t</sup> dn			Path
			to	KCL	to		KCL		
	DA DB DC DD		5.96	0.25	7.60	3	0.14	С	K → Q
	:   -	QA	Param	eter	Symbol	MIN	TYP	MAX	UNIT
	.		Clock Pulse Wi		t <sub>CW</sub>		8		ns
ck	·	QC	Data Set Up Ti	me	t <sub>SD</sub>		1		ns
		QD ·	Data Hold Tim	e	t <sub>HD</sub>		5		ns
	: :		Clock Pause Ti	me	t <sub>CWH</sub>		6		ns
nput Loading	Factor	Pin Name							
	2 lu	DA∼DD CK							
							-		
Output Drivin	g Factor	Pin Name		talani - 1 1 America					<u></u>
	18 <b>l</b> u	QA~QD			-				
AV-FDS-	F1					Г	FDS S	heet 1/2	



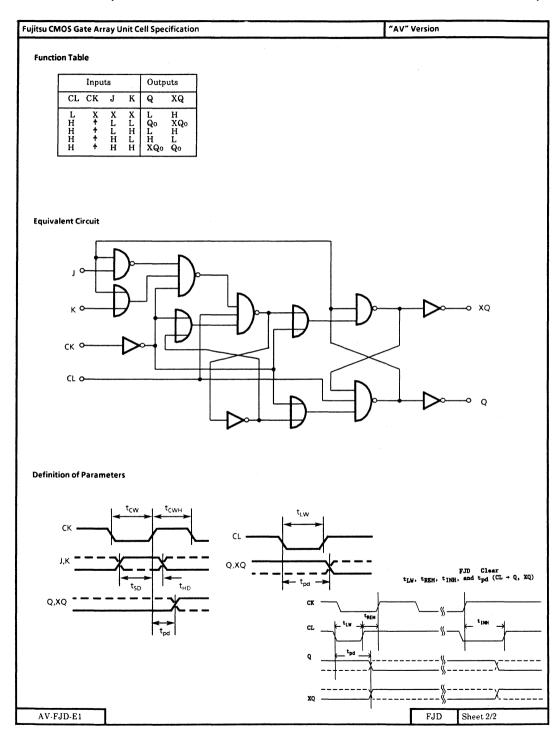
Cell Name	Function		*******					Number	of BC
FJ4	Power JKFF with CLF	AR						11	
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>up</sub>			<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		KCL		
			6.33 5.93	0.12 0.12	4.1 4.1	4	0.07 0.07	CK CL	$\rightarrow Q, XQ$ $\rightarrow Q, XQ$
,		• • • • • • • • • • • • • • • • • • •							
ск —			Parar	neter	Symbol	MIN	TYP	MAX	UNIT
к —	o   b	xq	Clock Pulse W	idth	t <sub>CW</sub>		4		ns
			Clear Pulse W	idth	t <sub>LW</sub>		6		ns
			J, K Set Up Ti	me	$t_{ m SD}$		2		ns
			J, K Hold Tim	е	t <sub>HD</sub>		1		ns
			Clock Pause T	ime	t <sub>CWL</sub>		4		ns
									<b> </b>
									ļ
Input Loading	Factor	Pin Name							
	2 / 11	CL			-				<b> </b>
	2 lu 4 lu 1 lu	ČK J, K							<del> </del>
		5,11							
Output Drivin	g Factor	Pin Name							
	36 lu	Q, XQ							
TTL Equivaler	. Circuit								L
i i L Equivaler	it Circuit								
		"1 <del>"</del>							
: !		İ							
•	74504	PR Q							
	K	_  !							
		CLRQ	<del></del>						
į		7476							
	74504 74LS04	1							
	. 1230-								
AV-FJ4-	FI					_	FJ4 S	heet 1/2	
AV-FJ4-							rJ4 5	neet 1/2	

## "AV" Version Fujitsu CMOS Gate Array Unit Cell Specification **Function Table** Inputs Outputs \*Note: "Note: In a logic simulation, this Flip-Flop must be initialized by "CL" input in order to achieve these outputs. If not, the outputs remain "X" (unknown state). CL CK XQ X H H L L X H L H L Н LHHHH H XQo H\* L\* Qo Q<sub>0</sub> L\* H\* XQ<sub>0</sub> 1555 **Equivalent Circuit** CL O **Definition of Parameters** $\mathsf{t}_{\mathsf{CWL}}$ $t_{\text{CW}}$ FJ4 Clear and t<sub>pd</sub> (CL + Q, XQ) AV-FJ4-E1 FJ4 Sheet 2/2

Cell Name	Function							Number	of BC
FJ5	Power JKFF with CLI	EAR and PRES	SET					1	2
Cell Symbol				Propagation	n Delay Param	eters			***************************************
			tul	)		<sup>t</sup> dn			Path
			to	KCL	to		K <sub>CL</sub>		
	PR		6.63	0.12	4.1	4	0.07	СК	→ Q XQ
			6.63 6.63	0.12 0.12	4.1 4.1	4	0.07 0.07	CL PR	→ Q, XQ → Q, XQ → Q, XQ
,	_d	o	Param	eter	Symbol	MIN	TYP	MAX	UNIT
			Clock Pulse Wi	dth	t <sub>CW</sub>		5		ns
ск —			Preset Pulse W	idth	t <sub>PW</sub>		6		ns
		×o · ·	Clear Pulse Wi	dth	t <sub>LW</sub>		6		ns
	٠		J, K Set Up Tin	ne	$t_{\mathrm{SD}}$		2		ns
			J, K Hold Time		t <sub>HD</sub>		1		ns
	<b>.</b>		Clock Pause Ti	me	t <sub>CWL</sub>		5		ns
nput Loading	Factor	Pin Name							<u> </u>
A 2		CV							
	4 lu CK 2 lu CL 2 lu PR						-		
	1 <i>l</i> u	J, K			_				
Output Drivin	g Factor	Pin Name							
	36 ℓu	Q,XQ		<del></del>					
				M 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					
		<u> </u>							
TTL Equivalen	it Circuit								
		ı							
	$+$ $\square$	<del></del>	[777]						
	74504	J PR Q	<b>→</b>						
-	74LS04	CK							
		K <sub>CLR</sub> Q							
			74504						
	74504	7476	74L\$04						
	74LS04								
AV-FJ5-E	E1						FJ5 S	heet 1/2	



Cell Name	Function							Number	of BC
FJD	Positive Edge Clocked	Power JKFF	with CLEAR						12
Cell Symbol		-		Propagatio	n Delay Param	eters			
			t <sub>up</sub>		<sup>t</sup> dn				Path
			to	KCL	to		KCL		
· · · · · · · · · · · · · · · · · · ·			7.83 5.03	0.12 0.12	4.3 3.4		0.07 0.07	CK	. → Q,XQ → Q, XQ
· · · CK			Parar	neter	Symbol	MiN	ТҮР	MAX	UNIT
к	· ·       - · ·		Clock Pulse W		t <sub>CW</sub>		6		ns
			Clear Pulse W		t <sub>LW</sub> .		5		ns
			J, K Set Up Ti	me	t <sub>SD</sub>		6		ns
			J, K Hold Tim		t <sub>HD</sub>		1		ns
			Clock Pause T		t <sub>CWH</sub>		6		ns
				,					
Innut I andina	Ender	Pin Name							
Input Loading	ractor	Pin Name							
	2 lu 1 lu	CL CK							
	1 lu	J, K							
Output Drivin	n Factor	Pin Name							
	9.1110.	1							
	36 ℓu	Q, XQ							
TTL Equivalen	t Circuit								
	C K	PR Q K CLR Q 745112 74(5112A	_						
AV-FJD-l	E1				***		FJD S	heet 1/2	



## **Data Latch Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3-149	LT1	S-R Latch with Clear	4
3-151	LT2	1-bit Data Latch	4
3-153	LT2	4-bit Data Latch	15
3-155	LT4	4-bit Data Latch	13
3-157	LTK	Data Latch	4
3-159	LTL	Data Latch with Clear	5
3-161	LTM	4-bit Data Latch with Clear	15

3

Cell Name	Function							Number	of BC
LT1	S-R Latch with CLEAR	₹ '							4
Cell Symbol				Propagation	n Delay Param	eters			
			tuj	)		tdn			Path
			t <sub>o</sub>	K <sub>CL</sub>	to		K <sub>CL</sub>		
s		- Q	2.54 2.84	0.25 0.25	1.5 1.3		0.14 0.14	R,CI S-	L → Q, XQ → Q,XQ
			Param	eter	Symbol	MIN	TYP	MAX	UNIT
			Set Pulse Widt		t <sub>SW</sub>		3		ns
· · · R —	q	xo · ·	Reset Pulse Wi		t <sub>RW</sub>		3		ns
	· · · · · · · · · · · · · · · · · · ·		Clear Pulse Wi		t <sub>LW</sub>		3		ns
	c.								
Input Loading	Factor	Pin Name							
	1 ℓu	S,R,CL							
Output Drivin	g Factor	Pin Name							
	18 <i>l</i> u	Q,XQ					ļ		
	10 tu	W.YM							
TTL Equivalen									
	741527	9	74504 741504						
AV-LT1-I	E1						LT1 SI	heet 1/2	

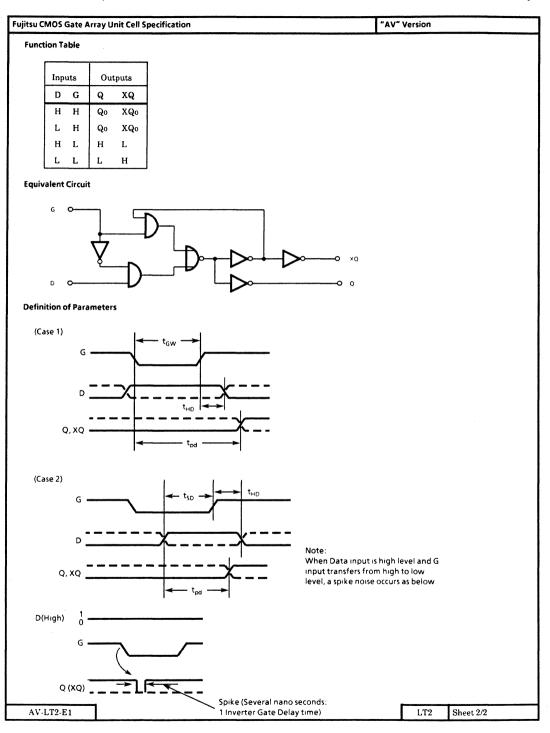
AV-LT1-E1

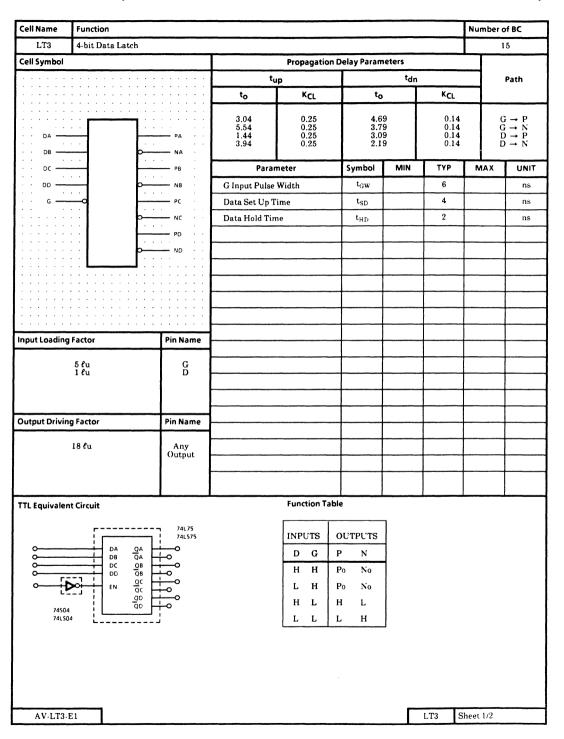
## "AV" Version Fujitsu CMOS Gate Array Unit Cell Specification **Function Table** Outputs Inputs CL S R Q XQ Н Н Н Н Н Qο $\mathbf{X}\mathbf{Q}_{0}$ Н Н L Н L Н Н Н L L Н L L Inhibited **Equivalent Circuit Definition of Parameters**

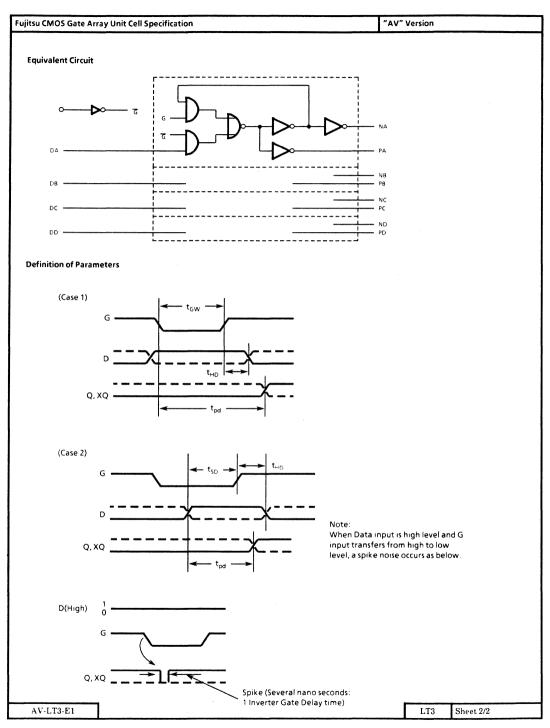
LT1

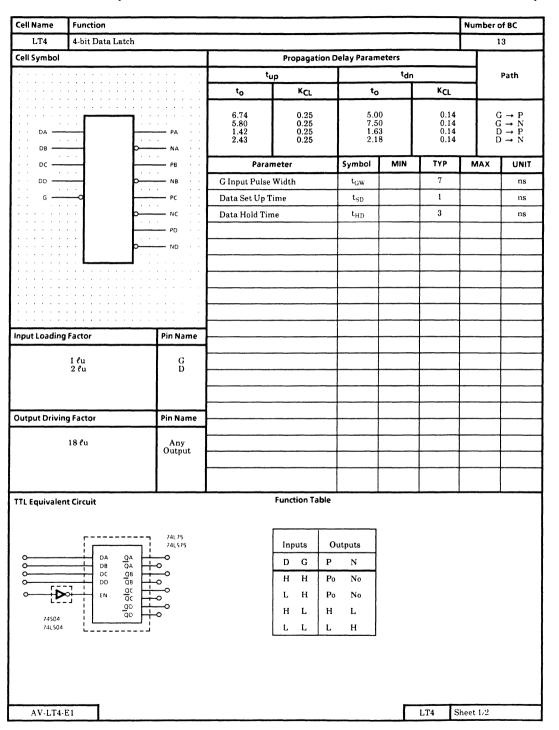
Sheet 2/2

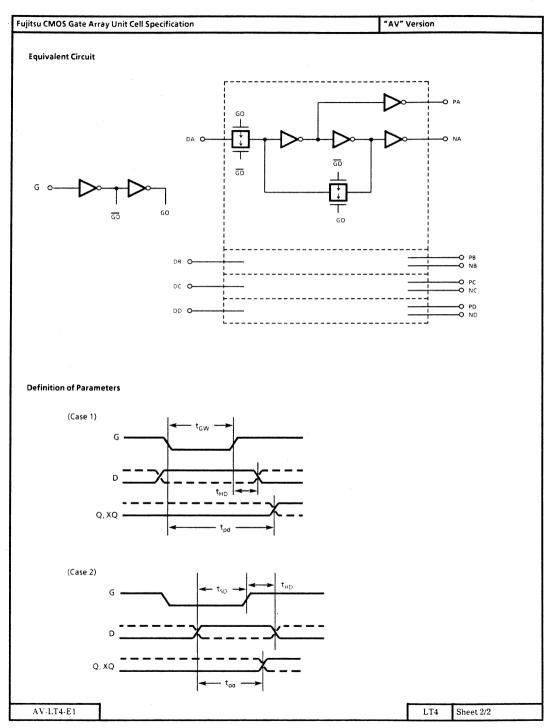
Cell Name	Function							Number	of BC
LT2	1-bit DATA Latch								4
Cell Symbol				Propagation	n Delay Param	eters			
			tu	р		<sup>t</sup> dn			Path
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
		Q	1.84 3.94 1.44 3.94	0.25 0.25 0.25 0.25	3.0 2.5 3.0 2.1	9	0.14 0.14 0.14 0.14	G I D	$G \to Q$ $G \to XQ$ $O \to Q$ $G \to XQ$
· · · · · · · · · · · · · · · · · · ·	a		Paran	neter	Symbol	MIN	ТҮР	MAX	UNIT
			G Input Pulse	Width	t <sub>GW</sub>		5		ns
		×Q · ·	Data Set Up T	ime	$t_{\mathrm{SD}}$		4		ns
			Data Hold Tim	ie	t <sub>HD</sub>		1		ns
Input Loading	g Factor	Pin Name							
	2 lu 1 lu	G D							
Output Drivin	ng Factor	Pin Name							
	18 ℓu	Q,XQ							
TTL Equivaler	nt Circuit								<u> </u>
	74551 74551		504 1504	<b>∘</b> •					
AV-LT2-	E1						LT2 S	heet 1/2	



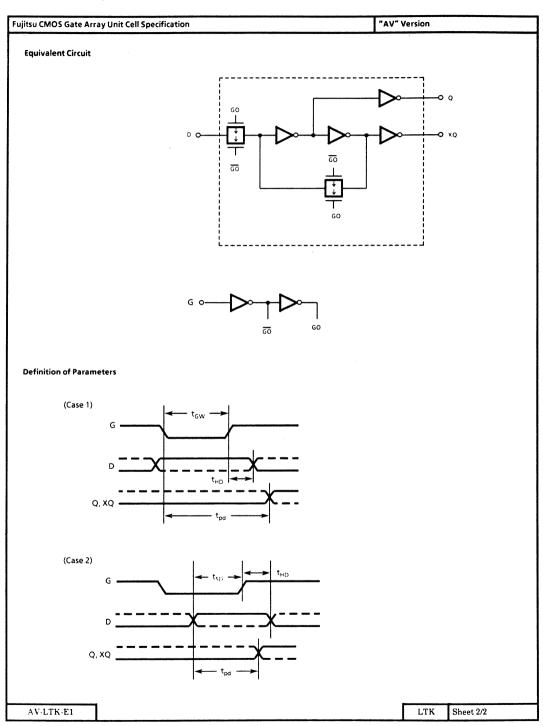








Cell Name	Function								Number	of BC
LTK	1-bit Data L	atch								4
Cell Symbol					Propagation	Delay Param	eters			
				t <sub>up</sub>			<sup>t</sup> dr	<sup>t</sup> dn		Path
				to	K <sub>CL</sub>	to		K <sub>CL</sub>		
			Q	1.42 2.43 5.35 4.41	0.25 0.25 0.25 0.25 0.25	1.6 2.1 3.6 6.1	8	0.14 0.14 0.14 0.14	G G	$\begin{array}{c} O \to Q \\ \to XQ \\ G \to Q \\ \to XQ \end{array}$
				Parai	meter	Symbol	MIN	TYP	MAX	UNIT
	~			G Input Pulse	Width	$t_{GW}$		6		ns
	<u>:</u> [	þ.	×Q	Data Set Up T	`ime	$t_{\mathrm{SD}}$		2		ns
	` <b>L</b>			Data Hold Tir	ne	t <sub>HD</sub>		2		ns
Input Loading	Factor		Pin Name							
mpat rodding	7 4 6 6 6		T III III III							
	2 lu 1 lu		D G							
Output Drivin	g Factor		Pin Name							
	18 ℓu		Q XQ							
	18 ℓu		XQ							
Function Tabl			L					<b></b>		
Function rabi	e									
	Inputs	Outpu	its							
	D G	Q	XQ							
	v u	0-	V()a							
	х н	Į.	XQo							
1	H L L L	H	н							
	. L									
							_	<del></del>		
AV-LTK-	E1							LTK S	heet 1/2	



LTL

Sheet 1/2

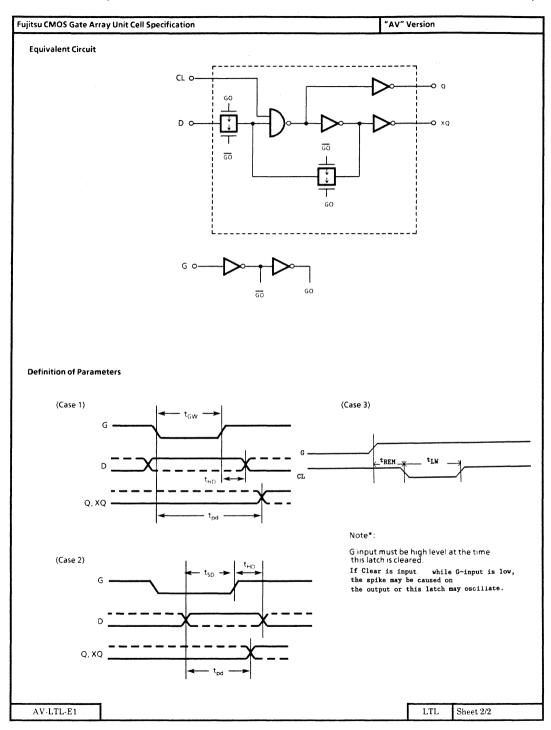
Cell Name	Function								Number	of BC
LTL	1-bit Data La	tch with Cl	lear	***************************************						5
Cell Symbol					Propagation [	Delay Param	eters			
				tu	t <sub>dn</sub>				Path	
				to	KCL	to		KCL		
D —		7	3 · ·	2.20 1.56 2.63 5.49 4.61	0.25 0.25 0.25 0.25 0.25	1.40 1.83 2.33 3.83 6.23	3 2 1	0.14 0.14 0.14 0.14 0.14	CL− D→ D→ G→	XQ
· · G —				Paran	neter	Symbol	MIN	TYP	MAX	UNIT
			xQ	G Input Pulse	Width	t <sub>GW</sub>		6		n ·
				Clear Pulse W	idth	t <sub>LW</sub>		2		ns
				Data Set Up T	ime	$t_{\mathrm{SD}}$		2		ns
				Data Hold Tin	ne	t <sub>HD</sub>		2		ns
				Data Input	Release Time	t <sub>REM</sub>		3		ns
Input Loadir	ng Factor		Pin Name					-		<u> </u>
	2 lu 1 lu 1 lu		D G CL							
Output Driv	ing Factor		Pin Name							
										-
	18 <b>l</b> u 18 <b>l</b> u		Q XQ							ļ
		- 1	ļ							ļ
		1								
Function Ta	ble									
	Inputs	Outpu	uts							
	CL D G	ધ	XQ							
	L X H	I.	Н							
	<b>2</b>	1	1							

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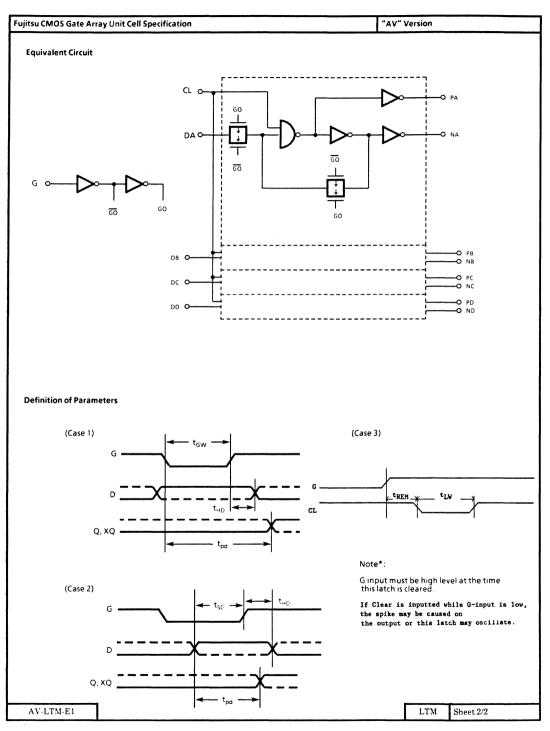
H L L H

H H L

AV-LTL-E1



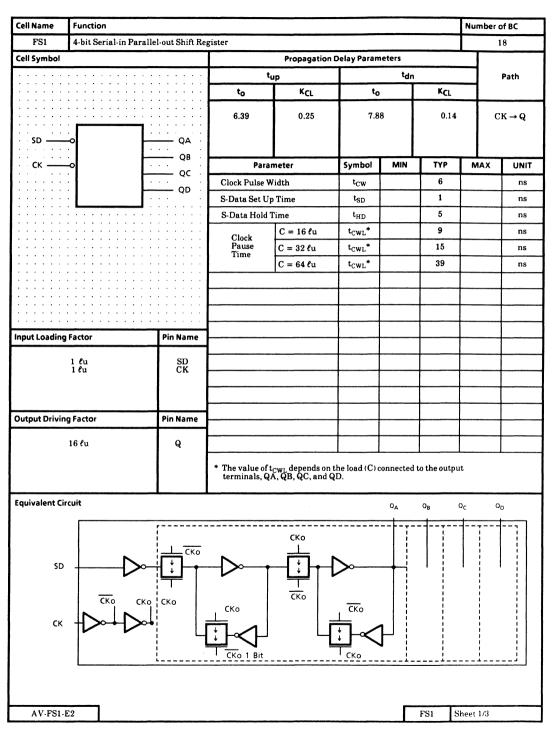
Cell Name	Function	<u> </u>						Number of BC		
LTM	4-bit Data La	tch with Clear							15	
Cell Symbol				Propagation Delay Parameters						
			· t <sub>t</sub>	t <sub>up</sub> t <sub>dn</sub>			1	Path		
			to	t <sub>o</sub> K <sub>CL</sub>		to				
			2.20	0.95	1.4	0	0.14	C	. D.M	
DA		PA	1.56	0.25 0.25	1.40 1.83 2.32		$0.14 \\ 0.14 \\ 0.14$	I	$CL \rightarrow P, N$ $D \rightarrow P$	
DB ———— NA ————— NA —————————————————————		6.88	2.63 0.25 6.88 0.25 6.00 0.25		5.20 7.64			$\begin{array}{c} D \rightarrow N \\ G \rightarrow P \\ G \rightarrow N \end{array}$		
DC —		D NB		neter	Symbol	MIN	0.14 TYP	MAX	UNIT	
		PC			t <sub>GW</sub>		7		ns	
· · · · · · · · · · · · · · · · · · ·	d	D NC		G Input Pulse Width  Clear Pulse Width  Data Set Up Time		t <sub>LW</sub>	2		ns	
	: :	PD					2		ns	
	: :	0 ND	Data Hold Tin		t <sub>SD</sub>		3		ns	
	: : <b>L</b>		<u> </u>	Release Time	t <sub>REM</sub>		3		ns	
							1			
							1			
							1			
							1			
			_				1			
Input Loading Factor Pin Name										
	2 lu	DA ~ D	D							
1 fu G 4 fu CL										
Output Drivin	a Factor	Pin Name	-							
Output Driving Factor Pin Name										
18 lu F 18 lu N			) 							
	1014	NA~ N								
									<u> </u>	
Function Ta	ble									
Г										
Inputs Outputs										
ļ	. D G	P N								
L	хн	LH								
Н	ХН	Po No								
Н	H L	H L								
Н	L L	LH								
AV-LTM-	Fi						LTM S	heet 1/2		

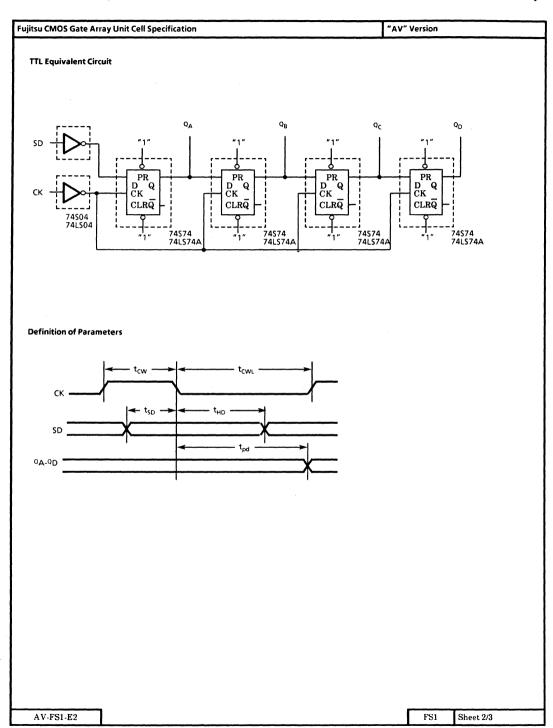


## **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
3-165	FS1	4-bit Serial-in Parallel-out Shift Register	18
3-168	FS2	4-bit Shift Register with Synchronous Load	30
2_171	FS3	A-hit Shift Register with Asynchronous Load	34

3





"AV" Version

### FS1

### **Function Table**

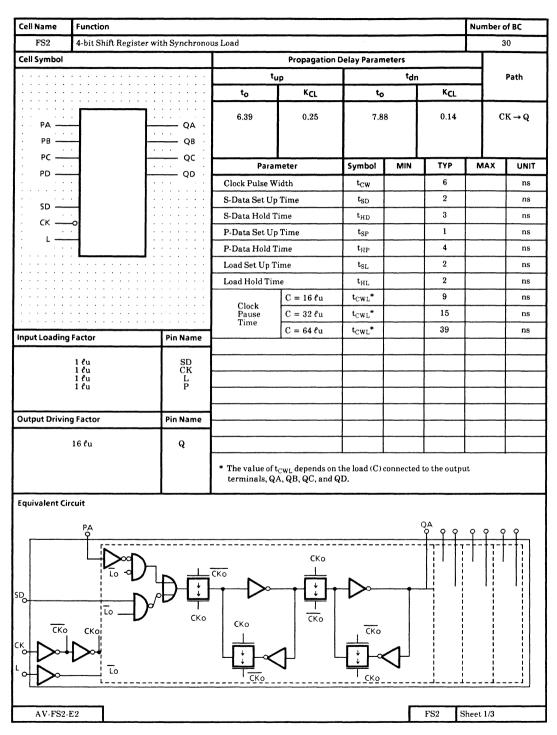
In	outs	Outputs							
SD	CK	QA	QB	QС	QD				
SD	1	SD	QAn	QBn	QCn				

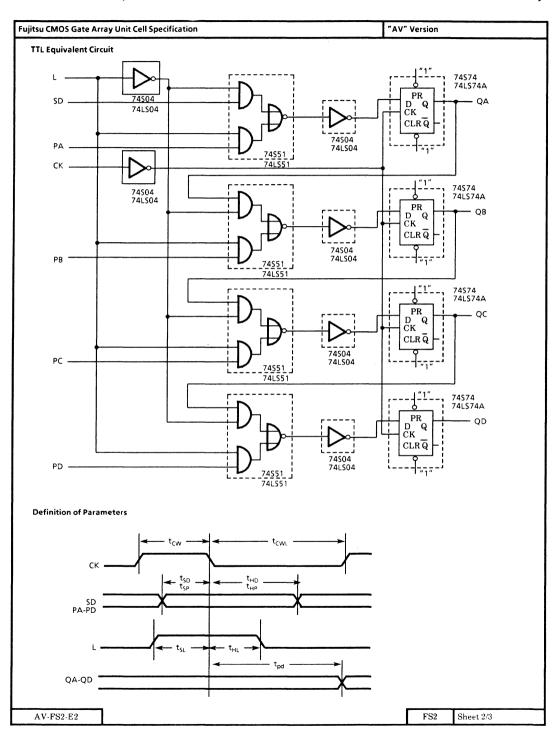
- Note: •SD = H or L
  - QAn, QBn, and QCn are levels of QA, QB, and QC, respectively, before the falling edge of CK, i.e.  $\boldsymbol{1}$  bit shift by the falling edge of CK.

AV-FS1-E2

FS1

Sheet 3/3





"AV" Version

### FS2

### **Function Table**

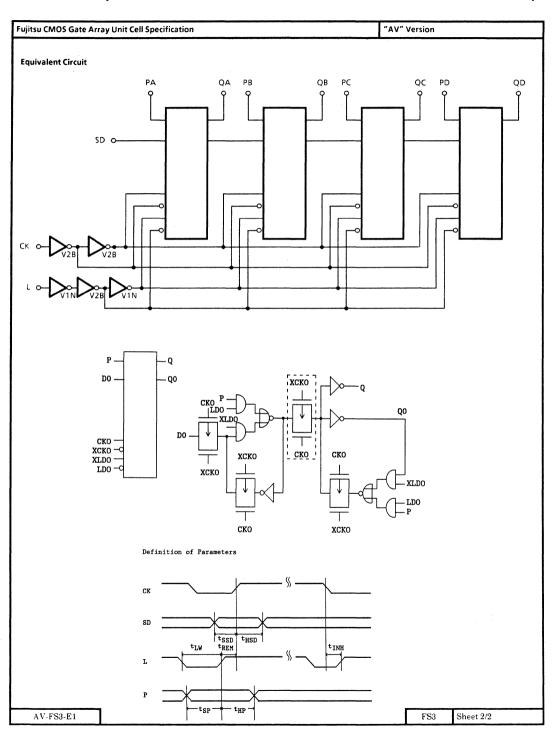
	Ir	puts		Outputs				
SD	L	P	CK	QA	QB	QC	QD	
SD	L	X	1	SD	QAn	QBn	QCn	
Х	Н	P	1	PA	РВ	PC	PD	

- Note: •SD = Hor L
  - QAn, QBn, and QCn are levels of QA, QB, and QC, respectively, before the falling edge of <math display="inline">CK,i.e. 1 bit shift by the falling edge of CK.
  - P represents PA, PB, PC, and PD.

AV-FS2-E2

FS2 Sheet 3/3

Cell Name	Function	on								Number	of BC
FS3	4-bit S	hift R	egiste	r With Asynchr	onous Load						34
Cell Symbol						Propagation	n Delay Param	eters			
					t <sub>up</sub> t			tdn			Path
					to	KCL	to		KCL		
			QA	4.34 0.25 6.36 0.25 1.98 0.25		8.0	6.04 8.01 3.63		•	$CK \to Q$ $L \to Q$ $P \to Q$	
· PB —	7			QB	Para	meter	Symbol	MIN	TYP	MAX	UNIT
PC QC ·			Clock Pulse W	/idth	t <sub>CW</sub>		6		ns		
PD —				QD :	Load Pulse W	idth	t <sub>LW</sub>		8		ns
					S-Data Set U	Time	t <sub>KD</sub>		3		ns
SD —					S-Data Hold	l'ime	t <sub>HD</sub>	, <del></del>	3		ns
. СК —	7				P Set Up Time	(Load)	tsp		1		ns
. L	9				P Hold Time (		t <sub>HP</sub>		4		ns
					Load Releas	e Time	t <sub>REM</sub>		3		ns
					Load Hold T		tINH		3		ns
				T	_				1		
Input Loading	Factor			Pin Name	_						
	2 <b>l</b> u 1 <b>l</b> u			ск		an described					
	1 €u 2 €u			L PA∼PD							
				SD							
Output Drivin	a Factor			Pin Name							
Output Dilvin	gractor			Fill Name	-						
:	18lu			QA~QD							
					<del></del>	······································			<u> </u>	L	<u> </u>
Function Table	e										
		PUTS		OUTPUT							
	L P	SD	CK	Q							
	LLL	X	X	L							
	LH	X	X	H							
	H X	L	1	L							
L	H X	Н	1	Н							
AV-FS3-I	F 1	ı						Г	FS3 S	Sheet 1/2	
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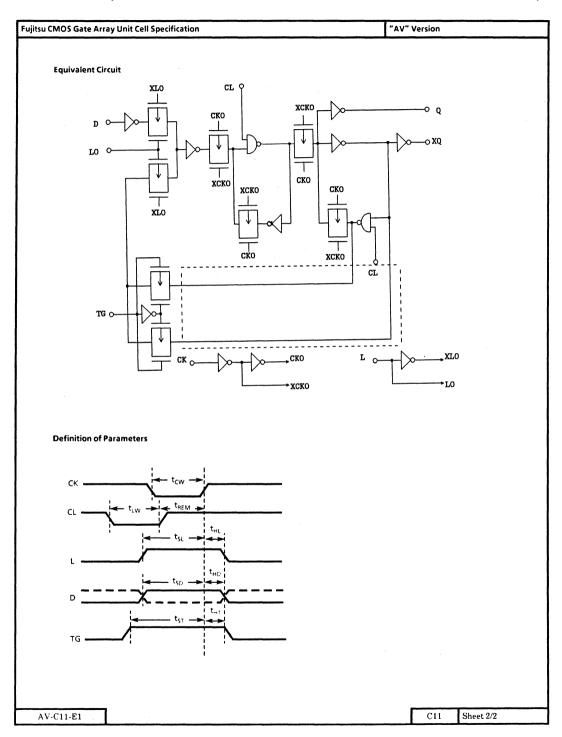


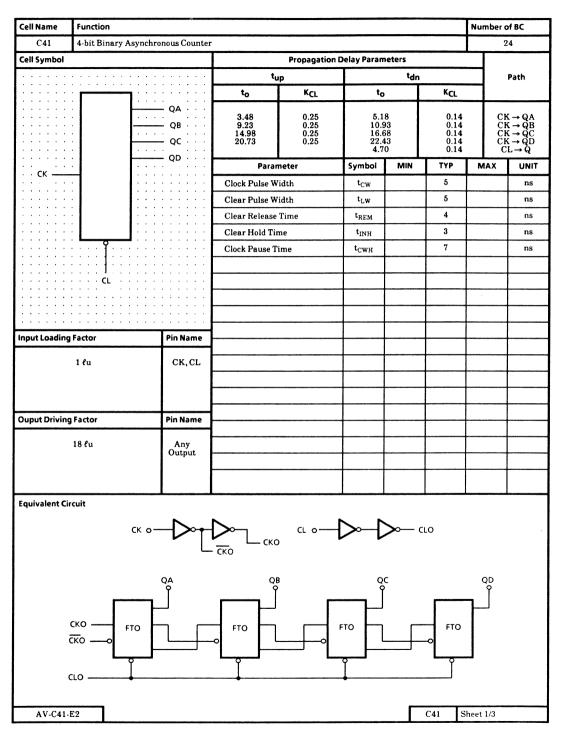
# **Counter Family**

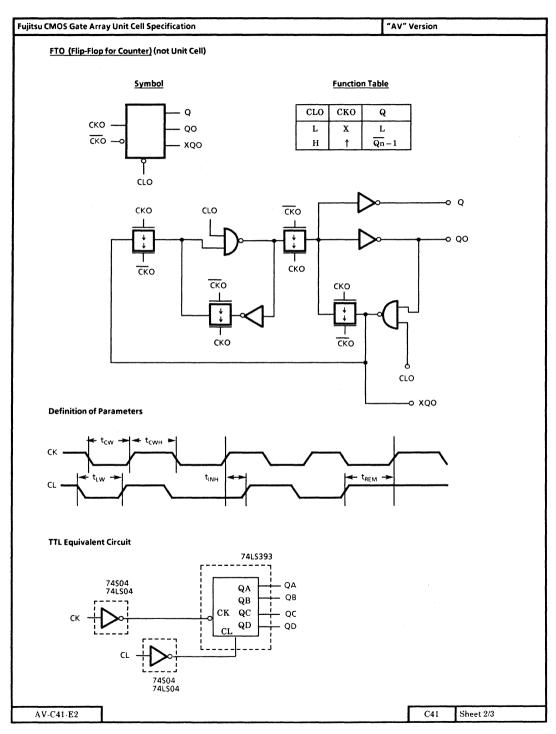
Page	Unit Cell Name	Function	Basic Cells
3-175	C11	Flip-Flop for Counter	11
3-177	C41	4-bit Binary Asynchronous Counter	24
3-180	C42	4-bit Binary Synchronous Counter	32
3-183	C43	4-bit Binary Synchronous Up Counter	48
3-186	C45	4-bit Binary Synchronous Up Counter	48
3-189	C47	4-bit Binary Synchronous Up/Down Counter	68

3

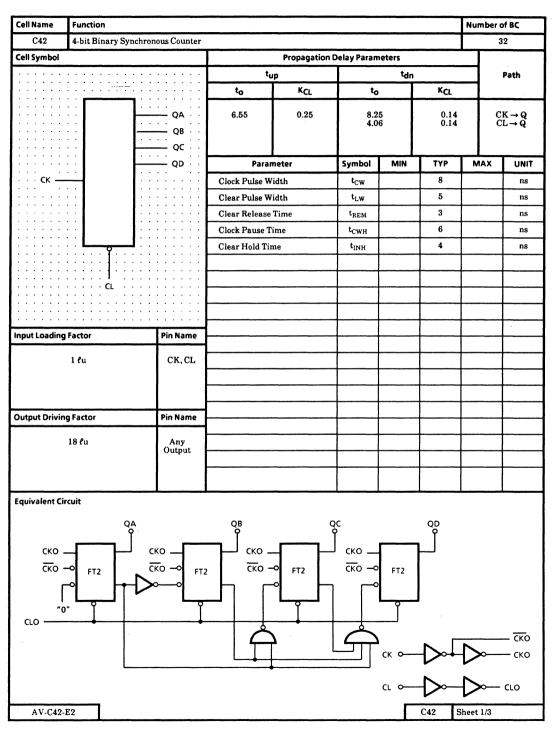
Cell Name	Function								Number	of BC
C11	Flip-Flop for	r Counter								11
Cell Symbol					Propagation	n Delay Param	eters			
				t <sub>up</sub>			<sup>t</sup> dr	<sup>t</sup> dn		Path
				to	KCL	to		K <sub>CL</sub>		
D			3.23 5.90 1.58 2.80	0.25 0.25 0.25 0.25	4.9 4.3 1.8 2.6	0 3	0.14 0.14 0.14 0.14	() () ()	$CK \rightarrow Q$ , $K \rightarrow XQ$ $CL \rightarrow Q$ $CL \rightarrow XQ$	
				Parar	neter	Symbol	MIN	TYP	MAX	UNIT
ск —				Clock Pulse W	idth	t <sub>CW</sub>		6		ns
				Clear Pulse W	idth	t <sub>£</sub> w		3		ns
· · · TG —		<b>-</b>	xQ	Clear Release	Time	t <sub>REM</sub>		1		ns
	: :			Load Set Up T	ime (CK)	$t_{\rm SL}$		5		ns
	<del>L</del>			Load Hold Tin	ne (CK)	t <sub>HL</sub>		1		ns
				Data Set Up T	ime (CK)	t <sub>SD</sub>		3		ns
				Data Hold Tin	ne (CK)	t <sub>HD</sub>		2		ns
				TG Set Up Tin	ne (CK)	$t_{ST}$		6		ns
				TG Hold Time	(CK)	t <sub>HT</sub>		1		ns
Input Loading	Factor		Pin Name							
mpat coading	1 4 (10)		T III TO SILITE							
	1 lu 2 lu		D, CK L, TG, CL							
Output Drivin	g Factor		Pin Name							<u> </u>
	18 ℓu		Q, XQ							
			<u> </u>						<u> </u>	
Function Table	e									
L	D TG	CL CK	$Q(Q_0)$							
X	x x 1	L X	L							
н	і н х і	н∣↑	н							
H	ı L X	н ↑	L							
L	XLI	н   ↑	Q(Q <sub>0</sub> )							
L	. х н і	н 🕇	$\overline{\mathbf{Q}}(\overline{\mathbf{Q}}_{\Omega})$							
AV COL							r	- C11 - L2	Sh 1/0	
AV-C11-	El							C11 S	Sheet 1/2	

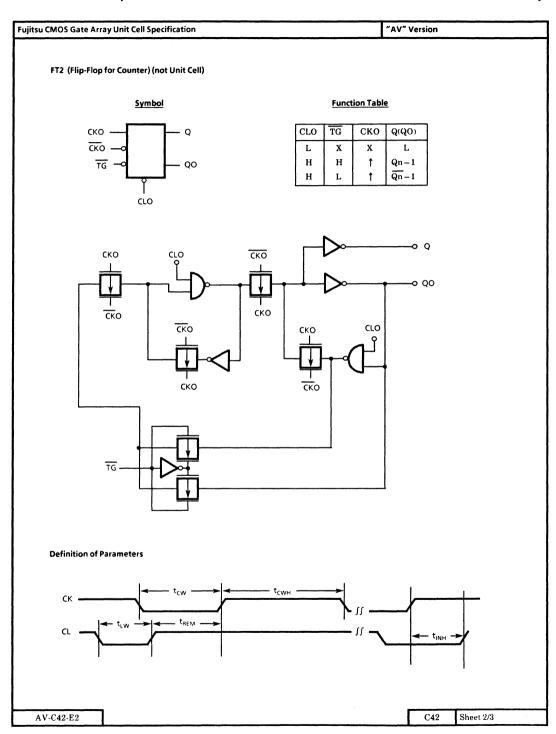






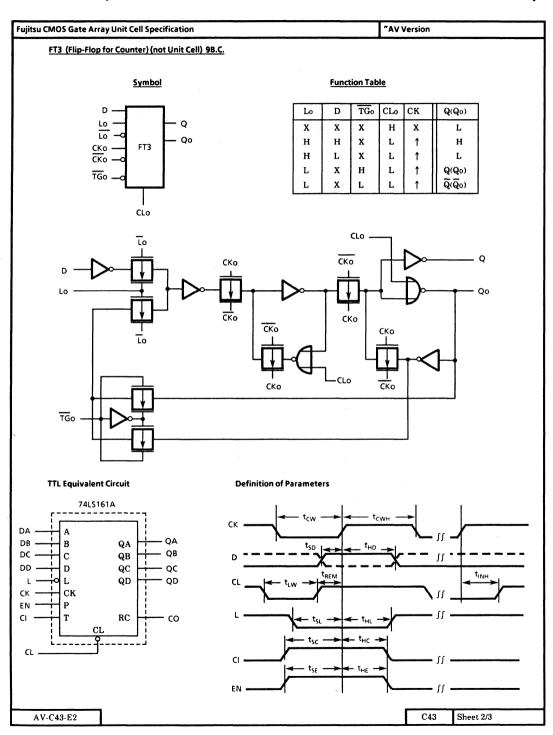
Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version	
Tapicas cines date Array only censpectification		
C41 Function Table		
ranction rable		
Inputs Outputs		
CL CK (QA-QD)		
H ↑ Count up L X L		
		:
AV-C41-E2	C41	Sheet 3/3





Fujitsu CMOS Gate Array Unit Cell Specification	"AV" Version
C42 <u>Function Table</u>	
Inputs Outputs	
CL CK (QA – QD)	
H	
AV-C42-E2	C42 Sheet 3/3

Cell Name	Function							Number	of BC
C43	4-bit Binary Synchron	ous Up Count	er						48
Cell Symbol				Propagation [	Delay Param	eters			
			tup	<sup>t</sup> dn				Path	
			to	K <sub>CL</sub>	to		K <sub>CL</sub>		
DA QA			6.67 13.40 2.94	0.25 0.25 0.25	8.3 12.4 3.0 5.5 9.6	14 4 4	0.14 0.14 0.14 0.14 0.14	C	CK → Q K → CO CI → CO CL → Q L → CO
DD	<u> </u>	QD : :	Param	eter	Symbol	MIN	TYP	MAX	UNIT
L —	<b></b> d   ∷		Clock Pulse Wie	lth	t <sub>CW</sub>		8		ns
ск —			Data Set Up Tir	ne	t <sub>SD</sub>		2		ns
EN			Data Hold Time	)	t <sub>HD</sub>		4		ns
: cı —	<u> </u>	co : :	Load Set Up Ti	ne	t <sub>SL</sub>		4		ns
			Load Hold Time	?	t <sub>HL</sub>		4		ns
			CI Set Up Time		t <sub>SC</sub>		6		ns
			CI Hold Time		t <sub>HC</sub>		1		ns
			EN Set Up Time	•	t <sub>SE</sub>		6		ns
			EN Hold Time		t <sub>HE</sub>		1		ns
		Pin Name	Clear Pulse Wid	lth	t <sub>LW</sub>		7		ns
nput Loading	g ractor	Pin Name	Clear Release T	ime	t <sub>REM</sub>		5		ns
	1 ℓu	D	Clear Hold Tim	e	t <sub>INH</sub>		8		ns
	1 <b>l</b> u 1 <b>l</b> u 2 <b>l</b> u	L, EN CK, CL CI	Clock Pause Tir	ne	t <sub>CWH</sub>		8		ns
	ztu								
Ouput Driving	n Factor	Pin Name							
Ouput Dilving	9, 000	T III NO.							
	18 ℓu	Any Output							
		Guspas							<u> </u>
Equivalent Ci	reuit			00 00	1	06 0			<u> </u>
Equivalent Ci	rcuit DA	QA I	DB I	QB DC		QC DI	ь	QD I	
CL +4>	CLO L			, T		-†t		7	]
	Lo —	Н	Lo —	L L <sub>0</sub> —		_J <sub>Lo</sub> .		$\vdash$	į
' †9 <b>&gt;</b> 1	<u></u>		<u>ro</u> —			Lo ·	<b>-</b> ∘		i
ck <b>⊹D</b> ⊙→	CKO CKO	FT3	CKo — FT3	<u> </u>	FT3	<u>CK</u> o -	FT3	L	!
	-ф ск₀						_		į
cı <del>                                    </del>	+ $  $	<b></b>	'-	J			L	<b>_</b>	4
EN †	<del> </del>				[				}
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11.7.040-						I	C #0		



"AV Version

C43

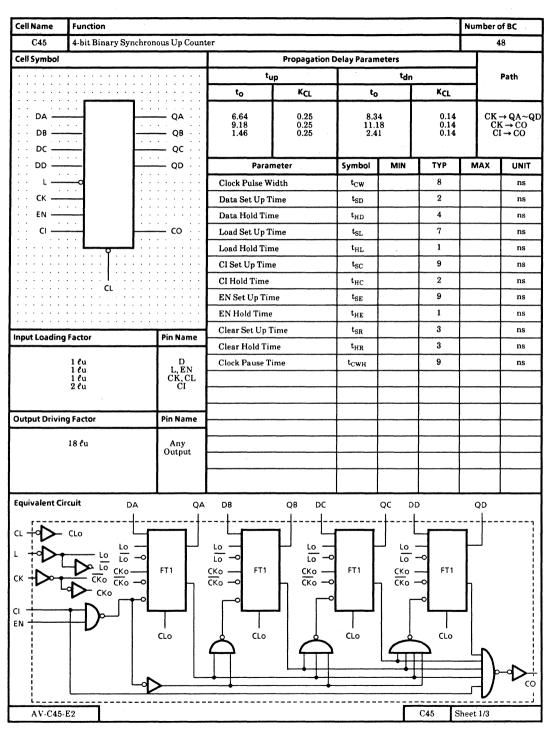
### **Function Table**

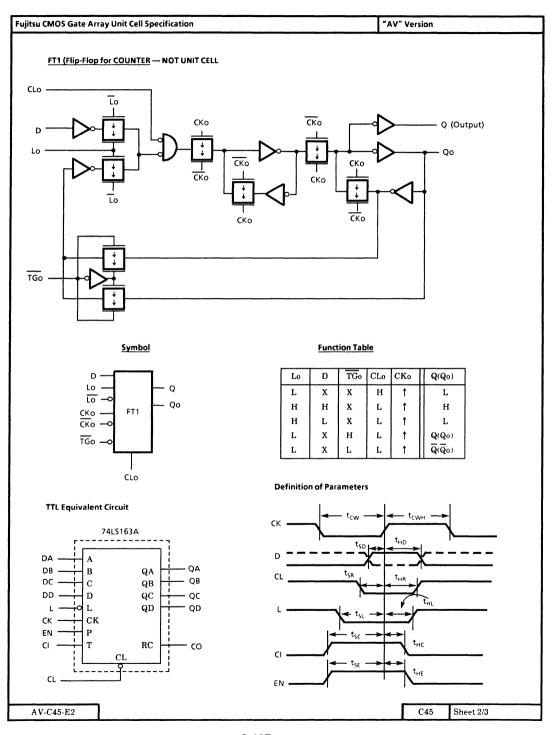
		Outputs				
CL	L	D	EN	CI	CK	(QA – QD)
L	Х	X	Х	Х	х	L
Н	L	Н	Х	Х	1	H
Н	L	L	X	X	1	L
Н	Н	X	X	L	Х	No Counting
Н	Н	X	L	X	Х	No Counting
Н	Н	X	Н	Н	1	Count up

Note: The CO output produces a high level output data when the counter overflows.

AV-C43-E2

C43 Sheet 3/3





"AV" Version

### C45 <u>Function Table</u>

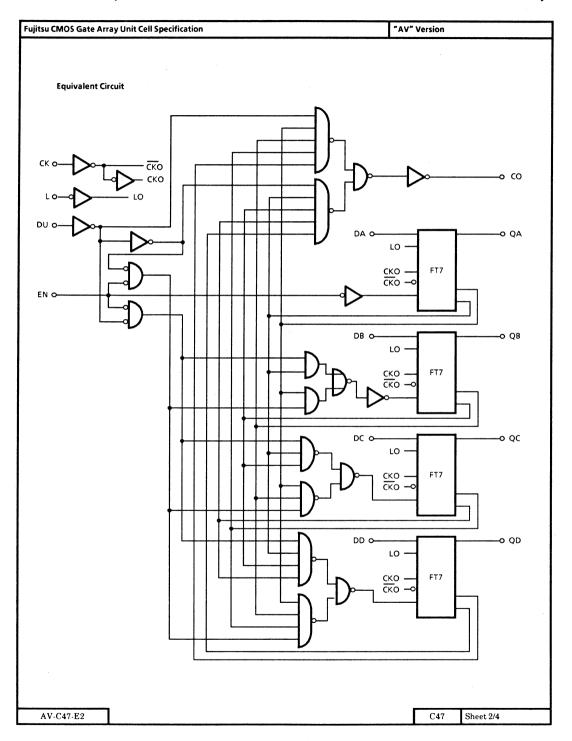
		Outputs				
CL	L	D	EN	CI	CK	(QA – QD)
L	X	X	X	X	1	L
Н	L	Н	X	X	1	Н
Н	L	L	X	Х	1	L
Н	Н	X	X	L	X	No Counting
Н	Н	Х	L	Х	. X	No Counting
Н	Н	X	Н	Н	1	Count up

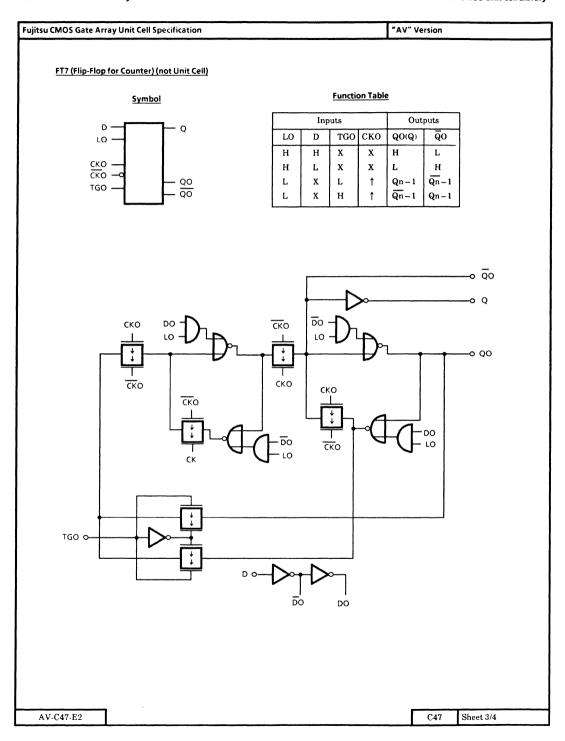
Note: The CO output produces a high level output data when the counter overflows.

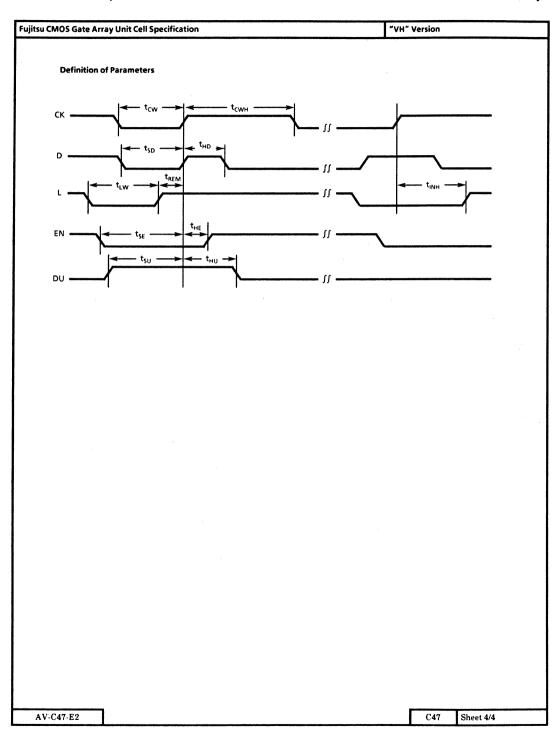
AV-C45-E2

C45 Sheet 3/3

Cell Name	Ti	uncti	on									Num	ber of BC	see note	
C47	4	l-bit B	inary :	Synchr	onous U	o/Down	Counter							68	
Cell Symb	ol						Propagation Delay Parameters								
								tu	р	<sup>t</sup> dn				Path	
							1	to	K <sub>CL</sub>	to		KCL			
				7	Q		9	.82 .65 .96 .07	0.25 0.25 0.25 0.25	8.5 9.4 4.4 5.7	3	0.14 0.14 0.14 0.14	C	CK → Q K → CO L → Q U → CO	
QB							Paran	neter	Symbol	MIN	TYP	MAX	UNIT		
DC		7			Q		Cloc	k Pulse W	idth	t <sub>CW</sub>		10		ns	
· · DD				T-	QI		Load	Pulse Wi	dth	t <sub>LW</sub>		5		ns	
CK		9				: : :	Date	Set Up T	ime (L)	t <sub>SD</sub>		7		ns	
EN				1:			Data	Hold Tin	ne (L)	t <sub>HD</sub>		3		ns	
DU				Ŀ		,	ENS	Set Up Tin	ne (CK)	t <sub>SE</sub>		9		ns	
		L			((	`	ENI	Iold Time	(CK)	t <sub>HE</sub>		3		ns	
				<del></del> .			DUS	Set Up Tin	ne(CK)	t <sub>SU</sub>		11		ns	
						: : : [	DUI	Iold Time	(CK)	t <sub>HU</sub>		2		ns	
						: : : <b>[</b>	Clea	r Release	Time	t <sub>REM</sub>		3		ns	
Input Load	ling Fa	ctor			Pin N	ame	Clear Hold Time			t <sub>INH</sub>		8		ns	
,					+		Clock Pause Time			t <sub>CWH</sub>		10		ns	
	2	lu lu lu				DU L N									
Output Dri	iving F	actor			Pin N	ame			<del></del>	<del> </del>		<b>†</b>		<del>                                     </del>	
	18	3 <b>l</b> u			An Out <sub>l</sub>										
Function T	able					1				TL Equivale	nt Circuit			l	
		Iı	nputs		T			1			5191				
DA	rDD	L	EN	DU	СК	Outr (QA)	outs 'QD)		DA	∔[A		7			
		L	х	X	х	Н		1	DB	В	QA	1			
0	,	L	х	х	x	L			DC	††¢	QB QC				
)	1	Н	н	х	1		unting		L —	₩ L	QD		)		
2	- 1	H H	L L	L H	†	Count	-		ск —	СК		,			
ــــــــــــــــــــــــــــــــــــــ	<u>.</u> ;	Note: The C	O outp	ut prod	uces a lo	Count	Down		EN —	DU M	AX/MINI	74S	_1	0	
	ì	inderi	flows.					Note*: (	C47 is not availa	ble for C350	AVB or C	540AVB.			
AV-C	47-E2		1								Г	C47 Si	neet 1/4		
			L												



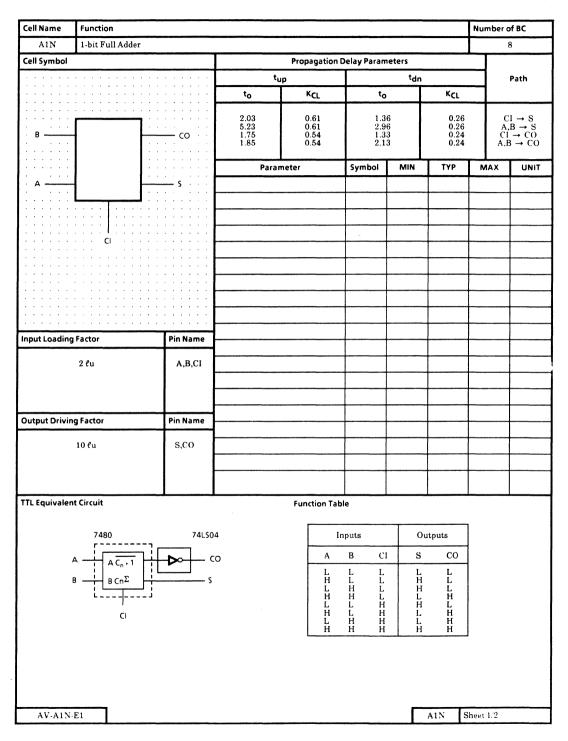


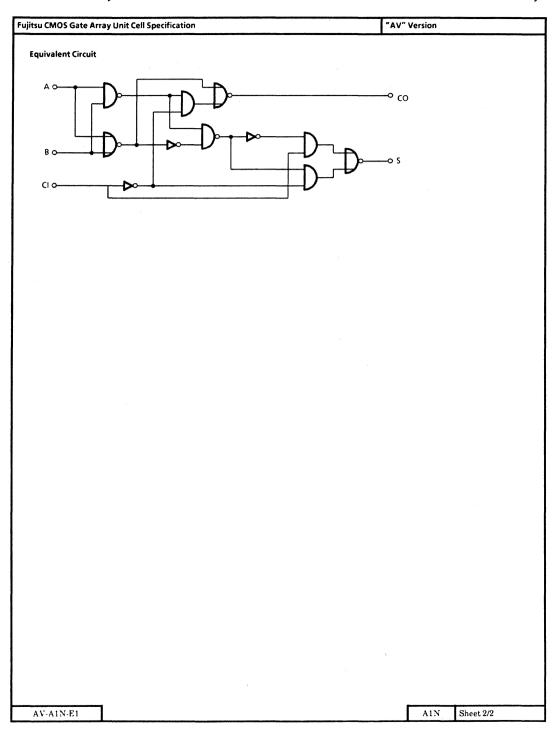


# **Adder Family**

Page	Unit Cell Name	Function	Basic Cells
3–195	A1N	1-bit Full Adder	8
3-197	A2N	2-bit Full Adder	16
3_199	ΔΔΗ	4-bit Full Adder	50

3





Cell Name	Function						***************************************	Number	of BC
A2N	2-bit Full Adder								16
Cell Symbol			Propagation Delay Parameters						
					<sup>t</sup> dn	n Pati		Path	
		t <sub>o</sub> K <sub>CL</sub>		to		K <sub>CL</sub>			
		4.93 5.23 4.65 4.75	0.61 0.61 0.54 0.54	3.06 2.96 3.03 3.83		0.26 0.26 0.24 0.24	CI A,E C A,	$CI \rightarrow S1,S2$ $A,B \rightarrow S1,S2$ $CI \rightarrow CO$ $A,B \rightarrow CO$	
B2	1 1	co · ·							
B1		S2	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
. A1 —	1	- S1 ::					-		-
	CI								
Input Loading	Factor	Pin Name					ļ		<u> </u>
2 lu		A,B,CI					<del> </del>		
		-						<b>-</b>	<del> </del>
									<u> </u>
Output Drivin	a Factor	Pin Name					i		
Output Drivin	ig ractor	rinvanie							
	10 ℓu	s,co					ļ		ļ
		-					ļ		ļ
TTL Equivaler	nt Circuit								
	7482								
	F								
	A2	CO 52 51							
	CI								
						_			
AV-A2N-	E1					Γ	A2N S	Sheet 1/2	

#### **Fujitsu CMOS Gate Array Unit Cell Specification** "AV" Version **Function Table** Outputs CI = LCI = HInputs В1 A2 S2 $\overline{co}$ SI S2 $c\overline{o}$ **B**2 Sı A1 L L L L L L L Н L L Н L L L Н L L L Н L L Н L Н L L Н L L L Н Н L L Н Н Н L L L Н Ĺ Н Н Н L Н Н L L Н Н L L L Н L Н Н L Н Н L Н Н Н Н L Н Н L L L Н Н Н Н L Н Н L L Н Н Н L L L Н Н Н L L Н Н L Н Н Н L Н Н Н L L Н Н L Н Н L Н Н Н Н Н Н L Н L L Н L Н Н Н Н L Н L Н Н Н Н Н Н L н Н Н Н Н **Equivalent Circuit** A2 0 AV-A2N-E1 A2N Sheet 2/2

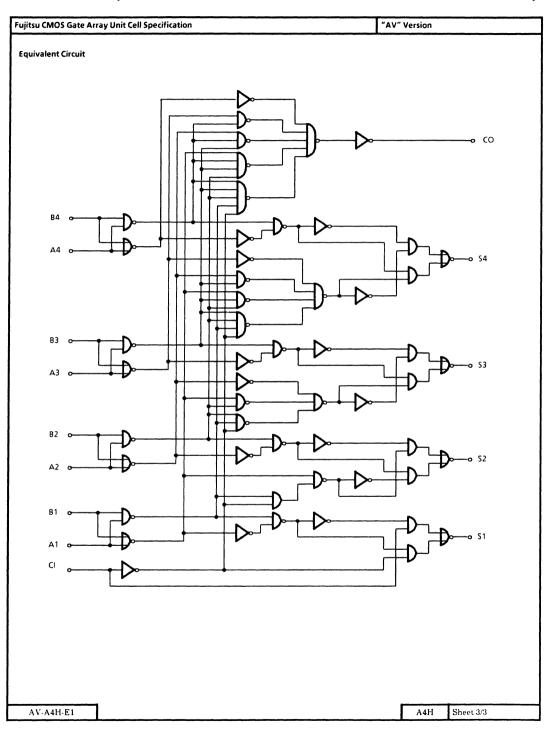
Cell Name	Function							Number of BC	
A4H	4-bit Full Adder						<del></del>		50
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>up</sub> t <sub>d</sub>			t <sub>dn</sub>	n		Path
		: : : : E	to	K <sub>CL</sub>	to		K <sub>CL</sub>		
B4 CO		co	6.73	0.61	5.16		0.26		u → s
Α4		S4	8.13 5.04	0.61 0.25	5.7 5.7	6	0.26 0.14	À	SI → S B → S I → CO B → CO
В3 —	<b>⊣</b> I∙		5.64	0.25	7.1	9	0.14	Ã,	B → CO
A3		S3	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
B2		:: <b> </b>					<del>                                     </del>		-
A2		S2					<del> </del>		$\dagger$
B1	<b></b> }   .	:: <b> </b>					†		<del> </del>
A1	<b>-</b>	S1  -	······································		_		<del>                                     </del>	<b> </b>	
	:						1		<u> </u>
									1
				· · · · · · · · · · · · · · · · · · ·					
nout Loading	Factor	Pin Name							
Input Loading Factor Pin Name								<u> </u>	
	2 lu	A,B,CI			_		<b>_</b>	ļ	ļ
		-					<del> </del>		<u> </u>
							<del> </del>		<u> </u>
Output Drivin	ng Factor	Pin Name —					<del> </del>		<u> </u>
10 <b>l</b> u 18 <b>l</b> u		s co	····				<del>                                     </del>		<del> </del>
		co –					†		
							<b> </b>		<b>†</b>
TTL Equivaler	nt Circuit	<u> </u>						L	<u></u>
	74LS83A								
		1							
	A4	co							
	B4	<b>←</b> \$4							
	B3	53							
	A4	S2							
	CO	<b>-</b> S1							
	<u> </u>	<u>.</u>							
	C,								
AV-A4H-	D						A4H S	heet 1/3	

AV-A4H-E1

#### Fujitsu CMOS Gate Array Unit Cell Specification "AV" Version **Function Table** Outputs Inputs $C_i = L$ $C_1 = H$ $C_2 = L$ $C_2 = H$ Α1 A2 В2 **S**1 **S**2 C2 **S1 S2** C2 A3 **S**3 60 Н L L н Н Н н L L L L L L Н Н Н Н Н L L L L L Н Н Н L L Н L L L L Н Н L Н L Н L L Н L Н Н L Н Н L L L н Н н Н L L L н Н L Н н Н Н Н L L L Н Н Н L н Н н н н L Н L L Н Н L Н L L Н Н L Н Note: Note: Input conditions at A1, B1, B2 and Cl are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4, and CO. Н L L Н Н L L Н Н L н L Н Н Н L Н L Н Н Н Н Н Н L Н L Н Н н Н Н Н н Н Н Н Н

A4H

Sheet 2/3



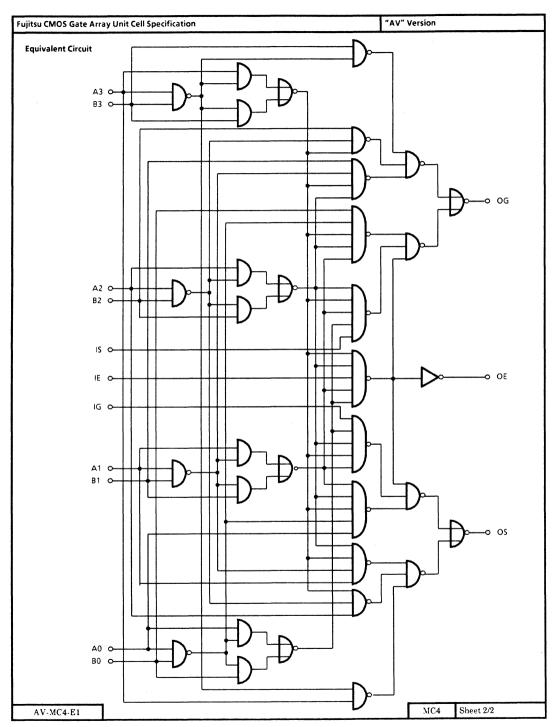
3

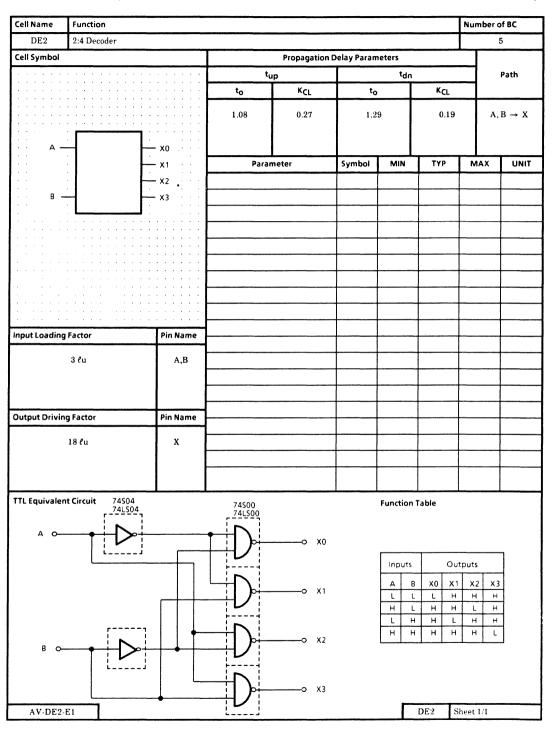
## **Miscellaneous Functions**

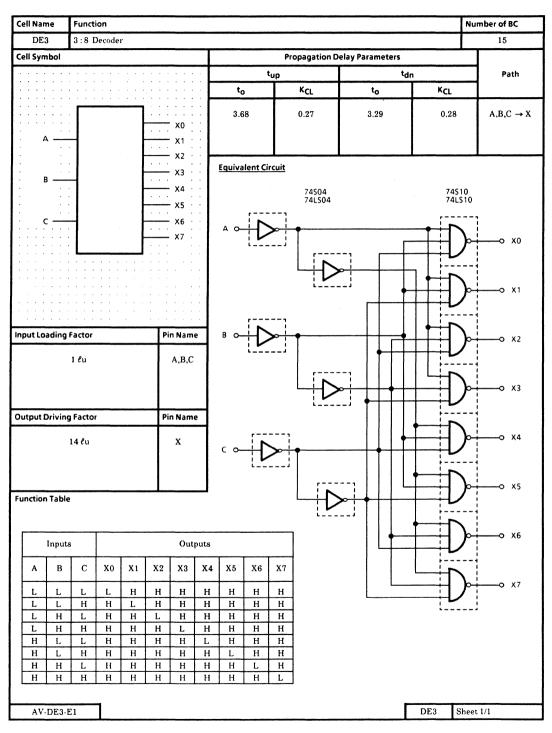
_	Unit Cell		Basic
Page	Name	Function	Cells
3-205	MC4	4-bit Magnitude Comparator	42
3-207	DE2	2:4 Decoder	5
3-208	DE3	3:8 Decoder	15
3-209	SM1	Schmitt Trigger Input	8
3-211	SM2	Schmitt Trigger Input	7
3-213	BD3	Buffer (Delay Cell)	5
3-214	BD5	Buffer (Delay Cell)	9
3-215	BD6	Buffer (Delay Cell)	17

3

Cell Name	Function											Ni	ımber	of BC
MC4	4-bit Mag	nitude Cor	nparator											42
Cell Symbol						Pı	opagati	on Dela	y Param	eters				
						t <sub>up</sub>			<sup>†</sup> dn			Path		Path
					to		KCL		to		Kc	L	]	
					9.25 8.77		$0.25 \\ 0.46$		8.70 8.33			14 13	3 A or B →	
B3 ——					4.75		0.25		4.60	2	0.	14	IF.	OG,OS C → OE
B2 ————————————————————————————————————					4.67 6.07	-	0.46 0.46		3.80 5.50	j	0.	13	10	$C \rightarrow OE$ $S \rightarrow OG$ , $G \rightarrow OS$ $\rightarrow OS or$
. A1					0.01		0.40		0.00	,	0.	10	"	og og
A0				:: -	D	aramete		Sv	mbol	MIN	TYP		MAX	UNIT
		:				aramete			507		+	+	-	- Olviii
IG —		<u> </u>	- OG · ·					_			<b>†</b>	+		<b>†</b>
1E		1	- OE					$\neg \dagger$			<del> </del>	+		
· · · IS —			- OS					$\dashv$			<del>                                     </del>	$\top$		
			• • • • •					$\neg$					-	
											$\top$			
Input Loading	Factor		Pin Na	me										
	3 ℓu		A,I											
	1 <i>l</i> u		IS,IE	,IG	····					···		_		ļ
			1	_						·				ļ
0.1.10:1-			-								+			
Output Driving	Factor		Pin Na	me										-
	18 ℓu 10 ℓu		OE OG,O	. H							-	-		<b> </b>
	10 tu		00,0	"  -				$\dashv$				-		<del> </del>
				}								+		<u> </u>
Function Table		<u> </u>							 T					L
74LS85 Compa	itible	ļ	Compari	ing Inputs	i I		ding In		0.7	Output				
		A3, B3	A2, B2	A1,B1	A0,B0		IS (A < B)	IE (A = B)	OG (A>B)	OS (A < B)	OE (A = B)			
		A3 > B3 A3 < B3	X X	X X	X X	X X	X X	X X	H L	L H	L L			
		A3 = B3 A3 = B3	A2>B2 A2 <b2< td=""><td>X X</td><td>X X</td><td>X X</td><td>X X</td><td>X X</td><td>H L</td><td>L H</td><td>L L</td><td></td><td></td><td></td></b2<>	X X	X X	X X	X X	X X	H L	L H	L L			
		A3 = B3 A3 = B3	A2 = B2 A2 = B2	A1 > B1 A1 < B1	X X	X X	X X	X X	H L	L H	L L			
		A3 = B3	A2 = B2 A2 = B2	A1 = B1	A0>B0	X X	X X	X X	H L	L H	L L			
		A3 = B3	A2=B2 A2=B2	A1 = B1	A0 = B0	X H	X	H	L H	L L	Н			
		A3 = B3	A2=B2 A2=B2 A2=B2	A1 = B1	A0 = B0	L H	H H	L L L	L L	H L	L L L			
		1 40 - 00	114-02	14:-5:	1 10 - BO			L						
		A3 = B3	A2 = B2	AI = BI	AU = BU	L	L	L	Н	Н	L			







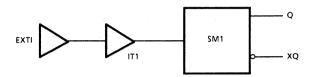
Cell Name	Function			***************************************				Number	of BC
SM1	Schmitt-Trigger Input	;							8
Cell Symbol				Propagation	n Delay Param	eters			
			t <sub>u</sub>	р	<sup>t</sup> dn			Path	
			to	K <sub>CL</sub>	to		KCL		
		- Q	7.70 12.7	0.16 0.16	10.6 7.4		0.10 0.11	I D	) → Q → XQ
D —			Parar	neter	Symbol	MIN	TYP	MAX	UNIT
		- xQ	Positive-going Voltage*		V <sub>T</sub> +	2.5	3.3	4.0	v
			Negative-goin Voltage*	g Threshold	V <sub>T</sub> -	0.7	1.4	2.0	v
			Hysteresis*		V <sub>T</sub> + - V <sub>T</sub> -	1.1	1.9	2.7	v
			Data Pulse W (Positive Pu Negative Pul	lse,	t <sub>DW</sub>		25**		
Input Loading	Factor	Pin Name							
Output Drivin	g Factor	Pin Name							
	18 <b>l</b> u	Q,XQ							
Equivalent Cir					Funct	ion Table			
D 0		D-		o XQ	Input D L H		ब 		
	Note: SM1 must not Also, the rule of		M2 in one chip.	O Q  be observed.					
		-	. 3						
AV-SM1-	E2						SM1 S	heet 1/2	

#### Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

#### Rule of Usage

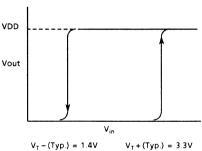
SM1 must be used with IT1, I/O cell for only protection circuit, as shown below. IT1 is available only for SM1.

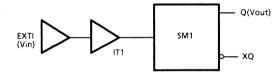


#### **AC Spec Condition**

$$V_{iL} = 0.6 \text{ V}, V_{iH} = 4.0 \text{ V}$$
  
 $t_r = t_f = 10 \text{ ns}$   
 $V_{DD} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

#### **Hysteresis Characteristics**





Note\*: The specification is expressed as follows:

Values of  $V_T + , V_T -$  and  $V_T + - V_T -$  are for reference only.

 $V_{IH_{(min)}} = V_{DD} \times 0.8 \text{ (V)}$ 

 $V_{\rm IL_{(max)}} = 0.6(V)$ 

 $(V_{DD} = 5V \pm 5\%, T_A = 0 \sim 70^{\circ}C)$ 

★\*minimum value with typical operation conditions.

AV-SM1-E2

SM1 Sheet 2/2

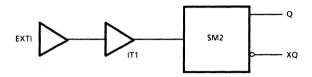
Cell Name	Function							Number	of BC	
SM2	Schmitt-Trigger Input	:							7	
Cell Symbol				Propagation	Delay Param	eters				
			tu	р	t <sub>dn</sub>			Path		
			to	KCL	to		KCL			
		- Q	7.30 0.16 13.8 0.14		11.6 6.50		0.13 0.07	l D	$\begin{array}{c} D \to Q \\ D \to XQ \end{array}$	
· · · · D —			Paran	neter	Symbol	MIN	TYP	MAX	UNIT	
		- XQ	Positive-going Voltage*	Threshold	V <sub>T</sub> +	1.4	1.9	2.5	v	
			Negative-goin Voltage*	g Threshold	V <sub>T</sub> -	0.8	1.3	1.8	v	
			Hysteresis*		$V_T + \overline{V}_{T^-}$	0.4	0.6	0.7	v	
			Data Pulse W (Positive Pu Negative Pul	lse,	t <sub>DW</sub>		25 <sup>**</sup>			
Input Loading	Factor	Pin Name								
	5 ℓu	D								
Output Drivin	g Factor	Pin Name								
***************************************	18 ℓu	0.40								
	18 tu	Q,XQ								
Equivalent Cir	rcuit	<u> </u>		A. 10	Funct	ion Table			<u> </u>	
D 0		<b>D</b> -		o XQ	Input D L	Q X L H	Q I			
		D-	<u> </u>	o Q						
	Note: SM2 must not l Also, the rule o	be used with S of usage on the	SM1 in one chip. e next page should	be observed.						
AV-SM2	E2						SM2 S	heet 1/2		

## Fujitsu CMOS Gate Array Unit Cell Specification

"AV" Version

#### Rule of Usage

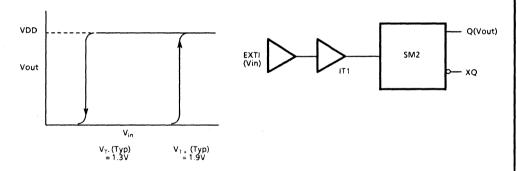
SM2 must be used with IT1, I/O cell for only protection circuit, as shown below. IT1 is available only for Schmitt-Trigger Input.



#### **AC Spec Condition**

$$\begin{array}{l} V_{1L} = 0.6 \; V, \, V_{1H} = 2.6 \; V \\ t_r = t_f = 10 \; ns \\ V_{DD} = 5 \; V, T_A = 25 ^{\circ}C \end{array}$$

#### **Hysteresis Characteristics**



Note\*: The specification is expressed as follows:

Values of  $V_T + , V_{T''}$  and  $V_{T} + - V_{T}$  - are for reference only.

$$V_{\rm IH_{(min)}} = V_{\rm DD} \times 0.5 \, (V)$$

$$V_{\rm IL_{(max)}} = 0.8(V)$$

 $(V_{DD} = 5V \pm 5\%, T_A = 0 \sim 70^{\circ}C)$ 

\*\*minimum value with typical operation conditions.

AV-SM2-E2

SM2

Sheet 2/2

Cell Name	Function							Number	of BC
BD3	Buffer (Delay Cell)								5
Cell Symbol				Propagation	Delay Param	eters			
			tu	p	H	<sup>t</sup> dn			Path
		::::::	to	KCL	to		KCL		
		::::: <b>-</b>			<u> </u>				
			11.80	0.16	11.7	6	0.10	į į	\ → X
		::::::		,		į		į	
								l	
			Parar	neter	Symbol	MIN	TYP	MAX	UNIT
		- ^ : : : : [							
							1		
							<b>†</b>		<del> </del>
		::::: <b> </b>					<del>                                     </del>		
					_		<del> </del>		
		: : : : <b> </b>					-		ļ
							<del> </del>		<b> </b>
		::::: <b>L</b>							
Input Loading	Factor	Pin Name							
							ļ		
	1 <i>l</i> u	A				<u></u>			ļ
		1 L							
Output Drivin	g Factor	Pin Name							
· · · · · · · · · · · · · · · · · · ·		<u> </u>							
	18 lu	х							
TTI Commission	• Ci i• (I i• F•	<u> </u>	Th						L
i i L Equivalen	t Circuit (Logic Function delay time is no	i Equivalent only ot equivalent.)	i ne propagati	on					
Ι.		7							
	$\sim \sim$	<del>-</del>							
į.		}							
	74504 74504								
	74LS04 74LS04								
AV-BD3-							BD3 S		

Cell Name	Function							Number	of BC
BD5	Buffer (Delay Cell)								9
Cell Symbol				Propagatio	n Delay Param	eters			
			tu	p		<sup>t</sup> dn			Path
			to	KCL	• t <sub>o</sub>		K <sub>CL</sub>		
			22.18	0.10	10.0		0.10		x → X
			22.18	0.16	18.7	°	0.10	, ,	. → x
			Parar		Symbol	MIN	TYP	MAX	UNIT
A —	$\rightarrow$	× : : : : :	Parar	neter	Symbol	IVIIN	1117	IVIAA	UNII
							<del> </del>		ļ
		: . : : : : <b>L</b>							
		: : : : : <b>-</b>			+		<b>†</b>	<del> </del>	<del> </del>
							<del> </del>	<del> </del>	ļ
		: : : : : <b> </b> _					-		ļ
		: : : : : <b>L</b>							
		[							
		: : : : : <b>-</b>					1		1
		· · · · · · -							
nput Loading	Factor	Pin Name —							
	1 <b>l</b> u						<del>                                     </del>		<u> </u>
							<del> </del>		<del> </del>
		<u> </u>			1		<del> </del>		<b></b>
							<b>†</b>		
Output Drivin	ig Factor	Pin Name —					<b>†</b>		<b>†</b>
	18 ℓu	х					1		
TTI Faviuslan	& Cinquit (Lauria Franction	Farmalant and	Theorem				<u> </u>	L	<u> </u>
i L Equivalen	nt Circuit (Logic Function delay time is no	Equivalent only t equivalent.)	r. The propagat	ion					
	[]	-;							
	$+$ $\searrow++$ $\searrow$	<del></del>							
		- !							
	74504 74504	1							
	74LS04 74LS0	)4							
	-								
AV-BD5-	F1						BD5 S	Sheet 1/1	

Cell Name	Function							Number	of BC
BD6	Buffer (Delay Cell)							17	
Cell Symbol			Propagation Delay Parameters						
			tu	p		tdn			Path
		::::: <b>[</b>	to	KCL	to		KCL		
		::::: <b>[</b>							
			43.10	0.16	32.6	0	0.10	- 1 '	A → X
						Ī		İ	
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A <u>-</u>		x * * * * *	Paran	neter	Symbol	MIN	TYP	MAX	UNIT
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3

# I/O Cell Family

Page	Unit Cell Name	Function
Input Buffe	ers	
3-219	I2B	Input Buffer (True)
3-220	I2BU	I2B with Pull-up Resistance
3-221	I2BD	I2B with Pull-down Resistance
3-222	ILB	Clock Input Buffer (True)
3-223	ILBU	ILB with Pull-up Resistance
3-224	ILBD	ILB with Pull-down Resistance
3-225	IKB	Clock Input Buffer (Inverter)
3-226	IKBU	IKB with Pull-up Resistance
3-227	IKBD	IKB with Pull-down Resistance
3-228	12C	CMOS Interface Input Buffer
3-229	I2CU	I2C with Pull-up Resistance
3-230	I2CD	I2C with Pull-down Resistance
3-231	IT1	Input Buffer for Schmitt Trigger Input
3-232	IT1U	IT1 with Pull-up Resistance
3-233	IT1D	IT1 with Pull-down Resistance
Output Bu	ffers	
3-234	O2B	Output Buffer (True
3-235	O2L	Power Output Buffer (True)
3-236	O4T	3-state Output Buffer (True)
3-237	O4W	Power 3-state Output Buffer (True)

## I/O Cell Family (Continued)

3-state Out	put and In	put Buffers
3-238	н6Т	3-state Output and Input Buffer (True)
3-239	H6TU	H6T with Pull-up Resistance
3-240	H6TD	H6T with Pull-down Resistance
3-241	H6W	Power 3-state Output and Input Buffer (True)
3-242	H6WU	H6W with Pull-up Resistance
3-243	H6WD	H6W with Pull-down Resistance
3-244	H6C	3-state Output and CMOS Interface Input Buffer (True)
3-245	H6CU	H6C with Pull-up Resistance
3-246	H6CD	H6C with Pull-down Resistance
3-247	H6E	Power 3-state Output and CMOS Interface Input Buffer (True)
3-248	H6EU	H6E with Pull-up Resistance
3-249	H6ED	H6E with Pull-down Resistance
3-250	H6D	3-state Input and Output Buffer for SM1, SM2
3-251	H6DU	H6D with Pull-up Resistance
3-252	H6DD	H6D with Pull-down Resistance
High-Drive	Buffers	
3-253	O2L2	O2L with 20mA Drive
3-254	O4W2	O4W with 20mA Drive
3-255	H6W2	H6W with 20mA Drive
3-256	H6W1	H6WU with 20mA Drive
3-257	H6W0	H6WD with 20mA Drive
3-258	H6E2	H6E with 20mA Drive
3-259	H6E1	H6EU with 20mA Drive
3-260	H6E0	H6ED with 20mA Drive
3-261	O2B2	O2B with 10mA Drive
3-262	O2B3	O2B with 15mA Drive
3-263	O4T2	O4T with 10mA Drive
3-264	O4T3	O4T with 15mA Drive
3-265	H6T2	H6T with 10mA Drive
3-266	H6T3	H6T with 15mA Drive
3-267	H6C2	H6C with 10mA Drive
3-268	H6C3	H6C with 15mA Drive
3-269	O1T	Crystal Oscillator CMOS Interface Input Buffer with Schmitt Trigger
3–270	OT1	Output Buffer with Protection Circuit Only

Cell Name	Function							Number	of BC
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Cell Name	Function							Number	of BC
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AV-ILBD-	-E1						ILBD :	Sheet 1/1	

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IKB	Clock Input Buffer (Ir	ivert)							-
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IKBU Clock Input Buffer with Pull Up Resistance (Invert)	Cell Name	Function							Number	of BC
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Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit								+		<del> </del> -
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit			· · · · · · L							
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit									1	
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit										<b>†</b>
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit									<del>                                     </del>	<del> </del>
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit				.,					ļ	ļ
Output Driving Factor Pin Name  360 lu CI  TTL Equivalent Circuit									1	ļ
Dutput Driving Factor Pin Name  360 éu CI  TTL Equivalent Circuit										
360 lu CI  TTL Equivalent Circuit	ut Loading Fa	actor	Pin Name —			+		<del></del>	<del>                                     </del>	<del> </del>
360 eu CI  TTL Equivalent Circuit										<del> </del>
360 eu CI  TTL Equivalent Circuit										
360 fu CI  TTL Equivalent Circuit			1							
360 fu CI  TTL Equivalent Circuit										
360 fu CI  TTL Equivalent Circuit								<del>                                     </del>	<del> </del>	
TTL Equivalent Circuit	put Driving I	Factor	Pin Name —		<del></del>			<del>                                     </del>	<del></del>	<del> </del>
TTL Equivalent Circuit	36	60 ℓu						+		
74540						-		<del> </del>	<u> </u>	<del> </del>
74540			1 F							<del> </del>
74540										
	Equivalent (	Circuit								
		<del></del>								
			W. Parallelian							
	•,	1" 745	40							
Note: This cell is available for AVB Series or	'	. /45	~~							
Note: This cell is available for AVB Series or										
						Note: This	ell is ava	ilable for A	VB Series o	nly.
AV-IKBD-E1 IKBD Sheet 1/1	AV-IKBD-F	:1					Г	IKBD S	Sheet 1/1	

Cell Name	Function							Number	of BC
12C	CMOS Interface Inpu	t Buffer			,			1	-
Cell Symbol				Propagation	Delay Param	eters		1	
			t <sub>i</sub>	р		<sup>t</sup> dn			Path
			to	KCL	to		K <sub>CL</sub>		
			2.29	0.08	2.4		0.05		X → PI
			1	0.13	[.		0.07	- 1	. → NI
			t <sub>dn</sub> (PI)* +0.48		t <sub>up</sub> (P +0.3	35			
<b>x</b>		NI · · ·	Parar	neter	Symbol	MIN	TYP	MAX	UNIT
		PI · · ·	High-level Inp	ut Voltage	$v_{\text{IH}}$	V <sub>DD</sub> ×0.7			v
			Low-level Inp	ıt Voltage	V <sub>IL</sub>			V <sub>DD</sub>	v
								×0.3	<del> </del>
							<del>                                     </del>	<del> </del>	<u> </u>
							<del> </del>	1	<b>†</b>
					1				<b>†</b>
	• • • • • • • • • • •								<del> </del>
					1				<b>†</b>
		T						ļ	
Input Loading	Factor	Pin Name							
		1							
Output Drivin	g Factor	Pin Name							
	00.0						ļ	<b></b>	ļ
	36 lu 18 lu	PI NI					<u> </u>	<u> </u>	<del> </del>
					-		-	<u> </u>	<del> </del>
							,		
TTL Equivalen	t Circuit					Functio	n Table		
	[	,	-, [	7		INPU	JT OUT	TPUTS	
× 0		$\Box$			IN C	х		NI	
				74504 74L504		L	L	H L	
	74504	74504				L			
	74LS04	74LS04	<del></del>		O PI				
NOTE	District of the second	v.C. (6)							
NOTE*:	$t_{dn}(PI) = t_0(dn) + K_{CL}(dn) + t_{up}(PI) = t_0(up) + K_{CL}(up)$	× CL(fu)							

Cell Name	Function							Number	of BC
12CU	CMOS Interface Inp	out Buffer with P	ull Up Resistance	(True & Inver	t)				-
Cell Symbol				Propagation	Delay Paran	neters			
			tu	p		<sup>t</sup> dn	····		Path
			to	KCL	to	,	KCL		
			2.29	0.08	2.4	1	0.05	ı	X → CI
			t <sub>dn</sub> (PI)* +0.48	0.13	t <sub>.ip</sub> (1 +0	PI)* .35	0.07	)	√ → NI
· · · · · <b>x</b>			Paran	neter	Symbol	MIN	TYP	MAX	UNIT
	<b></b>		Input High Vo	ltage	V <sub>IH</sub>	V <sub>DD</sub>			v
		::::: <b>!</b>				×0.7			
			Input Low Vol	tage	$\mathbf{v}_{\scriptscriptstyle \mathrm{IL}}$			$v_{\scriptscriptstyle DD}$	v
								×0.3	
	• • • • • • • • • •								
					-	<b></b>			<del>                                     </del>
									<u> </u>
						İ			<del> </del>
									ļ
nput Loading	Factor	Pin Name				ļ			ļ
									ļ
		1 1							
Output Driving	g Factor	Pin Name							
		1							
	36 lu 18 lu	PI NI							
	1014	'''							
TTL Equivalen	t Circuit					Function	n Table		<u> </u>
•					- PI	<u></u>		1	
	[]	[]	;	:		INPU	т от	PUTS	
				į		Х	PI	NI	
× 0		<b>TI</b>		>	- NI	L	L	Н	
	ii					Н	Н	L	
	74504 74L504	74504 741 504	74504 741504						
NOTE*:	ti. (PI) = tidni + Koolda	×CL for							
015.	$t_{dn}(PI) = t_0(dn) + K_{CL}(dn)$ $t_{up}(PI) = t_0(up) + K_{CL}(up)$	or × CL .fur							
				No	te: This cell i	is available	for AVB Se	eries only.	

Cell Name	Function							N	umber	of BC
I2CD	CMOS Interface Inpu	it Buffer with P	ull Down Resista	nce (True & Inv	vert)					-
Cell Symbol				Propagation	n Delay Paran	neters				
			t,	nb	,	<sup>t</sup> dn				Path
			to	KCL	to	,	K	CL		
			2.29	0.08	2.4	. 1	(	0.05	١,	ζ → PI
				0.13				0.07	1	L → NI
			t <sub>dn</sub> (PI)* +0.48		t <sub>up</sub> (I + 0.	35				
· · · · · x		NI · · ·	Para	meter	Symbol	MIN	TY	Р	MAX	UNIT
		PI · · ·	Input High Vo	oltage	V <sub>IH</sub>	Vnn	1			V
						V <sub>DD</sub> ×0.7				
			Input Low Vo	ltage	VIL		+	$ \frac{1}{v}$	SD	v
			•					×	DD (0.3	
					1		1			
							1		***************************************	
						<b></b>	1		······································	
							†			
							+	_		
	· · · · · · · · · · · · · · ·						1			
Input Loading	Factor	Pin Name			<u> </u>		<b>†</b>			
				***************************************		<u> </u>				
		1 1								
							1			
Outrus Dairies	- F	Pin Name								
Output Driving	g ractor	Pin Name								
	36 ℓu 18 ℓu	PI NI								
	1014	" [								
TTL Equivalen	• Cii•					Eumoti	on Table			<u> </u>
i i L'iquivalen	Circuit				- Pi					
	,	,	,	,		INP	UT	OUTPU	TS	
						7			NI	
× 0		∄ >∾	<del>・</del>	<b>&gt;</b>	- NI	ı	_	L	Н	
				i		L F	1	Н	L	
	74504 74LS04	74504 74LS04	74504 74LS04							
NOTE*: t	$t_{dn}(PI) = t_0(dn) + K_{CI}(dn)$	× C <sub>L</sub> (fu)								
t	$t_{dn}(PI) = t_0(dn) + K_{CL}(dn)$ $t_{up}(PI) = t_0(up) + K_{CL}(up)$	$\times C_L \cdot \ell u$								
				Note: This	cell is availal	ole for AV	B Series	only.		

Cell Name	Function							Number	of BC
IT1	Input Buffer for Schmi	itt Trigger Inp	out						_
Cell Symbol				Propagation	n Delay Paran	neters			
				t <sub>up</sub>	T	tdn		_	Path
			to	KCL	to		KCL	_	
				1					
			0	0	0	I	0		$X \rightarrow IN$
						لــــــــــــــــــــــــــــــــــــــ			
	*	IN	Par	ameter	Symbol	MIN	ТҮР	MAX	UNIT
1									
Input Loading	Enetar	Pin Name							
input Loading	ractor	riii Naine							
Output Drivin	n Factor	Pin Name							
output birtiii	g . u cto.	7							
		II							
Note: IT1 is	the input protection circ	cuit only for SI	M1,SM2						
									,
AV-IT1-E	1					Г	IT1 S	heet 1/1	
							10		

	1								
Cell Name	Function							Numi	oer of BC
IT1U	Input Buffer for Schmi	tt Trigger Inp	ut with Pull Up	Resistance					-
Cell Symbol				Propagation	n Delay Param	eters		i	
			t	up		<sup>t</sup> dn			Path
			to	KCL	to		K <sub>CL</sub>		
					<del>                                     </del>			-	
			0	0	0		0	ı	$X \rightarrow IN$
				İ	1	1		- 1	
	×	- IN · · ·	Para	meter	Symbol	MIN	TYP	MA	X UNIT
					<u> </u>		<del>                                     </del>	+	
							<del> </del>	+	
							<b>-</b>		
								-	1
							1	1	
							<del> </del>	+	
					+		<b>_</b>	+-	
			<del></del>		<del>                                     </del>		<del> </del>	+	
Input Loading	Factor	Pin Name					<del>                                     </del>	+	
					+		<del> </del>	+	
				· · · · · · · · · · · · · · · · · · ·	_		<del>                                     </del>	1	
							<del> </del>		
					<del></del>		<del> </del>	+	
Output Driving	g Factor	Pin Name			-		1	+	
					<del>-</del>		<u> </u>	1	
							<del> </del>	†	
Notes ITILI	is the input protection c		CM1 CM9		<u>L</u>		<u> </u>		
Note: IIIO	is the input protection c	reult only for	SW11, SW12						
				1	Note: This ce	ll is availa	ble for AV	B Series	only.
L									
AV-IT1U-	E1						IT1U	Sheet 1	/1

Cell Name	Function							Number	of BC
IT1D	Input Buffer for Schn	nitt Trigger Inpu	t with Pull Dow	n Resistance					-
Cell Symbol	*	T			n Delay Param	eters			
			t	1b		<sup>t</sup> dn			Path
		· · · · · · · <b> </b>	to	KCL	to		KCL		
		· · · · · · · · <b> </b>						1 ,	
			0	0	0		0	'	I→IN
						l			
		· · · · · · · · · <b> </b>		<u> </u>	1		T Tun		
	*	IN	Para	meter	Symbol	MIN	TYP	MAX	UNIT
							<b>-</b>		
							<b></b>		
		L							
		-							
					+		†		
		· · · · · · -					<del> </del>		
		-					<del> </del>		ļ
		- : : : : : L							
		::::: <b>L</b>							<u> </u>
Input Loading	Factor	Pin Name -							
mpat Louding		- Till teame							
Outrus Deivine	- Fo do-	Pin Name							
Output Driving	g ractor	Pin Name -							
		11							
Note: IT1D i	is the input protection	circuit only for S!	M1, SM2						
				7	Note: This cell	is availa	ble for AVR	Series only	1.
					Impeen				

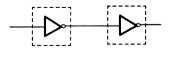
Cell Name	Function							Nur	Number of BC			
O2B	Output Buffer (True)							T				
Cell Symbol				Propagation I	Delay Param	eters						
			t	up ,		<sup>t</sup> dn			Path			
		to			t <sub>o</sub>							
		1.35 (6.15)	0.08	4.39 (8.59)		0.07		OT → X				
			Para	meter	Symbol	MIN	ТҮР		АХ	UNIT		
х :			Para	Parameter		IVIIN	1177	14	^^	UNII		
					1		-	┼				
					<u> </u>		-	┼				
							+	┼				
					<u> </u>		<del>                                     </del>	+				
			~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	*	<u> </u>		+	+-				
					<u> </u>		-	$\vdash$				
								<del> </del>				
							+	I				
	· · · · · · · · · · · · · · · · · · ·						<del>                                     </del>	<u> </u>	$\neg \uparrow$			
Input Loading	Factor	Pin Name			<b> </b>		<del></del>	†				
	2 <b>l</b> u	ОТ			1			1				
					1				$\neg \uparrow$			
				···			1					
Output Driving	Footon	Pin Name										
Output Driving	, ractor	Pili Name										
					l		1	<u> </u>				
Note: 1: The unit of K <sub>CL</sub> is ns/pF. 2: Output load capacitance of 60pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation.												
TTL Equivalent	: Circuit											
	>   >											
				Note:	This cell is a	vailable!	for AVB Ser	ies on	ly.			
	504 /4504 -504 74L504											
AV-O2B-I	€1					Г	O2B	Sheet	1/1			

Cell Name	O2L Power Output Buffer (True)							Number of BC			
O2L								_			
Cell Symbol											
		t <sub>up</sub>		t <sub>dn</sub>			Path				
			to	KCL	to		KCL				
			2.20 (4.60) 0.04		4.30 (6.70	4.30 (6.70)		(	$OT \rightarrow X$		
			Paran	neter	Symbol	MIN	ТҮР	MAX	רואט		
01 -		Pin Name									
nput Loading	2 lu	OT									
Output Drivin	g Factor	Pin Name									

Note: 1: The unit of  $K_{CL}$  is ns/pF.

- 2: Output load capacitance of 60pF is used for Fujitsu's logic simulation. 3: The parameters in parentheses are the values applied to the simulation. 4:  $V_{OL} = 0.5V$  at  $I_{OL} = 10mA$ ,  $T_A = 0 \sim 70^{\circ}C$ ,  $V_{DD} = 5V \pm 5\%$

### **TTL Equivalent Circuit**



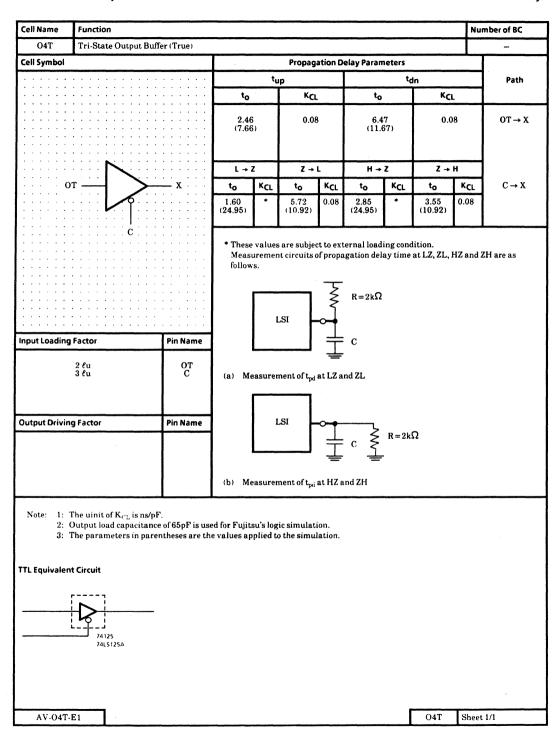
74504 74LS04

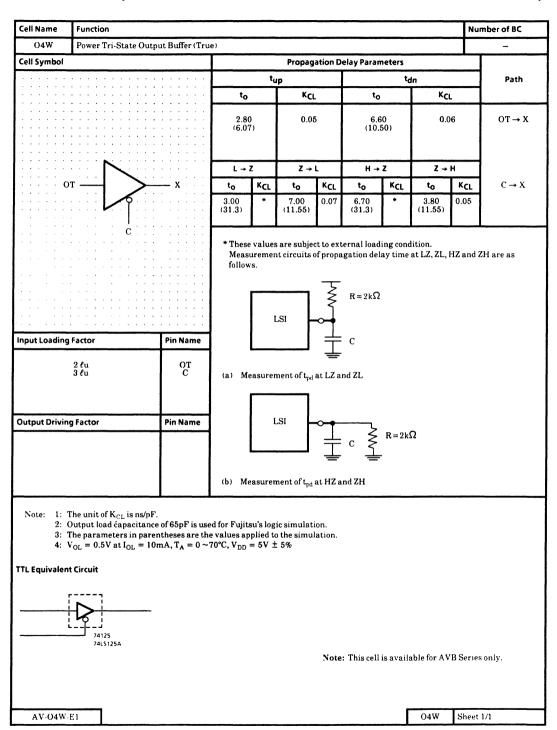
74504 74LS04

AV-O2L-E1

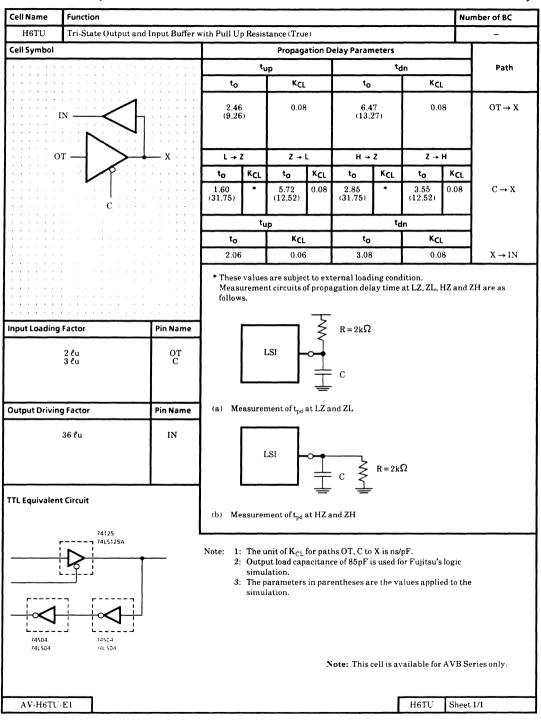
Note: This cell is available for AVB Series only.

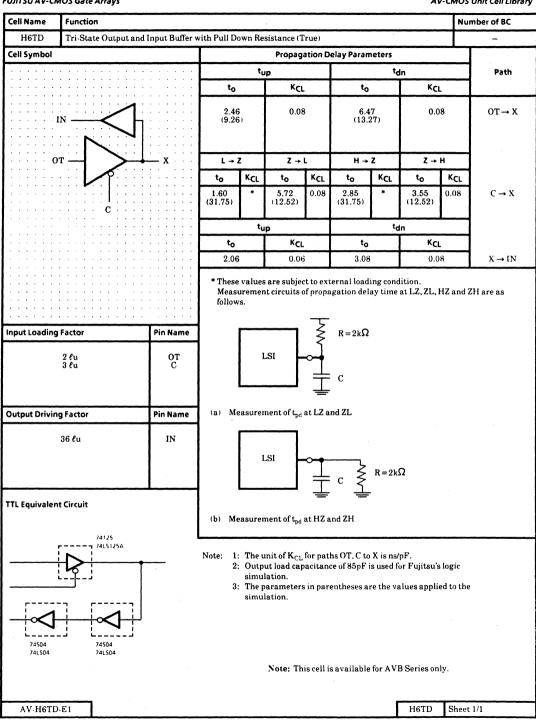
O2L Sheet 1/1



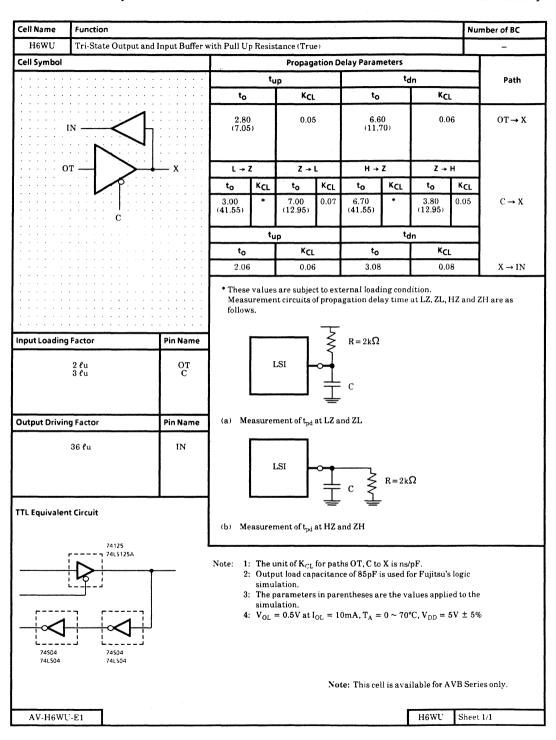


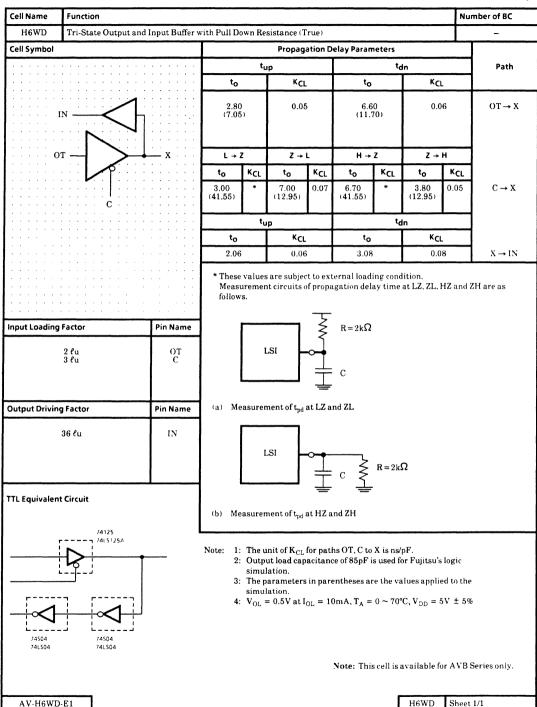
Cell Name	Function									Nur	mber of BC
Н6Т	Tri-State Output and I	nput Buffer (	True)								-
Cell Symbol					Propag	ation D	elay Param	neters			
				tլ	1b			t <sub>c</sub>	in		Path
			to		KCL		to		KCI		
			2.46 (9.26		0.08		6.4 (13.2		0.0	8	$OT \rightarrow X$
	OT.	x · · ·	L→i	Z	Z →	L	H→	z	Z→	н	
			to	KCL	to	KCL	to	KCL	to	KCL	
			1.60 (31.75)	•	5.72 (12.52)	0.08	2.85 (31.75)	*	3.55 (12.52)	0.08	$C \to X$
				tu	ıp			t <sub>c</sub>	in		
			to		KCL		to		KCI		
			2.06		0.06		3.08		0.0	8	$X \rightarrow IN$
Input Loading	ı Factor	Pin Name	follow			*	$R = 2k\Omega$				
	2 lu 3 lu	OT C		]	LSI		: <b>с</b>				
Output Drivin	g Factor	Pin Name	(a) Me	easurei	ment of t <sub>pd</sub>	at LZ a	nd ZL				
	36 ℓu	IN		1	LSI _	<b>⊶</b>		R = 2k	Ω		
TTL Equivalen	nt Circuit		(b) Me	easurei	ment of t <sub>pd</sub>	at HZ a	ind ZH	-			
74504 74504	74125 74LS125A 74LS125A	·	2:	Outp simu The p	ut load cap lation.	acitan		is used f	/pF. or Fujitsu's alues appli		
AV-H6T-	E1								Н6Т	Sheet	1/1





Cell Name	Function									Nu	mber of BC
H6W	Power Tri-State Outpo	ut and Input E	Buffer (True	2)						$\top$	_
Cell Symbol					Propag	ation D	elay Paran	neters		-	
			1	tu	ıp			tc	in		Path
			to		KCI		to		KCI		
			2.80 (7.05	)	0.05		6.6		0.0		$OT \rightarrow X$
	т	x	L→	Z	Z →	L	H→	z	Z →	н	
			to	KCL	to	KCL	to	KCL	to	KCL	
	C		3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05	$C \rightarrow X$
				tu	ıp			to	In		
			to		KCL		to		KCI		
			2.06		0.06		3.08		0.0	8	$X \rightarrow IN$
	2 lu 3 lu	OT C		I	LSI		C				
Output Drivin	g Factor	Pin Name	(a) Me	asurer	nent of t <sub>pd</sub>	at LZ a	nd ZL				
	36 lu	IN		I	LSI	~ <del>_</del>		R = 2k!	Ω		
TTL Equivalen	t Circuit		(b) <b>M</b> e	asuren	nent of t <sub>pd</sub>	at HZ a	nd ZH	•			
7.4504	74125 74L5125.a	<u> </u>	Note: 1: 2: 3:	The u Outp	init of K <sub>CL</sub> ut load cap lation. arameters lation.	for pati acitano in par	hs OT, C to ce of 85pF i	s used for	pF. or Fujitsu's alues applic CC, V <sub>DD</sub> = 5	ed to the	
74LS04	74L\$04					N	ote: This	cell is av	vailable for	AVB Se	eries only.





Cell Name	Function									N	ımber	of BC
H6C	Tri-State Output and O	CMOS Interfa	ce Input Bu	ıffer (T	rue)							_
Cell Symbol					Propaga	tion D	elay Paran	neters			T	
				tu	р			to	ln		]	Path
			to		KCL		to		KCL	-		
	IN —		2.46 (9.26		0.08		6.4 (13.		<b>0</b> .0	8	C	T → X
	OT	x	L⇒i	2	Z → I		H→	Z	Z →	н	1	
			to	KCL	to	KCL	to	KCL	to	KCL	1	
			1.60 (31.75)	*	5.72 (12.52)	0.08	2.85 (31.75)	*	3.55 (12.52)	0.08	1 '	$\mathbb{C} \to X$
				t <sub>u</sub>	D			to	ln	L	1	
			to		KCL	,	to		KCL		1	
			2.29		0.08		2.41		0.0		1 >	X → IN
				Parar	neter		Symbol	MIN	TYP		MAX	UNIT
			Input H	ligh Vo	ltage		V <sub>IH</sub>	V <sub>DD</sub> ×0.7				V
Input Loadin	g Factor	Pin Name	Input L	ow Vol	tage		V <sub>IL</sub>				OD 0.3	v
	2 lu 3 lu	OT C		aremer	s are subjec at circuits o					HZ and	ZH are	: as
Output Drivi	ng Factor	Pin Name				3	R=2kΩ					
	36 lu	IN		1	LSI		: c					
TTL Equivale	nt Circuit	L	(a) Me	easurei	nent of t <sub>pd</sub>	at LZ a	ınd <b>Z</b> L					
	74125 74L5125A			1	LSI		c \( \frac{1}{2} \)	R = 2k	Ω			
-√≪1			(b) Me	easurei	nent of t <sub>pd</sub>	at HZ	and ZH					
74504 74LS04	745Q4 74L504		2	Outp	init of K <sub>CL</sub> ut load cap parameters	acitan	ce of 85pF	is used f	or Fujitsu's			
			Note: Th	nis cell	is available	e for A	VB Series	only.				
								1	H6C	_	et 1/1	

Cell Name	Function									Nu	mber o	of BC
H6CU	Tri-State Output and	CMOS Interfa	ice Input B	uffer w	ith Pull Up	Resist	ance (True	:)		T	-	-
Cell Symbol					Propag	ation D	elay Parar	neters			П	
				tu	ıp.		I	tdı	n		1	Path
			to		KCI		to		KCL		1	
	$\sim$		2.46		0.08		6.4	17	0.0		0	T → X
		x	L →	Z	Z →	L	H→	z	2 →	н		
			to	KCL	to	KCL	to	KCL	to	KCL	1	
			1.60 (31.75)	*	5.72 (12.52)	0.08	2.85 (31.75)	•	3.55 (12.52)	0.08	C	C→X
				t <sub>u</sub>	D	I		tdr				
			to		KCL		to	T	KCL			
			2.29	,	0.08		2.41		0.0		х	→ IN
				Paran	neter		Symbol	MIN	TYP		/AX	UNIT
			Input H	ligh Vo	ltage		V <sub>IH</sub>	v <sub>DD</sub> ×0.7				V
nput Loading	Factor	Pin Name	Input L	ow Vol	tage		V <sub>IL</sub>			V <sub>D</sub>		v
Output Driving	ı Factor	Pin Name	follow	s.		7						
	36 ℓu	IN		I	.sı	~ -	R = 2kΩ					
TL Equivalent	Circuit		(a) Me	easurer	nent of t <sub>pd</sub>	at LZ a	ind ZL					
	74125 74LS125A			I	.si _	~ <u>†</u>	c \( \frac{1}{2} \)	R=2kΩ	Σ			
			(b) Me	asuren	nent of t <sub>pd</sub>	at HZ a	and ZH					
74504 74L504	74504 74LS04		2:	Outp	ut load cap	acitan	hs OT, C to ce of 85pF entheses a	is used for	r Fujitsu's			
			Note: Thi	is cell is	available		7D.C	nlu				
					available	ior A v	B Series o	my.				

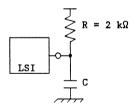
Cell Name	Function									Nu	mber o	of BC
H6CD	Tri-State Output and O	CMOS Interfa	ce Input B	ıffer w	ith Pull Do	wn Res	sistance (Tr	ue)				-
Cell Symbol					Propaga	tion D	elay Paran	neters				
				tլ	ıþ			t <sub>c</sub>	In		]	Path
			to		KCL		to		KCI			
			2.46 (9.26		0.08		6.4 (13.		0.0	8	0	$T \to X$
· · · · · · · · · · · · · · · · · · ·	т	x	L → i	Z	Z → 1		H→	Z	2 →	н	ł	
			to	KCL	to	KCL	to	KCL	to	KCL	1	
	C		1.60 (31.75)	*	5.72 (12.52)	0.08	2.85 (31.75)	*	3.55 (12.52)	0.08	(	$C \to X$
				t	ıp			to	ln	<b></b>	1	
			to		KCL		to		KCI		1	
			2.29	1	0.08		2.41		0.0	5	х	. → IN
				Parar	neter		Symbol	MIN	TYP	,	ИΑХ	UNIT
			Input H	ligh Vo	ltage		V <sub>iH</sub>	$V_{DD} \times 0.7$				v
Input Loading	Factor	Pin Name	Input L	ow Vol	tage		V <sub>IL</sub>			V <sub>E</sub>	D ).3	v
	2 lu 3 lu	OT C		ıremer	s are subjec nt circuits o					HZ and	ZH are	as
Output Drivin	ng Factor	Pin Name		r		Z	R=2k <b>Ω</b>					
	36 ℓu	IN		1	LSI		- c					
TTL Equivaler	nt Circuit		(a.) Me	easurei	ment of t <sub>pd</sub>	at LZ a	ınd ZL					
74504	74125 74L5125A		Note: 1	easurer	ment of t <sub>pd</sub>	for pat	hs OT, C to			logics	imulati	ion.
74LS04	74L 50-4		3	The	parameters is available	in par	entheses a	re the va				
							0	,. •				
AV-H6CI	D-E1								H6CD	Shee	t 1/1	

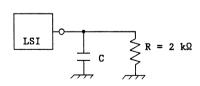
Cell Name	Function									Nu	mber o	f BC
H6E	Power Tri-State Outp	ut and CMOS	Interface l	nput Bu	ıffer (True	)						-
Cell Symbol					Propaga	ation D	elay Parar	neters				
				tu	ıp			to	In		]	Path
			to		KCL		to		KCI			
			2.80 (7.05	)	0.05	;	6.6 (11.	60 70)	0.0	6	0	T → X
o	or _	x	L→	z	Z →	L	H→	Z	Z →	н	1	
			to	KCL	to	KCL	to	KCL	to	KCL	1	
	C		3.00 (41.55)	*	7.00 (12.95)	0.07	6.70 (41.55)	*	3.80 (12.95)	0.05	(	C → X
				tu	p	<b>L</b>		to	ln	<u> </u>	1	
			to		KCL		to		KCI		1	
			2.29	)	0.08		2.41		0.0	5	x	→IN
				Paran	neter		Symbol	MIN	TYP	N	ЛАХ	UNIT
			Input H	ligh Vo	ltage		V <sub>lH</sub>	V <sub>DD</sub> ×0.7				V
Input Loading	Factor	Pin Name	Input L	ow Vol	tage		V <sub>IL</sub>			V <sub>D</sub>		v
	2 lu 3 lu	OT C		uremer			ternal load agation del			HZ and	ZH are	as
Output Drivin	g Factor	Pin Name	1			3	$R = 2k\Omega$					
	36 ℓu	IN		I	_SI _	<b>~</b>	: c					
TTL Equivalen	nt Circuit	:	(a) Me	easurer	nent of t <sub>pd</sub>	at LZ a	nd ZL					
	74125 74L\$125A			I	LSI		c \{ \frac{1}{2}	R=2k	Ω			
			(b) Me	easurer	nent of t <sub>pd</sub>	at HZ a	and ZH					
74504 74L504	74504 74LS04		2: 3:	Outp The p	ut load cap arameters	acitan in par	hs OT, C to ce of 85pF entheses a 0mA, T <sub>A</sub> =	is used for re the va	or Fujitsu's Ilues appli	ed to th	e simul	
AV-H6E-	F1		Note: Th	is cell i	s available	for AV	B Series o	nly. [	H6E	Shee	1/1	

Cell Name	Function									N	umber c	of BC
H6EU	Power Tri-State Outpu	it and CMOS	Interface II	nput B	uffer with F	ull Up	Resistanc	e (True)				_
Cell Symbol					Propaga	tion D	elay Paran	neters				
				tı	ıb			td	ln		1	Path
			to		KCL		to		KCI	_	1	
			2.80 (7.05	) 5)	0.05		6.6 (11.		0.0	6	0	)T → X
	от	_ x	L→i	Z	Z → I		H→	Z	Z →	н	1	
			to	KCL	to	KCL	to	KCL	to	KCL	1	
	C		3.00 (41.55)	•	7.00 (12.95)	0.07	6.70 (41.55)	•	3.80 (12.95)	0.05		$C \to X$
				<u> </u>	ıp			t <sub>d</sub>	ln	<u> </u>	1	
			to		K <sub>CL</sub>		to		KCI		1	
			2.29		0.08		2.41		0.0		<b>1</b> x	→IN
				Parar	neter		Symbol	MIN	TYP		MAX	UNIT
			Input H	ligh Vo	ltage		V <sub>tH</sub> ·	V <sub>DD</sub> ×0.7				V
nput Loading	Factor	Pin Name	Input L	ow Vo	tage		VIL			V <sub>1</sub>	<sub>DD</sub> ×0.	. V
	2 lu 3 lu	OT C		aremei	s are subjec nt circuits o					HZ and	ZH are	as
Output Drivin	ng Factor	Pin Name				3	$R = 2k\Omega$					
	36 lu	IN		1	LSI		: C					
TTL Equivaler	nt Circuit		(a) Me	asure	ment of t <sub>pd</sub> :	at LZ a	nd ZL					
	74125 74L5125A			1	LSI	<b>○</b>		R = 2k\$	Ω			
/4504 741504	74504 741504		Note: 1: 2: 3:	The to	ment of t <sub>pe</sub> ; unit of K <sub>CL</sub> out load cap parameters = 0.5V at I	for pat acitan in par	hs OT, C to ce of 85pF entheses a	is used for re the va	or Fujitsu's Hues appli	ed to th	ie simul	
AV-H6EU	J-E1		Note: Th	is cell i	s available	for AV	B Series o	nly.	H6EU	Shee	et 1/1	

Celi Name	Function									N	umber	of BC
H6ED	Power Tri-State Outp	ut and CMOS	Interface I	nput Bi	ıffer with F	Pull Do	wn Resista	nce (Tru	ie)	$\neg$		_
Cell Symbol					Propaga	ation D	elay Parar	neters				
				tu	р			td	İn		1	Path
			to		KCL		to		KCI	L.	7	
			2.80		0.05		6.6	:0	0.0	6		T → X
	IN		(7.05		0.00		(11.		0.0			1 - 1
	т	_ x	L→i	Z	2 →	L	H→	Z	Z →	н	1	
			to	KCL	to	KCL	to	KCL	to	KCL	]	
	C		3.00 (41.55)	•	7.00 (12.95)	0.07	6.70 (41.55)	•	3.80 (12.95)	0.05		C → X
				tu	D	-		td	n		1	
			to		KCL		to		KCI		1	
			2.29		0.08		2.41		0.0	5	<b>1</b> x	C→IN
				Paran	neter		Symbol	MIN	TYP		MAX	UNIT
			Input H	ligh Vo	ltage		$V_{!H}$	V <sub>⊃D</sub> ×0.7				V
nput Loading	Factor	Pin Name	Input L	ow Vol	tage		V <sub>IL</sub>			V 0.	× 3	V
Output Drivin	og Eactor	Pin Name		aremen				ay time	at LZ, ZL,	HZ and	ZH are	as
Jacpat Direit	ig ractor	riii waiiie				⋛	$R = 2k\Omega$					
	36 ℓu	IN		I	SI	<b>○</b>	C					
TL Equivaler	nt Circuit		(a) Me	easuren	nent of t <sub>od</sub> :	at LZ a	nd ZL					
	74125 7 74151254			1	.sı	<b>○</b> •	<del></del> -}	R = 2k\$	<b>.</b>			
						İ	c 🚽	K=2K2	.2			
-			(b) Me	asuren	nent of t <sub>pd</sub> :	at HZ a	nd ZH					
74864 746804	74504 746504		2: 3:	Outpo The p	it load cap arameters	acitano in par	entheses a	is used fo re the va	pF. or Fujitsu's dues applic C, V <sub>DD</sub> = 5	ed to th	e simul	
AV-H6ED	)-E1		Note: Thi	is cell i	s available	for AV	'B Sertes o	niy.	H6ED	Shee	or, 1/1	
									11000			

FUJITSU C	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"A	V" Version
	Function					Number of BC
				····		
H6D	Tri-state Outpu					_
Cell Symbol		P	ropagation	Delay Para		
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.46	0.08	6.47	0.08	OT → X
		(9.26)	_	(13.27)	_	
,	_	0	0	0	0	X → IN
IN	-					
,	$\backslash \backslash $					
от	X					
01	A					
l	Y					
	Ċ					
		L →	· Z	Z	<u>'</u> → L	
		t0	KCL	t0	KCL	$\neg c \rightarrow x$
		1.60		5.72	0.08	
		(31.75)	*	(12.52)		
					ł	
					<u> </u>	
	Input Loading				1	
Pin Name	Factor (lu)				1	
OT	2		L		L	
С	3	Н →			→ H	_
		t0	KCL	t0	KCL	_
	D-1	2.85	*	3.55	0.08	
Din Name	Output Driving	(31.75)	*	(12.52)		
Pin Name	Factor (lu)		1		1	
			1		1	
			1		1	
		l	l .	1	1	

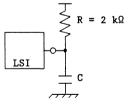


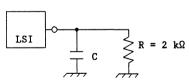


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.
  - 4. H6D is the bidirectional protection circuit only for SM1, SM2.

A	١V	-H	61	)-E1	She	et	1/	1

	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"2	AV" Version
Cell Name	Function					Number of BC
	Tri-state Outpu	t and Input	Buffer fo	r SM1, SM2		
H6DU	with Pull Up Re	sistance			1	_
Cell Symbol		P	ropagation	Delay Para	meter	
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.46	0.08	6.47	0.08	OT → X
		(9.26)		(13.27)		
		0	0	0	l 0	X → IN
			1			
IN	—< h				i	
	N 7		İ			
от —	<b>X</b>		Į.		}	
			Ì			
			1			
			1			
	Ċ		i			
	· ·		ļ			
		L -	<u> </u>	Z	→ L	
		t0	KCL	t0	KCL	¬ с → х
		1.60		5.72	0.08	
		(31.75)	*	(12.52)		ļ
		(01.75)		(12.32)		
	Input Loading					
Pin Name	Factor (lu)					
OT	2					
C	3	Н -	7.	7	→ H	
Ü		t0	KCL	t0	KCL	
		2.85	KOL	3.55	0.08	-
	Output Driving	(31.75)	*	(12.52)	0.08	
Pin Name	Factor (lu)	(31.73)	"	(12.32)		
I III Name	ractor (ku)					
				1	l	
		L	L	l	L	

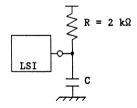


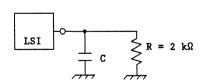


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.
  - 4.  ${\tt H6DU}$  is the bidirectional protection circuit only for SM1, SM2.

AV-H6DU-E1 | Sheet 1/1

FILITSII (	CMOS GATE ARRAY U	NIT CELL SP	FCIFICATIO	N	7.411	/" Version
Cell Name	Function	NII CELE SI	LCIFICATIO	14		Number of BC
	Tri-state Outpu	t and Input	Buffer fo	r SM1 SM2	<del></del>	tumber or bo
H6DD	with Pull Down		Du1,101 10	- J, J		
Cell Symbol	TOTAL TOTAL DOWN		ropagation	Delay Para	meter	
		tu			dn	1
		t0	KCL	t0	KCL	Path
		2.46	0.08	6.47	0.08	OT → X
		(9.26)		(13.27)		
		0	0	0	0	X -> IN
IN ——	<b>≺</b> ∖h					
İ	<u>                                     </u>					
ОТ	<b>X</b>					
	<b>A</b>					
	<b>"</b>					
1						
	С					
		L →	Z	Z	→ L	
		t0	KCL	t0	KCL	7 c → x
		1.60		5.72	0.08	
		(31.75)	*	(12.52)		
1						
		}				
	Input Loading					
Pin Name	Factor (lu)					
OT	2					
С	3	Н →	Z	Z	→ H	]
		t0	KCL.	t0	KCL	
		2.85		3.55	0.08	7
	Output Driving	(31.75)	*	(12.52)		
Pin Name	Factor (lu)					1
						1
					1	1



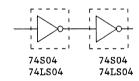


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.
  - 4. H6DU is the bidirectional protection circuit only for SM1, SM2.

AV-H6DD-E1 Sheet 1/1

FUJITSU C	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N		"AV"	Version
Cell Name	Function	ANTONIO DE LA COMPANIO DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL DE CONTROL		· · · · · · · · · · · · · · · · · · ·			mber of BC
	High Power Outpu						_
Cell Symbol		P	ropagation	Delay Para	meter		
		tu		t	dn		
		t0	KCL	t0	KCL		Path
		2.11	0.015	4.04	0.01	8	OT → X
		(3.01)		(5.12)			
						ļ	
						- 1	
1						-	
от —	>—_x					- 1	
					1		
						- 1	
		Parameter			Symbo	1	Typ(ns)*
					1		
					l		
					İ		
	Input Loading	1					
Pin Name	Factor (lu)						:
OT	4	1					
					Ì		
	Output Driving						
Pin Name	Factor (lu)	ļ					
		* Minimum	values for	the typics	1 oners	tine	g condition.
	1			worst case			
				naximum dela			
					·		

TTL Equivalent Circuit



Note: 1. The unit of KCL is ns/pF.

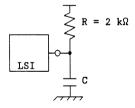
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

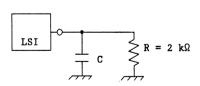
- Output load capacitation of the state of lagrangian and the state of lagrangian and the state of lagrangian and the state of lagrangian and the state of lagrangian and the state of lagrangian and the state of lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangian and lagrangia simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-02L2-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N		AV" Version
Cell Name	Function				i	Number of BC
	High Power Tri-	State Outpu	t Buffer (	True)		
04W2	(04W with 20mA d		_	•		-
Cell Symbol		P	Propagation Delay Parameter			
		tu		t	dn	
		t0	KCL	t0	KCL	Path
		3.09	0.015	6.17	0.021	OT → X
		(4.07)		(7.54)		
OT	>—x					
	V					
1	1					
1	С					
		L →			→ L	
		t0	KCL	t0	KCL	C → X
		5.00		6.10	0.021	
		(18.8)	*	(7.47)		
						}
	Input Loading					
Pin Name	Factor (lu)					
OT	4		L		<u></u>	
C	6	Н →			→ H	
		t0	KCL	t0	KCL	
		6.00		3.30	0.016	
l	Output Driving	(18.8)	*	(7.47)		
Pin Name	Factor (lu)			1		
		ĺ				
						1
	1					





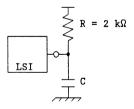
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 20mA,  $T_{\rm A}$  = 0 ~ 70°C, VDD = 5V±5%

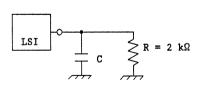
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-04W2-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N .		AV" Version
Cell Name	Function	COLUMN DI	<u> </u>		<del></del>	Number of BC
	High Power Tri-	State Outpu	t and Inpu	t Buffer (T	rue)	
H6W2	(H6W with 20mA d	rive)	-	•	·	-
Cell Symbol		P	ropagation	Delay Para	meter	
		tu		tdn		
		t0	KCL	t0	KCL	Path
		2.06	0.06	3.08	0.08	X → IN
IN ——	x	3.09 (4.37)	0.015	6.17 (7.96)	0.021	OT → X
	C	L →	Z	Z	→ L	
		t0	KCL	t0	KCL	C → X
		5.00		6.10	0.021	
		(22.6)	3%	(7.89)		
Pin Name OT	Input Loading Factor (lu)					
C	6	$H \rightarrow Z$ $Z \rightarrow H$		_		
		t0	KCL	t0	KCL	_
Pin Name IN	Output Driving Factor (£u)	6.00 (22.6)	<b>3</b> %	3.30 (7.89)	0.016	





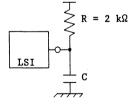
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF. 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 20mA,  $T_{\rm A}$  = 0  $\sim$  70°C, VDD = 5V±5%

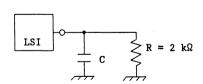
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6W2-E1 | Sheet 1/1

riiiireii (	CMOS GATE ARRAY U	NIT CELL OD	ECTETCATIO	AT .	<del></del>	'AV" Version
Cell Name	Function	NII CELL SP	ECITICALIO:	IN .		Number of BC
Cell Name	High Power Tri-	State Outer	t and Innu	+ Buffor "	+h	Number of BC
H6W1	Pluu Up Resista				LII	_
Cell Symbol	Tidu op Resista				meter	<u> </u>
Cell Dymbol		Propagation Delay Parameter tup tdn			<u>I</u>	
		t0	KCL	t0	KCL	Path
		2.06	0.06	3.08	0.08	X → IN
		_,,,,		0.00		
		3.09	0.015	6.17	0.021	1 OT → X
		(4.37)		(7.96)		
IN	<b>─</b> < h	( )		(,,,,,,		
ОТ	<b>X</b>					
						l
						•
	С					
	-		!	•		
		L →	· Z	Z	→ L	
		t0	KCL	t0	KCL	C → X
		5.00		6.10	0.02	1
		(22.6)	*	(7.89)	i .	Ì
						-
	Input Loading					
Pin Name	Factor (lu)					
TO	4					
С	6	Η →	Z	Z	→ H	
		t0	KCL	t0	KCL	
		6.00		3.30	0.01	6
	Output Driving	(22.6)	*	(7.89)		1
Pin Name	Factor (lu)	i				
IN	36					
1						1
ı						i
		1		l	1	





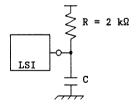
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation
  - 3. The parameters in parentheses are the values applied to the simulation.

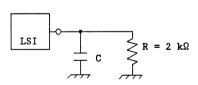
  - 4.  $V_{OL}$  = 0.5V at  $I_{OL}$  = 20mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6W1-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"A\	" Version
Cell Name	Function			<u> </u>		Number of BC
	High Power Tri-	State Outpu	t and Inpu	t Buffer wi	th	
H6W0	Pull Down Resis					_
Cell Symbol		P	ropagation	Delay Para	meter	
		tu	р	tdn		
		t0	KCL	t0	KCL	Path
		2.06	0.06	3.08	0.08	X → IN
IN ——	x	3.09 (4.37)	0.015	6.17 (7.96)	0.021	OT → X
	С	t0 5.00 (22.6)	Z KCL	t0 6.10 (7.89)	→ L   KCL   0.021	C → X
	Input Loading					
Pin Name	Factor (lu)					
OT	4	ļ	L	ļ	<u> </u>	4
С	6	H →	KCL	t0	→ H KCL	4
		6.00	KCL	3.30	0.016	4
Pin Name IN	Output Driving Factor (lu)	(22.6)	*	(7.89)	0.010	





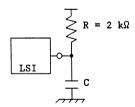
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{OL}$  = 0.5V at  $I_{OL}$  = 20mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%

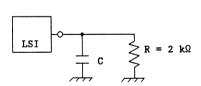
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6W0-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"A	V" Version
Cell Name	Function	***************************************				Number of BC
	Power Tri-State	Output and	CMOS Inte	rface Input	Buffer	
H6E2	(True) (H6E with			-	1	_
Cell Symbol				Delay Para	meter	
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.29	0.08	2.41	0.05	X + IN
		3.09	0.015	6.17	0.021	OT → X
		(4.37)		(7.96)		
IN	<b>─</b> < h	()		(,,,,,		İ
	/ 1					1
от —	x					1
7	6 "					
	Ċ					
	U					
		L →	7	7.	→ L	
		t0	KCL	t0	KCL	d c → x
		5.00	ROL	6.10	0.021	
		(22.6)	*	(7.89)	0.021	
		(22.6)	"	(7.09)		
	Input Loading					
Pin Name	Factor (lu)		:		1	
OT OT	Factor (xu)					
C	6	Н →	7	7	<u>I</u> → H	-
١	0		KCL	t0	KCL	
		6.00	KCT	3.30	0.016	
	Outros Dedectes	3	*	(7.89)	0.018	
Dia Name	Output Driving	(22.6)	^	(/.09)		
Pin Name	Factor (lu)					
IN	36			ļ		
						ļ
				1	1	1
1	İ	į .	1		l	





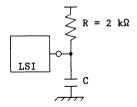
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 20mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%

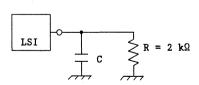
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6E2-E1 | Sheet 1/1

FULLTSU (	MOS GATE ARRAY U	NIT CELL SP	ECTETCATIO	N	Ι "Δ\	" Version
Cell Name	Function	VIII ODDD DI	BOIL TOWLLO			lumber of BC
	High Power Tri-	State Outpu	t and CMOS	Interface		
H6E1	Buffer w/ Pull					_
Cell Symbol				Delay Para		
		tu		tdn		
		t0	KCL	t0	KCL	Path
		2.29	0.08	2.41	0.05	X → IN
IN		3.09 (4.37)	0.015	6.17 (7.96)	0.021	OT → X
ОТ ——	C					
		L →			→ L	
		t0	KCL	t0	KCL	C → X
		5.00 (22.6)	ric	6.10 (7.89)	0.021	
Pin Name	Input Loading Factor (lu)					
OT	4		<u> </u>		 → H	-
С	6	H →	KCL		→ H   KCL	4
		t0 6.00	KCT	3.30	0.016	1
Pin Name	Output Driving Factor (lu)	(22.6)	*	(7.89)	0.016	
IN	36					
		,				





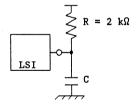
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 20mA,  $T_{\rm A}$  = 0 ~ 70°C, VDD = 5V±5%

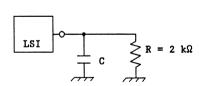
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6E1-E1 | Sheet 1/1

FUJITSU C	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N		AV" Version
	Function	0222 01.			i	Number of BC
	High Power Tri-S	tate Output	and CMOS	Interface I	nput	
H6E0	Buffer w/ Pull D					-
Cell Symbol				Delay Para		
		tu			dn	
	:	t0	KCL	t0	KCL	Path
		2.29	0.08	2.41	0.05	X → IN
IN		3.09 (4.37)	0.015	6.17 (7.96)	0.021	OT → X
от ——	C					
		L →			→ L	J
		t0	KCL	t0	KCL	C → X
		5.00 (22.6)	*	6.10 (7.89)	0.021	
	1-2					
Pin Name	Input Loading Factor (lu)					
OT	Factor (xu)					
C	6	Н →	7.	7.	→ H	
		t0	KCL	t0	KCL	
		6.00		3.30	0.016	
	Output Driving	(22.6)	*	(7.89)		
Pin Name	Factor (lu)					
IN	36				1	
					1	





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

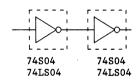
  - 4.  $V_{OL}$  = 0.5V at  $I_{OL}$  = 20mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AVB series only.

AV-H6E0-E1 | Sheet 1/1

Cell Name Function Number	C DC
	ot RC
02B2 Power Output Buffer(True) (02B with 10mA drive)	_
Cell Symbol Propagation Delay Parameter	
tup tdn	
	Path
	→ X
(3.20) (4.80)	
-	
OT — X	
Parameter Symbol Ty	o(ns)*
Input Loading	
Pin Name Factor (lu)	
OT 4	
Output Driving	
Pin Name Factor (lu)	
* Minimum values for the typical operating con	
The values for the worst case operating cond	lition
are given by the maximum delay multiplier.	

## TTL Equivalent Circuit



Note: 1. The unit of KCL is ns/pF.

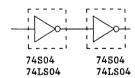
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{OL}$  = 0.5V at  $I_{OL}$  = 10mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%
- 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-02B2-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	-   "	AV" Version
Cell Name	Function					Number of BC
O2B3	High Power Outp	ut Buffer(T	rue) (02B	with 15mA	drive)	· <b>-</b>
Cell Symbol		P	ropagation	Delay Para		
		tu			dn	
		t0	KCL	t0	KCL	Path
		1.39	0.020	2.59	0.023	OT → X
		(2.59)		(3.97)		
!						
от —	x					
01	_ ^					
'						
		Parameter			Symbo1	Typ(ns)*
	Input Loading					
Pin Name	Factor (lu)					
OT	6					
	Output Driving				1	
Pin Name	Factor (lu)					
- 411 114m0	123001 (24)				<u> </u>	
		* Minimum	values for	the typica	l operat	ing condition.
						ng condition
				aximum dela		

TTL Equivalent Circuit



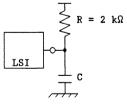
Note: 1. The unit of KCL is ns/pF.

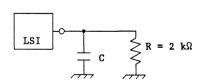
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{OL}$  = 0.5V at  $I_{OL}$  = 15mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%
- 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-02B3-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	/A"	" Version
Cell Name	Function					Number of BC
	Power Tri-State	Output Buf	fer (True)			
04T2	(04T with 10mA d		• •		1	_
Cell Symbol			ropagation	Delay Para	meter	
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.03	0.030	4.48	0.034	OT → X
		(3.98)		(6.69)		
		(		( )		1
						ļ
	$\wedge$					
ОТ ——	x					
	\( \text{"} \)					
	C			l		
	U			1	İ	
		L →	. 7	7	→ L	
		t0	KCL	t0	KCL	d c → x
		3.00	KCL	4.41	0.034	-
		(16.00)	*	(6.62)	0.054	
		(16.00)	,	(0.02)	1	
			1	1	j	
	Tame Tanding				l	1
D:- N	Input Loading		i	ļ		
Pin Name OT	Factor (lu)				1	ļ
			<u> </u>		l → H	4
С	6	H →				4
	1	t0	KCL	t0	KCL	4
	<del> </del>	3.50		2.57	0.030	
Dia Man	Output Driving	(16.00)	*	(6.62)	l	
Pin Name	Factor (lu)		1	1	1	
				1	İ	
					}	
					1	
		l	L	I	1	1





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

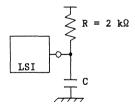
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation

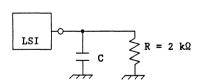
- 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 10mA,  $T_{\rm A}$  = 0 ~ 70°C, VDD = 5V±5% 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-04T2-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CELL SE	PECIFICATIO	N		'AV" Version
Cell Name	Function	·				Number of BC
	High Power Tri-		ıt Buffer(T	rue)		
04T3	(04T with 15mA d	rive)				-
Cell Symbol				Delay Para		
		tı			dn	
		t0	KCL	t0	KCL	Path
		2.01 (3.31)	0.020	4.16 (5.72)	0.024	OT → X
ОТ ——	x c			·		
		Τ, -	<u> </u>	Z	→ L	
		t0	KCL	t0	KCL	c → x
		3.50		4.33	0.023	3
		(16.8)	*	(5.83)		
***************************************	Input Loading				l	
Pin Name	Factor (lu)					
OT	6			İ		
C	9	Н -	→ Z	Z	→ H	
		t0	KCL	t0	KCL	
		4.46	T	2.52	0.02	
	Output Driving	(16.8)	*	(5.83)	1	
Pin Name	Factor (lu)		1	' '		
				1		
				l		
				1		
	1		1			





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

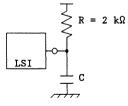
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

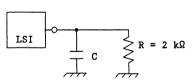
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation
- 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 15mA,  $T_{\rm A}$  = 0 ~ 70°C, VDD = 5V±5%
- 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-04T3-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	7A"	" Version
Cell Name	Function Number of B					
	Power Tri-State	Output and	Input Buf	fer(True)		
н6Т2	(H6T with 10mA d		Impac bar	101 (1140)		_
Cell Symbol	(1101 11011 101111 0		ropagation	Delay Para	meter	
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.06	0.06	3.08	0.08	X + IN
1		2.03	0.030	4.48	0.034	OT → X
	1	(4.58)		(7.37)		
IN	<b>─</b> < h	( )		(,,,,,		
	7					
от ——	x					
"	6 "					
ł						
	Ċ					
	· ·					ļ i
		L →	7.	7.	 → L	<u> </u>
		t0	KCL	t0	KCL	c → x
		3.00	NOL .	4.41	0.034	
		(20.00)	*	(7.30)	"""	
		(20.00)		(7.50)		
					1	
	Input Loading					
Pin Name	Factor (lu)					
OT	4				1	
C	6	Н →	7	7	<u> </u>	-
٠ .	"	t0	KCL	t0	KCL	-
1	1	3.50	VCT	2.57	0.030	-
L	Output Driving	(20.00)	*	(7.30)	0.030	
Pin Name	Factor (lu)	(20.00)	"	(7.30)	1	
IN	36					
IN	36					
			l		1	
1	1		l .	i	I	1



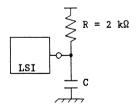


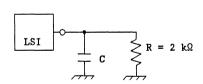
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.
  - 4.  $V_{OL} = 0.5V$  at  $I_{OL} = 10$ mA,  $T_A = 0 \sim 70$ °C,  $VDD = 5V \pm 5\%$
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-H6T2-E1 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "AV" V						AV" Version
Cell Name		Function Number of BC				
	High Power Tri-		t and Inpu	t Buffer(Tr	ue)	
Н6Т3	(H6T with 15mA d					
Cell Symbol				Delay Para		
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.06	0.06	3.08	0.08	X → IN
		0.01			0 00/	om . v
	1	2.01	0.020	4.16	0.024	• OT → X
IN	<b>─</b> < h	(3.71)		(6.20)	İ	
	7			l		
ОТ	X				ĺ	
01	^					
	Y					
				•	l	
	Ċ				I	
	· ·					
		L →	Z	Z	→ L	
		t0	KCL	t0	KCL	C → X
		3.50		4.33	0.023	3
		(20.9)	*	(6.29)	1	
				1		
	Input Loading				l	
Pin Name	Factor (lu)			1		
OT	6					
C	9	H →		Z	<b>→</b> H	
		t0	KCL	t0	KCL	
		4.46		2.52	0.020	)
	Output Driving	(20.9)	*	(6.29)	1	
Pin Name	Factor (lu)					
IN	36				1	
1	1	I	I	1	1	I '
1	ì	1		ļ	1	l l





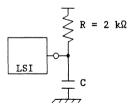
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 15mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%

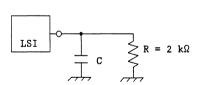
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-H6T3-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N		AV" Version
Cell Name	Function Number of BC					
	Power Tri-State	Output and	CMOS Inte	rface Input	Buffer	
H6C2		h 10mA driv				-
Cell Symbol		P	ropagation	Delay Para	meter	
		tu			dn	
		t0	KCL	t0	KCL	Path
		2.29	0.08	2.41	0.05	X → IN
IN	x	2.03 (4.58)	0.030	4.48 (7.37)	0.034	OT → X
	С	L → t0 3.00 (20.00)	Z KCL *	t0 4.41 (7.30)	→ L   KCL   0.034	_ c → x
	Input Loading					
Pin Name	Factor (lu)					
OT C	4	Н →	<u> </u>	7	<u>I</u> → H	
	6	t0 H →	KCL	t0	→ H KCL	-
		3.50	KCL	2.57	0.030	-
Pin Name IN	Output Driving Factor (£u) 36	(20.00)	*	(7.30)	0.030	
				<u> </u>	l	





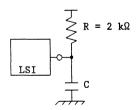
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 10mA,  $T_A$  = 0 ~ 70°C, VDD = 5V±5%

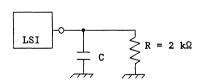
  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

This cell is available for AV & AVM series only.

AV-H6C2-E1 | Sheet 1/1

FUJITSU C	MOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	"AV	" Version
Cell Name	Function					Number of BC
	High Power Tri-	State Outpu	t and CMOS	Interface	Input	
H6C3		H6C with 15			-	_
Cell Symbol		P	ropagation	Delay Para	meter	
		tu			dn	I
		t0	KCL	. t0	KCL	Path
		2.29	0.08	2.41	0.05	X → IN
		2.01	0.020	4.16	0.024	OT → X
IN		(3.71)		(6.20)		
IN						
	_ 1					
OT —	<b>X</b>					
	$\checkmark$					
	C					1
		L →	Z	Z	→ L	
		t0	KCL	t0	KCL	c→x
	'	3.50		4.33	0.023	
		(20.7)	*	(6.29)	}	Ì
		, ,		, ,	•	
	Input Loading				[	Į.
Pin Name	Factor (lu)				l	1
ОТ	4					
С	6	H →	· Z	Z	→ H	
		t0	KCL	t0	KCL	1
		4.46		2.52	0.020	1
	Output Driving	(20.9)	*	(6.29)		ļ
Pin Name	Factor (lu)	,			i	
IN	36					1
					1	1
				1		
		1			1	1





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation. 4.  $V_{\rm OL}$  = 0.5V at  $I_{\rm OL}$  = 15mA,  $T_{\rm A}$  = 0 ~ 70°C, VDD = 5V±5%

  - 5. Pin numbers to which this buffer can be tied are predetermined for each package and device type. In using this buffer, rules regarding simultaneously switching outputs should be strictly observed.

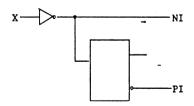
This cell is available for AV & AVM series only.

AV-H6C3-E1 | Sheet 1/1

FILITTSII	CMOS CATE ADDAY I	NIT CELL CE	PCIPICATIO	N.	n	AV" Version
Cell Name	CMOS GATE ARRAY UNIT CELL SPECIFICATION "AV" Version Function Number of BC					
	Crystal Oscillator					
15C	CMOS Interface I		with Schm	itt Trigger		0
Cell Symbol				Delay Para		
		tu			dn	
		t0	KCL	t0	KCL	Path
		84.18	0.12	72.39	0.05	X → PI *1
		1.00	1.123	0.91	0.990	X → NI *2
1						
İ			1			i
		İ	ł		l	
İ			1			1
			1		İ	
	<b></b>		•			
x	NI NI				İ	İ
	PI	İ	j			ı
		1				
		i		İ		
		Parameter	·		Symbol	Typ(ns)*
1						
					ļ	ŀ
	Input Loading				ļ.	
Pin Name	Factor (lu)	1				
l		į			l	
i					l	
		]				
	Out-out Daile	<b>{</b>				
Pin Name	Output Driving					
PIN Name PI	Factor (lu)	ł				
F 1	10 14				L	
		* Minimum	values for	the twnice	1 operst	ing condition.
1						ng condition.
	1			aximum dela		
	1				., muzuip	

Equivalent circuit

Crystal Oscillator Amp



Schmitt trigger

I5C cell should be used with OT1.

I5C is designed for low frequency ocillation.

## Note:

\*1 The unit of K<sub>CL</sub> is ns/pF.
\*2 Output load capacitance of 60pF is used for Fujitsu's logic simulation.

AV-I5C-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL SP	ECIFICATIO	N	'A"	/" Version
Cell Name	Function				1	Number of BC
OT1	Output Buffer wi	th Protecti	on Circuit	Only		0
Cell Symbol		P	ropagation	Delay Para	meter	
		tu	P		dn	
		t0	KCL	t0	KCL	Path OT → X
	ř.	0	0	0	0	OT → X
						ľ
1						
от	<b>&gt;</b> −x					ł
01	<b>/</b>					İ
					ŀ	
				l		
	•	Parameter			Symbol	Typ(ns)*
					į	
					1	
						}
						İ
					l	
					[	1
					]	
	T				1	
<b>5.</b>	Input Loading				1	
Pin Name	Factor (lu)				1	]
OT	0				1	
					l	
					1	
		1				
	0-44 D-//				1	
D	Output Driving	ļ		•		
Pin Name	Factor (lu)	l			l	1
		<b> </b>			L	1
	1	# M4=4=	1 f	. +ha +	1	na aanditi-
		The wal-	values ion	the typica	operati	ng condition.
		THE VAID	es for the	worst case maximum dela	operating	e condition
Note:		are give	n by the n	JAXIMUM GETA	y multipl	161.
HOLE :						
OT1 cell s	hould be used wit	h TSC				
OII CEII B	"oute he aben Ali	150.				
1						
1						
1						
AV-OT1-E1	Sheet 1/1					
	1 2					

## RAM Family for C-2301AVM

Page	Unit Cell Name	Function
3-273	R51	32w x 32b Single Port Static RAM
3-274	R51A	32w x 28b plus 32w x 4b Single Port Static RAM
3-275	R51B	32w x 24b plus 32w x 8b Single Port Static RAM
3-276	R51C	32w x 20b plus 32w x 12b Single Port Static RAM
3-277	R51D	32w x 16b plus 32w x 16b Single Port Static RAM
3-278	R61	64w x 16b Single Port Static RAM
3-279	R61A	64w x 12b plus 6w x 4b Single Port Static RAM
3-280	R61B	64w x 8b plus 64w x 8b Single Port Static RAM
3-281	R71	128w x 8b Single Port Static RAM
3-282	R71A	128w x 4b plus 128w x 4b Single Port Static RAM
3-283	R83	256w x 4b Single Port Static RAM
3-284	R83A	256w x 2b plus 256w x 2b Single Port Static RAM

## RAM Family for C1502AVM/C4002AVM

Page	Unit Cell Name	Function
3-285	R610	64w x 36b Single Port Static RAM
3-286	R611	64w x 20b plus 64w x 16b Single Port Static RAM
3-287	R711	128w x 18b Single Port Static RAM
3-288	R712	128w x 9b plus 128w x 9b Single Port Static RAM
3-289	R87	256w x 9b Single Port Static RAM

FUJITSU (	CMOS GATE ARRAY C	ELL SPECIFICA	TION			"AVM	" Version
	Function						
R51	32w x 32b Single	Port Static	RAM				
RAM Symbol		Pro	pagation	Delay Pa	rame	ter	
		tup			tdn		
		t0	KCL	t0		KCL	Path
		9	0.12	21		0.07	CK to D
I	оо доо — ∷		0.12		- 1	0.07	OK CO D
10	01 D01						
	02 D02						1
	03 D03						
:: — т	28 D28				-		
	29 D29						
I:	30 D30 — ∷						
:: - I:	31 D31 ├─ ∷				- 1		
- A	o   👯				- 1		
A: - A:							
:: — A:		Parameter	****	L		Symbol	Typ(ns)*
A A		Clock Pulse	Width (H		tCWH	25	
	11	Clock Pulse				tCWL	20
::	E   ;;	Clock Pulse		ow)		tCWM	5000
: - cı	к 🗎 🗒	Address Setu Address Hold				tSA tHA	5
:: — <sub>T</sub>	1 то⊢∷	Data Output		ie.	-+	tHD0	5
T.	1 ' '	Input Data S				tSDI	20
T: - T		Input Data H	old Time			tHDI	10
:: - <u>T</u> .		WE Setup Tim				tSEH	3
	1 ''	WE Hold Time		** * * * * * * * * * * * * * * * * * *		tHEH	3
	C1 ::	WE Setup Tim				tSEL	5
:: L	::	WB HOTO TIME	(IIIIII)	tion node	-	СППП	-
		* Minimum va	lues (or	mavimum	wa lu	e for tC	WM) for
		typical op				c 101 <b>c</b> 0	WII) 101
			Input L	oadino			
		Pin Name	Factor				
		700		,			
		I00 ~ I31 A0 ~ A4		lu lu			1
		WE ~ A4		lu			
		CK		lu			
				Driving			
::::::		Pin Name	Factor	(lu)			
		D00 ~ D31	36	lu			
N-4		<u> </u>	L	l			
Note:	: Data Inputs	D00 -	D31	· Dota	. Ou+	nute	
	: Address Inputs	D00 - T1, T2	, TI, TA	: Data			
1 .	: Write Enable		1, TC2	': Inpu	ıts f	or RAM T	est
ł	: Clock	TO			out f	or RAM T	est
7.51	<u> </u>	** A0	: LSB, A	4 : MSB			·
R51	Sheet 1/1			C_0.	201 477	M_D51(22	11 A 33F) E3
		3-273		C-23	συΑν	m-к51(32	w x 32b)-E3

	CMOS GATE ARRAY C	ELL SPECIFICA	TION			"AVM	" Version
RAM Name	Function						
R51A	32w x 28b + 32w	x 4b Single H	Port Stat	ic RAM			•
RAM Symbol			pagation	Delay Pa		ter	
		tup	TIOT		tdn	TOT	
		t0	KCL	t0		KCL	Path
			0.10	.,	1	0.07	OV to D
l :: r		9	0.12	21	- 1	0.07	CK to D
:: -  I	100 D00 ::						
	[01 D01   ::						
	[02 D02 ::						
:: 7	[03 D03 ::						
					İ		
	[26 D26						1
] :: 7	[27 D27						
::- I	128 D28 -				- 1		
:: <del>-  </del> 1	[29 D29 — : :			İ			
::- I	[30 D30 - ::			ļ	- 1		
∷ ─ 1	[31 D31 ::						
::	٠٠ ::	Parameter				Symbol	Typ(ns)*
	11 ::	Clock Pulse				tCWH	25
	12	Clock Pulse				tCWL	20
1 1	13	Clock Pulse		ow)		tCWM	5000
1 '' 1	14	Address Setu	ip Time			tSA	5
l II.		Address Hold				tHA	5
	30	Data Output				tHD0	5
	31	Input Data S Input Data B				tSDI tHDI	10
1 '' 1	33	WE Setup Tir				tSEH	3
	34	WE Setup in				tHEH	3
;;		WE Setup Tin		ition Mod	de)	tSEL	5
:: - W	VE1 ::	WE Hold Time				tHEL	5
· · · · · · · · · · · · · · · · · · ·	VE2		. (				
	1 ::						
!!	CK1						
	CK2	* Minimum va	alues (or	maximum	value	e for tC	WM) for
1 :: -	гі то	typical o	peration	condition	n.		
	r2 ::						
	TI <b>R51A</b>		Input L				
	ra ASIZ	Pin Name	Factor				
	rw ::	100 ~ 131		lu			
1 '' 1	rcı	A0 ~ A4		lu			
1	TC2	BO ~ B4		lu l			
		WE1, WE2	1	lu			
1		CK1, CK2		lu Driving			
		Pin Name	Factor				
		I III Name	Factor	(*4)			
		D00 ~ D31	36	lu			
Note:							
1	: Data Inputs	D00 -	D31	: Data	a Out	puts	
A0 - A4	· · · · · · · · · · · · · · · · · · ·		2, TI, TA		-	or RAM T	'est
BO - B4	: Address Inputs	TW, T	C1, TC2	. mp	ulo I	OI WALL I	COL
WE1, WE2	: Write Enable	TO			put f	or RAM T	est ,
CK1, CK2	: Clock		, BO : LS				
R51A	Sheet 1/1	A4	, B4 : MS				<u> </u>
		3-274	C-2301A	AVM-R51A(	32w x	28b + 3	$32w \times 4b)-E2$

FUJITSU CMOS GATE ARRAY (	CELL SPECIFICA	TION		"AVM"	Version
RAM Name Function				· · · · · · · · · · · · · · · · · · ·	
R51B 32w x 24b + 32w	x 8b Single F	ort Stati	c RAM		
RAM Symbol	Pro	pagation	Delay Para	meter	
	tup			dn	
	t0	KCL	t0	KCL	Path
	1			į	
	9	0.12	21	0.07	CK to D
11   11	i i	1			
:: - 100 D00	1			į	
:: 101 DO1		i		i	
102 D02	1	-		- 1	
103 D03		1			
Too Doo	1	1		Ì	
122 D22	1	1			
123 D23	]	1		į.	i
:: — 124 D24 — ::	1	1		i	
:: <u>  12</u> 5 D25  ::					
	1			ŀ	
::	Parameter			Symbol	Typ(ns)
:: - I31 D31 - ::	Clock Pulse	Width (Hi	oh)	tCWH	25
:: — AO ::	Clock Pulse			tCWL	20
11 A1	Clock Pulse			tCWM	5000
1 - A2	Address Setu		<del>"</del>	tSA	5
	Address Hold			tHA	5
A4 ::	Data Output			tHD0	5
	Input Data S			tSDI	20
:: B0	Input Data H	lold Time		tHDI	10
B1	WE Setup Tin			tSEH	3
B2 B3	WE Hold Time	)		tHEH	3
∷ — B3 B4 ::	WE Setup Tim	e (Inhibi	tion Mode)	tSEL	5
::   D4   ::	WE Hold Time	(Inhibit	ion Mode)	tHEL	5
:: — WE1 ::					
∷ — <sub>WE2</sub>					
:: CK1 ::	* Minimum va			lue for tCV	√M) for
:: — CK2	typical or	eration c	ondition.		
::   T1 T0   ::		Input Lo			
T2	Pin Name	Factor (			
TI R51B	100 ~ 131	1 &	-		
TA I	A0 ~ A4	1 2	1		
TW TC1	BO ~ B4 WE1, WE2	1 1 1 1 1 1	1		
TC2	CK1, CK2	1 2	-		
1102	CKI, CKZ	Output D			
	l .				
	Pin Name	Factor (	0.11)		
	Pin Name	Factor (	lu)		
	Pin Name	Factor (	Lu)		
	Pin Name D00 ~ D31	Factor (			
Note:					
Note: 100 - 131 : Data Inputs		36 <b>£</b>		utputs	
IOO - I31 : Data Inputs	D00 ~ D31	36 <b>£</b>	u : Data O	•	
I00 - I31 : Data Inputs	D00 ~ D31	36 &	u : Data O	utputs for RAM Te	est
A0 - A4 . Address Inputs	D00 ~ D31	36 &	u : Data O : Inputs	•	
IOO - I31 : Data Inputs AO - A4 BO - B4 : Address Inputs	D00 ~ D31  D00 - T1, T2 TW, T0	36 &	u : Data O : Inputs : Output	for RAM Te	

	GATE ARRAY C	ELL SPECIFICA	TION		"AVM"	Version
RAM Name Fun	ction					
R51C 32w	$x \times 20b + 32w$	x 12b Single	Port Stat	ic RAM		
RAM Symbol			pagation	Delay Param		
		tup	WOT.	to		D. 41
		t0	KCL	t0	KCL	Path
		9	0.12	21	0.07	CK to D
		'	0.12	21	0.07	CK to B
100 D	000			ĺ		
:: - IO1 D	001 ::		l	ŀ		1
:: T102 D	1 ' '		1			
:: 103 D	003		1	l		
- I18 D	118				ľ	
110 D					ļ	
	- :			1		
120 D	1 ''					
		]	]		Ì	}
130 D	30 —	<u> </u>			1 6-1-1	m ( )
131 D	)31	Parameter Clock Pulse	Width (Wi	ah)	Symbol tCWH	Typ(ns)
:: — A0	::	Clock Pulse	tCWL	20		
— A1		Clock Pulse			tCWM	5000
A2		Address Setu			tSA	5
A3	::	Address Hold			tHA	5
:: A4		Data Output	Hold Time		tHD0	5
ВО		Input Data S			tHDI	20
:: — B1	1::	Input Data F			tSEH	10
:: — B2	::	WE Hold Time			tHEH.	3
B3 B4		WE Setup Tin		tion Mode)	tSEL	5
.: D4	::	WE Hold Time	(Inhibit	ion Mode)	tHEL	5
WE1	::					
WE2						
		II.				
·· CK1		* Minimum va	ilues (or	maximum val	ue for tCV	M) for
CK1		* Minimum va			lue for tCV	√M) for
CK1		* Minimum va	peration c	ondition.	lue for tCV	WM) for
— СК2 — Т1	то	typical or	eration c	ondition.	lue for tCV	WM) for
CK2 — T1 — T2		typical op	Input Lo	ondition. ading	lue for tCV	VM) for
CK2 T1 T2 T1 R5		Pin Name	Input Lo Factor (	ondition.  ading lu) u	lue for tCV	VM) for
CK2  T1  T2  TI R5		Pin Name 100 ~ 131 A0 ~ A4	Input Lo Factor (	ading lu)	lue for tCV	VM) for
— CK2 — T1 — T2 — T1 R5 — TA — TW		Pin Name 100 ~ 131 A0 ~ A4 B0 ~ B4	Input Lo Factor ( 1 & 1 & 1 &	ading lu) u u	lue for tCV	VM) for
— CK2 — T1 — T2 — T1 R5 — TA		Pin Name 100 ~ 131 A0 ~ A4	Input Lo Factor (	ondition.  ading lu)  u u u	lue for tCV	VM) for
— CK2 — T1 — T2 — T1 R5 — TA — TW — TC1		Pin Name 100 ~ I31 A0 ~ A4 B0 ~ B4 WE1, WE2	Input Lo Factor ( 1	ading lu) u u u u u riving	lue for tCV	MM) for
— CK2 — T1 — T2 — T1 R5 — TA — TW — TC1		Pin Name 100 ~ I31 A0 ~ A4 B0 ~ B4 WE1, WE2	Input Lo Factor ( 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ading lu) u u u u u riving	lue for tCV	MM) for
	510	Pin Name 100 ~ 131 A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	Input Lo Factor ( 1	ading lu) u u u u u riving	lue for tCV	MM) for
— CK2 — T1 — T2 — T1 R5 — TA — TW — TC1	510	Pin Name 100 ~ I31 A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name	Input Lo Factor (  1 l 1 l 1 l 1 l Output D Factor (	ading lu) u u u u riving lu)	lue for tCV	M) for
	510	Pin Name 100 ~ 131 A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	Input Lo Factor ( 1	ading lu) u u u u riving lu)	lue for tCV	M) for
	510	Pin Name 100 ~ I31 A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name	Input Lo Factor (  1 l 1 l 1 l 1 l Output D Factor (	ading lu) u u u u riving lu)	lue for tCV	M) for
CK2 - T1 - T2 - T1 R5 - TA - TW - TC1 - TC2	510	Pin Name  100 ~ 131  A0 ~ A4  B0 ~ B4  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D31	Input Lo Factor (  1	ading lu) u u u u u uriving lu)		M) for
CK2 - T1 - T2 - T1 R5 - TA - TW - TC1 - TC2	510	Pin Name  100 ~ 131  A0 ~ A4  B0 ~ B4  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D31	Input Lo Factor (  1	ondition.  ading lu) u u u u uriving lu) u		M) for
CK2 - T1 - T2 - T1 R5 - TA - TW - TC1 - TC2 - TC2	510	Pin Name  100 ~ I31 A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name  D00 ~ D31	Input Lo Factor (  1	ondition.  ading lu)  u u u riving lu)		
CK2 - T1 - T2 - T1 R5 - TA - TW - TC1 - TC2  Note: 100 - 131 : Da A0 - A4 B0 - B4 : Ad	ata Inputs	Pin Name  100 ~ I31  A0 ~ A4  B0 ~ B4  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D31	Input Lo Factor (  1	ondition.  adding lu) u u u riving lu) u : Data On	itputs for RAM Te	est
CK2  T1  T2  TA  TM  TC1  TC2  Note:  100 - I31 : Da  A0 - A4  B0 - B4  WE1, WE2 : Wr	ata Inputs ddress Inputs	Pin Name  100 ~ I31  A0 ~ A4  B0 ~ B4  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D31	Input Lo Factor (  1 k 1 k 1 k 1 k 1 k 2 K 36 k  D31 2, TI, TA, 21, TC2	ondition.  ading lu) u u u riving lu) u : Data On : Inputs : Output	ıtputs	est
CK2  T1  T2  T1	ata Inputs ddress Inputs	Pin Name  100 ~ I31  A0 ~ A4  B0 ~ B4  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D31  D00 - T1, T2  TW, T0  ** A0	Input Lo Factor (  1	ondition.  ading lu) u u u riving lu) u : Data On : Inputs : Output	itputs for RAM Te	est

	OS GATE ARRAY (	CELL SPECIFICA	ATION		"AVM"	Version
	ınction					
	2w x 16b + 32w					
RAM Symbol			pagation Dela			T
		tup t0	KCL	t0 td	n KCL	Path
			ROB	-	- KOL	Tach
		9	0.12	21	0.07	CK to D
700	P00					
	D00 - : :					
	D02					
103	D03					}
	D14				,	j
	D14					
. –	::					
	D16 D17					
	D30 ::	Parameter			Symbol	Typ(ns)
131	D31 - :	Clock Pulse	Width (High)	tCWH	25	
:: A0	::	Clock Pulse		tCWL	20	
A1 A2		Clock Pulse Address Setu			tCWM tSA	5000
A3		Address Hold			tHA	5
A4		Data Output	Hold Time		tHD0	5
∷ — во	::	Input Data S			tSDI	20
В1		Input Data I	dold Time		tHDI tSEH	10
:: — B2	::	WE Hold Time	2		tHEH	3
B3 B4		WE Setup Tim	ne (Inhibition	n Mode)	tSEL	5
	::	WE Hold Time	(Inhibition	Mode)	tHEL	5
WE1						
WE2					·····	
CK1			alues (or maxi		ue for tCV	WM) for
CK2		typical or	peration condi	tion.		
T1	то		Input Loadir	10		
T2	10	Pin Name	Factor (lu)	•		
— √тт ;						
	R51D	I00 ~ I31	1 Lu			
TA	R51D	A0 ~ A4	1 lu			
TA TW	R51D	A0 ~ A4 B0 ~ B4	1 lu 1 lu			
TA	R51D ::	A0 ~ A4	1 lu			
TA TW TC1	R51D	A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 Lu 1 Lu 1 Lu 1 Lu Output Drive	ing		
TA TW TC1	R51D	A0 ~ A4 B0 ~ B4 WE1, WE2	1 Lu 1 Lu 1 Lu 1 Lu	ing		
TA TW TC1 TC2		A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 Lu 1 Lu 1 Lu 1 Lu Output Drive	ng		
TA TW TC1		A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 Lu 1 Lu 1 Lu 1 Lu Output Drive	ng		
TA TW TC1 TC2		A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 lu ivi	ing		
TA TW TC1 TC2		A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 lu ivi	ing		
TA TW TC1 TC2		A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2	1 lu 1 lu 1 lu 1 lu 1 lu 1 lu 6 lu 1 lu 6 lu 6 lu 7 sactor (lu)	ing Data Ou	tputs	
Note: 100 - I31 : I A0 - A4	Data Inputs	A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name D00 ~ D31	1 &u 1 &u 1 &u 1 &u 1 &u 1 &u 2 &u 1 &u 3 &u 1 &u 2 &u 1 &u 1 &u 2 &u 1 &u 1 &u 1 &u 1 &u 1 &u 1 &u 1 &u 1	Data Ou	<del>-</del>	
Note: 100 - I31 : I A0 - A4 B0 - B4	Data Inputs Address Inputs	A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name D00 ~ D31	1 lu 1 lu 1 lu 1 lu 1 lu 36 lu  D31 : 7, TI, TA, :	Data Ou Inputs	for RAM Te	
Note: 100 - I31 : I A0 - A4 B0 - B4 WE1, WE2 : V	Data Inputs Address Inputs Write Enable	A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name D00 ~ D31	1 lu 1 lu 1 lu 1 lu 1 lu 1 lu 36 lu  D31 : 2, TI, TA, : 11, TC2 :	Data Ou Inputs	<del>-</del>	
Note: 100 - 131 : 1 A0 - A4 B0 - B4 WE1, WE2 : WE1, CK2 : 0	Data Inputs Address Inputs	A0 ~ A4 B0 ~ B4 WE1, WE2 CK1, CK2 Pin Name D00 ~ D31 D00 - T1, T2 TW, T0 ** A0	1 lu 1 lu 1 lu 1 lu 1 lu 36 lu  D31 : 7, TI, TA, :	Data Ou Inputs	for RAM Te	

FUJITSU	CMOS GATE A	RRAY C	ELL SPECIFIC	ATION			l "AVM	" Version
RAM Name	Function		<u> </u>					, or or or or or or or or or or or or or
R61	64w x 16b	Single	Port Static	RAM				
RAM Symbol			Pr	opagation	Delay Pa	rame	eter	
			tur			tdr		
			t0	KCL	t0		KCL	Path
								GT . D
:: [			9	0.12	21		0.07	CK to D
	00 D00 ::							
	01 D01				ĺ			
	02 D02							
	03 D03							
	05 D05							
	06 D06							1
	07 D07							
	08 D08							
	09 D09 -					1		1
	10 D10				1			1
	11 D11		Parameter		L	一丁	Symbol	Typ(ns)*
	12 D12		Clock Pulse	Width (H	ligh)		tCWH	25
	14 D14 - ::		Clock Pulse				tCWL	20
	15 D15		Clock Pulse		ow)		tCWM	5000
			Address Set				tSA	5
l ∷∃A	1		Address Hol Data Output				tHA	5
:: -  A	, ,		Input Data			-	tHD0 tSDI	20
	3 ::		Input Data				tHDI	10
:: — A	1		WE Setup Ti				tSEH	3
A A	5		WE Hold Tin				tHEH	3
:: w	· ::		WE Setup Ti				tSEL	5
			WE Hold Tin	e (Inhibi	tion Mode	∍)	tHEL	5
:: ¬c	К ::							
::- T	1 TO :							
	2 ::		* Minimum v	alues (or	maximum	valı	ue for C	WM) for
	I <i>R61</i>			peration				,
	W ::							
	Č1			Input I	- 1			
	rc2		Pin Name	Factor	(lu)			
:: L	::		I00 ~ I15	1	Lu			
			A0 ~ A5	_	lu			
::::::			WE AS	1	lu			
			CK	-	lu			
					Driving			
::::::			Pin Name	Factor	(lu)			
: : : : : :								
			D00 - D15	20	0			
			D00 ~ D15	36	lu			
Note:								***************************************
	: Data Inpu	ts	D00 -	D15	: Data	a Ou	tputs	
A0 - A5	: Address I			2, TI, TA	4,Tnn	uts	for RAM T	est
WE	: Write Ena	ble		C1, TC2	_			
CK	: Clock		TO	. TOD :		put	for RAM T	est
R61	Sheet 1/1	1	жж Д(	) : LSB, A	ro : Mar			ſ
1.01	1 Direct 1/1	L	3-27		C-2	301 A	VM_D61(6/	w x 16b)-E3

	MOS GATE ARRAY ( Function	CELL SPECIFIC	ATION		"AVM"	Version
	64w x 12b + 64w	x 4b Single	Port Stat	ic RAM		
AM Symbol		Pr	opagation	Delay Para	neter	
		tup			in	T
		t0	KCL	t0	KCL	Path
	<del></del>					
∷ — то	о роо⊢∷	9	0.12	21	0.07	CK to D
, , ,	1 D01	1 1	***			
	2 D02 - ::	1				
	3 D03	1				
	4 D04	1				
	5 DO5	1				
	6 D06 - ::	1 1		1	į	
	7 D07 - ::	1 1			,	ľ
	8 D08 -:	1				ł
	9 D09 - ::					
	0 D10					1
	1				į	
∷⊢∺	1_D11	1			ł	
;; - I1	2 D12 ::	<u> </u>				70 ()
: - I1	3 D13	Parameter	11/ 1+1 /11	1.1.	Symbol	Typ(ns)
111	4 D14	Clock Pulse			tCWH	25
	5 D15 - ::	Clock Pulse			tCWL	20
::	::	Clock Pulse		OW)	tCWM	5000
:: — A0	1 ' ' '	Address Set			tSA	5
:: A1	1 , , ,	Address Hol			tHA	5
:: — A2	1	Data Output			tHD0	5
:: — A3	, , ,	Input Data	Setup Tim	е	tSDI	20
:: A4	1	Input Data			tHDI	10
:: ─ A5	::	WE Setup Ti			tSEH	3
∷ — во	::	WE Hold Tim	е		tHEH	3
- B1	, , ,	WE Setup Ti			tSEL	5
:: — B2	1 ''	WE Hold Tim	e (Inhibi	tion Mode)	tHEL	5
:: — B3	1	i				
	1	1				
RA	1					
:: — B4						
B4 B5		* Minimum v	alues (or	maximum va	lue for CV	WM) for
				maximum val	lue for CV	√M) for
B5 WE	1				lue for CV	VM) for
В5	1			condition.	lue for CV	VM) for
B5 WE	1 2		peration (	condition.	lue for CV	VM) for
B5 WE WE CK	1 2 1	typical o	Input L	condition.	lue for CV	VM) for
B5 WE WE	1 2 1	typical o	Input L Factor	condition.  oading (lu) lu	lue for CV	VM) for
B5 WE WE CK	1 2 2 2	Pin Name	Input L Factor	condition.  coading (lu)  lu	lue for CV	WM) for
	1 2 1 2 TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5	Input Le Factor	condition.  coading (Lu) Lu Lu Lu	lue for CV	WM) for
	1 2 1 2 TO —	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2	Input L Factor	condition.  coading (lu) lu lu lu	lue for CV	WM) for
	1 2 1 2 TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5	Input Le Factor	condition.  coading (lu) lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO R61A	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Legactor  Input Legactor  1	condition.  coading (lu) lu lu lu lu lu lu lu	lue for CV	M) for
	1 2 1 2 TO TO R61A	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2	Input Le Factor	condition.  coading (lu) lu lu lu lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Legactor  Input Legactor  1	condition.  coading (lu) lu lu lu lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name	Input L Factor	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Legactor  Input Legactor  1	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name	Input L Factor	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu	lue for CV	WM) for
	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name	Input L Factor	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu	lue for CV	₩) for
	1 2 1 2 TO R61A 1 2	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name	Input Le Factor  1	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu		₩) for
- B5 - WE - CK - CK - T1 - T2 - T1 - TA - TW - TC - TC	1 2 1 2 TO TO TO TO TO TO TO TO TO TO TO TO TO	Pin Name  100 ~ 115  A0 ~ A5  B0 ~ B5  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D15	Input Le Factor  1	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu		WM) for
DES NOTE:    100	1 2 1 2 TO R61A 1 2	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name  D00 ~ D15	Input Le Factor  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	condition.  coading (lu) lu lu lu lu lu lu lu lu lu lu lu lu lu		
ote: 100 - 115 : A0 - A5 : B5 - WE WE - CK - T1 - T2 - T1 - T4 - TC - TC	1 2 TO R61A  1 2 Data Inputs Address Inputs	Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name  D00 ~ D15	Input Le Factor  1	condition.  coading (lu) lu lu lu lu lu lu lu lu criving (lu) lu : Data On ': Inputs	itputs for RAM Te	est
Ote: 100 - 115 : A0 - A5 : WE - WE T1 - TC TC  Ote: WE1, WE2 :	1 2 1 2 TO R61A 1 2 Data Inputs Address Inputs Write Enable	Pin Name  100 ~ 115  A0 ~ A5  B0 ~ B5  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D15  D00 - T1, T  TW, T	Input Le Factor  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	condition.  coading (lu) lu lu lu lu lu lu lu lu criving (lu) lu : Data On : Inputs : Output	ıtputs	est
Ote:  100 - 115 : A0 - A5 : B0 - B5 : WE1, WE2 : CK1, CK2 :	1 2 TO R61A  1 2 Data Inputs Address Inputs	Pin Name  100 ~ 115  A0 ~ A5  B0 ~ B5  WE1, WE2  CK1, CK2  Pin Name  D00 ~ D15  D00 - T1, T  TW, T  TO  ** A0	Input Le Factor  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	condition.  coading (lu) lu lu lu lu lu lu lu lu lu li Driving (lu) lu : Data On : Inputs : Output	itputs for RAM Te	est

DAM Mann	CMOS GATE ARI	RAY C	ELL SPECIFICA	TION		"AVM"	Version
RAM Name	Function				***************************************		
R61B	64w x 8b +	64w x	8b Single Po	rt Static	RAM		
RAM Symbol				pagation D			
			tup			dn	
::::::			t0	KCL	t0	KCL	Path
	100 D00		9	0.12	21	0.07	CK to D
	01 D01 - ::					1	
	102 D02						
	04 D04						İ
	05 D05						l
	06 D06						
	107 D07						1
::  -	::						
	108 D08 ::						
	109 D09 ::						
, , ,	110 D10 ::			l		l i	
	111 D11			ŀ			l
	112 D12		Parameter			Symbol	Typ(ns)
	113 D13		Clock Pulse	Width (Hig	h)	tCWH	25
	14 D14		Clock Pulse			tCWL	20
::   -	115 D15		Clock Pulse	Width (Low	·)	tCWM	5000
::-	.: 04		Address Setu	p Time		tSA	5
:: - A	A1 ::		Address Hold	Time		tHA	5
:: ⊢∤	12 ::		Data Output			tHD0	5
:: -   <i>E</i>	13		Input Data S			tSDI	20
:: -   <i>I</i>	14 ::		Input Data H			tHDI	10
:: - I	A5 ; ;		WE Setup Tim			tSEH	3
::	30		WE Hold Time			tHEH	3
	31		WE Setup Tim			tSEL	5
	- 1						
1	32		WE Hold Time	(Inhibiti	on Mode)	tHEL	5
	32		WE Hold Time	(Inhibiti	on Mode)	tHEL	5
: - I	33		WE Hold Time	(Inhibiti	on Mode)	tHEL	5
I I		,					
	33 34 35		* Minimum va	lues (or m	naximum va		
	33		* Minimum va		naximum va		
	33 34 35		* Minimum va	lues (or m	aximum va		
	33 34 35 WE1 WE2		* Minimum va typical op	lues (or meration co	naximum va		
	33 34 35 WE1		* Minimum va typical op Pin Name	lues (or meration co	naximum va		
- I	33 34 35 WE1 WE2		* Minimum va typical op Pin Name 100 ~ 115	lues (or meration co	ding		
- I	33 34 35 WE1 WE2 CK1		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5	lues (or meeration co	ding u)		
- I	33 34 35 WE1 WE2 CK1 CK2		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5	lues (or meration co	ding		
- I	33 34 35 WE1 WE2 CK1 CK2 F1 TO		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2	lues (or meration co Input Loa Factor (l 1 lu 1 lu 1 lu	ding (u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5	llues (or meration co	ding (u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO— F1 R61B		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2	llues (or meration co	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO — F2 F1 <b>R61B</b> FA		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO— F1 R61B		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO — F2 F1 <b>R61B</b> FA		* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO — F2 F1 <b>R61B</b> FA		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
	33 34 35 WE1 WE2 CK1 CK2 F1 TO — F2 F1 <b>R61B</b> FA		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 &	ding u)		
I	33 34 35 WE1 WE2 CK1 CK2 F1 TO — F2 F1 <b>R61B</b> FA	s	* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2	Input Loa Factor (& 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 36 Lu	ding u)	lue for CV	
I	33 34 35 WE1 WE2 CK1 CK2 F1 TO F2 F1 R61B FA FW FC1 FC2 : Data Input		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name	Input Loa Factor (& 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 1 Lu 36 Lu	ding (u) (i) (i) (i) (i) (i) (i) (i) (i) (i) (i	Outputs	M) for
Note:  100 - 115	33 34 35 WE1 WE2 CK1 CK2 F1 TO F2 F1 R61B FA FW FC1 FC2		* Minimum va typical op Pin Name 100 ~ 115 A0 ~ A5 B0 ~ B5 WE1, WE2 CK1, CK2 Pin Name D00 ~ D15	Input Loa Factor (Language 1 Lugaria)  I lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugaria 1 Lugar	ding (u) (i) (i) (i) (i) (i) (i) (i) (i) (i) (i	lue for CV	M) for
Note: 100 - 115 A0 - A5	33 34 35 WE1 WE2 CK1 CK2 F1 TO F2 F1 R61B FA FW FC1 FC2 : Data Input	puts	* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2 CK1, CK2 Pin Name DOO ~ D15	Ilues (or meration co Input Loa Factor (l 1 lu 1 lu 1 lu 1 lu 1 lu 36 lu  D15 2, TI, TA, 21, TC2	aximum vandition.  ding	Outputs	M) for
Note: 100 - 115 A0 - A5 B0 - B5	33 34 35 WE1 WE2 CK1 CK2 F1 TO F2 F1 R61B FA FW FC1 FC2  : Data Input : Address In	puts	* Minimum va typical op Pin Name IOO ~ I15 AO ~ A5 BO ~ B5 WE1, WE2 CK1, CK2 Pin Name DOO ~ D15	Ilues (or meration co Input Loa Factor (l 1 lu 1 lu 1 lu 1 lu 1 lu 1 lu 1 lu 1 l	aximum vandition.  ding	Outputs	M) for

	MOS GATE ARRAY C	ELL SPECIFICA	TION		"AVM	" Version
	Function					
l	128w x 8b Single 					
RAM Symbol			pagation	Delay Par		
		tup	77.07		tdn	n .,
		t0	KCL	t0	KCL	Path
10 - 11 - 12 - 13 - 14	D1 — : : : : : : : : : : : : : : : : : :	9	0.12	22	0.07	CK to D
15 16 17 17 17 17 17 17 17 18 18 18	D6 — : : : : : : : : : : : : : : : : : :					
:: — A4	, , ,	Parameter			Symbol	Typ(ns)*
- A5		Clock Pulse			tCWH	25
- A6		Clock Pulse			tCWL	20
		Clock Pulse		ow)	tCWM	5000
WE WE		Address Setup Time Address Hold Time			tSA tHA	5
:: — ск		Data Output			tHDO	5
:: - T1	то — : :	Input Data S			tSDI	20
$T_2$		Input Data H		<u> </u>	tHDI	10
	R71	WE Setup Tim		tSEH	3	
:: — TA	1 ' '	WE Hold Time			tHEH	3
TW		WE Setup Tim		ition Mode	) tSEL	5
TC	1	WE Hold Time	(Inhibi	tion Mode)	tHEL	5
TC	2	* Minimum va				WM) for
			T	41 1		
		Pin Name	Input Lo Factor			
		TII Name	ractor	(~u)		
		10 ~ 17	1	lu		
		A0 ~ A6	1	lu		
		WE	1 :			
		CK	1			
		D	Output 1	Driving		
		Pin Name	Factor	(ku)		
		DO ~ D7	36 .	lu		
A0 - A6 : WE :	Data Inputs Address Inputs Write Enable Clock	TW, TO	D7 , TI, TA 1, TC2 : LSB, A	': Input	Outputs s for RAM T	
R71	Sheet 1/1	110	. 200, A			
		3-281		C-230	1AVM-R71(12	8w x 8b)-E3

	CMOS GATE ARRAY C	ELL SPECIFIC	ATION		"AVM"	Version
R71A	128w x 4b + 128w	x 4b Single	Port Sta	tic RAM		
RAM Symbol				Delay Par		
		tup t0	KCL	t0	tdn KCL	Path
- 10 - 11 - 12 - 13 - 14	1 D1 —	9	0.12	22	0.07	CK to D
— 16 — 17 — A1 — A2	7 D7 — : : : : : : : : : : : : : : : : : :	Parameter Clash Pulse	Width (U	ich)	Symbol	Typ(ns)*
:: — A4	4	Clock Pulse			tCWL	20
:: — A!	1 ''	Clock Pulse			tCWM	5000
:: — A	6   ;;	Address Set		(N)	tSA	5
. — во	o   ::	Address Hol			tHA	5
В: — В:	1	Data Output		e	tHD0	5
В: — В:	2	Input Data			tSDI	20
:: ─ B:	3 ∷	Input Data			tHDI	10
:: - B4		WE Setup Ti			tSEH	3
:: ─ B:	1 ' '	WE Hold Tim	ie		tHEH	3
:: - Be	6	WE Setup Ti				5
wı	E1 ::	WE Hold Tim	ie (Innibi	tion mode	)   tHEL	1 3
	K1 K2 1 TO		peration	condition	value for tCV	WM) for
:: - T	, , ,		Input I			-
	I <i>R71A</i>	Pin Name IO ~ I7	Factor	(lu) lu		
	1 ' '	A0 ~ A6 B0 ~ B6 WE1, WE2 CK1, CK2	1 1 1 1	lu lu lu lu Driving		
Note:		DO ~ D7	36	Lu		
10 - 17 A0 - A6	: Data Inputs : Address Inputs : Write Enable : Clock   Sheet 1/1	T1, 7 TW, 7 TO ** A	- D7 F2, TI, TA FC1, TC2 D, B0 : LS 5, B6 : MS	A, : Inpu : Outp SB SB	Outputs ts for RAM To tut for RAM To	est

FUJITSU C	MOS GATE ARRAY O	ELL SPECIFICA	TION		"AVM"	Version
	Function		22011			10101011
R83	256w x 4b Single	Port Static	RAM			
RAM Symbol		Pro	pagation	Delay Par	ameter	
		tup			tdn	
		t0	KCL	t0	KCL	Path
						a
		9	0.12	22	0.07	CK to D
		1				i
:: — 1c	, ро⊢∷					
:: — II	1 ''				1	
12		1				
13	D3 -					
Ac	,   ;;					
A1	1 ''					
A2	1 ''					
:: — A3	3					
:: A4	1 ' '					
:: A5	1 ' '	Parameter			Symbol	Typ(ns)*
A6	1 , ,	Clock Pulse	Width (H	igh)	tCWH	25
:: — A7		Clock Pulse	Width (L	ow)	tCWL	20
: : WE		Clock Pulse		ow)	tCWM	5000
:: — cr		Address Setu		<u></u>	tSA	5
- T1	то -	Address Hold			tHA tHD0	5
:: — T2		Data Output Input Data S	etun Tim	e	tSDI	20
:: - Ti		Input Data H			tHDI	10
TA		WE Setup Tim			tSEH	3
TV	1	WE Hold Time			tHEH	3
: : — TO	, , ,	WE Setup Tim				5
:: TO	22	WE Hold Time	(Inhibi	tion Mode)	tHEL	5
		* Minimum va typical op			value for tCV	M) for
			Input L	oading		
		Pin Name	Factor	- 1		
		10 ~ 13	1	0,,		
		10 ~ 13 A0 ~ A7	1	lu		
		WE A	1			
		CK		lu		
			Output	Driving		
		Pin Name	Factor	(lu)		
		DO ~ D3	36	o.,		
		DO ~ D3	30	~4		
Note:					_	
	Data Inputs	D0 -			Outputs	
	Address Inputs		, TI, TA	': Input	s for RAM Te	est
	: Write Enable : Clock	TW, TO	1, TC2	_	it for RAM Te	
OK :	OTOCK		: LSB, A		TOT WHILL	
R83	Sheet 1/1		,		Γ	_ :
		3-283	·	C-230	1AVM-R83(256	6w x 4b)-E3

FUJITSU (	CMOS GATE ARRAY C	ELL SPECIFICA	TION		L"AVM"	Version
R83A	256w x 2b + 256w	x 2b Single	Port Stat	tic RAM		
RAM Symbol	2304 1 25 - 2304			Delay Par	ameter	
Min Dymbol		tup	Pagarion		tdn	
			KCL	t0	KCL	Path
	1_D1	9	0.12	22	0.07	CK to D
A A A A A A A A A A A A A	0 1 2 3 4					
- A	1	Parameter			Symbol	Typ(ns)*
i - A	1 ''	Clock Pulse			tCWH	25
	1.	Clock Pulse			tCWL	20
:: — B	1 ''	Clock Pulse		ow)	tCWM	5000
:: - B	1 ' '	Address Setu	p Time		tSA	5
:: - B		Address Hold	l Time		tHA	5
:: - B		Data Output	Hold Tim	e	tHD0	5
: - B		Input Data S			tSDI	20
:: — B	5 ::	Input Data H			tHDI	10
:: — B	6 ::	WE Setup Tim			tSEH	3
:: — B	7	WE Hold Time			tHEH	3
:: w	E1	WE Setup Tim				5
		WE Hold Time	e (Inhibi	tion Mode)	tHEL	5
— с — с т	E2 K1 K2 1 T0			maximum v	alue for tCV	M) for
	2		Input L	oading		
	I R83A	Pin Name	Factor	(lu)		
	W ::	10 ~ 13	1	lu		
	C1	A0 ~ A7		lu		
, , ,	C2	BO ~ B7	1	lu		
:: L		WE1, WE2	1	lu		
::::::		CK1, CK2		<u>lu</u>		
		Pin Name	Output Factor	Driving (lu)		
		DO ~ D3	36	lu		
Note:						
10 - 13	: Data Inputs	DO -	D3	: Data	Outputs	
AO - A7	_		2, TI, TA	١.	_	set
BO - B7 WE1, WE2	: Address Inputs : Write Enable		Ci, TC2	: Input	s for RAM To	
CK1, CK2	: Clock	** A0	, BO : LS	SB		
R83A	Sheet 1/1	A/	, B7 : MS	D D D D D D D D D D D D D D D D D D D	5w x 2b + 25	Page

	MOS GATE ARRAY	CELL SPECIFIC	ATION		"AVM"	Version
	Function	1 5				
1	64w x 36b Sing					
RAM Symbol			opagation			
		tup	KCL	t0	KCL	Dath
		10	KCL	ισ	- KCE	Path
		12	0.12	26	0.07	CK to D
10	о роо⊢∷				""	
10	1 D01		1			
	2 D02				1	
	3 D03	1 1	1			
	4 D04 ::	1	1		1	
,	6 D06	1 1	1			
	7 D07 - ::	1	l l			1
	8 D08		1			
10	9 D09 — 🗄				1	
:: - 11	0 D10		1			
7.0	n na l	]	l		1, , , 1	- ·
	0 D30 - :: 1 D31 - ::	Parameter Clock Pulse	Width (Hi	ah)	Symbol tCWH	Typ(ns)
	2 D32	Clock Pulse			tCWL	20
	3 D33	Clock Pulse	Width (Lo	w)	tCWM	5000
	4 D34	Address Set	up Time		tSA	5
:: - 13	5 D35 ::	Address Hol			tHA	5
A0		Data Output	Hold Time		tHD0	5
- A1		Input Data Input Data			tSDI	20
:: — A2		WE Setup Ti			tSEH	3
. A3		WE Hold Tim			tHEH	3
A4		WE Setup Ti		tion Mode	) tSEL	5
A5		WE Hold Tim	e (Inhibit	ion Mode)	tHEL	5
:: WE	::					
∷ — ск						
:: — <sub>T1</sub>	то	* Minimum v	alues (or	mavimum v	alue for tCV	M) for
T2			peration c		arue for cov	111) 101
TI	R610	, , , , , , , , , , , , , , , , , , ,	<b>F</b>			
TA			Input Lo	ading		
TW		Pin Name	Factor (	lu)		
TC		700 705	1 .			
TC	2	100 ~ 135 A0 ~ A5	1 0	-		
		WE AS	1 2			
		CK	1 2			
			Output I			
		Pin Name	Factor (	lu)		
		Dog Bor	1			
		D00 ~ D35	36 8	u		
		1	1	I		
Note:						
	Data Inputs	D00 -		: Data (	Outputs	
A0 - A5 :	Address Input	s T1, T	2, TI, TA,		=	est.
I00 - I35 : A0 - A5 : WE :	Address Input: Write Enable	s T1, T TW, T		: Input:	s for RAM Te	
100 - 135 : A0 - A5 : WE :	Address Input	s T1, T TW, T T0	2, TI, TA, C1, TC2	: Input:	=	
100 - 135 : A0 - A5 : WE : CK :	Address Input: Write Enable	s T1, T TW, T T0	2, TI, TA,	: Input:	s for RAM Te	

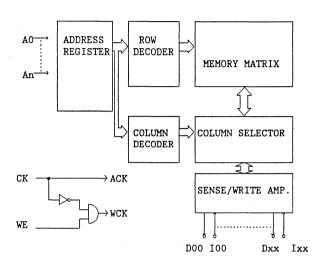
RAM Name	CMOS GATE ARRAY O	ADD SECTION	I I UN		AVII	Version
R611	64w x 20b + 64w	x 16b Single	Port Static	RAM		
AM Symbol		Pro	pagation Del	ay Parame	eter	
		tup		tdı	1	
		t0	KCL	t0	KCL	Path
		)	1	1		
:: [		12	0.12	26	0.07	CK to I
	100 D00		ļ	1		
	IO1 DO1 ::		1	1		
	IO2 DO2 ::	1	1	i		
	103 D03	1		1		
:: <u> </u>	717 017	1	1			
	I17 D17 ::		1			
	119 D19 — :			1	]	
	;;			j		
' ' 1	120 D20 ::					
	I21 D21	1			į	
:: <u>-</u>	122 D22	1			ĺ	
:: —		Parameter			Symbol	Typ(ns
	133 D33 ::	Clock Pulse	Width (High)		tCWH	25
	134 D34	Clock Pulse			tCWL	20
	135 D35	Clock Pulse			tCWM	5000
	AO ::	Address Setu			tSA	5
::⊢.	A1 ::	Address Hold			tHA	5
:: ⊢.	A2 ::	Data Output	Hold Time		tHD0	5
:: -	A3 ::	Input Data S			tSDI	20
:: -	A4 ::	Input Data H			tHDI	10
:: -	A5 ::		WE Setup Time			
:: -	во ::	WE Hold Time			tHEH	3
	B1 ::		e (Inhibitio		tSEL	5
	B2	WE Hold Time	(Inhibition	Mode)	tHEL	5
	В3					
	B4					
- : :	B5	* W	.1		f +CV	M) C
::	LTD 1	•	lues (or max		ue for tow	m) for
::	WE1	typical op	eration cond	ition.		
::	CK1	<u> </u>	Tanana Tanadi			
::	WE2	Pin Name	Input Loadi Factor (lu)			
::	ME2	100 ~ 135	1 Lu			
:: -	CK2	A0 ~ A5	1 &u			
::	т1 то ::	BO ~ B5	1 lu			
	T2	WE1, WE2	1 Lu			
	TI <i>R611</i>	CK1, CK2	1 lu			
	TA		Output Driv	ing		
	TW	Pin Name	Factor (lu)			
	TC1		1			
	TC2					
L	<del></del>	D00 ~ D35	36 lu			
* * * *						
7 .		<u></u>	<u></u>			
	. Data Innuta	DOO	D35 -	Data C	tnute	
	: Data Inputs	D00 -	ላጥ ፕፖ	Data Ou	•	
100 - 135	: Address Inputs		2, TI, TA, C1, TC2	Inputs	for RAM Te	est
I00 - I35 A0 - A5		14, 16	•	0	for DAM To	set.
I00 - I35 A0 - A5 B0 - B5	: Write Enable	ፐር				
A0 - A5 B0 - B5 WE1, WE2	: Write Enable	TO ** AO.		output	for RAM Te	236
I00 - I35 A0 - A5 B0 - B5	: Write Enable : Clock   Sheet 1/1	** A0,	; , BO : LSB , B5 : MSB	Output	101 KAN 16	

	CMOS GATE ARRAY C	ELL SPECIFICA	TION			"AVM"	'Version
RAM Name	Function						
R711	128w x 18b Singl	e Port Static	RAM				
RAM Symbol	<u> </u>	Pro	pagation	Delay Pa	ramet	ter	
		tup			tdn		
		t0	KCL	t0		KCL	Path
	100 D00 — 101 D01 — 102 D02 — 103 D03 — 104 D04 —	12	0.12	26		0.07	CK to D
	106 D06 — : : : : : : : : : : : : : : : : : :						The Cook
, , ,	[12 D12	Parameter	11/ 3+1- (17	/ - 1- \		Symbol	Typ(ns)*
	[13 D13	Clock Pulse Clock Pulse				tCWH	25
1 '' 1	[14 D14	Clock Pulse				tCWL tCWM	5000
	116 D16	Address Setu		OW)		tSA	5
	117 D17	Address Hold				tHA	5
		Data Output		e		tHD0	5
	70 ; ;	Input Data S				tSDI	20
	11 ::	Input Data H				tHDI	10
, , ,	12	WE Setup Tim				tSEH	3
	13	WE Hold Time				tHEH	3
, , ,	14	WE Setup Tim		ition Mod	le)	tSEL	5
	15 16	WE Hold Time	(Inhibi	tion Mode	)	tHEL	5
- W	VE CK C1 TO	* Minimum va				e for tCV	M) for
	[2 [] <i>R711</i>		Input L	oading			
	ra ii	Pin Name	Factor				
T —	TW TC1 TC2	100 ~ 117 A0 ~ A6 WE CK	1 : 1 : 1 : 1 : 1 : 1 : 1 : 1 : 1 : 1 :	lu lu lu Driving			
		Pin Name D00 ~ D17	Factor 36				
Note:	. Data Imputs	Doc	D1 7	, Det	. Out -		
AO - A6 WE CK	: Write Enable : Clock	TW, TC	TI, TA 1, TC2 : LSB, A	: Inpu	ts fo	or RAM Te	
R711	Sheet 1/1						-10.
Preliminary		3-287	C-1502A	VM/C-4002	:AVM-F	₹711(128₩	x 18b)-E2

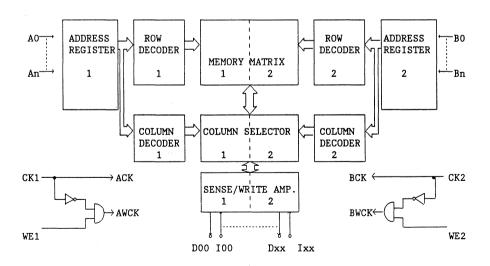
FUJITSU CMOS GATE ARRAY (	TETT COECTETCA	TION			II AT/M	' Version
RAM Name   Function	JELL STECIFICA	ITON			AVII	version
R712 128w x 9b + 128v	x 9b Single	Port Sta	tic RAM			
RAM Symbol	Pro	pagation	Delay Pa	rameter		
	tup	•		tdn		I
	t0	KCL	t0	I	CL	Path
:: [ ::	12	0.12	26	0.	.07	CK to D
:: - 100 DOO ::				-	1	ļ
:: - IO1 DO1 - ::					I	
102 D02					1	
103 D03					İ	1
104 D04 - :	1				ı	1
106 D06					l	
100 D00	1				1	
108 D08				1		
:: - 109 D09 - ::				l	1	1
:: <u>                                    </u>	.			i		1
	Parameter		<u> </u>	S	ymbol	Typ(ns)*
I16 D16	Clock Pulse	Width (H	igh)		CWH	25
117 D17	Clock Pulse	Width (L	ow)	t(	CWL	20
;	Clock Pulse		ow)	t(	CWM	5000
:: — A1 ::	Address Setu			t	SA	5
:: — A2	Address Hold				IA	5
:: A3	Data Output	Hold Tim	е		HD0	5
A4 ::	Input Data S				SDI	20
A5	Input Data H		,		HDI	10
A6 ::	WE Setup IIm	WE Setup Time				3
:: — BO ::	WE Setup Time		ition Mod		HEH SEL	3 5
:: - B1 ::	WE Hold Time				HEL	5
:: — B2	WE HOLD TIME	(IIIIIIDI	tion node	:) [	ши	
:: — B3						
:: — B4 ::						
B5	* Minimum va	lues (or	maximum	value :	for tC	WM) for
B6 ::	typical or	-				•
:: WE1 ::						
:: — ck1		Input L	oading			
	Pin Name	Factor				
:: - WE2 ::	I00 ~ I17	L	lu			
CK2	A0 ~ A6	1	lu			
	B0 ~ B6	1	lu			
T1 T0	WE1, WE2	i	lu			
T2 T1 R712	CK1, CK2		lu Driving			
$\vdots \longrightarrow \prod_{TA}^{T1} K^{T2} $	Pin Name	Factor				
::— TW   ::	1 III Name	1 20 001	(~u)			
TC1						
TC2	D00 ~ D17	36	lu			
N-+-	L	1				
Note:	00 <i>0</i>	D17	. Dot	. Outs	te	
I00 - I17 : Data Inputs A0 - A6	D00 -			a Outpu	LD	
BO - B6 : Address Inputs		2, TI, TA C1, TC2	՝ : Inpւ	uts for	RAM T	est
WE1, WE2 : Write Enable	TO	01, 102	: 011+1	put for	RAM T	'est
CK1, CK2 : Clock		, BO : LS		P 101	1	-50
R712   Sheet 1/1		, B6 : MS				<u> </u>
Preliminary				28w x 9	b + 12	8w x 9b)-E

FULITSU (	MOS GATE ARRAY C	ELL SPECIFIC	TTON		l "AV	M" Version
RAM Name	Function	ELL SIECIFICA	TITON		I AV	n version
R87	256w x 9b Single	Port Static	RAM			
RAM Symbol			pagation	Delay Pa		
		tup	VCI	+0	tdn KCL	Poth
		t0	KCL	t0	KCL	Path
		12	0.12	26	0.07	CK to D
10	D0 ⊢ ∷					11
::						
	1 ''					
∷ <b>⊣</b> is						
16	5 D6					
:: - 17					į.	
:: - 18	3 D8 ├─ ∷					
	)   <u>; ;</u>					
A1						
:: — A2	1 ''	Parameter		1	Symbol	Typ(ns)*
		Clock Pulse	Width (H	ligh)	tCWH	25
ii — A	1	Clock Pulse			tCWL	20
A6	1	Clock Pulse		ow)	tCWM	5000
A	7	Address Set			tSA tHA	5 5
:: wi	. ::	Data Output		ne	tHDO	5
; ;		Input Data			tSDI	20
CI CI		Input Data			tHDI	10
: T1		WE Setup Ti			tSEH	3
T	1	WE Hold Time			tHEH	3
T T		WE Setup Time				5 5
∷ — π		WE HOLD THE	s (Innibi	CIOII HOU	e)   thish	
	21					
: TO	C2 ::				value for t	CWM) for
		typical o	peration	condition	n.	
			Input L	andina I		
		Pin Name	Factor			
		1211 114115	140001	(~4)		
		10 ~ 18		lu		
		A0 ~ A7	i	lu		
		WE CK	_	lu 0		
		CK		lu Driving		
		Pin Name	Factor			
				`		
		DO ~ D8	36	lu		
Note:		L	1	l		
	: Data Inputs	DO -	D8	: Data	a Outputs	
	: Address Inputs		2, TI, TA	., : Inn	uts for RAM	Test
	: Write Enable		C1, TC2	_		
CK	: Clock	TO ** AO	: LSB, A		put for RAM	lest
R87	Sheet 1/1	AU	, пов, н	עטוו . יי		
Preliminary			C-150	2AVM/C-4	002AVM-R87(2	56w x 9h)-E2

Block Diagram of RAM (Case 1): R51, R61, R71, R83, R610, R710, R87

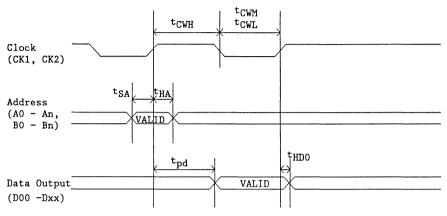


Block Diagram of RAM (Case 2): R51A, R51B, R51C, R51D, R61A, R61B, R71A R83A, R611, R712



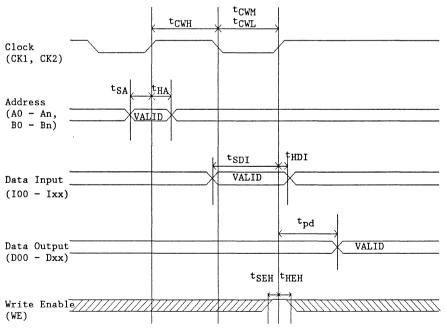
### Definition of Parameters for RAM

#### i) Read mode



 $t_{pd}$  = Access Time

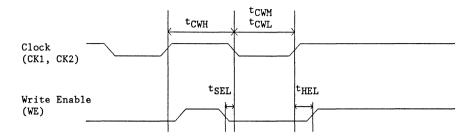
#### ii) Write mode



 $t_{pd}$  = Access Time

Definition of Parameters for RAM (cont'd)

### iii) Write Inhibit mode



### ROM Family for C-2301AVM

Unit Cell

Page Name

Function

3-295

YRn

256w x 8b ROM

### ROM Family for C-1502AVM/C-4002AVM

 Unit Cell Na64
 Function

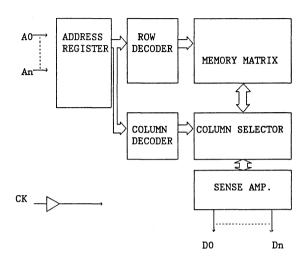
 3-296
 YRn
 256w x 18b ROM

 3-297
 YRn
 128w x 36b ROM

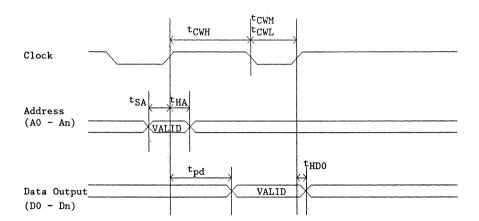
	OS GATE ARRAY	ONII CELE SPEC	JITICALIUN		AVM	Version
	256w x 8b Read	Only Memory				
ROM Symbol			pagation D	olay Par	ameter	
		tup	spagation 1		tdn	
		t0	KCL	t0	KCL	Path
		15	0.16	30	0.12	CK to D
A0 A1 A2 A3 A4 A5 A6 A6 A7	D0					
CV	1 ::	Parameter			Symbol	Typ(ns)
:: Ск		Clock Pulse			tCWH	35
:: <b>T1</b>	то 🗀 🗀	Clock Pulse			tCWL	25
:: T2	1 ::	Clock Pulse		)	tCWM	5000
	YRn ∷	Address Setu	ıp Time		tSA	5
:: TC1	1 ' '	Address Hold			tHA	5
TC2	<u>- ::</u>	Data Output	HOIG IIME		tHDO	5
		* Minimum va	alues (or m		alue for tCW	M) for
			Input Loa			
		Pin Name	Factor (1	u)		
		A0 ~ A7 CK	1 Lu 1 Lu			
		Pin Name	Output Dr Factor (&			
		DO ~ D7	36 Lu			
** A0: LSB, CK : C	Address Inputs A7: MSB Clock Data Outputs	T1, T2, TA,	, TC1, TC2:		for ROM Tes	
/Rn(256x8)   S	Sheet 1/1				Г	
reliminary		2 205		C-230	1AVM-YRn(256	w v 8h)-F

FUJITSU	CMOS GATE ARRAY U	NIT CELL SPEC	IFICATIO	N N	"AV	M" Version
ROM Name	Function					
YRn	256w x 18b Read	Only Me***ory				
ROM Symbol		Pro	pagation	Delay Pa	rameter	
		tup			tdn	
		t0 KCL t0 KCL				Path
A A A	0 D00 — 1 D01 — 2 D02 — 3 D03 — 4 D04 — 1	15	0.12	29	0.07	CK to D
: - A	.5 D05					
	D12	Parameter	177 141 (77		Symbol	
	D13	Clock Pulse			tCWH	30
	D14	Clock Pulse Clock Pulse			tCWL tCWM	25 5000
::	D16	Address Setu		OW)	tSA	5
1 ::	D17	Address Hold			tHA	5
::	sk iii	Data Output		e	tHDO	5
T - T	"2" A YRn CC1 CC2	* Minimum va				cCWM) for
		Pin Name	Input L Factor			
		A0 ~ A7 CK		Lu Lu		
		Pin Name	Output Factor	Driving (lu)		
		D00 ~ D17	36	Lu		
** A0: LSF CK : D00 - D17:	Clock Data Outputs	T1, T2, TA, TO	TC1, TC		s for ROM ?	
YRn(256x18)	Sheet 1/1					
Preliminary		3-206	C-150	2AVM/C-40	002AVM-YRn(	256w x 18b)-E1

		Y UNIT CELL SPEC	IFICATIO	N		"AVM"	Version
ROM Name	Function						
YRn	128w x 36b Re	ad Only Memory					
ROM Symbol			pagation	Delay Pa			
			tup         tdn           t0         KCL         t0         KCL				
		t0	KCL	t0		<u> </u>	Path
		15	0.12	29	0.	07	CK to D
l ∷-1,	AO DOO					`	
i:	A1 D01 :					- 11	
	A2 D02					11	
	A3 D03						
	A4 D04						
	A6 D06					11	
	D07						
	D08						
::	ДО9 — ∷						
::	D10 ::					- 11	
	D11				<u> </u>		
	D12 D13	Parameter Clock Pulse	111 d+b (11	/ ab	tC'	mbol	Typ(ns)*
::	D14	Clock Pulse			tC'		30 25
::	D15	Clock Pulse			tC'		5000
	D16	Address Setu			tS.		5
	D17	Address Hold			tH		5
	D18	Data Output	Hold Tim	e	tH	DO DO	5
11	D19 ::						
	D20						
11	D21						
::	D23						
	D24						
	D25 -						
::	D26 🗀 🗀						
	D27	4	1 (		1 6		
	D28 — — — — — — — — — — — — — — — — — — —	* Minimum va				or town	l) for
::	D30	typical op	eration	condition	Π.		
	D31 -		Input L	oading			
	D32	Pin Name	Factor				
	D33						
::	D34 ::	A0 ~ A6	I	lu			
	D35	CK	1	lu			
I ∷⊣,	CK 📑						
l ∷	ті то		Output	Driving			
	T2	Pin Name	Factor				
1 1	TA YRn			`			
	TC1						
::	TC2	D00 ~ D35	36	lu			
Note:							
A0 - A6	: Address Input	s T1, T2, TA,	TC1, TC		ts for R		
** A0: LS	B, A6: MSB	TO		: Outp	ut for R	OM Test	:
1	: Clock						
D00 - D35	: Data Outputs						
	) Sheet 1/1						
Preliminary		2 207	C-150	2AVM/C-4	002AVM-Y	Rn(128v	v x 36b)-E1



Definition of Parameters for ROM



### **APPENDIX A: General AC Specifications**

### Pre-layout Simulation Delay Specifications

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Min.	Max.	Unit
Propagation Delay Time	tPLH tPHL			
Enable Time	tPZL tPZH	(Typ)x0.45	(Typ)x1.6	ns
Disable time	tPLZ tPHZ			

### Post-layout Simulation Delay Specifications

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Min.	Max.	Unit
Propagation Delay Time	tPLH tPHL	<u> </u>		
Enable Time	tPZL tPZH	(Typ)x0.5	(Typ)x1.55	ns
Disable time	tPLZ tPHZ			

### **APPENDIX B: Estimation Tables for Metal Loading**

#### Master Table

Device			Table fo	r CL Estimat	ion		
	1	2	3	4	5	6	7
C-8000AV	•1			•²			
C-6600AV	•1			•²			
C-5000AV					•		
C-3900AV							•
C-2600AV	•						
C-4002AVM							
C-2301AVM	•3					●4	
C-1502AVM	<b>●</b> 3					•4	
C-2000AVB	•						
C-1600AVB	•						
C-1200AVB		•					
C-850AVB		•					
C-540AVB			•				
C-350AVB			•				

### Notes:

- 1. Internal block routing only.
- 2. Between-block routing only. (One I/O is regarded as one block.)
- 3. I/O cell not in the net.
- 4. I/O cell in the net.

# APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 1

NDI	CL (lu)	NDI	CL (lu)
1	1.2	11	7.9
2	3.5	12	8.0
3	4.7	13	8.1
4	5.5	14	8.3
5	6.1	15	8.3
6	6.6	16–30	9.0
7	7.2	31–50	10.3
8	7.5	51-75	12.3
9	7.7	76–100	14.4
10	7.9	100 and up	Prohibited

Table 2

NDI	CL (lu)	NDI	CL (ℓu)
1	1.1	11	5.2
2	2.3	12	5.3
3	3.1	13	5.3
4	3.6	14	5.5
5	4.0	15	5.5
6	4.4	16–30	5.9
7	4.8	31–50	6.8
8	5.0	51-75	8.1
9	5.1	76–100	9.5
10	5.2	100 and up	Prohibited

# APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 3

NDI	CL (lu)	NDI	CL (lu)
1	1.0	11	3.5
. 2	1.5	12	3.5
3	2.1	13	3.6
4	2.4	14	3.7
5	2.7	15	3.7
6	2.9	16–30	4.0
7	3.2	31–50	4.5
8	3.3	51-75	5.4
9	3.4	76–100	6.3
10	3.5	100 and up	Prohibited

Table 4

NDI	CL (lu)
1	22
2	27.5
3	33
4 and up	38.5
100 and up	Prohibited

# \_

### Table 5

NDI	CL (lu)	NDI	CL (lu)
1	1.9	11	11.9
2	5.3	12	12.1
3	7.2	13	12.2
4	8.3	14	12.4
5	9.1	15	12.4
6	9.9	16–30	13.5
7	10.8	31–50	15.5
8	11.2	51-75	18.5
9	11.6	76–100	21.7
10	11.9	100 and up	Prohibited

### Table 6

NDI	CL (lu)	NDI	CL (lu)
1	18.7	11	26.6
2	19.9	12	26.6
3	22.2	13	26.7
4	23.4	14	26.8
5	24.2	15	27.0
6	24.8	16–30	27.0
7	25.3	31–50	28.1
8	25.9	51-75	29.0
9	26.2	76–100	31.0
10	26.4	100 and up	Prohibited

# APPENDIX B: Estimation Tables for Metal Loading (Continued)

Table 7

NDI	CL (ℓu)	NDI	CL (ℓu)
1	1.5	11	10.1
2	4.5	12	10.2
3	6.0	13	10.4
4	7.0	14	10.6
5	7.8	15	10.6
6	8.4	16–30	11.5
7	9.2	31–50	13.2
8	9.6	51-75	15.7
9	9.9	76–100	18.4
10	10.1	100 and up	Prohibited

3

## APPENDIX C: AV CMOS Gate Array Available Package Types

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Dual In-line	Packages (Stan	dard type)				
DIP-24	Plastic	•	•	_	_	_
DIP-28	Ceramic	•	_	_	_	_
	Plastic	•		_	_	
DIP-40	Ceramic	•	•	_	_	-
	Plastic	•	•	•	_	_
DIP-42	Ceramic	•	•		_	
	Plastic	•	•	_	_	
Dlp-48	Ceramic	•	•	_	_	_
	Plastic	•	. •		_	_
DIP-64	Ceramic			_	•	_
DIP-42SH	Packages (Shri	•	— — — — — — — — — — — — — — — — — — —	<del>                                     </del>	_	
DIF-42311	Plastic	-	<u> </u>	<del>                                     </del>		
DIP-48SH	Plastic		•	<del> </del>		<del></del>
DIP-64SH	Plastic	<del></del>		<del>                                     </del>		
	es (with leads o	on all four sid	es of the page	ckage)	<del></del>	
FPT-48	Plastic	•	•			
FPT-64	Plastic	•	•	•	•	
FPT-80	Plastic	•	•	•	•	
FPT-100	Plastic	•	•	•	•	
FPT-120	Ceramic			•	•	•
	Plastic	*	•	•	•	•
FPT-160	Plastic	_	_	*	•	•
Pin Grid Arra	ay Packages					
PGA-64	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•
PGA-88	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•
PGA-135	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•
PGA-179	Ceramic	_	-	_	•	•
						+

<sup>=</sup> Available

<sup>\* =</sup> For these devices, standard pin assignment is not available; only the U version is available.

<sup>- =</sup> Not available

## APPENDIX C: AV CMOS Gate Array Available Package Types 316(Continued)

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Leadless Ch	ip Carriers					
LCC-48	Ceramic	•	•	•	_	
LCC-64	Ceramic	•	•	•	•	•
LCC-68	Ceramic	•	•	•	•	•
LCC-84	Ceramic	_	_	_	•	•
Plastic Lead	ed Chip Carrier					
PLCC-28	Plastic	•	_	_	_	_
PLCC-44	Plastic	•	•			
PLCC-68	Plastic	•	•	•		
PLCC-84	Plastic	•	•	•		-

- = Available
- = Not available

# APPENDIX C: AV CMOS Gate Array Available Package Types with U Type VSS and VDD Pin Assignment

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Dual In-line	Packages (Stan	dard type)				
DIP-24	Plastic	•	•	_	-	_
DIP-28	Ceramic	•	_	_	_	_
	Plastic	•	_	_	_	
DIP-40	Ceramic	•	•	_	_	_
	Plastic	•	•	•	_	_
DIP-42	Ceramic	•	•	_	_	
	Plastic	•	•		_	_
Dlp-48	Ceramic	•	•	_	_	_
	Plastic	•	•	_	_	_
	Packages (Shrii	nk type: 70 n	nil pin pitch)	<del></del>	<u> </u>	
DIP-42S	Ceramic	•			-	
	Plastic	•		<u> </u>		
DIP-48S	Plastic	•	•			
DIP-64S	Plastic	•	•	<u> </u>	•	
Flat Packag	es (with leads o	n all four sid	les of the pa	ckage)		
FPT-48	Plastic	•	•			
FPT-64	Plastic	•	•	•	•	<b>–</b>
FPT-80	Plastic	•	•	•	•	
FPT-100	Plastic	•	•	•	•	_
FPT-120	Ceramic			•	•	•
	Plastic	•	•	•	•	•
FPT-160	Plastic	_	_	•	•	•
Pin Grid Arr	ay Packages					
PGA-64	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•
PGA-88	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•
PGA-135	Ceramic	•	•	•	•	•
	Plastic	•	•	•	•	•

<sup>=</sup> Available

<sup>— =</sup> Not available

The U type pinout has the same number of VSS pins as the AVB version; that is, it has more VSS pins than the standard AV type. The part number of the device using this type of pinout is suffixed with U; e.g., MB652xxxU.

# APPENDIX C: AV CMOS Gate Array Available Package Types with U Type VSS and VDD Pin Assignment (Continued)

		C-2600AV (MB654K)	C-3900AV (MB653K)	C-5000AV (MB652K)	C-6600AV (MB651K)	C-8000AV (MB650K)
Leadless Ch	ip Carriers					
LCC-48	Ceramic	•	•	•	_	_
LCC-64	Ceramic	•	•	•	•	•
LCC-68	Ceramic	•	•	•	•	•
Plastic Lead	ed Chip Carrier		· .			
PLCC-28	Plastic	•	_	-	_	_
PLCC-44	Plastic	•	•	_	_	_
PLCC-68	Plastic	•	•	•	_	
PLCC-84	Plastic	•	•	•	_	_

- = Available
- = Not available

## APPENDIX C: AV CMOS Gate Array AVB Version Available Packages

MB675K)   MB674K)   MB672K)   MB672K)   MB670K)   MB670K)   MB670K)   MB670K)   MB670K)   MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB670K    MB67			C 350AVB	C EADAVB	C-850AVB	C 1200AVB	C 1600AVB	C-2000AVB
Dual In-line Packages (Standard type)								
DIP-16	Dual la line	Dooksoo (Ct		·	(	(2072.0)	(	(
Plastic					I			
DIP-18	DIP-16							<del></del>
Plastic								
DIP-20	DIP-18							
Plastic	DID 00							
DIP-22	DIP-20					_		
Plastic	5:5 66							
DIP-24	DIP-22							
Plastic				<u> </u>				
DIP-28	DIP-24							
Plastic					•			
DIP-40   Ceramic	DIP-28							
Plastic					<b></b>			
DIP-42   Ceramic	DIP-40		•		•	•	•	•
Plastic			•	•	•	•	•	•
DIP-48	DIP-42					•	•	•
Plastic         ●         ●         ●           Dual In-line Packages (Shrink type: 70 mil pin pitch)           DIP-28SH         Ceramic         —         —         —           Plastic         ●         ●         ●         —         —           DIP-42SH         Ceramic         —         —         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●				•	•	•	•	•
Dual In-line Packages (Shrink type: 70 mil pin pitch)           DIP-28SH         Ceramic         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —	DIP-48	Ceramic				•	•	•
DIP-28SH		Plastic		•	•	•	•	•
Plastic         ●         ●         —           DIP-42SH         Ceramic         —         —         ●         ●           Plastic         ●         ●         ●         ●         ●         ●           DIP-48SH         Plastic         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●	Dual In-line	Packages (Sh	rink type: 7	0 mil pin pi	itch)			
DIP-42SH         Ceramic         —         —         —         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●	DIP-28SH	Ceramic	_	•	•	•	_	_
Plastic         ●         ●         ●         ●           DIP-48SH         Plastic         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●		Plastic	•	•	•	•	•	
DIP-48SH         Plastic         ●         ●         ●         ●         DIP-64SH         Plastic         -         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●	DIP-42SH	Ceramic	_	_	_	•	•	•
DIP-64SH         Plastic         —         ●         ●         ●           Dual In-line Packages (Skinny type: 300 mil row space)         DIP-22SK         Plastic         ●         —         —         —         —           DIP-24SK         Plastic         ●         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —		Plastic	•	•	•	•	•	•
Dual In-line Packages (Skinny type: 300 mil row space)           DIP-22SK         Plastic         ●         —         —         —           DIP-24SK         Plastic         ●         ●         —         —         —           DIP-28SK         Plastic         ●         ●         —         —         —           Flat Packages (with leads on two sides of the packages)         FPT-16         Plastic         ●         —         —         —         —           FPT-20         Plastic         ●         ●         ●         —         —         —         —         FPT-24         Plastic         ●         ●         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —	DIP-48SH	Plastic	•	•	•	•	•	•
DIP-22SK         Plastic         ●         ●         -         -         -         -         DIP-24SK         Plastic         ●         ●         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -	DIP-64SH	Plastic	_	•	•	•	•	•
DIP-24SK         Plastic         ●         ●         —         —         —           DIP-28SK         Plastic         ●         ●         ●         —         —         —           FIat Packages (with leads on two sides of the packages)         FPT-16         Plastic         ●         —         —         —         —           FPT-20         Plastic         ●         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —	Dual In-line	Packages (Sk	inny type: 3	300 mil row	space)			
DIP-28SK         Plastic         ●         −         −         −           Flat Packages (with leads on two sides of the packages)           FPT-16         Plastic         ●         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −         −	DIP-22SK	Plastic	•	•	•	_	_	_
Flat Packages (with leads on two sides of the packages)         FPT-16       Plastic       ●       —       —       —         FPT-20       Plastic       ●       ●       —       —       —         FPT-24       Plastic       ●       ●       ●       —       —       —         FPT-28       Plastic       ●       ●       ●       ●       —       —         Flat Packages (with leads on all four sides of the packages)         FPT-44       Plastic       ●       ●       ●       ●       ●         FPT-48       Plastic       ●       ●       ●       ●       ●         FPT-64       Plastic       —       ●       ●       ●       ●         FPT-80       Plastic       —       —       ●       ●       ●       ●	DIP-24SK	Plastic	•	•	•		_	_
FPT-16         Plastic         •         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         -         - <t< td=""><td>DIP-28SK</td><td>Plastic</td><td>•</td><td>•</td><td>•</td><td></td><td></td><td></td></t<>	DIP-28SK	Plastic	•	•	•			
FPT-20         Plastic         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         <	Flat Packag	es (with leads	on two sid	es of the p	ackages)			
FPT-20         Plastic         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         <								_
FPT-24         Plastic         ●         ●         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         —         <	FPT-20		•	•				
FPT-28         Plastic         ●         ●         —         —         —           Flat Packages (with leads on all four sides of the packages)         FPT-44         Plastic         ●         ●         ●         ●         ●         ●         FPT-48         Plastic         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●         ●	FPT-24		•	•	•	•		
FPT-44         Plastic         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         • <t< td=""><td></td><td>Plastic</td><td>•</td><td>•</td><td>•</td><td>•</td><td></td><td></td></t<>		Plastic	•	•	•	•		
FPT-48         Plastic         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         • <t< td=""><td>Flat Packag</td><td>es (with leads</td><td>on all four</td><td>sides of th</td><td>e packages</td><td>)</td><td></td><td></td></t<>	Flat Packag	es (with leads	on all four	sides of th	e packages	)		
FPT-48         Plastic         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         •         • <t< td=""><td>FPT-44</td><td>Plastic</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td><td>•</td></t<>	FPT-44	Plastic	•	•	•	•	•	•
FPT-64         Plastic         —         •         •         •         •           FPT-80         Plastic         —         —         •         •         •			•	•	•	•	•	•
FPT-80 Plastic • • •			_	•	•	•	•	•
			_			•	•	•
	FPT-100		_			_	I –	•

<sup>=</sup> Available

<sup>- =</sup> Not available

## AV CMOS Gate Array AVB Version Available Packages (Continued)

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Repeated In-line Packages (Pin Grid Array Packages)							
PGA-64	Ceramic	-	•	•	•	•	•
	Plastic	_	•	•	•	•	•
PGA-88	Ceramic	_	_		_	•	•
	Plastic	_	_	_	_	•	• 1
Leadless C	hip Carriers						
LCC-28	Ceramic	•	•	•	•	•	_
LCC-48	Ceramic	•	•	•	•	•	_
LCC-64	Ceramic		•	•	•	•	•
LCC-68	Ceramic		_	_	-	•	•
Plastic Lead	ded Chip Carri	ers					
PLCC-28	Plastic	•	•	•	•	•	
PLCC-44	Plastic	•	•	•	•	•	•
PLCC-68	Plastic	_	_	_	•	•	•
PLCC-84	Plastic	_	_	_	_	-	•

<sup>=</sup> Available

<sup>- =</sup> Not available

# APPENDIX C: AV CMOS Gate Array AVB Version Available Packages (U-type Pinout Configuration)\*

		C-350AVB (MB675K)	C-540AVB (MB674K)	C-850AVB (MB673K)	C-1200AVB (MB672K)	C-1600AVB (MB671K)	C-2000AVB (MB670K)
Dual In-line Packages (Standard type)							
DIP-16	Ceramic	•	•	_	_	_	_
	Plastic	•	•				-
DIP-18	Ceramic	•	•	_	_	_	_
	Plastic	•	•		_		<del></del>
DIP-20	Ceramic	•	•	_	_	_	_
Ī	Plastic	•	•	•	_	_	_
DIP-22	Ceramic	•	•	•	•	•	_
1	Plastic	•	•	•	•	•	_
DIP-24	Ceramic	•	•	•	•	•	_
	Plastic	•	•	•	•	•	•
DIP-28	Ceramic	•	•	•	•	•	•
Ī	Plastic	•	•	•	•	•	•
DIP-40	Ceramic	•	•	•	•	•	•
	Plastic	•	•	•	•	•	•
DIP-42	Ceramic	_	_		•	•	•
	Plastic	•	•	•	•	•	•
Dlp-48	Ceramic	_	_	_	•	•	•
· ·	Plastic	_	•	•	•	•	•
Dual In-line	Packages (Sh	rink type: 7	0 mil pin pi	tch)			
DIP-28SH	Ceramic	Г <u>— —</u>	•	•	•	_	
	Plastic	•	•	•	•	•	_
DIP-42SH	Ceramic	_		_	•	•	•
	Plastic		<b></b>		•	•	•
DIP-48SH	Plastic	•	•	•	•	•	•
DIP-64SH	Plastic	_	•	•	•	•	•
Dual In-line	Packages (Sk	inny type: 3	300 mil row	space)		L	L
DIP-22SK	Plastic	•	•	•	_	_	_
DIP-24SK	Plastic	•	•	•	_		
DIP-28SK	Plastic	. •	•	•			
Flat Packag	es (with leads	on two sid	es of the p	ackages)			
FPT-16	Plastic	•	•				
FPT-20	Plastic	•	•				_
FPT-24	Plastic	•	•	•	•		_
FPT-28	Plastic	•	•	•	•	_	

<sup>\*</sup>The U-type pinout configurations have fewer VSS pins and are for designs that use no high-drive output buffers and need more signal pins than those specified for standard pinout. If a design does not require more signal pins than defined for standard pinout, the standard pinout is preferred.

<sup>=</sup> Available

<sup>- =</sup> Not available

# APPENDIX C: AV CMOS Gate Array AVB Version Available Packages (U-type Pinout Configuration)\*(Continued)

		C-350AVB	C-540AVB	C-850AVB	C-1200AVB	C-1600AVB	C-2000AVB		
		(MB675K)	(MB674K)	(MB673K)	(MB672K)	(MB671K)	(MB670K)		
Flat Packag	Flat Packages (with leads on all four sides of the packages)								
FPT-44	Plastic	•	•	•	•	•	•		
FPT-48	Plastic	•	•	•	•	•	•		
FPT-64	Plastic		•	•	•	•	•		
FPT-80	Plastic	_	_	_	•**	•	•		
FPT-100	Plastic		-	_	_	_	•		
Repeated In	n-line Package:	s (Pin Grid	Array Packa	iges)					
PGA-64	Ceramic	_	•	•	•	•	•		
	Plastic	_	•	•	•	•	•		
PGA-88	Ceramic		_	_	_	•**	•		
	Plastic	_		_	_	•**	•		
Leadless Cl	hip Carriers						*		
LCC-28	Ceramic	•	•	•	•	•	_		
LCC-48	Ceramic	•	•	•	•	•	_		
LCC-64	Ceramic		•	•	•	•	•		
LCC-68	Ceramic		_		_	•	•		
Plastic Lead	ded Chip Carri	ers							
PLCC-28	Plastic	•	•	•	•	•			
PLCC-44	Plastic	•	•	•	•	•	•		
PLCC-68	Plastic				•	•	•		
PLCC-84	Plastic	-	_	-	_	_	•		

<sup>\*</sup>The U-type pinout configurations have fewer VSS pins and are for designs that use no high-drive output buffers and need more signal pins than those specified for standard pinout. If a design does not require more signal pins than defined for standard pinout, the standard pinout is preferred.

- = Available
- = Not available
- \*\* = U-type version is not available

## AV CMOS Gate Array AVM Version Available Package Types (RAM)

		C-1502AVM (MB662K)	C-2301AVM (MB661K)	C-4002AVM (MB660K)
Dual In-line I	Packages (Star	ndard type)		
DIP-24	Plastic	•	•	_
DIP-28	Plastic	•	_	_
DIP-40	Ceramic	•	•	_
	Plastic	•	•	_
DIP-42	Ceramic	•	•	_
	Plastic	•	•	
DIP-48	Ceramic	•	•	_
Dual In-line I	Packages (Shri	nk type: 70 mil	pin pitch)	
DIP-42S	Plastic	•		
DIP-48S	Plastic	•	•	
DIP-64S	Plastic	•	•	•
Flat Package	es			
FPT-48	Plastic	•	•	_
FPT-64	Plastic	•	•	•
FPT-80	Plastic	•	•	•
FPT-100	Plastic	• .	•	•
FPT-120	Plastic	•*	•*	•*
FPT-160	Plastic			•**
Pin Grid Arra	ay Packages			
PGA-64	Ceramic	•	•	•
	Plastic	•	•	•
PGA-88	Ceramic	•	•	•
	Plastic	•	•	•
PGA-135	Ceramic	•	•	•
	Plastic	<u> </u>	•	<u> </u>
Leadless Ch	ip Carriers			
LCC-48	Ceramic	•	•	
LCC-64	Ceramic	•	•	•
LCC-68	Ceramic	•		•
Plastic Lead	ed Chip Carrie	rs		
PLCC-44	Plastic	•	•	
PLCC-68	Plastic	•	•	
PLCC-84	Plastic	•	•	

- = Available
- = Not available
- \* = 8 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 662xxxU. Fujitsu recommends the 8 ground pin option for the package.
- \*\* = 12 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 660xxV. Fujitsu recommends the 12 ground pin option for the package.

		C-1502AVM (MB662K)	C-2301AVM (MB661K)	C-4002AVM (MB660K)
Dual In-line F	Packages (Stan	dard type)		
DIP-24	Plastic	•	•	_
DIP-28	Plastic	•	_	_
DIP-40	Ceramic	•	•	_
	Plastic	•	•	_
DIP-42	Ceramic	•	•	
	Plastic	•	•	
Dlp-48	Ceramic	•	•	
Dual In-line F	Packages (Shrir	nk type: 70 mil	pin pitch)	
DIP-42S	Plastic	•		
DIP-48S	Plastic	•	•	
DIP-64S	Plastic	•	•	•
Flat Package	s			
FPT-48	Plastic	•	. •	_
FPT-64	Plastic	• .	•	•
FPT-80	Plastic	•	•	•
FPT-100	Plastic	•	•	•
FPT-120	Plastic	•*	•*	•*
FPT-160	Plastic		L	•**
Pin Grid Arra	y Packages			
PGA-64	Ceramic	•	•	•
	Plastic	•	•	•
PGA-88	Ceramic	•	•	•
	Plastic	•	•	•
PGA-135	Ceramic	•	•	•
	Plastic	•	•	•
Leadless Ch	ip Carriers			
LCC-48	Ceramic	•	•	
LCC-64	Ceramic	•	•	•
LCC-68	Ceramic	•	<u> </u>	•
Plastic Lead	ed Chip Carrier	s		
PLCC-44	Plastic	•	• .	
PLCC-68	Plastic	• .	•	
PLCC-84	Plastic	•	•	

- = Available
- -- = Not available
- \* = 8 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 662xxxU. Fujitsu recommends the 8 ground pin option for the package.
- \*\* = 12 ground pin option. The part number of the device using this type of pinout is suffixed with "U"; e.g., 660xxxU. Fujitsu recommends the 12 ground pin option for the package.

# APPENDIX D: AV Unit Cell Library Alphanumeric Index (Memory Cells are listed separately at the end of this index)

Name	Function	Page	No.
A1N	1-bit Full Adder		3-195
A2N	2-bit Full Adder		3-197
A4H	'4-bit Binary Full Adder with Fast Carry		3-199
BD3	Buffer (Delay Cell)		3-213
BD5	Buffer (Delay Cell)		3-214
BD6	Buffer (Delay Cell)		3-215
C11	Flip-Flop for Counter		3-175
C41	4-bit Binary Asynchronous Counter		3-177
C42	4-bit Binary Synchronous Counter		3-180
C43	4-bit Binary Synchronous Up Counter		3-183
C45	4-bit Binary Synchronous Up Counter		3-186
C47	4-bit Binary Synchronous Up/Down Counter		3-189
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<sup>\*</sup> Can be used only with AVB technology

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<sup>\*</sup> Can be used only with AVB technology

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# Section 4

## Sales Information

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## Headquarters Locations — Worldwide

#### WORLD HEADQUARTERS

#### Fujitsu Limited

Furukawa Sogo Bldg. 6-1 Marunouchi 1-chome Chiyoda-ku, Tokyo 100 Japan

Tel: 81-3-216-3211 TWX: 781-228833 Fax: 81-3-216-9771

#### U.S.A. HEADQUARTERS

Fujitsu Microelectronics, Inc.

3545 North First Street San Jose, CA 95134-1804 USA

Tel: (408) 922-9000 Fax: (408) 432-9044 TWX: 910-338-0190

#### **EUROPEAN HEADQUARTERS**

#### Fujitsu Mikroelektronik GmbH

Arabella Centre 9. OG./A Lyoner Strasse 44-48 D-6000 Frankfurt 71 F.R. Germany Tel: 49-69-66320

Telex: 411963 Fax: 49-69-663-2122

#### ASIA/PACIFIC HEADQUARTERS

Fujitsu Microelectronics Pacific Asia Limited 805 Tsimshatsui Centre

West Wing 66 Mody Road Tsimshatsui East Kowloon, Hong Kong

Tel: 852-3-732-0100 Telex: 31959 FUJIS HX Fax: 852-3-722-7984

#### CALIFORNIA

Fujitsu Microelectronics, Inc. 3545 North First Street San Jose, CA 95034 Tel: (408) 922-9444 Fax: (408) 725-8746

#### **GEORGIA**

Fujitsu Microelectronics, Inc. 3500 Parkway Lane Suite 200

Norcross, GA 30092 Tel: (404) 242-5865 Fax: (404) 242-5869

#### ILLINOIS

Fujitsu Microelectronics, Inc. One Pierce Place Suite 930 Itasca, IL 60143 Tel: (312) 250-7160

#### **MASSACHUSETTS**

Fax: (312) 250-7176

Fujitsu Microelectronics, Inc. 75 Wells Avenue

Suite 3 Newton Centre, MA 02159 Tel: (617) 964-7088

Fax: (617) 964-1939

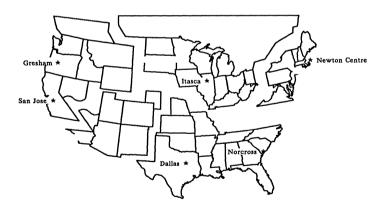
#### OREGON (Late 1989)

Fujitsu Microelectronics, Inc. 21015 S.E. Stark Street Gresham, OR 97030 Tel: (503) 669-6000 Fax: (503) 669-8471

#### **TEXAS**

Fujitsu Microelectronics, Inc. 14785 Preston Road Suite 665 Dallas, TX 75240

Tel: (214) 960-7392 Fax: (214) 386-7921



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## ■ Technical Resource Centers — Europe

#### BRITAIN

Fujitsu Microelectronics Ltd. Vaughan Street West Gorton Manchester M12 5DU

Tel: 44-061-230-6262 Fax: 44-061-230-6276 Telex: 667-403-FMLG

#### GERMANY

Fujitsu Mikroelektronik GmbH Arabella Center 9. OG Lyoner Strasse 44-48 D-6000 Frankfurt 71 Tel: 49-69-66320

Fax: 49-69-663-2122 Telex: 411963

#### NORTHERN CALIFORNIA

Fuiltsu Microelectronics, Inc. 10600 N. DeAnza Blvd.

Suite 225

Cupertino, CA 95014 Tel: (408) 996-600 Fax: (408) 725-8746

#### SOUTHERN CALIFORNIA

Fujitsu Microelectronics, Inc. Century Centre 2603 Main Street Suite 510 Irvine, CA 92714

Tel: (714) 724-8777 Fax: (714) 724-8778

Fujitsu Microelectronics, Inc. 5330 Carroll Canyon Road Suite 206 San Diego, CA 92121

Tel: (619) 452-3717

#### **GEORGIA** (Atlanta)

Fujitsu Microelectronics, Inc. 3500 Parkway Lane Suite 210

Norcross, GA 30092 Tel: (404) 449-8539 Fax: (404) 441-2016

#### ILLINOIS (Chicago)

Fuiltsu Microelectronics, Inc. One Pierce Place Suite 910 Itasca, IL 60143-2681

Tel: (312) 250-8580 Fax: (312) 250-8591

#### MASSACHUSETTS (Boston)

Fujitsu Microelectronics, Inc. 75 Wells Avenue Suite 5

Newton Centre, MA 02159-3251 Tel: (617) 964-7080

Fax: (617) 964-3301

### MINNESOTA (Minneapolis)

Fuiltsu Microelectronics, Inc. 3460 Washington Drive Suite 209

Eagan, MN 55122-1303 Tel: (612) 454-0323 Fax: (612) 454-0601

#### **NEW JERSEY (Cherry Hill)**

Fuiltsu Microelectronics, Inc. Horizon Corporate Center 3000 Atrium Way Suite 100

Mt. Laurel, NJ 08054 Tel: (609) 727-9700 Fax: (609) 727-9797

#### NEW YORK (Long Island)

Fuiltsu Microelectronics, Inc. 601 Veterans Memorial Highway

Suite P

Hauppauge, NY 11788-1054

Tel: (516) 361-6565 Fax: (516) 361-6480

#### OREGON (Portland)

Fujitsu Microelectronics, Inc. 5285 SW Meadows Road Suite 222

Lake Oswego, OR 97035-9998

Tel: (503) 684-4545 Fax: (503) 684-4547

#### **TEXAS**

Fujitsu Microelectronics, Inc. 14785 Preston Road Suite 670

Dallas, TX 75240 Tel: (214) 233-9394 Fax: (214) 386-7917

### Sales Office Locations — Europe

France

Fujitsu Immeuble le Trident 3-5, Voie Felix Eboue F-94024 Creteil Cedex Tel: 33-14-207-8200

Telex: 62861 Fax: 33-14-207-7933

North Germany

Fujitsu Mikroelektroniks GmbH Lyoner Strasse 44-48 Arabella Center 9. OG D-6000 Frankfurt 71 Tel: 49-69-66320 Telex: 441963

South Germany

Fax: 49-69-663-2122

Fujitsu Mikroelektronik GmbH Arbeostrasse 5 D-8057 Echina Tel: 49-89-3190990

Telex: 5213905 Fax: 49-89-319-0922 Italy

Fujitsu Microelectronics Italia S.R.L. Centro Direzionale Milanofiori Strada 4 - Palazzo A/2 Tel: 34-2-824-6170 Telex: 318546 Fax: 34-2-824-6189

Netherlands

Fujitsu Mikroelektronik GmbH Europalaan 6/B 5623 LJ Eindhoven Tel: 31-40-447-440 Telex: 59265

Fax: 31-40-444-158

Sweden

Fujitsu Nordic AB Torggatan 8 17154 Solna Tel: 46-87646365 Telex: 13411 Fax: 46-8280345

**United Kingdom** 

Fujitsu Microelectronics Ltd. Hargrave House Belmont Road Maidenhead Berkshire SL6 6NE Tel: 44-6-287-6100

Telex: 848955 Fax: 44-6-28781484



1	Design	Information
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2 UHB Series Unit Cell Library

AV Series Unit Cell Library

4. Sales Information

## FUJITSU LIMITED

Communications and Electronics

Marunouchi Headquarters 6-1 Marunouchi 1-chome Chiyoda-ku, Tokyo 100, Japan Tel: National (03) 216-3211 International (011) (81) (3) 216-3211 Telex: 781-22833 FAX: 011-81-3-213-7174

For further information, please contact

#### Japan

FUJITSU LIMITED Integrated Circuits and Semiconductor Marketing Furukawa Sogo Bldg.
6-1 Marunouchi, 1-chome, Chiyoda-ku Tokyo 100, Japan Tel: National (03) 216-3211 International (011) (81) (3) 216-3211 Telex: 781-222-4361 FAX: (011) (81) (3) 216-9771

#### **Europe**

FUJITSU MIKROELEKTRONIK GmbH Arabella Centre 9.0G Lyoner Straße 44-48 D-6000 Frankfurt am Main 71, FR. Germany Tel: (069) 66320 Telex: 411963 FAX: (069) 6632122

#### Asia

FUJITSU MICROELECTRONICS PACIFIC ASIA LIMITED 805 TsimShaTsui Centre West Wing 66 Mody Road Kowloon, Hong Kong Tel: (852) (3) 732-0100 Telex: 31959 FAX: (852) (3) 772-7984

North and South America FUJITSU MICROELECTRONICS, INC. Integrated Circuits Division 3545 North First Street San Jose, California 95134 U.S.A. Tel: (408) 922-9000

Telex: 910-338-0190 FAX: (408) 432-9044