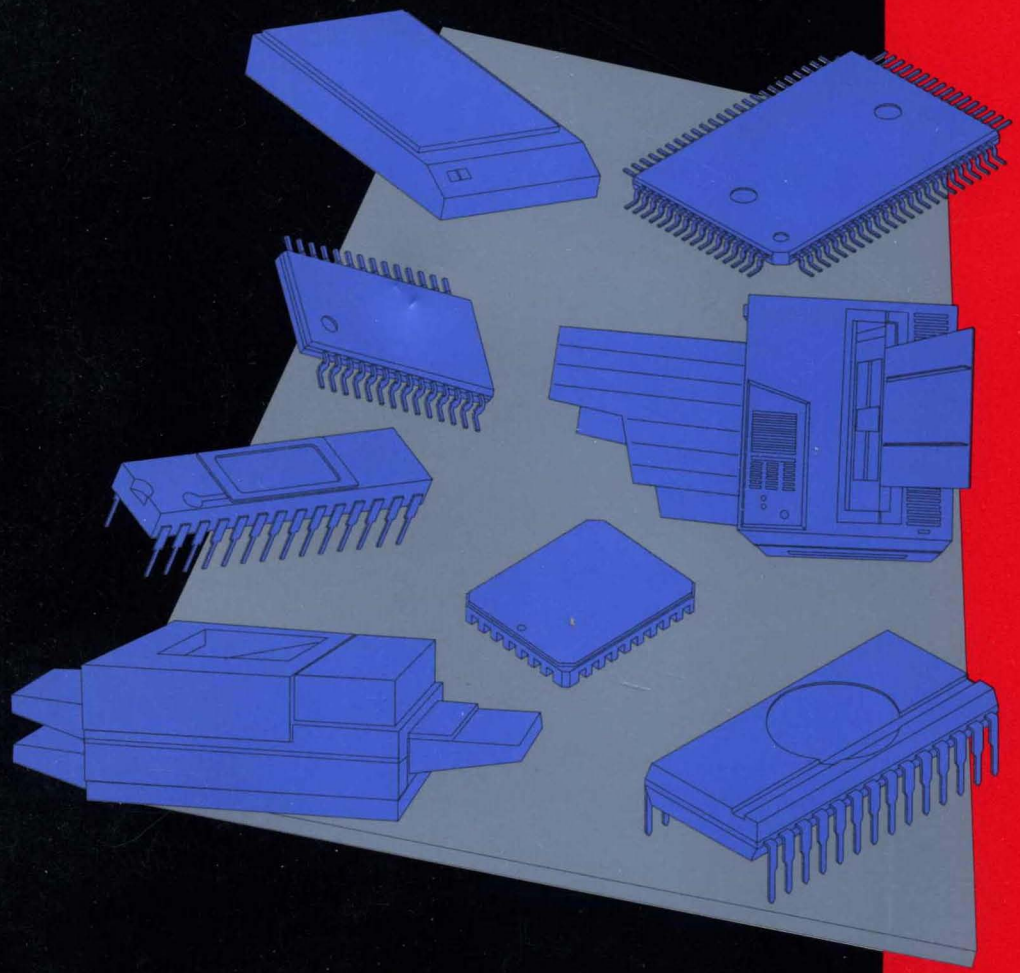
Data Book

Static RAM Products

1990

FUJITSU

Static RAM Products



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Edition 1.0

Contents and Alphanumeric Product List

SRAM Products

Contents and Alphanumeric Product List (Continued)

SRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

SRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

SRAM PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

Fujitsu's Static RAM Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs.

The static RAM product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

This data book includes product information on the following SRAM products:

High-speed CMOS SRAMs

Fujitsu's high-speed CMOS SRAMs offer the advantages of low power dissipation, low cost, and high performance. Features include TTL compatibility and a separate chip-select pin that simplifies multipackage systems design.

High-speed BiCMOS SRAMs

Advanced BiCMOS technology adds ultra-fast access times to CMOS low power dissipation in Fujitsu's new family of static RAMs. Most devices feature an automatic power-down mode and are generally available in small outline packages with J–leads (SOJ).

Low-speed CMOS SRAMs

Our low-power CMOS SRAMs are ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. The memories use asynchronous circuitry and may be maintained in any state for an indefinite period of time.

Application-Specific SRAMs

To address the system needs of cache memory chips, Fujitsu's application-specific memory line includes both cache TAG RAM and high-speed static RAM, as well as port RAMs for multiprocessor systems.

Fujitsu's Static RAM Products (Continued)

Wide Temperature Range SRAMs

For applications requiring MIL-STD-883 processing, Fujitsu offers a selection of high-performance, TTL-compatible CMOS static RAM products. All of these devices operate in the "W" temperature range, generally 55° to 125°C. (See product specifications for specific temperature range.)

CMOS SRAM Modules

Fujitsu manufactures a complete family of reliable CMOS static RAM memory modules for those applications requiring high density and large memory storage capability. Fujitsu's family of memory modules are pin-compatible with JEDEC standards.

Section 1

1

High-Speed CMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
1–3	MB81C67–35	35	16384 bits	20-pin Plastic DIP
	–45	45	(16384w x 1b)	20-pin Ceramic DIP
	–55	55		20-pad Ceramic LCC
1–15	MB81C68A–25	25	16384 bits	20-pin Plastic DIP, ZIP
	–30	30	(4096w x 4b)	20-pin Ceramic DIP
	–35	35		
1–27	MB81C69A–25	25	16384 bits	20-pin Plastic DIP
	–30	30	(4096w x 4b)	20-pin Ceramic DIP
	–35	35		
1–39	MB81C71A–25	25	65536 bits	22-pin Plastic DIP
	–35	35	(65536w x 1b)	24-pin Plastic LCC
				22-pad Ceramic LCC
1–51	MB81C74–25	25	65536 bits	22-pin Plastic DIP
	–35	35	(16384w x 4b)	22-pad Ceramic LCC
1–61	MB81C75–25	25	65536 bits	24-pin Plastic DIP
	–35	35	(16384w x 4b)	24-pin Plastic LCC
1–73	MB81C78A–35	35	65536 bits	28-pin Plastic DIP, FPT
	–45	45	(8192w x 8b)	32-pad Ceramic LCC
1–87	MB81C79A–35	35	73728 bits	28-pin Plastic DIP, FPT
	–45	45	(8192w x 9b)	32-pad Ceramic LCC
1–101	MB81C81A–35	35	262144 bits	24-pin Plastic DIP, LCC
	–45	45	(262144w x 1b)	24-pin Ceramic DIP
				24-pad Ceramic LCC
1–113	MB81C84A–35	35	262144 bits	24-pin Plastic DIP, LCC
	–45	45	(65536w x 4b)	
1–123	MB81C86–55	55	262144 bits	28-pin Ceramic DIP
	–70	70	(65536w x 4b)	32-pad Ceramic LCC
1–131	MB8289–25	25	262144 bits	32-pin Plastic DIP, FPT
	–35	35	(32768w x 9b)	

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FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB 81C67-35
MB 81C67-45
MB 81C67-55

March 1986
Edition 2.0

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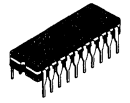
16,384 WORDS x1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB 81C67 is 16,384 words x 1 bit static random access memory fabricated with a CMOS silicon gate process. All pins are TTL compatible and a single 5 volts power supply is required.

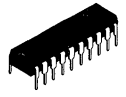
For ease of use, chip select ($\overline{CS}$) permits the selection of an individual package when outputs are OR-tied, and automatically power down the MB 81C67. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 16,384 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 35 ns max. (MB 81C67-35)
  45 ns max. (MB 81C67-45)
  55 ns max. (MB 81C67-55)
- Single +5 V supply, ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 20-pin DIP package (Suffix: CZ, Suffix: P)
- Standard 20-pad Leadless Chip Carrier (Suffix: TV)
- Pin compatible with Fujitsu MB 8167A



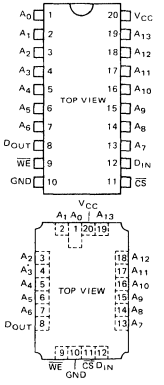
CERAMIC PACKAGE
CERDIP
DIP-20C-C03

CERAMIC PACKAGE
LCC-20C-F01



PLASTIC PACKAGE
DIP-20P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7.0	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.2	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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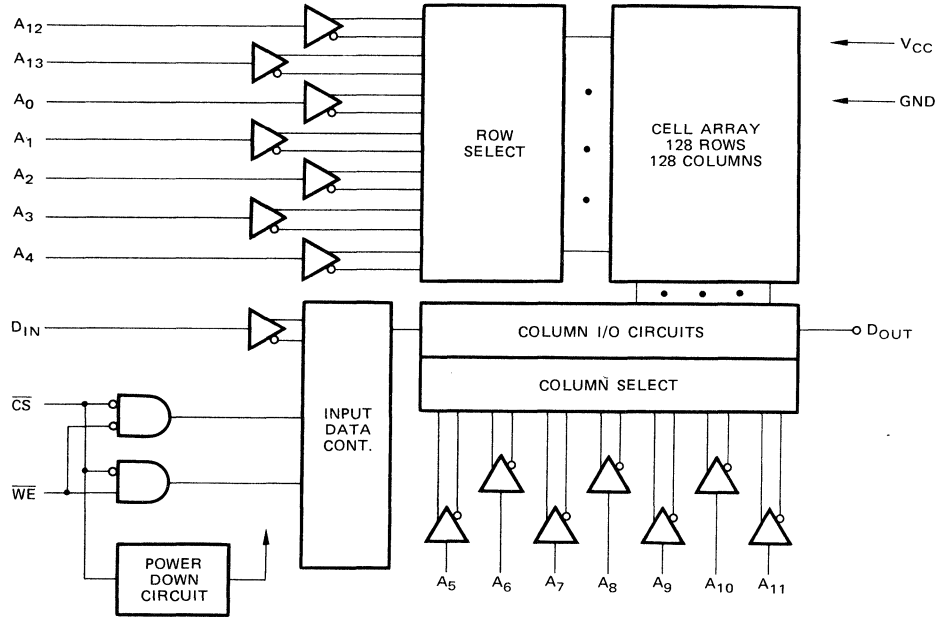
Fig. 1 – MB 81C67 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*-3.0V Min. for pulse width less than 20ns. (V_{IL} Min = -1.0 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

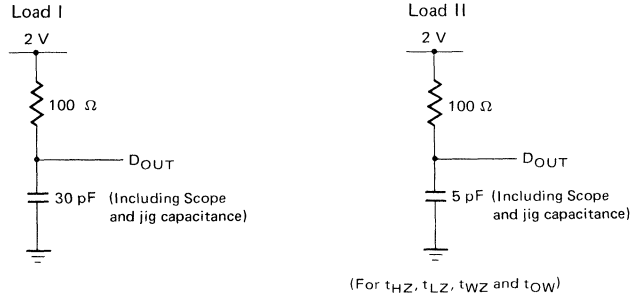
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-2.0		2.0	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}	I_{LO}	-2.0		2.0	μA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	40	mA
Operating Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA Cycle = Min, C_L = 0 pF	I_{CC2}		35	60	mA
Standby Supply Current	$\overline{CS} \geqq V_{CC} - 0.2$ V $V_{IN} \geqq V_{CC} - 0.2$ V or $V_{IN} \leqq 0.2$ V	I_{SB1}		2	15	mA
Standby Supply Current	$\overline{CS}$ = V_{IH}	I_{SB2}		15	25	mA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

1

AC TEST CONDITIONS

Input Pulse Levels :	0.6 V to 2.4 V
Input Pulse Rise And Fall Times :	5 ns
Timing Measurement Reference Levels :	Input : 1.5 V Output : 1.5 V

Output Load : Fig. 2



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

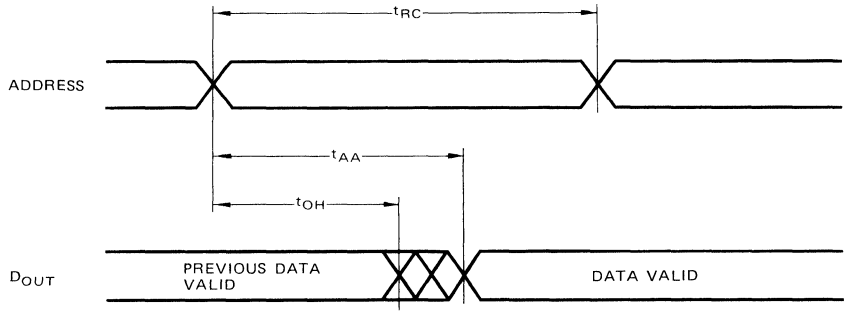
Parameter	Symbol	MB 81C67-35		MB 81C67-45		MB 81C67-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	35		45		55		ns
Address Access Time*3	t_{AA}		35		45		55	ns
Chip Select Access Time*4	t_{ACS}		35		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low-Z*5	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*5	t_{HZ}	0	25	0	25	0	30	ns
Chip Selection to Power Up	t_{PU}	0		0		0		ns
Chip Deselection to Power Down	t_{PD}		30		40		50	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

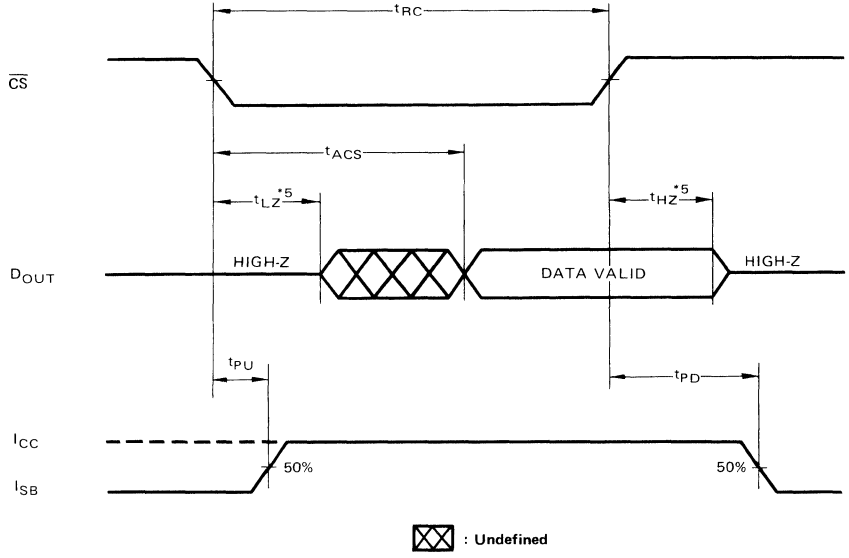
1

READ CYCLE TIMING DIAGRAM*1*2

READ CYCLE: ADDRESS CONTROLLED*3



READ CYCLE: $\overline{CS}$ CONTROLLED*4



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

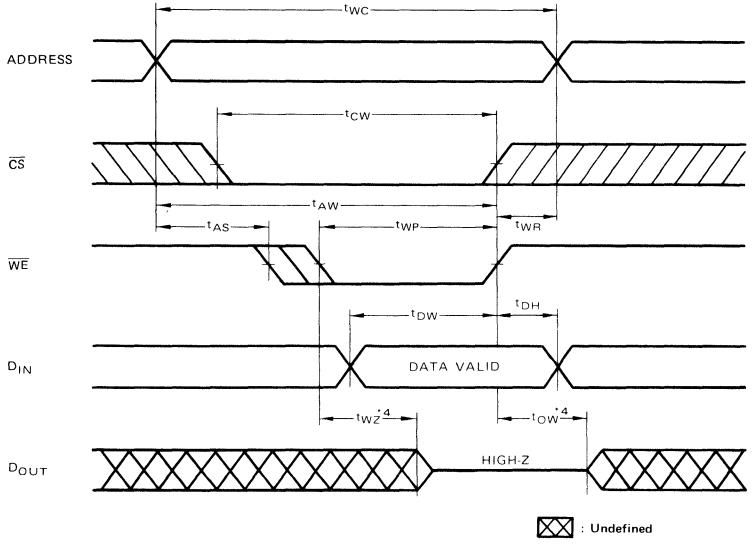
1

WRITE CYCLE*1*2

Parameter	Symbol	MB 81C67-35		MB 81C67-45		MB 81C67-55		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	35		45		55		ns
Chip Selection to End of Write	t_{CW}	30		35		50		ns
Address Valid to End of Write	t_{AW}	30		35		50		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Valid to End of Write	t_{DW}	20		20		25		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in High-Z*4	t_{WZ}	0	25	0	25	0	30	ns
Output Active from End of Write*4	t_{OW}	0	25	0	25	0	30	ns

WRITE CYCLE TIMING DIAGRAM*1*2

WRITE CYCLE: $\overline{WE}$ CONTROLLED*3

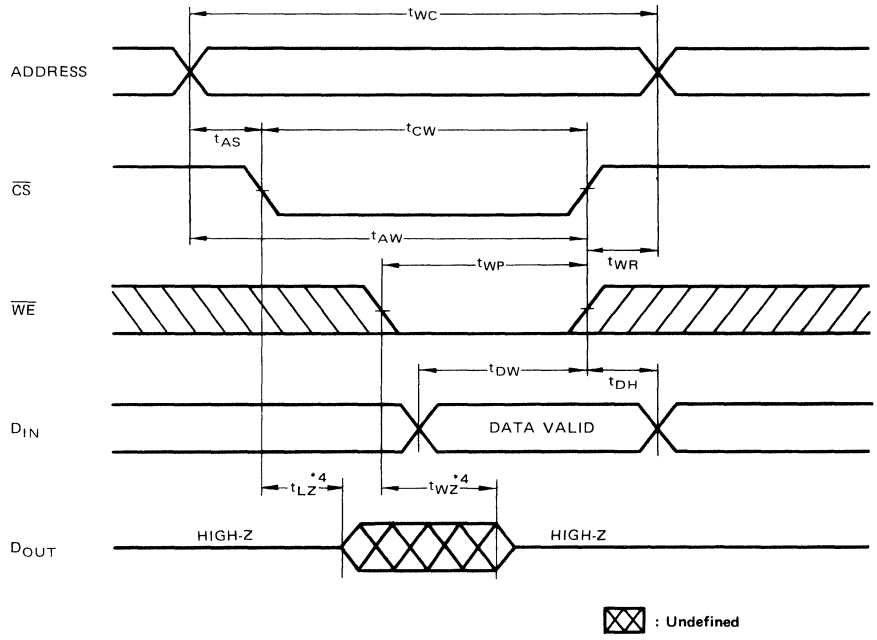


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transition to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

1

WRITE CYCLE TIMING DIAGRAM *1*2

WRITE CYCLE: $\overline{CS}$ CONTROLLED*3



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transistion.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transistion to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

TYPICAL CHARACTERISTICS CURVES

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Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

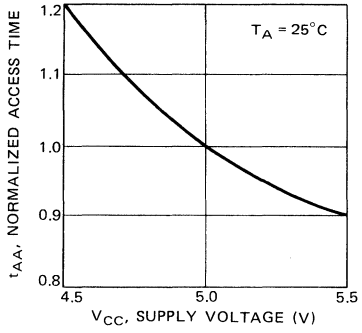

Fig. 4 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

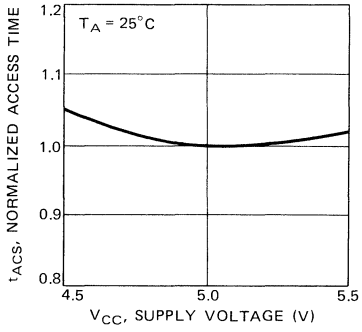

Fig. 5 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

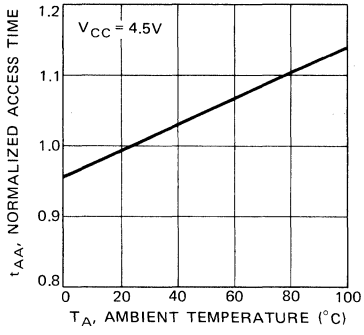

Fig. 6 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

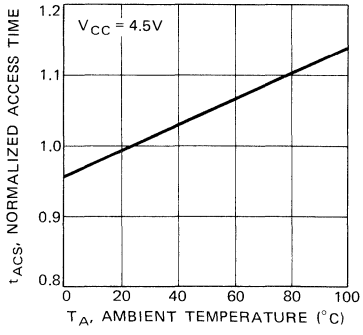

Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

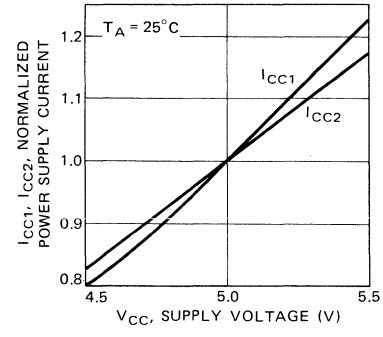

Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

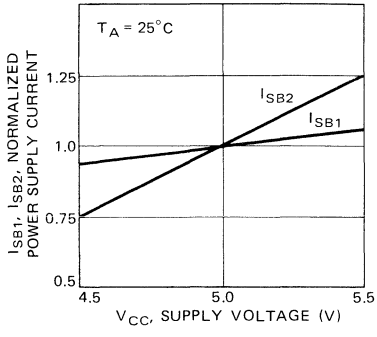

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Fig. 9 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

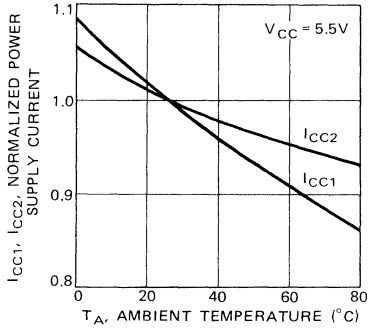

Fig. 10 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

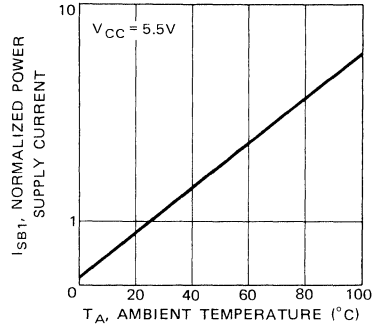

Fig. 11 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

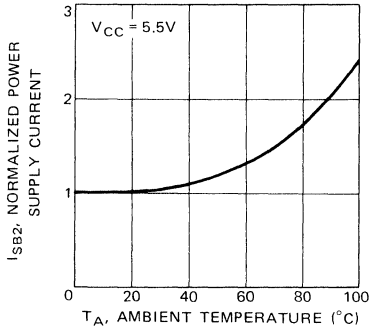

Fig. 12 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

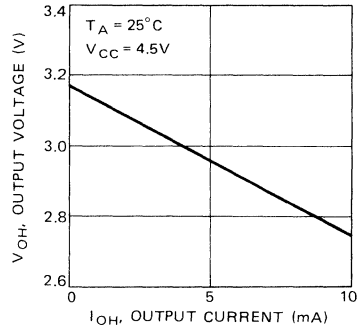

Fig. 13 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

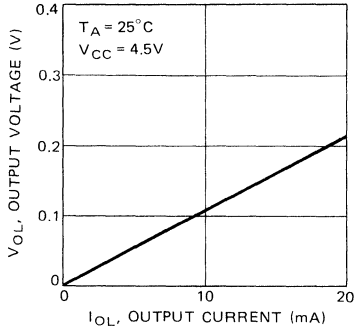

Fig. 14 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

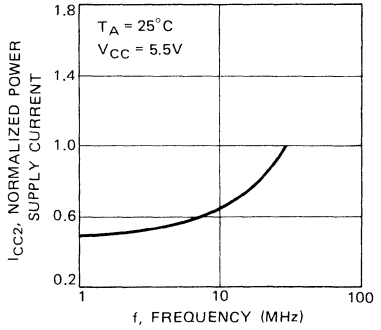

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Fig. 15 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

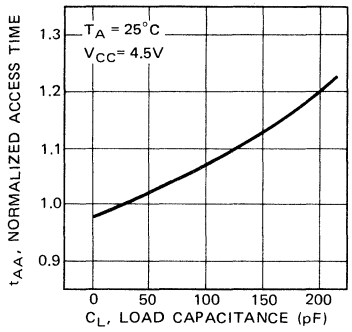
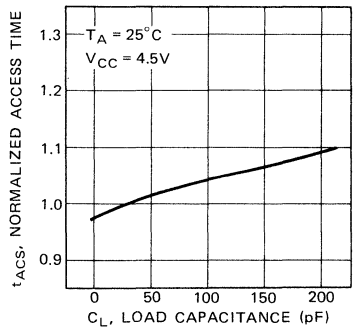


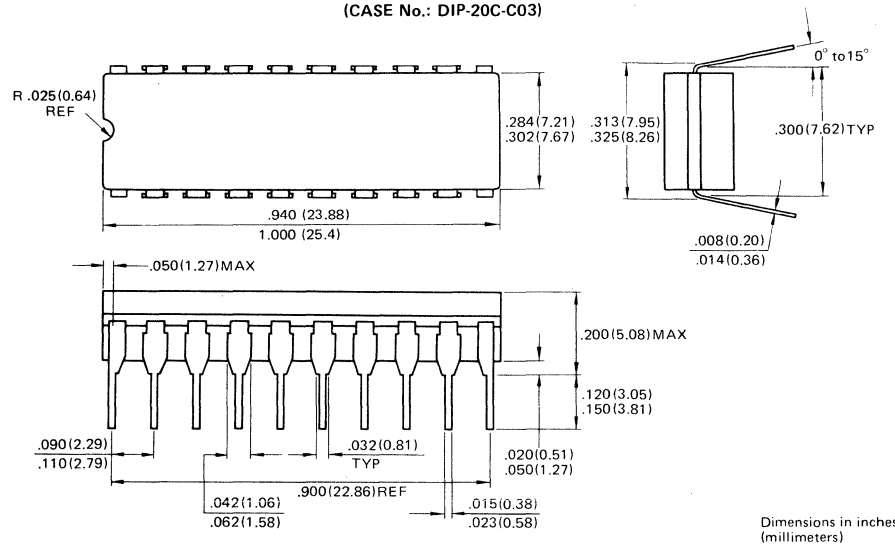
Fig. 16 — NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: CZ)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

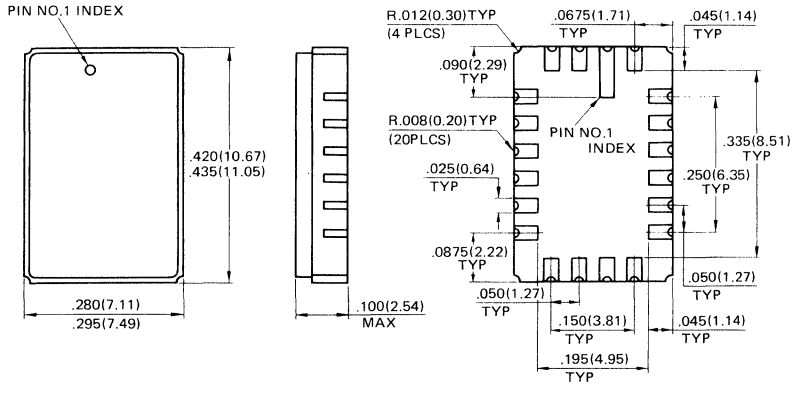


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: TV)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



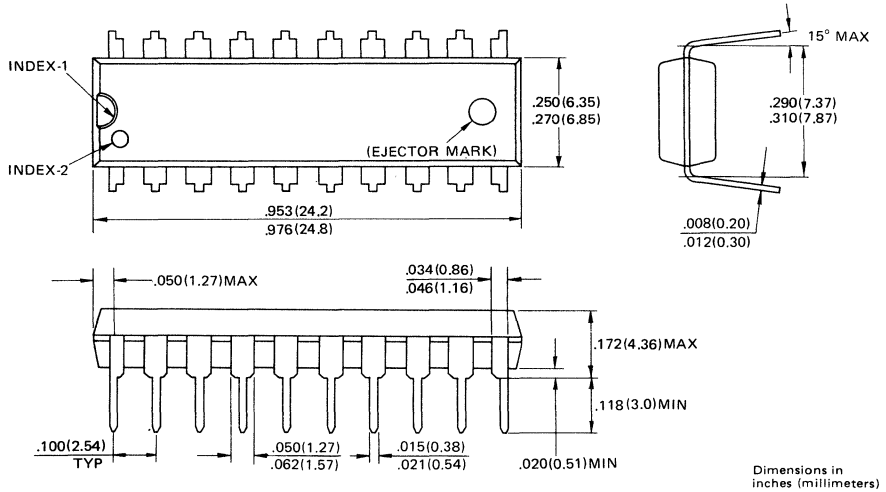
Dimension in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: P)

1

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



Dimensions in inches (millimeters)

FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB81C68A-25
MB81C68A-30
MB81C68A-35

4K x 4 (16,384-BIT) STATIC RANDOM ACCESS MEMORY WITH SUPER HIGH SPEED AND AUTOMATIC POWER DOWN

January 1988
Edition 2.0

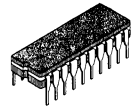
1

The Fujitsu MB 81C68A is 4096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and all pins are TTL compatible and a single 5 volts power supply is required.

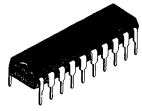
A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

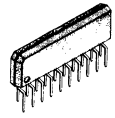
- Organization: 4096 words x 4 bits
- Static operation: No clocks or timing strobe required
- Fast access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB 81C68A-25)
  $t_{AA} = t_{ACS}$ = 30 ns max. (MB 81C68A-30)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB 81C68A-35)
- Low power consumption: 385 mW max. (Active)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 20-pin DIP (Suffix -P(plastic)/Suffix: -Z(cerdip))
- Standard 20-pad LCC (Suffix: -TV)
- Standard 20-pin ZIP (Suffix: -PSZ)



CERAMIC PACKAGE
CERDIP
(DIP-20C-C03)

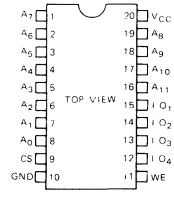


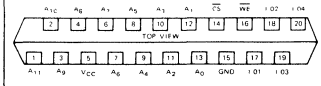
PLASTIC PACKAGE
(DIP-20P-M01)



PLASTIC PACKAGE
(ZIP-20P-M01)

PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

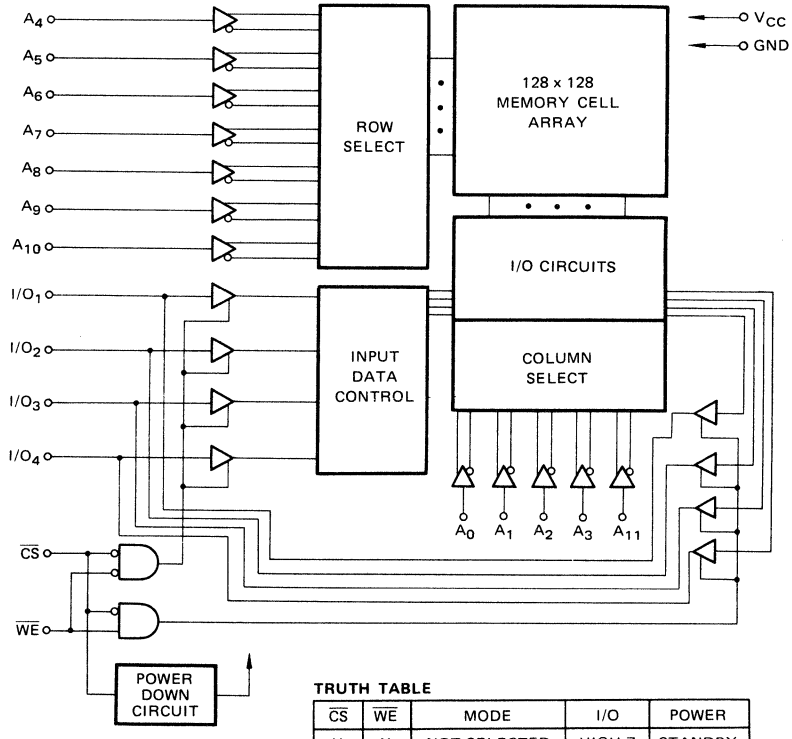
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on Any Pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on Any I/O Pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	−65 to +150	°C
	PLASTIC		−45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB 81C68A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note: * -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

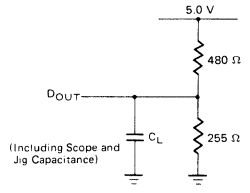
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}	I_{LO}	-10		10	μA
Active (DC) Supply Current	I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, Cycle = Min	I_{CC2}		40	70	mA
Standby Supply Current	$\overline{CS}$ = V_{CC} – 0.2V, $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$ – 0.2V	I_{SB1}		0.5	15	mA
Standby Supply Current	$\overline{CS}$ = V_{IH}	I_{SB2}		10	25	mA
Output Low Voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

1

AC TEST CONDITION

Input Pulse Levels:	0 V to 3.0 V
Input Pulse Rise and Fall Times:	5 ns (Transient Time between 0.8 V and 2.2 V)
Timing Reference Levels:	Input : 1.5 V Output: 1.5 V

Output Load: Fig. 2



C_L = 30 pF
C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

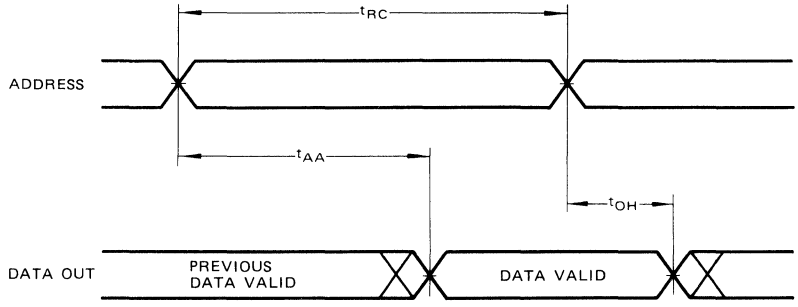
Parameter	Symbol	MB 81C68A-25		MB 81C68A-30		MB 81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time*2	t_{AA}		25		30		35	ns
Chip Select Access Time*3	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*4	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*4	t_{HZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500 mV from steady state voltage.

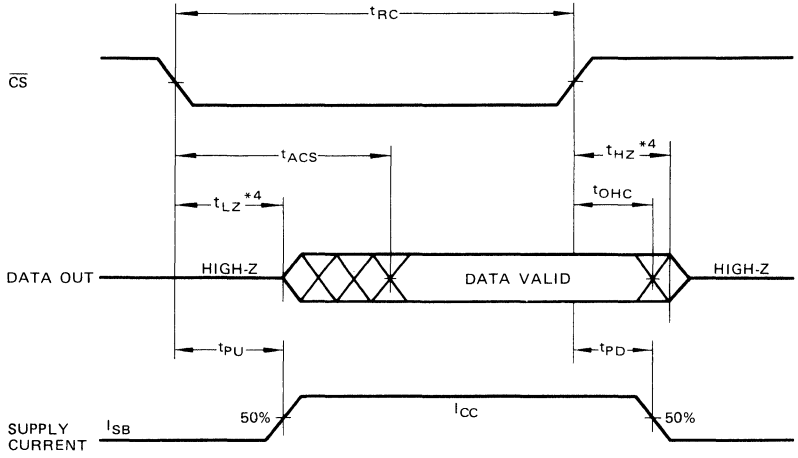
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2



READ CYCLE: $\overline{CS}$ CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500 mV from steady state voltage.

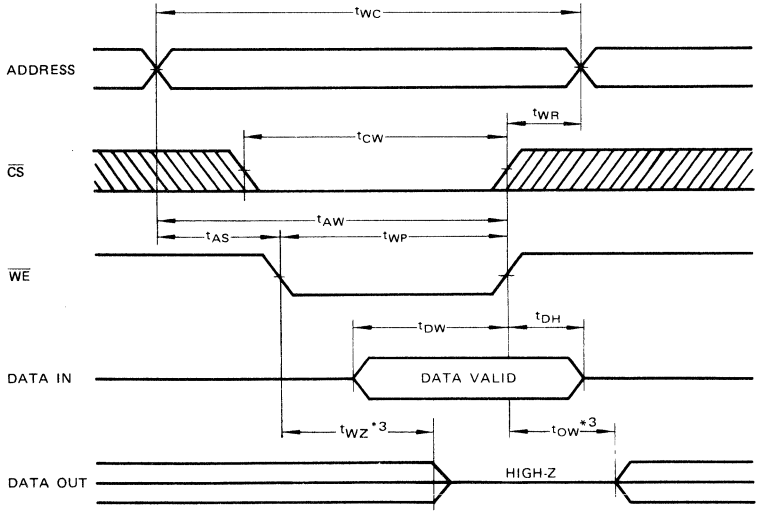
1

WRITE CYCLE*1*2

Parameter	Symbol	MB 81C68A-25		MB 81C68A-30		MB 81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*3	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*3	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{WE}$ CONTROLLED*1*2

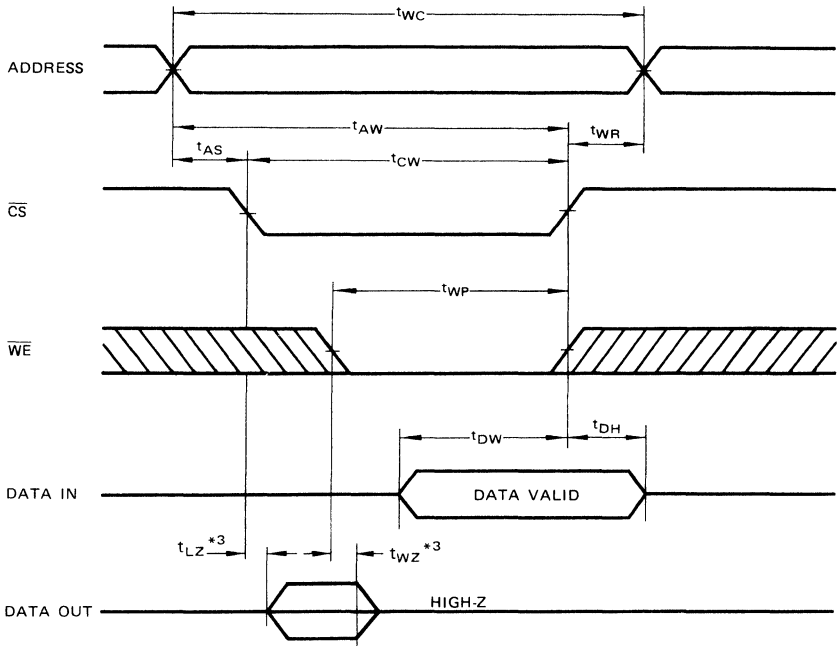


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500 mV from steady state voltage.

1

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500 mV from steady state voltage.

TYPICAL CHARACTERISTICS CURVES

1

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

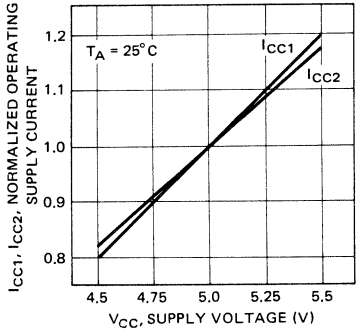


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

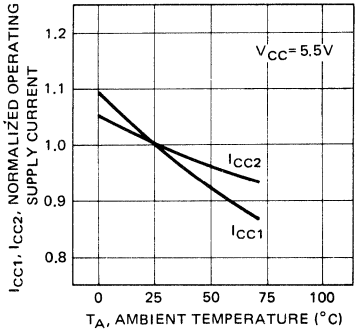


Fig. 5 STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

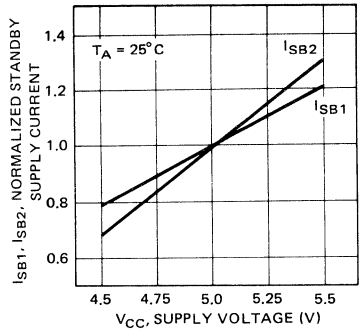


Fig. 6 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

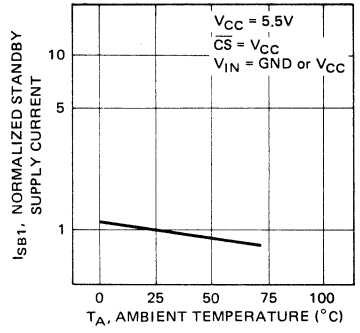


Fig. 7 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

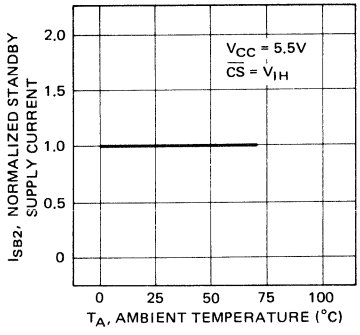
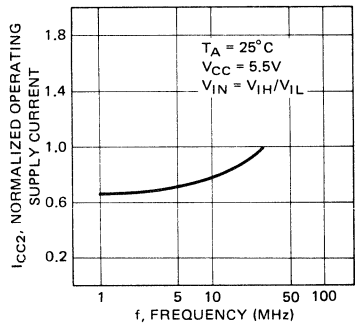


Fig. 8 OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 9 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

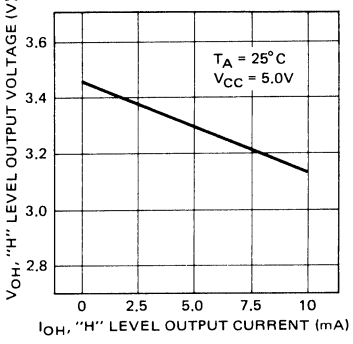


Fig. 10 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

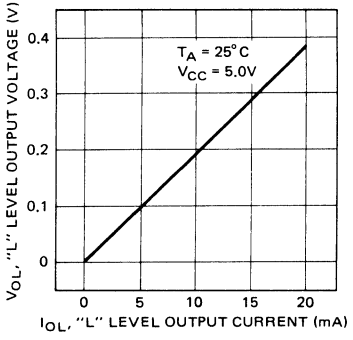


Fig. 11 ACCESS TIME vs. SUPPLY VOLTAGE

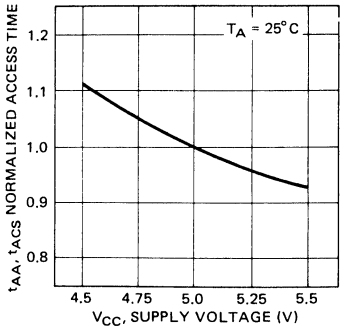


Fig. 12 ACCESS TIME vs. AMBIENT TEMPERATURE

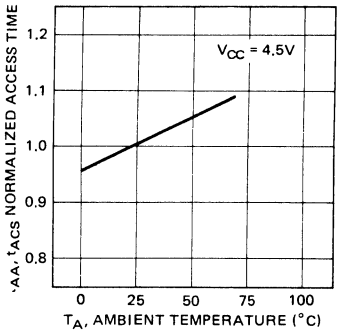
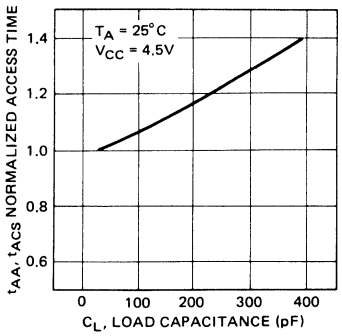


Fig. 13 ACCESS TIME vs. LOAD CAPACITANCE

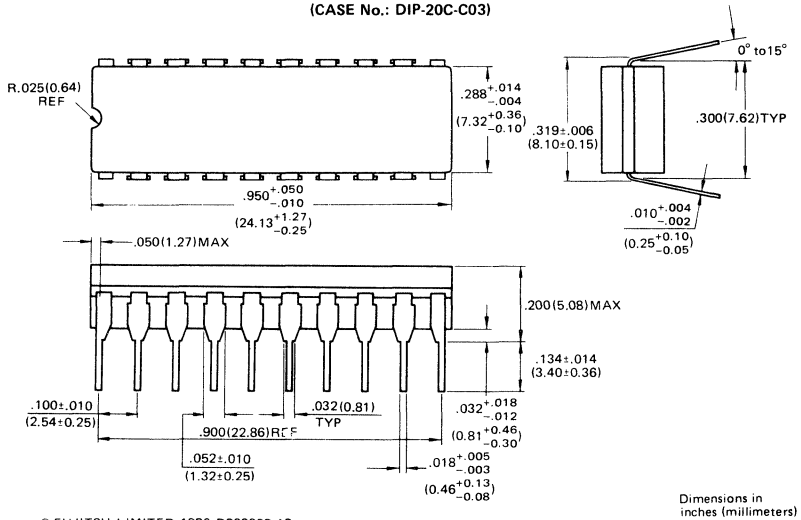


1

PACKAGE DIMENSIONS

(Suffix: -Z)

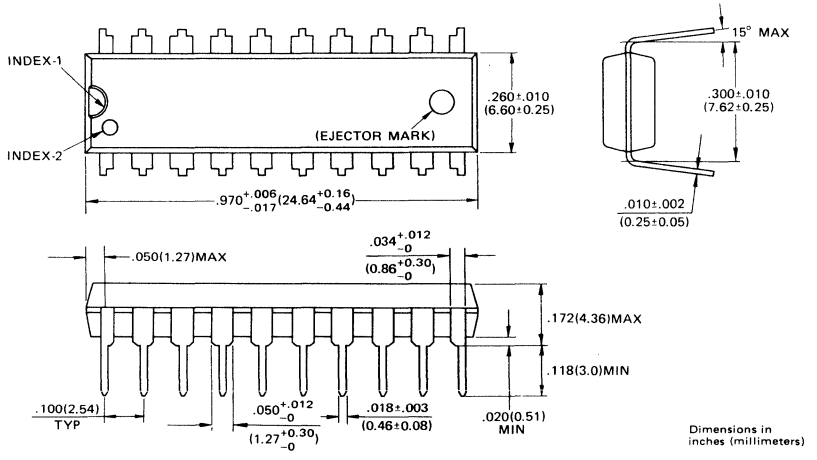
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in inches (millimeters)

(Suffix: -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)

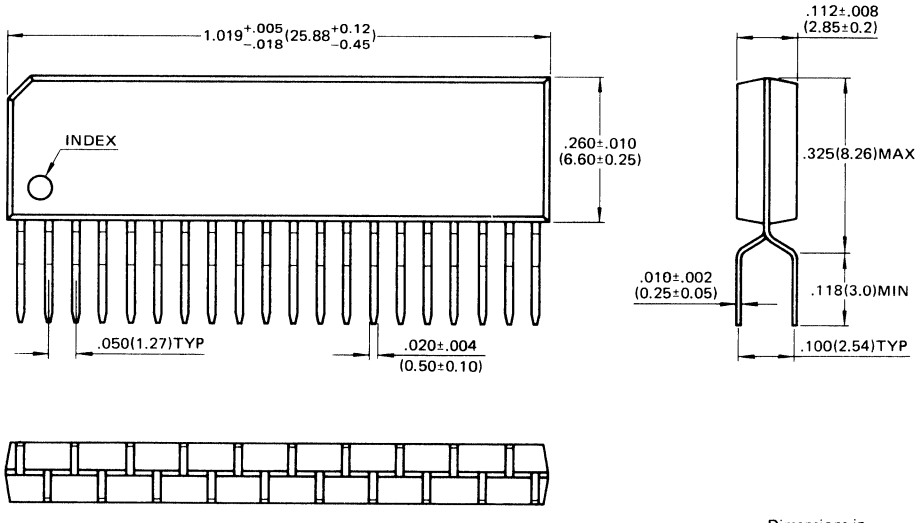


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PSZ)

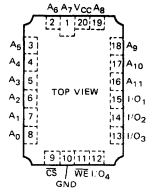
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)

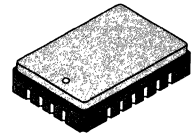


Dimensions in
inches (millimeters)

1

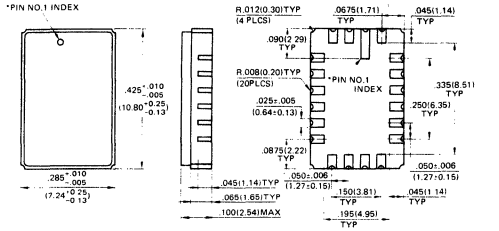
(Suffix: -TV)





CERAMIC PACKAGE
LCC
(LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

FUJITSU

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB81C69A-25
MB81C69A-30
MB81C69A-35

January 1988
Edition 2.0

1

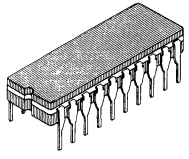
4K x 4 (16,384-BIT) STATIC RANDOM ACCESS MEMORY WITH SUPPER HIGH SPEED

The Fujitsu MB 81C69A is 4096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and all pins are TTL compatible and a single 5 volts power supply is required.

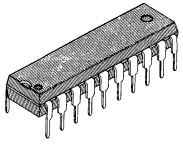
A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied.

All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 4096 words x 4 bits
- Static operation: No clocks or timing strobe required
- Fast access time: t_{AA} = 25 ns max, t_{ACS} = 15 ns max (MB 81C69A-25)
  t_{AA} = 30 ns max, t_{ACS} = 18 ns max (MB 81C69A-30)
  t_{AA} = 35 ns max, t_{ACS} = 20 ns max (MB 81C69A-35)
- Low power consumption: 385 mW max. (Active)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion
- All inputs and outputs have protection against static charge
- Standard 20-pin DIP (Suffix: -P(plastic)/Suffix: -Z(cerdip))
- Standard 20-pad LCC (Suffix: -TV)

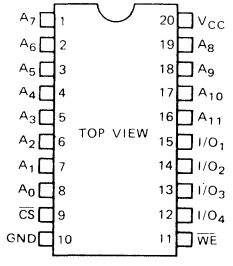


CERAMIC PACKAGE
CERDIP
(DIP-20C-C03)



PLASTIC PACKAGE
(DIP-20P-M01)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

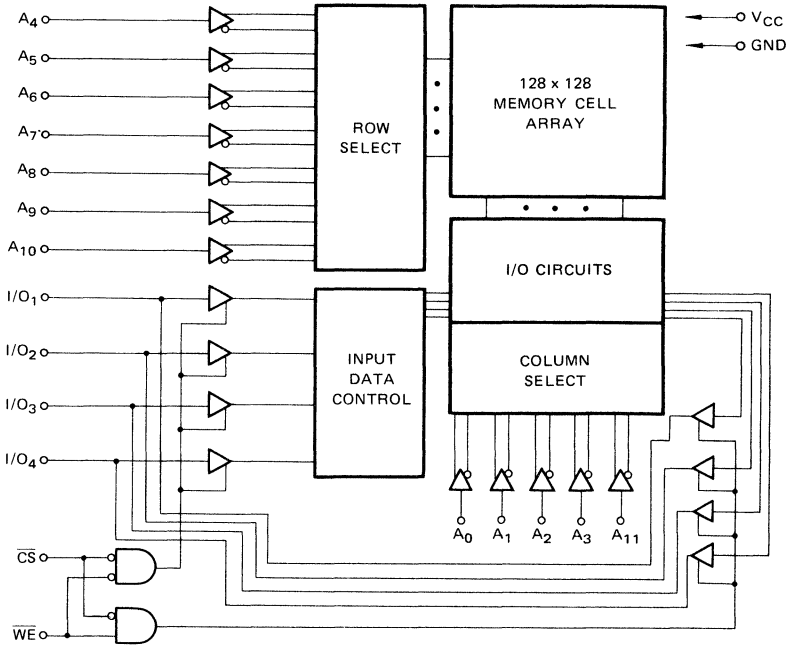
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on Any Pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Volage on Any I/O Pin with respect to GND		V_{OUT}	-0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C69A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	NOT SELECTED	HIGH-Z
L	L	WRITE	D_{IN}
L	H	READ	D_{OUT}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note: * -2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = -0.5 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

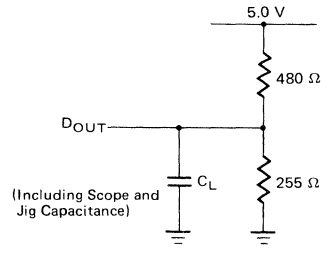
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	-10		10	μA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0 mA, Cycle = Min	I_{CC2}		40	70	mA
Output Low Voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V

1

AC TEST CONDITION

Input Pulse Levels	0 V to 3.0 V
Input Pulse Rise and Fall Times:	5 ns (Transient Time between 0.8 V and 2.2 V)
Timing Reference Levels:	Input : 1.5 V
	Output: 1.5 V

Output Load: Fig. 2



C_L = 30 pF
C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

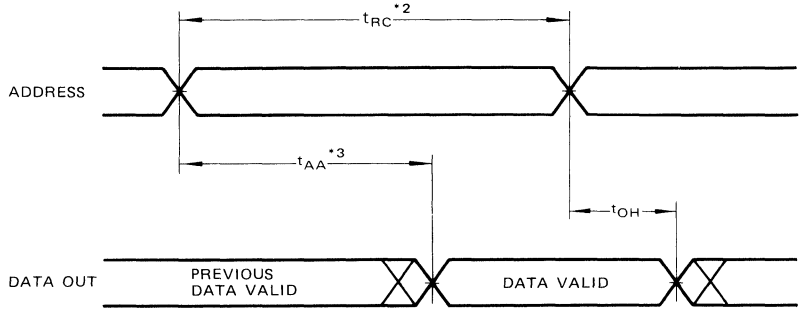
Parameter	Symbol	MB 81C69A-25		MB 81C69A-30		MB 81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4	t_{ACS}		15		18		20	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*5	t_{LZ}	0		0		0		ns
Chip Deselection to Output in High-Z*5	t_{HZ}		10		13		15	ns

Note: *1 $\overline{WE}$ is high for Raed cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state Voltage with Load II in Fig. 2.

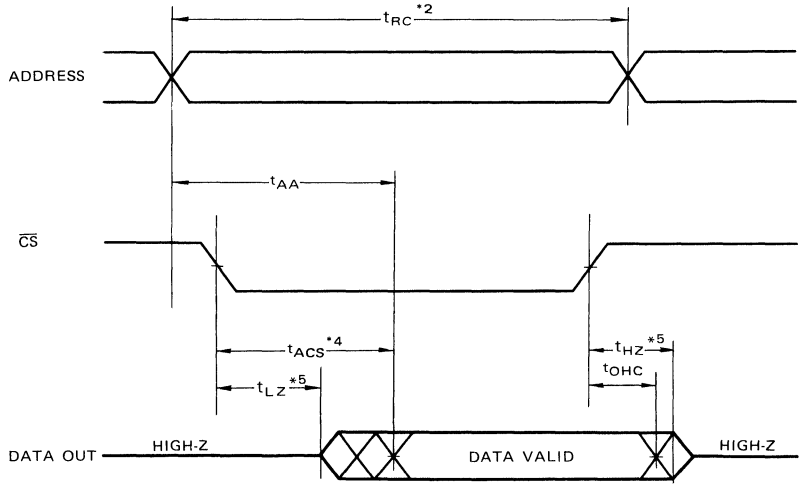
1

READ CYCLE TIMING DIAGRAM *1

READ CYCLE: ADDRESS CONTROLLED



READ CYCLE: $\overline{CS}$ CONTROLLED *3



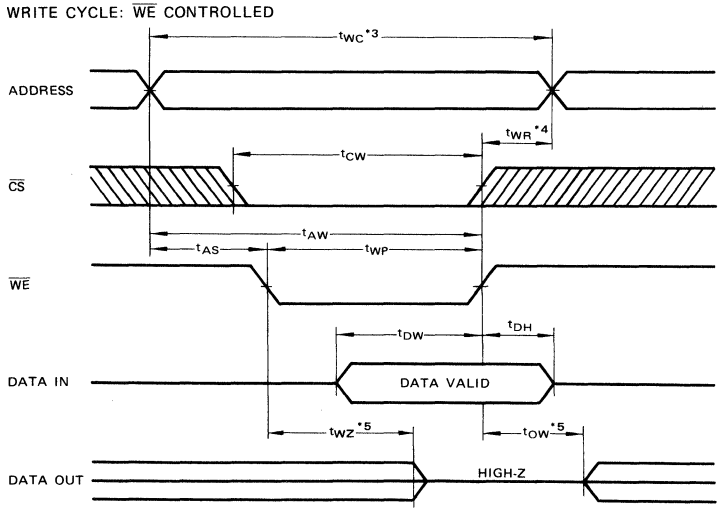
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500 mV from steady state voltage with Lead II in Fig. 2.

1

WRITE CYCLE *1*2

Parameter	Symbol	MB 81C69A-25		MB 81C69A-30		MB 81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time*4	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2

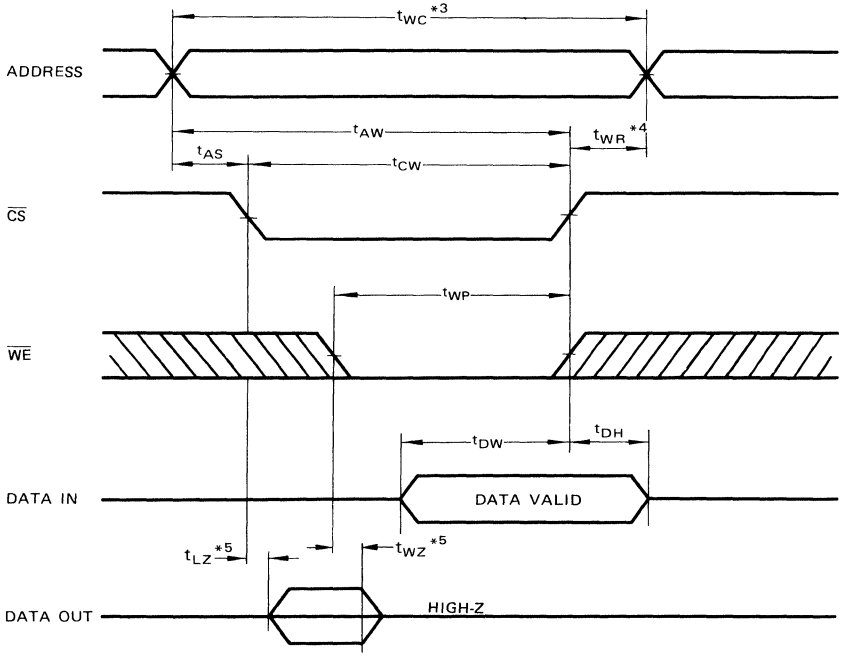


Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simulatneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified at the point of ±500mV from steady state voltage, with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

TYPICAL CHARACTERISTICS CURVES

1

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

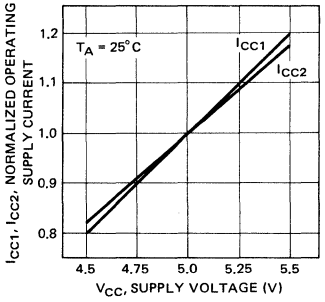


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

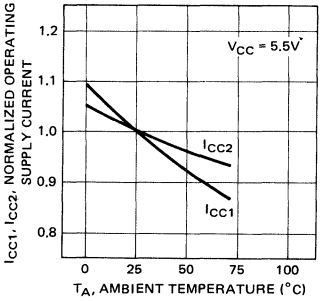


Fig. 5 OPERATING SUPPLY CURRENT vs. FREQUENCY

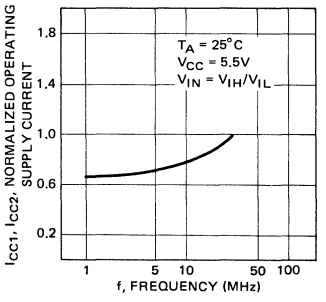


Fig. 6 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

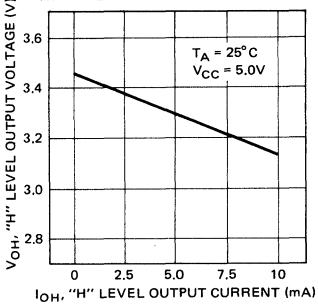


Fig. 7 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

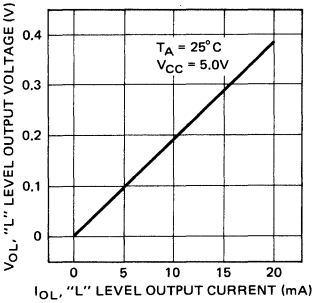


Fig. 8 ACCESS TIME vs. SUPPLY VOLTAGE

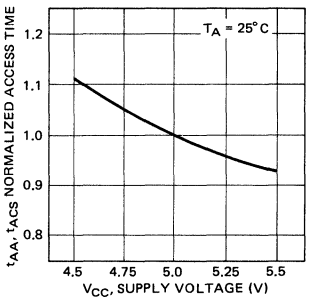


Fig. 9 ACCESS TIME vs. AMBIENT TEMPERATURE

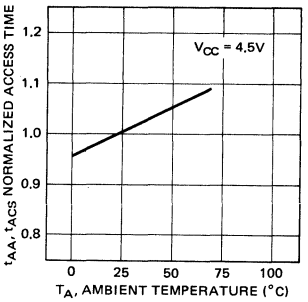
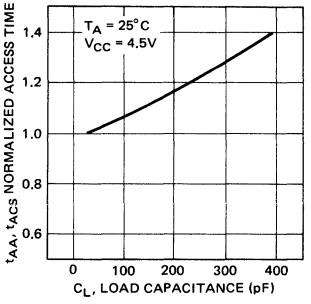


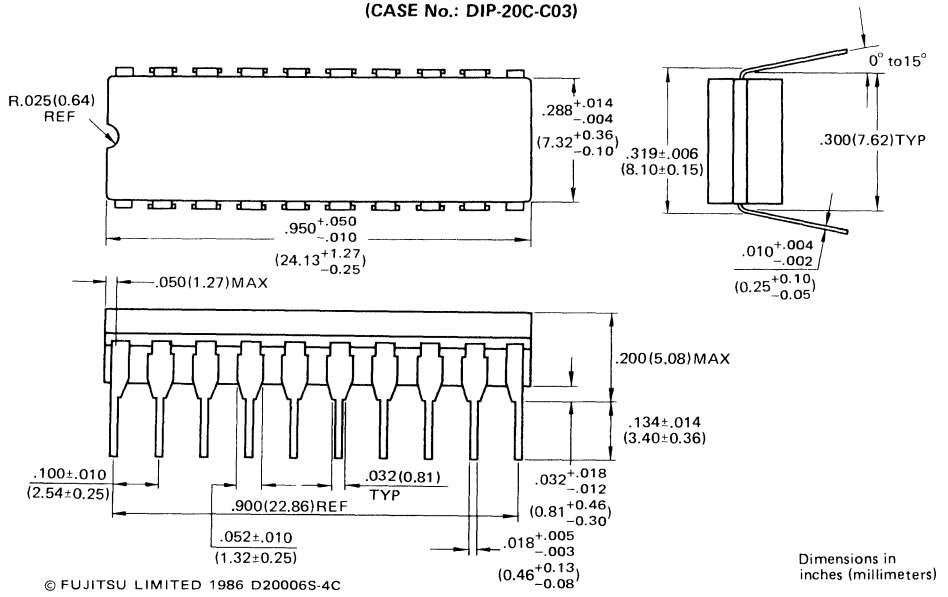
Fig. 10 ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: -Z)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



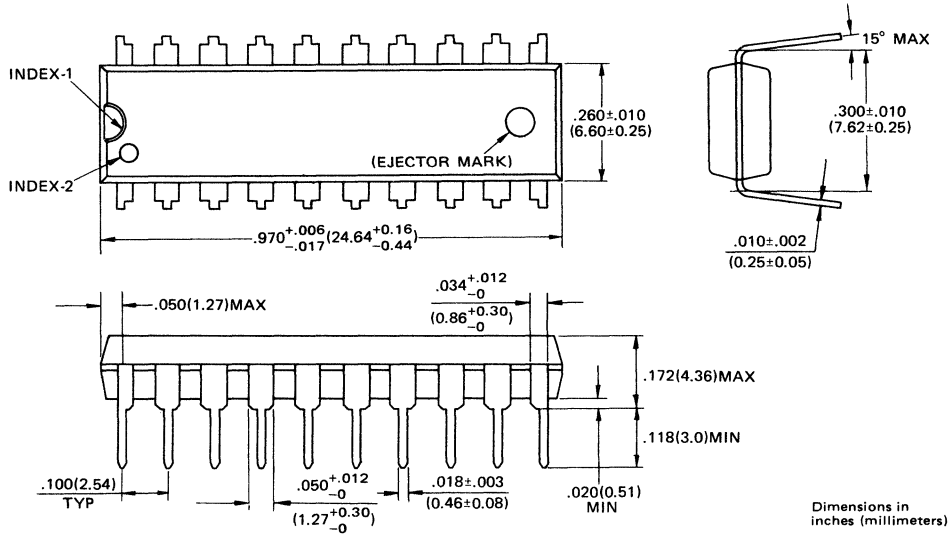
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

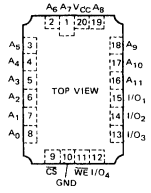
20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)

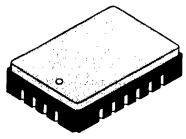


1

PACKAGE DIMENSIONS

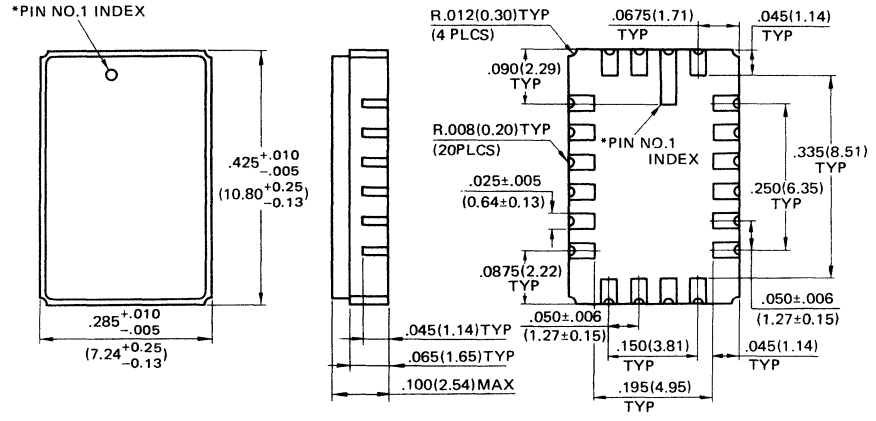
CERAMIC LCC (Suffix: -TV)





CERAMIC PACKAGE
(LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in inches (millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

1

FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

MB81C71A-25
MB81C71A-35

February 1988
Edition 2.0

1

65,536 WORDS X 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

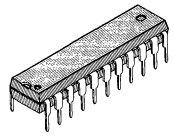
The Fujitsu MB 81C71A is 65,536 words x 1 bit static random access memory fabricated with a CMOS technology.
It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.
The MB 81C71A is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.
MB 81C71A is compatible with TTL logic families in all respects; input, output and a single +5 V supply.

- Organization : 65,536 words x 1 bit
- Static operation : No clocks or refresh required
- Fast access time : $t_{AA} = t_{ACS}$ = 25 ns (MB 81C71A-25)
  $t_{AA} = t_{ACS}$ = 35 ns (MB 81C71A-35)
- Single +5 V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 22-pin DIP (300 mil) (Suffix: P)
- Standard 22-pad LCC (Suffix: CV)
- Standard 24-pin SOJ (300 mil) : (Suffix : PJ)

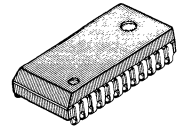
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

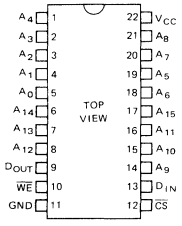


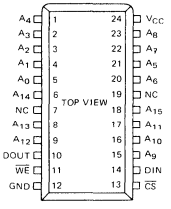
PLASTIC PACKAGE
DIP-22P-M04



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT

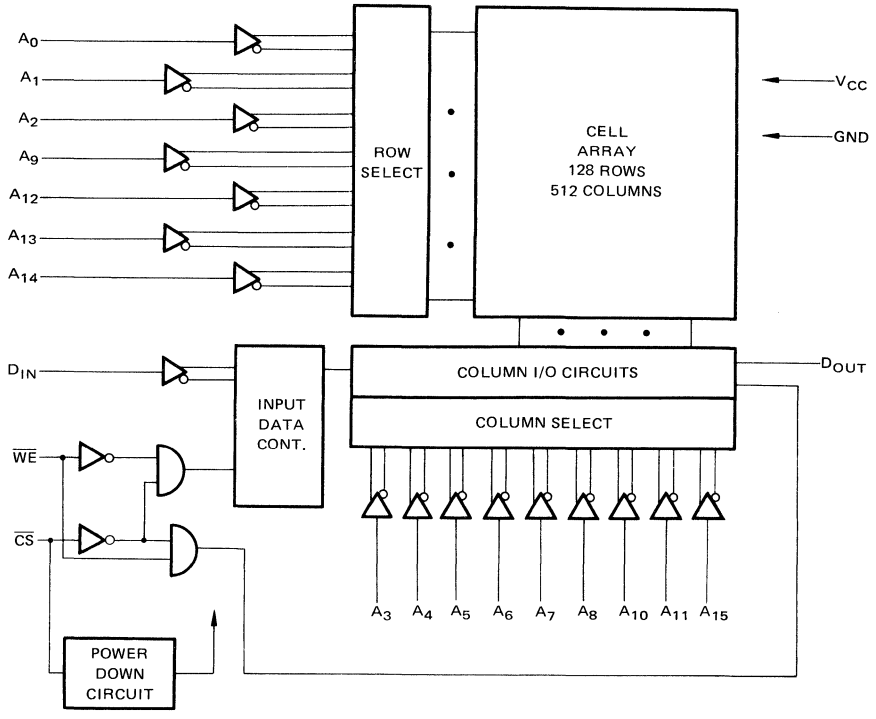




This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1– MB 81C71A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance (V_{IN} = 0 V)	C_{IN}		7	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		7	pF

1

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min, for pulse width less than 20 ns. (V_{IL} Min = -0.5 V at DC Level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

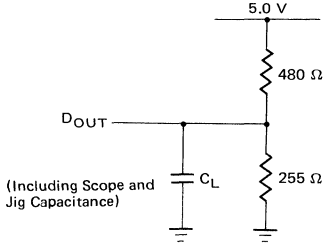
Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current	V_{IN} = 0 V to V_{CC} V_{CC} = Max.	I_{LI}	-10		10	μA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 V to 4.5 V V_{CC} = Max.	I_{LO}	-10		10	μA
Operating Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max. D_{OUT} = Open, Cycle = Min.	I_{CC}			80	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS} \geqq V_{CC}$ -0.2 V $V_{IN} \leqq$ 0.2 V or $V_{IN} \geqq V_{CC}$ -0.2 V	I_{SB1}			10	mA
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}			20	mA
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = -4 mA	V_{OH}	2.4			V
Peak Power on Current	V_{CC} = 0 V to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	I_{PO}			30	mA

1

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise And Fall Times: 5 ns
- Timing Measurement Reference Levels: Input : 1.5 V
  Output: 1.5 V

- Output Load:



Load I: C_L = 30 pF
Load II: C_L = 5 pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

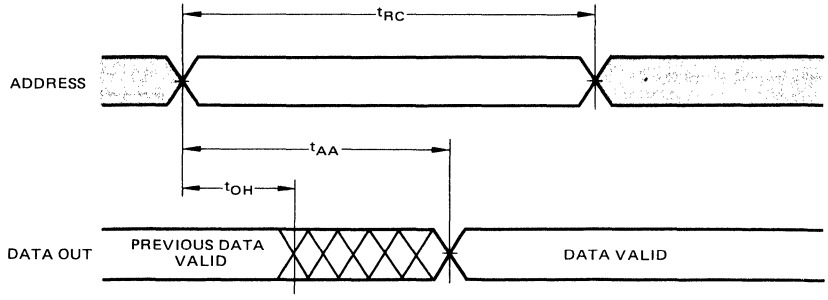
Parameter	Symbol	MB 81C71A-25		MB 81C71A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		35		ns
Address Access Time*3	t_{AA}		25		35	ns
Chip Select Access Time*4*5	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z*6*7	t_{LZ}	5		5		ns
Chip Deselection to Output in High-Z*6*7	t_{HZ}	0	10	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0		0		ns
Chip Deselction to Power Down time	t_{PD}		20		30	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This parameter is measured with specified loading Load II in Fig. 2.

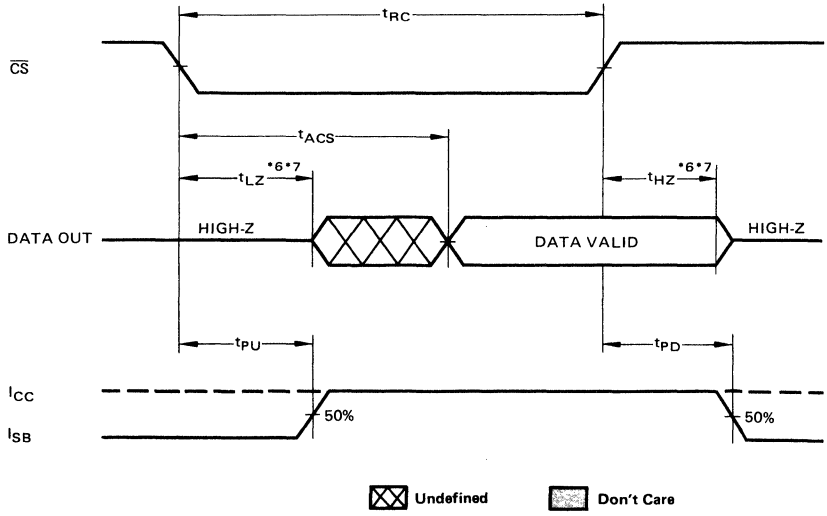
1

READ CYCLE TIMING DIAGRAM*1*2

READ CYCLE: ADDRESS CONTROLLED*3



READ CYCLE: $\overline{CS}$ CONTROLLED*4*5



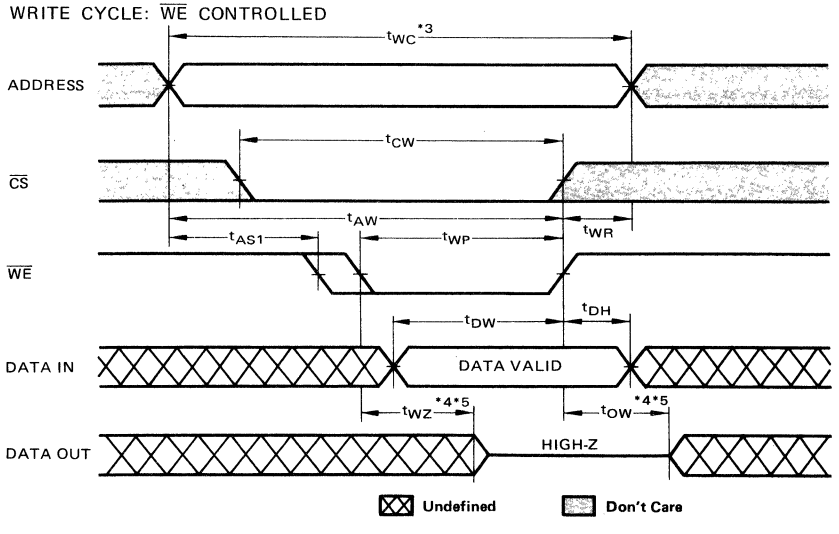
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage.
*7 This parameter is measured with specified loading Load II in Fig. 2.

1

WRITE CYCLE*1*2

Parameter	Symbol	MB 81C71A-25		MB 81C71A-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	20		30		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Address Setup Time	t_{AS1}	0		0		ns
Address Setup Time	t_{AS2}	0		0		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Write Recovery Time	t_{WR}	2		2		ns
Data Hold Time	t_{DH}	2		2		ns
Write Enable to Output in High-Z*4*5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write*4*5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM*1*2

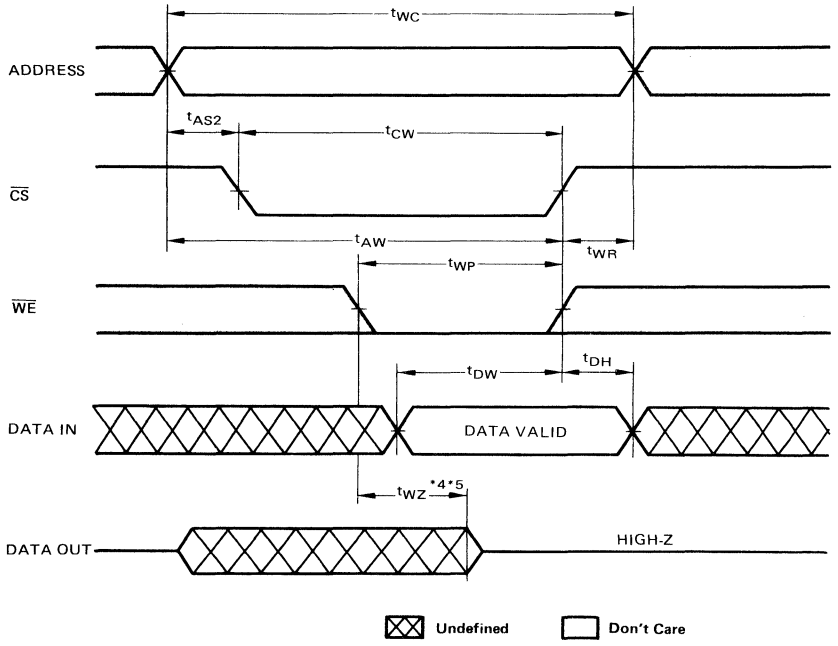


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM *1*2

WRITE CYCLE: $\overline{CS}$ CONTROLLED *3



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

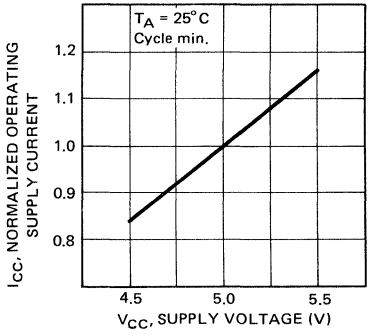


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

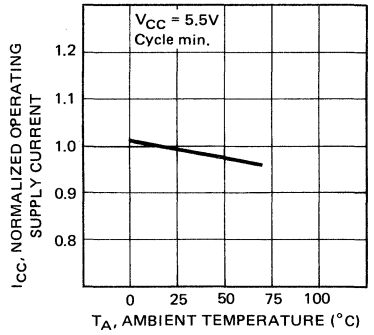


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

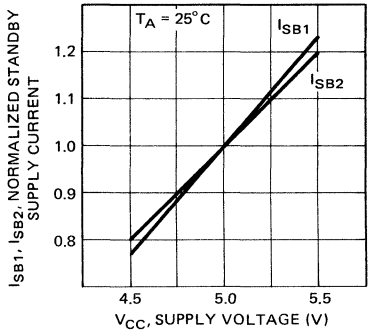


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

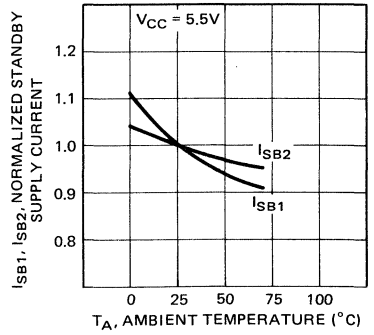
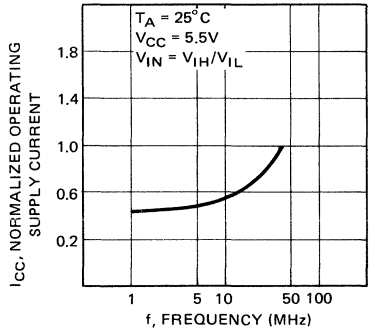


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

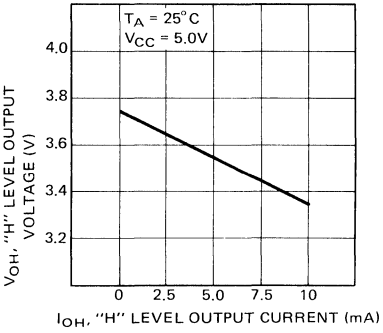


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

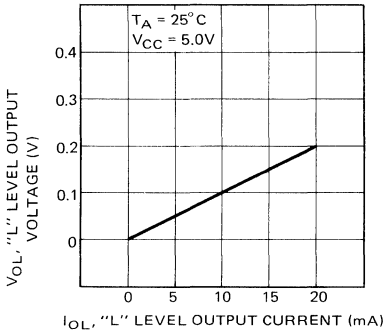


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

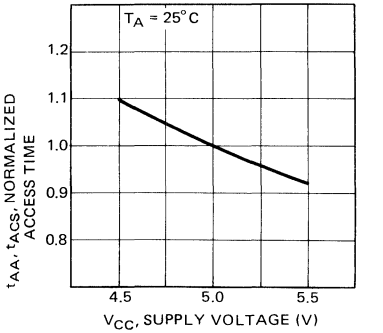


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

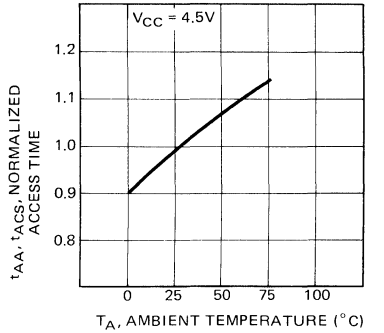
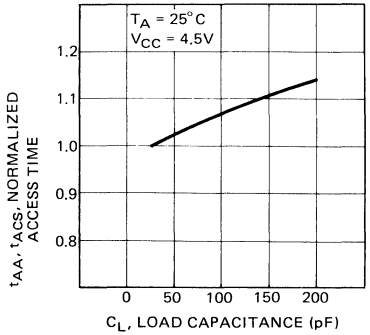


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE

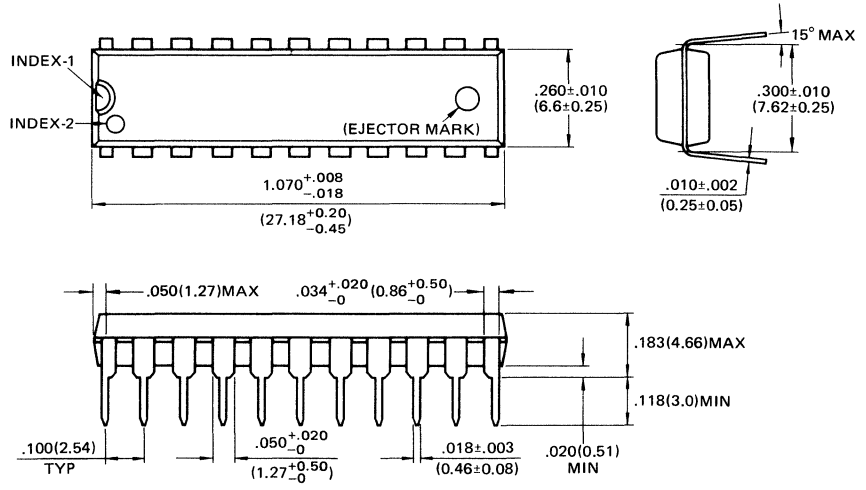


PACKAGE DIMENSIONS

(Suffix: -P)

1

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



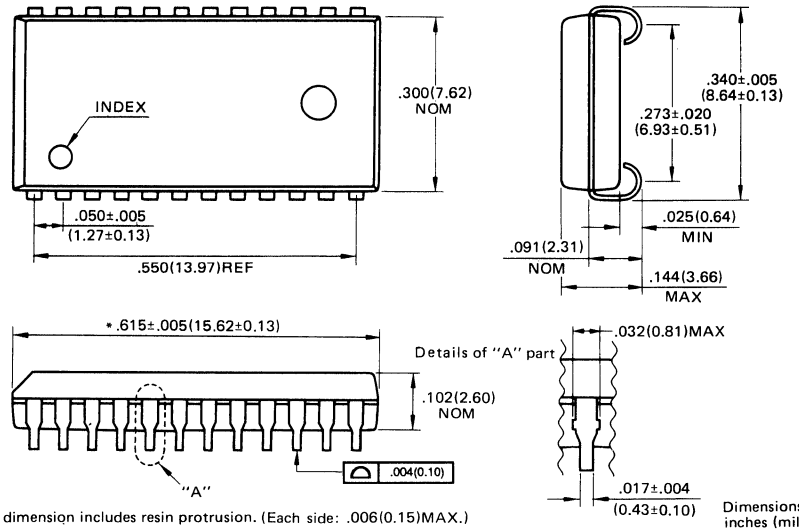
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

(Suffix: -PJ)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



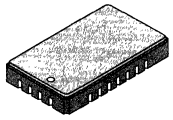
Dimensions in inches (millimeters)

* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

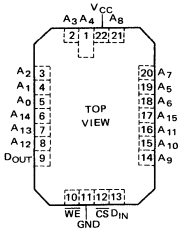
PACKAGE DIMENSIONS

(Suffix: -CV)

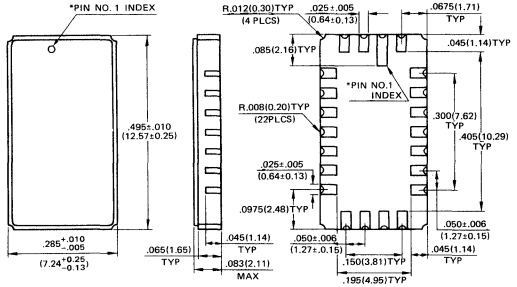
1



CERAMIC PACKAGE
LCC-22C-A01



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

MB81C74-25
MB81C74-35

December 1987
Edition 2.0

1

16K x 4 BIT (65,536-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C74 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicongate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

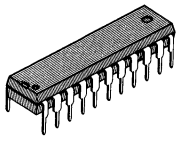
The MB 81C74 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 16,384 words x 4 bits
- Fast access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB 81C74-25)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB 81C74-35)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply ±10% tolerance
- Low power standby: 440 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 22-pin DIP (300 mil): Suffix: P
- Standard 22-pad LCC : Suffix: CV

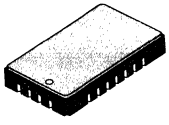
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-3.5 to +7.0	V
Output Voltage		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

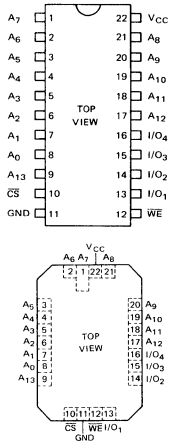


PLASTIC PACKAGE
DIP-22P-M04



CERAMIC PACKAGE
LCC-22C-A01

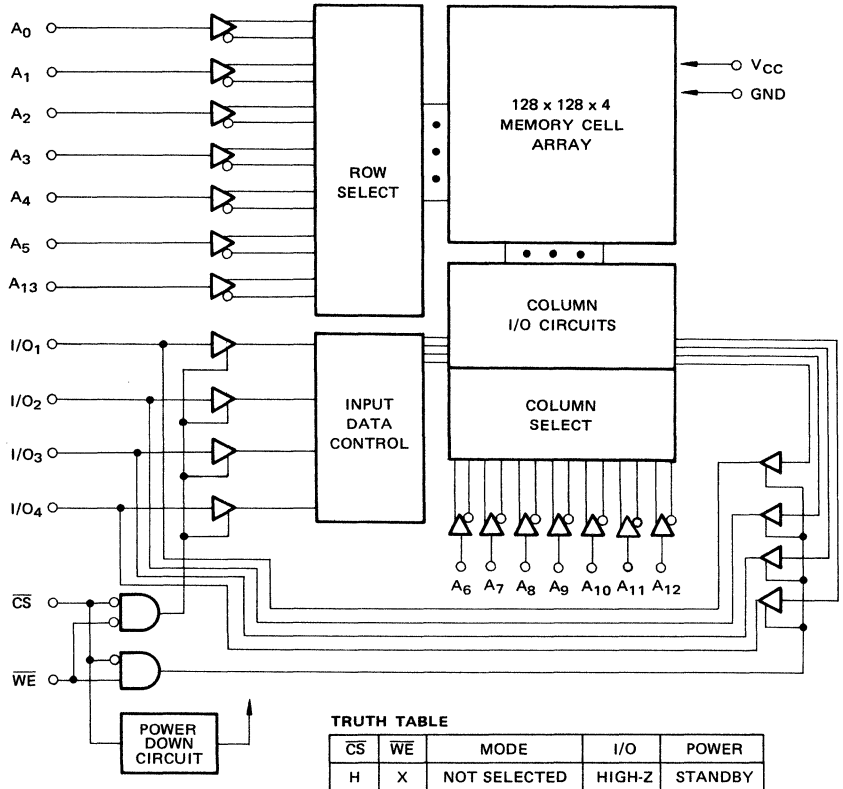
PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C74 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

1

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 -2.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = -0.5 V at DC level)

DC CHARACTERISTICS

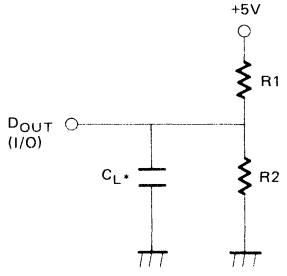
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		10	mA	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		20	mA	$\overline{CS} = V_{IH}$
Active Supply Current	I_{CC1}		60	mA	I_{OUT} = 0 mA, $\overline{CS} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}
Operating Supply Current	I_{CC2}		80	mA	Cycle = Min., I_{OUT} = 0 mA
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-10	10	μA	$\overline{CS} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA

Note: All voltages are referenced to GND

Fig. 2 — AC TEST CONDITIONS

- Output Load



- Input Pulse Levels: 0 V to 3.0 V
- Input Pulse Rise & Fall Times: 5 ns (Transient between 0.8 V and 2.2 V)
- Timing Reference Levels: Input: 1.5 V
  Output: 1.5 V

* Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, and t_{WHZ}
Load II	480Ω	255Ω	5 pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}

1

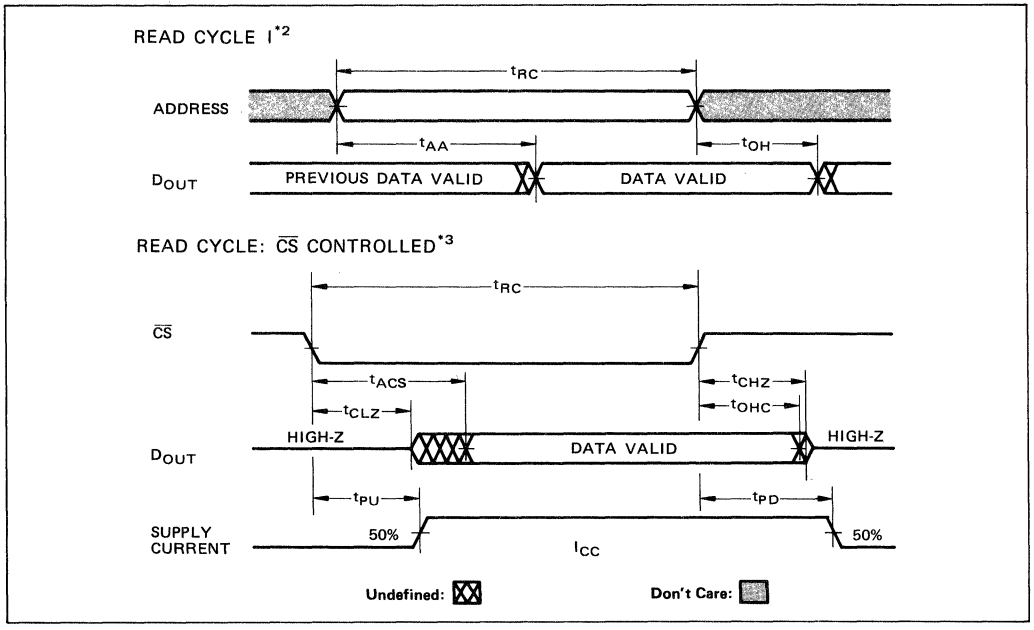
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

Parameter	Symbol	MB 81C74-25		MB 81C74-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time[*2]	t_{AA}		25		35	ns
$\overline{CS}$ Access Time[*3]	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns
Chip Selection to Output Low-Z[*4*5]	t_{CLZ}	5		5		ns
Chip Deselection to Output High-Z[*4*5]	t_{CHZ}		10		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM[*1]



Note:

*1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500 mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

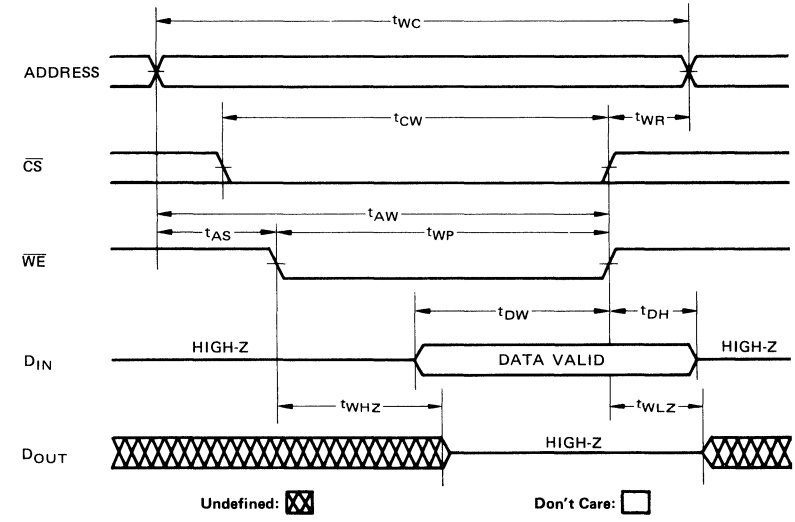
1

WRITE CYCLE*1

Parameter	Symbol	MB 81C74-25		MB 81C74-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Chip Select to End of Write	t_{CW}	20		30		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$*3*4	t_{WHZ}		10		15	ns
Output Low-Z from $\overline{WE}$*3*4	t_{WLZ}	0	10	0	15	ns

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE I: $\overline{WE}$ CONTROLLED*1*2

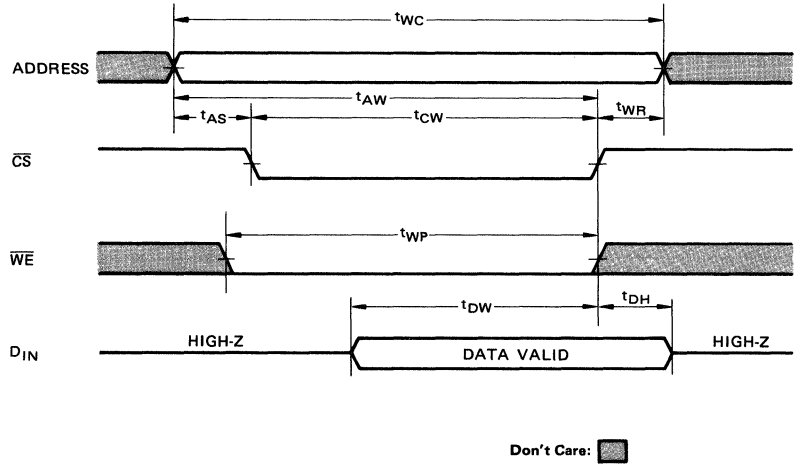


Note:

*1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500 mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note:

*1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

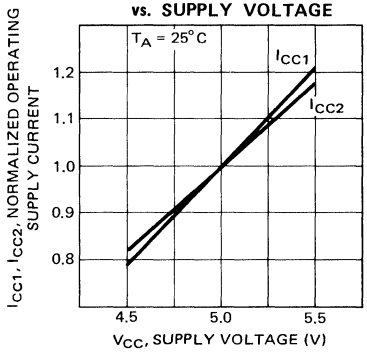


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

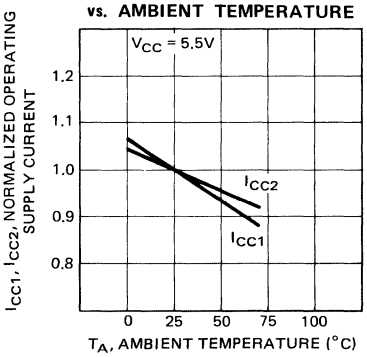


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

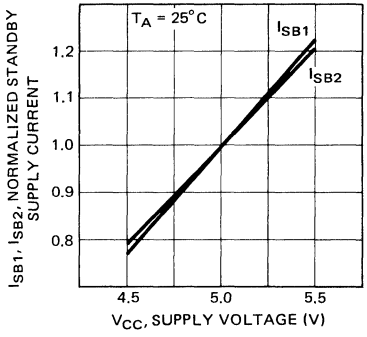


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

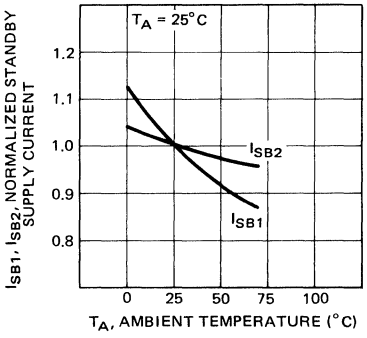
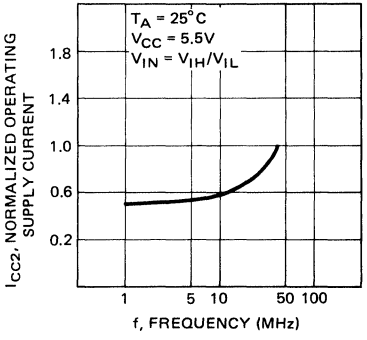


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



1

TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

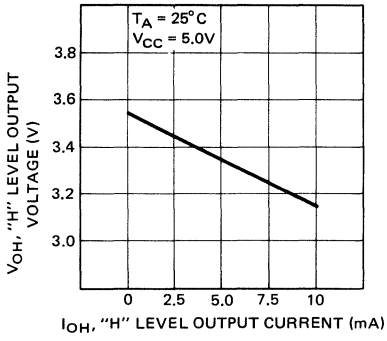


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

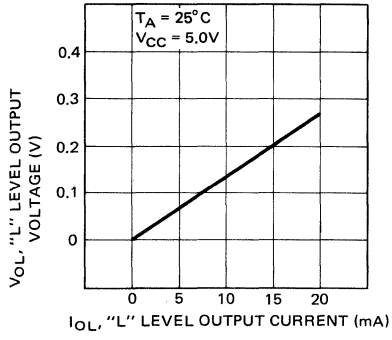


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

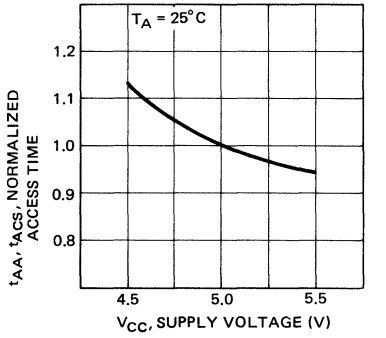


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

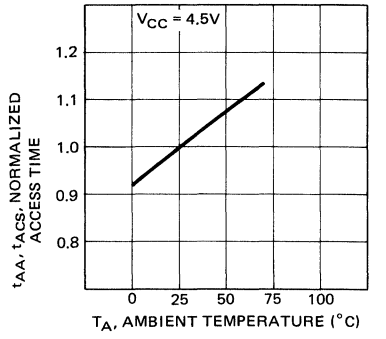
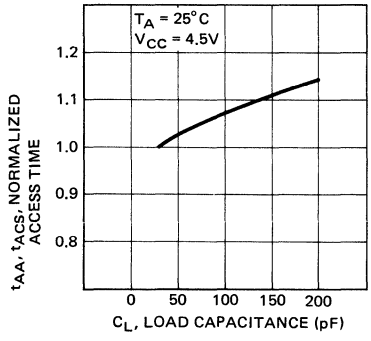


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE

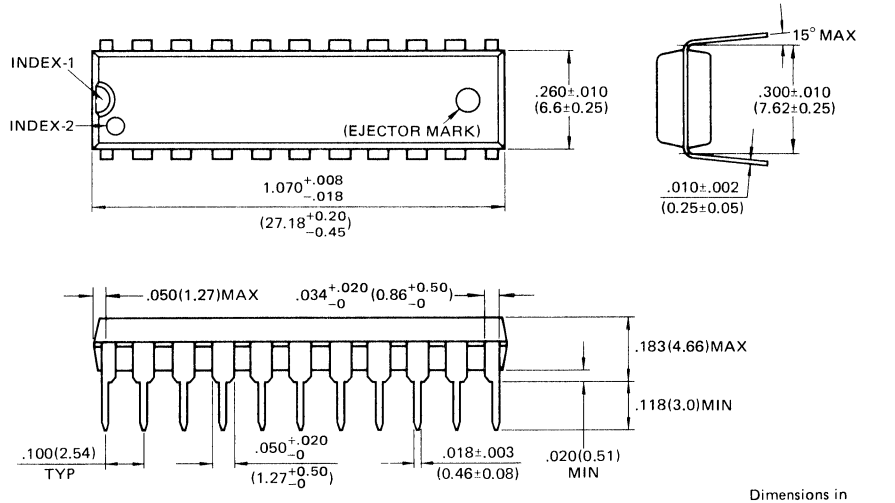


1

PACKAGE DIMENSIONS

(Suffice: -P)

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



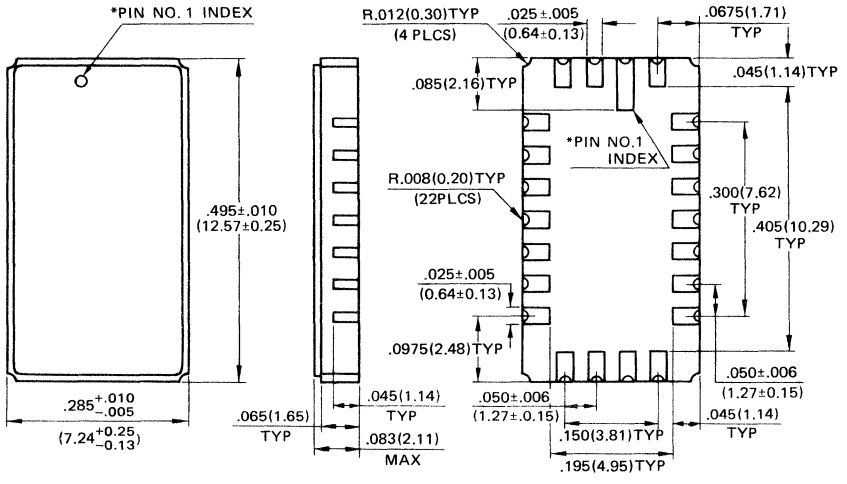
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffice: -CV)

1

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

FUJITSU

CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

MB81C75-25
MB81C75-35

February 1988
Edition 2.0

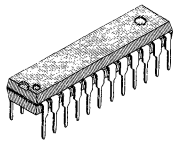
1

16K x 4 BIT (65,536-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

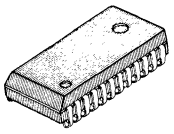
The Fujitsu MB 81C75 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicongate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

The MB 81C75 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization : 16,384 words x 4 bits
  Fast access time : $t_{AA} = t_{ACS} = 25$ ns max. (MB 81C75-25)
  $t_{OE} = 10$ ns max.
  $t_{AA} = t_{ACS} = 35$ ns max. (MB 81C75-35)
  $t_{OE} = 15$ ns max.
- Completely static operation : No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5 V power supply ±10% tolerance
- Low power standby : 440 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 24-pin DIP (300 mil) : Suffix: P
- Standard 28-pad LCC : Suffix: CV
- Standard 24-pin SOJ (300 mil) : Suffix : PJ

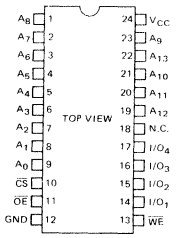


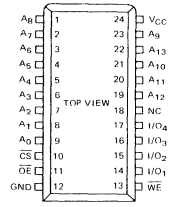
PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

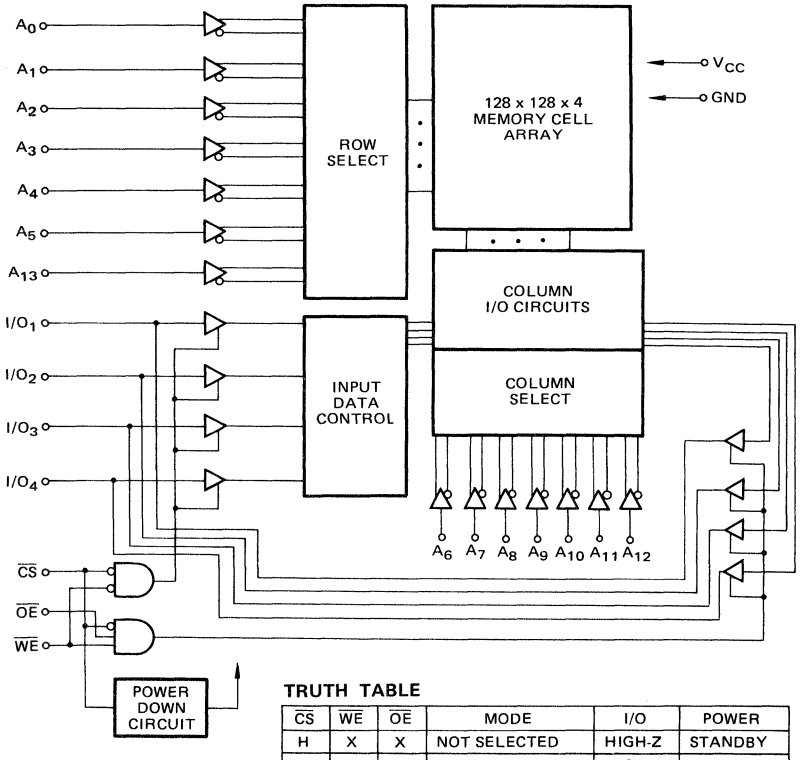
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-3.5 to +7.0	V
Output Voltage		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C75 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O	POWER
H	X	X	NOT SELECTED	HIGH-Z	STANDBY
L	H	H	OUTPUT DESABLE	HIGH-Z	ACTIVE
L	H	L	READ	D_{OUT}	ACTIVE
L	L	X	WRITE	D_{IN}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
I/O Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN} = 0 V)	C_{IN}			7	pF

1

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min, for pulse width less than 20 ns. (V_{IL} Min = -0.5 V at DC Level)

DC CHARACTERISTICS

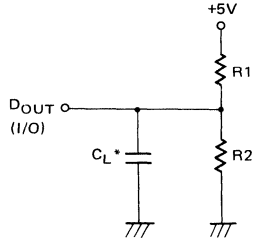
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Value		Unit
			Min	Max	
Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	I_{SB1}		10	mA
	$\overline{CS} = V_{IH}$	I_{SB2}		20	
Active Supply Current	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}, $I_{OUT} = 0$ mA	I_{CC1}		60	mA
Operating Supply Current	Cycle = Min., $I_{OUT} = 0$ mA	I_{CC2}		80	
Input Leakage Current	$V_{IN} = 0$ V to V_{CC}	I_{LI}	-10	10	μA
Output Leakage Current	$\overline{CS} = V_{IH}$, $V_{I/O} = 0$ V to V_{CC}	$I_{LI/O}$	-10	10	μA
Output High Voltage	$I_{OH} = -4$ mA	V_{OH}	2.4		V
Output Low Voltage	$I_{OL} = 8$ mA	V_{OL}		0.4	V

Note: All voltages are referenced to GND

Fig. 2 – AC TEST CONDITIONS

- Output Load



* Including Scope and Jig Capacitance

- Input Pulse Levels: : 0 V to 3.0 V
- Input Pulse Rise & Fall Times : 5 ns (Transient between 0.8 V and 2.2 V)
- Timing Reference Levels : Input : 1.5 V
  : Output : 1.5 V

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}
Load II	480Ω	255Ω	5 pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}

1

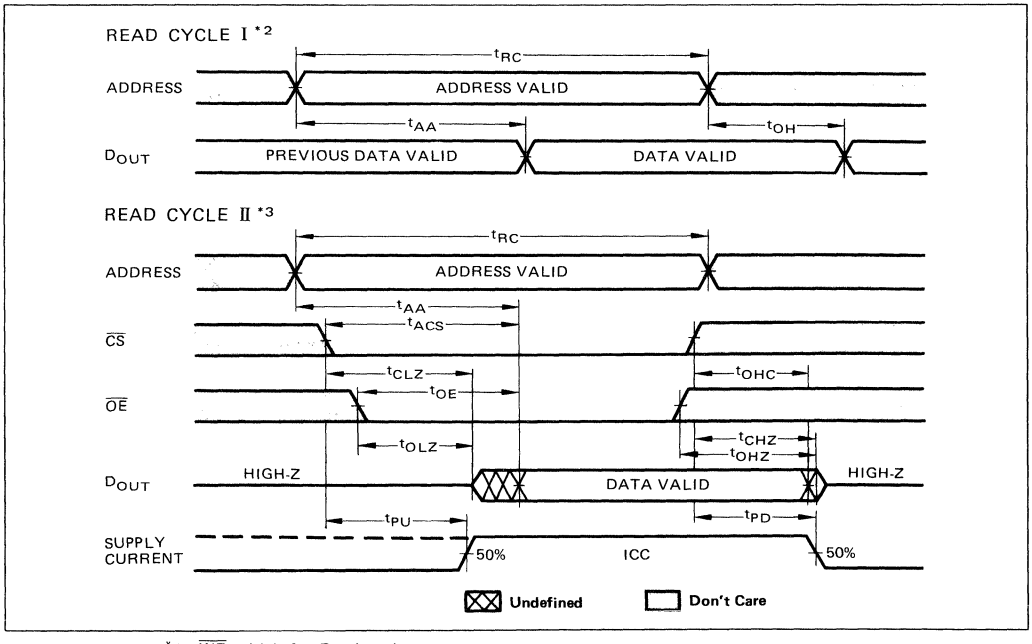
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C75-25		MB 81C75-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS}$ Access Time*3	t_{ACS}		25		35	ns
$\overline{OE}$ Access Time*3	t_{OE}		10		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns
$\overline{CS}$ to output Low-Z*4*5	t_{CLZ}	5		5		ns
$\overline{OE}$ to Output in Low-Z*4*5	t_{OLZ}	0		0		ns
$\overline{CS}$ to Output High-Z*4*5	t_{CHZ}		10		15	ns
$\overline{OE}$ to Output High-Z*4*5	t_{OHZ}		10		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Dwown from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM*1

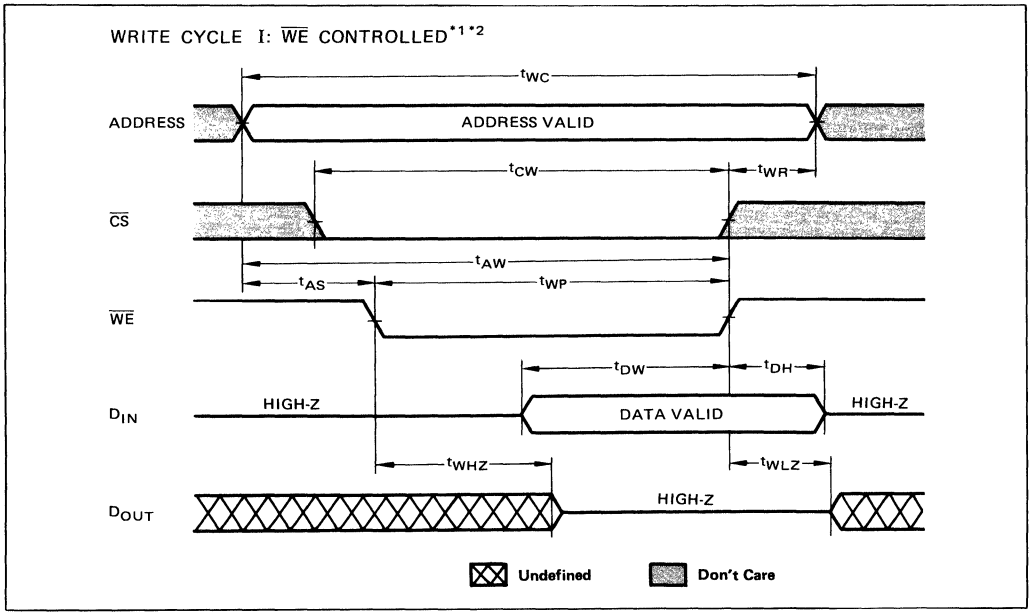


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1

Parameter	Symbol	MB 81C75-25		MB 81C75-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	20		30		ns
Chip Select to End of Write End of Write	t_{CW}	20		30		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$*3*4	t_{WHZ}		10		15	ns
Output Low-Z from $\overline{WE}$*3*4	t_{WLZ}	0	20	0	30	ns

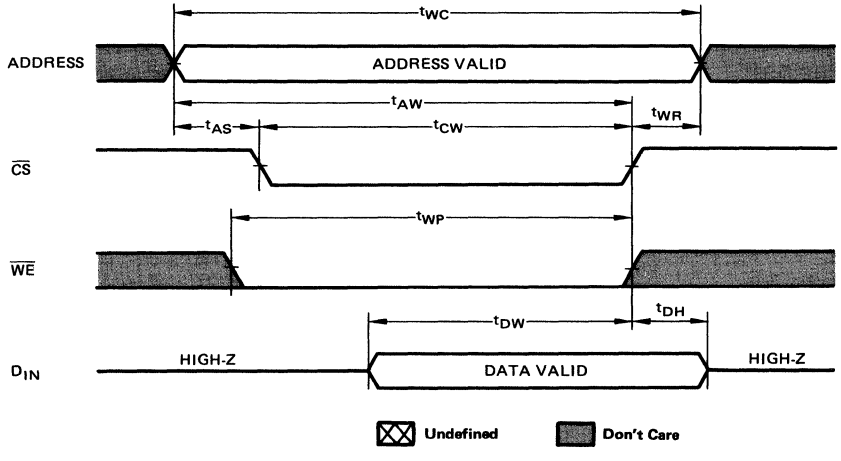
WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

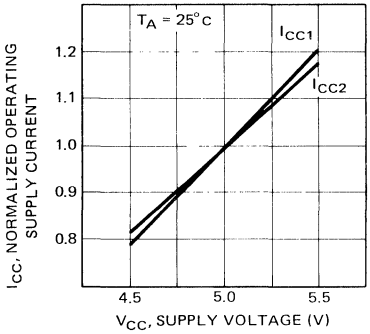


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

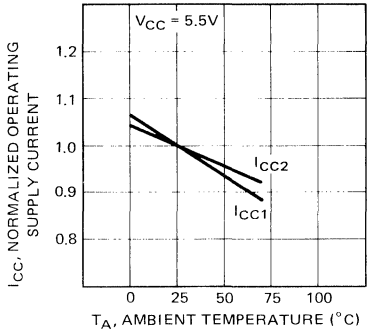


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

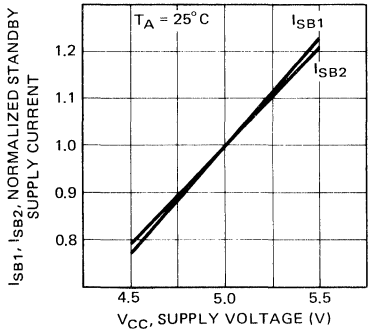


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

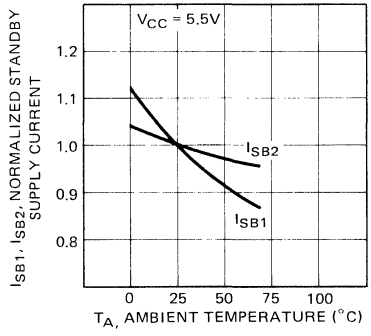
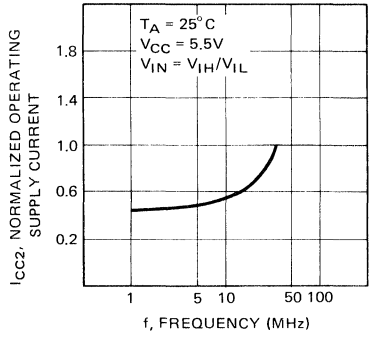


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



1

TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

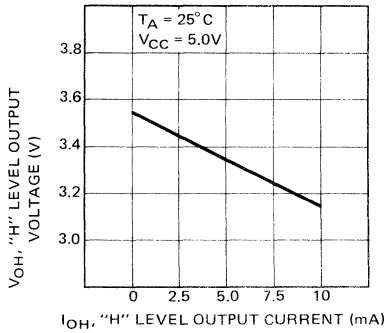


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

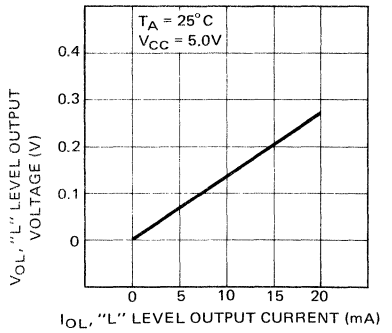


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

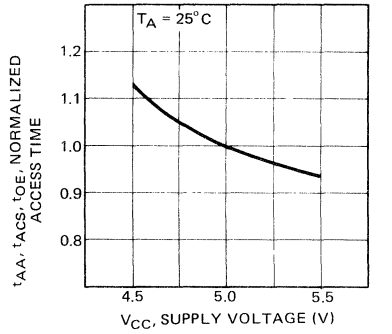


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

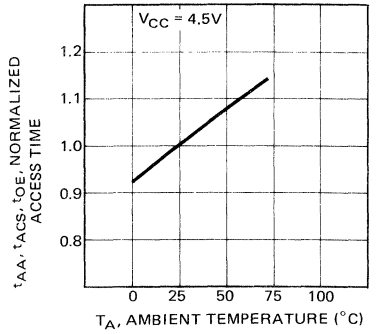
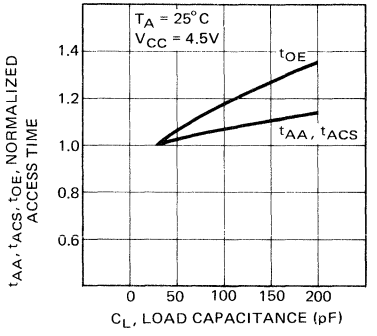


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE

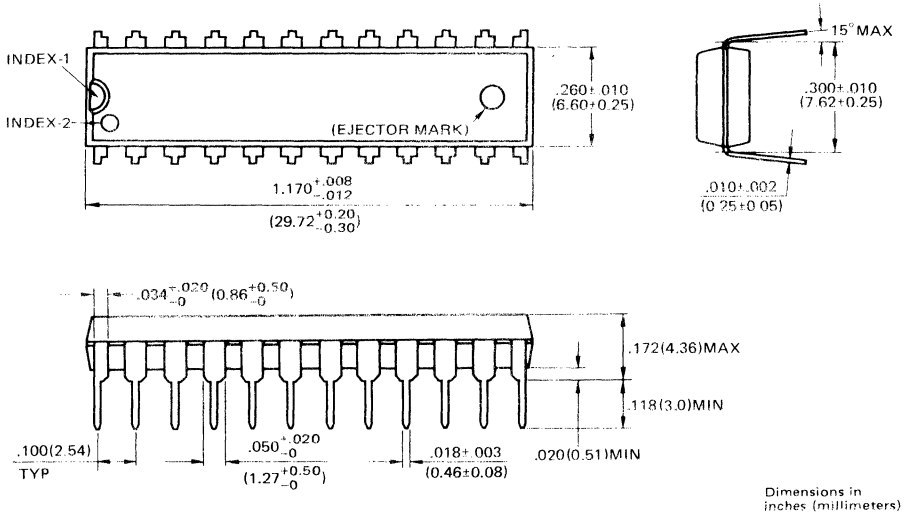


1

PACKAGE DIMENSIONS

(Suffix: P)

24-LEADS PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



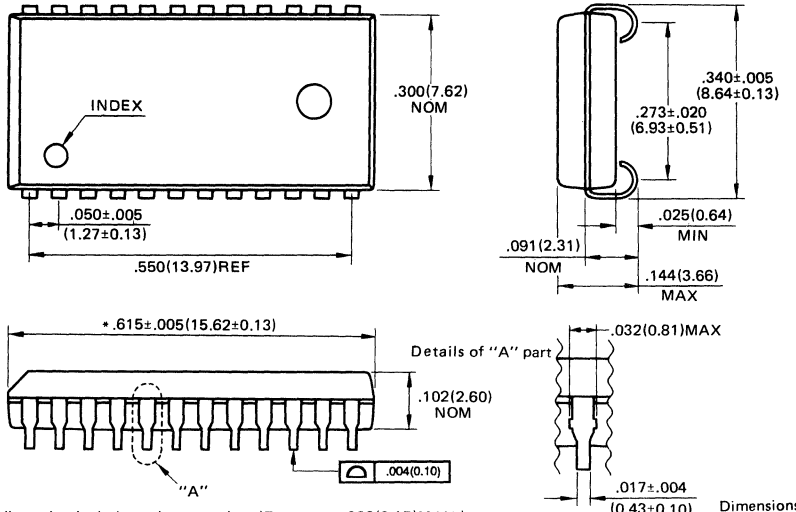
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PJ)

1

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



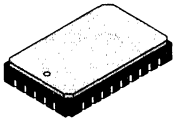
* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)

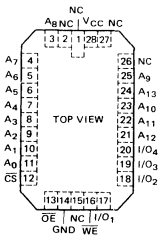
1

PACKAGE DIMENSIONS

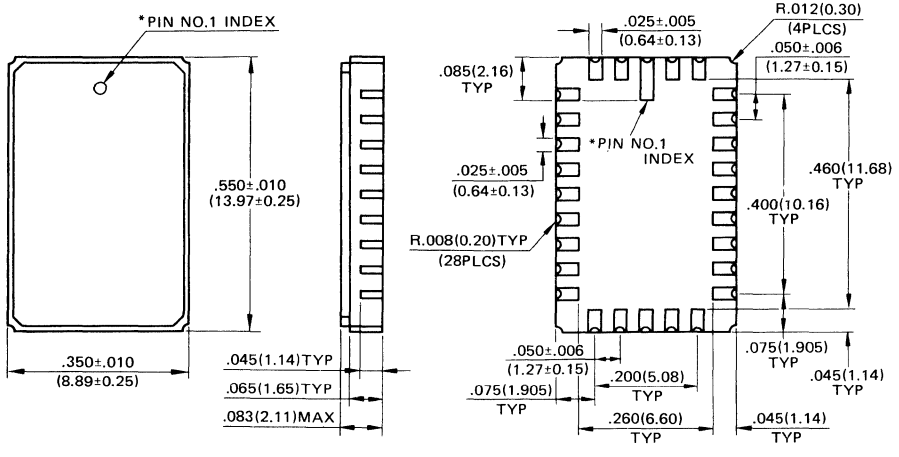
(Suffix: CV)



CERAMIC PACKAGE
LCC-28C-A03



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches
and (millimeters)

1

FUJITSU

CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB81C78A-35
MB81C78A-45

November 1987
Edition 2.0

1

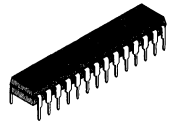
64K-BIT (8192x8) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C78A is 8192 words x 8 bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

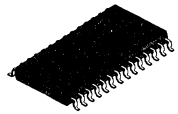
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

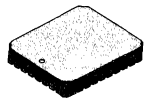
- Organization: 8192 words x 8 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 35 ns max. (MB 81C78A-35)
  $t_{AA} = t_{ACS1}$ = 45 ns max. (MB 81C78A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin Bend type Plastic Flat package (Suffix: -PF)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



PLASTIC PACKAGE
DIP-28P-M04

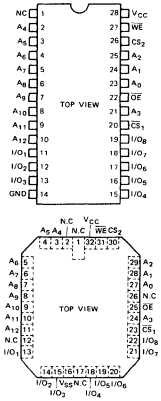


PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

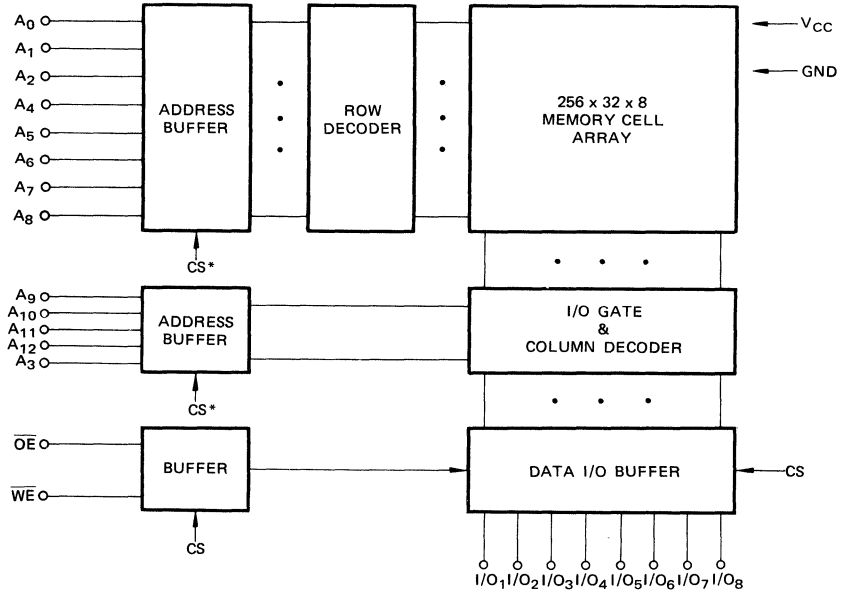
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any I/O with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature	PLASTIC	T_{STG}	−40 to +125	°C
	CERAMIC		−65 to +150	

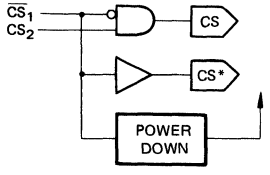
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C78A BLOCK DIAGRAM





TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1}$ = V_{IL} I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min to Max. $\overline{CS_1}$ = V_{CC}-0.2V $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		25	mA	$\overline{CS_1}$ = V_{IH}
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

1

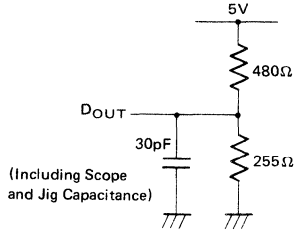
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

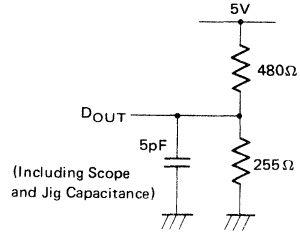
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

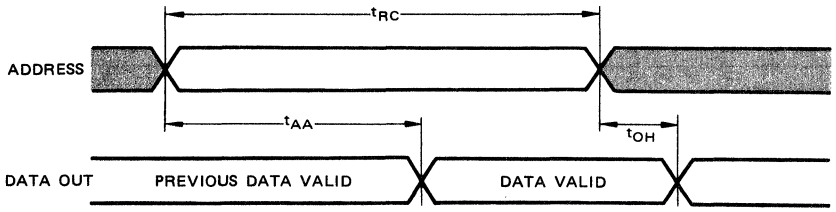
Parameter	Symbol	MB 81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time[*2]	t_{AA}		35		45	ns
$\overline{CS_1}$ Access Time[*3]	t_{ACS1}		35		45	ns
CS_2 Access Time[*3]	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS_1}$[*4*5]	t_{LZ1}	5		5		ns
Output Active from CS_2[*4*5]	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$[*4*5]	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS_1}$[*4*5]	t_{HZ1}		20		25	ns
Output Disable from CS_2[*4*5]	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$[*4*5]	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

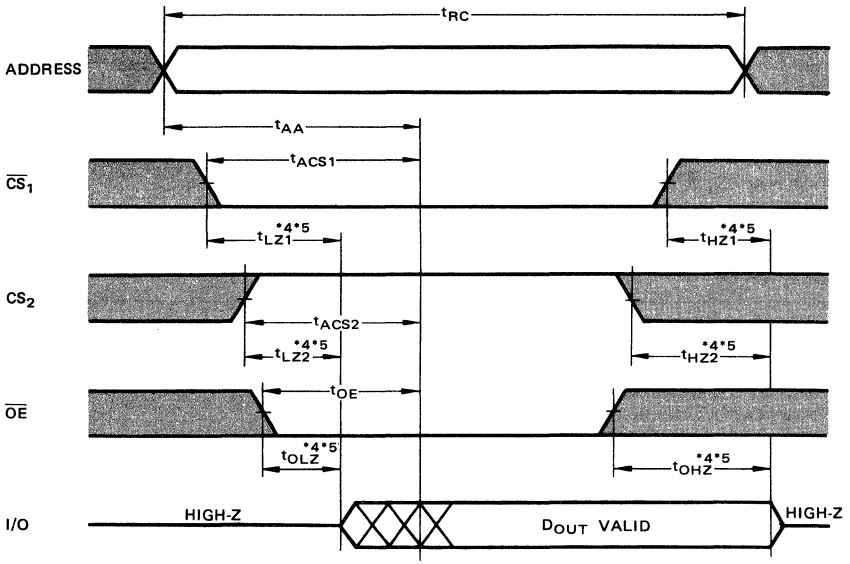
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



: Don't Care : Undefined

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE *1

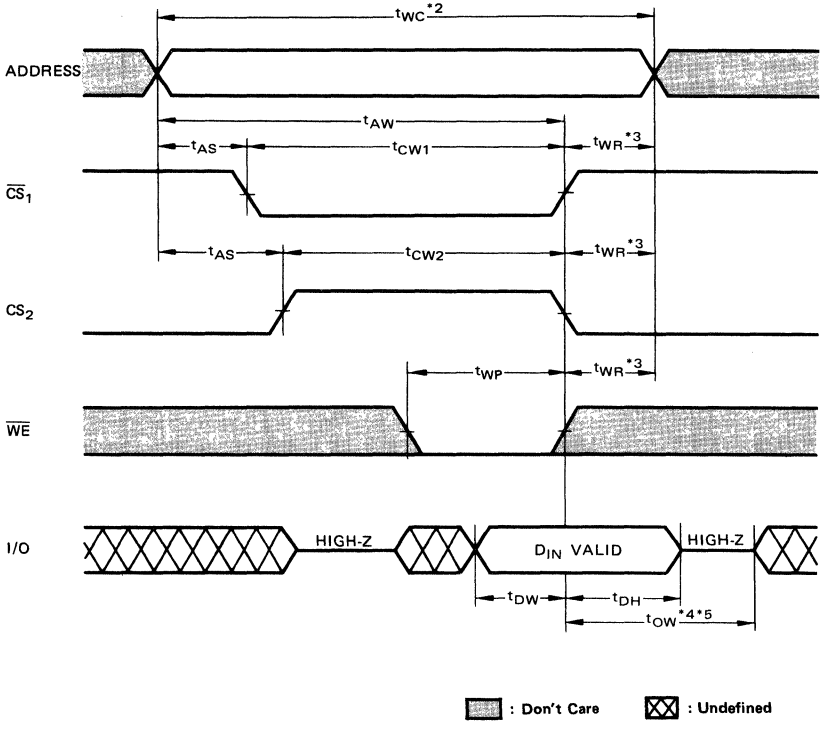
Parameter	Symbol	MB 81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time *3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$ *4*5	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$ *4*5	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED

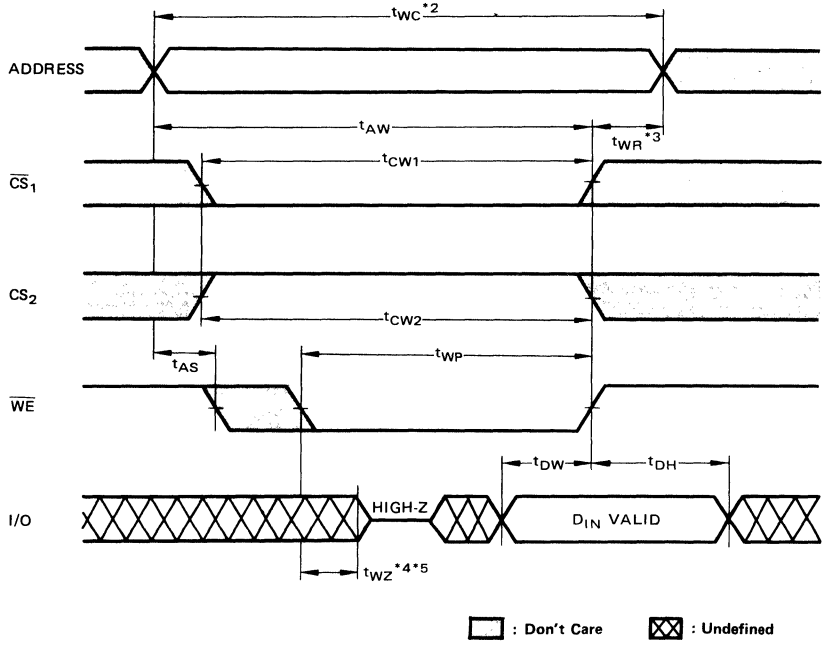


Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

1

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

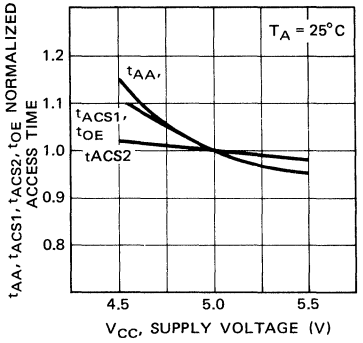


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

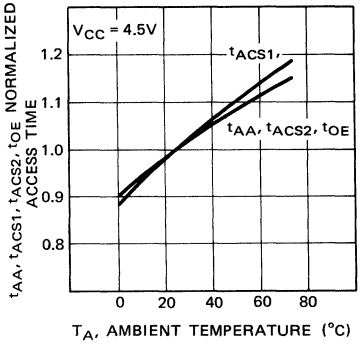


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

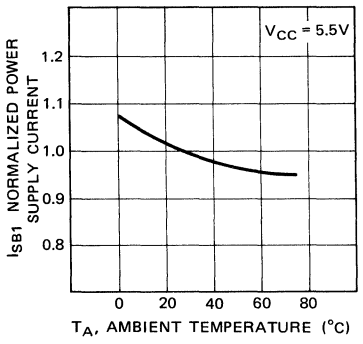


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

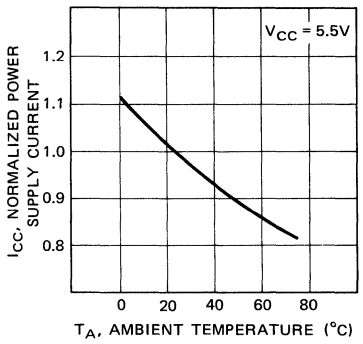
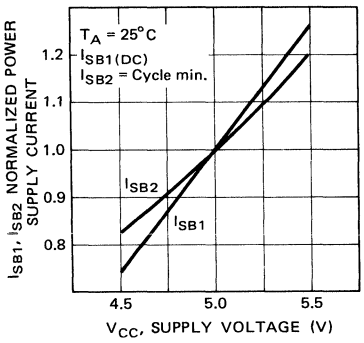


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE



1

Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

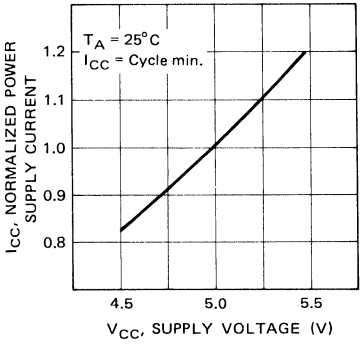


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

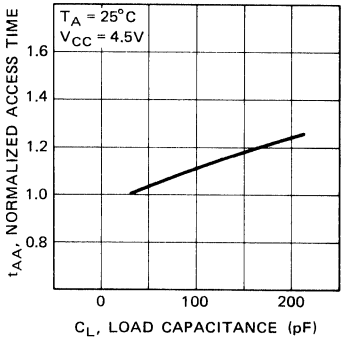


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

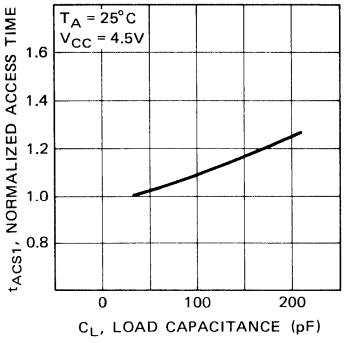


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

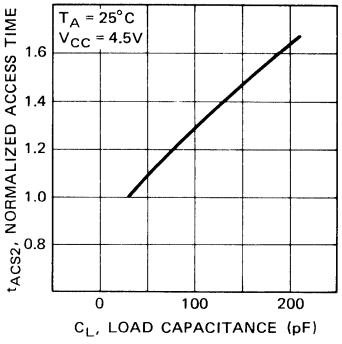
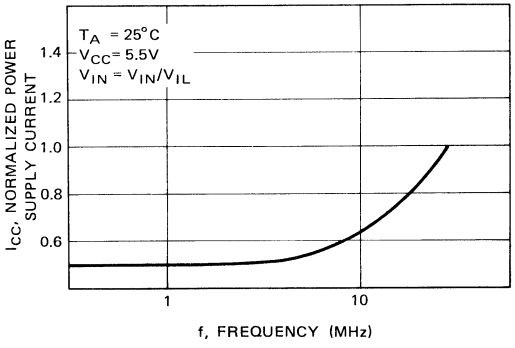


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

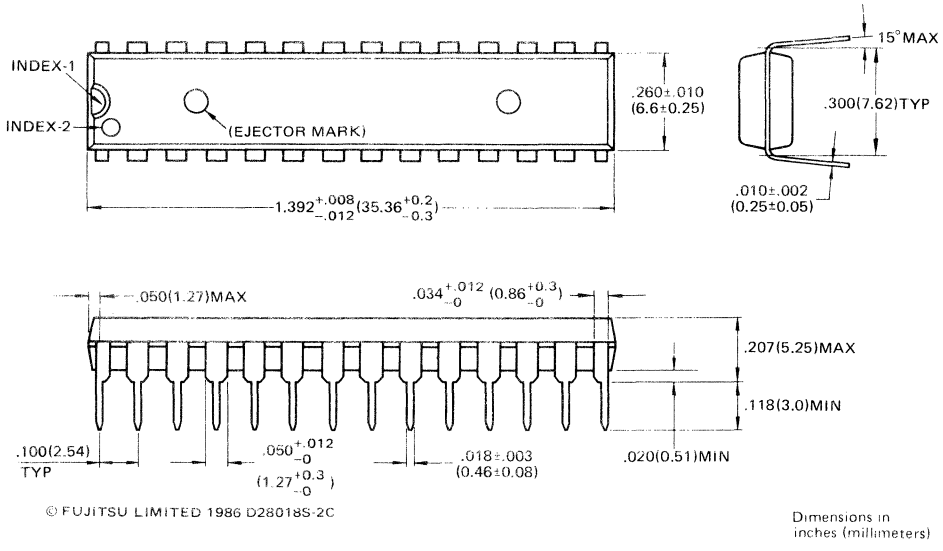


PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

1

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



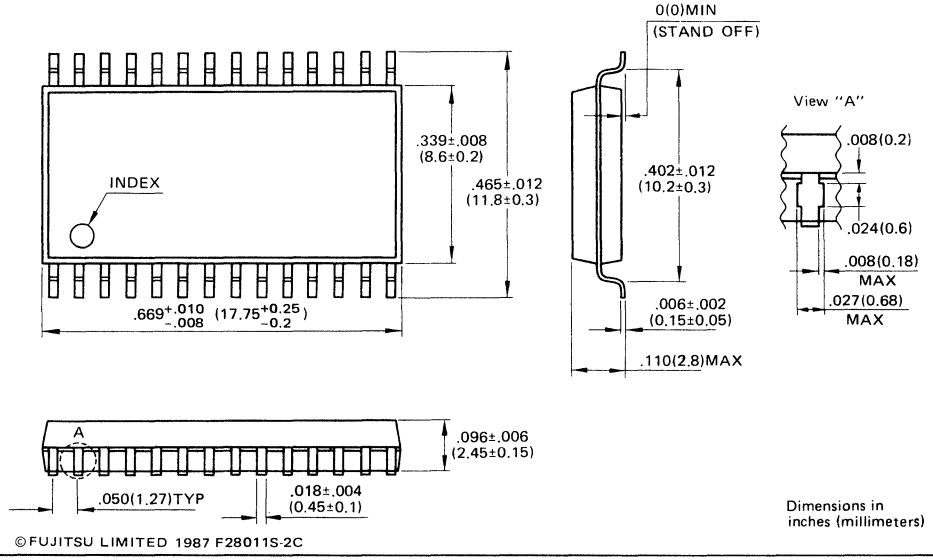
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



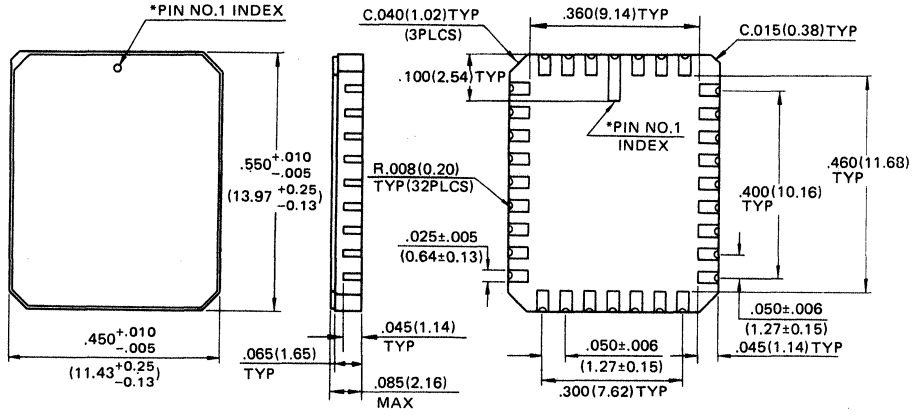
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

CERAMIC LCC (Suffix: -CV)

1

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB81C79A-35
MB81C79A-45

November 1987
Edition 2.0

1

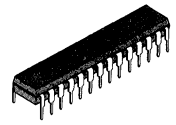
72K-BIT (8192x9) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 81C79A is 8192 words x 9 bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

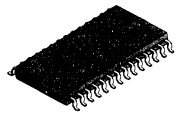
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

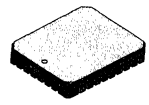
- Organization: 8192 words x 9 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 35 ns max. (MB 81C79A-35)
  $t_{AA} = t_{ACS1}$ = 45 ns max. (MB 81C79A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin Bend type Plastic Flat package (Suffix: -PF)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



PLASTIC PACKAGE
DIP-28P-M04

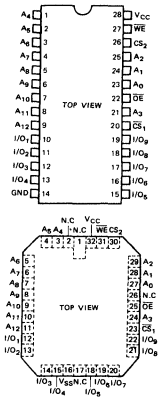


PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

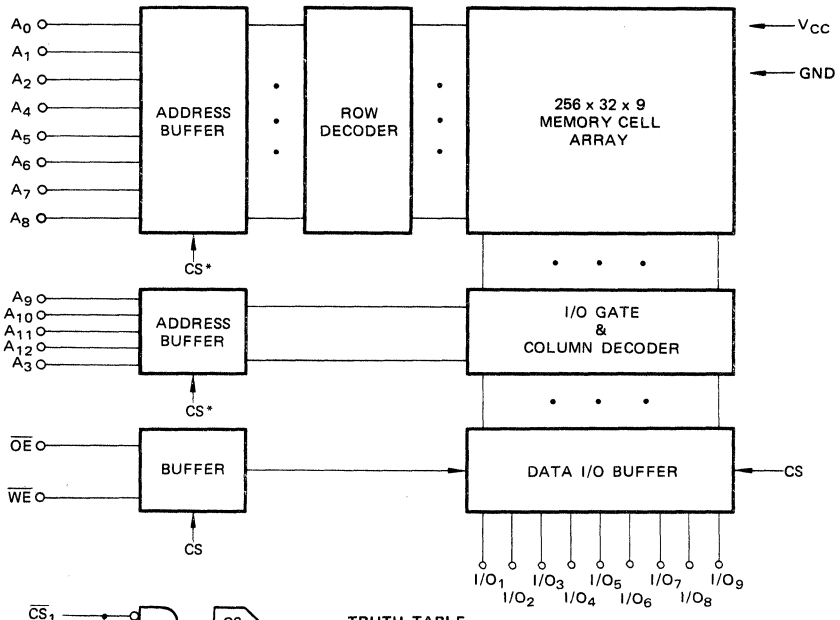
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.5 to +7	V
Output Voltage on any I/O with respect to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	PLASTIC	T_{STG}	-40 to +125	°C
	CERAMIC		-65 to +150	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C79A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS}_1$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1}$ = V_{IL} I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min to Max. $\overline{CS_1}$ = V_{CC}-0.2V $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$-0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$ = V_{IH}
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

1

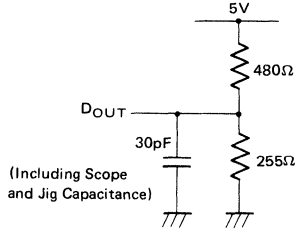
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

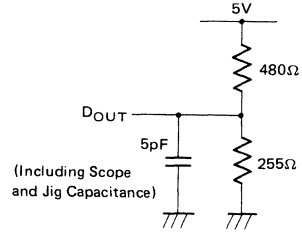
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

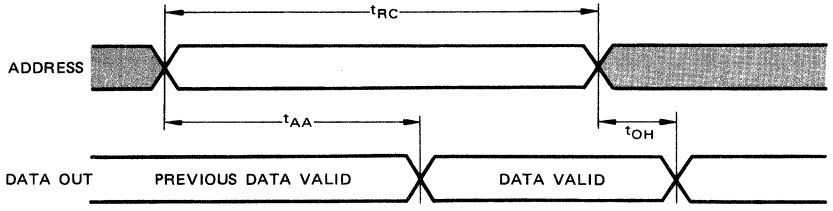
Parameter	Symbol	MB 81C79A-35		MB 81C79A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time[*2]	t_{AA}		35		45	ns
$\overline{CS_1}$ Access Time[*3]	t_{ACS1}		35		45	ns
CS_2 Access Time[*3]	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS_1}$[*4*5]	t_{LZ1}	5		5		ns
Output Active from CS_2[*4*5]	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$[*4*5]	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS_1}$[*4*5]	t_{HZ1}		20		25	ns
Output Disable from CS_2[*4*5]	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$[*4*5]	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

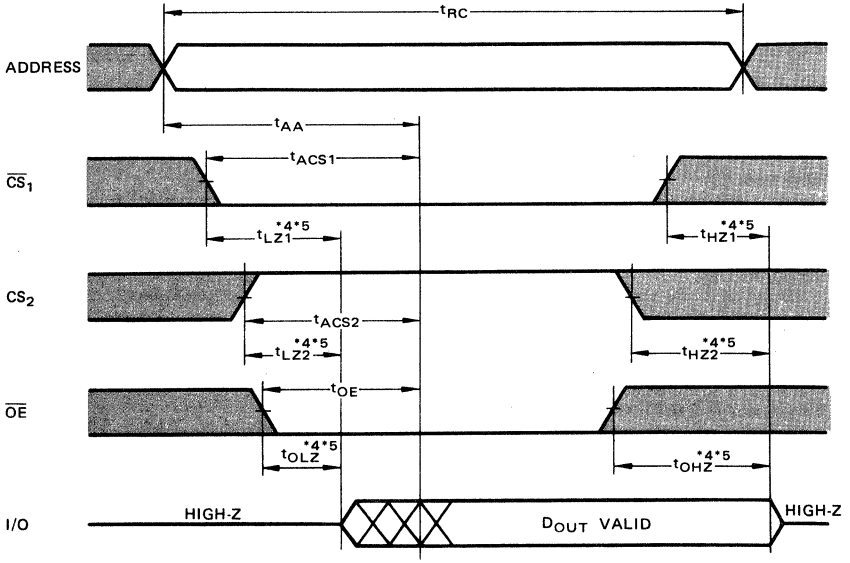
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



: Undefined : Don't Care

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE*1

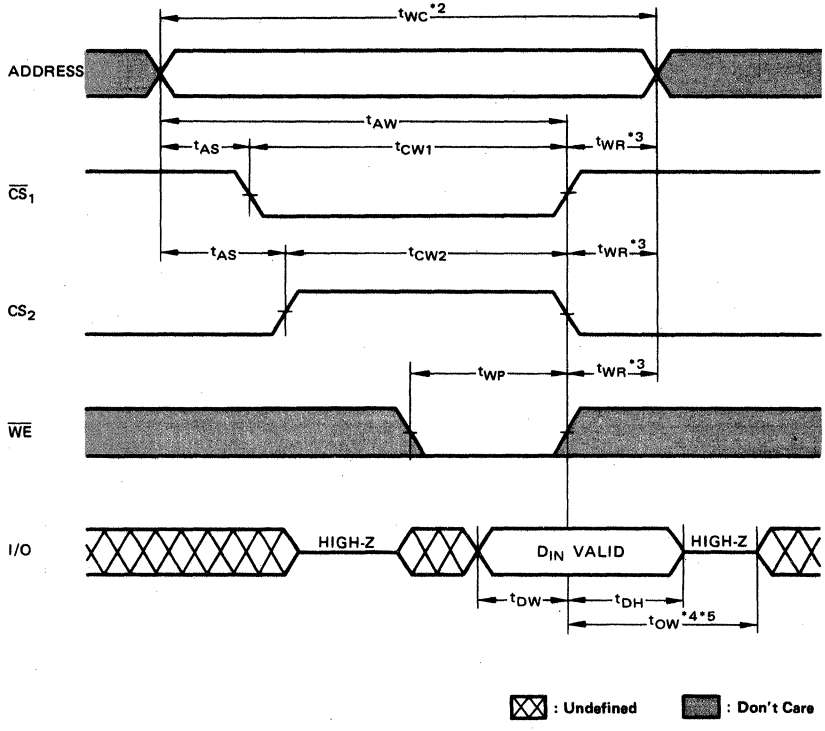
Parameter	Symbol	MB 81C79A-35		MB 81C79A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time*3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$*4*5	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$*4*5	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED

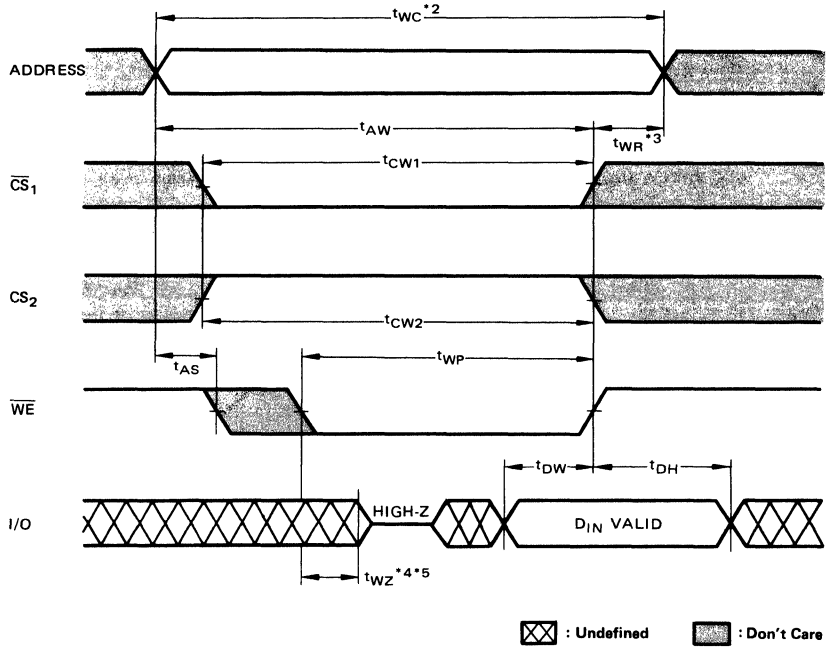


Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

1

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

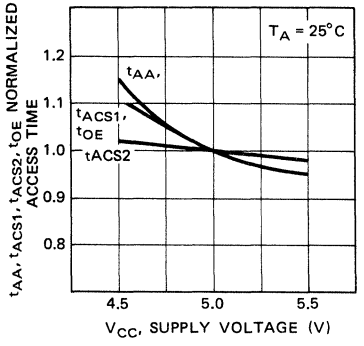


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

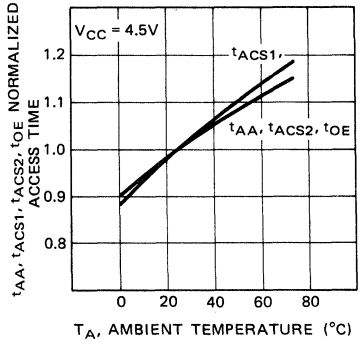


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

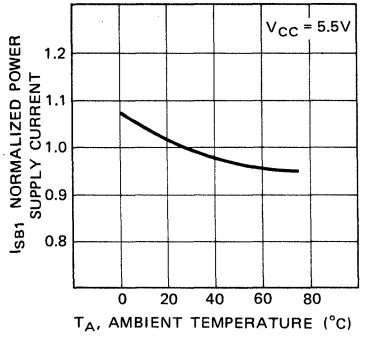


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

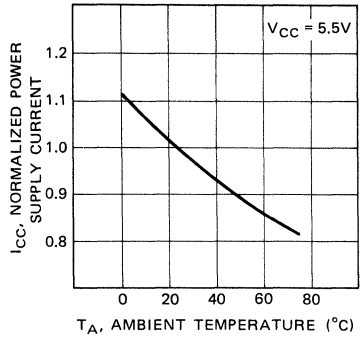
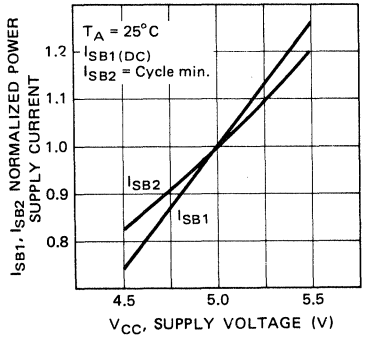


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE



1

Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

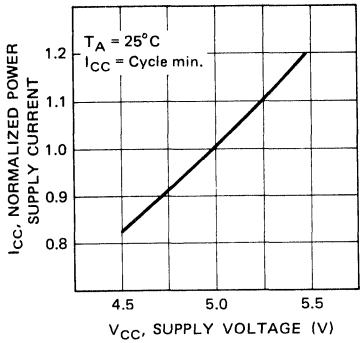


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

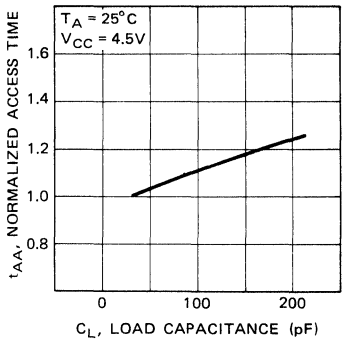


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

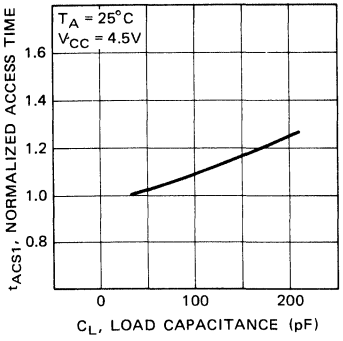


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

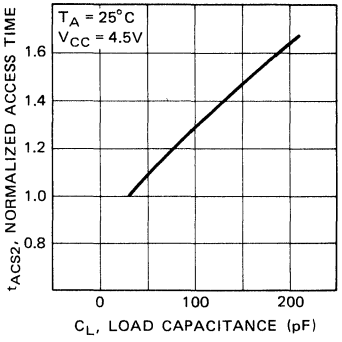
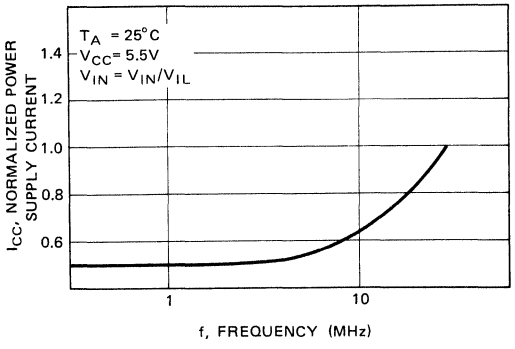


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

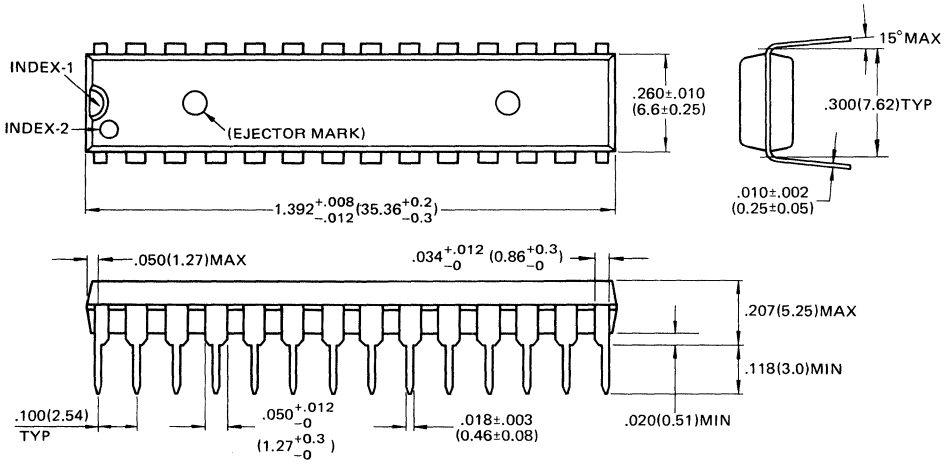


PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

1

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



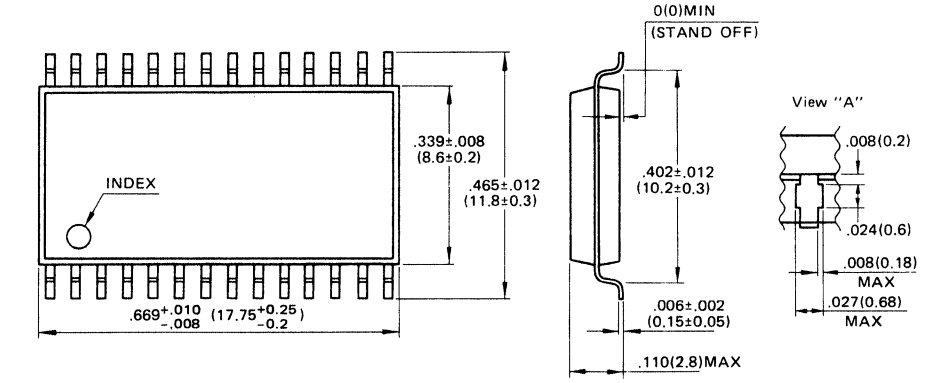
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



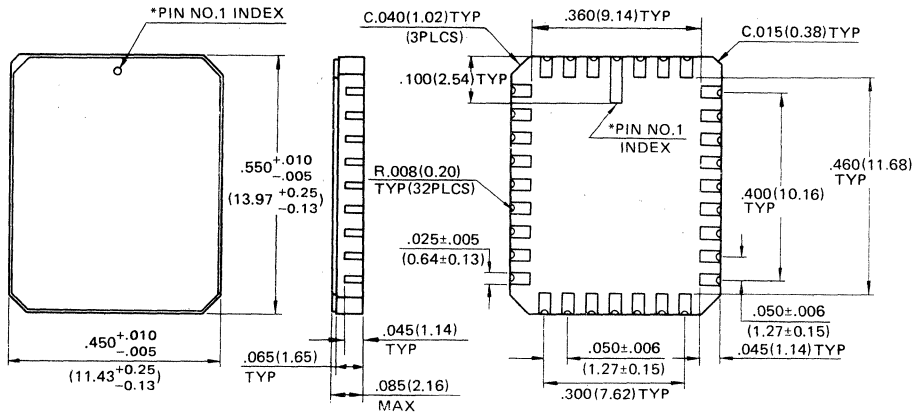
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

CERAMIC LCC (Suffix: -CV)

1

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

FUJITSU

CMOS 262,144 BIT STATIC RANDOM ACCESS MEMORY

MB81C81A-35
MB81C81A-45

May 1988
Edition 1.0

1

262,144 WORDS x 1 BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY

The Fujitsu MB81C81A is 262,144 words x 1 bit static random access memory fabricated with a CMOS technology.

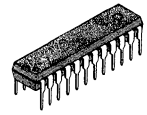
Since MB81C81A consists of NMOS cells and CMOS peripherals, it is packaged in 300 mil DIP and reached low power dissipation such as 550 mW.

It uses fully static circuitry and therefore requires no clocks or refreshing to operate.

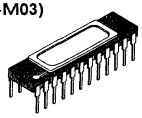
The MB81C81A is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

MB81C81A is compatible with TTL logic families in all respects; input, output and a single +5 V supply.

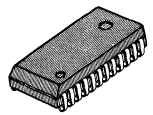
- Organization: 262,144 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 35 ns max. (MB81C81A-35)
  45 ns max. (MB81C81A-45)
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 300 mil width 24-pin Dual In-Line Package
  (Suffix: Plastic DIP; P-SK, Ceramic DIP; C-SK)
  24 pad LCC (Suffix: CV)
  24 pad SOJ (Suffix: PJ)



PLASTIC PACKAGE
(DIP-24P-M03)



CERAMIC PACKAGE
(DIP-24C-A08)

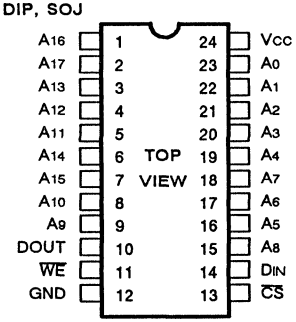


PLASTIC PACKAGE
(LCC-24P-M02)

LCC-24C-A02, See page 11

PIN ASSIGNMENT

DIP, SOJ



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7	V
Input Voltage on any pin with to GND		V_{IN}	-3.5* to +7	V
Output Voltage on any pin with to GND		V_{OUT}	-0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-45 to +125	

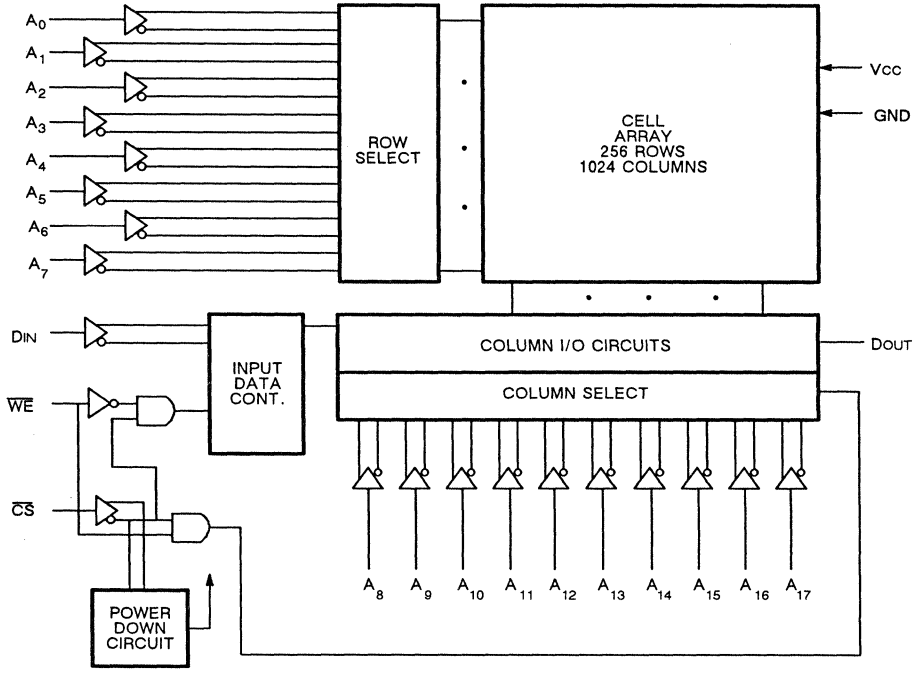
* DC: min. = -0.5 V

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MB81C81A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

CAPACITANCE (TA = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		8	pF
Output Capacitance (VOUT = 0 V)	COUT		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* -3.0 V Min. for pulse width less than 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition		Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC} V_{CC} = Max.		I_{LI}	-10		10	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 V to 4.5 V V_{CC} = Max.		I_{LO}	-50		50	µA
Power Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{CC} = Max. Cycle = Min.	MB81C81A-45	I_{CC}			100	mA
		MB81C81A-35				120	
Standby Current	$\overline{V_{CC}}$ = Min. to Max. $\overline{CS} \geq V_{CC}$ -0.2 V $V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{CC}$ - 0.2 V		I_{SB1}			15	mA
	$\overline{V_{CC}}$ = Min. to Max. $\overline{CS}$ = V_{IH}		I_{SB2}			30	
Output Low Voltage	I_{OL} = 16 mA		V_{OL}			0.4	V
Output High Voltage	I_{OH} = -4 mA		V_{OH}	2.4			V
Peak Power on Current*1	$\overline{V_{CC}}$ = 0 to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.		I_{PO}			30	mA

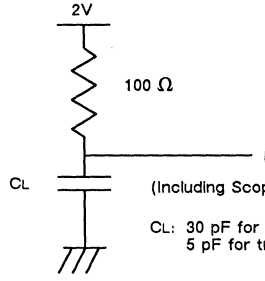
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

1

AC TEST CONDITIONS

Input Pulse Levels:	0.6 V to 2.4 V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Input: V_{IL} = 0.8 V/V_{IH} = 2.2 V Output: V_{OL} = 0.8 V/V_{OH} = 2.2 V

Output Load: **Fig. 2**



(Including Scope and Jig)

CL: 30 pF for all except tHZ, tWZ, tLZ and tOW.
5 pF for tHZ, tWZ, tLZ and tOW.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

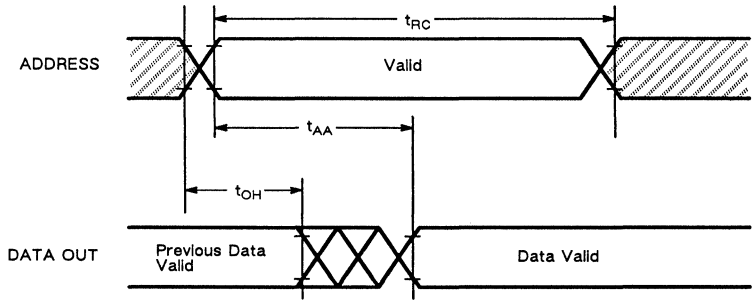
Parameter	Symbol	MB81C81A-35		MB81C81A-45		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
Read Cycle Time *1	tRC	35		45		ns
Address Access Time	tAA		35		45	ns
Chip Select Access Time *2	tACS1		35		45	ns
Output Hold from Address Change	tOH	5		5		ns
Chip Selection to Output in Low-Z *3	tLZ	5		5		ns
Chip Deselection to Output in High-Z *3	tHZ	0	20	0	25	ns
Chip Selection to Power Up time	tPU	0		0		ns
Chip Deselection to Power Down	tPD		35		45	ns

*1 All Read cycles are determined from the last valid address transitioning to the first address transitioning of next cycle.
*2 Addesses valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500 mV from steady state voltage with specified load in Figure 2.

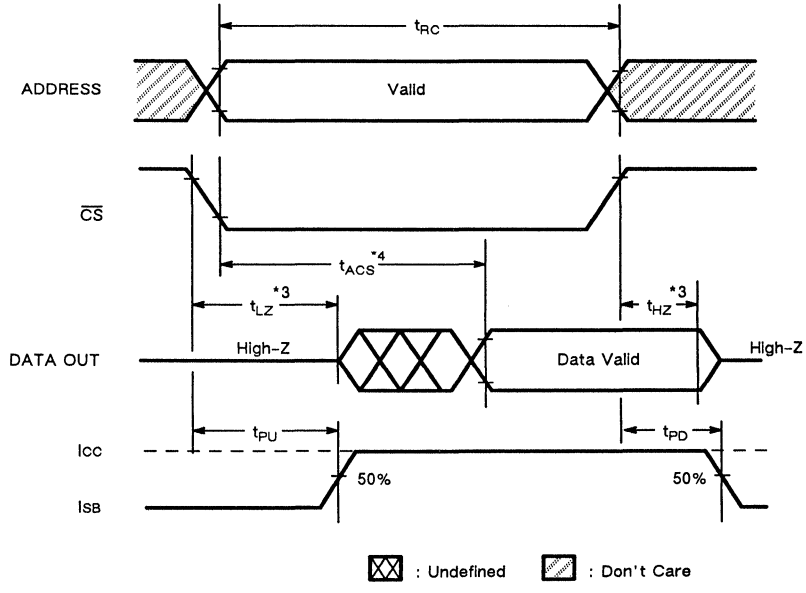
1

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *2



READ CYCLE: $\overline{CS}$ CONTROLLED *2



*1 $\overline{CS}$ is Low.
*2 $\overline{WE}$ is high for Read cycles.
*3 transition is measured at ±500mV from steady state voltage with specified load in Fig. II.
*4 Addresses valid prior to or coincident with $\overline{CS}$ transition low.

1

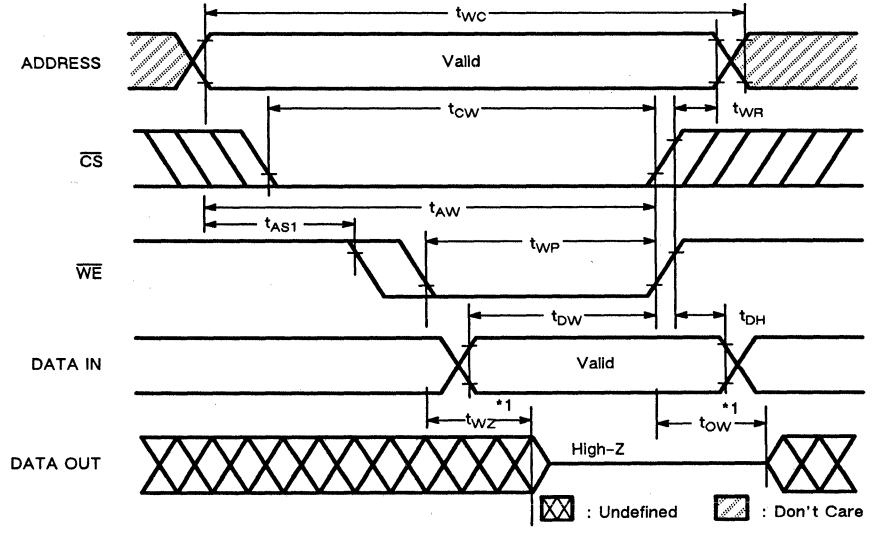
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C81A-35		MB81C81A-45		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
Write Cycle Time	t_{WC}	35		45		ns
Chip Selection to End of Write	t_{CW}	30		40		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS1}	5		5		ns
Address Setup Time	t_{AS2}	0		0		ns
Write Pulse Width	t_{WP}	25		30		ns
Data Valid to End of Write	t_{DW}	20		25		ns
Write Recovery Time	t_{WR}	5		5		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *1	t_{WZ}	0	20	0	25	ns
Output Active from End of Write *1	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{WE}$ CONTROLLED *2

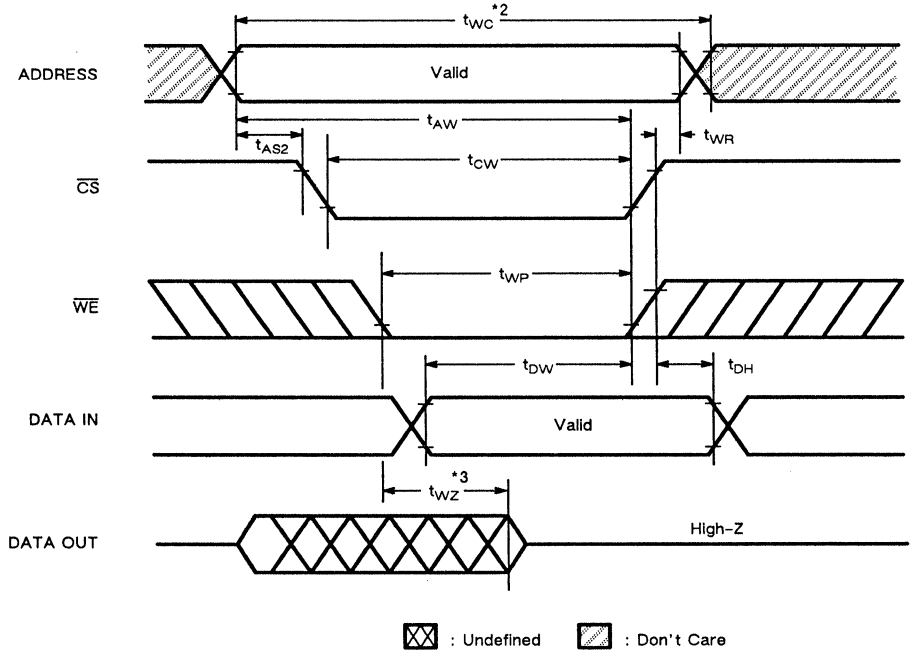


*1 Transition is measured at the point of ±500 mV from steady state voltage.
*2 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

1

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1

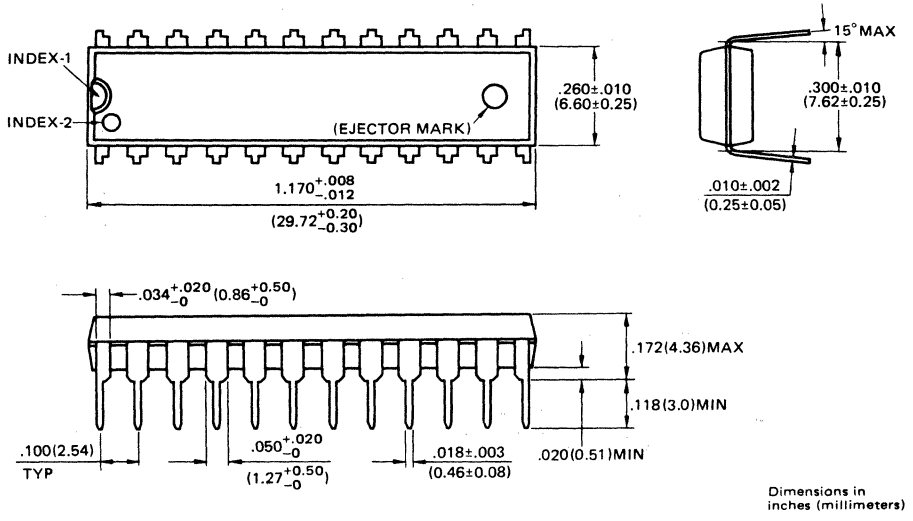


*1 $\overline{CS}$ OR $\overline{WE}$ must be high during address transitions.
*2 All write cycle are determined from last valid address transitioning to the first address transitioning of next cycle.
*3 Transition is measured at ±500mV from steady state voltage with specified load in Fig. II.

PACKAGE DIMENSIONS

1

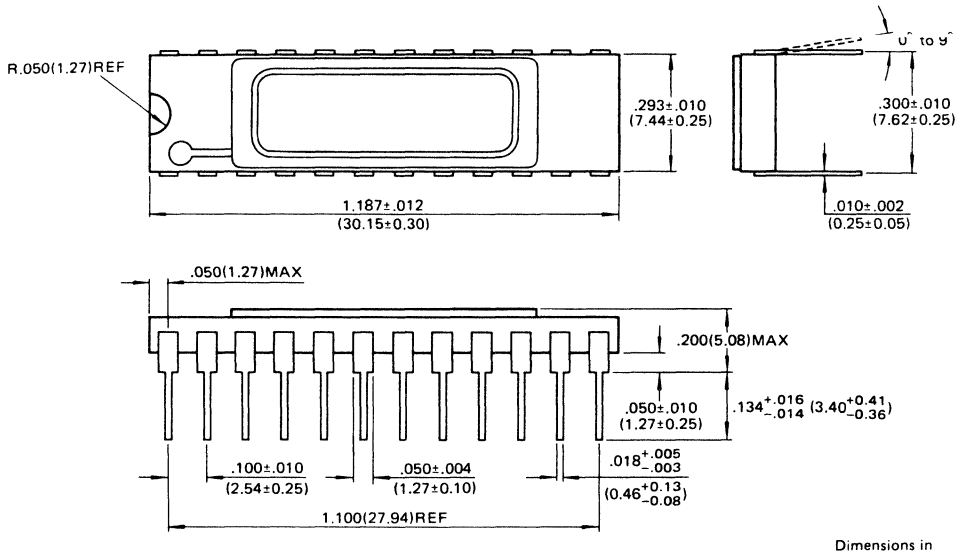
24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

24-LEAD CERAMIC(CERDIP) DUAL IN-LINE PACKAGE
(CASE No: DIP-24C-A08)

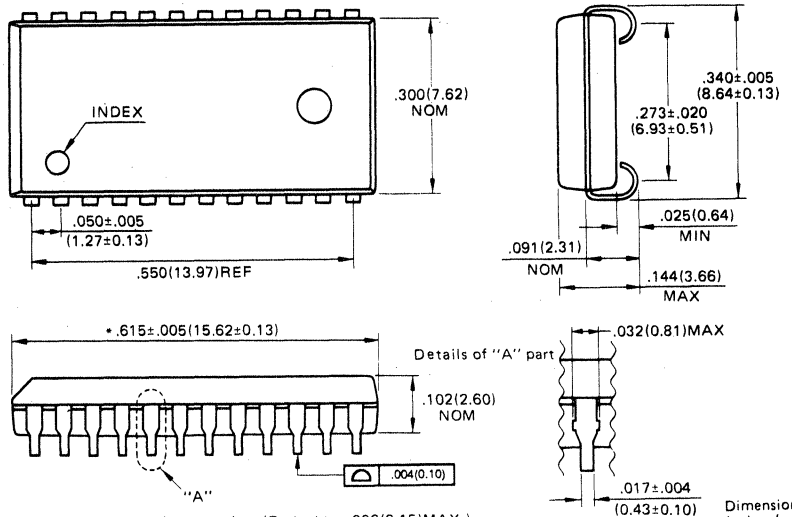


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

1

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

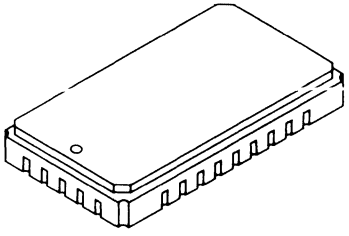


* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

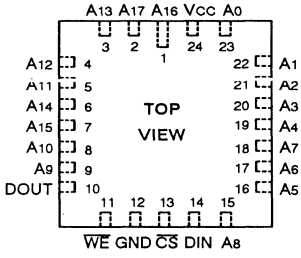
Dimensions in inches (millimeters)

1

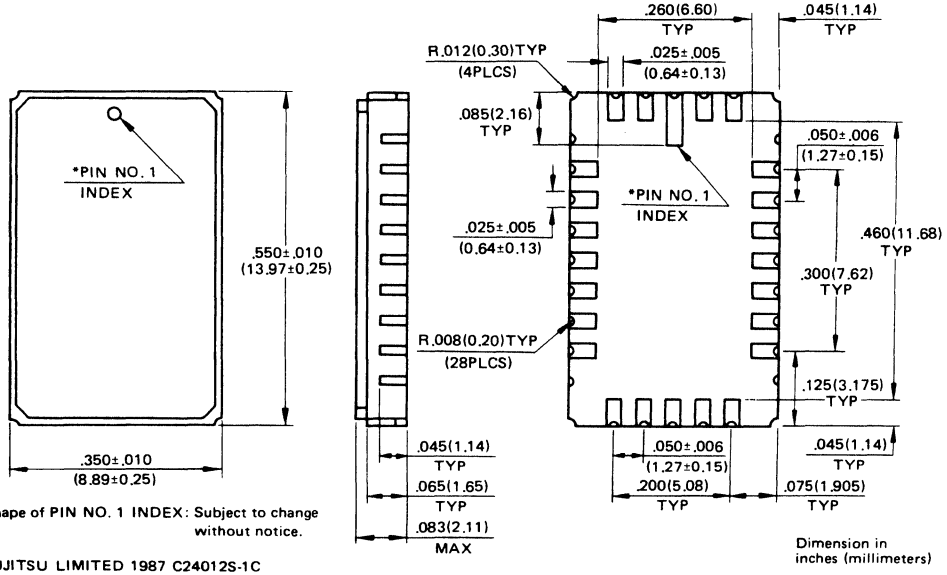
PACKAGE DIMENSIONS (Continued)



CERAMIC PACKAGE
(LCC-24C-A02)



24-LEAD CERAMIC LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

1

October 1989
Edition 4.0

FUJITSU

DATA SHEET

MB81C84A-35/-45
CMOS 256K-BIT HIGH SPEED SRAM

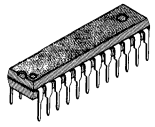
1

65,536 WORDS x 4 BITS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

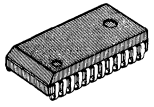
The Fujitsu MB81C84A is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon-gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. MB81C84A has 300mil plastic DIP and 300mil plastic small outline J-lead (SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB81C84A is ideally suited for use in latge computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 65,536 words x 4 bits
  Fast access time: $t_{AA} = t_{ACS}$ = 35ns max.(MB81C84A-35)
  $t_{AA} = t_{ACS}$ = 45ns max. (MB81C84A-45)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three–state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 660mW max. (Active)
  165mW max. (Standby, TTL level)
  83mW max. (Standby, CMOS level)
- Standard 24-pin PLASTIC DIP package (300mil): Suffix -P-SK
- Standard 24-pin PLASTIC SOJ package (300mil): Suffix -PJ

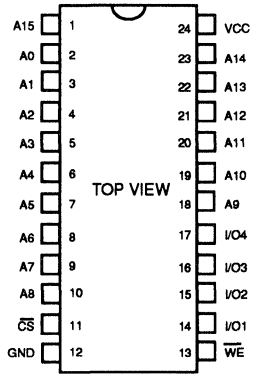


PLASTIC PACKAGE
DIP–24P–M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE.)

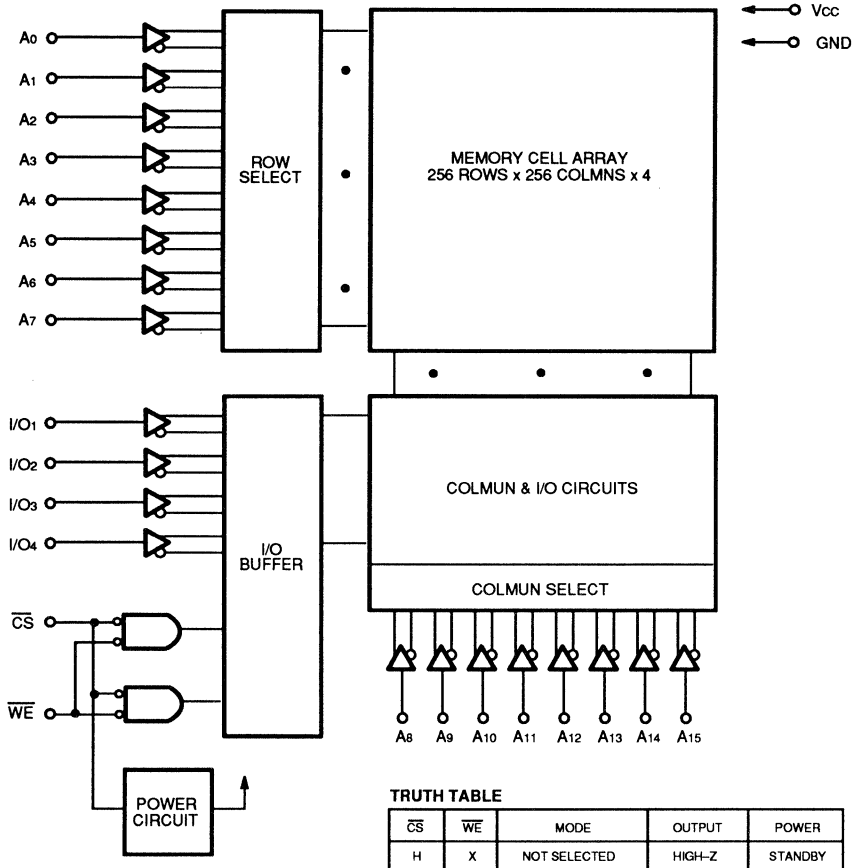
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–3.0 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipaiton	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MB81C84A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	DOUT	ACTIVE

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{I/O}$ = 0V)	C_{OUT}			8	pF
Input Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

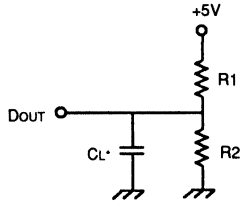
Parameter	Symbol	Min	Max	Unit	Test Conditon
Standby Supply Current	I_{SB1}		15	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{CC} –0.2V, $V_{IN} \geq V_{CC}$–0.2V or $V_{IN} \leq$ 0.2V
Standby Supply Current	I_{SB2}		30	mA	V_{IN} = V_{IN} or V_{IL} $\overline{CS}$ = V_{IH}, V_{CC} = Min. to Max.
Operating Supply Current	I_{CC}		120	mA	Cycle = Min., I_{OUT} = 0mA, $\overline{CS}$ = V_{IL}
Input Leakage Current	I_{LI}	–10	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	–50	50	µA	$\overline{CS}$ = V_{IH}, V_{OUT} = 0 to V_{CC}
Input Low Voltage	V_{IL}	–2.0 *1	0.8	V	
Input High Voltage	V_{IH}	2.2	6.0	V	
Output High Voltage	V_{OH}	.24		V	I_{OH} = –4mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA

Note: All voltages are referenced to GND
*1 –2.0V Min. for pulse width less than 20 ns. (V_{IL} min. = –0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Output Load

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5 ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.2V



* Including Scope and Jig Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}

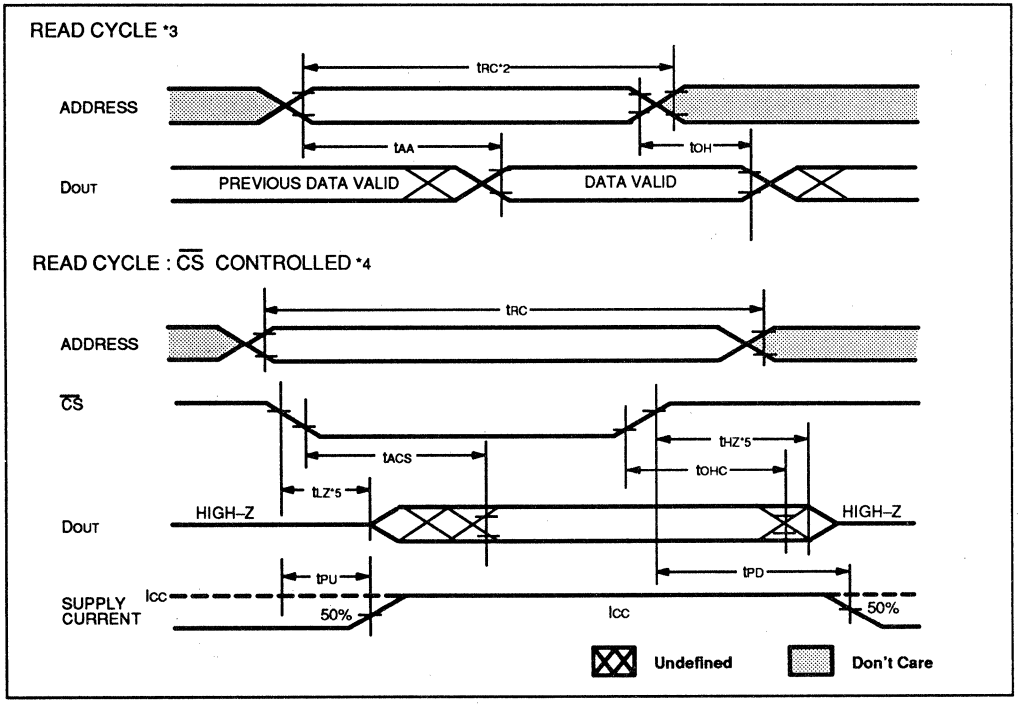
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB81C84A-35		MB81C84A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	35		45		ns
Address Access Time	tAA		35		45	ns
Chip Selection Access Time	tACS		35		45	ns
Output Hold from Address Change	tOH	0		0		ns
Output Hold from Chip Selection	tOHC	0		0		ns
Chip Selection to Output Low-Z	tLZ	5		5		ns
Chip Deselection to Output High-Z	tHZ	0	20	0	25	ns
Power Up from Chip Selection	tPU	0		0		ns
Power Down from Chip Selection	tPD		35		35	ns

READ CYCLE TIMING DIAGRAM *1

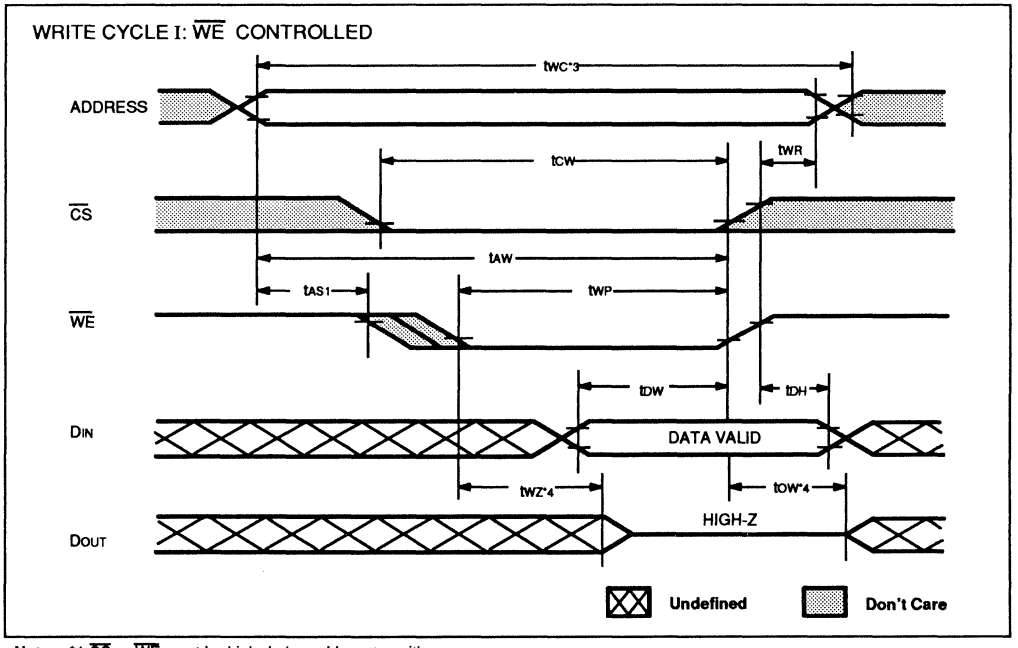


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transtioning address.
*3 Device is continously selected, $\overline{CS}$ = VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at ±500mV from steady state voltage specified load in Fig. 2.

WRITE CYCLE

Parameter	Symbol	MB81C84A-35		MB81C84A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	35		45		ns
Address Valid to End of Write	tAW	30		35		ns
Chip Select to End of Write	tCW	30		35		ns
Data Valid to End of Write	tDW	15		20		ns
Data Hold Time	tDH	5		5		ns
Write Pulse Width	tWP	30		35		ns
Address Setup Time from $\overline{WE}$	tAS1	2		5		ns
Address Setup Time from $\overline{CS}$	tAS2	0		0		ns
Write Recovery Time	tWR	3		5		ns
Output High-Z from Write Enable	tWZ	0	15	0	15	ns
Output Low-Z from Write Enable	tOW	5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2*5

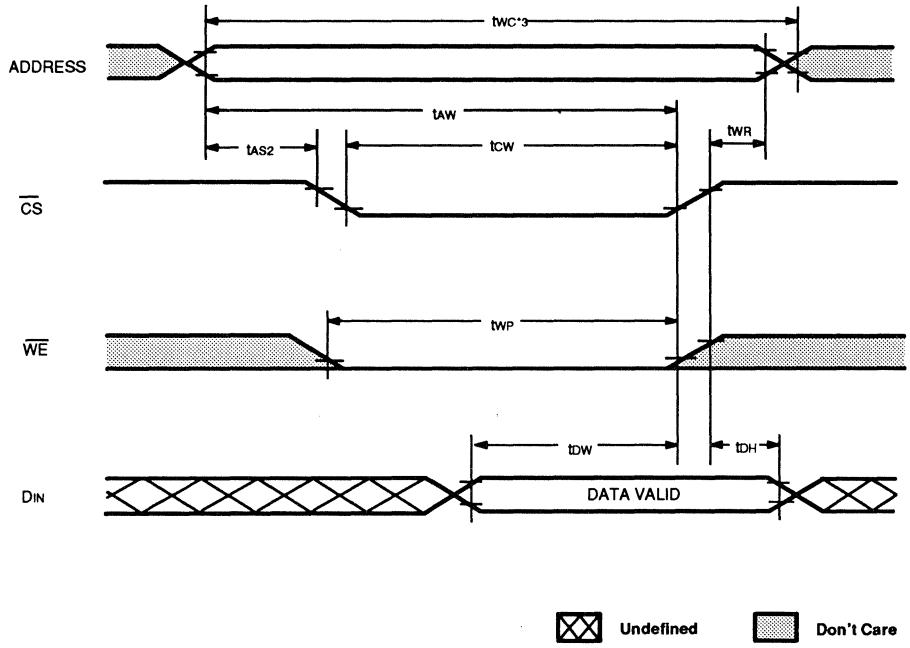


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the READ mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

1

WRITE CYCLE TIMING DIAGRAM (Continued) *1*2*4

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.
*4 If $\overline{CS}$ is in the READ mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

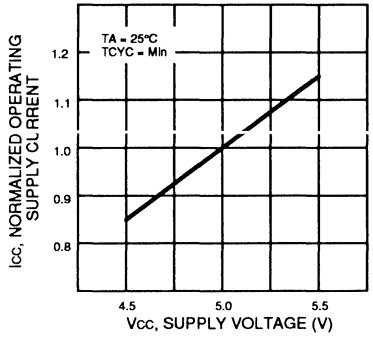


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

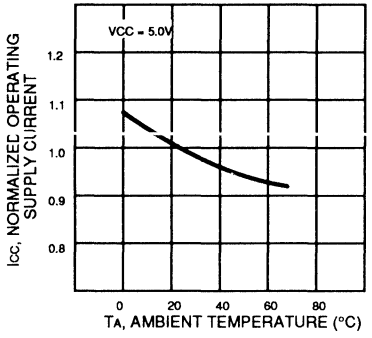


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

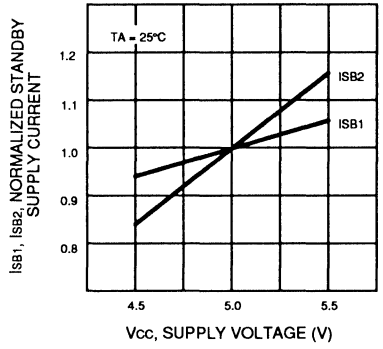


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

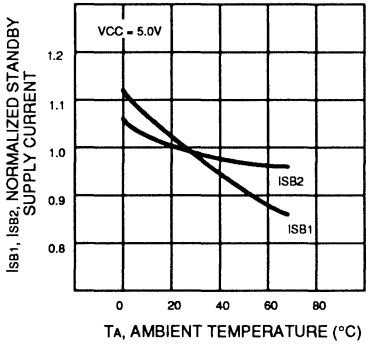
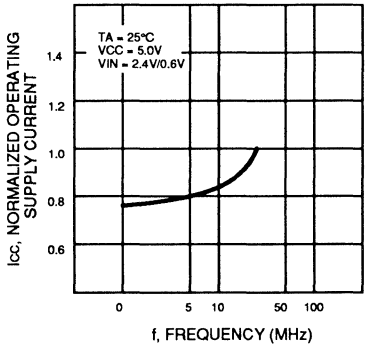


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

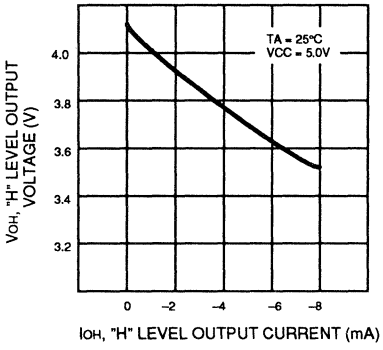


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

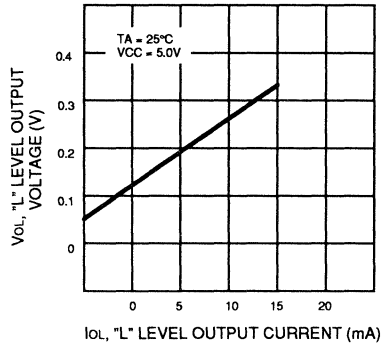


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

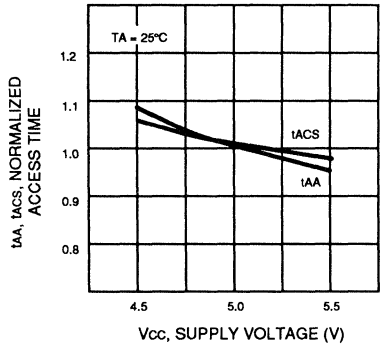


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

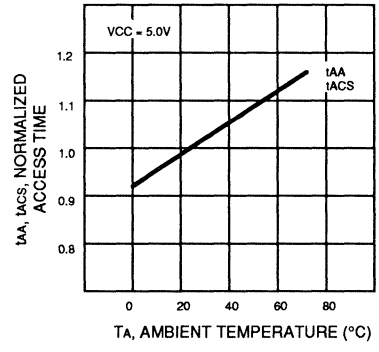
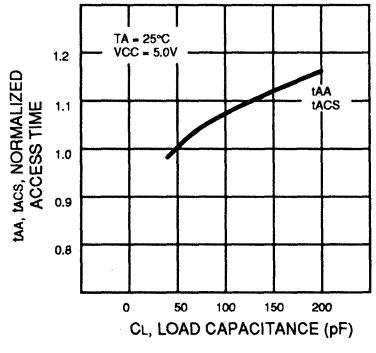
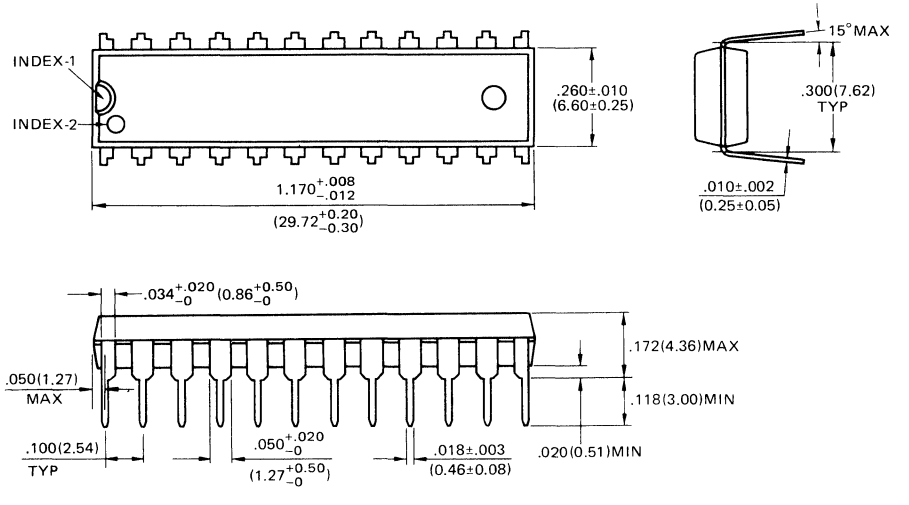


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

24-LEADS PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)

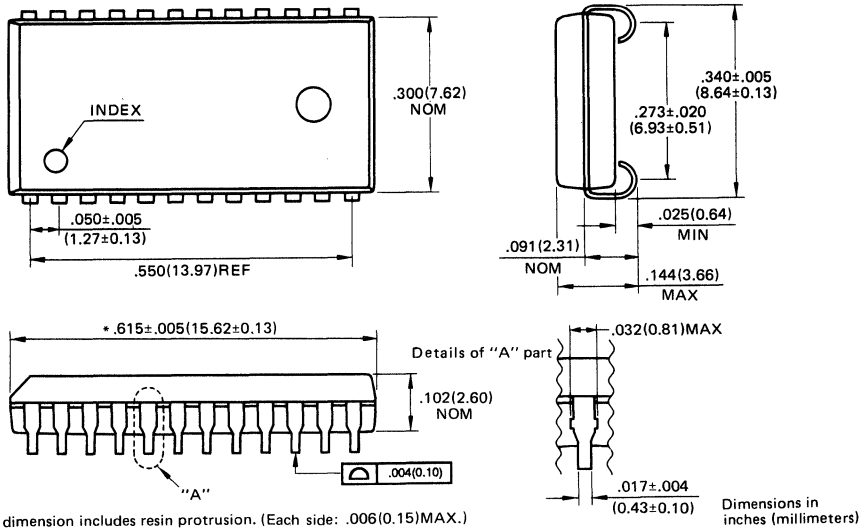


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

1

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



Dimensions in inches (millimeters)

* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

MB 81C86-55
MB 81C86-70

September 1986
Edition 1.0

1

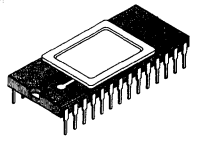
64K x 4 BIT(262,144-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

PRELIMINARY

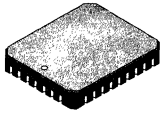
The Fujitsu MB 81C86 is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. The memory utilizes asynchronous and requires single +5V power supply. All pins are TTL compatible.

The MB 81C86 is ideally suited for use in large computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 65,536 words x 4 bits
- Fast access time: $t_{AA} = t_{ACS}$ = 55 ns max. (MB 81C86-55)
  $t_{AA} = t_{ACS}$ = 70 ns max. (MB 81C86-70)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Separate data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby)
- Standard 28-pin DIP: (Suffix: -C)
- Standard 32-pad LCC: (Suffix: -CV)

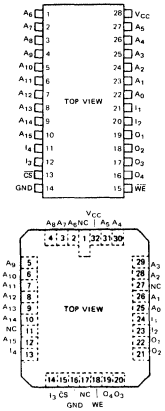


CERAMIC PACKAGE
DIP-28C-A07



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

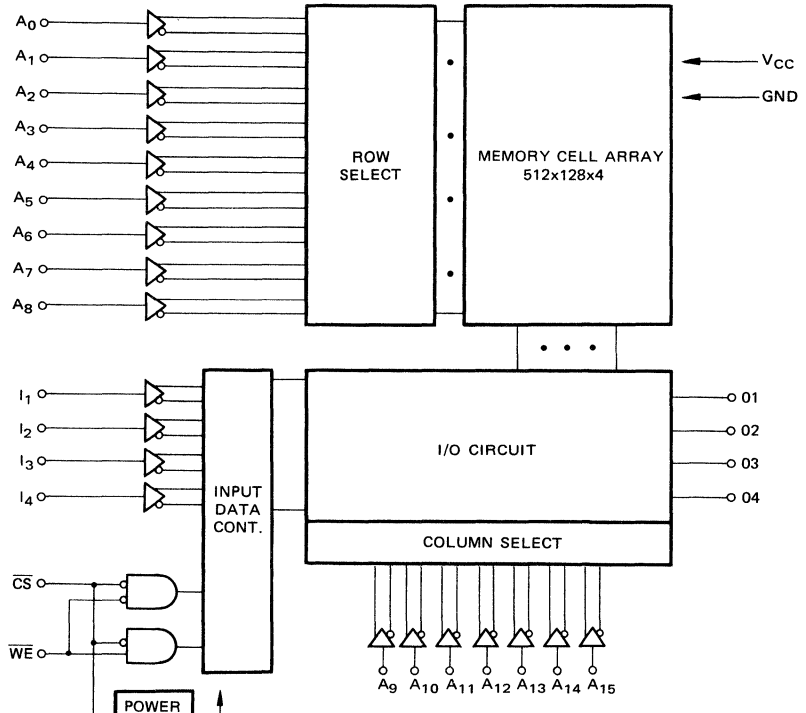
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.0 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81C86 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT}= 0V)	C_{OUT}			8	pF
Input Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

1

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 -3.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = -0.5 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB}		10	mA	$\overline{CS} = V_{IH}$ V_{IN} = 0 V to V_{CC}
Operating Supply Current	I_{CC}		100	mA	Cycle = Min., I_{OUT} = 0 mA $\overline{CS} = V_{IL}$
Input Leakage Current	I_{LI}	-5	5	μA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-5	5	μA	$\overline{CS} = V_{IH}$ V_{OUT} = 0 V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA
Peak Power-on Current	I_{PO}		40	mA	V_{CC} = 0V to V_{CC} MAX. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.

Note: All voltages are referenced to GND

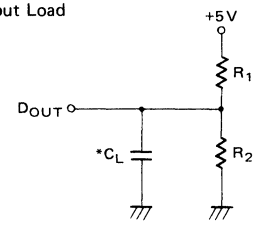
Fig. 2 – AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V

Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)

Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.2V

Output Load



*Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}

1

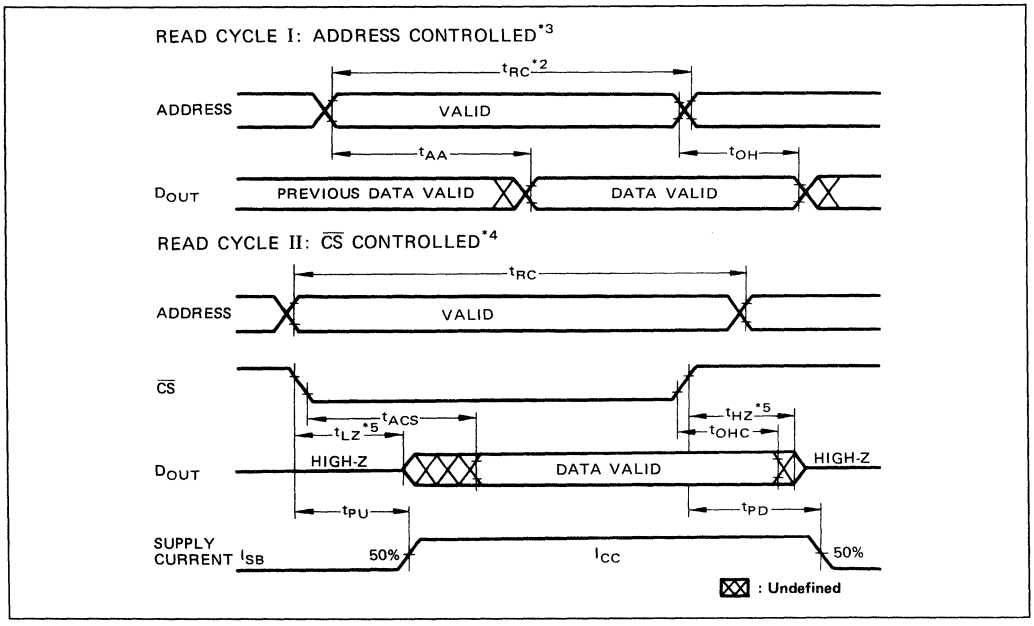
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	55		70		ns
Address Access Time*3	t_{AA}		55		70	ns
$\overline{CS}$ Access Time*4	t_{ACS}		55		70	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	5		5		ns
Chip Selection to Output Low-Z*5	t_{LZ}	10		10		ns
Chip Deselection to Output High-Z*5	t_{HZ}	5	25	5	25	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		40		40	ns

READ CYCLE TIMING DIAGRAM*1



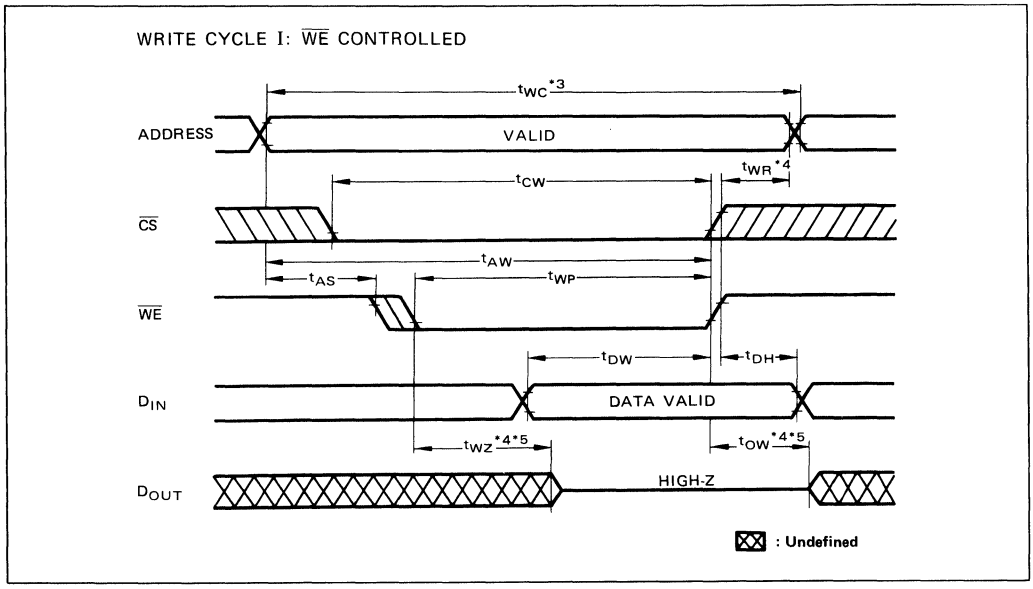
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

1

WRITE CYCLE *1*2

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	55		70		ns
Address Valid to End of Write	t_{AW}	45		50		ns
Chip Select to End of Write	t_{CW}	45		50		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	5		5		ns
Write Pulse Width	t_{WP}	30		35		ns
Address Setup Time	t_{AS}	5		5		ns
Write Recovery Time*4	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}	0	25	0	25	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5	30	5	35	ns

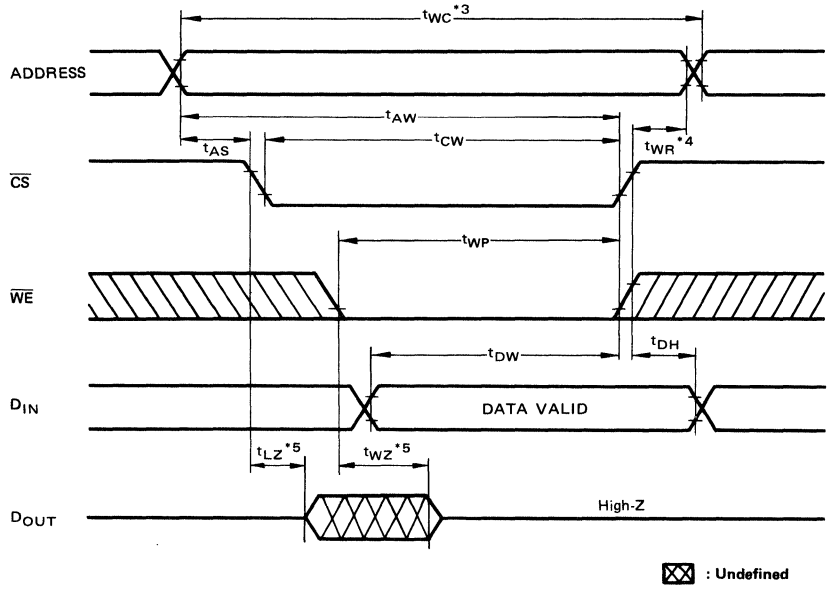
WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

1

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



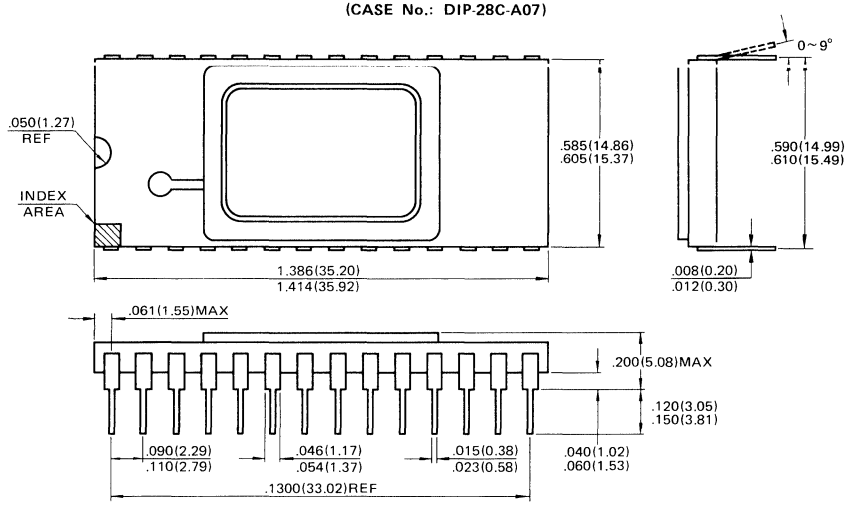
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified Load II in Fig.2.

1

PACKAGE DIMENSIONS

(Suffix: -C)

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A07)



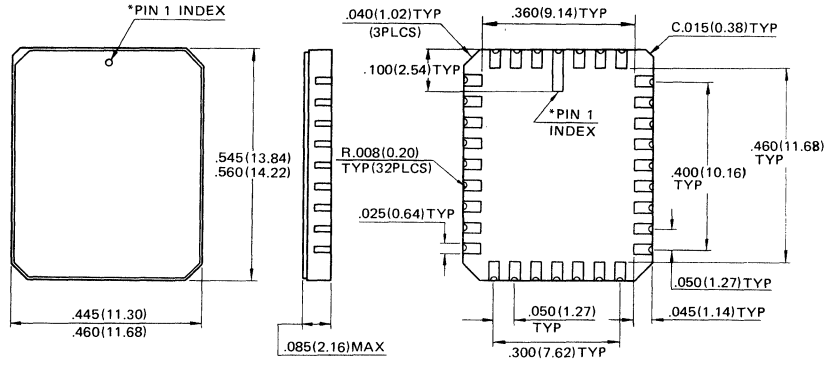
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -CV)

1

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice

FUJITSU

CMOS 294912-BIT STATIC RANDOM ACCESS MEMORY

MB8289-25 MB8289-35

April 1989
Edition 1.0

1

32K x 9-BIT STATIC RANDOM ACCESS MEMORY WITH PARITY GENERATOR AND CHECKER

The Fujitsu MB8289 is 32768 words x 9 bits high speed static random access memory with parity generator and checker, fabricated with CMOS technology. To obtain smaller chip, cell consists of NMOS transistors and resistors therefore this device is assembled in 300 mil DIP and has such small power dissipation as 605mW max.
All pins are TTL compatible and single 5 volt power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$ the other deselected packages automatically power down.
All devices offer the advantages of low power dissipation, low cost, and high performance.

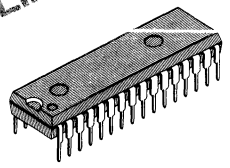
- Organization: 32768 words x 9 bits
- Static operation: no clocks or timing strobe required
- Fast access time:
  $t_{AA} = t_{ACS1}$ = 25ns max,
  t_{ACS2} = 14ns max (MB8287-25)
  $t_{AA} = t_{ACS1}$ = 35ns max,
  t_{ACS2} = 15ns max (MB8287-35)
- Low power consumption:
  715mW max. (Operating) for 25ns
  605mW max. (Operating) for 35ns
  138mW max. (TTL Standby)
  83mW max. (CMOS Standby)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- Internal parity generator and checker.
- All inputs and outputs have protection against static charge
- Standard 32-pin DIP package (300 mil): (Suffix: P–SK)
- Standard 32-pin FPT package (450 mil): (Suffix: PF)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

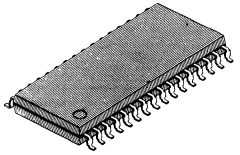
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	–3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	–0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–45 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

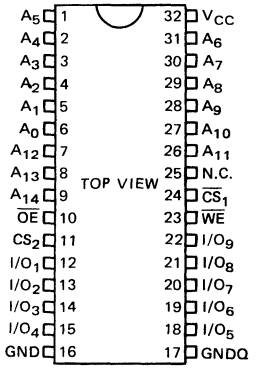


PLASTIC PACKAGE (DIP-32P-M02)



PLASTIC PACKAGE (FPT-32P-M02)

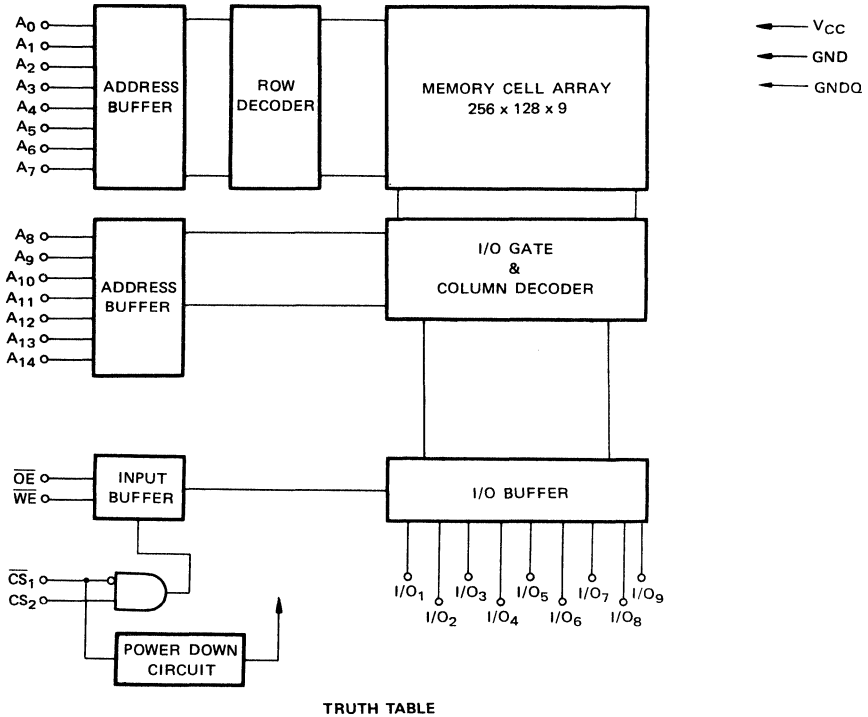
PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB8289 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	C_{I1}			8	pF
Input Capacitance (Other Input)	V_{IN} = 0V	C_{I2}			7	pF
I/O Capacitance	$V_{I/O}$ = 0V	$C_{I/O}$			8	pF

1

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

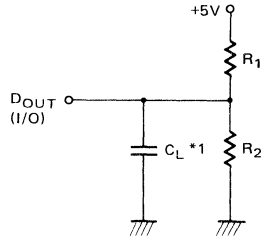
(Recommended operating conditions unless otherside noted.)

Parameter		Symbol	Test Conditions	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS_1} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS_1} = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	I_{OUT} = 0mA, $\overline{CS_1} = V_{IL}$ Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	-5	5	μA
Output Leakage current		$I_{LI/O}$	$\overline{CS_1} = V_{IH}$ = or $\overline{CS_2} = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}	-5	5	μA
Input Low Voltage		V_{IL}		-2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	I_{OH} = -4mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL} = 8mA		0.4	V

Note: *1 -2.0V Min. for pulse width less than 20ns. (V_{IL} min. = -0.5V at DC level)
All voltages are referenced to GND.

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.2V
- Output Load:



*1 Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ} and t_{OHZ}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ} and t_{OHZ}

1

AC CHARACTERISTICS

READ CYCLE*1

(Recommended operating conditions unless otherwise noted)

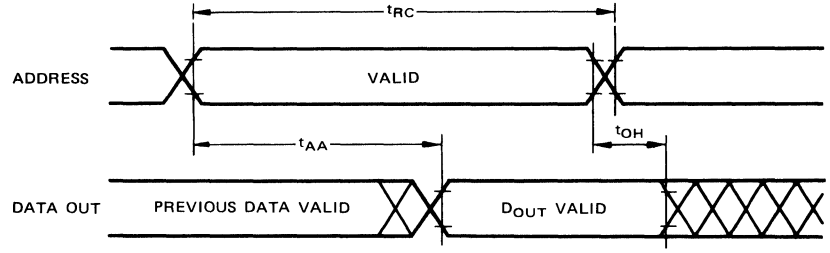
Parameter	Snymbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS}_1$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Access Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS}_1$ *4*5	t_{LZ1}	5		8		ns
Output Active from CS_2 *4*5	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$ *4*5	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS}_1$ *4*5	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2 *4*5	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$ *4*5	t_{OHZ}	1	15	1	15	ns

Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

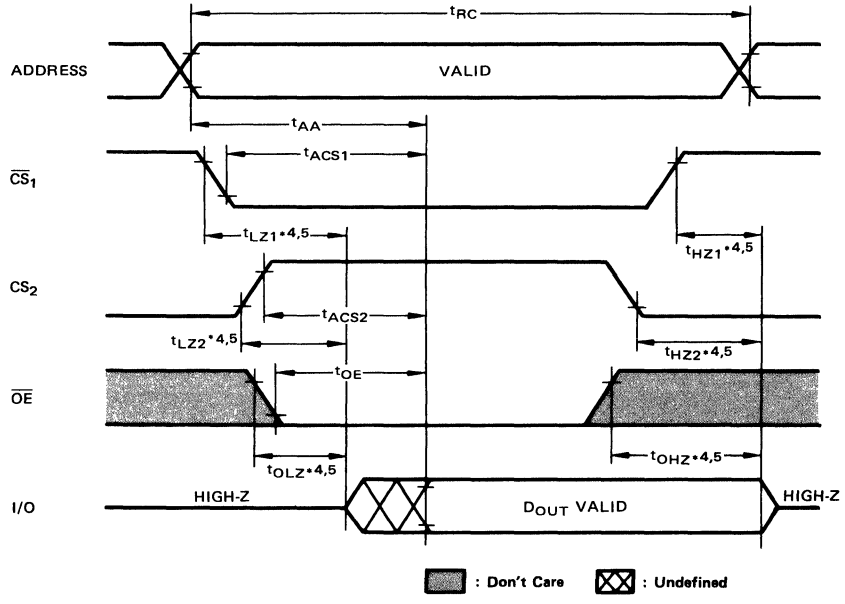
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2



READ CYCLE: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1

Parameter	Symbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4*5	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4*5	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All Write Cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of Write Mode.

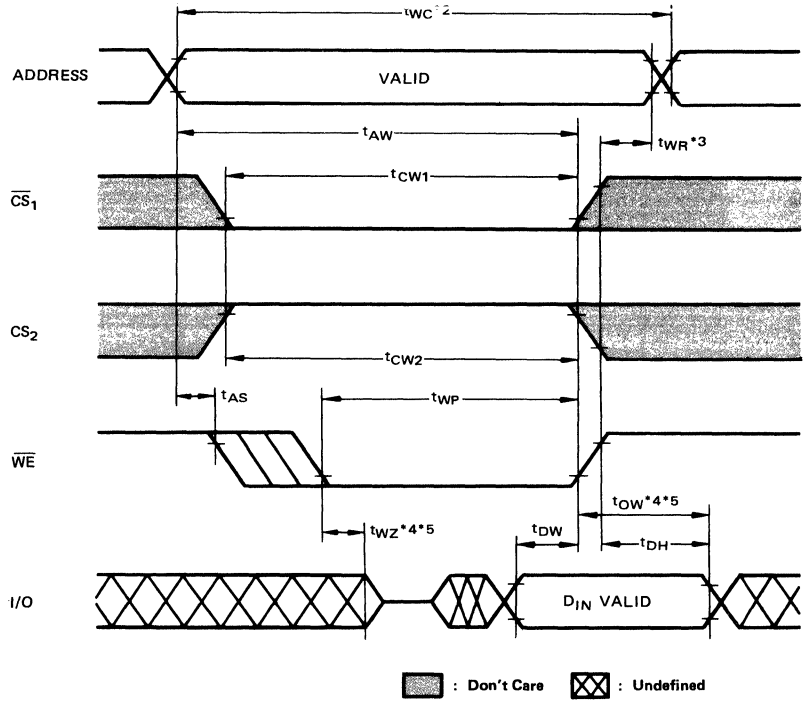
*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM *1,*6,*7

WRITE CYCLE No. 1 ($\overline{WE}$ CONTRORRED)

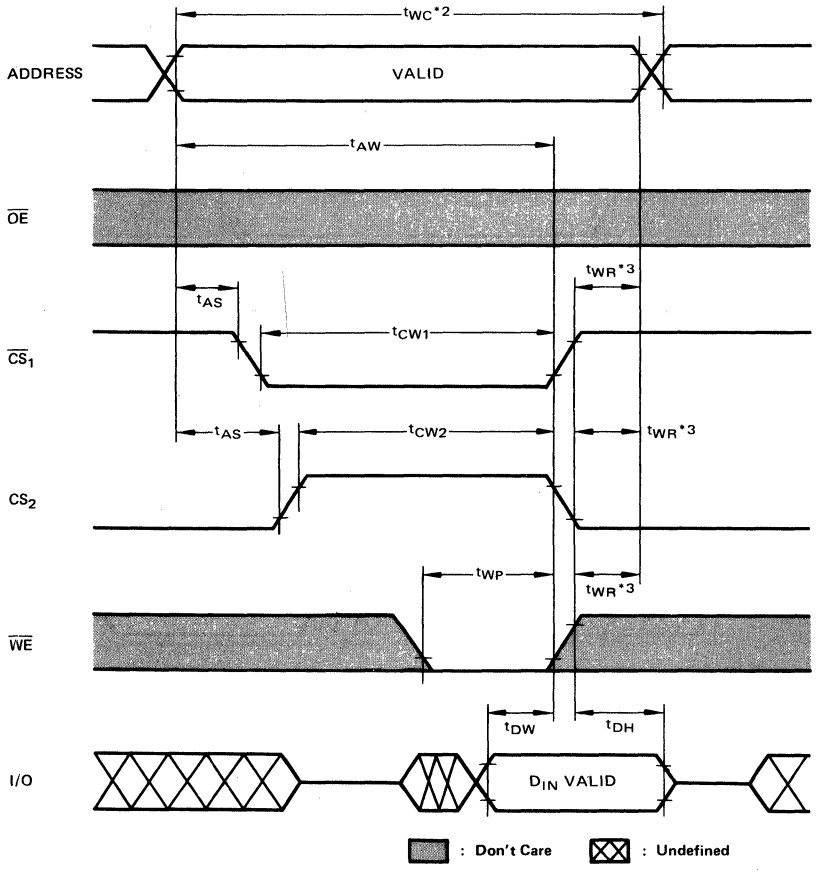


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM *1,*6,*7

WRITE CYCLE No. 2 ($\overline{CS_1}$, CS_2 CONTROLLED)

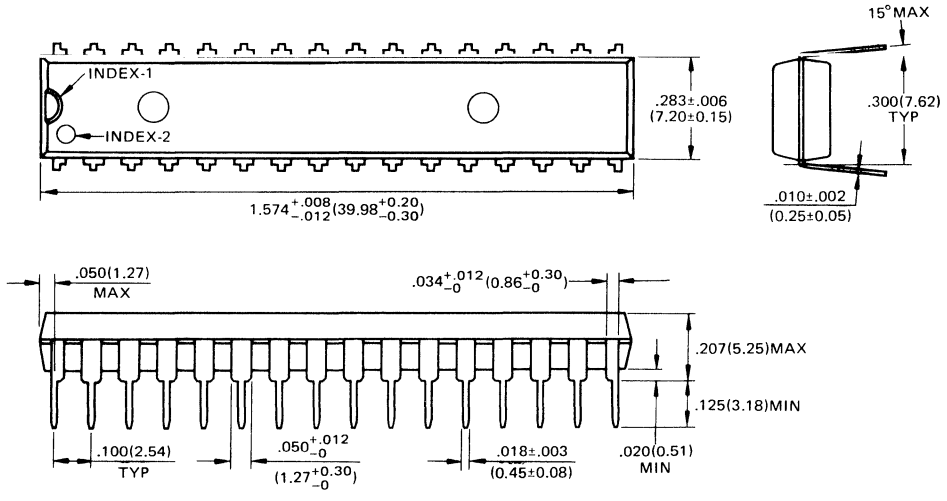


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

1

PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)

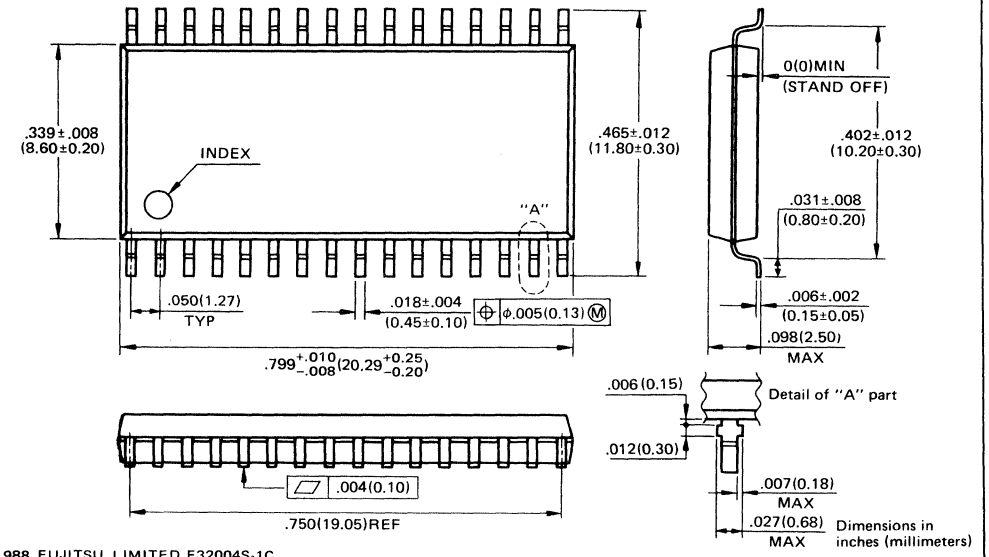


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

1

32-LEAD PLASTIC SMALL OUTLINE PACKAGE
(CASE No.: FPT-32P-M02)



Section 2

High-Speed BiCMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
2–3	MB82B001–25	25	1048576 bits	28-pin Plastic LCC
	–35	35	(1048576w x 1b)	
2–11	MB82B005–25	25	1048576 bits	28-pin Plastic LCC
	–35	30	(262144w x 4b)	
2–19	MB82B006–25	25	1048576 bits	32-pin Plastic LCC
	–35	35	(262144w x 4b)	
2–27	MB82B71—15	15	65536 bits	22-pin Plastic DIP, LCC
	–20	20	(65536b x 1b)	24-pin Plastic LCC
2–37	MB82B74–15	15	65536 bits	22-pin Plastic DIP
	–20	20	(16384w x 4b)	22-pad Ceramic LCC
2–45	MB82B75–15	15	65536 bits	24-pin Plastic DIP, LCC
	–20	20	(16384w x 4b)	28-pad Ceramic LCC
2–55	MB82B79–15	15	73728 bits	28-pin Plastic DIP, FPT
	–20	20	(8192w x 9b)	
2–65	MB82B81–15	15	262144 bits	24-pin Plastic DIP, LCC
	–20	20	(262144w x 1b)	
2–73	MB82B84–15	15	262144 bits	24-pin Plastic DIP, LCC
	–20	20	(65536w x 4b)	

2

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB82B001-25/-35
1M BIT HIGH SPEED BI-CMOS SRAM

1,048,576 WORDS x 1 BIT HIGH SPEED BI-CMOS STATIC RANDOM ACCESS MEMORY

ADVANCE INFO.

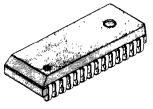
The Fujitsu MB82B001 is 1,048,576 words x 1 bit static random access memory fabricated with a Bi-CMOS process technology. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required. The MB82B001 has 400mil plastic small out-line J-lead(SOJ) as package option.

The MB82B001 is ideally suited for use in dataprocessing systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high peformance.

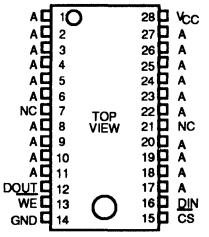
- Organization: 1,048,576 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time: 25ns max. (MB82B001-25)
  35ns max. (MB82B001-35)
- Single +5V(±10%) power supply with low current drain

  Active operation = 120mA max.
  Standby operation = 15mA max. (CMOS level)
  Standby operation = 25mA max. (TTL level)
- Separate data input and output
- TTL compatible inputs and output
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 400 mil width 28-pin SOJ package (Suffix: -PJ)



PLASTIC PACKAGE
LCC-28P-M05

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

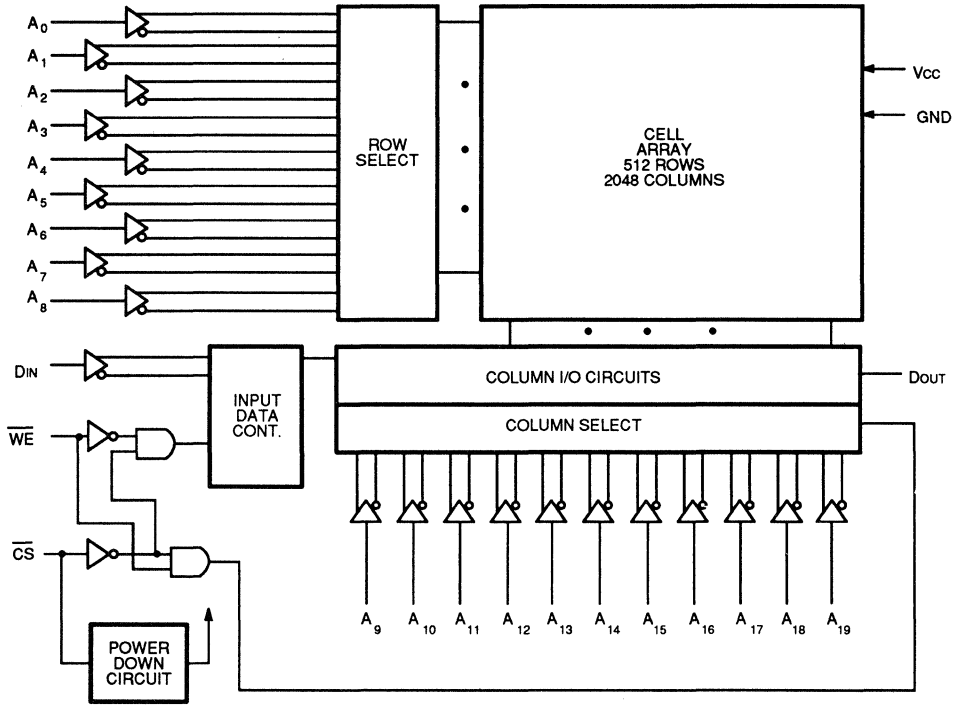
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	-0.5 to +7.0	V
Output Voltage on any pin with to GND	V_{OUT}	-0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB82B001 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A9	Address Input	$\overline{WE}$	Write Enable
D_{IN}	Data Input	V_{CC}	Power Supply(+10%)
D_{OUT}	Data Output	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC} V_{CC} = Max.	I_{LI}	–1		1	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = Max.	I_{LO}	–1		1	µA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	I_{CC1}		50	80	mA
	V_{CC} = Max., $\overline{CS}$ = V_{IL} Cycle = Min., I_{OUT} = 0mA	I_{CC2}		80	120	
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ ≥ V_{CC} –0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	I_{SB1}		2	15	mA
	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}		10	25	
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4			V
Peak Power on Current *1	V_{CC} = 0V to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	I_{PO}			50	mA
Input Low Voltage		V_{IL}	–0.5 *2		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V

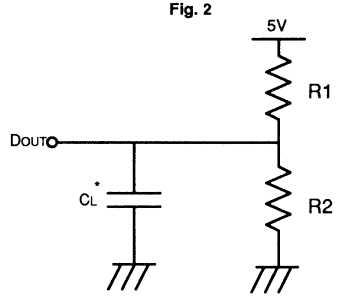
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

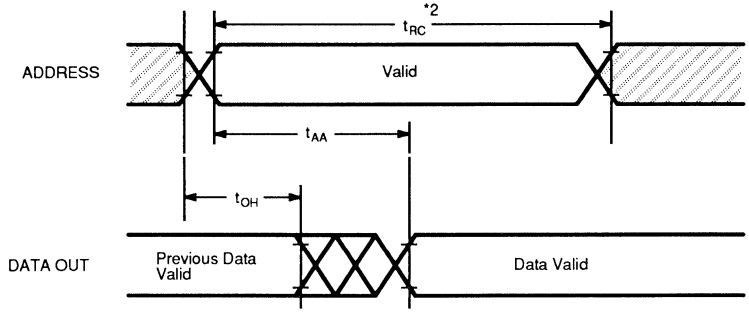
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	t_{RC}	25		35		ns
Address Access Time *3	t_{AA}		25		35	ns
Chip Select Access Time *4	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *5 *6	t_{LZ}	5		5		ns
Chip Deselection to Output in High-Z *5 *6	t_{HZ}	2	15	2	15	ns
Chip Selection to Power Up time	t_{PU}	0		0		ns
Chip Deselection to Power Down	t_{PD}		20		30	ns

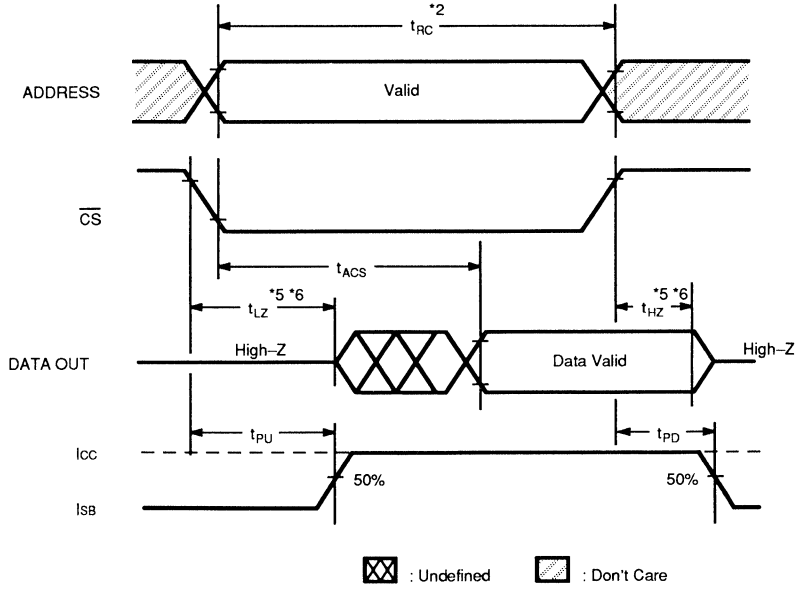
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



: Undefined : Don't Care

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

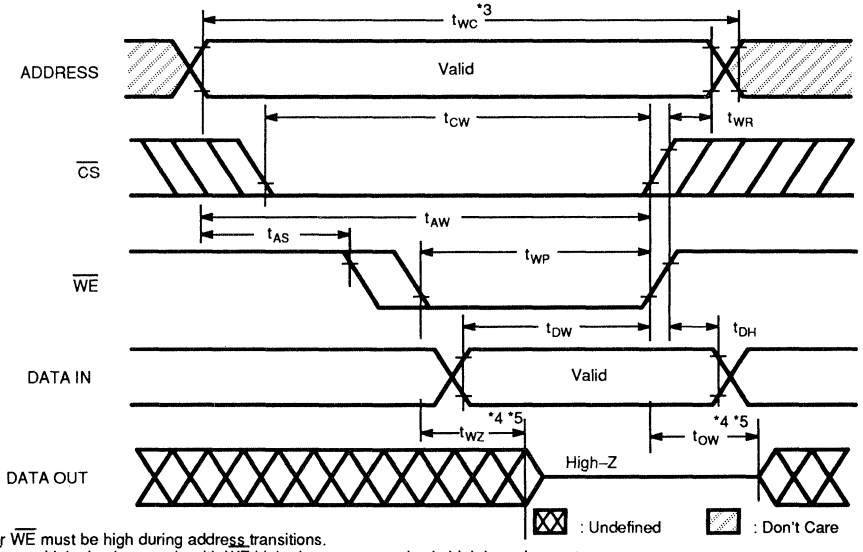
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	10		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

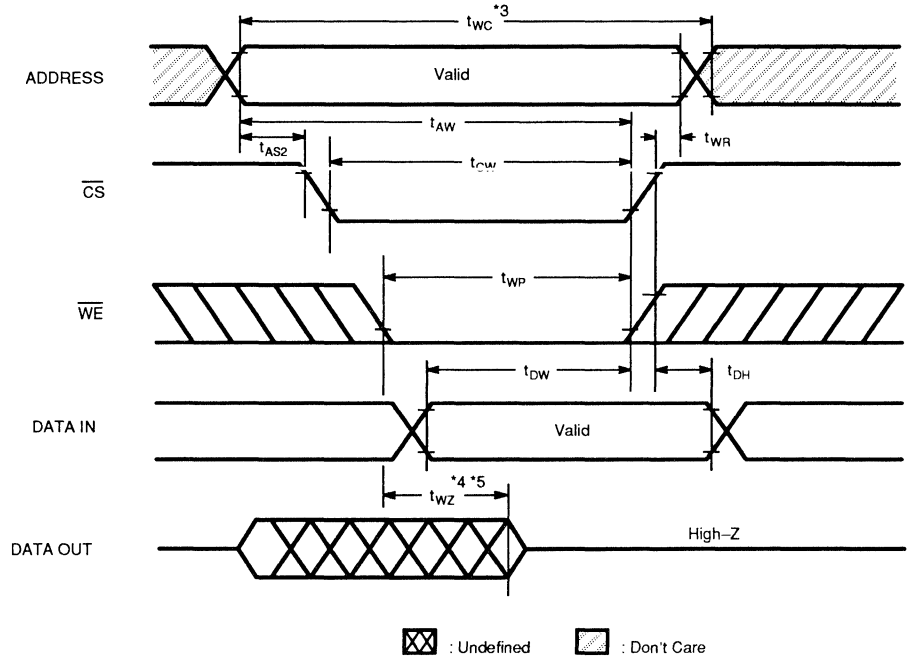
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

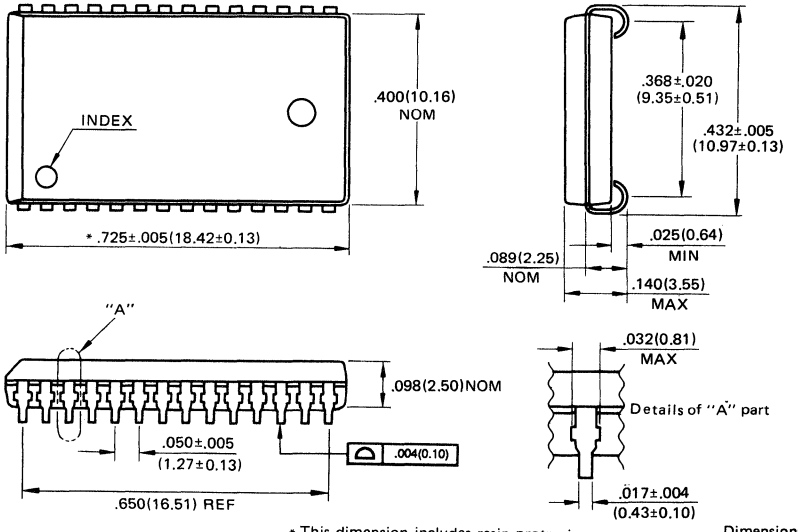


*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

2

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)



* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB82B005-25/-35
1M BIT HIGH SPEED BI-CMOS SRAM

262,144 WORDS x 4 BITS HIGH SPEED BI-CMOS STATIC RANDOM ACCESS MEMORY

ADVANCE INFO.

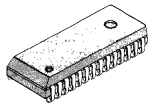
The Fujitsu MB82B005 is 262,144 words x 4 bits static random access memory fabricated with a Bi-CMOS process technology. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required. The MB82B005 has 400mil plastic small out-line J-lead(SOJ) as package option.

The MB82B005 is ideally suited for use in dataprocessing systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high peformance.

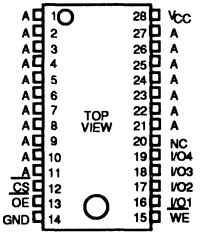
- Organization: 262,144 words x 4 bits
- Static operation: No clocks or refresh required
- Fast access time: 25ns max. (MB82B005-25)
  35ns max. (MB82B005-35)
- Single +5V(±10%) power supply with low current drain

  Active operation = 120mA max.
  Standby operation = 15mA max. (CMOS level)
  Standby operation = 25mA max. (TTL level)
- Common data input and output
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 400 mil width 28-pin SOJ package (Suffix: -PJ)



PLASTIC PACKAGE
LCC-28P-M05

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

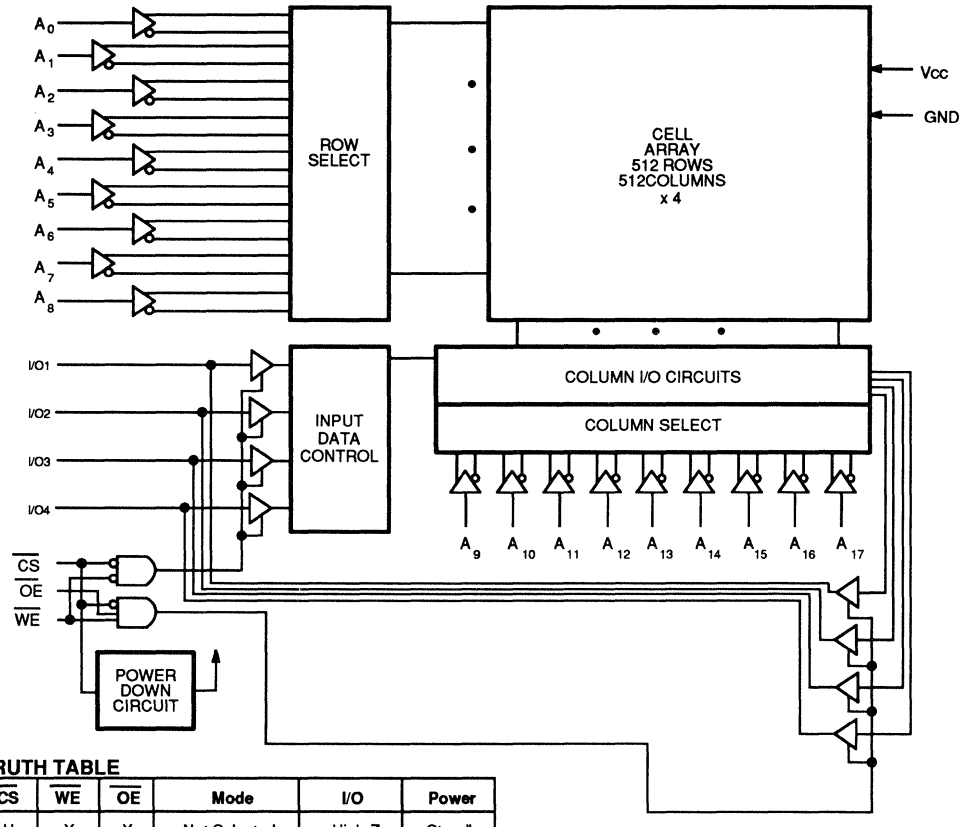
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	-0.5 to +7.0	V
Output Voltage on any pin with to GND	V_{OUT}	-0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB82B005 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Desable	High-Z	Active
L	L	X	Writte	DIN	Active
L	H	L	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O4	Data Input/Output	Vcc	Power Supply(±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to Vcc Vcc = Max.	ILI	–1		1	µA
Output Leakage Current	$\overline{CS}$ = VIH, or $\overline{OE}$=VIH VOUT = 0V to Vcc Vcc = Max.	ILO	–1		1	µA
Active Supply Current	$\overline{CS}$ = VIL, IOUT = 0mA Vcc = Max., VIN = VIL or VIH	ICC1		50	80	mA
	Vcc = Max., $\overline{CS}$ = VIL Cycle = Min., IOUT = 0mA	ICC2		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ ≥ Vcc –0.2V VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V	ISB1		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = VIH	ISB2		10	25	
Output Low Voltage	IOL = 8 mA	VOL			0.4	V
Output High Voltage	IOH = –4 mA	VOH	2.4			V
Peak Power on Current *1	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or VIH Min.	IPO			50	mA
Input Low Voltage		VIL	–0.5 *2		0.8	V
Input High Voltage		VIH	2.2		6.0	V

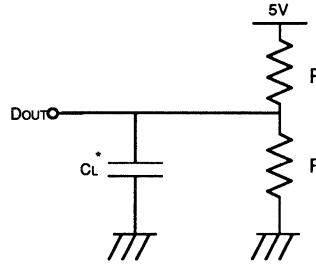
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ

AC CHARACTERISTICS

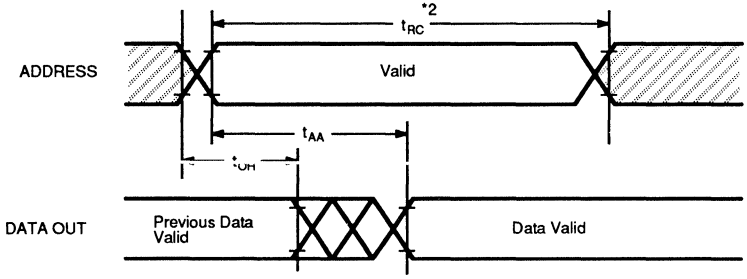
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	tRC	25		35		ns
Address Access Time *3	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Enable Access Time	tOE		10		15	ns
Output Hold from Address Change	tOH	5		5		ns
Chip Selection to Output in Low-Z *5 *6	tCLZ	5		5		ns
Chip Selection to Output in High-Z *5 *6	tCHZ	2	15	2	15	ns
Output Enable to Output in Low-Z *5 *6	tOLZ	0		0		ns
Output Enable to Output in High-Z *5 *6	tOHZ	0	15	0	15	ns
Chip Selection to Power Up time	tPU	0		0		ns
Chip Deselection to Power Down	tPD		20		30	ns

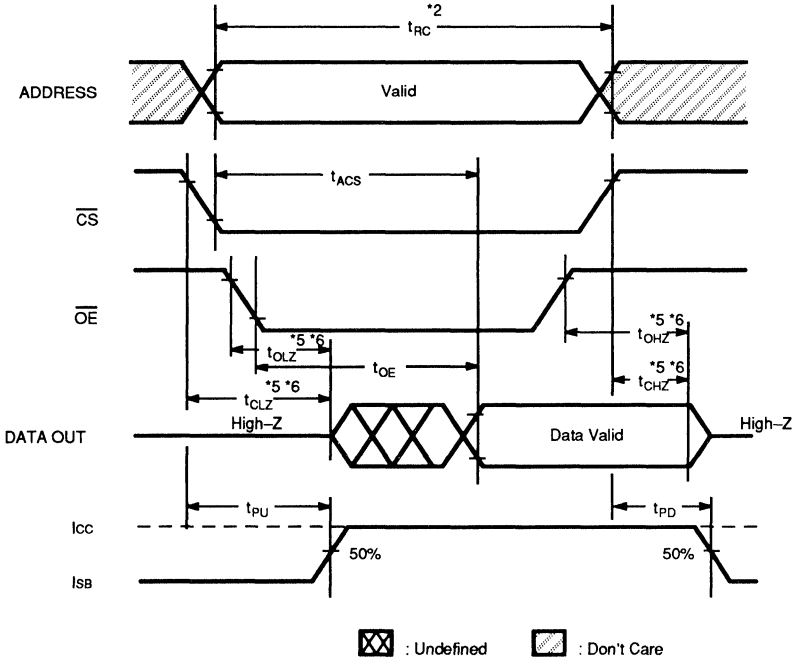
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL} $\overline{OE}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



: Undefined : Don't Care

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}, $\overline{OE}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

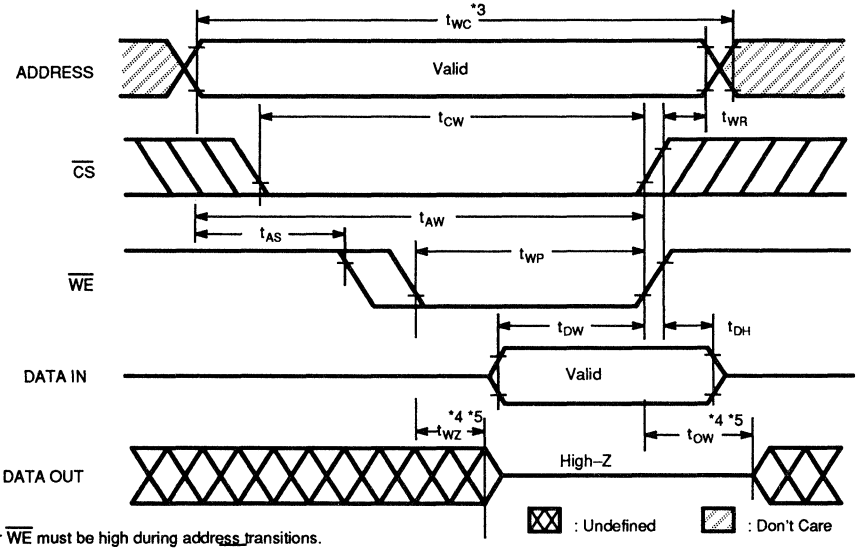
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	8		12		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	8	0	14	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

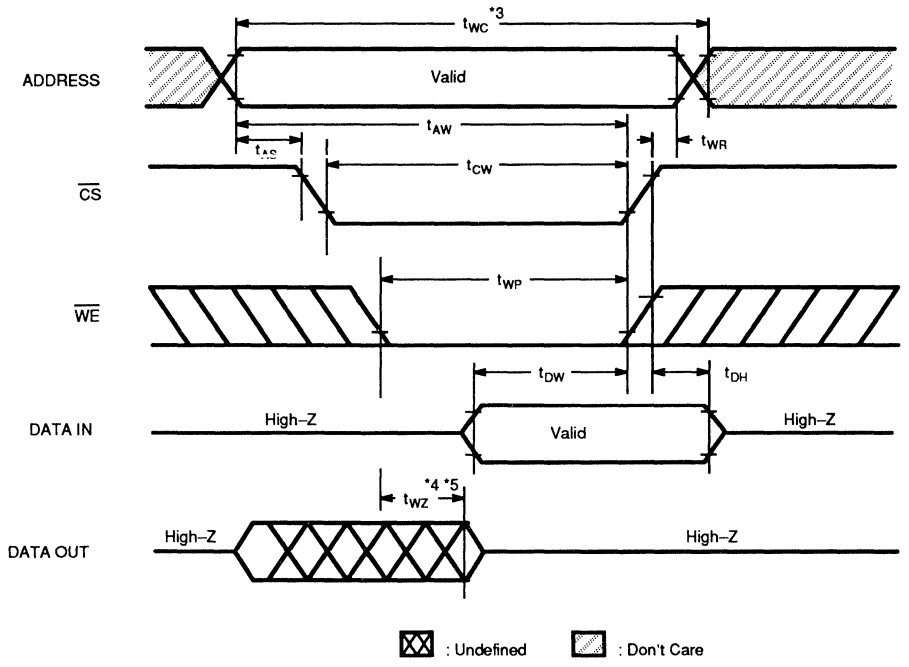
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

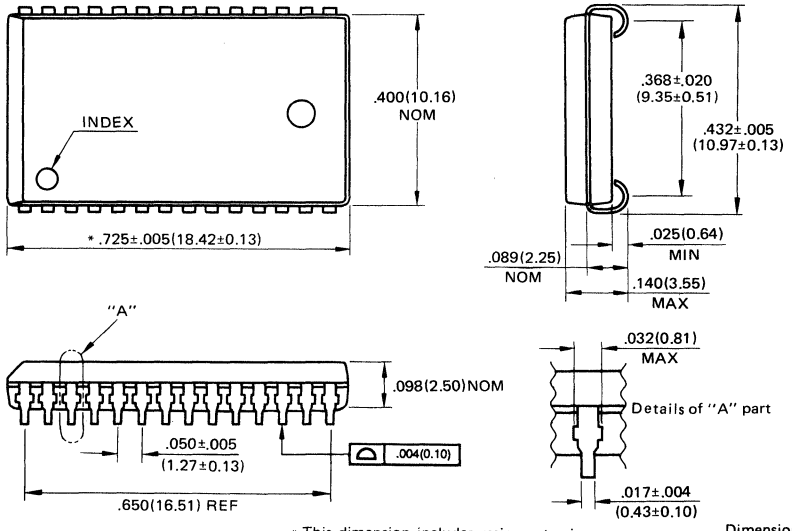


*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

2

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)



* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

November 1989
Edition 1.1

FUJITSU

DATA SHEET

MB82B006-25/-35
1M BIT HIGH SPEED BI-CMOS SRAM

262,144 WORDS x 4 BITS HIGH SPEED BI-CMOS STATIC RANDOM ACCESS MEMORY

ADVANCE INFO.

2

The Fujitsu MB82B006 is 262,144 words x 4 bits static random access memory fabricated with a Bi-CMOS process technology. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required. The MB82B006 has 400mil plastic small out-line J-lead(SOJ) as package option.

The MB82B006 is ideally suited for use in dataprocessing systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high peformance.

- Organization: 262,144 words x 4 bits
- Static operation: No clocks or refresh required
- Fast access time:
  25ns max.(MB82B006-25)
  35ns max.(MB82B006-35)
- Single +5V(±10%) power supply with low current drain

  Active operation = 120mA max.
  Standby operation = 15mA max. (CMOS level)
  Standby operation = 25mA max. (TTL level)

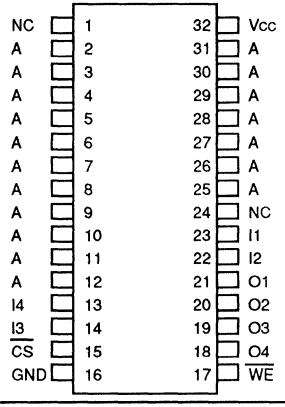
- Separate data input and output
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- 400 mil width 32-pin SOJ package (Suffix: -PJ)

T.B.D.

PLASTIC PACKAGE
LCC-32P-MXX

PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

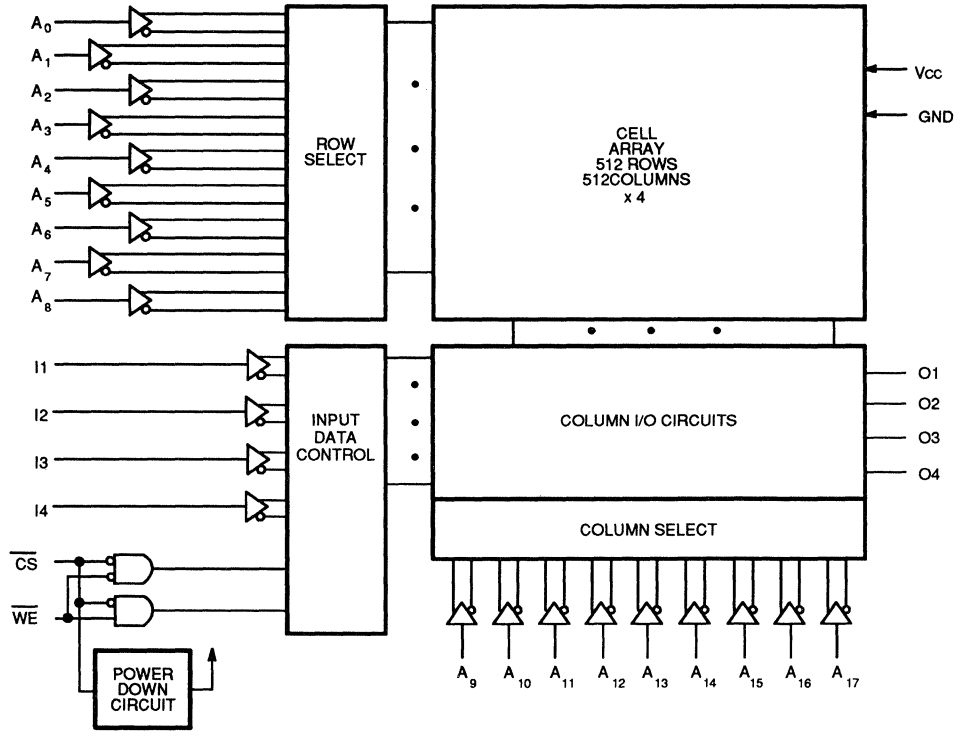
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	-0.5 to +7.0	V
Output Voltage on any pin with to GND	V_{OUT}	-0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB82B006 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High–Z	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
I1 to I4	Data Input	Vcc	Power Supply(±10%)
O1 to O4	Data Output	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to Vcc Vcc = Max.	ILI	–1		1	µA
Output Leakage Current	$\overline{CS}$ = VIH VOUT = 0V to Vcc Vcc = Max.	ILO	–1		1	µA
Active Supply Current	$\overline{CS}$ = VIL, IOUT = 0mA Vcc = Max., VIN = VIL or VIH	ICC1		50	80	mA
	Vcc = Max., $\overline{CS}$ = VIL Cycle = Min., IOUT = 0mA	ICC2		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ ≥ Vcc –0.2V VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V	ISB1		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = VIH	ISB2		10	25	
Output Low Voltage	IOL = 8 mA	VOL			0.4	V
Output High Voltage	IOH = –4 mA	VOH	2.4			V
Peak Power on Current *1	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or VIH Min.	IPO			50	mA
Input Low Voltage		VIL	–0.5 *2		0.8	V
Input High Voltage		VIH	2.2		6.0	V

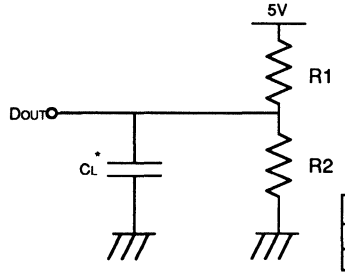
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tLZ, tHZ, tOW and tWZ

*Including Scope and Jig capacitance

AC CHARACTERISTICS

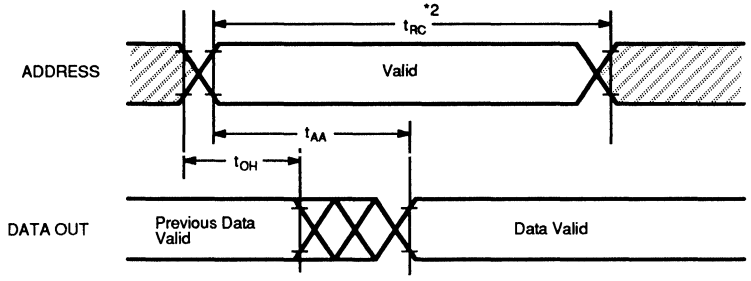
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B006-25		MB82B006-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	t_{RC}	25		35		ns
Address Access Time *3	t_{AA}		25		35	ns
Chip Select Access Time *4	t_{ACS}		25		35	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *5 *6	t_{LZ}	5		5		ns
Chip Selection to Output in High-Z *5 *6	t_{HZ}	2	15	2	15	ns
Chip Selection to Power Up time	t_{PU}	0		0		ns
Chip Deselection to Power Down	t_{PD}		20		30	ns

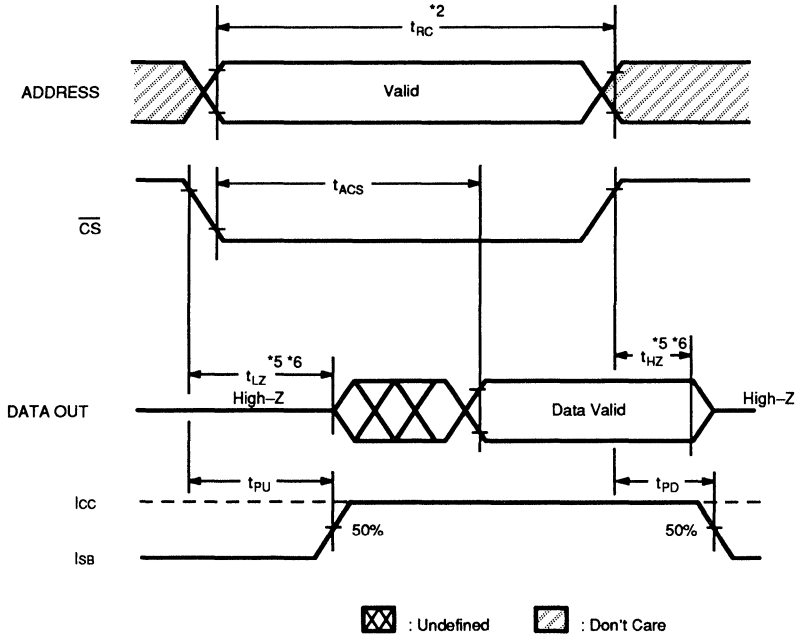
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

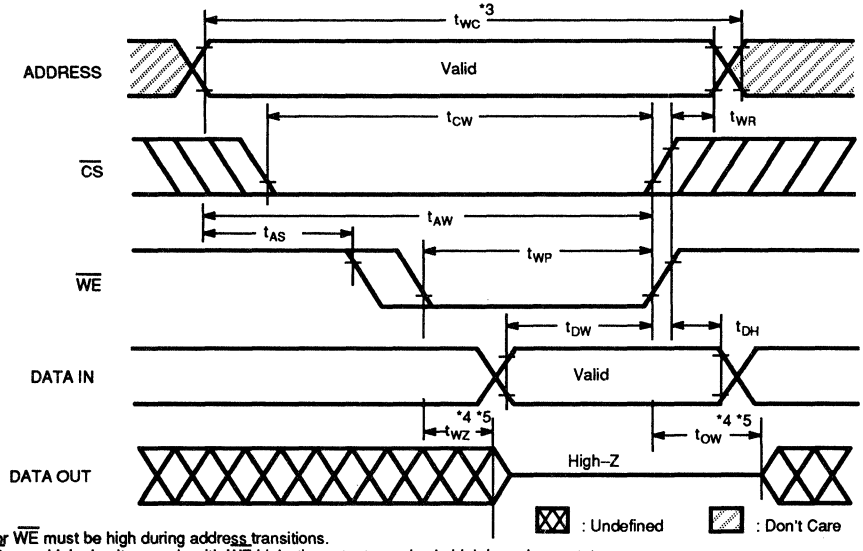
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B006-25		MB82B006-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	10		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

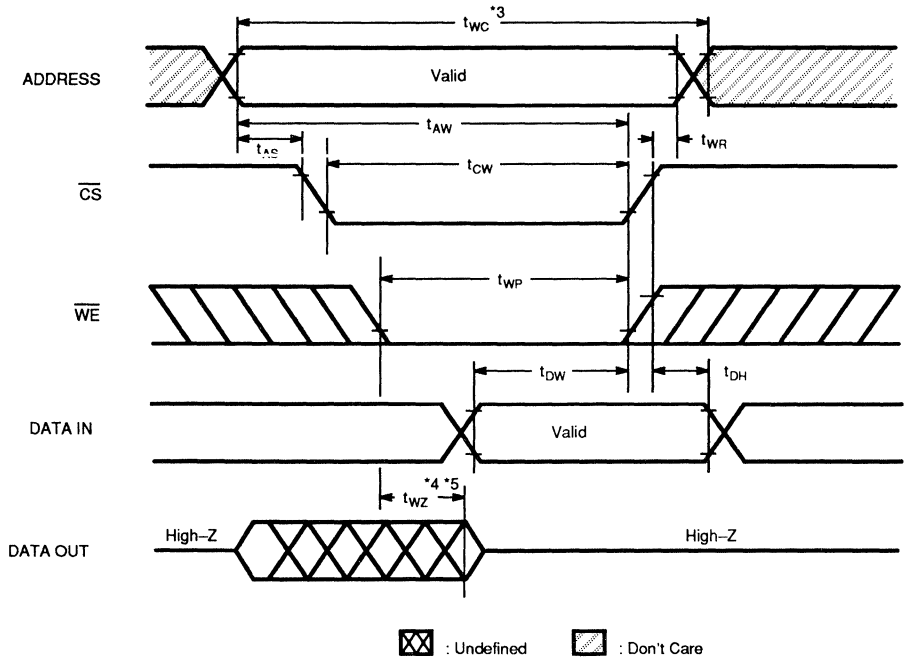
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

2

TS280–A89Z
December 1989

FUJITSU

DATA SHEET

MB82B71-15/-20
64K BIT HIGH SPEED BI-CMOS SRAM

65,536-WORD x 1-BIT Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY

ADVANCE INFO.

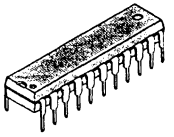
2

The Fujitsu MB82B71 is a 65,536 words by 1 bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi–CMOS technology, and to obtain amaller chip size, cells consist of NMOS transistors and resistors.

MB82B71 has 300mil plastic DIP, leadless chip carrier (LCC) and 300mil plastic small out–line J–lead (SOJ) package as package option. The memory utilizes asynchronous circuitry and requires +5V power supply. All pins are TTL compatible.

The MB82B71 is ideally suited for use in large computer and other applications where fast access time, large–capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.

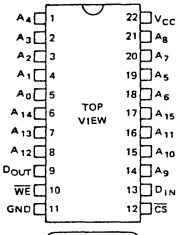
- Organization: 65,536 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time:
  tAA=tACS=15ns max.(MB82B71–15)
  tAA=tACS=20ns max.(MB82B71–20)
- Single=5V(+10%) power supply with low current drain:
  Active operation=120mA max.
  Standby operation=15mA max.(CMOS level)
  Standby operation=30mA max.(TTL level)
- Bi–CMOS peripheral
- TTL compatible inputs/outputs
- Three–state output
- 300 mil width 22–pin plastic Skinny DIP package (Suffix: –P–SK)
- 300 mil width 24–pin plastic SOJ package (Suffix: –PJ)
- 22–pad Leadless Chip Carrier package (Suffix:–CV)
- Pin compatible with MB81C71A

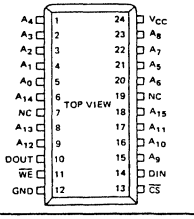


PLASTIC PACKAGE
DIP–22P–M04

PLASTIC PACKAGE
LCC–24P–M02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with to GND		V_{IN}	–0.5 to +7.0	V
Output Voltage on any pin with to GND		$V_{I/O}$	–0.5 to +7.0	V
Power Dissipation		P_D	1.0	W
Output Current		I_{OUT}	±20	mA
Temperature under Bias		T_{BIAS}	–10 to +85	°C
Storage Temperature	Plastic	T_{STG}	–40 to +125	°C
	Ceramic		–65 to +150	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 - MB82B71 BLOCK DIAGRAM

T.B.D

CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			7	pF
Input Capacitance(VIN=0V)	CIN			7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A15	Address input.	$\overline{WE}$	Write Enable.
DIN	Data input.	VCC	Power Supply(+5V±10%).
DOUT	Data output.	GND	Ground.
$\overline{CS}$	Chip Select.		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power Supply Current
H	X	NottSelected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

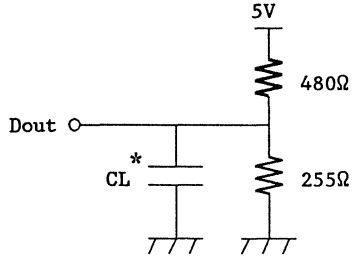
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-5	5	µA
Output Leakage Current	VOUT=GND to VCC $\overline{CS}$=VIH or $\overline{WE}$=VIL	ILI/O	-5	5	µA
Operating Supply Current	$\overline{CS}$=VIL, DOUT=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{CS}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS}$=VIH VCC=min. to max.	ISB2		30	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	-0.5 *1	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{CS}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tLZ, tHZ, tOW and tWZ
Load II	5pF	tLZ, tHZ, tOW and tWZ

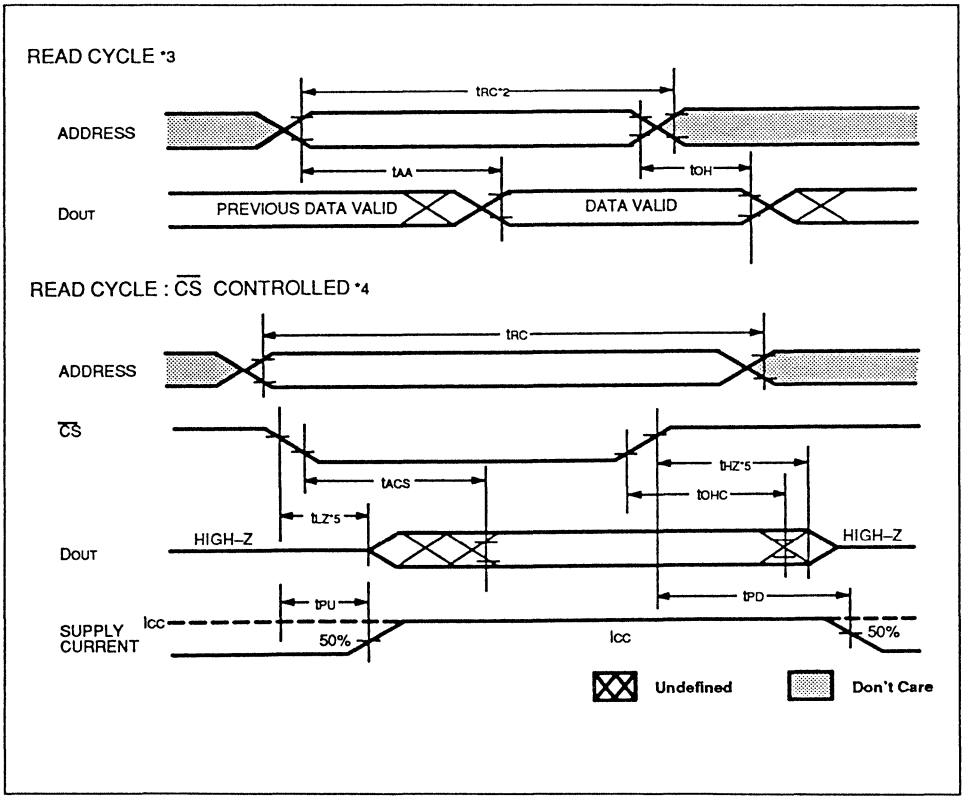
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B71-15		MB82B71-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time	tAA		15		20	ns
/CS Access Time	tACS		15		20	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from /CS	tLZ	3		3		ns
Output High-Z from /CS	tHZ		8		10	ns
Power Up from /CS	tPU	0		0		ns
Power Down from /CS	tPD		15		15	ns

READ CYCLE TIMING DIAGRAM *1



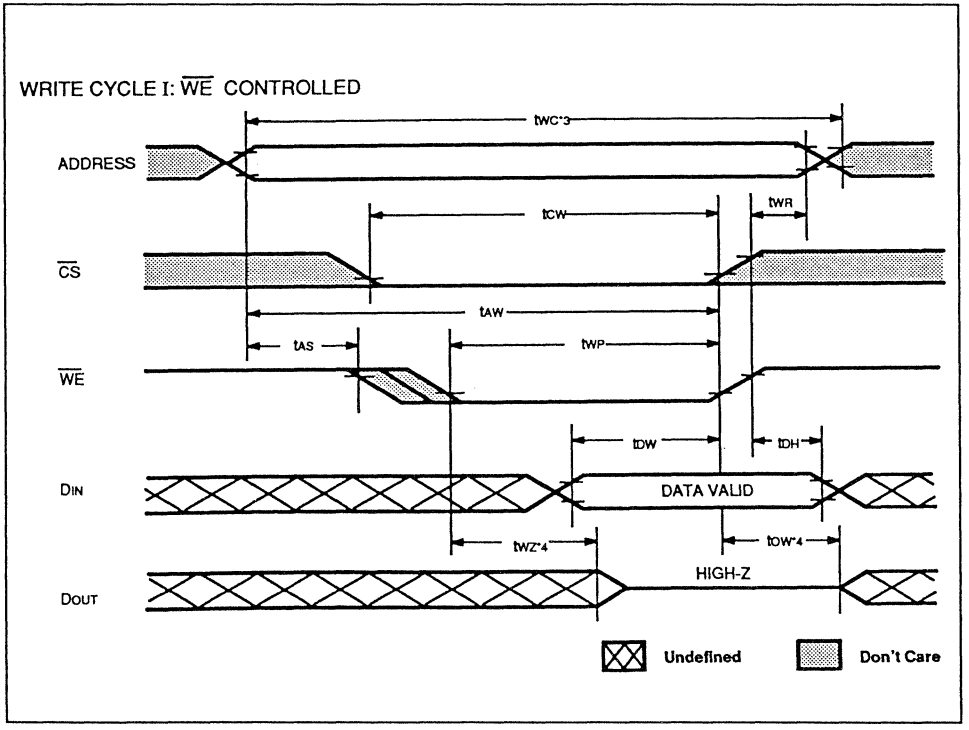
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continously selected, $\overline{CS}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE

Parameter	Symbol	MB82B71-15		MB82B71-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15		20		ns
Address Valid to End of Write	tAW	12		17		ns
/CS to End of Write	tCW	12		17		ns
Data Setup Time	tDW	4		9		ns
Data Hold Time	tDH	0		2		ns
Write Pulse Width	tWP	11		16		ns
Write Recovery Time	tWR	1		3		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from /WE	tOW	0		0		ns
Output High-Z from /WE	tWZ		6		8	ns

2

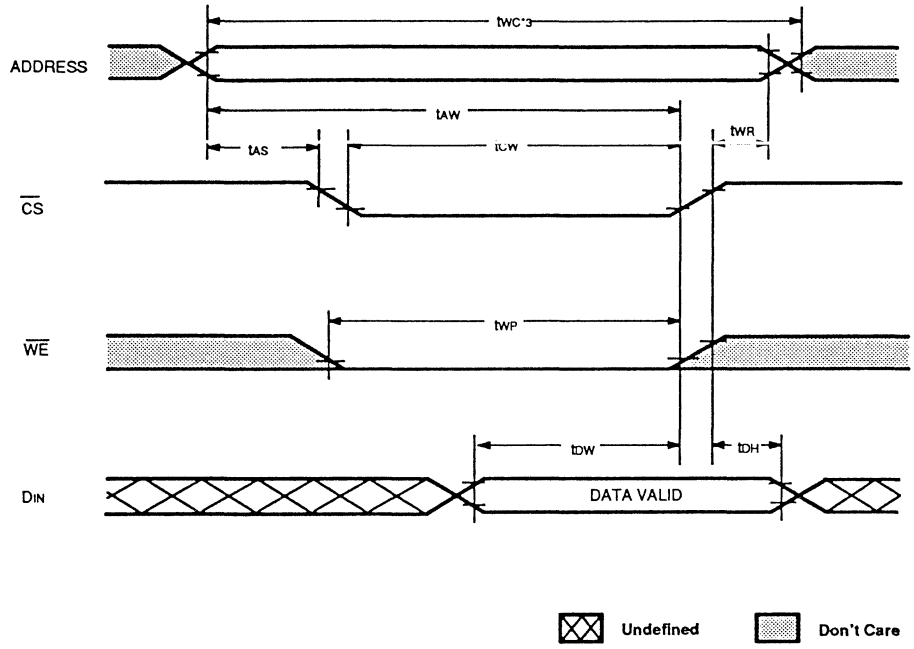
WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM (Continued) *1*2*4

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2

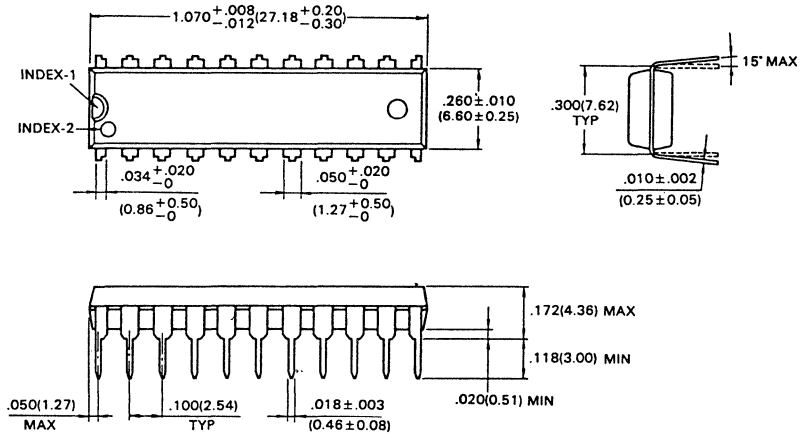


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.

PACKAGE DIMENSIONS

(Suffix:-P-SK)

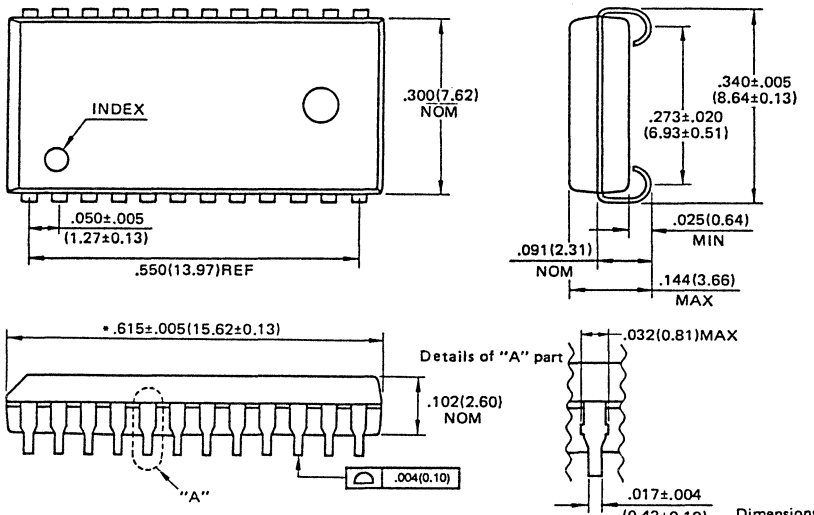
22-LEADS PLASTIC DUAL-IN LINE PACKAGE
(CASE No.:DIP-22P-M04)



Dimensions in inches (millimeters)

(Suffix:-PJ)

24-LEAD PLASTIC SOJ PACKAGE
(CASE No.: LCC-24P-M02)



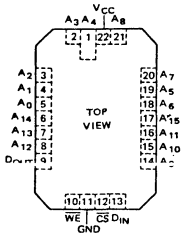
* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)

PACKAGE DIMENSION

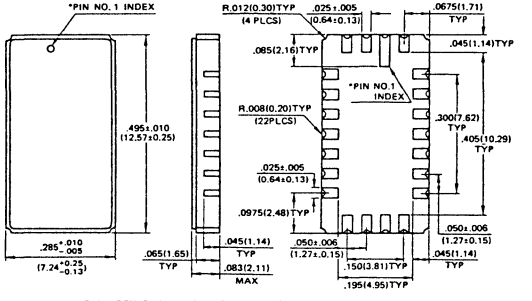
(Suffix:-CV)

CERAMIC PACKAGE
LCC-22C-A01



2

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

2

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB82B74-15/-20
64K-BIT HIGH SPEED BI-CMOS SRAM

16,384 WORDS x 4 BITS Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

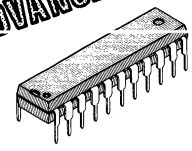
The Fujitsu MB82B74 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

MB82B74 has 300mil plastic DIP and leadless chip carrier (LCC) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

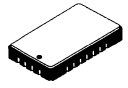
The MB82B74 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost high performance.

- 16,384 words x 4 bits organization
- Fast access time:
  t_{AA}=t_{ACS}=15ns max. (MB82B74-15)
  t_{AA}=t_{ACS}=20ns max. (MB82B74-20)
- Bi-CMOS peripheral
- TTL compatible inputs/outputs
- Completely static operation: No clock required
- Three-state output
- Common data input/output
- Single=5V(±10%) power supply with low current drain
  Active operation=120mA max.
  Standby operation=15mA max. (CMOS level)
  Standby operation=25mA max. (TTL level)
- Standard 22-pin plastic DIP package: Suffix -P
- Standard 22-pad Leadless Chip Carrier: Suffix -CV
- Pin compatible with MB81C74

ADVANCE INFO.

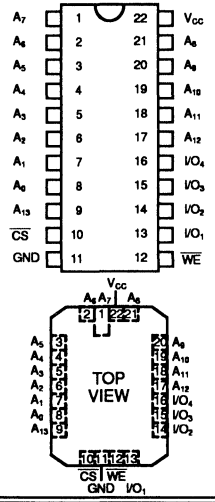


PLASTIC PACKAGE
DIP-22P-M04



CERAMIC PACKAGE
LCC-22C-A01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Values	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage		V_{IN}	-3.5 to +7.0	V
Output Voltage		$V_{I/O}$	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB82B74 BLOCK DIAGRAM

T.B.D.

2

CAPACITANCE (Ta=25° C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{13}	Address input	$\overline{WE}$	Write Enable
I/O_1 to I/O_4	Data input/output	V_{CC}	Power Supply (+5V±10%)
$\overline{CS}$	Chip Select 1	GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O pin	Power Supply Curent
H	X	Standby	High–Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

Legend: H=High level
L=Low level
X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

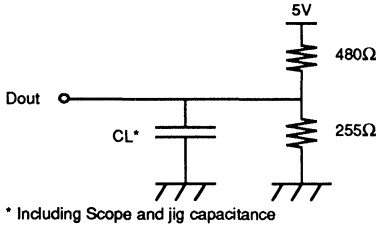
(Recommended operating conditions otherwise noted)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=Max.	I_{LI}	–5	5	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}	$I_{LI/O}$	–5	5	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, I/O=Open Cycle=Min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=Min. to Max. $\overline{CS}$=V_{CC}–0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}–0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH} or V_{IL} V_{CC}=Min. to Max.	I_{SB2}		30	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5 *1	0.8	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.	I_{PO}		50	mA

Note: *1 –2.0V Min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}
Load II	5pF	t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

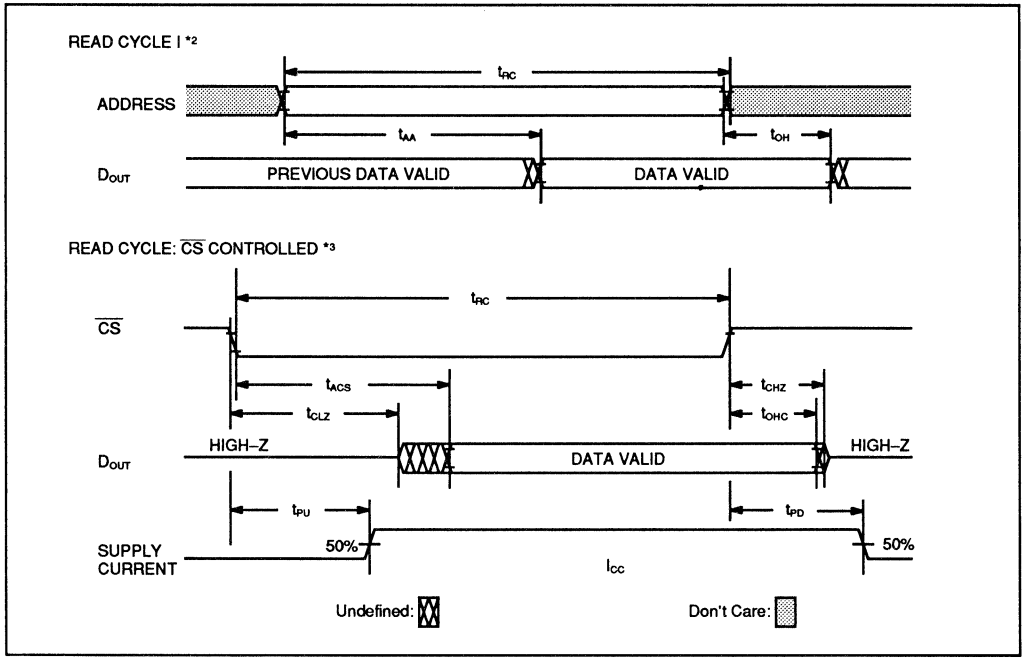
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B74–15		MB82B74–20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time *2	t_{AA}		15		20	ns
$\overline{CS}$ Access Time *3	t_{ACS}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Low–Z from $\overline{CS}$ *4 *5	t_{CLZ}	3		3		ns
Output High–Z from $\overline{CS}$ *4 *5	t_{CHZ}		8		10	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		15		15	ns

READ CYCLE TIMING DIAGRAM *1

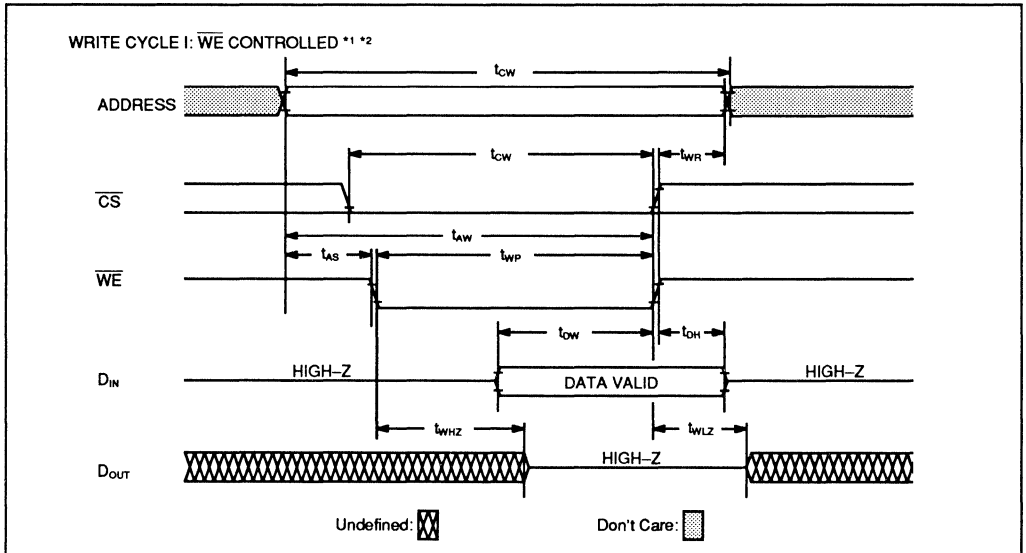


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continously selected, $\overline{CS}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE *1

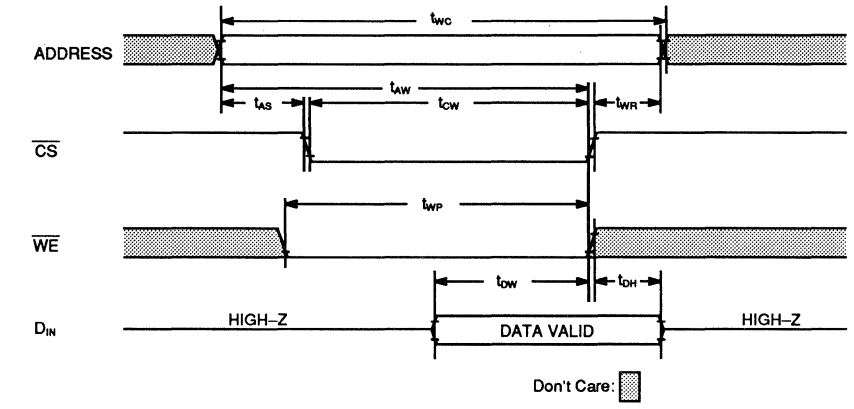
Parameter	Symbol	MB82B74–15		MB82B74–20		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	15		20		ns
Address Valid to End of Write	t_{AW}	12		17		ns
$\overline{CS}$ to End of Write	t_{CW}	12		17		ns
Data Setup Time	t_{DW}	4		9		ns
Data Hold Time	t_{DH}	0		2		ns
Write Pulse Width	t_{WP}	11		16		ns
Write Recovery Time	t_{WR}	1		3		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low–Z from $\overline{WE}$ *3 *4	t_{WLZ}	0		0		ns
Output High–Z from $\overline{WE}$ *3 *4	t_{WHZ}		6		8	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in. Fig2.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1 *2

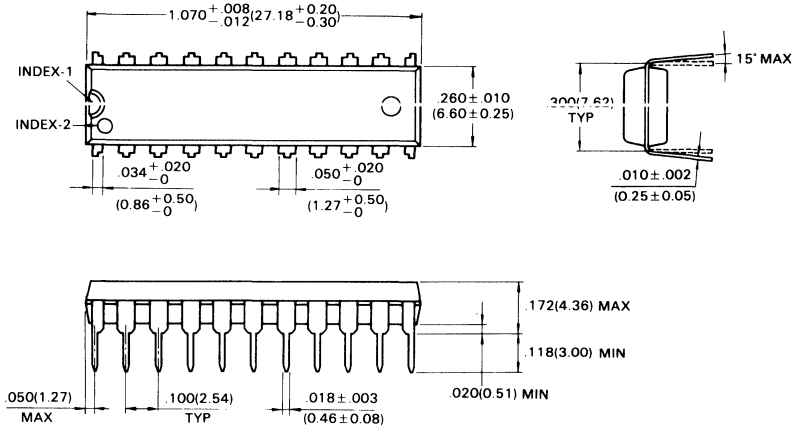


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.

PACKAGE DIMENSIONS

22-LEAD PLASTIC DUAL IN-LINE PACKAGE

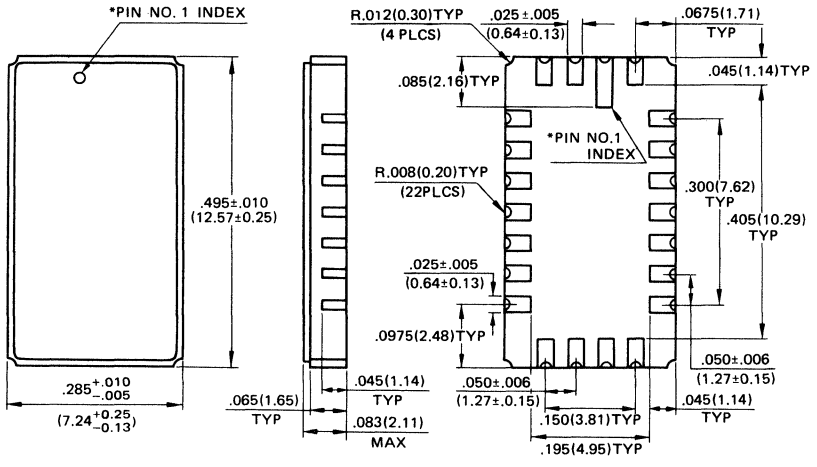
(Case No. : DIP-22P-M04)



Dimensions in
inches (millimeters)

2

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

FUJITSU

CMOS 65536-BIT BI-CMOS STATIC RANDOM ACCESS MEMORY	MB82B75-15 MB82B75-20

TS270-A893
March 1989

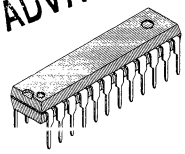
64K-BIT(16,384 x 4) Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

ADVANCE INFO.

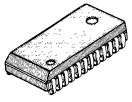
The Fujitsu MB82B75 is a 16,384-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

MB82B75 has 300mil plastic DIP and plastic small outline J-lead(SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB82B75 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.



PLASTIC PACKAGE
DIP-24P-M03

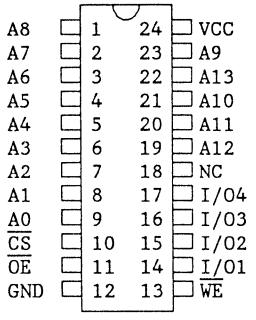


PLASTIC PACKAGE
LCC-24P-M02

- 16,384 words x 4 bits organization
- Fast access time:
  tAA=tACS=15ns max. / tOE=10ns max. (MB82B75-15)
  tAA=tACS=20ns max. / tOE=12ns max. (MB82B75-20)
- Bi-CMOS peripheral
- TTL compatible inputs/outputs
- Completely static operation: No clock required
- Three-state output
- Common data input/output
- Single=5V(±10%) power supply with low current drain
  Active operation = 120mA max.
  Standby operation = 15 mA max.(CMOS level)
  Standby operation = 25 mA max.(TTL level)
- Standard 24-pin plastic DIP package : Suffix -P-SK
- Standard 28-pad Leadless Chip Carrier:Suffix -CV
- Standard 24-pin plastic SOJ package : Suffix -PJ
- Pin compatible with MB81C75

PIN ASSIGNMENT

(TOP VIEW)



LCC: See page 9

ABSOLUTE MAXIMUM RATINGS (See Note)

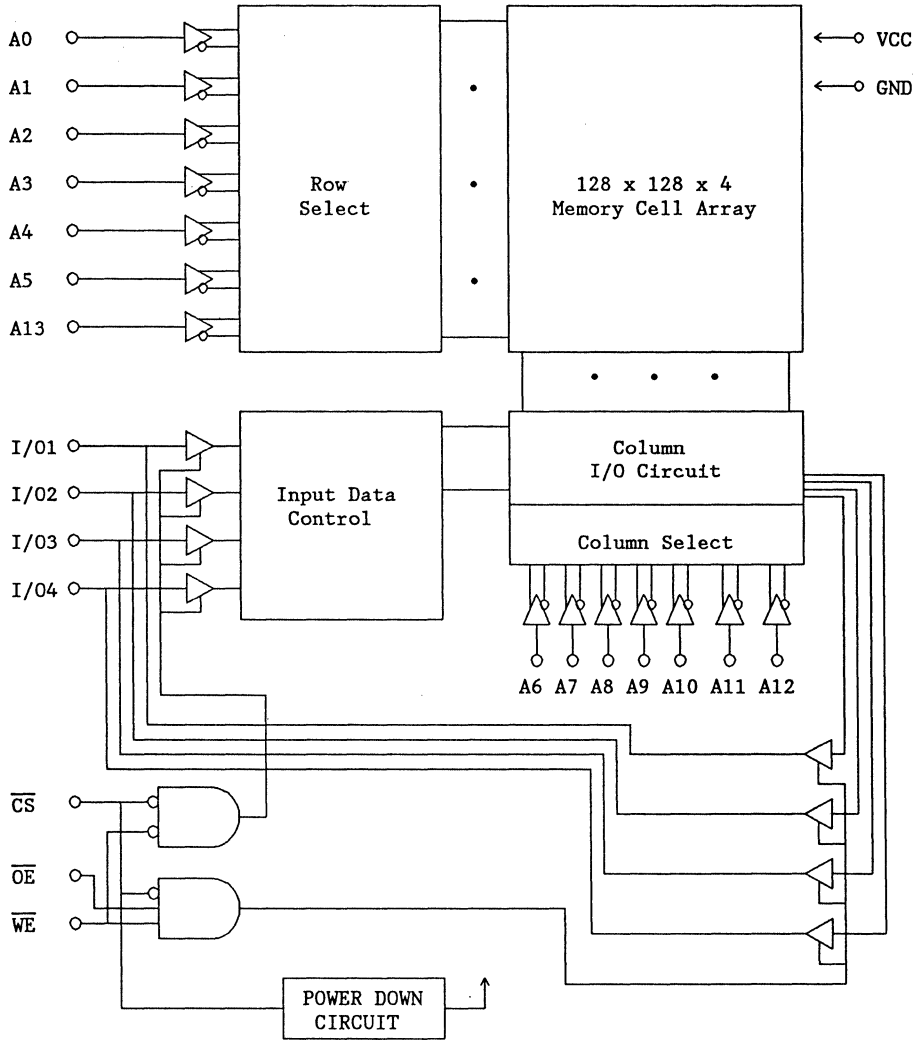
Rating		Symbol	Values	Unit
Supply Voltage		VCC	-0.5 to +7.0	V
Input Voltage		VIN	-3.5 to +7.0	V
Output Voltage		VI/O	-0.5 to +7.0	V
Output Current		IOUT	±20	mA
Power Dissipation		PD	1.0	W
Temperature Under Bias		TBIAS	-10 to +85	°C
Storage Temperature Range	Ceramic	TSTG	-65 to +150	°C
	Plastic		-45 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 - MB82B75 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance(V/CS=0V)	C/CS			6	pF
Input Capacitance(VIN=0V)	CIN			5	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A13	Address input.	$\overline{WE}$	Write Enable.
I/O1 to I/O4	Data input/output.	VCC	Power Supply(+5V±10%).
$\overline{CS}$	Chip Select 1.	GND	Ground.
NC	No Connect		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	Power Supply Current
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Disable	High-Z	Active
L	H	L	Read	DOUT	Active
L	L	X	Write	DIN	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

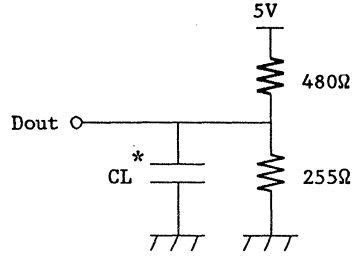
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-5	5	µA
Output Leakage Current	$\overline{VI}$/O=GND to VCC $\overline{CS}$=VIH or $\overline{WE}$=VIL	ILI/O	-5	5	µA
Operating Supply Current	$\overline{CS}$=VIL, I/O=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{CS}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS}$=VIH VCC=min. to max.	ISB2		25	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	-0.5 *1	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{CS}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ
Load II	5pF	tCLZ, tCHZ, tWLZ, tWHZ, tOLZ and tOHZ

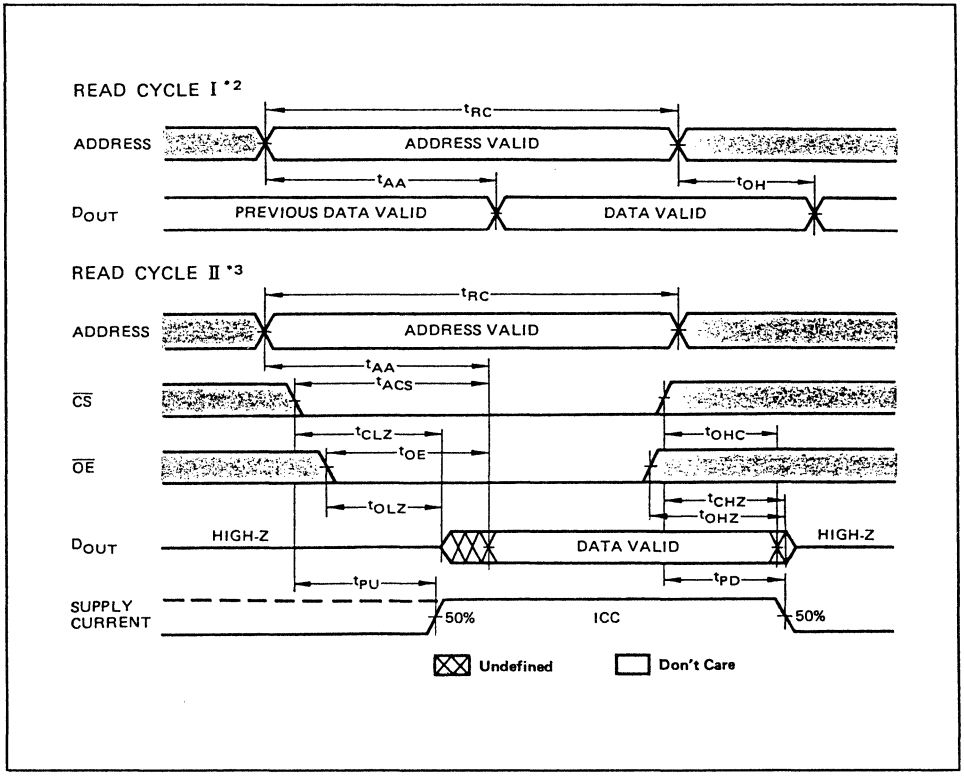
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B75-15		MB82B75-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time	tAA		15		20	ns
/CS Access Time	tACS		15		20	ns
/OE Access Time	tOE		10		12	ns
Output Hold from Address Change	tOH	3		3		ns
Output Hold from /CS	tOHC	2		2		ns
Output Low-Z from /CS	tCLZ	3		3		ns
Output Low-Z from /OE	tOLZ	2		2		ns
Output High-Z from /CS	tCHZ		8		10	ns
Output High-Z from /OE	tOHZ		8		10	ns
Power Up from /CS	tPU	0		0		ns
Power Down from /CS	tPD		15		15	ns

READ CYCLE TIMING DIAGRAM *1



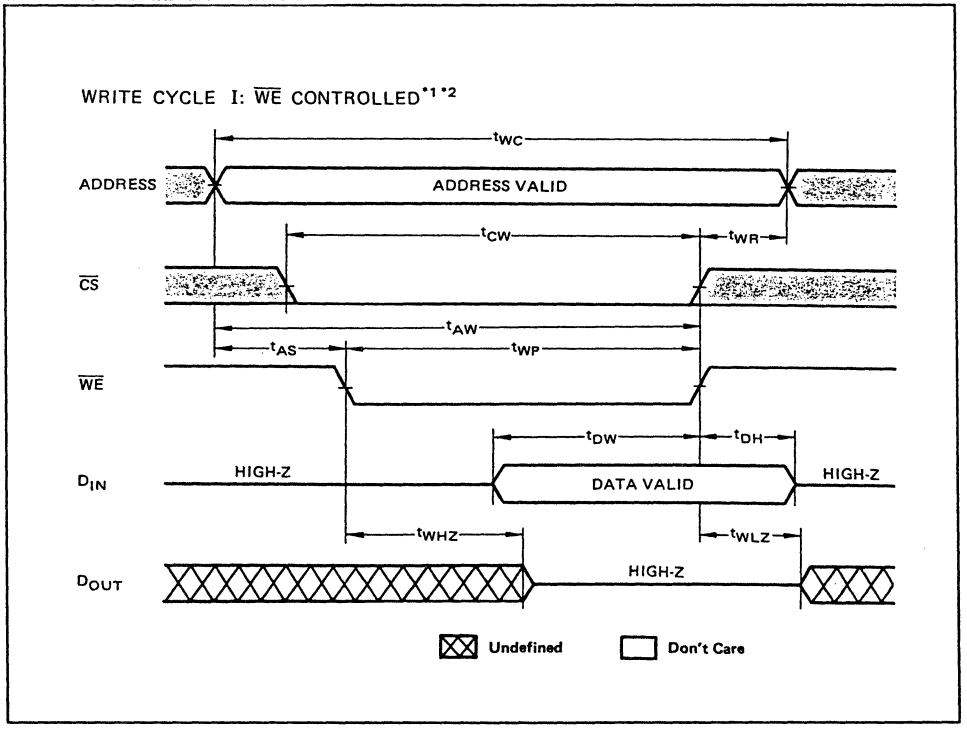
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continously selected, $\overline{CS}$=VIL, $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE

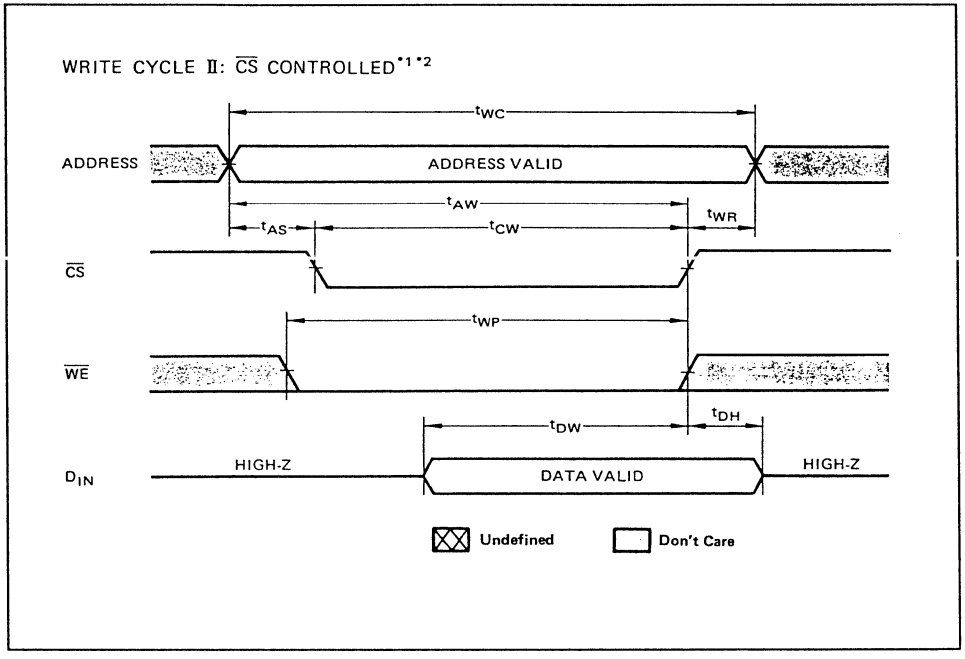
Parameter	Symbol	MB82B75-15		MB82B75-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15		20		ns
Address Valid to End of Write	tAW	10		15		ns
/CS to End of Write	tCW	10		15		ns
Data Setup Time	tDW	7		10		ns
Data Hold Time	tDH	3		3		ns
Write Pulse Width	tWP	8		10		ns
Write Recovery Time	tWR	2		2		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from /WE	tWLZ	0		0		ns
Output High-Z from /WE	tWHZ		8		10	ns

2

WRITE CYCLE TIMING DIAGRAM



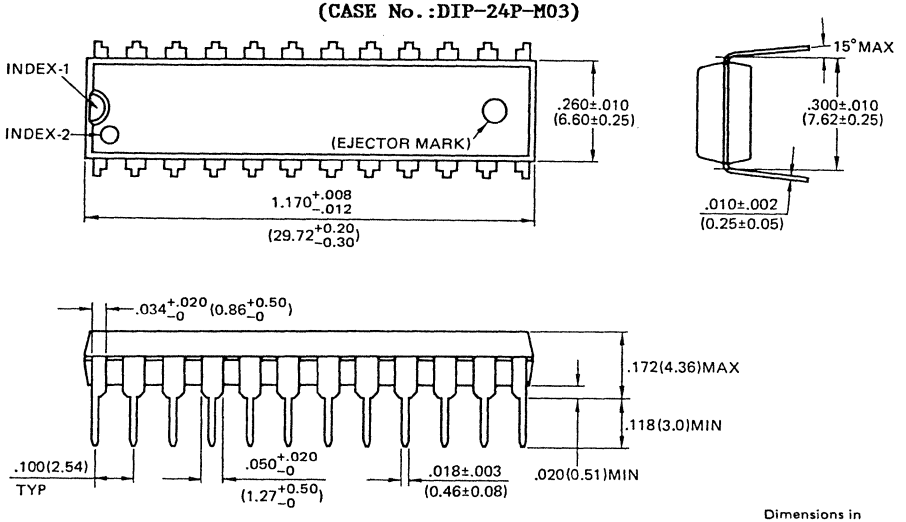
Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write cycle are determined from last address transition to the first address transition of the next address.

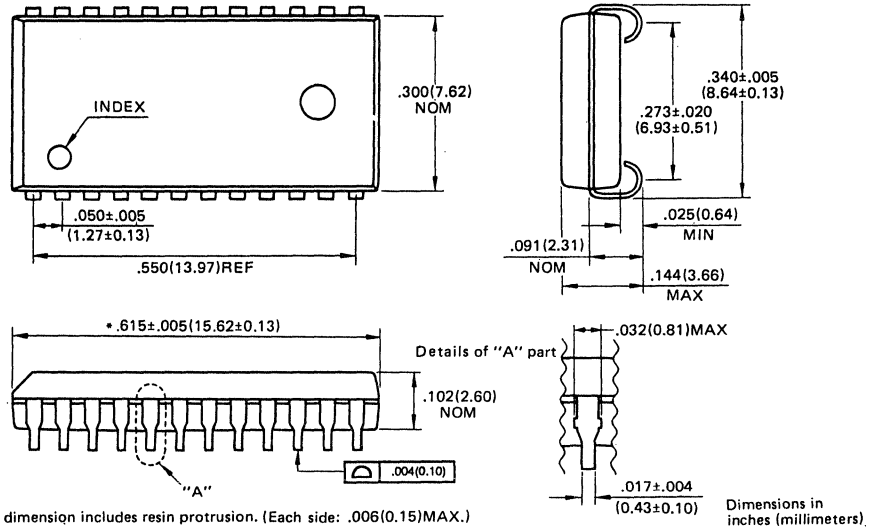
PACKAGE DIMENSIONS

24-LEADS PLASTIC DUAL-IN LINE PACKAGE
(CASE No.:DIP-24P-M03)



Dimensions in inches (millimeters)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

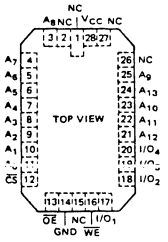


Dimensions in inches (millimeters).

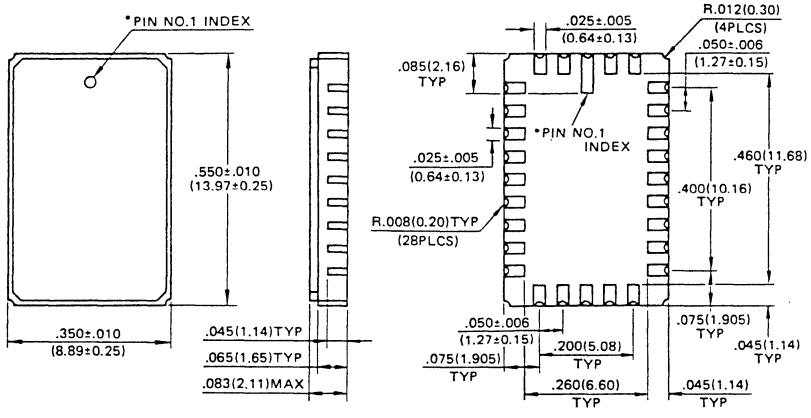
* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

PACKAGE DIMENSIONS

CERAMIC PACKAGE
LCC-28C-A03



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches
and (millimeters)

2

TS248–E89Y
Nov. 1989

FUJITSU

DATA SHEET

MB82B79-15-20
72K BIT HIGH SPEED BI-CMOS SRAM

8,192–WORD x 9–BIT Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY

PRELIMINARY

2

The Fujitsu MB82B79 is a 8,192 words by 8 bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi–CMOS technology, and to obtain amaller chip size, cells consist of NMOS transistors and resistors.

MB82B79 has 300mil plastic DIP and plastic flat (SOIC) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB82B79 is ideally suited for use in large computer and other applications where fast access time, large–capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.

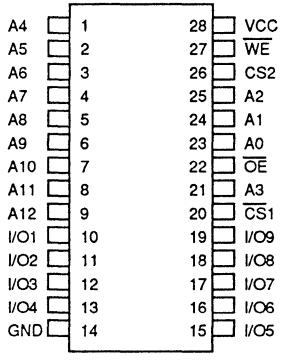
- Organization: 8,192 words x 9 bits
- Static operation: No clocks or refresh required
- Fast access time:
  tAA=tACS1=15ns max. / tACS2=tOE=8ns max. (MB82B79–15)
  tAA=tACS1=20ns max. / tACS2=tOE=10ns max.(MB82B79–20)
- Single=5V(+10%) power supply with low current drain:
  Active operation=120mA max.
  Standby operation=15mA max.(CMOS level)
  Standby operation=25mA max.(TTL level)
- Bi–CMOS peripheral
- TTL compatible inputs/outputs
- Three–state output
- 300 mil width 28–pin plastic Skinny DIP package (Suffix: –P–SK)
- 450 mil width 28–pin plastic SOP package (Suffix: –PF)

PLASTIC PACKAGE
FPT–28P–M02

PLASTIC PACKAGE
DIP–28P–M04

PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

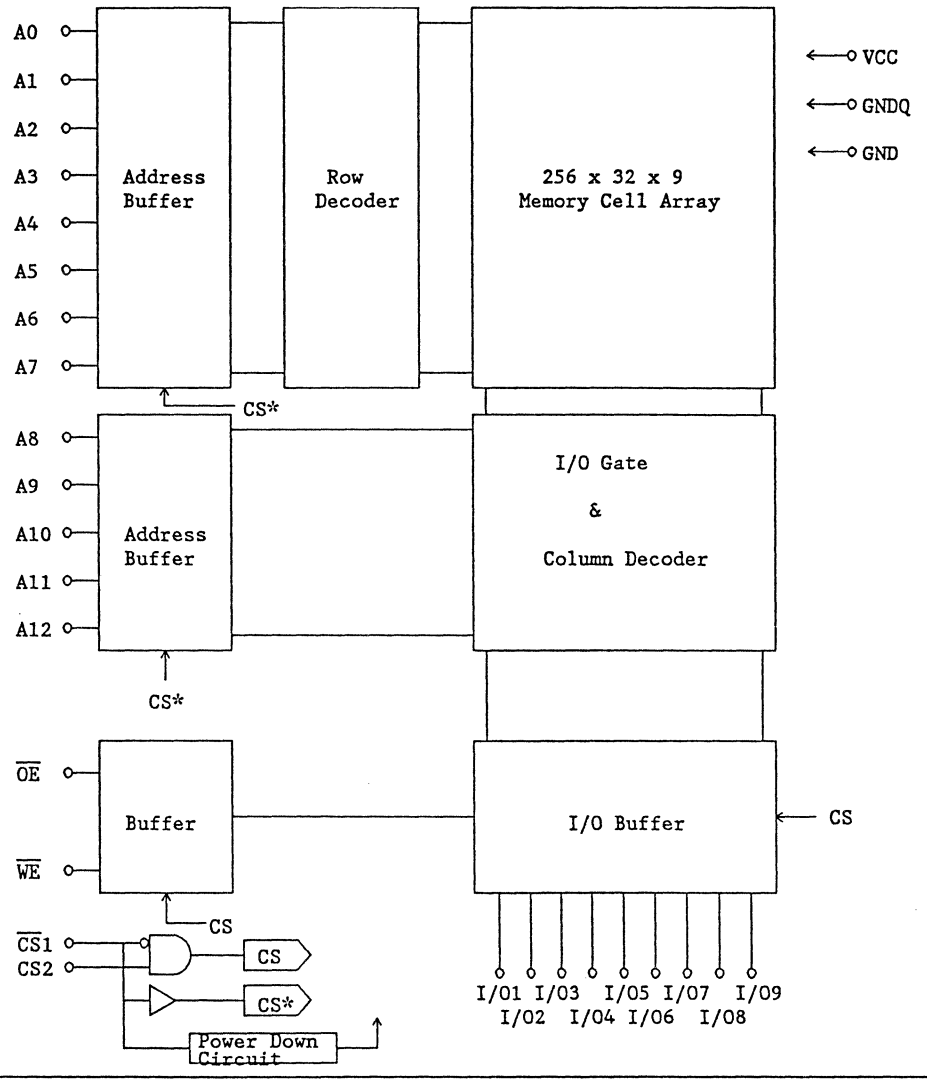
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	–0.5 to +7.0	V
Output Voltage on any pin with to GND	$V_{I/O}$	–0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 - MB82B79 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance(VIN=0V) (/CS1, CS2, /WE, /OE)	CI1			7	pF
Input Capacitance(VIN=0V) (Other inputs)	CI2			6	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A12	Address input.	$\overline{WE}$	Write Enable.
I/01 to I/09	Data input/output.	VCC	Power Supply(+5V±10%)
$\overline{CS1}$	Chip Select 1.	GND	Ground.
CS2	Chip Select 2.	GNDQ	Ground for output.
$\overline{OE}$	Output Enable.	NC	No Connection.

TRUTH TABLE

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O pin	Power Supply Current
X	H	X	X	Standby	High-Z	Standby
X	L	L	X	Not selected	High-Z	Active
H	L	H	H	Dout disable	High-Z	Active
H	L	H	L	Read	Data out	Active
L	L	H	X	Write	Data in	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

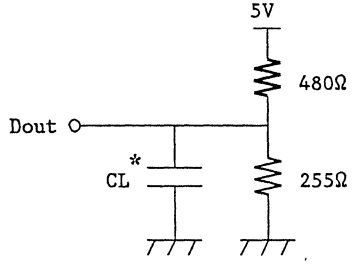
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-10	10	µA
Output Leakage Current	$\overline{VI}$/O=GND to VCC $\overline{CS1}$=VIH or CS2=VIL or $\overline{WE}$=VIL or $\overline{OE}$=VIH	ILI/O	-10	10	µA
Operating Supply Current	$\overline{CS1}$=VIL, I/O=Open Cycle=min.	ICC		120	mA
Standby Supply Current	$\overline{VCC}$=min. to max. $\overline{CS1}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS1}$=VIH	ISB2		25	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	-0.5 *1	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	$\overline{VCC}$=GND to 4.5V $\overline{CS1}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS1}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tLZ, tHZ, tOW, tOLZ and tOHZ
Load II	5pF	tLZ, tHZ, tOW, tOLZ and tOHZ

AC CHARACTERISTICS

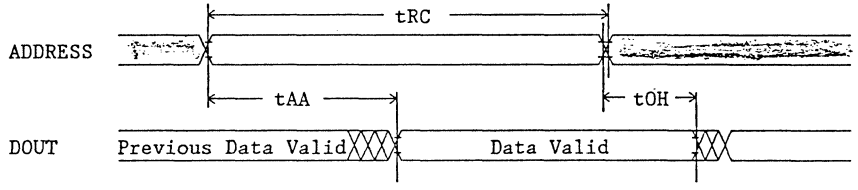
(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

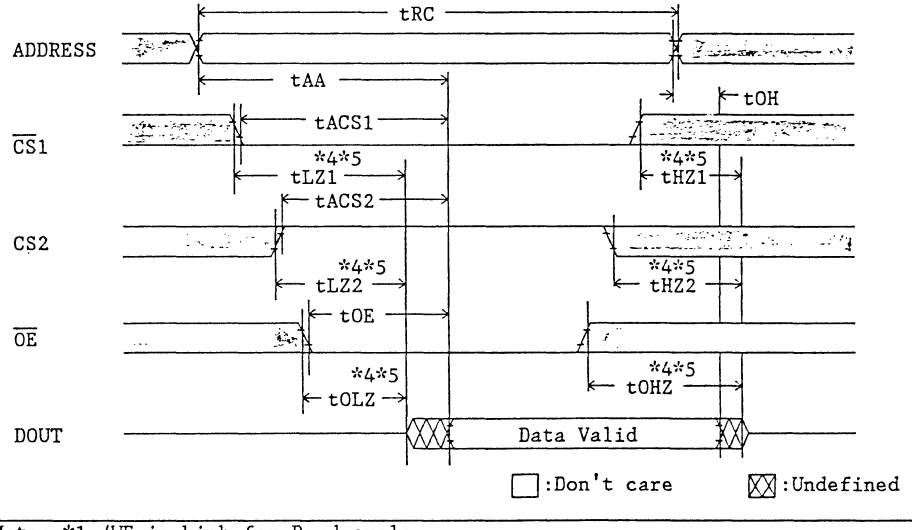
Parameter	Symbol	MB82B79-15		MB82B79-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time *2	tAA		15		20	ns
/CS1 Access Time *3	tACS1		15		20	ns
CS2 Access Time	tACS2		8		10	ns
/OE Access Time	tOE		8		10	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from /CS1 *4*5	tLZ1	3		3		ns
Output Low-Z from CS2 *4*5	tLZ2	2		2		ns
Output Low-Z from /OE *4*5	tOLZ	2		2		ns
Output High-Z from /CS1 *4*5	tHZ1		8		10	ns
Output High-Z from CS2 *4*5	tHZ2		8		10	ns
Output High-Z from /OE *4*5	tOHZ		8		10	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE I: ADDRESS CONTROLLED *3 ($\overline{CS1}$=$\overline{OE}$="L")



READ CYCLE II: $\overline{CS1}$, CS2 CONTROLLED *4

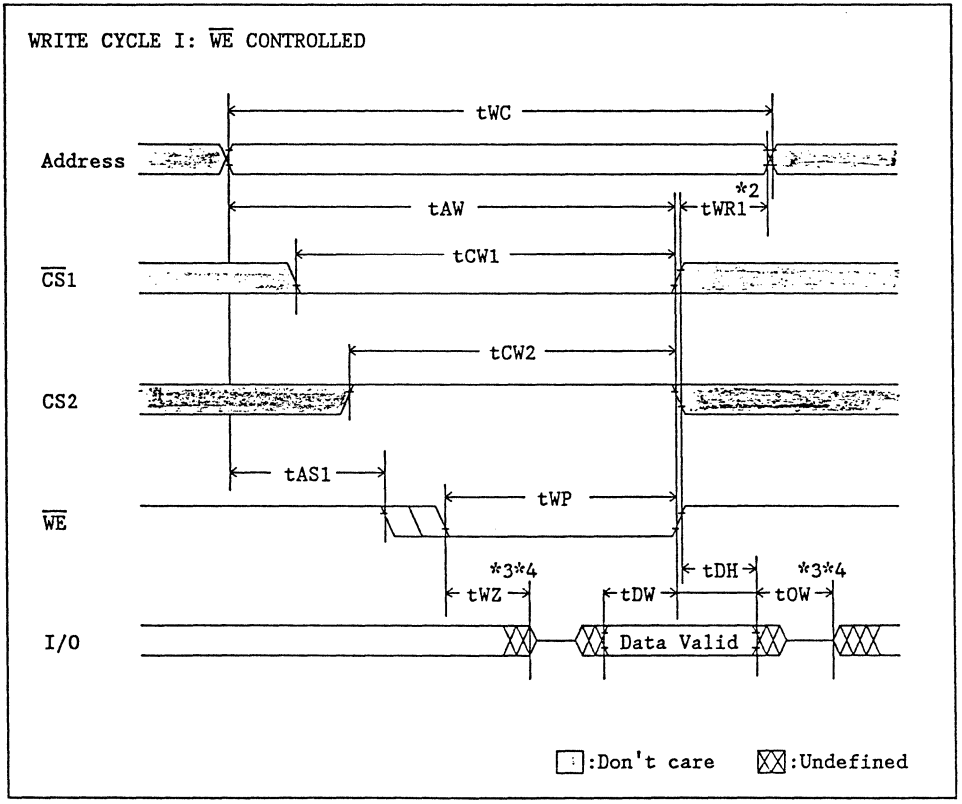


Note: *1 /WE is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE *1

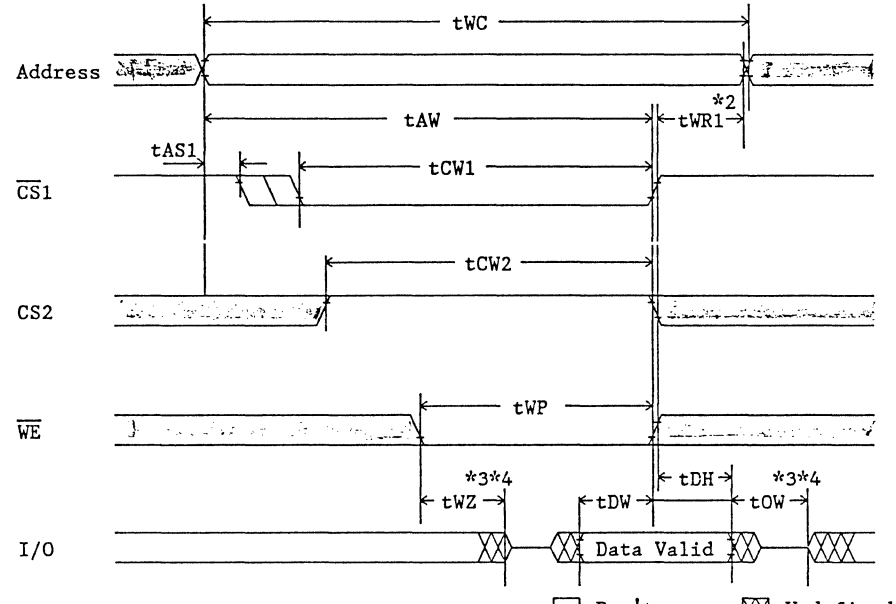
Parameter		Symbol	MB82B79-15		MB82B79-20		Unit
			Min	Max	Min	Max	
Write Cycle Time		tWC	15		20		ns
Address Valid to End of Write		tAW	10		15		ns
/CS1 to End of Write		tCW1	10		15		ns
CS2 to End of Write		tCW2	6		8		ns
Data Setup Time		tDW	7		10		ns
Data Hold Time		tDH	3		3		ns
Write Pulse Width		tWP	8		10		ns
Write Recovery Time*2	/CS1,/WE	tWR1	3		3		ns
	CS2	tWR2	5		5		ns
Address Setup Time	/CS1,/WE	tAS1	0		0		ns
	CS2	tAS2	2		2		ns
Output Low-Z from /WE *3*4		tOW	0		0		ns
Output High-Z from /WE *3*4		tWZ		8		10	ns

WRITE CYCLE TIMING DIAGRAM *1

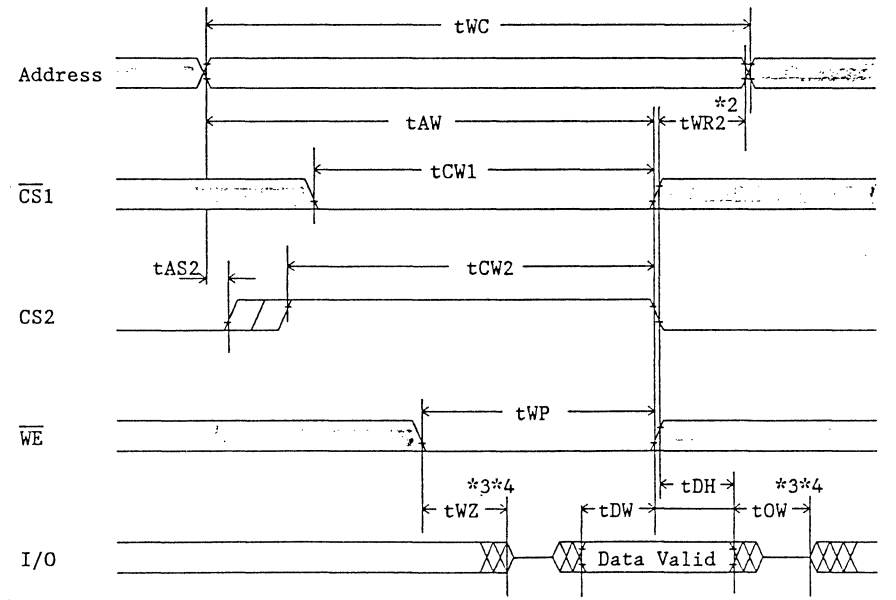


Note: *1 If $\overline{CS1}$, $\overline{OE}$ and CS2 are in the READ Mode during this period, I/O pins are in the out put state so that the input signals of opposite phase to the outputs must not be applied.
*2 tWR is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS1}$ CONTROLLED



WRITE CYCLE III: $\overline{WE}$ CONTROLLED



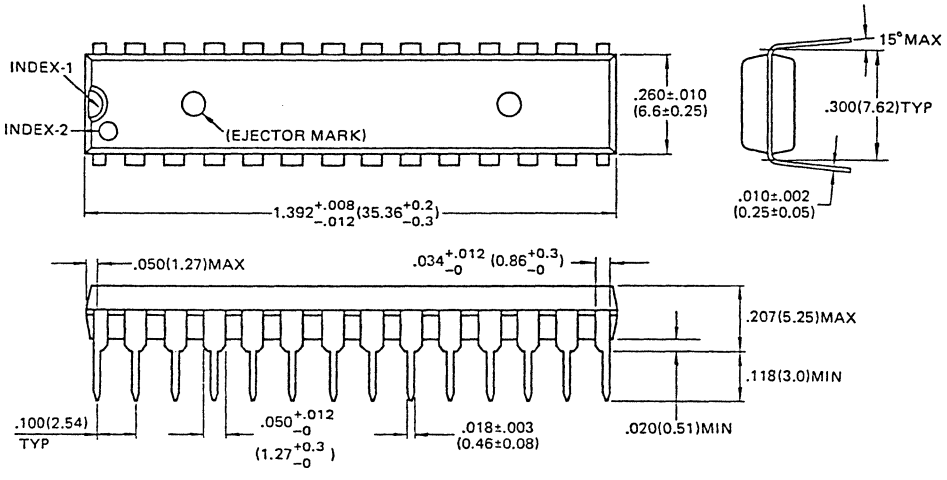
*Notes: See Write Cycle I

2

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

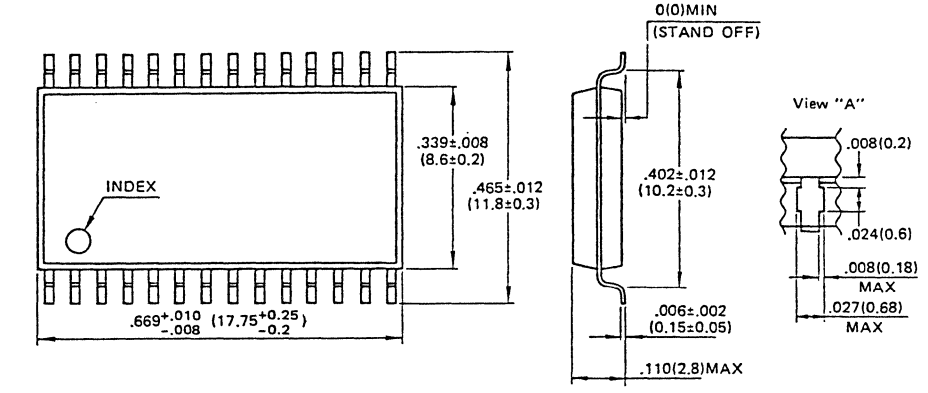


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in
inches (millimeters)

TS281–A89Z
December 1989

FUJITSU

DATA SHEET

MB82B81-15/-20
256K BIT HIGH SPEED BI-CMOS SRAM

262,144-WORD x 1-BIT Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY

ADVANCE INFO.

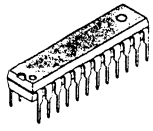
2

The Fujitsu MB82B81 is a 65,536 words by 1 bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi–CMOS technology, and to obtain amaller chip size, cells consist of NMOS transistors and resistors.

MB82B81 has 300mil plastic DIP and 300mil plastic small out–line J–lead (SOJ) package as package option. The memory utilizes asynchronous circuitry and requires +5V power supply. All pins are TTL compatible.

The MB82B81 is ideally suited for use in large computer and other applications where fast access time, large–capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.

- Organization: 262,144 words x 1 bit
- Static operation: No clocks or refresh required
- Fast access time:
  tAA=tACS=15ns max.(MB82B81–15)
  tAA=tACS=20ns max.(MB82B81–20)
- Single=5V(+10%) power supply with low current drain:
  Active operation=120mA max.
  Standby operation=15mA max.(CMOS level)
  Standby operation=30mA max.(TTL level)
- Bi–CMOS peripheral
- TTL compatible inputs/outputs
- Three–state output
- 300 mil width 24–pin plastic Skinny DIP package (Suffix: –P–SK)
- 300 mil width 24–pin plastic SOJ package (Suffix: –PJ)
- Pin compatible with MB81C81A

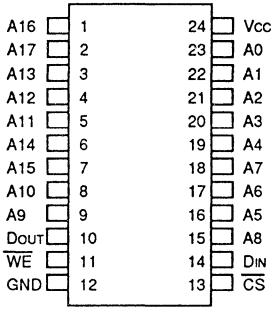


PLASTIC PACKAGE
DIP–24P–M03

PLASTIC PACKAGE
LCC–24P–M02

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE)

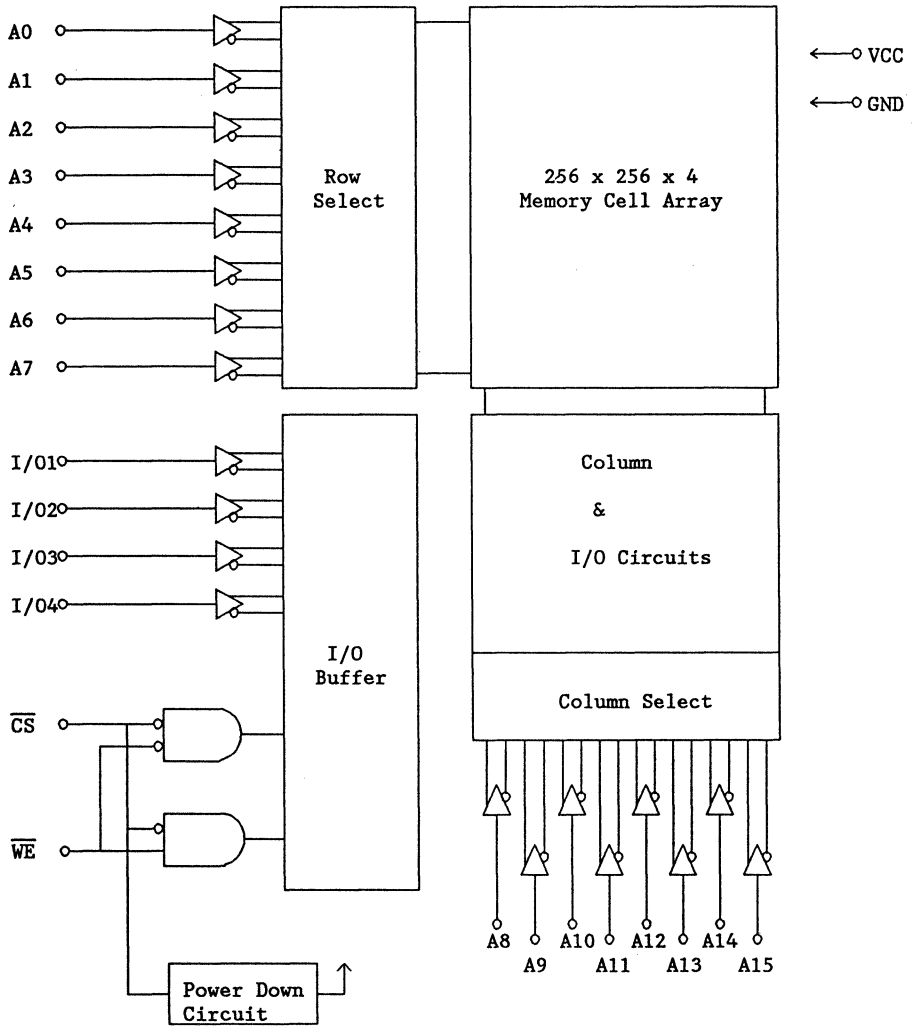
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	–0.5 to +7.0	V
Output Voltage on any pin with to GND	$V_{I/O}$	–0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 - MB82B81 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			7	pF
Input Capacitance(VIN=0V)	CIN			7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address input.	$\overline{WE}$	Write Enable.
DIN	Data input.	VCC	Power Supply(+5V±10%).
DOUT	Data output.	GND	Ground.
$\overline{CS}$			

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power Supply Current
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

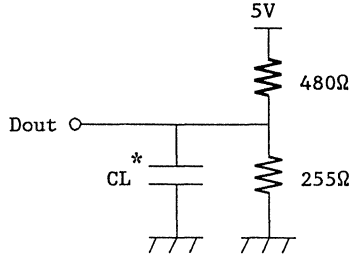
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-5	5	µA
Output Leakage Current	VOUT=GND to VCC $\overline{CS}$=VIH or $\overline{WE}$=VIL	ILI/O	-5	5	µA
Operating Supply Current	$\overline{CS}$=VIL, DOUT=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{CS}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS}$=VIH VCC=min. to max.	ISB2		30	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	*1 -0.5	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{CS}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tLZ, tHZ, tOW and tWZ
Load II	5pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

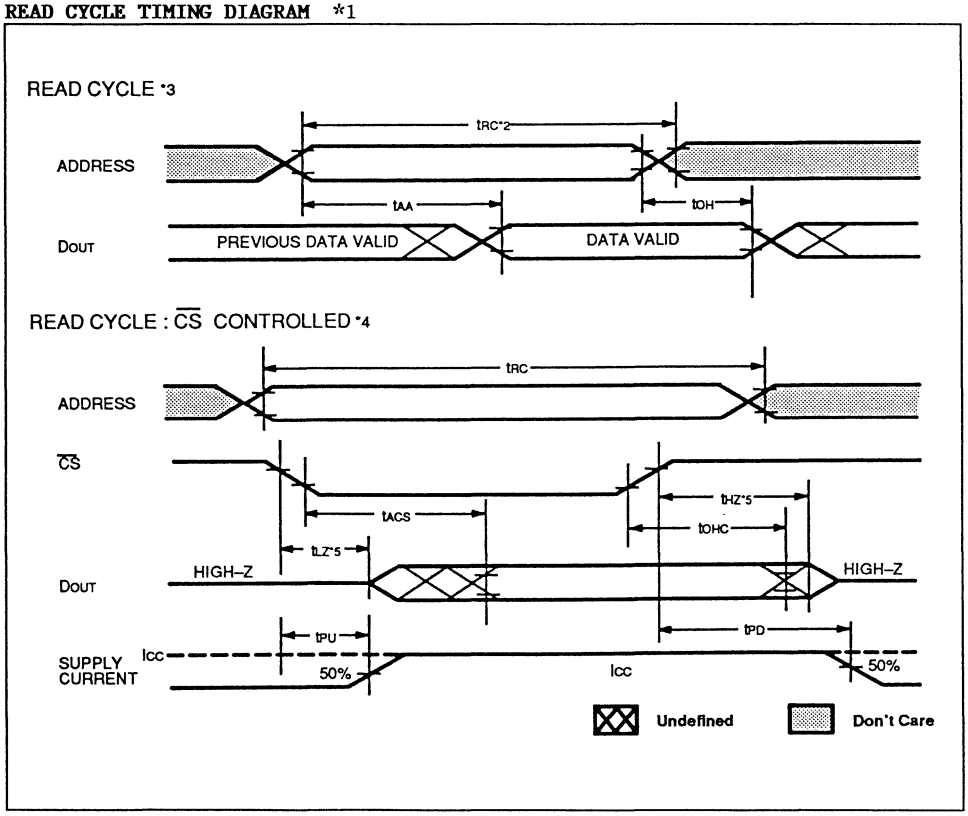
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B81-15		MB82B81-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time	tAA		15		20	ns
/CS Access Time	tACS		15		20	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from /CS	tLZ	3		3		ns
Output High-Z from /CS	tHZ		8		10	ns
Power Up from /CS	tPU	0		0		ns
Power Down from /CS	tPD		15		15	ns

2

READ CYCLE TIMING DIAGRAM *1



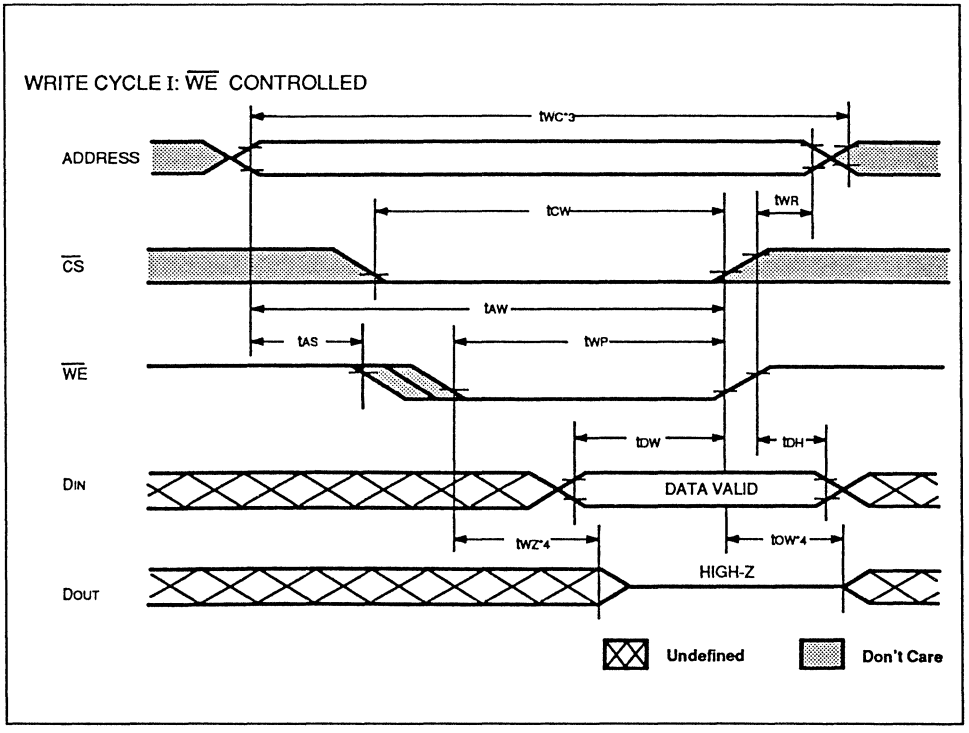
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

WRITE CYCLE

Parameter	Symbol	MB82B81-15		MB82B81-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15		20		ns
Address Valid to End of Write	tAW	12		17		ns
/CS to End of Write	tCW	12		17		ns
Data Setup Time	tDW	4		9		ns
Data Hold Time	tDH	0		2		ns
Write Pulse Width	tWP	11		16		ns
Write Recovery Time	tWR	1		3		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from /WE	tOW	0		0		ns
Output High-Z from /WE	tWZ		6		8	ns

2

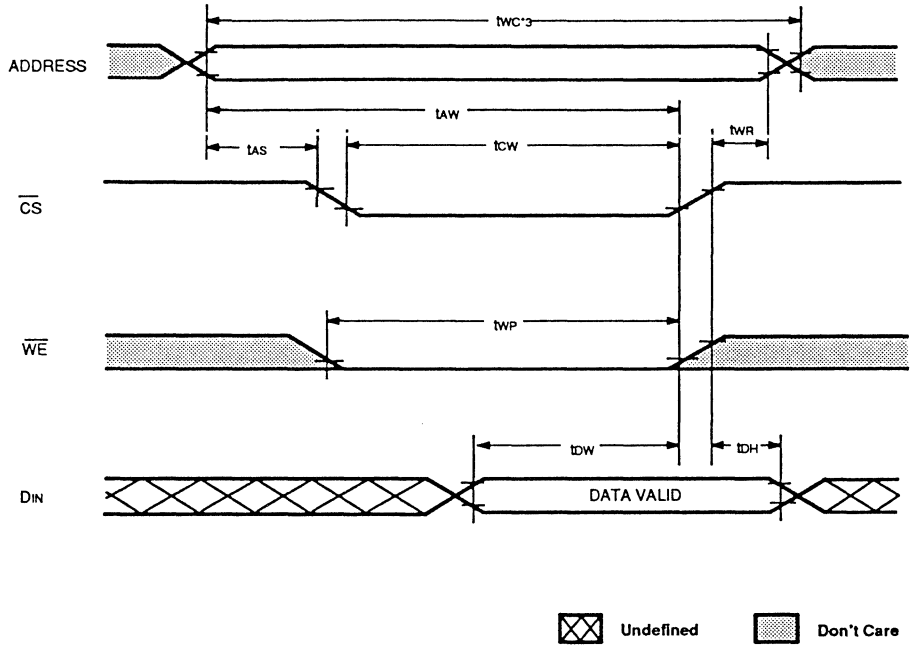
WRITE CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.

WRITE CYCLE TIMING DIAGRAM (Continued) *1*2*4

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2

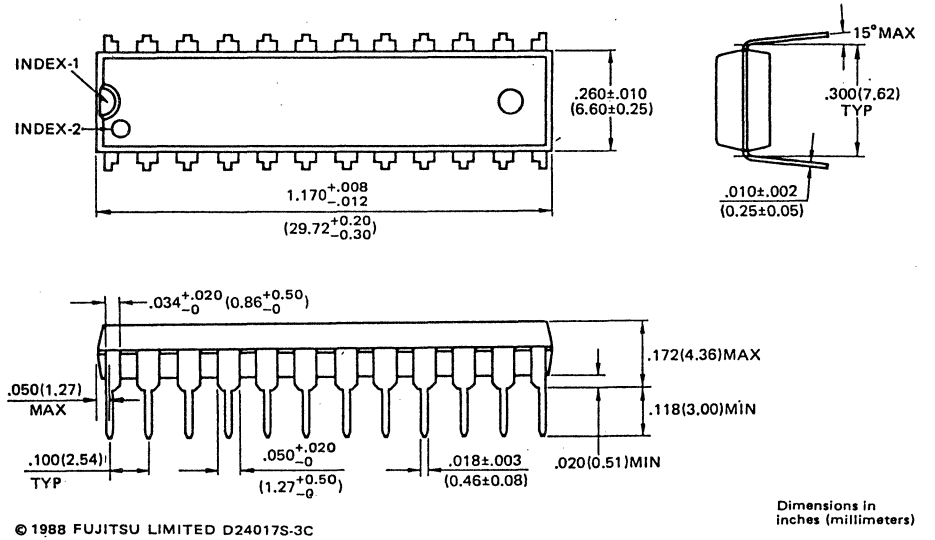


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.

PACKAGE DIMENSIONS

(Suffix:-P-SK)

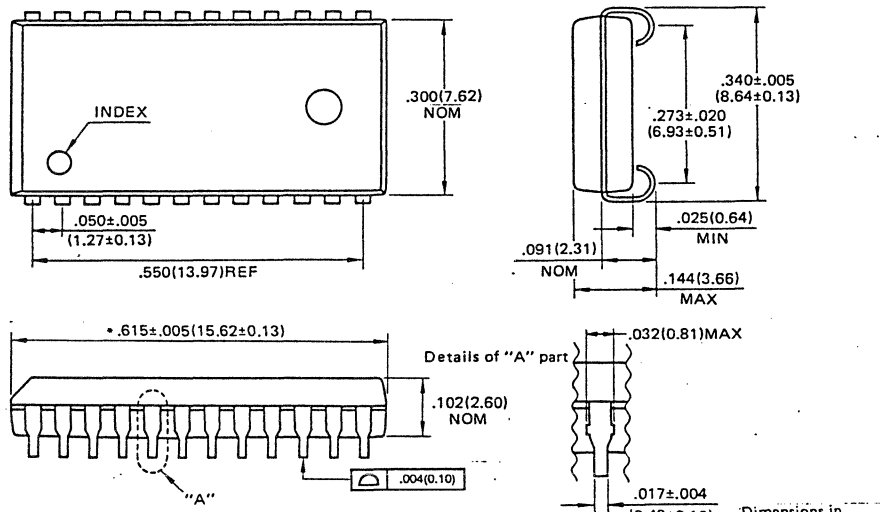
24-LEADS PLASTIC DUAL-IN LINE PACKAGE
(CASE No.:DIP-24P-M03)



Dimensions in inches (millimeters)

(Suffix:-PJ)

24-LEADS PLASTIC SOJ PACKAGE
CASE No.: LCC-24P-M02)



Dimensions in inches (millimeters)

* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

FUJITSU

CMOS 262144-BIT BI-CMOS STATIC RANDOM ACCESS MEMORY	MB82B84-15 MB82B84-20

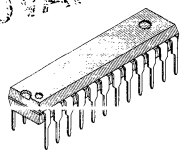
TS268-B893
March 1989

256K-BIT(65,536 x 4) Bi-CMOS HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

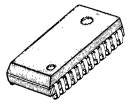
The Fujitsu MB82B84 is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower and high speed, peripheral circuits consist of Bi-CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors.

MB82B84 has 300mil plastic DIP and plastic small outline J-lead(SOJ) as package option. The memory utilizes asynchronous circuitly and requires +5V power supply. All pins are TTL compatible.

The MB82B84 is ideally suited for use in large computer and other applications where fast access time, large capacity and ease of use are required.
All devices offer the advantages of low power dissipation, low cost high performance.



PLASTIC PACKAGE
DIP-24P-M03

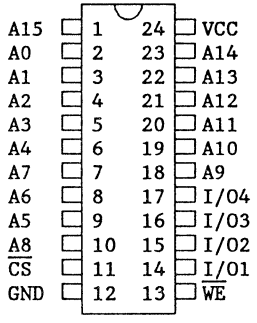


PLASTIC PACKAGE
LCC-24P-M02

- 65,536 words x 4 bits organization
- Fast access time:
  tAA=tACS=15ns max.(MB82B84-15)
  tAA=tACS=20ns max.(MB82B84-20)
- Bi-CMOS peripheral
- TTL compatible inputs/outputs
- Completely static operation: No clock required
- Three-state output
- Common data input/output
- Single=5V(±10%) power supply with low current drain
  - Active operation = 120mA max.
  - Standby operation = 15 mA max.(CMOS level)
  - Standby operation = 25 mA max.(TTL level)
- Standard 24-pin plastic DIP package : Suffix -P-SK
- Standard 24-pin plastic SOJ package : Suffix -PJ
- Pin compatible with MB81C84A

PIN ASSIGNMENT

(TOP VIEW)



(DIP & SOJ Package)

ABSOLUTE MAXIMUM RATINGS (See Note)

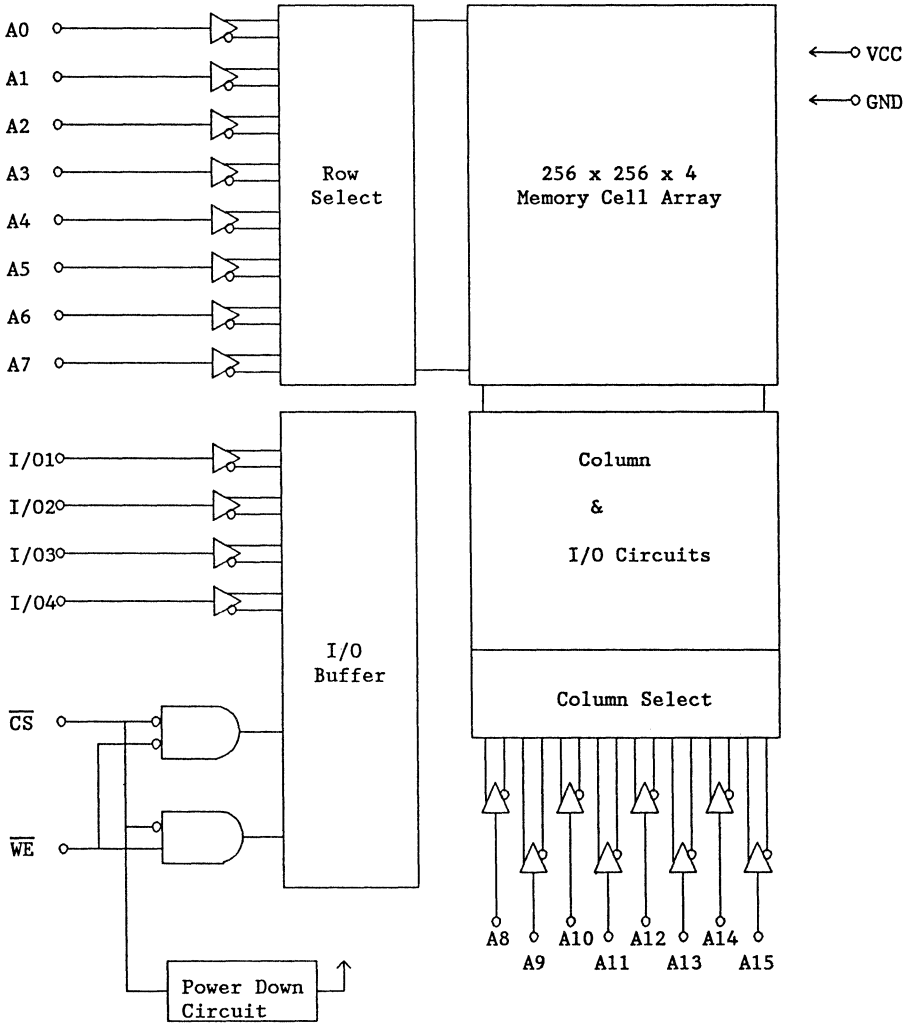
Rating	Symbol	Values	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-3.5 to +7.0	V
Output Voltage	VI/O	-0.5 to +7.0	V
Output Current	IOUT	±20	mA
Power Dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature Range	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 - MB82B84 BLOCK DIAGRAM



CAPACITANCE(Ta=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance(V/CS=0V)	C/CS			6	pF
Input Capacitance(VIN=0V)	CIN			5	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A15	Address input.	$\overline{WE}$	Write Enable.
I/O1 to I/O4	Data input/output.	VCC	Power Supply(+5V±10%).
$\overline{CS}$	Chip Select 1.	GND	Ground.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O pin	Power Supply Current
H	X	Standby	High-Z	Standby
L	L	Write	DIN	Active
L	H	Read	DOUT	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

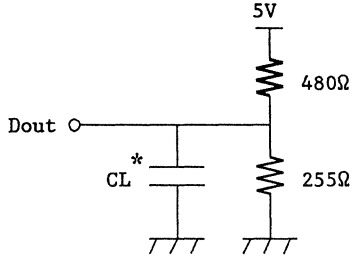
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	VIN=GND to VCC VCC=max.	ILI	-5	5	μA
Output Leakage Current	VI/O=GND to VCC $\overline{CS}$=VIH or $\overline{WE}$=VIL	ILI/O	-5	5	μA
Operating Supply Current	$\overline{CS}$=VIL, I/O=Open Cycle=min.	ICC		120	mA
Standby Supply Current	VCC=min. to max. $\overline{CS}$=VCC-0.2V, VIN≤0.2V or VIN≥VCC-0.2V	ISB1		15	mA
Standby Supply Current	$\overline{CS}$=VIH VCC=min. to max.	ISB2		25	mA
Input High Voltage		VIH	2.2	6.0	V
Input Low Voltage		VIL	-0.5 *1	0.8	V
Output High Voltage	IOH=-4mA	VOH	2.4		V
Output Low Voltage	IOL=8mA	VOL		0.4	V
Peak Power-on Current *2	VCC=GND to 4.5V $\overline{CS}$=Lower of VCC or VIH min.	IPO		50	mA

Note: *1 -2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS}$ input should be connected to VCC to keep the device deselected.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: VIL=0.8V, VIH=2.2V
- Output: VOL=0.8V, VOH=2.2V
- Output Load



* Including Scope and jig capacitance

	CL	Parameters measured
Load I	30pF	except tLZ, tHZ, tOW and tWZ
Load II	5pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

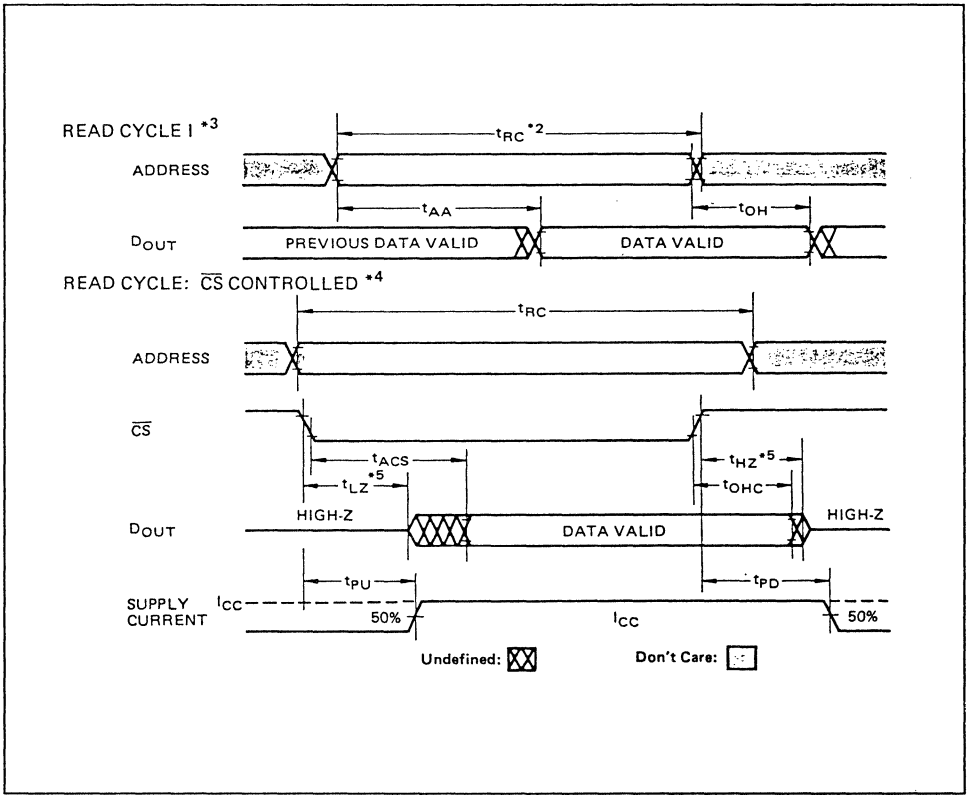
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B84-15		MB82B84-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15		20		ns
Address Access Time	tAA		15		20	ns
/CS Access Time	tACS		15		20	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from /CS	tLZ	3		3		ns
Output High-Z from /CS	tHZ		8		10	ns
Power Up from /CS	tPU	0		0		ns
Power Down from /CS	tPD		15		15	ns

2

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

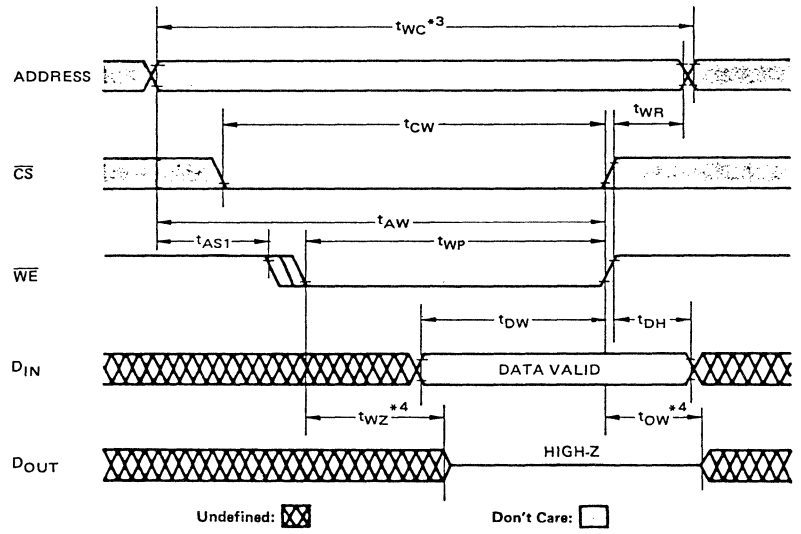
WRITE CYCLE

Parameter	Symbol	MB82B84-15		MB82B84-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15		20		ns
Address Valid to End of Write	tAW	10		15		ns
/CS to End of Write	tCW	10		15		ns
Data Setup Time	tDW	7		10		ns
Data Hold Time	tDH	3		3		ns
Write Pulse Width	tWP	8		10		ns
Write Recovery Time	tWR	2		2		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from /WE	tOW	0		0		ns
Output High-Z from /WE	tWZ		8		10	ns

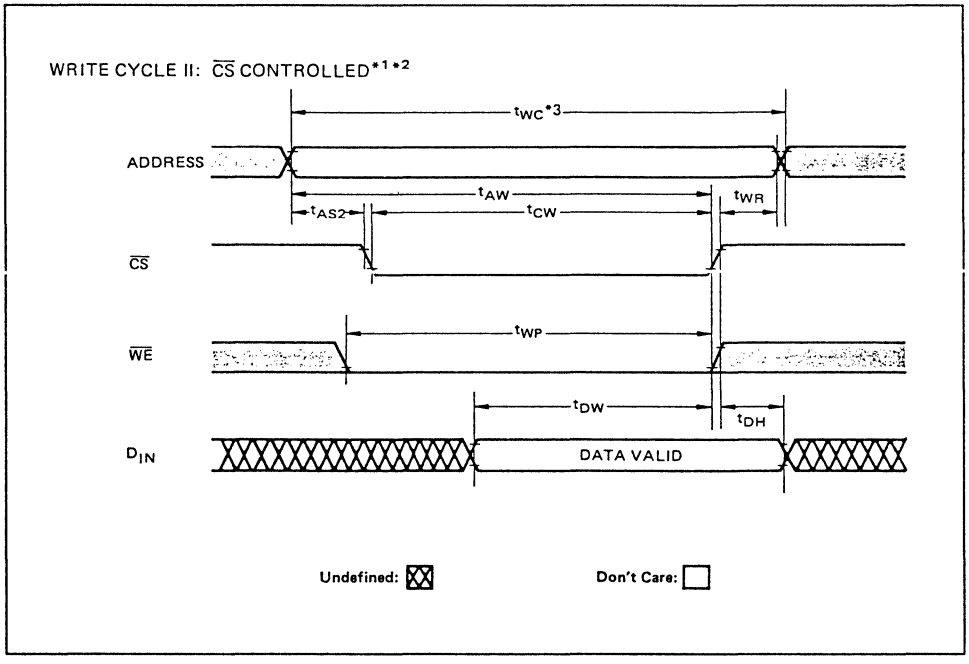
2

WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE I: $\overline{WE}$ CONTROLLED



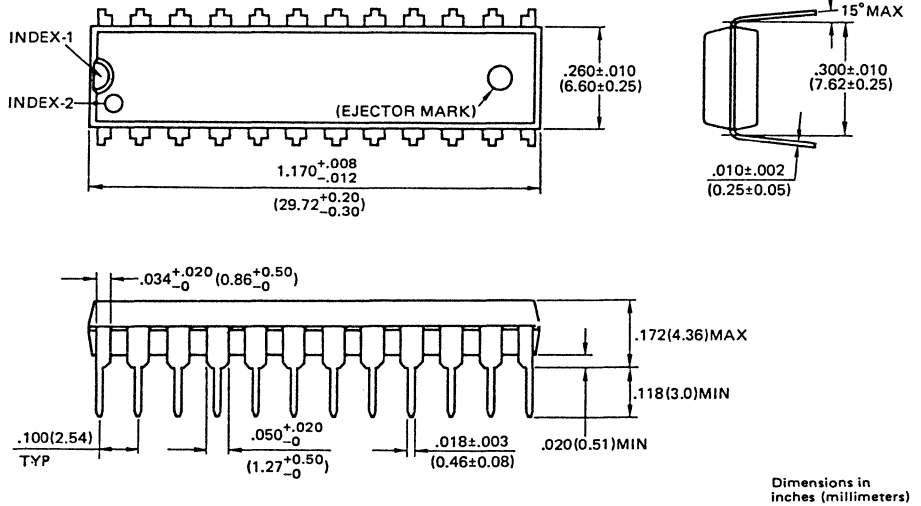
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.



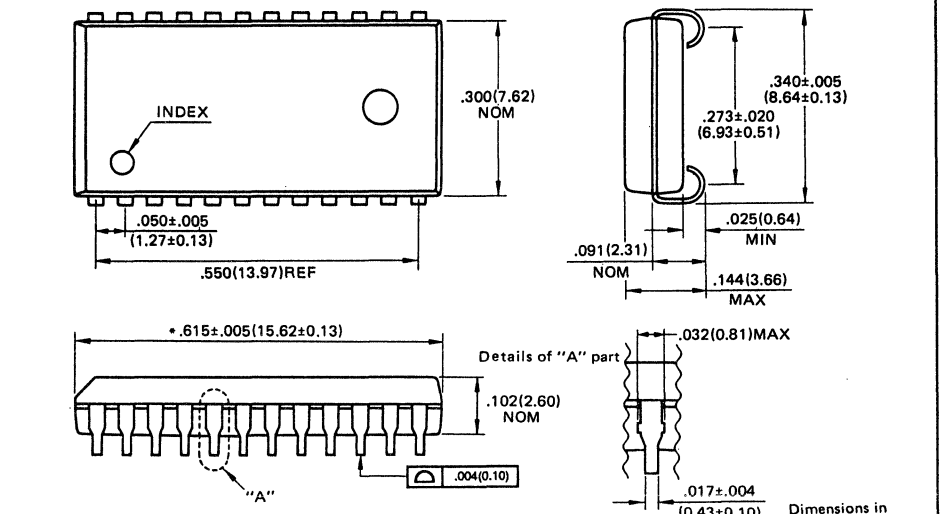
Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

PACKAGE DIMENSIONS

24-LEADS PLASTIC DUAL-IN LINE PACKAGE
(CASE No.:DIP-24P-M03)



24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Section 3

Low Power CMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
3–3	MB8464A–80/L/LL	80	65536 bits	28-pin	Plastic	DIP, FPT
	–10/L/LL	100	(8192w x 8b)	32-pad	Ceramic	LCC
	–15/L/LL	150				
3–15	MB84256–10/L/LL	100	262144 bits	28-pin	Plastic	DIP, FPT
	–12/L/LL	120	(32768w x 8b)	32-pad	Ceramic	LCC
	–15/L/LL	150				
3–25	MB84256A–70/L/LL	70	262144 bits	28-pin	Plastic	DIP, FPT
	–10/L/LL	100	(32768w x 8b)			
	–12/L/LL	120				
	–15/L/LL	150				
3–35	MB84F256–25	250	262144 bits (32768w x 8b)	28-pin	Plastic	DIP, FPT
3–47	MB841000–80/L	80	1048576 bits	32-pin	Plastic	DIP, FPT
	–10/L	100	(131072w x 8b)			
	–12/L	120				

3

FUJITSU

CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB 8464A-80/80L/80LL
MB 8464A-10/10L/10LL
MB 8464A-15/15L/15LL

March 1987
Edition 2.0

8,192 WORDS x 8 BIT CMOS STATIC RAM WITH LOW POWER AND DATA RETENTION

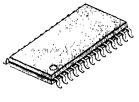
The Fujitsu MB 8464A is a 8192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volts power supply is required.

The MB 8464A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

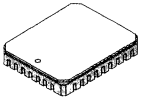
- Organization: 8192 words x 8 bits
- Fast access time: 80 ns max. (MB 8464A-80/80L/80LL)
  100 ns max. (MB 8464A-10/10L/10LL)
  150 ns max. (MB 8464A-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 11mW max. (MB 8464A-80/10/15)
  0.55mW max. (MB 8464A-80L/10L/15L)
  0.55mW max. (MB 8464A-80LL/10LL/15LL)
- Data retention current: 1mA max. (MB 8464A-80/10/15)
  25μA max. (MB 8464A-80L/10L/15L)
  2μA max. at 0°C to 40°C
  (MB 8464A-80LL/10LL/15LL)
- Data retention: 2.0V min.
- Standard 28-pin DIP (300mil width) (Suffix: P-SK)
  (600mil width) (Suffix: P)
- Standard 28-pin bend-type Flat package (450mil width) (Suffix: PF)
- Standard 32-pad LCC (Suffix: CV)

PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04

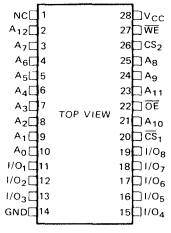


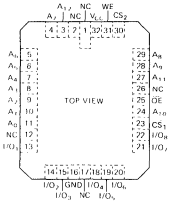
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5* to V_{CC}+0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC}+0.5	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	CERAMIC	T_{STG}	−65 to +150	°C
	PLASTIC		−45 to +125	

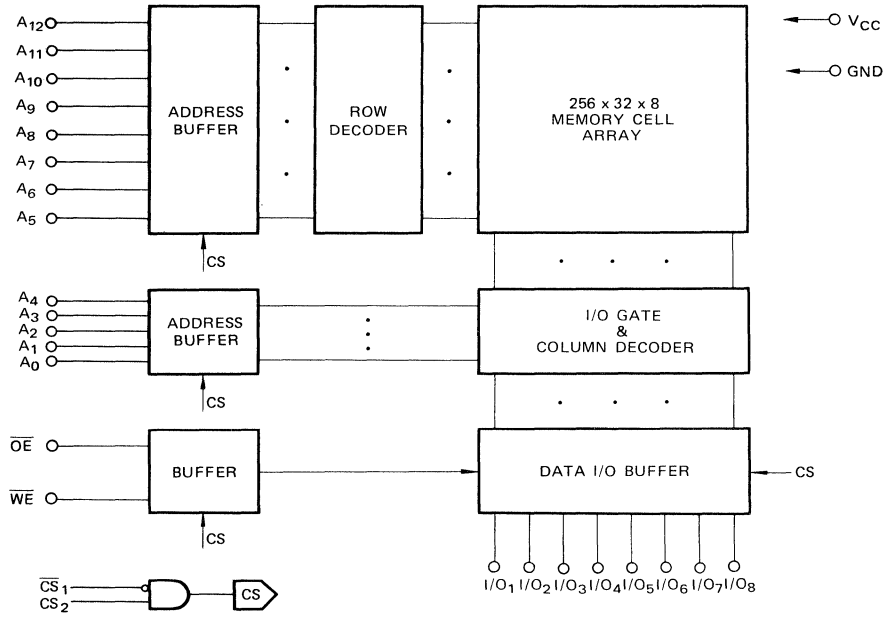
*−2.0V for pulse width less than 20ns.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB 8464A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	D_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

*-2.0 V Min for pulse width less than 20 ns. (V_{IL} Min. = -0.3 V at DC level)

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

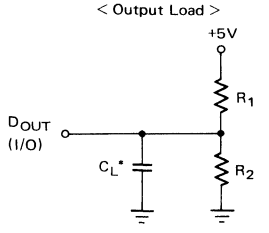
Parameter	Symbol	MB 8464A-80/10/15		MB 8464A-80L/80LL 10L/10LL/15L/15LL			Unit	Test Condition
		Min	Max	Min	Typ	Max		
Standby Supply Current	I_{SB1}		2		1μA	0.1	mA	$CS_2 \leqq 0.2V$, $\overline{CS_1} \geqq V_{CC}-0.2V$ ($CS_2 \leqq 0.2V$ or $CS_2 \geqq V_{CC}-0.2V$)
	I_{SB2}		3			3	mA	$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$
Active Supply Current	I_{CC1}		50			50	mA	$\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0mA
Operating Supply Current	I_{CC2}		60			60	mA	Cycle = Min., Duty = 100% I_{OUT} = 0mA
Input Leakage Current	I_{LI}	-1	1	-1		-1	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-2	2	-2		2	μA	$V_{I/O}$ = 0V to V_{CC} $\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4			V	I_{OH} = -1.0mA
Output Low Voltage	V_{OL}		0.4			0.4	V	I_{OL} = 2.1mA

Note: All voltages are referenced to GND

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load:

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100 pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5 pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}



*Including jig and stray capacitance

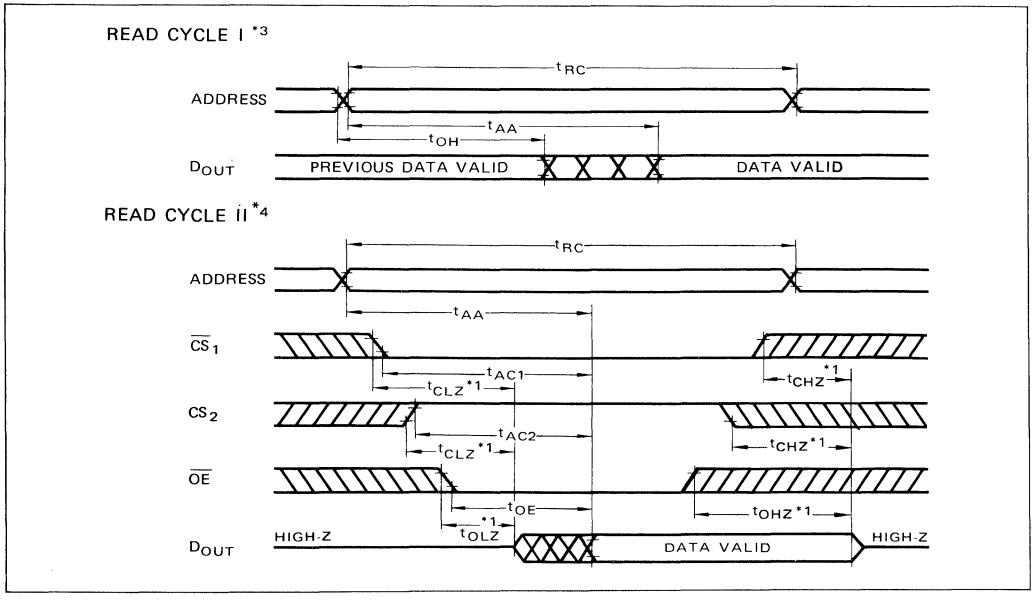
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB 8464A-80/80L/80LL		MB 8464A-10/10L/10LL		MB 8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		150		ns
Address Access Time	t_{AA}		80		100		150	ns
$\overline{CS}_1$ Access Time	t_{AC1}		80		100		150	ns
CS_2 Access Time	t_{AC2}		80		100		150	ns
Output Enable to Output Valid	t_{OE}		35		45		55	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output Low-Z*1	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*1	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*1	t_{CHZ}		35		35		40	ns
Output Enable to Output High-Z*1	t_{OHZ}		30		35		40	ns

READ CYCLE TIMING DIAGRAM*2



Note: *1 Transition is measured at the point of ±500mV from steady state voltage.

*2 $\overline{WE}$ is high for Read Cycle.

*3 Device is continuously selected, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $CS_2 = V_{IH}$.

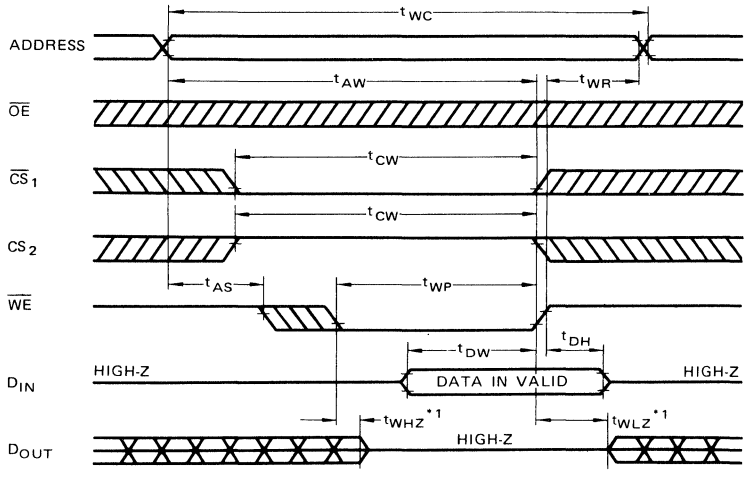
*4 Address vaild prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high.

WRITE CYCLE

Parameter	Symbol	MB 8464A-80/80L/80LL		MB 8464A-10/10L/10LL		MB 8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		150		ns
Address Valid to End of Write	t_{AW}	60		80		100		ns
Chip Select to End of Write	t_{CW}	60		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		ns
Data Hold Time	t_{DH}	5		5		5		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	10		10		10		ns
Write Enable to Output Low-Z*1	t_{WLZ}	5		5		5		ns
Write Enable to Output High-Z*1	t_{WHZ}		30		35		40	ns

WRITE CYCLE TIMING DIAGRAM *2

WRITE CYCLE I : $\overline{WE}$ CONTROLLED



Note: *1 Transition is measured at the point of ±500mV from steady state voltage.

*2 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

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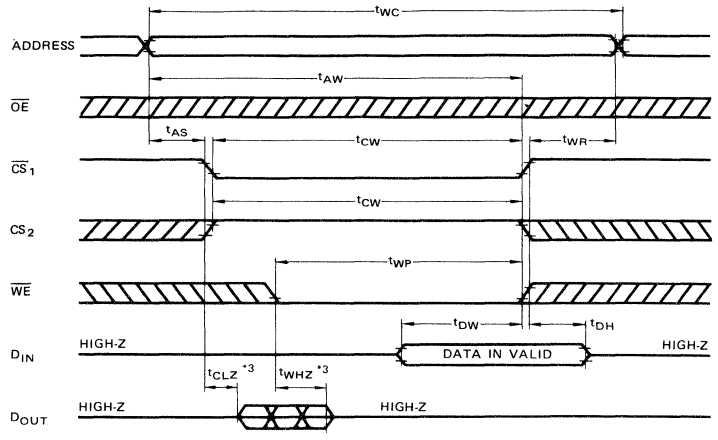
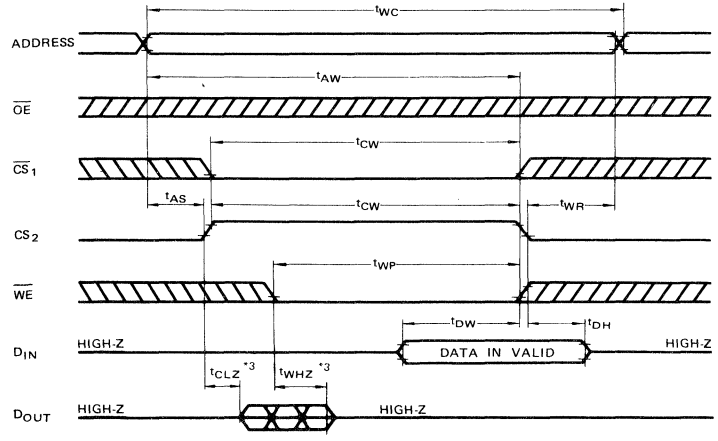
WRITE CYCLE II: $\overline{CS_1}$ CONTROLLED*1



WRITE CYCLE III: CS_2 CONTROLLED*2



Note: *1 If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{OE}$, $\overline{CS_1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

DATA RETENTION CHARACTERISTICS

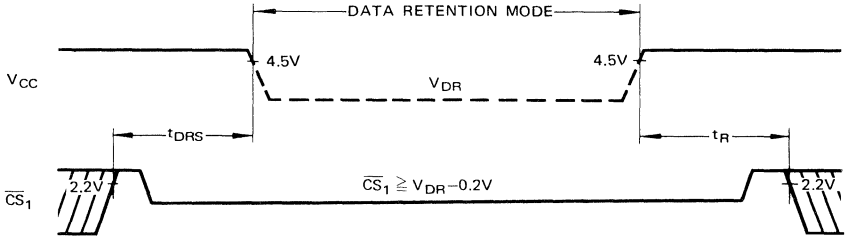
(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current*2	Standard	I_{DR}			1.0	mA
	L-Version			1.0	25	μA
	LL-Version*3			1.0	2.0	μA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

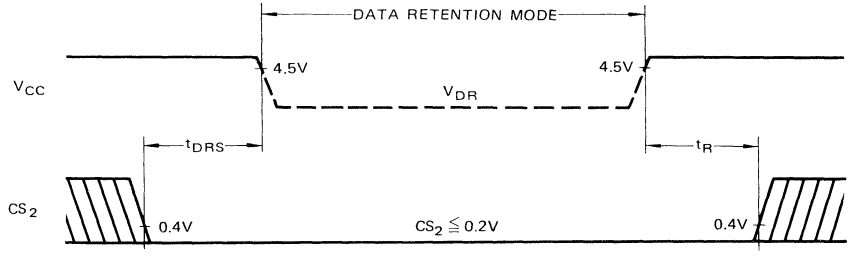
Note: *2 CS_2 controlled: V_{DR} = 3.0V, $CS_2 \leqq 0.2V$
$\overline{CS_1}$ controlled: V_{DR} = 3.0V, $\overline{CS_1} \geqq V_{DR}-0.2V$ ($CS_2 \leqq 0.2V$ or $CS_2 \geqq V_{DR}-0.2V$)
*3 V_{DR}=3.0V, T_A=0°C to 40°C

DATA RETENTION TIMING

DATA RETENTION I: $\overline{CS_1}$ CONTROLLED



DATA RETENTION II: CS_2 CONTROLLED



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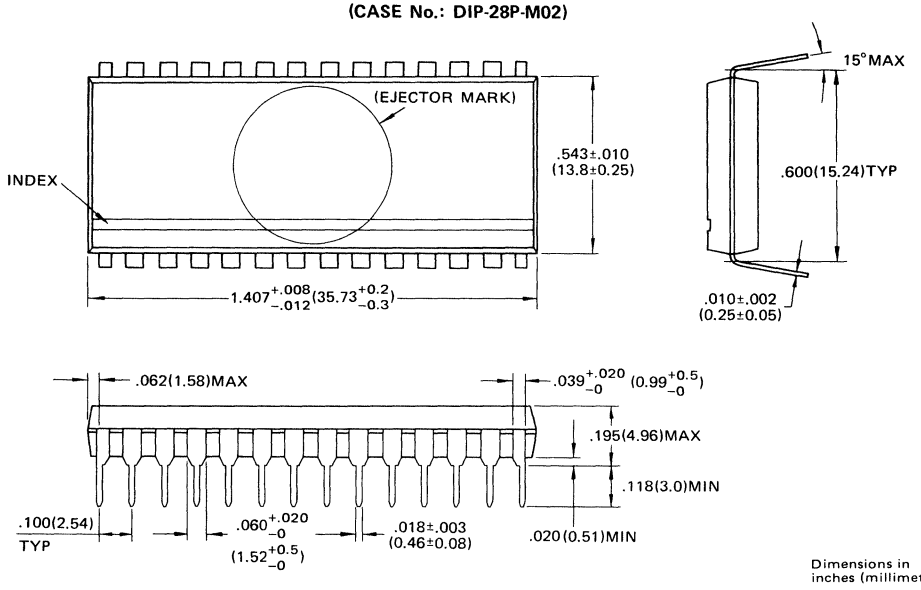
PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)

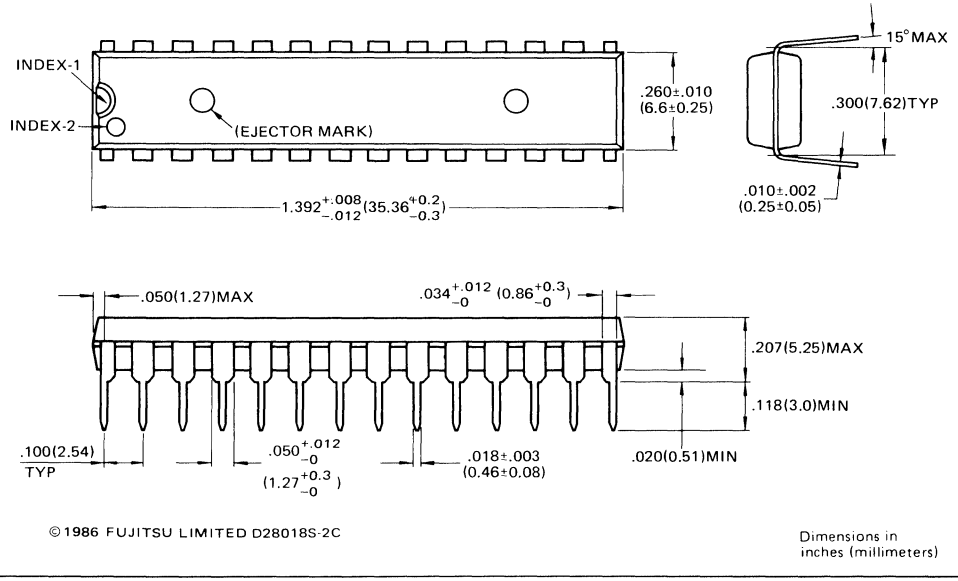


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in
inches (millimeters)

3

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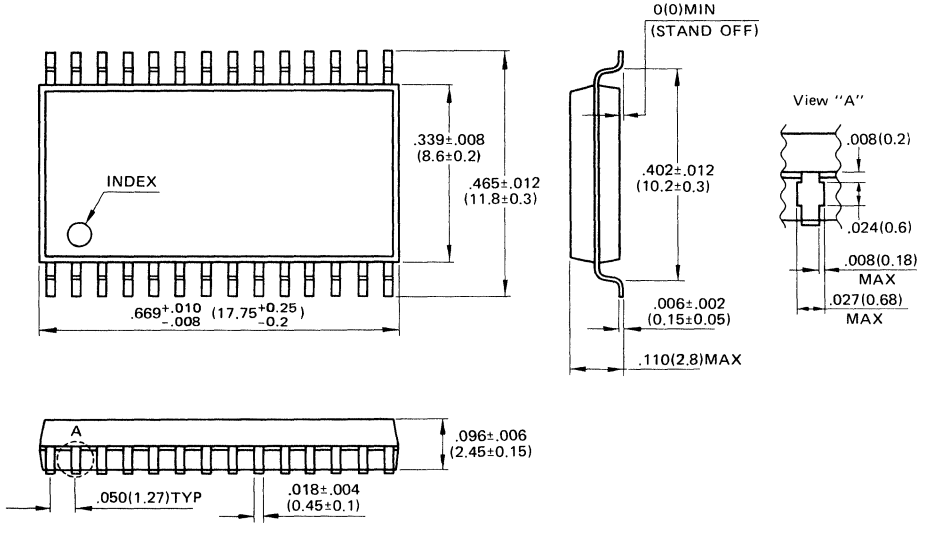
PACKAGE DIMENSIONS

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)

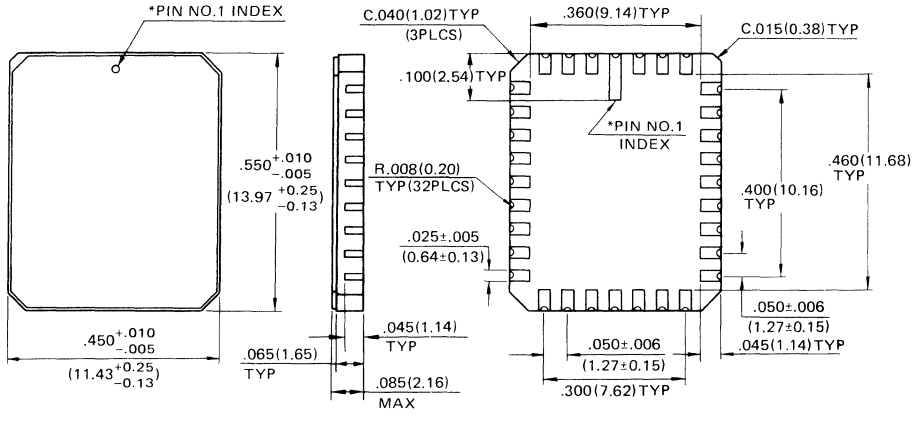


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

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FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB 84256-10/10L/10LL
MB 84256-12/12L/12LL
MB 84256-15/15L/15LL

August 1986
Edition 2.0

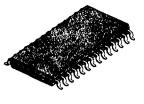
256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronouse circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

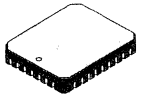
The MB 84256 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
  120 ns max. (MB 84256-12/12L/12LL)
  150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
  CMOS level: 5.5 mW max. (MB 84256-10/12/15)
  0.55 mW max. (MB 84256-10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB 84256-10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)

PLASTIC PACKAGE
DIP-28P-M02

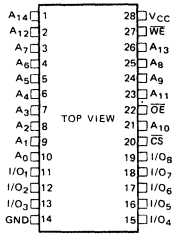


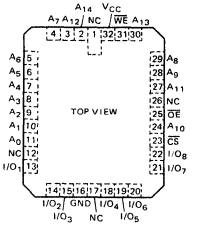
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC}+0.5	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	CERAMIC	T_{STG}	−65 to +150	°C
	PLASTIC		−40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

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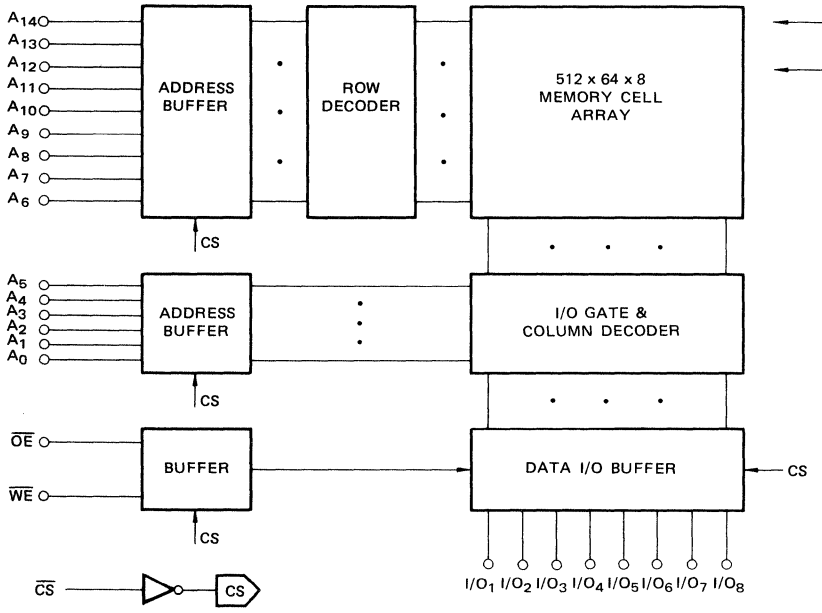
Fig. 1 – MB 84256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	DOUT DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-2.0 *		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

* -2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.3 V at DC level)

3

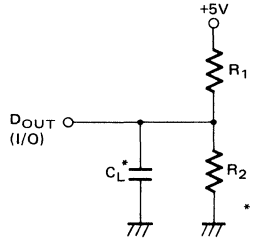
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB 84256-10/12/15		MB 84256-10L/10LL/12L/12LL/15L/15LL		Unit	Test Conditions
		Min	Max	Min	Max		
Standby Supply Current	I_{SB1}		1		0.1	mA	$\overline{CS} \geqq V_{CC}$-0.2V
	I_{SB2}		3		3		$\overline{CS} = V_{IH}$
Active Supply Current	I_{CC1}		45		45	mA	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating Supply Current	I_{CC2}		70		70		Cycle = Min., Duty = 100%, I_{OUT} = 0 mA
Input Leakage Current	I_{LI}	-1	1	-1	1	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	-1	1	-1	1	μA	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4		V	I_{OH} = -1.0 mA
Output Low Voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to GND

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V; Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

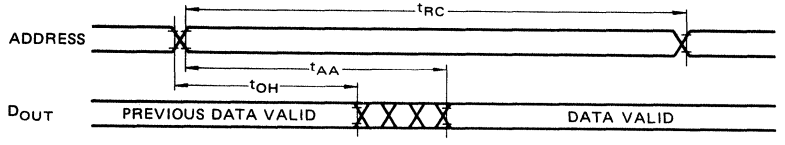
(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

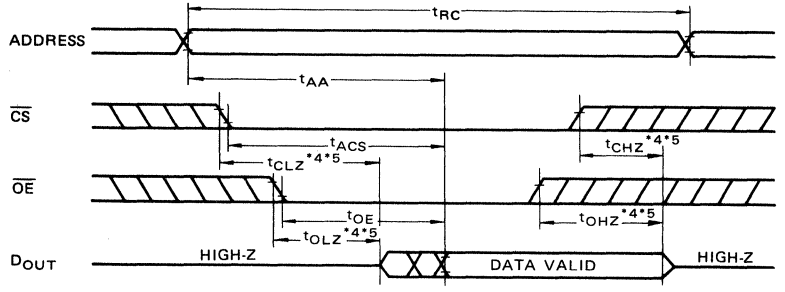
Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time*2	t_{AA}		100		120		150	ns
$\overline{CS}$ Access Time*3	t_{ACS}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		40		50		60	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Select to Output Low-Z*4*5	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*4*5	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*4*5	t_{CHZ}		40		40		50	ns
Output Enable to Output High-Z*4*5	t_{OHZ}		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS}$ CONTROLLED*3



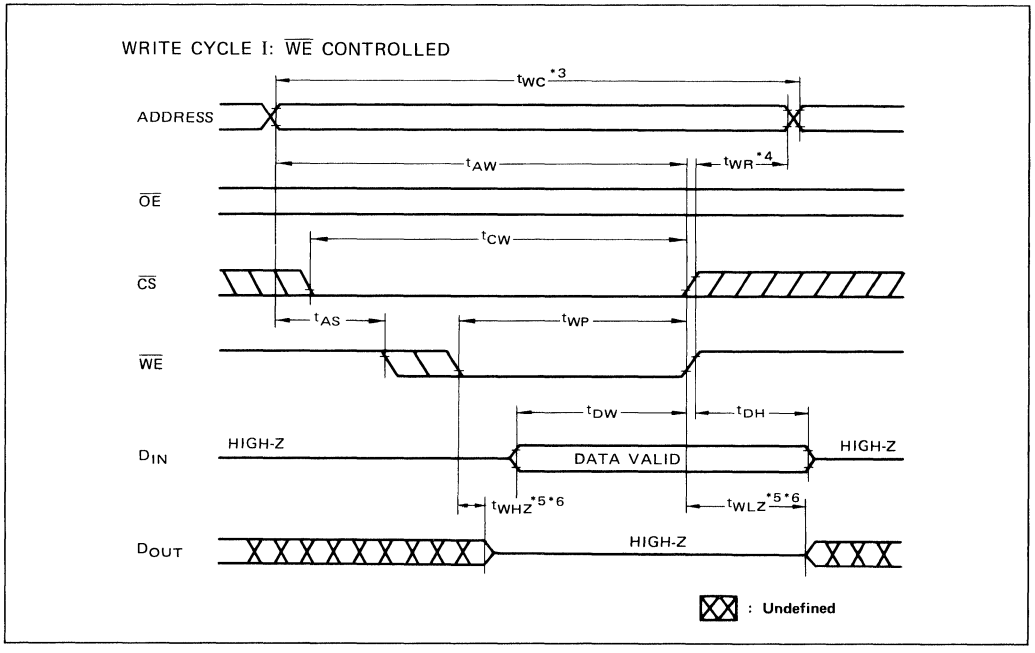
: Undenfined

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1*2

Parameter	Symbol	MB 84256-10/ 10L/10LL		MB 84256-12/ 12L/12LL		MB 84256-15/ 15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	100		120		150		ns
Address Valid to End of Write	t_{AW}	80		85		100		ns
Chip Select to End of Write	t_{CW}	80		85		100		ns
Data Valid to End of Write	t_{DW}	40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time*4	t_{WR}	5		5		5		ns
$\overline{WE}$ to Output Low-Z*5*6	t_{WLZ}	5		5		5		ns
$\overline{WE}$ to Output High-Z*5*6	t_{WHZ}		40		40		50	ns

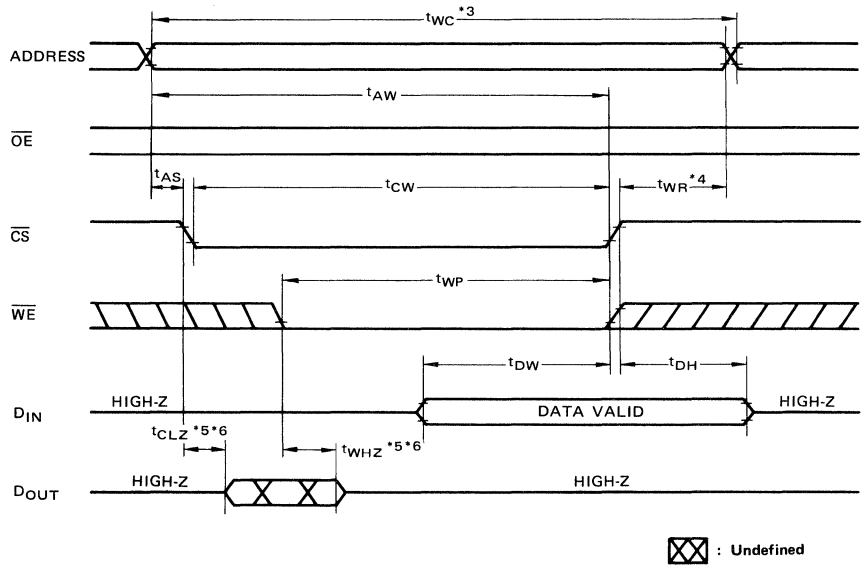
WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined form last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

3

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is specified with Load II in Fig. 2.

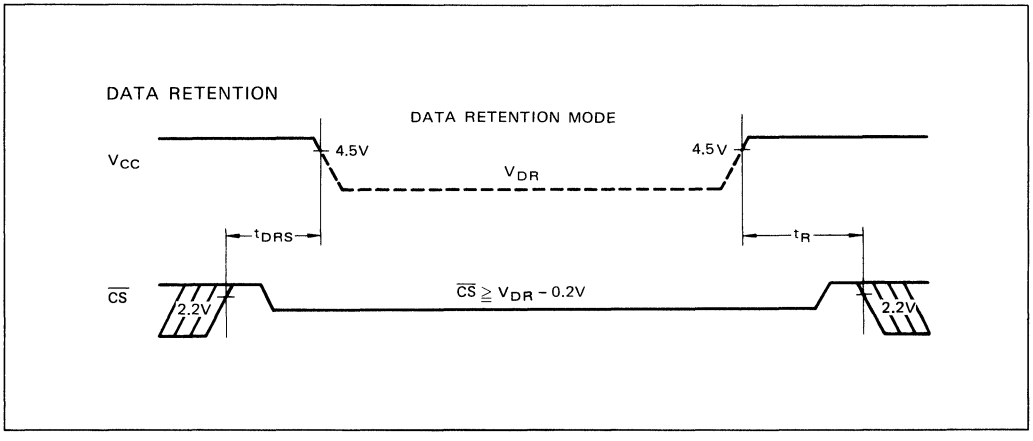
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Data Retention Supply Voltage*1		V_{DR}	2.0	5.5	V
Data Retention*2 Supply Current	Standard	I_{DR}		1	mA
	L-Version			50	μA
	LL-Version*3			5	
Data Retention Setup Time		t_{DRS}	0		ns
Operation Recovery Time		t_R	t_{RC}		ns

Note: *1 $\overline{CS} \geqq V_{DR}-0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geqq V_{DR}-0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

DATA RETENTION TIMING

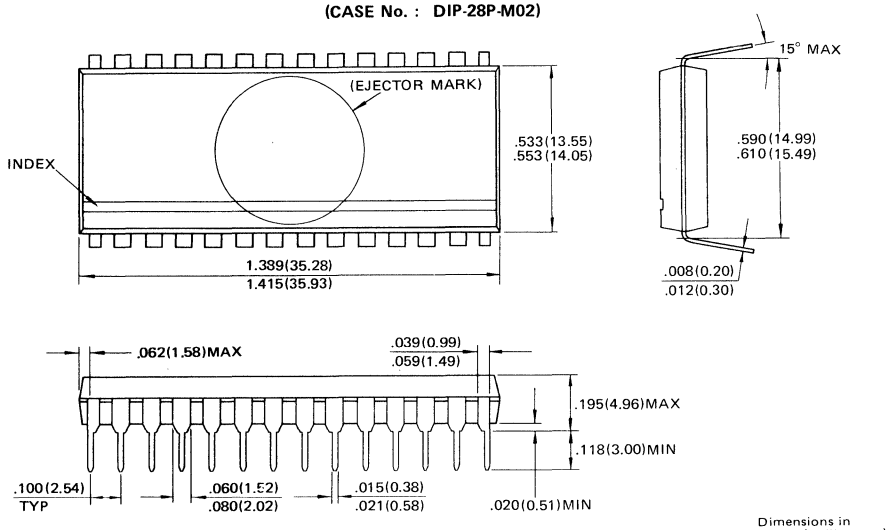


3

PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)

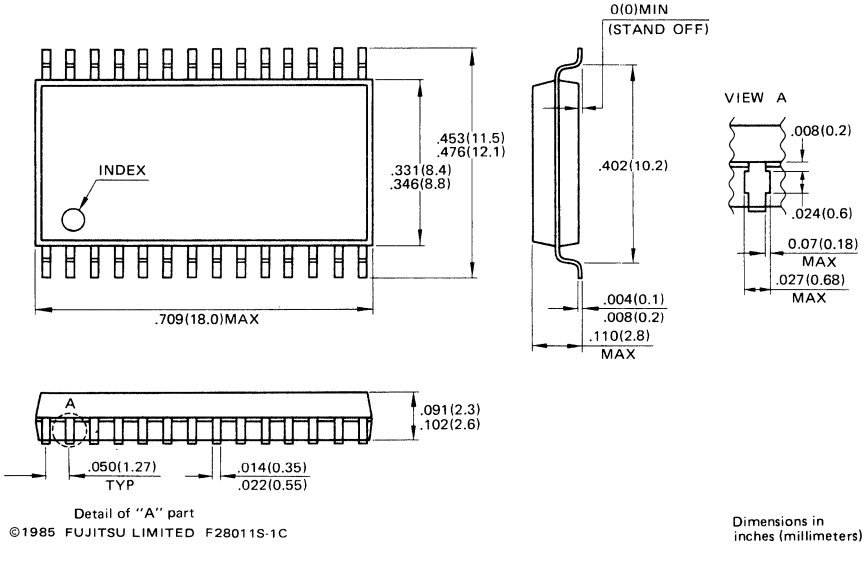


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in
inches (millimeters)

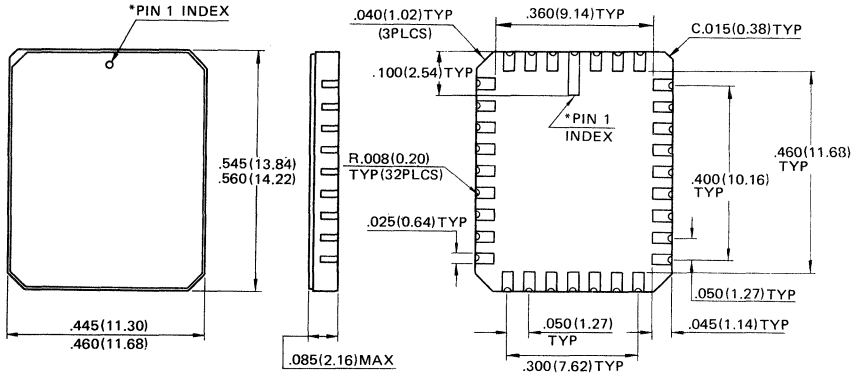
3

3

PACKAGE DIMENSIONS

(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice

FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

MB84256A-70/70L/70LL
MB84256A-10/10L/10LL
MB84256A-12/12L/12LL
MB84256A-15/15L/15LL

TS256-B889
Sept. 1988

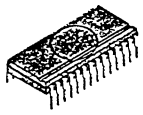
256K-BIT (32,768x8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

PRELIMINARY

The Fujitsu MB84256A is a 32,768-word by 8-bit static random access memory fabricated with a CMOS sillicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The MB84256A is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization : 32,768 x 8 bits
- Fast access time : 70 ns max. (MB84256A-70/70L/70LL)
  100 ns max. (MB84256A-10/10L/10LL)
  120 ns max. (MB84256A-12/12L/12LL)
  150 ns max. (MB84256A-15/15L/15LL)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby :
  CMOS level: 5.5 mW max. (MB84256A-70/10/12/15)
  0.55 mW max. (MB84256A-70L/70LL/10L/10LL/12L/12LL/15L/15LL)
  TTL level: 16.5 mW max. (MB84256A-70/70L/70LL/10/10L/10LL/12/12L/12LL/15/15L/15LL)
- Data retention: 2.0V min.
- Standard 28-pin DIP (600mil) (Suffix: P)
- Standard 28-pin DIP (300mil) (Suffix: P-SK)
- Standard 28-pin Bend-type FPT (450mil) (Suffix: PF)

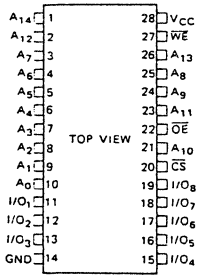


PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04

PLASTIC PACKAGE
FPT-28P-M02

PIN ASSIGNMENT



ABSOLUTEMAXIMUM RATINGS (see NOTE)

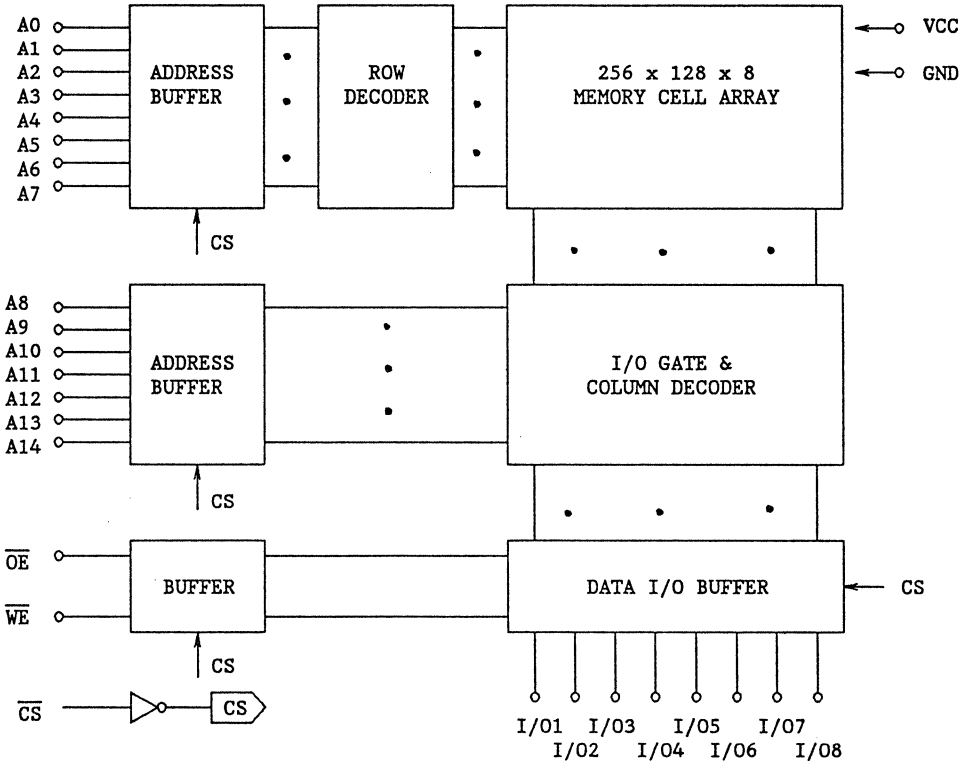
Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to VCC+0.5	V
Output Voltage	VI/O	-0.5 to VCC+0.5	V
Temperature under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	ISB	High-Z
L	H	H	DOUT Disable	ICC	High-Z
L	L	H	Read	ICC	DOUT
L	X	L	Write	ICC	DIN

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance (VIN=0V)	CIN			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

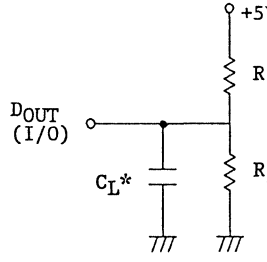
(Recommended operating conditions otherwise noted.)

Parameter		Symbol	MB84256A-70/10/12/15		MB84256A-70L/70LL/10L/10LL/12L/12LL/15L/15LL		Unit	Test Condition
			Min	Max	Min	Max		
Standby Supply Current		ISB1		1		0.1	mA	$\overline{CS}$≥VCC-0.2V
		ISB2		3		3	mA	$\overline{CS}$=VIH
Active Supply Current		ICC1		55		55	mA	VIN=VIH or VIL $\overline{CS}$=VIL, IOUT=0mA
Operating Supply Current	-70	ICC2		80		80	mA	Cycle=Min. Duty=100% IOUT=0mA
	-10/12/15			70		70		
Input Leakage Current		ILI	-1	1	-1	1	µA	VIN=0V to VCC
Output Leakage Current		ILI/O	-1	1	-1	1	µA	$\overline{VI}$/O=0V to VCC $\overline{CS}$=VIH $\overline{OE}$=VIH or $\overline{WE}$=VIL
Input High Voltage		VIH	2.2	VCC +0.3	2.2	VCC +0.3	V	
Input Low Voltage		VIL	-3.0 *	0.8	-3.0 *	0.8	V	
Output High Voltage		VOH	2.4		2.4		V	IOH=-1.0mA
Output Low Voltage		VOL		0.4		0.4	V	IOL=2.1mA

Note: All voltages are referenced to GND.

*: -3.0V min. for pulse width less than 20 ns. (VIL min. = -0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times:
  5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels
  Input: VIL=0.8V, VIH=2.2V
  Output: VOL=0.8V, VOH=2.0V
- Output Load

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load1	1.8KΩ	990Ω	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load2	1.8KΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS

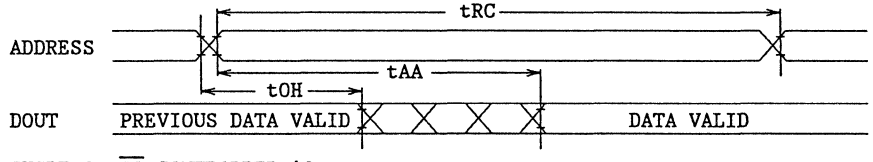
(Recommended operating conditions otherwise noted.)

READ CYCLE *1

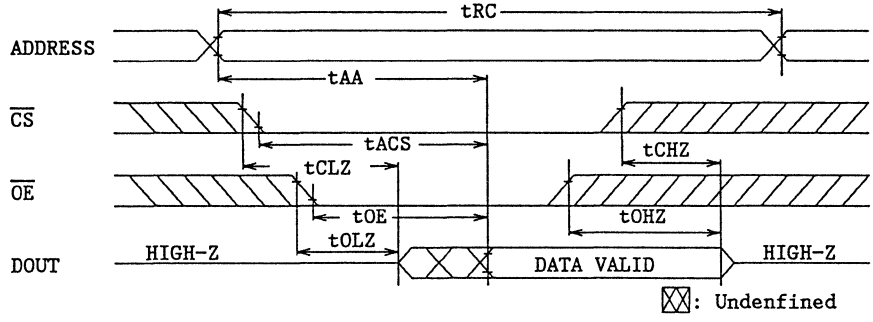
Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	70		100		120		150		ns
Address Access Time *2	tAA		70		100		120		150	ns
$\overline{CS}$ Access Time *3	tACS		70		100		120		150	ns
Output Enable to Output Valid	tOE		35		40		50		60	ns
Output Hold from Address Change	tOH	20		20		20		20		ns
Chip Select to Output Low-Z *4*5	tCLZ	10		10		10		10		ns
Output Enable to Output Low-Z *4*5	tOLZ	5		5		5		5		ns
Chip Select to Output High-Z *4*5	tCHZ		25		40		40		50	ns
Output Enable to Output High-Z *4*5	tOHZ		25		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2: $\overline{CS}$ CONTROLLED *3

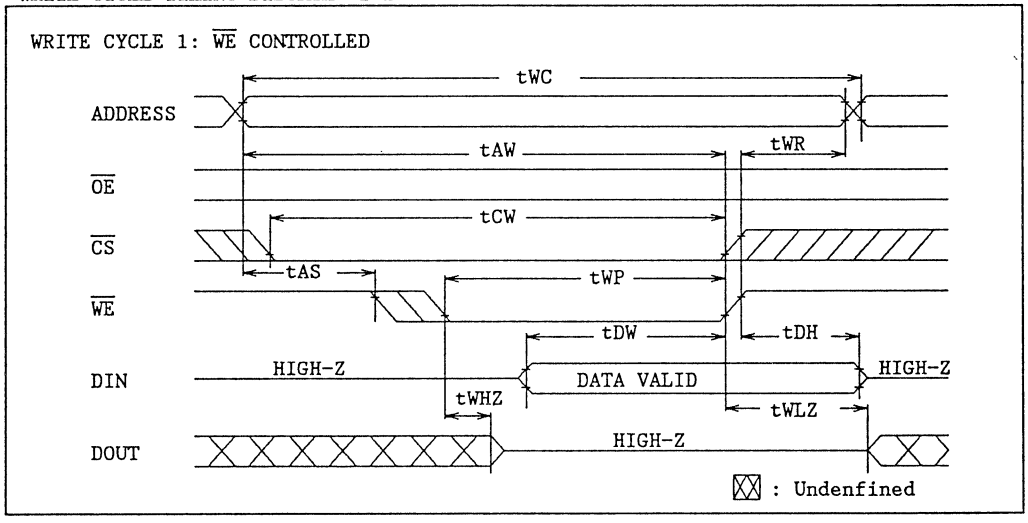


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load 2 in Fig. 2.

WRITE CYCLE *1*2

Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	tWC	70		100		120		150		ns
Address Valid to End of Write	tAW	50		80		85		100		ns
Chip Select to End of Write	tCW	50		80		85		100		ns
Data Valid to End of Write	tDW	25		40		45		50		ns
Data Hold Time	tDH	0		0		0		0		ns
Write Pulse Width	tWP	50		60		70		90		ns
Address Setup Time	tAS	0		0		0		0		ns
Write Recovery Time *4	tWR	5		5		5		5		ns
$\overline{WE}$ to Output Low-Z *5*6	tWLZ	5		5		5		5		ns
$\overline{WE}$ to Output High-Z *5*6	tWHZ		25		40		40		50	ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

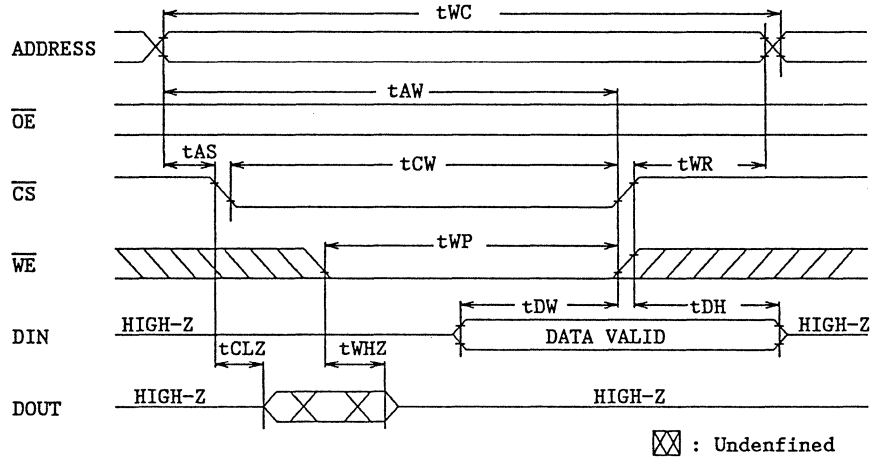
*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage.

*6 This parameter is specified with Load 2 in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1*2

WRITE CYCLE 2: $\overline{CS}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage.

*6 This parameter is specified with Load 2 in Fig. 2.

DATA RETENTION CHARACTERISTICS

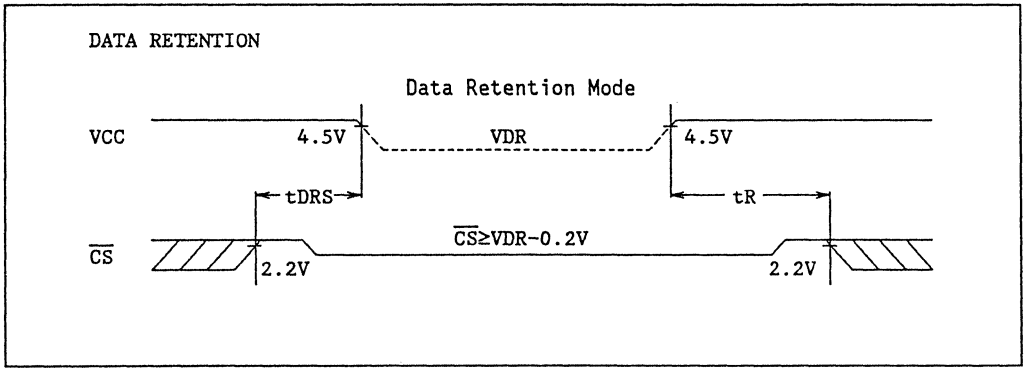
(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1		VDR	2.0		5.5	V
Data Retention Supply Current *2	MB84256A-70/10/12/15	IDR			1.0	mA
	MB84256A-70L/10L/12L/15L			1.0	50	µA
	MB84256A-70LL/10LL/12LL/15LL			1.0	5.0 *3	
Data Retention Setup Time		tDRS	0			ns
Operation Recovery Time		tR	tRC			ns

Note: *1 $\overline{CS}$≥VDR-0.2V
*2 VDR=3.0V, $\overline{CS}$≥VDR-0.2V
*3 VDR=3.0V, TA=40°C

3

DATA RETENTION TIMING

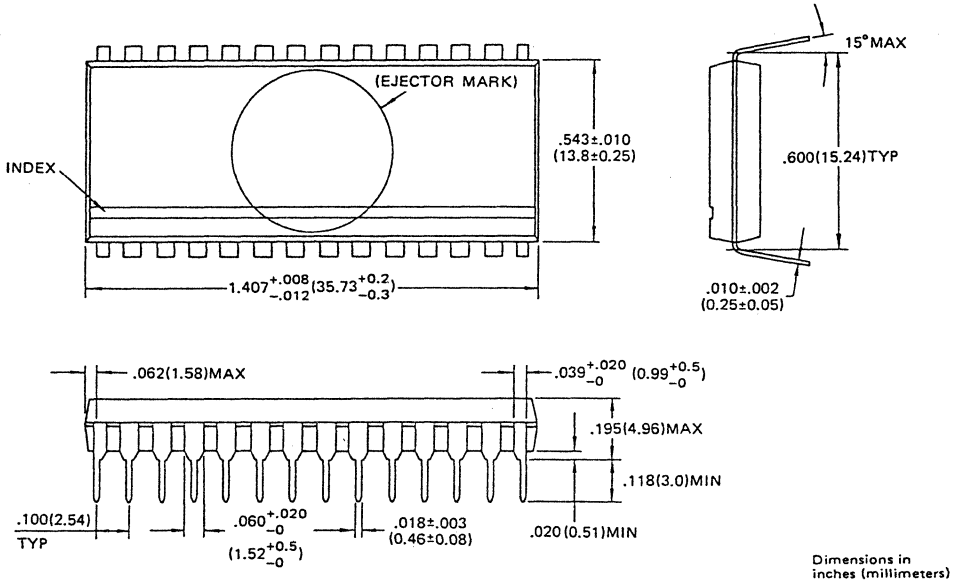


3

PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)

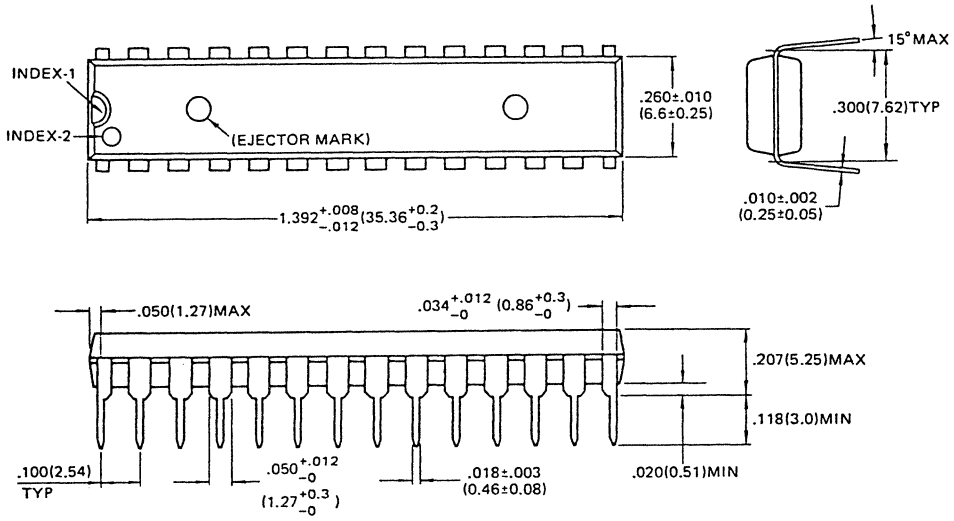


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in
inches (millimeters)

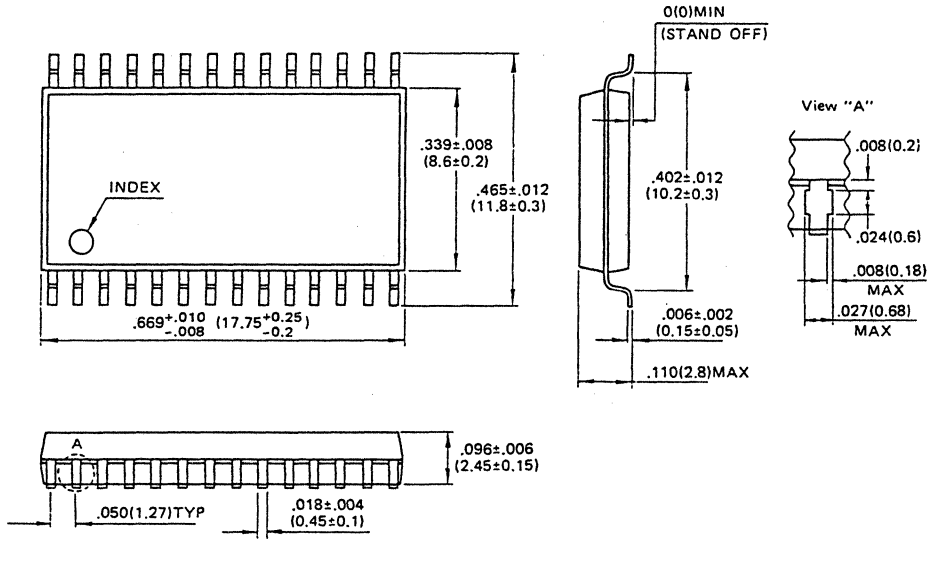
3

3

PACKAGE DIMENSIONS

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in
inches (millimeters)

TS258–C89Y
Nov. 1989

FUJITSU

DATA SHEET

MB84F256-25
CMOS 256K BIT LOW POWER SRAM

32,768-WORD x 8-BIT FULL CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION

PRELIMINARY

The Fujitsu MB84F256 is a 32,768–word by 8–bit static random access memory. Fabricated with full CMOS circuit, MB84F256 realizes extremely low data retention current compared with that of MB84256, which can allows MB84F256 to use non–volatile memory using a back up battery.

The MB84F256 has 600mil 28–pin plastic DIP package and 28–pin plastic SOP package as package option.

The device suits for application where, low and wide supply voltage and low power comsumption are required.

- Organization: 32,768 words x 8 bits
- Static operation: No clocks or refresh required
- Fast access time:
  250ns max. @Vcc=5V
  2000ns max. @Vcc=3V
- Low power comsumption:
  Vcc=3V: 5.0µA (CMOS standby)
  0.5mA (TTL standby)
  20mA (Active)
  Vcc=5V: 10µA (CMOS standby)
  2mA (TTL standby)
  40mA (Active)

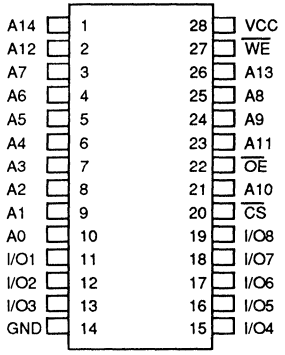
- Data retention voltage: 2.0V min.
- Full CMOS
- 600 mil width 28–pin plastic DIP package (Suffix: –P)
- 450 mil width 28–pin plastic SOP package (Suffix: –PF)

PLASTIC PACKAGE
FPT–28P–M02

PLASTIC PACKAGE
DIP–28P–M02

PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

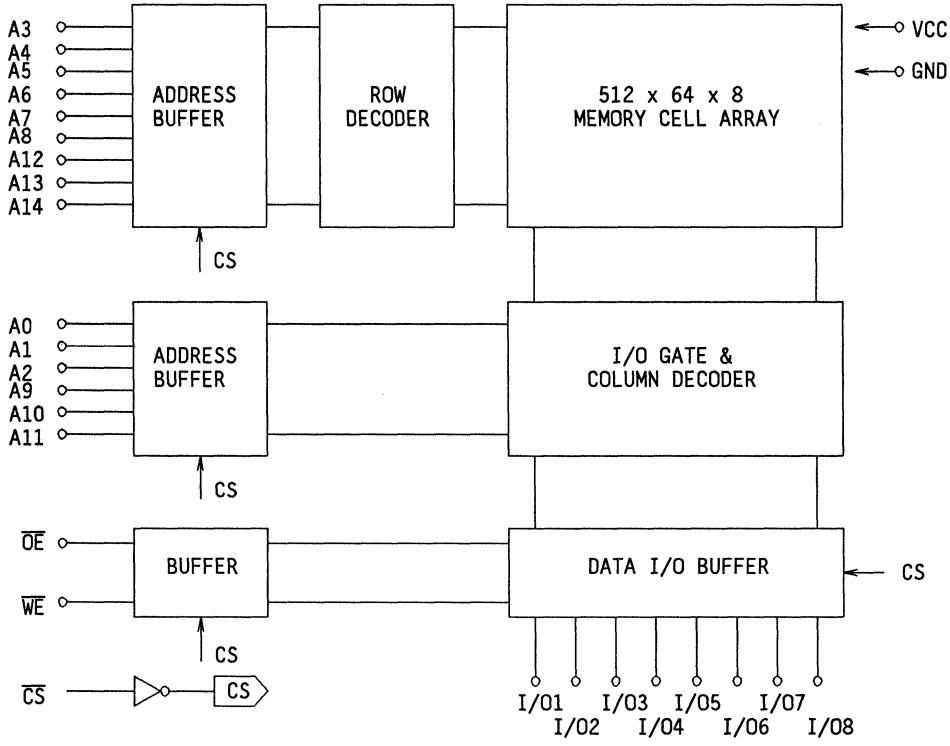
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with to GND	V_{IN}	–0.5 to VCC+0.3	V
Output Voltage on any pin with to GND	$V_{I/O}$	–0.5 to VCC+0.3	V
Power Dissipation	P_D	1.0	W
Output Current	I_{OUT}	±20	mA
Temperature under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 - MB84F256 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	ISB	High-Z
L	H	H	DOUT Disable	ICC	High-Z
L	L	H	Read	ICC	DOUT
L	X	L	Write	ICC	DIN

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			8	pF
Input Capacitance (VIN=0V)	CIN			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	2.2	3.0	3.6	V
		4.0	5.0	5.5	
Ambient Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Supply Voltage VCC (V)	Min	Max	Unit	Condition
Standby Supply	ISB1	2.2V to 3.6V		5.0	µA	$\overline{CS}$≥VCCx0.9V
		4.0V to 5.5V		10.0		
	ISB2	2.2V to 3.6V		0.5	mA	$\overline{CS}$=VIH
		4.0V to 5.5V		2.0		
Active Supply Current	ICC1	2.2V to 3.6V		5.0	mA	VIN=VIH or VIL IOUT=0mA, $\overline{CS}$=VIL
		4.0V to 5.5V		10.0		
Operating Supply Current	ICC2	2.2V to 3.6V		20.0	mA	Cycle=Min Duty=100%,IOUT=0mA
		4.0V to 5.5V		40.0		
InputnLeakage Current	ILI	2.2V to 3.6V		0.5	µA	VIN=0V to VCC
		4.0V to 5.5V		1.0		
Output Leakage Current	ILI/O	2.2V to 3.6V		0.5	µA	VI/O=0 to VCC,CS=VIH $\overline{OE}$=VIH or $\overline{WE}$=VIL
		4.0V to 5.5V		1.0		
Input High Voltage	VIH	2.2V to 3.6V	VCCx0.8	VCC+0.3	V	
		4.0V to 5.5V	2.2	VCC+0.3		
Input Low Voltage	VIL	2.2V to 3.6V	-0.3	0.3	V	
		4.0V to 5.5V	-0.3	0.6		
Output High Voltage	VOH	2.2V to 3.6V	2.0		V	IOH=-0.5mA
		4.0V to 5.5V	2.4			IOH=-1.0mA
Output Low Voltage	VOL	2.2V to 3.6V		0.3	V	IOL= 1.0mA
		4.0V to 5.5V		0.4		IOL= 2.1mA

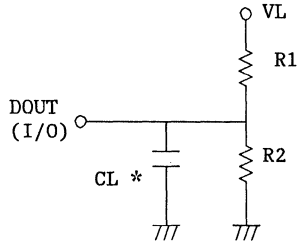
Note: All voltages are referenced to GND.

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Supply Voltage VCC (V)	Conditions
Input Pulse Level	2.2V to 3.6V	VIH=VCC, VIL=0V
	4.0V to 5.5V	VIH=2.4V, VIL=0.5V
Input Pulse Rise & Fall Times	2.2V to 3.6V	5 ns (Transient between 0.3V and VCCx0.8)
	4.0V to 5.5V	5 ns (Transient between 0.7V and 2.2V)
Timing Reference Level	2.2V to 3.6V	Input: VIH=VCCx0.8, VIL=0.3V Output: VOH=VCCx0.7, VOL=0.4V
	4.0V to 5.5V	Input: VIH=2.2V, VIL=0.7V Output: VOH=2.2V, VOL=0.8V
Output Load	2.2V to 3.6V	VL=3.0V
	4.0V to 5.5V	VL=5.0V

3

Fig. 2 – AC TEST CONDITIONS



* Including Jig and stray capacitance.

	R1	R2	CL	Parameters Measured
Load1	1.8KΩ	990Ω	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load2	1.8KΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

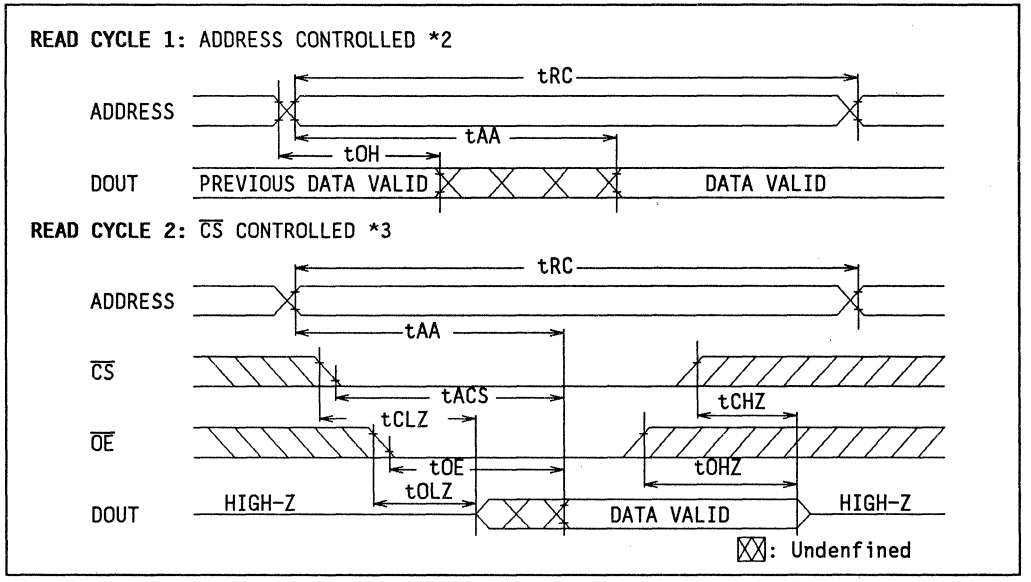
READ CYCLE *1

Parameter	Symbol	VCC= 2.2V to 3.6V		VCC= 4.0V to 5.5V		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	2000		250		ns
Address Access Time *2	tAA		2000		250	ns
$\overline{CS}$ Access Time *3	tACS		2000		250	ns
Output Enable to Output Valid	tOE		500		100	ns
Output Hold from Addresss Change	tOH	100		50		ns
$\overline{CS}$ to Output Low-Z *4*5	tCLZ	70		30		ns
Output Enable to Output Low-Z *4*5	tOLZ	100		20		ns
$\overline{CS}$ to Output High-Z *4*5	tCHZ	40	100	5	50	ns
Output Enable to Output High-Z *4*5	tOHZ		100		50	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the following points from steady state voltage.
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*5 This parameter is specified with Load 2 in Fig. 2.

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the following points from steady state voltage.
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*5 This parameter is specified with Load 2 in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	VCC= 2.2V to 3.6V		VCC= 4.0V to 5.5V		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	tWC	2000		250		ns
Address Valid to End of Write	tAC	1500		200		ns
Chip Select to End of Write	tCW	1500		200		ns
Data Valid to End of Write	tDW	800		100		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	1000		150		ns
Address Setup Time	tAS	0		0		ns
Write recovery Time *4	tWR	0		0		ns
$\overline{WE}$ to Output Low-Z *5*6	tWLZ	30		10		ns
$\overline{WE}$ to Output High-Z *5*6	tWHZ		100		50	ns

Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.

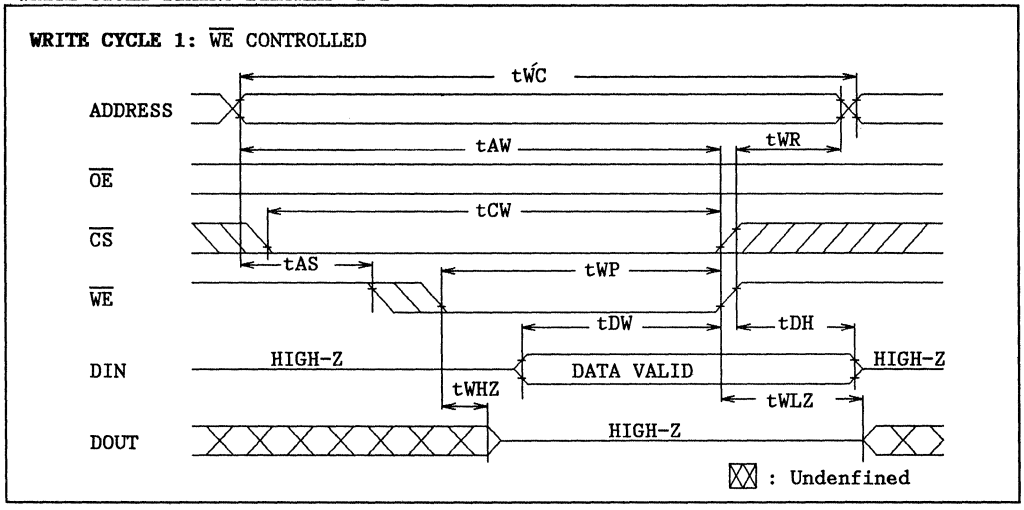
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*6 This parameter is specified with Load 2 in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

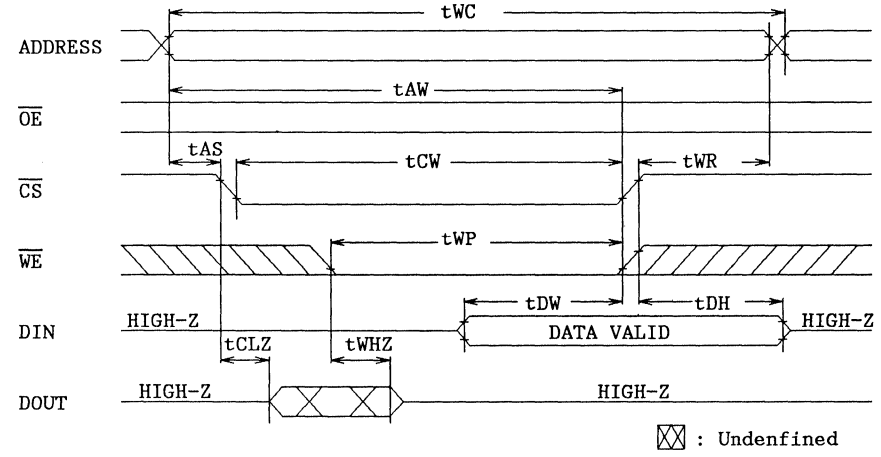
*6 This parameter is specified with Load 2 in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1*2

WRITE CYCLE 2: $\overline{CS}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the following points from steady state voltage.
- VCC=2.2V to 3.6V : ±200mV
- VCC=4.0V to 5.5V : ±500mV

*6 This parameter is specified with Load 2 in Fig. 2.

DATA RETENTION CHARACTERISTICS

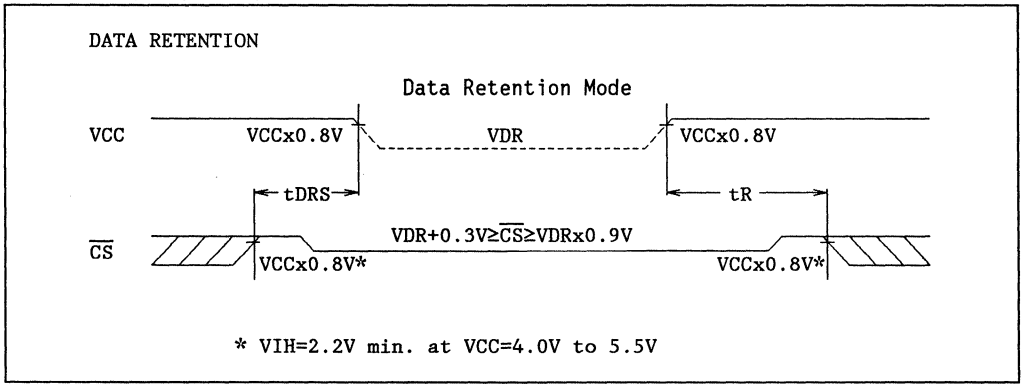
(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Data Retention Supply Voltage *1	VDR	1.1	5.5	V
Data Retention Supply Current *2	IDR		1.0	µA
Data Retention Setup Time	tDRS	0		ns
Operation Recovery Time	tR	tRC *3		ns

3

Note: *1 VDR+0.3V≥$\overline{CS}$≥VDRx0.9
*2 VDR=1.8V, VDR≥$\overline{CS}$≥VDRx0.9
*3 tRC: Read Cycle

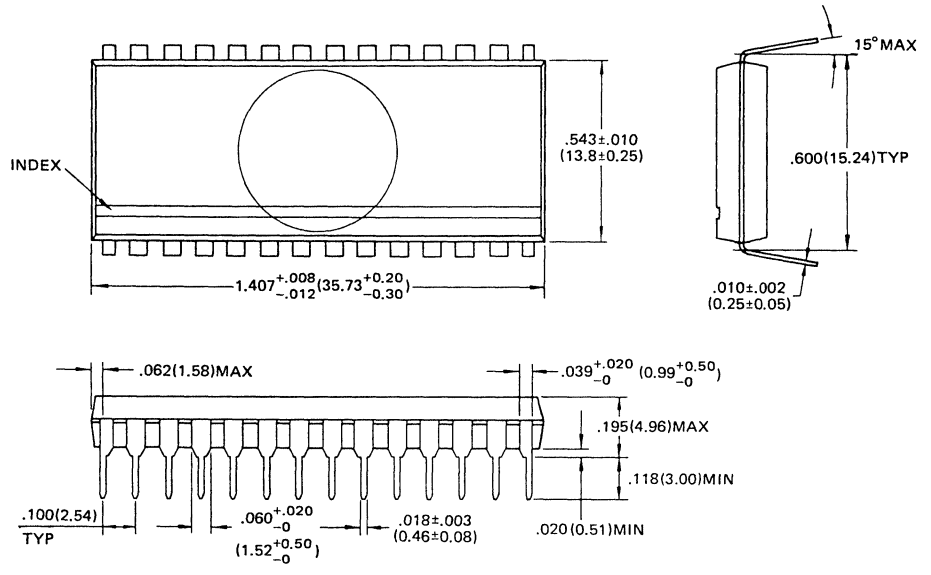
DATA RETENTION TIMING



PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)

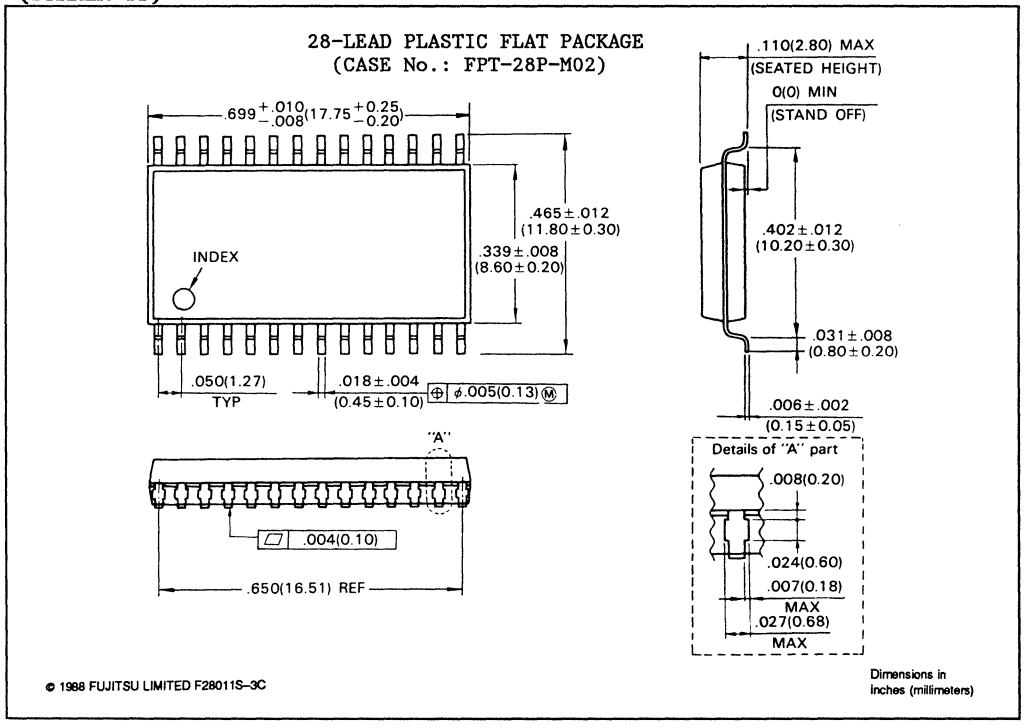


Dimensions in
inches (millimeters)

3

PACKAGE DIMENSIONS

(Suffix: PF)



Dimensions in inches (millimeters)

FUJITSU

CMOS 1,048,576-BIT STATIC RANDOM ACCESS MEMORY

MB841000-80/80L
MB841000-10/10L
MB841000-12/12L

TS279-A89X
Oct. 1989

1M-BIT (131,072x8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

ADVANCE INFO.

The Fujitsu MB841000 is a 131,072-word x 8-bit static random access memory fabricated with a CMOS sillicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The MB841000 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

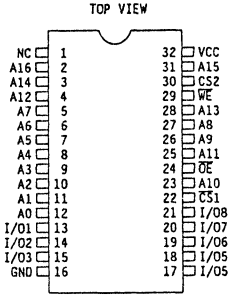
PLASTIC PACKAGE
(DIP-32P-M01)

PLASTIC PACKAGE
(FPT-32P-M03)

3

- Organization : 131,072 x 8 bits
- Fast access time : 80 ns max. (MB841000-80/80L)
  100 ns max. (MB841000-10/10L)
  120 ns max. (MB841000-12/12L)
- Complete static operation: No clock required
- TTL compatible inputs/outputs
- Three state outputs
- Single +5V ±10% power supply
- Low power standby :
  CMOS level: 5.5 mW max. (MB841000-80/10/12)
  1.1 mW max. (MB841000-80L/10L/12L)
  TTL level : 16.5 mW max. (MB841000-80/80L/10/10L/12/12L)
- Data retention: 2.0V min.
- Standard 32-pin DIP (600mil) (Suffix: P)
- Standard 32-pin FPT (525mil) (Suffix: PF)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

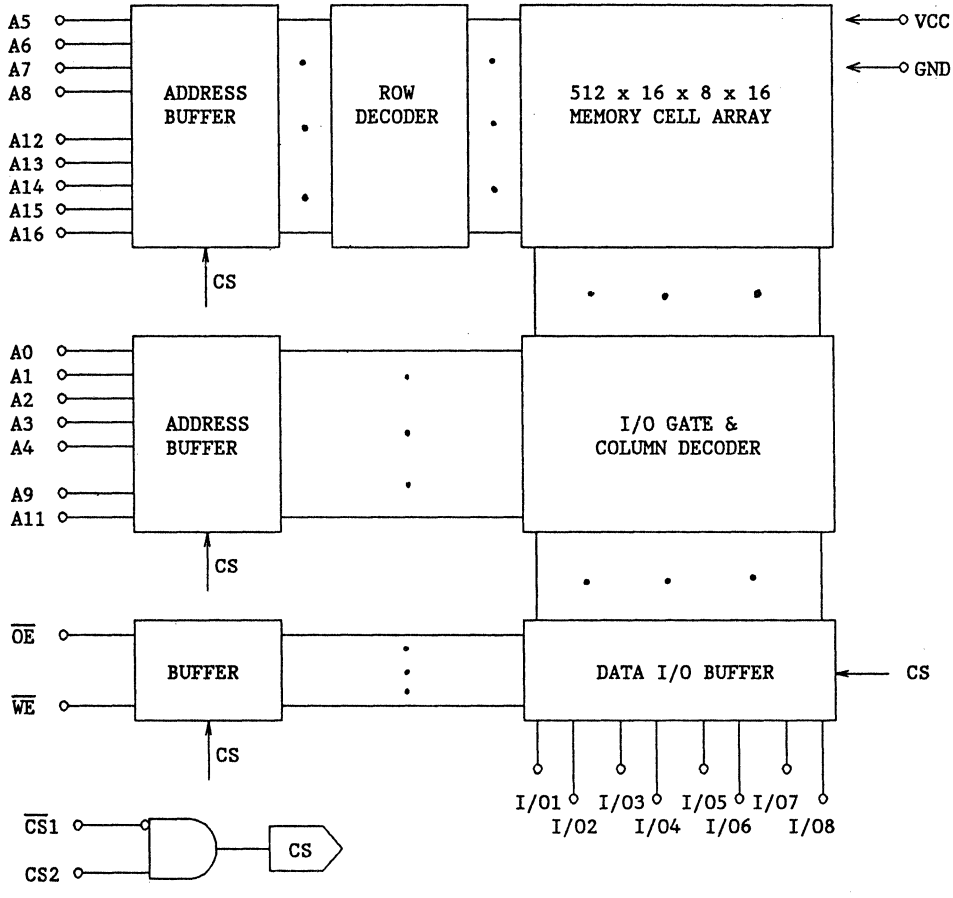
Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to VCC+0.5	V
Output Voltage	VI/O	-0.5 to VCC+0.5	V
Temperature under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB841000 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

FUNCTION TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	ISB	High-Z
X	L	X	X	Not Selected	ISB	High-Z
L	H	H	H	DOUT Disable	ICC	High-Z
L	H	L	H	Read	ICC	DOUT
L	H	X	L	Write	ICC	DIN

CAPACITANCE (TA=25°C, f=1MHz)

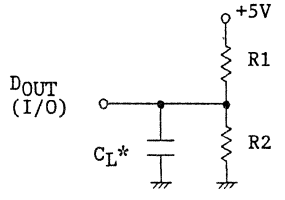
Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O=0V)	CI/O			10	pF
Input Capacitance (VIN=0V)	CIN			8	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB841000 -80/10/12		MB841000 -80L/10L/12L		Unit
			Min	Max	Min	Max	
Standby Supply Current	$\overline{CS2}\leq 0.2V$ or $\overline{CS1}\geq VCC-0.2V$ (with $CS2\leq 0.2V$ or $CS2\geq VCC-0.2V$)	ISB1		1		0.2	mA
	$\overline{CS1}$=VIH or CS2=VIL	ISB2		3		3	mA
Active Supply Current	$\overline{VIN}$=VIH or VIL, $\overline{CS1}$=VIL, CS2=VIH IOUT=0mA	ICC1		5		5	mA
Operating Supply Current	Cycle=Min. Duty=100%, IOUT=0mA	ICC2		80		80	mA
Input Leakage Current	VIN=0V to VCC	ILI	-1	1	-1	1	µA
Output Leakage Current	$\overline{VI/O}$=0V to VCC $\overline{CS1}$=VIH or CS2=VIL or $\overline{OE}$=VIH or $\overline{WE}$=VIL	ILI/O	-2	2	-2	2	µA
Input High Voltage		VIH	2.2	VCC+0.3	2.2	VCC+0.3	V
Input Low Voltage		VIL	-0.3*	0.8	-0.3*	0.8	V
Output High Voltage	IOH=-1.0mA	VOH	2.4		2.4		V
Output Low Voltage	IOL=2.1mA	VOL		0.4		0.4	V

Note: All voltages are referenced to GND.
*: -3.0V min. for pulse width less than 20 ns. (VIL min. = -0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels
  Input: VIL=0.8V, VIH=2.2V
  Output: VOL=0.8V, VOH=2.0V

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load1	1.8KΩ	990Ω	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load2	1.8KΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

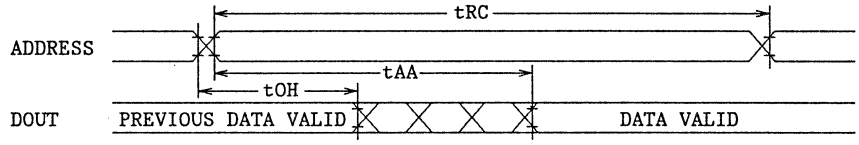
Parameter	Symbol	MB841000-80/80L		MB841000-10/10L		MB841000-12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	80		100		120		ns
Address Access Time	tAA		80		100		120	ns
$\overline{CS}$1 Access Time	tAC1		80		100		120	ns
CS2 Access Time	tAC2		80		100		120	ns
Output Enable to Output Valid	tOE		35		40		50	ns
Output Hold from Address Change	tOH	10		10		10		ns
Chip Select to Output Low-Z *2*3	tCLZ	10		10		10		ns
Output Enable to Output Low-Z *2*3	tOLZ	5		5		5		ns
Chip Select to Output High-Z *2*3	tCHZ		30		35		40	ns
Output Enable to Output High-Z *2*3	tOHZ		30		35		40	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Transition is measured at the point of ±500mV from steady state voltage.
*3 This parameter is specified with Load 2 in Fig. 2.

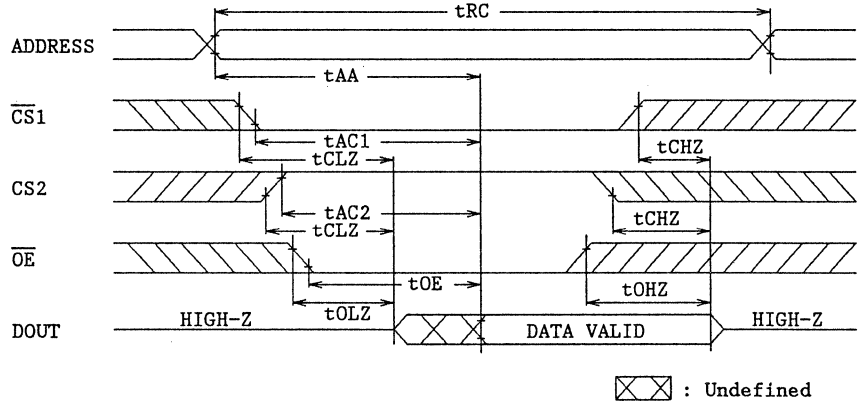
AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2: $\overline{CS1}$, CS2 CONTROLLED *3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS1}$=$\overline{OE}$=VIL, CS2=VIH.
*3 Address valid prior to or coincident with $\overline{CS1}$ transition low, CS2 transition high.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	MB841000-80/80L		MB841000-10/10L		MB841000-12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	tWC	80		100		120		ns
Address Valid to End of Write	tAW	60		80		85		ns
Chip Select to End of Write	tCW	60		80		85		ns
Data Valid to End of Write	tDW	30		40		45		ns
Data Hold Time	tDH	0		0		0		ns
Write Pulse Width	tWP	50		60		70		ns
Address Setup Time	tAS	0		0		0		ns
Write Recovery Time *4	tWR	5		5		5		ns
Write Enable to Output Low-Z *5*6	tWLZ	5		5		5		ns
Write Enable to Output High-Z *5*6	tWHZ		30		35		40	ns

Note: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS1}$ goes high or CS2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

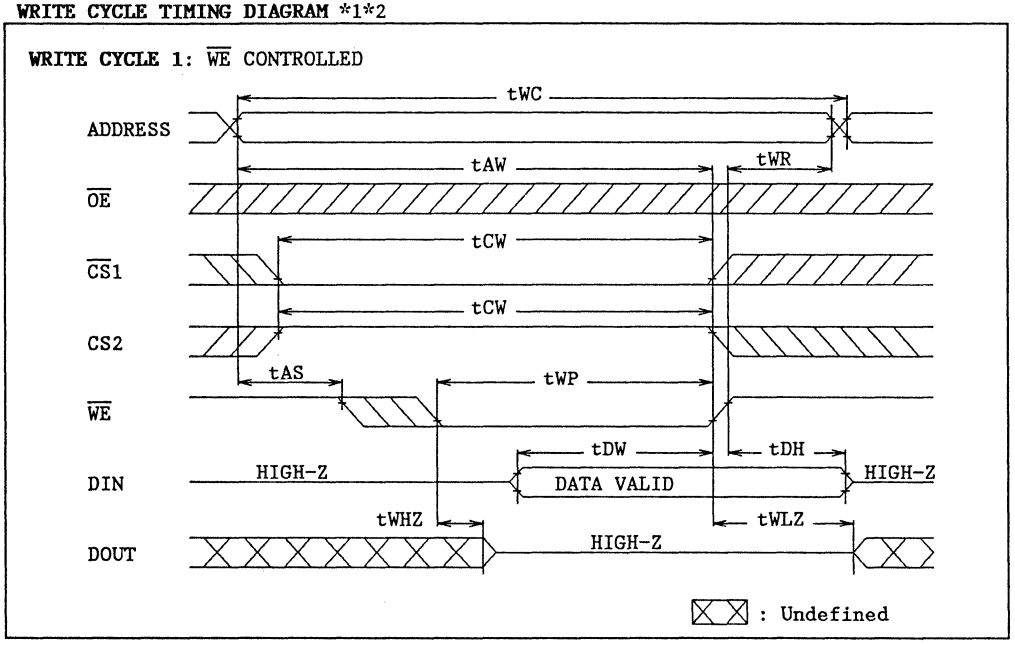
*4 tWR is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage.

*6 This parameter is specified with Load 2 in Fig. 2.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1*2

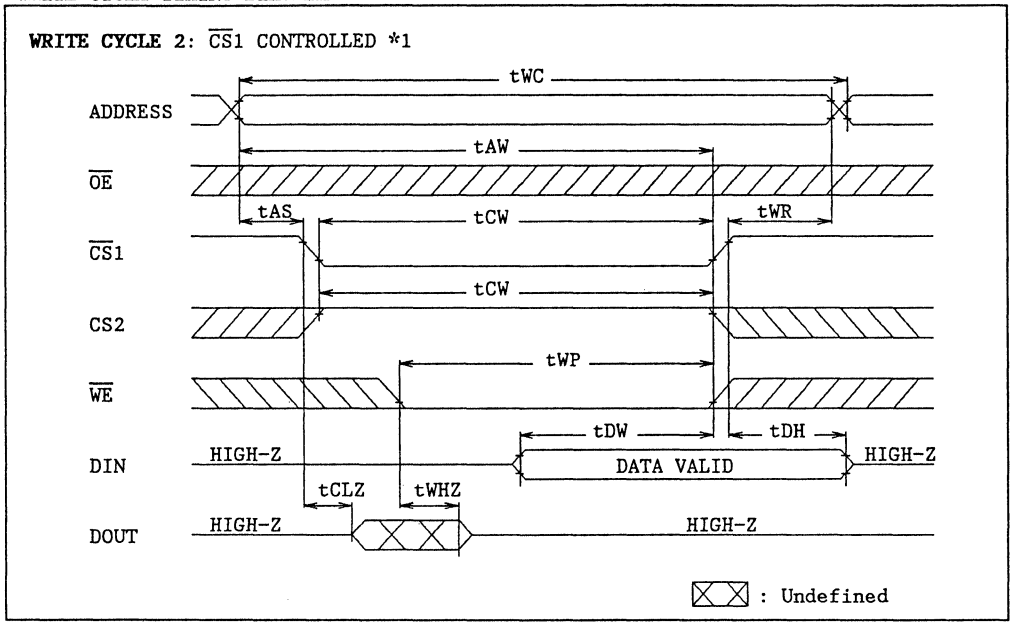


Note: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS1}$ goes high or CS2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

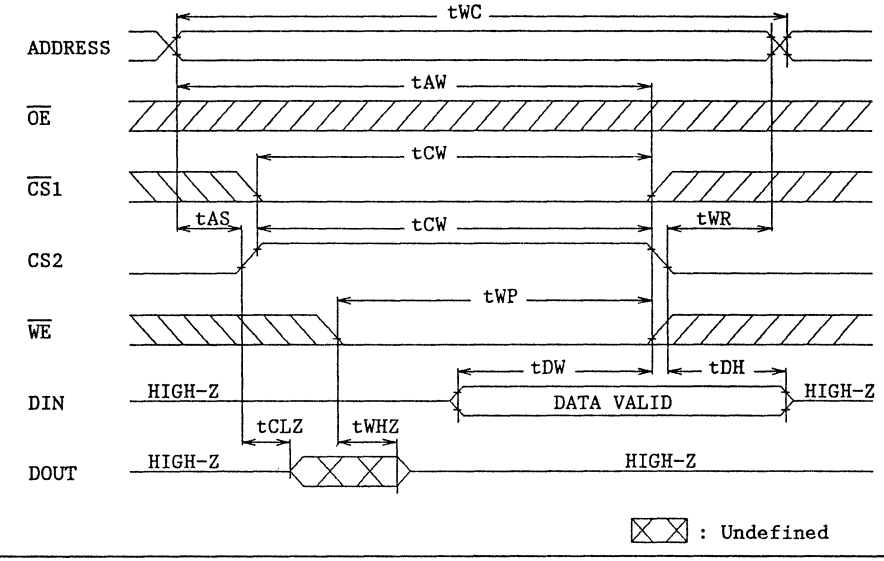


Note: *1 If $\overline{OE}$, CS2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE 3: CS2 CONTROLLED *1



Note: *1 If $\overline{OE}$, $\overline{CS1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

DATA RETENTION CHARACTERISTICS

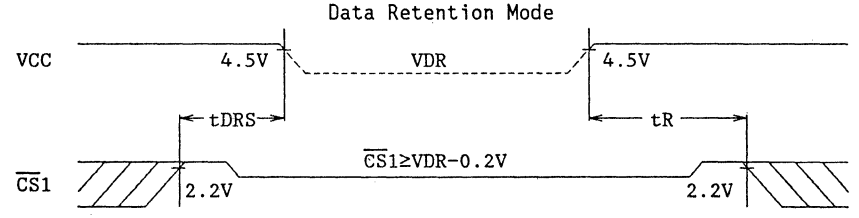
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		VDR	2.0		5.5	V
Data Retention Supply Current *1	MB841000-80/10/12	IDR			0.5	mA
	MB841000-80L/10L/12L				0.1 *2	mA
Data Retention Setup Time		tDRS	0			ns
Operation Recovery Time *2		tR	tRC			ns

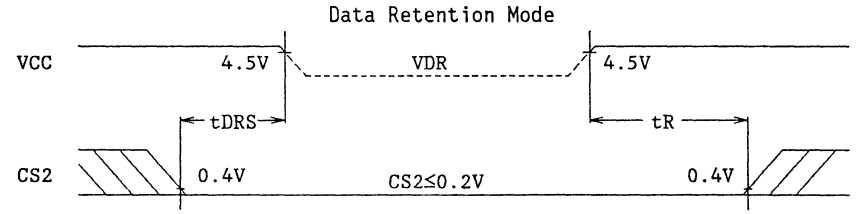
Note: *1 VCC=VDR=3.0V
$\overline{CS1}$≥VDR-0.2V, CS2≥VDR-0.2V or CS2≤0.2V (at $\overline{CS1}$ CONTROLLED)
CS2≤0.2V (at CS2 CONTROLLED)
*2 tRC: Read Cycle Time

DATA RETENTION TIMING

$\overline{CS1}$ CONTROLLED



CS2 CONTROLLED



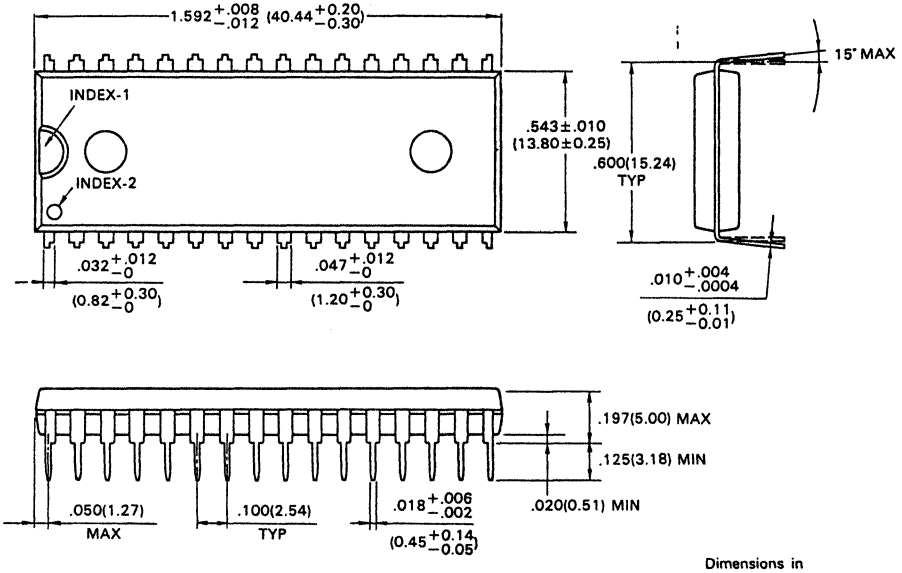
3

PACKAGE DIMENSIONS

(Suffix: P)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-32P-M01)

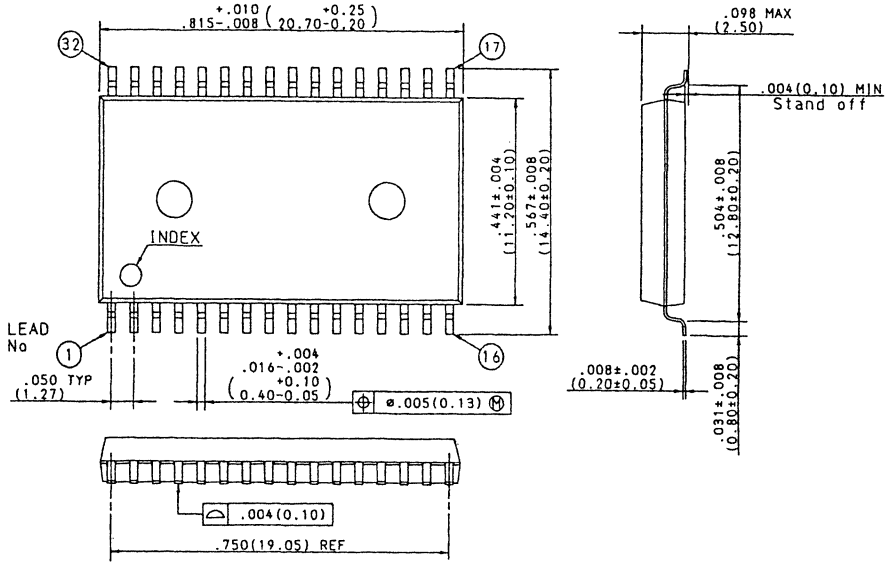


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M03)



Dimensions in inches
(millimeters)

3

Section 4

Application Specific SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
4–03	MB81C51–25	25	2048 bits	64-pin	Ceramic	PGA
	–30	30	512 x 4–way or 1024 x 2–way			
4–19	MB81C79B–35	35	73728 bits	28-pin	Plastic	DIP, FPT
	–45	45	(8192w x 9b)			
4–31	MB8279RT–20	20	73728 bits	32-pin	Plastic	DIP, FPT
	–25	25	(8192w x 9b)			
4–43	MB8287–25	25	262144 bits	32-pin	Plastic	DIP, FPT
	–35	35	(32768w x 8b)			
4–55	MB8421–90/L	90	16384-bits	48-pin	Plastic	DIP
	–12/L	120	(2048w x 8b)	52-pin	Plastic	DIP
	MB8422–90/L	90		64-pin	Plastic	FPT
	–12/L	120				
4–69	MB8431–90/L/LL	90	16384-bits	48-pin	Plastic	DIP
	–12/L/LL	120	(2048w x 8b)	52-pin	Plastic	DIP
	MB8432–90/L/LL	90		64-pin	Plastic	FPT
	–12/L/LL	120				

4

FUJITSU

CMOS TAG RANDOM ACCESS MEMORY

MB81C51-25
MB81C51-30

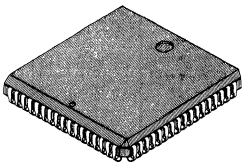
November 1988
Edition 1.0

CMOS TAG RANDOM ACCESS MEMORY

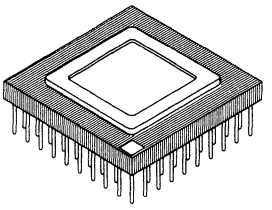
The Fujitsu MB81C51 is 512 entry x 4 way/1024 entry x 2 way TAG Random Access Memory (TAG RAM) fabricated with a CMOS technology.

MB81C51 has been developed aiming to be used in an easily handled cache system with the other DATA RAMs (ex. MB81C79A). Especially this device offers the advantages on designing compact and high performance cache system which will be used in a system adopting 32-bit CPU.

- Organization: 512 Entry x 4 Way or 1024 Entry x 2 Way
- Fast access time: 25/30 ns max from Address Inputs 18 ns max from Compare Data Inputs
- Power Consumption: 1100mW max.
- Single +5 V supply ±10% tolerance
- TTL compatible inputs and outputs
- LRU (Least Recently Used) Replacement Logic
- Purge Function (All-purge & Partial-purge)
- Internal Parity Generator/Checker
- 64 pin Pin-Grid-Array (Suffix: CR)
- 68 pin Plastic LCC (Suffix: PD)



LCC-68P-**M02**
(PLASTIC PACKAGE)



PGA-64C-A02
(PIN GRID ARRAY)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	-0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	-3.0 to +7.0	V
Output Voltage on any pin with respect to GND		V_{OUT}	-0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.5	W
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	-65 to +125	°C
	Plastic		-45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB81C51 BLOCK DIAGRAM 1

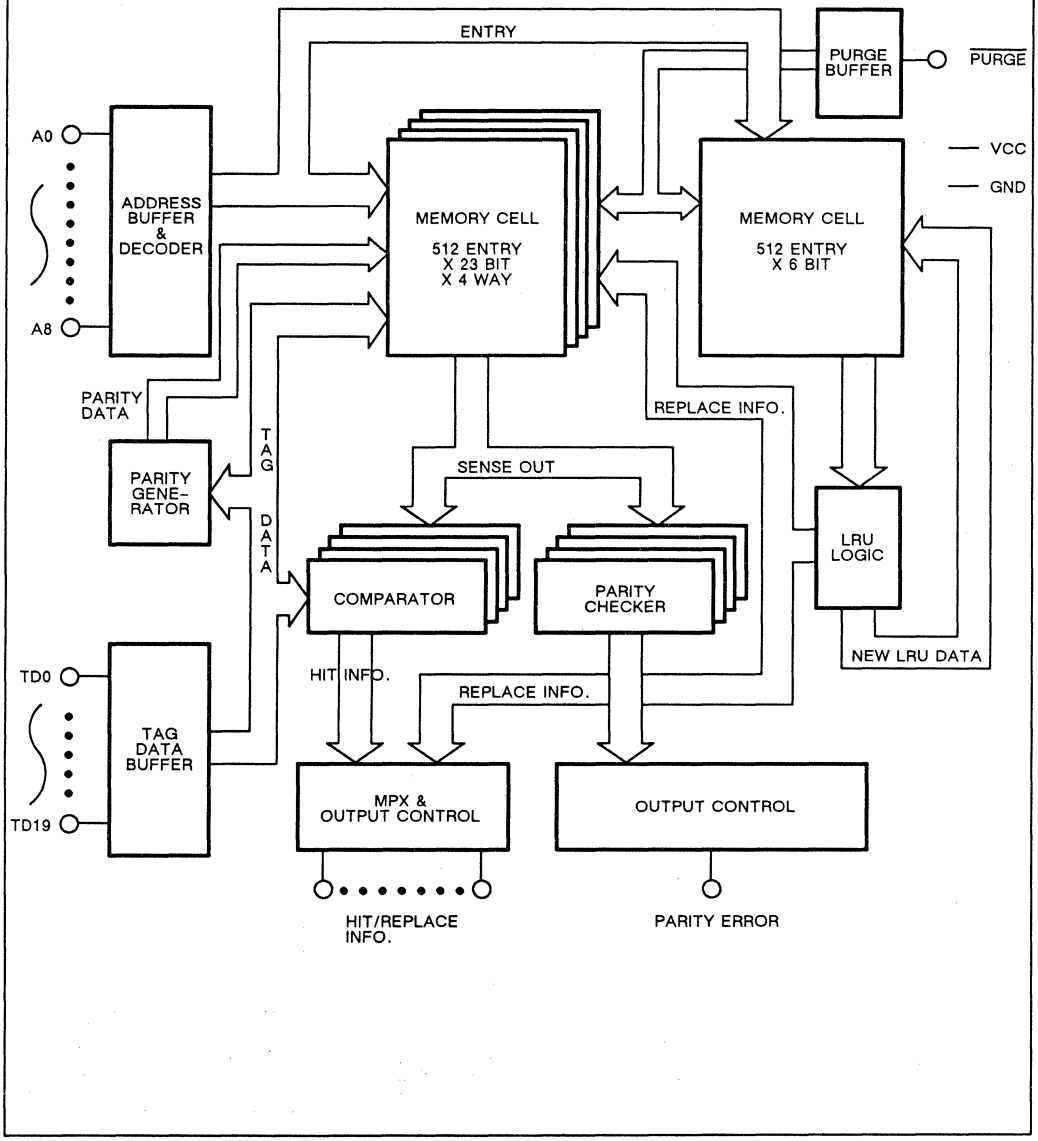
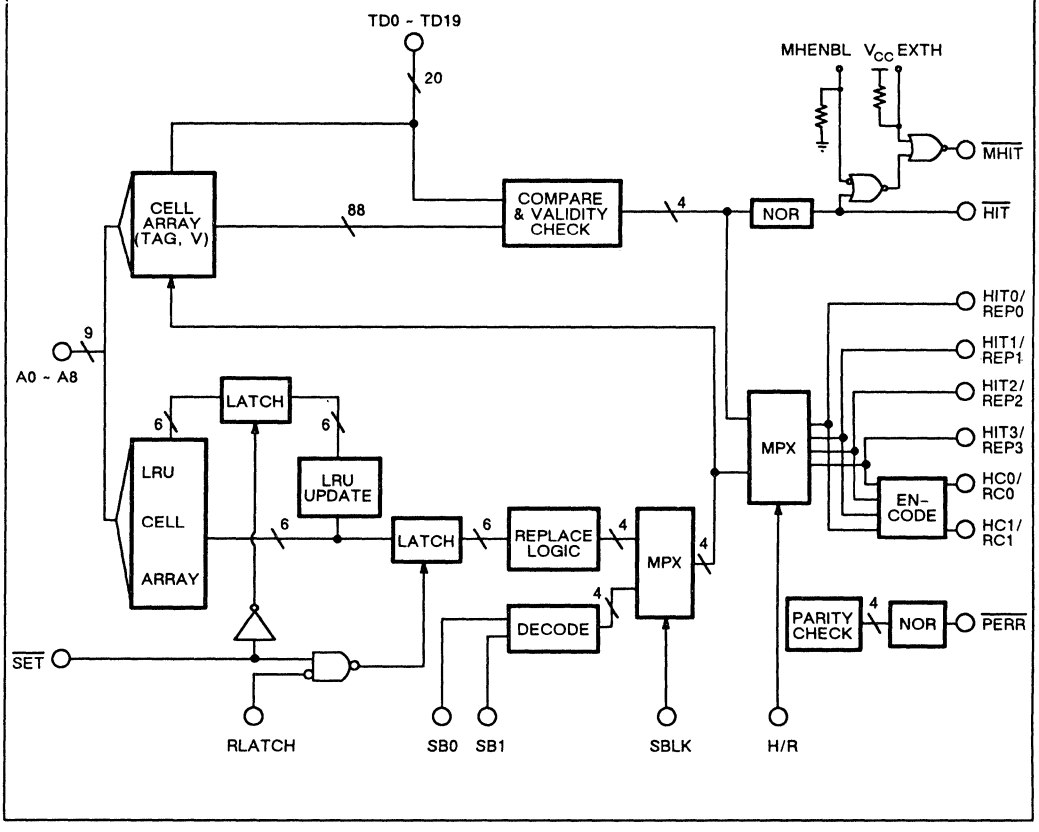


Fig. 2 — MB81C51 BLOCK DIAGRAM 2



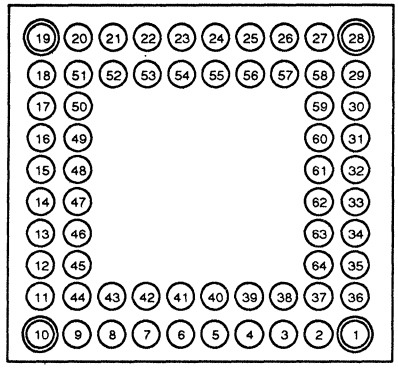
4

CAPACITANCE (T_A = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		10	pF

PIN ASSIGNMENT

64 PIN PIN GRID ARRAY(PGA-64C-A02)



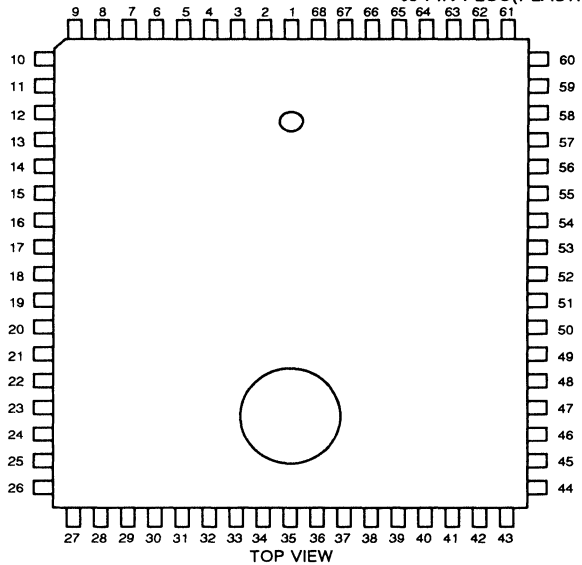
BOTTOM VIEW

4

PIN FUNCTION

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A4	45	TD6
2	$\overline{\text{MHIT}}$	24	A5	46	TD9
3	HIT0/REP0	25	A7	47	Vcc
4	HIT2/REP2	26	A9	48	TD13
5	HIT3/REP3	27	N.C.	49	TD15
6	TD0	28	N.C.	50	TD17
7	TD2	29	$\overline{\text{PINV}}$	51	TD19
8	EXTH	30	SBLK	52	A0
9	MHENBL	31	SB1	53	A2
10	N.C.	32	$\overline{\text{INH}}$	54	GND
11	TD7	33	$\overline{\text{INVL}}$	55	A6
12	TD8	34	$\overline{\text{SET}}$	56	A8
13	TD10	35	H/R	57	$\overline{\text{PURGE}}$
14	TD11	36	$\overline{\text{HIT}}$	58	MODE
15	TD12	37	HC0/RC0	59	$\overline{\text{VINV}}$
16	TD14	38	HC1/RC1	60	SB0
17	TD16	39	HIT1/REP1	61	Vcc
18	TD18	40	GND	62	$\overline{\text{WRITE}}$
19	N.C.	41	TD1	63	RLATCH
20	N.C.	42	TD3	64	$\overline{\text{PERR}}$
21	A1	43	TD4		
22	A3	44	TD5		

PIN ASSIGNMENT 68 PIN PLCC(PLASTIC LEAD CHIP CARRIER)



TOP VIEW

4

PIN FUNCTION (continued)

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	GND	24	TD17	47	$\overline{\text{PINV}}$
2	TD0	25	TD18	48	SBLK
3	TD1	26	TD19	49	SB0
4	TD2	27	N.C.	50	SB1
5	TD3	28	N.C.	51	$\overline{\text{INH}}$
6	EXTH	29	N.C.	52	Vcc
7	TD4	30	A0	53	$\overline{\text{INV}}$
8	N.C.	31	A1	54	$\overline{\text{WRITE}}$
9	N.C.	32	A2	55	$\overline{\text{SET}}$
10	MHENBL	33	A3	56	RLATCH
11	TD5	34	A4	57	H/R
12	TD6	35	GND	58	$\overline{\text{PERR}}$
13	TD7	36	A5	59	$\overline{\text{HIT}}$
14	TD8	37	A6	60	HC0/RC0
15	TD9	38	A7	61	N.C.
16	TD10	39	A8	62	N.C.
17	TD11	40	A9	63	HC1/RC1
18	Vcc	41	N.C.	64	$\overline{\text{MHIT}}$
19	TD12	42	N.C.	65	HIT0/REP0
20	TD13	43	N.C.	66	HIT1/REP1
21	TD14	44	$\overline{\text{PURGE}}$	67	HIT2/REP2
22	TD15	45	MODE	68	HIT3/REP3
23	TD16	46	$\overline{\text{VINV}}$		

PIN DESCRIPTION

OUTPUTS

$\overline{HIT}$	HIT OUTPUT. "NOR" OF HIT0 TO HIT3
HCn/RCn	CODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 1)
HITn/REPn	UNCODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 3)
$\overline{PERR}$	PARITY ERROR
$\overline{MHIT}$	HIT OUTPUT MODIFIED BY MHENBL AND EXTH

INPUTS

MODE	MODE SELECTION MODE = 1 : 512 Entry x 4 Way MODE = 0 : 1024 Entry x 2 Way
A0-A9	ADDRESS INPUTS (A9 is not used for 4 way)
TD0-19	TAG INFORMATION INPUTS
$\overline{PURGE}$	ALL-PURGE TIMING PULSE
$\overline{INVL}$	PARTIAL-PURGE. V-BIT FORCED TO "0". LRU IS REVERSIVELY UPDATED
SBLK	ENABLE WAY-SELECTION EXTERNALLY AT REPLACEMENT AND INVALIDATION
SB0, SB1	EXTERNAL WAY-ADDRESS INPUTS
$\overline{WRITE}$	WRITE CYCLE SIGNAL
$\overline{SET}$	TIMING PULSE Write : Registrate TAG, V-bit "H", LRU update Read : LRU updated PARTIAL PURGE : LRU reversively update, V-bit "L"
$\overline{INH}$	ALL FUNCTIONS EXCEPT PURGE ARE INHIBITED
H/R	OUTPUT SELECTION H/R = 1 : Hit Information H/R = 0 : Replace Information
RLATCH	LATCH CONTROL FOR REPLACE INFORMATION
$\overline{PINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
$\overline{VINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
MHENBL	ENABLE $\overline{MHIT}$ OUTPUT
EXTH	FORCE $\overline{MHIT}$ OUTPUT TO "L"

FUNCTION TABLE

1) BASIC FUNCTION (Any combination except below are inhibited.)

Input					TAG Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	TAG	P bit	V bit	LRU	Function Mode
L	H	X	X	X	N-CNG	N-CNG	N-CNG	N-CNG	INHIBIT[3]
H	H	H	X	X	N-CNG	N-CNG	N-CNG	N-CNG	TAG READ
H	H	⊓	H	H	N-CNG	N-CNG	N-CNG	N-CNG[1] or UP-D	TAG READ
H	H	⊓	L	H	TD0 to TD19	SET	H	UP-D	TAG WRITE
X	L	H	X	X	UNDEFINED	UNDEFINED	L (All)	INCLZ	ALL PURGE
H	H	⊓	H	L	N-CNG	N-CNG	N-CNG/L[2]	N-CNG[1] or RUP-D	PARTIAL PURGE

X : "H" or "L"
N-CNG : No Change INCLZ : INITIALIZE
UP-D : Up Dated RUP-D : Reversively Updated
1. When SBLK = "L" and no-HIT, then LRU is no change (N-CNG).
2. When SBLK = "L" and no-HIT, then V-Bit is no change (N-CNG).
3. During INHIBIT mode, HIT and PERR outputs are "H" but the other outputs are "L".

2) OUTPUT PIN FUNCTION

Input		Internal Info.[1, 2]				Output							
Mode	A9	hit0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	$\overline{\text{HIT}}$[3]	Mode
H	X	L	L	L	L	L	L	L	L	L	L	H	
H	X	H	L	L	L	H	L	L	L	L	L	L	4
H	X	L	H	L	L	L	H	L	L	H	L	L	W
H	X	L	L	H	L	L	L	H	L	L	H	L	A
H	X	L	L	L	H	L	L	L	H	H	H	L	Y
L	L	L	X	L	X	L	L	L	L	L	L	H	
L	L	H	X	L	X	H	L	L	L	L	L	L	2
L	L	L	X	H	X	L	L	H	L	L	H	L	W
L	H	X	L	X	L	L	L	L	L	L	L	H	A
L	H	X	H	X	L	L	H	L	L	H	L	L	Y
L	H	X	L	X	H	L	L	L	H	H	H	L	

X: "H" or "L"

1. Internal information, rep0 to rep3 are determined by on-chip LRU logic when SBLK = "L". When SBLK = "H", the internal information are determined by external signal of SB0 & SB1.
2. Correct operation is not guaranteed if 2 ways or more become HIT at the same time.
3. Output of $\overline{\text{HIT}}$ is valid when H/R = "H".

3) PARTIAL PURGE ($\overline{\text{INVL}}$ = "L")

INPUT					INTERNAL INFO.				PURGE BLOCK				$\overline{\text{SET}}$	
					HIT				BLOCK					
MODE	A9	SBLK	SB0	SB1	0	1	2	3	0	1	2	3	LRU	MODE
H	X	L	X	X	L	L	L	L	—	—	—	—	---	
H	X	L	X	X	H	L	L	L	Q	—	—	—	RUP-D	4
H	X	L	X	X	L	H	L	L	—	Q	—	—	RUP-D	
H	X	L	X	X	L	L	H	L	—	—	Q	—	RUP-D	W
H	X	L	X	X	L	L	L	H	—	—	—	Q	RUP-D	A
H	X	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	Y
H	X	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
H	X	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	
H	X	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	
L	L	L	X	X	L	X	L	X	—	—	—	—	---	
L	L	L	X	X	H	X	L	X	Q	—	—	—	RUP-D	
L	L	L	X	X	L	X	H	X	—	—	Q	—	RUP-D	2
L	L	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	
L	L	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	W
L	H	L	X	X	X	L	X	L	—	—	—	—	---	A
L	H	L	X	X	X	H	X	L	—	Q	—	—	RUP-D	Y
L	H	L	X	X	X	L	X	H	—	—	—	Q	RUP-D	
L	H	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
L	H	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	

Note: Correct operation is not guaranteed if 2 ways or more become HIT at the same time.

4

4) PARITY ERROR & V-BIT[1] (n : 0 to 3)

pen	vn0	vn1	PEn	HIT Info.[2]
L	L	L	L	---
L	L	H	H	HIT
L	H	L	H	HIT
L	H	H	L	HIT
H	L	L	L	---
H	L	H	H	HIT
H	H	L	H	HIT
H	H	H	H	HIT

1. $\overline{PERR}$ is "NOR" of PE0 to PE3
2. Output information when internal "HIT" is valid.

pen : Internal parity error of way "n"
vn0/vn1 : Duplicate validity bits.
PEn : Determined by the following equation.

$$PEn = (vn0 + vn1) \cdot pen + (vn0 \oplus vn1)$$

4

BASIC FUNCTIONS

TAG READ

A comparison between the TAG input data (TD0-19) and the contents of the addressed location is performed. If both data are the same, that is "FOUND". Then $\overline{HIT}$ will be "LOW" and outputs of HCn, HITn indicate hitted "Associative way". In the case of "NOT-FOUND", the TAG RAM will specify the "way", which should be replaced, by using the LRU logic automatically.

The replacement information will be presented at the outputs of RCn and REPn by forcing the H/R input into "LOW". These signals will be latched and used for the data Memory move-in operation.

TAG WRITE

When "NOT-FOUND" is occurred, the TAG-RAM also should be updated. The write operation is performed by $\overline{WRITE}$ "LOW" and $\overline{SET}$ pulse input. The TAG data will be written into the proper "way" by the internal LRU logic.

TAG-WRITE mode, V-bit (Validity bit) and the parity are set, and LRU logic is updated.

On the other hand, it will be able to specify the "way" externally by using SBLK, SB0 and SB1 inputs.

ALL PURGE

By asserting $\overline{PURGE}$ input "LOW", the V-bit are reset and LRU logic is initialized.

In this operation, the contents of each TAG and its parity will not be identified.

PARTIAL PURGE

The partial purge operation is performed by $\overline{INVL}$ "LOW" and $\overline{SET}$ pulse input.

The V-bit, which is specified by the address inputs, will be reset, and LRU logic will be reversively updated.

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note:

*-3.0V min. for pulse width less than 20ns.

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10	10	µA
Operating Supply Current	D_{OUT} = Open, Cycle = min.	I_{CC}		200	mA
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = -4mA	V_{OH}	2.4		V

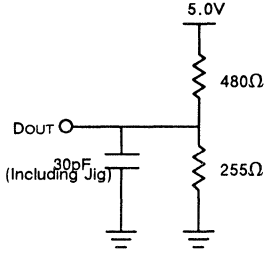
Fig. 3 — AC TEST CONDITION

INPUT PULSE LEVELS : 0.0V to 3.0V

INPUT PULSE RISE AND FALL TIMES : 5ns (Transient time between 0.8V and 2.2V)

TIMING REFERENCE LEVELS : Input : 1.5V
Output : 1.5V

OUTPUT LOAD:



4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H", or "L", $\overline{\text{VINV}}$ = "H" or "L", $\overline{\text{INH}}$ = "H")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	50		50		ns
Address Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{AH}		25		30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}		27		32	ns
TAG Data Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{TH}		18		18	ns
TAG Data Valid to $\overline{\text{MHIT}}$	t_{TMH}		20		20	ns
$\overline{\text{HIT}}$, HCn, HITn Hold Time	t_{HH}	0		0		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
RCn, REPn Hold Time for RLATCH	t_{RH}	0		0		ns
SBLK, SB0, SB1 Setup Time for RCn, REPn	t_{SBR}		25		25	ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns
RCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0		0		ns
H/R to Multiplex output change	t_{HR}		10		12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ output	t_{MMH}		10		12	ns

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", H/R = "L", $\overline{\text{INH}}$ = "H")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	50		50		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Setup Time for PCn, REPn	t_{SBR}		25		25	ns
PCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK Hold Time	t_{SBH}	5		5		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Setup Time for $\overline{\text{SET}}$	t_{IS}	25		25		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Recovery Time for $\overline{\text{SET}}$	t_{IR}	5		5		ns

PERTIAL PURGE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$= "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Pertial Purge Cycle	t_{PPC}	50		50		ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns

ALL PURGE ($\overline{\text{SET}}$ = "H", Other control inputs are "H" or "L")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
All Purge Cycle Time	t_{APC}	100		100		ns
Purge Pulse Width	t_{PPW}	50		50		ns
Purge Recovery Time	t_{PR}	50		50		ns

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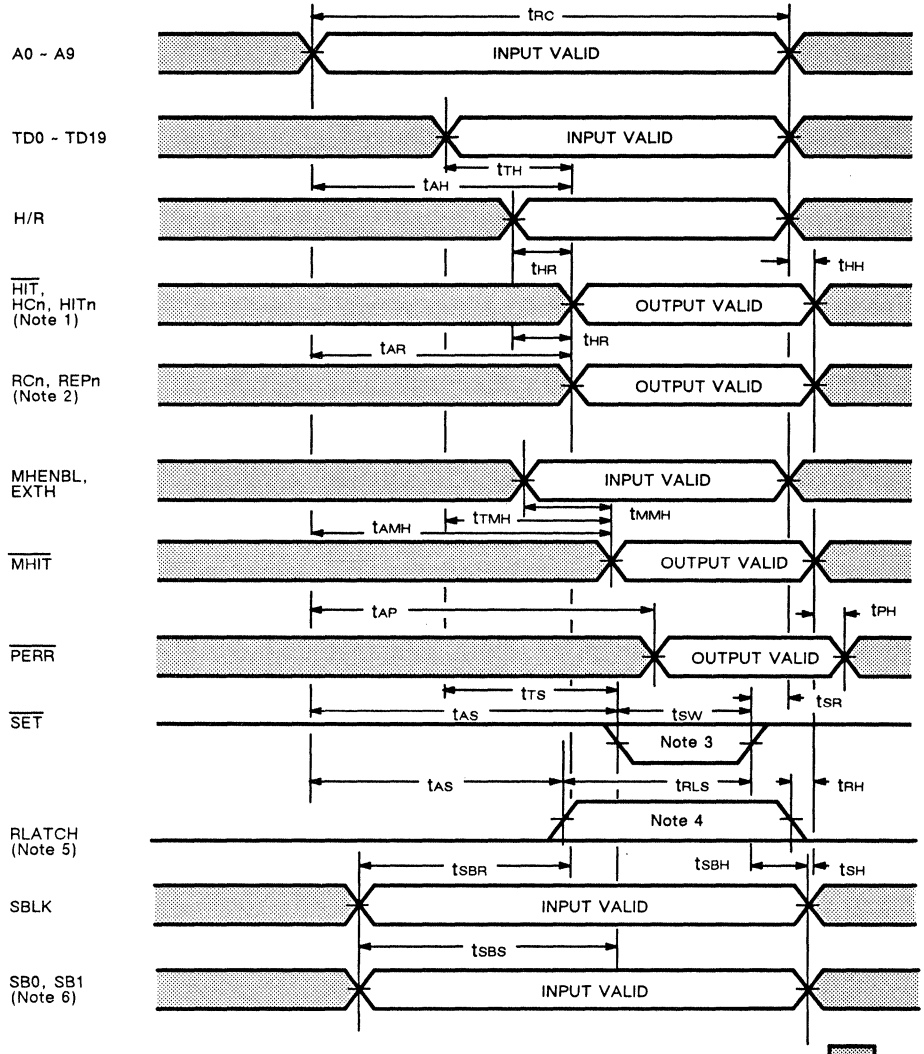
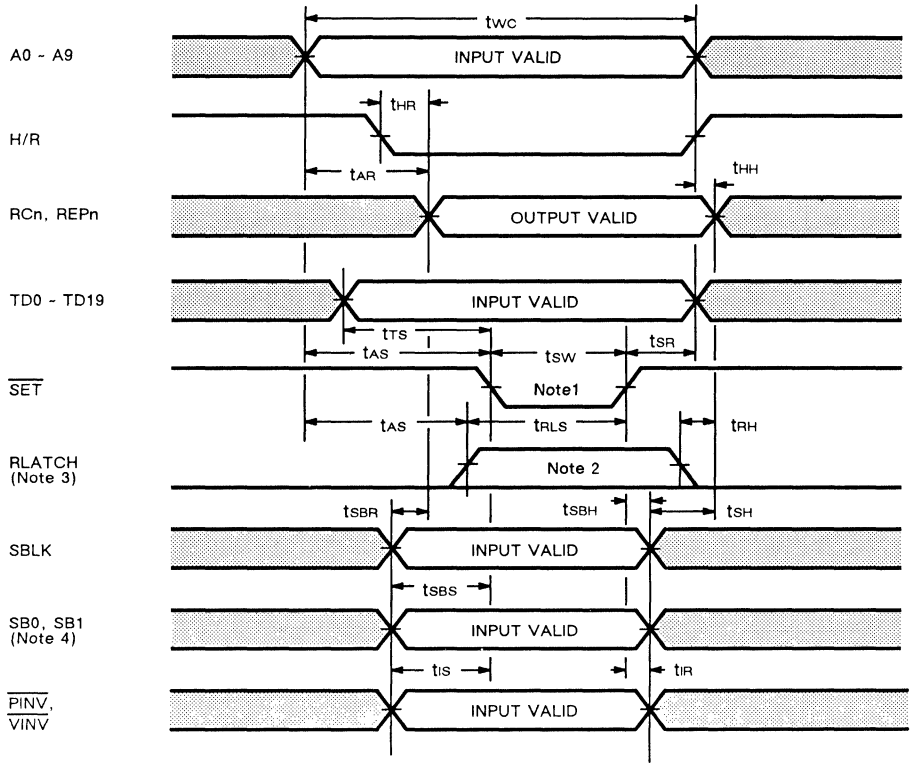
TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L", INH = "H")



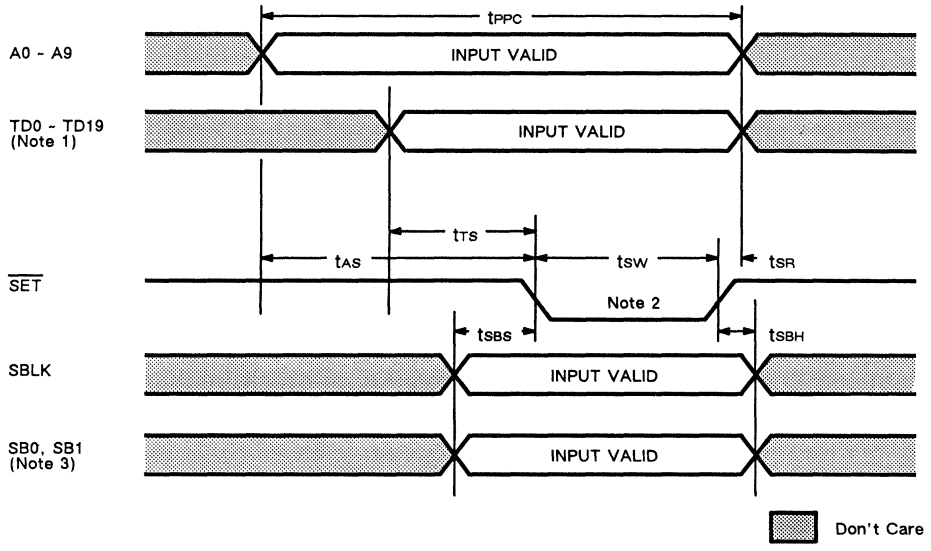
Notes 1: Valid at H/R = "H".
2: Valid at H/R = "L".
3: LRU is updated at $\overline{\text{SET}}$ = "L".
4: Replace latched at RLATCH = "H".
5: Valid at SBLK = "L".
6: Valid at SBLK = "H".

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{PURGE}$ = "H", $\overline{WRITE}$ = "L", $\overline{INVL}$ = "H", $\overline{INH}$ = "H")



Notes 1. Registrate TAG, V-bit "H", LRU update.
2. Replace latched at $\overline{RLATCH}$ = "H".
3. Valid at SBLK = "L".
4. Valid at SBLK = "H".

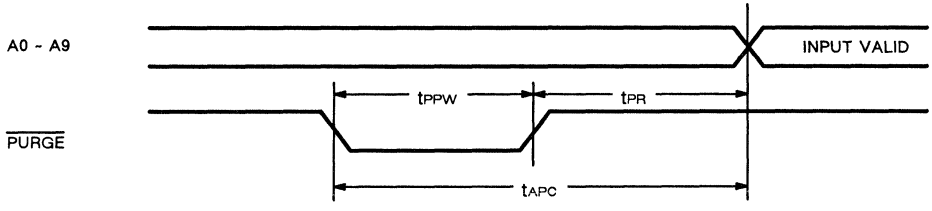
PARTIAL PURGE CYCLE (MODE = "H" or "L", $\overline{PURGE}$ = "H", $\overline{WRITE}$ = "H", $\overline{INVL}$ = "L", H/R = "H" or "L", $\overline{INH}$ = "H", RLATCH = "L", $\overline{PINV}$ = "H" or "L", $\overline{VINV}$ = "H" or "L")



Notes:

1. Valid at SBLK = "L".
2. LRU is reversively updated, V-bit "L".
3. Valid at SBLK = "H".

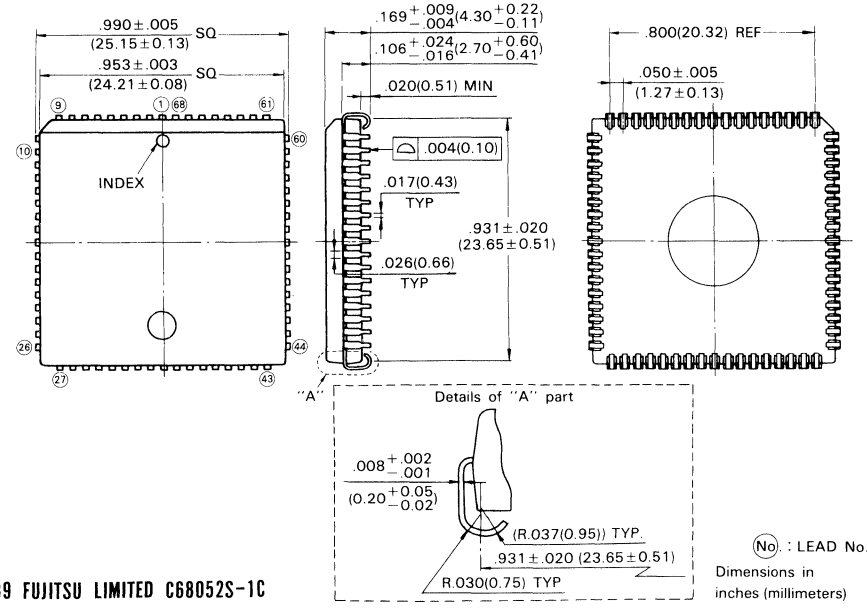
All purge ($\overline{SET}$ = "H", OTHER CONTROL INPUTS ARE "H" or "L")



PACKAGE DIMENSIONS

68-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-68P-M02)



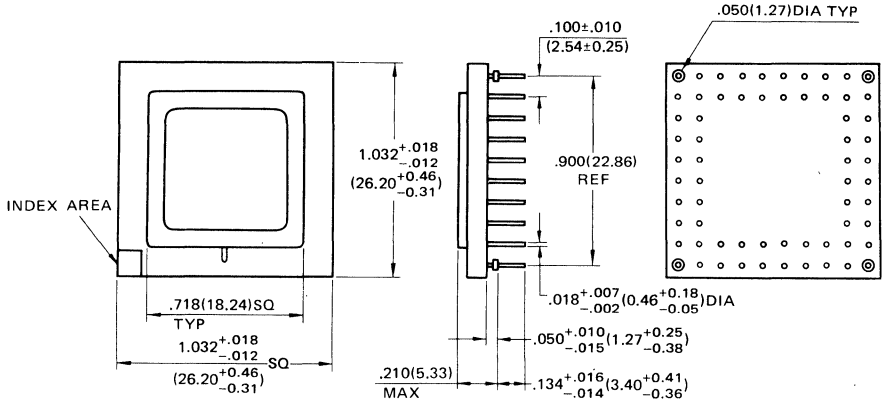
(No). : LEAD No.

Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS (continued)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-64C-A02)



Dimensions in
inches (millimeters)

4

October 1989
Edition 1.0

FUJITSU

DATA SHEET

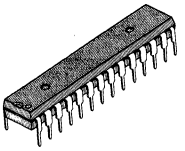
MB81C79B-35/-45
CMOS 72K-BIT HIGH SPEED SRAM

8192-WORDS x 9-BIT HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

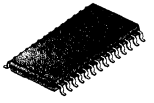
The Fujitsu MB81C79B is 8192words x 9bits static random access memory fabricated with a CMOS process. Because of 9 bit organization, this device is convenient to be used for parity check function and also this device has two fast column addresses, therefore MB81C79B is very suitable to used as cache buffers. To make power dissipation lower, peripheral circuits consist of CMOS technology,and to obtain smaller chip size, cells consisit of NMOS transistors and resistors. All pins are TTL compatible and a single 5 volts power supply is required.

All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 8192words x 9bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA}=t_{ACS1}$=35ns max, t_{OE}=10ns max.
  A11, A12 access time=12ns max. (MB81C79B-35)
  $t_{AA}=t_{ACS1}$=45ns max, t_{OE}=15ns max.
  A11, A12 access time=15ns max. (MB81C79B-45)
- Low power consumption: 550mW (Operation)
  138mW (TTL Standby)
  83mW (CMOS Standby)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state inputs and outputs
- Chip selects for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin 300mil Plastic DIP package (Suffix: -P-SK)
- Standard 28-pin 450mil Gull wing flat package (Suffix: -PF)



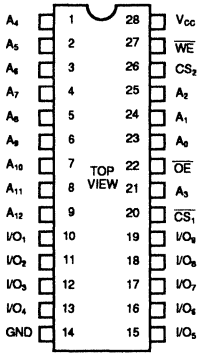
PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02

4

PIN ASSIGNMENT



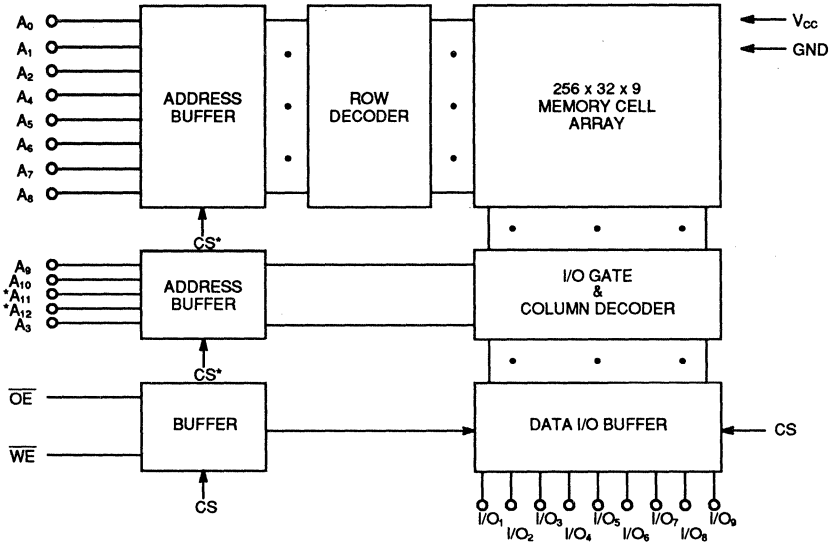
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	-3.5 to +7	V
Output Voltage on any I/O with respect to GND	V_{OUT}	-0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storag Temperature	T_{STG}	-40 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB81C79B BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH–Z
L	L	X	X	DESELECT	I_{CC}	HIGH–Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH–Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

* Fast address

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN}=0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	−10	10	μA	V_{IN}=0V to V_{CC}
Output Leakage Current	I_{LO}	−10	10	μA	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC}		130	mA	$\overline{CS_1}$=V_{IL} I/O=Open, Cycle=Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC}=Min to Max. $\overline{CS_1}$=V_{CC}−0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}−0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$=V_{IH}
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC}=0V to V_{CC} Min. $\overline{CS_1}$=Lower of V_{CC} or V_{IH} Min.

4

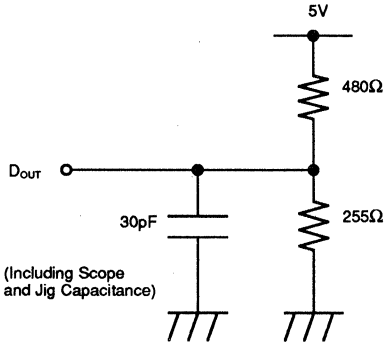
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 1.5V

Fig. 2

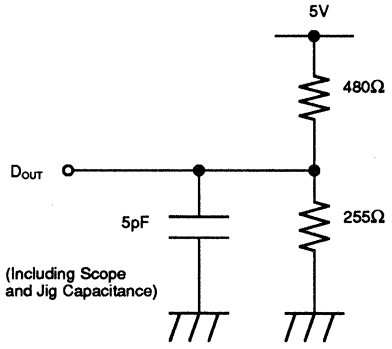
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

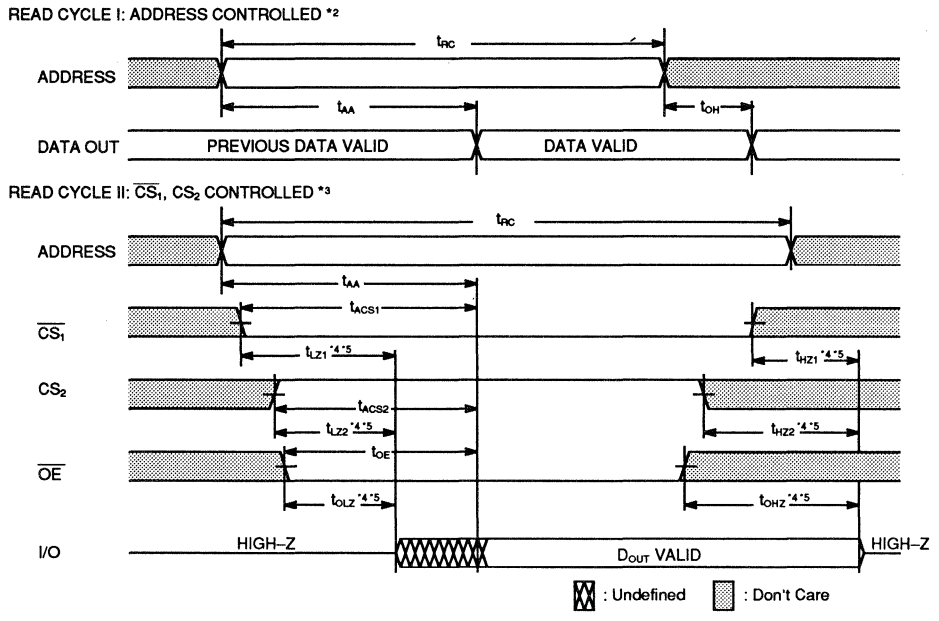
READ CYCLE*1

Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time *2	t_{AA}		35#1		45#2	ns
$\overline{CS_1}$ Access Time *3	t_{ACS1}		35		45	ns
CS_2 Access Time *3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		10		15	ns
Output Active from $\overline{CS_1}$ *4*5	t_{LZ1}	5		5		ns
Output Active from CS_2 *4*5	t_{LZ2}	2		2		ns
Output Active from $\overline{OE}$ *4*5	t_{OLZ}	2		2		ns
Output Disable from $\overline{CS_1}$ *4*5	t_{HZ1}		20		25	ns
Output Disable from CS_2 *4*5	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$ *4*5	t_{OHZ}		20		25	ns

Note : *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
#1 A11, A12 address access time is 12ns max.
#2 A11, A12 address access time is 15ns max.

4

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1

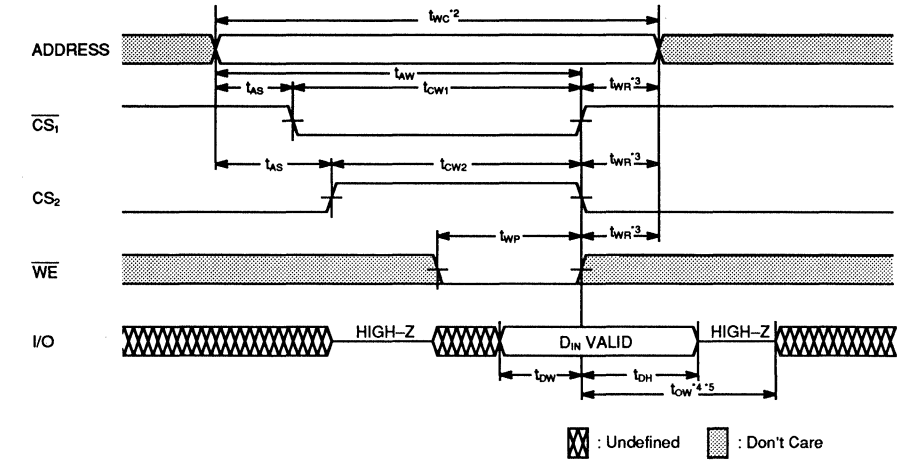
Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time *3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$ *4*5	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$ *4*5	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

4

WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

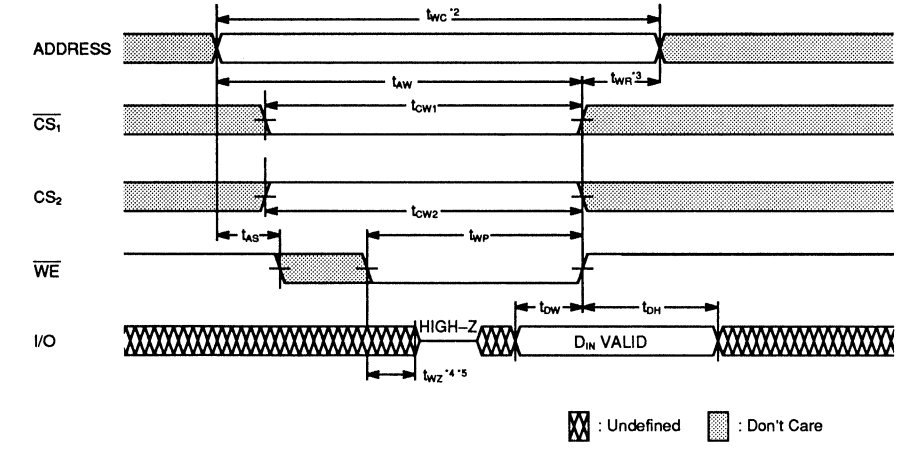
*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

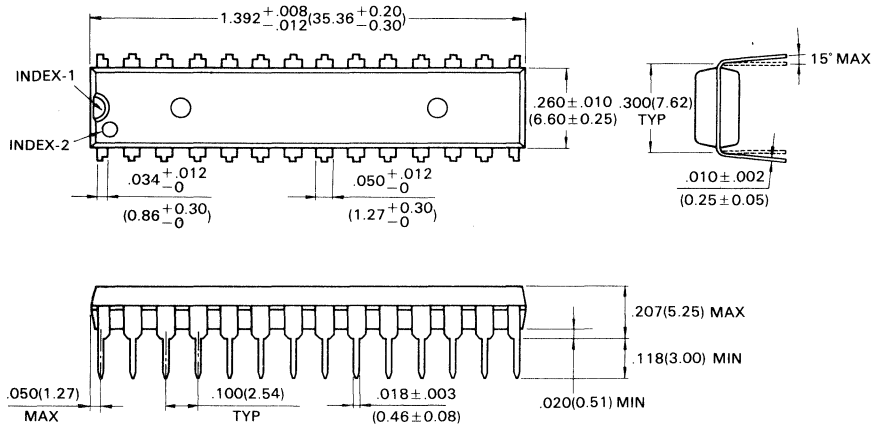
*5 This parameter is specified with Load II in Fig. 2.

4

PACKAGE DIMENSIONS

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)

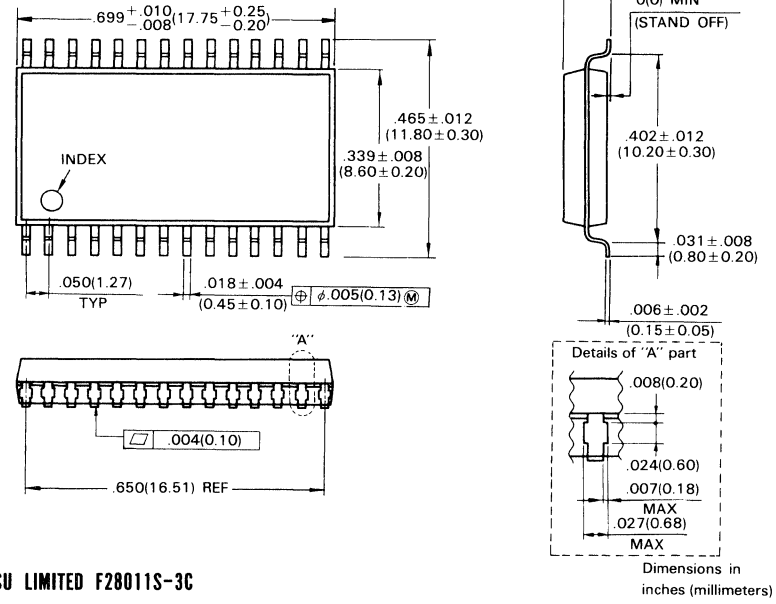


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M02)



Dimensions in
inches (millimeters)

4

4

FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB8279RT-20 MB8279RT-25

March 1989
Edition 2.0

72K-BIT (8192 x 9) SYNCHRONOUS CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

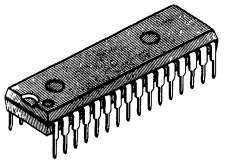
The Fujitsu MB8279RT is a 8,192-words by 9-bits synchronous static random access memory fabricated with a CMOS silicon gate process.

Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK pin therefore external control of write pulse width is not necessary. Compared to the traditional RAM, MB8279RT drastically improves the system level cycle time because signal skews are not necessarily concerned.

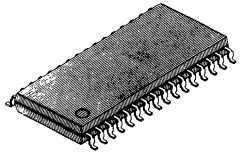
The MB8279RT has a 32-pin plastic skinny DIP package and 32-pin plastic flat package as package options.

All pins are TTL compatible, and a single +5V power supply is required.

- 8,192 words x 9 bits organization
- Fast access time:
  t_{ACL} = 20ns max. /
  t_{ACS2} = t_{PE2} = 10ns max. (MB8279RT-20)
  t_{ACL} = 25ns max. /
  t_{ACS2} = t_{PE2} = 12ns max. (MB8279RT-25)
- Registered addresses, $\overline{CS_1}$, $\overline{WE}$ and Data inputs
- Write cancel function by asynchronous CS_2 pin
- On-chip write pulse generator
- On-chip parity checker
- CMOS peripheral
- Single = 5V (±10%) power supply with low current drain
  Active operation = 120mA max.
  Standby operation = 30mA max.
- Common data inputs/outputs
- TTL compatible inputs/outputs
- Three-state data output and open drain parity error output
- Standard 32-pin plastic DIP package: (Suffix P-SK)
  Standard 32-pin plastic flat package (Suffix PF)



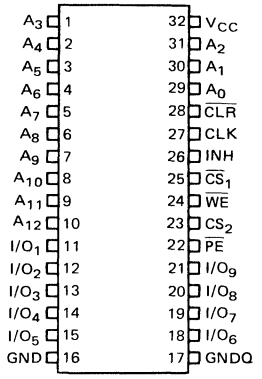
PLASTIC PACKAGE
DIP-32P-M02



PLASTIC PACKAGE
FPT-32P-M02

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

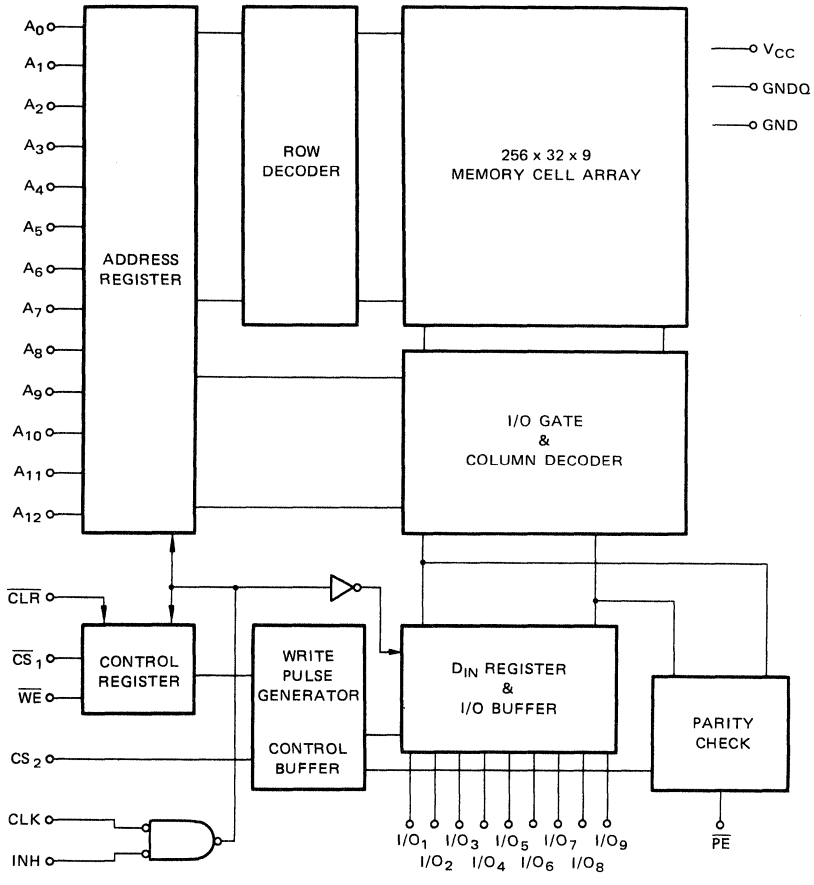
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Output Voltage	$V_{I/O}$	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB8279RT BLOCK DIAGRAM



CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CLK	Clock	Input	Address, $\overline{CS_1}$ and $\overline{WE}$ are fetched at the rising edge of the CLK, and D_{IN} is fetched at falling edge of the CLK.
INH	Inhibit	Input	While INH = "H", a low level of CLK is disabled.
$\overline{CLR}$	Clear	Input	When $\overline{CLR}$ = "L", the contents of $\overline{CS_1}$ and $\overline{WE}$ register are cleared to standby.
A_0 to A_{12}	Address Input	Input	Synchronous address inputs.
$\overline{CS_1}$	Chip Select 1	Input	Synchronous Chip Select 1 ($\overline{CS_1}$) input. (This pin can be used as power down.)
CS_2	Chip Select 2	Input	Asynchronous high-speed Chip Select 2 (CS_2) input. (This pin can be used as write cancel.)
$\overline{WE}$	Write Enable	Input	Synchronous Write Enable ($\overline{WE}$) input.
I/O_1 to I/O_9	Data Input/Output	Input/ Output	Data inputs/outputs. (Synchronous data inputs/Asynchronous data outputs)
$\overline{PE}$	Parity Error	Output	Asynchronous parity error output: $\overline{PE}$ output remains High-Impedance state through undefined area.
V_{CC}	Power Supply	–	+5V ±10% power supply.
GNDQ	Ground for Output	–	Ground for output circuits.
GND	Ground for Others	–	Ground for other circuits.

TRUTH TABLE

$\overline{CLR}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	MODE	I/O PIN	$\overline{PE}$ OUTPUT PIN	SUPPLY CURRENT
L	X	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	H	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	L	L	X	CHIP DISABLE	HIGH-Z	HIGH-Z	ACTIVE
H	L	H	H	READ	D_{OUT}	$\overline{PE}$ OUTPUT	ACTIVE
H	L	H	L	WRITE	D_{IN}	HIGH-Z	ACTIVE

Legend: H = High level, L = Low level, X = Don't care.
Notes: $\overline{CS_1}$ and $\overline{WE}$ are input at the rising edge of the CLK.
$\overline{PE}$ output remains High-Impedance state through undefined area.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

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DC CHARACTERISTICS

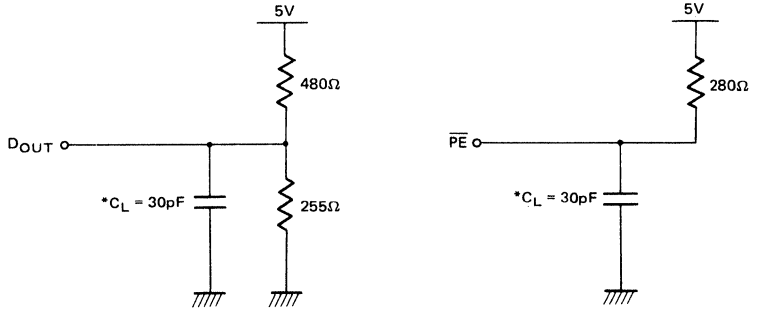
(Recommended operating conditions otherwise noted.)

Parameter		Test Conditions	Symbol	Min	Max	Unit
Standby Supply Current		$\overline{CS_1} = V_{IH}$	I_{SB}		30	mA
Operating Supply Current		$\overline{CS_1} = V_{IL}$, I/O = Open Cycle = min.	I_{CC}		120	mA
Input Leakage Current		V_{IN} = GND to V_{CC}	I_{LI}	-10	10	μA
Output Leakage Current		$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ V_{OUT} = GND to V_{CC}	$I_{LI/O}$	-10	10	μA
Input Low Voltage			V_{IL}	-2.0*1	0.8	V
Input High Voltage			V_{IH}	2.2	6.0	V
Output High Voltage		I_{OH} = -4mA	V_{OH}	2.4		V
Output Low Voltage	D_{OUT}	I_{OL} = 8mA	V_{OL}		0.4	V
	$\overline{PE}$	I_{OL} = 16mA				
Peak Power-on Current*2		V_{CC} = GND to 4.5V $\overline{CLR}$ = GND	I_{PO}		90	mA

Note: *1 -2.0V Min. for pulse width less than 20ns. (V_{IL} = -0.3V at DC level)
*2 The $\overline{CLR}$ input should be connected to GND to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- INPUT PULSE LEVELS: 0.6V TO 2.4V
- TIMING REFERENCE LEVELS: INPUT: V_{IL} = 0.8V, V_{IH} = 2.2V
  OUTPUT: V_{OL} = 0.8V, V_{OH} = 2.2V
- OUTPUT LOAD



*INCLUDING JIG AND STRAY CAPACITANCE.

(C_L = 5pF for t_{LZ}, t_{HZ}, t_{LZ2}, t_{HZ2} and t_{CRHZ})

(C_L = 5pF for t_{PLZ}, t_{PHZ}, t_{PLZ2}, t_{PHZ2} and t_{CRHZ})

AC CHARACTERISTICS

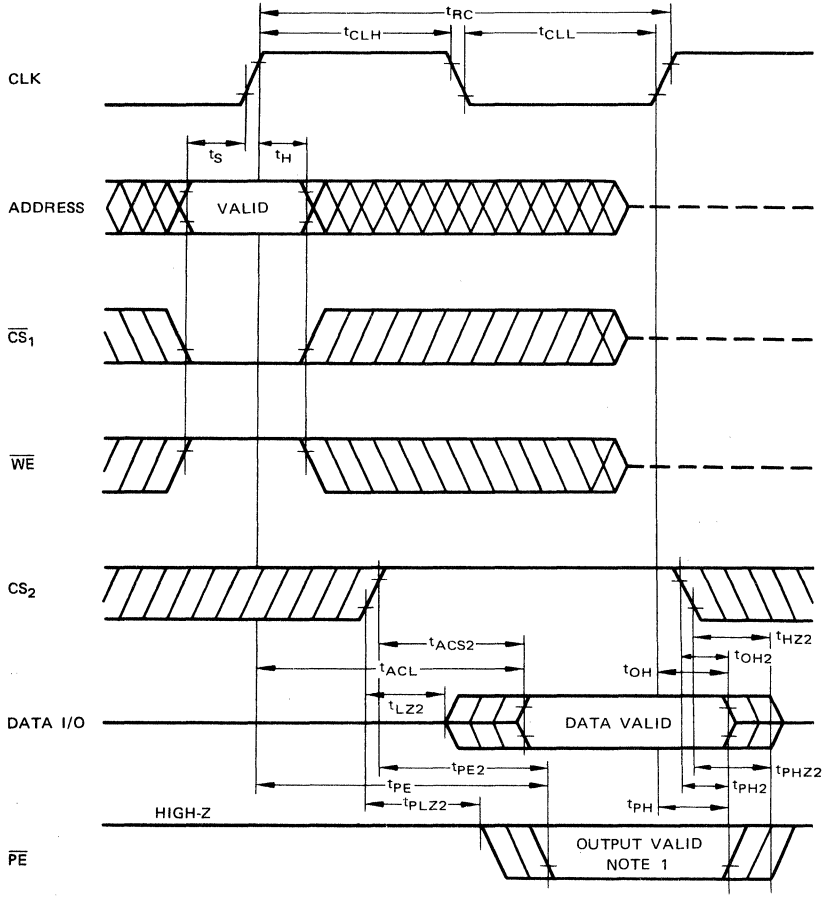
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Read Cycle Time	When no uses $\overline{PE}$	t_{RC}	20		25		ns
	When uses $\overline{PE}$	t_{RC}	25		30		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
Clock Access Time	D_{OUT}	t_{ACL}		20		25	ns
	$\overline{PE}$	t_{PE}		25		30	ns
CS_2 Access Time	D_{OUT}	t_{ACS2}		10		12	ns
	$\overline{PE}$	t_{PE2}		10		12	ns
CS_2 to Output Low-Z	D_{OUT}	t_{LZ2}	2		2		ns
	$\overline{PE}$	t_{PLZ2}	2		2		ns
CS_2 to Output High-Z	D_{OUT}	t_{HZ2}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ2}	2	8	2	10	ns
Output Hold from Clock	D_{OUT}	t_{OH}	2		2		ns
	$\overline{PE}$	t_{PH}	2		2		ns
Output Hold from CS_2	D_{OUT}	t_{OH2}	2		2		ns
	$\overline{PE}$	t_{PH2}	2		2		ns

4

READ CYCLE TIMING DIAGRAM



Note 1: $\overline{PE}$ output remains High-Impedance state through undefined area.

WRITE CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	20		25		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
CS_2 Setup Time		t_{CS}	2		2		ns
CS_2 Hold Time		t_{CH}	8		10		ns
Data Setup Time		t_{DS}	0		0		ns
Data Hold Time		t_{DH}	6		6		ns
CLK to Output High-Z	D_{OUT}	t_{HZ}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ}	2	8	2	10	ns
CLK to Output Low-Z	D_{OUT}	t_{LZ}	2		2		ns
	$\overline{PE}$	t_{PLZ}	2		2		ns

CLOCK INHIBIT TIMING

Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clock Inhibit Setup Time	t_{CLIS}	2		2		ns
Clock Inhibit Hold Time	t_{CLIH}	2		2		ns
Clock Enable Setup Time	t_{CLES}	2		2		ns
Clock Enable Hold Time	t_{CLEH}	0		0		ns

REGISTOR CLEAR TIMING

Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clear Pulse Width	t_{CRW}	7		7		ns
Clear Hold Time	t_{CRH}	10		10		ns
Clear Recovery Time	t_{CRR}	10		10		ns
Clear to Output High-Z	t_{CRHZ}	2	8	2	10	ns

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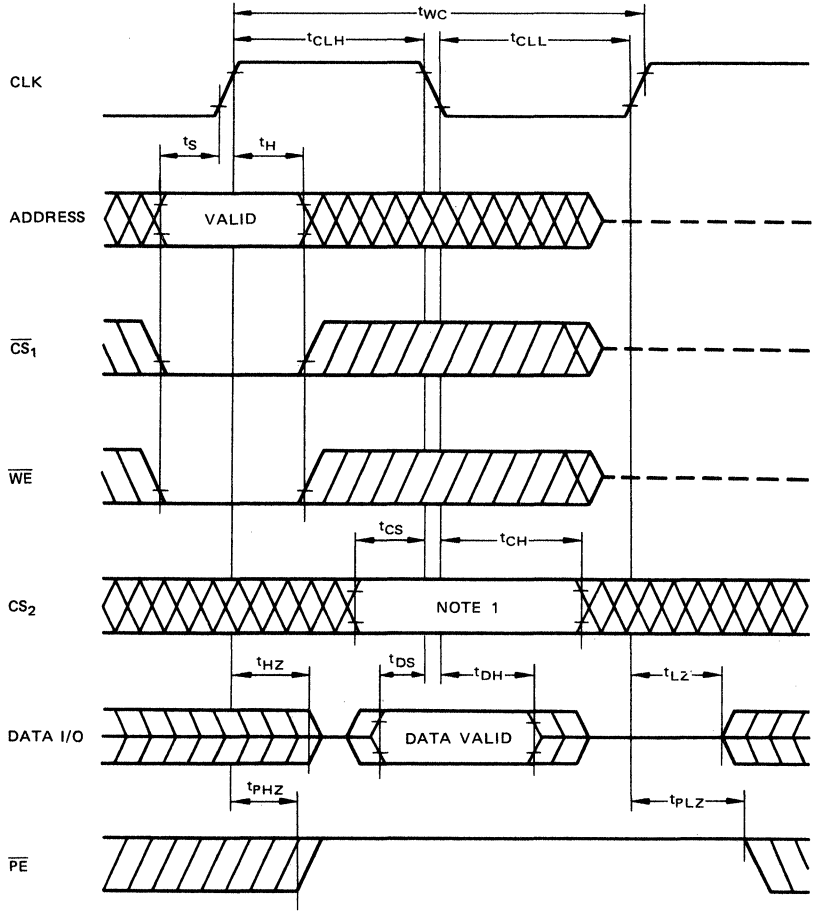
WRITE CYCLE TIMING DIAGRAM

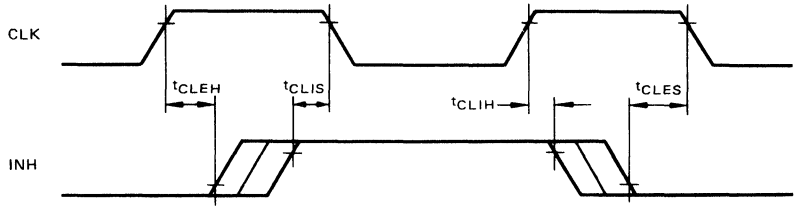
WRITE CYCLE (INH = L, $\overline{CLR}$ = H)



Note 1: When CS_2 = H level, write operation is excuted and when CS_2 = L level, write operation is cancelled.

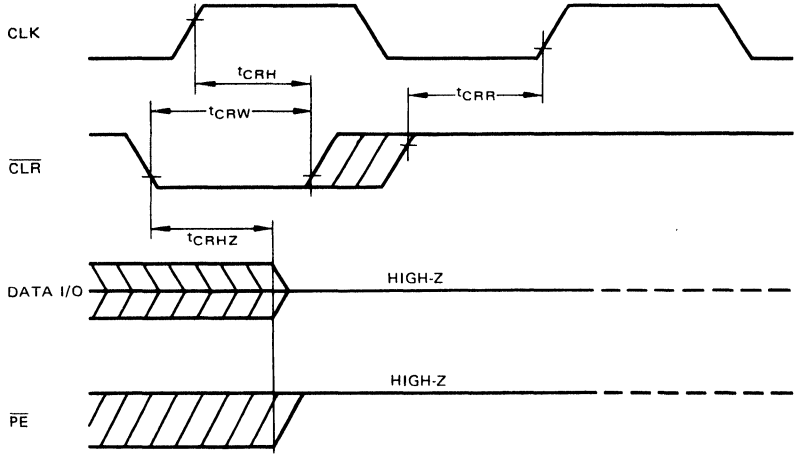
CLOCK INHIBIT TIMING DIAGRAM

CLOCK INHIBIT



REGISTER CLEAR TIMING

REGISTER CLEAR



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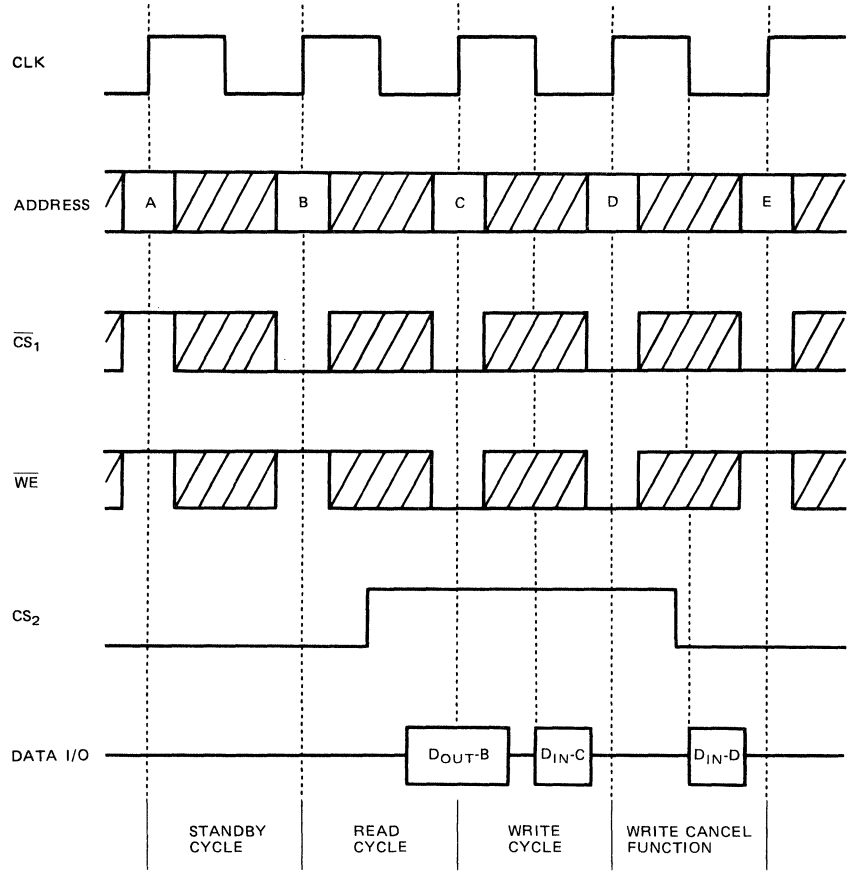
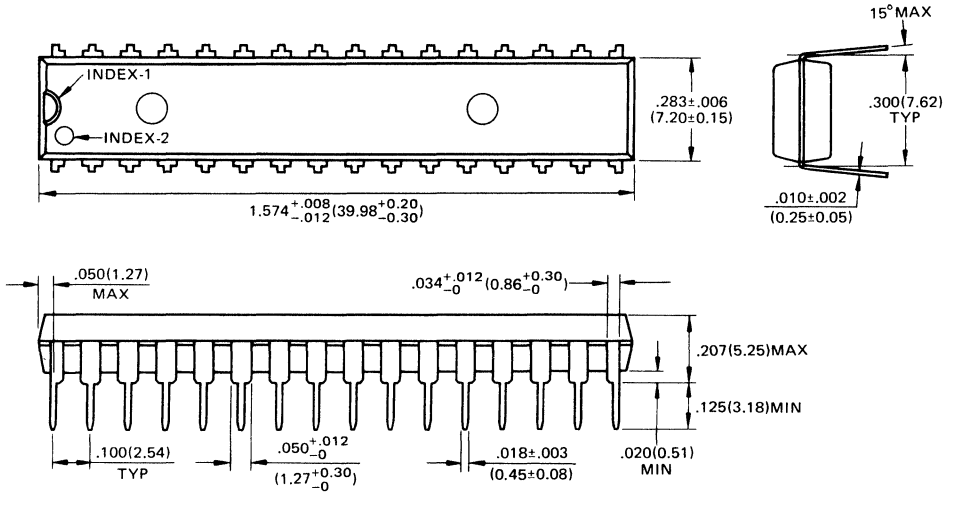
EXAMPLE OF MB8279RT BASIC FUNCTION



PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)

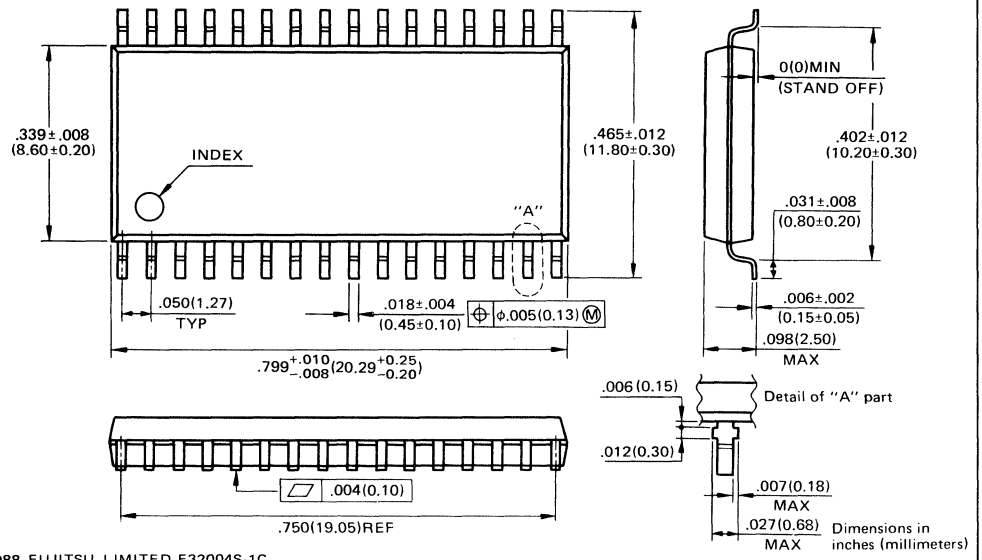


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (continued)

32-LEAD PLASTIC SMALL OUTLINE PACKAGE
(CASE No.: FPT-32P-M02)



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FUJITSU

CMOS 262144-BIT STATIC RANDOM ACCESS MEMORY

MB8287-25
MB8287-35

March 1989
Edition 2.0

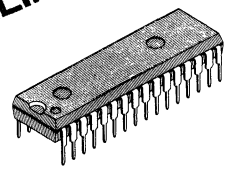
32K x 8-BIT STATIC RANDOM ACCESS MEMORY WITH PARITY GENERATOR AND CHECKER

PRELIMINARY

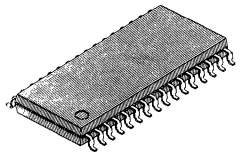
The Fujitsu MB8287 is 32768 words x 8 bits high speed static random access memory with parity generator and checker, fabricated with CMOS technology. To obtain smaller chip, cell consists of NMOS transistors and resistors therefore this device is assembled in 300 mil DIP and has such small power dissipation as 605mW max.
All pins are TTL compatible and single 5 volt power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$ the other deselected packages automatically power down.
All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 32768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Fast access time:
  $t_{AA} = t_{ACS1}$ = 25ns max,
  t_{ACS2} = 14ns max (MB8287-25)
  $t_{AA} = t_{ACS1}$ = 35ns max,
  t_{ACS2} = 15ns max (MB8287-35)
- Low power consumption:
  715mW max. (Operating) for 25ns
  605mW max. (Operating) for 35ns
  138mW max. (TTL Standby)
  83mW max. (CMOS Standby)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- Internal parity generator and checker.
- All inputs and outputs have protection against static charge
- Standard 32-pin DIP package (300 mil): (Suffix: P–SK)
- Standard 32-pin FPT package (450 mil): (Suffix: PF)

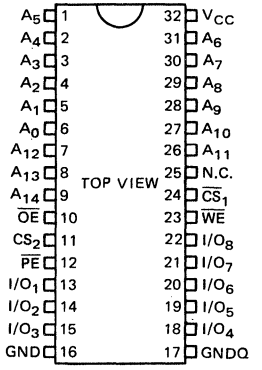


PLASTIC PACKAGE
(DIP-32P-M02)



PLASTIC PACKAGE
(FPT-32P-M02)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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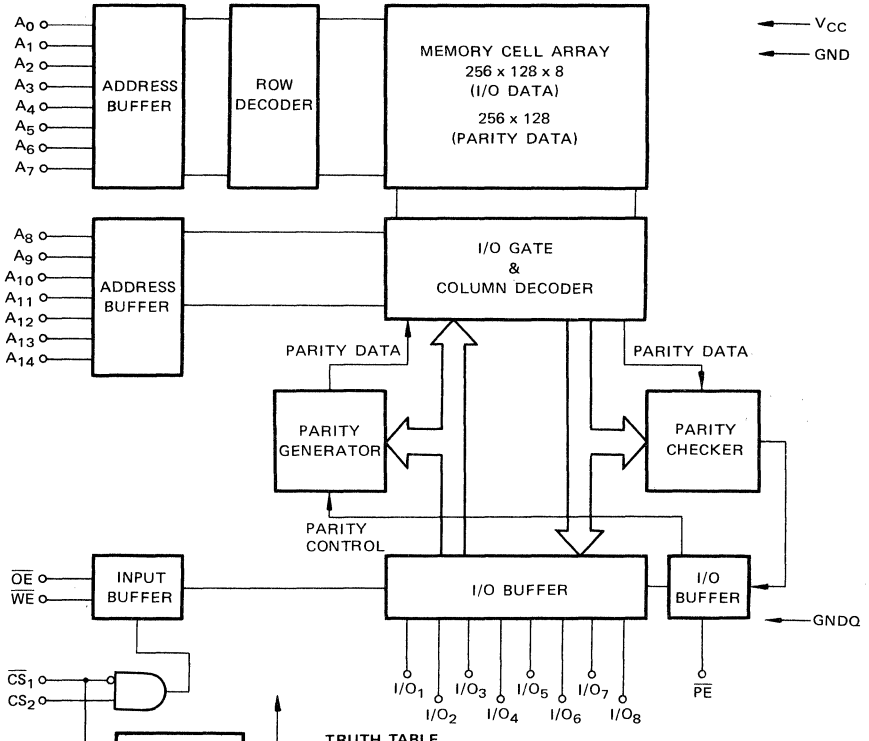
Fig. 1 – MB8287 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O, PE STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	C_{I1}			8	pF
Input Capacitance (Other Input)	V_{IN} = 0V	C_{I2}			7	pF
I/O Capacitance (with $\overline{PE}$)	$V_{I/O}$ = 0V	$C_{I/O}$			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

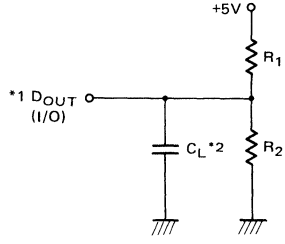
(Recommended operating conditions unless otherside noted.)

Parameter		Symbol	Test Conditions	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS_1} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS_1} = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	I_{OUT} = 0mA, $\overline{CS_1} = V_{IL}$ Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	-5	5	μA
Output Leakage current		$I_{LI/O}$	$\overline{CS_1} = V_{IH}$ = or $\overline{CS_2} = V_{IL}$ or $\overline{WE} = V_{IL}$ or $OE = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}	-5	5	μA
Input Low Voltage		V_{IL}		-2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	I_{OH} = -4mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL} = 8mA		0.4	V

Note: *1 -2.0V Min. for pulse width less than 20ns. (V_{IL} min. = -0.5V at DC level)
All voltages are referenced to GND.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
  Output: V_{OL} = 0.8V, V_{OH} = 2.2V
- Output Load:



*1 $\overline{PE}$ pin is included.
*2 Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE*1

Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Acces Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS_1}$*4*5	t_{LZ1}	5		8		ns
Output Active from CS_2*4*5	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$*4*5	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS_1}$*4*5	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2*4*5	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$*4*5	t_{OHZ}	1	15	1	15	ns
Parity Error Access from Address*2	t_{APA}		28		40	ns
Parity Error Access from $\overline{CS_1}$*3	t_{APCS1}		28		40	ns
Parity Error Access from CS_2*3	t_{APCS2}		14		15	ns
Parity Error Access from $\overline{OE}$	t_{APOE}		12		14	ns
Parity Error Hold from Address Change	t_{POH}	3		3		ns
Parity Error Disable from Address Change*4*5	t_{PHZA}	1	20	1	25	ns
Parity Error Disable from $\overline{CS_1}$*4*5	t_{PHZ1}	1	15	1	15	ns
Parity Error Disable from CS_2*4*5	t_{PHZ2}	1	15	1	15	ns
Parity Error Disable from $\overline{OE}$*4*5	t_{POHZ}	1	15	1	15	ns

Note: *1 $\overline{WE}$ is high for Read Cycle.

*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.

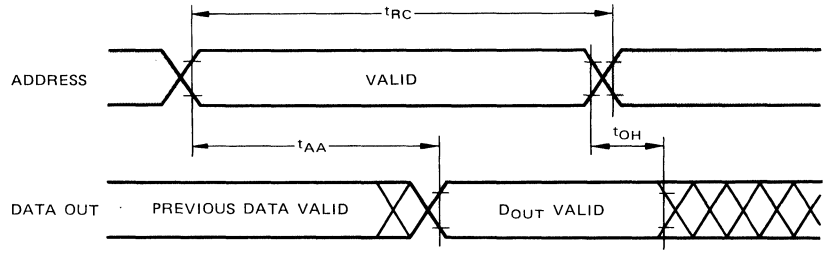
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is specified at the point of ±500mV from steady state voltage.

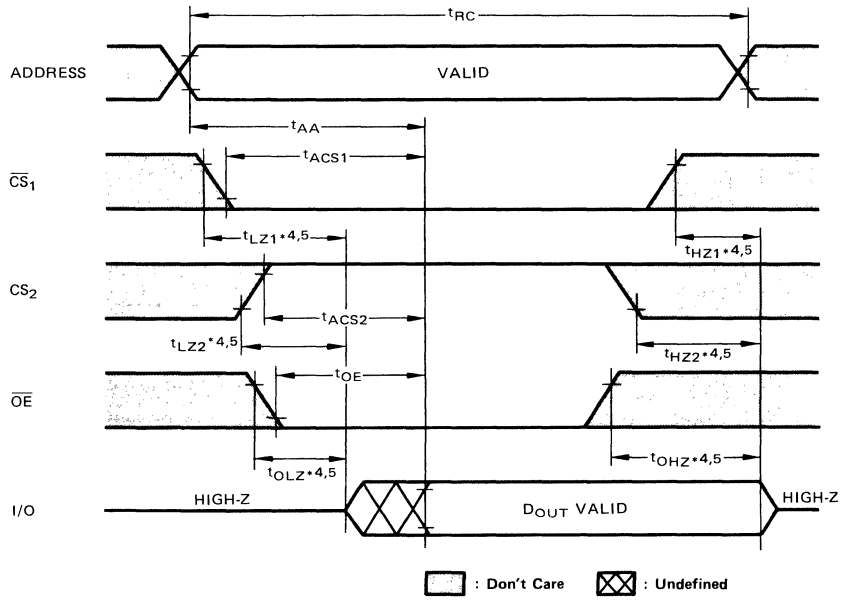
*5 This parameter is specified with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2



READ CYCLE: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.

*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

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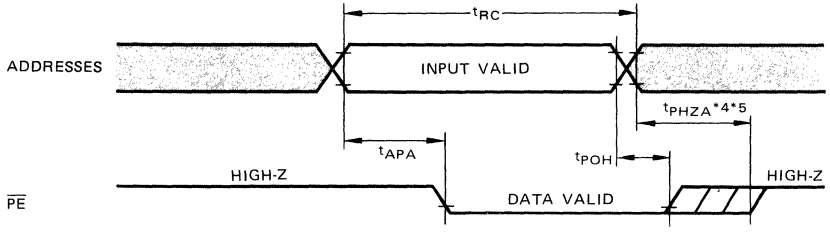
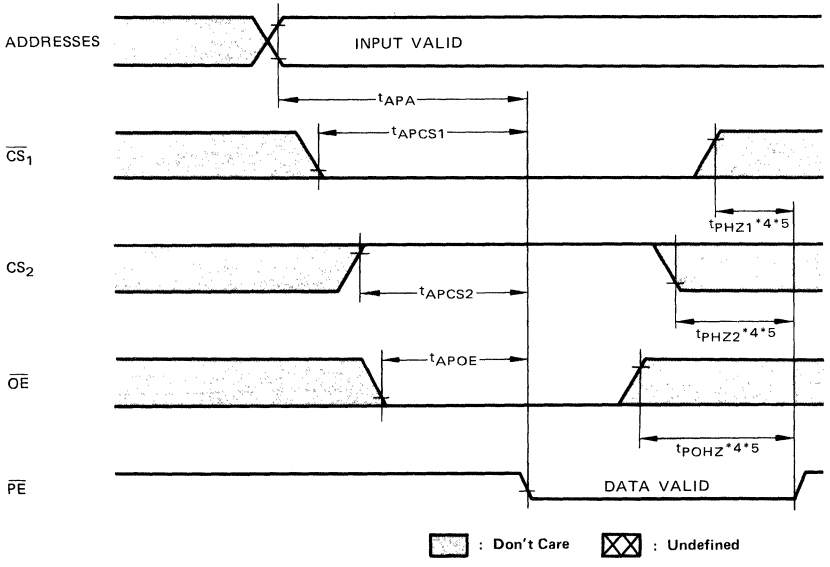
PARITY READ FUNCTION TIMING DIAGRAM*1,6

1) ADDRESS CONTROLLED*2



2) $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}$ = "L", CS_2 = "H" and $\overline{OE}$ = "L".
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 When error occurred, $\overline{PE}$ pin outputs "L". But when no error, $\overline{PE}$ pin is in High-Z state.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1,*6,*7

Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4*5	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4*5	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All Write Cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of Write Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.

*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

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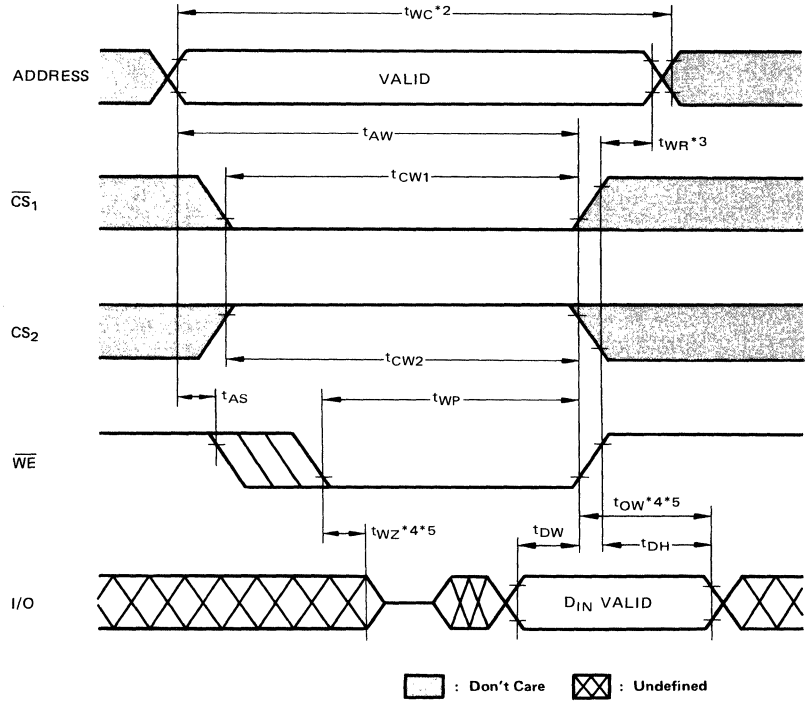
WRITE CYCLE TIMING DIAGRAM *1,*6,*7

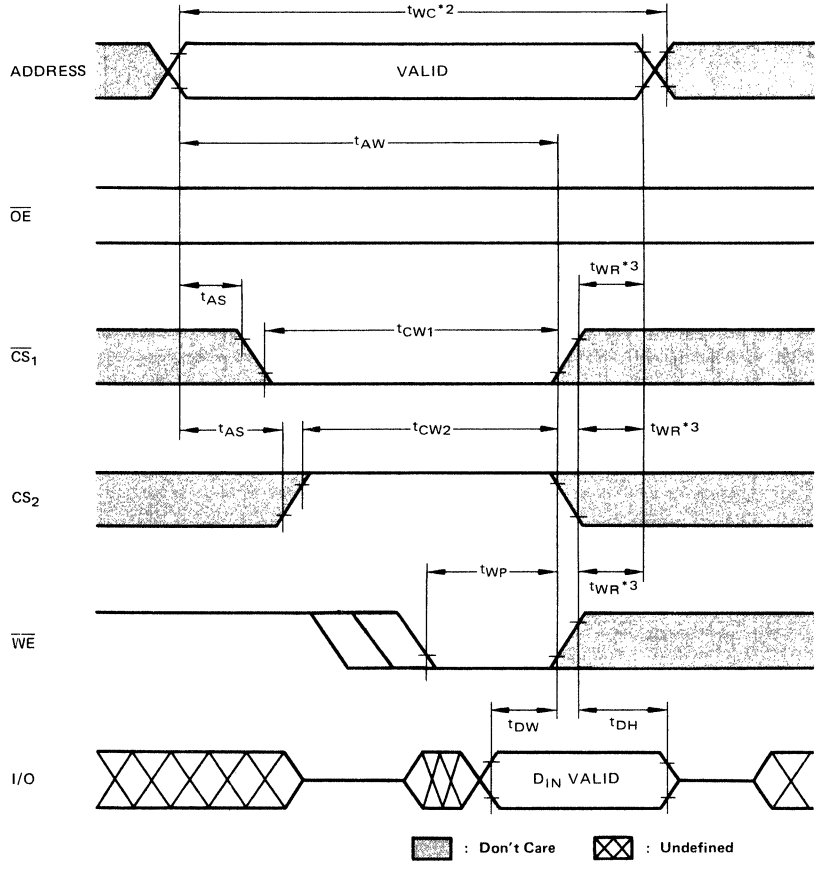
WRITE CYCLE No. 1 ($\overline{WE}$ CONTRORRED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

WRITE CYCLE TIMING DIAGRAM *1,*6,*7

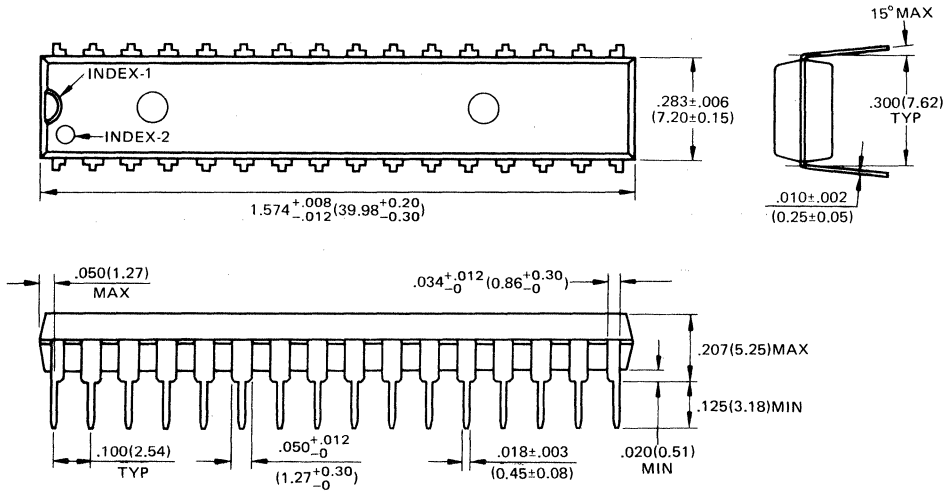
WRITE CYCLE No. 2 ($\overline{CS_1}$, CS_2 CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
*6 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*7 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

PACKAGE DIMENSIONS

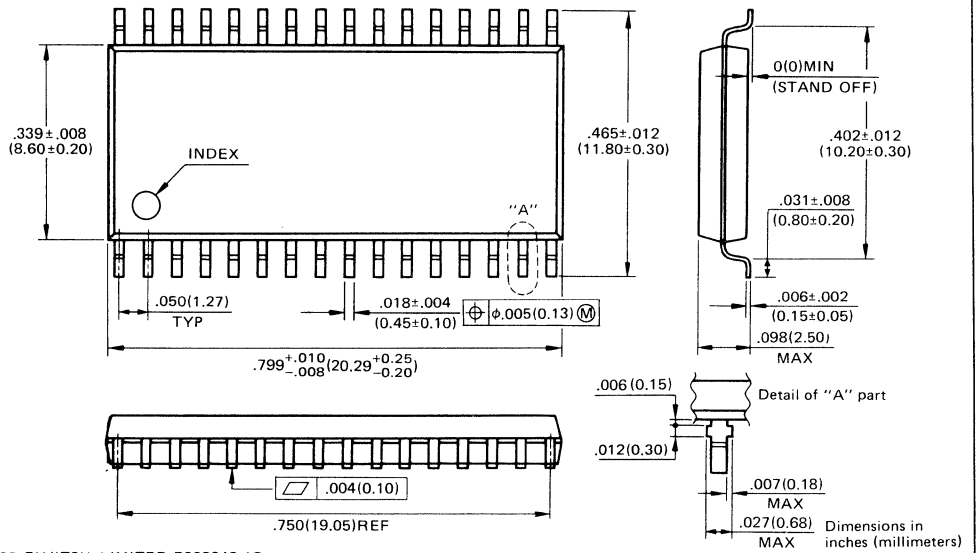
32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

32-LEAD PLASTIC SMALL OUTLINE PACKAGE
(CASE No.: FPT-32P-M02)



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FUJITSU

DUAL PORT STATIC RAM 2K x 8-BIT CMOS

MB8421/22-90
MB8421/22-90L
MB8421/22-12
MB8421/22-12L

May 1989
Edition 2.0

DUAL PORT STATIC RAM 2K X 8-BIT CMOS

The Fujitsu MB8421/MB8422 are 2K by 8 dual-port high-performance Static Random Access Memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus, no external clocks are required. The MB8421 and MB8422 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation — a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$.

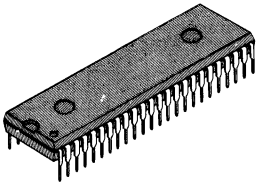
To avoid data contention on the same address, a ($\overline{BUSY}$) flag is provided for address arbitration; in addition, the MB8421 utilizes an ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. Both devices use a single 5-volt power supply and all pins are TTL-compatible.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.

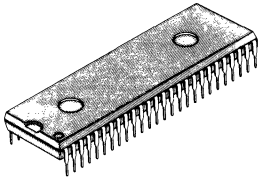
- Organization: 2048 words by 8 bits.
- Static operation: No clocks or timing strobes required.
- Fast Access Time:
  - MB8421/22-90, MB8421/22-90L: $t_{AA} = t_{ACS} = 90$ ns (max)
  - MB8421/22-12, MB8421/22-12L: $t_{AA} = t_{ACS} = 120$ ns (max)
- Low Power Consumption:

	Standard Version	Low Power Version
Both ports active	= 660 mW (max)	495 mW (max)
One port active	= 385 mW (max)	275 mW (max)
Both ports standby/ CMOS	= 11 mW (max)	1.1 mW (max)
Both ports standby/ TTL	= 38.5 mW (max)	27.5 mW (max)

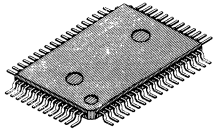
- TTL-Compatible Inputs and Outputs.
- Three-State Outputs with Or-tie Capability.
- Electrostatic Protection for All Inputs and Outputs.
- Address Arbitration: ($\overline{BUSY}$) flag.
- Interrupt Function for Communication Between Systems (MB8421 only): ($\overline{INT}$) flag.
- Data Retention Voltage: 2.0V min.
- Single +5V ($\pm$ 10%) Supply.



DIP-48P-M02



DIP-52P-M01



FPT-64P-M01

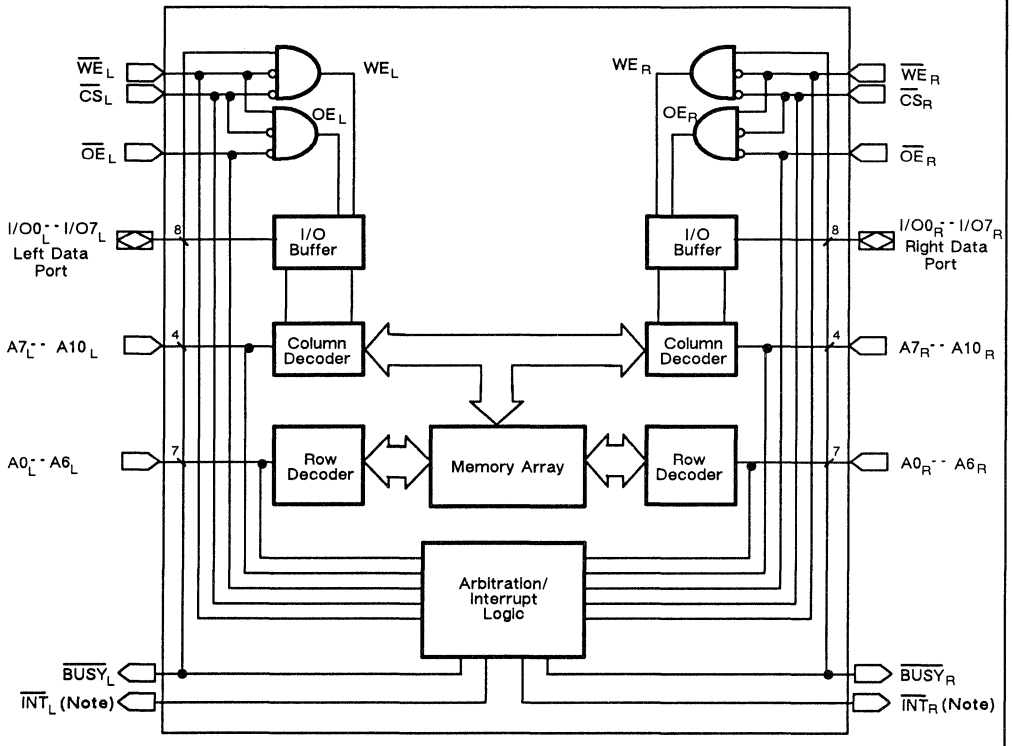
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS [1, 2]

Parameter	Designator	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	VIN	-0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	VOUT	-0.5 to V_{CC} +0.5	V
Output Current	IOUT	$\pm$ 20	mA
Power dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-45 to +125	°C

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — BLOCK DIAGRAM OF MB8421/22



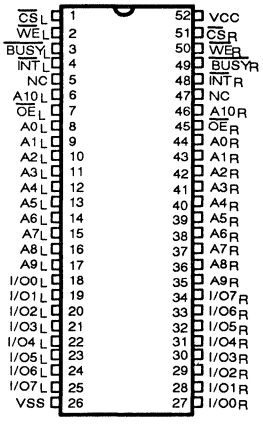
NOTES: MB8421 only.

I/O CAPACITANCE (T_A = 25 °C, f = 1 MHz)

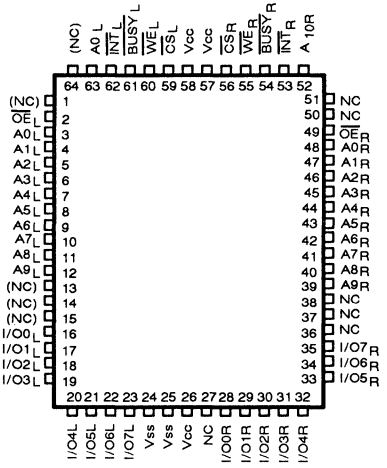
Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN		10	pF
I/O Capacitance (VI/O = 0V)	CI/O		10	pF

PIN ASSIGNMENTS

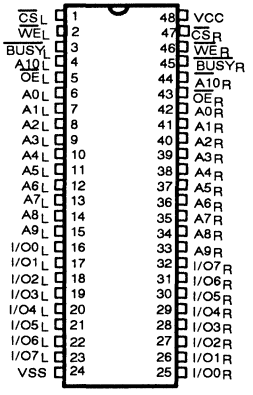
MB8421 - Top View
(DIP-52P-M01)



MB8421 - Top View
(FPT-64P-M01)



MB8422 - Top View
(DIP-48P-M02)



PIN DESCRIPTIONS

Left Port	Right Port	Function	Left Port	Right Port	Function
$\overline{WE}_L$	$\overline{WE}_R$	Write Enable	$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select	$A0_L$ -- $A10_L$	$A0_R$ -- $A10_R$	Address
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable	$I/O0_L$ -- $I/O7_L$	$I/O0_R$ -- $I/O7_R$	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag			
Vcc					Power (Common)
Vss					Ground (Common)

FUNCTIONAL OPERATION

The MB8421 and MB8422 provide two ports with separate control signals, address inputs, and input/output data pins that allow asynchronous read and write operations to any memory location. Each device has an on-chip automatic power-down feature controlled by $\overline{CS}$ that places the respective port in the standby mode when the chip is deselected ($\overline{CS}$ is HIGH).

When a port is enabled, access to the entire memory array is permitted. Each port has an independent Output Enable ($\overline{OE}$) control that is active in the read mode and enables the output drivers. Non-contention Read/Write conditions are shown in the following Truth Table; a simplified block diagram of the dual-port SRAM is shown in Figure 1.

NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS[1]			RIGHT PORT INPUTS[1]			FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. $A0_L$-$A10_L \neq A0_R$ - $A10_R$
2. H = HIGH, L = LOW, X = Don't Care

ARBITRATION LOGIC

4

The arbitration logic resolves an address match or chip-enable match and determines the access priority. In both cases, an active $\overline{BUSY}$ flag is set for the port-in-waiting. Since both ports are asynchronous, there is the possibility of accessing the same memory location from both sides. In the read mode, this condition is not a problem. However, this is a problem when both ports are in a write mode with different data words or when one port is reading and the other is writing. When both ports access the same memory location, the on-chip arbitration logic determines which port has access and the $\overline{BUSY}$ flag for the delayed port is set active LOW and all operations on that port are inhibited. The delayed port can be accessed when the $\overline{BUSY}$ flag becomes inactive. Basic modes of abitration are described in subsequent paragraphs.

1. When addresses for both the left and right ports match and are valid before $\overline{CS}$ is active, the on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for device access. Refer to the following Truth Table for signal states; timing detail is shown later in this data sheet under "Data Contention Cycle No. 2 ($\overline{CS}$ controlled)."
2. When $\overline{CS}_L$ and $\overline{CS}_R$ are LOW before an address match, on-chip control logic arbitrates between the left and right addresses for device access. Signal states for this condition are shown in the following Truth Table; timing detail is shown under "Data Contention Cycle No. 1 (Address Controlled)."

ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Right Operation Permitted Left Operation Not Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, LST= Low Same Time, LBR = Low Before Right, LBL = Low Before Left

ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Right Operation Permitted Left Operation Not Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left

When both $\overline{CS}_L$ and $\overline{CS}_R$ are low at the same time ($\overline{CS}$ controlled) or when both left-and-right addresses are valid at the same time (address controlled), the $\overline{BUSY}_R$ flag for the right port is set to the active LOW state and access is granted to the left port.

For the Intel 8086 and Fujitsu's MBL8086 as well as most other microprocessors, the asynchronous $\overline{BUSY}$ signal can be directly tied to the READY input, providing setup-and-hold time requirements are met.

INTERRUPT FUNCTION

The interrupt ($\overline{INT}$) function provides communication between systems on both sides of the dual-port RAM. $\overline{INT}_L$ is set LOW when the processor on the right port writes to address 7FE (A0 = L and A1-A10 = H). When the left port acknowledges by reading address 7FE, $\overline{INT}_L$ is then reset to HIGH. In essence, address 7FE serves as an 8-bit mailbox that transfers information from the right port to the left port. When $\overline{INT}_R$ is set LOW, the processor on the left port writes to address 7FF (A0-A10=H). When the right port acknowledges by reading address 7FF, $\overline{INT}_R$ is then reset to HIGH. Hence, address 7FF serves as a second 8-bit mailbox, transferring information from the left port to the right port.

On power-up, $\overline{INT}_L$ and $\overline{INT}_R$ are set to a HIGH state. However, if one port is in the standby mode, the standby port can still be interrupted by the processor on the other port. But if the $\overline{BUSY}$ flag is set to the LOW state, the port associated with that flag cannot set or reset the $\overline{INT}$ flag.

4

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	Vcc	4.5	5.0	5.5	V
Input High Voltage	VIH	2.2		Vcc +0.3	V
Input Low Voltage	VIL	-0.3		0.8	V
Operating Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8421-90/12 MB8422-90/12		MB8421-90L/12L MB8422-90L/12L		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	ICC	Cycle = Min Duty = 100% IOUT = 0 mA		120		90	mA
Standby Supply Current	ISB1	Both ports at Standby $\overline{CS}_L$ & $\overline{CS}_R$ = VIH		7		5	mA
	ISB2	One port at Standby $\overline{CS}_L$ or $\overline{CS}_R$ =VIH, IOUT = 0 mA		70		50	mA
	ISB3	Both ports at Full Standby $\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc -0.2V		2		0.2	mA
	ISB4	One port at Full Standby $\overline{CS}_L$ or $\overline{CS}_R \geq$ Vcc -0.2V IOUT = 0 mA		70		50	mA
Input Leakage Current	ILI	VIN = 0V to Vcc	-10	10	-10	10	µA
Output Leakage Current	ILO	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	-10	10	-10	10	µA
Output High Voltage	VOH (Note)	IOUT = -1.0 mA	2.4		2.4		V
Output Low Voltage	VOL	IOUT = 3.2 mA		0.4		0.4	V
Output Low Voltage for Open-Drain	VOL	IOUT = 8 mA		0.4		0.4	V

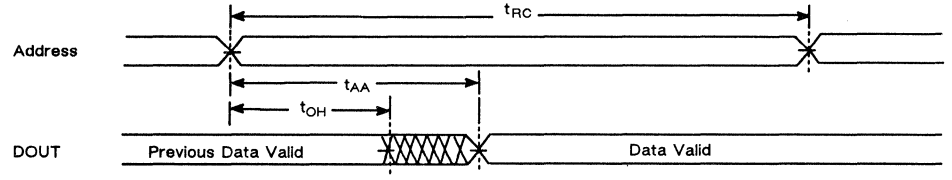
NOTE: The $\overline{BUSY}$ and $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC CHARACTERISTICS

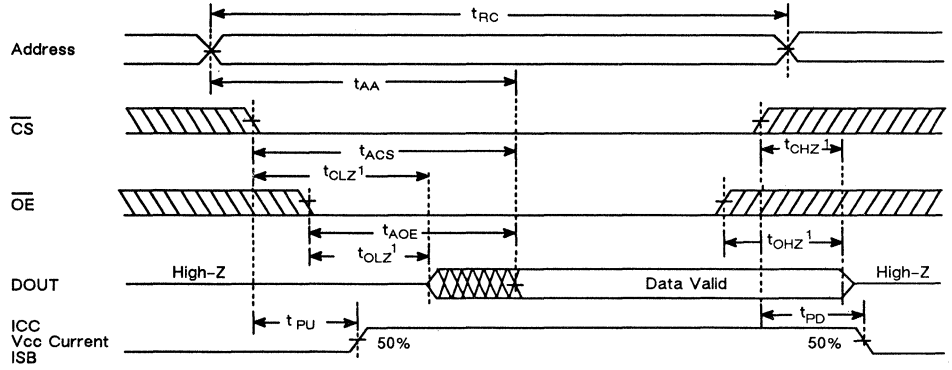
(Recommended Operations Conditions unless otherwise noted.)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
Read Cycle Parameters & Timing Diagrams						
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z (Note 1)	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z (Note 1)	t_{OLZ}	5		5		ns
Chip Select to Output High-Z (Note 1)	t_{CHZ}		40		50	ns
Output Enable to Output High-Z (Note 1)	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

Read Cycle No. 1 [2, 3]:



Read Cycle No. 2 [2]:



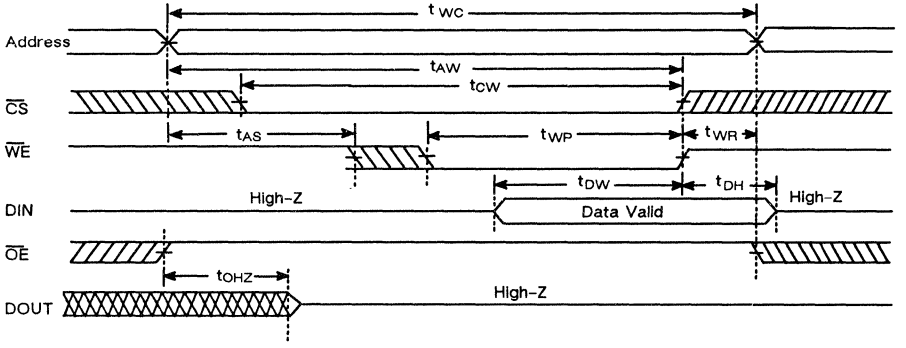
NOTES:

1. Transition is measured at a point of ± 500 mV from steady-state voltage with an output capacitance of 5pF.
2. $\overline{WE}$ is High during read cycle.
3. Device is continuously selected ($\overline{CS}$ = $\overline{OE}$ = VIL).

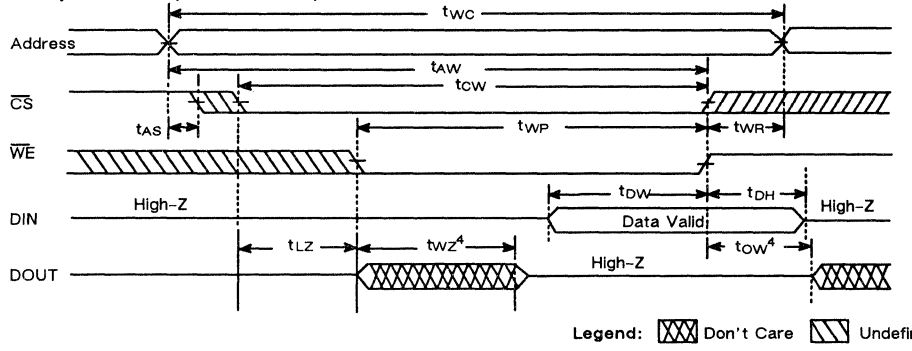
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L Min	MB8421-90/90L MB8422-90/90L Max	MB8421-12/12L MB8422-12/12L Min	MB8421-12/12L MB8422-12/12L Max	Unit
Write Cycle Parameters & Timing Diagrams						
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z (Note 4)	t_{OW}	0		0		ns
Write Enable to Output High-Z (Note 4)	t_{WZ}		40		50	ns

Write Cycle No. 1 ($\overline{WE}$ Controlled) [1,2]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [1,2,3]



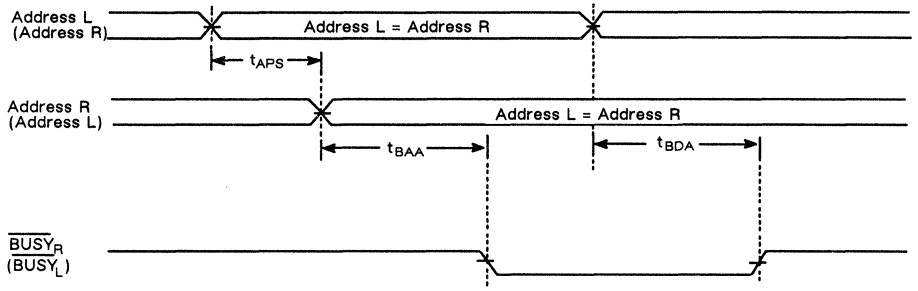
Legend: Don't Care, Undefined

NOTES:
1. The Write Enable ($\overline{WE}$) signal must be high during an address transition.
2. If the Output Enable ($\overline{OE}$) and Chip Select ($\overline{CS}$) signals are in the Read Mode, the associated I/O pins are in the output state; accordingly, input signals of opposite phase must not be applied to the outputs.
3. If $\overline{CS}$ goes high prior to or coincident with the low-to-high transition of $\overline{WE}$, the output remains in high-impedance state.
4. This parameter is specified at a point ± 500 mV from steady-state voltage with an output capacitance of 5 pF.

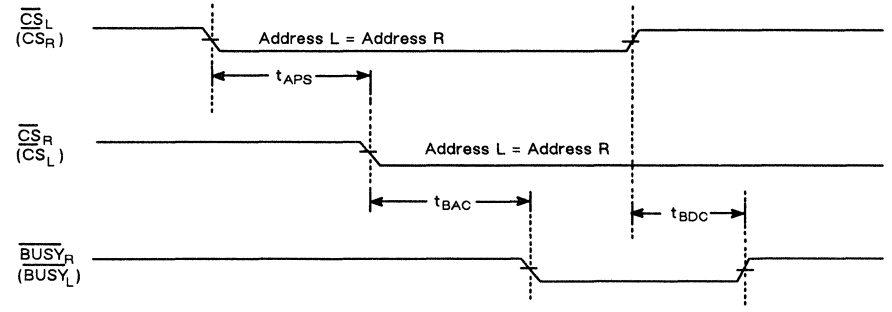
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
$\overline{BUSY}$ Parameters & Data Contention Timing						
$\overline{BUSY}$ Access Time from Address	t_{BAA}		45		60	ns
$\overline{BUSY}$ Output High-Z from Address	t_{BDA}		45		60	ns
$\overline{BUSY}$ Access Time from $\overline{CS}$	t_{BAC}		45		60	ns
$\overline{BUSY}$ Output High-Z from $\overline{CS}$	t_{BDC}		45		60	ns
Arbitration Priority Set up Time	t_{APS}	20		25		ns

Data Contention Cycle No. 1 (Address Controlled)[1, 2]:



Data Contention Cycle No. 2 ($\overline{CS}$ Controlled)[1, 3]:



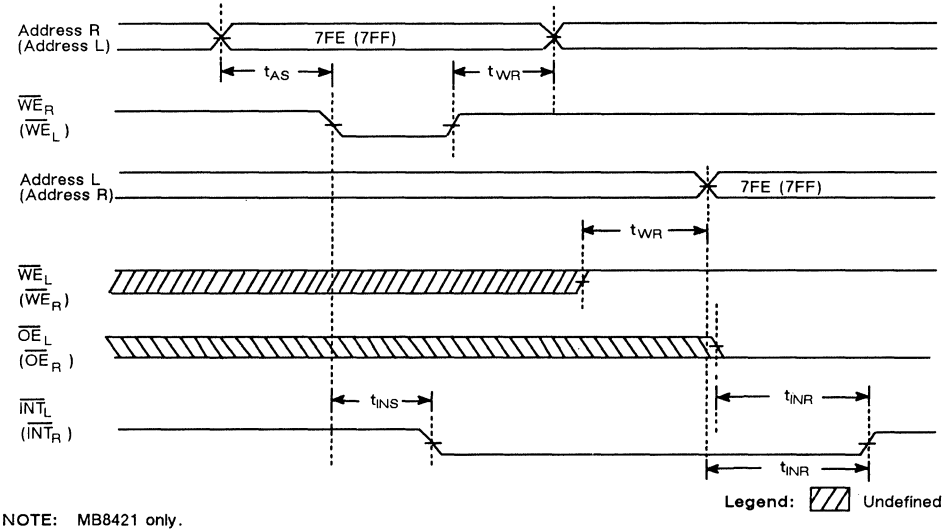
NOTES:

1. In case of dual-access at the same memory location, the port that accesses the RAM first sets the $\overline{BUSY}$ flag HIGH.
2. Chip Select ($\overline{CS}$) signal must be low before or coincident with an address transition.
3. Address is valid prior to or coincidence with the high-to-low transition of $\overline{CS}$.

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
Interrupt Parameters & Timing Diagram						
$\overline{INT}$ Set Time (Note)	t_{INS}		80		100	ns
$\overline{INT}$ Reset Time (Note)	t_{INR}		80		100	ns

Interrupt Cycle Timing



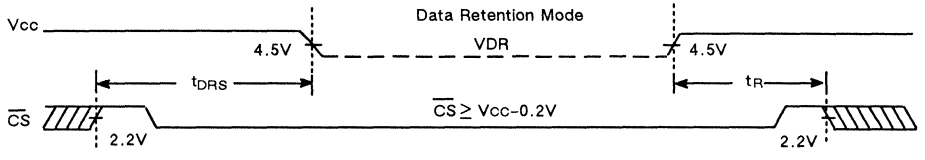
NOTE: MB8421 only.

4

AC CHARACTERISTICS (Continued)

DATA RETENTION PARAMETERS & TIMING

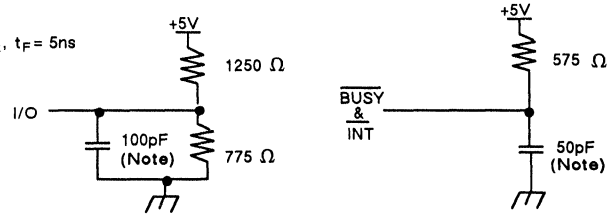
Parameter	Symbol	MB8421-90/12 MB8422-90/12		MB8421-90L/12L MB8422-90L/12L		Unit
		Min	Max	Min	Max	
Data Retention Parameters & Timing						
Data Retention Supply Voltage	VDR	2.0	5.5	2.0	5.5	V
Data Retention Supply Current (Note)	IDR		0.2		0.02	mA
Data Retention Setup Time	t_{DRS}	0		0		ns
Operation Recovery Time	t_R	t_{RC}		t_{RC}		ns



NOTE: Vcc = VDR = 3V
$\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc - 0.2

AC TEST CONDITIONS

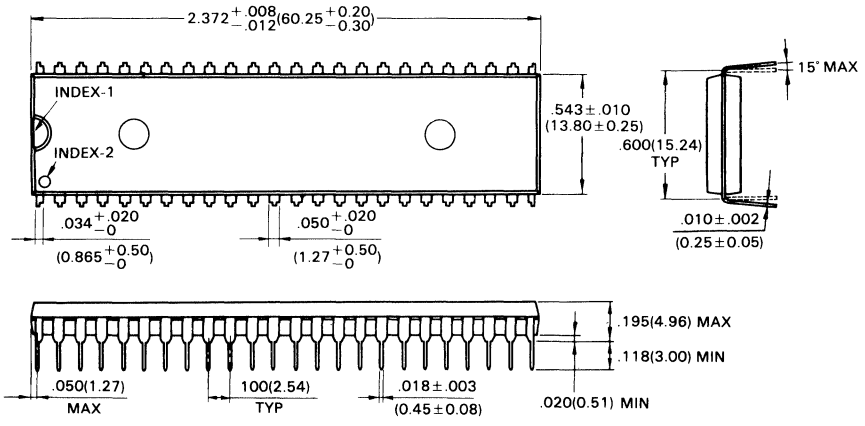
Input Pulse Levels: 0 to 3.0V
Input Pulse Rise & Fall Times: t_R, t_F = 5ns
Timing Reference Levels: 1.5V
Output Loads:



NOTE: Includes jig and stray capacitance.

PACKAGE DIMENSIONS

48-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE NO.: DIP-48P-M02)

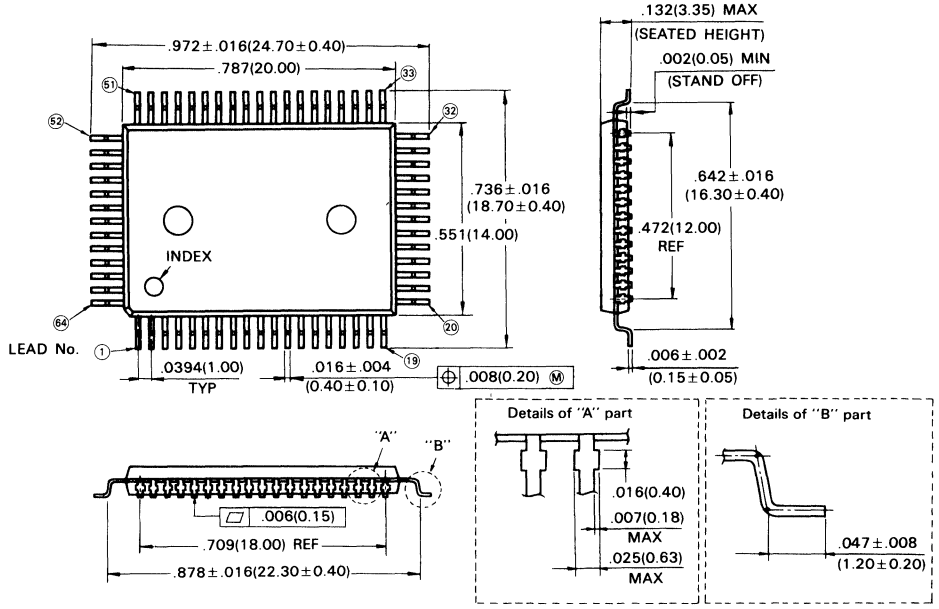


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

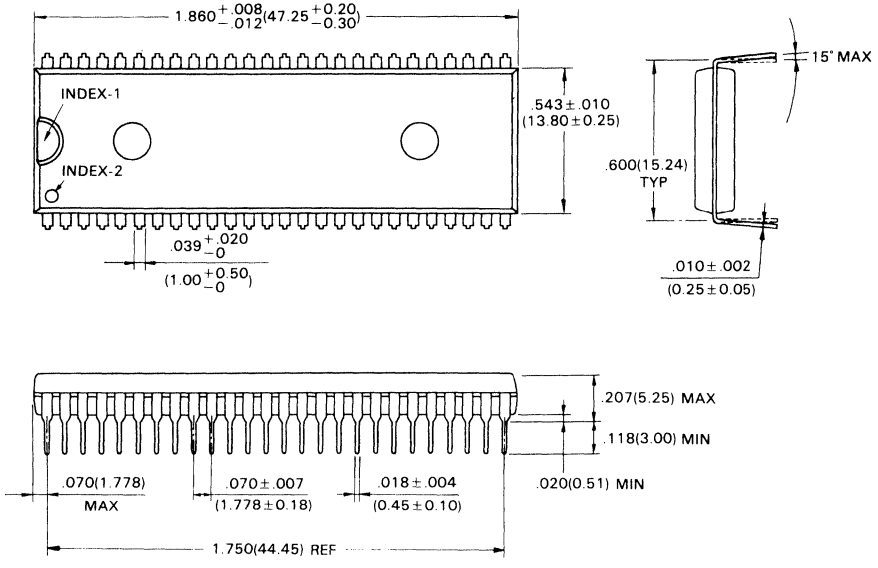
64 LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

52-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-52P-M01)



Dimensions in
inches (millimeters)

4

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB8431/32-90/-90L/-90LL/-12/-12L/-12LL
CMOS 16K-BIT DUAL PORT SRAM

2K X 8–BIT CMOS DUAL PORT STATIC RANDOM ACCESS MEMORY

The Fujitsu MB8431/32 are 2K words x 8 bits Dual port high–performance–static Random Access Memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus no external clockes are required.

The MB8431 and MB8432 provide the user with two separately contorolled I/O ports with independent address, Chip select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$) and I/O functions.

This arrangement permits independent access to any memory location for either a Read or Write operation – a useful feature for shared data processing applications. These devices have an automatic power–down feature controlled by ($\overline{CS}$).

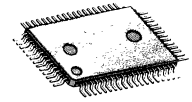
To avoide data contention on the same address, a ($\overline{BUSY}$) input is provided for address arbitration; In addition, MB8431 utilizes ($\overline{INT}$) flag which allows communication between systems on either side of the RAM.

Both devices use a single +5volt power supply and all pins are TTL–compatible. A simplified block diagram of the SRAM is shown in Figure 1.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files and peripheral controllers.

- Organization: 2048 words x 8 bits
- Static operation: No clocks or timing strobe required
- Fast access time: $t_{AA}=t_{ACS}$=90ns max. (MB8431/32–90, MB8431/32–90L/–90LL)
  $t_{AA}=t_{ACS}$=120ns max. (MB8431/32–12, MB8431/32–12L/–12LL)
- Low power consumption: 660mW max. (Both ports active)
  385mW max. (One port active)
  38.5mW max. (Both ports standby, TTL)
  11mW max. (Both ports standby, CMOS)
  L–version/LL–version: 495mW max. (Both ports active)
  275mW max. (One port active)
  27.5mW max. (Both ports standby, TTL)
  1.1mA max. (Both ports standby, CMOS)
- Single +5V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three–state outputs with OR–tie capability
- All inputs and outputs have protection against static charge
- Data Retention Voltage: 2V min.
- Address Arbitration Function: $\overline{BUSY}$ input
- Interrupt Function for Communication between Systems (MB8431 only): $\overline{INT}$ flag
- Expanding capability using MB8421/22 (Master)–MB8431/32 (Slave)

DIP–52P–M01
(MB8431)



FPT–64P–M01
(MB8431)

DIP–48P–M02
(MB8432)

PIN ASSIGNMENT

See Page 15

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

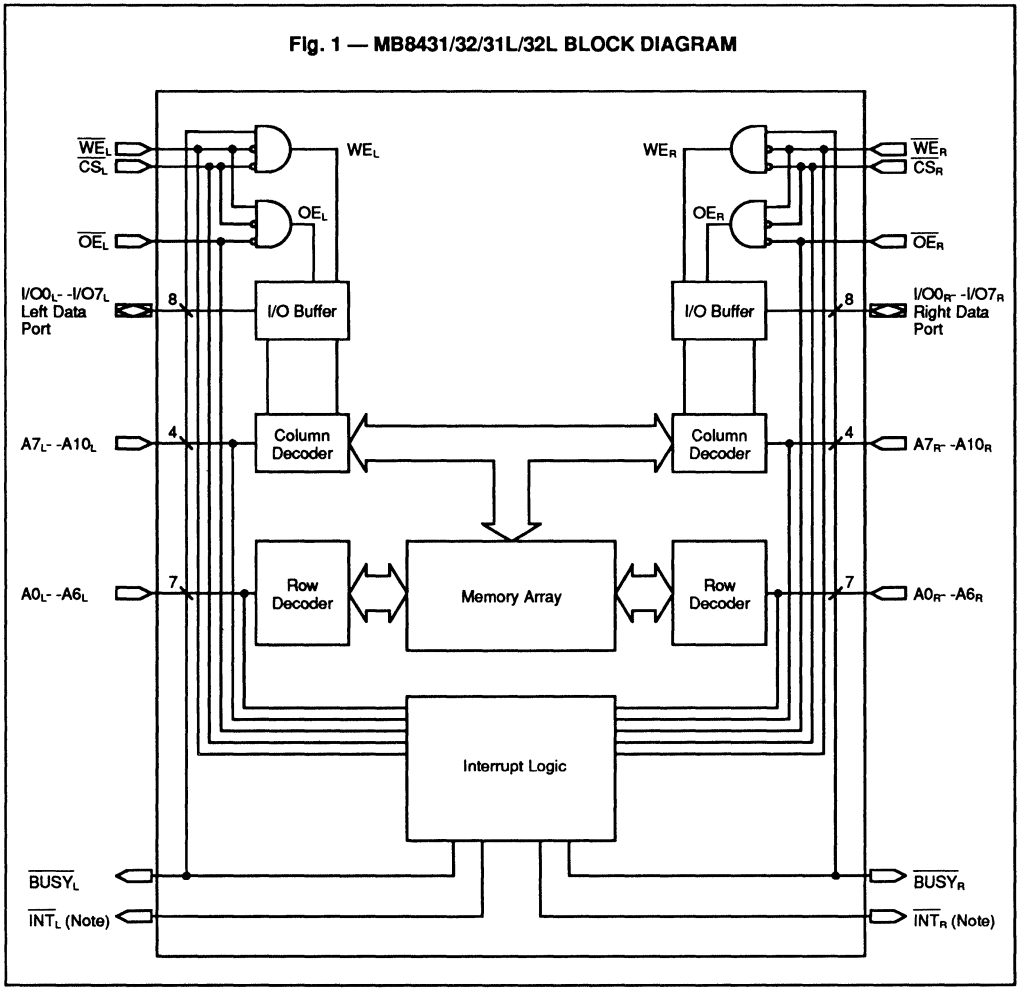
4

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS_L}$	$\overline{CS_R}$	Chip Select Input
$\overline{WE_L}$	$\overline{WE_R}$	Write Enable Input
$\overline{OE_L}$	$\overline{OE_R}$	Output Enable Input
$\overline{INT_L}$	$\overline{INT_R}$	Interrupt * Flag Output
$\overline{BUSY_L}$	$\overline{BUSY_R}$	Busy Flag Input
$A0_L$ to $A10_L$	$A0_R$ to $A10_R$	Address Input
$I/O0_L$ to $I/O7_L$	$I/O0_R$ to $I/O7_R$	Data Input/Output
V_{CC}		Power
GND		Ground

*: Applies to MB8431 only.

Fig. 1 — MB8431/32/31L/32L BLOCK DIAGRAM



Note: MB8431 only.

4

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN=0V)	C_{IN}		10	pF
I/O Capacitance (VI/O=0V)	$C_{I/O}$		10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS

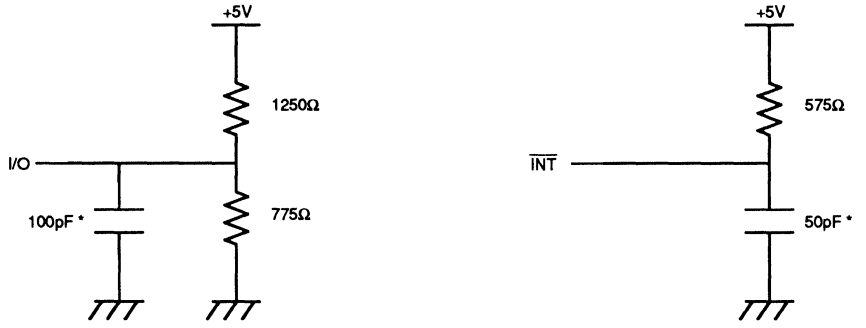
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8431/ MB8432-90/12		MB8431/ MB8432-90L/90LL/12L/12LL		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	I_{CC}	Cycle=Min. Duty=100% I_{OUT}=0mA		120		90	mA
Standby Supply Current	I_{SB1}	Both ports=Standby $\overline{CS_L}$ & $\overline{CS_R}$=V_{IH}		7		5	mA
	I_{SB2}	One port=Standby $\overline{CS_L}$ or $\overline{CS_R}$=V_{IH}, I_{OUT}=0mA		70		50	mA
	I_{SB3}	Both ports=Full standby $\overline{CS_L}$ & $\overline{CS_R}$≥V_{CC}–0.2V		2		0.2	mA
	I_{SB4}	One port=Full standby $\overline{CS_L}$ or $\overline{CS_R}$≥V_{CC}–0.2V, I_{OUT}=0mA		70		50	mA
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	–10	10	–10	10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, I/O=0V to V_{CC}	–10	10	–10	10	µA
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3 *1	0.8	–0.3 *1	0.8	V
Output High Voltage	V_{OH} *2	I_{OUT}=–1.0mA	2.4		2.4		V
Output Low Voltage	V_{OL}	I_{OUT}=3.2mA		0.4		0.4	V
Output Low Voltage for Open-Drain	V_{OL}	I_{OUT}=8mA		0.4		0.4	V

*1 Undershoot –3.0V min at less than 20ns pulse width.
*2 The $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: tR, tF=5ns
- Timing Reference Levels: 1.5V
- Output Load



* Including Jig and stray capacitance

4

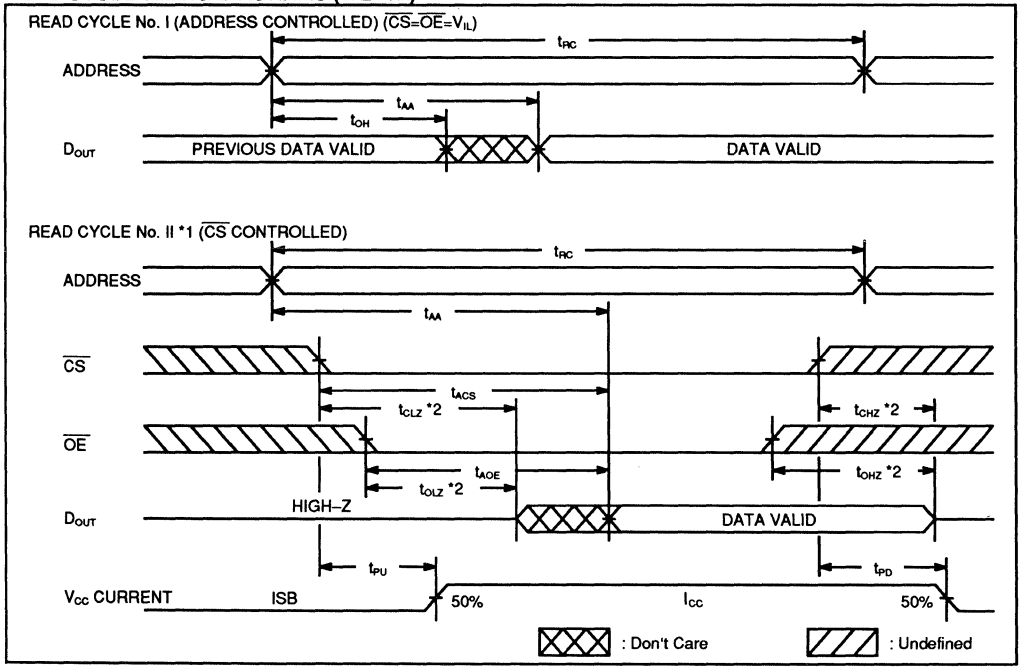
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z *2	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z *2	t_{OLZ}	5		5		ns
Chip Select to Output High-Z *2	t_{CHZ}		40		50	ns
Output Enable to Output High-Z *2	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

READ CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

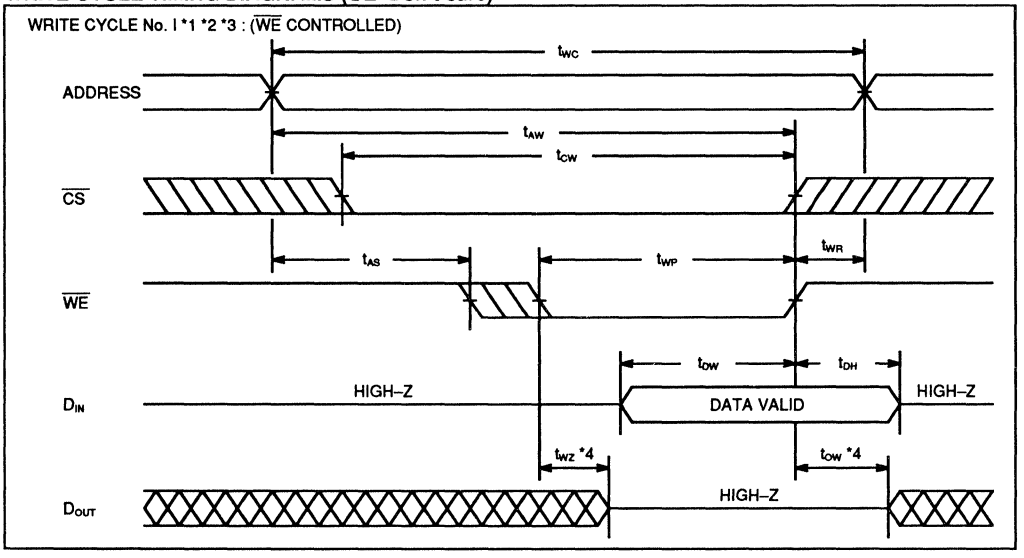


Note: *1 Address should be fixed before high-to-low transition of $\overline{CS}$.
*2 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

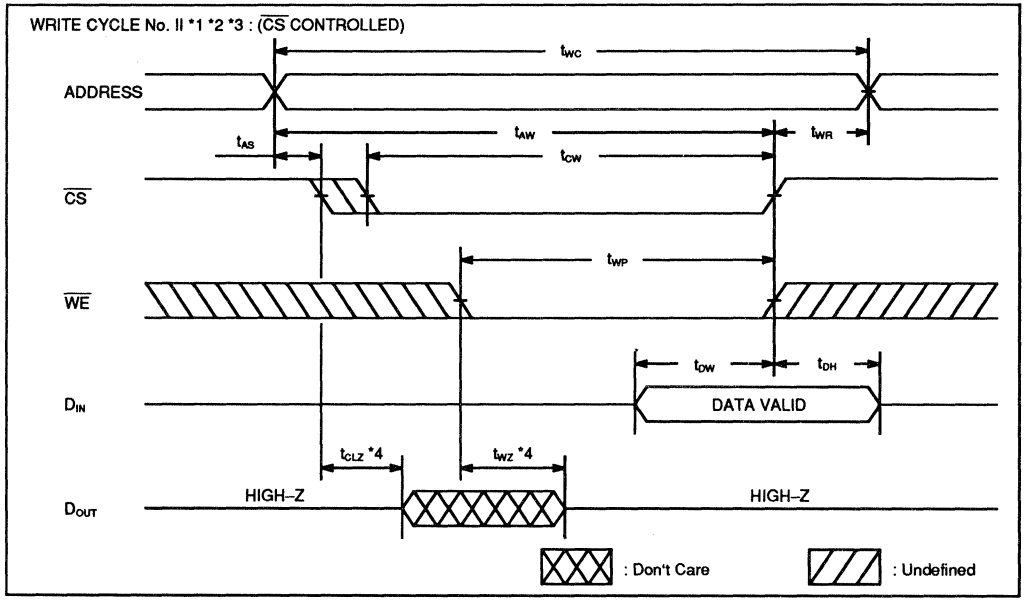
WRITE CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z *4	t_{OW}	0		0		ns
Write Enable to Output High-Z *4	t_{WZ}		40		50	ns

WRITE CYCLE TIMING DIAGRAMS ($\overline{OE}$=Don't care)



Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 Transition is measured at the point of ±500mV from steady state voltage with C_L=5pF.



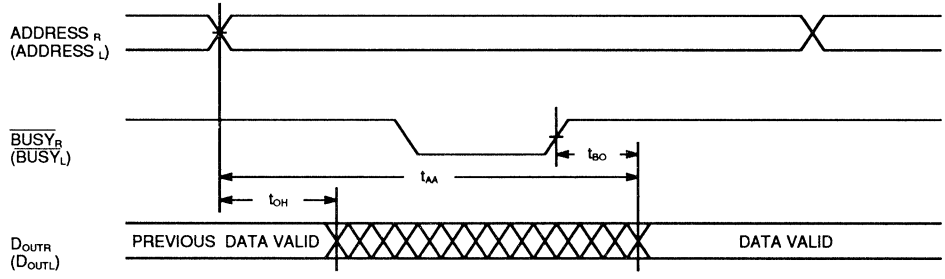
Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

SLAVE BUSY TIMING

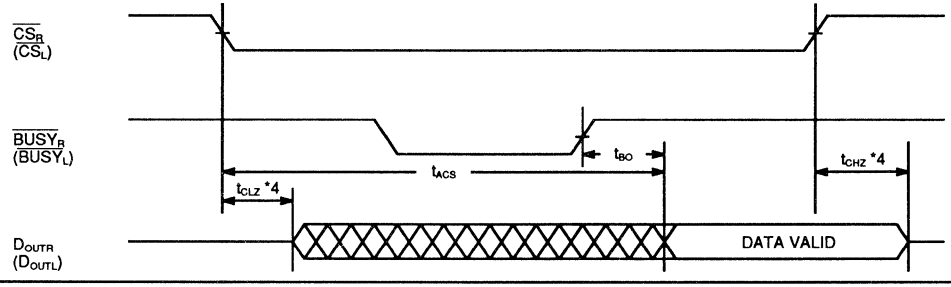
Parameter	Symbol	MB8431–90/90L/90LL MB8432–90/90L/90LL		MB8431–12/12L/12LL MB8432–12/12L/12LL		Unit
		Min	Max	Min	Max	
Busy Access Time	t_{BO}		0		0	ns
Write Set Up Time To Busy	t_{WS}	–10		–10		ns
Write Hold Time From Busy	t_{WH}	20		25		ns

CONTENTION CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

CONTENTION READ CYCLE No. I *1 *2 : (ADDRESS CONTROLLED) ($\overline{CS}$=$\overline{OE}$=V_{IL})



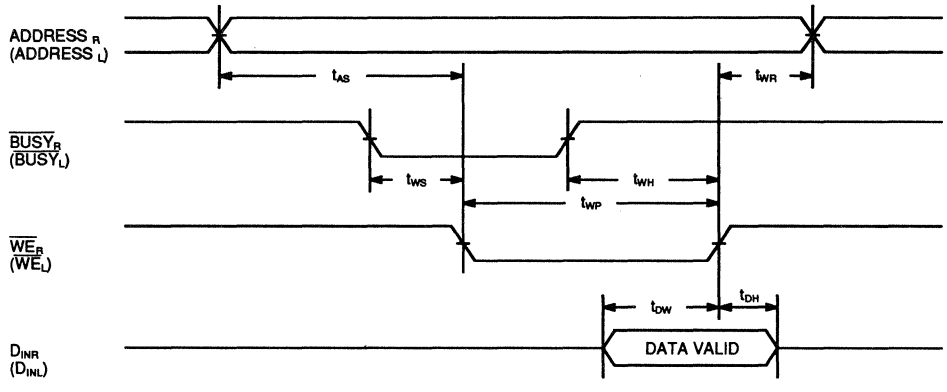
CONTENTION READ CYCLE No. II *1 *3 : ($\overline{CS}$ CONTROLLED)



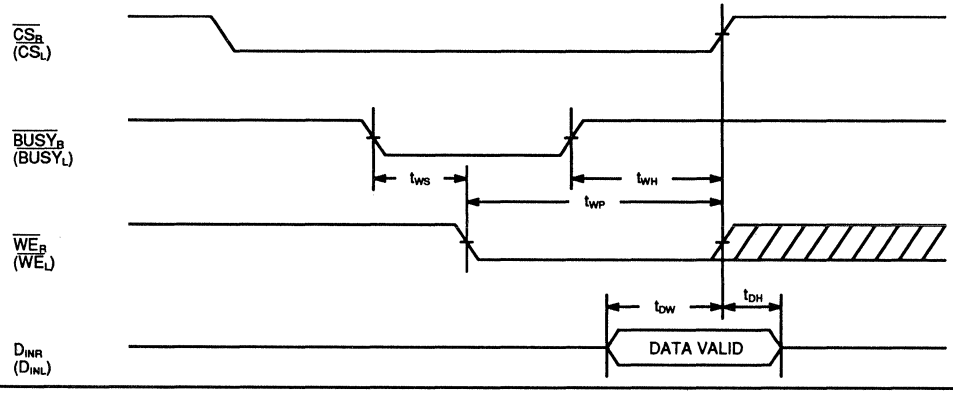
Note: *1 In case of dualaccess at the same memory location, the port that access the RAM first sets the $\overline{BUSY}$ flag high.
*2 $\overline{CS}$ must be low before or coincident with transition of address.
*3 Address is valid prior to cincident with high–to–low transition of $\overline{CS}$.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

CONTENTION CYCLE TIMING DIAGRAMS

CONTENTION WRITE CYCLE No. I *1 *2 *3 ($\overline{WE}$ CONTROLLED)



CONTENTION WRITE CYCLE No. II *3 : *1 *2 *3 ($\overline{CS}$ CONTROLLED)

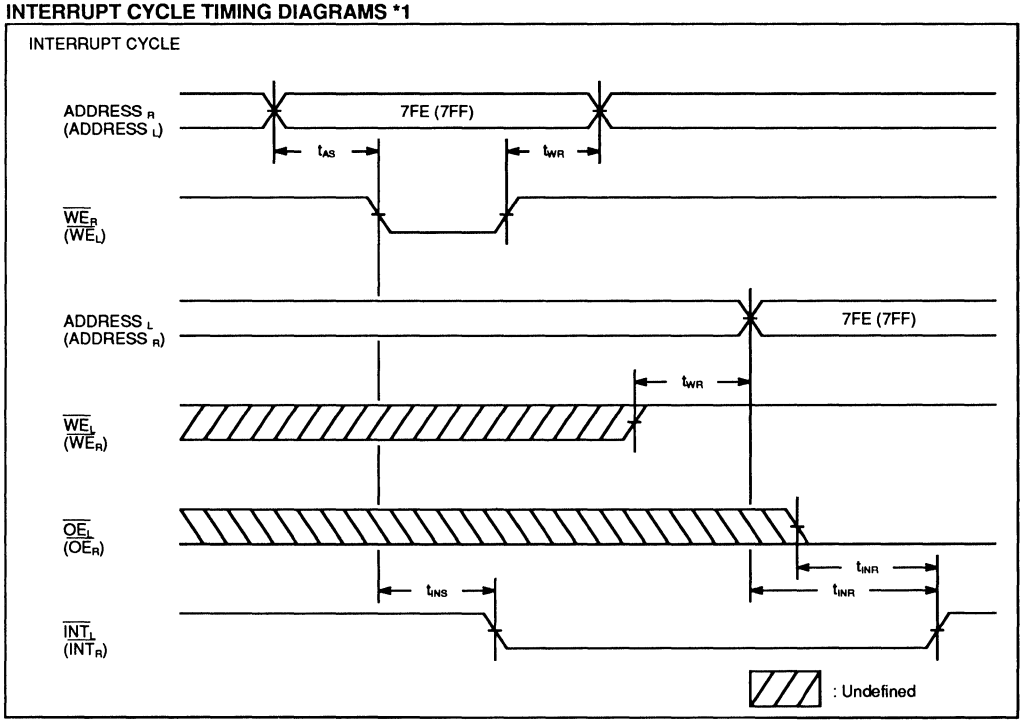


Note: *1 $\overline{WE}$ must be high during address transition.
*2 I/O pins are in the output state, so the input signals of opposite phase must not be applied.
*3 During $\overline{BUSY}$ input is low, write operation can not be excuted even if $\overline{WE}$ is low.

INTERRUPT TIMING *1

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
INT Set Time	t_{INS}		80		100	ns
INT Reset Time	t_{INR}		80		100	ns

INTERRUPT CYCLE TIMING DIAGRAMS *1



Note: *1 Applies to MB8431 only.

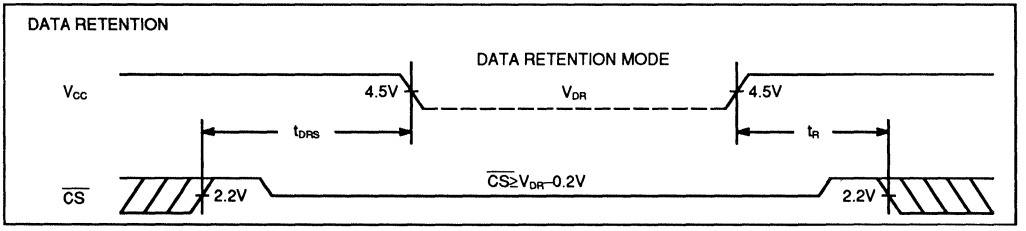
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			0.2	mA
	L-Version				20	µA
	LL-Version *2				2	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $V_{CC}=V_{DR}=3V$, $\overline{CS_L}$ & $\overline{CS_R}\geq V_{CC}-0.2V$
*2 $V_{DR}=3V$, $T_A=0°C$ to $40°C$

DATA RETENTION TIMING



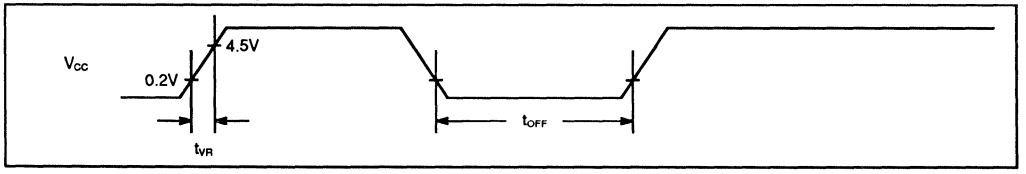
POWER ON/RESET CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Power Up Time *1	t_{VR}	0.05	50	0.05	50	ms
Power Off Time *2	t_{OFF}	1		1		S

*1 This is required to keep normal operation for power on/reset circuit which initialize $\overline{INT}$ output to "H" automatically when V_{CC} is applied.
*2 This is required to keep normal operation for power on/reset circuit which V_{CC} is repeatly turn on/off.

POWER ON/RESET TIMING

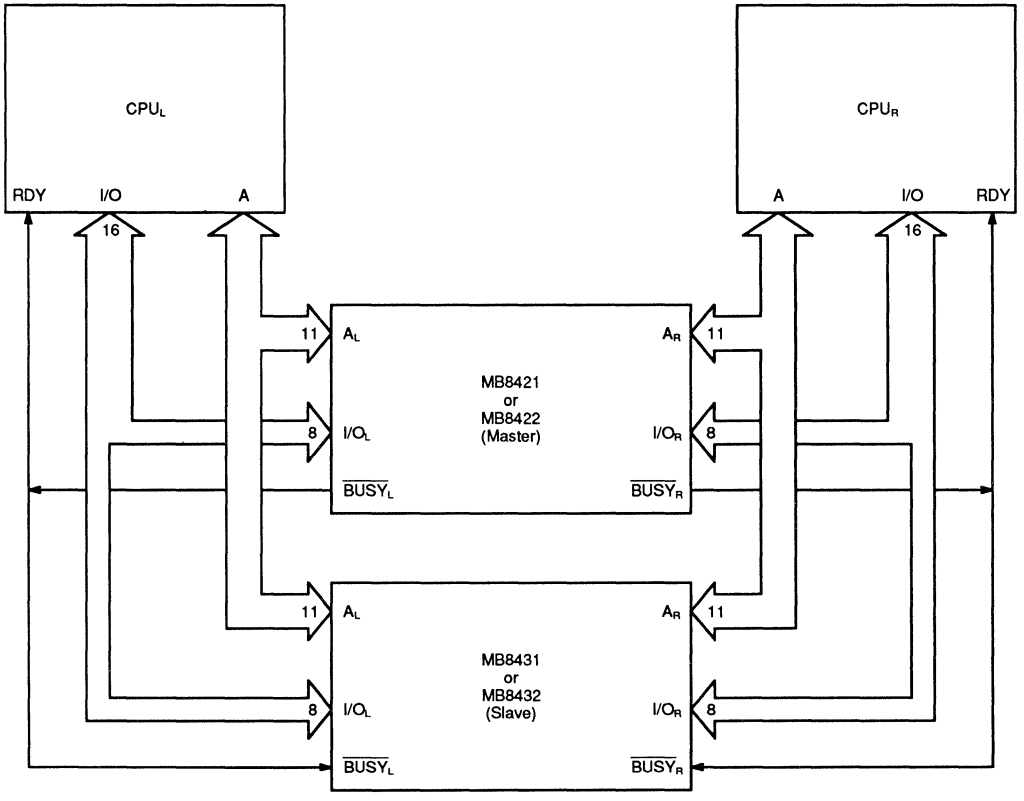


Function Description:

1. ORGANIZATION:
   MB8431/32 are 2K words x 8 bit Dual port Static Random Access Memory.
   Each port has independent addresses, chip select ($\overline{CS}$), write enable ($\overline{WE}$), output enable ($\overline{OE}$) and data input/output (I/O) functions.

2. SLAVE BUSY FUNCTION:
   In order to do bit expansion using 8 bit width dual port RAM such as MB8421/22, two or more parts should be connected paralel. But such case, there is a possibility, which depends on arbitration timing, of outputting $\overline{BUSY}$ signal to different ports and put both CPUs in waiting state. This causes a trouble. Using MB8431/32 which have slave busy function (busy input) is one of the solutaion for such trouble. Bit expansion is easily achievable to pair–use slave type dual port RAM such as MB8431/32 and master type dual port RAM such as MB8421/22.

(Example)
As an example, Fig1 shows 16 bit dual port memory system.
In this system, master type Dual port RAM (MB8421/22) judge arbitration for address contention and output result of the judgement from $\overline{BUSY}$ pin. This output returned to CPU and make the CPU in waiting state and also the output is applied to slave type dual port RAM (MB8431/32). Though slave type dual port RAM (MB8431/32) do not judge for arbitration, they have $\overline{BUSY}$ input pin and inhibit write operation of the correspondent port during "L" signal form $\overline{BUSY}$ output of master type dual port RAM (MB8421/22) is applied to the $\overline{BUSY}$ input.
A system consists of one master dual port RAM (MB8421/22) and three slave dual port RAMs (MB8431/32) is harmonized for 32 bit application.



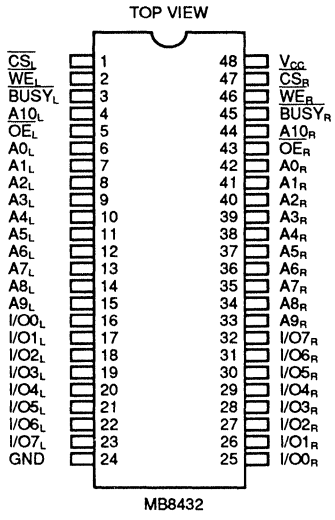
3. INTERRUPT FUNCTION:
The interrupt function ($\overline{INT}$) is provided to allow communication between the systems on either sides of the dual–port RAM. $\overline{INT}_L$ is set to low, when the processor on the right port writes to address 7FE (A0=L and A1 to A10=H). $\overline{INT}_L$ is then reset to High, when the left port acknowledges by reading the same address 7FE. Thus the address 7FE is like a 8 bit word mail–box transferring information from the right–port to the left–port.

$\overline{INT}_R$ on the other hand is set to low, when processor on the left port writes to the address 7FF (A=0 to A10=H). $\overline{INT}_R$ is reset to High, when the right port acknowledges by reading this address. Hence, the address 7FF is a second 8 bit word mail–box transferring information form the left port to the right port.

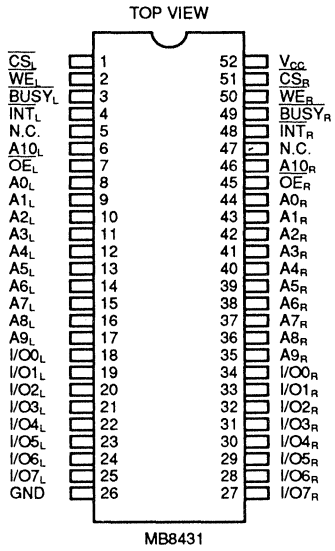
The $\overline{INT}_L$ and $\overline{INT}_R$ are set to High on power–up. If the port is in the standby mode, it can still get interrupted by the processor on the other side.

In case he $\overline{BUSY}$ flag is set to low, then the pertinent port can not set or reset the $\overline{INT}$ flag.

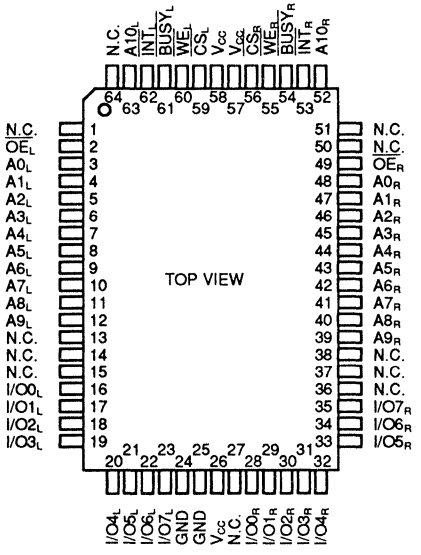
4



MB8432



MB8431

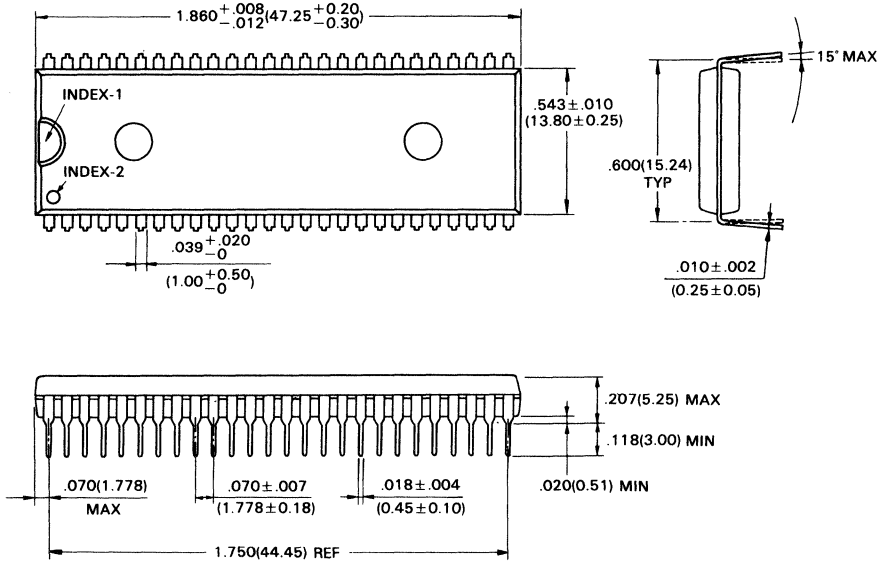


MB8431

4

52-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-52P-M01)

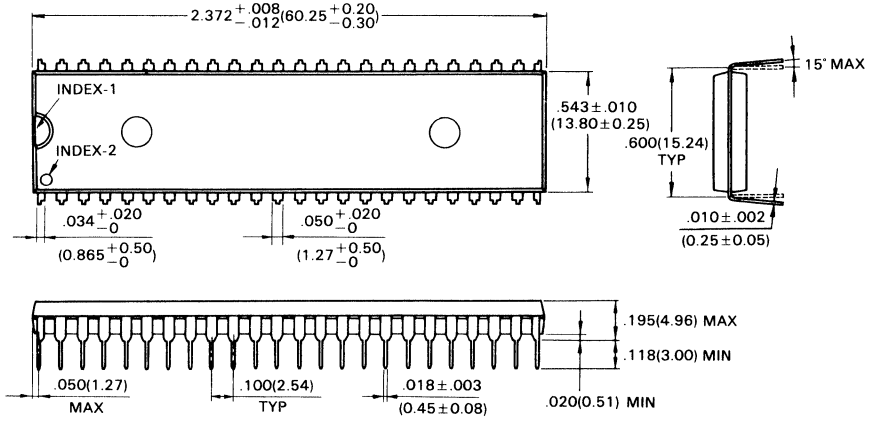


Dimensions in
inches (millimeters)

4

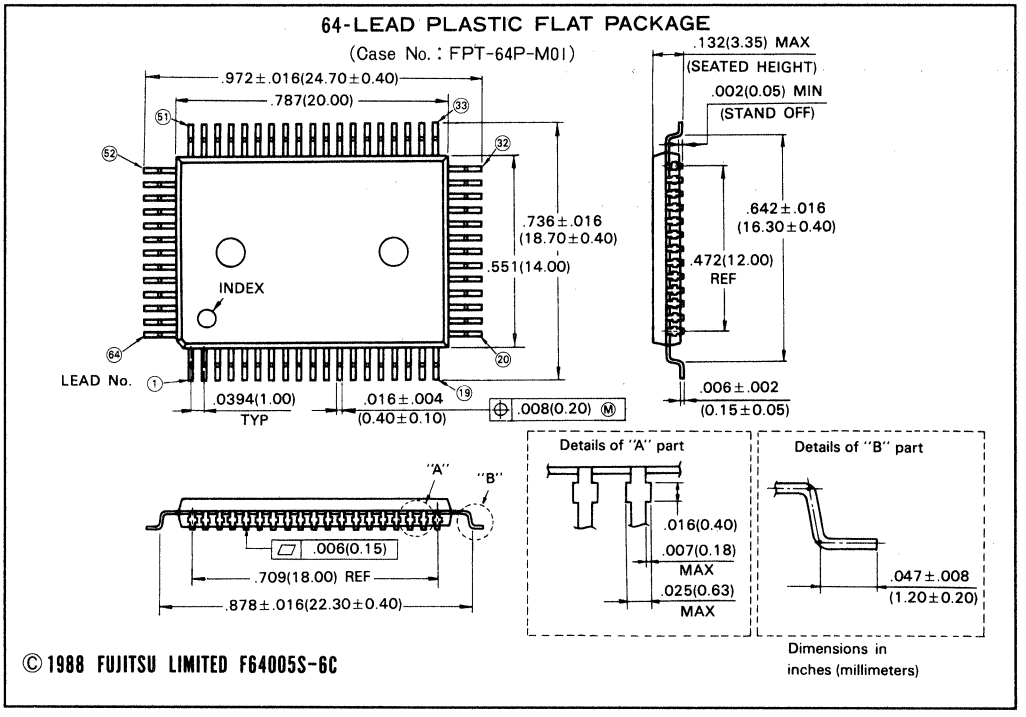
48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M02)



Dimensions in
inches (millimeters)

4



4

Section 5

Wide Temperature Range SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
5–3	MB81C68A–45W	45	16384 bits (4096w x 4b)	20-pin Ceramic DIP
5–11	MB81C78A–45W	45	65536 bits (8192w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC
5–23	MB81C79A–45W	45	73728 bits (8192w x 9b)	28-pin Ceramic DIP 32-pad Ceramic LCC
5–35	MB8464A–10W –15W	100 150	65536 bits (8192w x 8b)	28-pin Ceramic DIP 32-pad Ceramic LCC

5

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C68A–45–W
CMOS 16K–BIT HIGH SPEED SRAM

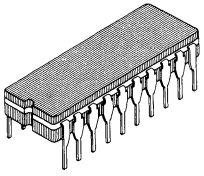
4096 WORDS x 4 BITS SRAM WITH HIGH SPEED AND AUTOMATIC POWER DOWN

The Fujitsu MB81C68A–W is 4096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR–tied, and furthermore on selecting a single package by $\overline{CS}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

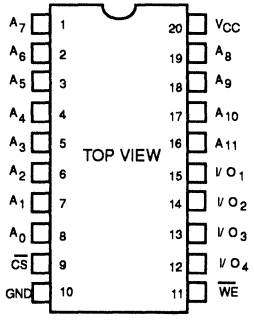
- Organization : 4096 words x 4 bits
- Static operation : No clocks or timing strobe required
- Fast acces time : $t_{AA} = t_{ACS} = 45$ns max.(MB81C68A–45–W)
- Low power consumption : 495mW max. (Operating)
  193mW max. (TTL standby)
  110mW max. (CMOS standby)
- Single + 5V supply ± 10% tolerance
- TTL compatible inputs and outputs
- Three–state outputs with OR–tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 20–pin DIP (Suffix : CZ)



CERAMIC PACKAGE
CERDIP
(DIP–20C–C03)

5

PIN ASSIGNMENT



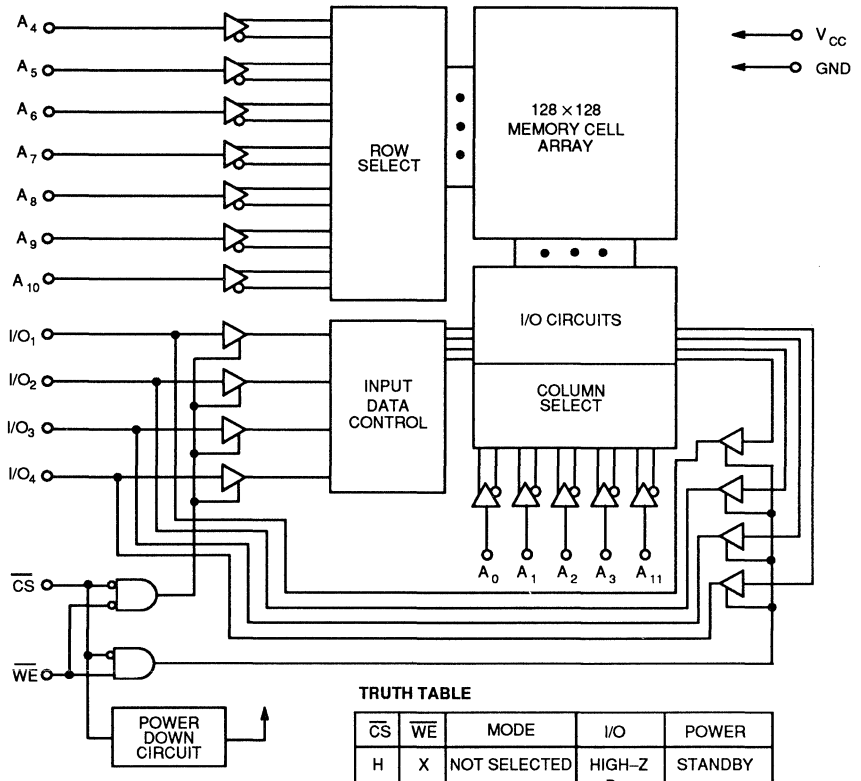
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 6.0	V
Input Voltage on Any Pin with respect to GND	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output Voltage on Any I/O Pin with respect to GND	V_{OUT}	–0.5 to V_{CC} + 0.5	V
Output current	I_{OUT}	± 20	mA
Power dissipation	P_D	1.0	W
Temperature under Bias	T_{BIAS}	–55 to 125	°C
Storage Temperature	T_{STG}	–65 to 150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 – MB81C68A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$		7	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

PIN DESCRIPTION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3 *1		0.6	V
Input High Voltage	V_{IH}	2.4		V_{CC} + 0.3	V
Ambient Temperature	T_A	−55		125	°C

Note : * −2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = −0.3V at DC level)

DC CHARACTERISTICS

(Recommended opereating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	−50		+50	µA
Active (DC) Supply Current	I_{OUT} = 0mA $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	70	mA
Operating Supply Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0mA, Cycle = Min	I_{CC2}		40	90	mA
Standby Supply Current	$\overline{CS}$ = V_{CC} −0.2V, $V_{IN} \leqq$ 0.2V or $V_{IN} \geqq V_{CC}$ −0.2V	I_{SB1}		0.5	20	mA
Standby Supply Current	$\overline{CS}$ = V_{IH}	I_{SB2}		10	35	mA
Output Low Voltage	I_{OL} = 8mA	V_{OL1}			0.4	V
Output Low Voltage	I_{OL} = 100 µA	V_{OL2}			0.2	V
Output High Voltage	I_{OH} = −4mA	V_{OH1}	2.4			V
Output High Voltage	I_{OH} = 100 µA	V_{OH2}	2.6			V

5

AC TEST CONDITION

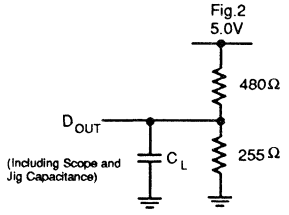


Fig.2

Input Pulse Levels: 0.4 to 2.6V
Input Pulse Rise and Fall Times: 5ns (Ttansient Time between 0.8V and 2.2V)
Timing Reference Levels: Input:1.5V
Output:1.5V

Output Load:

C_L = 30pF
C_L = 5pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE *1

Parameter	Symbol	MB81C68A-45-W		Unit
		Min	Max	
Read Cycle Time	t_{RC}	45		ns
Address Access Time*2	t_{AA}		45	ns
Chip Select Access Time*3	t_{ACS}		45	ns
Output Hold from Address Charge	t_{OH}	0		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		ns
Chip Selection to Output in Low-Z*4	t_{LZ}	0		ns
Chip Deselection to Output in High -Z*4	t_{HZ}	0	20	ns
Power Up from $\overline{CS}$	t_{PU}	0		ns
Power Down from $\overline{CS}$	t_{PD}		45	ns

Note: *1 $\overline{WE}$ is high for Read cycle.

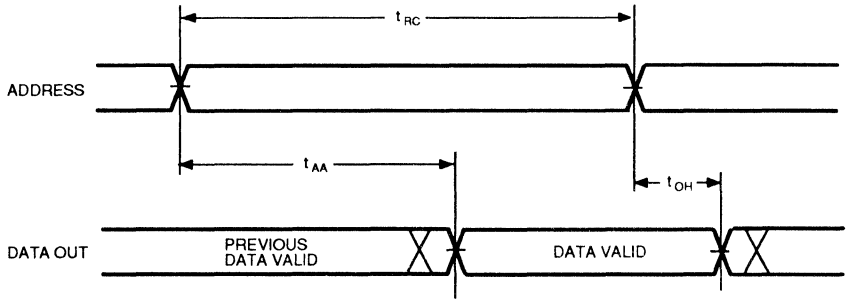
*2 Device is continuously selected, $\overline{CS}$ = V_{IL}

*3 Address valid prior to or coincident with $\overline{CS}$ transition low.

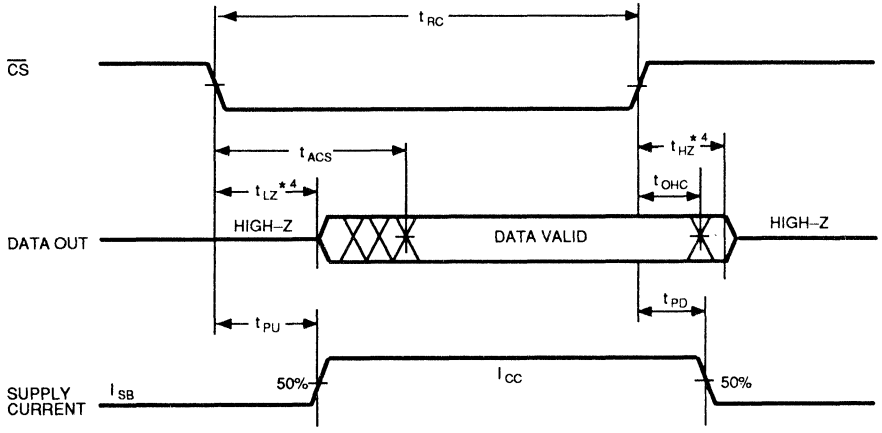
*4 Transition is specified at the point of ± 500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM *1

READ CYCLE: ADDRESS CONTROLLED *2



READ CYCLE: $\overline{CS}$ CONTROLLED *3



Note: * 1 $\overline{WE}$ is high for Read cycle.

* 2 Device is continuously selected, $\overline{CS} = V_{IL}$

* 3 Address valid prior to or coincident with $\overline{CS}$ transition low.

* 4 Transition is specified at the point of ± 500mV from steady state voltage.

WRITE CYCLE *1 *2

Parameter	Symbol	MB81C68A–45–W		Unit
		Min	Max	
Write Cycle Time	t_{WC}	45		ns
Chip Selection to End of Write	t_{CW}	35		ns
Address Valid to End of Write	t_{AW}	35		ns
Address Setup Time	t_{AS}	3		ns
Write Pulse Width	t_{WP}	35		ns
Data Setup Time	t_{DW}	25		ns
Write Recovery Time	t_{WR}	5		ns
Data Hold Time	t_{DH}	0		ns
Output High–Z from $\overline{WE}$ *3	t_{WZ}	0	20	ns
Output Low–Z from $\overline{WE}$ *3	t_{OW}	0		ns

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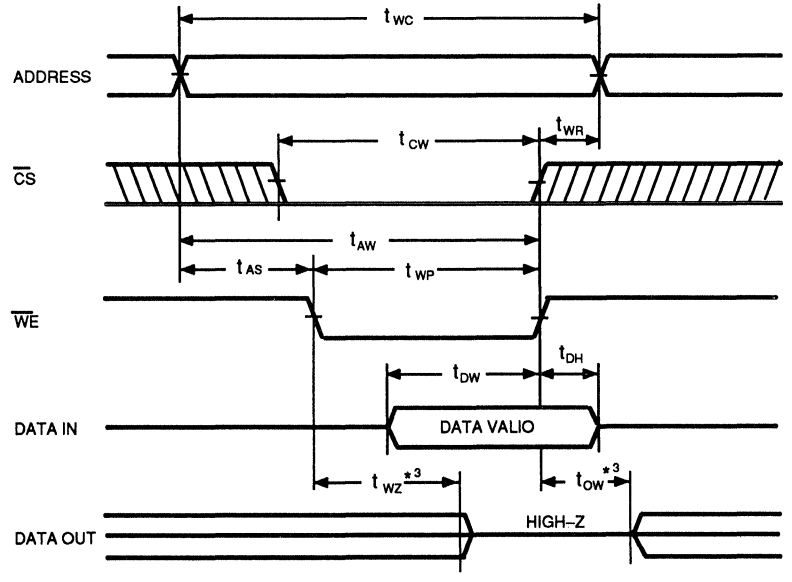
WRITE CYCLE TIMMING DIAGRAM

WRITE CYCLE: $\overline{WE}$ CONTROLLED*1 *2



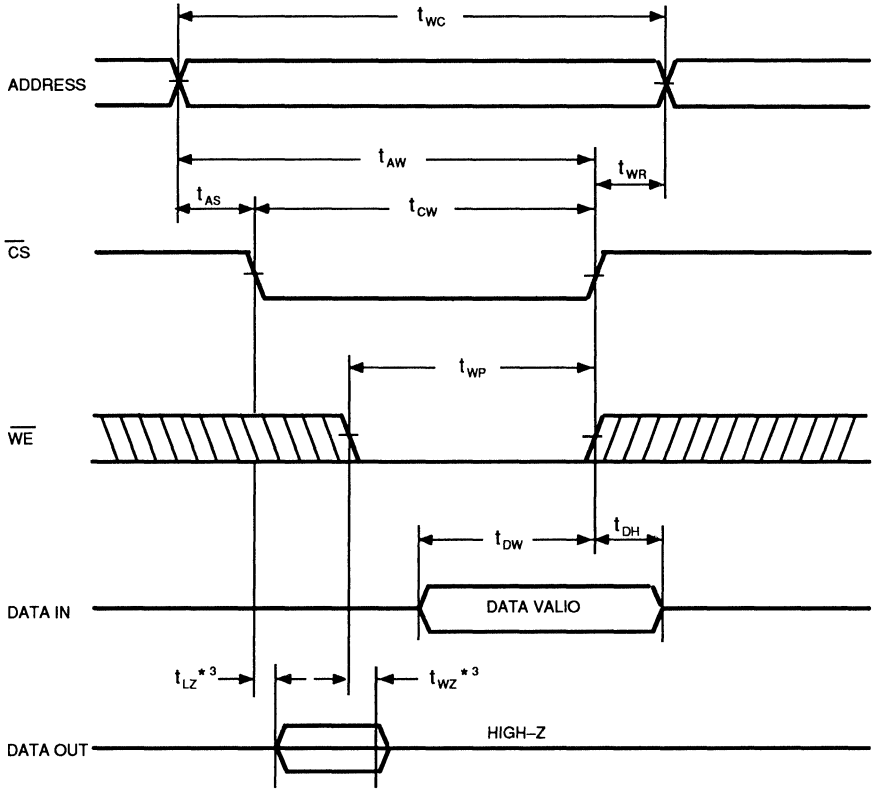
Notes : * 1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

* 2 If $\overline{CS}$ goes simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

* 3 Transition is specified at the point of ± 500mV from steady state voltage.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



Notes : * 1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

* 2 If $\overline{CS}$ goes high simulyaneously with $\overline{WE}$ high, the output remains in a high impedance state.

* 3 Transition is specified at the point of ±500mV from steady state voltage.

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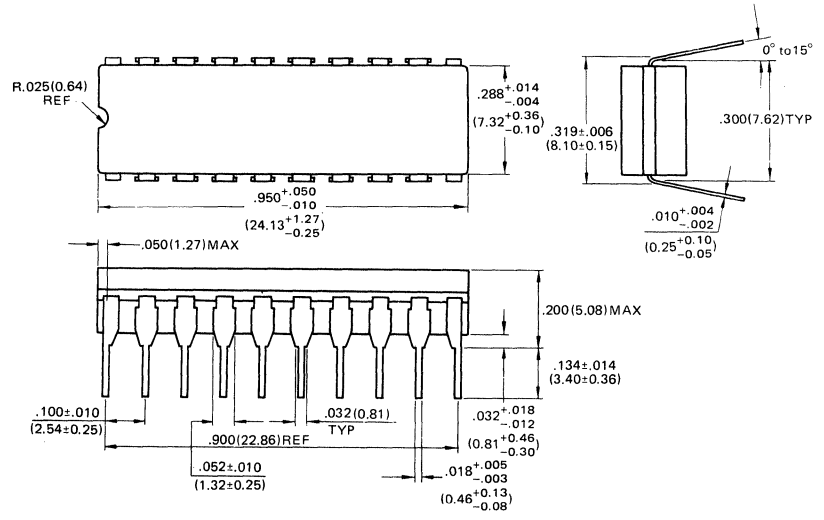
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: DIP-20C-C03)



Dimensions in
inches (millimeters)

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FUJITSU

CMOS 65536-BIT STATIC RANDOM ACCESS MEMORY

MB81C78A-45-W

September 1988
Edition 1.0

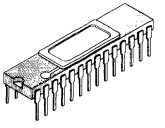
64K-BIT (8192x8) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB81C78A-W is 8192 words x 8bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

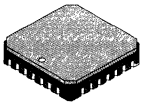
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 8192 words x 8 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 45 ns max. (MB81C78A-45-W)
- Low power consumption: 660 mW max. (Operating)
  165 mW max. (Standby, TTL level)
  110 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Ceramic DIP package (Suffix: -C)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



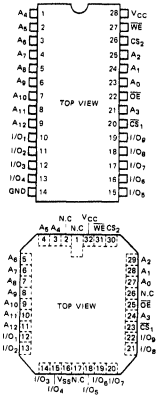
CERAMIC PACKAGE
DIP-28C-A08



CERAMIC PACKAGE
LCC-32C-A02

5

PIN ASSIGNMENT



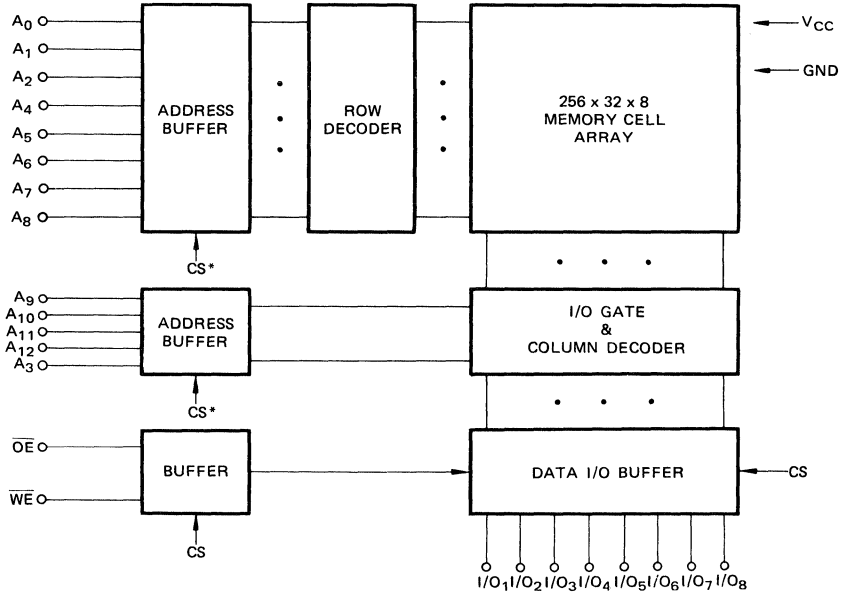
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	-0.5 to +7	V
Output Voltage on any I/O with respect to GND	V_{OUT}	-0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	-65 to +135	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 81C78A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS}_1$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5		0.4	V
Input High Voltage	V_{IH}	2.6		6.0	V
Ambient Temperature	T_A	-55		125	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		120	mA	$\overline{CS_1}$ = V_{IL} I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		20	mA	V_{CC} = Min to Max. $\overline{CS_1}$ = V_{CC}-0.2V $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		30	mA	$\overline{CS_1}$ = V_{IH}
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

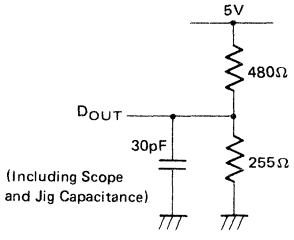
AC TEST CONDITIONS

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.4V and 2.6V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

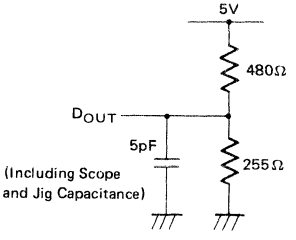
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



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AC CHARACTERISTICS

READ CYCLE*1

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C78A-45-W		Unit
		Min	Max	
Read Cycle Time	t_{RC}	45		ns
Address Access Time*2	t_{AA}		45	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		45	ns
CS_2 Access Time*3	t_{ACS2}		20	ns
Output Hold from Address Change	t_{OH}	3		ns
$\overline{OE}$ Access Time	t_{OE}		20	ns
Output Active from $\overline{CS_1}$ *4*5	t_{LZ1}	5		ns
Output Active from CS_2 *4*5	t_{LZ2}	0		ns
Output Active from $\overline{OE}$ *4*5	t_{OLZ}	0		ns
Output Disable from $\overline{CS_1}$ *4*5	t_{HZ1}		25	ns
Output Disable from CS_2 *4*5	t_{HZ2}		25	ns
Output Disable from $\overline{OE}$ *4*5	t_{OHZ}		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with CS_1 transition low, CS_2 transition high.
*4 Transistion is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

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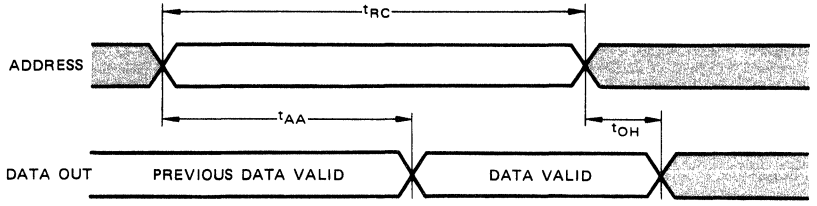
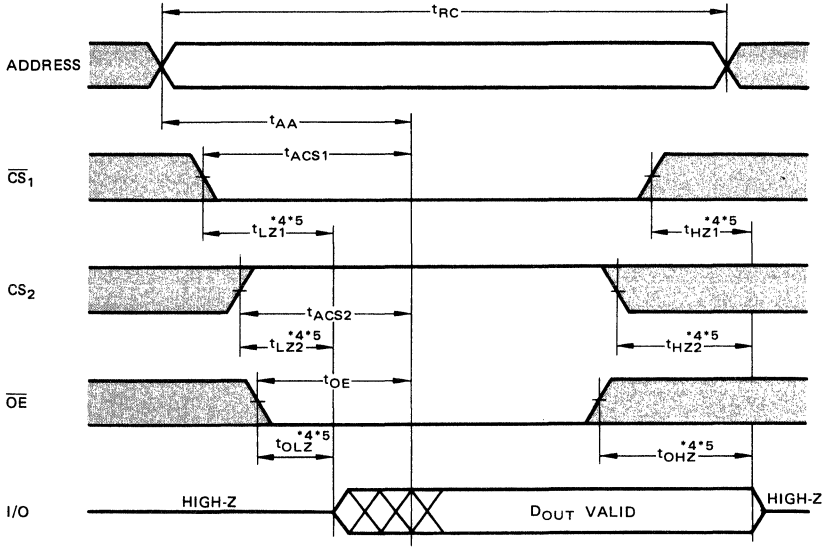
READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE[*1]

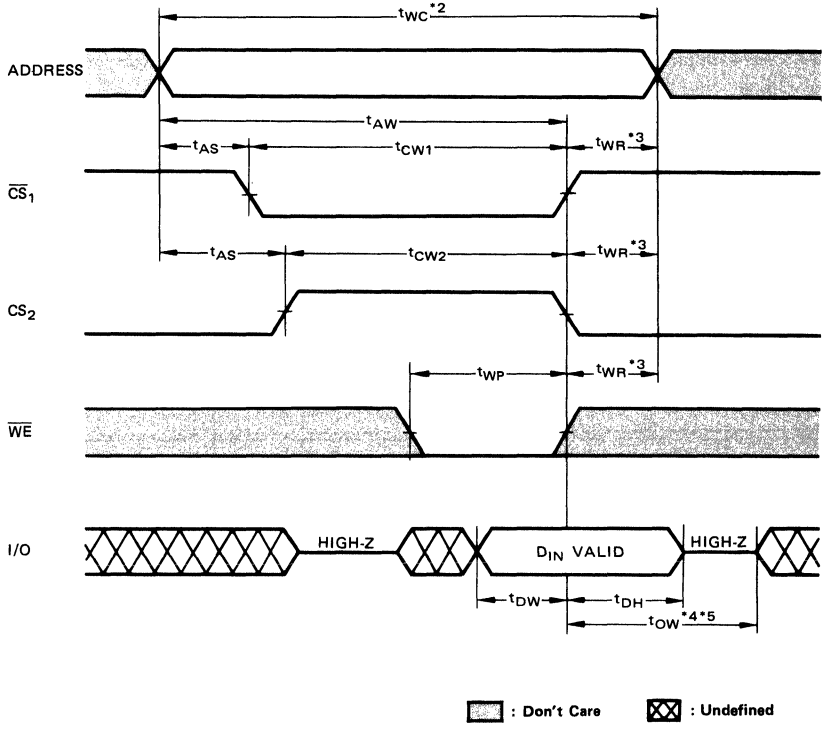
Parameter	Symbol	MB81C78A-45-W		Unit
		Min	Max	
Wirte Cycle Time[*2]	t_{WC}	45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	40		ns
CS_2 to End of Write	t_{CW2}	25		ns
Address Valid to End of Write	t_{AW}	40		ns
Address Setup Time	t_{AS}	2		ns
Write Pulse Width	t_{WP}	25		ns
Data Setup Time	t_{DW}	20		ns
Write Recovery Time[*3]	t_{WR}	3		ns
Data Hold Time	t_{DH}	3		ns
Output High-Z from $\overline{WE}$[*4 *5]	t_{WZ}		20	ns
Output Low-Z from $\overline{WE}$[*4 *5]	t_{OW}	0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM*1

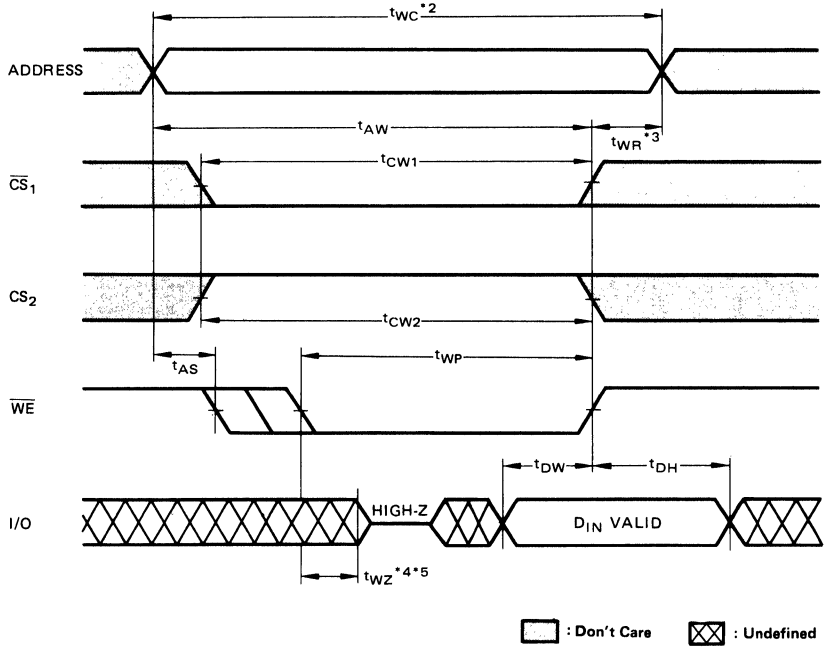
WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

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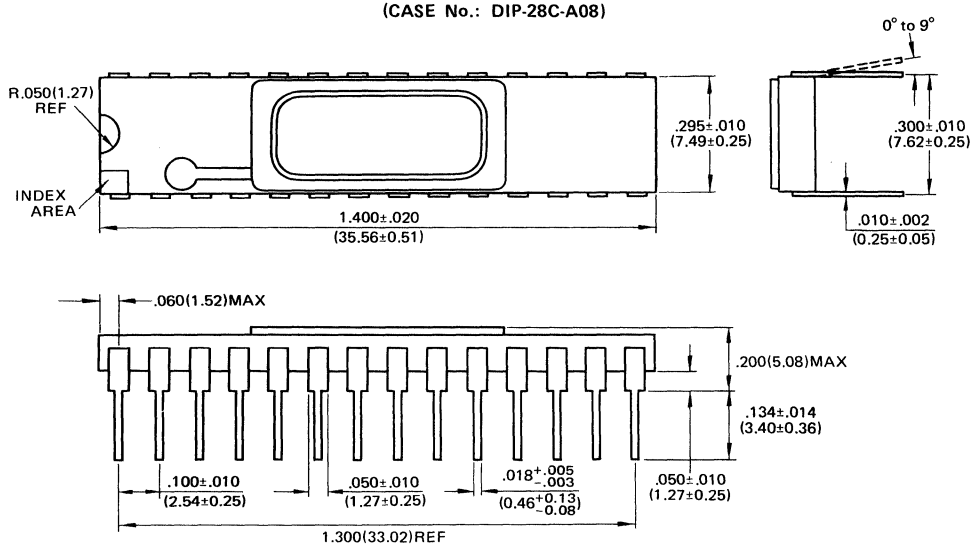
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A08)



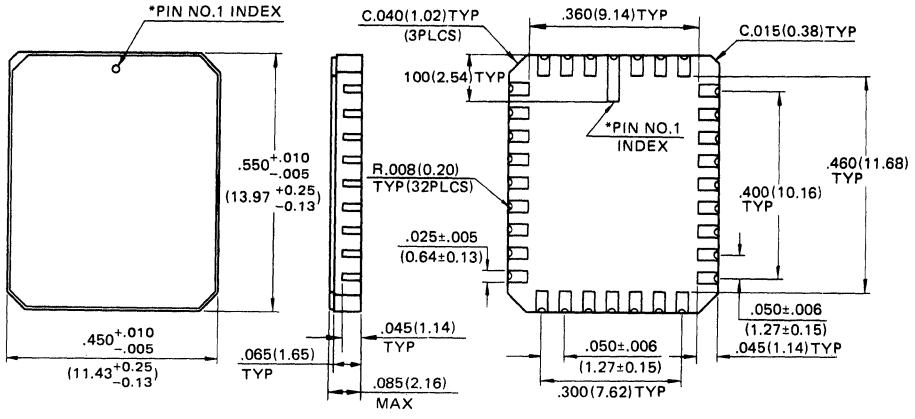
Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (continued)

CERAMIC LCC (Suffix: -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

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FUJITSU

CMOS 73728-BIT STATIC RANDOM ACCESS MEMORY

MB81C79A-45-W

September 1988
Edition 1.0

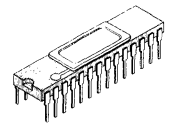
72K-BIT (8192x9) HIGH SPEED CMOS STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB81C79A-W is 8192 words x 9bits static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single 5 volts power supply is required.

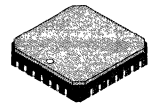
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{CS_1}$, the other deselected packages automatically power down.

All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 8192 words x 9 bits
- Static operation: No clock or timing strobe required
- Fast access time: $t_{AA} = t_{ACS1}$ = 45 ns max. (MB81C79A-45-W)
- Low power consumption: 660 mW max. (Operating)
  165 mW max. (Standby, TTL level)
  110 mW max. (Standby, CMOS level)
- Single +5V supply, ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 28-pin Ceramic DIP package (Suffix: -C)
- Standard 32-pad Leadless Chip Carrier (Suffix: -CV)



CERAMIC PACKAGE
DIP-28C-A08



CERAMIC PACKAGE
LCC-32C-A02

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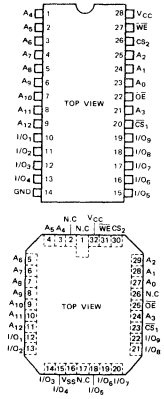
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	-0.5 to +7	V
Output Voltage on any I/O with respect to GND	V_{OUT}	-0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	-65 to +135	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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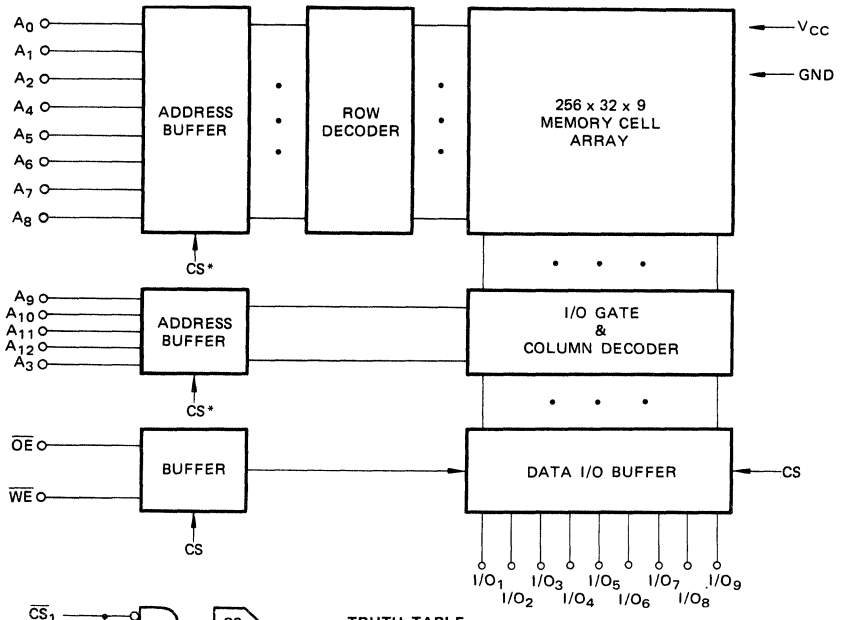
Fig. 1 – MB 81C79A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN} = 0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.5		0.4	V
Input High Voltage	V_{IH}	2.6		6.0	V
Ambient Temperature	T_A	-55		+125	°C

* -2.0V Min. for pulse width less than 20 ns. (V_{IL} Min = -0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	-10	10	μA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}
Operating Supply Current	I_{CC}		120	mA	$\overline{CS_1}$ = V_{IL} I/O = Open, Cycle = Min
Standby Supply Current	I_{SB1}		20	mA	V_{CC} = Min to Max. $\overline{CS_1}$ = V_{CC}-0.2V $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
	I_{SB2}		30	mA	$\overline{CS_1}$ = V_{IH}
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC} = 0V to V_{CC} Min. $\overline{CS_1}$ = Lower of V_{CC} or V_{IH} Min.

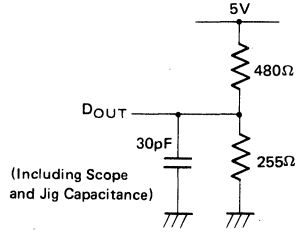
AC TEST CONDITIONS

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise And Fall Times:	5ns (Transient time between0.4V and 2.6V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

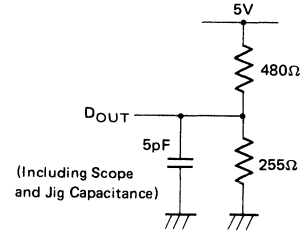
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



5

AC CHARACTERISTICS

READ CYCLE[*1] **(Recommended operating conditions unless otherwise noted.)**

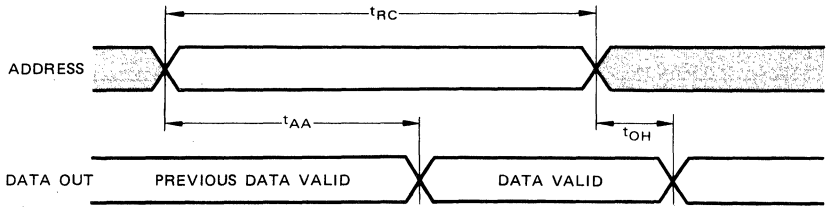
Parameter	Symbol	MB81C79A-45-W		Unit
		Min	Max	
Read Cycle Time	t_{RC}	45		ns
Address Access Time[*2]	t_{AA}		45	ns
$\overline{CS_1}$ Access Time[*3]	t_{ACS1}		45	ns
CS_2 Access Time[*3]	t_{ACS2}		20	ns
Output Hold from Address Change	t_{OH}	3		ns
$\overline{OE}$ Access Time	t_{OE}		20	ns
Output Active from $\overline{CS_1}$[*4*5]	t_{LZ1}	5		ns
Output Active from CS_2[*4*5]	t_{LZ2}	0		ns
Output Active from $\overline{OE}$[*4*5]	t_{OLZ}	0		ns
Output Disable from $\overline{CS_1}$[*4*5]	t_{HZ1}		25	ns
Output Disable from CS_2[*4*5]	t_{HZ2}		25	ns
Output Disable from $\overline{OE}$[*4*5]	t_{OHZ}		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with CS_1 transition low, CS_2 transition high.
*4 Transistion is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

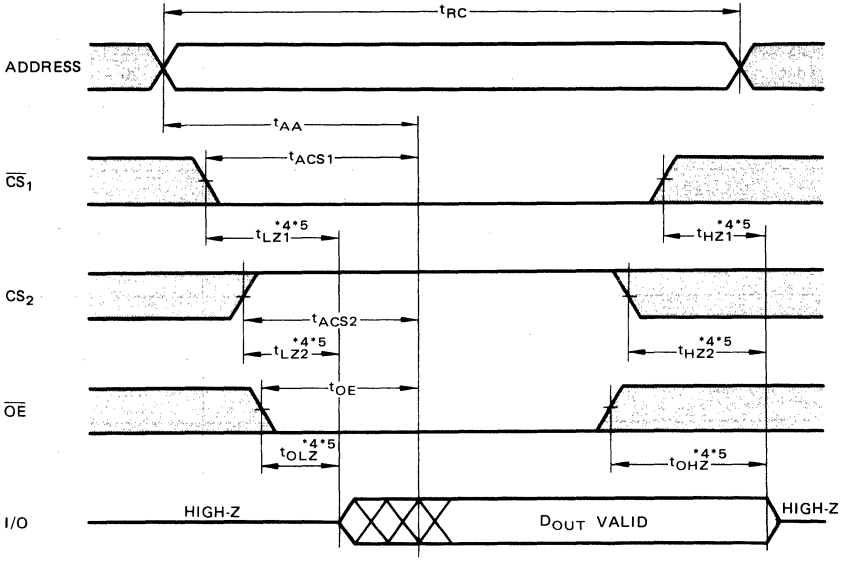
5

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



: Don't Care : Undefined

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE*1

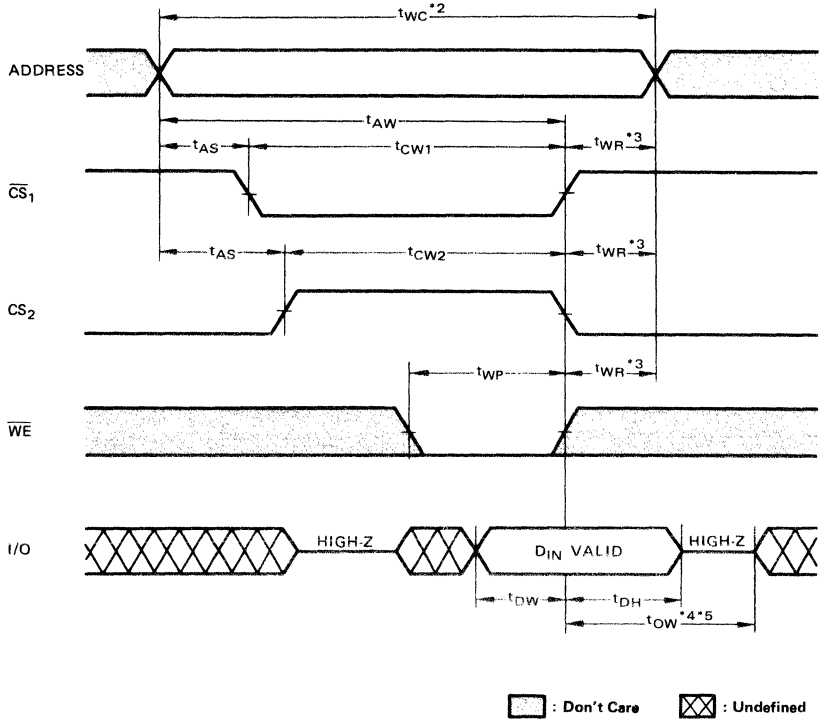
Parameter	Symbol	MB81C79A-45-W		Unit
		Min	Max	
Wirte Cycle Time*2	t_{WC}	45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	40		ns
CS_2 to End of Write	t_{CW2}	25		ns
Address Valid to End of Write	t_{AW}	40		ns
Address Setup Time	t_{AS}	2		ns
Write Pulse Width	t_{WP}	25		ns
Data Setup Time	t_{DW}	20		ns
Write Recovery Time*3	t_{WR}	3		ns
Data Hold Time	t_{DH}	3		ns
Output High-Z from $\overline{WE}$*4*5	t_{WZ}		20	ns
Output Low-Z from $\overline{WE}$*4*5	t_{OW}	0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM*1

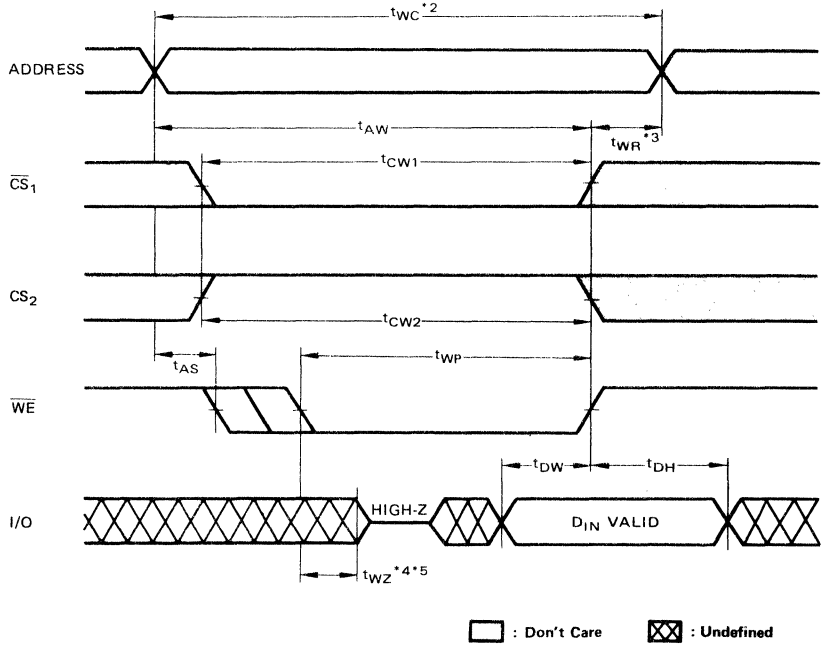
WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

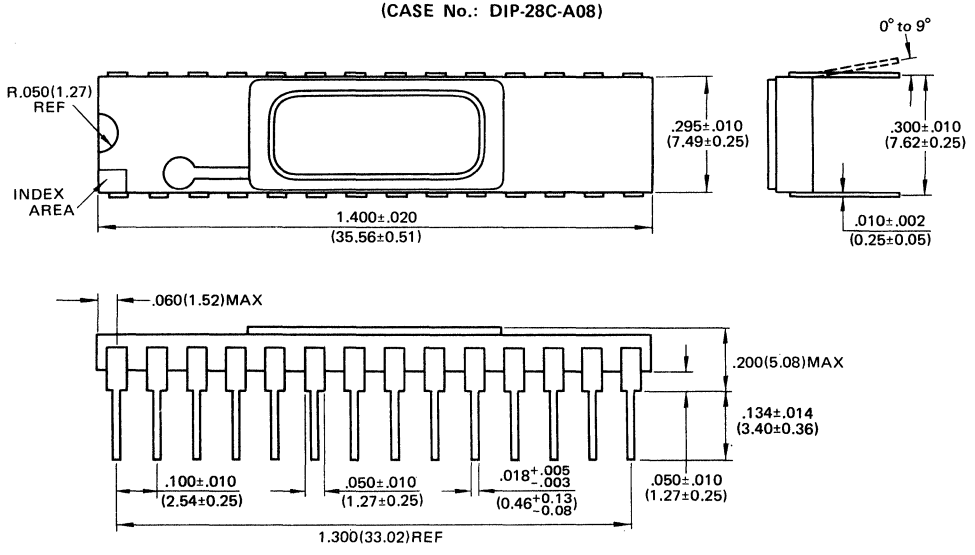
WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of WRITE Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A08)



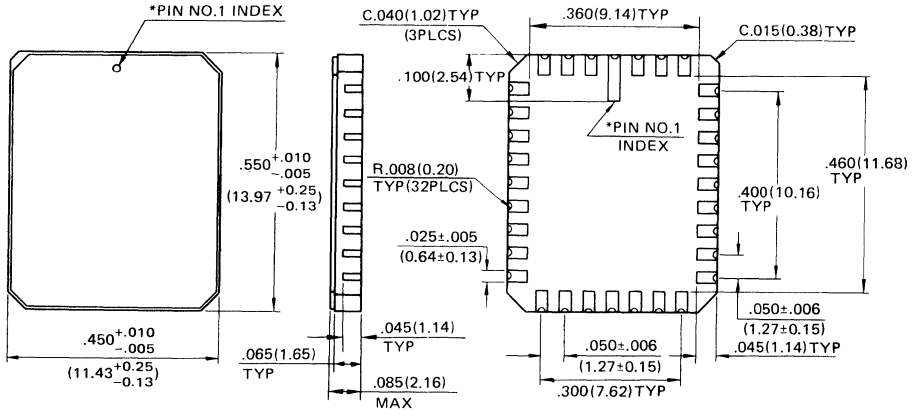
Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (continued)

CERAMIC LCC (Suffix: -CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches
(millimeters)

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October 1989
Edition 1.0

FUJITSU

DATA SHEET

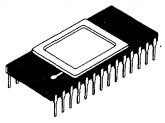
MB8464A-10-W/-15-W
CMOS 64K-BIT LOW POWER SRAM

8,192WORDS x 8BIT CMOS STATIC RAM WITH LOW POWER AND DATA RETENTION

The Fujitsu MB8464A is a 8192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5volts power supply is required.

The MB8464A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Organization: 8192 words x 8 bits
- Fast access time: 100ns max. (MB8464A-10-W)
  150ns max. (MB8464A-15-W)
- Completely static operation: No clock required
- TTL compatible input/output
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 11mW max.
- Data retention: 2.0V min.
- 28-pin Ceramic package (300mil width)
  (600mil width)
- 32-pad Leadless Chip Carrier



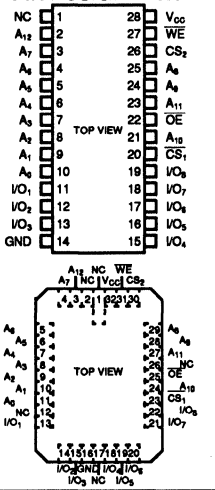
Ceramic Package (600mil)
DIP-28C-A07

Ceramic Package (300mil)
DIP-28C-A08

Ceramic Package
LCC-32C-A02

5

PIN ASSIGNMENT



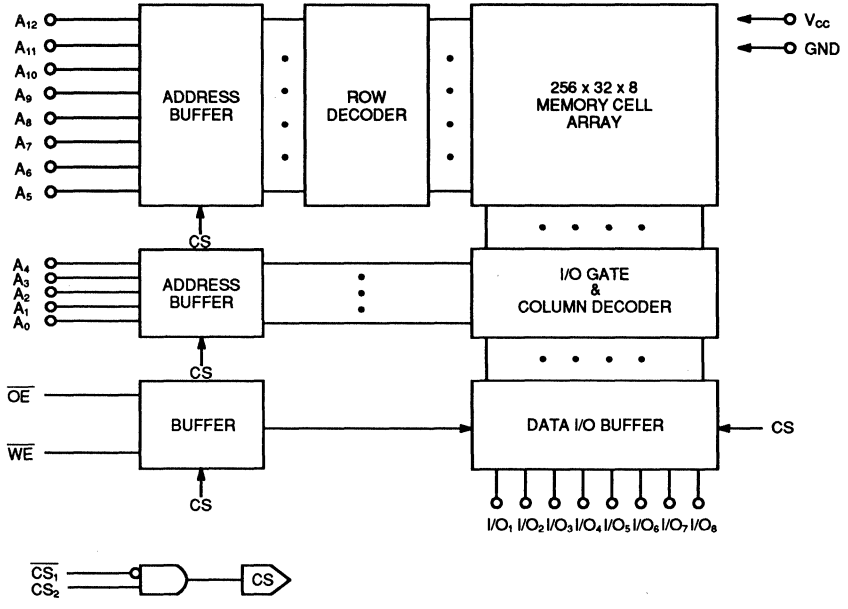
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Storage Temperature Range	T_{STG}	−65 to +150	°C
Temperature Under Bias	T_{BIAS}	−55 to +125	°C
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	T_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB8464A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH–Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH–Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH–Z
L	H	L	H	READ	I_{CC}	D_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}

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CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			10	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3 *1		0.6	V
Input High Voltage	V_{IH}	2.4		V_{CC}+0.3	V
Ambient Temperature	T_A	−55		+125	°C

*1 −3.0V min. for pulse width less than 20ns. (V_{IL} min.=−0.3V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-10-W/15-W		Unit	Test Condition
		Min	Max		
Standby Supply Current	I_{SB1}		2	mA	CS2≤0.2V, $\overline{CS1}$≥V_{CC}−0.2V (CS2≤0.2V or CS2≥V_{CC}−0.2V)
	I_{SB2}		5	mA	$\overline{CS1}$=V_{IH} or CS2=V_{IL}
Active Supply Current	I_{CC1}		70	mA	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA
Operating Supply Current	I_{CC2}		90	mA	Cycle=Min., Duty=100%, I_{OUT}=0mA
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	−50	50	µA	$V_{I/O}$=0V to V_{CC} $\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}
Output Hligh voltage	V_{OH}	2.4		V	I_{OH}=−1.0mA
Output Low voltage	V_{OL}		0.4	V	I_{OL}=2.1mA

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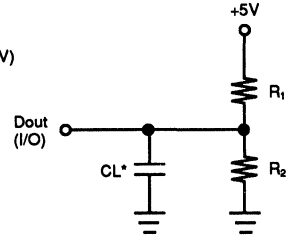
Fig. 2 — AC TEST CONDITIONS

- Input Pulse Levels: : 0.4V to 2.6V
- Input Pulse Rise and Fall Times: : 5ns (Transition Time between 0.6V and 2.4V)
- Timing Reference Levels: : Input: V_{IL}=0.6V, V_{IH}=2.4V
  Output: V_{OL}=0.8V, V_{OH}=2.0V
- Output Load:

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990KΩ	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990KΩ	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

< Output Load >



* Including jig and stray capacitance

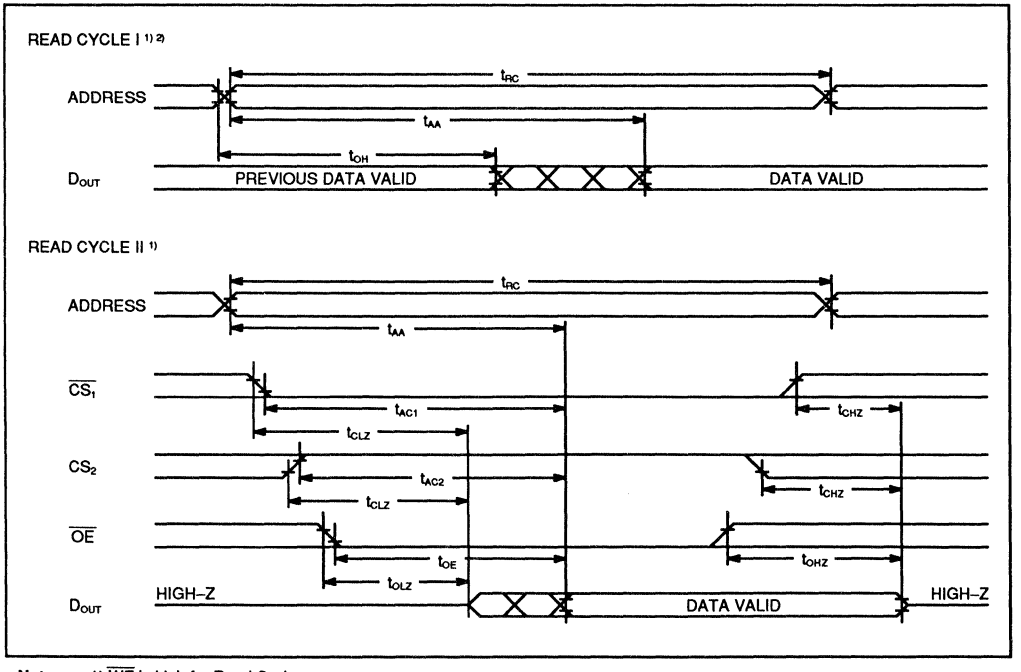
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)
READ CYCLE

Parameter	Symbol	MB8464A-10-W		MB8464A-15-W	
		Min	Max	Min	Max
Read Cycle Time	t_{RC}	100		150	
Address Access Time	t_{AA}		100		150
CS1 Access Time	t_{AC1}		100		150
CS2 Access Time	t_{AC2}		100		150
Output Enable to Output Valid	t_{OE}		45		60
Output Hold from Address Change	t_{OH}	10		10	
Chip Select to Output Low-Z *1	t_{CLZ}	10		10	
Output Enable to Output Low-Z *1	t_{OLZ}	5		5	
Chip Select to Output High-Z *1	t_{CHZ}		40		50
Output Enable to Output High-Z *1	t_{OHZ}		40		50

*1 Transition is measured at the point of ±500mV from stady state voltage.

READ CYCLE TIMING DIAGRAM



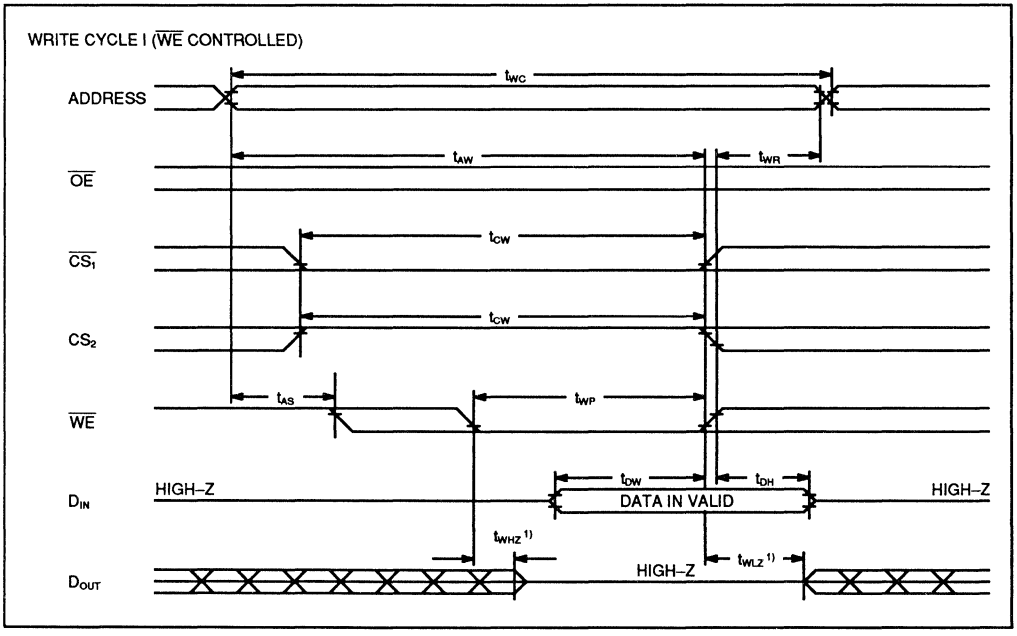
Note: 1) $\overline{WE}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.

WRITE CYCLE

Parameter	Symbol	MB8464A–10–W		MB8464A–15–W	
		Min	Max	Min	Max
Write Cycle Time	t_{WC}	100		150	
Address Valid to End of Write	t_{AW}	80		100	
Chip Select to End of Write	t_{CW}	80		100	
Data Valid to End of Write	t_{DW}	40		50	
Data Hold Time	t_{DH}	5		5	
Write Pulse Width	t_{WP}	80		100	
Address Set Up Time	t_{AS}	0		0	
Write Recovery Time	t_{WR}	10		10	
Write Enable to Output Low–Z *1	t_{WLZ}	5		5	
Write Enable to Output High–Z *1	t_{WHZ}		40		50

*1 Transition is measured at the point of ±500mV from stady state voltage.

WRITE CYCLE TIMING DIAGRAM



Note: 1) If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

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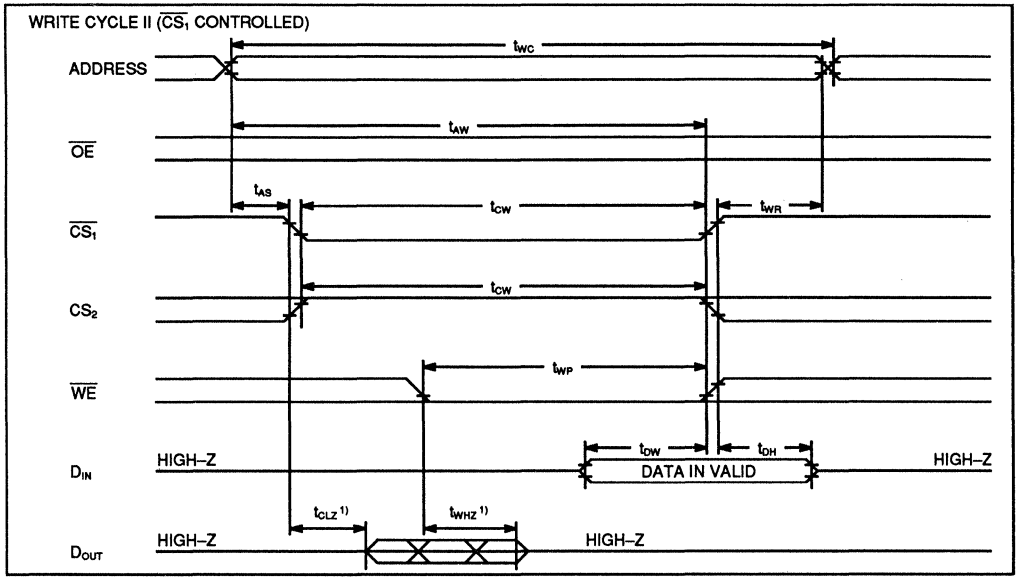
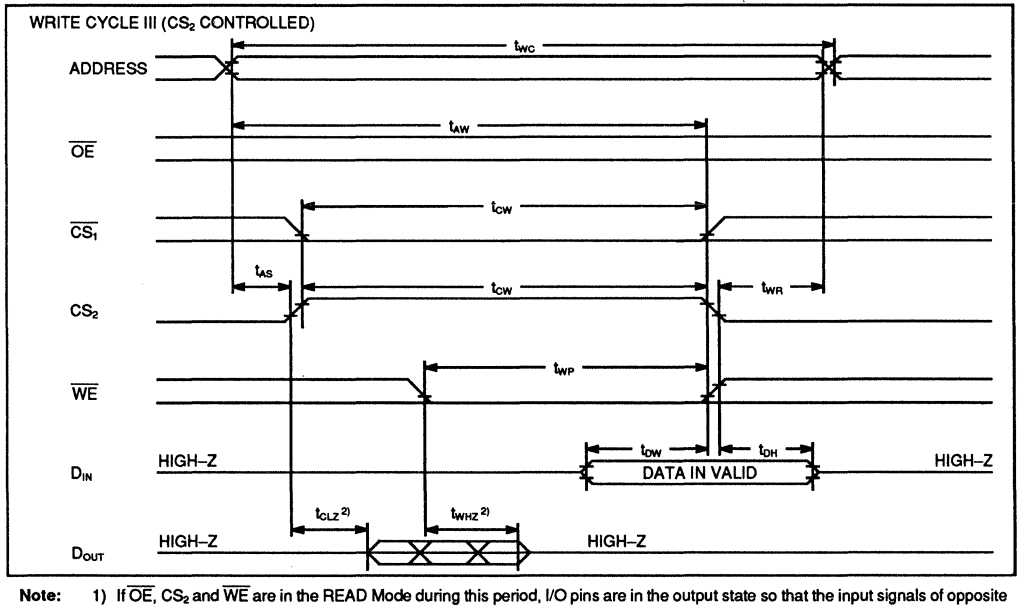
WRITE CYCLE II ($\overline{CS_1}$ CONTROLLED)



WRITE CYCLE III (CS_2 CONTROLLED)



Note: 1) If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

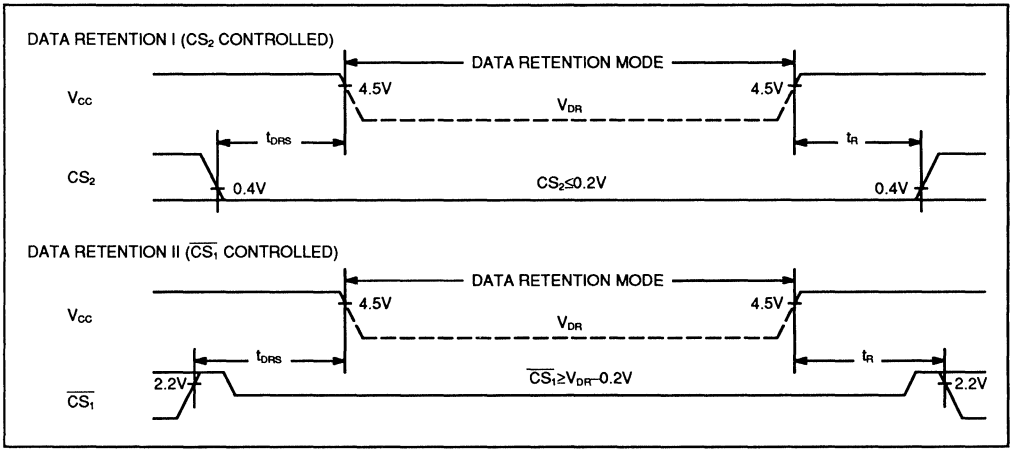
2) If $\overline{OE}$, $\overline{CS_1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max
Data Retention Supply Voltage *1	V_{DR}	2.0	5.5	V
Data Retention Supply Current *2	I_{DR}		0.5	mA
Data Retention Setup Time	t_{DRS}	0		ns
Operation Recovery Time	t_R	tRC		ns

DATA RETENTION TIMING



Note: *1 CS_2 controlled: $CS_2 \leq 0.2V$
$\overline{CS_1}$ controlled: $\overline{CS_1} \geq V_{DR} - 0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{DR} - 0.2V$)
*2 CS_2 controlled: $V_{DR} = 3.0V$, $CS_2 \leq 0.2V$
$\overline{CS_1}$ controlled: $V_{DR} = 3.0V$, $\overline{CS_1} \geq V_{DR} - 0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{DR} - 0.2V$)

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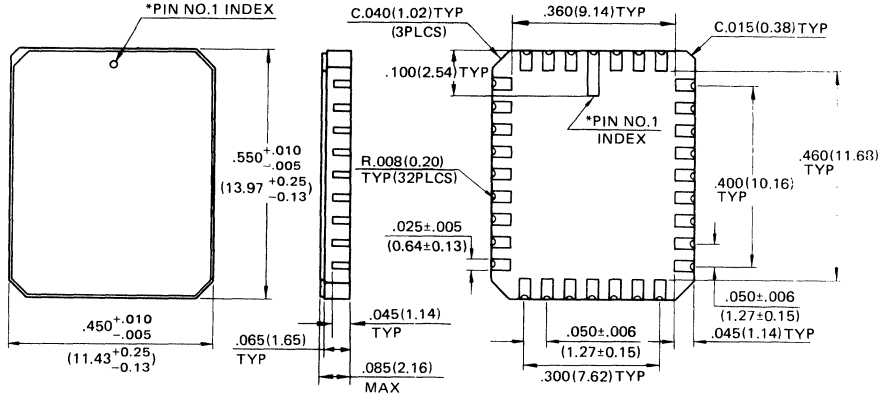
PACKAGE DIMENSIONS

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



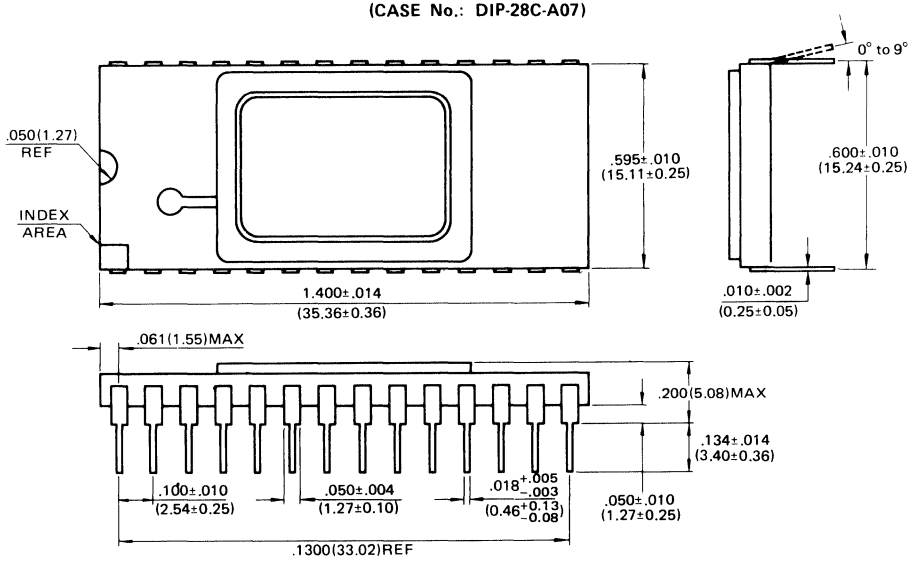
Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

5

PACKAGE DIMENSIONS (Continued)

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A07)

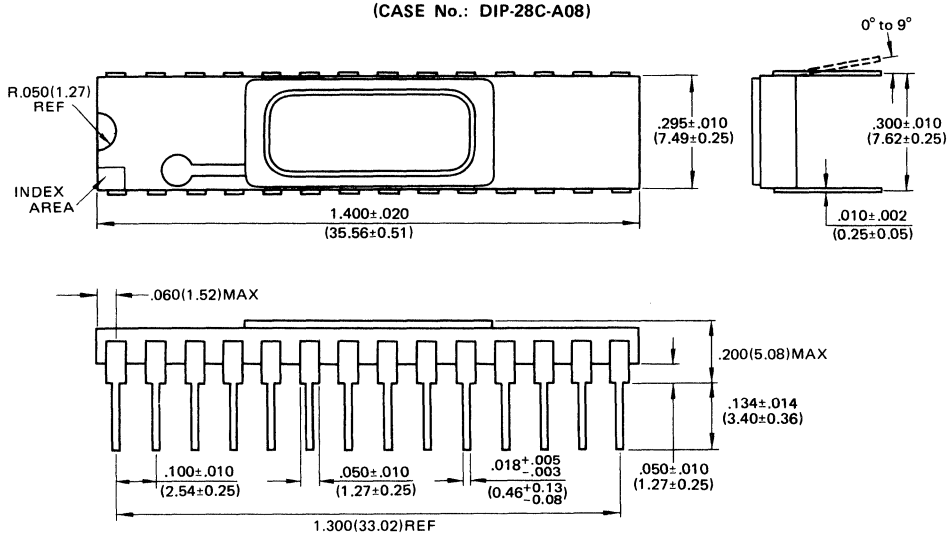


Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (Continued)

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A08)



Dimensions in inches (millimeters)

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Section 6

CMOS SRAM Modules — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
6–3	MB85402–30 –40	30 40	262144 bits (16384w x 16b)	36-pin Ceramic SIP
6–11	MB85403A–40 –50	40 50	2097152 bits (262144w x 8b)	44-pin Ceramic SIP
6–19	MB85410–30 –40	30 40	524288 bits (65536w x 8b)	60-pin Plastic ZIP
6–27	MB85414–30 –40	30 40	524288 bits (16384w x 32b) or (32768w x 16b)	64-pin Plastic ZIP
6–35	MB85420–40 –50	40 50	2097152 bits (262144w x 8b)	60-pin Plastic ZIP

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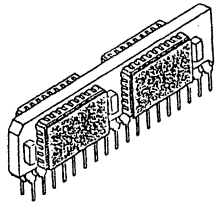
TS255-B88Y
Nov. 1988

CMOS 16,384 Words x 16-Bit STATIC RANDOM ACCESS MEMORY MODULE

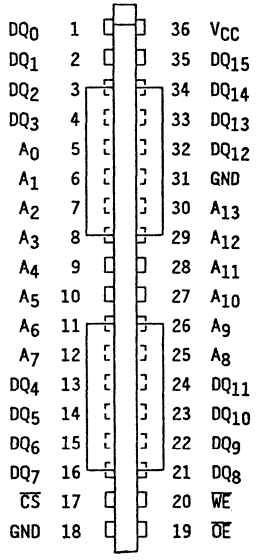
The Fujitsu MB85402 is a fully decoded, CMOS Static random access memory module comprised of four MB81C75 devices mounted on a 36-pin ceramic board. Organized as four 16K x 4 devices, the MB85402 is optimized for those applications requiring high speed, high performance, low power and high density.
A separate output enable function provides maximum control for those systems where bus contention may be a problem.

- Organized as 16,384 x 16-bit Words
- Memory : MB81C75, 4 pcs
- Access Time : 30 ns max (MB85402-30)
  40 ns max (MB85402-40)
- Low Power Dissipation
  Standby: 220 mW max (CMOS level)
  440 mW max (TTL level)
  Active : 1760 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- TTL Compatible Input/Output Pins
- 3-State Output
- 36-Pin 100 MIL Ceramic DIP/SIP



CERAMIC PACKAGE
MTP-36C-C01

PIN ASSIGNMENT
TOP VIEW



ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	4.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 – BLOCK DIAGRAM

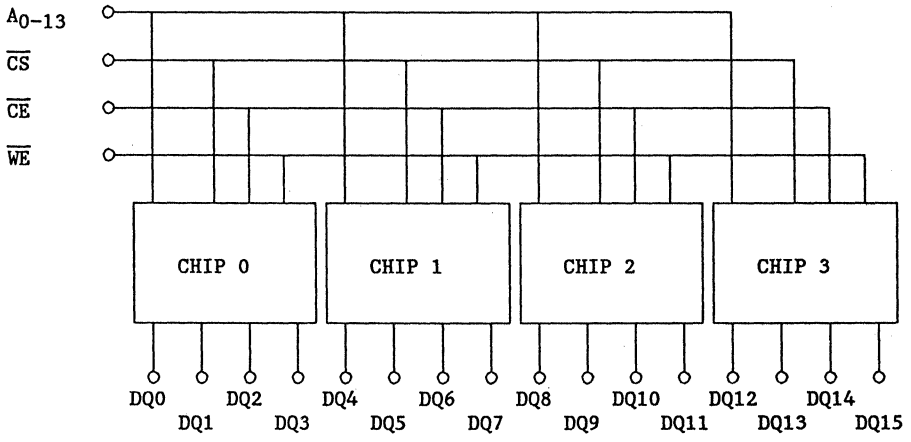
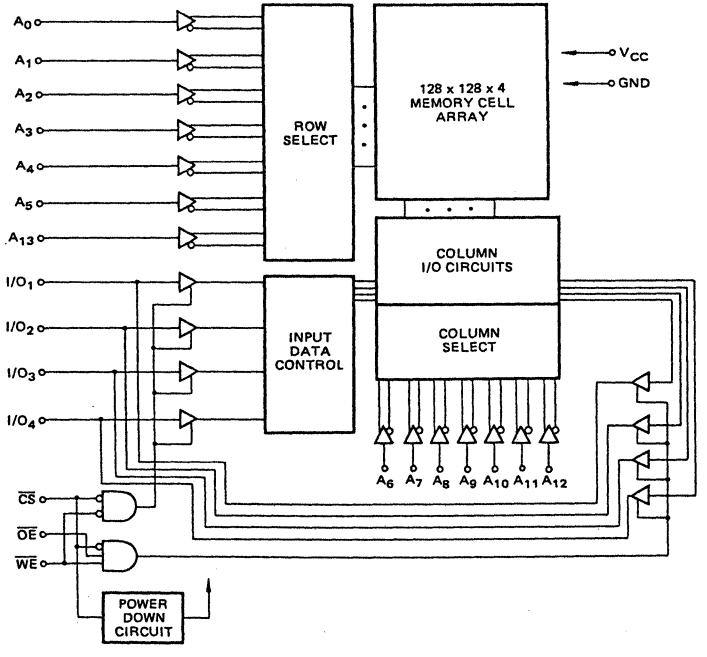


Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



6

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input1Capacitance (V_{IN}=0V)	C_{IN}		50	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		15	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
STANDBY	DON'T CARE	V_{IH}	DON'T CARE	DON'T CARE	HIGH-Z	STANDBY
READ	VALID	V_{IL}	V_{IH}	V_{IL}	D_{OUT}	ACTIVE
OUTPUT DESABLE	VALID	V_{IL}	V_{IH}	V_{IH}	HIGH-Z	ACTIVE
WRITE	VALID	V_{IL}	V_{IL}	DON'T CARE	D_{IN}	ACTIVE

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

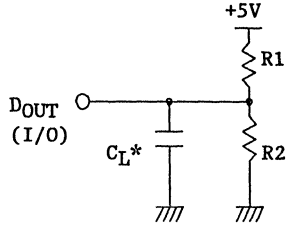
(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-40		40	μA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-10		10	μA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			40	mA
	TTL level	I_{SB2}			80	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA, V_{IN}=0V or V_{CC})		I_{CC1}			240	mA
OPERATING POWER SUPPLY CURRENT (I_{OUT}=0mA, t_{CYCLE}=Min.)		I_{CC2}			320	mA
INPUT HIGH LEVEL		V_{IH}	2.2		6.0	V
INPUT LOW LEVEL*1		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=8mA)		V_{OL}			0.4	V

Note: *1 -2.0V level with a maximum pulse width of 20ns.

Fig. 2 - AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3.0V
- Input Rise and Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)
- Output Load :



	R1	R2	C_L
Load I	480Ω	255Ω	30pF
Load II	480Ω	255Ω	5pF

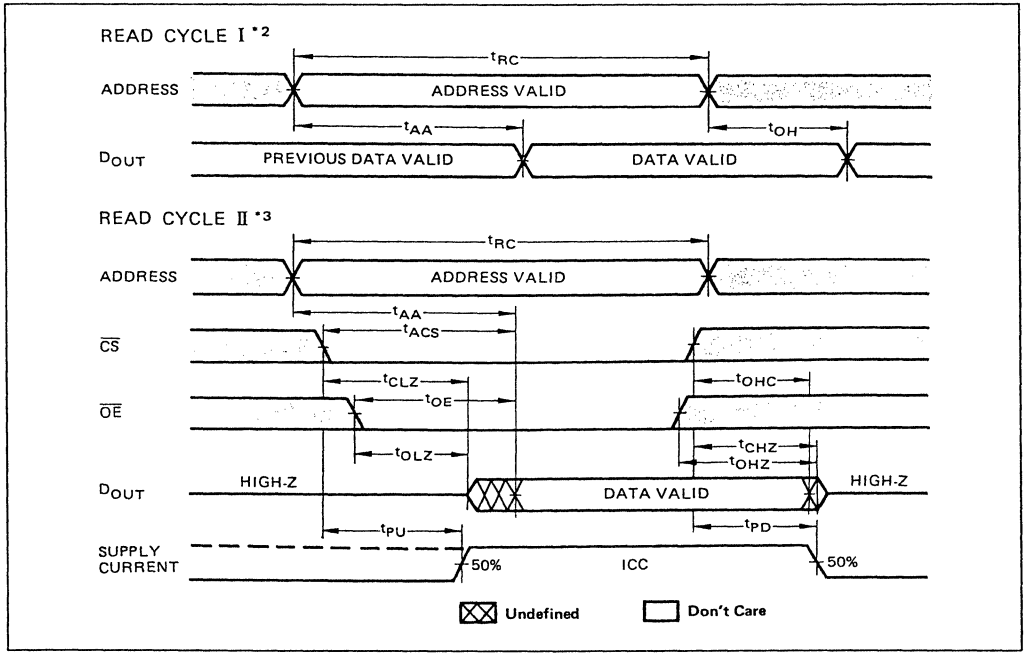
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB85402-30		MB85402-40		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	30		40		ns
Address Access Time *2	t_{AA}		30		40	ns
$\overline{CS}$ Access Time *3	t_{ACS}		30		40	ns
$\overline{OE}$ Access Time *3	t_{OE}		13		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		ns
$\overline{CS}$ to Output Low-Z *4*5	t_{CLS}	5		5		ns
$\overline{OE}$ to Output Low-Z *4*5	t_{OLZ}	0		0		ns
$\overline{CS}$ to Output High-Z *4*5	t_{CHZ}		13		15	ns
$\overline{OE}$ to Output High-Z *4*5	t_{OHZ}		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		25		30	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}, $\overline{OE}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

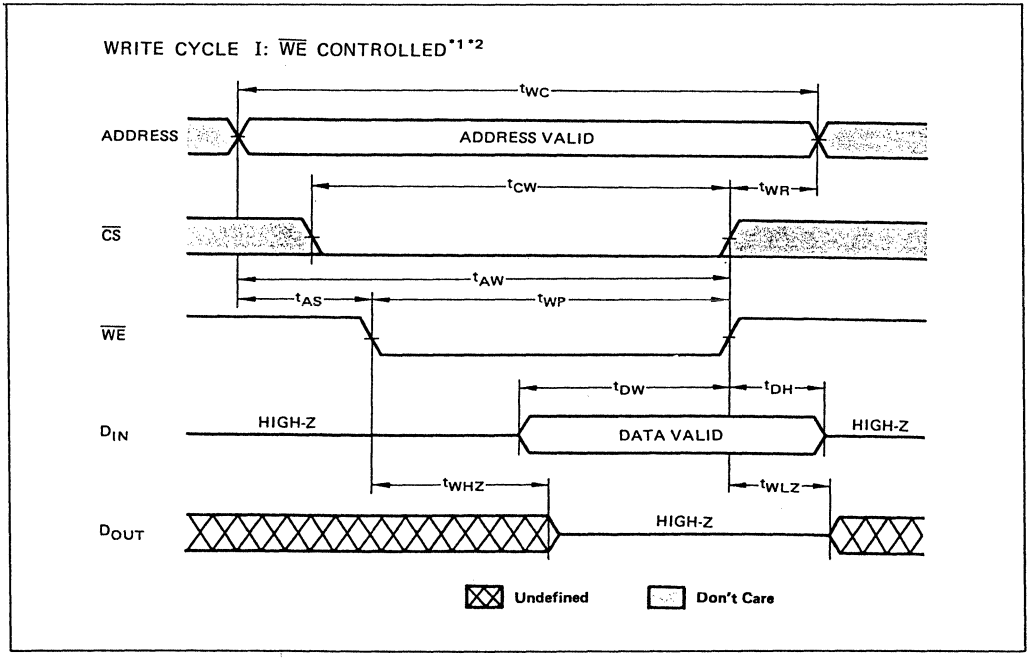
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85402-30		MB85402-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns
Data Valid to End of Write	t_{DW}	13		17		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	25		35		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WHZ}		13		15	ns
Output Low-Z from $\overline{WE}$ *3*4	t_{WLZ}		25		35	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

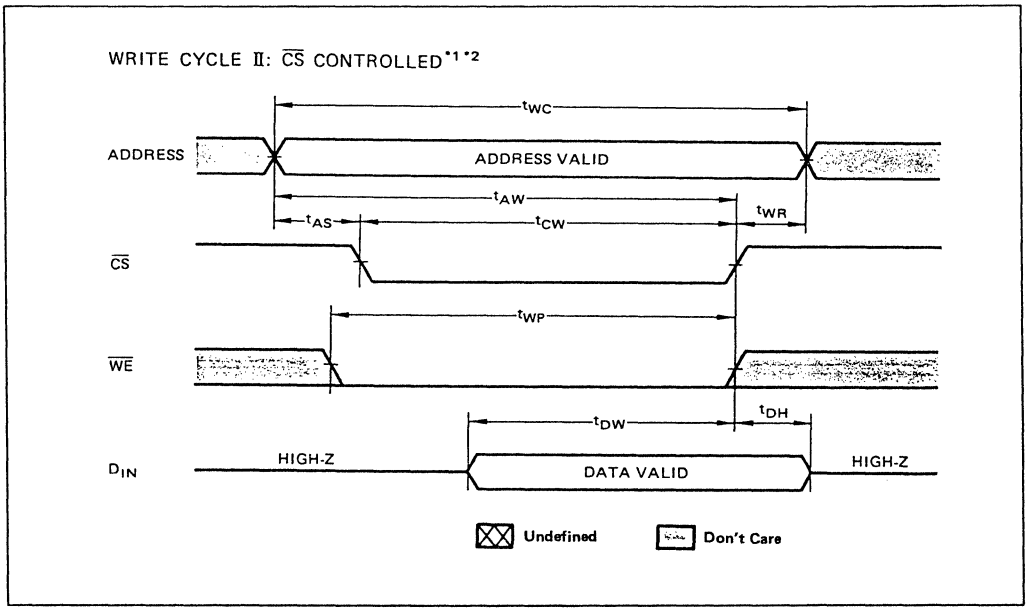
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

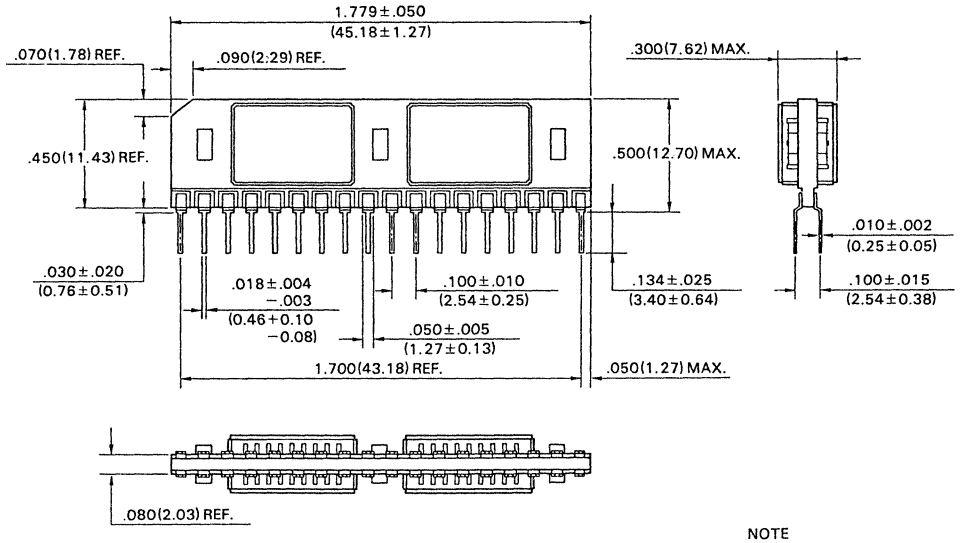
*2 All write cycle are determined from last address transition to the first address transition of the next address.

PACKAGE DIMENSIONS

(Suffix: CVCT)

36-LEAD CERAMIC MODULE

(Case No. : MTP-36C-C01)



NOTE

1. Dimension in inches and (millimeters).

6

FUJITSU

256K x 8 CMOS SRAM MODULE

MB85403A-40
MB85403A-50

TS261-A88Y
Nov. 1988

CMOS 262,144 Words x 8-Bit STATIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

The Fujitsu MB85403A is a fully decoded, CMOS static random access memory module consists of eight MB81C81A devices mounted on a 44-pin ceramic board. Organized as eight 256K x 1 devices, the MB85403 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

- Organized as 262,144 x 8-bit Words
- Memory : MB81C81A, 8 pcs
- Access Time : 40 ns max (MB85403A-40)
  50 ns max (MB85403A-50)
- Low Power Dissipation
  Standby: 660 mW max (CMOS level)
  1320 mW max (TTL level)
  Active : 5280 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- 44-Pin 100 MIL Ceramic Twin SIP (TSIP)

CERAMIC PACKAGE
MTP-44C-C02

PIN ASSIGNMENT
TOP VIEW

GND	1	44	VCC
DOUT0	2	43	DOUT7
DIN0	3	42	DIN7
A16	4	41	A0
A17	5	40	A1
A13	6	39	A2
GND	7	38	A3
DOUT1	8	37	DOUT6
DIN1	9	36	DIN6
A12	10	35	A4
A11	11	34	A7
NC	12	33	/WE
/CSA	13	32	/CSB
DOUT2	14	31	DOUT5
DIN2	15	30	DIN5
A14	16	29	GND
A15	17	28	A6
A10	18	27	A5
A9	19	26	A8
DOUT3	20	25	DOUT4
DIN3	21	24	DIN4
VCC	22	23	GND

ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 – BLOCK DIAGRAM

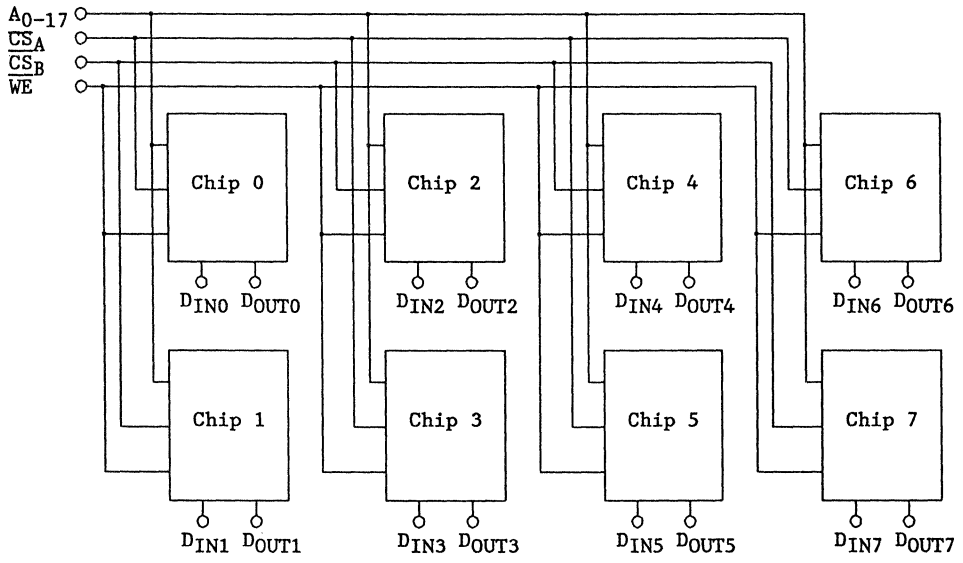


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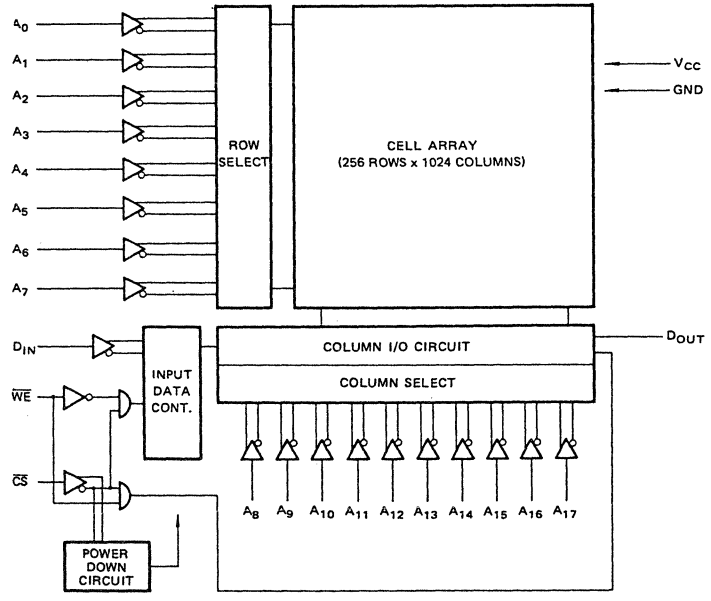
Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (except $\overline{CS}_A$, $\overline{CS}_B$)	C_{IN}		100	pF
Input Capacitance ($\overline{CS}_A$+$\overline{CS}_B$)	$C_{\overline{CS}}$		120	pF
Output Capacitance	C_{OUT}		20	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}_A$	$\overline{CS}_B$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	DON'T CARE	V_{IH}	V_{IH}	DON'T CARE	HIGH-Z	HIGH-Z	STANDBY
WRITE	VALID	V_{IL}	V_{IL}	V_{IL}	D_{IN}	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IL}	V_{IH}	HIGH-Z	D_{OUT}	ACTIVE

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

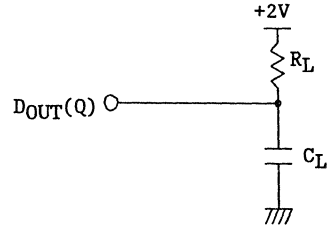
(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	μA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-50		50	μA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			120	mA
	TTL level	I_{SB2}			240	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)	MB85403A-40	I_{CC}			960	mA
	MB85403A-50				800	
PEAK POWER ON SUPPLY CURRENT ($\overline{CS}$=Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=16mA)		V_{OL}			0.4	V

Note: *1 -3.0V min. for pulse width less than 20ns.

Fig. 3 - AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns
- Timing Reference Levels : V_{IL}/V_{OL}=0.8V, V_{IH}/V_{OH}=2.2V
- Output Load :



	R_L	C_L
Load I	100Ω	30pF
Load II	100Ω	5pF

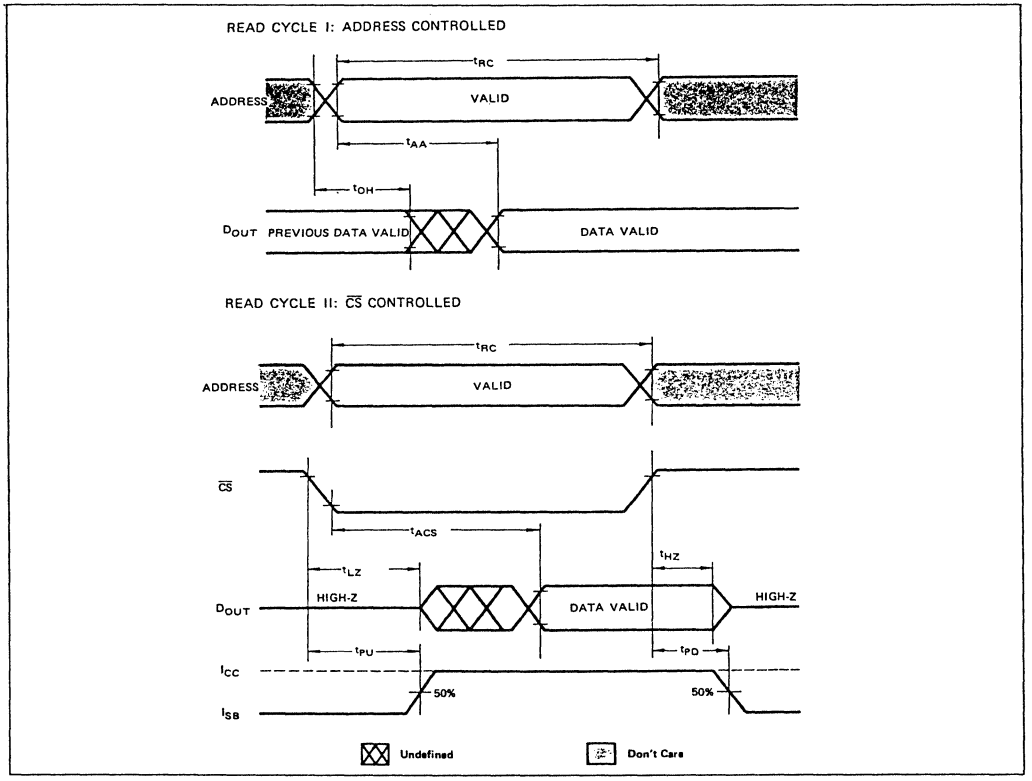
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Read Cycle Time *2	t_{RC}	40		50		ns
Address Access Time	t_{AA}		40		50	ns
CS Access Time *3	t_{ACS}		40		50	ns
Output Hold from Address Change	t_{OH}	5		5		ns
CS to Output Low-Z *4*5	t_{LZ}	5		5		ns
CS to Output High-Z *4*5	t_{HZ}	0	25	0	30	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		40		50	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high during Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 3.

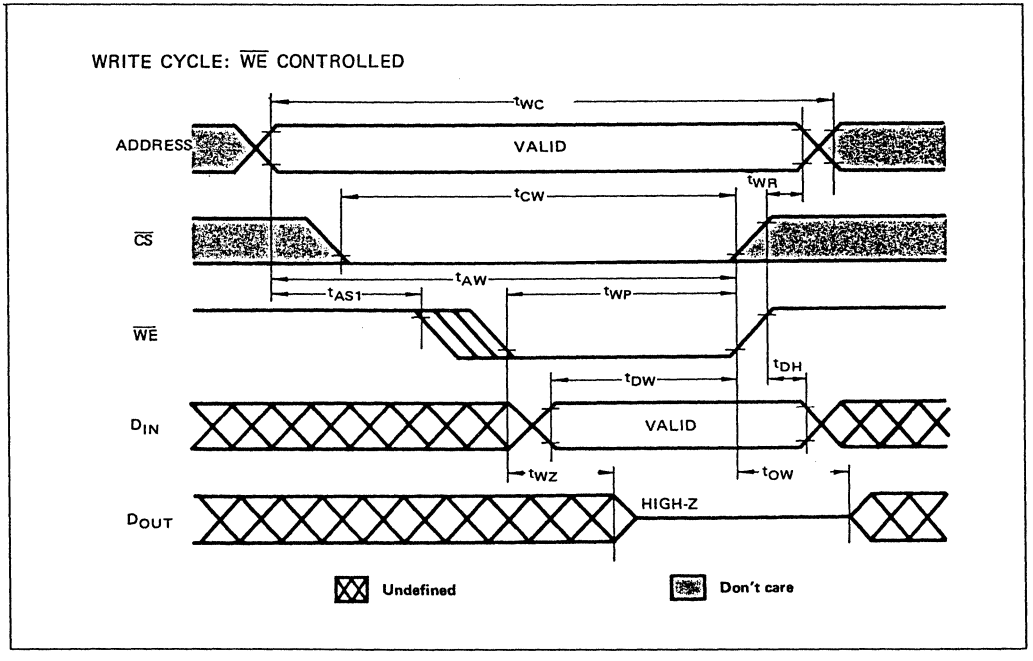
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85403A-40		MB85403A-50		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	40		50		ns
Address Valid to End of Write	t_{AW}	35		45		ns
CS to End of Write	t_{CW}	35		45		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	25		30		ns
Address Setup Time	t_{AS1}	5		5		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WZ}	0	25	0	30	ns
Output Low-Z from $\overline{WE}$ *3*4	t_{OZ}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

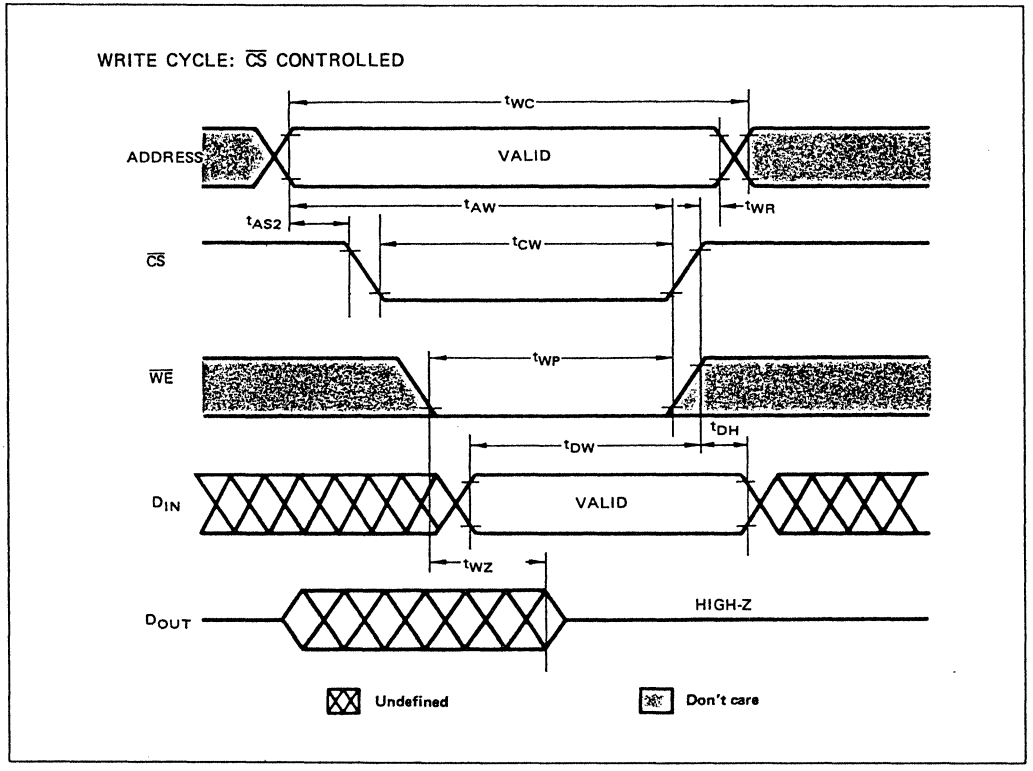
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

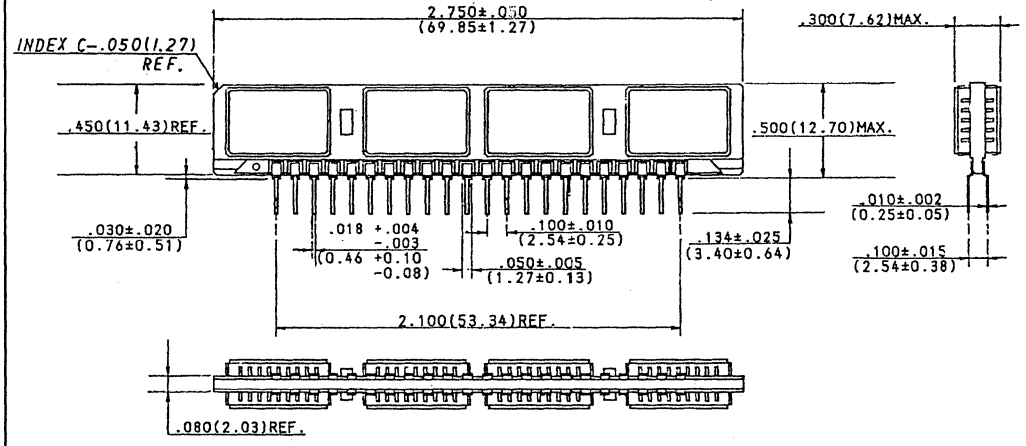


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

PACKAGE DIMENSIONS
(Suffix: CVCT)

44-LEAD CERAMIC DUAL IN-LINE MODULE
(Case No.: MTP-44C-C02)

PRELIMINARY



NOTE
1. Dimension in inches and (millimeters).

6

October 1989
Edition 1.0

FUJITSU

DATA SHEET

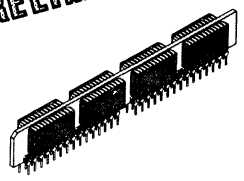
MB85410-30/-40
64K x 8 CMOS SRAM MODULE

CMOS 65,536 WORDS x 8-BIT HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

The Fujitsu MB85410 is a fully decoded, CMOS static random access memory module consists of eight MB81C71A devices mounted on a 60-pin plastic board. Organized as eight 64K x 1 devices, the MB85410 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

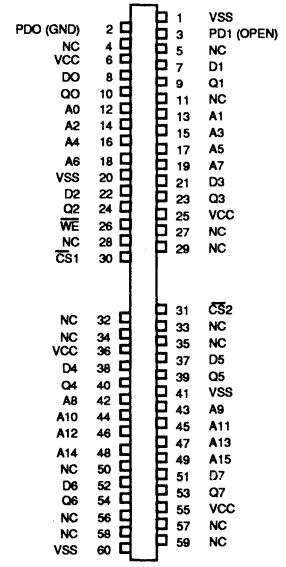
- Organized as 65,536 x 8-bit Words
- Memory: MB81C71A, 8 pcs
- Access Time: 30 ns max (MB85410-30)
  40 ns max (MB85410-40)
- Low Power Dissipation
  Standby : 440 mW max (CMOS level)
  880 mW max (TTL level)
  Active : 3200 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor: .22µF, 8pcs
- 60-Pin Plastic(FR-4) ZIP

PRELIMINARY



PLASTIC PACKAGE
MZP-60P-P02

PIN ASSIGNMENT
TOP VIEW



ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Ouput Voltage	V_{OUIT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 — BLOCK DIAGRAM

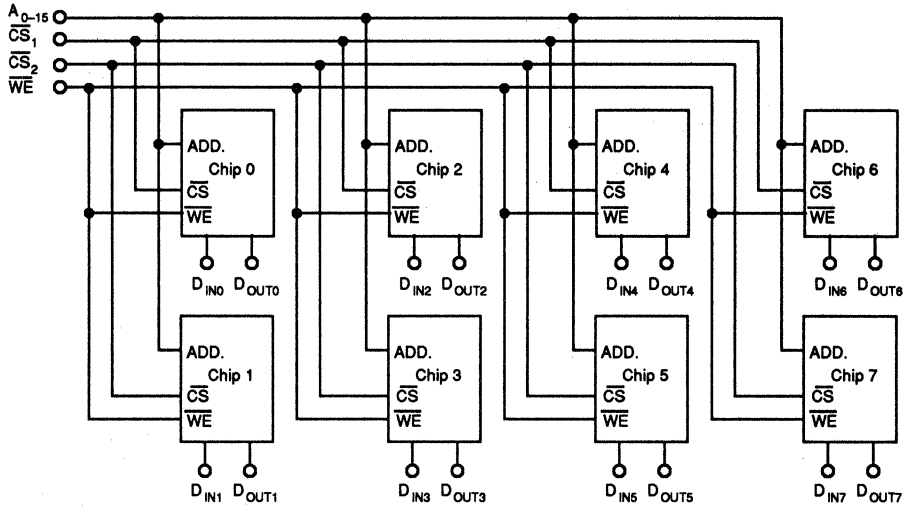
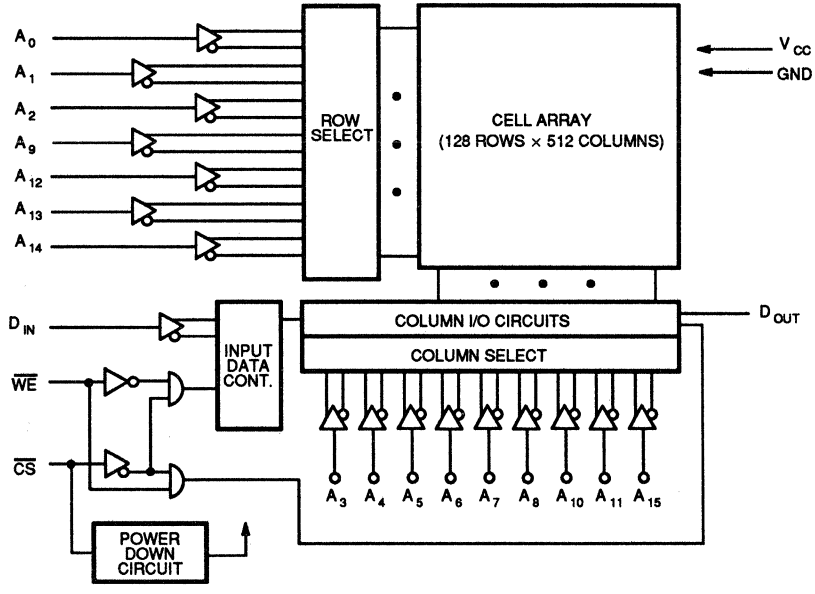


Fig. 2 – BLOCK DIAGRAM FOR EACH MEMORY



6

CAPACITANCE

(T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, Address and $\overline{WE}$	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		40	pF
Input Capacitance, D_{IN}	C_{IN3}		10	pF
Output Capacitance, D_{OUT}	C_{OUT}		10	pF

FUNCTIONAL TRUTH TABLE

Mode	Address	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	Input	Output	Power
Standby	Don't Care	V_{IH}	V_{IH}	Don't Care	High–Z	High –Z	Standby
Write	Valid	V_{IL}	V_{IL}	V_{IL}	D_{IN}	High–Z	Active
Read	Valid	V_{IL}	V_{IL}	V_{IH}	High–Z	D_{OUT}	Active

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

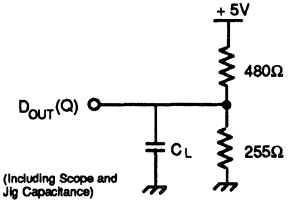
Parameter (conditions)		Symbol	Values			Unit
			Min	Typ	Max	
Input Leakage Current (V_{IN} = 0V to V_{CC})		I_{LI}	–80		80	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC})		I_{LO}	–10		10	µA
Standby Power Supply Current	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
Active Power Suppry Current ($\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)		I_{CC}			640	mA
Peak Power on Supply Current ($\overline{CS}$ = Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	–0.5		0.8	V
Output High Level (I_{OH} = – 4mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16mA)		V_{OL}			0.4	V

Note : *1 – 2.0V min. for pulse width less than 20ns.

6

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)
- Output Load:



	C_L
Load I	30pF
Load II	5pF

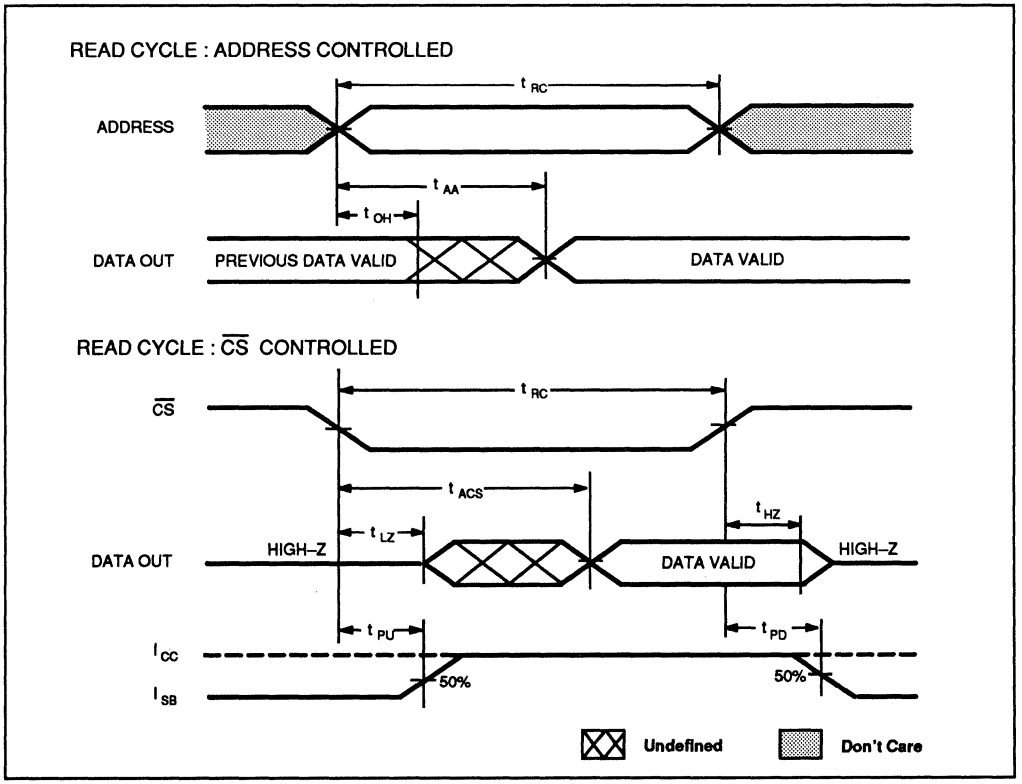
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	30		40		ns
Address Access Time	t_{AA}		30		40	ns
$\overline{CS}$ Access Time *2	t_{ACS}		30		40	ns
Output Hold from Address Change	t_{OH}	5		5		ns
$\overline{CS}$ to Output Low-Z *3*4	t_{LZ}	5		5		ns
$\overline{CS}$ to Output High-Z *3*4	t_{HZ}	0	10	0	15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS} = V_{IL}$.

*2 Address valid prior to or coincident with $\overline{CS}$ transition low.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

*4 This parameter is specified with Load Π in Fig. 3.

6

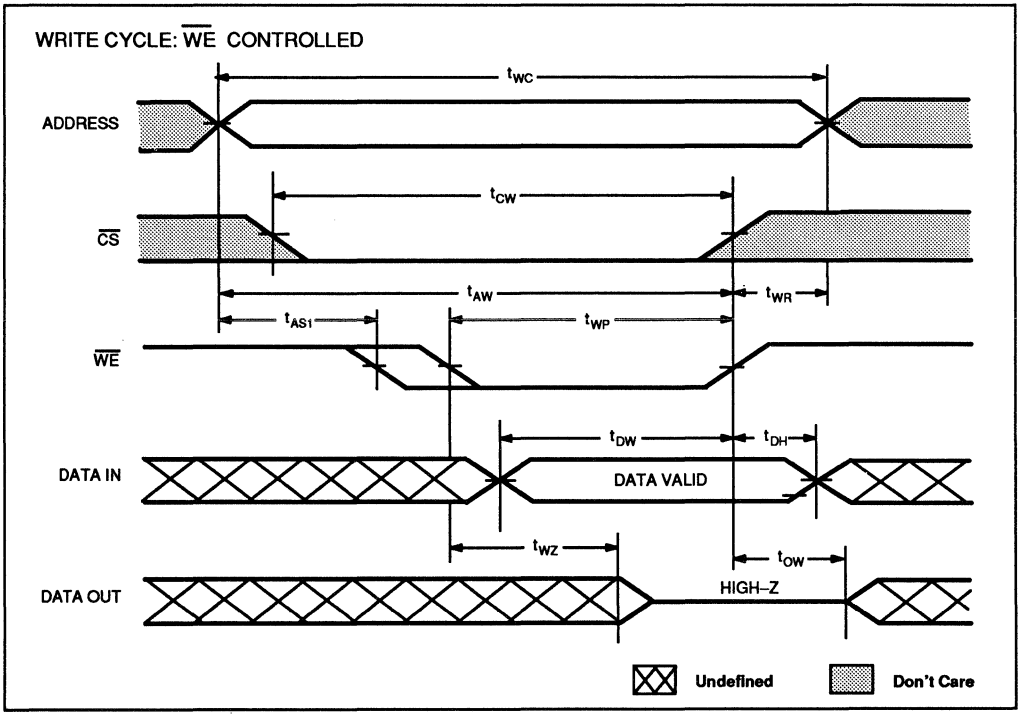
AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Address Setup Time	t_{AS1}	0		0		ns
	t_{AS2}	0		0		ns
Write Recovey Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$ *3 *4	t_{WZ}	0	10	0	15	ns
Output Low-Z from $\overline{WE}$ *3 *4	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

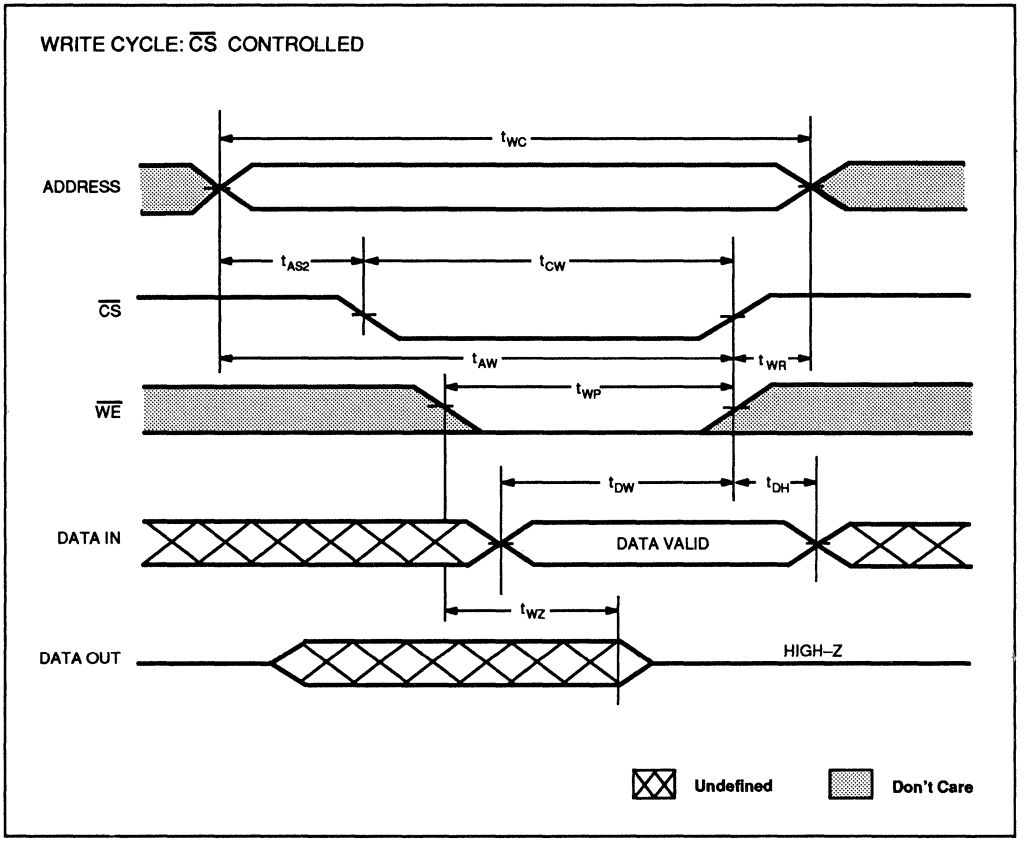
*3 Transition is measured at the point of ± 500mV from steady state voltage.

*4 This parameter is specified with Load Π in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

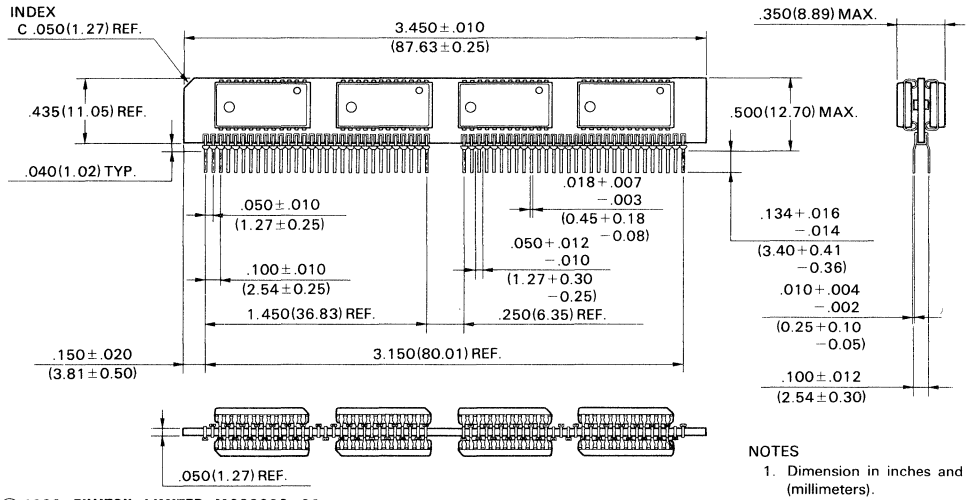


PACKAGE DIMENSIONS

(Suffix: –PJPZ)

60-LEAD PLASTIC MODULE

(Case No. : MZP-60P-P02)



NOTES

1. Dimension in inches and (millimeters).
2. Pin No. 1; Back side

6

FUJITSU

16K x 32 CMOS SRAM MODULE

MB85414-30
MB85414-40

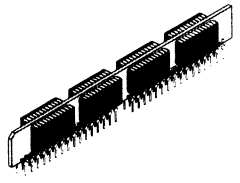
TS260-A88Y
Nov. 1988

CMOS 16,384 Words x 32-Bit HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

The Fujitsu MB85414 is a fully decoded, CMOS static random access memory module consists of nine MB81C75A devices mounted on a 64-pin plastic board.
Organized as eight 16K x 4 devices, the MB85414 is optimized for those applications requiring high speed, high performance, wide word width, and high density.

- Organized as 16,384 x 32-bit Words
- Optional organization as 32,768 x 16-bit
- Memory : MB81C75A, 8 pcs
- Access Time : 30 ns max (MB85414-30)
  40 ns max (MB85414-40)
- Low Power Dissipation
  Standby: 440 mW max (CMOS level)
  880 mW max (TTL level)
  Active : 3520 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor : .22µF, 8 pcs
- 64-Pin Plastic(FR-4) ZIP

PRELIMINARY



PLASTIC PACKAGE
MZP-64P-P01

PIN ASSIGNMENT
TOP VIEW

PD0(GND)	2	1	VSS
DQ0	4	3	PD1(OPEN)
DQ1	6	5	DQ4
DQ2	8	7	DQ5
DQ3	10	9	DQ6
VCC	12	11	DQ7
A6	14	13	A7
A10	16	15	A5
A3	18	17	A11
DQ8	20	19	DQ12
DQ9	22	21	DQ13
DQ10	24	23	DQ14
DQ11	26	25	DQ15
$\overline{WE}$	28	27	VSS
NC	30	29	NC
$\overline{CS1}$	32	31	$\overline{CS2}$
$\overline{CS3}$	34	33	$\overline{CS4}$
NC	36	35	NC
VSS	38	37	$\overline{OE}$
DQ16	40	39	DQ20
DQ17	42	41	DQ21
DQ18	44	43	DQ22
DQ19	46	45	DQ23
A1	48	47	A2
A9	50	49	A4
A0	52	51	A13
A12	54	53	VCC
DQ24	56	55	A8
DQ25	58	57	DQ28
DQ26	60	59	DQ29
DQ27	62	61	DQ30
VSS	64	63	DQ31

ABSOLUTE MAXIMUM RATING (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 – BLOCK DIAGRAM

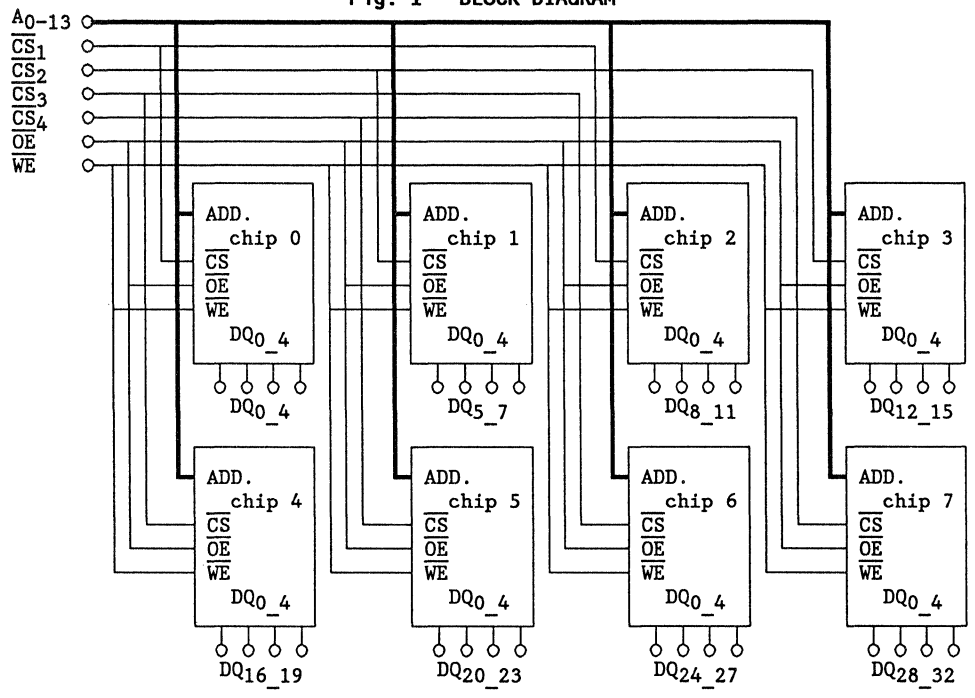
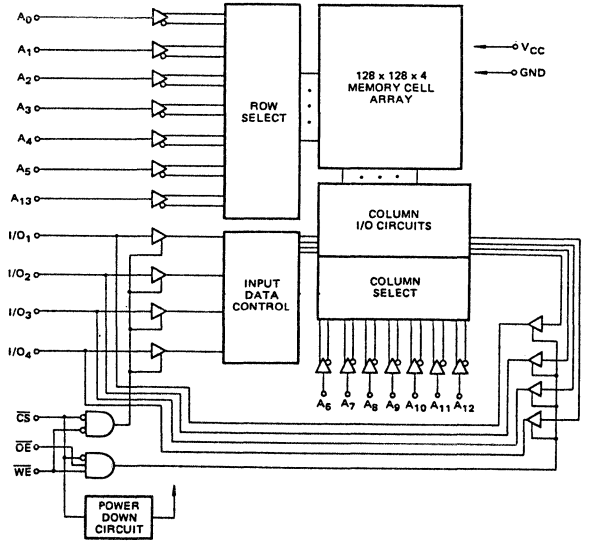


Fig. 2 – BLOCK DIAGRAM for EACH MEMORY



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CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, ADDRESS	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}$	C_{IN2}		30	pF
Input Capacitance, $\overline{WE}$ and $\overline{OE}$	C_{IN3}		80	pF
Input Capacitance, I/O	$C_{I/O}$		12	pF

FUNCTIONAL TRUTH TABLE

MODE	ADDRESS	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
STANDBY	X	V_{IH}	X	X	HIGH-Z	STANDBY
OUTPUT DISABLE	VALID	V_{IL}	V_{IH}	V_{IH}	HIGH-Z	ACTIVE
WRITE	VALID	V_{IL}	V_{IL}	X	HIGH-Z	ACTIVE
READ	VALID	V_{IL}	V_{IH}	V_{IL}	D_{OUT}	ACTIVE

X can be either V_{IH} or V_{IL}.

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

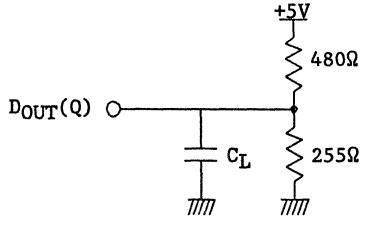
Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
INPUT LEAKAGE CURRENT (V_{IN}=0V to V_{CC})		I_{LI}	-80		80	µA
OUTPUT LEAKAGE CURRENT ($\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC})		I_{LO}	-10		10	µA
STANDBY POWER SUPPLY CURRENT	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
ACTIVE POWER SUPPLY CURRENT ($\overline{CS}$=V_{IL}, I_{OUT}=0mA)		I_{CC1}			480	mA
OPERATING SUPPLY CURRENT (Cycle=Min., I_{OUT}=0mA)		I_{CC2}			640	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	-0.5		0.8	V
OUTPUT HIGH LEVEL (I_{OH}=-4mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=8mA)		V_{OL}			0.4	V

Note: *1 -2.0V min. for pulse width less than 20ns.

6

Fig. 3 - AC TEST CONDITIONS

- Input Pulse Levels : 0V to 3V
- Input Rise and Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)
- Output Load :



(Including Scope and Jig Capacitance)

	C_L
Load I	30pF
Load II	5pF

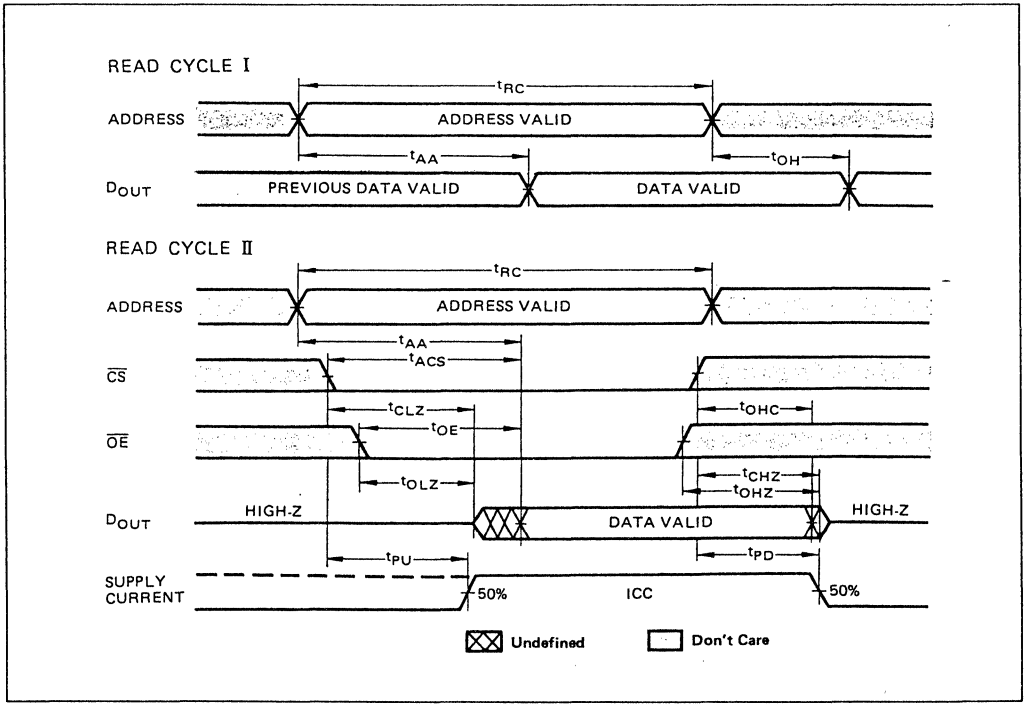
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85414-30		MB85414-40		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	30		40		ns
Address Access Time	t_{AA}		30		40	ns
CS Access Time *2	t_{ACS}		30		40	ns
OE Access Time *2	t_{OE}		15		20	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from Output Disable	tOHC	3		3		ns
CS to Output Low-Z *3*4	t_{CLZ}	5		5		ns
OE to Output Low-Z *3*4	t_{OLZ}	0		0		ns
CS to Output High-Z *3*4	t_{CHZ}		10		15	ns
OE to Output High-Z *3*4	t_{OHZ}		10		15	ns
Power Up from CS	t_{PU}	0		0		ns
Power Down from CS	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS}$=V_{IL}.
*2 Address valid prior to or coincident with $\overline{CS}$ transition low.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 3.

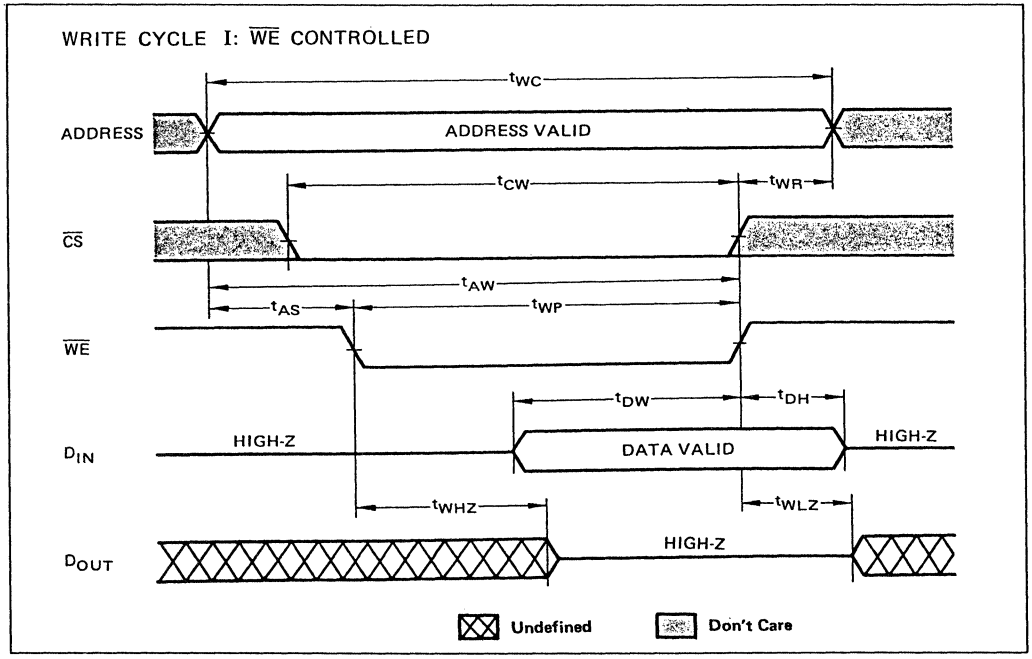
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85414-30		MB85414-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
CS to End of Write	t_{CW}	25		35		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	2		2		ns
Output High-Z from WE *3*4	t_{WHZ}		10		15	ns
Output Low-Z from WE *3*4	t_{WLZ}	0	20	0	30	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

*3 Transition is measured at the point of ±500mV from steady state voltage.

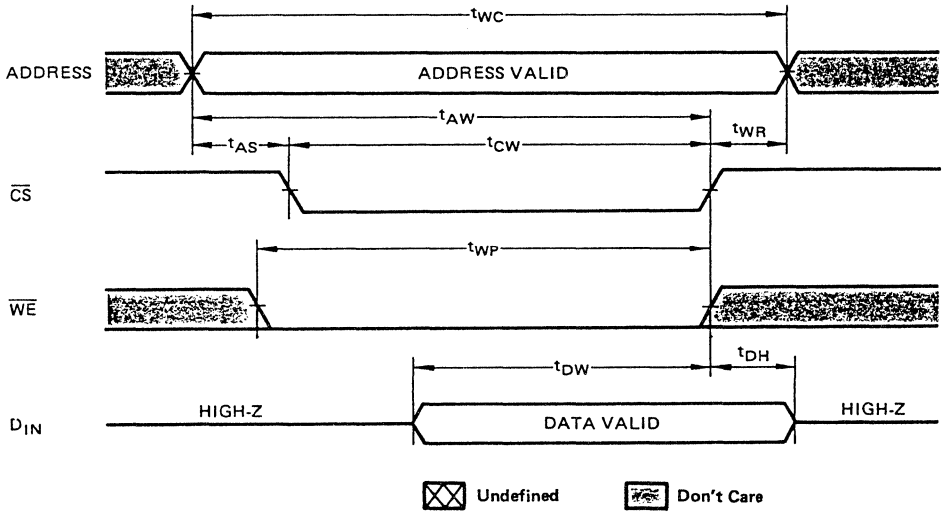
*4 This parameter is specified with Load II in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

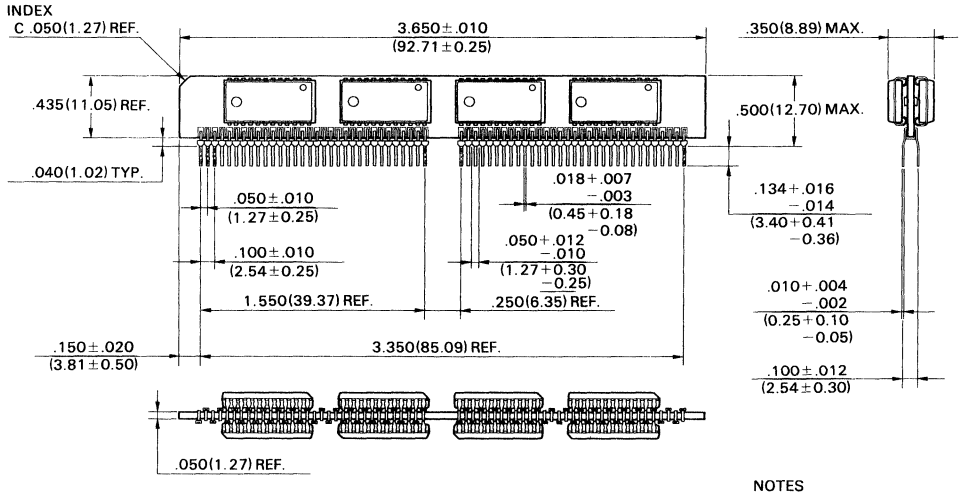
WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE II: $\overline{CS}$ CONTROLLED



PACKAGE DIMENSIONS
(Suffix: PJPZ)

64-LEAD PLASTIC MODULE
(Case No. : MZP-64P-P01)



NOTES
1. Dimension in inches and (millimeters).
2. Pin No.1; Back side.

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November 1989
Edition 1.0

FUJITSU

DATA SHEET

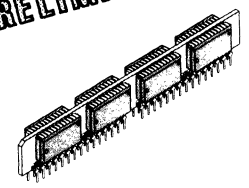
MB85420-40/-50
256K x 8 CMOS SRAM MODULE

CMOS 262,144 WORDS x 8-BIT HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

The Fujitsu MB85420 is a fully decoded, CMOS static random access memory module consists of eight MB81C81A devices mounted on a 60-pin plastic board.
Organized as eight 256K x 1 devices, the MB85420 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

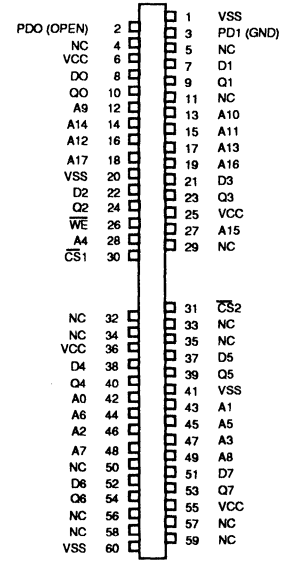
- Organized as 262,144 x 8-bit Words
- Memory: MB81C81A, 8 pcs
- Access Time: 40 ns max (MB85420-40)
  50 ns max (MB85420-50)
- Low Power Dissipation
  Standby : 660 mW max (CMOS level)
  1320 mW max (TTL level)
  Active : 5280 mW max (MB85240-40)
  4400 mW max (MB85420-50)
- Single +5V Power Suppry, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor: .22μF, 8pcs
- 60-Pin Plastic(FR-4) ZIP
- Upgrade version of MB85410

PRELIMINARY



PLASTIC PACKAGE
MZP-60P-P02

PIN ASSIGNMENT
TOP VIEW



ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Output Current	I_{OUT}	± 20	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 — BLOCK DIAGRAM

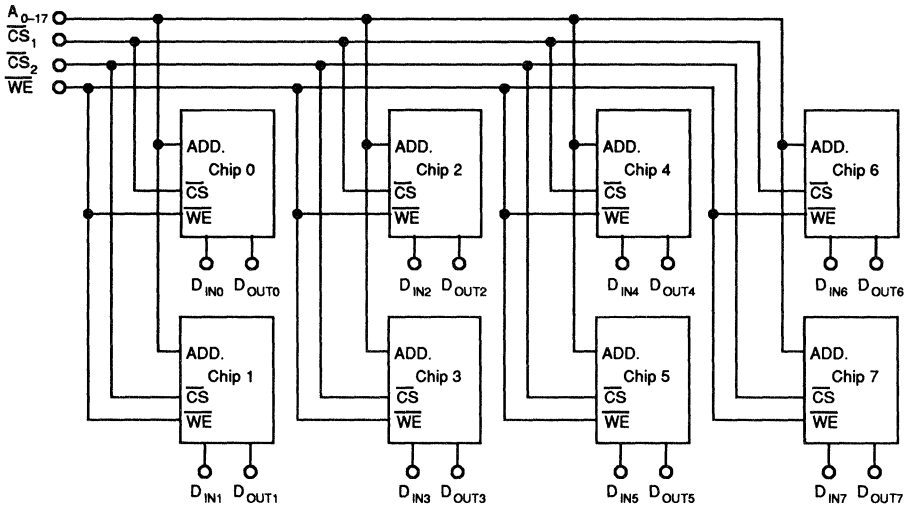
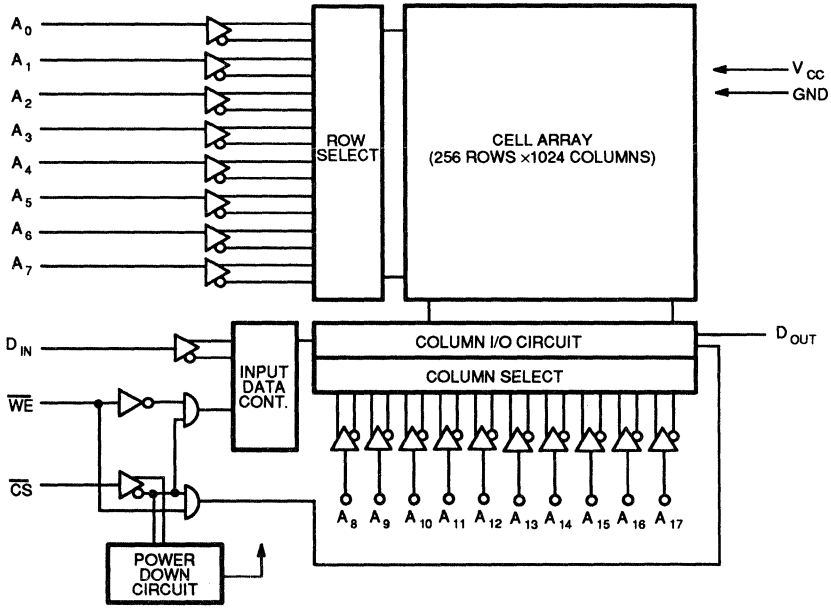


Fig. 2 – BLOCK DIAGRAM FOR EACH MEMORY



6

CAPACITANCE

(T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, Address and $\overline{WE}$	C_{IN1}		70	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		45	pF
Input Capacitance, D_{IN}	C_{IN3}		9	pF
Outout Capacitance, D_{OUT}	C_{OUT}		12	pF

FUNCTIONAL TRUTH TABLE

Mode	Address	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	Input	Output	Power
Standby	Don't Care	V_{IH}	V_{IH}	Don't Care	High–Z	High –Z	Standby
Write	Valid	V_{IL}	V_{IL}	V_{IL}	D_{IN}	High–Z	Active
Read	Valid	V_{IL}	V_{IL}	V_{IH}	High–Z	D_{OUT}	Active

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

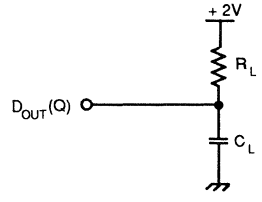
Parameter (Conditions)		Symbol	Values			Unit
			Min	Typ	Max	
Input Leakage Current (V_{IN} = 0V to V_{CC})		I_{LI}	–80		80	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC})		I_{LO}	–50		50	µA
Standby Power Supply Current	CMOS level	I_{SB1}			120	mA
	TTL level	I_{SB2}			240	mA
Active Power Suppry Current ($\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	MB85420–40	I_{CC}			960	mA
	MB85420–50				800	mA
Peak Power on Supply Current ($\overline{CS}$ = Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input High Level *1		V_{IL}	–0.5		0.8	V
Output High Level (I_{OH} = – 4mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16mA)		V_{OL}			0.4	V

Note : *1 – 3.0V min. for pulse width less than 20ns.

6

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns
- Timing Reference Levels : V_{IL} /V_{OL} = 0.8V, V_{IH}/V_{OH} = 2.2V
- Output Load:



	R_L	C_L
Load I	100Ω	30pF
Load II	100Ω	5pF

AC CHARACTERISTICS

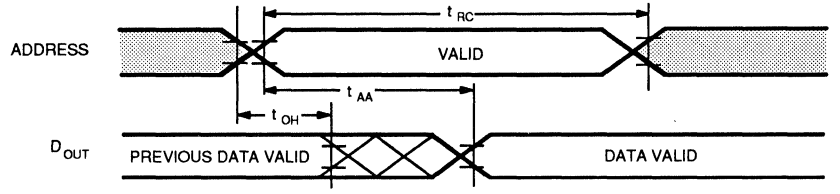
(At recommended operating conditions unless otherwise noted.)

READ CYCLE

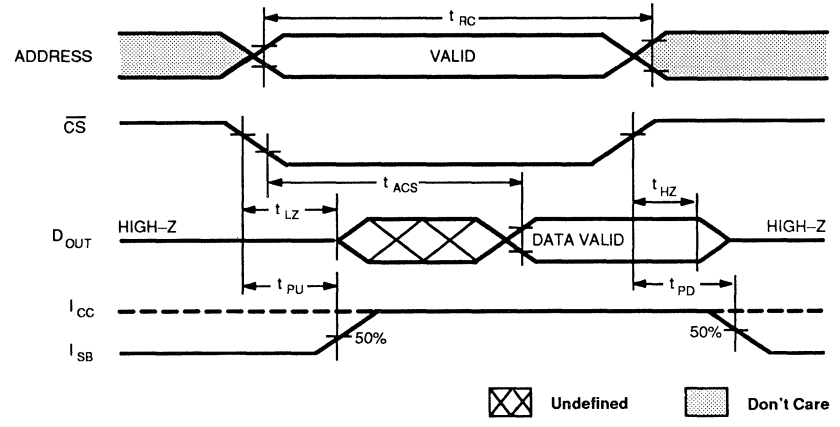
Parameter	Symbol	MB85420–40		MB85420–50		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	40		50		ns
Address Access Time	t_{AA}		40		50	ns
$\overline{CS}$ Access Time *2	t_{ACS}		40		50	ns
Output Hold from Address Change	t_{OH}	5		5		ns
$\overline{CS}$ to Output Low–Z *3*4	t_{LZ}	5		5		ns
$\overline{CS}$ to Output High–Z *3*4	t_{HZ}	0	20	0	25	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		40		50	ns

READ CYCLE TIMING DIAGRAM

READ CYCLE I: ADDRESS CONTROLLED



READ CYCLE II: $\overline{CS}$ CONTROLLED



Note: *1 Device is continuosly selected, $\overline{CS} = V_{IL}$.

*2 Address valid prior to or coincident with $\overline{CS}$ transition low.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

6

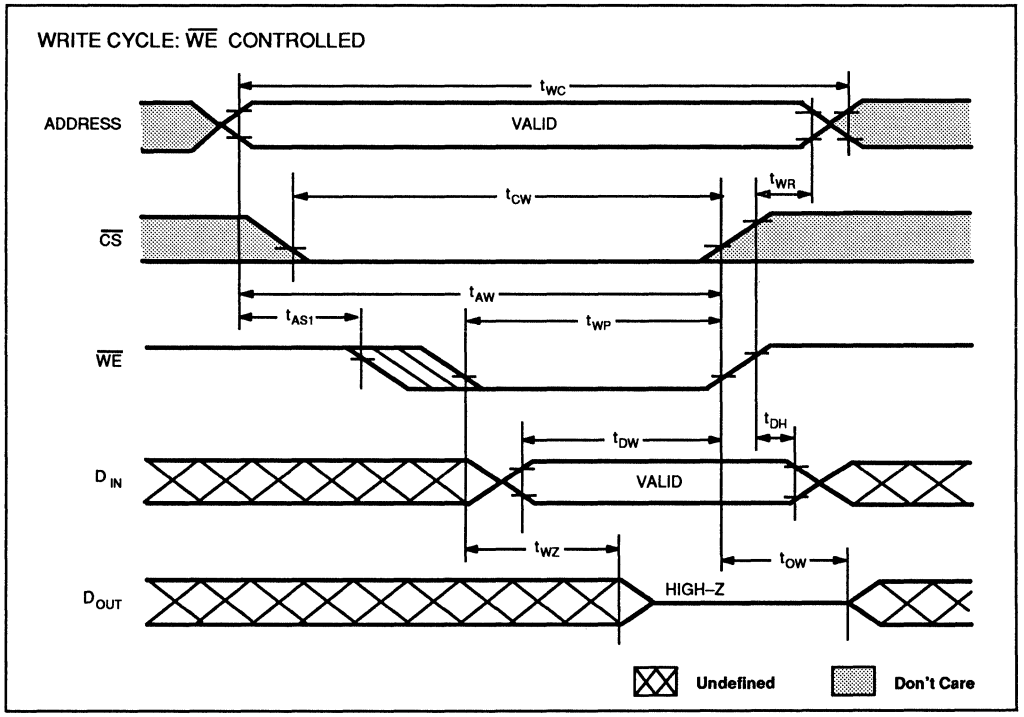
AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85420-40		MB85420-50		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	40		50		ns
Address Valid to End of Write	t_{AW}	35		45		ns
$\overline{CS}$ to End of Write	t_{CW}	35		45		ns
Data Valid to End of Write	t_{DW}	20		25		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	30		35		ns
Address Setup Time	t_{AS1}	5		5		ns
	t_{AS2}	0		0		ns
Write Recovery Time	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WZ}	0	20	0	25	ns
Output Low-Z from $\overline{WE}$ *3*4	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

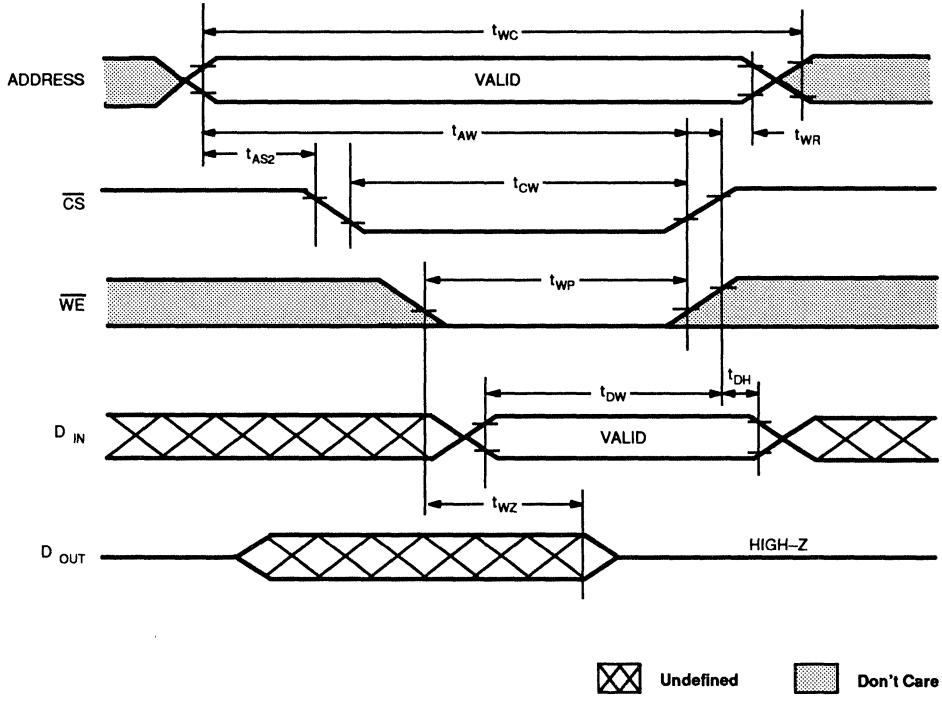
*4 This parameter is specified with Load Π in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED



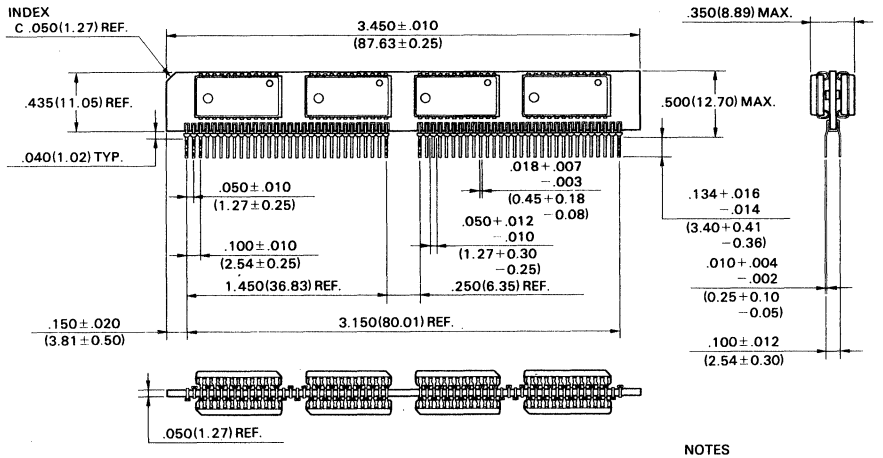
6

PACKAGE DIMENSIONS

(Suffix: –PJPZ)

60-LEAD PLASTIC MODULE

(Case No. : MZP-60P-P02)



NOTES

1. Dimension in inches and (millimeters).
2. Pin No.1; Back side

6

Section 7

Quality and Reliability — *At a Glance*

7

Quality Control at Fujitsu

Built-in Quality and Reliability

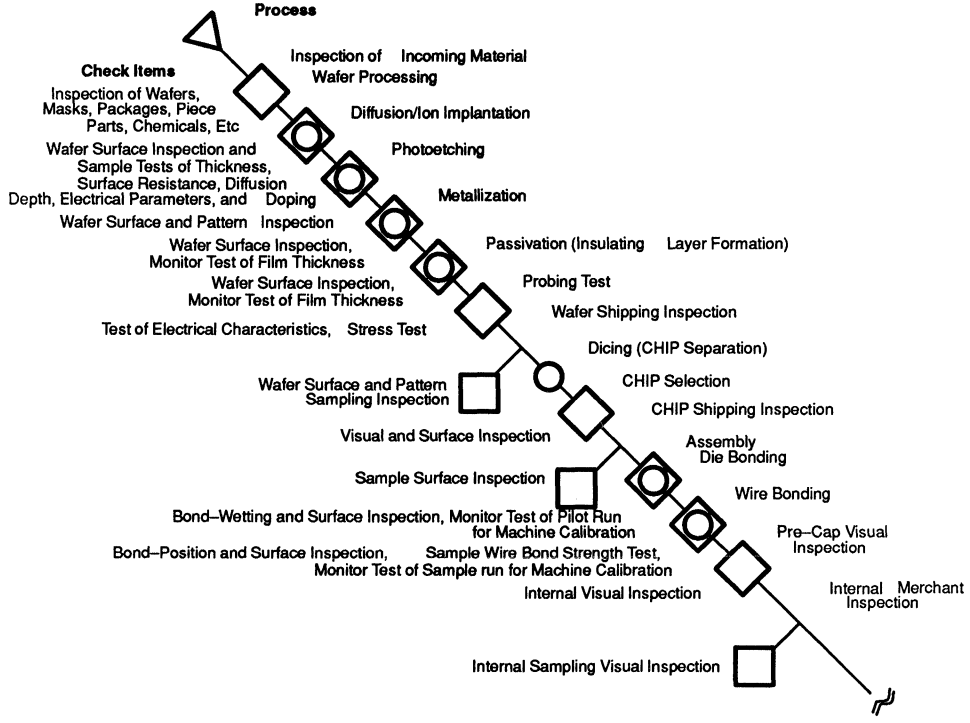
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



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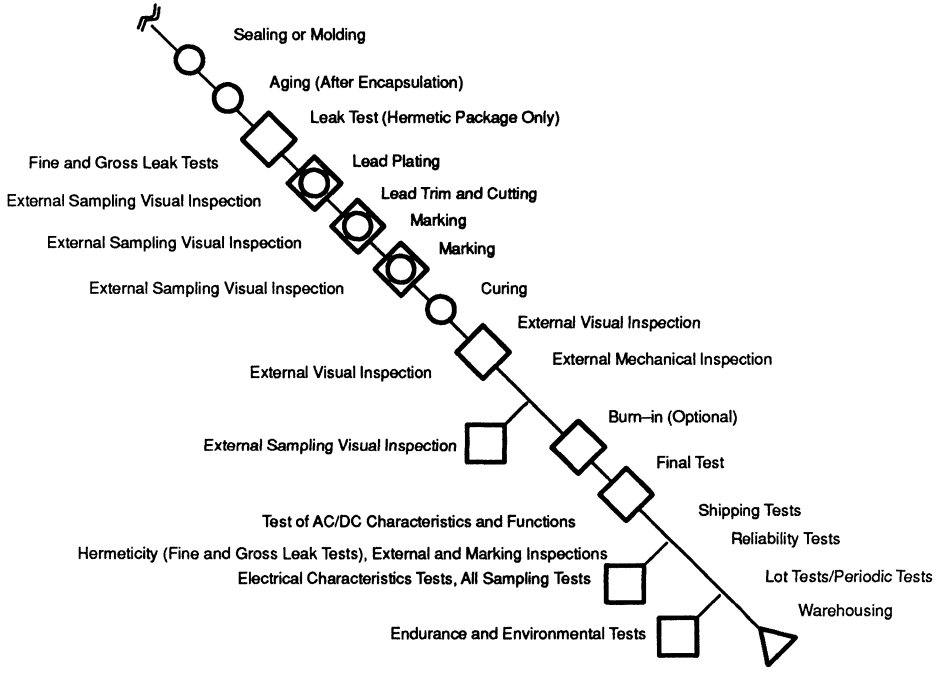
Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

7

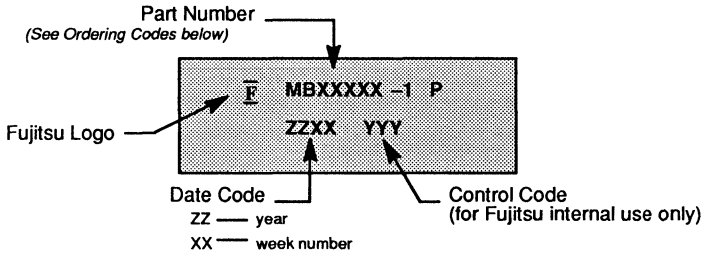
7

Section 8

Ordering Information — *At a Glance*

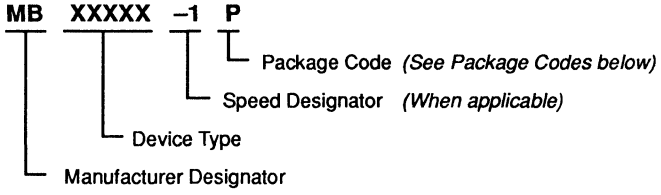
8

IC Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

IC Ordering Code (Part Number)



MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.

MBM Identifies an IC designed and manufactured by Fujitsu that uses a device number designated by the industry to be the industry standard number.

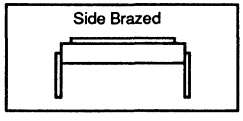
Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

IC Package Codes

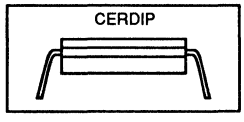
Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed)[1]	C
DIP (CERDIP)[2]	Z
Shrink DIP	CSH
Flatpack, Metal Seal	CF
Flatpack, Glass Seal	ZF
SOJ (Single Outline Junction)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, straight leads	PS
Single in-line, zig-zag leads	PSZ,PZ
SOJ (Single Outline Junction)	PJ

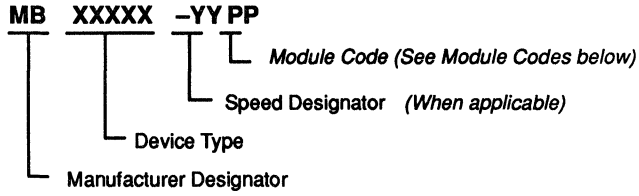
1 Side Brazed



2 CERDIP



IC Module Ordering Code (Part Number)



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Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

IC Module Package Codes

Ceramic	
Package Type	*Module Code*
Ceramic dual leads	CDL

Plastic	
Package Type	*Module Code*
Single in-line, leads	PL
Single in-line, zig-zag leads	PZ
Single in-line, pads	PS

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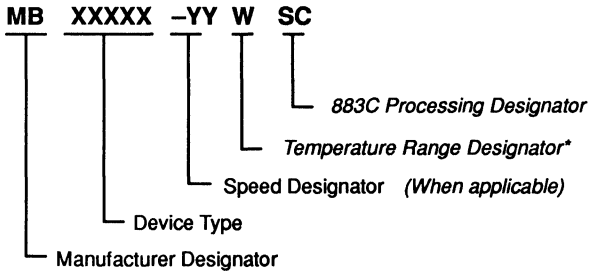
Wide Temperature Range IC Ordering Codes (Part Number)



MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.
***W** Indicates wide temperature range; see product specifications for exact temperature information.

Note: Please contact your Fujitsu sales office for exact part number/order information.

Wide Temperature Range IC Package

Ceramic	
Package Type	*Package Code*
DIP (CERDIP)	Z
DIP (Side Brazed)	C
Flatpack	F (ZF),
LCC (Leadless Chip Carrier)	V (CV), TV

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Section 9

Sales Information — *At a Glance*

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to include one research and development division, two marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

- DRAMs and DRAM Modules
- EPROMs
- EEPROMs
- NOVRAMs
- CMOS masked ROMs
- CMOS SRAMs and CMOS SRAM Modules
- BiCMOS SRAMs
- Bipolar PROMs
- ECL RAMs
- STRAMs (self-timed RAM)
- Hi-Rel PROMs and SRAMs
- Ultra High-speed ECL/ECL—TTL Translator Circuits
- Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

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Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

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SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet® is a registered trademark of Xerox Corporation.
EtherStar™ is a trademark of Fujitsu Microelectronics, Inc.
StarLAN™ is a trademark of AT&T.

Integrated Circuits Corporate Headquarters — Worldwide

International Corporate Headquarters

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Chiyoda–ku, Tokyo 100
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Telex: 781–22833
FAX: (03) 213-7174

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Integrated Circuits and Semiconductor Marketing
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Integrated Circuits Division
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Telex: 910–338–0190
FAX: (408) 432–9044

Headquarters for Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44–48
Arabella Centre 9. OG
D–6000 Frankfurt 71
Federal Republic of Germany
Tel: (069) 66320
Telex: 441963
FAX: (069) 6632122

Headquarters for Asia and Australia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
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Singapore 0719
Tel: (65) 336–1600
Telex: 55573
FAX: (65) 336–1609

Fujitsu Microelectronics, Inc. (FMI) Sales Offices for *North and South America*

NORTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
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SOUTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
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Irvine, CA 92714
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FAX: (714) 724–8778

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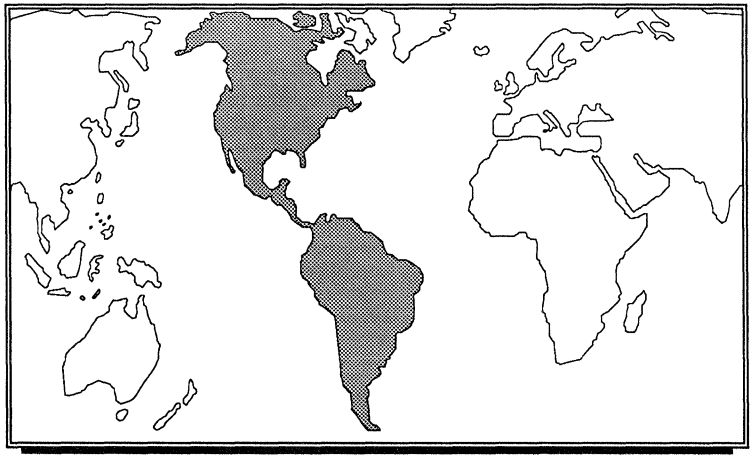

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For product information, contact your nearest Representative.

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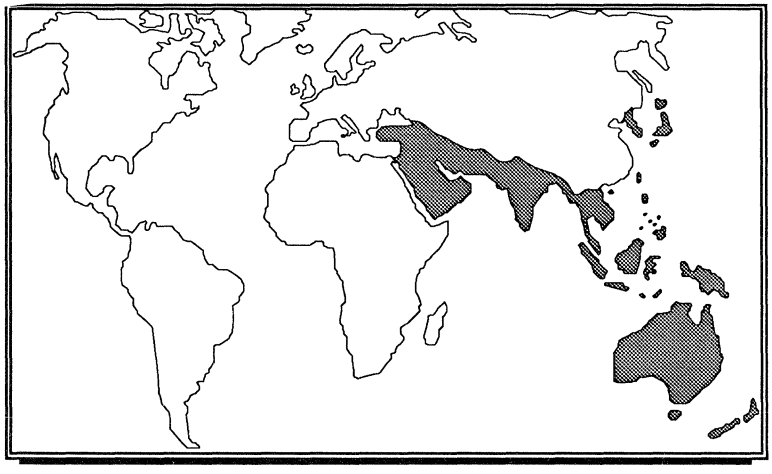

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Section 10

Design Information — *At a Glance*

Appendix 1

Self-Timed RAMs

10

Internally timed RAMs build fast writable control stores

Mohammad Shakaib Iqbal
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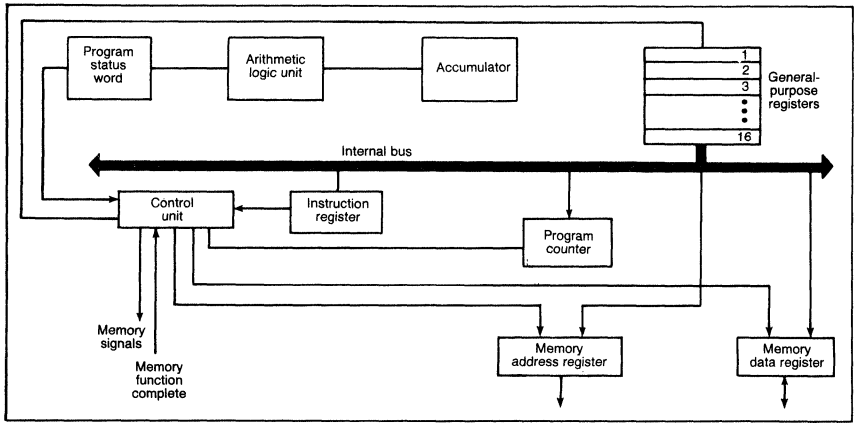
Create faster computers without sacrificing board space. Self-timed RAMs do the trick, replacing standard ECL RAMs in control memories.

The increasing speed of mainframes and minicomputers produces a need for memory access even faster than that supplied by ECL RAMs. One way to cut into 15-ns memory-access times is through process improvements, but this avenue quickly reaches its limits. Another method is to rework the architecture of the writable control store, which holds the microinstructions that implement the machine's assembly-language instructions. For instance, adding registers in the address and data lines to the control memory causes a pipeline effect that speeds up both read and write operations.

But the number of registers needed to process the size of control words in some of today's minicomputers can be prohibitive. The solution lies in the new self-timed RAMs (STRAMs)—pipelined memory devices containing on-board registers or latches, as well as a write-pulse generator. STRAMs not only shrink access times to 7 ns, but they also cut board space and reduce the number of lengthy connections between discrete parts. The latter is important because at ECL speeds these leads act as transmission lines, generating reflections and crosstalk.

To better understand how a STRAM can help a designer perform a specific task, consider a minicomputer's basic architecture. Both mainframes and minicomputers use microprogrammed processors in their CPUs. A microprogram is a flexible way to generate the control signals that implement assembly language. These control sequences or microinstructions reside in a control memory, usually a set of PROMs addressed by a microprogram counter.

In a microprogrammable machine, however, the control memory consists of fast RAMs, so a user can alter the control signals and modify the instructions. For example, a typical minicomputer CPU

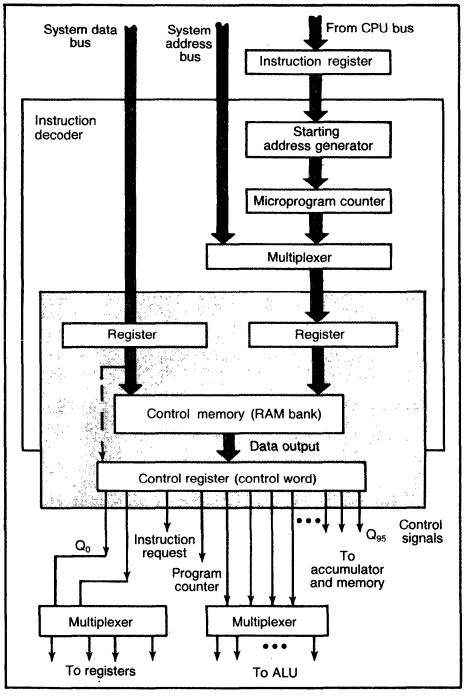


1. In a typical microprogrammed CPU, a control unit holds a control word employed for register loading, identification, and reading.

contains 12 kbytes of microprogrammable memory in its writable control store to diagnose problems, perform certain instructions, and change the microcode. For the sophisticated user, the CPU has an extra 12 kbytes of writable control store. This architecture lets a user change the way the computer responds to machine-language instructions.

A microprogrammable CPU usually contains general-purpose registers, an instruction register, a memory data register, a memory address register, a program counter, a 16-function arithmetic logic unit, a temporary register called an accumulator, and a control unit *(Fig. 1)*. The memory data register holds the data word to be sent to the memory, and the memory address register holds the address to the memory. The control unit sends a control word for register identification, loading, and reading. It generates signals like memory read and write, accumulator read and load, and ALU operations. The accumulator holds the ALU inputs and outputs.

The writable control store is implemented within the control unit *(Fig. 2)*. Its task is to generate the correct sequence of steps to execute the assembly-language instruction. Included in the controller are a starting address generator, microprogram counter, control memory, and control register. The control memory, addressed by the microprogram counter, stores the microinstructions. The control register holds the control word.



2. Adding registers to a writable control store's data and address paths speeds up the computer but at a steep price in board space. An alternative is to replace the components in the highlighted area with a self-timed RAM, which contains a write-pulse generator and registers.

The process begins when the CPU fetches a machine-language instruction from the main memory and loads it into the instruction register. Microprogramming then takes over. The instruction register puts the instruction into the starting address generator, which decodes the address of the first microinstruction in the control memory and loads this address into the microprogram counter. Next, the contents of the control memory pointed to by the microprogram counter are fetched and loaded into the control-word register. The microprogram counter is then updated to point to the next microinstruction in the desired sequence.

Minicomputers have control words 10 to 100 bits long. Each bit placed into the control-word register controls a part of the computer, including the instruction register, program counter, accumulator, memory, and ALU control. Hence, each bit is connected to a specific destination. The various control signals open or close data paths to these destinations or instruct the locations to perform an operation. For example, to transfer data between two registers, a control signal must instruct the source register to place the data on the bus, and a second signal must tell the destination register to read the data on the bus.

If the control store is writable, there must be a multiplexer between the microprogram counter and the control memory, because the address can come from either the microprogram counter or the system address bus. The system address bus's only task is to write to the control memory.

This is where a register between the counter and control memory input is beneficial. While the microprogram counter is generating an address during a read cycle (when it increments), the previous address can be in the register pointing to the control memory. That's the desired pipeline effect.

The computer gains a similar advantage during write cycles—that is, when the instructions in the microprogram are being altered. In this case, the new data is carried over the system bus and written in the control memory. If the memory consists of standard ECL RAMs and no registers, the address-hold time requirement will slow down the process.

Adding a register again creates a pipeline effect because the address and the data are both placed in the register. The address remains valid on the register's outputs until a new clock edge arrives, bringing a new address from the microprogram counter. The data and the address inputs are placed in the register on the true ongoing

edge of the clock. The Write Enable signal is also placed in the register *(Fig. 3a)*.

The several nanoseconds saved on each read and write cycle can add up to a considerable speed increase during normal computer operation. As noted, using STRAMs gives the designer this speed boost without the space penalty exacted by discrete registers.

In the example noted, a totally pipelined architecture was desired, so the registered STRAMs were used. This configuration yields the highest bit rate at the system level because the succeeding cycle can begin while the output signal is slewing and propagating. The data isn't available at the outputs until the next clock edge.

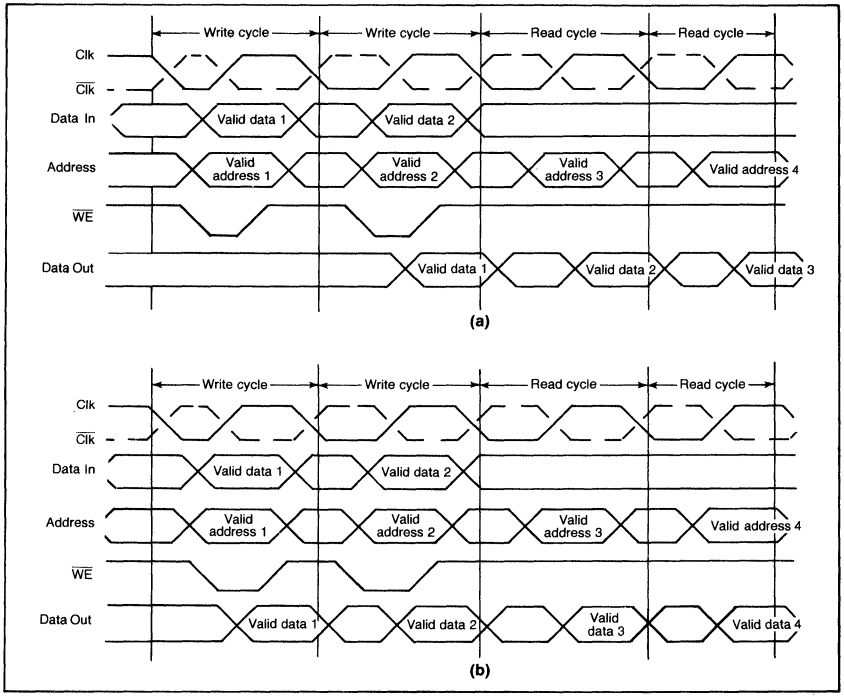
In some computers, however, the control store might have to read data from the RAM in one memory cycle. When this is the case, the control memory's inputs must have latches to hold the input data and address for saving the hold times. The output lines are also latched so that data can be placed on the data bus in one cycle. A latched STRAM fills the bill. This device's timing diagrams show that in read cycles the data is read in the same memory cycle *(Fig. 3b)*.

In a STRAM, the Address, Data In, Chip Enable, and Write Enable signals are latched into the on-chip registers or latches by the true-going edge or level of the clock pulse at the start of the memory cycle. All these signals remain valid throughout the memory cycle until the next true-going clock edge or level. As a result, signals need not be held stable during the entire cycle. They can slew down during one cycle to prepare for the next one.

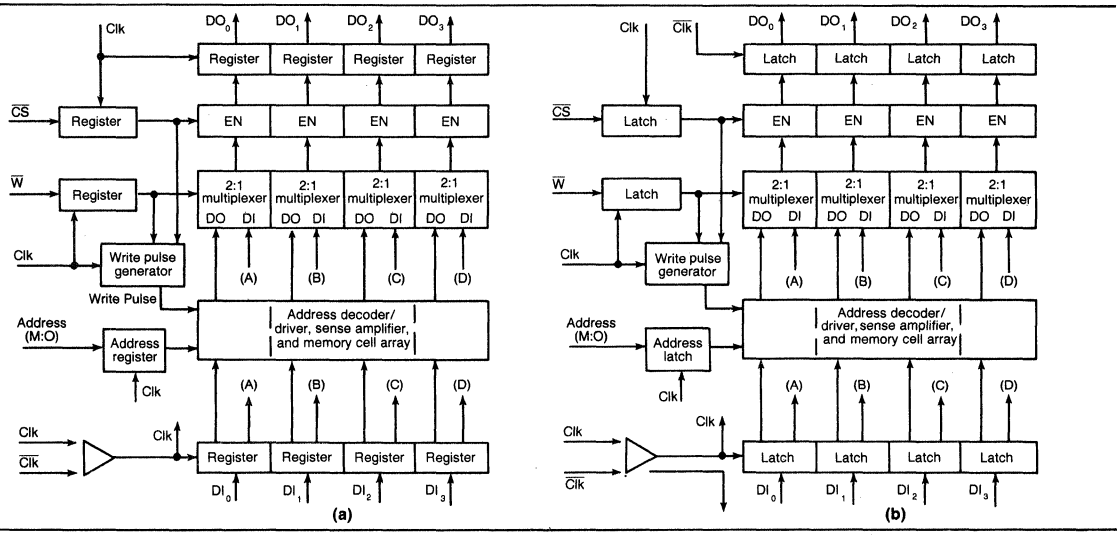
It's advantageous to trigger the write operation at the true going clock edge by latching the Address, Data, and Write Enable signals. Then the new Data and Address signals can be placed at the inputs while the old data is being written to the RAM cells. Also, this technique eliminates address skew because all the timing is clock-edge driven.

The basic difference between the registered and the latched STRAM, in fact, is that the former is clock-edge sensitive, while the latter is level sensitive *(Fig. 4)*. During a registered STRAM's read cycle, the data is available in the next clock cycle. For the latched STRAM, the data is available during the same memory cycle.

An advantage of both the latched and the register STRAM, however, is the built-in write-pulse generator, which eliminates an annoying problem associated with



3. Timing diagrams show that in a registered STRAM (a) the control word is read in the second clock cycle, while a latched STRAM (b) reads the data in the same clock cycle.



4. Both the registered (a) and latched versions (b) of the STRAM include a write-pulse generator. The devices have differential clock inputs—Clock and Clock—but single-ended operation is possible by connecting either clock line to an internal reference voltage.

fast ECL RAMs—the generation of a narrow write pulse. This on-board capability not only simplifies the designer's task, since creating very narrow pulses can be difficult, but it also speeds up the write cycle.

For instance, the length of a write cycle for a typical static RAM, MBM10474-15, employed without input and output latches is the sum of the minimum setup time, 2 ns; the write-pulse length, 12 ns; and the minimum hold time, 1 ns. That comes to 15 ns. For a latched STRAM with an internal write pulse generator, MBM10476LL-9, the write cycle time is the minimum setup time, 1 ns, plus the minimum high or low clock time, 6 ns—a total of 7 ns.

Another advantage of the STRAM is that the data written in the RAM is transparent to the outputs. This boosts the speed of the system for a cache write-through and improves the write-cycle timing for the writable control store. Also, the input data is transparent to the output in the same clock cycle for the latched STRAM and in the next cycle for the registered version. The transparent feature is helpful in diagnostic tasks and for writing back the data into the next location.

In both types of STRAMs the setup and hold times are identical for all inputs, simplifying the timing. The sum of the setup and hold times, also called the required valid window, is only 30% of the overall cycle time. For example, a 1k-by-4 latched STRAM, the MBM10476LL, has a clock cycle of 10 ns and a setup time plus hold time of 3 ns. This low ratio leaves enough time for the inputs to get ready for the next cycle.

The read and write cycles also have the same timing, because the data-input registers and latches are loaded at the start of each cycle, regardless of the type of cycle. This balanced read-write configuration is helpful for systems integration. When Write Enable is low at the beginning of a cycle, an internal write operation writes the data into memory and restores internal write lines to their original values.

The devices have differential clock inputs—Clock and $\overline{\text{Clock}}$—to increase timing accuracy. They can be connected in either the differential or single-ended mode. In the differential mode, data is latched at the cross point of the rising edge of Clock and at the falling edge of $\overline{\text{Clock}}$. Connecting either Clock or $\overline{\text{Clock}}$ to the internal reference voltage configures the STRAM in the single-ended mode, latching data at the true going edge of the clock.□

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Appendix 2

Static RAMs

November 1989
Edition 1.1

APPLICATION NOTE

FUJITSU

Separate Data Inputs and Outputs SRAMs Provide New Architectural Solutions for System Designers

Applications Engineering Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

ABSTRACT

Traditionally, Static Random Access Memories (SRAMs) which can store greater than one-bit-wide words are available in packages with common data inputs and outputs. This is a consequence of the package size constraints, for wider word widths. Fujitsu also offers byte wide and word-wide devices such as MB81C78A, MB81C79 and MB81C40. In the case of SRAMs with four-bit wide words or less, the increase in package size is not significant. Instead, the advantages of separate I/Os for system designers more than outweigh the slight increase in package size. The basic benefit of having separate data inputs and outputs is that it does not require the data bus direction to be changed during a read-modify write cycle. Thus, the need for multiplexing and demultiplexing in the data paths is eliminated. This application note deals with some specific usage areas which take advantage of the separate data input and output SRAMs.

A large variety of new applications, as well as some old memory designs have a need for separate data input and output pins on the SRAMs. Some of the key application areas are as follows: writeable ritual microprogram control stores, cache memory systems, and deep FIFO data buffers for disks and LANs. The following discussion covers each of these application areas, highlighting the importance of the separate data input and output SRAMs.

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Edition 1.1

Contents

Illustrations

Microprogramming and Writeable Control Store

Microprogramming has become one of the most powerful tools currently available to designers of high-speed, microprocessor-based systems. It provides a degree of flexibility previously unattainable in sophisticated processors and controllers.

Microprogramming is actually accomplished by execution of a machine language program that is made up of a sequence of microinstructions. This execution is performed at a microinstruction level by having each microinstruction interpreted on the host machine hardware through a microprogram[1]

Microprograms comprise a sequence of microinstructions that activate the control primitives of the host machine. Individual sequences contain all the elemental steps required to perform system function. The microprogram is kept in a high-speed, random access storage unit that is called a control store or control memory. Control storage is normally found implemented as a ROM. However, control storage may also exist as a dynamically alterable memory known as a writeable control store. A read only memory cannot be modified by an executing microprogram. The contents of the control ROM are unalterable and provide a fixed interpretation sequence for a given microinstruction set. On the other hand, the contents of the writeable control store can be modified by executing a microprogram. This allows the architecture of the host machine to be redefined under microprogram control since a different microprogram module may be loaded in the writeable control store under the control of the user program. A processor having this capability is called a flexible architecture machine.

A writeable control store memory provides the main application for the static RAM with separate data inputs and outputs. This will be evident from the arrangement of the control store as shown in Figure 1.

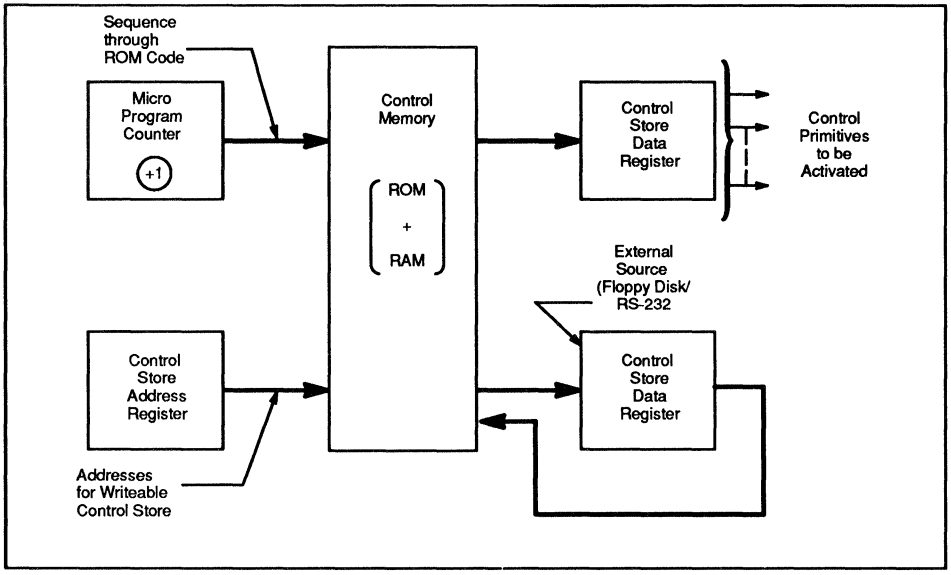

Figure 1. Arrangement of a Control Store Memory

The Main Parts of a Control Store

1. *Microprogram Counter*
   The microprogram counter contains the address of the next microinstruction which is loaded in the control store. Usually, it is incremented by one, and the program sequencing is done by adding one (1) to the current contents of the microprogram counter.

2. *Microprogram Instruction Register*
   The microinstruction register contains the current microinstruction being executed by the host machine. For a read only store, the microinstruction register would not provide leads for data to be written into the control memory — it would only receive data from the control store.

3. *Control Store Data Register*
   Since many microprogrammed machines use a combination of read only storage and writeable storage, another register must be provided to supply data to be written in the writeable control memory. This register can be called the control store data register.

4. *Control Store Address Register*
   Generally, the microcode which is loaded in the writeable control store is not written into the same location as that of the next instruction; therefore, a fourth register is needed. This register is called the control store address register. It points to the location in the writeable control store where the data word in the microcode is to be stored.

It is possible to combine the functions of the microprogram counter and the control address register as well as the functions of the microinstruction register and the control store data register. In general, these four registers will be kept separated, with the control store address register and

the control store data register forming a pair that references writeable control store and functions independently of the register pair formed by the microprogram counter and the microinstruction register. The microprogram counter and the microinstruction register, in turn, reference read-only control storage in terms of microprogram execution. Thus, a block of microcode could be loaded from a system peripheral, such as a floppy disk, into the writeable control store for usage by a specific microprogram. Similarly, data from either writeable control store or control ROM could be copied by control memory over into the main storage. The precise reasons for performing these operations would be dictated by the requirements of the user. In this application it is desirable to us an SRAM, with separate data inputs and outputs to avoid the multiplexing and demultiplexing in the data paths.

Some systems use only writeable control store as control memory. In this case, the sequencer needs the addresses for read cycles of the RAM, while the microprocessor sends the addresses for the write cycle of the RAM. Typically the outputs of the writeable control store are to be configured in a very wide microword, anywhere between 64 to 96 bits wide. This is a horizontal microword implementation. The term horizontal here implies that the microword has enough bits to directly control all the significant machine resources without additional decoding, encoding or other hardware interpretation. The inputs, however, are configured into an 8- or 16-bit wide data bus, in order to be loaded directly from the host microprocessor. This is evident from Figure 2 presenting the more detailed arrangement in as typical system, which uses only a writeable control store.

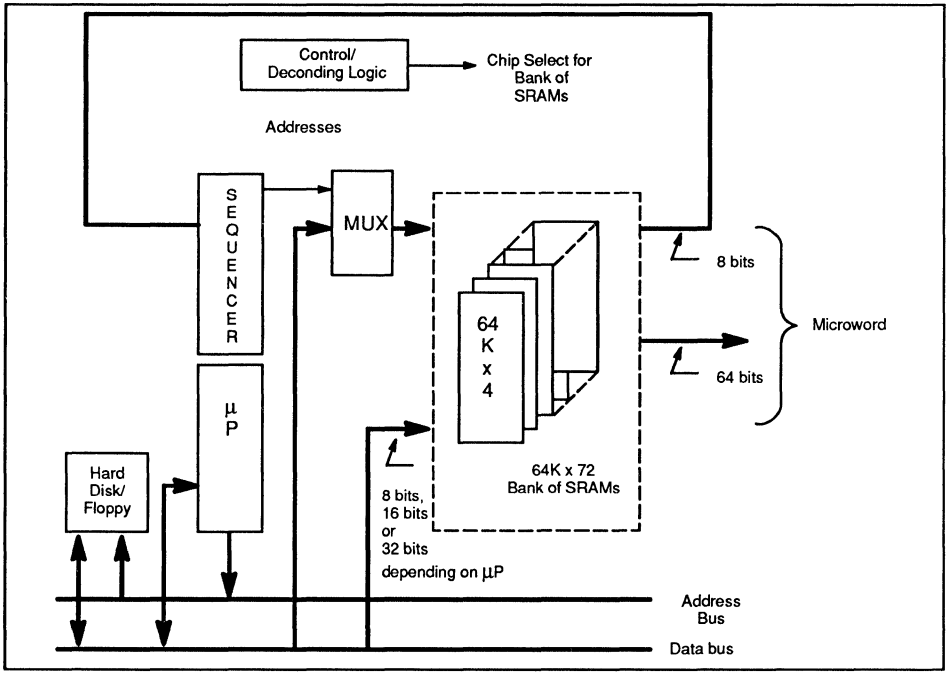

Figure 2. Writeable Control Store Memory

For this type of architecture, a static RAM with separate data inputs and outputs is required. If this design is implemented by devices having a common data input and output bus, then the design would require numerous buffers, or transceivers to accomplish this function. Thus, by using the separate data input and output static RAM, like the Fujitsu MB81C86 which is 64K x 4 bits wide, the designer realizes a significant savings in IC count, as well as PC board real estate.

Some Thoughts on Application Areas

Due to the flexibility and cost reductions throughout the design development and maintenance, microprogrammed (MP) systems extend across large product and application areas, ranging from simple control functions to complex real time control systems.

Aside from the more common applications, such as emulation of other systems, and upward/downward compatibility among series configured minicomputer systems, microprogram control units (because of their cost effectiveness) can be applied to functions previously performed only by special circuits or custom made devices. For example:

1. Process control systems (factory automation).
2. Instrumentation systems (signal generators, synthesizers etc.).
3. Intelligent terminal for off-line editing (supermarket checkouts, terminals of investment houses).
4. Real time data processing (spectral analysis, pattern recognition, etc.).
5. Data communications systems have MP systems controlling polling, scheduling tasks, buffer management (front end processors, communication processors, etc.).

Applications of MP systems are virtually unlimited because of their high performance/low cost implementation. Hence, the availability of static RAMs with separate data inputs and outputs has a substantial impact on the design of MP systems which, in turn, find their way into a wide variety of applications, as discussed previously. Another area of system architecture which benefits from the separate data inputs and outputs on the static RAMs is the cache memory system design.

Cache Memory Systems

In a cache-based system, a small, fast memory known as the buffer or the cache, (with roughly the same speed as the processor registers) is interposed between the processor and the main memory. This cache serves as a transparent bridge between their speeds. The "cache bridge" is transparent in the sense that is is invisible, making it inaccessible to the users, since it is completely hidden from them and not directly addressable (cache means "a hiding place"). However, by providing the processor with all the current information it requires at a faster speed, the cache creates an illusion of having a large main memory operating.[3]

During the era of early computing, the main memory technology was quite slow compared to the speed of the CPU. In order to overcome the slow access of the main memory, a small high performance cache buffer memory was placed between the CPU and the main memory. Figure 3 shows two of the most common memory hierarchy.

The two-level cache has already been discussed; i.e., slow memory communicates with a fast CPU. The three-level case takes into account the advantages of having a cache. With this memory hierarchy scheme, the CPU would execute data from the very fast cache buffer and would only have to slow down when this

buffer required new data from the slow main memory. Thus, with a small fast buffer, the overall performance of the large, slow main memory approaches that of the buffer.

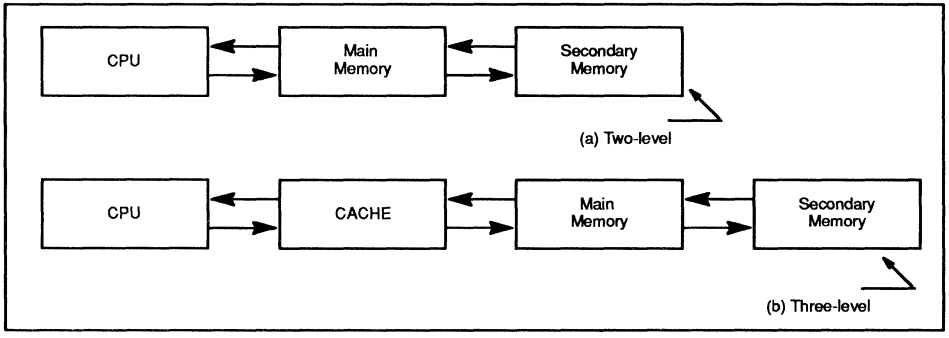

Figure 3. Common Memory Hierarchies: (a) Two-level, (b) Three-level

Basic Blocks of a Cache Memory

As already discussed, the philosophy behind the concept of buffering or caching is to use a fast, relatively small memory between the processor and the main memory. Figure 4 shows a typical way of implementing a cache memory system.

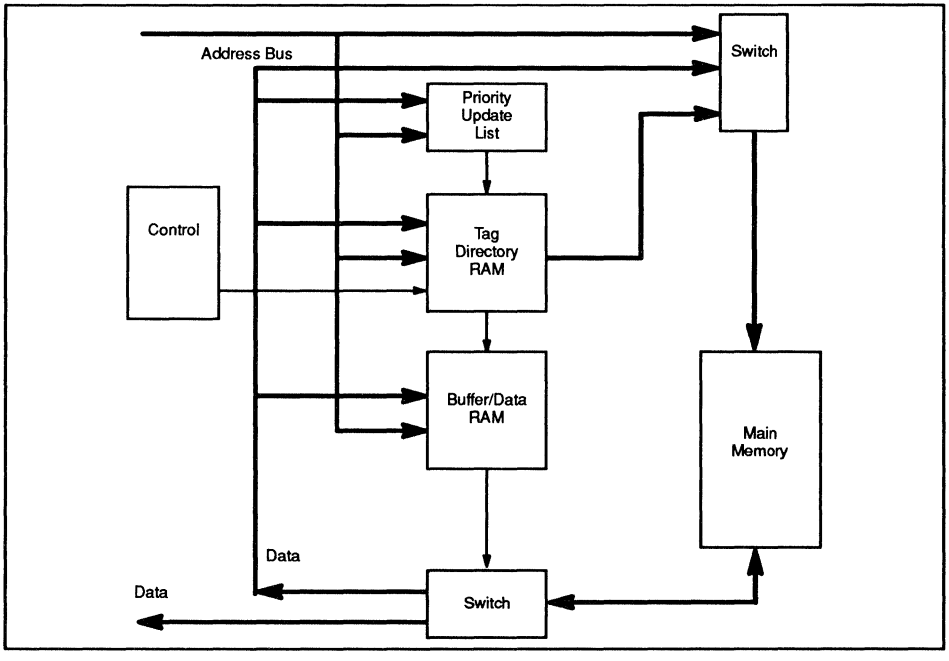

Figure 4. Typical Cache Memory Structure

Buffer Block

A cache memory is basically a small, high-speed memory with main memory information. This information may be addresses, data or instructions. Hence, the cache can be an address cache, data cache or an instruction cache. Its speed is typically an order of magnitude faster than that of the main memory, while its capacity is typically one or two orders of magnitude less than that of the main memory.

Tag/Directory Block

A cache memory system requires an identifier or tag store to indicate which entries of main memory have been copied into the cache store. Data in the large main memory has to be mapped into the smaller cache buffer, where it is partitioned or subdivided into small segments called blocks. Each block is identified with a label called the tag address. These tag addresses are stores in an associative RAM called the tag/directory RAM. It operates like a search memory.

Priority Update List

A buffered memory requires a logical network that selects words or blocks to be removed when the new entries (words or blocks) need to be brought into the cache. This structure is called the priority update list.

Control Logic

A cache memory system also requires control logic to generate all timing for synchronizing various activities; for example: searching the tag store, getting the data out of the cache, and replacing proper entries in the cache.

The operation of the total system is quite simple. Whenever the CPU requests the data from the main memory, the first operation that takes place is the matching of addresses coming from the CPU with the addresses inside the directory RAM. If this matches, then the data associated with this tag address is sent to the CPU. This is known as "hit" or address match. If the directory RAM does not contain the address being accessed by the CPU, then a "miss" takes place. When this happens then the data from the main memory is sent to the CPU. It will also be simultaneously stored in the buffer RAM. Hence, if this address is accessed again then the data will come from the cache.

The cache buffer design involve many parameters such as type of memory mapping schemes,(fully associative, direct and set associative), cache size, block size, data replacement algorithm, and a variety of other features which will not be covered in this paper.

In the earlier cache-based systems. the capacity and performance of main memory were modest in comparison to today's systems. Designers were using expensive bipolar RAM technology for performance considerations. Due to the improvements in semiconductor process technology, both bipolar and MOS, the size and performance of cache memories have continued to grow as shown in Figures 5 and 6.[2]

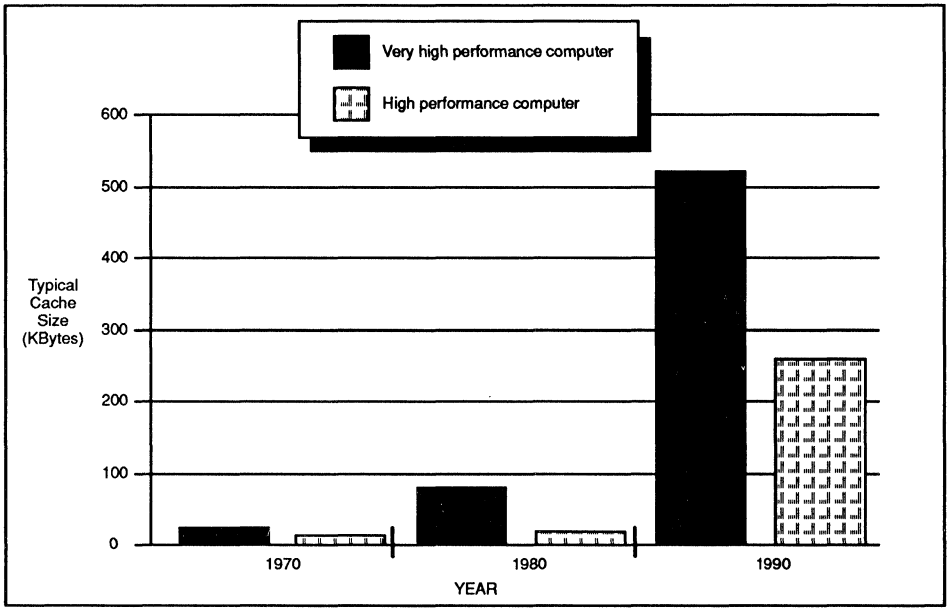

Figure 5. Cache Capacity Trends by Typical Cache Size

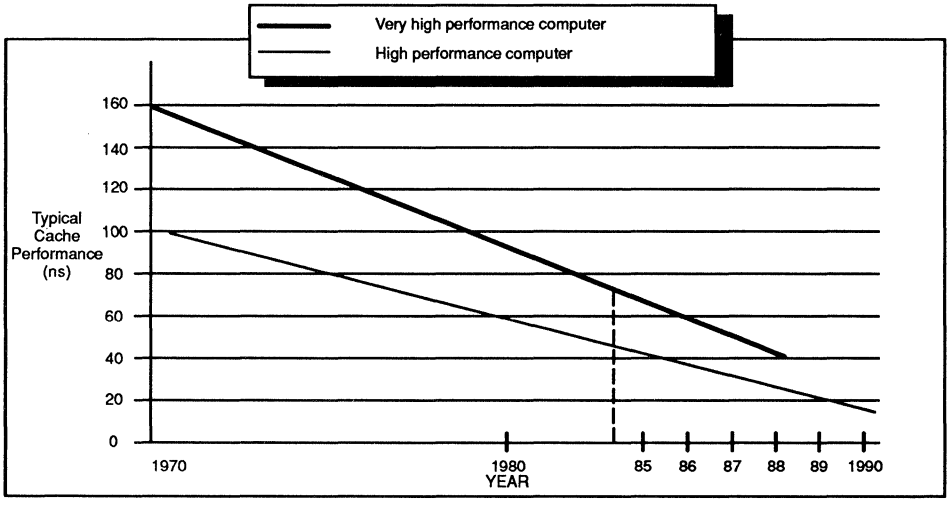

Figure 6. Cache Capacity Trends by Typical Cache Performance

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As shown in Figure 6, the typical CPU cache times are approaching 55 ns or less. As far as the performance or hit rate of the cache is concerned, it is primarily determined by the buffer size. Consequently, if a cache buffer size is large, in the order of 256K or 512K, the miss rate is low (see Figures 5 and 6.) Hence, a RAM 64K deep, will be an excellent choice. The third most important thing in the selection is the word width. Historically, a RAM with a large number of output drivers is slower than a device with fewer outputs because of high ground noise. Also, with wider word widths, the system designer usually winds up with a large number of unused bits/word. A by-1-organization would provide the highest performance and exact word widths but it will use a large number of devices. Therefore, a by-4-organization usually provides a more optimum alternative. This choice also affects the board layout.

The majority of by-4-bits and by-8-bits wide SRAMs have their inputs and outputs multiplexed over the same pins. This arrangement, however, increases turnaround and settling delays, thereby slowing system performance. As shown in Figure 4, if the tag and data RAM have a separate data input and output channel, then the glue logic for comparisons will not be followed by multiplexers and demultiplexers. Thus, a SRAM with a separate data input and output bus is ideal for this case. The Fujitsu MB81C86 is a CMOS 64K x 4 SRAM, with an access time of 55 ns, and a separate data input and output bus. For systems which require very high performance, without board layout constraints, MB81C71A (the 64K x 1 CMOS SRAM with access times as fast as 25 ns) from Fujitsu provides a unique solution. It is also useful for high-speed minicomputers and mainframe applications.

Building a Large Disk Cache

Real time interactive graphics and CAD systems are two high-speed computing applications which require a large on-line data base. Only mass storage can deal with such huge quantities of data. Disk drives, as well as the mag tapes are extremely slow, although their capacity is sufficient. These devices transfer data much too slowly for today's high performance mainframes, minicomputers, or microcomputers.

One solution is to place a semiconductor cache memory between the CPU and the disk subsystem. The cache should be large enough to hold a significant percentage of the data the CPU requires from an I/O device. This cache not only improves the disk data transfer rate, but also more closely matches the speed of the central processing unit of the host system. Incidentally, this cache will not place a heavy demand on the power from either the system or battery back-up.[4]

The Fujitsu MB81C81A-35/45 is a prime candidate since the cache would be several megawords in size. This is a 256K x 1 CMOS SRAM. This device has separate data inputs and outputs. In order to design a 512K bytes of disk cache, for an 8-bit wide data bus, only 16 of these devices are needed. If the host's main memory access time is 80 ns, then a 45 ns device shortens the system throughput time. A typical system is shown in Figure 7.

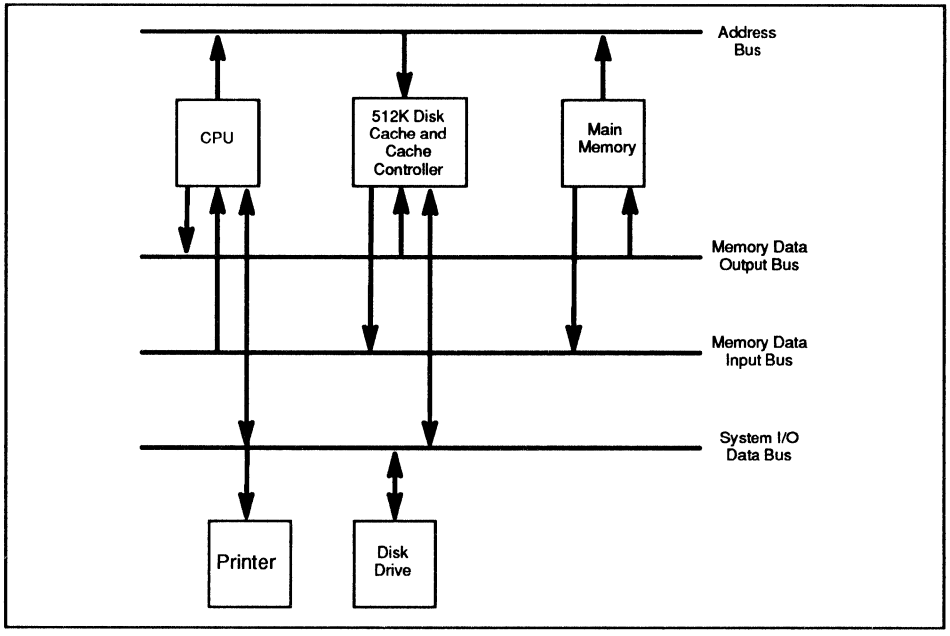

Figure 7. A Large Disk Cache for a Disk Drive Enhances System Performance

Building Deep FIFO Buffers

Separate data input and output SRAMs have a wide variety of applications. They are useful in building deep FIFO buffers. FIFO is a First-In-First-Out memory which can be implemented in different ways. The main function of this type of memory is to read out the data in the same order that it was written. The basic design of a FIFO implemented from the separate data input and output SRAM is shown in Figure 8.

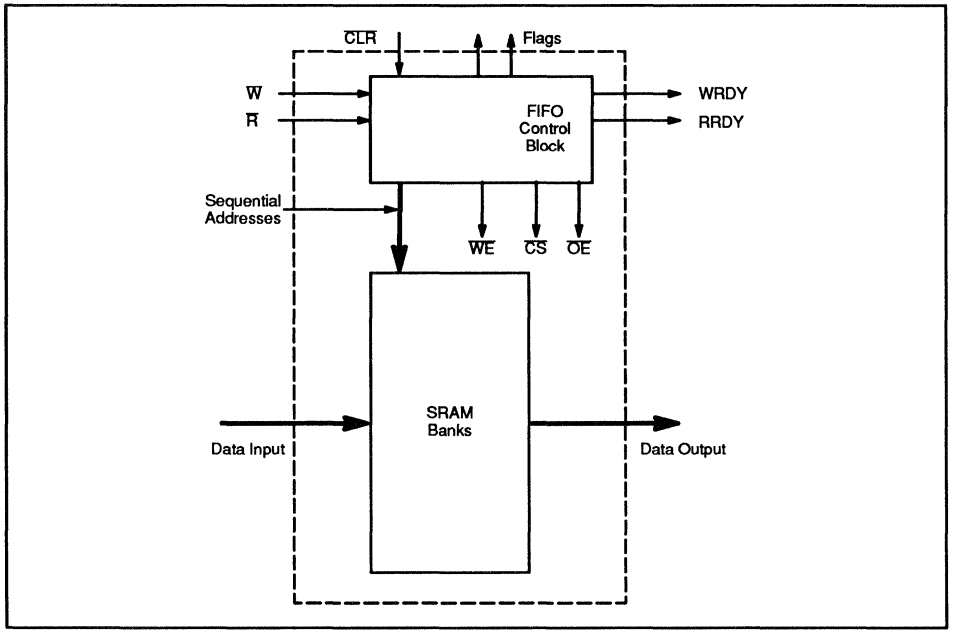

Figure 8. Basic FIFO Design

The FIFO control logic consists of two ring counters for generating read and write addresses. When the FIFO is empty, then both of these counters are initialized to location zero in the SRAM. In the case of a write to the SRAM, the write counter is incremented, thus pointing to the next empty location. The read counter always points to the full location; i.e., the location which has data written into it. When all the data has been read, and the read and write counters point to the same location, the FIFO control logic generates an empty flag. A full flag is generated when the write counter points to an address on less than the read counter. At this point no further data dumps ar allowed in the FIFO. This FIFO control block is commercially available as FIFO RAM controller, which can easily create 64K deep buffers from the separate data input and output SRAMs.

FIFO devices are marketed with onboard RAMs. These commercially available FIFO devices provide asynchronous operation, but are not deep enough for such applications as buffers for disk systems, printers, and local area networks where the data usually comes in the form of large blocks. Designers cannot afford to lose the data, consequently, the FIFO buffer should be large enough to hold the complete block. The deepest commercially available devices are 2K words deep.

In order to implement a deep FIFO buffer, it is desirable to have a SRAM with separate data inputs and outputs. This avoids the turnaround delays and muxes/demuxes. Another advantage of using the SRAMs over commercially available devices is that the data can be accessed by the CPU. Therefore, in the disk environment the error correction can be done on the fly. This is not possible in commercially available FIFO devices as they do not have an address Bus.

Conclusion

Fujitsu offers a CMOS 64K x 4 SRAM (MB81C86, with 55 ns access speed), 64K x 1 SRAM (MB81C71A, 25 ns access speed), 256K x 1 SRAM (MB81C81A-35 access speed) with separate data inputs and outputs. Also, all Fujitsu ECL SRAMs (deepest configuration available = 256K x 1 at 15 ns and the fastest available is 5 ns at 4K and 1k depth) have separate data inputs and outputs. The availability of separate data inputs and outputs SRAMs, help system designers develop not only an efficient system, but also a less expensive system because of smaller board space. The important application areas which exploit this feature are writeable control stores, cache memory systems, and deep FIFO buffers for disk controller boards and LANs.

References

1. Brick, Jim and John Mick. "Microprogramming Ups Your Options in Microprocessor System Design", *EDN*. January 20, 1978.
2. Brunner, Dick. "High Performance Cache Memory". *IEEE Conference Proceedings*. WesCon 1986
3. Pohm, A.V. and O.P. Agrawal. *High Speed Memory Systems*. Reston Publishing Company.
4. Hartwig, Knorpp., Mears and Osman. "Large Disk Cache Uses Fast 64K by 1 SRAMs to Speed Database Accesses". *Electronic Design*. September 19, 1985.

Appendix 3

Intelligent Cache Tag RAMs

November 1989
Edition 1.1

APPLICATION HANDBOOK

FUJITSU

The Effective Design of CMOS-based Caches in CISC- and RISC-based Architectures

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Manager, Applications Engineering

Fujitsu Microelectronics, Inc.
Integrated Circuits Division

Introduction, An Overview

This manual is intended to serve two purposes: to provide an extensive tutorial on cache design and to aid in the process of designing a tag buffer, Fujitsu's MB81C51, into the engineer's high-performance end system. This guide focuses on cache design, various cache architectures and system requirements. The appendix to this handbook supplies details on Fujitsu's cache tag RAM, the MB81C51. Theory and performance analysis of cache are covered in moderate detail; they are covered in greater depth in the references found at the conclusion of this Application Handbook.

The information contained within this Application Handbook, supplemented with the appropriate data sheet, is intended to address the majority of typical design-in issues related to cache design with Fujitsu's RAMs. However, if additional information is necessary for the designer's successful application of these devices, please contact the nearest Fujitsu Sales Office. (See the Sales Information Section.)

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Edition 1.1

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1. Caches: Growing in Popularity, Mysterious in Definition

As depicted in Figure 1–1, Fujitsu supports a number of devices for the implementation of cache in computers ranging from high-end ECL-based mainframes through ECL- and MOS-based minicomputers to rapidly advancing desktop 32-bit microprocessor-based computers. Fujitsu's broad line of standard and application specific MOS and ECL SRAMs are designed to address the needs of today's designers who are facing the memory implementation problems faced in years past only by mainframe and minicomputer designers. This new wave of design requirements and resulting innovations are largely due to the introduction of second generation 32-bit microprocessors, the growing popularity of micro-based multiprocessing systems, and the commercial acceptance of RISC processors, which boast unusually fast clock rates, and require one or two memory accesses per cycle. Consequently, memory performance, the fundamental bottleneck for most CPUs, must keep up with processor technology if the system performance is to improve. Even if main memory could keep pace, it can only match the speed performance of a dedicated processor. In multiprocessor systems, coprocessor systems and systems that best utilize DMA for I/O, sharing bandwidth is still the critical issue.

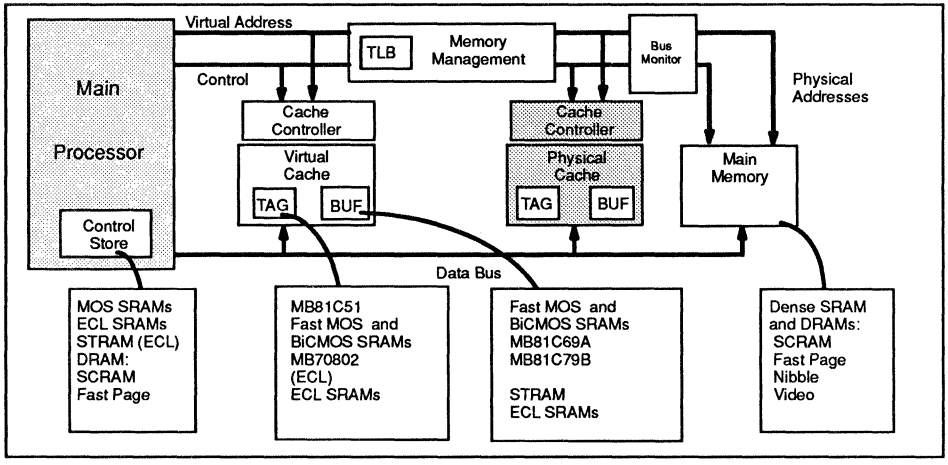

Figure 1–1. Fujitsu's Role in the Functions of a Computer-based System

1.1 Motivations for Using a Cache

Cache memory is an additional level of the memory hierarchy that performs two functions. First, it provides a cost effective way to perform a memory cycle in a time that approximates that of the local processor's memory cycle time. Secondly, by providing an additional level to the memory subsystem hierarchy, the cache isolates the local processor's high-speed bus from that of main memory. This extra level of high-speed memory permits main memory to be implemented with inexpensive DRAMs, and to continue to provide a wide bandwidth for other devices that access the main buffer, such as other multiprocessors, DMA channels, graphics processors and math coprocessors.

1.2 Cache Terminology and Implementation

Cache is implemented by mapping a subset of the main memory into another memory subsystem whose cycle time is less than the minimum bus cycle time of the local processor to avoid wait states. Cached entries reside in this high speed cache data buffer, which is usually implemented with CMOS or ECL Static RAMs (SRAMs).

1.3 Cache Association, Storage and Control

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Since cache supports only a subset of main memory, some way of identifying the original, or parent location in main memory from which the cached data originated is necessary, so that residency of a referenced instruction or datum can be determined (instructions and data will often collectively be termed data). A valid memory address will reference data located in one or more locations: local cache, main memory, or secondary storage (disk). To determine which is the case for a given memory access, cached data is stored with its associated address or *tag*. The tag is compared against the requested address to determine cache residency. Just as a request for data in a page that is not in main memory produces a page fault, so a cache reference that is not resident is termed a *miss*, while its counterpart is the always desired *hit*.

The tag buffer, best implemented with CMOS or ECL tag RAMs, interfaces to the *cache data buffer*, with which it is tightly coupled, and both are controlled by the *cache controller* that interfaces to the processor and the cache. The controller, responding to a processor memory cycle, initiates the interrogation of the tag RAM to determine residency, then takes the appropriate action, depending on whether the result was a hit or miss. These hardware functions and their relationship are represented in Figure 1–1, which also reveals the breadth of Fujitsu devices available to implement the tag and data buffers in both ECL and CMOS systems.

The last major cache system element is the *bus monitor/bus controller*, which observes the system bus (under most protocols) and controls access to and from the cache to main memory. To summarize, there are four functional blocks that make up the typical cache subsystem:

1. tag buffer
2. cache data buffer
3. cache controller
4. bus monitor

The implementation of the tag and data buffers will be thoroughly covered in this Application Handbook, while the controller and monitor will receive an overview.

1.4 Cache Performance Justification: The Principle of Locality

Because the cache is a subset of the main memory, it is susceptible to misses. These misses result in main memory accesses to read or write the missing data (usually by allocating and updating a line entry in cache). However, access to main memory suffers a delay penalty and, if such misses are frequent, cache may provide no obvious advantage except to isolate the processor from main memory. So why does cache work for buffers of surprisingly small size? Figure 1–2 shows a histogram of a program execution sequence that plots the frequency (mode) of specific, logical address references for a single task over a period of time. The results are not too surprising: the references tend to cluster, a phenomenon described as the principle of *locality*. Since programs often execute in loops or recurrently referenced procedures, and as instruction fetches are sequential in nature, the probability that a subsequent reference will be nearby in the logic address space is fairly high. While data references are not quite as orderly, they also tend to cluster because of frequent operations on data structures such as arrays, records and stacks.

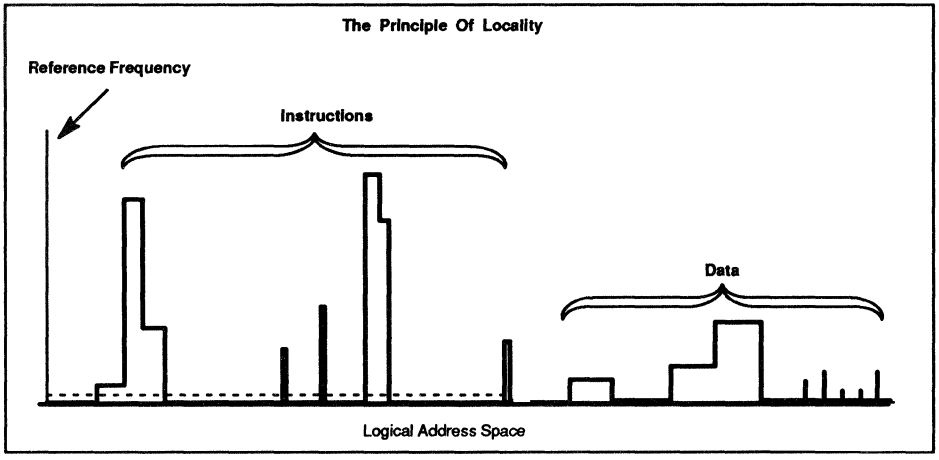

Figure 1–2. Typical "Clustering" of Instructions and Data Address References

1.5 Determining Cache Residency

Cache is defined by a number of protocols and parameters which explains its many and varied implementations in today's systems, each having unique requirements. These requirements include depth, block or line size, coherency and protocols, and *mapping* method of *look-up*. The latter impacts the structure of cache and the implementation technology, as well as performance, warranting its discussion in this introduction. There are three fundamental methods of look-up: direct mapped, fully associative, and set associative. Another, less popular method called sector mapped, which was pioneered for the IBM 360, uses a fully associative tag buffer mapping into large data blocks.

1.5.1 Direct Mapped

Direct mapped (Figure 1–3) cache uses an index as an address into two standard static random access memories (SRAMs). One stores the data/instructions and the other stores tags that correspond to the data buffer contents at the same address (index). The tag buffer data at that address is compared against the tag of the pending request. A successful comparison results in a hit, and a miss indicates the tag at that index differs. (The index represents the lower order address bits of the cache address while the tag represents the higher order bits, as illustrated in Figure 1–3).

The disadvantage with this scheme is that multiple code or data *lines* (a line is one or more words of data associated with a particular tag, also called a *block*) which map to the same index will exclude all but one line from being resident in cache at a given time. Potentially, this may lead to an alternating miss scenario similar to the problem of thrashing in paged virtual memory systems. The advantages of this scheme are that the implementation is simple and access to the data is fast, since the index addresses both the tag buffer and the data buffer simultaneously.

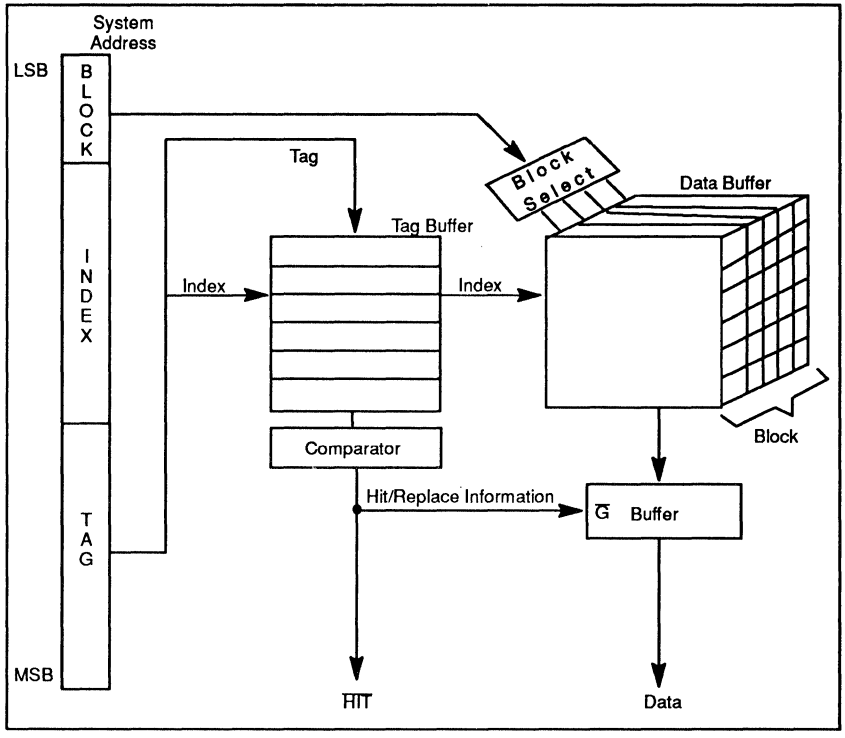

Figure 1–3. Mapping Methods: Direct Mapped

1.5.2 Fully Associative

Fully associative mapped caches, illustrated in Figure 1–4, solve the problem of index contention introduced by direct mapped caches by storing the entire address (sum of the tag and index) in a content addressable memory (CAM) which simultaneously compares the requested address against all entries. Therefore, a number of commonly referenced lines may be stored in cache up to the depth of the cache, and may be located anywhere in the mapped main memory without contention.

One disadvantage of this scheme is that before the line entry from the cache data buffer may be accessed, the determination of the hit and its location must first occur. Compared to direct mapped, this increases the overall cache access time by the access (hit determination) time of the tag buffer. Furthermore, because CAMs tend to be expensive, slow and small, they are more commonly used for Translation Lookaside Buffer (TLB) implementations and much less often used for cache tags. However, a more effective scheme exists: *set associative cache.*

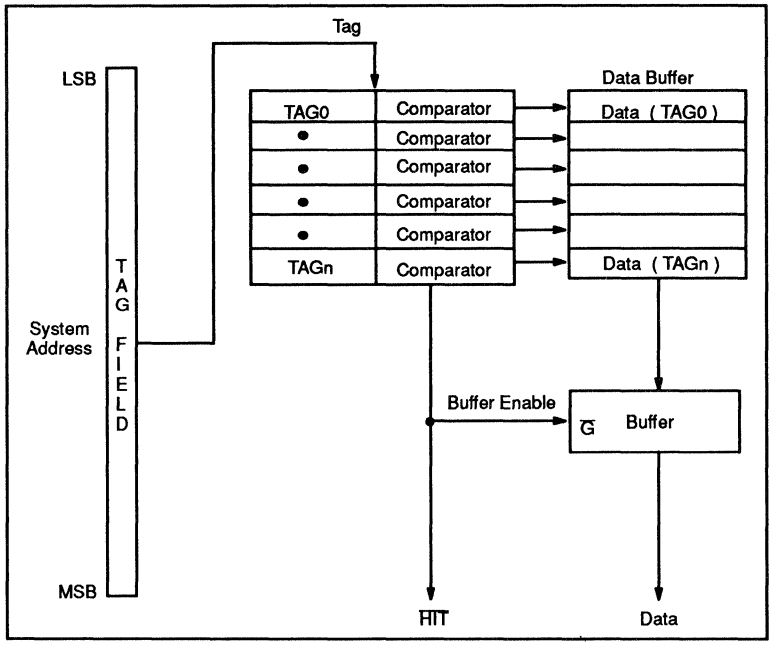

Figure 1–4. Mapping Methods: Fully Associative

1.5.3 Set Associative

A set associative cache (Figure 1–5) of N set elements (degree of associativity, or ways), permits N different line entries to map to the same index. As with direct mapped caches, set associative stores only the tag in a RAM and uses the index as the address for this tag buffer. By contrast, the index selects N different ways which are simultaneously compared against the tag to determine if a hit occurred, and at which set element it occurred. Since the set size is manageably small (2 to 4 elements), standard static RAM (SRAM) technology may be employed for both the tag and data buffer, thereby reducing cost, decreasing look-up time, and supporting large caches. Its primary disadvantage is that the selection of the set element in the data buffer is stalled until the tag buffer look-up is performed. Fujitsu has helped solve this problem with the development of fast SRAMs specifically designed for data buffer implementations (see Section 4.2).

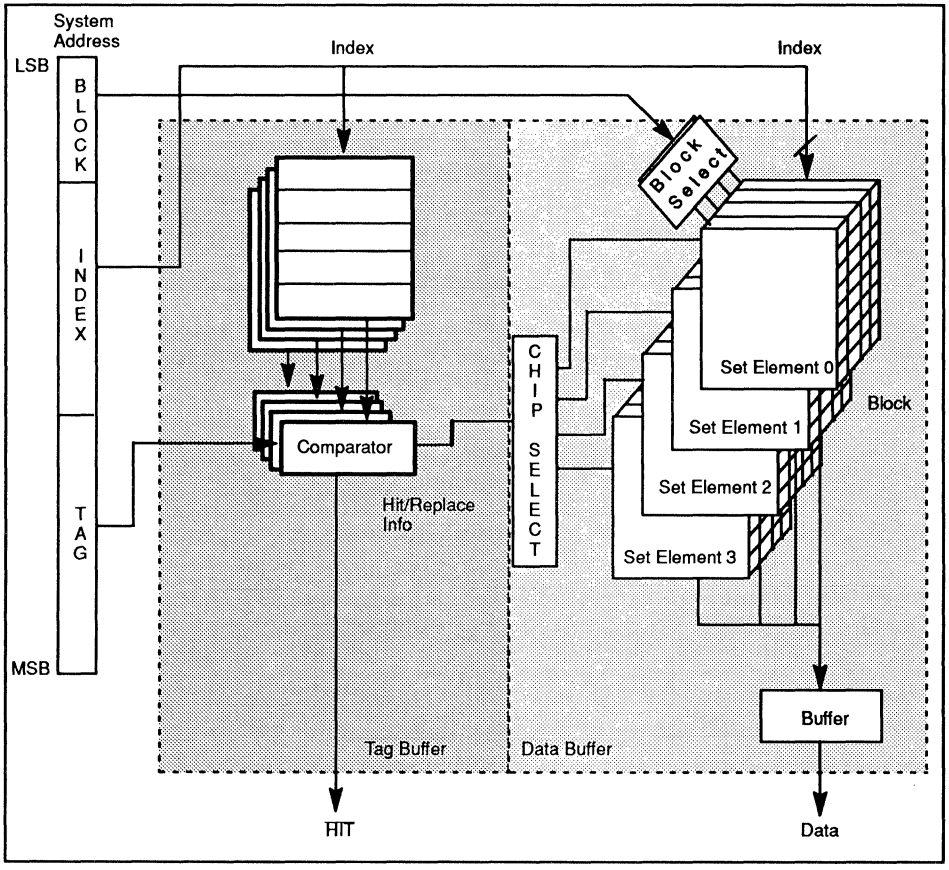

Figure 1–5. Mapping Methods: Set Associative

The most popular and generally accepted cache implementation is set associative, since it can be made to meet performance goals (average access time, hit rate and hit detection time) while still maintaining reasonable cost. Furthermore, although studies have shown that hit rate increases with degree of associativity, Figure 1–6 suggests that the greatest improvement in hit rate occurs when changing from degree equals one to two or four. The set size on the independent axis of Figure 1–6 indicates the degree of associativity, which is two or more for set associative mapping, but more commonly two or four. A degree of one is the case of direct mapping, while degree of N is the case of the fully associative implementation where N is the depth of the tag buffer.

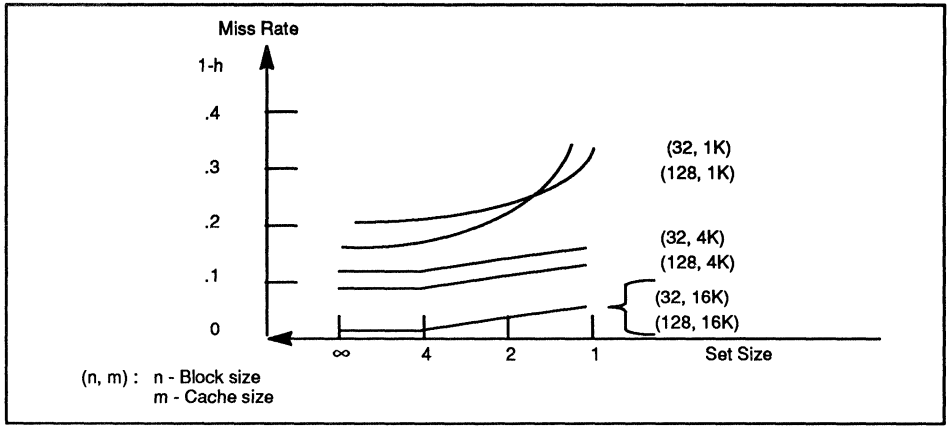

Figure 1–6. Efficiency of a Cache System

Fujitsu has implemented set associative mapping with the MB81C51. Therefore, it will be assumed that set associativity is being employed throughout our discussions.

1.6 Cache Coherency

Incoherency may result in bad side effects due to inconsistency between copies of the same data. Although it is not necessarily an error for cache and main memory to possess differing copies of the same line, if at any time the most current copy is not the one referenced or is mistakenly overwritten, then we have lost data integrity. There are primarily two situations in which coherency may be compromised if corrective or preventive policies are not imposed.

1. The local processor causes cache and main memory copies, as well as any other copies in the system, to differ by writing to the local cache buffer. This problem of locally affecting incoherency can be resolved by updating.
2. Another processor or an I/O device writes to main memory data that references a line cached somewhere else in the system. One method of avoiding this globally affecting incoherency is by bus monitoring.

Although the goal of cache design is to enhance system performance, more specific goals that can be empirically measured are often used as guidelines for design. One goal is to minimize average cache cycle time and a second is to maximize available system bus bandwidth (use as little of it as possible).

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These interdependent yardsticks of cache performance, along with practical issues such as design complexity and cost, are responsible for the division in the two fundamental protocols of cache coherency: *write-through* and *copyback* (or write-back). Write-through schemes are simpler and inherently exhibit higher data integrity, while providing moderate performance. This makes them ideal for the high performance desktop and deskside workstations and business computers which require low cost blended with high performance. A variation known as buffered write-through is well suited for the very high performance desktop/deskside systems such as workstations, because it provides for optimal average cycle times. There are so many factors associated with and impacted by any given coherency protocol that Section 5.0 has been dedicated to this subject.

1.7 The Concept of Virtual and Real Caches

Virtual cache is one that is referenced by virtual addresses, while a *real cache* is one that accepts real addresses such as those addressing physical main memory. Therefore, in virtual memory systems using a real cache, a memory management unit (MMU) resides between the cache and the processor. A virtual cache, by contrast, does not translate the address unless main memory is to be referenced, (although the translation normally proceeds concurrent with the tag inquiry to minimize delay, should a miss occur). The placement of the MMU, determined by the use of a real or virtual cache, was shown in Figure 1–1.

Whether virtual or real caches are employed affects the coherency protocol as well as the address translation and the overall construction and operation of cache. Section 6.0 provides application recommendations which consider the effect of virtual or real cache on the design of the cache subsystem.

1.8 Summary and Introduction

The cache, as a high-speed local memory storing a subset of main memory, offers the advantages of zero wait state memory cycles at a cost that benefits from permitting DRAM primary memory to store the bulk of the data. As an added level of memory hierarchy, it isolates the processor from demands for the system bus and restricts system bus accesses to miss-induced replacements, I/O space accesses, non-cachable data references and other general system bus routines.

Having reviewed some of the basic cache concepts and terminology of cache, as well as the fundamental theory and mapping mechanisms, we are now prepared to investigate the operation and function of the Intelligent Cache Tag RAM, followed by its system integration.

2. Supporting Operations Initiated by the Processor

Certain general operations that the cache must perform are dependent upon processor-generated states and system bus-generated states. This section briefly addresses these operations, their detection and invocation. Set associativity is the assumed protocol unless otherwise indicated. Fujitsu's MB81C51 Cache Tag RAM is used to illustrate the buffer construction. For more information on this device, refer to Appendix 1.

2.1 Responding to Processor Bus Actions

The cache system must perform the following functions in interfacing the local processor:

1. The cache system must be able to determine whether the current bus cycle initiated by the processor is one in which cache should participate (a cache cycle).
2. If the current bus cycle is a cache cycle, the cache system must respond appropriately to the request by either executing a cache cycle or suspending the processor until the request can be satisfied.
3. In the case of a non-cache cycle (such as a graphics I/O port operation that is not cached), the cache system must become dormant or inhibited and must not provide contention when the processor wishes to bypass the cache.
4. The cache system must perform all necessary functions, requested by the processor and/or its co-processors that may access the local cache (read, write, cache flush, invalidate entry, disable cache). These functions may be performed with or without the processor's direct control, depending on system requirements (whether software or hardware controlled functions are implemented).

The state diagram in Figure 2–1 describes a generic controller that can perform such operations. These operations, such as selective invalidation, may not always be initiated by the processor, but the example should provide an understanding of the initiation of operations and their function.

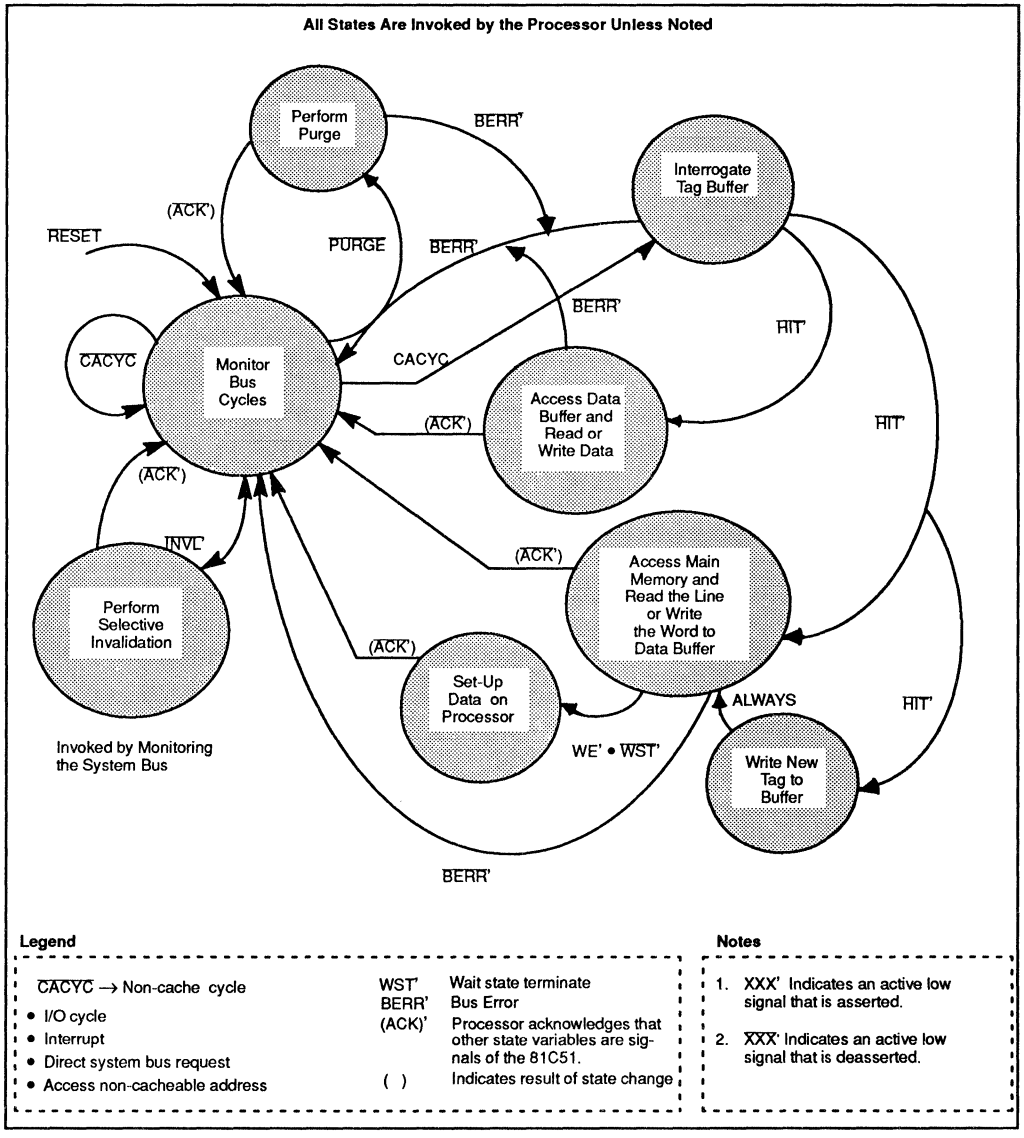

Figure 2–1. State Diagram of Cache Controller

2.2 Performing a Cache Cycle

Cache, because of its performance requirements and complex timing considerations, is tightly coupled with the processor in use. Therefore, this section will discuss how processor and cache signals are coordinated to perform read and write functions.

2.2.1 The Sequence of Performing a Cache Cycle

During processor data/instruction cycles, the processor initiates the cycle by driving address and control signals (READ/WRITE, FUNCTION CODES, MEMORY/I/O indicator) and an ADDRESS STROBE, CLOCK and/or other qualifying signals to sample the CONTROL and ADDRESS lines. At this time, the cache must quickly determine whether the current bus cycle is one it should participate in, or whether it should back off.

If the access is to cache, then the cache controller enables the processor address to the index and tag inputs of the tag buffer while also driving the index, block address and byte select signals to the cache data buffer. As the tag buffer is performing an interrogation to determine residency of the requested entry, the data buffer is being addressed by the index, block and byte addresses.

2.2.2 Executing the Cache Cycle on a Hit

When the tag buffer indicates a hit has occurred by asserting HIT' the HIT/REP (set element selection) is used to select data that corresponds to the set element forcing the tag hit. Depending on the timing requirements of the processor, an ACKNOWLEDGE signal (which will generically be called ACK) is usually generated from the HIT' at this time. Once the data is selected from the data buffer, it is set up on the processor's data bus with sufficient set-up time to be clocked by the edge terminating the bus cycle.

In the read cycle, the timing of the ACK to the processor and the data from the cache data buffer are the most critical. An example of cache timing in a 68020 environment is depicted in Figure 2–3 using the synchronous timing mode of the 68020. Since set associative caches do not generate set element selection information until the time a hit is determined, the data buffer enable time is quite important. Section 4.2 deals with alternatives in the construction of the data buffer to minimize this delay.

In the case of a processor memory write cycle, the tag buffer is also interrogated but, when HIT' is asserted, the data buffer (already enabled for a write) is written to as the HIT/REP signals select the set element. If a write-through coherency scheme is employed, then main memory is written to concurrently with the cache write.

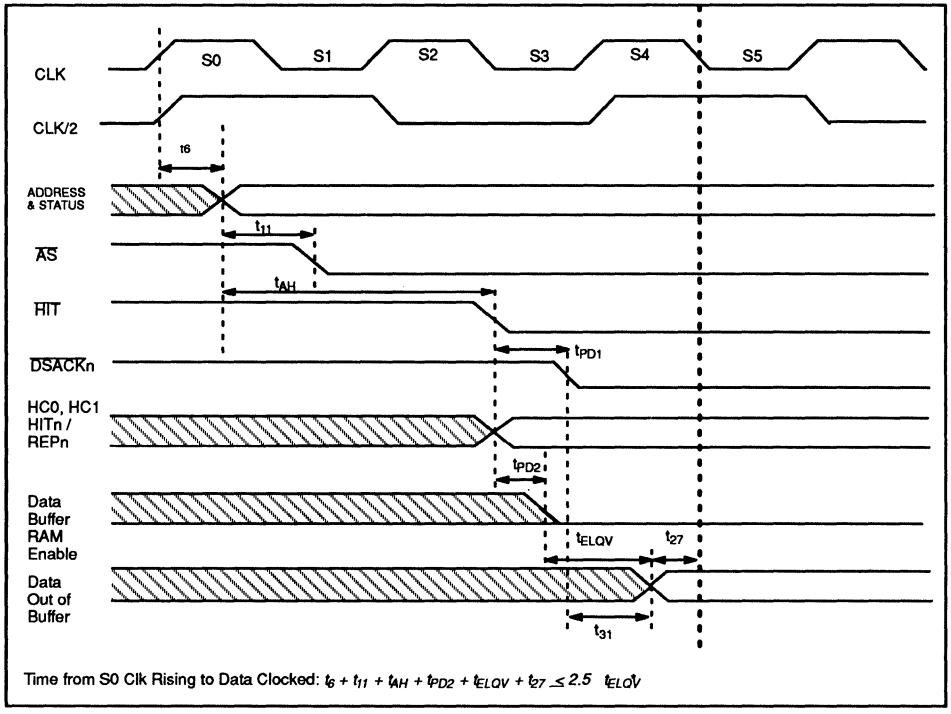

Figure 2–2. Cache Timing of a 68020 Environment

2.2.3 Cache Hit Sequence (81C51 to 68020)

An example of interface timing is shown in Figure 2-2, which illustrates the important timing relationships in interfacing Fujitsu's 81C51 to a processor such as the 68020. The address, which appears after t_6, drives the cache buffer directly, saving the delay of waiting till AS' appears t_{11} later (though there is no reason the address could not be registered by the qualifying AS and CLK'). The HIT' and HIT/REPLACE information appear t_{AH} later and generate the acknowledge (DSACK') and data buffer enable signals, as well as others. t_{ELQV}, the chip select access time is, at this point, the only major component of delay remaining before data is retrieved and set up on the processor t_{27} in advance of the falling edge of the S4 CLK. The inequality shown at the bottom of Figure 2–2 represents the requirement to meet zero wait-state cache operation, given the described configuration and timing.

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2.2.4 Executing the Cache Cycle on a Miss

When a cache read cycle results in a miss, the requested data must be retrieved from main memory and written to the cache and the processor. A *slot*, or new line, must be allocated in the tag and data buffers to accommodate the missing tag and line. The determination of this slot is performed by the cache tag buffer or cache controller using an algorithm in hardware. To retrieve the data, cache requests access to main memory and fetches the line containing the missing data. The tag is then (or often concurrently) written to the tag buffer to validate the cache line. The fetched line is then written to the data buffer and

the requested word is set up on the processor. The ACK, which has remained deasserted up to this point, is now asserted, thereby terminating the bus cycle.

In the case of a write cycle that misses, precisely the same sequence occurs, including the fetch of the line from main memory (unless the block size equals one). Since a write operation is of one word, the other words in the block are unaffected; they must be copied into the data buffer and then the write may be performed on the affected line entry. For a higher performance, there are existing variations that involve registering the data to be written and updating the data buffer after the processor's bus cycle has been terminated.

2.3 Selecting the Optimal Replacement Way: the LRU Algorithm

H/R# is a signal that determines whether the tag inquiry references a replacement or searches for a hit. When a miss occurs, the H/R# input is cleared (LOW) in order to select replacement data for two purposes. The first purpose is to select the set element to be written into the data buffer (using the external HIT/REP outputs) and the second purpose is to enable the way in the tag buffer to overwrite (using the internal HIT/REP signals). The H/R# signal selects a 2:1 mux which passes either the hit information about the individual way's hit, or the replacement data which is driven by the least recently used (LRU) logic. This LRU logic maps data from the LRU table into enable signals that indicate which set element at that index is the "oldest" and thus prime for replacement. The inverse of this logic function also updates this table when read, write, and selective invalidation operations are executed, as shown earlier in Figure 2–1. There are three updates that are performed on the LRU table: initialization, forward update, and inverse update; a more detailed discussion of these updates follows.

2.3.1 Initializing the LRU

When the tag RAM is initialized by asserting the PURGE' signal, the validity bits for each entry (and all set elements) are reset to indicate cache is empty; thereby making all set elements invalid. At the same time, the LRU table is reset to a known, defined state shown in Figure 2–3.

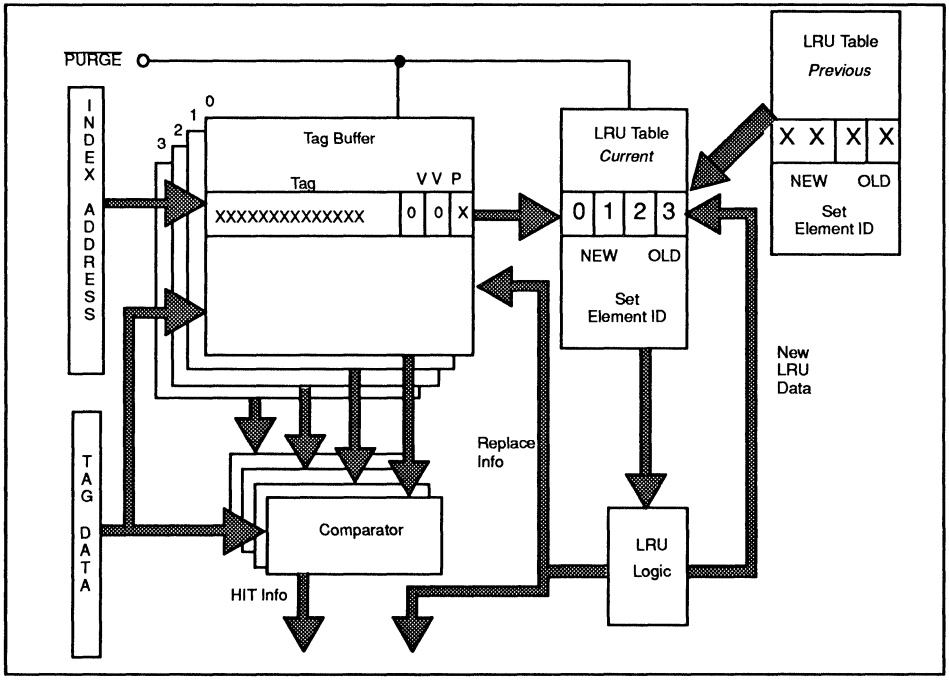

Figure 2–3. Initializing the LRU

2.3.2 Forward Updating of the LRU Table

When an inquire mode read cycle occurs (SET' kept high during the read), it has no effect on the LRU table: nothing ages, nothing regresses. However, an update mode read operation in which a hit occurs or a write operation, both modify the table to reflect that the referenced element in the set is the most recently referenced. As an example, assume the LRU table has been initialized as shown in Figure 2–3. The processor initiates a cycle and the tag buffer is interrogated at index 001H. The tag on TD0..TD19 matches that of set element #2, indicating a hit that, as SET' is asserted, modifies the LRU state to reflect that #2 is the youngest, or most recently used. This is illustrated in Figure 2–4.

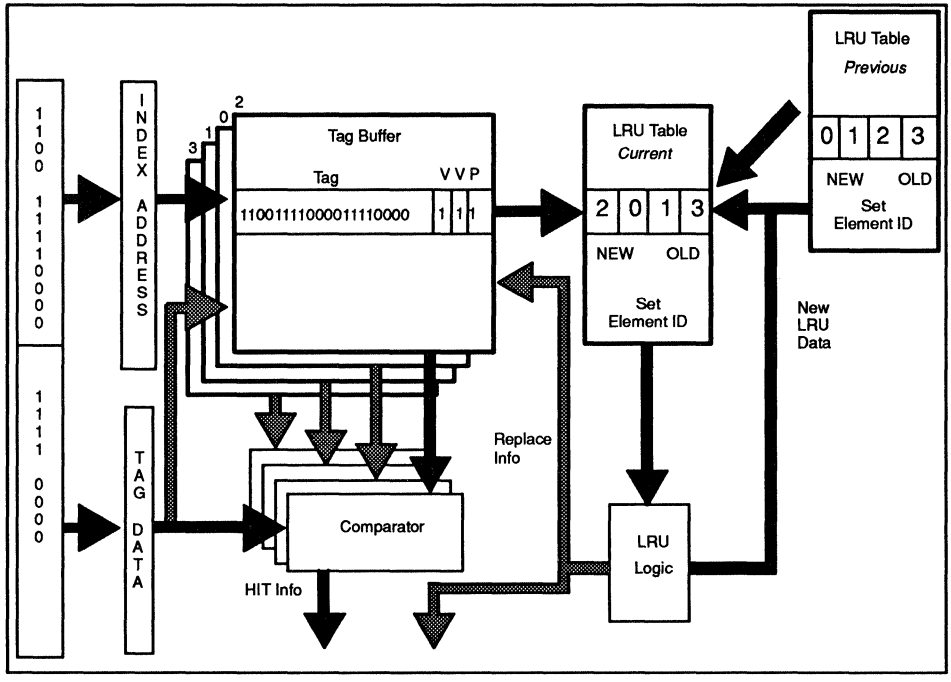

Figure 2–4. Forward Updating the LRU

2.3.3 Inverse Updating of the LRU Table

Selective invalidation clears the validity bits of the set element selected by either explicit invalidation (selecting the set element from signal pins, such as the SB0/SB1 signals of the MB81C51) or implicit invalidation (performing a tag comparison to determine the set element, then incuding it). Since the element that is invalidated is the preferred one to replace, the invalidation cycle modifies the LRU table so that the invalid element is now the oldest. Since this ages the element and has an effect that is the complement of the forward update, it is termed an *inverse update*, because the update algorithm is essentially applied in reverse.

Using the existing example (after the forward update), let's say that we implicitly invalidate a tag that hits element #2 of index = 001H. The element hit is inversely updated and the LRU table is modified at the assertion of SET' to the state indicated by Figure 2–5.

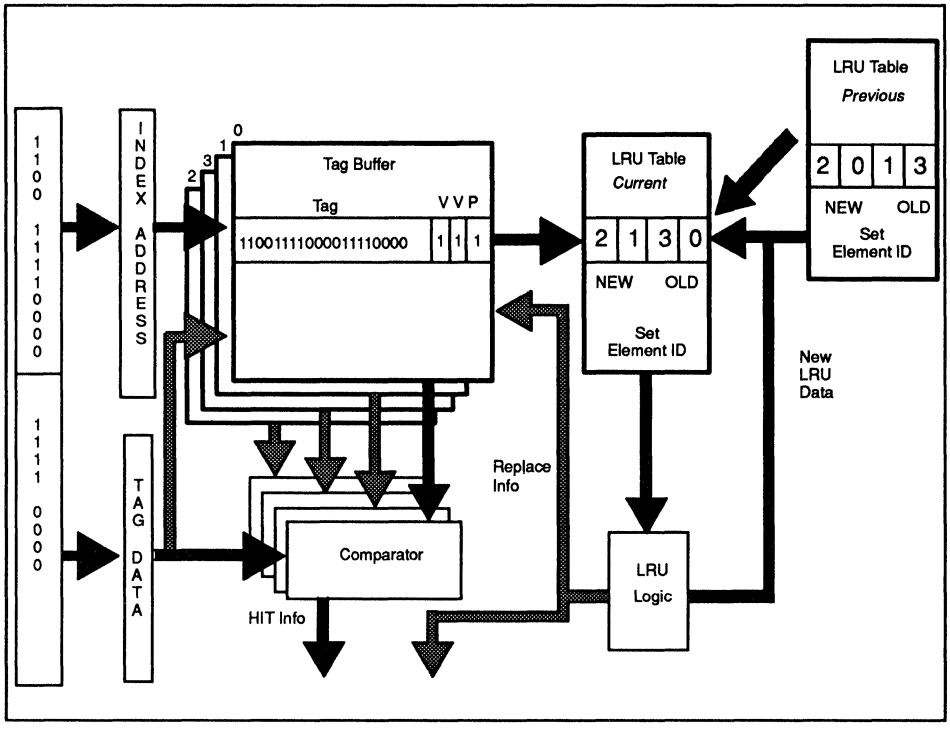

Figure 2–5. Inversely Updating the LRU

3. Constructing the Cache Tag Buffer

This section will discuss the hardware configuration based on the specification of parameters such as set size, depth, and tag size.

3.1 Choosing the Index and Tag Size

The size of cache is defined in terms of its depth (D), block size (B) and degree of associativity (W) in the following way:

Eq 3.1

$$cache\ size = D * B * W$$

Since the index is used to address the cache in depth, the size of the index address field should be (in bits):

Eq 3.2

$$index\ size = LOG_2(D)$$

As an example, if we have a two-way cache with a block size of 4 words, an 18-bit tag, (2-bit byte select) and a 10-bit index, we then have a cache buffer that is $2 * 4 * 2 * 2^{10}) = 8K\ 32\text{-}bit\ words$, with a tag buffer depth of 2K tags. This 32K byte cache can be implemented with a single 81C51.

3.2. Effect of the MMU on Hit Access Time

For systems that use virtual memory, the address consists of two fields, a page number and an offset. The page number is virtual and must be translated into a page frame number that maps to main memory, and the offset is real or not translated. In the TLB translation, the page number field incurs a delay relative to the offset. This delay does not occur when the MMU is on board the processor and the entire address becomes valid simultaneously.

Set associative tag buffers generally provide a faster hit access time from tag transition than from the index. If the index, lower order bits and page offset share the same bit field of the address, as shown in Figure A–1–9, then the TLB translation delay can be effectively reduced by up to (t_{AH}-T_{TH}), the difference in the index and tag access times. Therefore, the worst case hit access time, including the MMU delay, is defined as:

Eq 3.3

if $$t_{MMU} > (t_{AH} - t_{TH})$$

then $$t_{HIT} = t_{AH} + (t_{MMU} - (t_{AH} - t_{TH}))$$

Eq 3.4

if $$t_{MMU} \leq (t_{AH} - t_{TH})$$

then $$t_{HIT} = t_{AH}$$

where t_{MMU} is the delay (translate) time of the MMU, and t_{AH} and t_{TH} are the index address to hit and the tag field to hit times, respectively).

However, if any part of the page number maps into the index field, then that part of the index field must propagate through the MMU. In the event of such a propagation, the worst case cache access time becomes:

Eq 3.5

$$t_{HIT} = t_{AH} + t_{MMU}$$

Thus, in real cache implementations where a MMU skews the higher order address bits, optimal hit access time occurs when the page offset is *at least* the size of the index field plus the byte and line address (all in bits per address field).

Eq 3.6

$$PAGE\_OFFSET \geq INDEX + BYTE\_SEL + BLOCK\_ADDR$$

3.3 Configuring the Tag Buffer Given the Tag Size

As discussed in Appendix A–1, the address is comprised of a tag field, an index field, and a block and byte select field. Thus there is a proportionality between the field sizes and the address width (see Figure 3–1). For a given address width, say 32 bits, increasing the cache tag buffer size results in reducing the tag size, because the index field increases while the address size remains fixed. For these reasons, a tag size of 20 bits is, typically, more than adequate. However, cases may arise in which larger tags are needed. One case that may be an example is the new RISC processors which drive the virtual address space field with a page number and offset to be translated. If the cache is virtual, it may well see an unusually large address which requires a larger tag. Fujitsu's MB81C51, for example, supports a 20-bit tag field. If larger tags should be necessary, they should pose no particular hardship on the MB81C51, as the following application information will show.

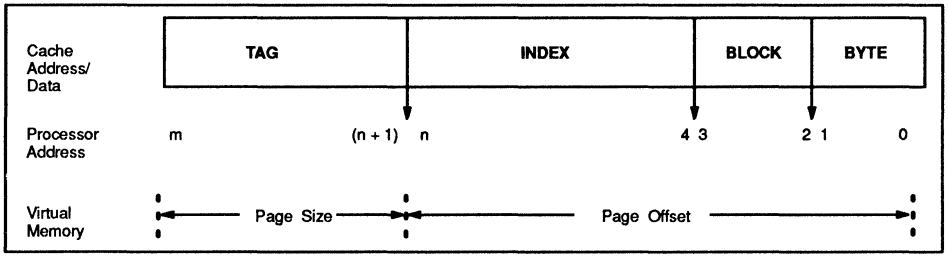

Figure 3–1. Address Bus Fields

By applying all inputs to multiple tag RAMs in common, with the exception of the unique tag fields, the width of the tag buffer and, consequently, the tag size can be enlarged. Figure 3–2 provides an example of a circuit that supports a 40-bit tag and a cache size of 2K lines configured as two-way. Notice that the outputs must now be gated and the timing sequence will change, since the LRU update on the read cycle (and the implicit selective invalidation) now require a hit to occur in both tag RAMs in parallel before the entire buffer is considered to be "hit." The operation of this circuit is described as follows.

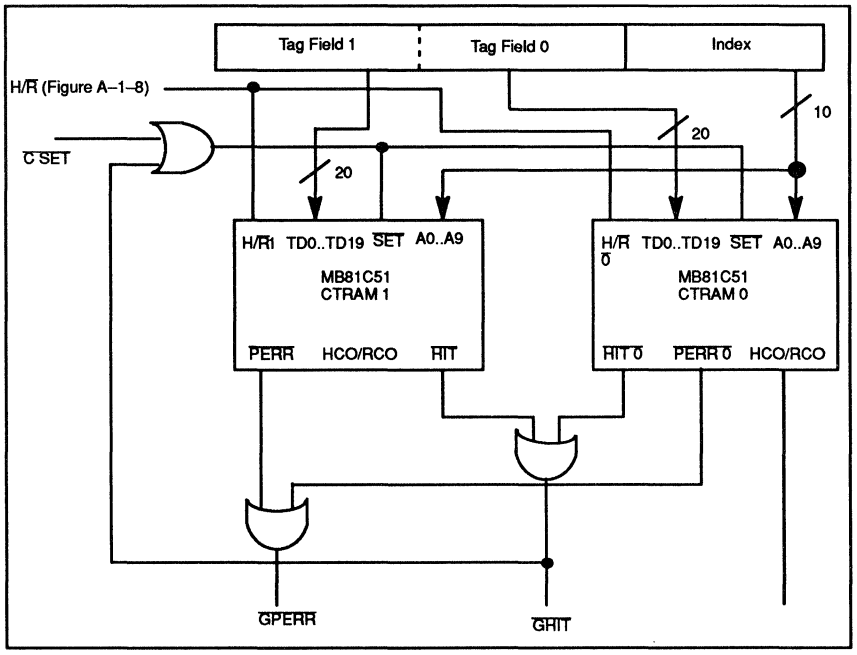

Figure 3–2. Implementation Example for Wide Tags (>20 Bits)

3.3.1 HIT Detection on the Read Operation

Index, decoded tag (split fields as shown) and other inputs, except SET', are applied in the same way as in the single width case. The individual HIT' lines are ORed to produce the global cache hit signal (GHIT') and used in the same manner as HIT' to generate system control signals. Notice that the gating of HIT' is such that all devices in parallel must assert their respective outputs to assert a system HIT'. This is necessary since all parts of the tag field must match in order to have a complete match. This is different from the method described in Appendix A–1.10 (stacking devices in depth) in which a hit in any one device indicates a complete cache hit.

3.3.2 Updating the LRU

The LRU table should only be updated when both RAMs, in parallel, are hit (GHIT' asserted). Since SET' updates the LRU, its assertion can be delayed until the global hit is detected. The effect of this approach is to increase the hold times of the tag, index and the other input signals.

Furthermore, selective invalidation that depends on a hit for execution (implicit invalidation) must wait for GHIT' to assert SET'. If the invalidation is initiated but SET' is never asserted (as the result of one or more of the tag fields not matching), then no invalidation will occur.

The purge and write operations can be performed in the same manner as in the single width case; therefore, the WRITE' and PURGE' signals can be tied common, as can INVL' and all inputs except the tag data.

Since the LRU table of all devices in parallel is modified in unison, the tables will be identical. Therefore, the HIT/REP outputs of either device can select the data buffer set element. In fact, the duplication in the LRU buffers could be utilized in fault tolerant systems with the aid of hardware comparison circuitry.

3.4 Relating the Index and Tag to Main Memory Mapping

Index and tag field sizes relate to main memory because they create a type of partitioning of main memory (similar to the way that paging partitions memory into frames). Figure 3–3 illustrates how the choice of index and tag size affects this segmentation. These field sizes, combined with the way in which data and instructions are stored in main memory, influence the hit rate and establish that there is an important relationship between the compiler, the operating system and the hardware architecture; i.e., the combination gains an optimal performance. Therefore, this can be a helpful model not only for hardware engineers, but compiler, linker and loader writers as well. Furthermore, this model is quite useful for the designer when defining fixed function memory segments (I/O space, frame buffers or other buffers) and fixed shared memory spaces.

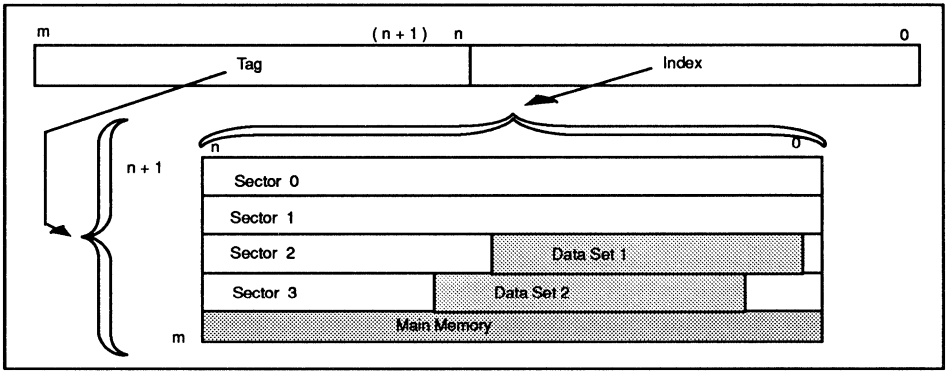

Figure 3–3. Effect of Tag and Index Fields on Main Memory Partitions

Using this model, a vertical line drawn down through all the sectors represents the largest set of tags that can have the same index. If, during program execution, the "working set" of main memory pages happens to include data or instructions having the same index, then some cache entries may be replaced by other data (if the number having the same index exceeds the set size of the cache). This is demonstrated in the model in Figure 3–3 by observing that the constant index line (vertical) "cuts" more addresses in the working set than the degree of associativity of the cache. Therefore, the choice of the tag and index size, as well as the degree of associativity, are all interdependent with software and quite important in guaranteeing a successful cache implementation and utilization.

4. Construction of the Cache Data Buffer

Up to this point, the focus has been on the implementation and characteristics of the tag buffer. Once a hit or miss has occurred, upon interrogating the tag buffer, the next action usually involves reading from or writing to the data buffer. This coordination requires a close coupling of the two buffers, an important consideration in the construction of the tag and data buffers.

4.1 Interface Between the Data and Tag Buffers

The tag buffer stores addresses which correspond to data contained within the cache data buffer. Therefore, it is the data buffer, comprised of SRAMs (such as Fujitsu's MB81C69A, MB81C78A, or MB81C79A) or special purpose data buffer device (such as the MB81C79B), which stores the actual instructions and data.

For example, in order to select a data entry, an index address, a set element (generated by the tag buffer) and a block, address and byte enables are used to define where the referenced data resides. The index applied to the tag buffer simultaneously addresses the data buffer. While the tag comparison in a read cycle is being performed, the known addresses are used to access the data buffer (a read cycle will be used throughout this section as an example). The known addresses are the index, block, and byte enable signals. However, since the HIT information is not generated until the HIT access time after address transition, t_{AH} becomes a gating factor in retrieving data from the buffer when it is present in cache. The following schemes of constructing buffers attempt to minimize this delay.

4.2 Fast Selection of the Proper Set Element (Way)

The time to select the set element after hit determination is critical enough to warrant a discussion of tradeoffs in speed, convenience, memory size granularity, and implicitly, cost. The following are three fundamental approaches to data buffer design that consider the set element selection delay.

4.2.1 Element Selection: Chip Select or Output Enable

Figure 4–1 depicts a scheme in which the outputs of all set elements for all common data bits are wire-ORed and depend on the output enable signals (G') or chip selects (E') to select the particular element using the HIT select outputs of the tag buffer. Each HIT drives a group of chip selects that select the set element; then each group is further qualified by the byte enables. This method selects the element in a time constrained by the chip select access time. CMOS SRAMs such as Fujitsu's MB81C69A, with chip select access time faster than address access times, are ideal for this implementation.

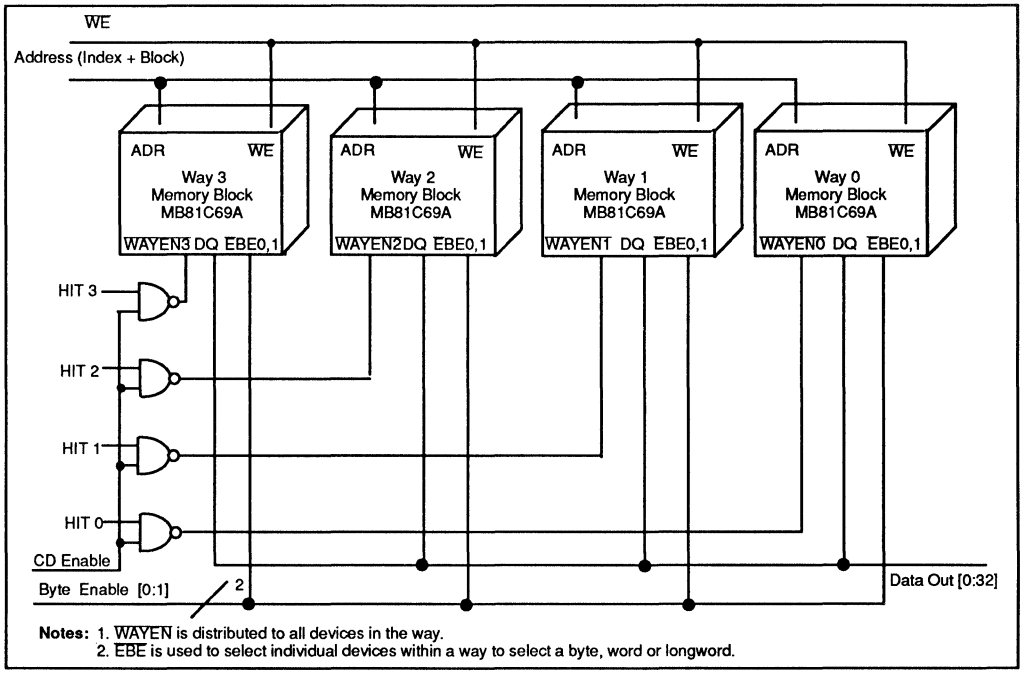

Figure 4–1. Cache Data Buffer Set Element Selection by Decoded Enables

4.2.2 Element Selection: Encoded Address Inputs

If the HIT/REP signals are encoded, they may be used to directly drive address inputs of the data buffer RAMs, provided the last address access time of the RAMs is sufficient to guarantee data selection time (see Figure 4–2). (See Figure 4–2). This would also permit finer granularity of the memory devices used for cache memory since four ways (or two) would be combined into one memory device, reducing the depth by that same factor.

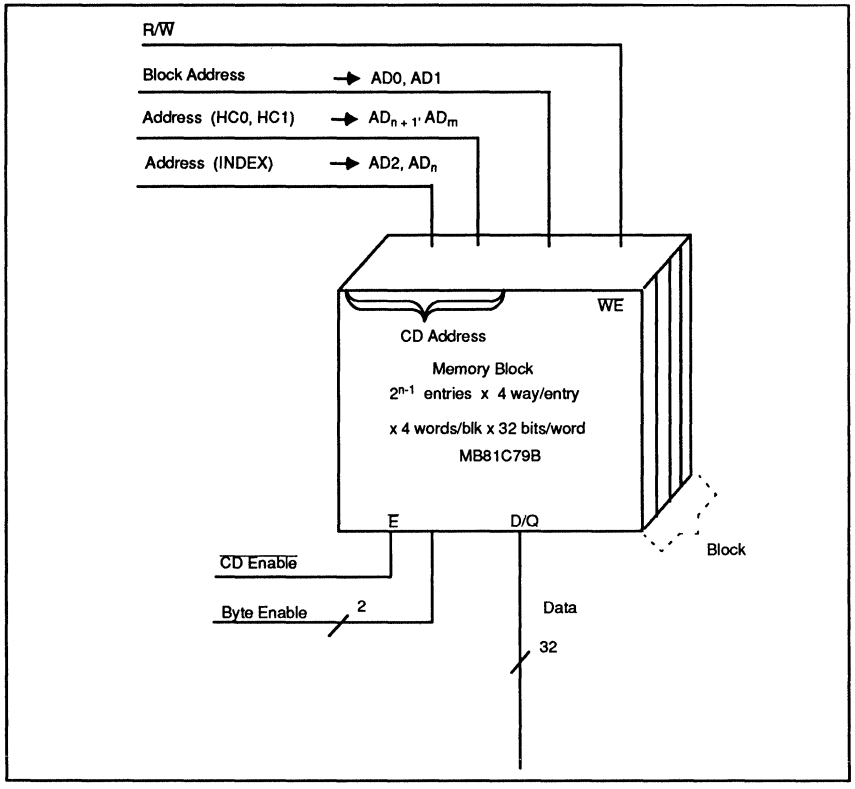

Figure 4–2. Cache Data Buffer Set Element Selection by Encoded Address

This approach may be useful in systems which can afford the address access time in addition to the HIT access time, need finer granularity of the cache memory depth or utilize innovative "nibble access" SRAMs by Fujitsu.

4.2.3 Element Selection: Application Specific Devices

Fujitsu's MB81C79B is an example of a memory designed especially for cache implementations (though it suits other implementations). It supports a wide word width (9 bits), fast column address for fast addressing of line elements at a faster access than the remaining address bits. Fujitsu will continue to develop devices architecturally suited for specific cache implementation.

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4.3 The Implementation of Split Caches

In systems based on the Harvard architecture in which data and instruction buses are disjointed and simultaneous fetches can occur on both, dual caches exist to support the buses independently. The same is true of modern Von Neumann processors that possess multiple bus paths and caches for data and instruc-

tions, such as the Motorola 68030 or the Intergraph Clipper™. These are examples of split caches that discriminate by data type (data or instruction). Split caches may also separate user from supervisor space, or a four-way split cache may distinguish both types of characteristics.

4.3.1 Data/Instruction Caches

Many general studies have failed to show conclusively that split instruction/data caches in Von Neumann machines are necessarily better than combined caches [Alexander, '86]. However, studies have shown that instruction references are more localized over time averaging than are their data counterparts. The discussion of this phenomenon will not be addressed here. but the references at the conclusion of this Applications Handbook offer additional sources. The construction of split caches and consideration of their performance merits follows.

As Section 5 will describe, the control of modifiable data is complex and ties up the cache with additional overhead. By splitting the caches, the control of the instruction cache (assuming code cannot be modified) becomes much simpler since instructions will not be locally modified, thereby reducing the opportunities for incoherency and simplifying the cache control logic. Additionally, the reduced logic overhead may provide for faster instruction fetch times, particularity important for RISC architectures employing single-cycle instruction execution. Furthermore, with proper bus isolation, it is possible for the processor to access the instruction cache while the bus monitor accesses the data cache. The very sequential nature of the instruction addressed could also be used to the best advantage. Certainly if the processor is Harvard-based, the split caches would be the natural implementation choice. Obviously, there are many advantages of split caches when one looks beyond the single issue of hit rate to other issues such as those discussed above.

The implementation of split caches is not difficult and can be transparent to software. Unlike main memory, cache is demand fetched at the time of processor fetch. During a bus cycle, most processors signal whether data or instruction, or user or supervisor data is being referenced. These signals control which of the split caches is to be selected. When designing these caches, the arbiter/controller that coordinates processor and system accesses must carefully arbitrate the caches and ensure no bus contention occurs. This is aided by the use of bus isolation to provide separate bus paths for the caches to the system, and perhaps registers to isolate the cache from the local processor.

4.3.2 User/Supervisor Caches

Split caches separating the user and supervisor spaces can be implemented to provide elegant solutions to coherency control. In virtual memory systems requiring cache to be flushed on context switches, a simple solution is to flush the entire cache. However, since this approach invalidates valid entries as well, it is not optimal. By separating user and supervisor code, the user space may be flushed independently, leaving the supervisor space intact. This is advantageous since the supervisor space often maintains the same virtual space (perhaps even a real space) and therefore need not be flushed.

5. Implementation of Coherency Protocols

There is a plethora of protocol and implementation alternatives for coherency control falling into two basic categories. The two catagories are write-through (or immediate) and copyback (or delayed update, also called write-back). Both are implemented by hardware and, perhaps, assisted by software. This section will begin by briefly discussing the coherency protocols.

5.1 Write-through Cache Schemes

The write-through protocol dictates that every cache write operation should also be directed to main memory. This permits all cache modifications to be visible to any unit interfacing to the system bus and assures that main memory and cache copies are identical at all times.

This method is simple and reliable, and intrinsically protects against coherency violations in cases where I/O or another processor may read from main memory. However, the issue of I/O or other processor writes to main memory presents a problem which is resolved in Section 5.4 on bus monitoring mechanisms.

The write-through update method guarantees coherency by ensuring that main memory copies are always consistent with cache copies, for all cached data. Furthermore, write-through is the simplest to implement and requires the least hardware. There are two basic variations to write-through, depending on whether the write to main memory is immediate (straight write-through) or delayed (buffered write-through).

5.1.1 Straight Write-through Updating

A simple approach in securing coherency is to force the processor to wait while the data is written to the local cache and main memory. When the processor write is detected, the tag buffer is interrogated to determine residency while the write cycle to main memory commences. By delaying the acknowledgement to the local processor, the controller may acquire the system bus and write data to the main memory and local cache (often done concurrently).

In the case that the written data is not cached, there is no performance penalty in directing the write to main memory, since the entire block must be retrieved in any case. A technique motivated by this fact is one in which cache slots are not allocated on cache write misses, only hits. Although interrogation is still required, additional slots are freed for read-only and read-first, read/write entries. Furthermore, if a slot is allocated for a missing entry, the entire block must be copied into cache from main memory after the write data has been written to the system bus. Therefore, in the case of straight write-through, avoiding allocation reduces the write time by an amount equal to the main memory block transfer time.

5.1.2 Buffered Write-through Updating

The two drawbacks associated with the write-through scheme are 1) a long cache write cycle time and 2) high system bus bandwidth consumption. Buffered write-through reduces the write cycle time to that of the read cycle by releasing the processor from having to wait until the main memory write cycle is complete. Figure 5–1 illustrates a block diagram of a buffered write-through system at the heart of which is a buffer and controller that stores the written data and its associated address for subsequent transfer to main memory. With written data in the buffer, the controller then accesses the system bus and updates

main memory. Should the processor perform a subsequent write while the previous one is pending, it is also buffered. This may continue until the buffer's capacity is exhausted.

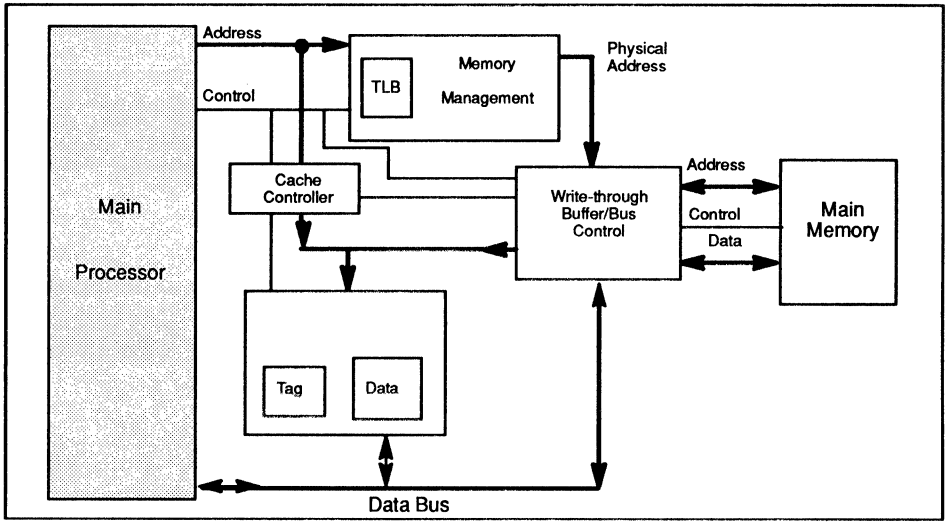


Figure 5–1. Buffered Write-through System

Though implementing a buffer and controller for buffered write-through may appear complex, it can be as simple as using a register for both the data and corresponding address. The write data is then registered, the processor freed to continued and the data transferred to main memory by cycle stealing. If a subsequent write happens to appear before the latent write data is transferred to main memory, the processor is then halted. Alternatively, the buffer may be extended in depth. If the maximum time to transfer a write is less than the minimum time between successive writes by the processor, the buffer will never force the processor to wait. More realistically, however, is a probable determination of average cycle time; an issue discussed in Section 5.3 regarding quantitative analysis of the coherency schemes.

The function of the buffered bus monitor is depicted in the state diagram in Figure 5–2. Several variations of the scheme are possible, depending on the protocol choices made by the designer. For example, if cache slots are allocated on cache misses during writes, a block transfer after the main memory write is required. A more detailed discussion of buffered write-through is presented in Section 5.5.

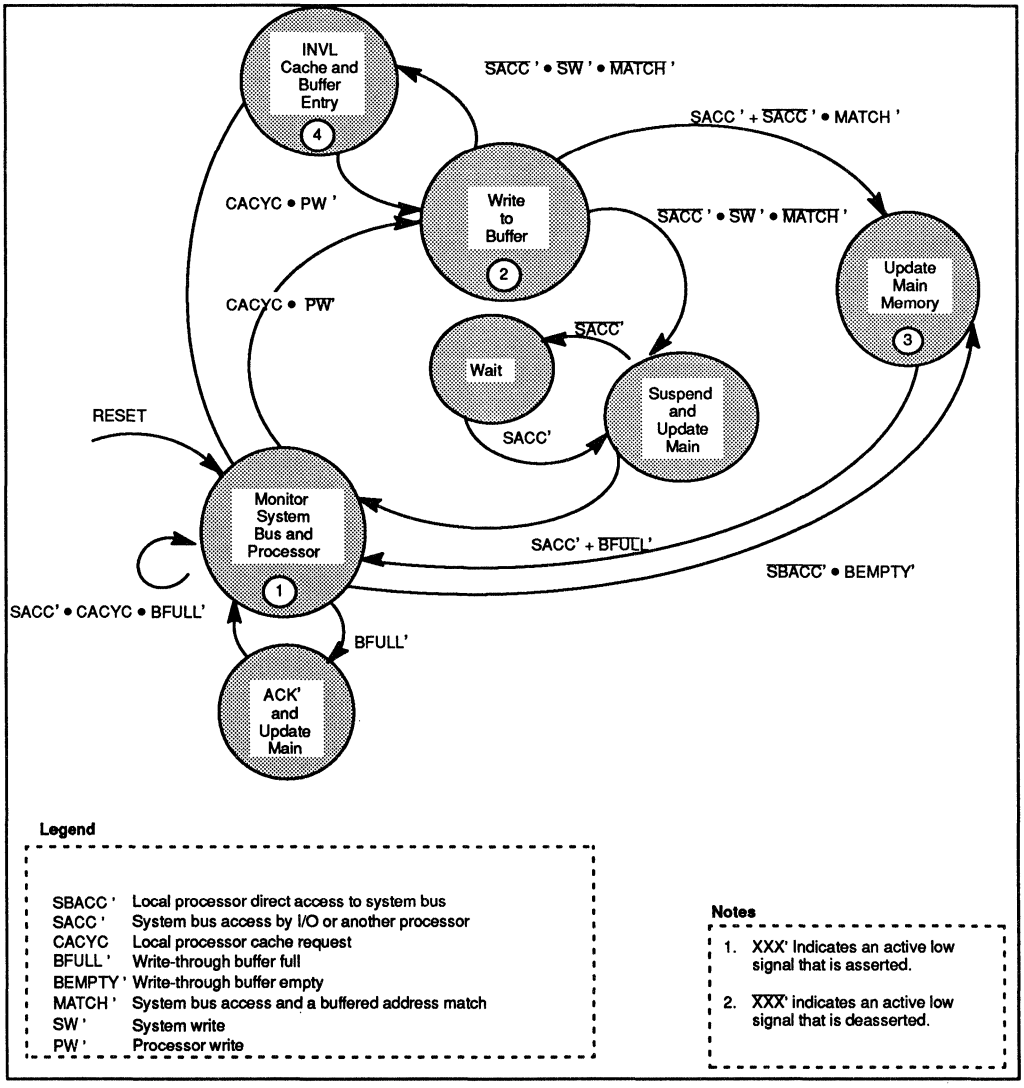


Figure 5–2. State Diagram of a Buffered Write-through Bus Monitor

5.2 Copyback Schemes

While buffered write-through shows great promise by supporting fast cache write cycle times, it still degrades available system bandwidth since every write must eventually reach main memory. Consequently, parallel processing systems may be inclined to employ copyback schemes, which reduce bandwidth requirements by updating the store only when necessary.

Although popular in mainframe computers, copyback schemes are complex to implement, requiring more overhead logic and more complicated analysis to ensure coherency reliability when compared to write-through or buffered write-through systems. Furthermore, although bus bandwidth is gained with the use of copyback, many high performance desktop computers, including high-end workstations, utilize the more economical write-through or buffered write-through approaches. While the bandwidth issue has often driven designers of multiprocessor implementations to copyback schemes, write-through and its variations find their way into many highly parallel systems, even those with up to 32 processors. For this reason, Fujitsu has designed the MB81C51 to be used in write-through and buffered write-through systems which demand fairly large, high-speed caches. This section, therefore, is provided for the interested designer as an introduction to copyback and its various implementations.

5.2.1 Approaches to Copyback

There are a vast number of approaches to copyback which vary in control (distributed versus centralized), allocation of data, monitoring other requests for data, etc. Examples are write-once, the Goodman public/private cache, and the snoopy cache by Rudolph and Segall. Generally, copyback schemes require additional descriptors which are associated with each line and indicate the privilege (level of local access) and update condition of the line. These descriptors are managed and kept in the local caches (or main memory if centralized control is employed). Although varied, most of the methods have some commonality in their access permission and update approach; these are:

1. Requests for data to be cached are directed to main memory (as with typical misses).
2. Read or Write (or equivalently public or owner) privileges to the data are assigned to the requested line. The privileges are often implemented as another field along with the tag.
3. Other caches holding the same line may have to change the rights of the local line to be consistent with the granted rights.
4. Any dirty lines (containing data that has been modified in cache but not in main memory) in cache must be updated before a new copy is granted. This may involve suspending the current system request and updating main memory.

Even with copyback implementations, there are still several occasions when main memory access is required, but the frequency of these accesses is generally much less than exhibited by write-through schemes where typically 18 percent to 33 percent of the total number of memory accesses are writes and, consequently, must go to main memory. RISC processors, however, tend to have different requirements that may make copyback somewhat less advantageous than write-through. Due to the large register files that have defined RISC machines, many writes never go to the external bus. In fact, the Fujitsu RISC processor SPARC™ typically accesses the external bus only about 5 percent of the time when compared to the frequency of instruction and data fetches. This reduces the penalty for writes and makes write-through systems nearly equal in bandwidth performance with copyback. Conditions that may force a main memory access when copyback is employed are:

1. Cache miss on read requires reading a line from memory (perhaps assigning read-only, or public access privileges to the cached line).
2. Cache miss on a write means a line may be provided to the local cache under read/write privileges (meaning exclusive or private ownership).
3. A cached line has write privileges and a main memory request is made for the same line. In some schemes the line is always written to main memory and either invalidated locally (if the request is

for a write) or local rights are reduced to read-only (if the successor received read-only privileges). A more efficient scheme is to update main memory only if the local copy is dirty, though this requires tracking a dirty bit.

4. When context switches in a virtual cache scheme, it is usually necessary to flush out entries in the virtual space of the swapped task. This may require writing dirty data out to main memory.

   This is a function that the MB81C51 cannot directly support, since the tag, once written, cannot be read back out, only compared against another tag. However, future Fujitsu tag RAMs should provide expanded functionality to support these and other operations.

Notice that I/O may operate given the above protocol, but without holding its own privileges, since all caches will be monitoring the system bus with I/O operates.

5.2.2 Centralized versus Distributed Control in Copyback Cache

If centralized control is implemented, then main memory must store the access level bits of each line and coordinate the assignment of the lines. Additionally, in some way, local caches must be capable of responding to update cached lines to main memory, as well as invalidating them as necessary. There are two drawbacks to centralized copyback control. First, a centralized controller can not determine consistency (dirty data), since local accesses to the data are hidden from the system bus and, therefore, main memory must always be updated when read/write privileges are reduced. Second, the local cache must still manage the privilege level and, in particular, enforce the read-only level by intercepting the writes to these restricted lines and treat them as misses.

Distributed systems require a bus monitor, similar to that used for write-through systems, with the exception that it must detect system bus reads as well as writes. Distributed copyback must also be capable of enforcing read-only protection.

5.3 Evaluation of Performance Efficiency

Having determined the optimal coherency protocol to employ, the designer must consider cost, reliability, ease of design, and of course, performance. In this section, two performance measures will be evaluated for each of the coherency protocols previously discussed. These are average cycle time and bus bandwidth utilization.

5.3.1 Evaluation of Straight Write-through Systems

When all cache writes are being directed to main memory, the cache write cycle time becomes constrained by the average main memory write cycle time, which includes arbitration time to acquire the system bus. Furthermore, since an entire line must be transferred into cache from main memory, the block transfer time is critical to the overall average cycle time of a system, regardless of the update protocol employed. Assuming that H, the average cache hit rate for both reads and writes, has been reasonably determined, the average memory cycle time can be represented as the following equation (assuming zero wait state operation):

Eq 5.1a

$$t_{MWCT} = H * [t_{RC} * (1 - W) + t_{MWC} * W] (1 - H) * [(1 - W) * t_{BT}(L) + W * (t_{BT}(L) + t_{MWC})]$$

$$= H * [t_{RC} * (1 - W) + t_{MWC} * W] + (1 - H) * [t_{BT}(L) + W * t_{MWC}]$$

where a fraction W of the memory cycles are writes and incur a main memory write cycle time of t_{MWC}, which reflects the system bus arbitration time. t_{BT} is the time to transfer a block of size L, which includes the time to acquire the system bus and transfer an entire line in burst fashion. t_{RC} is the cache read cycle time. The $(1 - H)$ term is fairly complex, since in the case of a write miss, it must include t_{MWC} and may or may not include the block transfer time, depending on the chosen protocol. This operation is more fully described in Section 5.6. Equation 5.1a assumes the transfer takes place on write misses.

Since write-through may consume much of the available main memory bandwidth, it is important that the utilization be quantified so that system behavior can be properly modelled. Using the same notation as equation 5.1a, and representing the average available main memory bandwidth by FSB (in words/sec, assuming main memory and the processor bus are of the same size), the average main memory bus utilization can be approximated by:

Eq 5.1b

$$U_{BW} = F_{PU}/F_{SB}$$

$$\approx 1/[F_{SB} * [F_B * H * [t_{RC} * (1 - W) + t_{MWC} * W] + (1 - H) * [t_{BT}(L) + W * t_{MWC}]]]$$

where F_{PU} is the average system bus frequency of utilization by the local processor. F_B, which is the local processor's average memory cycle frequency (accesses per second), can be calculated by averaging the total number of reads and writes over time (regardless of whether or not they are cache resident, an issue considered by the average hit rate).

The calculation of F_{SB} for use in equation 5.1b is important and should include burst transfer modes for DMA and cache line transfers, if the system supports such a function. This utilization estimate, being simply an average, may not anticipate the most catastrophic scenarios in which the bus is most heavily utilized. Modelling buses more completely is covered by texts on computer architecture, and typically involves modelling the bus by applying queuing theory and assuming that bus cycles are sufficiently represented by a Poisson or other distribution. This approach is used in Section 5.5.3 to determine FIFO size for buffered write-through systems.

5.3.2 Evaluation of Buffered Write-through Systems

Buffered write-through will reduce the average memory cycle time by reducing the cache write cycle time to that (or nearly that) of the cache read cycle (i.e., t_{WC} -> t_{RC}). Therefore, the average memory cycle time is now (again assuming zero wait state operation):

Eq 5.2a

$$t_{MCBWT(1)} = H * t_{RC} + (1 - H) * [(1 - W) * t_{BT}(L) + W * t_{BT}(L) + t_{MWC})]$$

By design, it is also possible to free the processor up in case of a write miss, as long as the time to transfer the remaining line elements is less than the average time to a subsequent read, since the processor must halt if the transfer is not complete by the time of the next read or write of that line. If this approach is taken, the average cycle time approaches:

Eq 5.2b

$$t_{MCBWT(2)} \approx H * t_{RC} + (1 - H) * [(1 - W) * t_{BT}(L)]$$

Note that equations 5.2a and 5.2b assume that the time to transfer a write to the buffer is no more than the cache read cycle time.

Although the added buffer reduces the average memory cycle time, it does not reduce the number of main memory cycles. Therefore, assuming identical block transfer and write cycle times, as well as main memory frequency, the average bus utilization time is the same as for straight write-through. However, the distribution of writes, that is, the time at which specified writes occur in time, is not necessarily the same due to the buffer's effect.

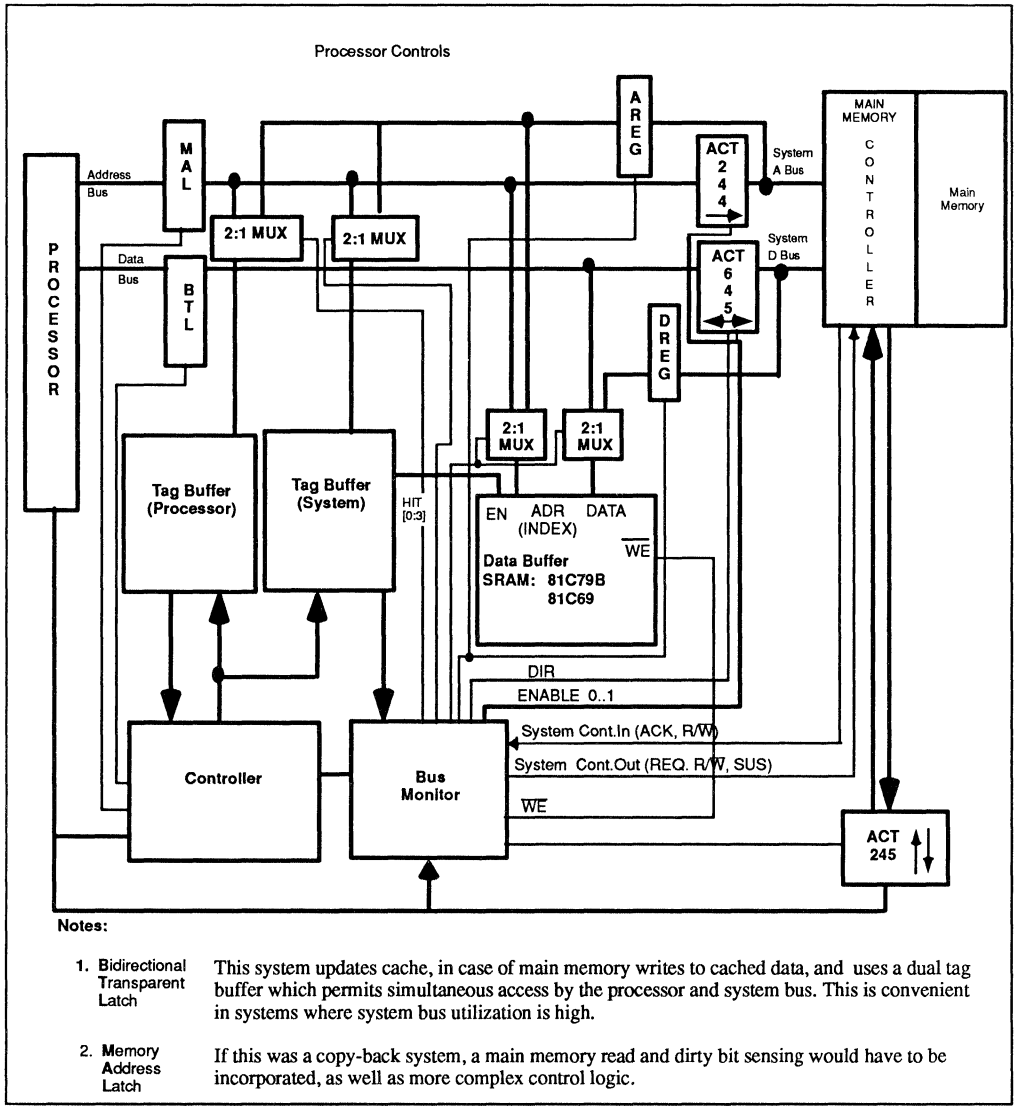
Due to the variety of methods, implementation dependency and sensitivity to program behavior, copyback performance criteria are difficult to determine and therefore, are not evaluated in this Application Handbook. In general the average cycle time for a copyback system lies somewhere between that of a straight and that of a buffered write-through, since there are times when the processor may be preempted in order for a line to be flushed from the local cache, and time is also required for handling read and write misses. However, bandwidth utilization can be reduced by an amount proportional to the frequency of write hits.

5.4 Bus Monitors

All of the protocols discussed so far, straight write-through, buffered write-through and copyback, require that the system bus be monitored to determine when the parent (in main memory) of a cached location is being modified or read in a situation (such as copyback) where data in the local cache may be dirty. The bus monitor, therefore, is a critical function, but because of all the possible coherency protocol variations, bus protocols and special data transfer modes, the best bus monitors are generally those that are customized for the entire system. However, the following are some considerations for design with the MB81C51 interfacing to a bus monitor in a write-through system; Section 5.5 provides additional detail for buffered write-through monitors.

First, when interrogating the tag buffer in response to a main memory (system) bus cycle, do not perform an updating interrogation, but rather an inquire, which is performed without asserting SET'. This prevents the LRU from being updated when the cache is not being accessed under normal operation.

Second, interleaving the bus monitor and processor cycles may require a tag RAM that has nearly twice the bandwidth of the processor's bus in order to perform a processor-initiated interrogation and a system bus reference in the same cycle. It is, however, possible to interleave the contending system and processor tag accesses by comparing the system bus address with the processor's bus address to determine if preemption is warranted. If interleaving is inadequate to the task, a technique may be employed that has been used in mainframe and minicomputers for some time, duplicate tag buffers. This technique requires a duplicate tag buffer for interrogation by the bus monitor, which is concerned only with residency and not with replacement ways. Figure 5–3 illustrates the dual buffer scheme and its integration into the system.



Notes:

1. Bidirectional Transparent Latch — This system updates cache, in case of main memory writes to cached data, and uses a dual tag buffer which permits simultaneous access by the processor and system bus. This is convenient in systems where system bus utilization is high.
2. Memory Address Latch — If this was a copy-back system, a main memory read and dirty bit sensing would have to be incorporated, as well as more complex control logic.

Figure 5–3. Cached System with Dual Tag Buffers for Asynchronous Tag Inquire, Read and Write

This shadow buffer is modified any time the primary buffer is updated, relative to the tag and validity bits. Primary buffer operations that must also be performed by the shadow tag buffer are the following: replacement writes, purge cycles and selective invalidation cycles; reads are independent. There are two optional responses when it is determined that a main memory write references cached data, (1) invalidation or (2) update of the data buffer. Invalidation requires that both the primary and shadow buffer be

selectively invalidated. If the update approach is taken, the corresponding local cache entry is updated, which could force the local processor to suspend a current bus cycle.

Since the LRU tables are not consistent between the two buffers, the shadow LRU table is ordinarily not used for any purpose. Let us use the MB81C51 as an example. For shadow buffer operations initiated by the primary buffer (replacement writes and selective invalidation), SBLK of the shadow buffer is enabled (high) and SBO/SBI of the shadow buffer is driven by HC0/HC1 of the primary buffer so that only the appropriate set element is written or invalidated. When routing main memory operations to the shadow buffer, however, SBLK is disabled (low) and HC0/HC1 of the shadow buffer drives SB0/SB1 of the primary buffer. The SBLK of the primary buffer is generally the complement of the state of the shadow buffer's SBLK.

The tags in both buffers must be consistent in their index location, set element position and state (valid or invalid) at all times to guarantee coherency.

5.5 Constructing a Buffered Write-through Monitor

In the previous section, the fundamental requirements and operation of a bus monitor were presented, preparing the designer for implementation of such a circuit. Because of tight performance requirements, and the fact that most systems with Standard Bus implementations utilize a broad variety of cache protocols, standard bus monitors and interfaces are rarely available to suit the application. This places the difficulties of implementation upon the designer. In this section, the considerations of constructing a buffered write-through monitor are presented in an attempt to simplify the design process.

The write-through buffer relies on the system bus protocol for main memory interfacing and for supporting the local cache. Given the functions of the bus monitor, it is only natural that these two functions should be integrated, so that the buffered write-through monitor is made up of the following functional elements.

Bus monitor	Senses system bus writes and invalidates or updates cache
Burst transfer	Transfers a line from main to cache memory
Bus protocol controller	Arbitrates the system bus
Queue latency control	Senses system bus reads and compares buffered addresses
Buffer management	Supports FIFO reads, writes,and flag generation

These functions are represented in the block diagram of Figure 5–4. Implementing the function of the queue latency controller and buffer manager will be topics of this section.

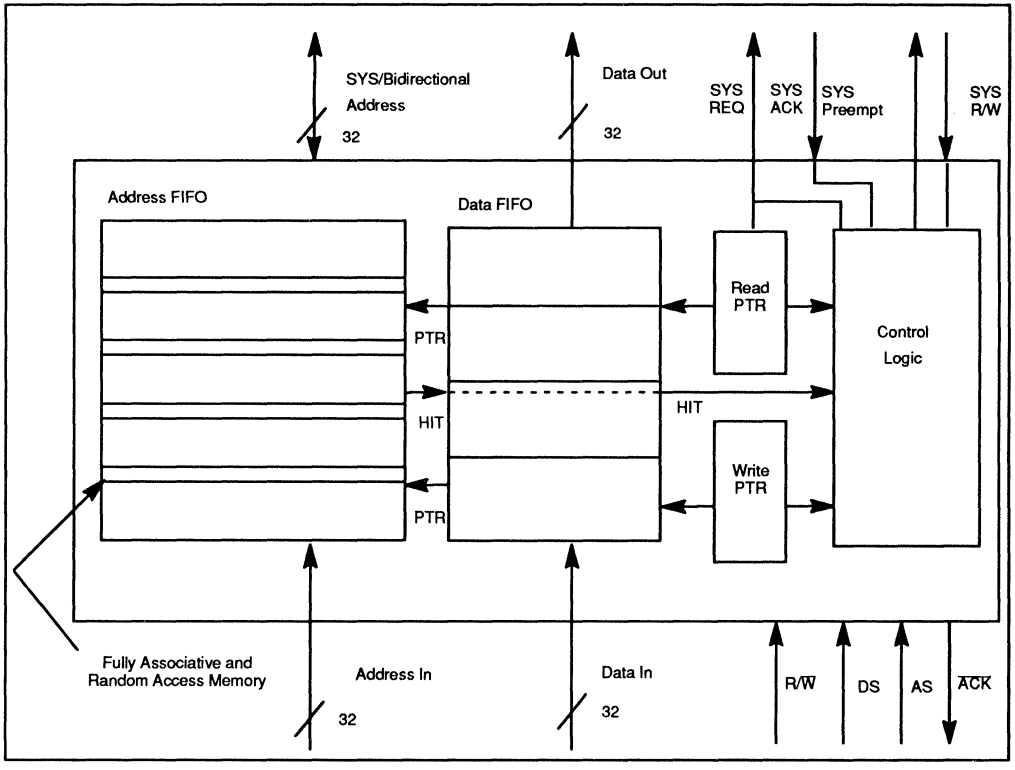


Figure 5–4. Buffered Write-Through

Functions of the Buffer

1. Operates as a FIFO to accept data and corresponding addresses from the processor after a processor write.
2. Transfers data in FIFO order to main memory by writing it to the address specified by the corresponding address FIFO.
3. Determines whether system bus access of main memory data is also latent in the FIFO by performing address comparison. For virtual caches, either the translated address may be buffered (since it must be translated at some point anyway) or only the real part of the address compared.
4. Pre-empts the system bus access and updates main memory in the case of a system read of an address stored or latent in the FIFO. This requires a RAM approach to the FIFO buffer.
5. When the system bus access is a write of data latent in the FIFO, the buffer decides whether the FIFO entry and the corresponding local cache entry are invalidated or the system bus operation is halted. In any case, two writes from different origins may be a condition to be prevented, not just resolved.

Due to the integration of a number of related functions sharing the same signals, it is usually desirable to implement the bus monitor circuit in a semi-custom VLSI such as gate array or standard cell.

Fujitsu's ASIC technology provides various levels of integration, a variety of packaging options, very high-speed CMOS and ECL technologies, and high drive, all necessary for bus monitors typically requiring 4K-8K logic gates, high I/O count and high output drive capability.

5.5.1 Buffer Management

When a write is performed, it must be buffered and transferred to main memory without holding up the processor or interrupting system bus activity. To do this, two small-depth, wide FIFOs are used, one which buffers the written data and one which buffers the corresponding addresses. Addresses must be buffered because the processor is driving the address bus when the transfer to main memory occurs. In addition to the FIFOs, control logic is needed to accept the written data, request the system bus and transfer the data to main memory when access is gained. Since the FIFOs may be greater than one word in depth, the controller must be capable of performing a write and transfer simultaneously. Handling the condition of overflow (FIFO buffer full) is a critical operation involving suspending the processor, if a current write cycle is in operation, and transferring the contents (all or at least one word) of the FIFO to Main Memory. Avoidance of this issue by early transfer from the buffer prevents the processor from waiting, but may require preemption of a current bus cycle if a long transfer such as DMA is in progress. It is the physical address that is usually buffered, since the address must then reference main memory, as shown in Figure 5–1, in which the MMU precedes the buffer.

5.5.2 Queue Latency Controller

There is a single anomaly making the design of the controller somewhat tedious. While a written word is being buffered, it is in limbo for a period of time equal to queue latency. Any read cycle of main memory referencing this location is in danger of reading bad data. Further, it is unreasonable to route system bus reads to the cache tag, since only the buffer is aware of which addresses are dirty and latent. Therefore, the buffer must monitor system bus cycles, and determine if they reference any of the buffered addresses — a type of mini-cache operation. However, it is not necessary to employ a CTRAM, since the buffer depth is usually very short (1 to 4 words). As Figure 5–4 illustrates, the address comparison access can be implemented as long as all addresses in the buffer are available in parallel for simultaneous comparison (which is the case if the FIFOs used to construct the buffer are built with registers). If a hit is detected from this comparison, then appropriate action must be taken.

If a system bus read was in progress when the hit was detected, it must be preempted so that the update may take place. The update can either be of the single word only, all words up to and including the referenced word, or the entire buffer. Since buffers are usually short, it is often better to dump the entire buffer, although burst transfer cannot be used since the buffered data are randomly located.

10

If the system bus cycle was a write, then several possibilities exist. However, the designer should first determine the implication of near simultaneous writes. Is I/O simply overwriting old data which is no longer valid? Is another processor updating a shared semaphore, or a shared variable? In other words, should this situation be permitted and if so, is the order of arrival of the writes significant?

If the order is not important, the designer may opt to simply invalidate both the buffered entry and the local entry in cache (since the system bus write would otherwise create a discrepancy with the local cache). This requires a buffer that can selectively shift forward all entries below a given position, retaining all other entries at their current position. This will overwrite the lowest entry held static, thereby nullifying its write operation and removing it.

However, if order of multiple writes is important, it is necessary to design a buffer that attempts to transfer all buffered entries at the earliest opportunity. Furthermore, it must always ensure that the last write initiated is reflected in main memory. And last, the bus monitor in conjunction with the latency controller must ensure that any other subsequent overwrite results in invalidation of the cached entry.

5.5.3 Determining Optimal Buffer Depth

The buffer, or more fundamentally the data and address FIFOs, can be as simple as a single register pair, or it can be 2, 4 or 8 entries deep. Its purpose is twofold; to store the data and address of a write in order to free the processor to continue, and to buffer one or more words until the data can be written to main memory. To determine the best depth for the FIFO, we will rely on a little queuing theory, but first, some definitions are necessary.

As shown in Figure 5–5, the buffer can be modeled as a queue with an arrival time characteristic ($\lambda(t)$) dependent on the behavior of local processor writes and a service time characteristic ($\mu(t)$) dependent on system bus activity and main memory. If λ is the average arrival period, and L is the average service period (wait time plus transfer time), the following relationships hold for steady state buffer behavior:

$$L = 1/\mu,\ 1/\mu = W$$

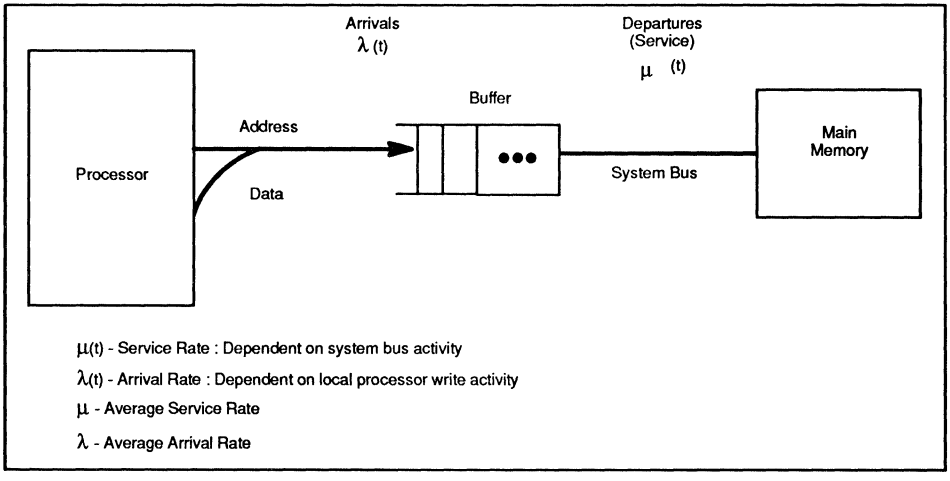


Figure 5–5. Model of Buffered Write-through

The average utilized buffer length (L) is the product of the arrival rate and the waiting time (W). Note that this assumes that the average service time is less than the average arrival time ($\lambda > \mu$), otherwise the buffer would usually be overflowed.

By considering the worst case conditions, the maximum queue length may be defined as:

$$L_{max} = \lambda_{max} * W_{max} + L_{pre}$$

where L_{pre} is the number of queued entries already waiting, which will be assumed zero.

If a protocol exists in which a bus request has a maximum waiting time before it is granted, this may be added to the main memory write cycle time and used for W_{max}. As for λ_{max}, the inverse of the minimum back-to-back write cycle time is a worst case for maximum arrival rate. For example, if 1000 ns is the maximum wait time and 200 ns is the main memory write cycle time with a minimum back-to-back processor write cycle time of 250 ns, the necessary buffer is:

$$L_{max} = \frac{(1000 + 200)ns}{250ns} = 4.8 \text{ entries}$$

The buffer serves to provide a type of averaging, or cushioning, of bursts in system bus traffic and processor writes. Therefore, though under transient conditions transfers from the buffer may not keep up, as long as the steady state behavior is satisfied and long bursts are considered, the buffer should prevent the processor from waiting. The exception is the case where system bus utilization is 80 to 100 percent. In this case, special bus architectures such as multiple split buses may be necessary.

5.6 Effect of Allocating Slots on Write Misses

In certain cases, it has been proven more efficient not to replace a cache entry on a cache miss during a write operation. This design practice involves directing the write operation to main memory, but not allocating a slot or transferring the referenced line to cache. The effect is to save the time necessary to transfer the line into cache while avoiding the replacement of a line that may be referenced. On a write miss it is not a requirement to replace the line in cache, only to write the data supplied by the processor.

There are three notable advantages of non-allocation on write misses which should be considered before determining whether to use this technique. The first is that more available slots are effectively freed, since a resident slot is saved for every write cycle forcing a miss. If LRU is used, then this number can be thought of as the number of write-first entries that exist, since a read-first entry is likely to already be resident in cache. This implies that a line which is first written, then read receives a lower priority than a line which is read-only or a read-first read/write line. Verifying the validity of this approach relies on the evaluation of some fundamentally conditional probabilities; the probability of a subsequent read or write given a primary (first) write (PWR) and the probability of a subsequent read or write given a primary read (t_{RR}). The latter may be more easily evaluated if thought to be the sum of the probability of a read-only reference plus the probability of a read/write reference in which the first reference is a read. Figure 5–6 is a Venn Diagram illustrating these probabilities, where the universe is all references by the local processor. If the PRR is greater than the PWR, then this approach may be reasonable.

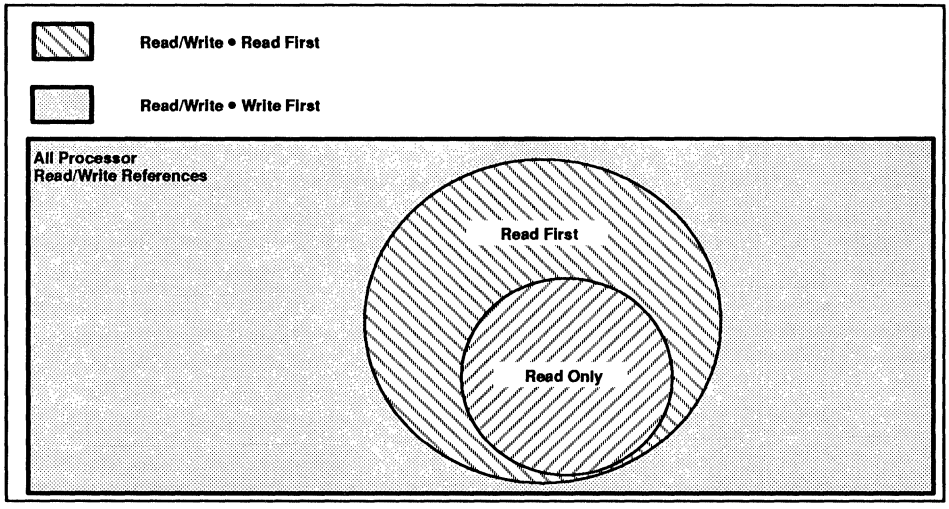


Figure 5–6. Venn Diagram of Bus Cycles

The second advantage is the reduction of the write cycle time. Supposing that a miss on a write did force a replace, not only must the entry being written enter the cache, but the other members of the referenced line must also be copied to the cache. Non-allocation, therefore, removes the contribution of the block transfer time to the overall write cycle time. Equation 5.1a can be evaluated for the effect of non-allocation on write misses, though in its original form, allocation of slots for write misses was assumed:

Eq 5.2

$$t_{MCWT} = H * [t_{RC} * (1 - W) + t_{MCW} * W] + (1 - H) * [(1 - W) * t_{BT}(L) + W * (t_{BT}(L) + t_{MWC})]$$

If, however, write misses go unreplaced, the average memory cycle time becomes:

Eq 5.3

$$t_{MCWT(NA)} = H * [t_{RC} * (1 - W) + t_{MCW} * W] + (1 - H) * [(1 - W) * t_{BT}(L) + t_{MWC}]$$

The fractional improvement becomes:

Eq 5.4

$$IMP = -[t_{MCWT} - t_{MCWT(NA)}] / t_{MCWT}$$

For example, if the hit rate (H) is 95 percent, the write:read mix (W) is 20 percent, the average time to transfer a block of 4 words is 720 ns ($t_{BT}(L)$, which includes bus acquisition time), and the average cycle time with allocation on write misses is 95 ns, the improvement is 7.2/95, reducing the average cycle time to 87.8 ns. Though not extraordinary, it is easily accomplished by a simple state sequence and with little increase in hardware.

The last advantage of non-allocation to be discussed is system bus bandwidth, an important issue in particular for write-through systems. Since only the single main memory write cycle is performed and not the block transfer, the system bus is tied up for a shorter period of time. However a degradation in performance may be suffered if the line is subsequently referenced on a read miss. The improvement in

bandwidth is, therefore, related to the percentage of write-first lines that are never read and to the line size. The bandwidth utilization for the replacement case can be approximated as (modifying equation 5.1b from Section 5.3.1):

Eq 5.5

$$U_{BW(NA)} = F_{PU(NA)} / F_{SB}$$

$$= 1 / [F_{SB} * [H * W * t_{MWC} + (1 - H) * [(1 - W) * t_{BT}(L) + W * t_{MWC}]]]$$

So with little, or no additional hardware, the non-allocation technique may be effectively employed to reduce average cache cycle time and reduce the utilized bandwidth. The above equations are intended to aid in the evaluation of this technique, given the characteristics of the designer's end-system. Though determination of some of the parameters used in the equations may be difficult, these equations should nevertheless provide a reasonable guideline.

6. Real and Virtual Cache

Virtual cache, as discussed in Section 1.7, is one addressed by virtual addresses, while a real cache is preceded by some form of address translation such as an MMU, if virtual addressing is employed. With the rapid advancement of 32-bit microprocessors with clock periods of 50ns, 40ns and faster, as well as the success of RISC processors that demand single-cycle instruction fetches, the turnaround time of the cache (its access) is critical. Therefore, it should not be surprising that virtual caches are gaining in popularity, even in the workstation arena. Our discussions thus far have been centered around real cache implementations, which have the advantage of simpler and typically cheaper cache coordination.

Implementations of virtual cache are quite varied, but all must address the following potential coherency hazards:

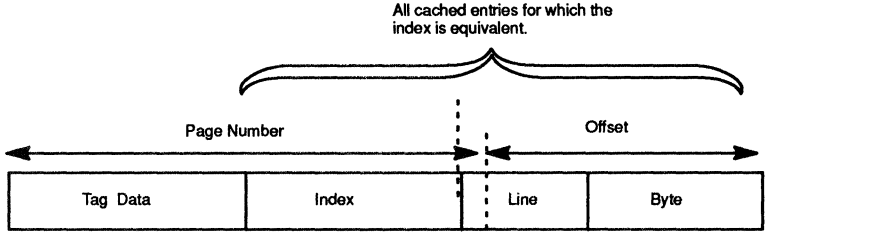
1. Real and virtual address correlation with regard to bus monitoring
2. Address aliasing
3. Virtual address space switches and other conditional addressing problems.

The construction of cache typically varies with the way these issues are handled; therefore, they will be addressed one at a time.

6.1 Virtual Cache Construction: Address Correlation

Correlation refers to the correspondence between virtual addresses which access cache and their translated real addresses, which reference main memory. It is often necessary to determine if two addresses, a virtual and its translated real address, are equivalent. For instance, in a common scenario, the system bus monitor may see real addresses referencing main memory and must determine which of these are resident in the local cache which is virtually addressed. To do this, the bus monitor may inverse translate the real address, perform a partial (real) field comparison or perform some other technique of coordinating the addresses.

A popular way of invalidating all cache lines that may be copies of a modified main memory location is to invalidate all of those that have matching page offsets. Since virtual addresses have a real field which is common, all real addresses in cache with matching offsets are purged. If the index is at least the size of the page offset, then this amounts to selectively invalidating (explicitly) all set elements at the index address contained in the page offset (see Figure 6–1). In the case of four set elements, this would require four clock cycles while counting through the individual set element select lines. Though this method purges $W * B$ entries, where W is the degree of the cache and B is the block size, it does work effectively for moderately small blocks (1–8) and large caches.



Given that the cache degree of associativity is W and the line size is L, then flushing by real offset comparison where the index plus line plus byte address (see above) is at least the size of the offset results in the deletion of $W * L$ entries. If the exact rather than incomplete comparison is performed, either 1 or 0 entries would have been invalidated. Therefore, the waste factor is $W * L$ at most.

Figure 6–1. Virtual Cache Address Field Partitioning

6.2 Virtual Cache Construction: Address Aliasing

Aliasing occurs when two different virtual addresses map onto a single real address, which presents problems in monitoring main memory addresses,and opens the possibility that local cache contains two copies of the same data. These duplicate addresses form pseudonyms (aliases) that may result in inconsistent data copies. This side-effect of virtual caches is applicable to both write-through and copyback schemes. For example, suppose that data is cached under virtual address #1 for a given process (A). A task switch is performed in which the cache remains intact (i.e., not flushed). A successive task (B) requests the same line under a different virtual address, virtual address #2, and modifies it. If write-through is used, main memory will always be updated to the most recent state, but the local cache copies can be different. Therefore, if process A is restarted under the same virtual address space, it is not referencing the most recent copy of the data in the local cache, since that would reside at virtual address #2. Figures 6–2a, b, and c illustrate this and demonstrate the impact of index size and associativity on aliasing.

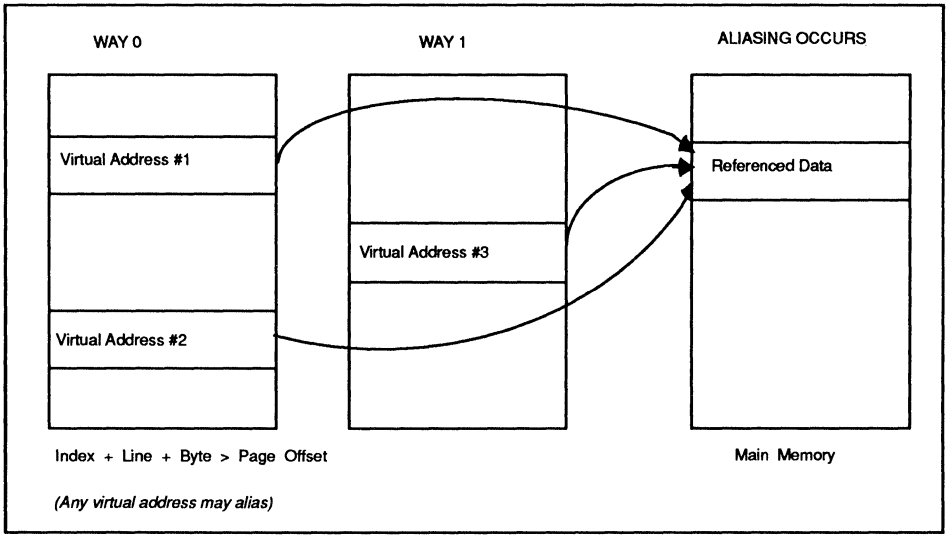


Figure 6–2a. Address Aliasing with Virtual Cache

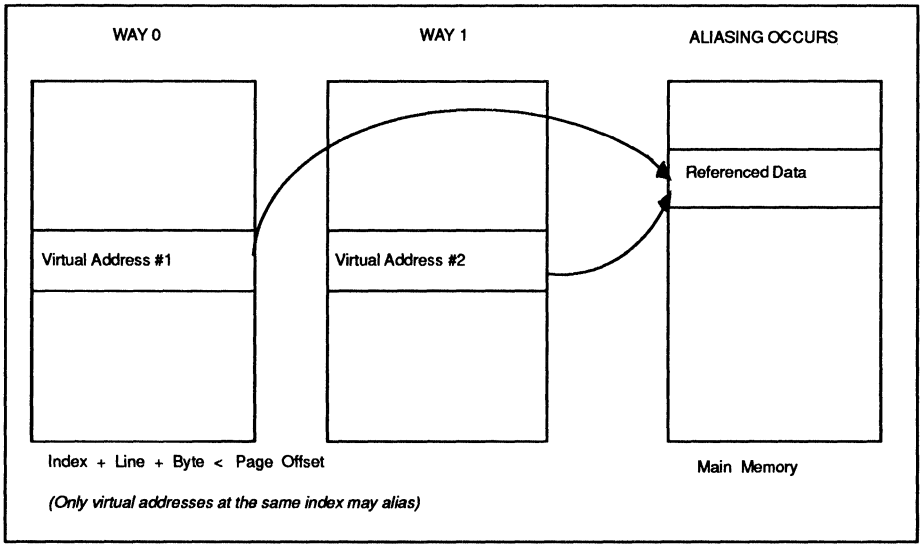


Figure 6–2b. Avoidance of Address Aliasing through Address Partitioning

Although it is possible to permit aliasing and manage it, for the reasons discussed above, most systems engineers building virtual caches design to prevent or avoid aliasing from occurring. Avoidance can be implemented by ensuring that no task running on a processor may leave valid (not invalidated) data from its virtual address space in cache when it is switched. This prevents the new data from being as-

signed to a succeeding task's space. This requires that either 1) the entire cache is flushed on context switches, or 2) only entries associated with the blocked task's virtual space are flushed. Another technique, shown in Figure 6–2c, prevents aliasing with use of a direct mapped cache having an index + line + byte select size not less than the page offset size. In this case, only one entry with a common real address field may reside in cache at the same time, mutually excluding possible pseudonyms. However, the consequence is that the less efficient direct mapping technique must be employed, perhaps nullifying the advantage, though it does yield a simple implementation.

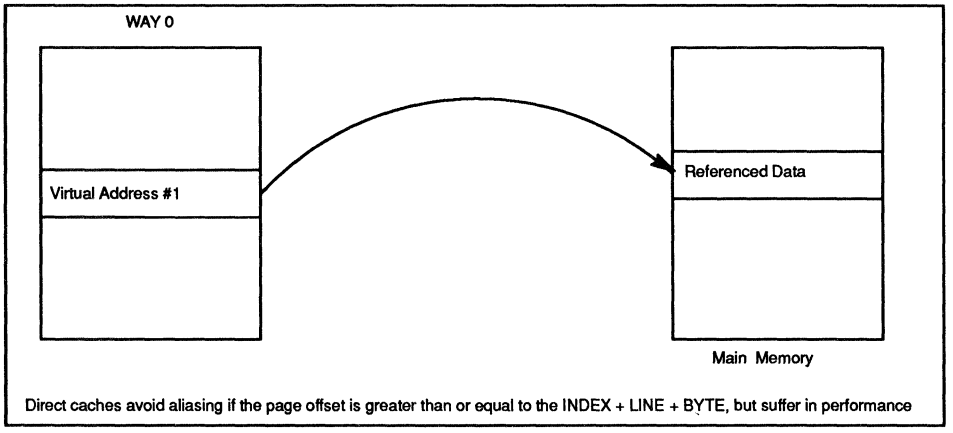


Figure 6–2c. Avoiding Address Aliasing through Direct Cache

6.3 Conditional Selective Flushes

Conditional flushing by virtual address space ID or page number may be useful in some systems to remedy the aliasing problem and may be controlled by hardware or software, depending on the system design. However, the 81C51 does not easily support such selective flushes since a given tag, or part of it, cannot be conditionally flushed. However, since the purpose of this flush is to flush all entries contained in the virtual address space of a blocked, or swapped task, there are several solutions when implementing the tag buffer.

First, the entire cache could be indiscriminately flushed upon the detection of a context switch. Context switches can be detected in a variety of ways, such as sensing a transition from user to supervisor space. Alternatively, if the page tables are located in a fixed region of memory, a write to this area signals the probability of an address space change, indicating cache should be flushed.

If the cache is large, flushing it entirely may reduce performance greatly. However, flushing only user mode entries on context switches will preserve the supervisor's code/data cache and prevent aliasing (assuming the supervisor does not create aliases that are hazardous), yet only requires the implementation of a split user/supervisor cache and hardware to sense the context switch.

6.4 Other Techniques for Virtual Cache Coherency Control

The following are techniques that can simplify the problems of coherency maintenance in virtual cache systems by imposing system restrictions to limit the required range of monitoring and address correlation problems.

6.4.1 I/O through Cache

Inverse address translation and selective invalidation by offset are mechanisms that can detect I/O reads and writes on copies of cached data. However, it is also possible to bring I/O transfers through the local cache requesting it, then broadcast them to main memory.

6.4.2 Fixed Main Memory Partitions

I/O spaces and buffers that are memory mapped could be made to occupy fixed locations in the address space and use hardwired translated (fixed mapping) or even direct real addresses. This prevents address aliasing and facilitates address correlation by inverse translation, since references to these regions are made by common addresses with a known inverse mapping algorithm. This common set of addresses could then easily be monitored and aliasing prevented. Another, perhaps more extreme application of hardwired, fixed address spaces is that of assigning specific regions in the memory space for shared pages. This simplifies the monitoring and coherency issues that make managing shared data so complex, yet it may be unduly restrictive to limit the physical size of data that can be shared. Only the designer can rationalize these issues.

6.4.3 Flushing to Avoid Aliasing

The idea of selectively or indiscriminately flushing cache on a context switch can be used to guarantee coherency due to I/O writes as well. Let's assume a task is always blocked and its cache space flushed on the request of an I/O resource. I/O then writes to main memory locations to be addressed by the blocked task. When the task is restarted, accessing these locations will force main memory access of the new data, bringing them into the cache.

6.5 Summary of Virtual Memory Operations

Discussed were two primary and a variety of other mechanisms to resolve the problems presented by address correlation and aliasing in virtual cache implementations. Incomplete addressing and inverse translation were discussed as solutions to the problem of correlating real and virtual addresses. Flushing on context switch was shown to be an excellent approach to preventing aliasing, with split caches providing a higher performance option. Other aliasing solutions posed were I/O through cache and hardwired, fixed memory spaces. For additional information, the reader is encouraged to research the references at the end of this document.

Clipper is a trademark of the Fairchild Corporation.
SPARC is a trademark of Sun Microsystems, Inc.

References

C. Alexander, W. Keshlear, F. Cooper, and F. Briggs. "Cache Memory Performance in a UNIX Environment." *Computer Architecture News*, June 1986, Vol. 14, No. 3.

Chandy, K. Mani, Reiser, Martin. "Computer Performance." *Proceedings of the International Symposium on Computer Modelling, Measurement and Evaluation.* Yorktown Heights, N.Y.: IBM Thomas J. Watson Research Center, Aug. 10-18, 1977

Fairchild Corporation. *Clipper Module Product Description.* 1985

J. R. Goodman. "Using Cache Memory to Reduce Processor-Memory Traffic." *10th Annual Symposium on Computer Architecture.* 1983.

M. Hill and A. J. Smith. "Experimental Evaluation of On-chip Processor Cache Memories." *Proceedings of the 11th Annual Symposium on Computer Architecture.* June 1984.

Intel Corporation. *80386 Hardware Reference Manual.* 1986

Motorola Corporation. *MC68020 User's Manual.* Englewood Cliffs, N.J.: Prentice-Hall, 1984, 1985

M. S. Papamarcos and J. M. Patel. "A Low Overhead Coherency Solution for Multiprocessors with Private Cache Memories." *11th Annual Symposium on Computer Architecture.* 1984.

A. V. Pohm and O. P. Agrawal. *High Speed Memory Systems.* Reston Publishing Company, Inc. 1983.

A. J. Smith, "Cache Memories." *Computing Surveys.* September 1982, Vol. 14, No. 3.

P. Sweazey and A. J. Smith, "A Class of Compatible Consistency Protocols and their Support by the IEEE Futurebus." *13th Annual Symposium on Computer Architecture.* June 1986.

A. W. Wilson, "Hierarchical Cache/ Bus Architecture for Shared Memory Multiprocessors." *14th Annual Symposium on Computer Architecture.* June 1987.

Fujitsu's MB81C51 Intelligent Cache Tag RAM

A–1. MB81C51 Functions and Uses

The Fujitsu Intelligent Cache Tag RAM, the MB81C51, is designed to address a broad range of cache implementations in MOS-based uniprocessing or multiprocessing system environments by employing a building block approach. By incorporating important autonomous functions (such as look-up, replacement, selective invalidation, purge and parity), but purposely omitting circuits that are often centralized and integrated with other functions, Fujitsu has positioned the MB81C51 to support large cache spaces in a variety of system configurations.

A–1.1 Cache Tag RAM Features

The features of the Fujitsu MB81C51 Intelligent Cache Tag RAM are as follows:

- Provides high density: 2K lines each; may be cascaded
- Supports 512-by-4-way set associative cache or 1024-by-2-way set associative cache
- Provides single-cycle, single-entry invalidation (selective invalidation)
- Executes a single cycle all purge (cache clear)
- Provides circuitry to quickly determine a cache hit (hit time from address change is 25/30 ns)
- Generates both encoded and decoded set element selection lines concurrent with HIT' generation
- Supports an efficient implementation of the least recently used (LRU) algorithm for replacement resulting from a cache miss
- Offers an ideal environment for write-through and buffered write-through systems

- Assures data integrity by providing parity generation and checking for both tag data and validity bits
- Permits other external selective invalidation and replacement schemes through free selection of the way
- Offers low-cost packaging with 68-pin PLCC and 64-pin PGA packages
- Uses the high-performance 1.0m (drawn) process

A–1.2 Expandability of the MB81C51

The MB81C51 is designed to support today's faster 32-bit processors, with longer, more demanding caches. It is designed to permit simple expansion of the tag RAM depth by the fastest and simplest means.

The MHIT' output is driven by the internal HIT' signal gated with an input, EXTH. This function is enabled by the MHENBL input. A pull-up resistor is included on the EXTH input, with a pull-down resistor on MHENBL, so they may be left open.

A–1.3 Internal Architecture and Block Diagram

Figure A–1–1 is the block diagram of the 81C51 cache configured as four-way. The major components are the tag and control memory storage array (512 x 23 x 4), the tag data comparator and hit generator, the LRU state table (512 x 6 bit memory array) and replacement logic, and the parity generator and checker.

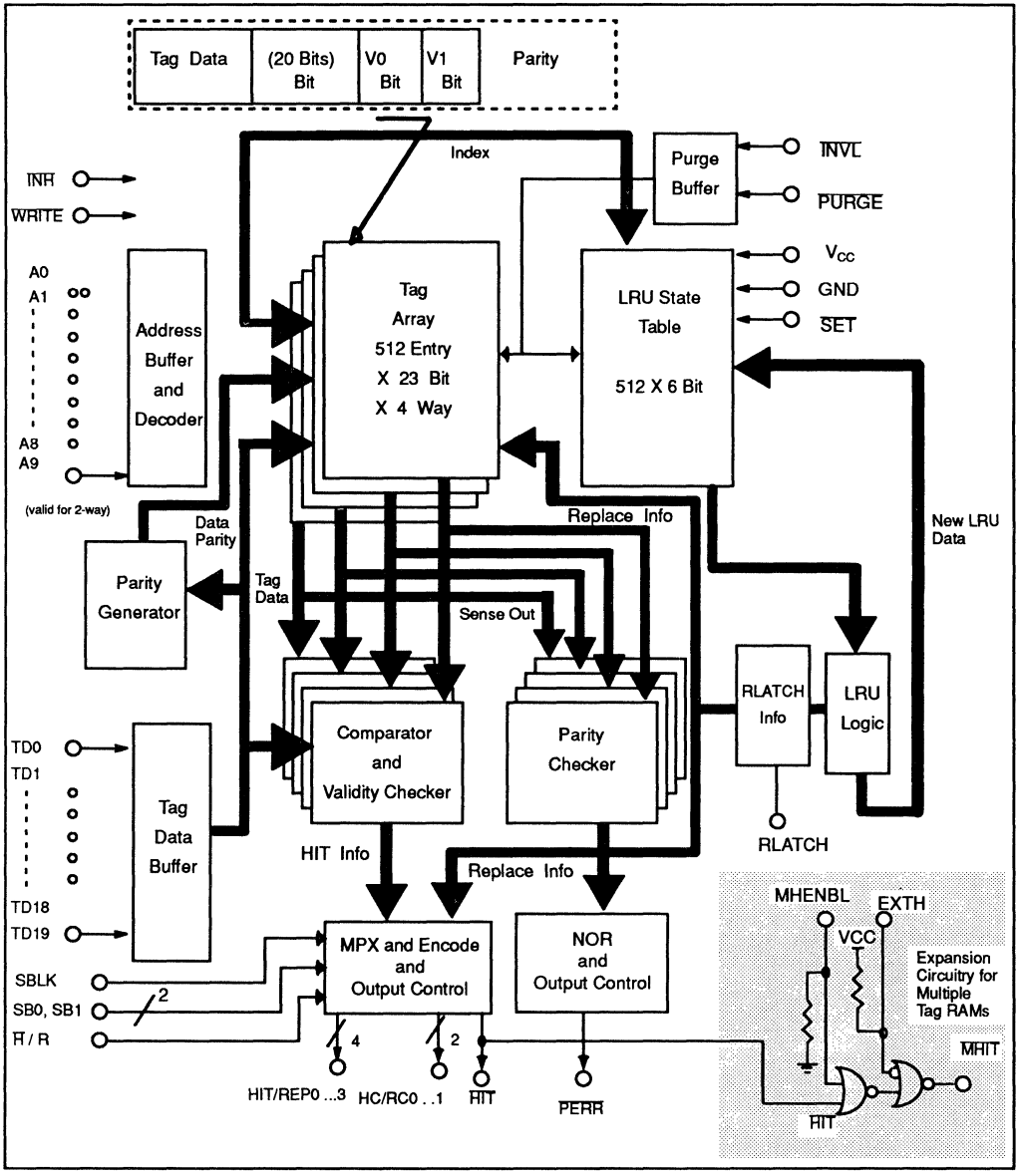


Figure A–1–1. MB81C51 Block Diagram

10

A–1.4 Differences Between Two-way and Four-way Configuration

Figure A–1–1 describes a four-way configuration. If the device is to be configured as a two-way configuration, the only deviations are as follows: the address inputs are now A0 through A9 (10 bits), the TAG and control memory cell array becomes 1024 x 23 x 2 bits and the LRU state table becomes 1024 x 2 bits. The four-way configuration will typically be referenced in this Application Handbook unless otherwise noted.

Although its functionality is extended beyond other tag RAMs and its performance is unsurpassed, high volume manufacture and availability in the industry standard 68-pin PLCC package makes the MB81C51 the most inexpensive cache tag RAM in its performance class.

A–1.5 General Functional Modes of the MB81C51

Cache, as a subset of main memory, requires management hardware to determine whether data resides in cache or the main memory. It must also be able to retrieve and store in cache data that is requested, but missing. Since cached data has a duplicate copy (or *parent* copy) in main memory, cache management hardware must also ensure that, over time, the copies remain identical; i.e., coherency is maintained. To implement these management functions, the following types of device operation are provided by the MB81C51. These device functions are illustrated by the waveforms of Figures A–1.2 through A–1.5, described in corresponding order below.

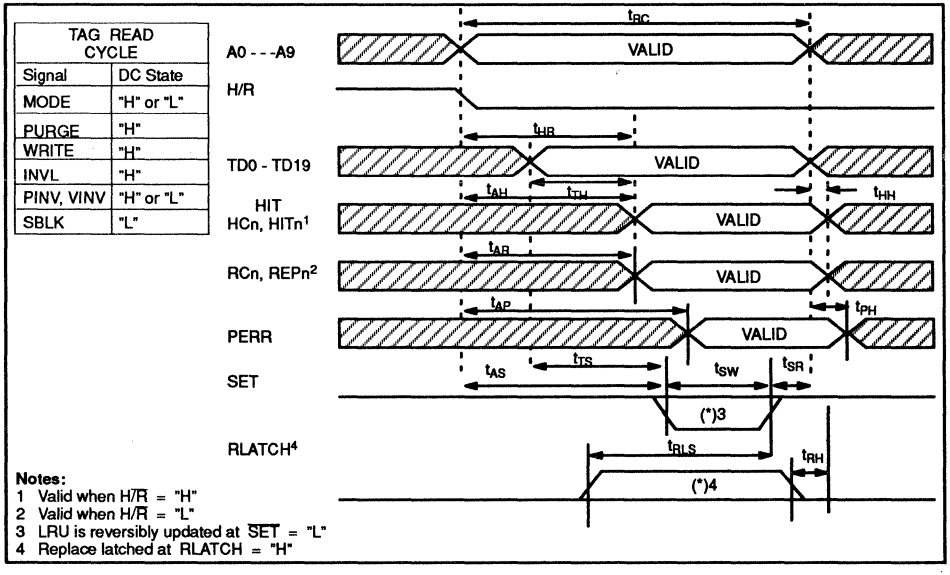


Figure A–1–2. Tag Read Cycle

A–1.5.1 Read Cycle

The read cycle is invoked when WRITE', PURGE' and INVL' are all high, as shown in Figure A–1.2. This cycle accepts an index address and a tag for comparison to determine whether the requested tag is resident in cache. A tag is resident if the tag provided to the TD0..TD19 inputs matches one of the tags

stored at any set element selected by the index (A0..A9). From this search and compare, a hit or miss is generated. The hit is then used to signal the processor that the bus cycle will successfully complete without wait states (typical). Hit information outputs denoting the set element that was hit are then used to select data from the data buffer.

To avoid potential confusion, keep in mind that whether the cache cycle to be performed is a read or a write, the tag operation to be performed will first be a read to determine whether the data is resident in cache.

The read cycle supports two modes (depending whether or not the least recently used (LRU) state table is updated). The LRU table tracks the age of each set element relative to the others at that same index to determine which is the best candidate for replacement. Whether or not the LRU table is updated is determined by SET'. Asserting SET' (UPDATE mode) forces the LRU UPDATE, while maintaining SET' high inhibits the LRU update, whether a hit or miss occurred (termed an *inquire* cycle). The read cycle in general, regardless of the mode, is termed *interrogation*. (See Section 2.3 for more details on the LRU.)

Read cycle may be initiated by the processor when reading or writing, in which case the LRU update mode is used. The read cycle may also be initiated by the system bus in the case of bus monitoring, during which the inquire cycle would be invoked because an update of the LRU is not desired. (Bus monitors are discussed in Section 5.4.) A processor-invoked read or write will first perform a cache tag read to determine residency. If the read cycle determined a miss, then a line in cache (termed a *slot*) is usually allocated requiring the tag to be written to the tag buffer. Therefore, a processor read or write cycle resulting in a miss is usually followed by a tag write cycle.

A–1.5.2 Write Cycle

A write is initiated following a missing read cycle by asserting WRITE' (low) and SET' according to the waveforms shown in Figure A–1–3, which also shows that INVL', PURGE' and INH' should all be deasserted throughout the cycle (high). During the operation of the write, the MB81C51 writes the tag and the internally generated parity bit to the line specified by the index (A0..A9) at the set element location specified by HITn/REPn or SB0 and SB1 (see Section A–1.6.2). The write operation updates the LRU table to show that this entry is now the newest one (details given in Section A–1.5.3). As a result of the write operation, the previous data is overwritten.

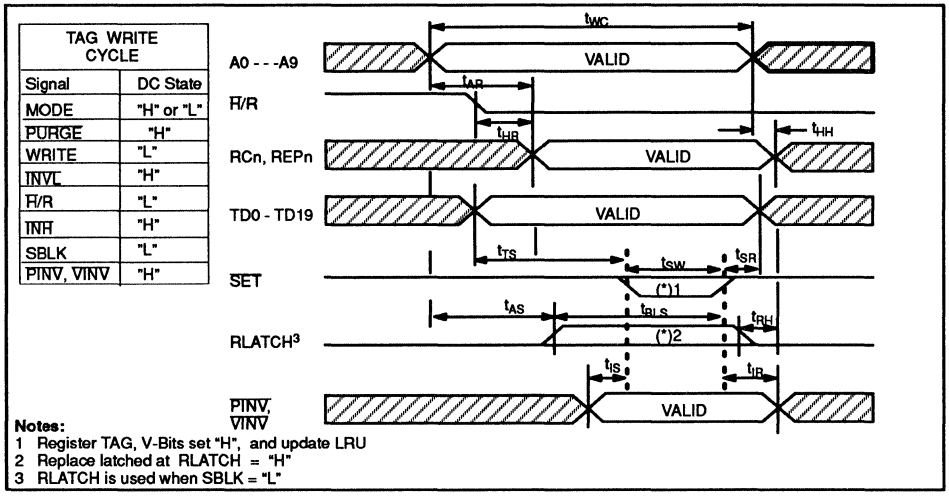


Figure A–1–3. Tag Write Cycle

A–1.5.3 Selective Invalidation (Partial Purge)

When the bus monitor initiates an inquiry to determine if a system bus cycle is referencing cached data, the option of invalidation versus updating is confronted if the entry is resident. If an update is to be performed, then the tag read cycle is used to determine residency, followed by a data buffer write to update the entry. However, if invalidation is the preferred approach, then selective invalidation is performed (see Figure A–1–4).

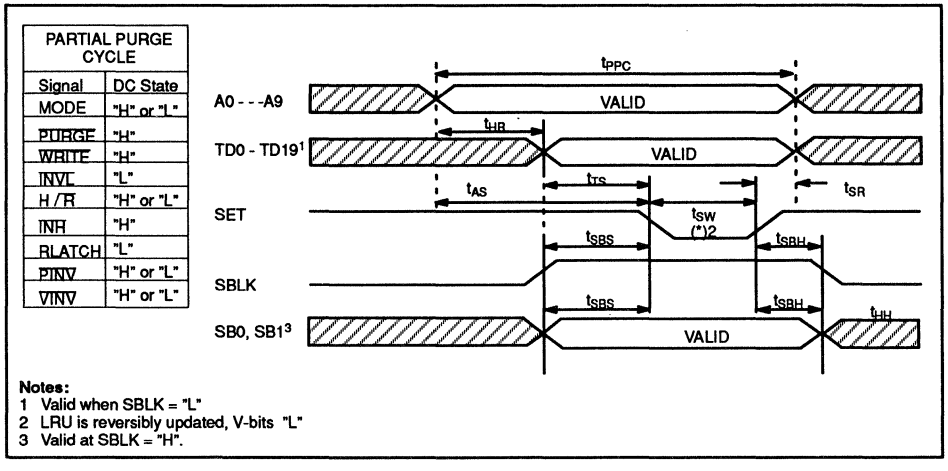


Figure A–1–4. Partial Purge Cycle (Selective Invalidation)

To invalidate specified entries, the MB81C51 supports a selective invalidation (or partial purge) for which two modes exist, explicit and implicit invalidation. In the case of implicit invalidation, the system

need only supply the index address, as it normally would for a read cycle, and, if the 81C51 determines the entry is resident, invalidates it. The invalidation is executed in one cycle,and updates the LRU state to indicate that this invalidated location is the preferred one for subsequent replacement. If a miss occurs when invalidation is attempted, then no entry is invalidated and the tag buffer and LRU state remain the same.

Explicit invalidation always invalidates the set element selected by SB0 and SB1, while implicit invalidation requires a tag to successfully compare against. Both modes require an index to select the line however, and the result of either invalidation operation is to clear the validity bits to indicate that the entry has been invalidated. Note that neither the data nor the tag is ever modified during invalidation; only the validity bit which marks the entry absent is modified.

A–1.5.4 All Purge

The All Purge, also termed an indiscriminate flush, or clear, cycle initializes the cache to reflect that there are no entries resident and resets the LRU state table (see Figure A–1–5). In virtual cache systems (see Section 6.0), it may be necessary to flush cache when changes in the virtual address space occur (as during context switches). Flushing is also required for power-on reset and, perhaps, following the detection of certain bus errors (such as cache parity errors).

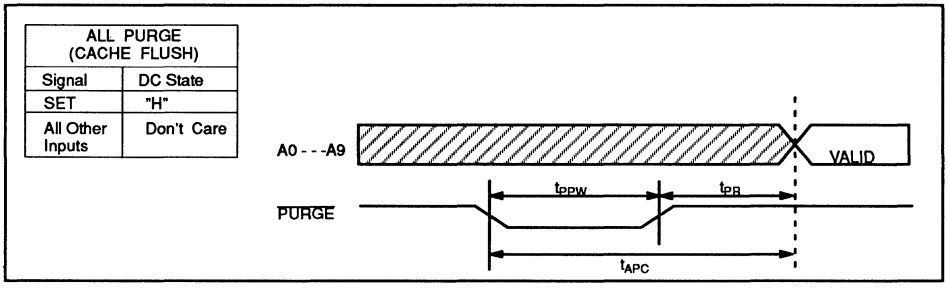


Figure A–1–5. All Purge Cycle

The PURGE' signal which invokes this mode is an asynchronous input which inhibits all other inputs except SET'. Therefore, all other inputs are don't care, while SET' remains de-asserted (high) throughout the purge operation. Any cache request will result in a miss following the indiscriminate flush, since the validity bits of all lines and all set elements have been cleared.

A–1.6 The Tag and Control Bits: Use and Response

This section presents the structure of the tag array words, how operations affect these words and how to use the outputs controlled by them.

A–1.6.1 Description of the Tag Memory Entry

Referring to Figure A–1–6 (the structure of the tag buffer entries), you will note that each entry consists of three fields:

1. the tag field
2. the validity bits

3. the parity bit

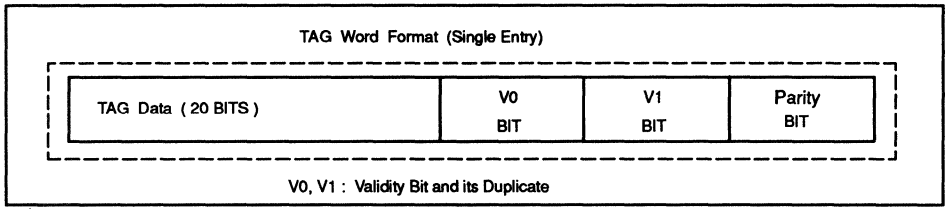


Figure A–1–6. Tag Memory Array

A–1.6.2 The Tag Field

The tag entry, TD0..TD19, is a field of the address that corresponds to data residing in the associated data buffer. There are a number of tags at a given index address equal to the number of ways in which the cache is configured (or degree of associativity) in the tag buffer. When an index is applied in read mode, it is the tag field of all set elements that are fed to the comparators, along with the TD0..TD19 inputs, that define the tag for which we are searching.

A–1.6.3 Control Bits (Validity And Parity)

Validity bits exist for every set element at all index addresses to indicate which are invalid and which are valid. An invalid entry will force a miss, even if its tag matches the requested tag. These bits are active high (low indicates an invalid entry), while mutually exclusive bits indicate a bit error in one of the validity bits. Thus, duplicate validity bits are provided for data integrity. Without duplicate validity bits, a single-bit error, altering the state from low to high, could occur. The single-bit error could interpret an invalid entry as a valid entry resulting in an erroneous instruction/data fetch. With duplicate bits, a double-bit error must occur. Validity bits are cleared in the all purge and selective invalidation cycles and set during the tag write cycle.

Figure A–1–6 also shows the location of the duplicate validity bits of each entry, as well as a *parity bit*. This is a tag parity bit which is minimizes the possibility of tag corruption. The parity bit is generated and stored along with the tag and validity bits during the tag write operation. When a tag read or selective flush operation is performed, the tag parity bit is again generated and compared against the stored parity bit for discrepancy.

A–1.6.4 Tag or Validity Bit Parity Errors

If a parity or validity bit error occurs (perhaps due to an alpha particle induced soft error), then corruption has occurred. If the affected entry is a valid one, this false tag may match during a look-up, resulting in false instruction/data fetches. Therefore, the signal PERR' is used to indicate validity bit errors and, if the tag is not invalidated, tag parity errors as well. The Boolean equation for this PERR' signal is:

Eq A–1–1

$$\overline{PERR} = \text{the NOR of } PE0..PE3$$

where

$$PEn = (V0n + V1n) * PEn + (V0n \text{ XOR } V1n)$$

NOTE: *V0n* and *V1n* are the 0^{th} and 1^{st} validity bits of the n^{th} set element, and *PEn* is the parity error bit for the n^{th} set element.

When a parity error does occur, the access should be treated as a miss. Furthermore, since there is no way of isolating the set element that introduced the parity error, we may either treat all further accesses of this location as a miss and essentially inhibit the use of the set element until the next flush occurs or, alternatively, we may choose to respond with a more effective action. This action may be performed in hardware or software and performs one of the following functions:

1. Flush all set elements at the affected index.
2. Flush the entire cache, or at least the affected device.

To invoke this error recovery, the PERR' signal may be used to generate a bus error signal for either operating system resolution or as a signal for a hardware controlled flush. (In either case, the acknowledgement to the processor may have to be delayed to allow time for the fault resolution.)

A–1.7 The HIT, Its Detection, and Related Signals and Functions

When an address is supplied to A0..A9, it will access the tag memory array, as well as the LRU state table. In the case of the tag memory, the address will access all set elements simultaneously. After the internal SRAM access time from the address transition, all set elements at that line are presented to the comparators. The tag fields of each element are then compared with the tag data applied to inputs TD0..TD19. A match of any set element asserts HIT' which, along with the PERR' signal, should be used to determine if a true cache hit has occurred. The Boolean equation for HIT' is:

Eq A–1–2

$$\overline{HIT} = \text{the NOR of } hit0..hit3$$

where

$$HITn \text{ is the HIT result of th } n^{th} \text{ set element.}$$

A–1.7.1 Generating HIT from Multiple CTRAMs

As will be shown in Appendix A–1.10.3, when integrating more than one MB81C51 into the tag buffer, it becomes necessary to gate the HIT' outputs of the individual tag RAMs to generate a single tag buffer HIT' signal. In the MB81C51, when MHENBL (Modified Hit ENaBLe) is asserted (high), MHIT' will be asserted (low); if either the internal HIT' or the external HIT (EXTH, active high) are asserted, MHIT' is deasserted (high). When MHENBL is driven low or floats (its input has a pull-down resistor) and EXTH is high or left floating (it has a pull-up resistor), MHIT' defaults to a low. The use of this feature is described in Appendix A–1.10.3.

A–1.7.2 Selection of Hit/Replace Information

When a hit occurs, it is necessary to select the proper set element from the data buffer to be read or written. The HITn/REPn outputs (4 bits, active HIGH, which indicate the set element that was hit) are used for selection of the proper set element. These signals are also encoded and output on HC0/RC0, HC1/RC1, as illustrated by Table A–1–1. The decoded information (HITn/REPn) is designed to drive chip or output enable signals to banks of RAMs whose data outputs are dotted; the encoded outputs are ideal as address inputs to the data buffer RAMs.

Table A–1–1. Encoding of Hit and Replace Locations for 4-Way Buffers

INPUT		INTERNAL INFO.				OUTPUT							
						DECODED				*ENCODED*			
MODE	A9	hit 0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT 0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	HIT*	MODE
H	X	L	L	L	L	L	L	L	L	L	L	H	
H	X	H	L	L	L	H	L	L	L	L	L	L	
H	X	L	H	L	L	L	H	L	L	H	L	L	4-Way
H	X	L	L	H	L	L	L	H	L	L	H	L	
H	X	L	L	L	H	L	L	L	H	H	H	L	

* Ouput of HIT is Valid when H/R = "H".

If two degrees of associativity are employed, the HITn/REPn or HCn/RCn outputs must be gated to generate simple signals for set element selection of the data buffer. Table A–1–2 illustrates the coding of the HITn/REPn and HC0/RC0, HC1/RC1 outputs for the two-way case. However, gating these signals in the following way produces the desired results:

Eq A–1–3a

$$GHIT0/GREP0 = (HIT0/REP0 + HIT1/REP1)$$

Eq A–1–3b

$$GHIT1/GREP1 = (HIT2/REP2 + HIT3/REP3$$

and if encoded signals are used:

Eq A–1–4

$$GHC0/GRC0 = (HC1/RC1)$$

Table A–1–2. Encoding of Hit and Replace Locations for 2-Way Buffers

INPUT		INTERNAL INFO.				OUTPUT							
						DECODED				*ENCODED*			
MODE	A9	hit 0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT 0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	HIT*	MODE
L	L	L	X	L	X	L	L	L	L	L	L	H	
L	L	H	X	L	X	H	L	L	L	L	L	L	
L	L	L	X	H	X	L	L	H	L	L	H	L	2-Way
L	H	X	L	X	L	L	L	L	L	L	L	H	
L	H	X	H	X	L	L	H	L	L	H	L	L	
L	H	X	L	X	L	L	L	L	H	H	H	L	

* Ouput of HIT is valid when H/R = "H".

In the case of a miss, we need to know which element should be replaced, based on the LRU algorithm implemented internally. For convenience this information is also output on HITn/REPn and HC0/RC0,HC1/RC1. To differentiate hit information from replace information, the H/R' signal is provided as a select for both encoded and decoded outputs (refer to Figure A–1–7 showing the internal mux structure).

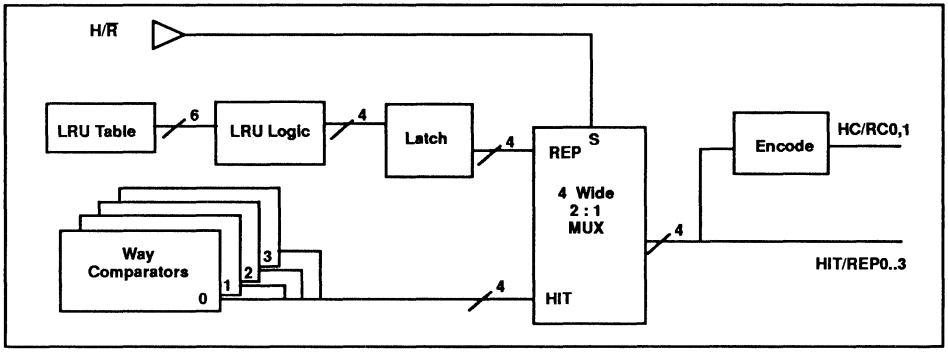
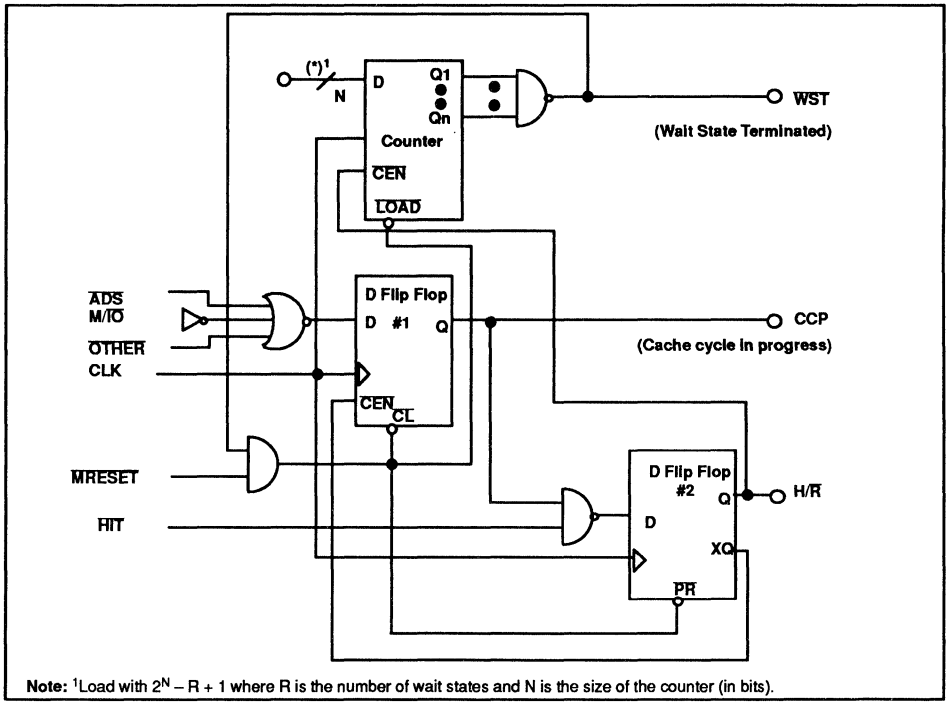


Figure A–1–7. Mux Circuit for Selecting Hit or Replace Information

When a miss is detected, a delay occurs because the cache controller must request the missing data from main memory. This request suspends the processor by inserting wait states. Therefore, the time to detect a miss is not as critical as it is for detecting a hit and suggests that the state of the H/R′ signal should default to high, as demonstrated by the sample circuit in Figure A–1–8. H/R′ is then reset after a miss is detected, in order to select the replacement information. The replacement information then appears t_{HR} (Hit/Replace select time) after H/R′ goes low.



Note: [1]Load with $2^N - R + 1$ where R is the number of wait states and N is the size of the counter (in bits).

Figure A–1–8. Example of Circuit to Generate H/R

A–1.7.3 Circuit Example (to Generate H/$\overline{R}$)

At the beginning of the bus cycle, CLK (1) samples the status lines M/IO' and OTHER', which are used to qualify the cacheable address space (contingent on the assertion of ADS') and (2) generates cache cycle in progress (CCP), if all are active. CCP going high enables HIT' to the D input of flip-flop #2, whose output is high by default. These two activities permit hit information to be selected as quickly as possible, while enabling replace information to be selected one cycle after the initiation of the cache access (in case of a miss). Consequently, the cache hit time (tAH), plus the prop delays and set-up of HIT' on flip-flop #2 are less than the CLK period. HIT' may directly generate the acknowledge to the processor while H/R' drives the H/R' and WRITE of the 81C51 tag RAMs. H/R' and the WE' from the processor are ANDed to drive the WE(M)' of the data buffer SRAMs. The WE(M)' is synchronized by a D flip-flop clocked by CLK, (not shown).

If a miss occurs, H/R' falls on the second cycle of the cache operation, enabling the wait-state counter (already loaded on reset or previous wait-state completion) with $2^N - R + 1$ (where N is the size of the counter, in bits, and R is the number of cycles to wait). Successive CLKs will increment the counter until the outputs are all high. At that time wait state terminates (WST') and triggers, setting up a CLEAR on flip-flop #1, a PRESET on flip-flop #2 and a LOAD on the counter (all synchronous to the same rising edge of CLK). The replace information is then selected throughout the write to the data and tag buffers.

CCP, indicating a current active cache cycle, could be gated with WE(M)' to control the bus transceivers and registers for data transfer from/to main memory, as well as a device enable for the data buffer RAMs. Notice that H/R' will disable the clock of flip-flop #1 in the case of a replace, thus maintaining CCP at a high state until the replace is complete.

Different designs will employ different replacement strategies and use different processors with varying control signals and timings. This example is useful only as a generic guideline for the generation of important signals used to control cache. For example, this circuit assumes a miss will always be replaced within the same number of clock cycles (R) although it is usually necessary to gain access first to the system bus, which may not be idle.

A–1.7.4 RLATCH – Its Function and Use

After a miss is detected, the replace information needs to be internally latched since a subsequent tag write cycle will cause a change in the LRU table and, consequently, a change in the replacement information. As noted in Table A–1–3, the Pin Description Table, the RLATCH signal is used to stabilize the replace information because its rising edge will latch the information (which remains valid until RLATCH goes low again) plus a disable time (tRH). RLATCH rising should lead the rising edge of SET' (during the tag write cycle following the miss) by tRLS and remain asserted until the replace information is no longer needed externally.

Table A–1–3. Functional Pin Description of the MB81C51

Signal	I/O	Type	Active	Sync to Set	Function
A0 - A9	Input	Data	High	Yes	INDEX address inputs to the TAG buffer and LRU table.
TD0 - TD19	Input	Data	High	Yes	TAG data for comparison against internal TAG entries at the applied INDEX address (A0 . . A9)
MODE	Input	Select	——	Yes	Selects TAG RAM organization: MODE — ORGANIZATION 1 — 512 x 4 way 0 — 1024 x 2 way
$\overline{\text{WRITE}}$	Input	Enable	Low-Level	Yes	Active only in cycles in which SET is asserted. This signal defines a WRITE (active low) or READ (high) cycle.
$\overline{\text{PURGE}}$	Input	Control	Low-Level	No	This asynchronous signal resets the V bits for all entries in the TAG RAM, and initializes the LRU.
$\overline{\text{INVL}}$	Input	Control	Low-Level	Yes	This level sensitive signal, sampled by SET, is used to initiate the Selective Invalidation ("PARTIAL PURGE") mode.This operation invalidates the "V" bits and reversibly updates the LRU table for a single entry.
$\overline{\text{INH}}$	Input	Disable	Low-Level	No	This level sensitive signal, asynchronous to SET. Inhibits all operations except for the PURGE function, when asserted.
H/$\overline{\text{R}}$	Input	Select	——	No	This signal determines whether HITn/REPn and HCn/RCn are selected to output hit information, or replace information H/$\overline{\text{R}}$ STATE — OUTPUT STATE 0 — Replacement Set Element Selected 1 — Hit Data Selected
RLATCH	Input	Clock	Latch Enable ↑	Yes	This signal enables the internal latch that clocks the LRU replacement data.
SBLK	Input	Select	——	No	This signal controls whether the way selection for replacement or invalidation comes from an outside source, described by SB0 and SB1, or whether the internal replacement way is selected according to the LRU algorithm. SBLK STATE — REPLACEMENT SOURCE 0 — Internal 1 — External
SB0, SB1	Input	Data	High	Yes	These signals are "don't care" in the case of SBLK = L. However, when the external replacement source is enabled, they select which way is to be replaced or invalidated.
$\overline{\text{SET}}$	Input	Clock	Latch Enable ↑	——	This clock signal is used to update the LRU table and stabilize replacement data. In READ mode, if it is not asserted, a tag compare can occur without a LRU update.
$\overline{\text{HIT}}$	Output	FLAG	Low-Level	——	This output is the NOR of the 4-way comparators thus, when asserted, indicates that the tag applied to TD0..TD19 matches at least one set element at the line specified index
HITn/REPn	Output	Data	High	——	These signals indicate which way was hit (if any) or which way should be replaced. The selection of the hit or replacement is controlled by the H/$\overline{\text{R}}$[1] signal. (See Tables A–1–1 and A–1–2.)
HCn/RCn	Output	Data	High	——	These are the encoded HITn/REPn signals. (See Tables A–1–1 and A–1–2.)
$\overline{\text{MHIT}}$	Output	Flag	Low	——	Indicates internal ($\overline{\text{HIT}}$) or external (EXTH) HIT is detected. This output is low when disabled. Used for multiple device configuration to expand cache depth.
MHENBL	Input	Select	High	——	Enables multiple $\overline{\text{HIT}}$ logic by setting $\overline{\text{MHIT}}$ to the NOR of EXTH and HIT signals. Disabled by floating or pulling low.
$\overline{\text{EXTH}}$	Input	Flag	High	——	External HIT signal (driven from another 81C51 by an inverter) when unused, should float or be pulled high.

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A simple way to generate RLATCH is to use SET', qualified by the WRITE' signal. The designer should be careful that *tRLS* is satisfied. Satisfaction is guaranteed as long as the qualifying WRITE' signal lags SET' going low by no more than *tSW - tRLS - tL* (where *tL* is the propagation delay in generating RLATCH from SET' and WRITE').

A–1.7.5 LRU Logic and Replacement

The LRU logic (its algorithm is described in Section 2.3) is designed to track the age of each tag since its last reference and relative to the other tags in the same set. The age information is used to determine which set element, at a given index, is to be replaced when a miss occurs. The replacement data specified by the 81C51 corresponds to that set element specified by the LRU as the least recently used; i.e., a good candidate for replacement. As the state table (Table A–1–6) reveals, the LRU table is either forwardly or reversibly updated (it remains unaffected by certain CTRAM cycles) to reflect any change in the relative age of the element as a result of the operation.

A–1.8 The Signals of the MB81C51

This section discusses the use and purpose of chip level signals, referring to the pin description table (Table A–1–3.). The use and effect of the INH' and SBLK (including SB0 and SB1) are discussed in detail.

A–1.8.1 Pin Description Table and Discussion of Signals

Table A–1–3 lists all the device pins, their basic timing nature (synchronous or asynchronous) and other pertinent information. Since the storage arrays (tag buffer and LRU table) of the MB81C51 are constructed by a mixed MOS SRAM approach, it should not be surprising that similar timing and signals are required for its operation, along with timing related to comparison, update and flush operations.

A–1.8.2 The INH' Signal and Its Effect

The INH' signal, as determined from the pin description table, serves primarily two purposes:

1. Inhibits all functions including tag read (either update or inquire), tag write, and selective flush. It does not inhibit the all purge operation.
2. INH' sets all outputs to predetermined levels that are most suitable for permitting multiple devices to be stacked in depth, and generally preventing any side effects arising from devices that have been disabled. It does NOT place the outputs into a high impedance state since, typically, the outputs will feed combinational logic. Table A–1–4 illustrates the output states and conditions of the inputs when INH' is asserted.

Table A–1–4. Output States for INH' = "L"

Signal Name	State
HITn/REPn	L
HCn/RCn	L
HIT'	H
PERR'	H

Note: ALL inputs are inhibited by the INH' active except PURGE' which is asynchronous.

A–1.8.3 SBLK and External Way Selection

The SBLK signal selects between internal and external replacement information and is in effect only during the tag write cycle or invalidation (selective flush). When SBLK is asserted, SB0 and SB1 signals (or simply SB0 in the two-way case) become the external set element selection lines for the tag RAM, as specified in Table A–1–5. This mode is very useful for flushing all set elements at a particular index or implementing another replacement method.

Table A–1–5. External Element Selection Using SBLK

Cycle Type	SBLK	Set Element Selection Scheme	Effect on LRU Table
Write Cycle	L	LRU Selects Way	Always Updated
	H	SB0 & SB1 Select Way	Always Updated
Selective Invalidation	L	LRU Selects Way	Update on a Hit
	H	SB0 & SB1 Select Way	Always Updated

A–1.9 Device Mode State Table

The MB81C51 performs all basic operations necessary to support cache operations initiated by hardware and software including interrogation (look-up), retrieval control, replacement, update, and coherency by selective and indiscriminate flush functions. The function table, Table A–1–6, provides a description of the input states required to invoke these operations, and the effect of these modes on the internal states, such as the tag array and the LRU table.

Table A–1–6. MB81C51 Functional Modes Table

Input Signals					Tag Data	Control Data		Replace Data	Cycle Type
INH	PURGE	SET	WRITE	INVL	Tag	P Bits	V Bits	LRU Data	Function Mode
L	H	X	X	X	No Chg	No Chg	No Chg	No Chg	Inhibit
H	H	H	X	X	No Chg	No Chg	No Chg	No Chg	Tag Read without LRU Update
H	H	↓	H	H	No Chg	No Chg	No Chg	No Chg or Update[1]	Tag Read with LRU Update
H	H	↓	L	H	TD0 to TD19	SET	H	Update	TAG Write
X	L	↓	X	X	X	X	L (all) or L[2]	Reset or R'Update[1]	Cache Clear
H	H	H	H	L	No Chg	No Chg	L[2]	R'Update[1]	Partial Purge Selective Invalidation

Notes:
[1]When (SBLK = "L" S ($\overline{HIT}$ = "H"), LRU → NO CHG
[2](SBLK = "L" S ($\overline{HIT}$ = "H"), V BITS → NO CHG

KEY	
X	Undefined
No Chg	Data Remains Unchanged
Update	LRU Forward Update
Reset	LRU Initialized
R'Update	LRU Reversibly Updated

A–1.10 Configuring the MB81C51 for Various Applications

The configuration of the number of set elements in the MB81C51 is controlled by the MODE pin, which selects between two-way or four-way set associativity. MODE controls the internal organization of the tag array, LRU table and associated logic. Since all affected internal logic is also reconfigured to support the selected organization, MODE provides for a simple hardware reconfiguration option.

The initial organization of tag array and the LRU table is as follows:

	Ways	Entries
Internal Tag	2	1024 x 23 bits
		4512 x 23 bits
LRU Table	2	1024 x 1 bit
	4	512 x 6 bits

A–1.11 Defining the Tag and Index

The address bus interfacing to cache is composed of several distinct fields. The descending order of significance for these fields are the tag, index and block. Figure A–1–9 illustrates the relative significance of each field and the relationship of these to the virtual memory fields.

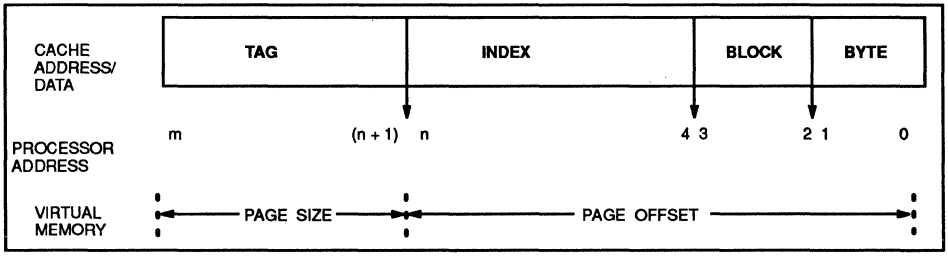

Figure A–1–9. Address Bus Fields

A–1.11.1 Choosing the Index and Tag Size

The MB81C51 permits tags up to 20 bits in size, and index sizes of 10 bits per each device (configured as two-way implementation) or 9 bits per device (configured as four-way implementation). However, the 81C51 may be expanded in depth in multiples of 1024 (two-way) or 512 (four-way) lines. Furthermore, any line or block size may be used, therefore providing for large caches to be implemented with a single MB81C51.

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The size of cache is defined in terms of its depth (D), block size (B) and degree of associativity (W) in the following way:

Eq A–1–5a

$$cache\ size = D * B * W$$

Since the index is used to address the cache in depth, the size of the index address field should be (in bits):

Eq A–1–5b

$$index\ size = LOG2(D)$$

For example, if we have a two-way cache with a block size of 4 words, an 18-bit tag (2-bit byte select) and a 10-bit index, we then have a cache buffer that is $2 \bullet 4 \bullet 2 \bullet 2^{10}) = 8K$ words, with a tag buffer depth of 2K tags. This 32K byte can be implemented with a single 81C51.

A–1.11.2 Configuring the Tag Buffer Given the Index Size

In certain implementations, if caches of larger than 2K lines are desired, multiple 81C51s will be needed to construct the tag buffer. If a larger cache is desired, it is easily implemented by extending the 81C51s in depth.

There are fundamentally two ways to "stack" multiple 81C51s in depth to increase the number of available tags. One way is to gate the signals. The second way is to use MHIT'. A discussion of both implementations is in the following sections.

A–1.11.3 Gate Signals to Implement Multiple 81C51s in Depth

The most significant bits of the index address are decoded and used to generate inhibit signals (INH') when gating the signals. In the inhibit state, the outputs go to values that permit simple interfacing of multiple devices, as was shown in Table A–1–4. Therefore, we need only gate the individual HIT' and the individual PERR' signals, and multiplex the HITn/REPn or HCn/RCn signals (depending on which data buffer selection scheme we are utilizing). Figure A–1–10 illustrates this control and mux logic with an example of a four-way set associative implementation that has a depth of 2K and supports 8K blocks. To extend beyond this configuration, realize that the N most significant index bits are used to address 2N different 81C51s, each with a size of 2K blocks and a depth of 512 (4-way) or 1K (2-way). Two 2N-wide AND gates are used to generate the system GPERR' and GHIT' outputs. The N most significant index bits feeds N of 2N decoder which drives the INH' signals of the individual devices. The most significant index bits are also used to select a W-wide (where W is the number of ways) 2N-to-1 mux which selects from the individual HITn/REPn lines that drive the data buffer. If the NCn/RCn (encoded) signals are used, then a LOG2 (W) wide 2N mux is needed. However, if individual data buffer RAMs are driven by the HCn/RCn lines of each individual tag RAM, this muxing is not necessary.

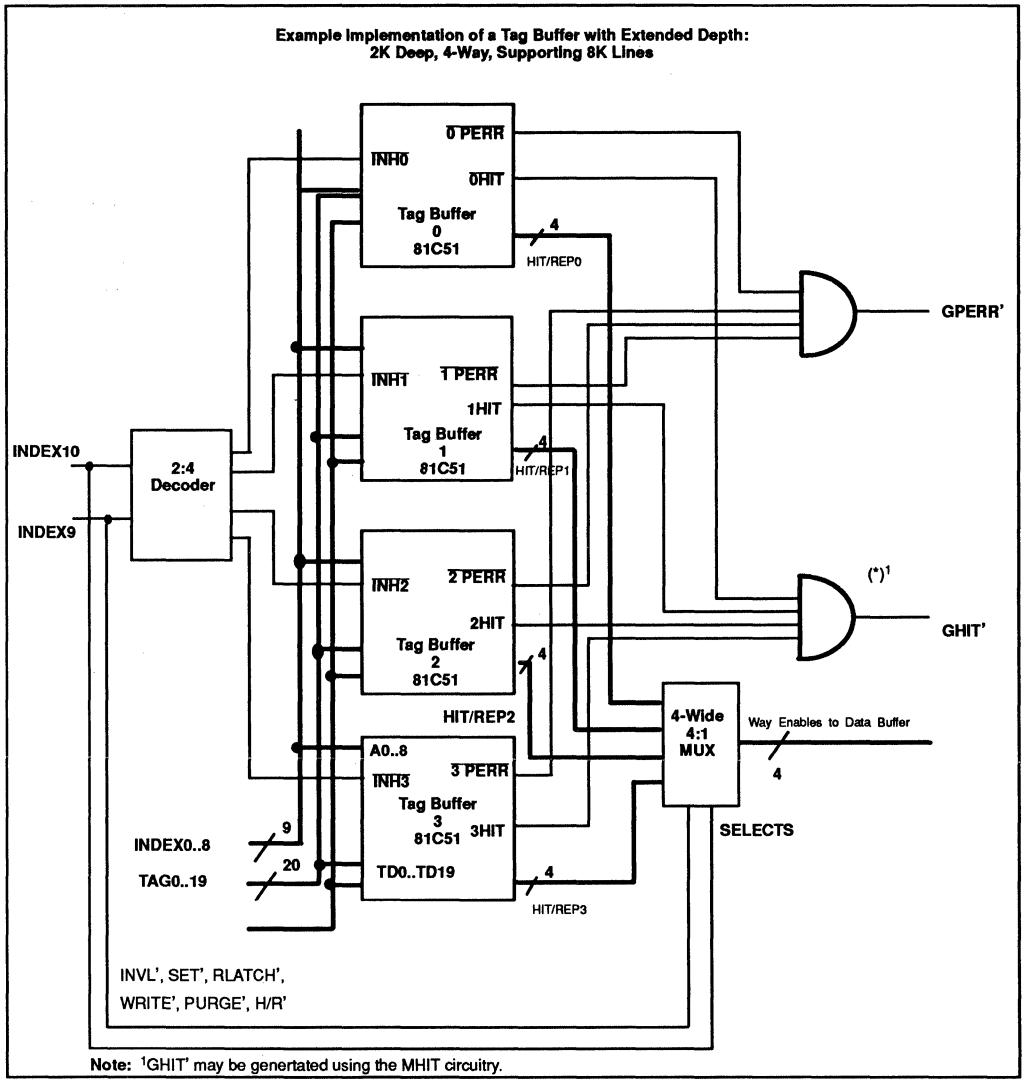

Figure A–1–10. Example Implementation of a Tag Buffer with Extended Depth

As an example, to construct a 2-way tag buffer with 16K tags and a block size of 8K to yield a 64K word tag buffer that uses the encoded hit/replace select lines (HCn/RCn), the implementation would be as follows:

$$W = 2\ ways \Rightarrow 1K\ depth\ per\ device 2N = 16K/1K = 16\ MB81C51s$$

Notice that since INH' inhibits all device functions except ALL PURGE, (usually performed on the entire cache simultaneously), it can be easily used to isolate devices for any operation. Therefore, it can extend the TAG in depth with no change in function and an addition of only a mux, a decoder and two ANDs. Since INH' is the device selector and inhibits/enables all functions except ALL PURGE, the functions of reading (with update or simply inquiry), writing (in the case of replacement) and selective invalidation are performed as if only one 81C51 were utilized.

A–1.11.4 Configuring Multiple MB81C51s Using MHIT'

The MB81C51 supports expansion of cache by gating the internal HIT' signal with an external HIT signal called EXTH (active high) when the MHENBL input is asserted (high). This permits a system hit (MHIT', active low) to be quickly generated from multiple devices without the use of external logic, except an inverter that complements and drives the HIT' output of the other MB81C51(s).

It is also possible to support more than two cache tag RAMs by feeding the MHIT' output of the second device to the EXTH input of a third via an inverter, and so on in "daisy chain" fashion. The method of parallel gating presented in Figure A–1–10 provides a high-speed solution when many tag RAMs are arranged in depth. For implementations requiring two or three tag RAMs, the "daisy chain" provides the highest speed solution with minimum hardware.

A–1.12 Unused Inputs/Outputs

If four-way associativity is selected by the MODE pin, then only nine address bits are required, as opposed to the ten required for the two-way case. In the case of a four-way implementation, the designer should then use address pins AD0..AD8 and tie AD9 high (since better noise margin exists when it is pulled high). Additionally, the tag inputs TD0..TD19 comprise a 20-bit word in which the unused bits should be tied high (VIH as the minimum or higher), preferably to the power rail.

In general, no input signals of CMOS devices should float, but rather should reference some valid voltage level (VIL (max) or VIH (min)). Unused outputs, however, such as HCn when HITn is used instead, should be left open.

A–1.13 Supporting Copyback with the MB81C51

The local cache must support functions initiated by the local bus monitor or central controller, such as change of privilege, invalidation, and update. These operations are detected as system bus activity and are routed to the local cache tag buffers to determine residency and then respond appropriately if resident. Implementing copyback within the cache tag buffer requires integrating the privilege bits and dirty bits into the tag buffer and providing support hardware to read and modify these bits. To perform an invalidation of a line, for example, the bus monitor/cache controller would perform a selective invalidation on the tag buffer with the system bus address. Since the HC0/HC1 information is output for invalidation cycles, this information would be used to select the associated descriptor bits in an external descriptor RAM. If the dirty bit was set, the line could then be updated to main memory. Read-only protection can be enforced in a similar way by using HC0/HC1 to select the descriptor bits and generating the acknowledge to the processor depending on the state of the read-only status bit.

Since the MB81C51, as previously explained, does not directly support the flushing of dirty entries that must be written to main memory, the user may find that implementation of write-through and buffered write-through caches (either real or virtual) to be more efficient and simpler to implement. If performance is of utmost importance, buffered write-through has proven to be faster in average cache time than copyback options except in those systems where bus traffic makes write-through an impossibility.

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