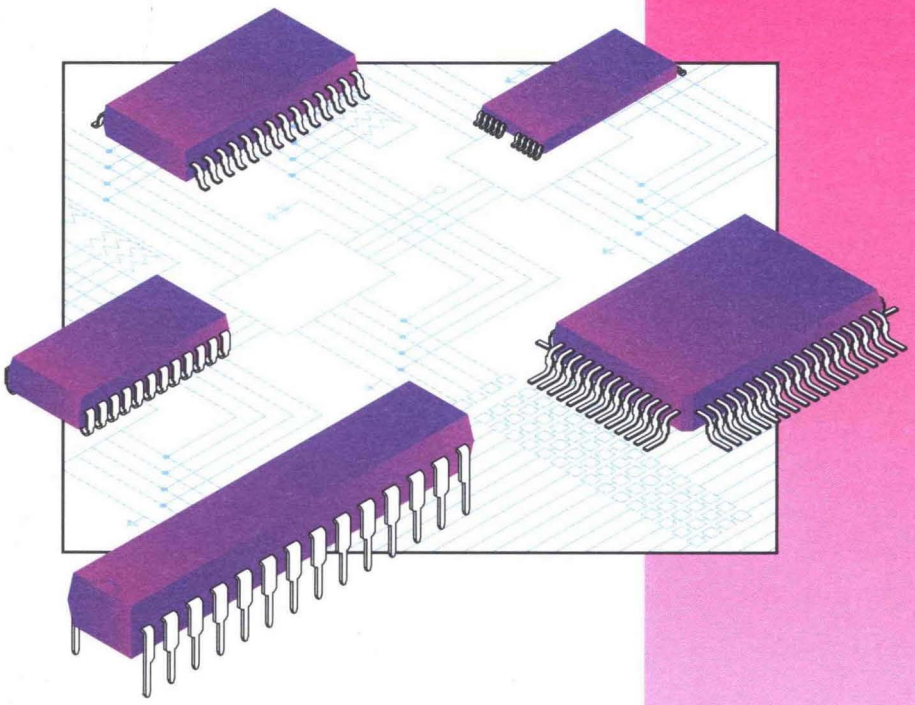
FUJITSU

Static RAM Products

1991 Data Book



Data Book

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1991
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Book

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PREFACE

This data book contains the latest product information for Fujitsu's line of Static RAM ICs. This year's edition, however, does not include a section for SRAM modules. Both DRAM and SRAM modules are now in a Modules Data Book which you can obtain from your nearest Fujitsu Sales Office or Sales Representative. (See the Sales Information listing in this book.)

In addition to the collection of SRAM data sheets, you will find valuable information on ordering and expanded packaging descriptions, both in the Order Information section. A cross reference for SRAMs is in Appendix 4, and again in each respective product section. You will also find a new technical paper, *Fast SRAMs in Zero Wait-State Memory Intefaces*, in the Design Information section.

If you are interested in obtaining other Fujitsu product information, see the publications listing on the following pages for titles and brief descriptions of other Fujitsu product literature. To obtain a copy of any of the documents, call one of our sales offices.

FUJITSU PRODUCT PUBLICATIONS

The following is a list of the product publications available from Fujitsu Microelectronics, Inc. Call your nearest FMI Sales Office or Sales Representative to order any document(s) you need. (See the Sales Information section for phone numbers.)

MEMORY PRODUCTS

Dynamic RAM Products Data Book	Contains product data sheets for NMOS and CMOS DRAMs, including 1M and 4M devices, and MOS application-specific RAMs.
Static RAM Products Data Book	Contains product data sheets for high-speed CMOS and BiCMOS SRAMs, low-power CMOS SRAMs and application-specific SRAMs.
ECL RAM Products Data Book	Contains product data sheets for ECL and TTL bipolar ECL RAMs, BiCMOS ECL RAMs, and application-specific RAMS including self-timed RAMs (STRAMs).
Programmable Memory Products Data Book	Contains product data sheets for programmable ROMs (including registered and wide-temperature range PROMs); CMOS mask-programmable ROMS, OTP ROMs, erasable PROMs, and EEPROMs; NMOS erasable PROMs and non-volatile RAMs.
Memory Modules Data Book	Contains product data sheets for CMOS DRAM modules (including high density and low profile) and CMOS SRAM modules.
Memory Card Products Data Book	Contains product data sheets and programming information for 68-pin JEIDA and PCMCIA standard memory cards and connectors and for 38-pin memory cards.
Power Transistor Products Data Book	Contains product data sheets for RETs, Darlington arrays, and FETs.
Linear Products Data Book	Contains product data sheets for op amps, comparators, automotive audio amps, power supply controls, motor drivers, disk drivers, and converters (A/D, D/A, A/D-D/A, and F/V).
Linear Products Selector Guide	Presents an overview of linear products.
Telecommunication Devices Data Book	Contains product data sheets for bipolar prescalers and VCOs, CMOS PLLs, BiCMOS single-chip PLLs and Prescalers, CODECs, CMOS telephone ICs, and cellular mobile radio ICs.
Telecommunication Devices Selector Guide	Presents an overview of telecommunication products and piezoelectric devices.
Interface and Logic Products Selector Guide	Presents an overview of logic and interface devices.
CMOS 4-bit Microcontrollers Data Book, Vol. I	Contains product information, including the development tool for the MB8850 and MB88200 families of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Data Book, Vol. II	Contains product information, including the development tool for the MB88500 family of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Selector Guide	Presents an overview of the MB88500 (high end), MB8850 (mid-range), and MB88200 (low end) families of 4-bit microcontrollers.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC PRODUCTS

CMOS Channeled Gate Arrays Data Book and Design Evaluation Guide	Contains product information for UHB Series High Drive CMOS Gate Arrays and CG10 Series High Drive CMOS Gate Arrays.
CMOS Channelless Gate Arrays Data Book and Design Evaluation Guide	Contains product information for AU Series CMOS Series Gate Arrays and CG21 Series CMOS Gate Arrays.
ASIC CMOS Products Selector Guide	Presents an overview of CMOS channeled and channelless gate arrays and standard cell products.
BiCMOS Gate Arrays Data Book and Design Evaluation Guide	Contains product information for BC Series BiCMOS Gate Arrays and BC-H Series BiCMOS Gate Arrays.
ECL Gate Arrays Data Book and Design Evaluation Guide	Contains product information for ET Series ECL Gate Arrays, H Series ECL Gate Arrays, Ultra-High Performance ECL Gate Arrays, and VH Series ECL Gate Arrays.
ASIC Bipolar Products Selector Guide	Presents an overview of BiCMOS and ECL gate array products.

ASIC SOFTWARE

The ASIC Gallery™ (catalog)	Discusses the trend in ASICs: migration from using gates as primitives to using LSI and even VLSI macros as design elements.
The ASIC Design Environment (catalog)	Provides an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD™, BankCAD™, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.
ViewCAD User's Guide	Provides a basic understanding of Fujitsu's proprietary CAD/CAE system, ViewCAD. This book provides information necessary to design, test, simulate, and analyze circuits using Fujitsu's unit cell libraries for AU, UHB, CG10, CG21, and CG31 CMOS technologies.
ViewCAD Installation Guide	Explains how to install Fujitsu's proprietary CAD/CAE system, ViewCAD.
CMOS ASIC Reference Manual for Valid	Provides a basic understanding of the Valid System on the Sun platform as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries for AU and UHB CMOS technologies.
FAME User's Guide	Provides a basic understanding of the Fujitsu ASIC Management Environment (FAME) software as it interfaces with third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
FAME Reference Manual	Provides installation and directory information for the Fujitsu ASIC Management Environment (FAME) software, which uses third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
Synopsys User's Guide	Provides a basic understanding of the Synopsys® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC SOFTWARE (Continued)

Verilog-XL User's Guide	Provides a basic understanding of the Verilog-XL® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.
Future Publications	
For Fujitsu Microelectronics, Inc.:	
Master Product Guide/Catalog (1991)	Presents an overview of the entire range of products offered by Fujitsu Microelectronics.
For Memory Products:	
Hybrid Products (1991)	Presents Fujitsu's hybrid products and discusses thick- and thin-film capabilities.
For ASIC Software:	
ASIC Design Environment Data Book (1991)	Provides detailed information about the ASIC Design Methodology at Fujitsu. It contains an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD, BankCAD, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.
ASICOpen™ Catalog (1991)	Provides information about the Fujitsu ASIC Design framework. It explains the design processes between two third-party tools, Synopsys and Verilog-XL, and Fujitsu's proprietary tools, ViewCAD and BankCAD.

Contents and Alphanumeric Product List

SRAM Products

Contents and Alphanumeric Product List (Continued)

SRAM Products

Contents and Alphanumeric Product List (Continued)

SRAM Products

Contents and Alphanumeric Product List (Continued)

SRAM PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

Page	Title
xi	Fujitsu's Static RAM Products

Fujitsu's Static RAM Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs.

The static RAM product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

This data book includes product information on the following SRAM products:

High-speed CMOS SRAMs

Fujitsu's high-speed CMOS SRAMs offer the advantages of low power dissipation, low cost, and high performance. Features include TTL compatibility and a separate chip-select pin that simplifies multipackage systems design.

High-speed BiCMOS SRAMs

Advanced BiCMOS technology adds ultra-fast access times to CMOS low power dissipation in Fujitsu's new family of static RAMs. Most devices feature an automatic power-down mode and are generally available in small outline packages with J-leads (SOJ).

Low-speed CMOS SRAMs

Our low-power CMOS SRAMs are ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. The memories use asynchronous circuitry and may be maintained in any state for an indefinite period of time.

Application-Specific CMOS SRAMs

To address the system needs of cache memories, Fujitsu's application-specific memory line includes both cache TAG RAM and high-speed static RAM, as well as dual-port RAMs for multiprocessor systems.

Extended Temperature Range SRAMs

For applications requiring devices that operate in the industrial temperature range, Fujitsu offers a selection of TTL-compatible CMOS SRAMs. These devices are specified for operation in the range from –40°C to +85°C. The designator "–X", following the standard part number, identifies SRAMs that operate in the extended temperature range. See specific data sheets for full product specification.

High-Speed CMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity (Organization)	Package Options
1–3	*High-Speed CMOS SRAMs Product Cross Reference*			
1–5	MB81C67–35	35	16384 bits	20-pin Plastic DIP
	–45	45	(16384 x 1)	20-pin Ceramic DIP
	–55	55		20-pad Ceramic LCC
1–17	MB81C68A–25	25	16384 bits	20-pin Plastic DIP, ZIP
	–30	30	(4096 x 4)	20-pin Ceramic CERDIP
	–35	35		20-pad Ceramic LCC
1–29	MB81C69A–25	25	16384 bits	20-pin Plastic DIP
	–30	30	(4096 x 4)	20-pin Ceramic CERDIP
	–35	35		20-pad Ceramic LCC
1–41	MB81C71A–25	25	65536 bits	22-pin Plastic DIP
	–30	30	(65536 x 1)	24-pin Plastic SOJ
	–35	35		22-pad Ceramic LCC
1–53	MB81C74–25	25	65536 bits	22-pin Plastic DIP
	–30	30	(16384 x 4)	22-pad Ceramic LCC
	–35	35		
1–63	MB81C75–25	25	65536 bits	24-pin Plastic DIP, SOJ
	–30	30	(16384 x 4 /OE)	24-pin Plastic LCC
	–35	35		
1–75	MB81C78A–35	35	65536 bits	28-pin Plastic DIP, SOP, SOJ
	–45	45	(8192 x 8)	32-pad Ceramic LCC
1–91	MB81C79A–35	35	73728 bits	28-pin Plastic DIP, SOP, SOJ
	–45	45	(8192 x 9)	32-pad Ceramic LCC
1–107	MB81C81A–25	25	262144 bits	24-pin Plastic DIP, SOJ
	–35	35	(262144 x 1)	
1–117	MB81C84A–25	25	262144 bits	24-pin Plastic DIP, SOJ
	–35	35	(65536 x 4)	
1–127	MB8289–25	25	294912 bits	32-pin Plastic DIP, SOP
	–35	35	(32768 x 9)	
1–137	MB8298–25	25	262144 bits	28-pin Plastic DIP, SOP, SOJ
	–35	35	(32768 x 8)	
1–147	MB8299–25	25	294912 bits	32-pin Plastic DIP, SOP, SOJ
	–35	35	(32768 x 9)	

High-Speed CMOS SRAMs Product Cross Reference

64K Static RAMs

Vendors	Fujitsu Part Numbers				
	MB81C71A (64K x 1)	**MB81C74 (16K x 4)**	**MB81C75 (16K x 4/OE)**	**MB81C78A (8K x 8/OE)**	**M81C79A (8K x 9/OE)**
Cypress	CY7C187	CY7C164	CY7C166	CY7C185	CY7C182
Hitachi	HM6287	HM6288	HM6289		
IDT	IDT7187	IDT7188	IDT7198	IDT7164	IDT7169
Micron	MT5C6401	MT5C6404	MT5C6405	MT5C6408	
Mitsubishi	M5M5187A	M5M5188A	M5M5189A	M5M5178	M5M5179
Motorola	MCM6287	MCM6288	MCM6290	MCM6264	MCM6265
NEC	µPD4361	µPD4362	µPD4363		
Performance	P4C187	P4C188	P4C198	P4C164	P4C163
Samsung	KM6165	KM6465	KM6466	KM6865	
Sharp	LH5261	LH5262	LH5267	LH5165 and 5164	
Sony	CXK5164	CXK5464	CXK5465	CXK5863	CXK5971
Toshiba	TC5562	TC55416	TC55417	TC5588	TC5589

256K Static RAMs

Vendors	Fujitsu Part Numbers			
	MB81C81A (256K x 1)	**MB81C84A (64K x 4)**	**MB8298 (32K x 8/OE)**	**MB8299 (32K x 9/OE)**
Cypress	CY7C197	CY7C194	CY7C199	
Hitachi	HM6207	HM6208	HM62832	
IDT	IDT71257	IDT71258	IDT71256	IDT71259
Micron	MT5C2561	MT5C2564	MT5C2568	
Mitsubishi	M5M5257	M5M5258		
Motorola	MCM6207	MCM6208	MCM6206	MCM6205
NEC		µPD43254		
Performance	P4C1257	P4C1258	P4C1256	
Samsung	KM61257	KM64257	KM68257	
Sharp	LH52251	LH52252 and 52255	LH52254 and 52258	
Sony	CXK51256	CXK54256	CXK58258	CX58289
Toshiba		TC55464	TC55328	TC55329

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FUJITSU

DATA SHEET

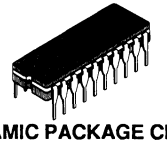
MB81C67-35/-45/-55
CMOS 16K-BIT HIGH-SPEED SRAM

16K Words x 1 Bit High-Speed CMOS Static Random Access Memory

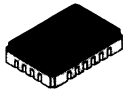
The Fujitsu MB81C67 is a 16,384 words x 1 bit static random access memory fabricated with a CMOS silicon gate process. All pins are TTL compatible and a single +5 V power supply is required.

A chip select ($\overline{CS}$) pin permits the selection of an individual package when outputs are OR-tied, and automatically powers down the device. The MB81C67 offers low power dissipation, low cost, and high performance.

- Organization: 16,384 words x 1 bit
- Static operation: no clocks or refresh required
- Access time: 35 ns max. (MB81C67-35)
  45 ns max. (MB81C67-45)
  55 ns max. (MB81C67-55)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 20-pin Plastic Package:
  DIP MB81C67-xxP
- Standard 20-pad Ceramic Package:
  LCC MB81C67-xxTV
- Standard 20-pin Ceramic Package:
  CERDIP MB81C67-xxZ
- Pin compatible with Fujitsu MB8167A



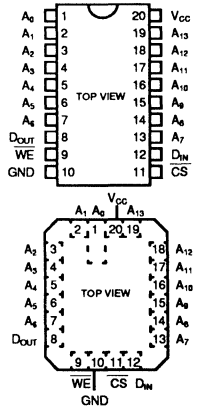
CERAMIC PACKAGE CERDIP
DIP-20C-C03



CERAMIC PACKAGE
LCC-20C-F01

PLASTIC PACKAGE
DIP-20P-M01

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any pin with respect to GND		V_{OUT}	−0.5 to +7.0	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.2	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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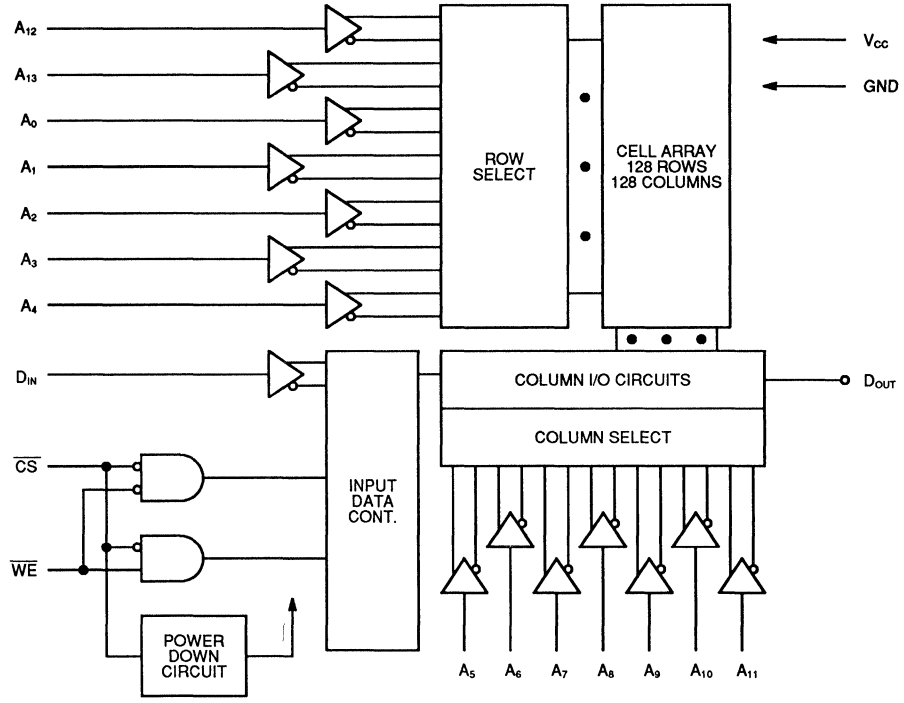
Fig. 1 — MB81C67 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A= 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	–3.0*		0.8	V
Input High Voltage	V_{IL}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*–3.0V Min. for pulse width less than 20ns. (V_{IL} Min=–1.0V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	–2.0		2.0	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, V_{OUT}=0V to V_{CC}	I_{LO}	–2.0		2.0	µA
Active Supply Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA V_{IN}=V_{IL} or V_{IH}	I_{CC1}		25	40	mA
Operating Supply Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA Cycle=Min, C_L=0pF	I_{CC2}		35	60	mA
Standby Supply Current	$\overline{CS}$≥V_{CC}–0.2V V_{IN}≥V_{CC} –0.2V or V_{IN}≤0.2V	I_{SB1}		2	15	mA
Standby Supply Current	$\overline{CS}$=V_{IH},	I_{SB2}		15	25	mA
Output Low Voltage	I_{OL}=16mA	V_{OL}			0.4	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4			V

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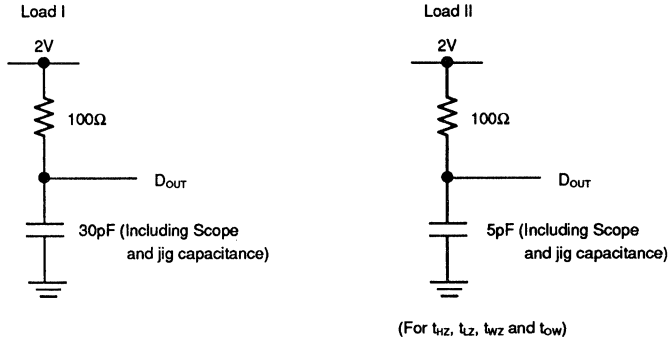
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns
Timing Measurement Reference Levels:	Input : 1.5V Output : 1.5V

Output Load: Fig.2



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

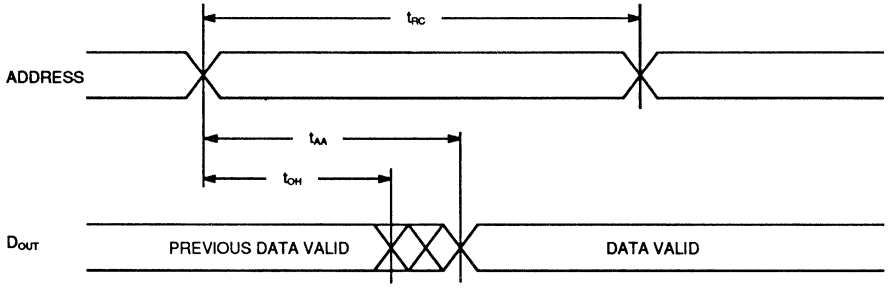
READ CYCLE *1

Parameter	Symbol	MB81C67–35		MB81C67–45		MB81C67–55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time *2	t_{RC}	35		45		55		ns
Address Access Time *3	t_{AA}		35		45		55	ns
Chip Select Access Time *4	t_{ACS}		35		45		55	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low–Z *5	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High–Z *5	t_{HZ}	0	25	0	25	0	30	ns
Chip Selection to Power Up	t_{PU}	0		0		0		ns
Chip Deselection to Power Down	t_{PD}		30		40		50	ns

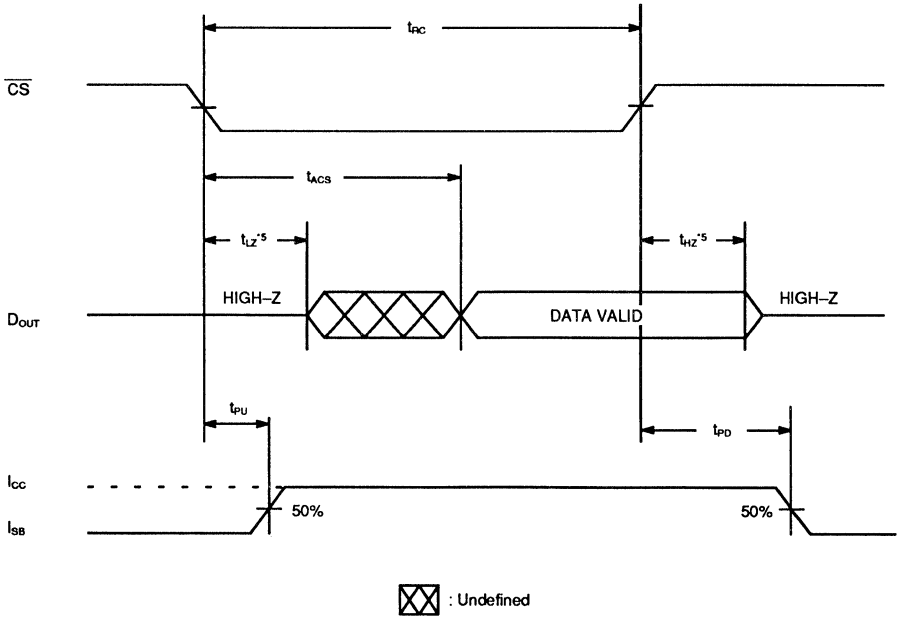
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS}=V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM *1*2

READ CYCLE : ADDRESS CONTROLLED *3



READ CYCLE : $\overline{CS}$ CONTROLLED *4



: Undefined

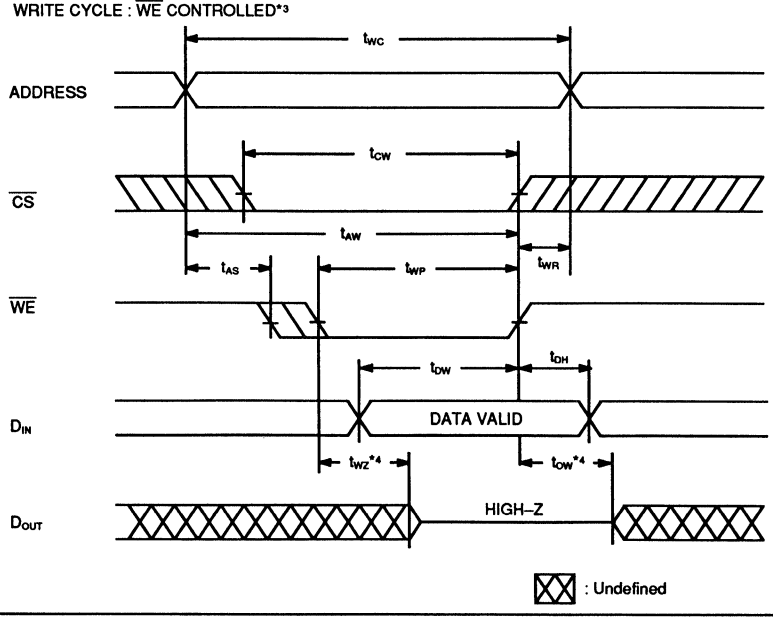
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle are determined from the last address transition to the first address transition of the next address.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

1

WRITE CYCLE *1*2

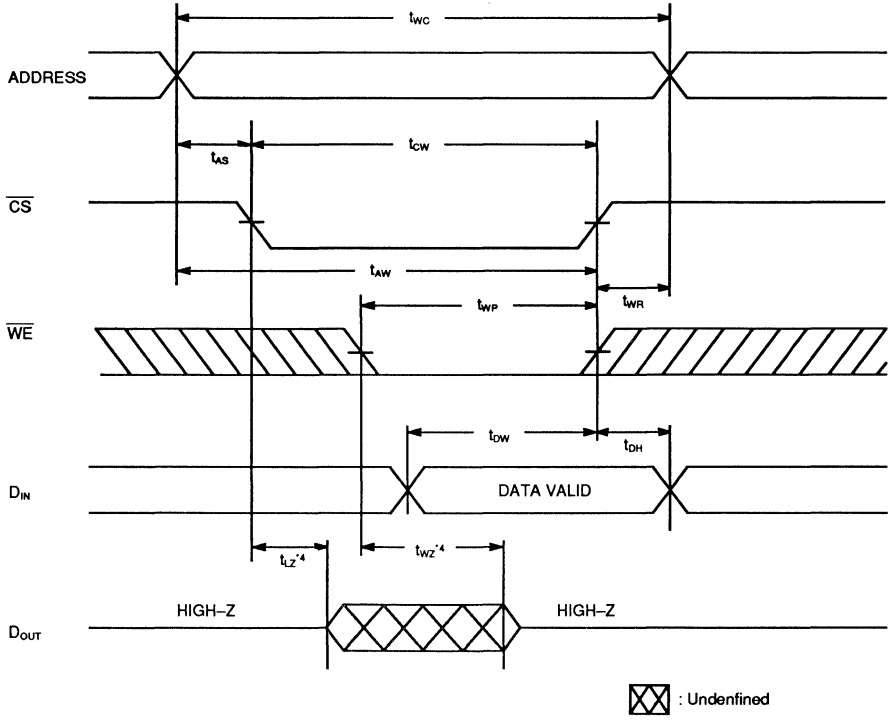
Parameter	Symbol	MB81C67–35		MB81C67–45		MB81C67–55		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	35		45		55		ns
Chip Selection to End of Write	t_{CW}	30		35		50		ns
Address Valid to End of Write	t_{AW}	30		35		50		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Valid to End of Write	t_{DW}	20		20		25		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in High–Z *4	t_{WZ}	0	25	0	25	0	30	ns
Output Active from End of Write *4	t_{OW}	0	25	0	25	0	30	ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transition to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transistion.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle are determined from the last address transistion to the first address transition of next address.
*4 Transition is measured at the point of ±500mV from steady state voltage.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

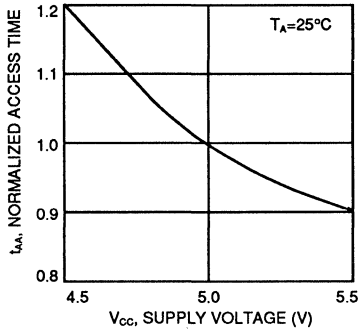


Fig. 4 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

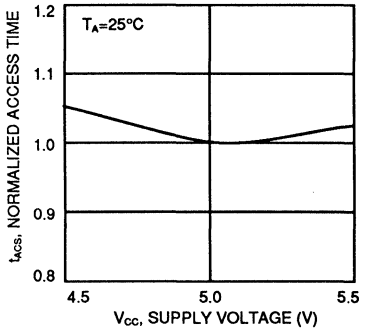


Fig. 5 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

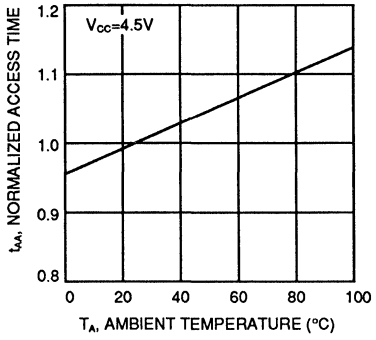


Fig. 6 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

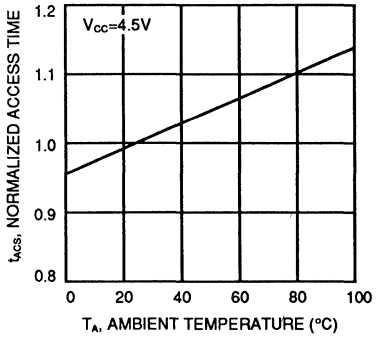


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

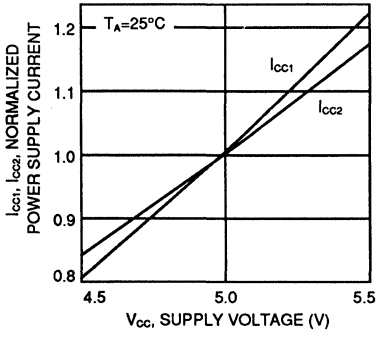


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

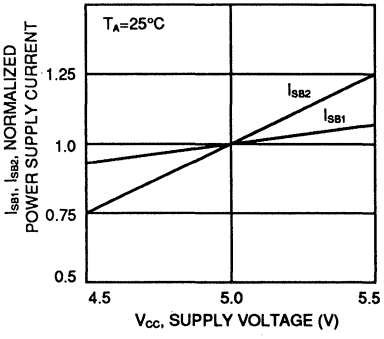


Fig. 9 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

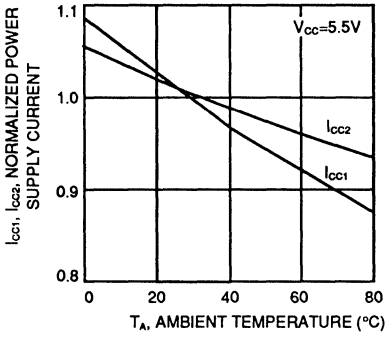


Fig. 10 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

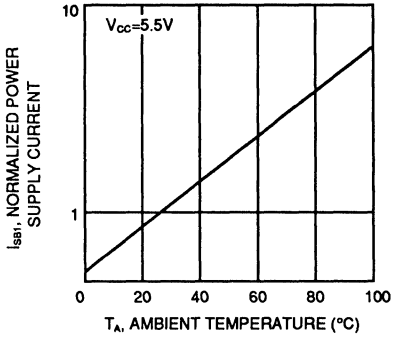


Fig. 11 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

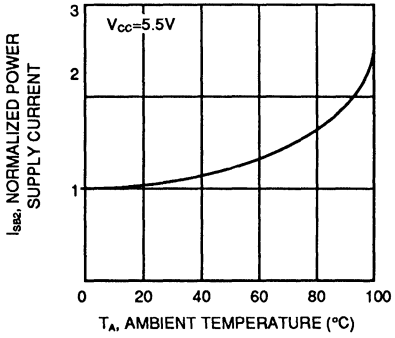


Fig. 12 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

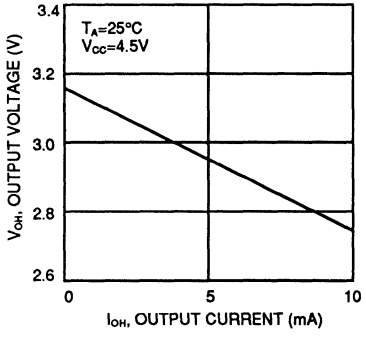


Fig. 13 – OUTPUT VOLTAGE vs. OUTPUT CURRENT

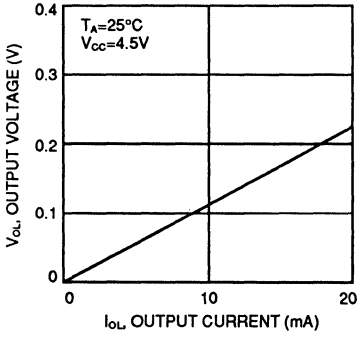


Fig. 14 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

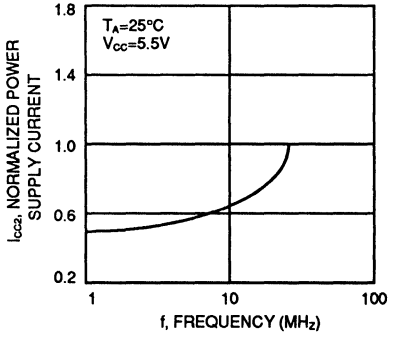


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Fig. 15– NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

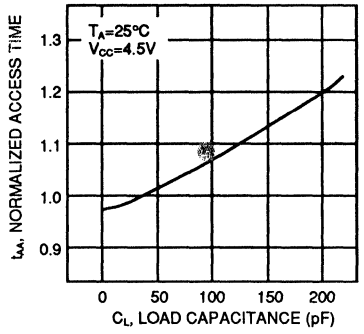
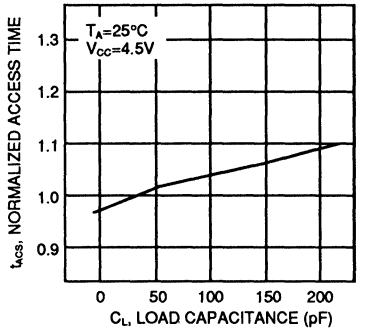


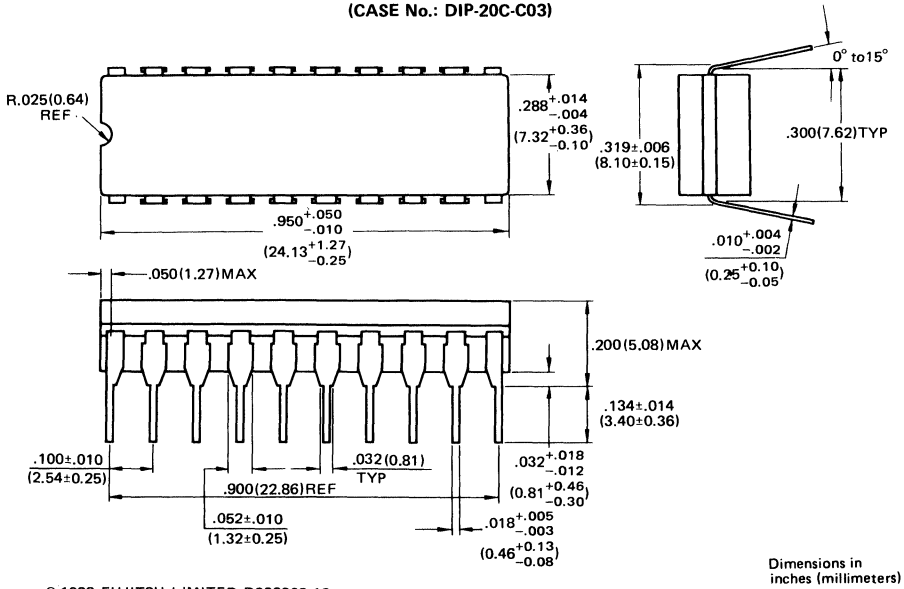
Fig. 16– NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: CZ)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

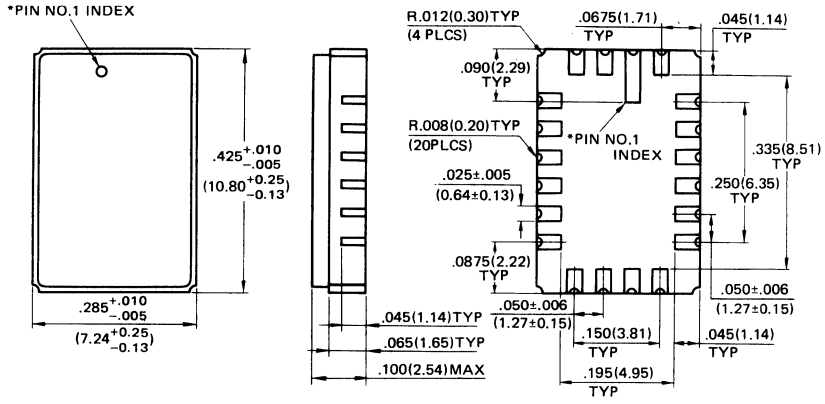


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: TV)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)

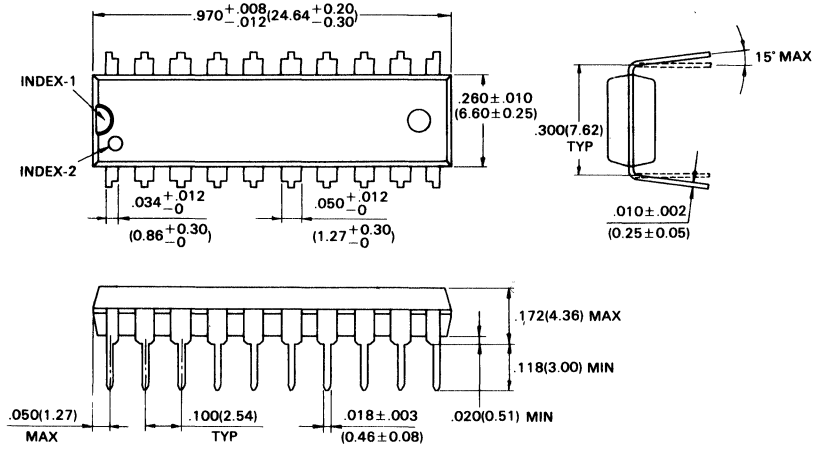
* Shape of PIN NO. 1 INDEX: Subject to change without notice.

PACKAGE DIMENSIONS

(Suffix: P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M01)



Dimensions in
inches (millimeters)

April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C68A-25/-30/-35
CMOS 16K-BIT HIGH-SPEED SRAM

4K Words x 4 Bits Static Random Access Memory with Super High-Speed and Automatic Power Down

The Fujitsu MB81C68A is a 4,096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design by permiting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

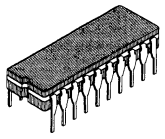
The MB81C68A offers low power dissipation, low cost, and high performance.

- Organization: 4,096 words x 4 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB81C68A-25)
  $t_{AA} = t_{ACS}$ = 30 ns max. (MB81C68A-30)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB81C68A-35)
- Low power consumption: 385 mW max. (Active)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 20-pin Plastic Package:
  DIP MB81C68A-xxP
  ZIP MB81C68A-xxPSZ
- Standard 20-pin Ceramic Package:
  CERDIP MB81C68A-xxZ

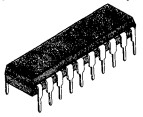
Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

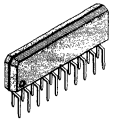
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CERAMIC PACKAGE CERDIP
(DIP-20C-C03)



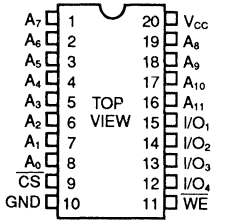
PLASTIC PACKAGE
(DIP-20P-M01)



PLASTIC PACKAGE
(ZIP-20P-M01)

LCC: See page 12

PIN ASSIGNMENT



LCC: See page 12

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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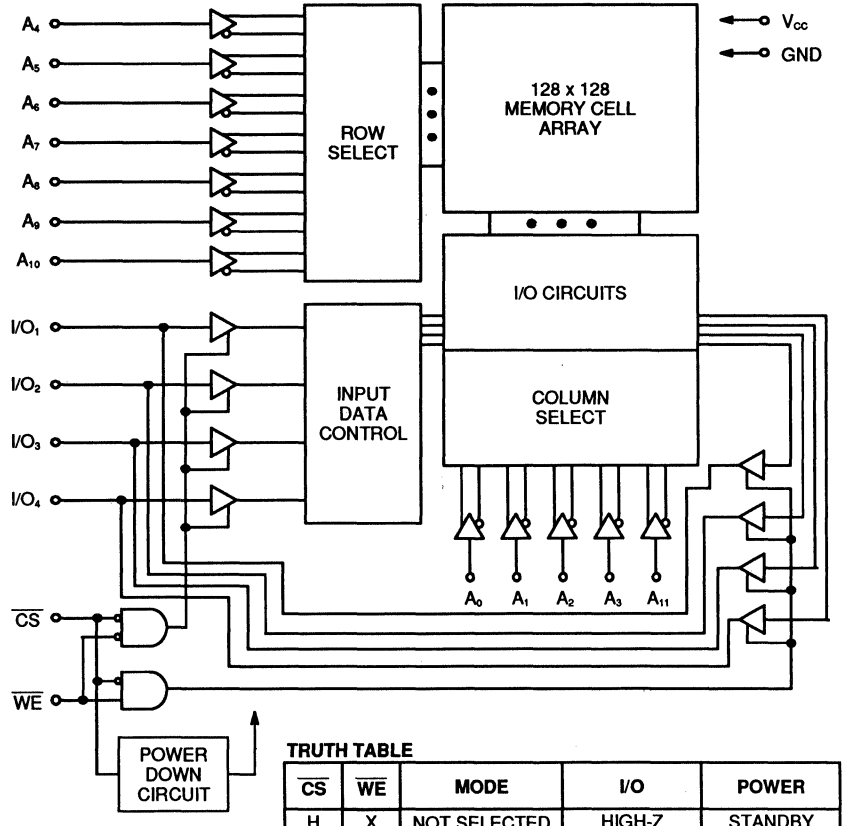
Fig. 1 – MB81C68A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

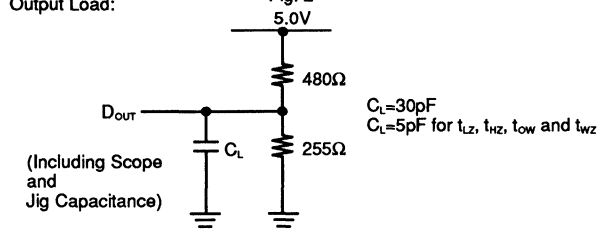
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}	I_{LO}	−10		10	µA
Active (DC) Supply Current	I_{OUT}=0mA $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$=V_{IL} I_{OUT}=0mA, Cycle=Min	I_{CC2}		40	70	mA
Standby Supply Current	$\overline{CS}$=V_{CC}−0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC} −0.2V	I_{SB1}		0.5	15	mA
Standby Supply Current	$\overline{CS}$=V_{IH}	I_{SB2}		10	25	mA
Input Low Voltage		V_{IL}	−2.0*		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V
Output Low Voltage	I_{OL}=8mA	V_{OL}			0.4	V
Output High Voltage	I_{OH}=−4mA	V_{OH}	2.4			V

Note: * −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

AC TEST CONDITION

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input : 1.5V Output : 1.5V
Output Load:	Fig. 2



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

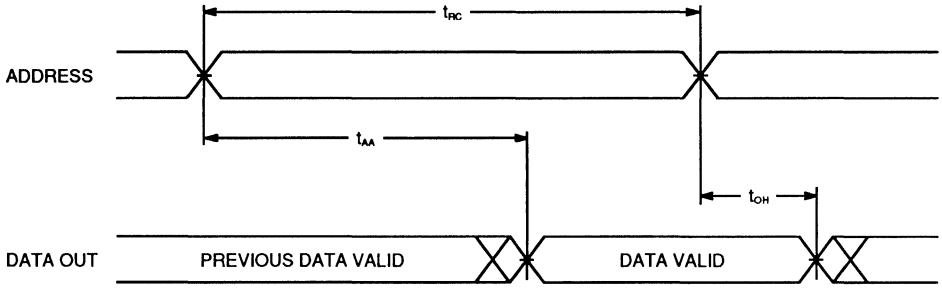
READ CYCLE*1

Parameter	Symbol	MB81C68A-25		MB81C68A-30		MB81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time*2	t_{AA}		25		30		35	ns
Chip Select Access Time*3	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*4	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*4	t_{HZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

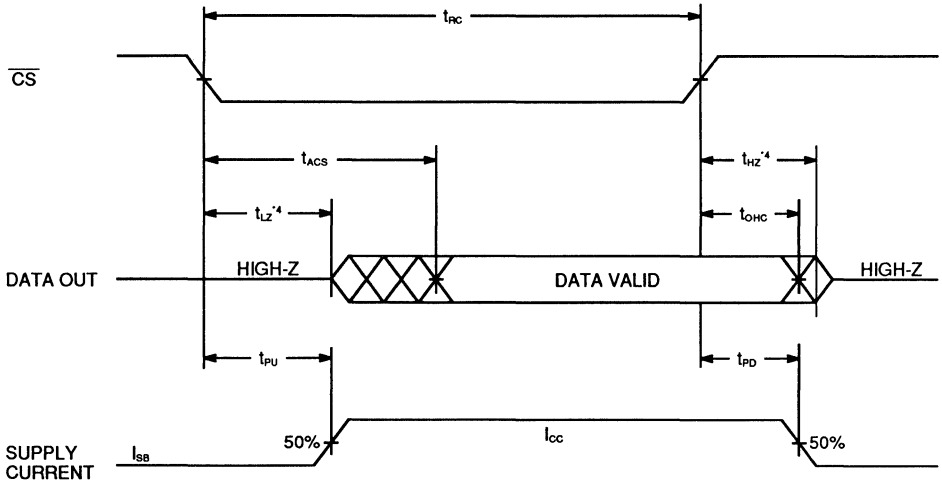
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2



READ CYCLE : $\overline{CS}$ CONTROLLED*3



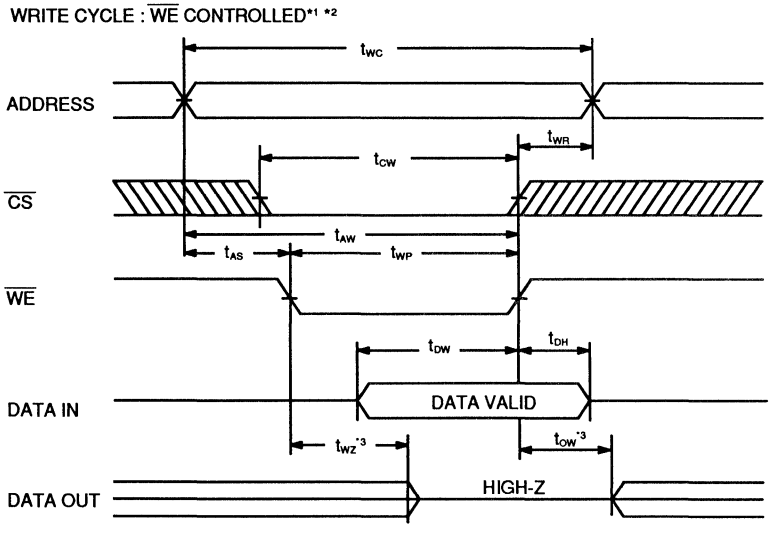
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500mV from steady state voltage.

1

WRITE CYCLE*1 *2

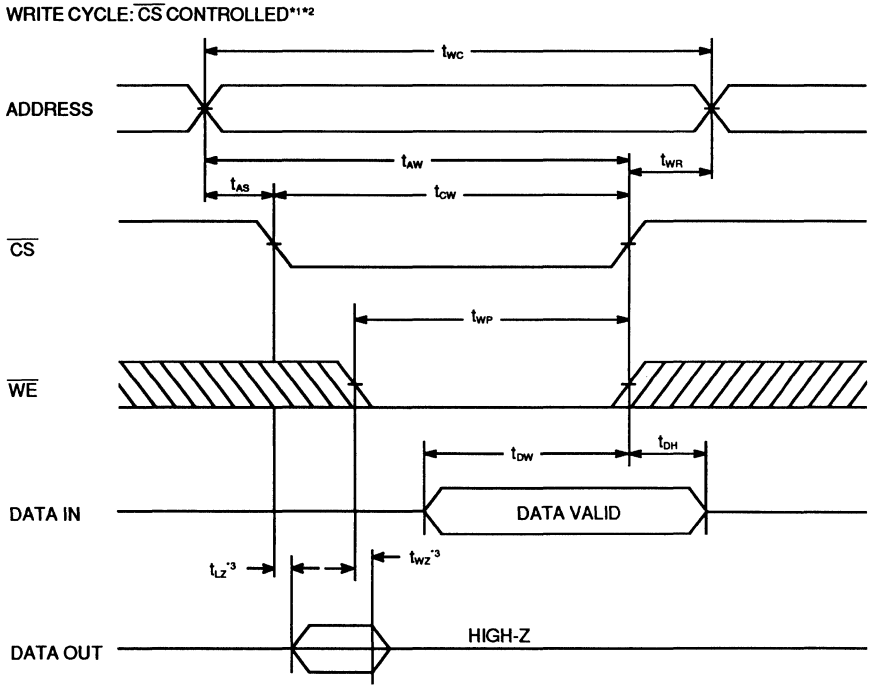
Parameter	Symbol	MB81C68A-25		MB81C68A-30		MB81C68A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*3	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*3	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500mV from steady state voltage.

WRITE CYCLE TIMING DIAGRAM



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
*3 Transition is specified at the point of ±500mV from steady state voltage.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

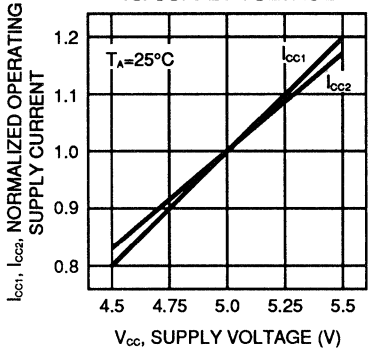


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

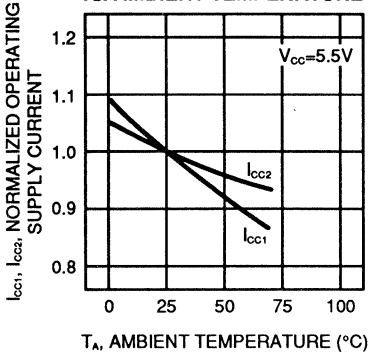


Fig. 5 STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

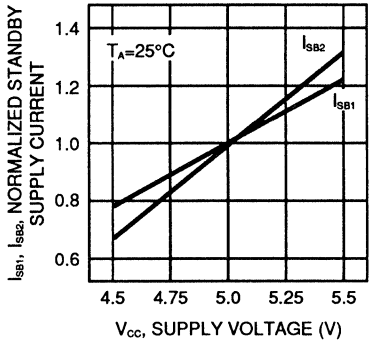


Fig. 6 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

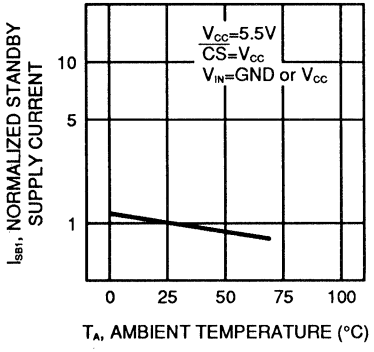


Fig. 7 STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

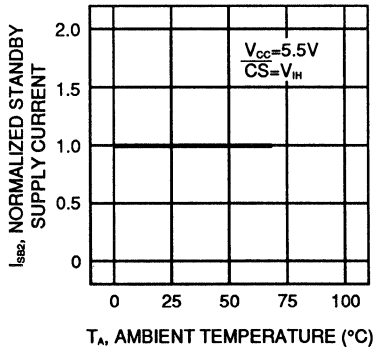
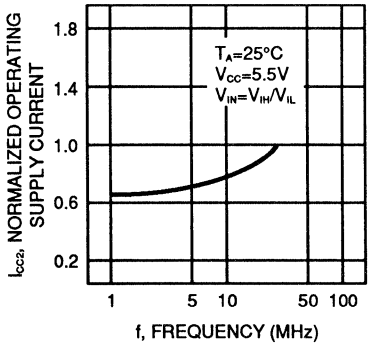


Fig. 8 OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES

Fig. 9 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

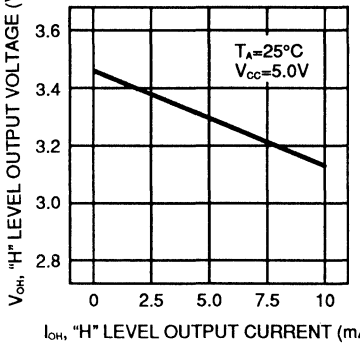


Fig. 10 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

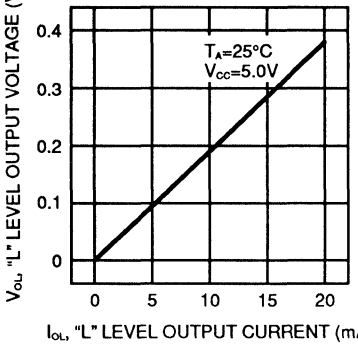


Fig. 11 ACCESS TIME vs. SUPPLY VOLTAGE

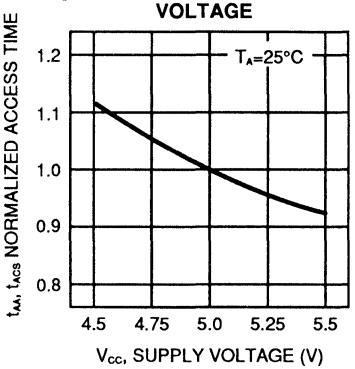


Fig. 12 ACCESS TIME vs. AMBIENT TEMPERATURE

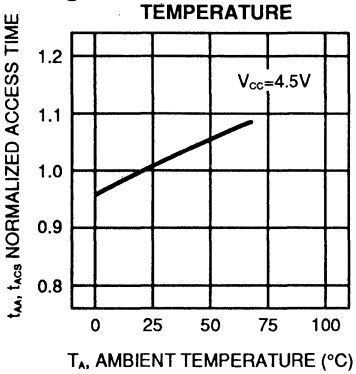
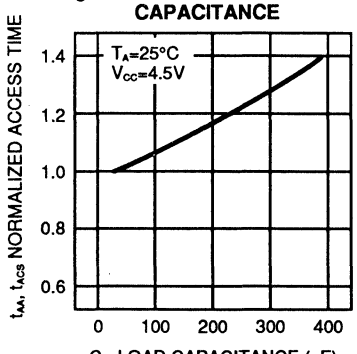


Fig. 13 ACCESS TIME vs. LOAD CAPACITANCE

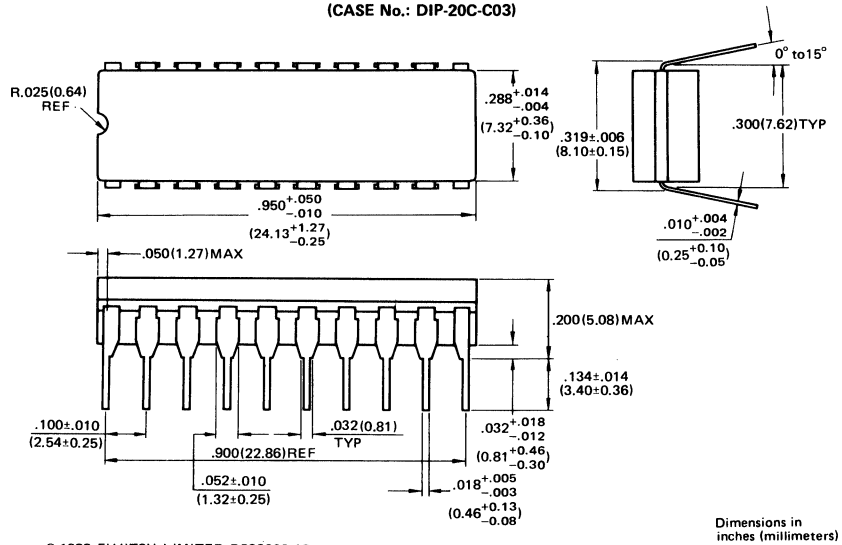


1

PACKAGE DIMENSIONS

(Suffix: –Z)

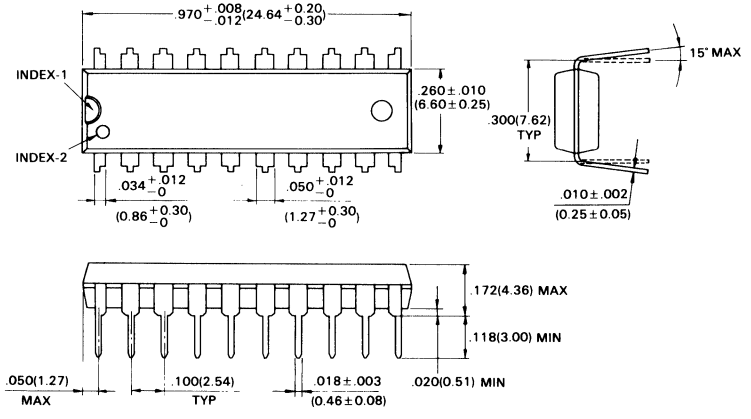
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in
inches (millimeters)

(Suffix: –P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-20P-M01)



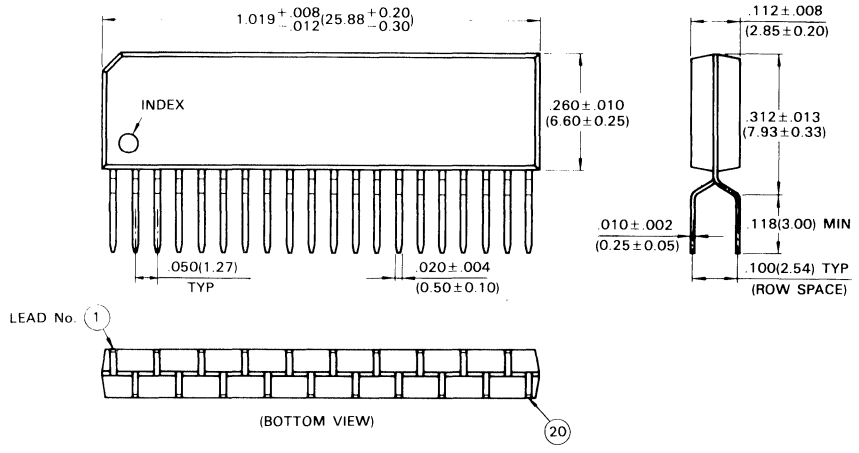
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

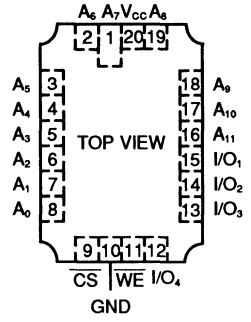
(Case No. : ZIP-20P-M01)

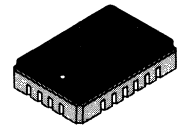


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

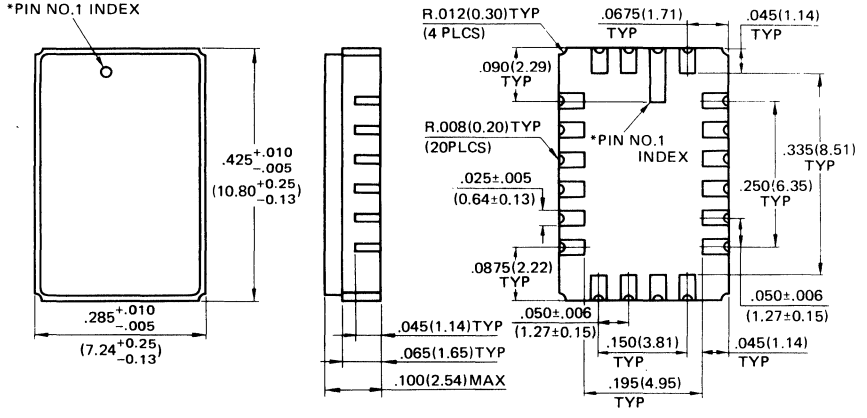
(Suffix: –TV)





CERAMIC PACKAGE LCC
(LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C69A-25/-30/-35
CMOS 16K-BIT HIGH-SPEED SRAM

1

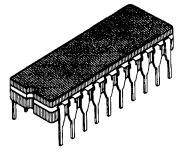
4K Words x 4 Bits Static Random Access Memory with Super High-Speed

The Fujitsu MB81C69A is a 4,096 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry. All pins are TTL compatible and a single +5 V power supply is required.

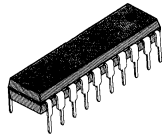
A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design by permiting the selection of an individual package when outputs are OR-tied.

The MB81C69A offers low power dissipation, low cost, and high performance.

- Organization: 4,096 words x 4 bits
- Static operation: no clocks or timing strobe required
- Access time: t_{AA} = 25 ns max, t_{ACS} = 15 ns max. (MB81C69A-25)
  t_{AA} = 30 ns max, t_{ACS} = 18 ns max. (MB81C69A-30)
  t_{AA} = 35 ns max, t_{ACS} = 20 ns max. (MB81C69A-35)
- Low power consumption: 385 mW max. (Active)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion
- Electrostatic protection for all inputs and outputs
- Standard 20-pin Plastic Package:
  DIP MB81C69A-xxP
- Standard 20-pad Ceramic Package:
  LCC MB81C69A-xxTV
- Standard 20-pin Ceramic Package:
  CERDIP MB81C69A-xxZ



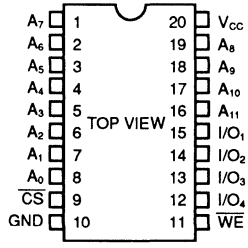
CERAMIC PACKAGE CERDIP
(DIP-20C-C03)



PLASTIC PACKAGE
(DIP-20P-M01)

LCC: See page 11

PIN ASSIGNMENT



LCC: See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

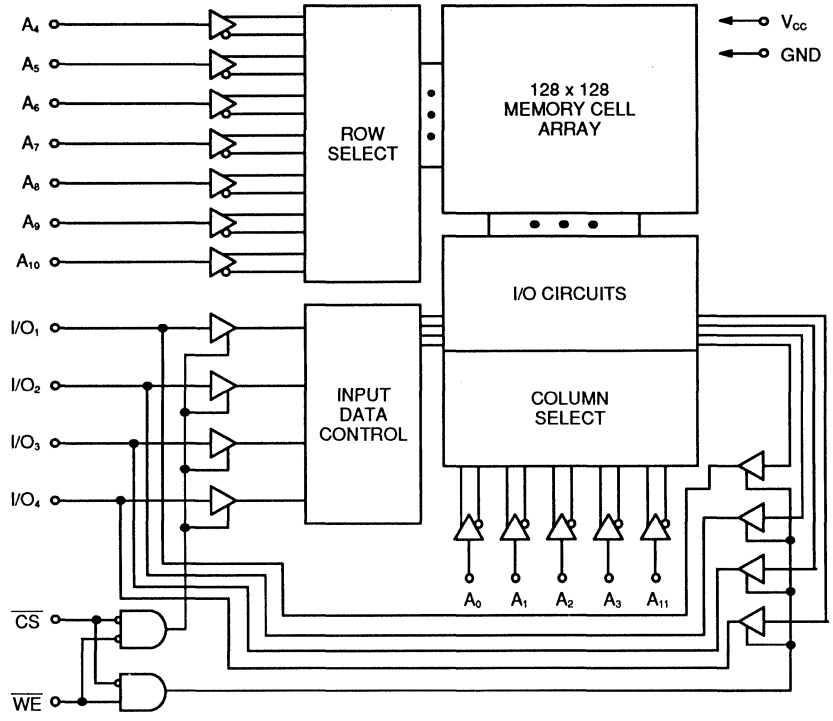
Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{out}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB81C69A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	NOT SELECTED	HIGH-Z
L	L	WRITE	D_{IN}
L	H	READ	D_{OUT}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}		5	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}	I_{LO}	−10		10	µA
Active Supply Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA V_{IN}=V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating Supply Current	$\overline{CS}$=V_{IL} I_{OUT}=0mA, Cycle=Min	I_{CC2}		40	70	mA
Input Low Voltage		V_{IL}	−2.0*		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V
Output Low Voltage	I_{OL}=8mA	V_{OL}			0.4	V
Output High Voltage	I_{OH}=−4mA	V_{OH}	2.4			V

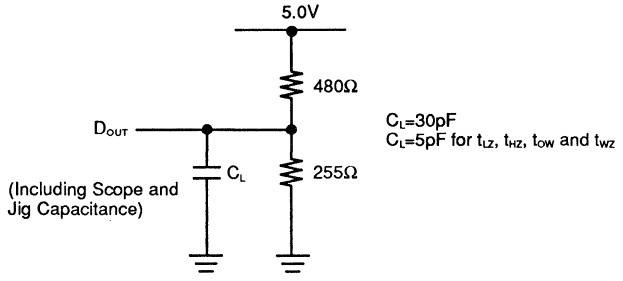
Note: * −2.0V Min. for pulse width less than 20ns. (V_{IL} Min.=−0.5V at DC level)

1

AC TEST CONDITION

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input : 1.5V Output : 1.5V
Output Load:	

Fig. 2



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

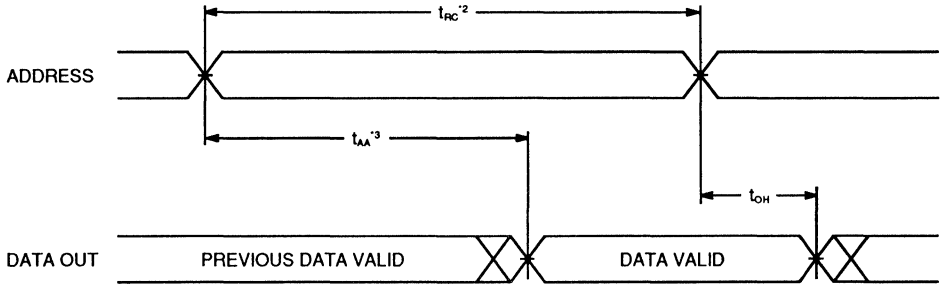
READ CYCLE*1

Parameter	Symbol	MB81C69A-25		MB81C69A-30		MB81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4	t_{ACS}		15		18		20	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Output Hold from $\overline{CS}$	t_{OHC}	0		0		0		ns
Chip Selection to Output in Low-Z*5	t_{LZ}	0		0		0		ns
Chip Deselection to Output in High-Z*5	t_{HZ}		10		13		15	ns

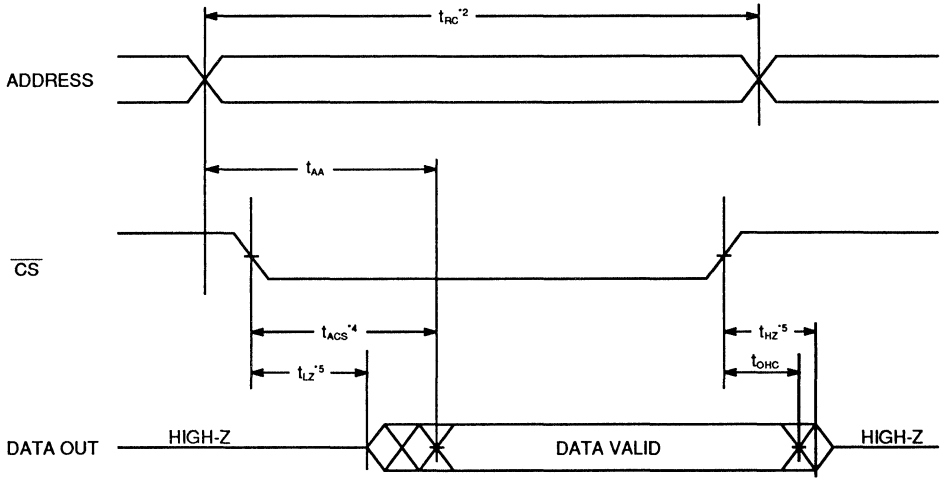
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}=V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state Voltage with Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED



READ CYCLE : $\overline{CS}$ CONTROLLED*3



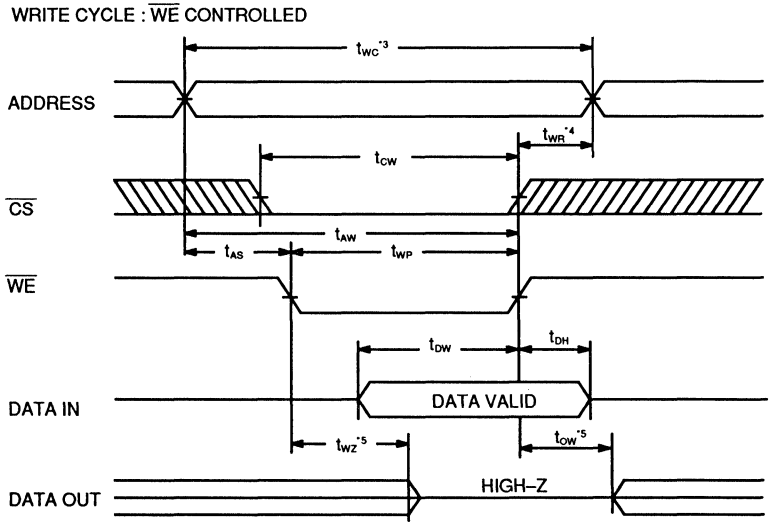
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

1

WRITE CYCLE*1 *2

Parameter	Symbol	MB81C69A-25		MB81C69A-30		MB81C69A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Setup Time	t_{DW}	13		15		15		ns
Write Recovery Time*4	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	0		0		0		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}		10		13		15	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5		5		5		ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

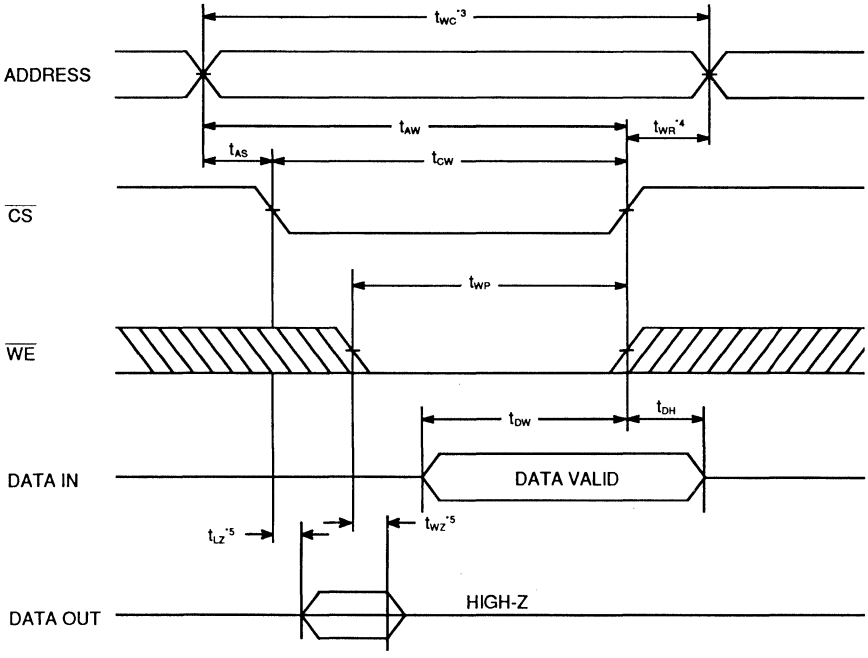
*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is specified at the point of ±500mV from steady state voltage with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED*1*2



Note: *1 If $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is specified at the point of +500mV from steady state voltage with Load II in Fig. 2.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

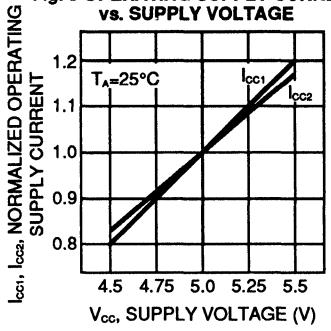


Fig. 4 OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

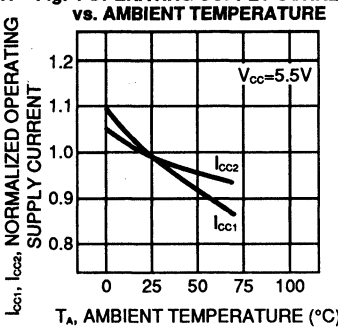


Fig. 5 OPERATING SUPPLY CURRENT vs. FREQUENCY

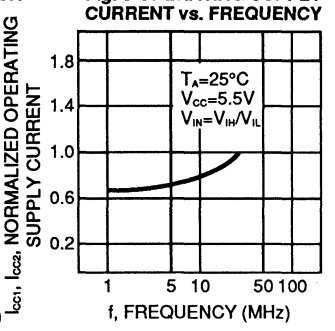


Fig. 6 "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

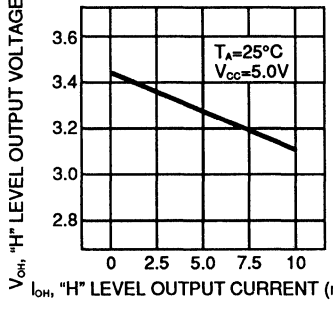


Fig. 7 "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

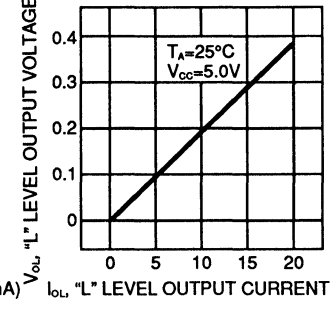


Fig. 8 ACCESS TIME vs. SUPPLY VOLTAGE

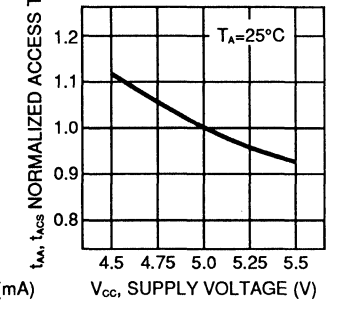


Fig. 9 ACCESS TIME vs. AMBIENT TEMPERATURE

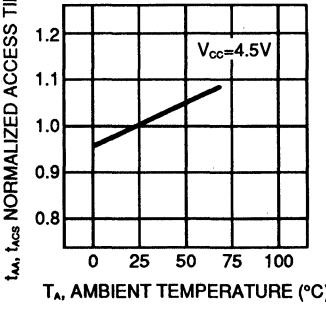
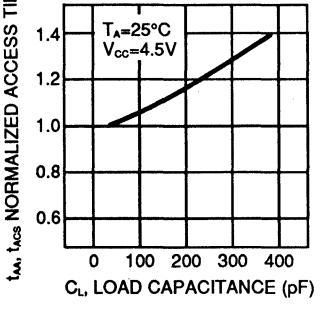


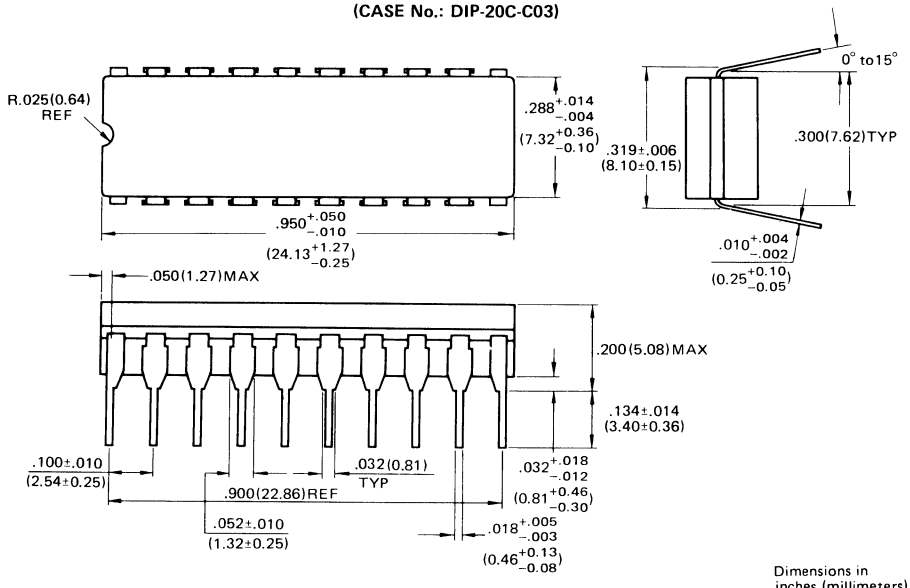
Fig. 10 ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: Z)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



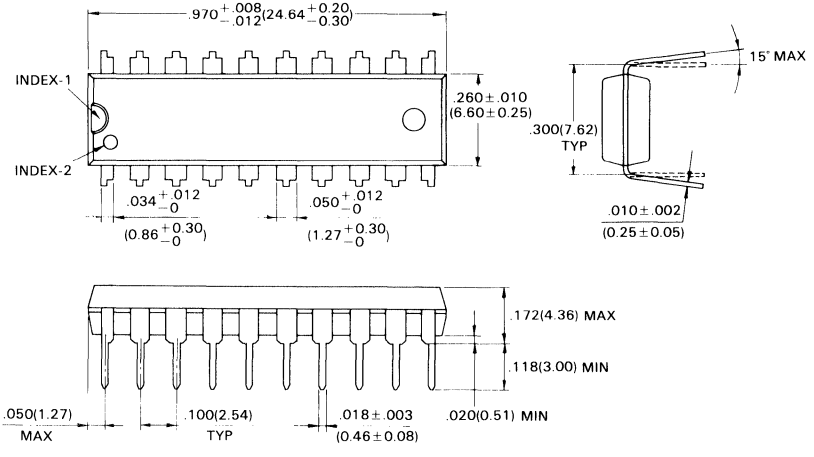
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

PLASTIC DIP (Suffix: P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

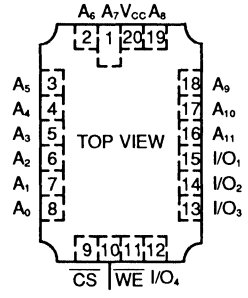
(Case No. : DIP-20P-M01)

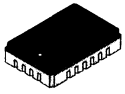


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

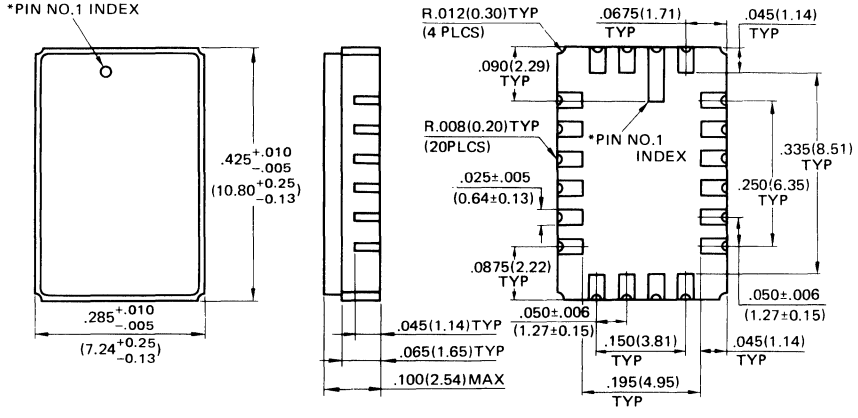
CERAMIC LCC (Suffix: TV)





CERAMIC PACKAGE (LCC-20C-F01)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER (CASE No.: LCC-20C-F01)



Dimension in inches (millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

March 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C71A-25/-30/-35
CMOS 64K-BIT HIGH-SPEED SRAM

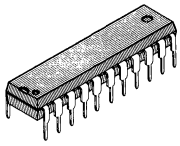
1

64K Words x 1 Bit High-Speed CMOS Static Random Access Memory

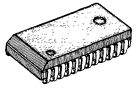
The Fujitsu MB81C71A is a 65,536 words x 1 bit static random access memory fabricated with a CMOS technology. It uses fully static circuitry throughout and, therefore, requires no clocks or refreshes to operate.

The MB81C71A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. It is compatible with TTL logic, and requires a single +5 V supply.

- Organization: 65,536 words x 1 bit
- Static operation: no clocks or refresh required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB81C71A-25)
  $t_{AA} = t_{ACS} = 30$ ns max. (MB81C71A-30)
  $t_{AA} = t_{ACS} = 35$ ns max. (MB81C71A-35)
- Single +5 V power supply ±10% tolerance
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 22-pin Plastic Package:
  DIP MB81C71A-xxP
- Standard 24-pin Plastic Package:
  SOJ MB81C71A-xxPJ
- Standard 22-pad Ceramic Package:
  LCC (metal seal) MB81C71A-xxCV



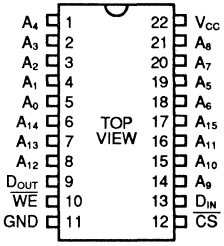
PLASTIC PACKAGE
DIP-22P-M04

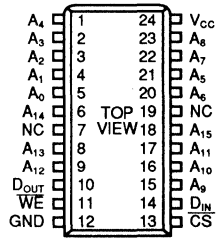


PLASTIC PACKAGE
LCC-24P-M02

LCC : See page 12.

PIN ASSIGNMENT





LCC : See 12 page.

Absolute Maximum Ratings (See Note)

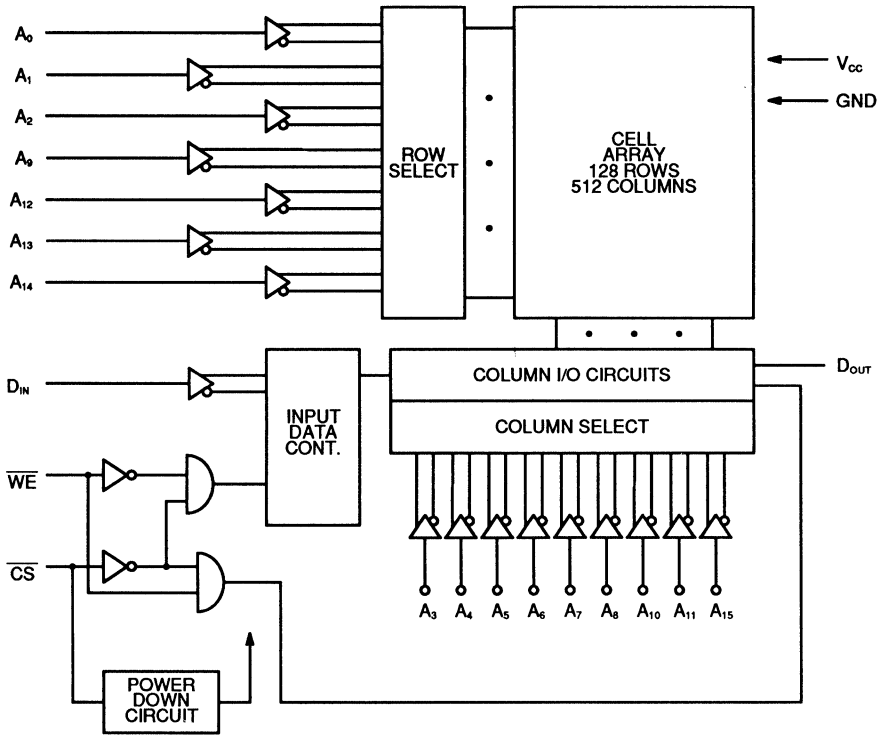
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C71A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance (V_{IN}=0V)	C_{IN}		7	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current	V_{IN}=0V to V_{CC} V_{CC}=Max.	I_{LI}	–10		10	µA
Output Leakage Current	$\overline{CS}$=V_{IH}, V_{OUT}=0V to 4.5V V_{CC}=Max.	I_{LO}	–10		10	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, V_{CC}=Max. D_{OUT}=Open, Cycle=Min.	I_{CC}		50	80	mA
Standby Current	V_{CC}=Min. to Max. $\overline{CS}$≥V_{CC} –0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC} –0.2V	I_{SB1}		1	10	mA
Standby Current	V_{CC}=Min. to Max. $\overline{CS}$=V_{IH}	I_{SB2}		10	20	mA
Input Low Voltage		V_{IL}	–2.0*		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V
Output Low Voltage	I_{OL}=16mA	V_{OL}			0.45	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4			V
Peak Power on Current**	V_{CC}=0V to V_{CC} Min. $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.	I_{PO}			30	mA

* –2.0V Min, for pulse width less than 20 ns. (V_{IL} Min=–0.5V at DC Level)

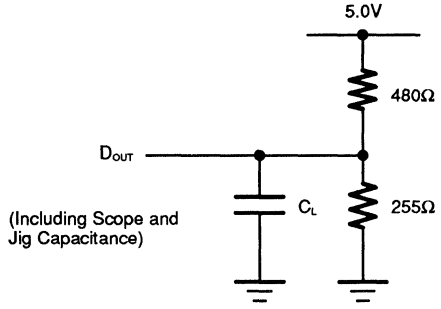
** A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

1

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise And Fall Times: 5ns
- Timing Measurement Reference Levels: Input : 1.5V
  Output : 1.5V

- Output Load:



Load I: C_L=30pF
Load II: C_L=5pF for t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

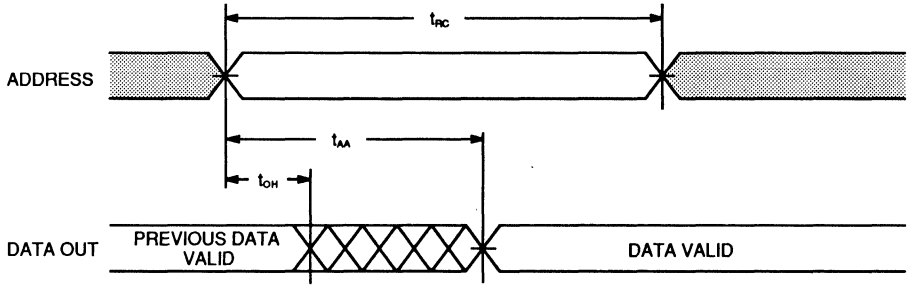
READ CYCLE*1

Parameter	Symbol	MB81C71A-25		MB81C71A-30		MB81C71A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time*2	t_{RC}	25		30		35		ns
Address Access Time*3	t_{AA}		25		30		35	ns
Chip Select Access Time*4*5	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Output in Low-Z*6	t_{LZ}	5		5		5		ns
Chip Deselection to Output in High-Z*6	t_{HZ}	0	10	0	13	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down time	t_{PD}		20		25		30	ns

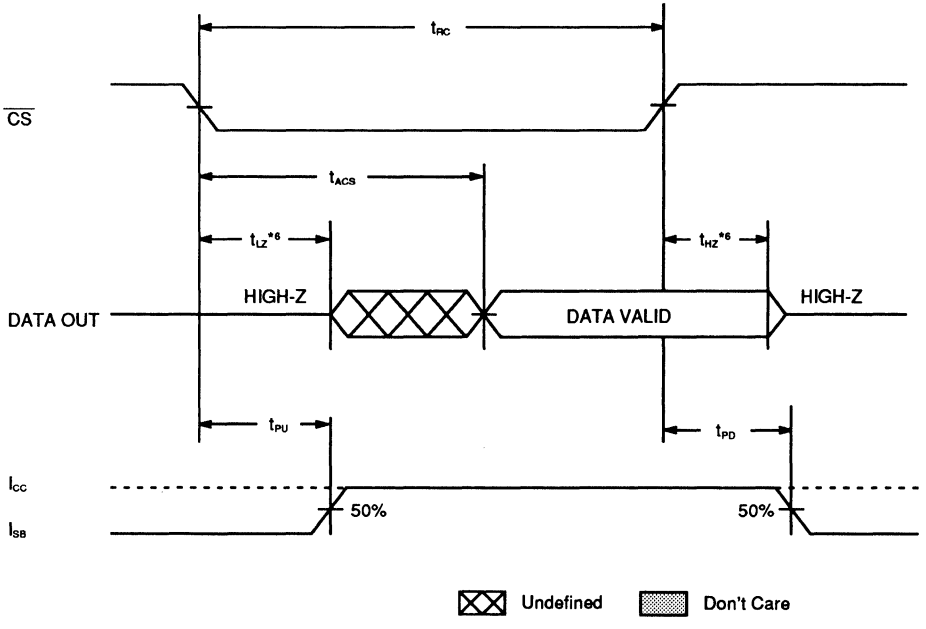
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM *1*2

READ CYCLE : ADDRESS CONTROLLED*3



READ CYCLE : $\overline{CS}$ CONTROLLED*4*5



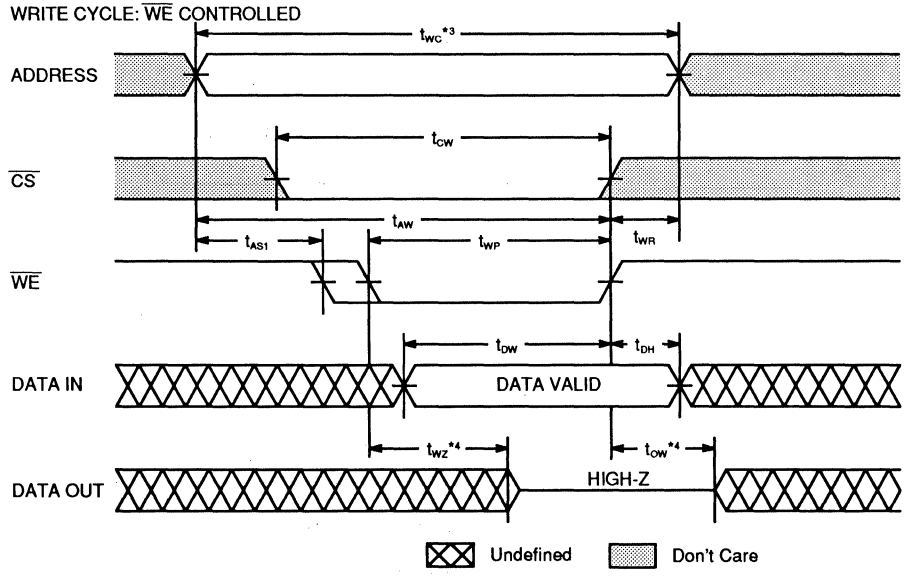
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Chip deselection for a finite time is less than t_{RC} prior to selection.
*6 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE*1*2

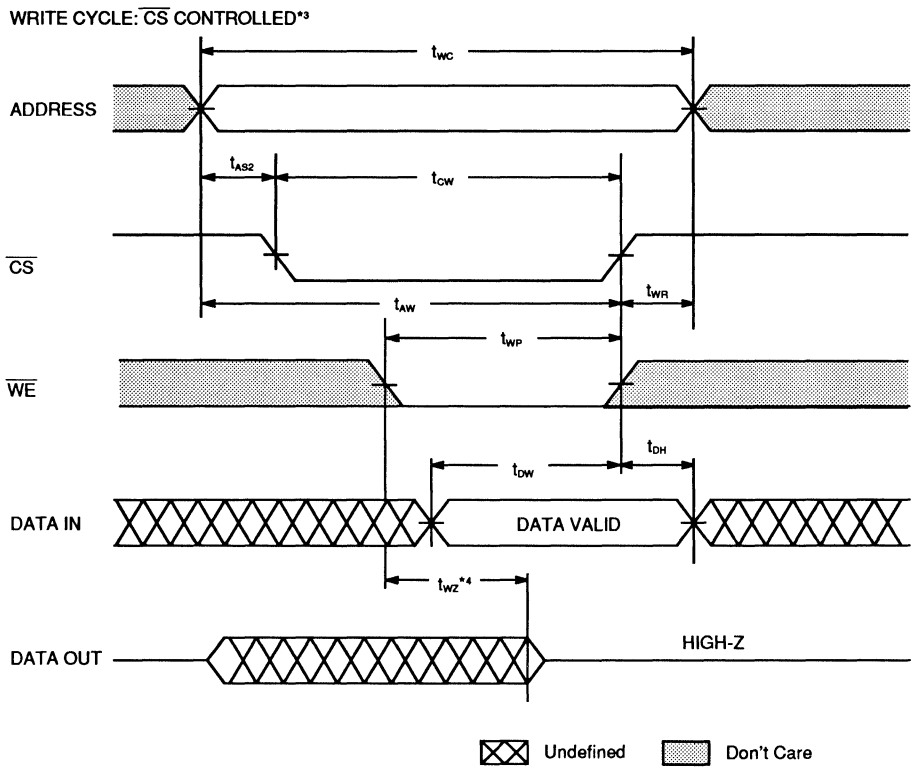
Parameter	Symbol	MB81C71A-25		MB81C71A-30		MB81C71A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	25		30		35		ns
Chip Selection to End of Write	t_{CW}	20		25		30		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Address Setup Time	t_{AS1}	0		0		0		ns
Address Setup Time	t_{AS2}	0		0		0		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Data Valid to End of Write	t_{DW}	15		18		20		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Data Hold Time	t_{DH}	2		2		2		ns
Write Enable to Output in High-Z*4	t_{WZ}	0	10	0	13	0	15	ns
Output Active from End of Write*4	t_{OW}	0		0		0		ns

WRITE CYCLE TIMING DIAGRAM*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

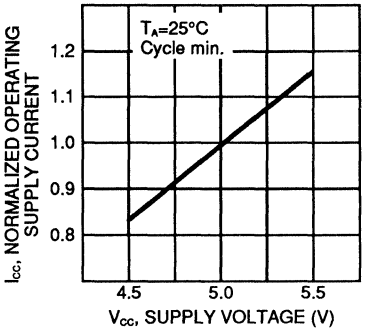


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

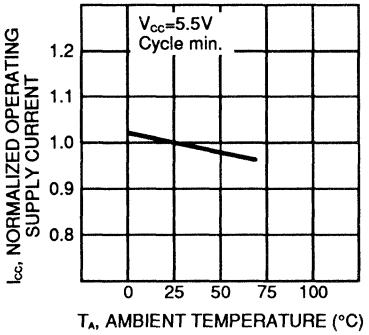


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

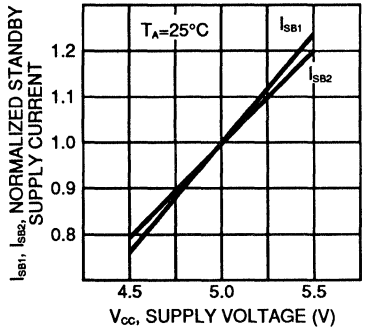


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

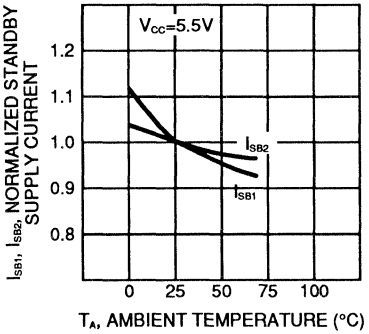
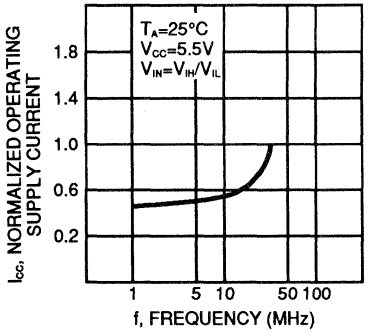


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

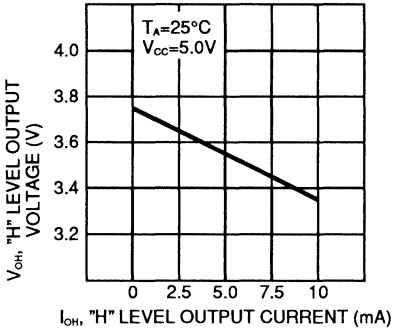


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

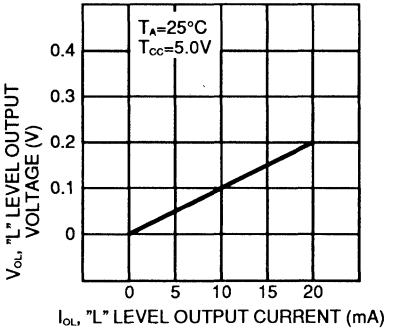


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

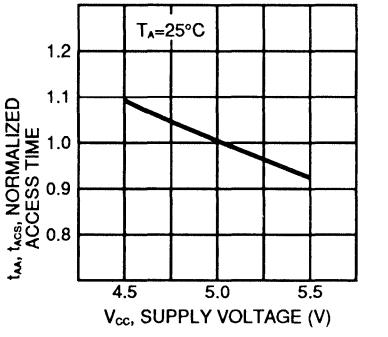


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

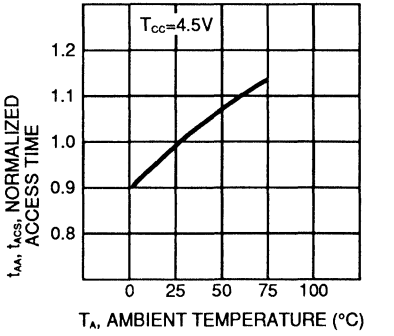
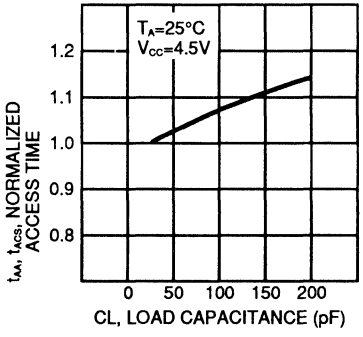


Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE

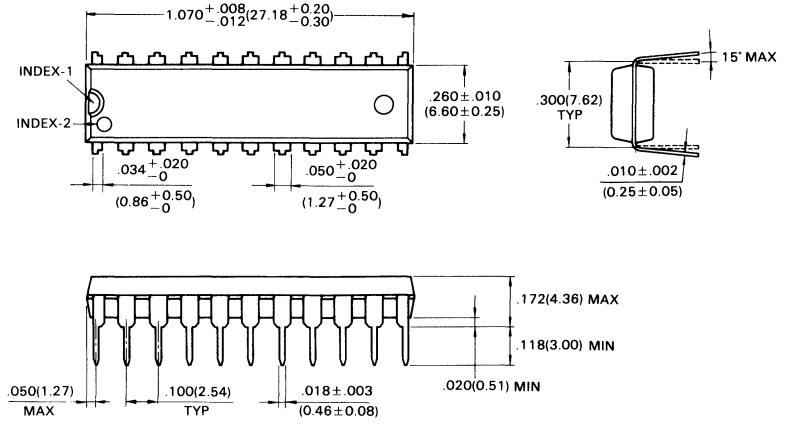


PACKAGE DIMENSIONS

(Suffix: –P)

22-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-22P-M04)

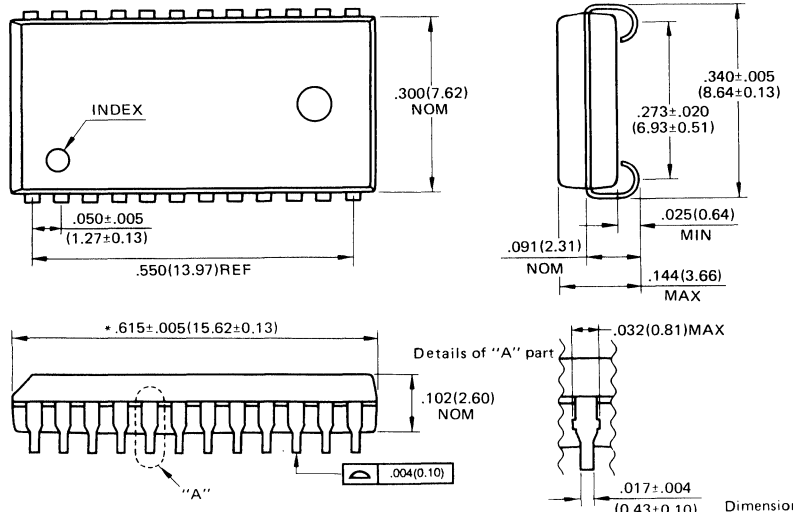


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: –PJ)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

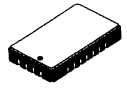


* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

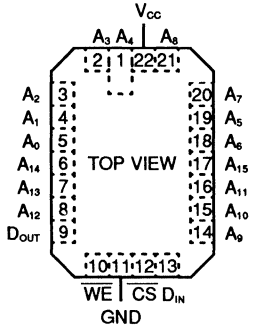
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

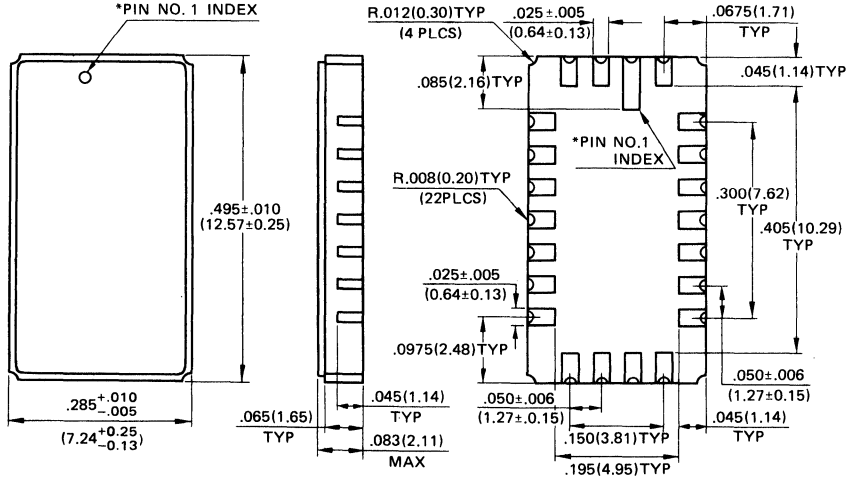
(Suffix: –CV)



CERAMIC PACKAGE
LCC-22C-A01



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

March 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C74-25/-30/-35
CMOS 64K-BIT HIGH-SPEED SRAM

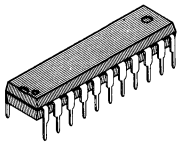
1

16K Words x 4 Bits High-Speed CMOS Static Random Access Memory

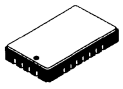
The Fujitsu MB81C74 is a 16,384 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and it may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB81C74 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 16,384 words x 4 bits
- Access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB81C74-25)
  $t_{AA} = t_{ACS}$ = 30 ns max. (MB81C74-30)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB81C74-35)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 22-pin Plastic Package:
  DIP MB81C74-xxP
- Standard 22-pad Ceramic Package:
  LCC (metal seal) MB81C74-xxCV

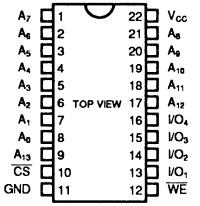


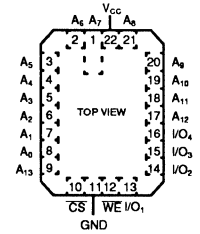
PLASTIC PACKAGE
DIP-22P-M04



CERAMIC PACKAGE
LCC-22C-A01

PIN ASSIGNMENT





Absolute Maximum Ratings (See Note)

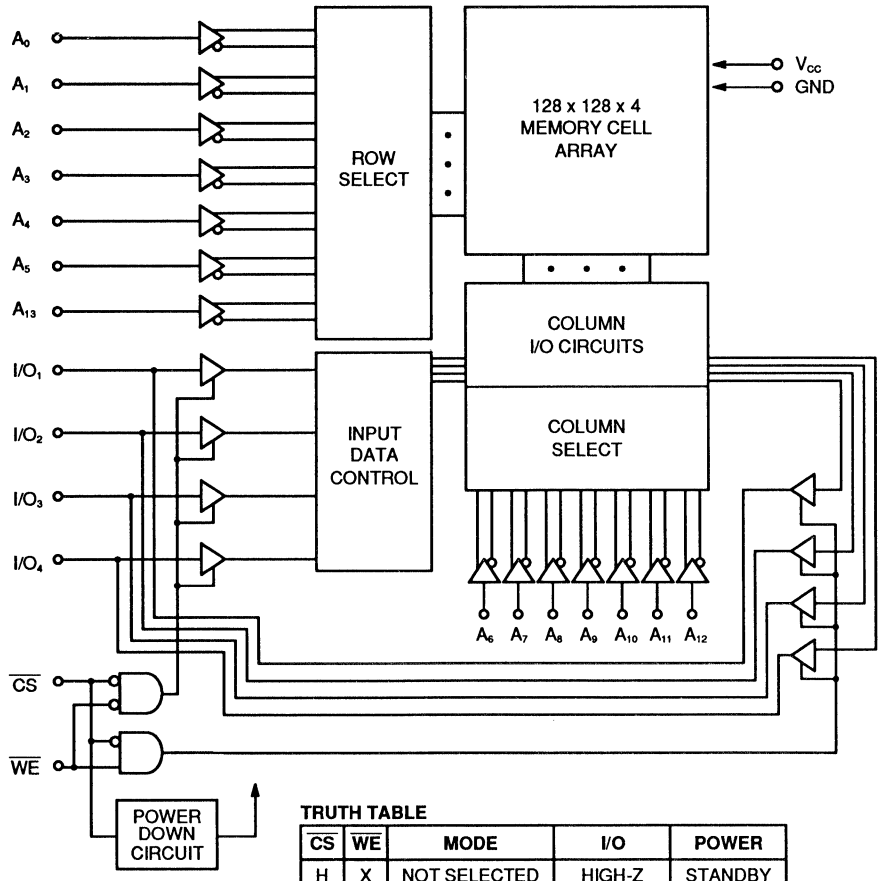
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C74 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

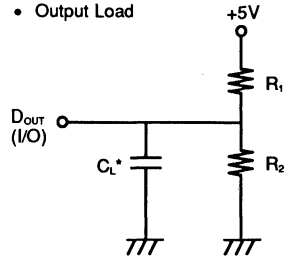
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		10	mA	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$
	I_{SB2}		20	mA	$\overline{CS}=V_{IH}$
Active Supply Current	I_{CC1}		60	mA	I_{OUT}=0mA, $\overline{CS}=V_{IL}$ $V_{IN}=V_{IL}$ or V_{IH}
Operating Supply Current	I_{CC2}		100	mA	Cycle=Min., I_{OUT}=0mA, $\overline{CS}=V_{IL}$
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}
Output Leakage Current	$I_{LI/O}$	−10	10	µA	$\overline{CS}=V_{IH}$, $V_{I/O}$=0V to V_{CC}
Input Low Voltage	V_{IL}	−2.0*1	0.8	V	
Input High Voltage	V_{IH}	2.2	6.0	V	
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA

Note: All voltages are referenced to GND
*1 −2.0V Min. for pulse width less than 20ns. (V_{IL} min. =−0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : 1.5V
  Output : 1.5V

* Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, and t_{WHZ}
Load II	480Ω	255Ω	5pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}

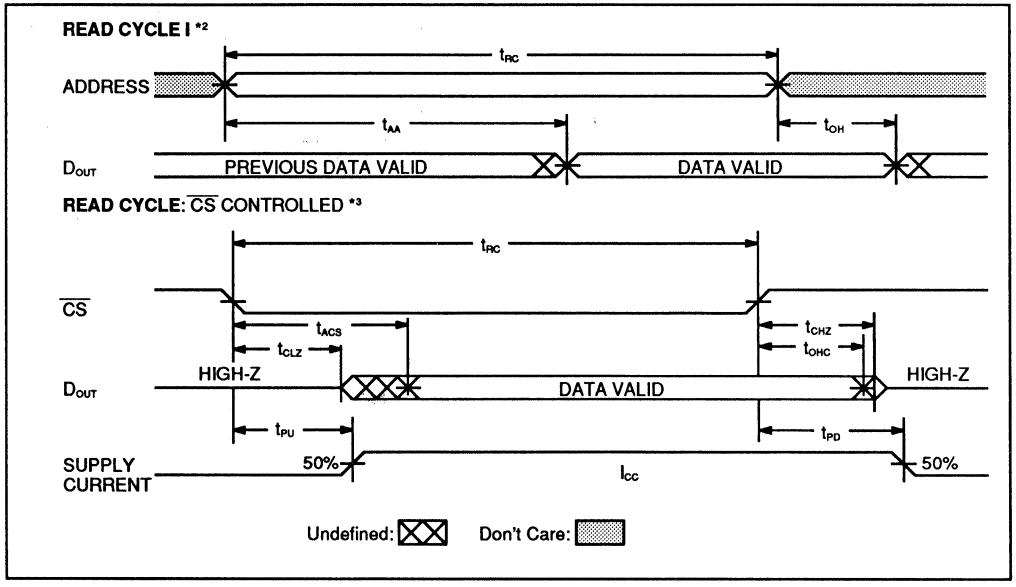
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB81C74-25		MB81C74-30		MB81C74-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time*2	t_{AA}		25		30		35	ns
$\overline{CS}$ Access Time*3	t_{ACS}		25		30		35	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		3		ns
Chip Selection to Output Low-Z*4*5	t_{CLZ}	5		5		5		ns
Chip Deselection to Output High-Z*4*5	t_{CHZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

READ CYCLE TIMING DIAGRAM *1

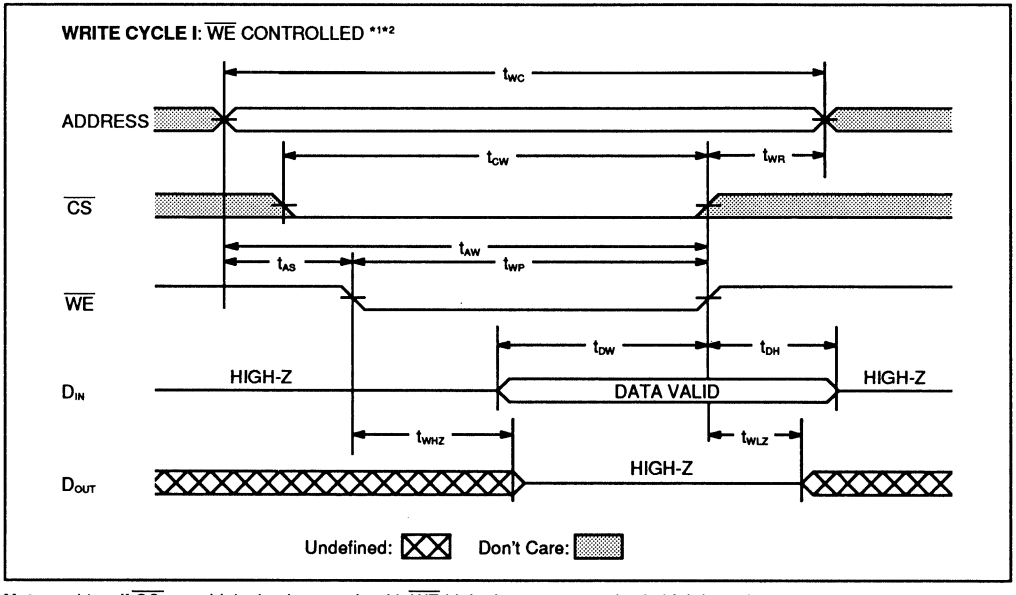


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE *1

Parameter	Symbol	MB81C74-25		MB81C74-30		MB81C74-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		30		35		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Chip Select to End of Write	t_{CW}	20		25		30		ns
Data Valid to End of Write	t_{DW}	13		15		17		ns
Data Hold Time	t_{DH}	2		2		2		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Output High-Z from $\overline{WE}$*3*4	t_{WHZ}	0		0		0		ns
Output Low-Z from $\overline{WE}$*3*4	t_{WLZ}		10		13		15	ns

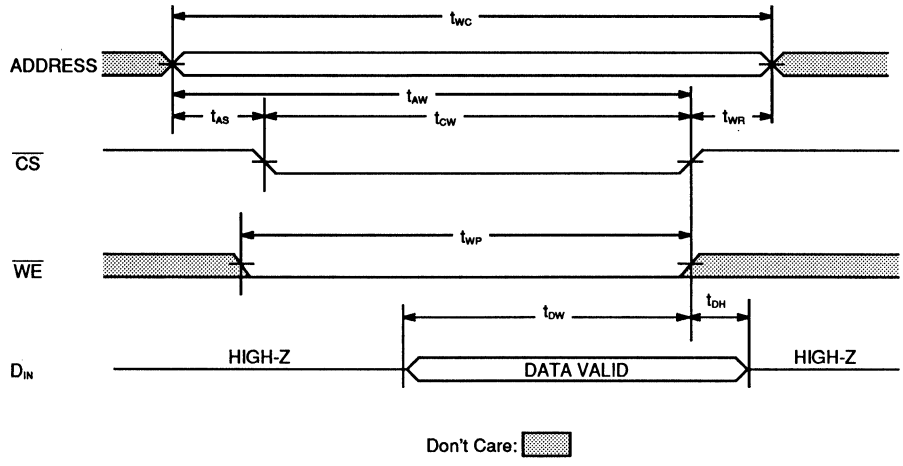
WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage.
*4 This parameter is specified with Load II in Fig. 2.

1

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

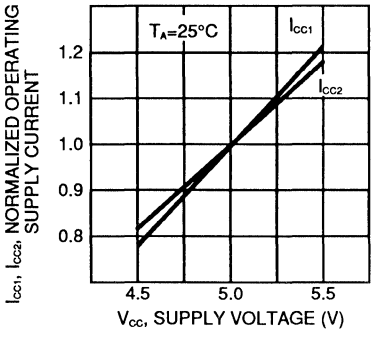


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

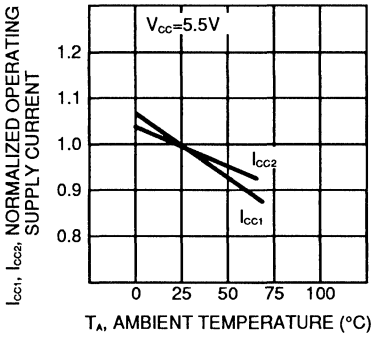


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

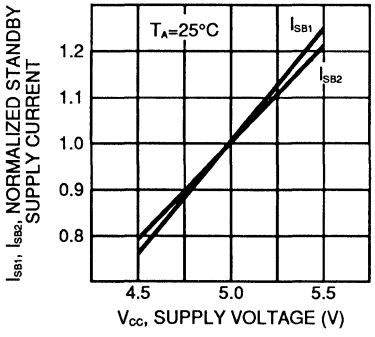


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

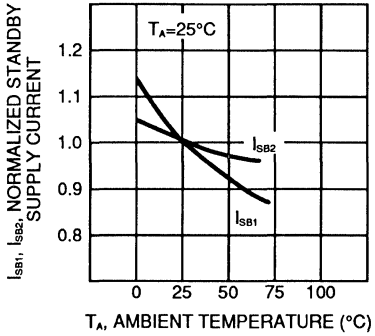
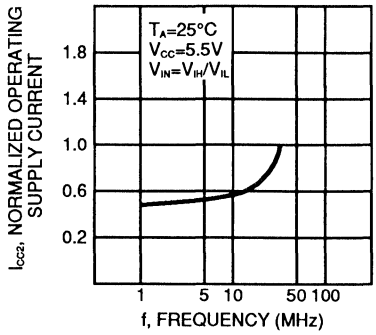


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

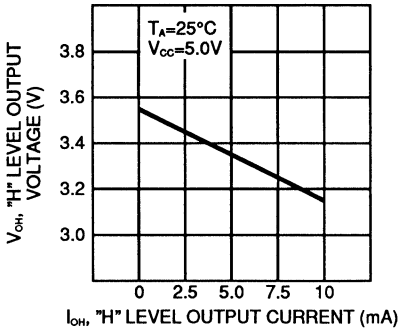


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

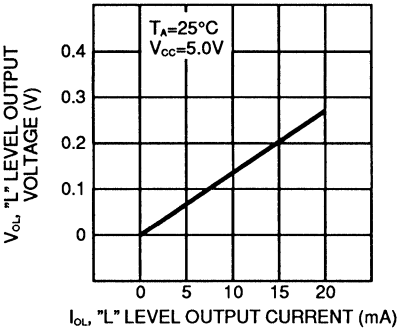


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

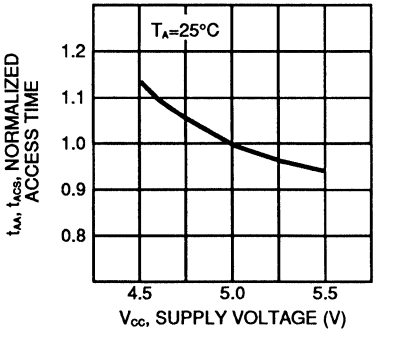


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

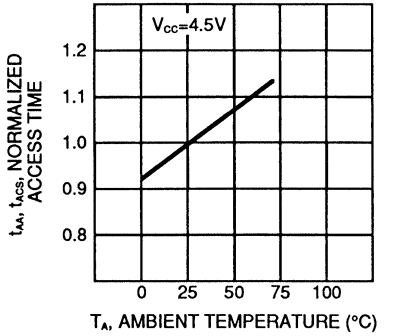
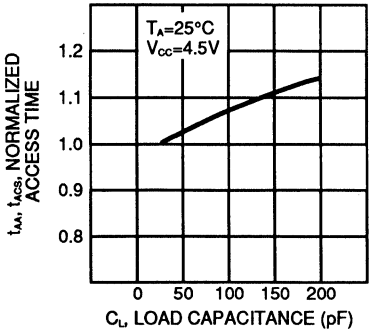


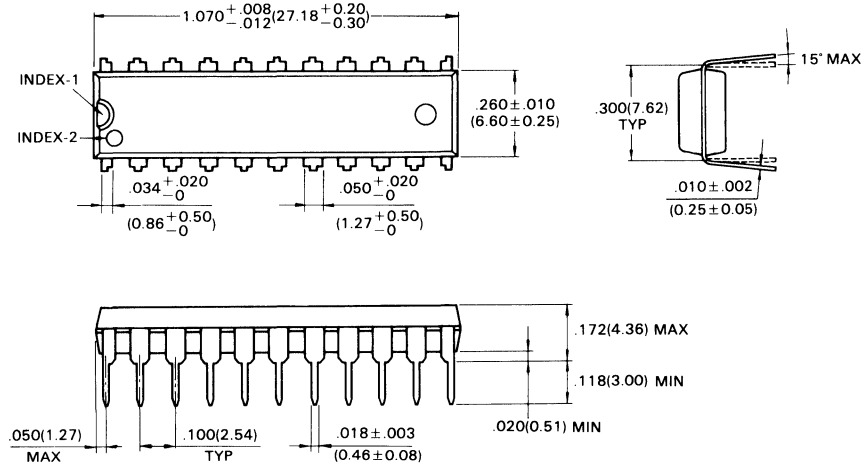
Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: P)

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-22P-M04)

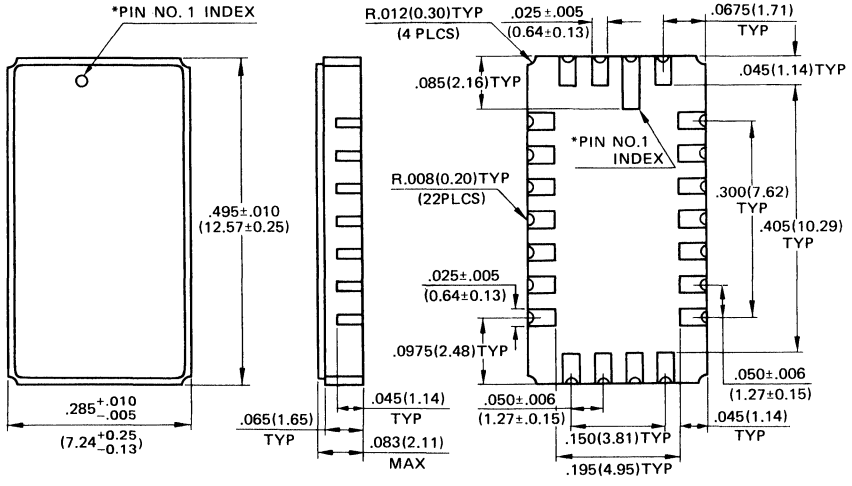


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

(Suffix: CV)

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in
inches (millimeters)

March 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C75-25/-30/-35
CMOS 64K-BIT HIGH-SPEED SRAM

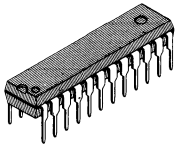
1

16K Words x 4 Bits High-Speed CMOS Static Random Access Memory

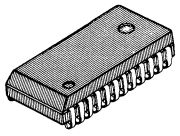
The Fujitsu MB81C75 is a 16,384 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and it may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB81C75 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 16,384 words x 4 bits
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB81C75-25)
  $t_{OE} = 10$ ns max.
  $t_{AA} = t_{ACS} = 30$ ns max. (MB81C75-30)
  $t_{OE} = 13$ ns max.
  $t_{AA} = t_{ACS} = 35$ ns max. (MB81C75-35)
  $t_{OE} = 15$ ns max.
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby, CMOS level)
  110 mW max. (Standby, TTL level)
- Standard 24-pin Plastic Package:
  DIP MB81C75-xxP
  SOJ MB81C75-xxPJ
- Standard 28-pad Ceramic Package:
  LCC (metal seal) MB81C75-xxCV

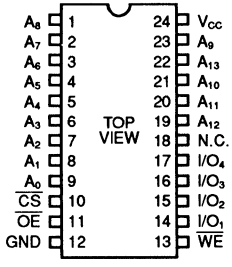


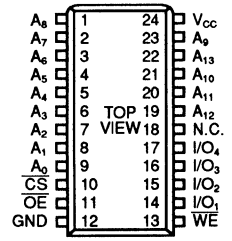
PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT





Absolute Maximum Ratings (See Note)

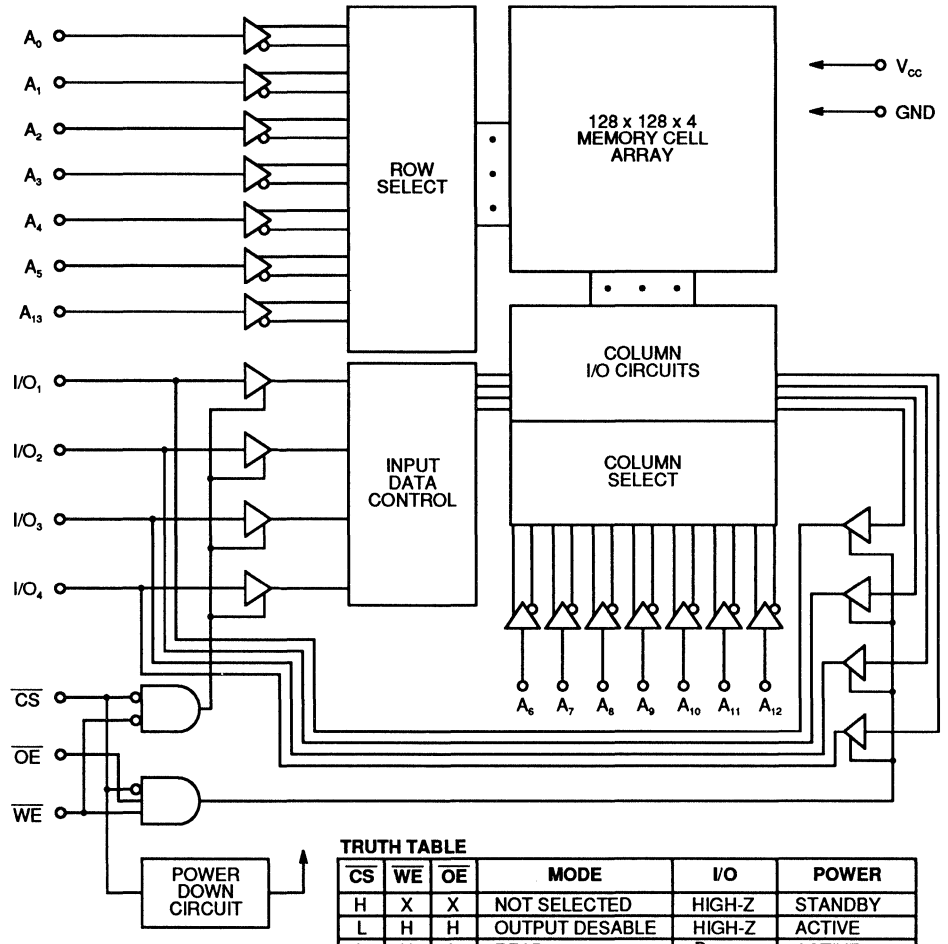
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C75 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O	POWER
H	X	X	NOT SELECTED	HIGH-Z	STANDBY
L	H	H	OUTPUT DESABLE	HIGH-Z	ACTIVE
L	H	L	READ	D_{OUT}	ACTIVE
L	L	X	WRITE	D_{IN}	ACTIVE

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			7	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

DC CHARACTERISTICS

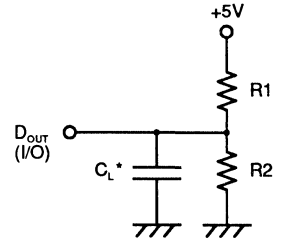
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Value		Unit
			Min	Max	
Standby Supply Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	I_{SB1}		10	mA
	$\overline{CS}=V_{IH}$	I_{SB2}		20	
Active Supply Current	$\overline{CS}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH}, I_{OUT}=0mA	I_{CC1}		60	mA
Operating Supply Current	Cycle=Min., I_{OUT}=0mA, $\overline{CS}=V_{IL}$	I_{CC2}		100	
Input Leakage Current	V_{IN}=0V to V_{CC}	I_{LI}	–10	10	µA
Output Leakage Current	$\overline{CS}=V_{IH}$, $V_{I/O}$=0V to V_{CC}	$I_{LI/O}$	–10	10	µA
Input Low Voltage		V_{IL}	–2.0*	0.8	V
Input High Voltage		V_{IH}	2.2	6.0	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V

Note: All voltages are referenced to GND
* –2.0V Min, for pulse width less than 20ns. (V_{IL} Min=–0.5V at DC Level)

Fig. 2 – AC TEST CONDITIONS

- Output Load



* Including Scope and Jig Capacitance

- Input Pulse Levels : 0V to 3.0V
- Input Pulse Rise & Fall Times : 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels : Input : 1.5V
  : Output: 1.5V

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}
Load II	480Ω	255Ω	5pF	t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ}, t_{OLZ} and t_{OHZ}

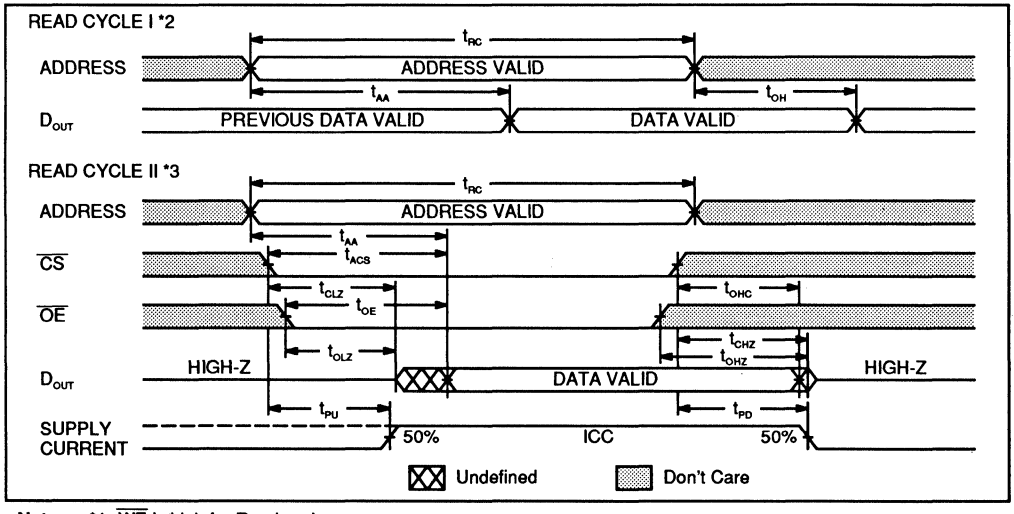
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB81C75-25		MB81C75-30		MB81C75-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		35		ns
Address Access Time *2	t_{AA}		25		30		35	ns
$\overline{CS}$ Access Time *3	t_{ACS}		25		30		35	ns
$\overline{OE}$ Access Time *3	t_{OE}		10		13		15	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	3		3		3		ns
$\overline{CS}$ to Output Low-Z *4	t_{CLZ}	5		5		5		ns
$\overline{OE}$ to Output in Low-Z *4	t_{OLZ}	0		0		0		ns
$\overline{CS}$ to Output High-Z *4	t_{CHZ}		10		13		15	ns
$\overline{OE}$ to Output High-Z *4	t_{OHZ}		10		13		15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		0		ns
power Down from $\overline{CS}$	t_{PD}		20		25		30	ns

READ CYCLE TIMING DIAGRAM *1

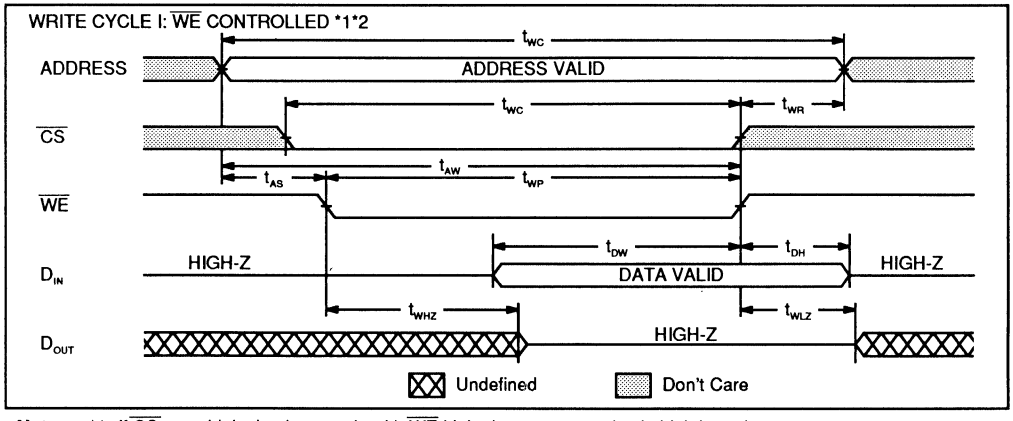


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$=V_{IL}, $\overline{OE}$=V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE *1

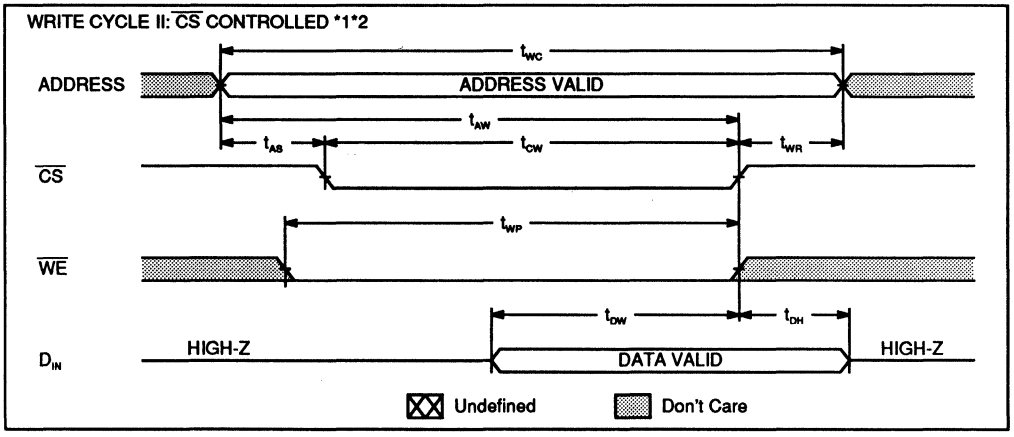
Parameter	Symbol	MB81C75-25		MB81C75-30		MB81C75-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	25		30		35		ns
Address Valid to End of Write	t_{AW}	20		25		30		ns
Chip Select to End of Write	t_{CW}	20		25		30		ns
Data Valid to End of Write	t_{DW}	13		15		17		ns
Data Hold Time	t_{DH}	2		2		2		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	2		2		2		ns
Output High-Z from $\overline{WE}$ *3	t_{WHZ}	0		0		0		ns
Output Low-Z from $\overline{WE}$ *3	t_{WLZ}		10		13		15	ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED *1*2



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycle are determined from last address transition to the first address transition of the next address.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OPERATING SUPPLY CURRENT vs. SUPPLY VOLTAGE

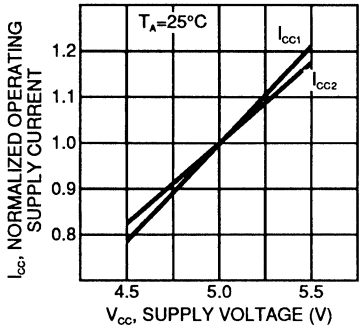


Fig. 4 – OPERATING SUPPLY CURRENT vs. AMBIENT TEMPERATURE

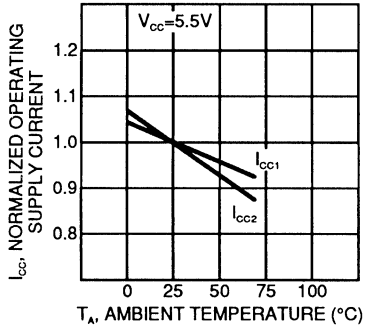


Fig. 5 – STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

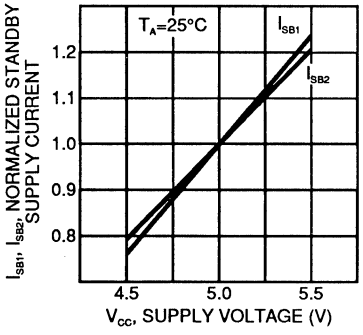


Fig. 6 – STANDBY SUPPLY CURRENT vs. AMBIENT TEMPERATURE

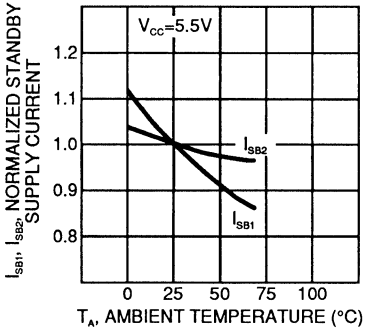
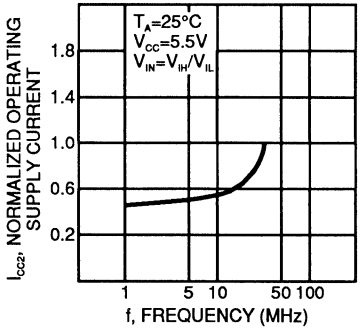


Fig. 7 – OPERATING SUPPLY CURRENT vs. FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (Cont'd)

Fig. 8 – "H" LEVEL OUTPUT VOLTAGE vs. "H" LEVEL OUTPUT CURRENT

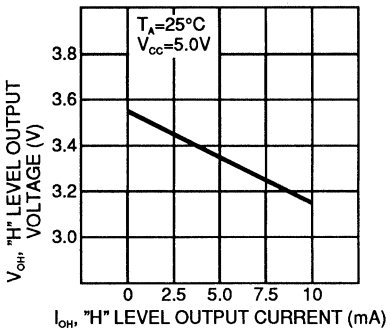


Fig. 9 – "L" LEVEL OUTPUT VOLTAGE vs. "L" LEVEL OUTPUT CURRENT

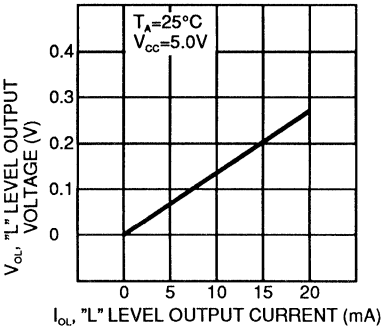


Fig. 10 – ACCESS TIME vs. SUPPLY VOLTAGE

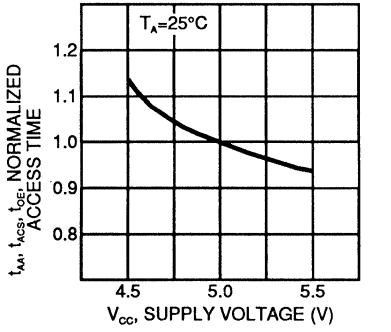


Fig. 11 – ACCESS TIME vs. AMBIENT TEMPERATURE

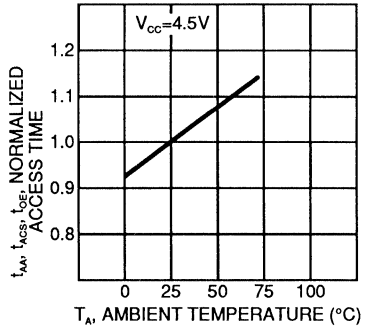
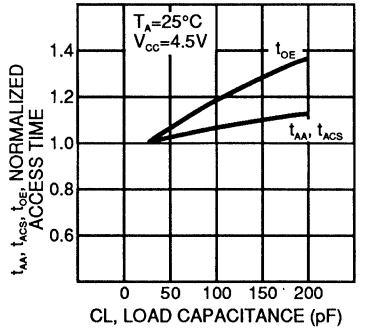


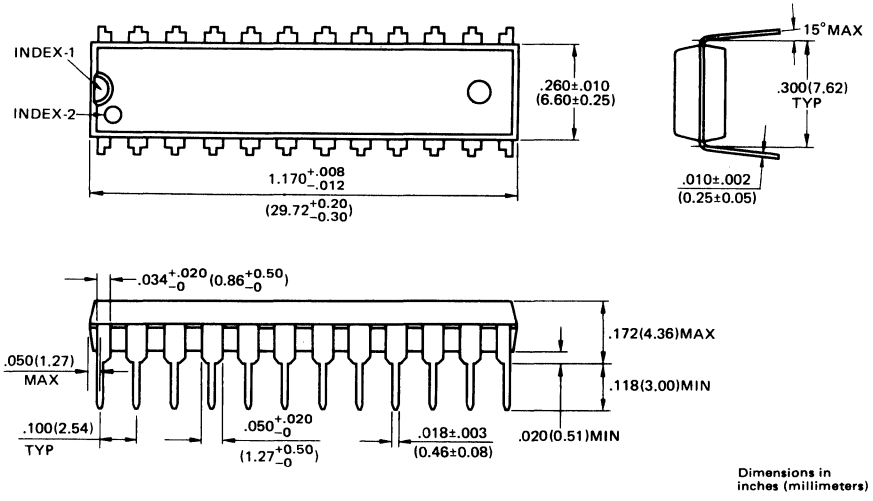
Fig. 12 – ACCESS TIME vs. LOAD CAPACITANCE



PACKAGE DIMENSIONS

(Suffix: P)

24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)

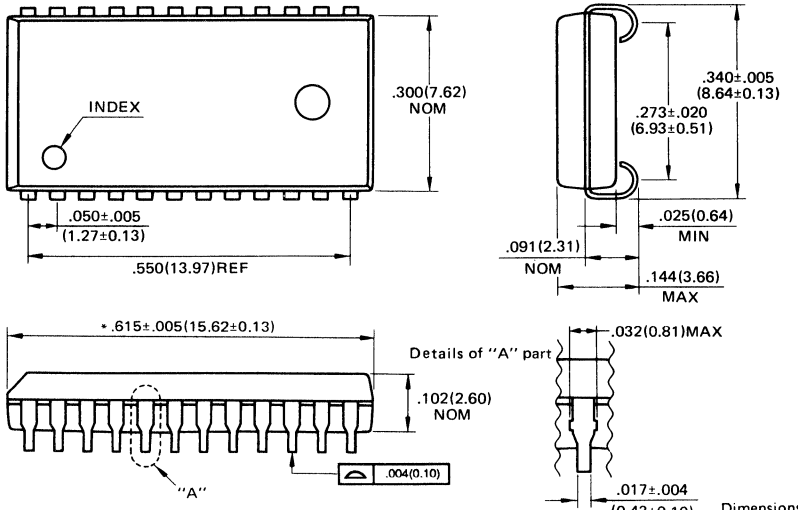


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PJ)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)

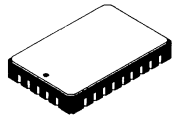


* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

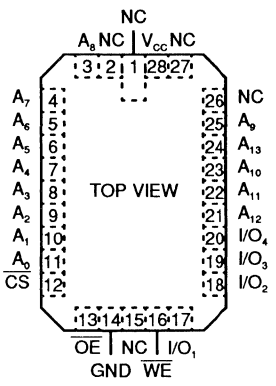
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

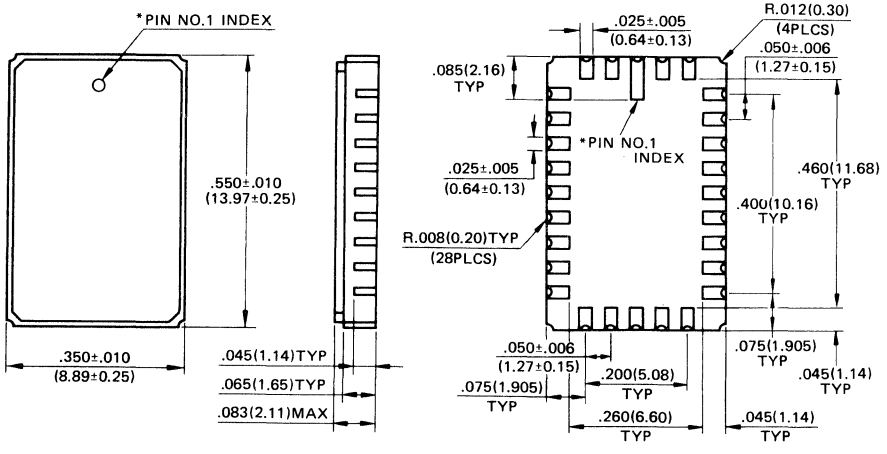
(Suffix: CV)



CERAMIC PACKAGE
LCC-28C-A03



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A03)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in inches
and (millimeters)

April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C78A-35/-45
CMOS 64K-BIT HIGH-SPEED SRAM

1

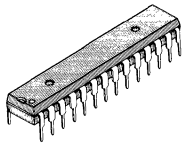
8K Words x 8 Bits High-Speed CMOS Static Random Access Memory with Automatic Power Down

The Fujitsu MB81C78A is a 8,192 words x 8 bits static random access memory fabricated with a CMOS process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

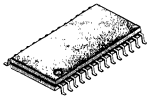
A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permiting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

The MB81C78A offers low power dissipation, low cost, and high performance.

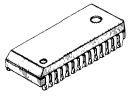
- Organization: 8,192 words x 8 bits
- Static operation: no clock or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 35$ ns max. (MB81C78A-35)
  $t_{AA} = t_{ACS1} = 45$ ns max. (MB81C78A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Package:
  Skinny DIP (300 mil) MB81C78A-xxPSK
  SOP MB81C78A-xxPF
  SOJ MB81C78A-xxPJ
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB81C78A-CV



PLASTIC PACKAGE
DIP-28P-M04

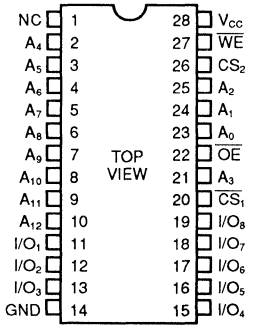


PLASTIC PACKAGE
FPT-28P-M02



PLASTIC PACKAGE
LCC-28P-M04

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

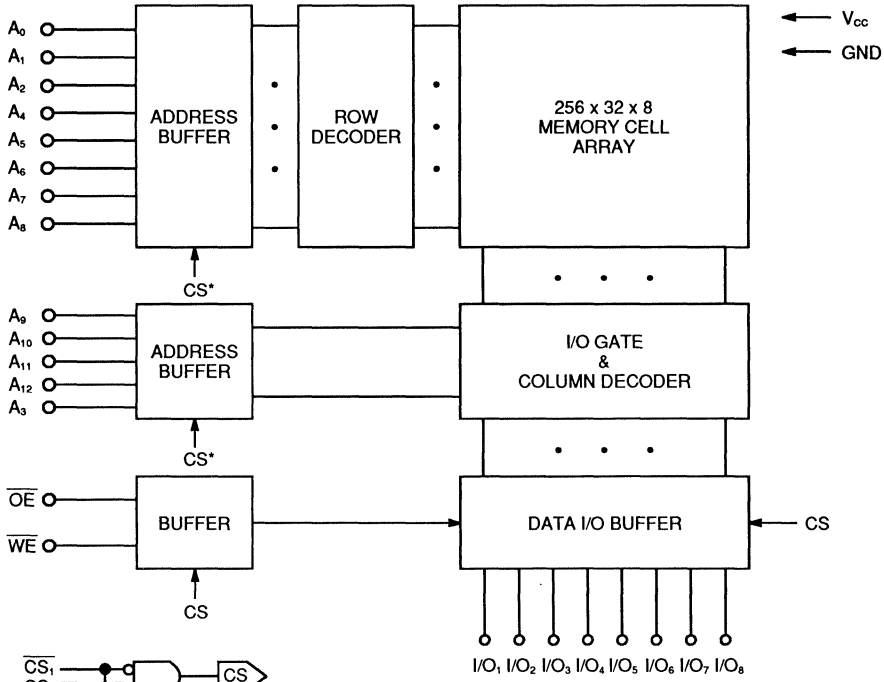
Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB81C78A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN}=0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}, V_{CC}=Max.
Output Leakage Current	I_{LO}	−10	10	µA	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1}$=V_{IL} I/O=Open, Cycle=Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC}=Min to Max. $\overline{CS_1}$=V_{CC} −0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC} −0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$=V_{IH}
Input Low Voltage	V_{IL}	−2.0*	0.8	V	
Input High Voltage	V_{IH}	2.2	6.0	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC}=0V to V_{CC} Min. $\overline{CS_1}$=Lower of V_{CC} or V_{IH} Min.

* −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

1

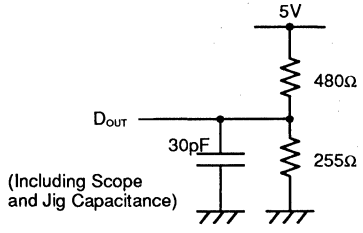
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

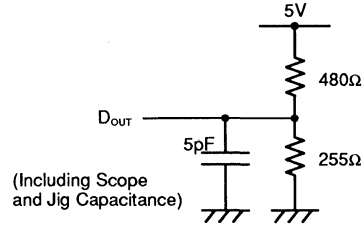
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

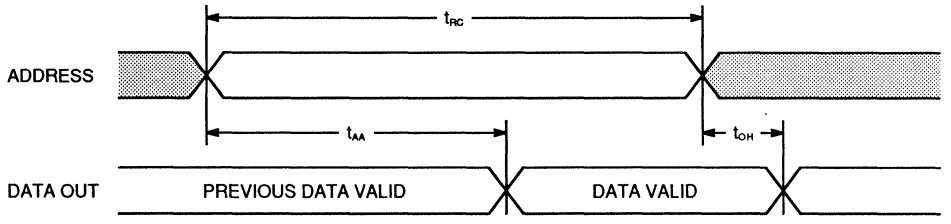
Parameter	Symbol	MB81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time*2	t_{AA}		35		45	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		35		45	ns
CS_2 Access Time*3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		5		ns
Output Active from CS_2*4	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}		20		25	ns
Output Disable from CS_2*4	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

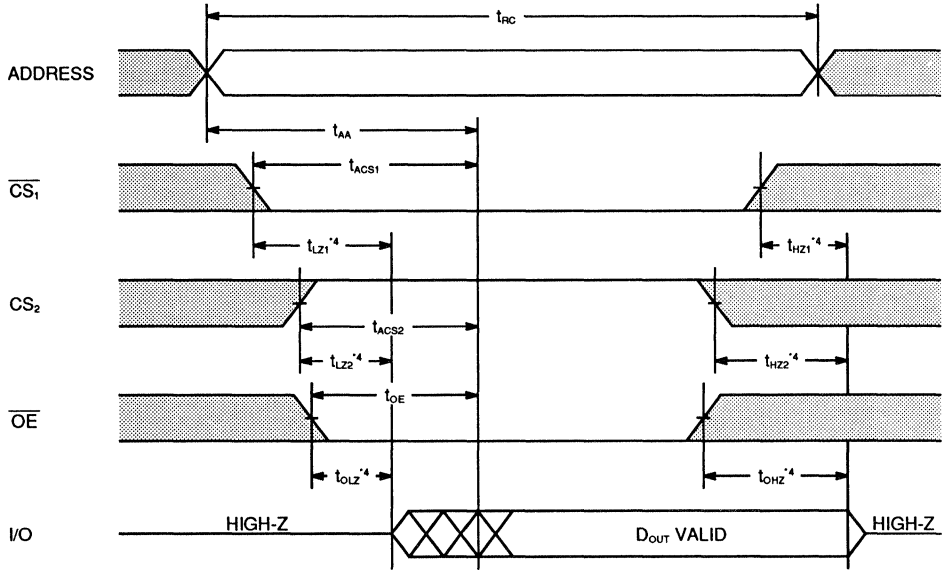
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

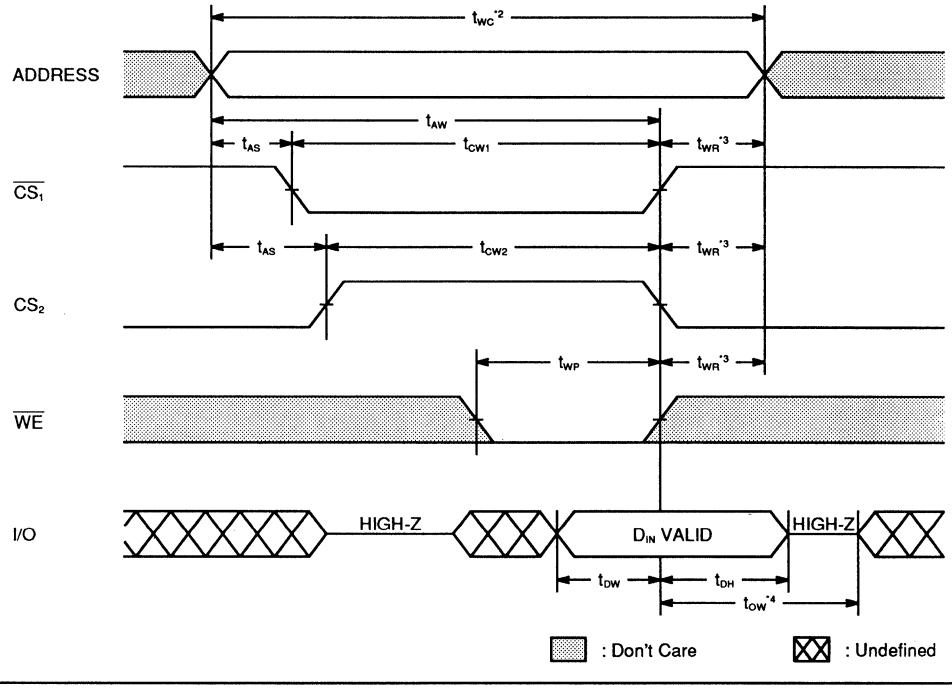
WRITE CYCLE*1

Parameter	Symbol	MB81C78A-35		MB81C78A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time*3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

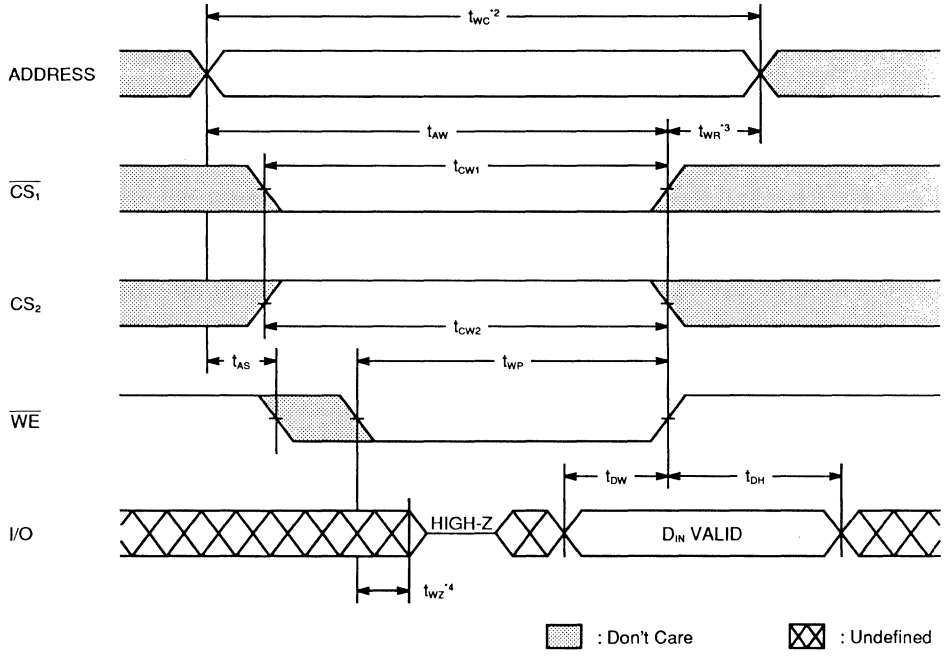
*2 All write cycle are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

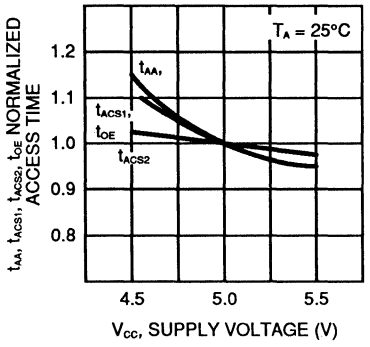


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

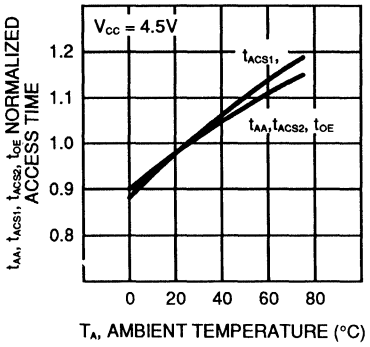


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

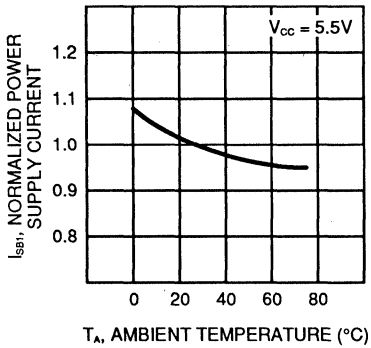


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

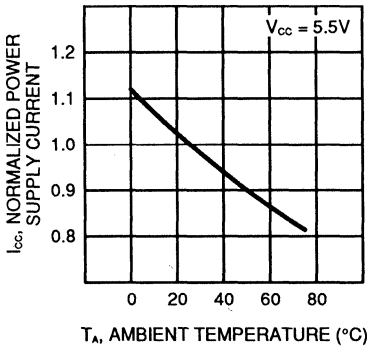


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

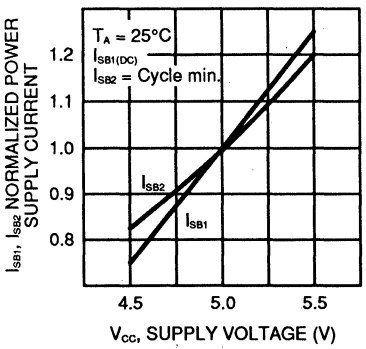


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

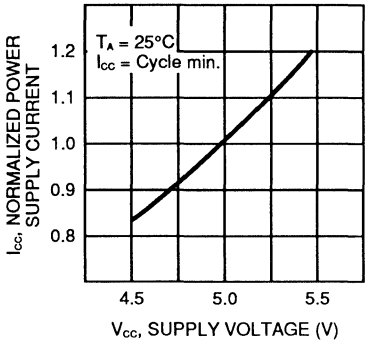


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

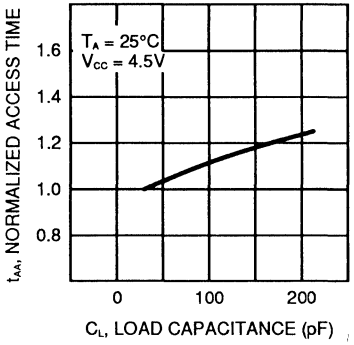


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

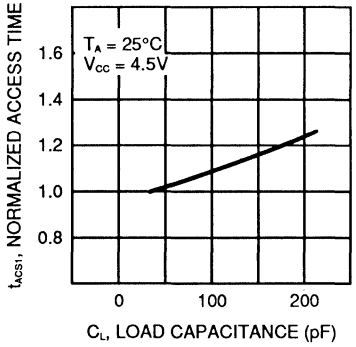


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

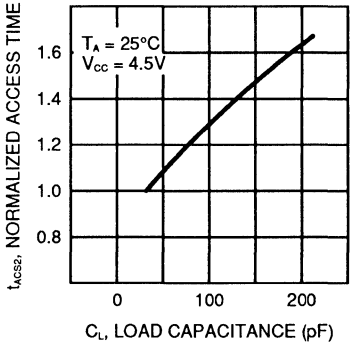
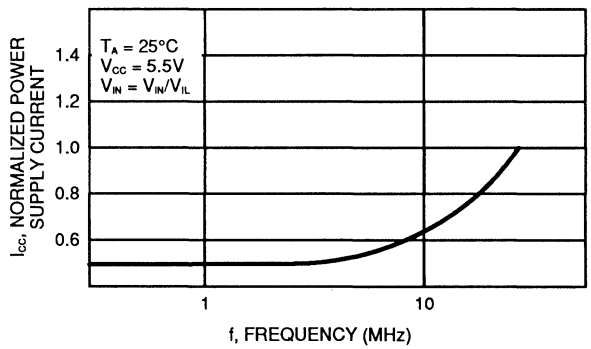


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

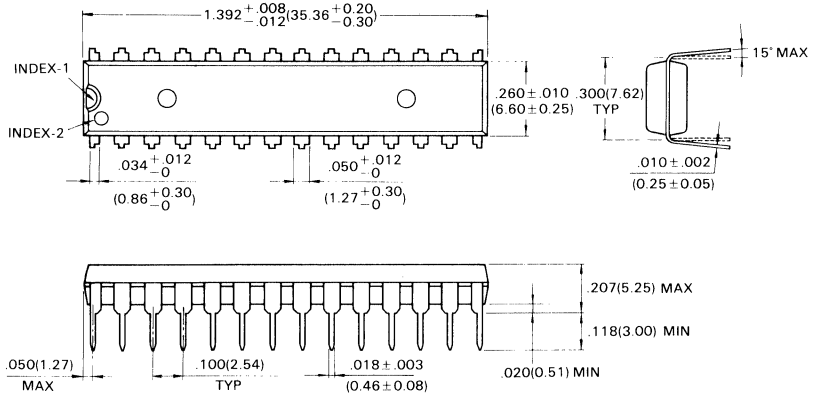


PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

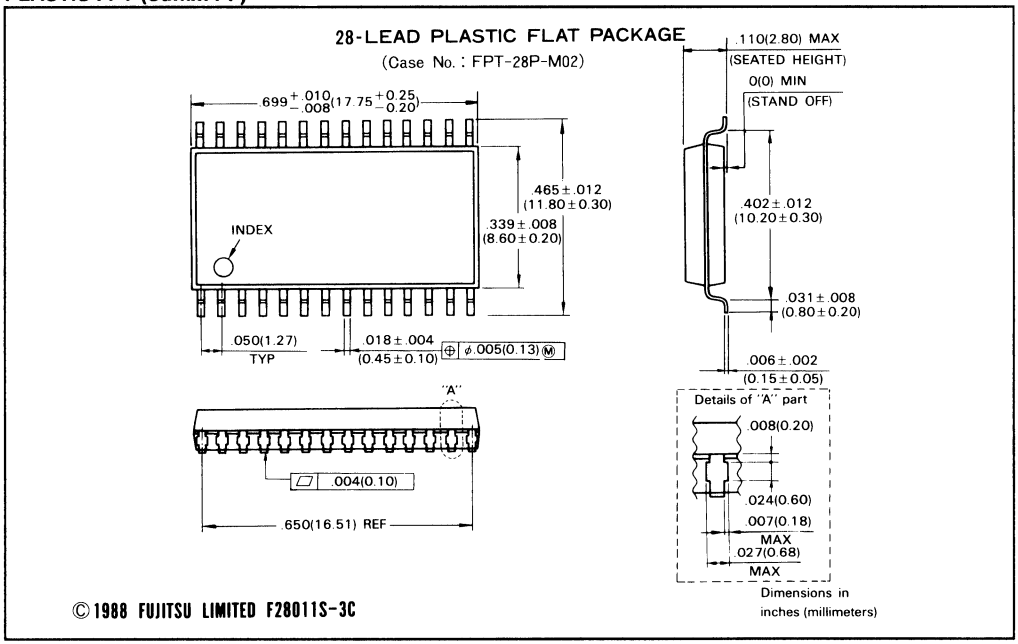
(Case No. : DIP-28P-M04)



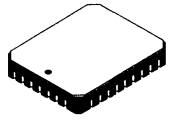
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: PF)

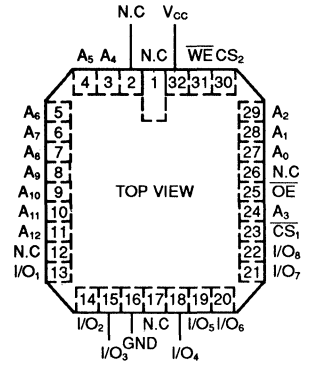


PACKAGE DIMENSIONS (Cont'd)



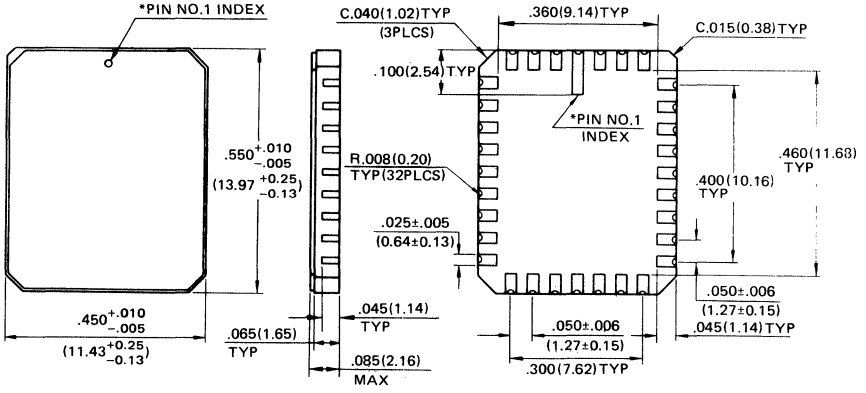
CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



CERAMIC LCC (Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

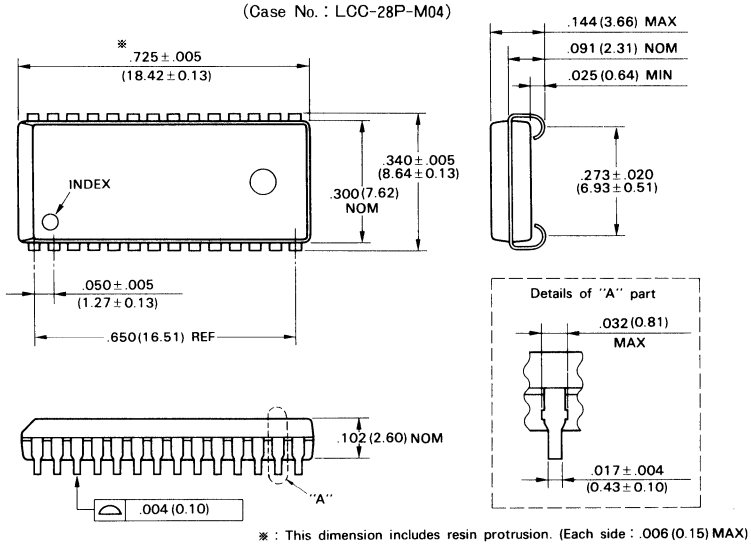
* Shape of PIN NO. 1 INDEX: Subject to change without notice.

PACKAGE DIMENSIONS

Plastic (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in inches (millimeters)

April 1990
Edition 3.0

FUJITSU

DATA SHEET

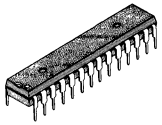
MB81C79A-35/-45
CMOS 72K-BIT HIGH-SPEED SRAM

8K Words x 9 Bits High-Speed CMOS Static Random Access Memory with Automatic Power Down

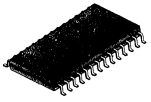
The Fujitsu MB81C79A is a 8,192 words x 9 bits static random access memory fabricated with a CMOS process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

- Organization: 8,192 words x 9 bits
- Static operation: no clocks or refresh required
- Access time: $t_{AA} = t_{ACS1} = 35$ ns max. (MB81C79A-35)
  $t_{ACS2} = t_{OE} = 45$ ns max. (MB81C79A-45)
- Low power consumption: 495 mW max. (Operating)
  138 mW max. (Standby, TTL level)
  83 mW max. (Standby, CMOS level)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C79A-xxPSK
  SOP MB81C79A-xxPF
  SOJ MB81C79A-xxPJ
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB81C79A-CV



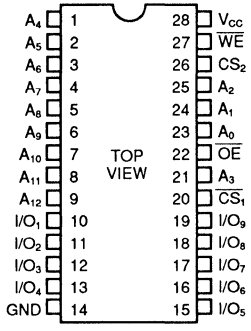
PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02

PLASTIC PACKAGE
LCC-28P-M04

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

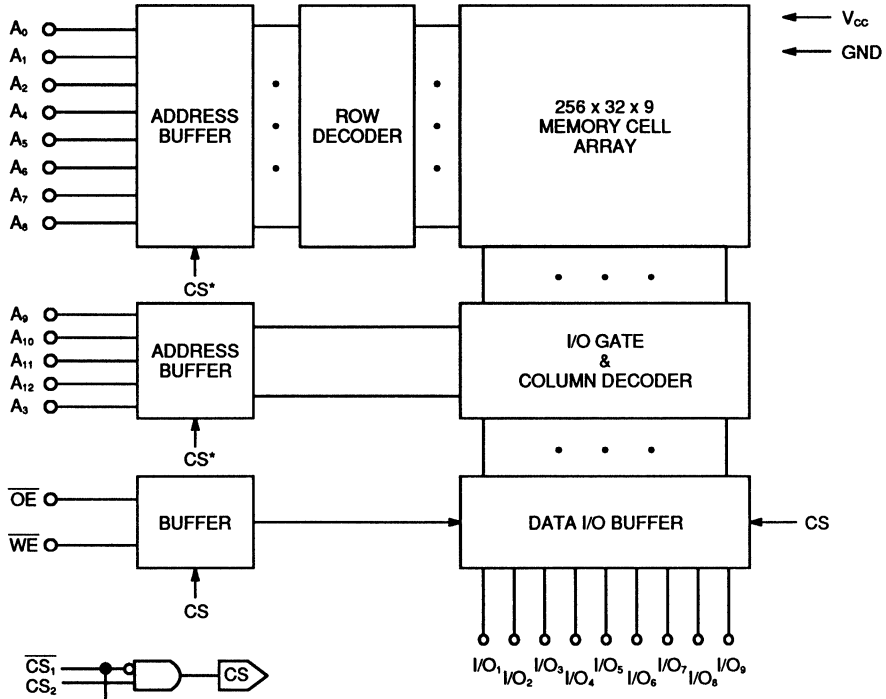
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND		V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7.0	V
Output Current		I_{OUT}	±20	mA
Power Dissipation		P_D	1.0	W
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C79A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN}=0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}, V_{CC}=Max.
Output Leakage Current	I_{LO}	−10	10	µA	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC}		90	mA	$\overline{CS_1}$=V_{IL} I/O=Open, Cycle=Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC}=Min to Max. $\overline{CS_1}$=V_{CC} −0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC} −0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$=V_{IH}
Input Low Voltage	V_{IL}	−2.0*	0.8	V	
Input High Voltage	V_{IH}	2.2	6.0	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC}=0V to V_{CC} Min. $\overline{CS_1}$=Lower of V_{CC} or V_{IH} Min.

* −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

1

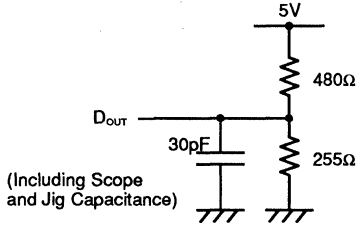
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V

Fig. 2

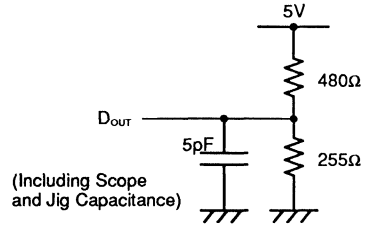
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

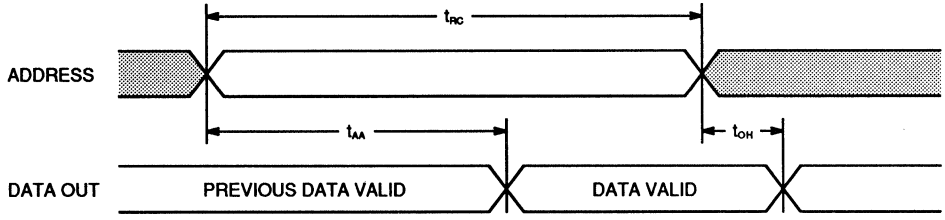
Parameter	Symbol	MB81C79A-35		MB81C79A-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time*2	t_{AA}		35		45	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		35		45	ns
CS_2 Access Time*3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		15		20	ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		5		ns
Output Active from CS_2*4	t_{LZ2}	3		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	3		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}		20		25	ns
Output Disable from CS_2*4	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}		20		25	ns

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with CS_1 transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

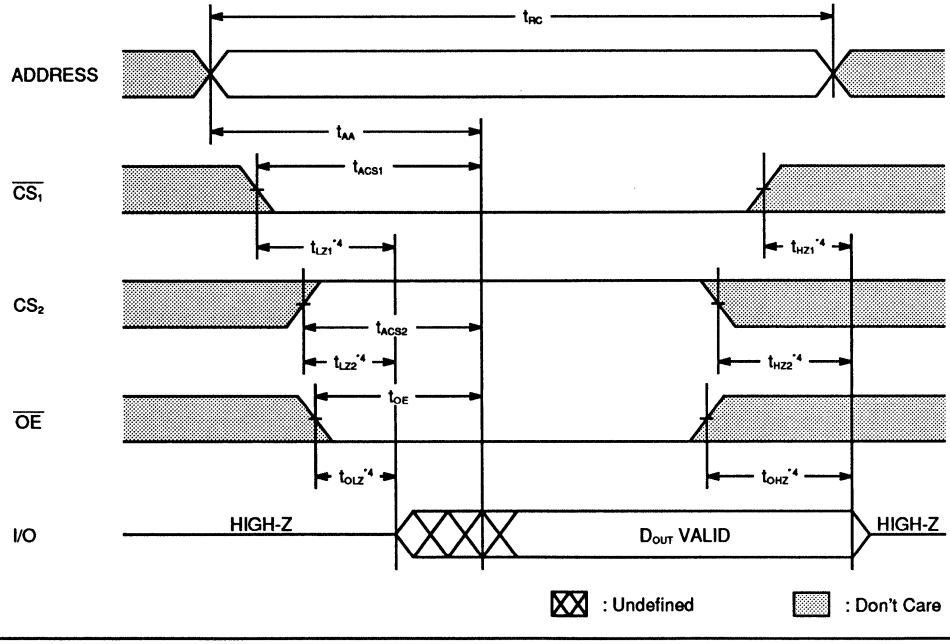
1

READ CYCLE TIMING DIAGRAM*1

READ CYCLE I: ADDRESS CONTROLLED*2



READ CYCLE II: $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read cycle.

*2 Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} and $\overline{OE}$ = V_{IL}.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE*1

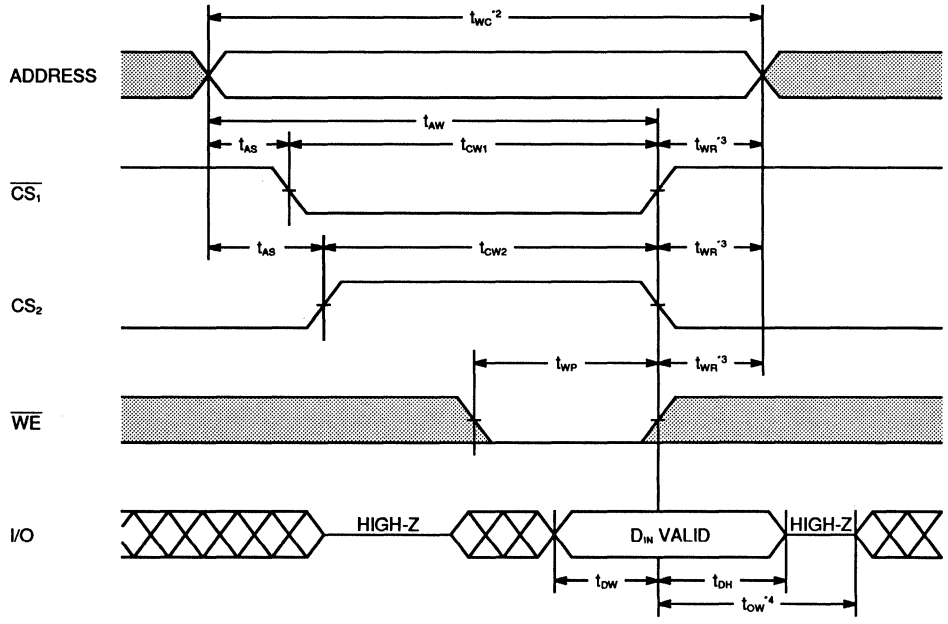
Parameter	Symbol	MB81C79A-35		MB81C79A-45		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time*3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

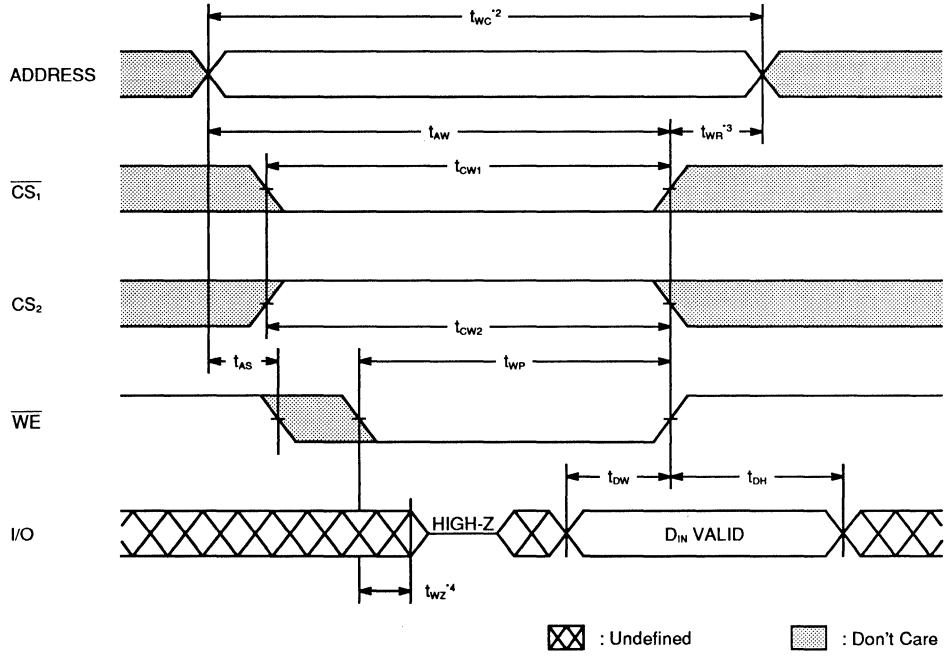
*2 All write cycle are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

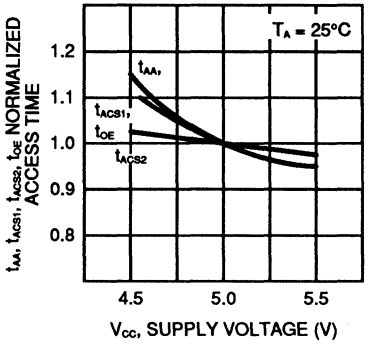


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

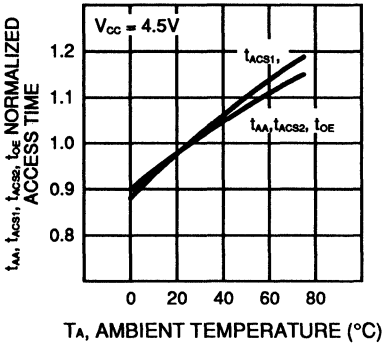


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

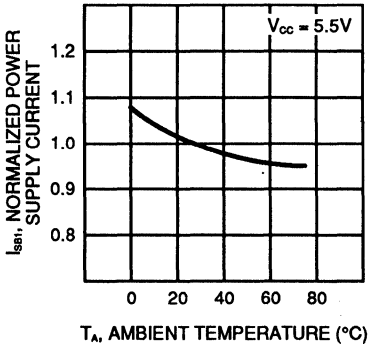


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

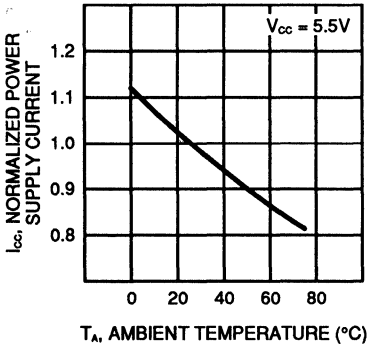


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

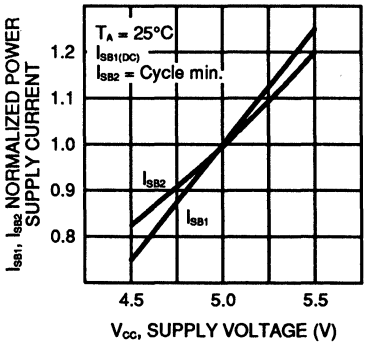


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

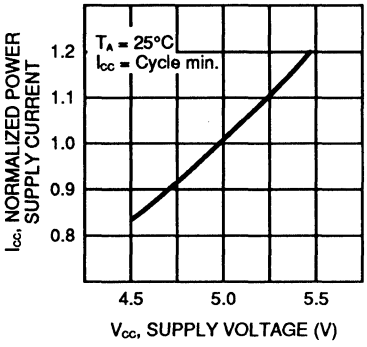


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

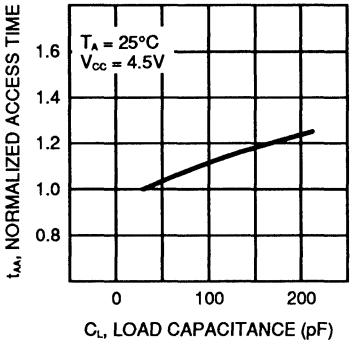


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

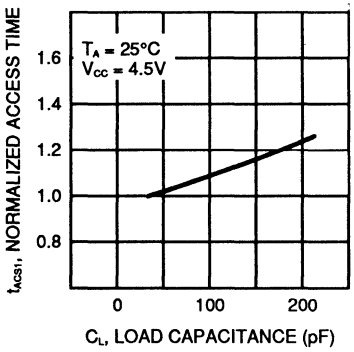


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

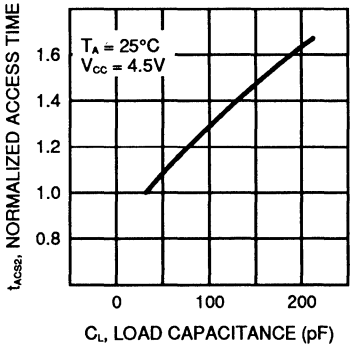
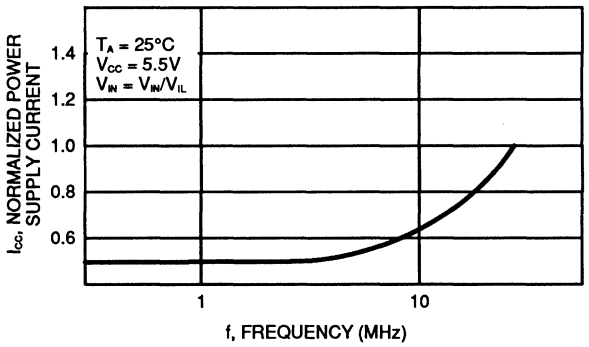


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY

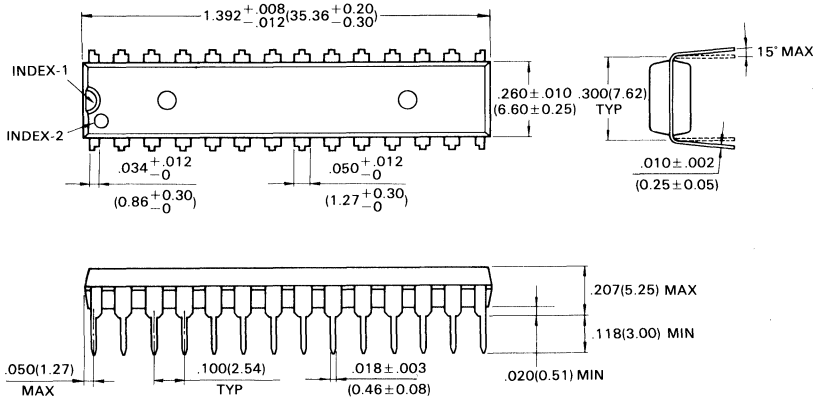


PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

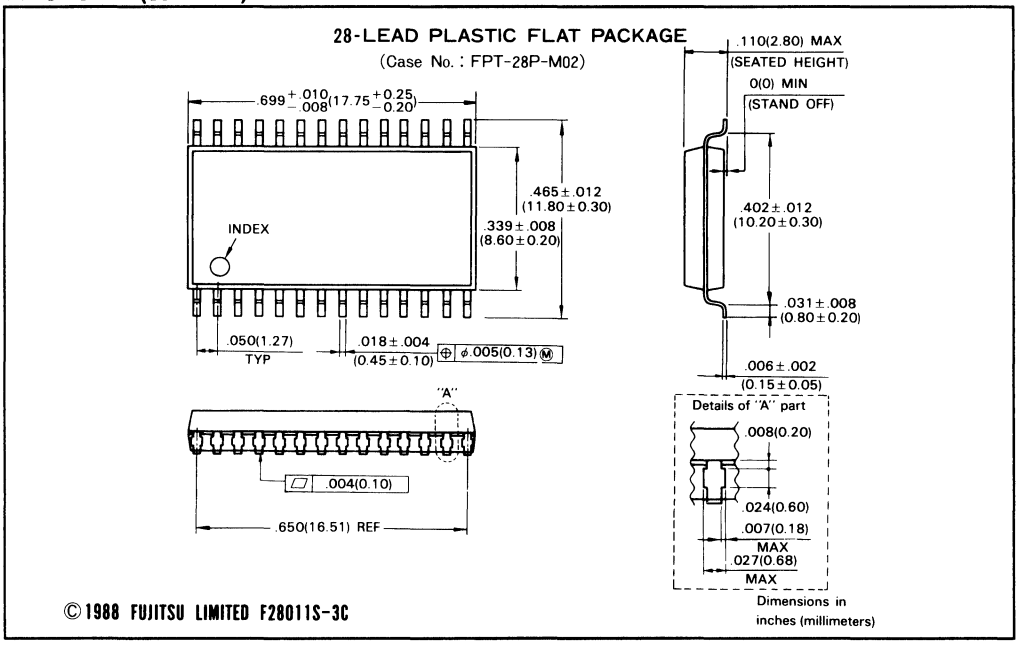
(Case No. : DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: PF)

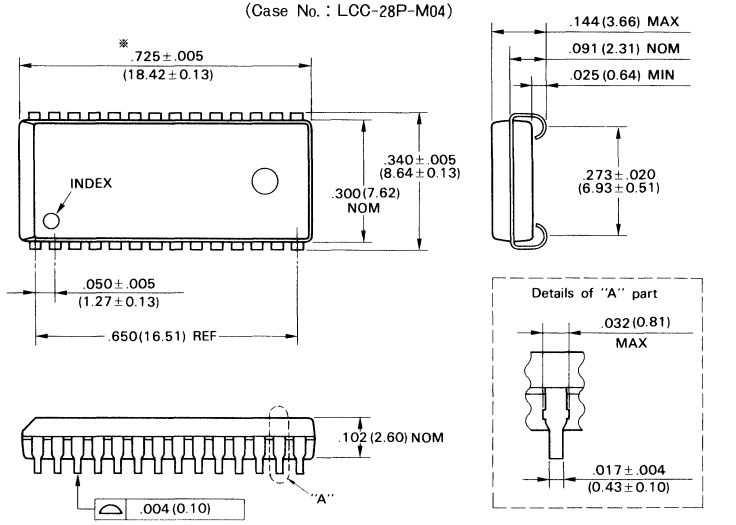


PACKAGE DIMENSIONS (Cont'd)

PLASTIC (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER

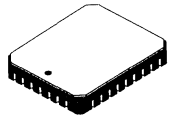
(Case No. : LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

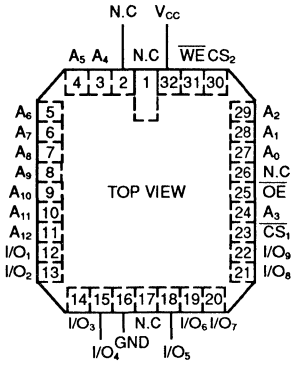
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)



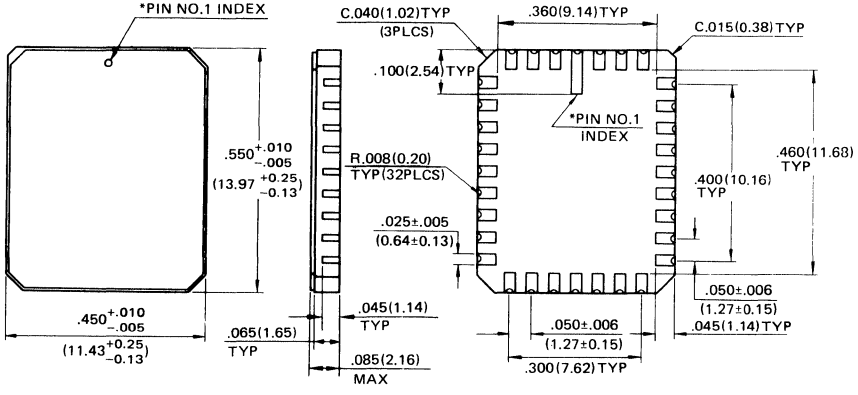
CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT



CERAMIC LCC (Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

May 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C81A-25/-35
CMOS 256K-BIT HIGH-SPEED SRAM

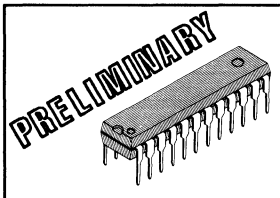
1

256K Words x 1 Bit High-Speed CMOS Static Random Access Memory

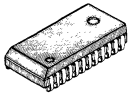
The Fujitsu MB81C81A is a 262,144 words x 1 bit static random access memory fabricated with a CMOS technology. The MB81C81A uses NMOS cells and CMOS peripherals and has 300 mil plastic DIP and SOJ packages. It uses fully static circuitry throughout and, therefore, requires no clocks or refreshes to operate.

The MB81C81A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. It is compatible with TTL logic and requires a single +5 V supply.

- Organization: 262,144 words x 1 bit
- Static operation: no clocks or refresh required
- Access time: 25 ns max. (MB81C81A-25)
  35 ns max. (MB81C81A-35)
- Single +5 V power supply ±10% tolerance with low current drain:
  100 mA max. (Active operation)
  55 mA max. (Standby, CMOS level)
  30 mA max. (Standby, TTL level)
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Chip selected for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 24-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C81A-xxPSK
  SOJ (300 mil) MB81C81A-xxPJ

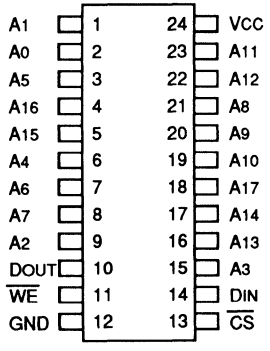


PLASTIC PACKAGE
DIP-24P-M03



PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT
TOP VIEW



Absolute Maximum Ratings (See Note)

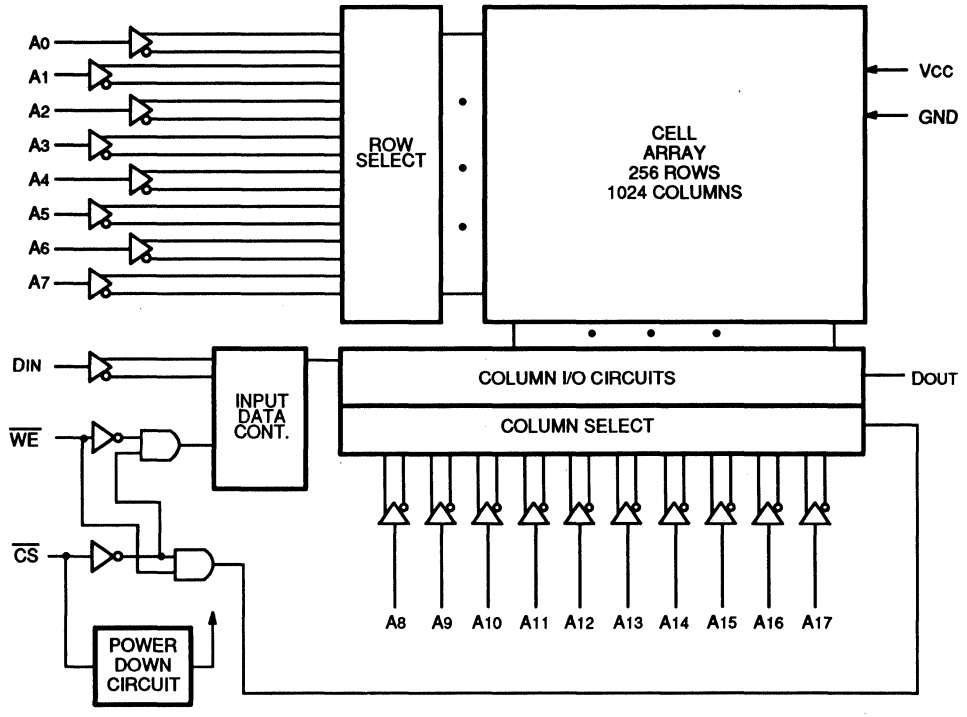
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.0 to +7	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C81A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V\overline{CS}$ = 0 V)	$C\overline{CS}$		8	pF
Output Capacitance (VOUT = 0 V)	COUT		8	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
DIN	Data Input	VCC	Power Supply (5V±10%)
DOUT	Data Output	GND	Ground
$\overline{CS}$	Chip Select		

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceed 2m/sec.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to VCC	ILI	–10		10	µA
Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to VCC	ILO	–50		50	µA
Power Supply Current	$\overline{CS}$ = VIL, VIN = VIH or VIL IOUT = 0mA, Cycle = Min.	ICC			100	mA
Standby Supply Current	$\overline{CS}$≥VCC–0.2V VIN≥VCC–0.2V or VIN≤0.2V	ISB1			15	mA
	$\overline{CS}$ = VIH, VIN = VIH or VIL	ISB2			30	mA
Peak Power on Current *1	VCC = 0V to VCC Min., $\overline{CS}$ = Lower of VCC or VIH Min.	IPO			30	mA
Input High Voltage		VIH	2.2		6.0	V
Input Low Voltage		VIL	–0.5 *2		0.8	V
Output High Voltage	IOH = –4mA	VOH	2.4			V
Output Low Voltage	IOL = 8mA	VOL			0.4	V

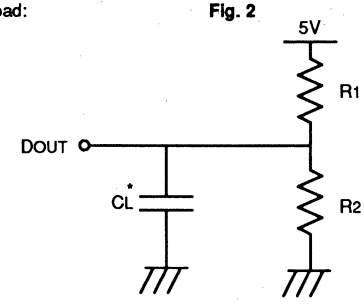
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –2.0 V Min. for pulse width less than 10 ns.

1

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 2 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: VIL = 0.8, VIH = 2.2 V
  Output: VOL = 0.8, VOH = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480 Ω	255 Ω	30 pF	except tLZ, tHZ, tOW and tWZ
Load II	480 Ω	255 Ω	5 pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

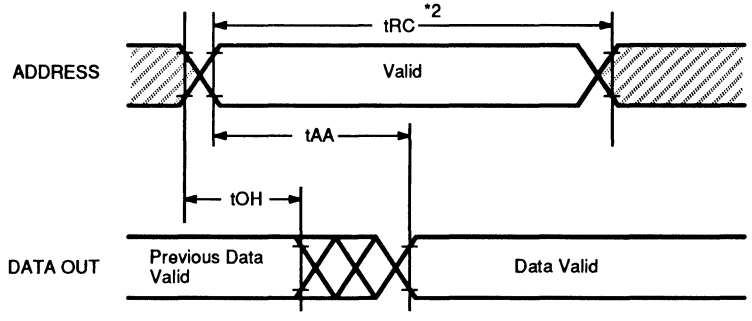
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C81A–25		MB81C81A–35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2 *3	tRC	25		35		ns
Address Access Time	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	3		3		ns
Chip Selection to Output in Low–Z	tLZ	3		3		ns
Chip Deselect to Output in High–Z	tHZ	0	15	0	20	ns
Chip Selection to Power Up Time	tPU	0		0		ns
Chip Selection to Power Down Time	tPD		25		35	ns

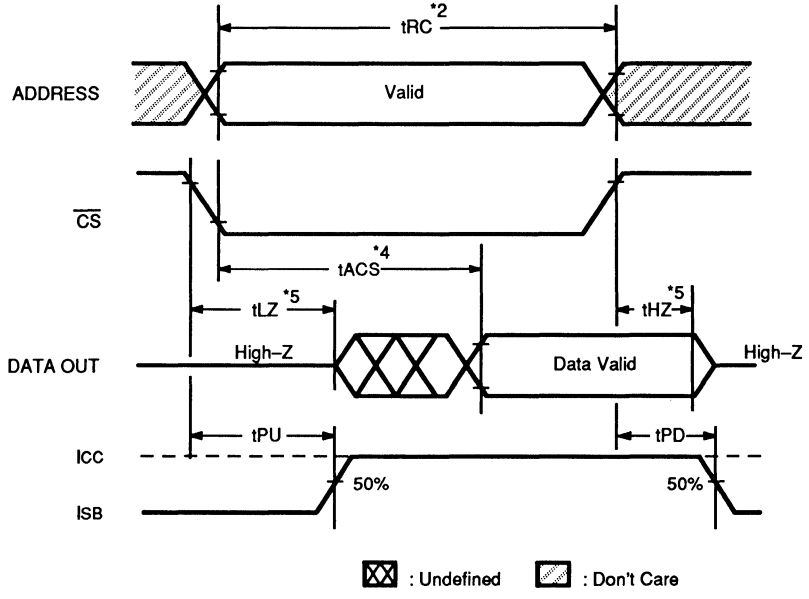
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



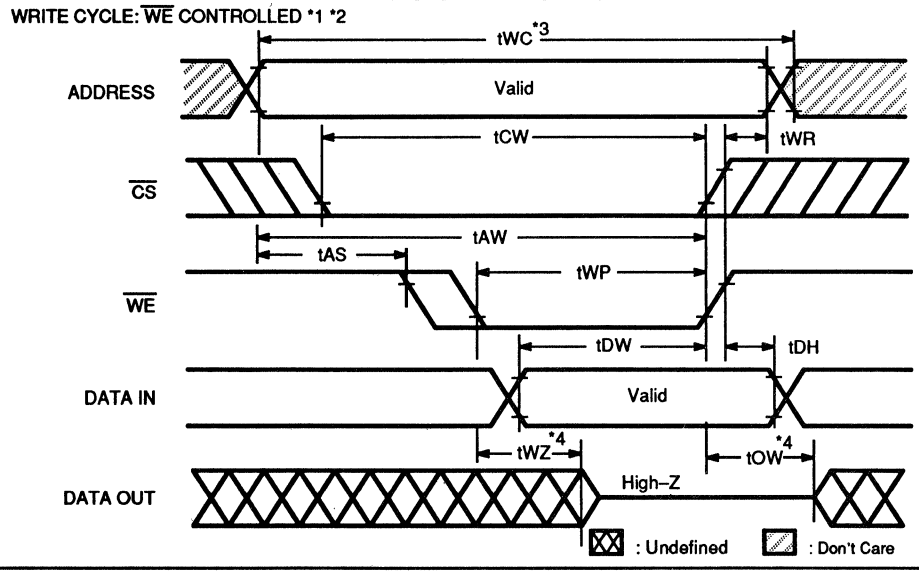
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C81A-25		MB81C81A-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time	tWC	25		35		ns
Address Valid to End of Write	tAW	20		30		ns
Chip Selection to End of Write	tCW	20		30		ns
Data Valid to End of Write	tDW	13		18		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	18		28		ns
Write Recovery Time	tWR	1		1		ns
Address Setup Time	tAS	0		0		ns
Output Active from End of Write	tOW	0		0		ns
Write Enable to Output in High-Z	tWZ	0	12	0	15	ns

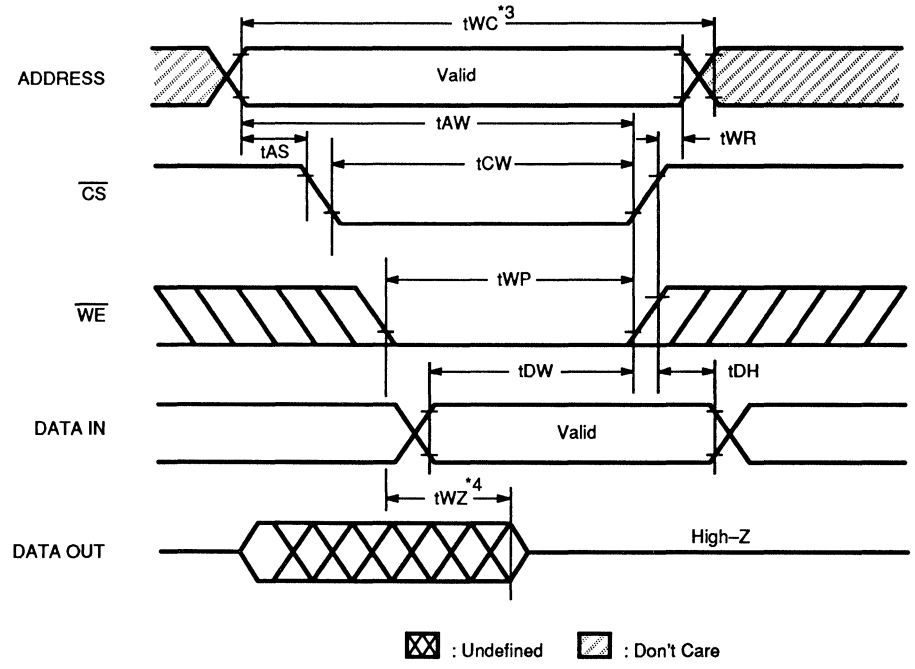
WRITE CYCLE TIMING DIAGRAM



*1 CS or WE must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

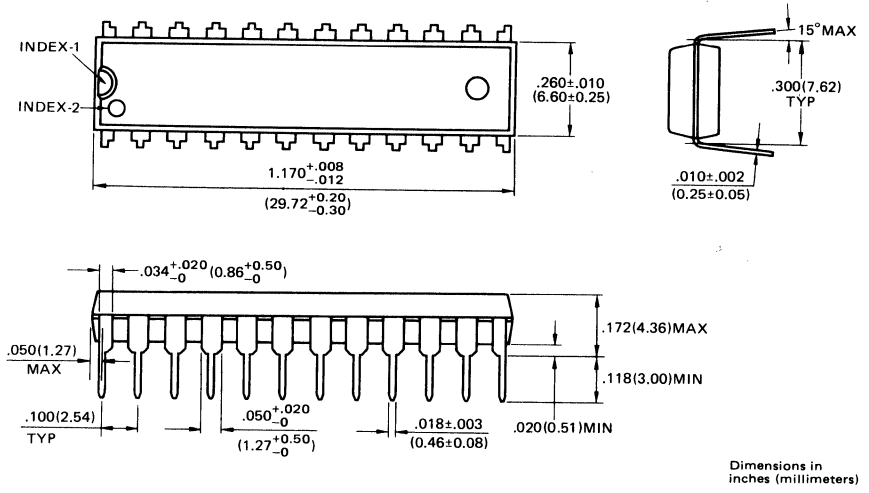


*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

PACKAGE DIMENSIONS

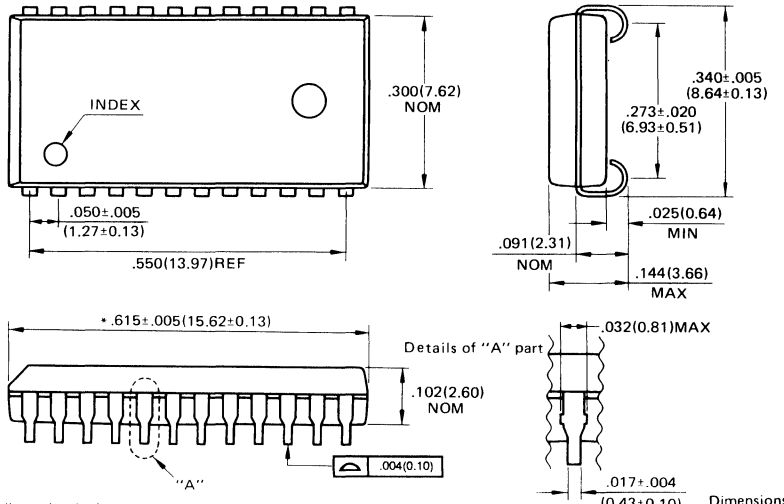
24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



Dimensions in inches (millimeters)

* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

May 1990
Edition 1.0

FUJITSU

DATA SHEET

MB81C84A-25/-35
CMOS 256K-BIT HIGH-SPEED SRAM

1

64K Words x 4 Bits High-Speed CMOS Static Random Access Memory

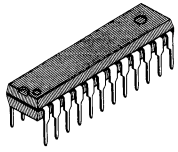
The Fujitsu MB81C84A is a 65,536 words x 4 bits static random access memory fabricated with CMOS silicon gate process technology. The MB81C84A uses NMOS cells and CMOS peripherals and is housed in 300 mil plastic DIP and SOJ packages.

The MB81C84A uses fully static circuitry and, therefore, requires no clocks or refreshes to operate. It is compatible with TTL logic and requires a single +5 V supply.

It is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required.

- Organization: 65,536 words x 4 bits
- Static operation: no clocks or refresh required
- Access time: 25 ns max. (MB81C84A-25)
  35 ns max. (MB81C84A-35)
- Single +5 V power supply ±10% tolerance with low current drain
  100 mA max. (Active operation)
  15 mA max. (Standby operation, TTL level)
  30 mA max. (Standby operation, CMOS level)
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Standard 24-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C84A-xxPSK
  SOJ (300 mil) MB81C84A-xxPJ

PRELIMINARY



PLASTIC PACKAGE
DIP-24P-M03

PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT
TOP VIEW

A1	1	24		VCC
A0	2	23		A11
A5	3	22		A12
A14	4	21		A8
A13	5	20		A9
A4	6	19		A10
A6	7	18		A15
A7	8	17		I/O4
A2	9	16		I/O3
A3	10	15		I/O2
$\overline{CS}$	11	14		I/O1
GND	12	13		$\overline{WE}$

Absolute Maximum Ratings (See Note)

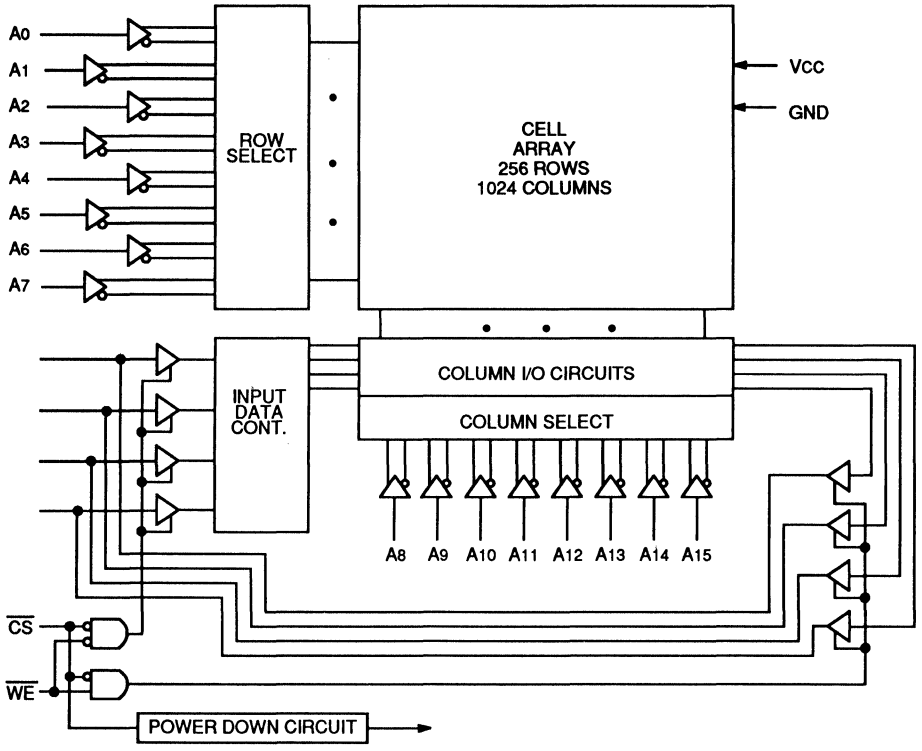
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.0 to +7.0	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB81C84A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	DIN	Active
L	H	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		8	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		8	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A0 to A15	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O4	Data Inputs/Data Outputs	VCC	Power Supply (5V±10%)
$\overline{CS}$	Chip Select	GND	Ground

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceed 2m/sec.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to VCC	ILI	–10		10	µA
Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to 4.5V	ILO	–50		50	µA
Power Supply Current	$\overline{CS}$ = VIL, VIN = VIH or VIL, IOUT = 0mA, Cycle = Min.	ICC			100	mA
Standby Supply Current	$\overline{CS}$≥VCC–0.2V VIN≥VCC–0.2V or VIN≤0.2V	ISB1			15	mA
	$\overline{CS}$ = VIH, VIN = VIH or VIL	ISB2			30	mA
Peak Power on Current *1	VCC = 0V to VCC Min., $\overline{CS}$ = Lower of VCC or VIH Min.	IPO			40	mA
Input High Voltage		VIH	2.2		6.0	V
Input Low Voltage		VIL	–0.5 *2		0.8	V
Output High Voltage	IOH = –4mA	VOH	2.4			V
Output Low Voltage	IOL = 8mA	VOL			0.4	V

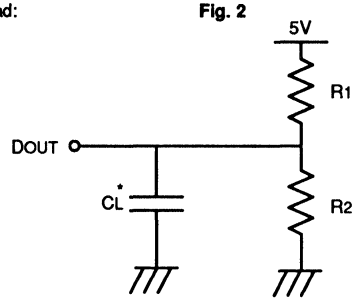
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –2.0 V Min. for pulse width less than 10 ns.

1

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 2 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: VIL = 0.8, VIH = 2.2 V
  Output: VOL = 0.8, VOH = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5 pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

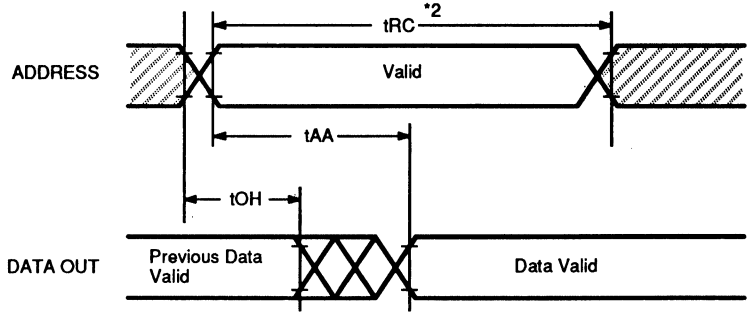
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C84A-25		MB81C84A-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2 *3	tRC	25		35		ns
Address Access Time	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	3		3		ns
Chip Selection to Output in Low-Z	tLZ	3		3		ns
Chip Deselect to Output in High-Z	tHZ	0	15	0	20	ns
Chip Selection to Power Up Time	tPU	0		0		ns
Chip Selection to Power Down Time	tPD		25		35	ns

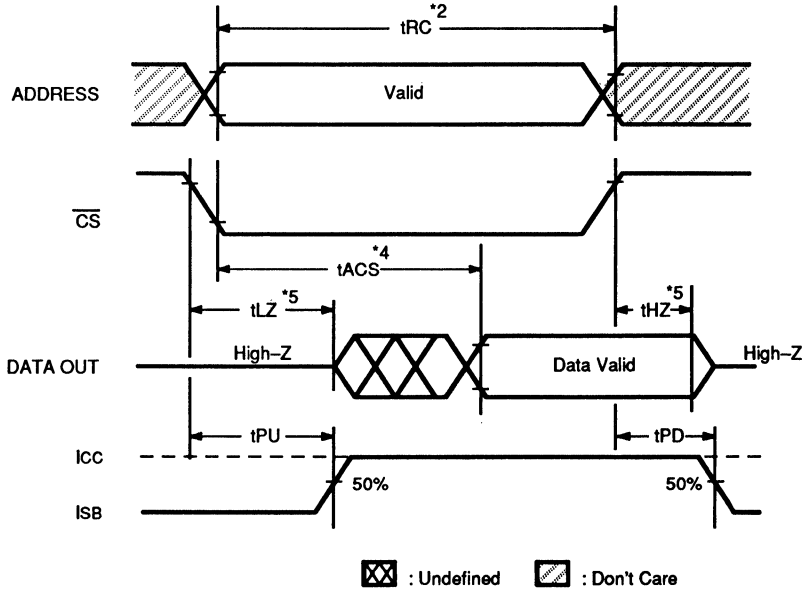
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



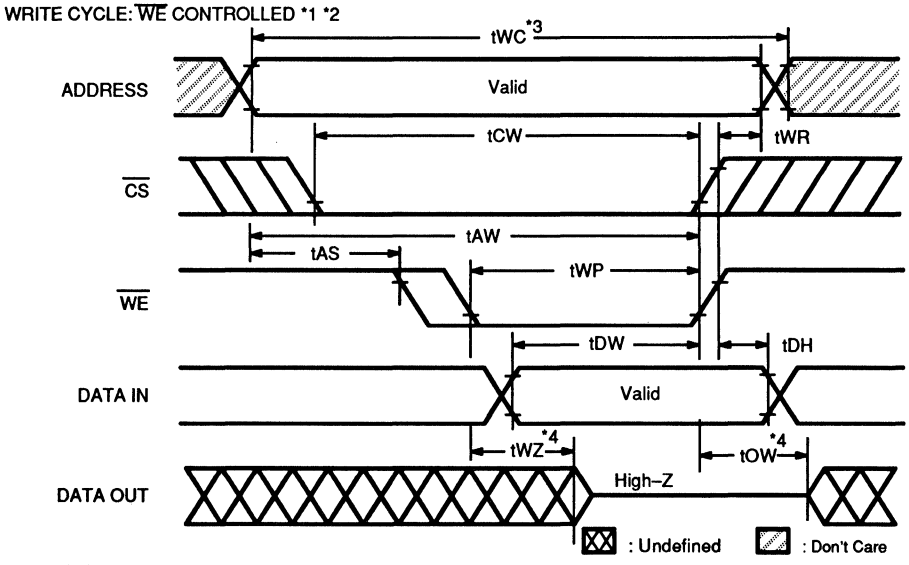
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C84A-25		MB81C84A-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time	tWC	25		35		ns
Address Valid to End of Write	tAW	20		30		ns
Chip Selection to End of Write	tCW	20		30		ns
Data Valid to End of Write	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	18		28		ns
Write Recovery Time	tWR	1		1		ns
Address Setup Time	tAS	0		0		ns
Output Active from End of Write	tOW	3		3		ns
Write Enable to Output in High-Z	tWZ	0	9	0	15	ns

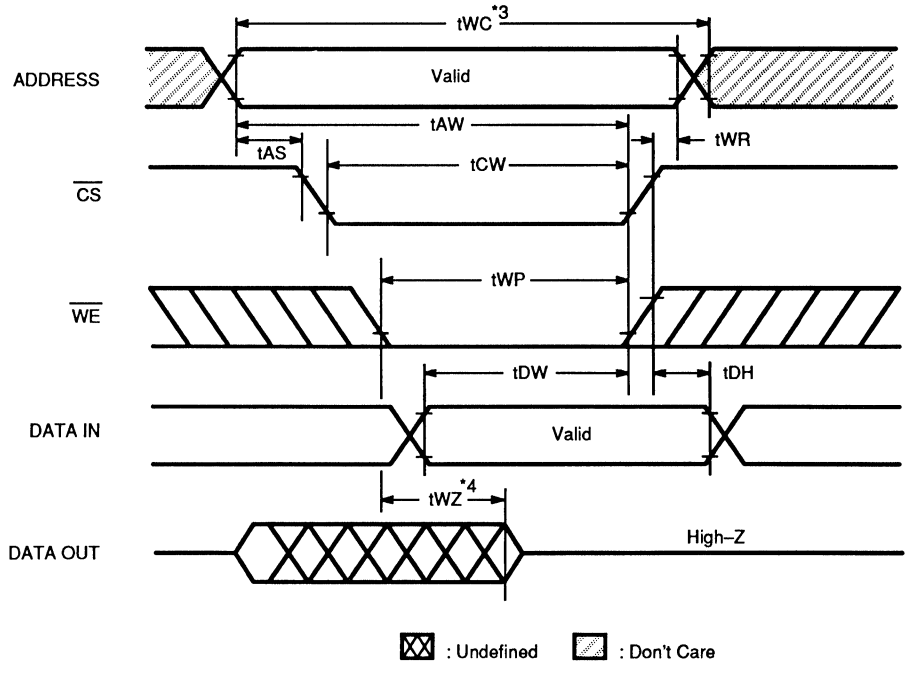
WRITE CYCLE TIMING DIAGRAM



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

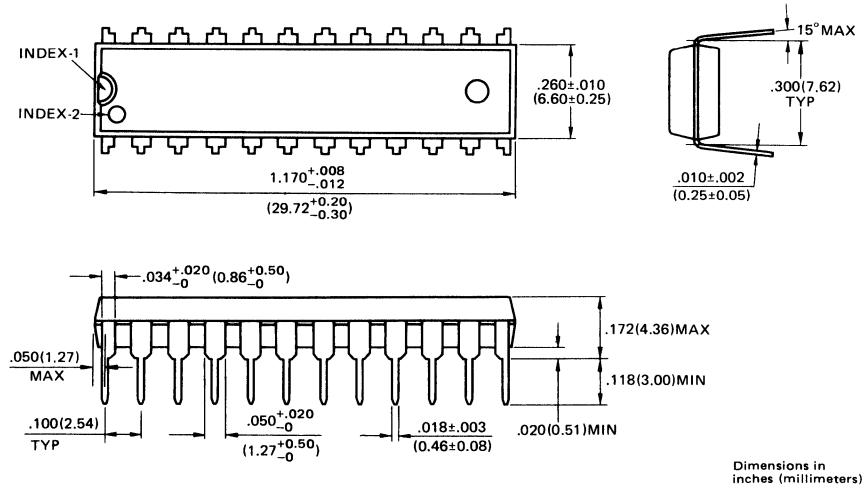
WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

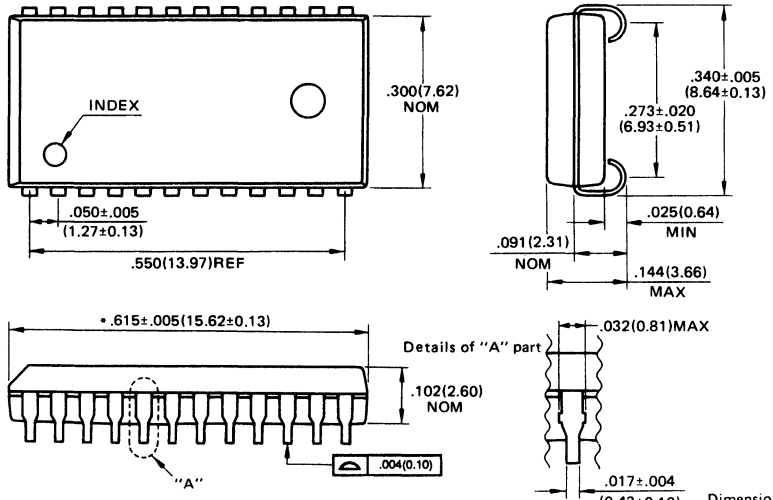
24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)

April 1990
Edition 2.0

FUJITSU

DATA SHEET

MB8289-25/-35
CMOS 288K-BIT HIGH-SPEED SRAM

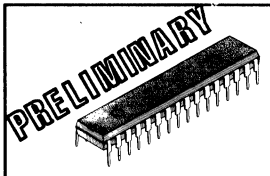
32K Words x 9 Bits Static Random Access Memory with Automatic Power Down

The Fujitsu MB8289 is a 32,768 words x 9 bits static random access memory with parity generator and checker, and fabricated with CMOS technology. To obtain a smaller chip size, the cell uses NMOS transistors and resistors. This device is housed in a 300 mil DIP package with low (605 mW max.) power dissipation. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

The MB8289 offers low power dissipation, low cost, and high performance.

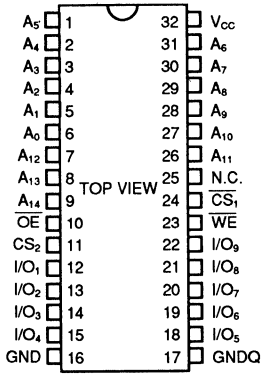
- Organization: 32,768 words x 9 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 25$ ns max, $t_{ACS2} = 14$ ns max. (MB8289-25)
  $t_{AA} = t_{ACS1} = 35$ ns max, $t_{ACS2} = 15$ ns max. (MB8289-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8289-xxPSK
  SOP (450 mil) MB8289-xxPF



PLASTIC PACKAGE
(DIP-32P-M02)

PLASTIC PACKAGE
(FPT-32P-M02)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

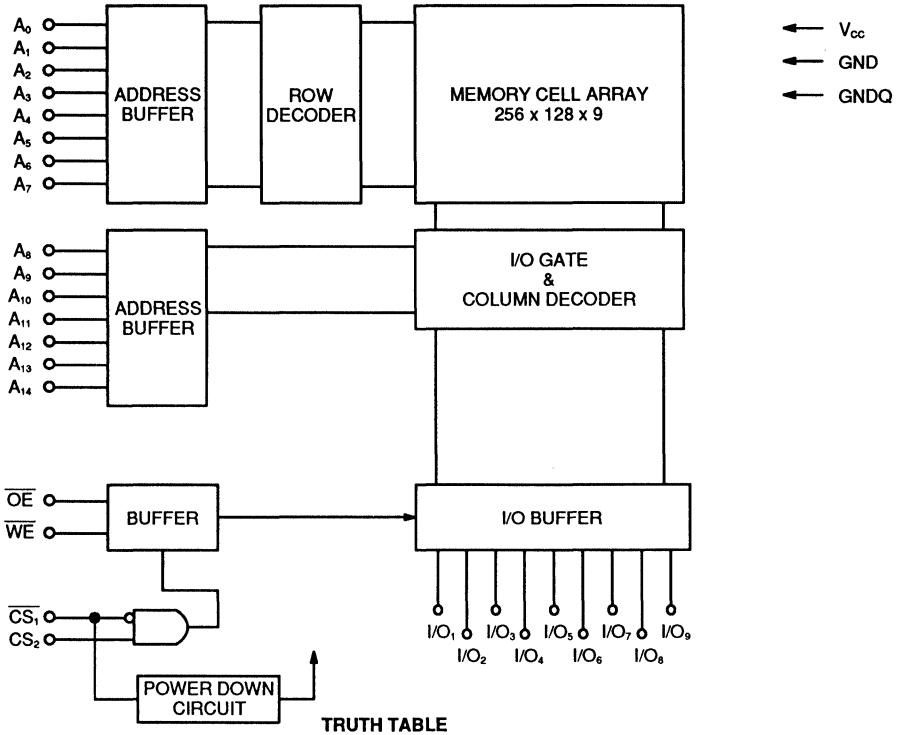
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB8289 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN}=0V	C_{I1}			8	pF
Inout Capacitance (Other Input)	V_{IN}=0V	C_{I2}			7	pF
I/O Capacitance	$V_{I/O}$=0V	$C_{I/O}$			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

1

DC CHARACTERISTICS

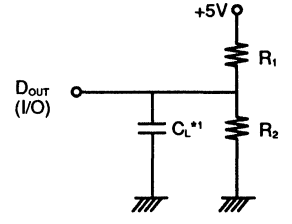
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS_1} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS_1} = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	I_{OUT}=0mA, $\overline{CS_1}=V_{IL}$ Cycle=Min.		130	mA
	35ns				110	
Input Leakage Current		I_{LI}	V_{IN}=0V to V_{CC}, V_{CC}=Max.	−5	5	µA
Output Leakage Current		$I_{LI/O}$	$\overline{CS_1}=V_{IH}$ or $\overline{CS_2}=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=0V to V_{CC}	−5	5	µA
Input Low Voltage		V_{IL}		−2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	I_{OH}=−4mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL}=8mA		0.4	V

Note: *1 −2.0V Min. for pulse width less than 20ns. (V_{IL} min. =−0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.2V
- Output Load:



	R_1	R_2	C_L	Parameters Measured
Load I	480kΩ	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ} and t_{OHZ}
Load II	480kΩ	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ} and t_{OHZ}

*1 Including Scope and Jig Capacitance

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE*1

Parameter	Symbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Access Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		8		ns
Output Active from CS_2*4	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2*4	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}	1	15	1	15	ns

Note: *1 $\overline{WE}$ is high for Read Cycle.

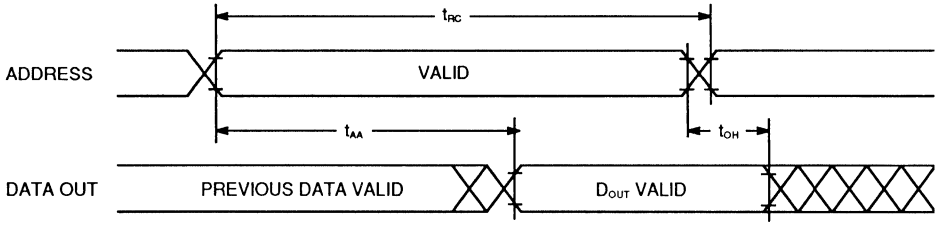
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $\overline{CS_2}=V_{IH}$ and $\overline{OE}=V_{IL}$.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

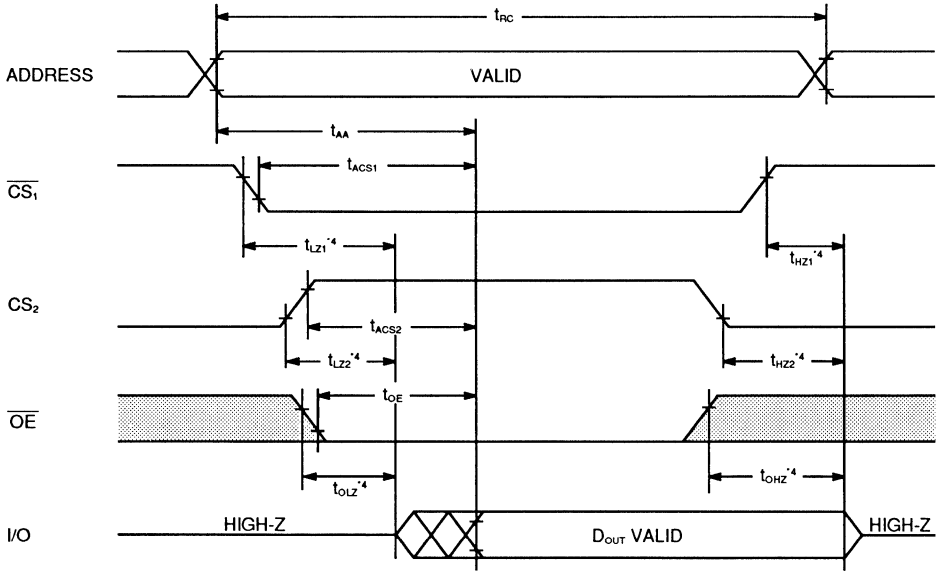
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE: ADDRESS CONTROLLED*2



READ CYCLE : $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.

*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

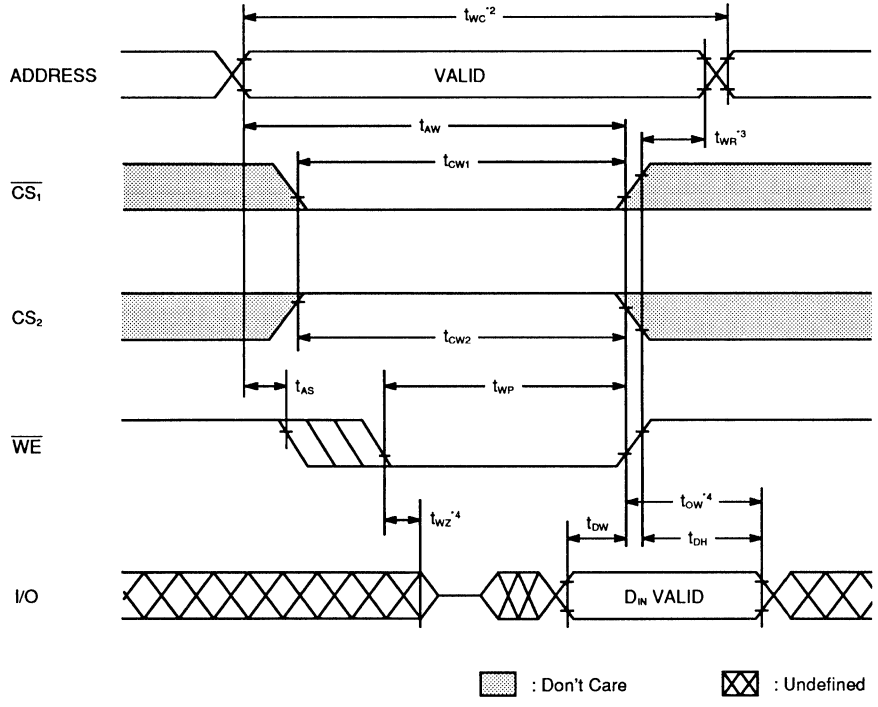
WRITE CYCLE*1

Parameter	Symbol	MB8289-25		MB8289-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM*1, *6, *7

WRITE CYCLE No. 1 ($\overline{WE}$ CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All Write Cycles are determined from the last address transition to the first address transition of next address.

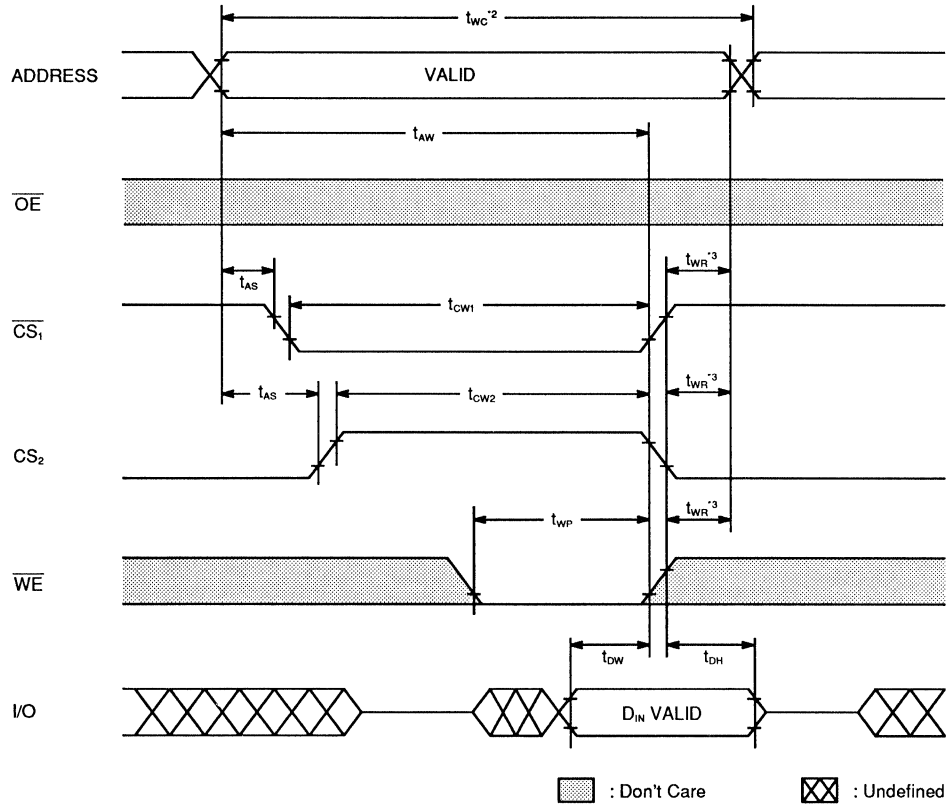
*3 t_{WR} is defined from the end point of Write Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1, *6, *7

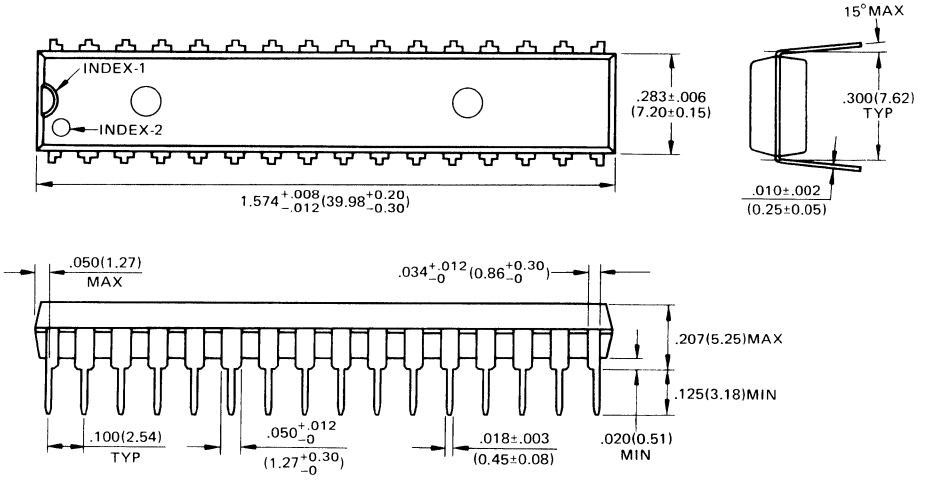
WRITE CYCLE: No. 2 ($\overline{CS_1}$, CS_2 CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.

PACKAGE DIMENSIONS

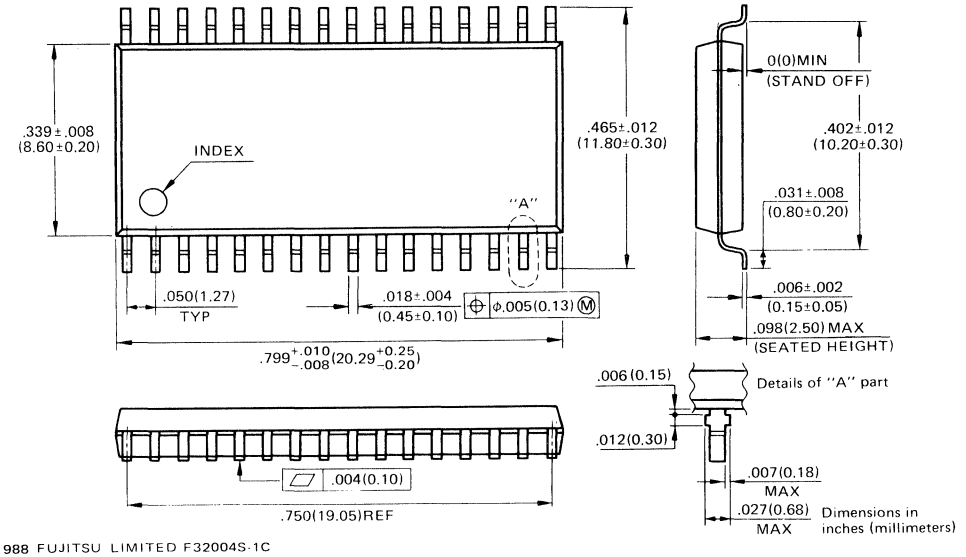
32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M02)



September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB8298-25/-35
CMOS 256K-BIT HIGH-SPEED SRAM

1

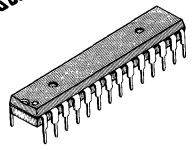
32K Words x 8 Bits High-Speed Static Random Access Memory

The Fujitsu MB8298 is a high-speed static random access memory organized as 32,768 words x 8 bits and fabricated with CMOS technology. To obtain a smaller chip size, the cells use NMOS transistors and resistors. The MB8298 is housed in 300 mil plastic DIP and SOJ packages and a 450-mil SOP package. All pins are TTL compatible and a single +5 V power supply is required.

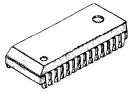
The MB8298 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB8298-25)
  $t_{AA} = t_{ACS} = 35$ ns max. (MB8298-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  27.5 mW max. (CMOS Standby)
- Single +5 V power Supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB8298-xxPSK
  SOP (450 mil) MB8298-xxPF
  SOJ (300 mil) MB8298-xxPJ

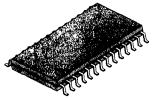
ADVANCE INFORMATION



Plastic Package
(DIP-28P-M04)

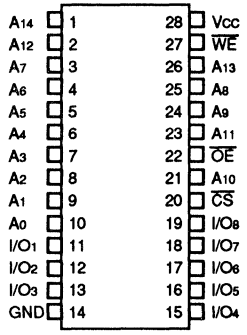


Plastic Package
(LCC-28P-M04)



Plastic Package
(FPT-28P-M02)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

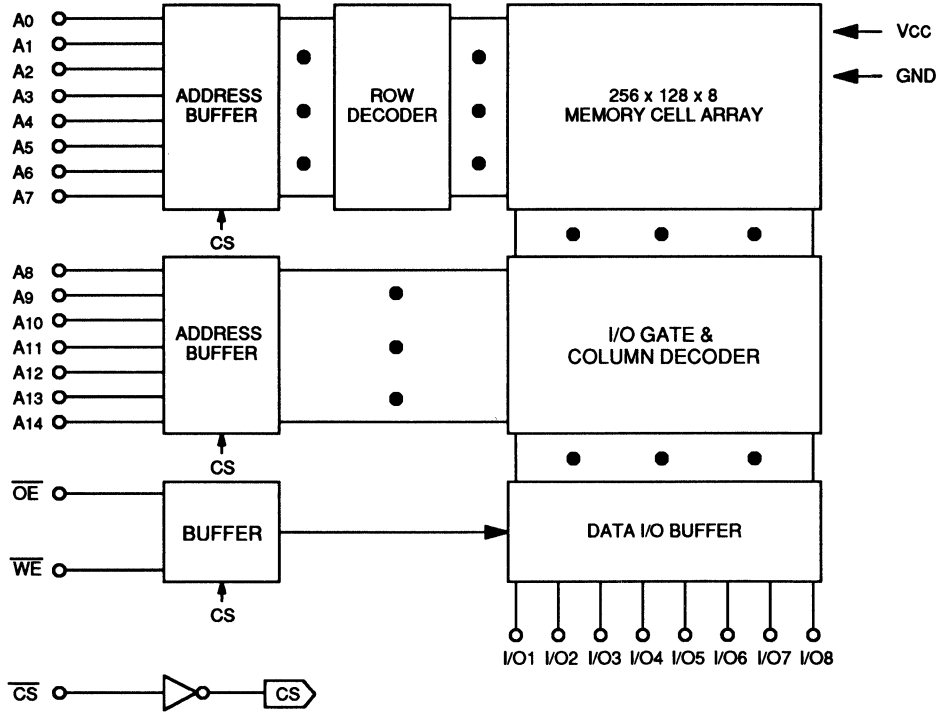
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB8298 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	STANDBY	ISB	HIGH-Z
L	H	H	DOUT DISABLE	ICC	HIGH-Z
L	H	L	READ	ICC	DOUT
L	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	CI1			8	pF
Input Capacitance (Other Input)	VIN = 0V	CI2			7	pF
I/O Capacitance	VI/O = 0V	CI/O			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

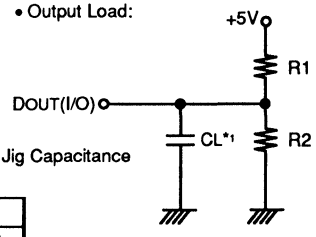
Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		ISB1	$\overline{CS} \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		5	mA
		ISB2	$VIN \leq 0.2V$ $\overline{CS} = VIH$		25	mA
Operating Supply Current	25ns	ICC	IOUT = 0mA, $\overline{CS}$ = VIL Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		ILI	VIN = 0V to VCC, VCC = Max.	–5	5	µA
Output Leakage Current		ILI/O	$\overline{CS}$ = VIH or $\overline{WE}$ = VIL or $\overline{OE}$ = VIH, VI/O = 0V to VCC	–5	5	µA
Input Low Voltage		VIL		–2.0*1	0.8	V
Input High Voltage		VIH		2.2	6.0	V
Output High Voltage		VOH	IOH = –4mA	2.4		V
Output Low Voltage		VOL	IOL = 8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20% of cycle time. (VIL min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
  Output :VOL=0.8V, VOH=2.2V

- Output Load:



*1 Including Scope and Jig Capacitance

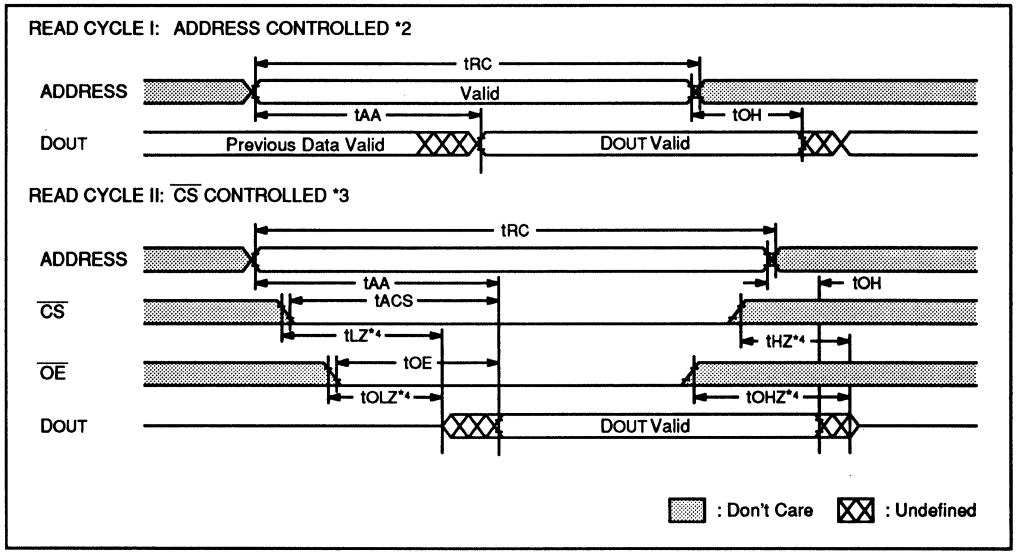
	R1	R2	CL	Parameters Measured
Load I	480kΩ	255Ω	30pF	except tLZ, tHZ, tWZ, tOW, tOLZ and tOHZ
Load II	480kΩ	255Ω	5pF	tLZ, tHZ, tWZ, tOW, tOLZ and tOHZ

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8298-25		MB8298-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
$\overline{CS}$ Access Time *3	tACS		25		35	ns
$\overline{OE}$ Access Time	tOE		12		14	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from $\overline{CS}$ *4	tLZ	5		8		ns
Output Low-Z from OE *4	tOLZ	2		3		ns
Output High-Z from $\overline{CS}$ *4	tHZ	1	15	1	15	ns
Output High-Z from $\overline{OE}$ *4	tOHZ	1	15	1	15	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}$ = VIL, and $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

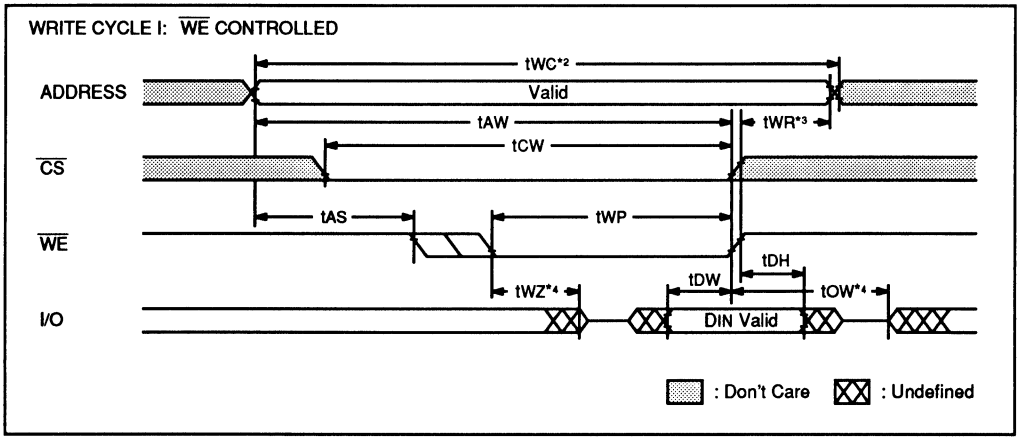
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1

Parameter	Symbol	MB8298-25		MB8298-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	tWC	25		35		ns
Address Valid to End of Write	tAW	18		28		ns
$\overline{CS}$ to End of Write	tCW	16		26		ns
Data Setup Time	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	15		20		ns
Write Recovery Time*3	tWR	0		0		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from $\overline{WE}$*4	tOW	0		0		ns
Output High-Z from $\overline{WE}$*4	tWZ	0	8	0	14	ns

WRITE CYCLE TIMING DIAGRAM *1

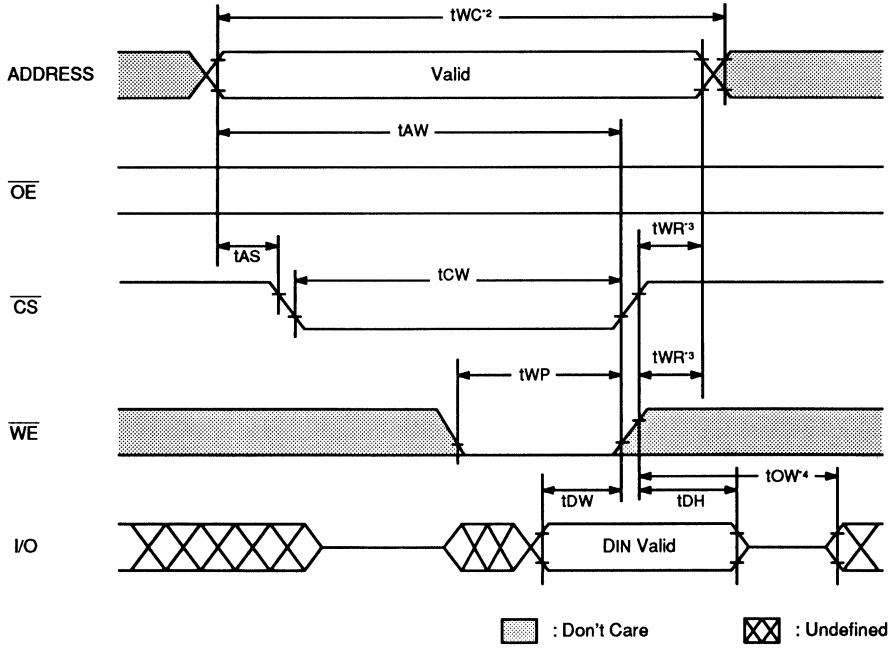


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE No. 2 ($\overline{CS}$ CONTROLLED)

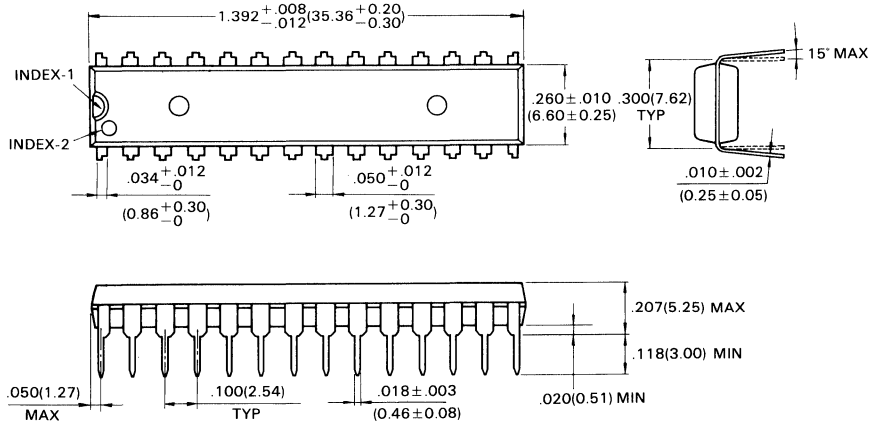


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

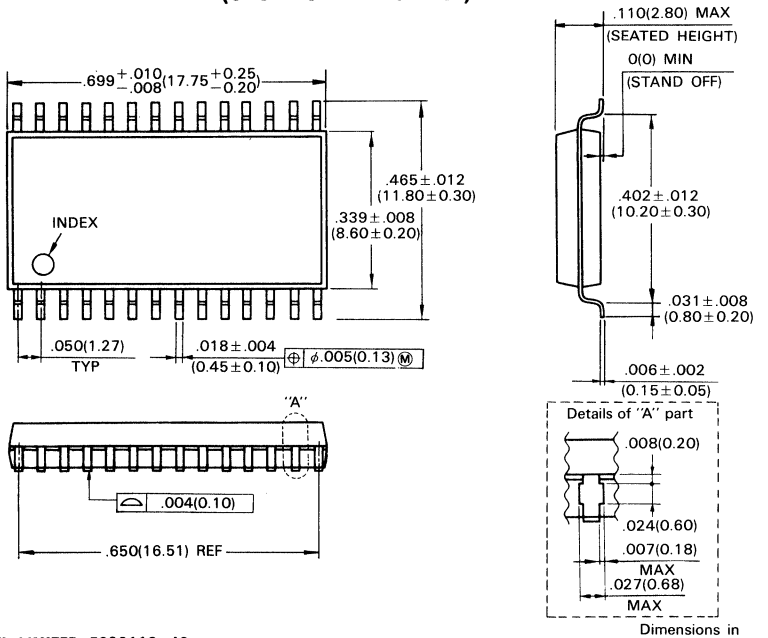


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PJ)

28-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-28P-M02)

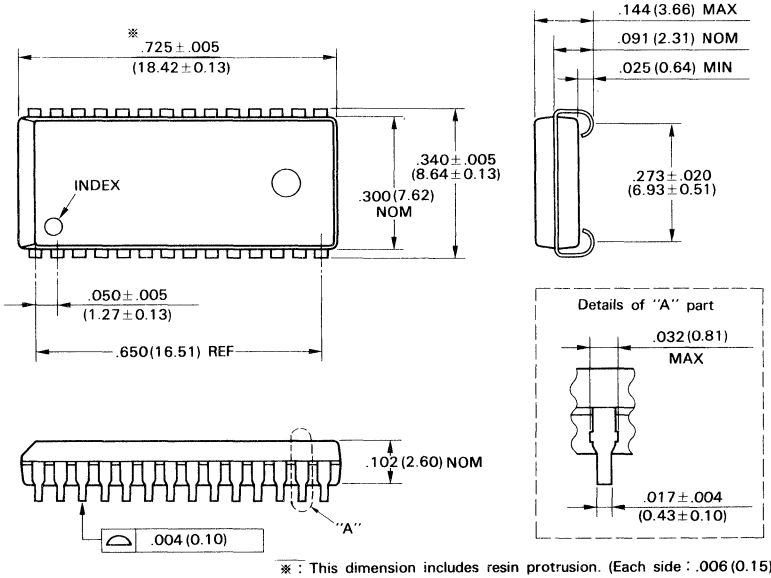


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in inches (millimeters)

1

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB8299-25/-35
CMOS 288K-BIT HIGH-SPEED BiCMOS SRAM

1

32K Words x 9 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB8299 is a high-speed static random access memory organized as 32,768 words x 9 bits and fabricated with CMOS technology. To obtain a smaller chip size, the cells use NMOS transistors and resistors. The MB8299 is housed in 300 mil plastic DIP and SOJ packages, and a 450 mil SOP package. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select (CS_1) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

The MB8299 offers low power dissipation, low cost, and high performance.

- Organization: 32,768 words x 9 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS}$ = 25 ns max. (MB8299-25)
  $t_{AA} = t_{ACS}$ = 35 ns max. (MB8299-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  27.5 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8299-xxPSK
  SOJ (300 mil) MB8299-xxPJ
  SOP (450 mil) MB8299-xxPF

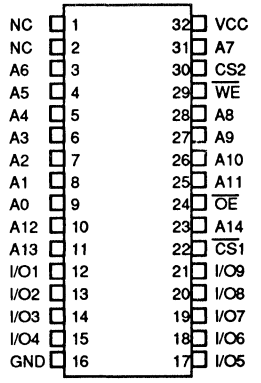
ADVANCE INFORMATION

Plastic Package
(DIP-32P-M02)

Plastic Package
(LCC-32P-M04)

Plastic Package
(FPT-32P-M02)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

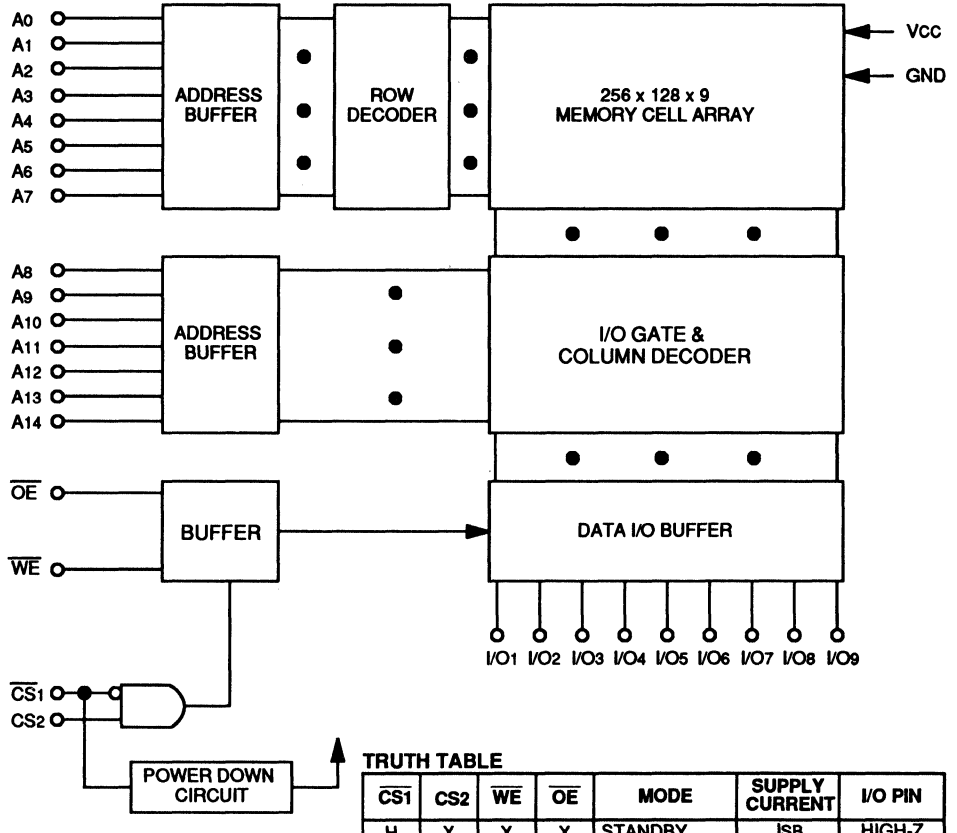
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 – MB8299 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	STANDBY	ISB	HIGH-Z
L	L	X	X	DESELECT	ICC	HIGH-Z
L	H	H	H	DOUT DESABLE	ICC	HIGH-Z
L	H	H	L	READ	ICC	DOUT
L	H	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS1}$, CS2 $\overline{OE}$, $\overline{WE}$)	VIN = 0V	CI1			8	pF
Input Capacitance (Other Input)	VIN = 0V	CI2			7	pF
I/O Capacitance	VI/O = 0V	CI/O			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

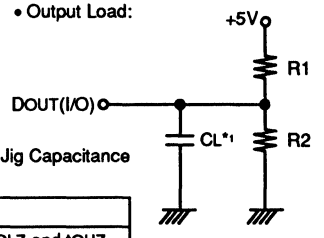
Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		ISB1	$\overline{CS1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		5	mA
		ISB2	$V_{IN} \leq 0.2V$ $\overline{CS1} = V_{IH}$		25	mA
Operating Supply Current	25ns	ICC	I_{OUT} = 0mA, $\overline{CS1} = V_{IL}$ Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		ILI	V_{IN} = 0V to VCC, VCC = Max.	–5	5	µA
Output Leakage Current		ILI/O	$\overline{CS1} = V_{IH}$ or $\overline{CS2} = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{I/O}$ = 0V to VCC	–5	5	µA
Input Low Voltage		VIL		–2.0*1	0.8	V
Input High Voltage		VIH		2.2	6.0	V
Output High Voltage		VOH	I_{OH} = –4mA	2.4		V
Output Low Voltage		VOL	I_{OL} = 8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20% of cycle time. (V_{IL} min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
  Output :VOL=0.8V, VOH=2.2V

- Output Load:



*1 Including Scope and Jig Capacitance

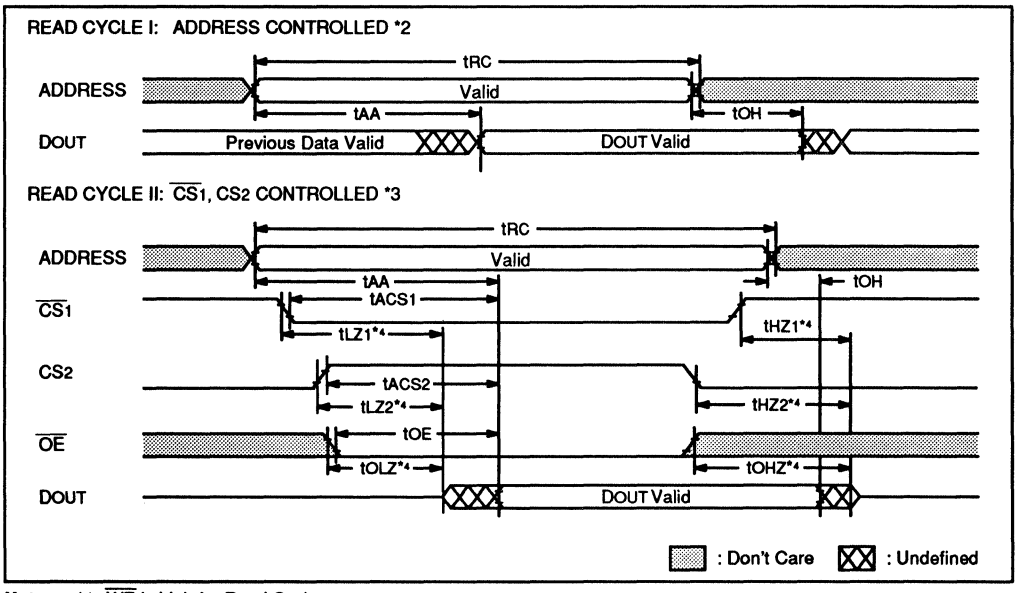
	R1	R2	CL	Parameters Measured
Load I	480kΩ	255Ω	30pF	except tLZ1, tLZ2, tHZ1, tHZ2, tWZ, tOW, tOLZ and tOHZ
Load II	480kΩ	255Ω	5pF	tLZ1, tLZ2, tHZ1, tHZ2, tWZ, tOW, tOLZ and tOHZ

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8299-25		MB8299-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
$\overline{CS1}$ Access Time *3	tACS1		25		35	ns
CS2 Access Time *3	tACS2		14		15	ns
$\overline{OE}$ Access Time	tOE		12		14	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from $\overline{CS1}$ *4	tLZ1	5		8		ns
Output Low-Z from CS2 *4	tLZ2	2		3		ns
Output Low-Z from $\overline{OE}$ *4	tOLZ	2		3		ns
Output High-Z from $\overline{CS1}$ *4	tHZ1	1	15	1	15	ns
Output High-Z from CS2 *4	tHZ2	1	15	1	15	ns
Output High-Z from $\overline{OE}$ *4	tOHZ	1	15	1	15	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS1}$ = VIL, CS2 = VIH and $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS1}$ transition low, CS2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

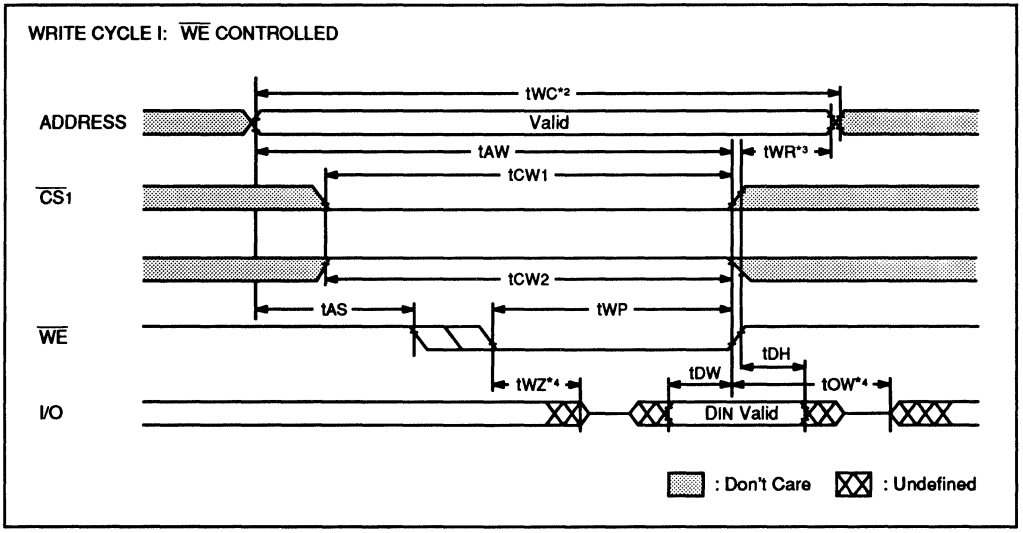
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1

Parameter	Symbol	MB8299-25		MB8299-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	tWC	25		35		ns
Address Valid to End of Write	tAW	18		28		ns
$\overline{CS1}$ to End of Write	tCW1	16		26		ns
CS2 to End of Write	tCW2	13		20		ns
Data Setup Time	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	15		20		ns
Write Recovery Time*3	tWR	0		0		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from $\overline{WE}$*4	tOW	0		0		ns
Output High-Z from $\overline{WE}$*4	tWZ	0	8	0	14	ns

WRITE CYCLE TIMING DIAGRAM *1

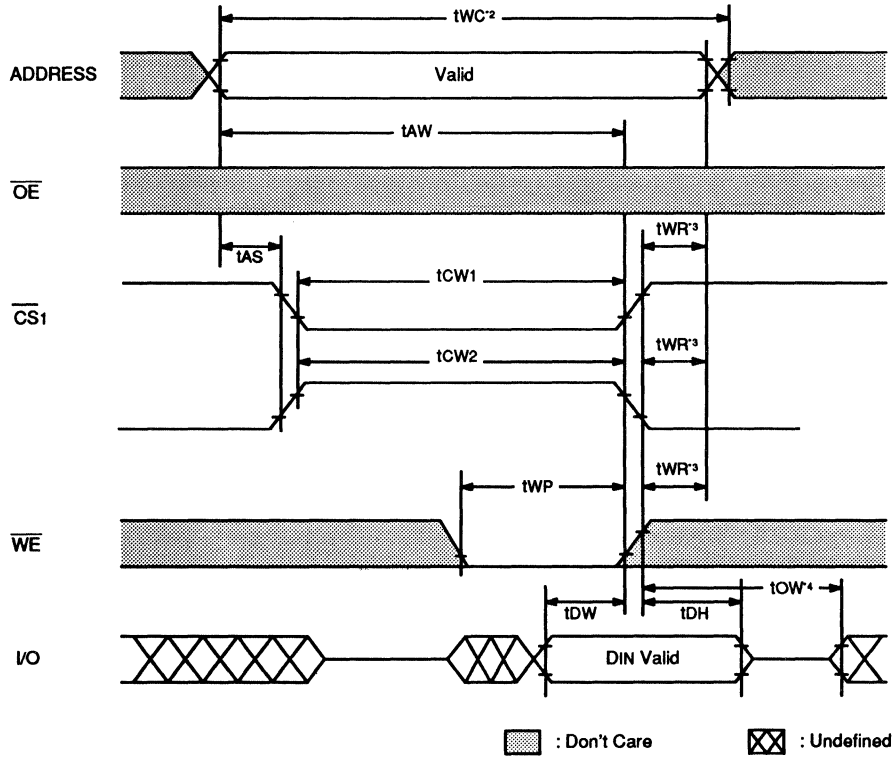


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

1

WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE No. II: $\overline{CS}_1$, CS_2 CONTROLLED

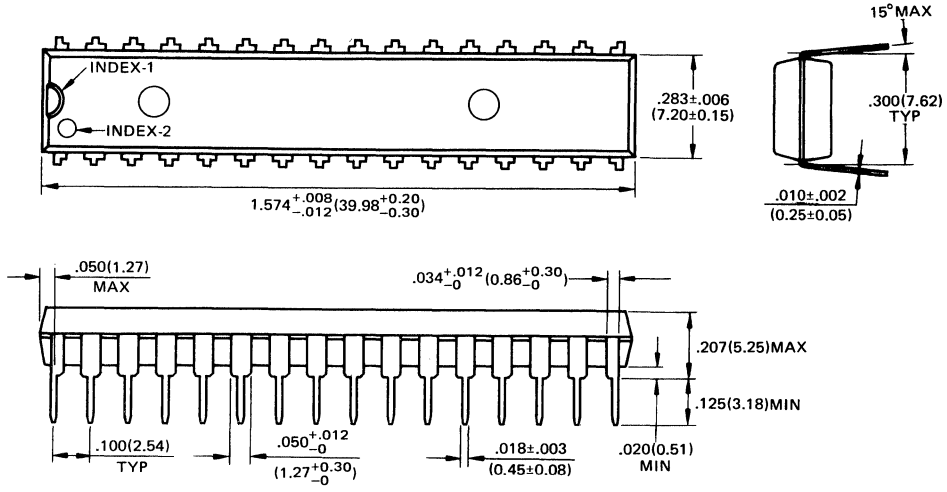


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)

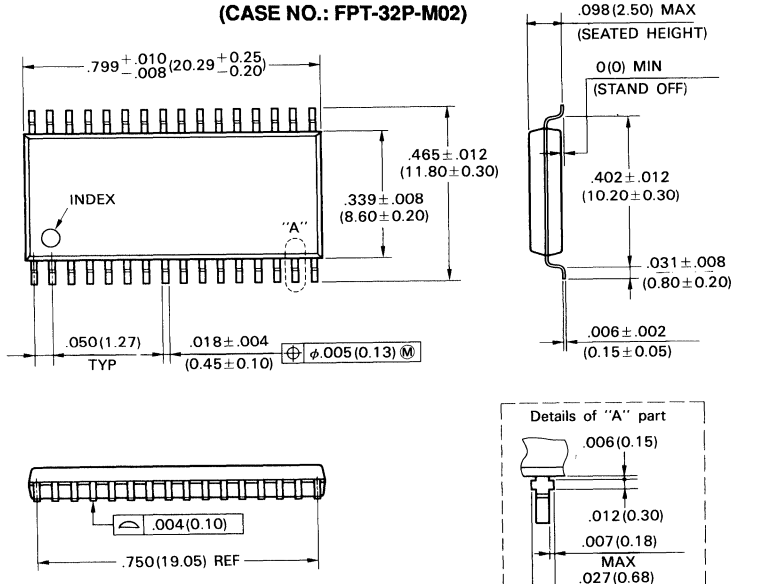


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PF)

32-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-32P-M02)

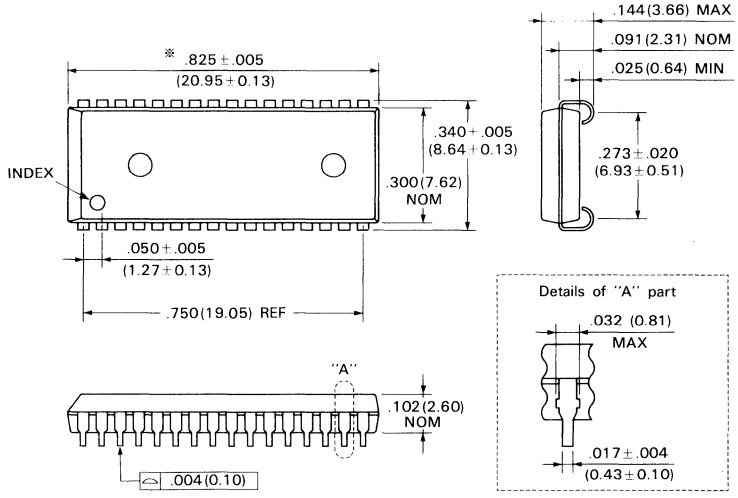


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PJ)

32-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-32P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

1

1

Section 2

High-Speed BiCMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity (Organization)	Package Options
2–3	*High-Speed BiCMOS SRAMs Product Cross Reference*			
2–5	MB82B001–25 –35	25 35	1048576 bits (1048576 x 1)	28-pin Plastic SOJ
2–13	MB82B005–25 –35	25 30	1048576 bits (262144 x 4 /OE)	28-pin Plastic SOJ
2–21	MB82B006–25 –35	25 35	1048576 bits (262144 x 4) Separate I/O	32-pin Plastic SOJ
2–29	MB82B78–15 –20	15 20	65536 bits (8192 x 8)	28-pin Plastic DIP, SOP, SOJ
2–39	MB82B79–15 –20	15 20	73728 bits (8192 x 9)	28-pin Plastic DIP, SOP, SOJ
2–49	MB82B81–15 –20	15 20	262144 bits (262144 x 1)	24-pin Plastic DIP, SOJ
2–57	MB82B84–15 –20	15 20	262144 bits (65536 x 4)	24-pin Plastic DIP, SOJ
2–65	MB82B85–15 –20	15 20	262144 bits (65536 x 4 /OE)	28-pin Plastic DIP, SOJ
2–75	MB82B88–15 –20	15 20	262144 bits (32768 x 8)	28-pin Plastic DIP, SOJ
2–77	MB82B89–15 –20	15 20	294912 bits (32768 x 9)	32-pin Plastic DIP, SOJ
2–79	MB82B008–25	25	1048576 bits (131072 x 8)	32-pin Plastic SOJ
2–81	MB82B009–25	25	1179648 bits (131072 x 9)	36-pin Plastic SOJ
2–83	MB82B201–25 –35	25 35	4194304 bits (4194304 x 1) or (1048576 x 4)	32-pin Plastic SOJ
2–85	MB82B206–25 –35	25 35	4194304 bits (1048576 x 4) Separate I/O	36-pin Plastic SOJ

2

High-Speed BiCMOS SRAMs Product Cross Reference

1M Static RAMs

Vendors	Fujitsu Part Numbers				
	MB82B001 (1M x 1)	MB82B005 (256K x 4)	MB82B006 (256K x 4)	MB82B008 (128K x 8)	M82B009 (128K x 9)
Hitachi	HM621100A	HM624256/A	HM624257		
Micron	MT5C1001	MT5C1005			
Mitsubishi	M5M51001	M5M51004			
Samsung	KM611001				
Sony					CXK581020

64K Static RAMs

Vendors	Fujitsu Part Numbers	
	MB82B78 (8K x 8)	MB82B79 (8K x 9)
Cypress	CY7B185	
Hitachi		
IDT	IDT7164	IDT7169
Micron	MT5C6408	
Mitsubishi	M5M5178A	M5M5179A
Motorola	MCM6264	MCM6265
Performance	P4C163	P4C164
Samsung		
Sony	CXK5863A	
Toshiba	TC5588	TC5589

256K Static RAMs

Vendors	Fujitsu Part Numbers				
	MB82B81 (256K x 1)	MB82B84 (64K x 4)	MB82B85 (64K x 4/OE)	MB82B88 (32K x 8/OE)	MB82B89 (32K x 9/OE)
Cypress	CY7C197	CY7C194	CY7C196	CY7C199	
Hitachi	HM6707/A	HM6708/A	HM6709/A		
IDT	IDT71257	IDT71258	IDT61298	IDT71256	IDT71259
Micron	MT5C2561	MT5C2564	MT5C2565	MT5C2568	
Mitsubishi	M5M5257B	M5M5258B			
Motorola	MCM6207	MCM6208	MCM6209	MCM6206	MCM6205
Performance	P4C1257	P4C1258	P4C1298	P4C1256	
Sony				CXK58258	CXK58289
Toshiba		TC55464	TC55465	TC55328	TC55329

2

September 1990
Edition 2.0

FUJITSU

DATA SHEET

MB82B001-25/-35
1M-BIT HIGH-SPEED BiCMOS SRAM

1M Words x 1 Bit High-Speed BiCMOS Static Random Access Memory

The Fujitsu MB82B001 is a 1,048,576 words x 1 bit static random access memory fabricated with a BiCMOS process technology. For lower power dissipation and higher speed, peripheral circuits are fabricated with BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors.

The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

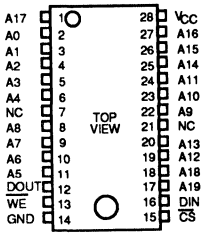
The MB82B001 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 1,048,576 words x 1 bit
- Static operation: no clock or refresh required
- Access time: 25 ns max. (MB82B001-25)
  35 ns max. (MB82B001-35)
- Single +5 V power supply ±10% tolerance
  120 mA max. (Active operation)
  5 mA max. (Standby, CMOS level)
  25 mA max. (Standby, TTL level)
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- 28-pin Plastic Package:
  SOJ (400 mil) MB82B001-xxPJ

PRELIMINARY

PLASTIC PACKAGE
LCC–28P–M05

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

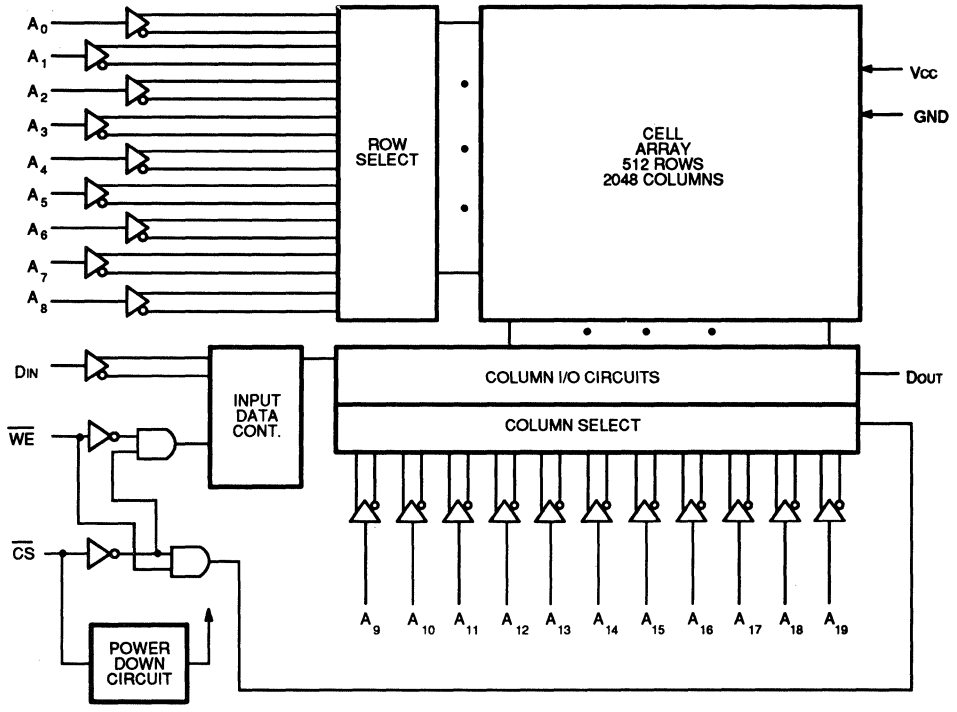
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	–3.5 to +7.0	V
Output Voltage on any pin with respect to GND	V_{OUT}	–0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB82B001 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	High-Z	Active
L	H	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A9	Address Input	$\overline{WE}$	Write Enable
D_{IN}	Data Input	V_{CC}	Power Supply(±10%)
D_{OUT}	Data Output	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC} V_{CC} = Max.	I_{LI}	–1		1	µA
Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = Max.	I_{LO}	–1		1	µA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	I_{CC1}		50	80	mA
	V_{CC} = Max., $\overline{CS}$ = V_{IL} Cycle = Min., I_{OUT} = 0mA	I_{CC2}		80	120	
Standby Current	V_{CC} = Min. to Max. $\overline{CS}$ ≥ V_{CC} –0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	I_{SB1}		2	15	mA
	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}		10	25	
Output Low Voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4			V
Peak Power on Current *1	V_{CC} = 0V to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	I_{PO}			50	mA
Input Low Voltage		V_{IL}	–0.5 *2		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V

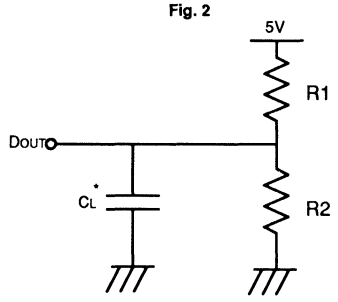
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



*Including Scope and Jig capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tLZ, tHZ, tOW and tWZ

AC CHARACTERISTICS

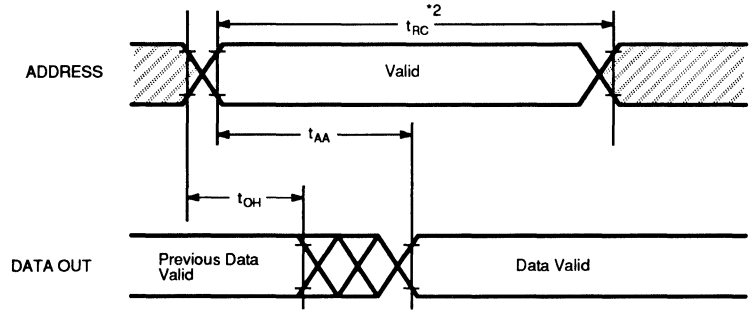
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	tRC	25		35		ns
Address Access Time *3	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	5		5		ns
Chip Selection to Output in Low-Z *5 *6	tLZ	5		5		ns
Chip Deselection to Output in High-Z *5 *6	tHZ	2	15	2	15	ns
Chip Selection to Power Up time	tPU	0		0		ns
Chip Deselection to Power Down	tPD		20		30	ns

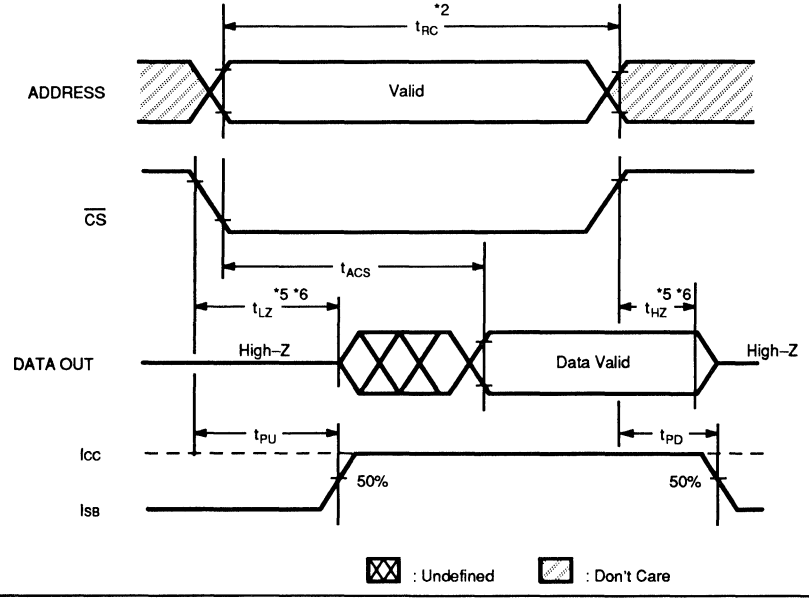
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

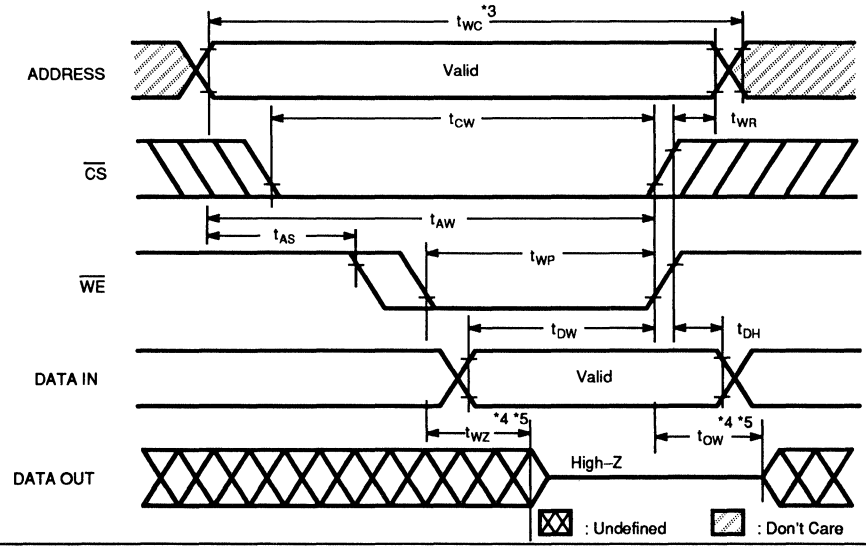
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B001-25		MB82B001-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	10		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

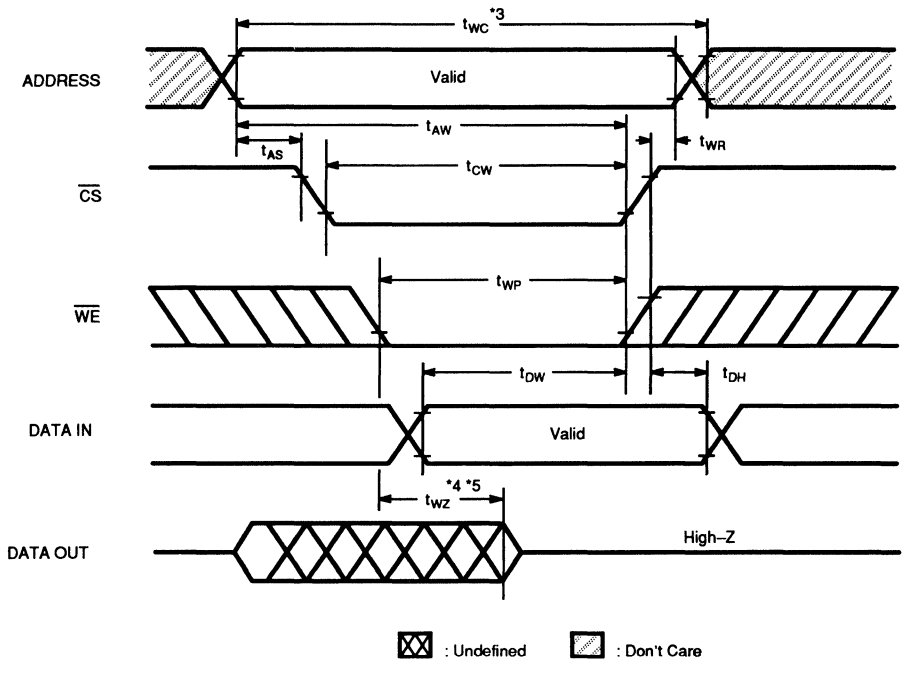
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

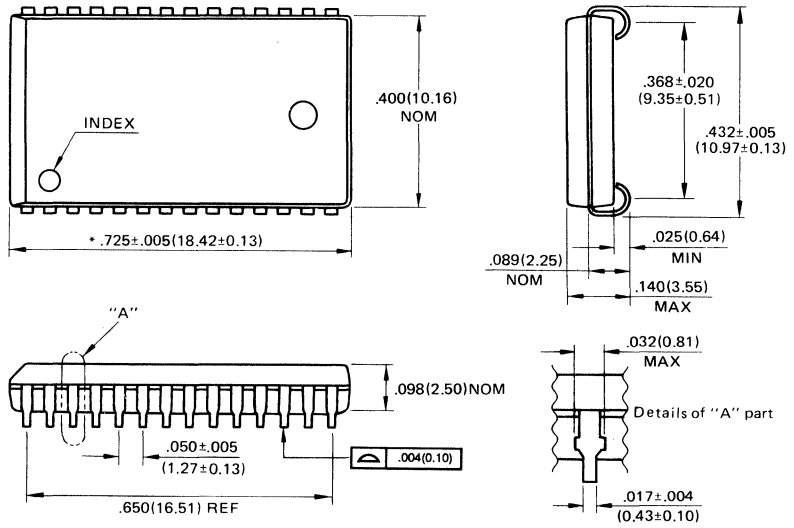


*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

2

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)



* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

September 1990
Edition 2.0

FUJITSU

DATA SHEET

MB82B005-25/-35
1M-BIT HIGH-SPEED BiCMOS SRAM

256K Words x 4 Bits High-Speed BiCMOS Static Random Access Memory

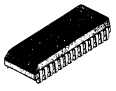
The Fujitsu MB82B005 is a 262,144 words x 4 bits static random access memory fabricated with a BiCMOS process technology. For lower power dissipation and higher speed, peripheral circuits use BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors.

The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required. The MB82B005 is housed in a 400 mil plastic small outline J-lead (SOJ) package.

The MB82B005 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

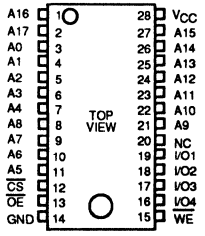
- Organization: 262,144 words x 4 bit
- Static operation: no clock or refresh required
- Access time: 25 ns max. (MB82B005-25)
  35 ns max. (MB82B005-35)
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. (Standby, CMOS level)
  25 mA max. (Standby, TTL level)
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- 28-pin Plastic Package:
  SOJ (400 mil) MB82B005-xxPJ

PRELIMINARY



PLASTIC PACKAGE
LCC–28P–M05

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

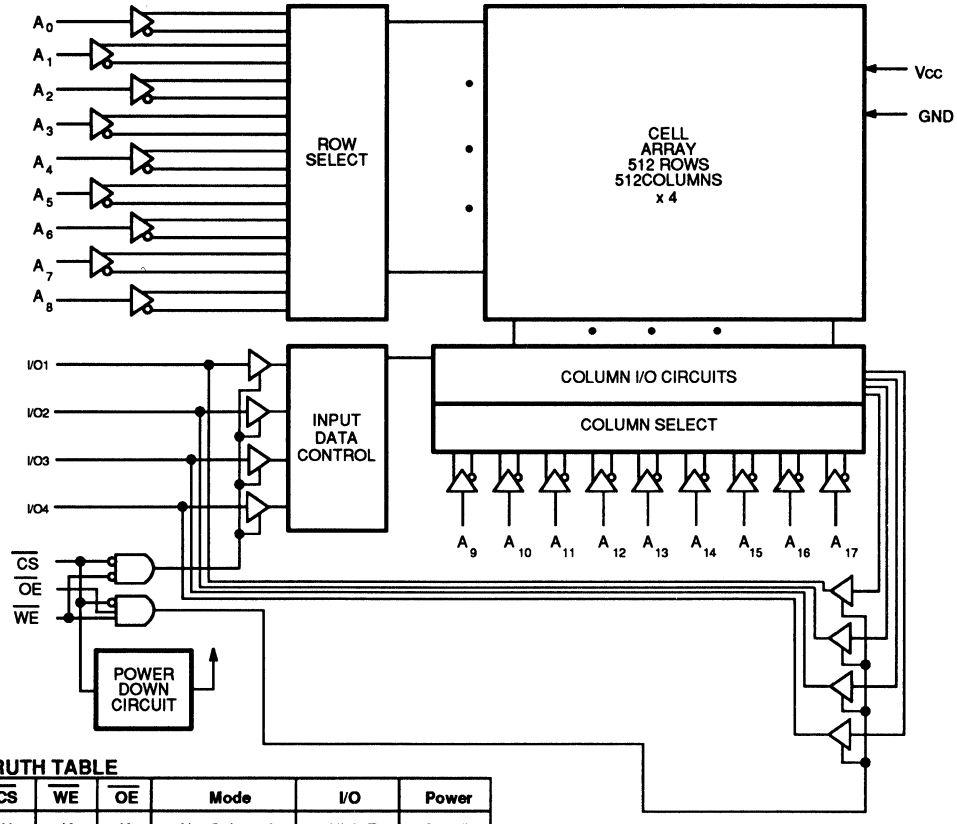
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB82B005 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Desable	High-Z	Active
L	L	X	Writte	DIN	Active
L	H	L	Read	DOUT	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O4	Data Input/Output	Vcc	Power Supply(±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	VIN = 0V to Vcc Vcc = Max.	ILI	–1		1	µA
Output Leakage Current	$\overline{CS}$ = VIH, or $\overline{OE}$=VIH VOUT = 0V to Vcc Vcc = Max.	ILO	–1		1	µA
Active Supply Current	$\overline{CS}$ = VIL, IOUT = 0mA Vcc = Max., VIN = VIL or VIH	ICC1		50	80	mA
	Vcc = Max., $\overline{CS}$ = VIL Cycle = Min., IOUT = 0mA	ICC2		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ ≥ Vcc –0.2V VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V	ISB1		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = VIH	ISB2		10	25	
Output Low Voltage	IOL = 8 mA	VOL			0.4	V
Output High Voltage	IOH = –4 mA	VOH	2.4			V
Peak Power on Current *1	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or VIH Min.	IPO			50	mA
Input Low Voltage		VIL	–0.5 *2		0.8	V
Input High Voltage		VIH	2.2		6.0	V

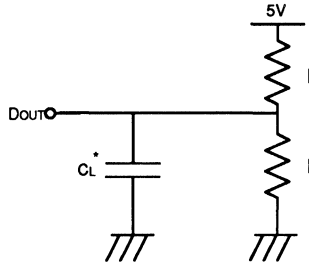
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (0.8V to 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tCLZ, tCHZ, tOLZ, tOHZ, tOW and tWZ

*Including Scope and Jig capacitance

AC CHARACTERISTICS

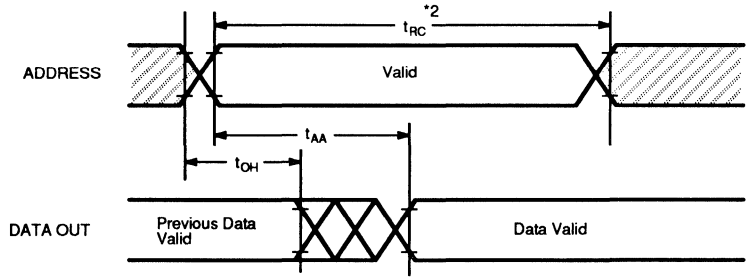
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	t_{RC}	25		35		ns
Address Access Time *3	t_{AA}		25		35	ns
Chip Select Access Time *4	t_{ACS}		25		35	ns
Output Enable Access Time	t_{OE}		10		15	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Chip Selection to Output in Low-Z *5 *6	t_{CLZ}	5		5		ns
Chip Selection to Output in High-Z *5 *6	t_{CHZ}	2	15	2	15	ns
Output Enable to Output in Low-Z *5 *6	t_{OLZ}	0		0		ns
Output Enable to Output in High-Z *5 *6	t_{OHZ}	0	15	0	15	ns
Chip Selection to Power Up time	t_{PU}	0		0		ns
Chip Deselection to Power Down	t_{PD}		20		30	ns

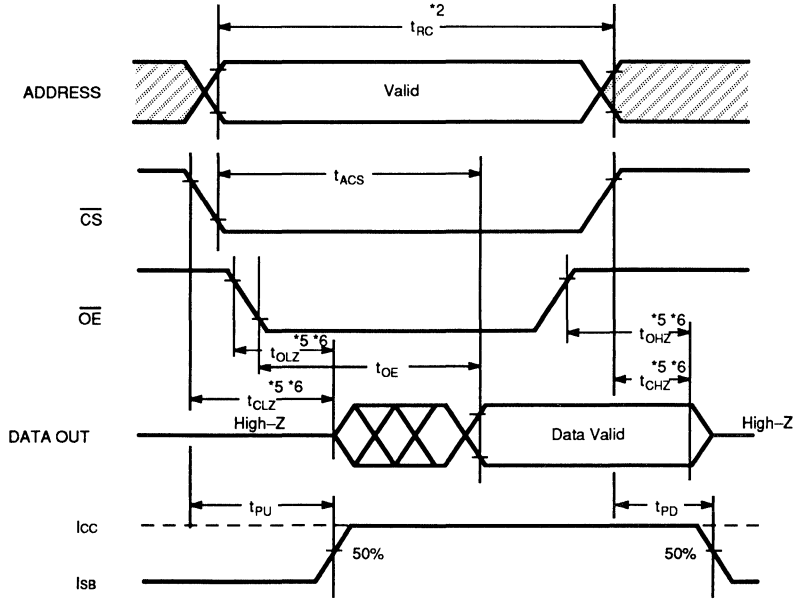
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=V_{IL} $\overline{OE}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



: Undefined : Don't Care

*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL, $\overline{OE}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

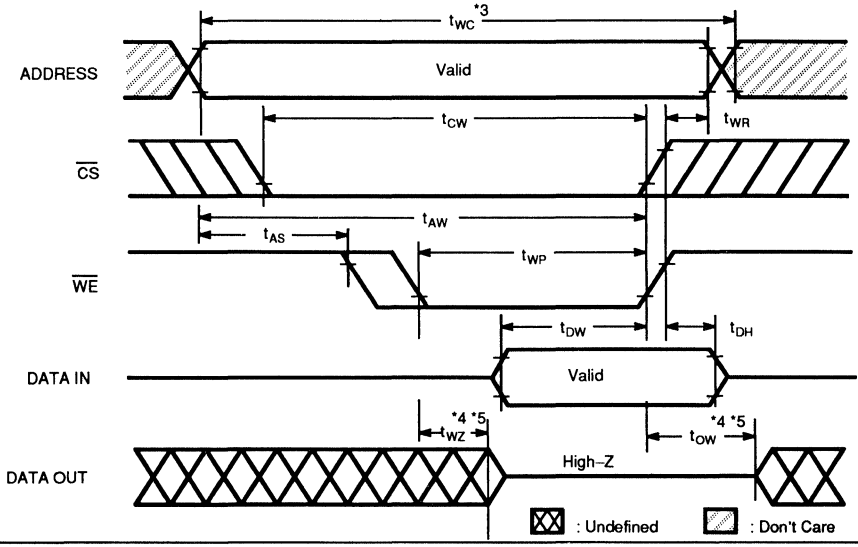
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B005-25		MB82B005-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	8		12		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	8	0	14	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

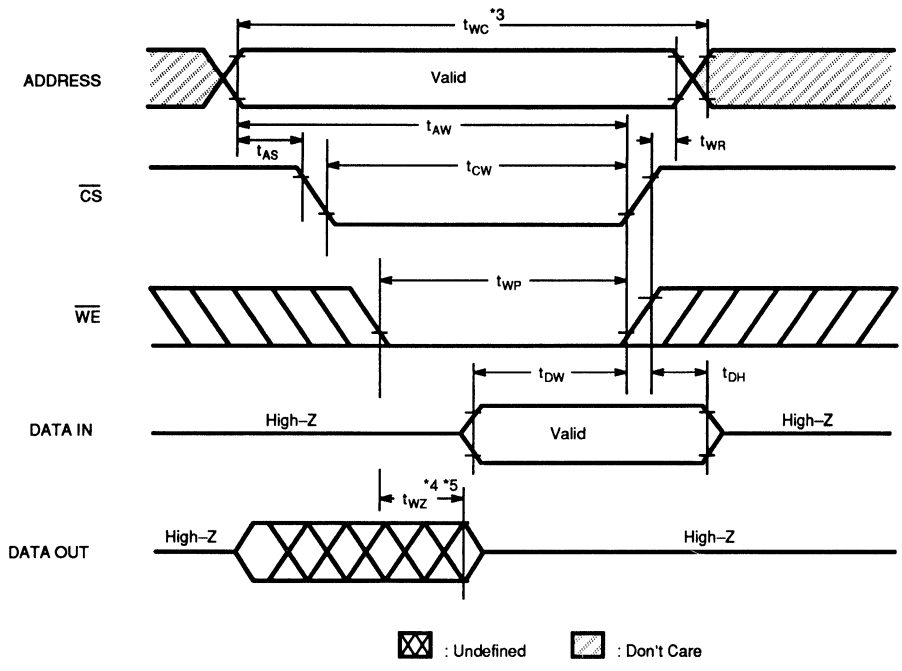
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

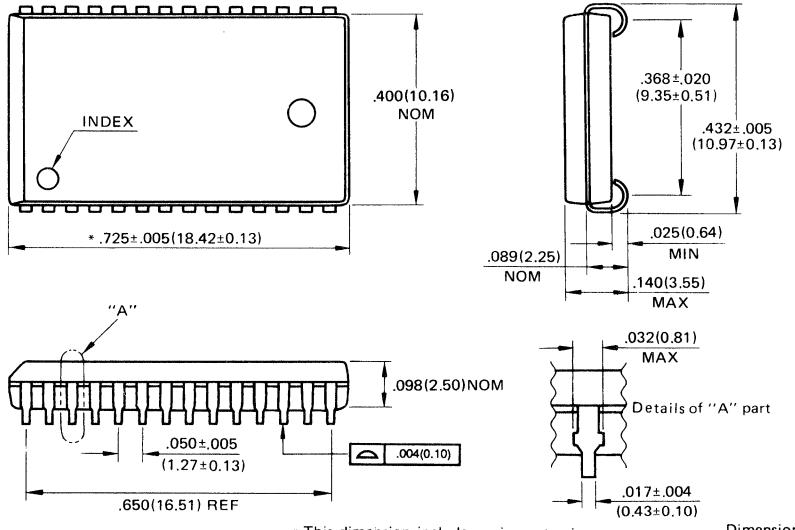
WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If CS goes high simultaneously with WE high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-28P-M05)



* This dimension includes resin protrusion.
(Each side:.006(0.15)MAX.)

Dimensions in
inches (millimeters)

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB82B006-25/-35
1M BIT HIGH-SPEED BiCMOS SRAM

256K Words x 4 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB82B006 is a static random access memory organized as 262,144 words by 4 bits and fabricated with BiCMOS process technology. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required. The MB82B006 is housed in a 400 mil plastic small outline J-lead (SOJ) package.

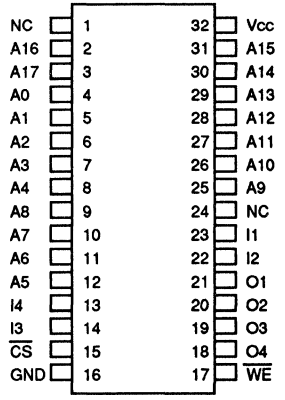
The MB82B006 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 262,144 words x 4 bits
- Static operation: no clocks or refresh required
- Access time: 25 ns max. (MB82B006-25)
  35 ns max. (MB82B006-35)
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active Operation)
  15 mA max. (CMOS Standby)
  25 mA max. (TTL Standby)
- Separate data inputs and outputs
- TTL compatible inputs and outputs
- Chip select for simplified memory expansion, automatic power drain
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Package:
  SOJ (400 mil) MB82B006-xxPJ

ADVANCE INFORMATION

Plastic Package (LCC-32P-M03)

Pin Assignment (TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

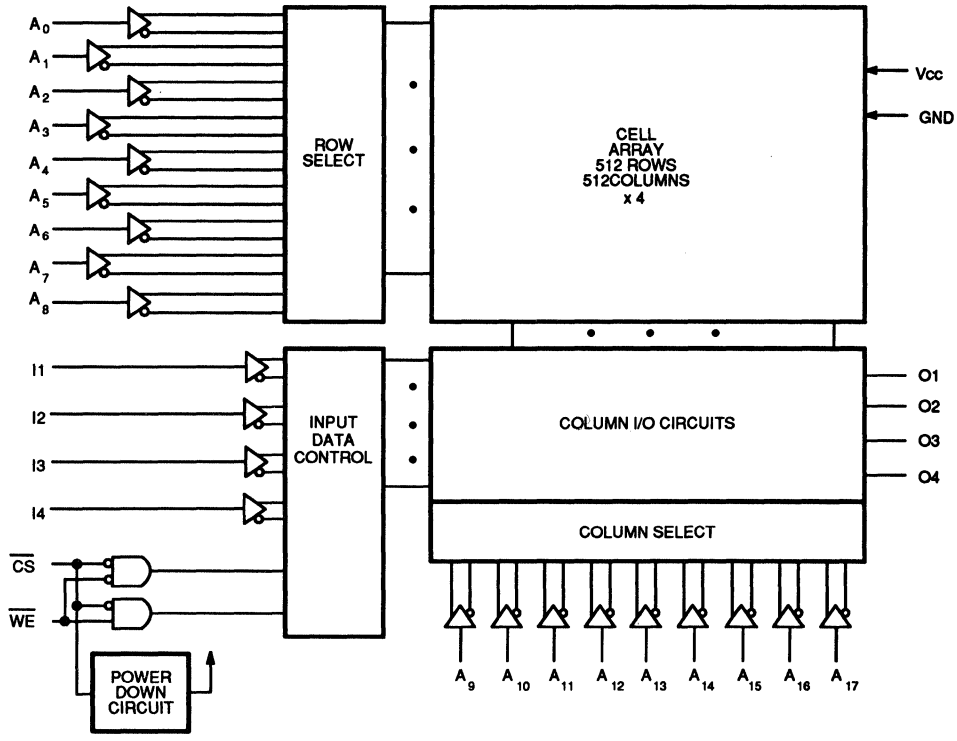
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−0.5 to +7	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB82B006 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High-Z	Standby
L	H	Read	DOUT	Active
L	L	Write	High–Z	Active

Legend: H = High level
L = Low level
X = Don't Care

CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0 V)	CIN		6	pF
$\overline{CS}$ Capacitance ($V_{\overline{CS}}$ = 0 V)	$C_{\overline{CS}}$		7	pF
Output Capacitance (VOUT = 0 V)	COUT		7	pF

PIN DISCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A17	Address Input	$\overline{WE}$	Write Enable
I1 to I4	Data Input	Vcc	Power Supply(±10%)
O1 to O4	Data Output	GND	Ground
$\overline{CS}$	Chip Select	NC	No Connect

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input Leakage Current	V_{IN} = 0V to Vcc Vcc = Max.	I_{LI}	–1		1	µA
Output Leakage Current	$\overline{CS}$ = V_{IH} V_{OUT} = 0V to Vcc Vcc = Max.	I_{LO}	–1		1	µA
Active Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA Vcc = Max., V_{IN} = V_{IL} or V_{IH}	I_{CC1}		50	80	mA
	Vcc = Max., $\overline{CS}$ = V_{IL} Cycle = Min., I_{OUT} = 0mA	I_{CC2}		80	120	
Standby Current	Vcc = Min. to Max. $\overline{CS}$ ≥ Vcc –0.2V V_{IN} ≥ Vcc – 0.2V or V_{IN} ≤ 0.2V	I_{SB1}		2	15	mA
	Vcc = Min. to Max. $\overline{CS}$ = V_{IH}	I_{SB2}		10	25	
Output Low Voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output High Voltage	I_{OH} = –4 mA	V_{OH}	2.4			V
Peak Power on Current *1	Vcc = 0V to Vcc Min. $\overline{CS}$ = Lower of Vcc or V_{IH} Min.	I_{PO}			50	mA
Input Low Voltage		V_{IL}	–0.5 *2		0.8	V
Input High Voltage		V_{IH}	2.2		6.0	V

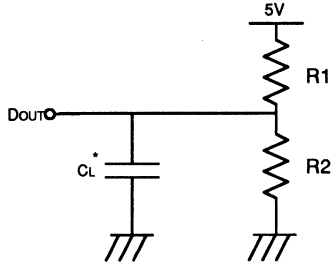
*1 A pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches Icc active.

*2 –3.0 V Min. for pulse width less than 20 ns.

2

AC TEST CONDITIONS

- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 3 ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8, V_{IH} = 2.2 V
  Output: V_{OL} = 0.8, V_{OH} = 2.2 V
- Output Load: **Fig. 2**



	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30pF	except tLZ, tHZ, tOW and tWZ
Load II	480Ω	255Ω	5pF	tLZ, tHZ, tOW and tWZ

*Including Scope and Jig capacitance

AC CHARACTERISTICS

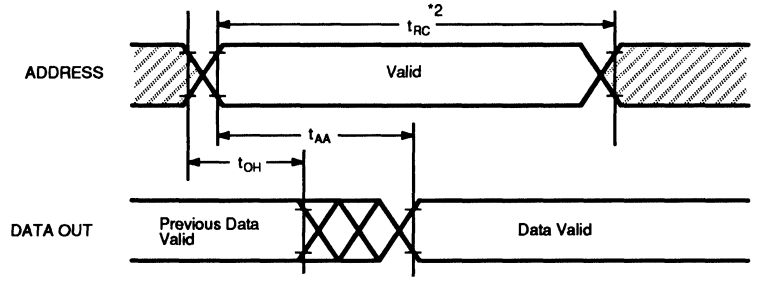
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B006-25		MB82B006-35		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE *1						
Read Cycle Time *2	tRC	25		35		ns
Address Access Time *3	tAA		25		35	ns
Chip Select Access Time *4	tACS		25		35	ns
Output Hold from Address Change	tOH	5		5		ns
Chip Selection to Output in Low-Z *5 *6	tLZ	5		5		ns
Chip Selection to Output in High-Z *5 *6	tHZ	2	15	2	15	ns
Chip Selection to Power Up time	tPU	0		0		ns
Chip Deselection to Power Down	tPD		20		30	ns

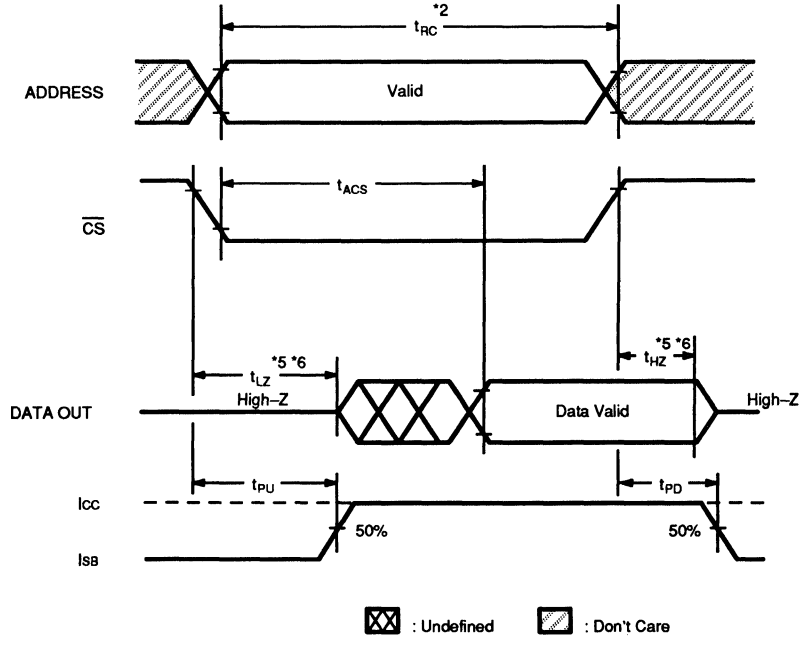
*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM

READ CYCLE: ADDRESS CONTROLLED *1 *3



READ CYCLE: $\overline{CS}$ CONTROLLED *1 *4



*1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycles are determined from the last address transition to the first address transition of next cycle.
*3 Device is continuously selected, $\overline{CS}$=VIL.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.
*6 This parameter is measured with specified Load II in Fig. 2.

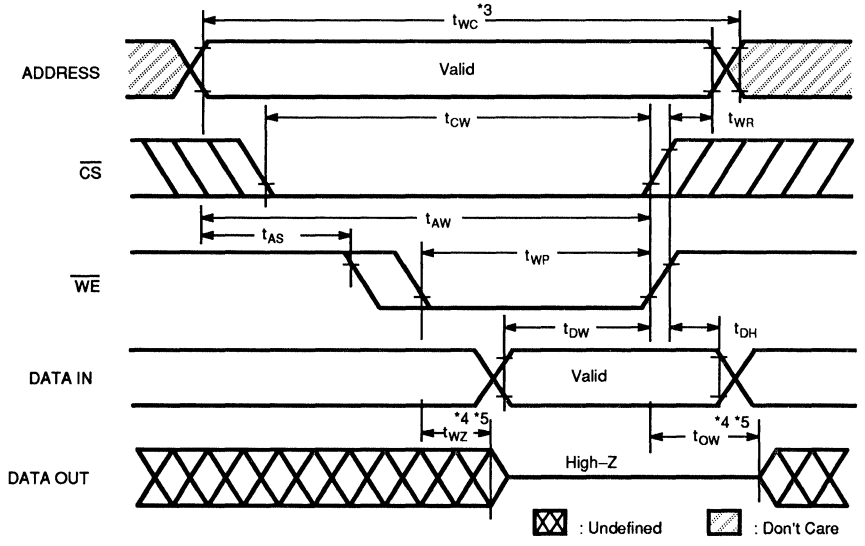
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB82B006-25		MB82B006-35		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE *1 *2						
Write Cycle Time *3	t_{WC}	25		35		ns
Chip Selection to End of Write	t_{CW}	16		26		ns
Address Valid to End of Write	t_{AW}	18		28		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Data Valid to End of Write	t_{DW}	10		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output in High-Z *4 *5	t_{WZ}	0	10	0	15	ns
Output Active from End of Write *4 *5	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM

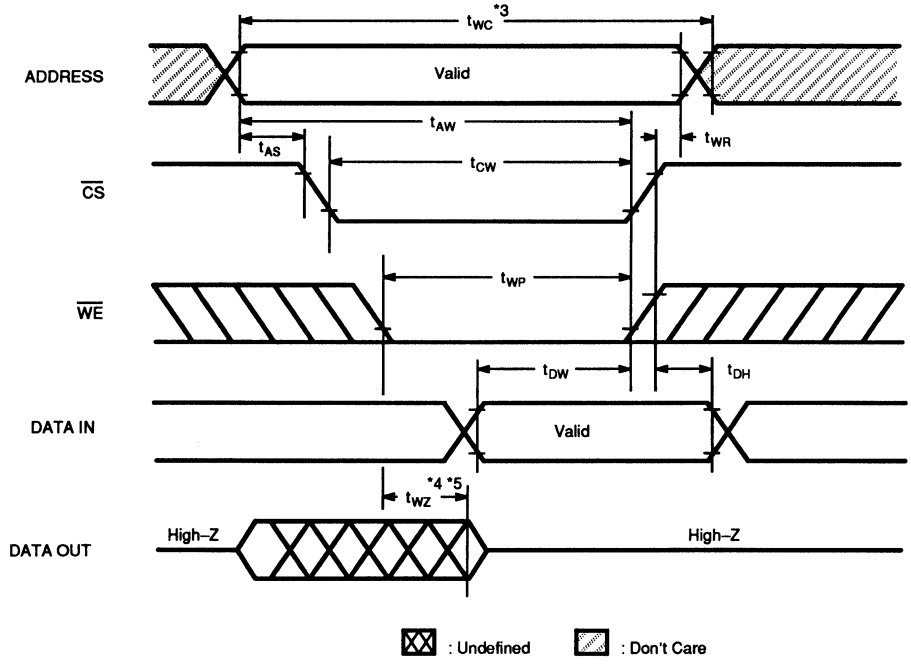
WRITE CYCLE: $\overline{WE}$ CONTROLLED *1 *2



*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE: $\overline{CS}$ CONTROLLED *1 *2

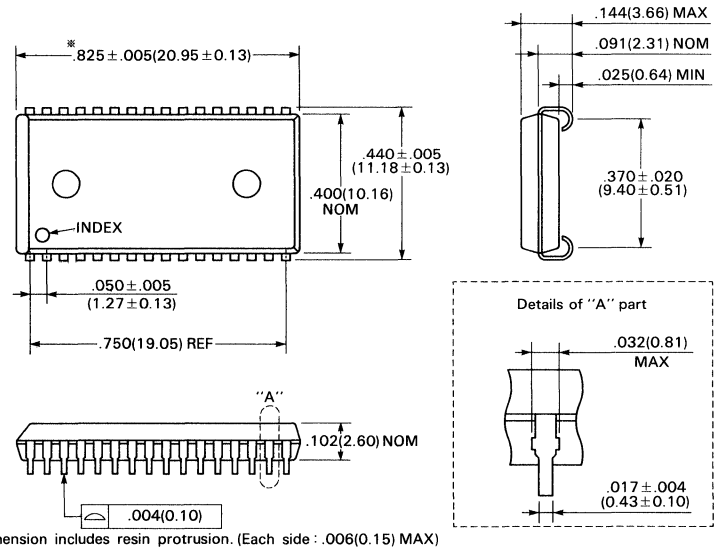


*1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycles are determined from the last address transition to the first address transition of next cycle.
*4 Transition is measured at the point of ±500mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: PJ)

32–LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-32P–M03)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB82B78-15/-20
64K-BIT HIGH-SPEED BiCMOS SRAM

8K Words x 8 Bits High-Speed Static Random Access Memory

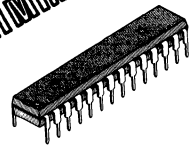
The Fujitsu MB82B78 is a static random access memory organized as 8,192 words x 8 bits and fabricated with CMOS silicon gate process. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B78 is housed in 300 mil plastic DIP and SOJ packages, and a 450 mil plastic SOP package. The memory uses asynchronous circuitry and requires +5 V power supply. All pins are TTL compatible.

The MB82B78 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

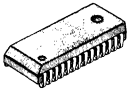
- Organization: 8,192 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time:
  $t_{AA} = t_{ACS1}$ = 15 ns max., $t_{ACS2} = t_{OE}$ = 8 ns max (MB82B78-15)
  $t_{AA} = t_{ACS1}$ = 20 ns max., $t_{ACS2} = t_{OE}$ = 10 ns max (MB82B78-20)
- Single 5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Operating)
  30 mA max. (TTL Standby)
  15 mA max. (CMOS Standby)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Three-state outputs
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB82B78-xxPSK
  SOP (450 mil) MB82B78-xxPF
  SOJ (300 mil) MB82B78-xxPJ

PRELIMINARY



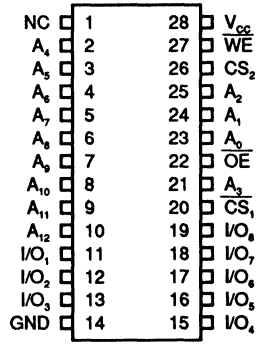
Plastic Package (DIP-28P-M04)

Plastic Package (FPT-28P-M02)



Plastic Package (LCC-28P-M04)

Pin Assignment (TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

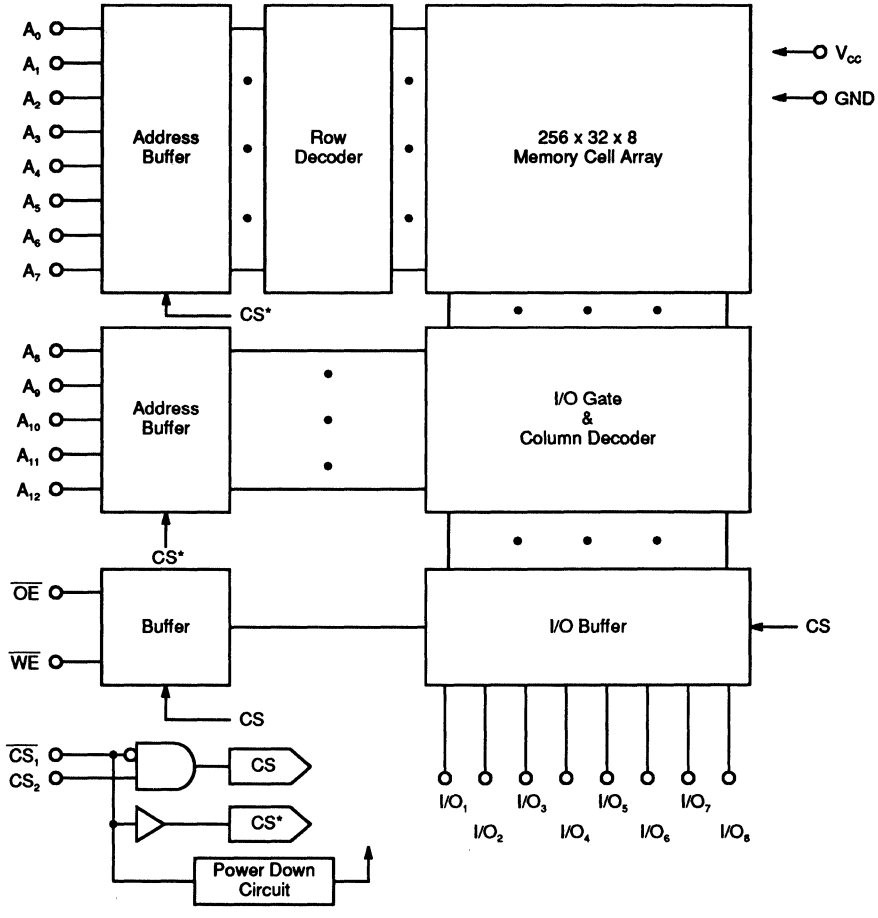
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	$V_{I/O}$	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB82B78 BLOCK DIAGRAM



CAPACITANCE (T_a = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A_0 to A_{12}	Address input.	$\overline{OE}$	Output Enable.
I/O_1 to I/O_8	Data input/output.	$\overline{WE}$	Write Enable.
$\overline{CS_1}$	Chip Select 1.	V_{CC}	Power Supply (+5V ±10%)
CS_2	Chip Select 2.	GND	Ground.

2

TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Power Supply Current
H	X	X	X	Standby	High-Z	Standby
L	L	X	X	Not selected	High-Z	Active
L	H	H	H	Dout disable	High-Z	Active
L	H	H	L	Read	Data out	Active
L	H	L	X	Write	Data in	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

DC CHARACTERISTICS

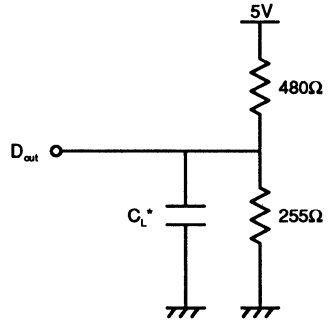
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=max.	I_{LI}	–10	10	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}	$I_{LI/O}$	–10	10	µA
Operating Supply Current	$\overline{CS_1}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=min. to max. $\overline{CS_1}$=V_{CC}–0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}–0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS_1}$=V_{IH} V_{IN}=V_{IH} or V_{IL}	I_{SB2}		30	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5*1	0.8	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS_1}$=Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 –2.0V min. for pulse width less than 8ns.
*2 The $\overline{CS_1}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Output Load



*Including Scope and jig Capacitance.

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V

	C_L	Parameters Measured
Load I	30pF	except t_{LZ}, t_{HZ}, t_{OW}, t_{OLZ} and t_{OHZ}
Load II	5pF	t_{LZ}, t_{HZ}, t_{OW}, t_{OLZ} and t_{OHZ}

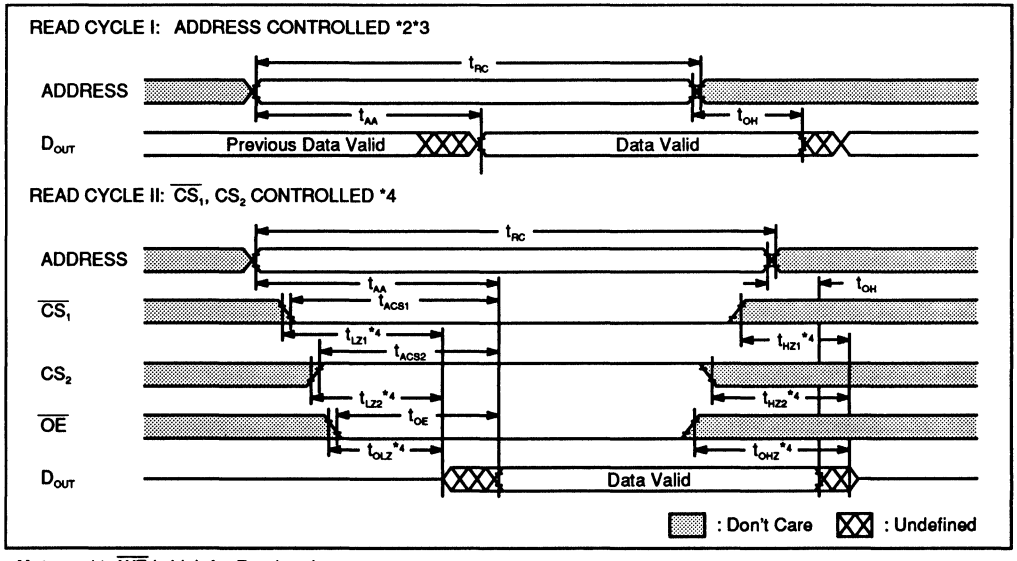
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB82B78-15		MB82B78-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time *2	t_{AA}		15		20	ns
$\overline{CS_1}$ Access Time *3	t_{ACS1}		15		20	ns
CS_2 Access Time	t_{ACS2}		8		10	ns
$\overline{OE}$ Access Time	t_{OE}		8		10	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Low-Z from $\overline{CS_1}$ *4	t_{LZ1}	3		3		ns
Output Low-Z from CS_2 *4	t_{LZ2}	2		2		ns
Output Low-Z from $\overline{OE}$ *4	t_{OLZ}	2		2		ns
Output High-Z from $\overline{CS_1}$ *4	t_{HZ1}		8		10	ns
Output High-Z from CS_2 *4	t_{HZ2}		8		10	ns
Output High-Z from $\overline{OE}$ *4	t_{OHZ}		8		10	ns

READ CYCLE TIMING DIAGRAM *1



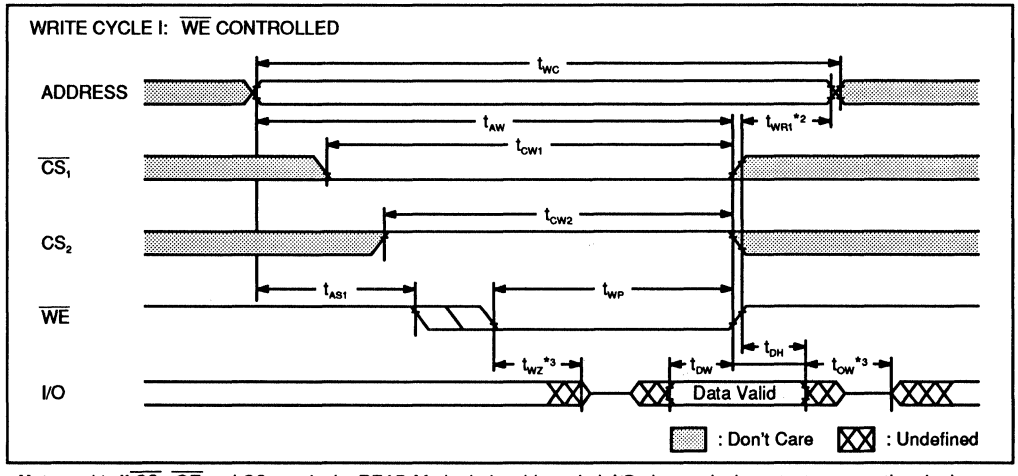
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.
*3 Address valid prior to or coincident with $\overline{CS_1}$ and CS_2 transition low and high, respectively.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

2

WRITE CYCLE *1

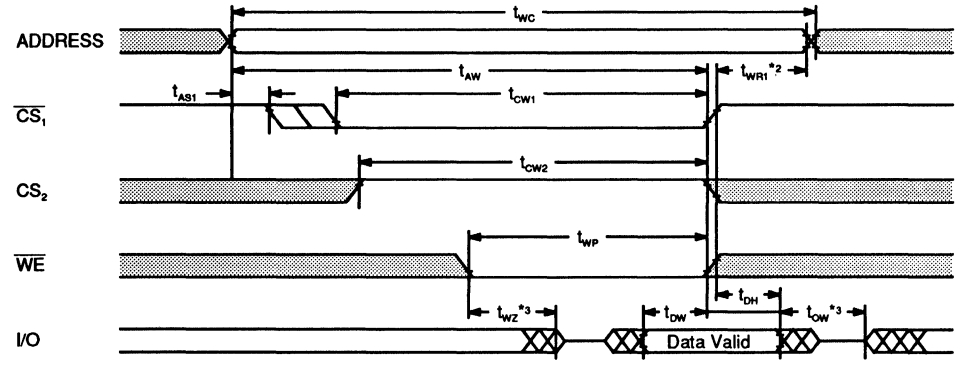
Parameter		Symbol	MB82B78-15		MB82B78-20		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	15		20		ns
Address Valid to End of Write		t_{AW}	10		15		ns
$\overline{CS_1}$ to End of Write		t_{CW1}	10		15		ns
CS_2 to End of Write		t_{CW2}	6		8		ns
Data Setup Time		t_{DW}	7		10		ns
Data Hold Time		t_{DH}	3		3		ns
Write Pulse Width		t_{WP}	8		10		ns
Write Recovery Time *2	$\overline{CS_1}$, $\overline{WE}$	t_{WR1}	3		3		ns
	CS_2	t_{WR2}	5		5		ns
Address Setup Time	$\overline{CS_1}$, $\overline{WE}$	t_{AS1}	0		0		ns
	CS_2	t_{AS2}	2		2		ns
Output Low-Z from $\overline{WE}$ *3		t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$ *3		t_{WZ}		8		10	ns

WRITE CYCLE TIMING DIAGRAM *1

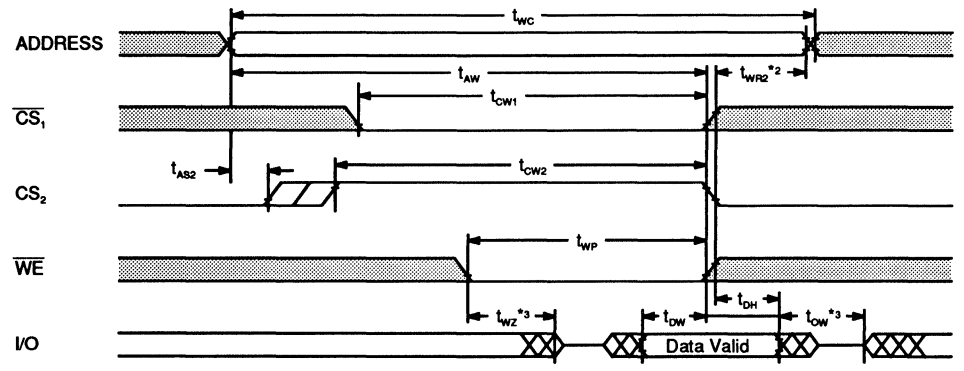


Note: *1 If $\overline{CS_1}$, $\overline{OE}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 t_{WR} is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS_1}$ CONTROLLED



WRITE CYCLE III: $\overline{CS_2}$ CONTROLLED

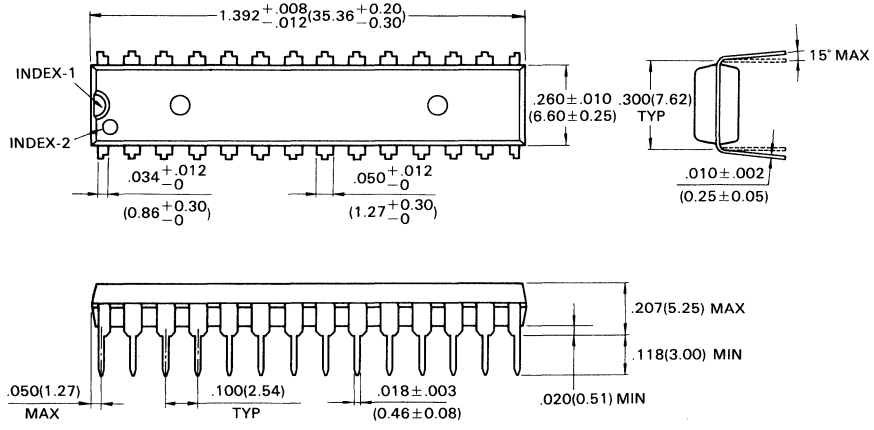


Note: *1 If $\overline{CS_1}$, $\overline{OE}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 t_{WR} is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

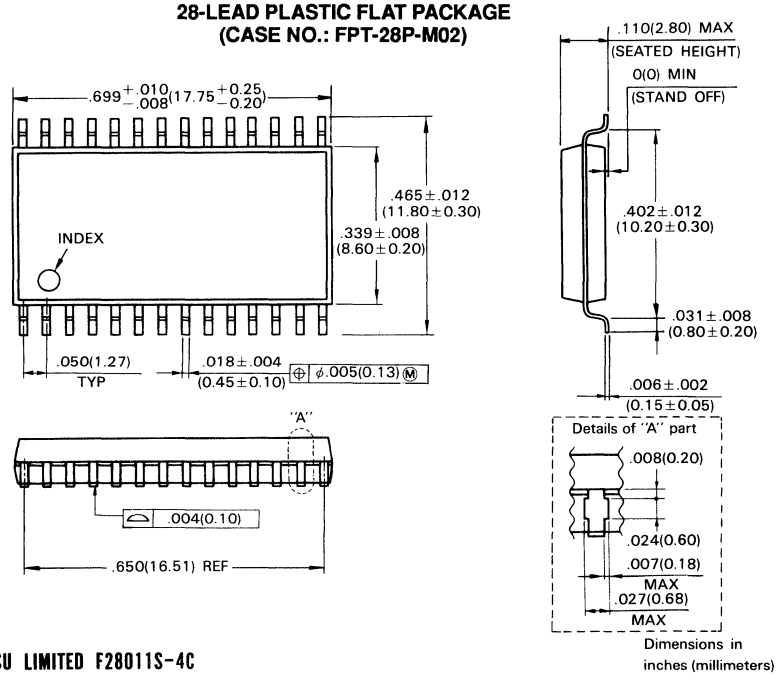


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-28P-M02)

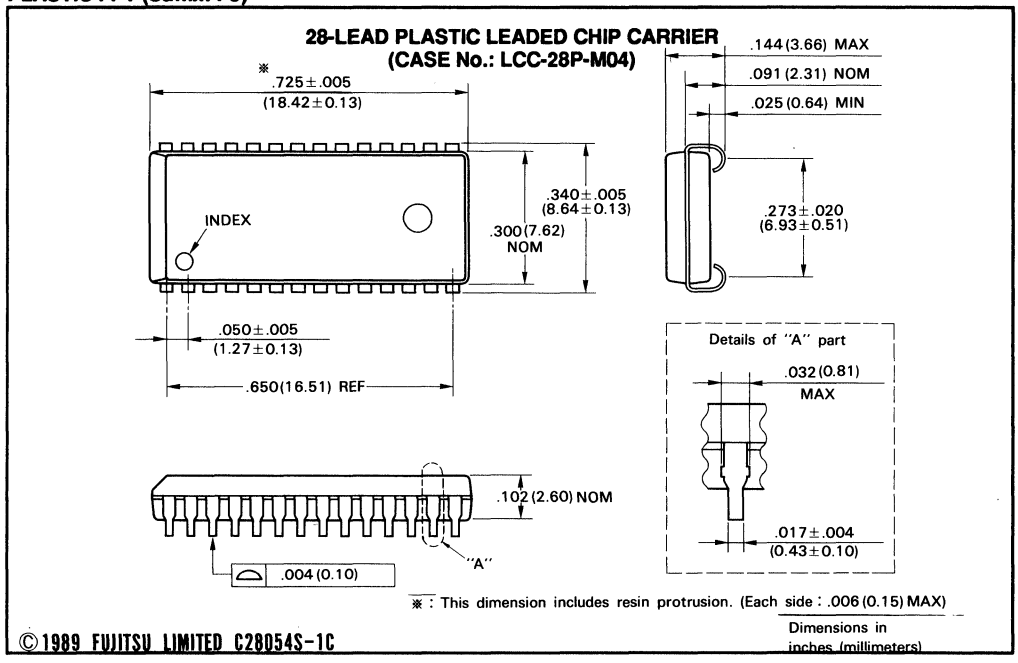


Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PJ)



May 1990
Edition 1.0

FUJITSU

DATA SHEET

MB82B79-15/-20
72K-BIT HIGH-SPEED BiCMOS SRAM

8K Words x 9 Bits High-Speed CMOS Static Random Access Memory

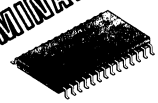
The Fujitsu MB82B79 is a 8,192 words x 9 bits static random access memory fabricated with a CMOS silicon gate process. For lower power dissipation and higher speed, the peripheral circuits use BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors. The MB82B79 has 300 mil plastic DIP and SOJ packages, and a 450 mil SOP package. The memory uses asynchronous circuitry and requires a +5 V power supply. All pins are TTL compatible.

The MB82B79 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

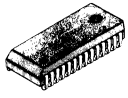
- Organization: 8,192 words x 9 bits
- Static operation: no clocks or refresh required
- Access time: $t_{AA} = t_{ACS1} = 15$ ns max.
  $t_{ACS2} = t_{OE} = 8$ ns max. (MB82B79-15)
  $t_{AA} = t_{ACS1} = 20$ ns max.
  $t_{ACS2} = t_{OE} = 10$ ns max. (MB82B79-20)
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. (Standby CMOS level)
  30 mA max. (StandbyTTL level)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Three-state outputs
- 28-pin Plastic Packages:

Skinny DIP	(300 mil)	MB82B79-xxPSK
SOJ	(300 mil)	MB82B79-xxPF
SOP	(450 mil)	MB82B79-xxPJ

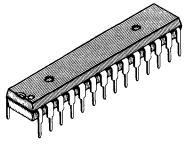
PRELIMINARY



PLASTIC PACKAGE
FPT-28P-M02



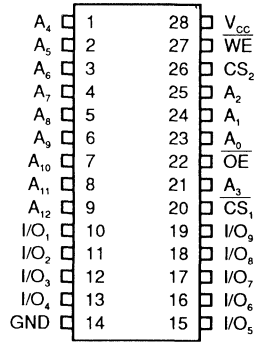
PLASTIC PACKAGE
LCC-28P-M04



PLASTIC PACKAGE
DIP-28P-M04

2

PIN ASSIGNMENT
(TOP VIEW)



Absolute Maximum Ratings (See Note)

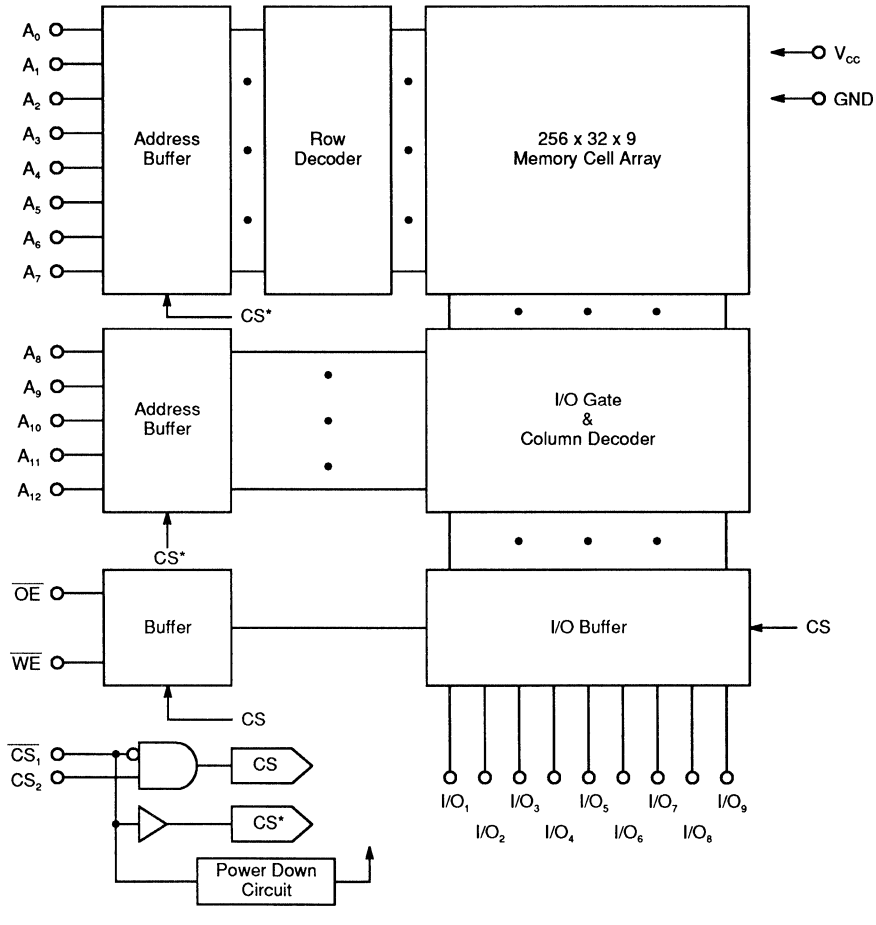
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	$V_{I/O}$	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB82B79 BLOCK DIAGRAM



CAPACITANCE (T_a = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			7	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A_0 to A_{12}	Address input.	$\overline{WE}$	Write Enable.
I/O_1 to I/O_9	Data input/output.	V_{CC}	Power Supply (+5V ±10%)
$\overline{CS_1}$	Chip Select 1.	GND	Ground.
CS_2	Chip Select 2.		
$\overline{OE}$	Output Enable.		

TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Power Supply Current
H	X	X	X	Standby	High-Z	Standby
L	L	X	X	Not selected	High-Z	Active
L	H	H	H	Dout disable	High-Z	Active
L	H	H	L	Read	Data out	Active
L	H	L	X	Write	Data in	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceed 2m/sec.

DC CHARACTERISTICS

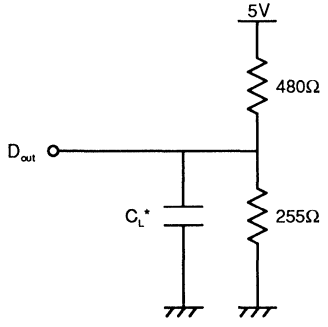
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=max.	I_{LI}	–10	10	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}	$I_{LI/O}$	–10	10	µA
Operating Supply Current	$\overline{CS_1}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=min. to max. $\overline{CS_1}$=V_{CC}–0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}–0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS_1}$=V_{IH} V_{IN}=V_{IH} or V_{IL}	I_{SB2}		30	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5*1	0.8	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS_1}$=Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 –2.0V min. for pulse width less than 20ns.
*2 The $\overline{CS_1}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Output Load



*Including Scope and jig Capacitance.

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V

	C_L	Parameters Measured
Load I	30pF	except t_{LZ}, t_{HZ}, t_{OW}, t_{OLZ} and t_{OHZ}
Load II	5pF	t_{LZ}, t_{HZ}, t_{OW}, t_{OLZ} and t_{OHZ}

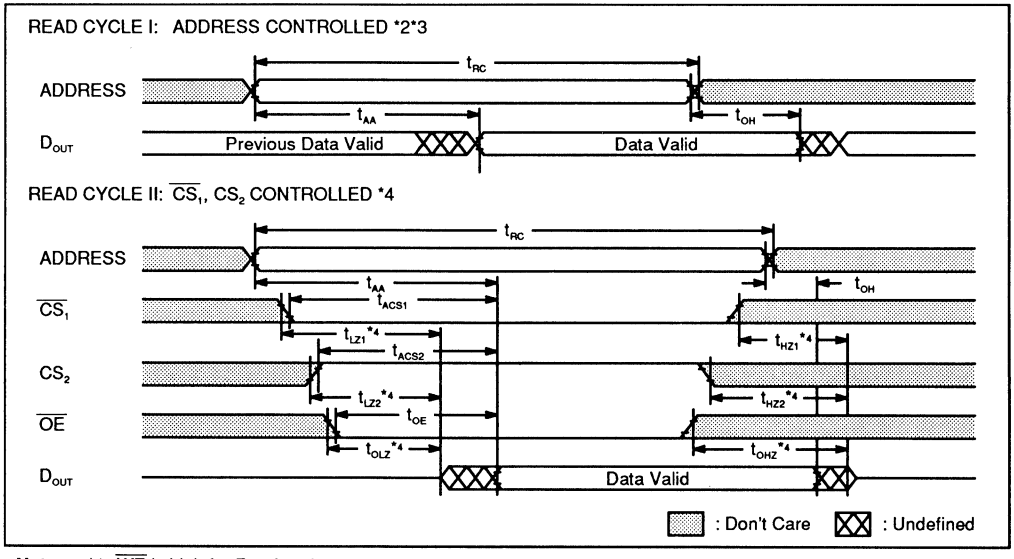
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB82B79-15		MB82B79-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time *2	t_{AA}		15		20	ns
$\overline{CS_1}$ Access Time *3	t_{ACS1}		15		20	ns
CS_2 Access Time	t_{ACS2}		8		10	ns
$\overline{OE}$ Access Time	t_{OE}		8		10	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Low-Z from $\overline{CS_1}$ *4	t_{LZ1}	3		3		ns
Output Low-Z from CS_2 *4	t_{LZ2}	2		2		ns
Output Low-Z from $\overline{OE}$ *4	t_{OLZ}	2		2		ns
Output High-Z from $\overline{CS_1}$ *4	t_{HZ1}		8		10	ns
Output High-Z from CS_2 *4	t_{HZ2}		8		10	ns
Output High-Z from $\overline{OE}$ *4	t_{OHZ}		8		10	ns

READ CYCLE TIMING DIAGRAM *1



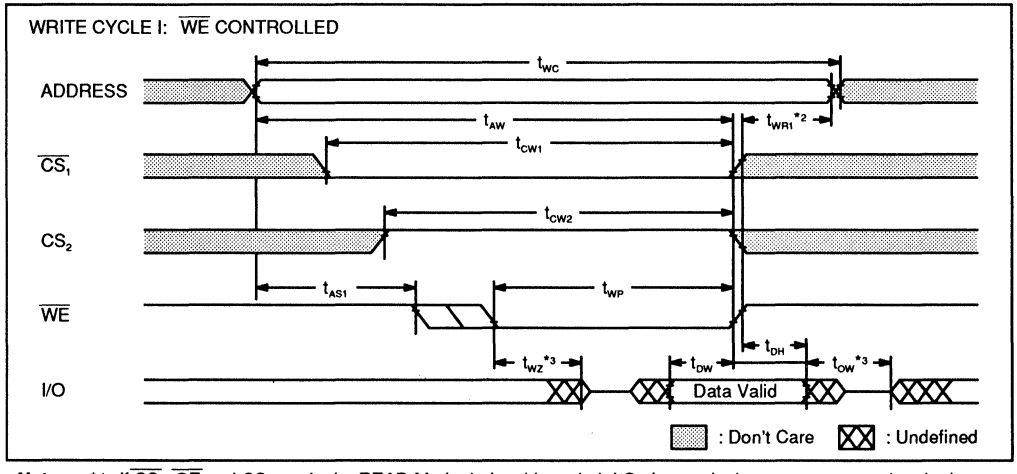
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.
*3 Address valid prior to or coincident with $\overline{CS_1}$ and CS_2 transition low and high, respectively.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

2

WRITE CYCLE *1

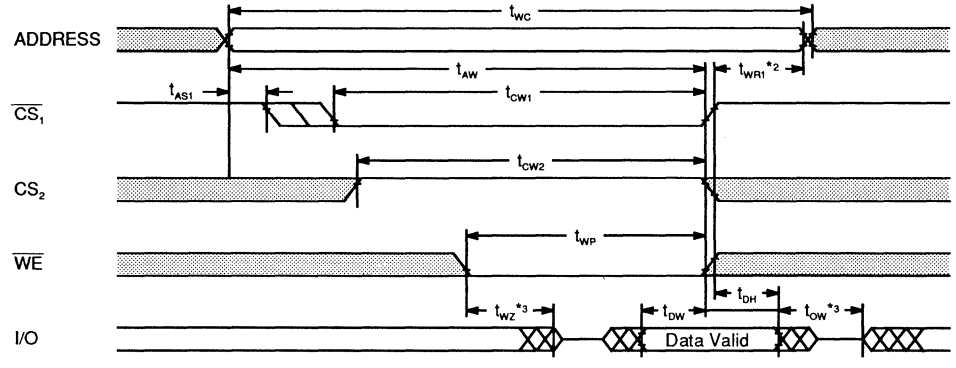
Parameter		Symbol	MB82B79-15		MB82B79-20		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	15		20		ns
Address Valid to End of Write		t_{AW}	10		15		ns
$\overline{CS_1}$ to End of Write		t_{CW1}	10		15		ns
CS_2 to End of Write		t_{CW2}	6		8		ns
Data Setup Time		t_{DW}	7		10		ns
Data Hold Time		t_{DH}	3		3		ns
Write Pulse Width		t_{WP}	8		10		ns
Write Recovery Time *2	$\overline{CS_1}$, $\overline{WE}$	t_{WR1}	3		3		ns
	CS_2	t_{WR2}	5		5		ns
Address Setup Time	$\overline{CS_1}$, $\overline{WE}$	t_{AS1}	0		0		ns
	CS_2	t_{AS2}	2		2		ns
Output Low-Z from $\overline{WE}$ *3		t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$ *3		t_{WZ}		8		10	ns

WRITE CYCLE TIMING DIAGRAM *1

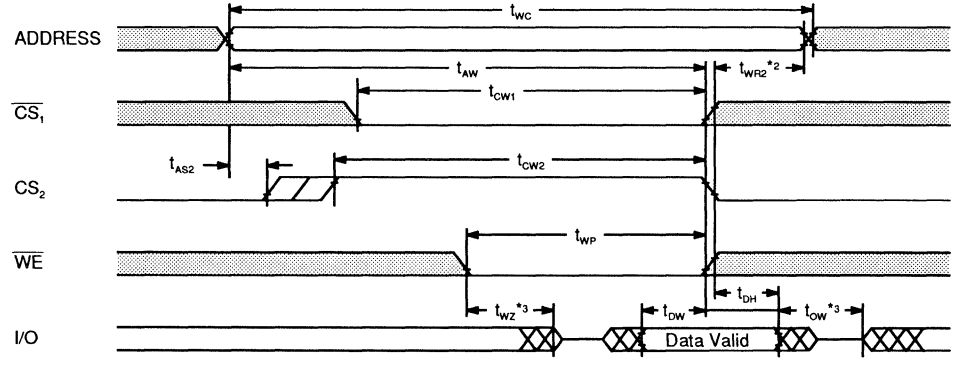


Note: *1 If $\overline{CS_1}$, $\overline{OE}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 t_{WR} is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE II: $\overline{CS_1}$ CONTROLLED



WRITE CYCLE III: $\overline{CS_2}$ CONTROLLED



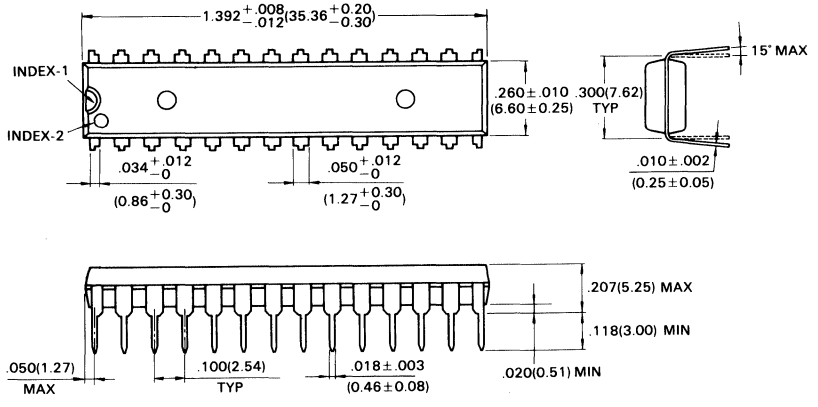
Note: *1 If $\overline{CS_1}$, $\overline{OE}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 t_{WR} is defined from the end point of WRITE Mode.
*3 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P–SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

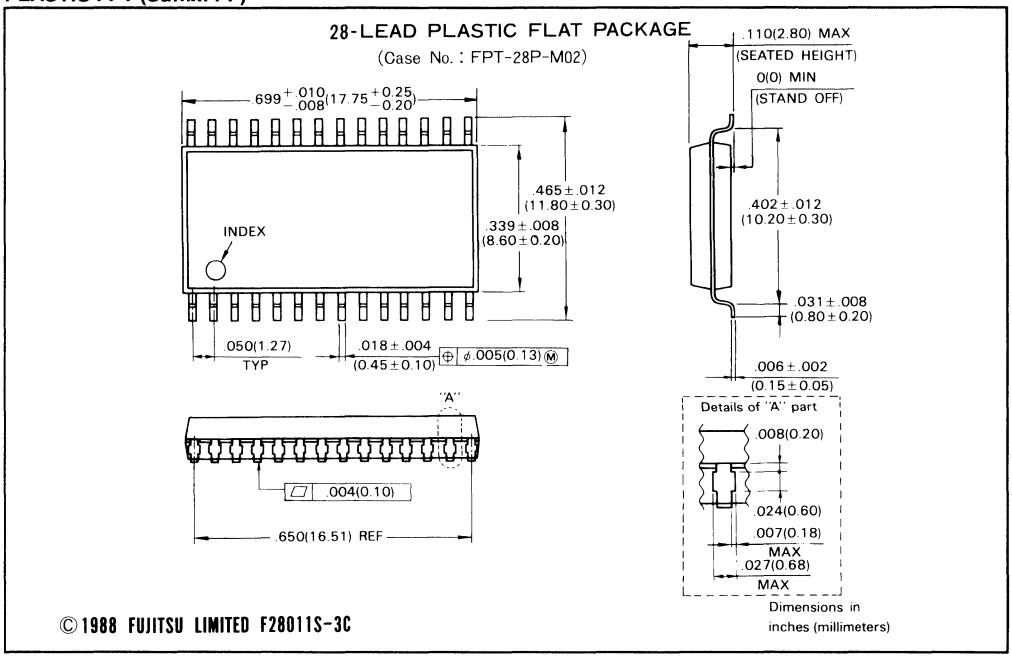
(Case No. : DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PF)



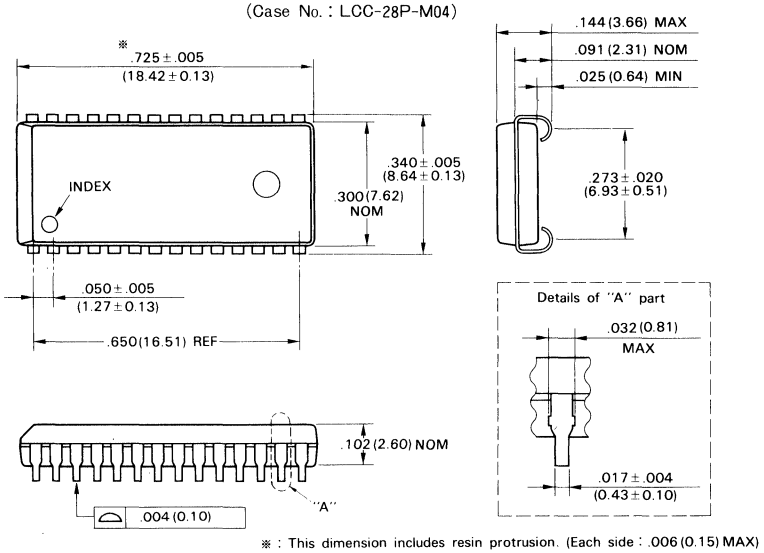
2

PACKAGE DIMENSIONS (Continued)

PLASTIC FPT (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB82B81-15/-20
256K-BIT HIGH-SPEED BiCMOS SRAM

256K Words x 1 Bit BiCMOS High-Speed Static Random Access Memory

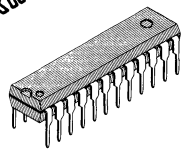
The Fujitsu MB82B81 is a static random access memory organized as 262,144 words x 1 bit and fabricated with a CMOS silicon gate process. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed.

The MB82B81 is housed in a 300 mil plastic DIP or small outline J-lead (SOJ) package. The memory uses asynchronous circuitry and requires a +5 V power supply. All pins are TTL compatible.

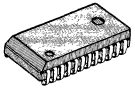
The MB82B81 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 262,144 words x 1 bit
- Static operation: no clocks or refresh required
- Fast access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B81-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B81-20)
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max (Active operation)
  15 mA max. (Standby Operation)
  25 mA max. (Standby Operation)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Three-state outputs
- Standard 24-pin Plastic Packages:
  Skinny DIP (300 mil) MB82B81-xxPSK
  SOJ (300 mil) MB82B81-xxPJ
- Pin compatible with MB81C81A

ADVANCE INFORMATION

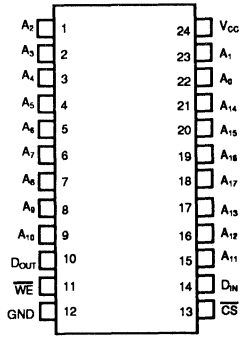


Plastic Package
(DIP-28P-M04)



Plastic Package
(LCC-28P-M04)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

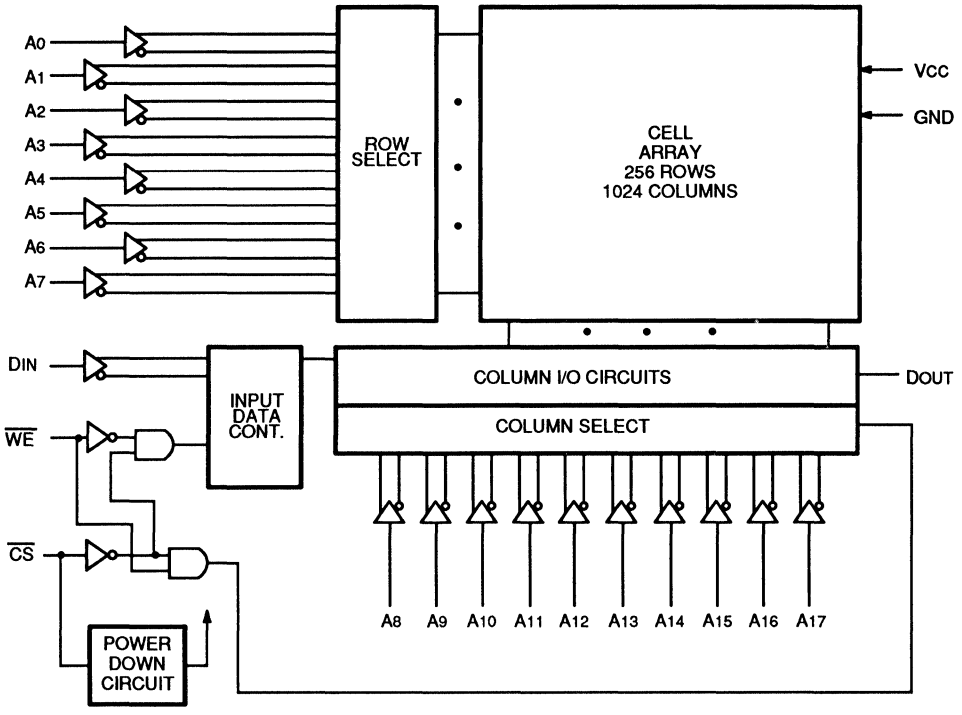
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−0.5 to +7	V
Output Voltage on any pin with respect to GND	$V_{I/O}$	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 — MB82B81 BLOCK DIAGRAM



CAPACITANCE (T_A= 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A_0 to A_{17}	Address input.	$\overline{WE}$	Write Enable.
D_{IN}	Data input.	V_{CC}	Power Supply (+5V ±10%).
D_{OUT}	Data Output.	GND	Ground.
$\overline{CS}$	Chip Select.		

2

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power Supply Current
H	X	Not Selected	High–Z	Standby
L	L	Write	High–Z	Active
L	H	Read	D_{OUT}	Active

Legend: H = High level, L = Low level, X = Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A *	0		70	°C

*: The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

DC CHARACTERISTICS

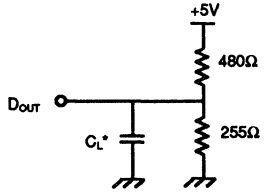
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = GND to V_{CC} V_{CC} = max.	I_{LI}	–10	10	µA
Output Leakage Current	V_{OUT} = GND to V_{CC} $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}	$I_{LI/O}$	–10	10	µA
Operating Supply Current	$\overline{CS}$ = V_{IL}, D_{OUT} = Open Cycle = min.	I_{CC}		120	mA
Standby Supply Current	V_{CC} = min. to max. $\overline{CS}$ = V_{CC} –0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} –0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS}$ = V_{IH} V_{CC} = min. to max.	I_{SB2}		25	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5*1	0.8	V
Output High Voltage	I_{OH} = –4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC} = GND to 4.5V $\overline{CS}$ = Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 –2.0V min. for pulse width less than 8ns.
*2 The $\overline{CS}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
- Output Load: Output: V_{OL} = 0.8V, V_{OH} = 2.2V



* Including Scope and Jig Capacitance

	C_L	Parameters measured
Load I	30pF	except t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}
Load II	5pF	t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

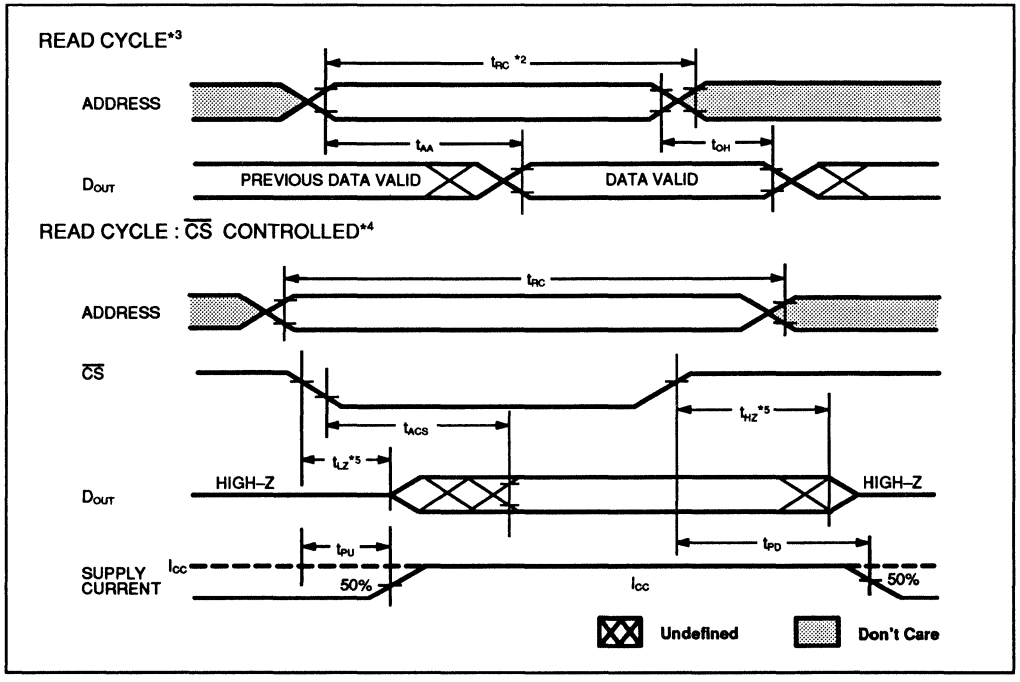
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B81-15		MB82B81-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time	t_{AA}		15		20	ns
$\overline{CS}$ Access Time	t_{ACS}		15		20	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Low-Z from $\overline{CS}$	t_{LZ}	3		3		ns
Output High-Z from $\overline{CS}$	t_{HZ}		8		8	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		15		20	ns

READ CYCLE TIMING DIAGRAM*1



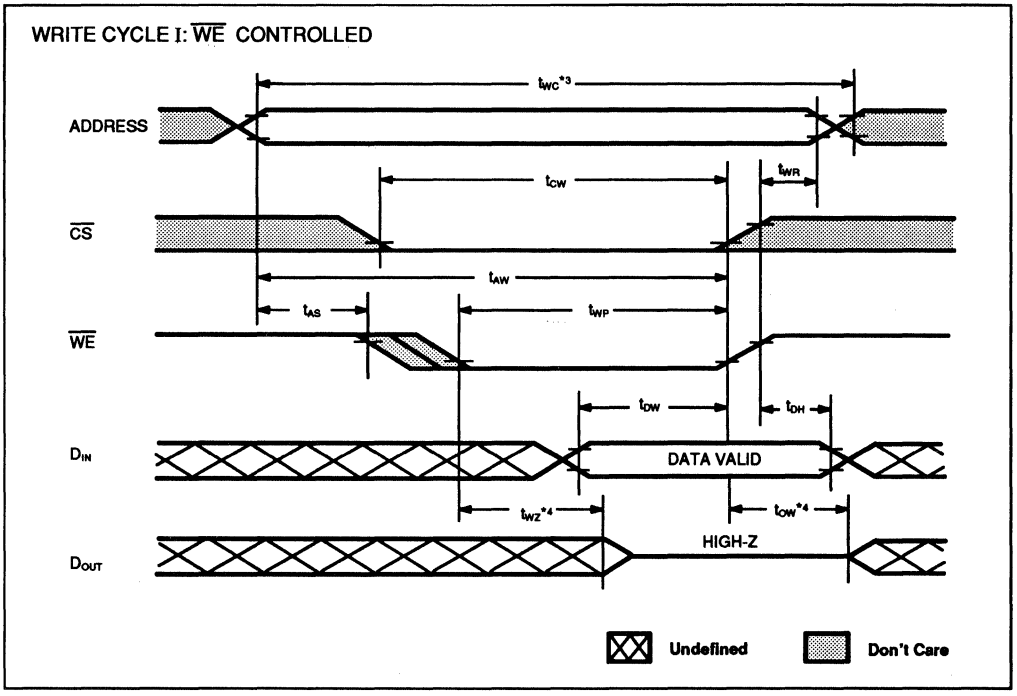
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timing are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

2

WRITE CYCLE

Parameter	Symbol	MB82B81-15		MB82B81-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		ns
Address Valid to End of Write	t_{AW}	11		15		ns
$\overline{CS}$ to End of Write	t_{CW}	11		15		ns
Data Setup Time	t_{DW}	4		8		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	11		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$	t_{WZ}		6		10	ns

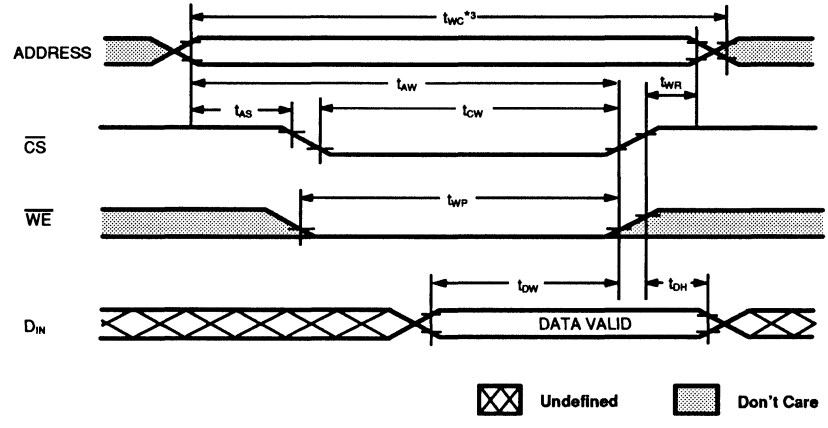
WRITE CYCLE TIMING DIAGRAM*1



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitions address.
*4 Transition measured at ±500mV from steady state voltage with specified load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM (Continued)*1*2*4

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2

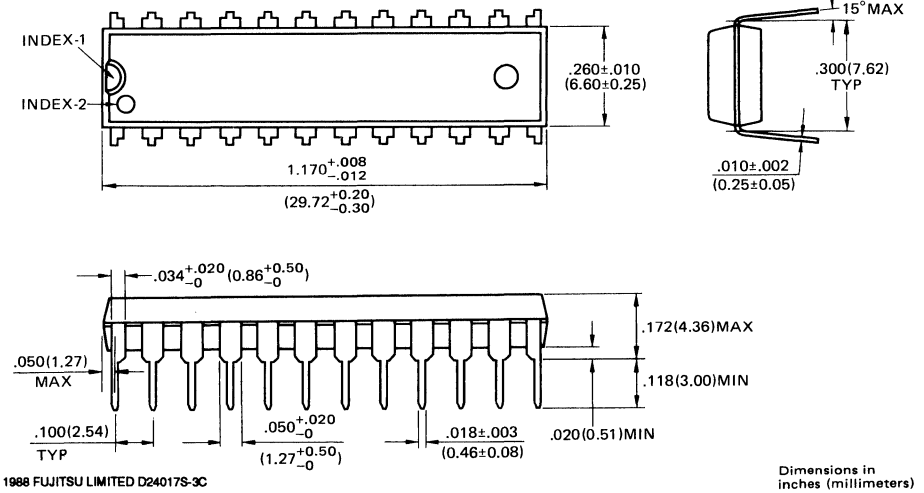


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.

PACKAGE DIMENSIONS

(Suffix: –P–SK)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)

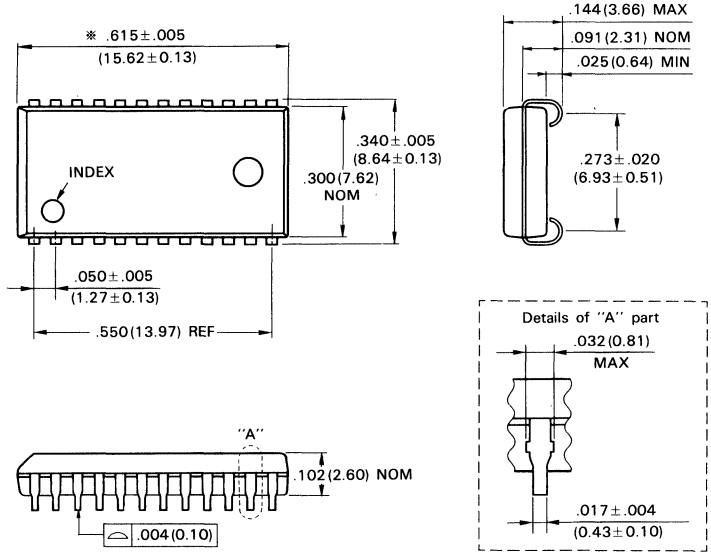


Dimensions in inches (millimeters)

2

PACKAGE DIMENSIONS (Continued)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-24P-M02)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

July 1990
Edition 1.0

FUJITSU

DATA SHEET

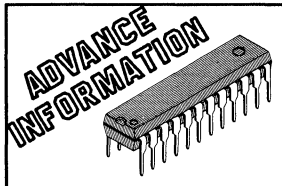
MB82B84-15/-20
CMOS 256K-BIT HIGH-SPEED BiCMOS SRAM

64K Words x 4 Bits BiCMOS High-Speed Static Random Access Memory with Automatic Power Down

The Fujitsu MB82B84 is a 65,536 words x 4 bits static random access memory fabricated with a CMOS silicon gate process. For lower power dissipation and higher speed, peripheral circuits use BiCMOS technology. To obtain a smaller chip size, cells use NMOS transistors and resistors. The MB82B84 is housed in 300 mil plastic DIP and small outline J-lead (SOJ) packages. The memory uses asynchronous circuitry and requires a +5 V power supply. All pins are TTL compatible.

The MB82B84 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

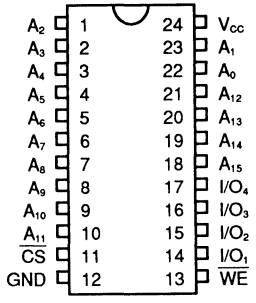
- Organization: 65,536 words x 4 bits
- Access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B84-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B84-20)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Static operation: no clock required
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. (Standby, CMOS level)
  25 mA max. (Standby, TTL level)
- Standard 24-pin Plastic Package:
  Skinny DIP (300 mil) MB82B84-xxPSK
  SOJ MB82B84-xxPJ
- Pin compatible with MB81C84A



PLASTIC PACKAGE
DIP-24P-M03

PLASTIC PACKAGE
LCC-24P-M02

PIN ASSIGNMENT
(TOP VIEW)



(DIP & SOJ Package)

Absolute Maximum Ratings (See Note)

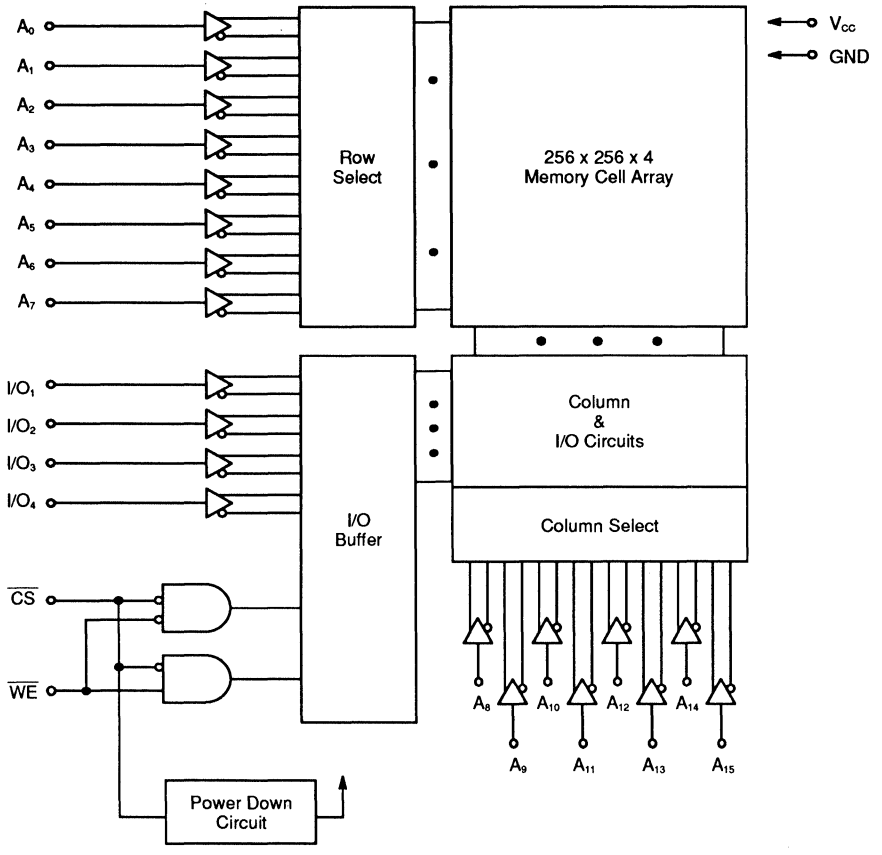
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	$V_{I/O}$	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB82B84 BLOCK DIAGRAM



CAPACITANCE (T_a= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V/CS=0V)	C/CS			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{15}	Address input	$\overline{WE}$	Write Enable
I/O_1 to I/O_4	Data input/output	V_{CC}	Power Supply (+5V ±10%)
$\overline{CS}$	Chip Select 1	GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O pin	Power Supply Current
H	X	Standby	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

2

DC CHARACTERISTICS

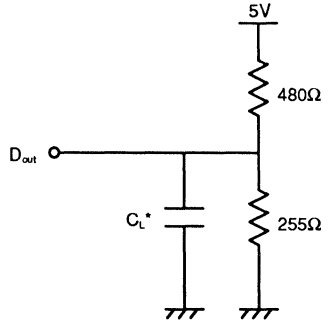
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=max.	I_{LI}	–10	10	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}	$I_{LI/O}$	–10	10	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=min. to max. $\overline{CS}$=V_{CC}–0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}–0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS}$=V_{IH} V_{CC}=min. to max.	I_{SB2}		25	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5*1	0.8	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS}$=Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 –2.0V min. for pulse width less than 8ns.
*2 The $\overline{CS}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
- Output Load



*Including Scope and jig capacitance

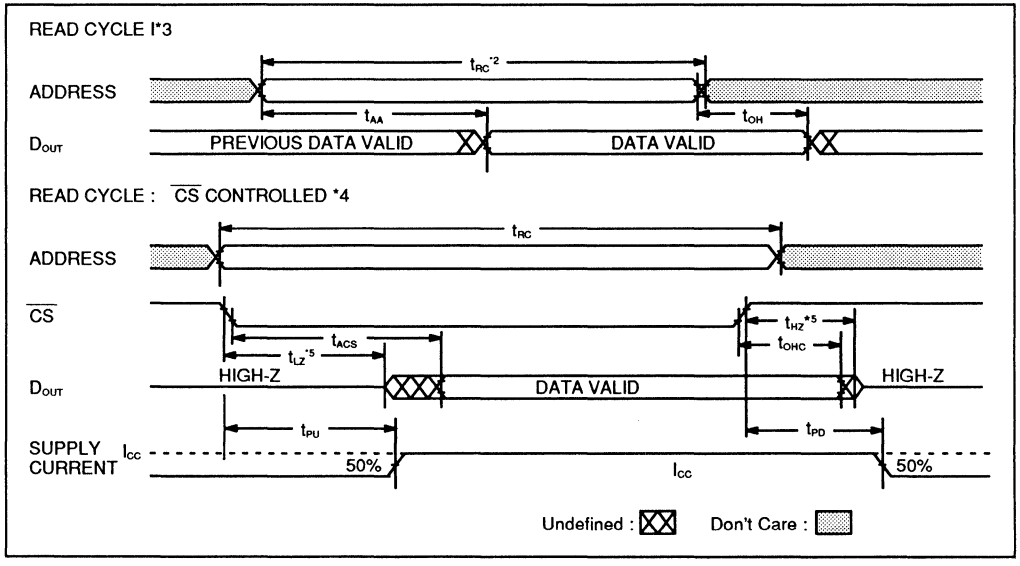
	C_L	Parameters measured
Load I	30pF	except t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}
Load II	5pF	t_{LZ}, t_{HZ}, t_{OW} and t_{WZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)
READ CYCLE

Parameter	Symbol	MB82B84-15		MB82B84-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time	t_{AA}		15		20	ns
$\overline{CS}$ Access Time	t_{ACS}		15		20	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Low-Z from $\overline{CS}$	t_{LZ}	3		3		ns
Output High-Z from $\overline{CS}$	t_{HZ}		8		8	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		15		20	ns

READ CYCLE TIMING DIAGRAM *1



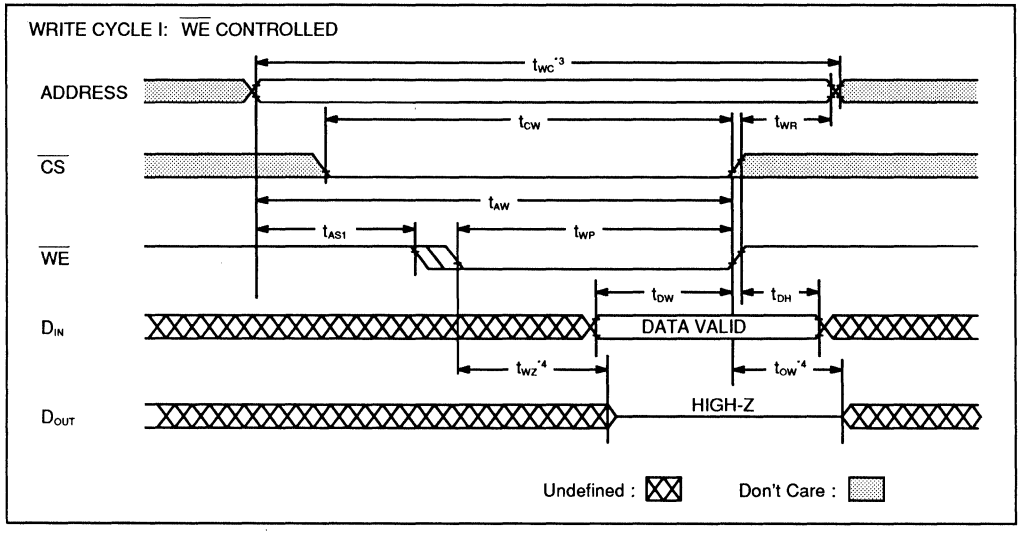
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage.

2

WRITE CYCLE

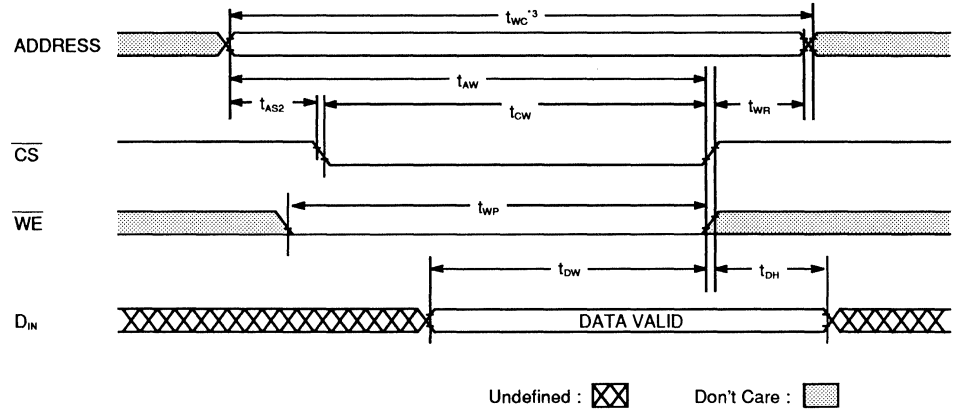
Parameter	Symbol	MB82B84-15		MB82B84-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		ns
Address Valid to End of Write	t_{AW}	11		15		ns
$\overline{CS}$ to End of Write	t_{CW}	11		15		ns
Data Setup Time	t_{DW}	4		8		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	11		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$	t_{WZ}		6		10	ns

WRITE CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2

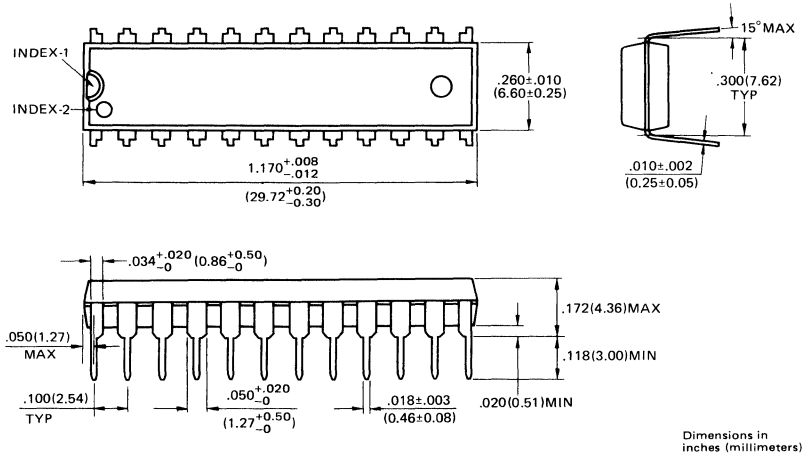


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load in Fig. 2.
*5 If $\overline{CS}$ is in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

PACKAGE DIMENSIONS

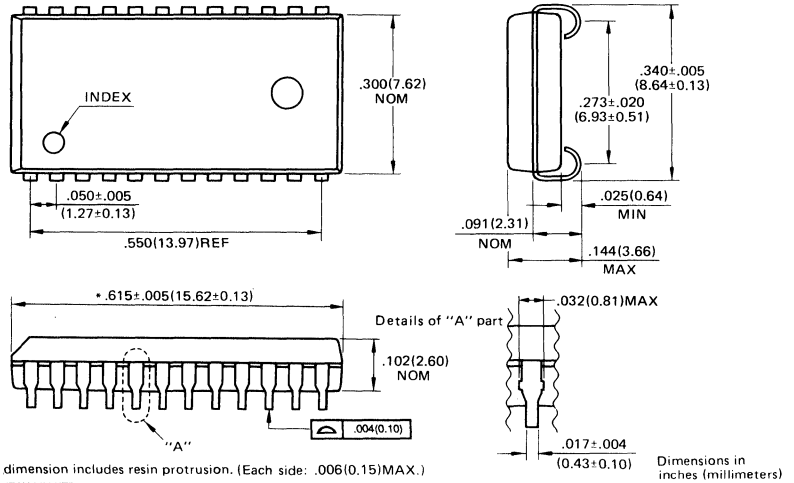
2

24-LEAD PLASTIC DUAL-IN LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in inches (millimeters)

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-24P-M02)



* : This dimension includes resin protrusion. (Each side: .006(0.15)MAX.)

Dimensions in inches (millimeters)

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB82B85-15/-20
256K-BIT HIGH-SPEED BiCMOS SRAM

64K Words x 4 Bits BiCMOS High-Speed Static Random Access Memory With Automatic Power Down

The Fujitsu MB82B85 is a static random access memory organized as 65,536 words by 4 bits and fabricated with a CMOS silicon gate process. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B85 is housed in 300 mil plastic DIP and small outline J-lead (SOJ) packages. The memory uses asynchronous circuitry and requires +5 V power supply. All pins are TTL compatible

The MB82B85 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

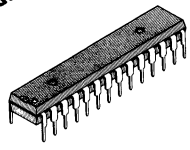
- Organization: 65,536 words x 4 bits
- Access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B85-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B85-20)
- BiCMOS peripheral circuits
- TTL compatible inputs and outputs
- Static operation: no clock required
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. (Active operation)
  15 mA max. CMOS Standby)
  25 mA max. (TTL Standby)
- Standard 28-pin Plastic Packages:
  Skinny DIP MB82B85-xxPSK
  SOJ MB82B85-xxPJ

Absolute Maximum Ratings (See Note)

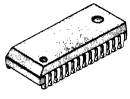
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	$V_{I/O}$	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFORMATION

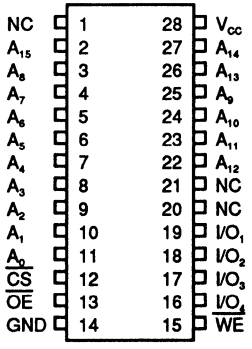


Plastic Package
(DIP-28P-M04)



Plastic Package
(LCC-28P-M04)

Pin Assignment
(TOP VIEW)



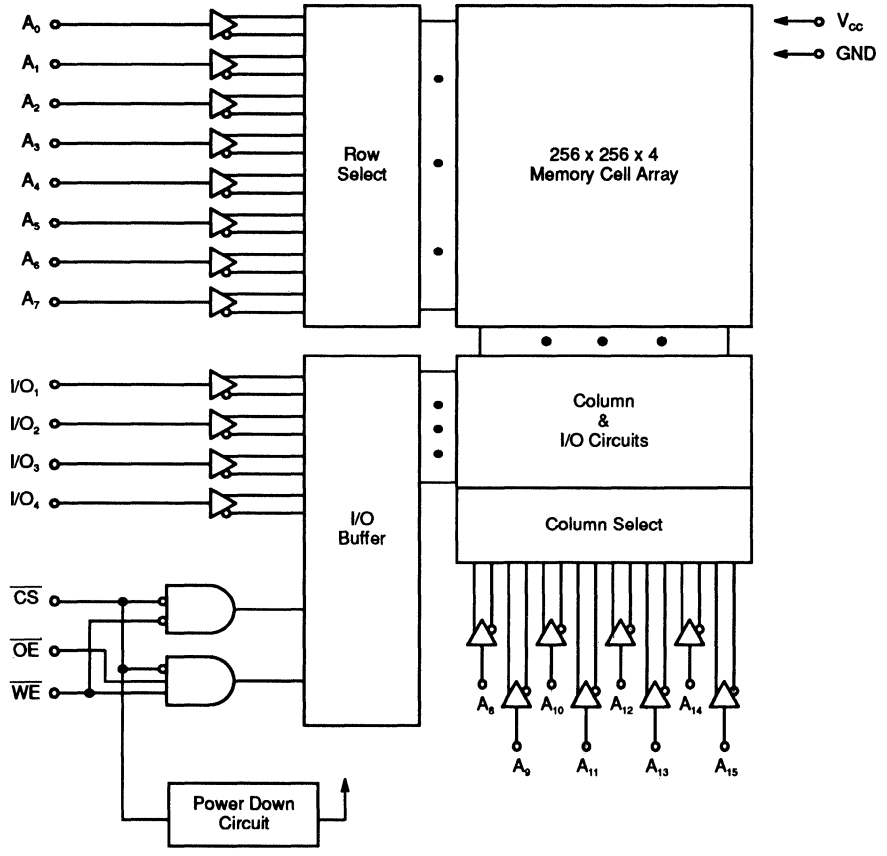
(DIP & SOJ Package)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

2

Fig. 1 – MB82B85 BLOCK DIAGRAM



CAPACITANCE (T_a= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance ($V_{\overline{CS}}$=0V)	$C_{\overline{CS}}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{15}	Address input	$\overline{WE}$	Write Enable
I/O_1 to I/O_4	Data input/output	V_{CC}	Power Supply (+5V ±10%)
$\overline{CS}$	Chip Select	GND	Ground
$\overline{OE}$	Output Enable		

2

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	Power Supply Current
H	X	X	Standby	High–Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	H	Output Desable	High–Z	Active
L	H	L	Read	D_{OUT}	Active

Legend: H=High level, L=Low level, X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A*	0		70	°C

* The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.

DC CHARACTERISTICS

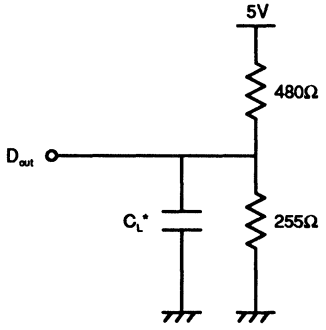
(Recommended operating conditions otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN}=GND to V_{CC} V_{CC}=max.	I_{LI}	–10	10	µA
Output Leakage Current	$V_{I/O}$=GND to V_{CC} $\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}	$I_{LI/O}$	–10	10	µA
Operating Supply Current	$\overline{CS}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Standby Supply Current	V_{CC}=min. to max. $\overline{CS}$=V_{CC}–0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}–0.2V	I_{SB1}		15	mA
Standby Supply Current	$\overline{CS}$=V_{IH} V_{CC}=min. to max.	I_{SB2}		25	mA
Input High Voltage		V_{IH}	2.2	6.0	V
Input Low Voltage		V_{IL}	–0.5*1	0.8	V
Output High Voltage	I_{OH}=–4mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL}=8mA	V_{OL}		0.4	V
Peak Power-on Current *2	V_{CC}=GND to 4.5V $\overline{CS}$=Lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

Note: *1 –2.0V min. for pulse width less than 8ns.
*2 The $\overline{CS}$ input should be connected to V_{CC} to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Time: 1ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
- Output Load



*Including Scope and jig capacitance

	C_L	Parameters measured
Load I	30pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

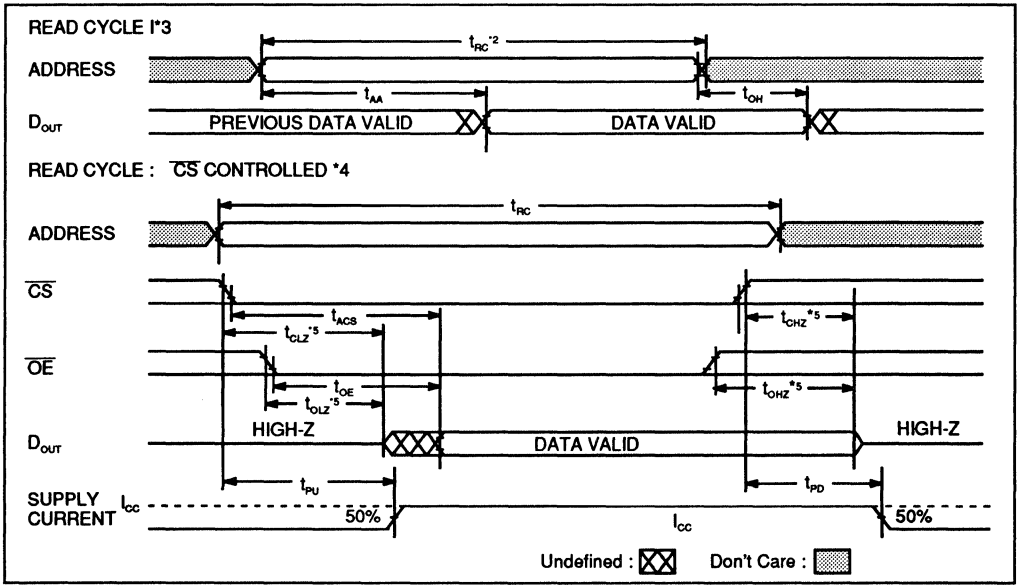
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB82B85-15		MB82B85-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		ns
Address Access Time	t_{AA}		15		20	ns
$\overline{CS}$ Access Time	t_{ACS}		15		20	ns
$\overline{OE}$ Access Time	t_{OE}		8		10	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Low-Z from $\overline{CS}$	t_{CLZ}	3		3		ns
Output Low-Z from $\overline{OE}$	t_{OLZ}	3		3		ns
Output High-Z from $\overline{CS}$	t_{CHZ}		8		8	ns
Output High-Z from $\overline{OE}$	t_{OHZ}		8		8	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		15		20	ns

READ CYCLE TIMING DIAGRAM *1



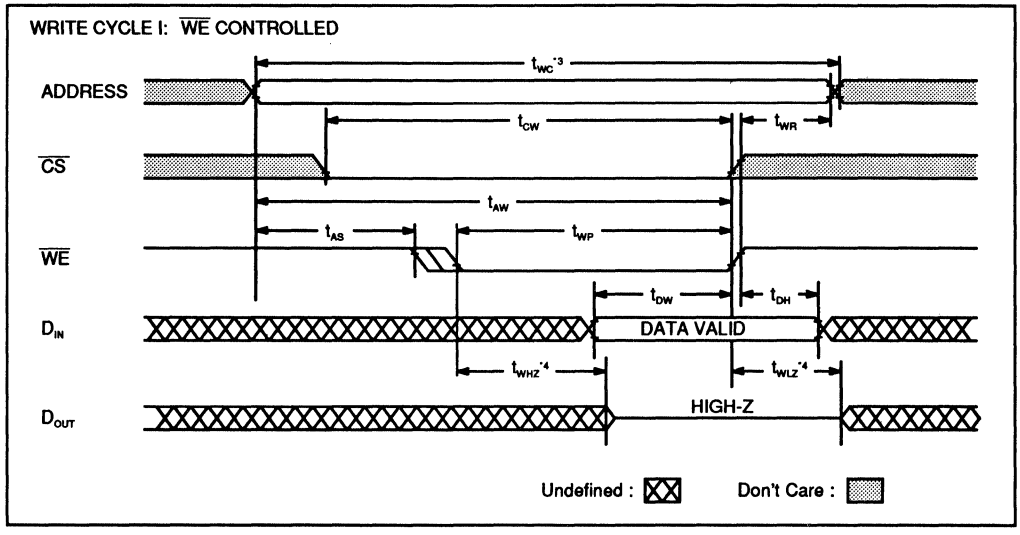
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS}$=$\overline{OE}$=V_{IL}.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

2

WRITE CYCLE

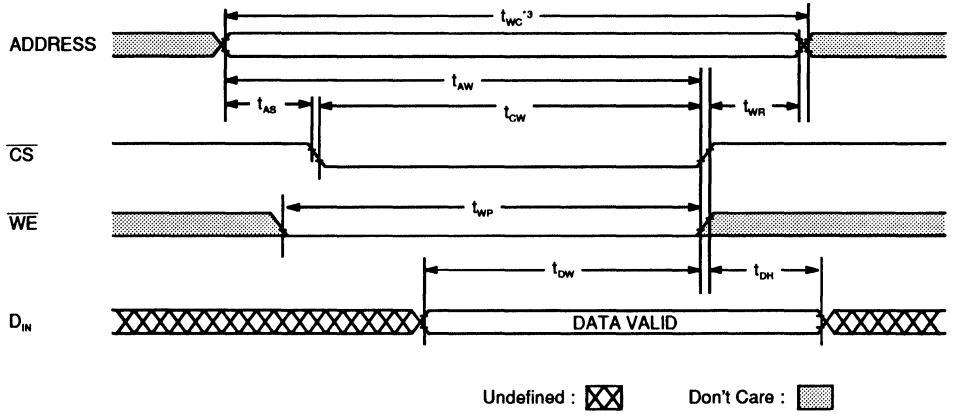
Parameter	Symbol	MB82B85-15		MB82B85-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		ns
Address Valid to End of Write	t_{AW}	11		15		ns
$\overline{CS}$ to End of Write	t_{CW}	11		15		ns
Data Setup Time	t_{DW}	4		8		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	11		15		ns
Write Recovery Time	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$	t_{WLZ}	0		0		ns
Output High-Z from $\overline{WE}$	t_{WHZ}		6		10	ns

WRITE CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load II in Fig. 2.
*5 If $\overline{CS}$, $\overline{OE}$ are in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2

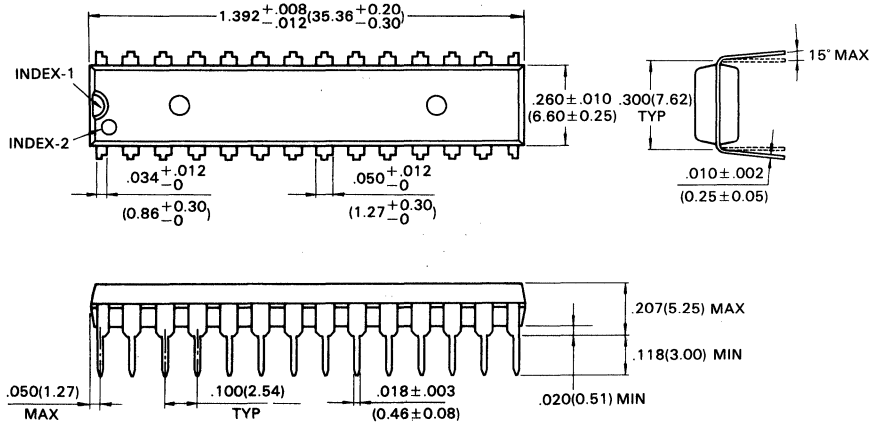


Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to first transitioning address.
*4 Transition measured at ±500mV from steady state voltage with specified load II in Fig. 2.
*5 If $\overline{CS}$, $\overline{OE}$ are in the Read Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

2

PACKAGE DIMENSIONS

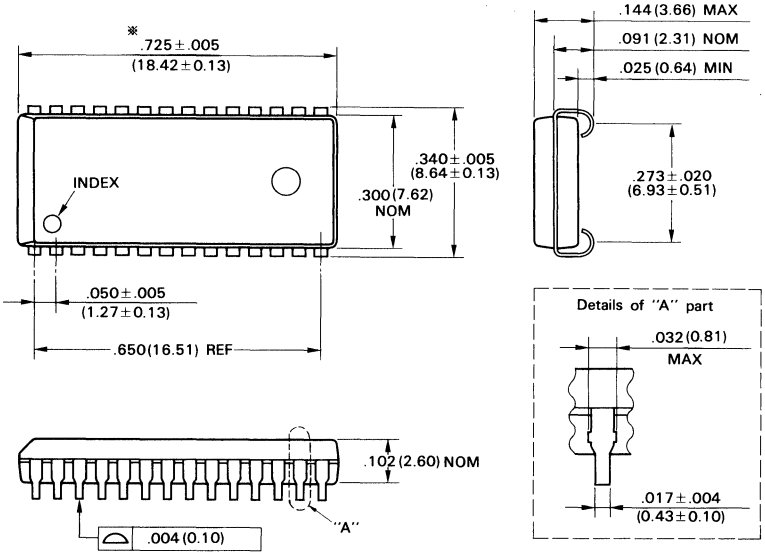
28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

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FUJITSU

DATA SHEET

MB82B88-15/-20
256K-BIT HIGH-SPEED BiCMOS SRAM

32K Words x 8 Bits BiCMOS High-Speed Static Random Access Memory

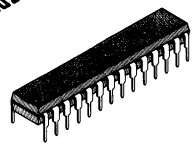
The Fujitsu MB82B88 is a high-speed static random access memory organized as 32,768 words x 8 bits and fabricated with CMOS technology. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B88 is housed in 300 mil plastic DIP and SOJ packages. All pins are TTL compatible and a single +5 V power supply is required.

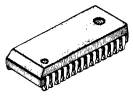
The MB82B88 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B88-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B88-20)
- Low power consumption: 715 mW max. (Operating)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB82B88-xxPSK
  SOJ (300 mil) MB82B88-xxPJ

ADVANCE INFORMATION

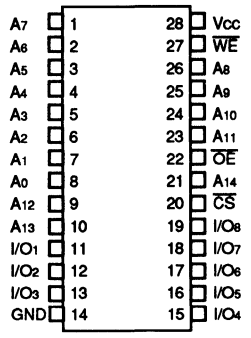


Plastic Package
(DIP-28P-M04)



Plastic Package
(LCC-28P-M04)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DATA SHEET

MB82B89-15/-20
288K-BIT HIGH-SPEED BiCMOS SRAM

32K Words x 9 Bits BiCMOS High-Speed Static Random Access Memory

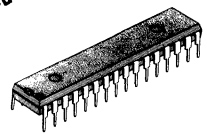
The Fujitsu MB82B89 is a 32,768 words x 9 bits high-speed static random access memory fabricated with CMOS technology. For lower power dissipation and higher speed, the peripheral circuits consist of BiCMOS technology. For smaller chip size, the cells use NMOS transistors and resistors.

The MB82B89 is housed in 300 mil plastic DIP and SOJ packages. All pins are TTL compatible and a single +5 V power supply is required.

The MB82B89 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 9 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 15$ ns max. (MB82B89-15)
  $t_{AA} = t_{ACS} = 20$ ns max. (MB82B89-20)
- Low power consumption: 715 mW max. (Operating)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB82B89-xxPSK
  SOJ (300 mil) MB82B89-xxPJ

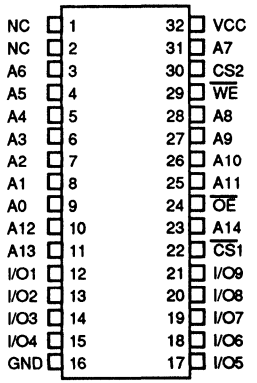
ADVANCE INFORMATION



Plastic Package
(LCC-32P-M02)

Plastic Package
(LCC-32P-M04)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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FUJITSU

DATA SHEET

MB82B008-25
1M-BIT HIGH-SPEED BiCMOS SRAM

128K Words x 8 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB82B008 is a high-speed static random access memory organized as 131,072 words x 8 bits and fabricated with CMOS technology. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain smaller chip size, the cells use NMOS transistors and resistors.

The MB82B008 is housed in a 400 mil plastic SOJ package. All pins are TTL compatible and a single +5 V power supply is required.

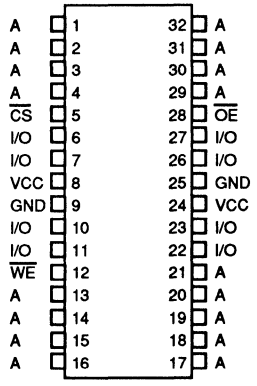
The MB82B008 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 131,072 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB82B008-25)
- Low power consumption: 715 mW max. (Operating)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Package:
  SOJ (400 mil) MB82B008-xxPJ

ADVANCE INFORMATION

Plastic Package
(LCC-32P-MXX)

Pin Assignment
(TOP VIEW)



Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

DATA SHEET

MB82B009-25
1,152M-BIT HIGH-SPEED BiCMOS SRAM

128K Words x 9 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB82B009 is a high-speed static random access memory organized as 131,072 words x 9 bits and fabricated with CMOS technology. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B009 is housed in a 400 mil plastic SOJ package. All pins are TTL compatible and a single +5 V power supply is required.

The MB82B009 is ideally suited for use in large computers and other applications where fast access time, large capacity, and ease of use are required. The device offers the advantages of low power dissipation, low cost, and high performance.

- Organization: 131,072 words x 9 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB82B009-25)
- Low power consumption: 715 mW max. (Operating)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 36-pin Plastic Package:
  SOJ (400 mil) MB82B009-25PJ

ADVANCE INFORMATION

Plastic Package
(LCC-36P-MXX)

Pin Assignment
(TOP VIEW)

T.B.D.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FUJITSU

DATA SHEET

MB82B201-25/-35
4M-BIT HIGH-SPEED BiCMOS SRAM

4M-Bit (x1 or x4) Configurable BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB82B201 is a 4M-bit high speed static random access memory fabricated with CMOS technology. The memory organization of MB82B201 can be configured to 1 bit or 4 bits with the MOD pin. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B201 is housed in a 400 mil plastic SOJ package. All pins are TTL compatible and a single +5 V power supply is required.

The MB82B201 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 4,194,304 words x 1 bit (MOD = H Input) or 1,048,576 words x 4 bits (MOD = L Input)
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB82B201-25); $t_{AA} = t_{ACS} = 35$ ns max. (MB82B201-35)
- Low power consumption: 660 mW max. (Operating); 138 mW max. (TTL Standby); 83 mW Max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Package: SOJ (400 mil) MB82B201-xxPJ

Absolute Maximum Ratings (See Note)

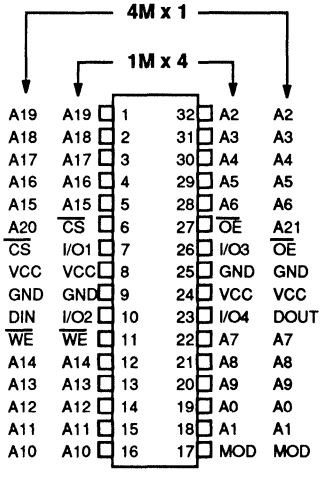
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFORMATION

Plastic Package
(LCC-32P-MXX)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Edition 1.0

FUJITSU

DATA SHEET

MB82B206-25/-35
4M-BIT HIGH-SPEED BiCMOS SRAM

1M Words x 4 Bits BiCMOS High-Speed Static Random Access Memory

The Fujitsu MB82B206 is a high-speed static random access memory organized as 1,048,576 words x 4 bits and fabricated with CMOS technology. BiCMOS technology is used in the peripheral circuits to provide lower power dissipation and higher speed. To obtain a smaller chip size, the cells use NMOS transistors and resistors.

The MB82B206 is housed in a 400 mil plastic SOJ package. All pins are TTL compatible and a single +5 V power supply is required.

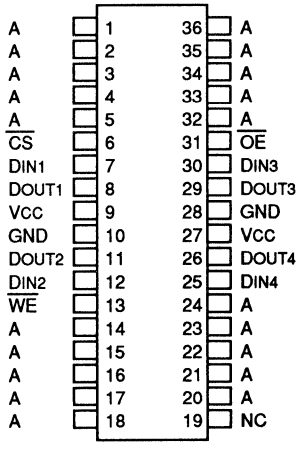
The MB82B206 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 1,048,576 words x 4 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB82B206-25)
  $t_{AA} = t_{ACS} = 35$ ns max. (MB82B206-35)
- Low power consumption: 660 mW max. (Operating)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 36-pin Plastic Package:
  SOJ (400 mil) MB82B206-xxPJ

ADVANCE INFORMATION

Plastic Package
(LCC-36P-MXX)

Pin Assignment
(TOP VIEW)



Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Section 3

Low Power CMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity (Organization)	Package Options
3–3	*Low-Power CMOS SRAMs Product Cross Reference*			
3–5	MB8464A–80, –80L and LL	80	65536 bits	28-pin Plastic DIP, Sk DIP, SOP
	–10, –10L and LL	100	(8192 x 8)	32-pad Ceramic LCC
	–15, –15L and LL	150		
3–17	MB84256A–70, –70L and LL	70	262144 bits	28-pin Plastic DIP, Sk DIP, SOP, TSOP
	–10, -10L and LL	100	(32768 x 8)	
	–12, -12L and LL	120		
	–15, -15L and LL	150		
3–29	MB841000–80, –80L	80	1048576 bits	32-pin Plastic DIP, SOJ
	–10, –10L	100	(131072 x 8)	
	–12, –12L	120		

3

Low-Power CMOS SRAMs Product Cross Reference

64K, 256K, and 1M Static RAMs

Vendors	Fujitsu Part Numbers		
	MB8464A (8K x 8)	**MB84256A (32K x 8/OE)**	**MB841000 (128K x 8/OE)**
Hitachi	HM6264 and 6264A	HM62256	HM628128
Mitsubishi	M5M5165	M5M52256	M5M51008
Motorola	MCM6064	MCM60256	
NEC	µPD4464	µPD43256A	µPD431000A
OKI	MSM5165	MSM51256 and 51257	
Samsung	KM6264	KM62256	KM681000
Sharp	LH5164	LH51256	
Sony	CXK5864	CXK58257	CXK581000
Toshiba	TC5565 and 5563	TC55256 and 55257	TC551001

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FUJITSU

DATA SHEET

MB8464A-80/-80L/-80LL/-10/-10L/-10LL/-15/-15L/-15LL
CMOS 64K BIT LOW POWER SRAM

8K Words x 8 Bits CMOS Static RAM with Low Power and Data Retention

The Fujitsu MB8464A is a 8,192 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

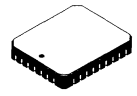
The MB8464A has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 8,192 words x 8 bits
- Access time: 80 ns max. (MB8464A-80/-80L/-80LL)
  100 ns max. (MB8464A-10/-10L/-10LL)
  150 ns max. (MB8464A-15/-15L/-15LL)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby: 11 mW max. (MB8464A-80/-10/-15)
  0.55 mW max. (MB8464A-80L/-10L/-15L)
  0.55 mW max. (MB8464A-80LL/-10LL/-15LL)
- Data retention current: 1 mA max. (MB8464A-80/-10/-15)
  25 µA max. (MB8464A-80L/-10L/-15L)
  2 µA max. at 0°C to 40°C (MB8464A-80LL/-10LL/-15LL)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  DIP (600 mil) MB8464A-xx(L/LL)P
  Skinny DIP (300 mil) MB8464A-xx(L/LL)PSK
  SOP (450 mil) MB8464A-xx(L/LL)PF
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB8464A-xx(L/LL)CV

PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04

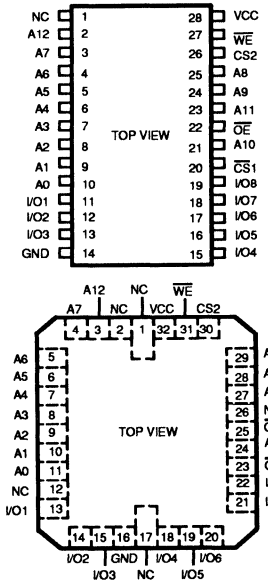
PLASTIC PACKAGE
FPT-28P-M02



CERAMIC PACKAGE
LCC-32C-A02

3

PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5* to V_{CC} +0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC} +0.5	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature Range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

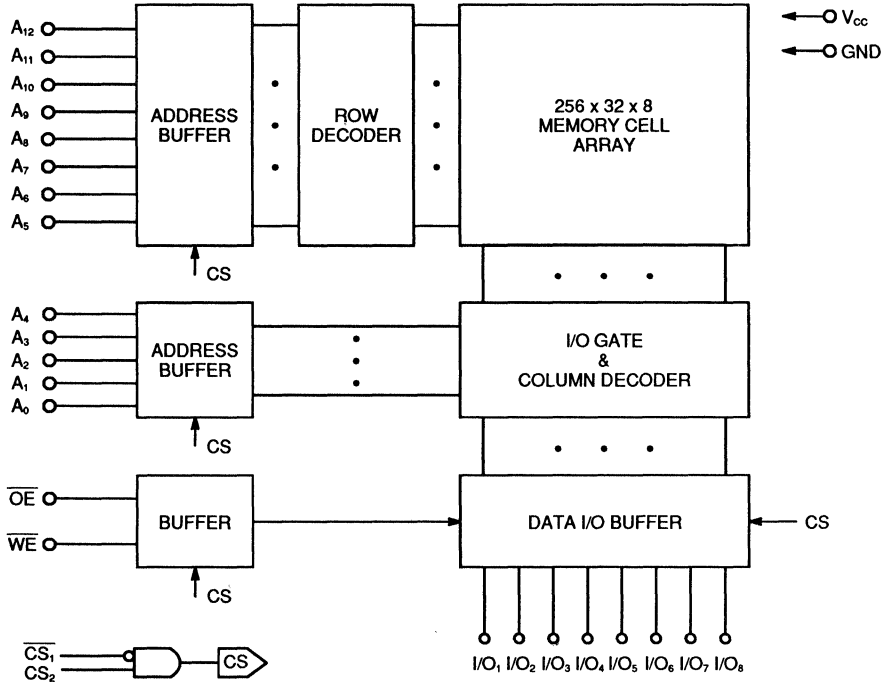
* −2.0 V for pulse width less than 20 ns.

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB8464A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	D_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

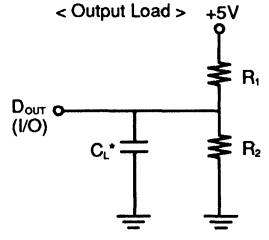
Parameter	Symbol	MB8464A-80/10/15		MB8464A-80L/80LL 10L/10LL/15L/15LL		Unit	Test Condition
		Min	Max	Min	Max		
Standby Supply Current	I_{SB1}		2		0.1	mA	$CS_2 \le 0.2V$, $\overline{CS_1} \ge V_{CC} - 0.2V$ ($CS_2 \le 0.2V$ or $CS_2 \ge V_{CC} - 0.2V$)
	I_{SB2}		3		3	mA	$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$
Active Supply Current	I_{CC1}		50		50	mA	$\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 0mA$
Operating Supply Current	I_{CC2}		60		60	mA	Cycle=Min., Duty=100% $I_{OUT} = 0mA$
Input Leakage Current	I_{LI}	−1	1	−1	−1	µA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	$I_{LI/O}$	−2	2	−2	2	µA	$V_{I/O} = 0V$ to V_{CC} $\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Input Low Voltage	V_{IL}	−2.0*	0.8	−2.0*	0.8	V	
Input High Voltage	V_{IH}	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V	
Output High Voltage	V_{OH}	2.4		2.4		V	$I_{OH} = -1.0mA$
Output Low Voltage	V_{OL}		0.4		0.4	V	$I_{OL} = 2.1mA$

* −2.0V Min for pulse width less than 20ns. (V_{IL} Min.=−0.3V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels: Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.0V
- Output Load:

	R_1	R_2	C_L	Parameters Measured
Load I	1.8kΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8kΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ} t_{OHZ} t_{WLZ}, and t_{WHZ}



* Including jig and stray capacitance

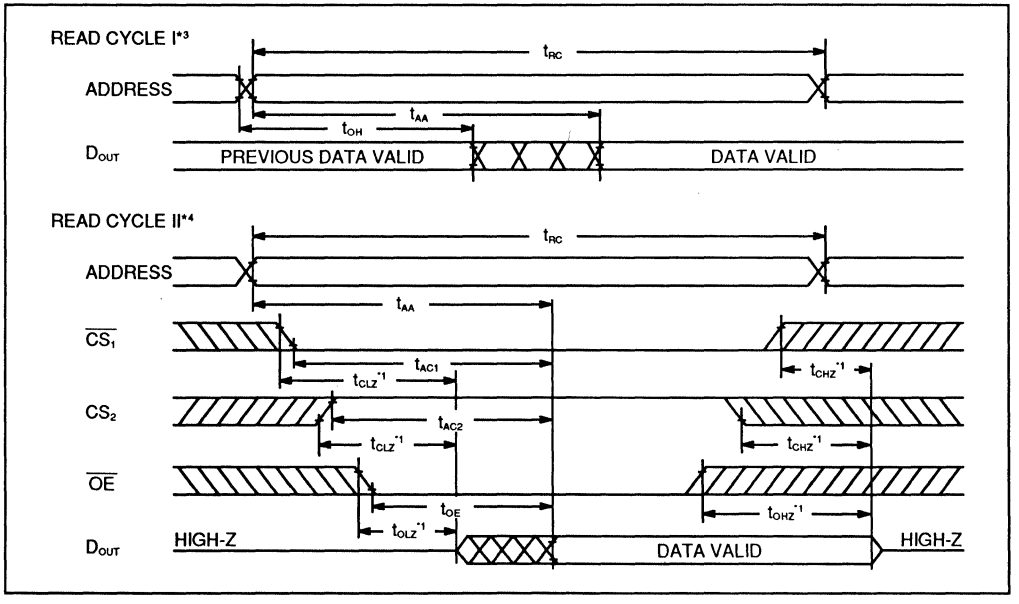
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8464A-80/80L/80LL		MB8464A-10/10L/10LL		MB8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		150		ns
Address Access Time	t_{AA}		80		100		150	ns
$\overline{CS_1}$ Access Time	t_{AC1}		80		100		150	ns
CS_2 Access Time	t_{AC2}		80		100		150	ns
Output Enable to Output Valid	t_{OE}		35		45		55	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output Low-Z*1	t_{CLZ}	10		10		10		ns
Output Enable to Output Low-Z*1	t_{OLZ}	5		5		5		ns
Chip Select to Output High-Z*1	t_{CHZ}		35		35		40	ns
Output Enable to Output High-Z*1	t_{OHZ}		30		35		40	ns

READ CYCLE TIMING DIAGRAM *2

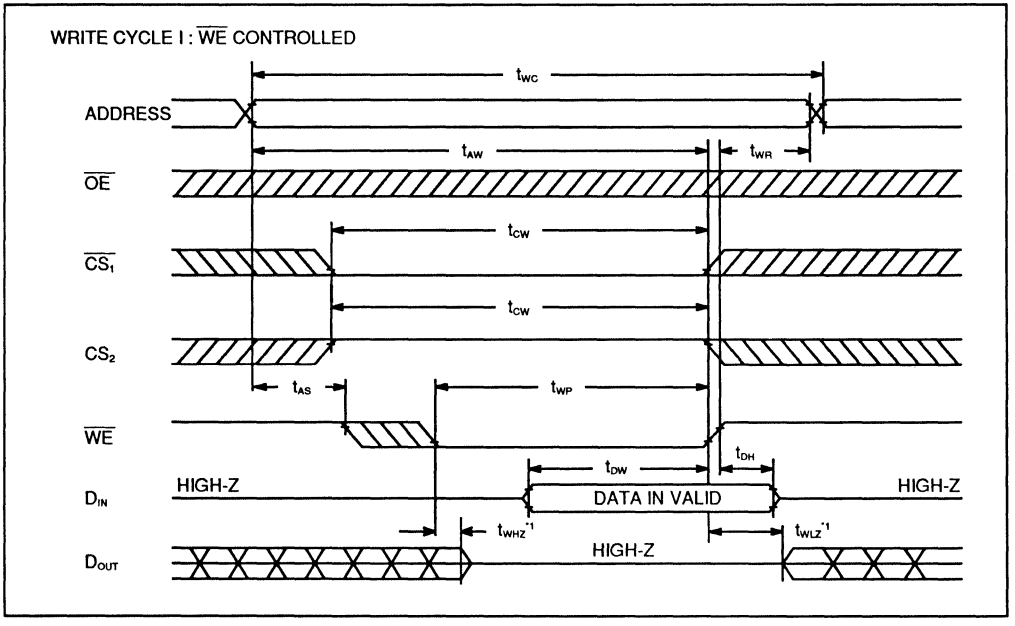


Note: *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 $\overline{WE}$ is high for Read Cycle.
*3 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.
*4 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

WRITE CYCLE

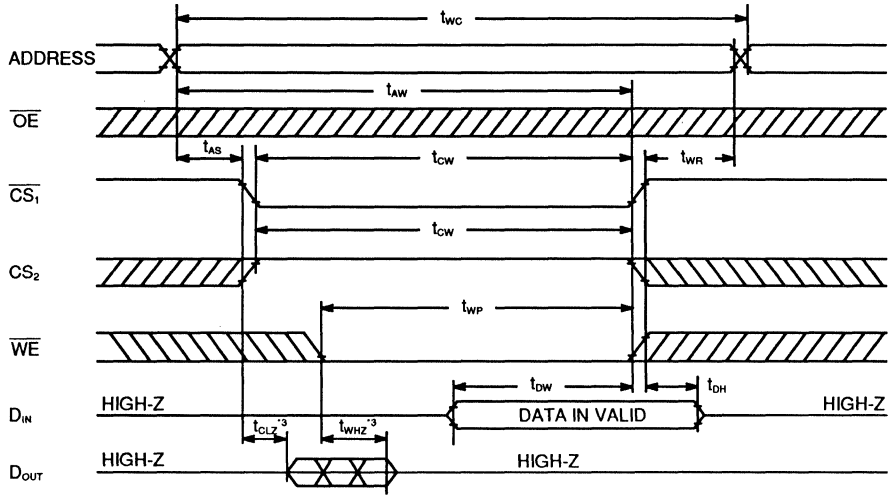
Parameter	Symbol	MB8464A-80/80L/80LL		MB8464A-10/10L/10LL		MB8464A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		150		ns
Address Valid to End of Write	t_{AW}	60		80		100		ns
Chip Select to End of Write	t_{CW}	60		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		ns
Data Hold Time	t_{DH}	5		5		5		ns
Write Pulse Width	t_{WP}	60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time	t_{WR}	5		5		5		ns
Write Enable to Output Low-Z*1	t_{WLZ}	5		5		5		ns
Write Enable to Output High-Z*1	t_{WHZ}		30		35		40	ns

WRITE CYCLE TIMING DIAGRAM *2

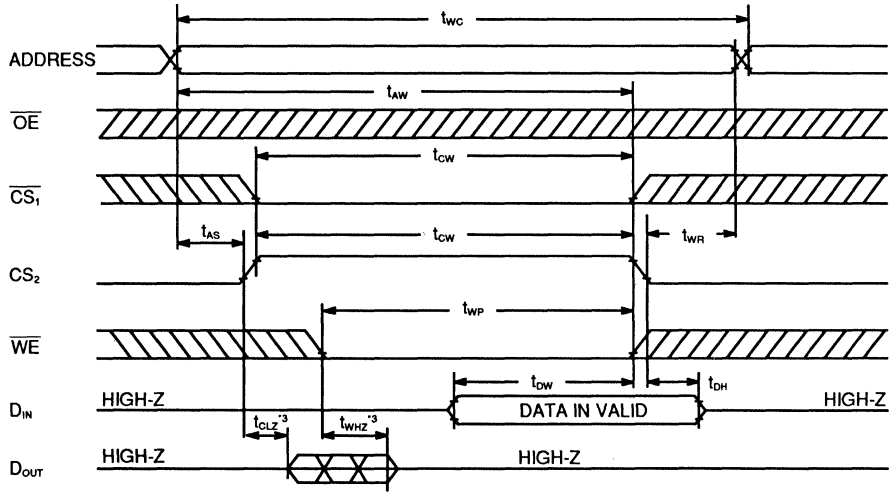


Note: *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE II : $\overline{CS_1}$ CONTROLLED*1



WRITE CYCLE III : CS_2 CONTROLLED*2



Note: *1 If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{OE}$, $\overline{CS_1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3 Transition is measured at the point of ±500mV from steady state voltage.

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

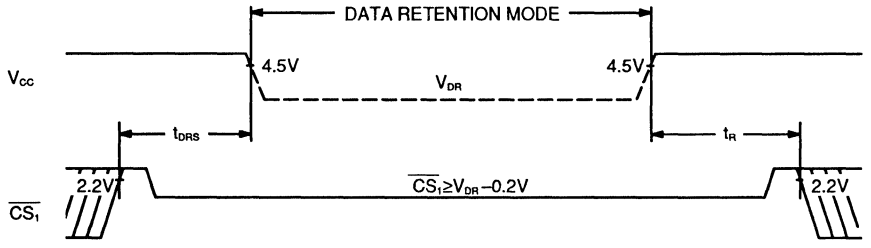
Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current*2	Standard	I_{DR}			1.0	mA
	L-Version			1.0	25	µA
	LL-Version*3			1.0	2.0	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *2 $\overline{CS_2}$ controlled: V_{DR}=3.0V, $\overline{CS_2}$≤0.2V
$\overline{CS_1}$ controlled: V_{DR}=3.0V, $\overline{CS_1}$≥V_{DR} −0.2V (CS_2≤0.2V or CS_2≥V_{DR} −0.2V)
*3 V_{DR}=3.0V, T_A=0°C to 40°C

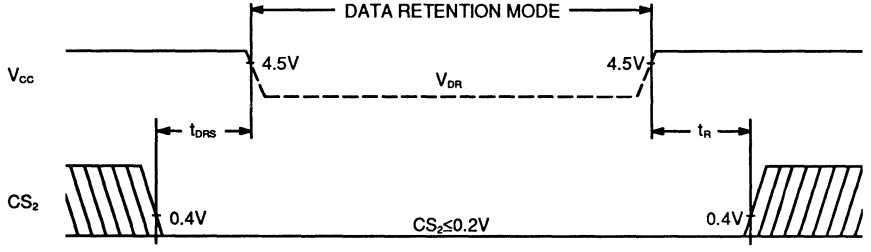
3

DATA RETENTION TIMING

DATA RETENTION I : $\overline{CS_1}$ CONTROLLED



DATA RETENTION II : CS_2 CONTROLLED



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

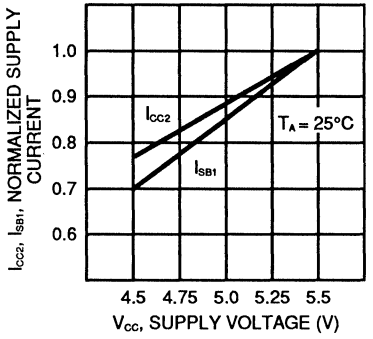


Fig. 4 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

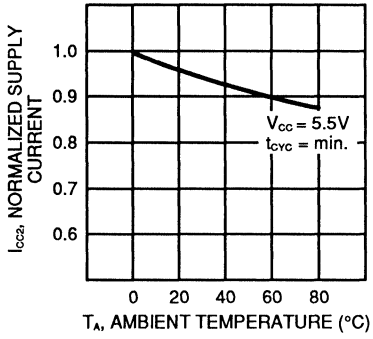


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. CYCLE TIME

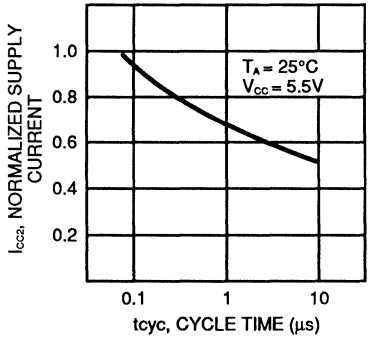


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

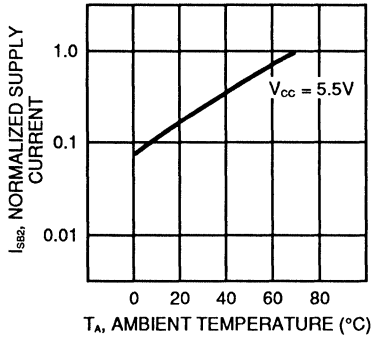


Fig. 7 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

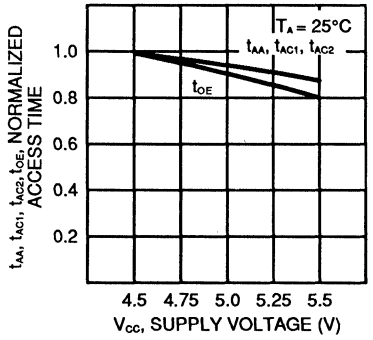
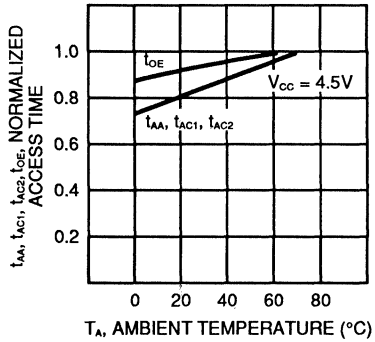


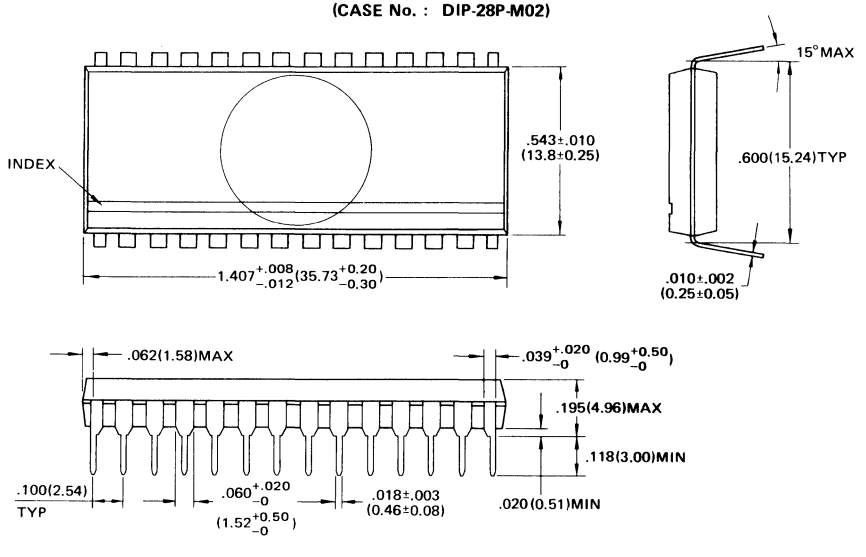
Fig. 8 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in
inches (millimeters)

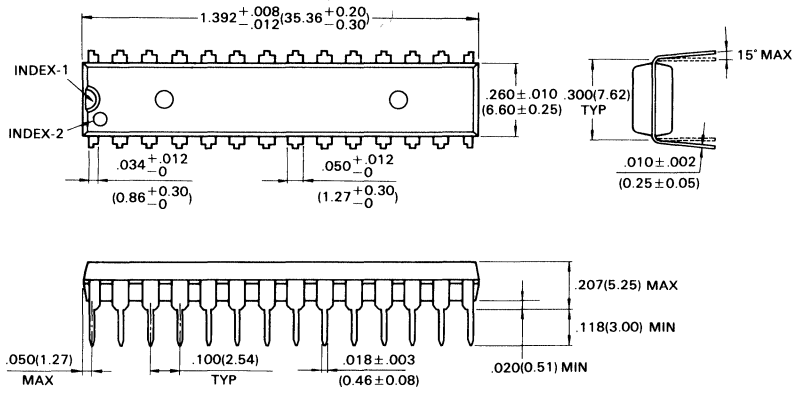
3

PACKAGE DIMENSIONS

(Suffix: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)



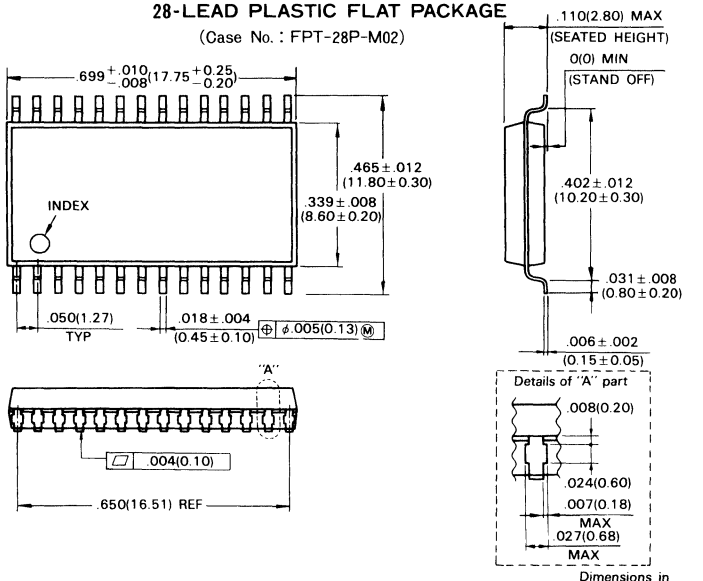
Dimensions in inches (millimeters)

3

PACKAGE DIMENSIONS (Cont'd)

(Suffix: PF)

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M02)



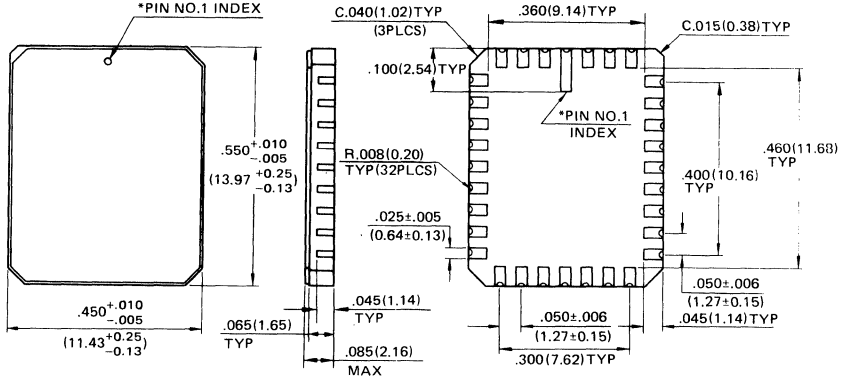
Dimensions in
inches (millimeters)

3

PACKAGE DIMENSIONS (Cont'd)

(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

September 1990
Edition 2.0

FUJITSU

DATA SHEET

MB84256A-70/70L/70LL/-10/10L/10LL/-12/12L/12LL/-15/15L/15LL
CMOS 256K-BIT LOW POWER SRAM

32K Words x 8 Bits CMOS Static Random Access Memory with Data Retention

The Fujitsu MB84256A is a 32,768 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB84256A has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

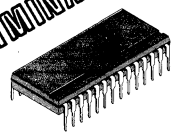
- Organization: 32,768 words x 8 bits
- Access time: 70 ns max. (MB84256A-70-/-70L/-70LL)
  100 ns max. (MB84256A-10/-10L/-10LL)
  120 ns max. (MB84256A-12/-12L/-12LL)
  150 ns max. (MB84256A-15/-15L/-15LL)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V power supply ±10% tolerance
- Low power standby:
  CMOS level 5.5 mW max. (MB84256A-70/-10/-12/-15)
  0.55 mW max. (MB84256A-70L/-70LL/-10LL, -12L/-12LL/-15LL)
  TTL level 16.5 mW max. (MB84256A-70/-70L/-70LL/-10L/-10LL, -12/-12L/-12LL/-15L/-15LL)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  DIP (600 mil) MB84256A-xx(L/LL)P
  Skinny DIP (300 mil) MB84256A-xx(L/LL)PSK
  SOP MB84256A-xx(L/LL)PF
  TSOP (normal bend) MB84256A-xx(L/LL)PFTN
  TSOP (reverse bend) MB84256A-xx(L/LL)PFTR

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

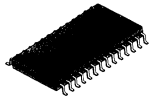
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY



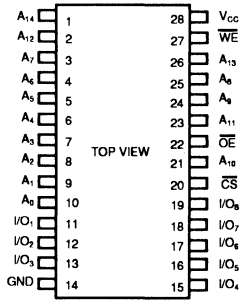
PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02
*TSOP packages: PFTN/PFTR

PIN ASSIGNMENT

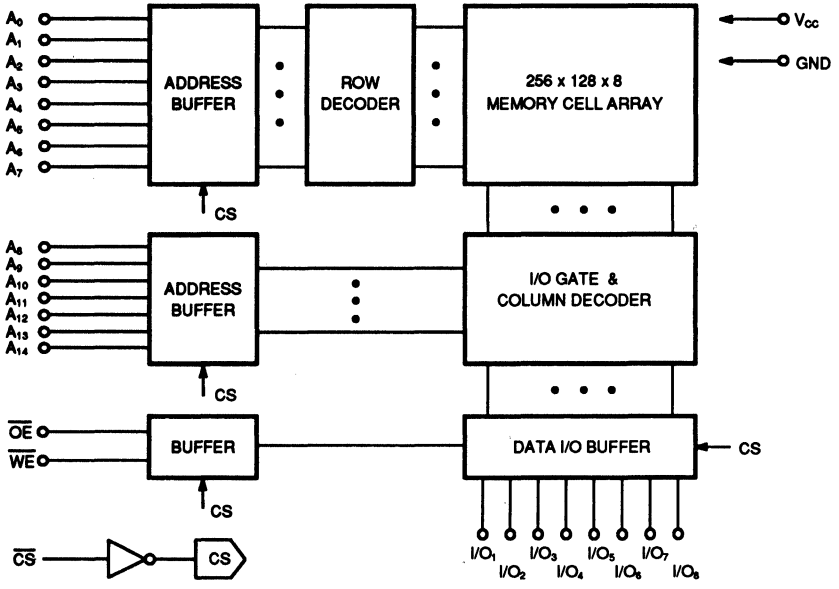


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

3

Fig. 1 – MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

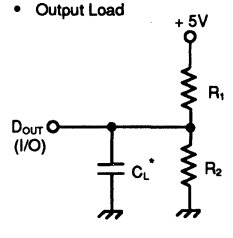
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Condition	MB84256A-70/10 /12/15		MB84256A-70L/70LL /10L/10LL/12L/12LL /15L/15LL		Unit
				Min	Max	Min	Max	
Standby Supply Current		I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$		1		0.1	mA
		I_{SB2}	$\overline{CS} = V_{IH}$		3		3	mA
Active Supply Current		I_{CC1}	$V_{IN} = V_{IH}$ or V_{IL}, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA		60		60	mA
Operating Supply Current	-70	I_{CC2}	Cycle = Min. Duty = 100% I_{OUT} = 0mA		80		80	mA
	-10/12/15				70		70	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	–1	1	–1	1	µA
Output Leakage Current		$I_{LI/O}$	$V_{I/O}$ = 0V to V_{CC}, $\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	–1	1	–1	1	µA
Input High Voltage		V_{IH}		2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
Input Low Voltage		V_{IL}		–3.0 *	0.8	–3.0 *	0.8	V
Output High Voltage		V_{OH}	I_{OH} = –1.0mA	2.4		2.4		V
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA		0.4		0.4	V

Note: All voltages are referenced to GND.
*: –3.0V min. for pulse width less than 20 ns.(V_{IL} min. = –0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.8V, V_{IH}=2.2V; Output: V_{OL}=0.8V, V_{OH}=2.0V

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

AC CHARACTERISTICS

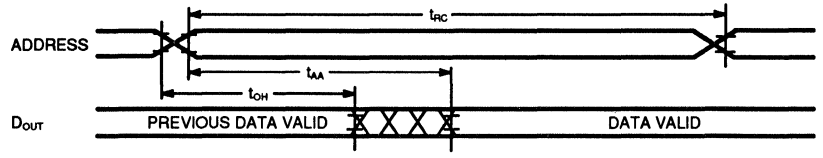
(Recommended operating conditions otherwise noted.)

READ CYCLE *1

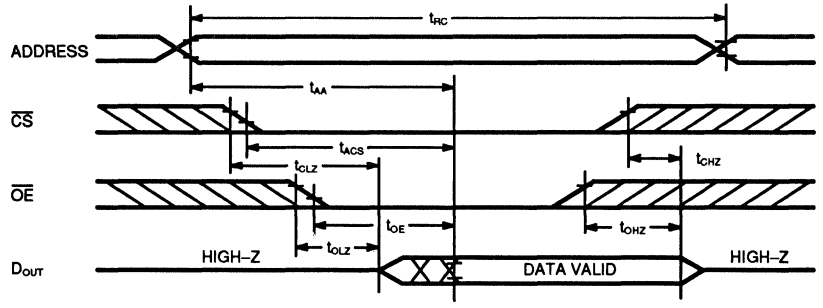
Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		150		ns
Address Access Time *2	t_{AA}		70		100		120		150	ns
$\overline{CS}$ Access Time *3	t_{ACS}		70		100		120		150	ns
Output Enable to Output Valid	t_{OE}		35		40		50		60	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		ns
Chip Select to Output Low–Z *4	t_{CLZ}	10		10		10		10		ns
Output Enable to Output Low–Z *4	t_{OLZ}	5		5		5		5		ns
Chip Select to Output High–Z *4	t_{CHZ}		25		40		40		50	ns
Output Enable to Output High–Z *4	t_{OHZ}		25		40		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED*2



READ CYCLE 2: $\overline{CS}$ CONTROLLED*3

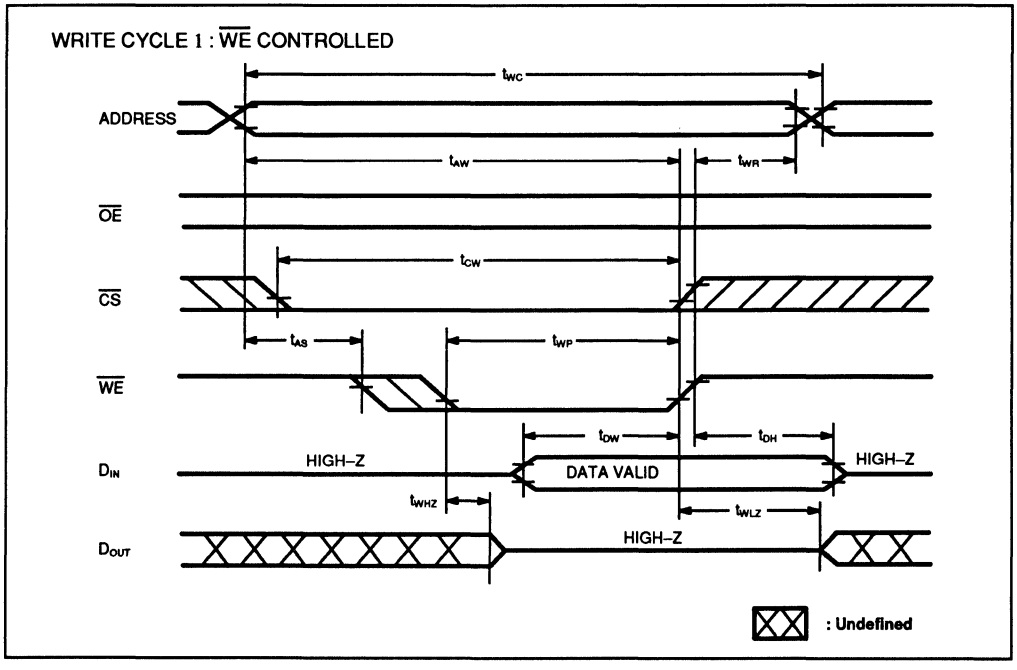


Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE *1*2

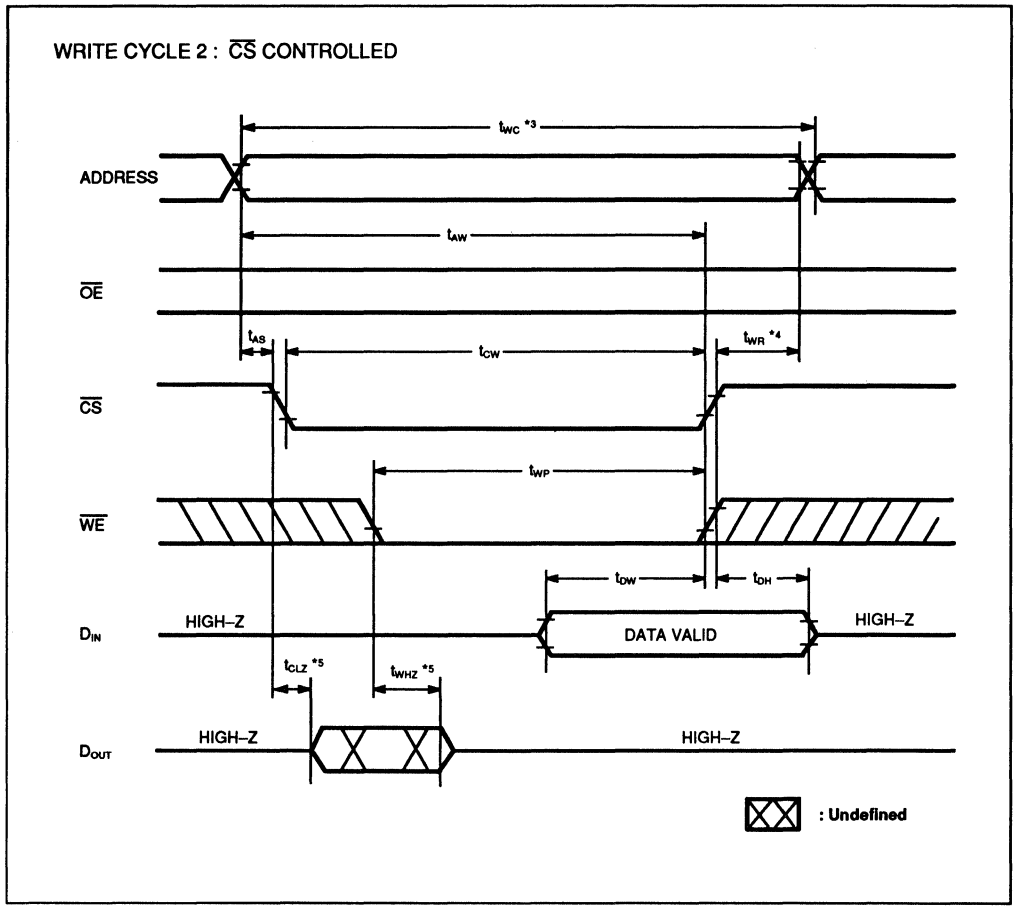
Parameter	Symbol	MB84256A-70/70L/70LL		MB84256A-10/10L/10LL		MB84256A-12/12L/12LL		MB84256A-15/15L/15LL		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	70		100		120		150		ns
Address Valid to End of Write	t_{AW}	50		80		85		100		ns
Chip Select to End of Write	t_{CW}	50		80		85		100		ns
Data Valid to End of Write	t_{DW}	25		40		45		50		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Pulse Width	t_{WP}	50		60		70		90		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Write Recovery Time *4	t_{WR}	5		5		5		5		ns
$\overline{WE}$ to Output Low–Z *5	t_{WLZ}	5		5		5		5		ns
$\overline{WE}$ to Output High–Z *5	t_{WHZ}		25		40		40		50	ns

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycle are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode..
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load I in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode..

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

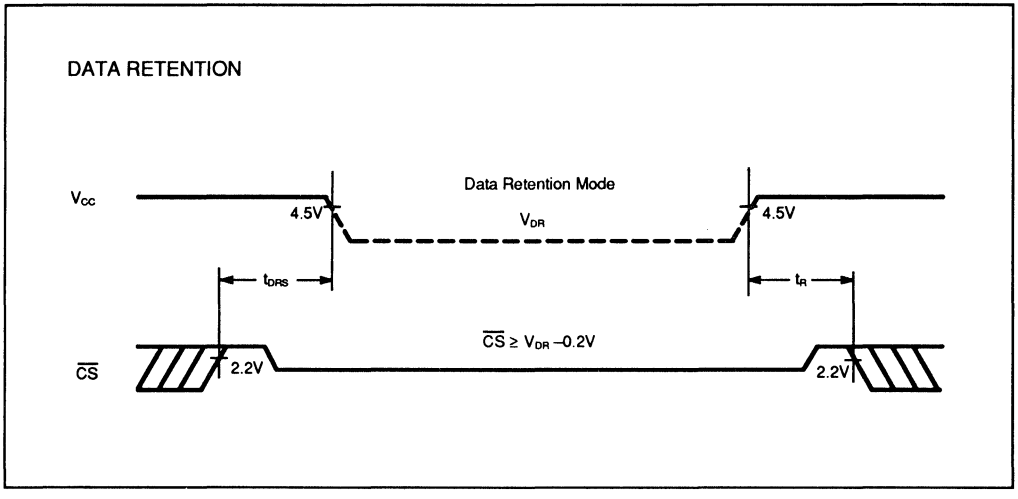
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1		V_{DR}	2.0		5.5	V
Data Retention Supply Current *2	Standard	I_{DR}			1.0	mA
	L-Version			1.0	50	µA
	LL-Version *3			1.0	5.0	
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $\overline{CS} \geq V_{DR} - 0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geq V_{DR} - 0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

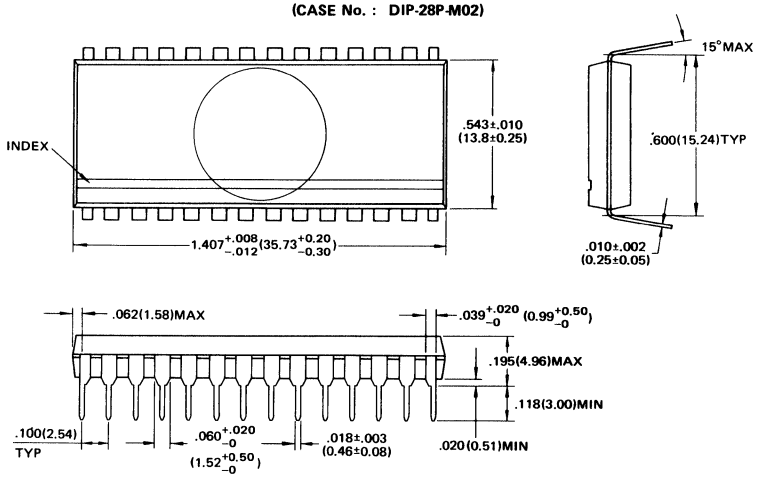
DATA RETENTION TIMING



PACKAGE DIMENSIONS

(Suffix: P)

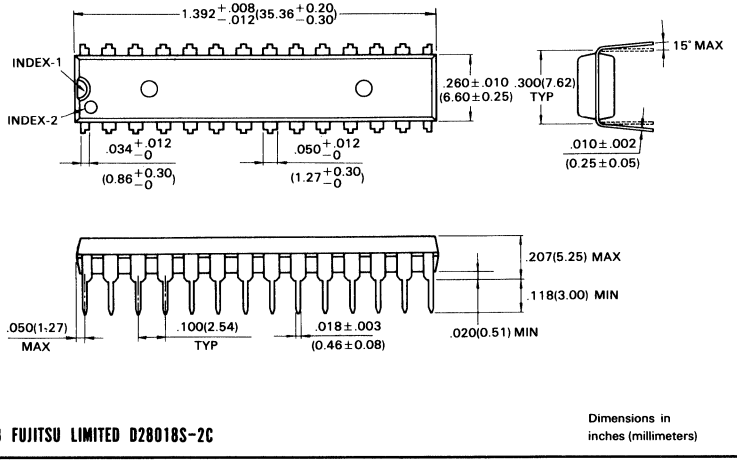
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in
inches (millimeters)

(Suffix: P-SK)

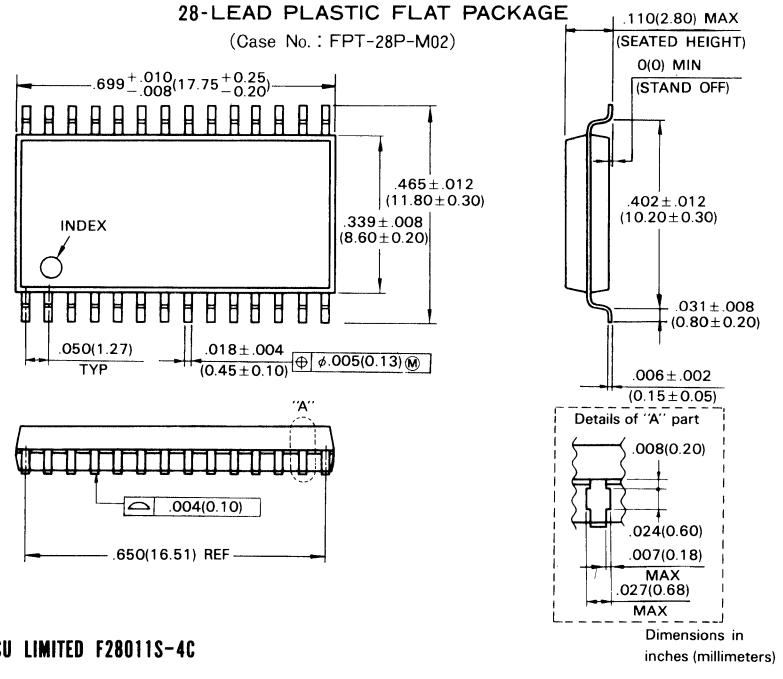
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)

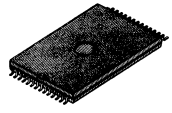


Dimensions in inches (millimeters)

3

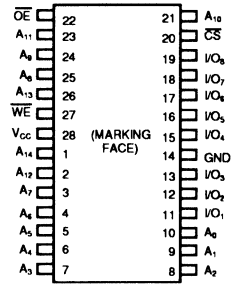
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



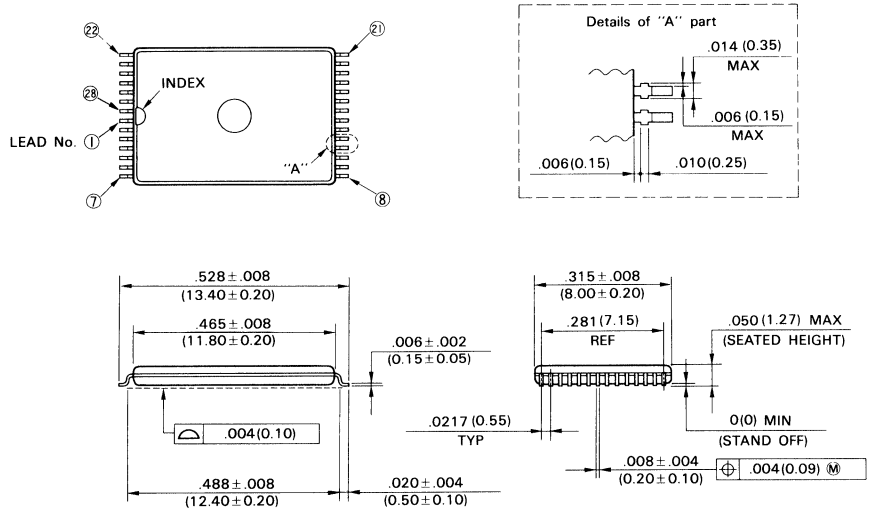
FPT-28P-M03

PIN ASSIGNMENT
(NORMAL BEND)



TOP VIEW

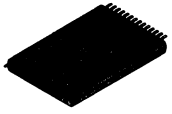
28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M03)



Dimensions in inches (millimeters)

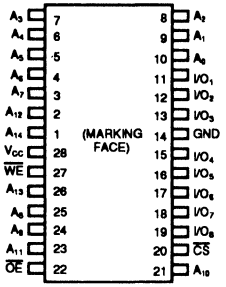
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



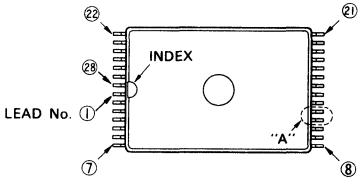
FPT-28P-M04

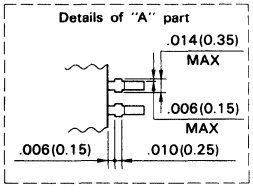
PIN ASSIGNMENT
(REVERSE BEND)

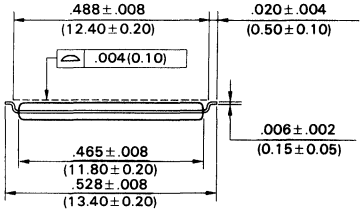


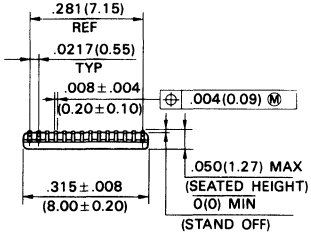
BOTTOM VIEW

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M04)









Dimensions in
inches (millimeters)

3

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July 1990
Edition 2.0

FUJITSU

DATA SHEET

MB841000-80/-80L/-10/-10L/-12/-12L
CMOS 1M LOW POWER SRAM

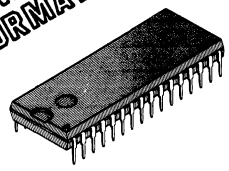
128K Words x 8 Bits CMOS Static Random Access Memory with Data Retention

The Fujitsu MB841000 is a 131,072 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and it may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

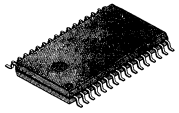
The MB841000 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 131,072 words x 8 bits
- Access time: 80 ns max. (MB841000-80/80L)
  100 ns max. (MB841000-10/10L)
  120 ns max. (MB841000-12/12L)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V power supply ±10% tolerance
- Low power standby:
  CMOS level 5.5 mW max. (MB841000-80/-10/-12)
  1.1 mW max. (MB841000-80L/-10L/-12L)
  TTL level 16.5 mW max. (MB841000-80/-80L,-10/-10L,-12/12L)
- Data retention voltage: 2.0 V min.
- Standard 32-pin Plastic Packages:
  DIP (600 mil) MB841000-xx(L)P
  SOP (525 mil) MB841000-xx(L)PF

ADVANCE INFORMATION



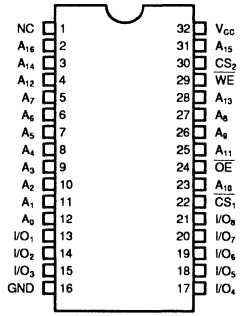
PLASTIC PACKAGE
(DIP-32P-M01)



PLASTIC PACKAGE
(FPT-32P-M03)

PIN ASSIGNMENT

TOP VIEW



Absolute Maximum Ratings (See Note)

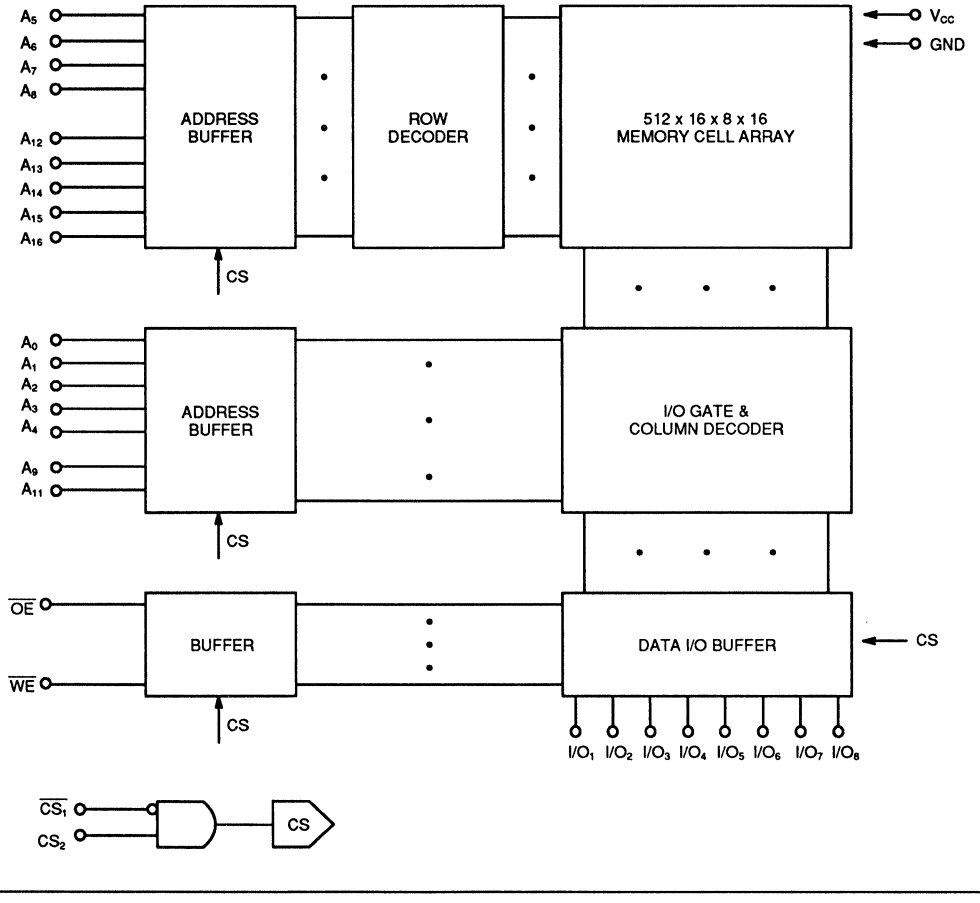
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — MB841000 BLOCK DIAGRAM



CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			10	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			8	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A_0 to A_{16}	Address Input	$\overline{WE}$	Write Enable
I/O_1 to I/O_8	Data Input/Output	V_{CC}	Power Supply (50±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS_1}$	Chip Select 1	NC	No Connect
CS_2	Chip Select 2		

FUNCTION TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High–Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

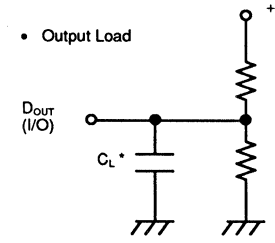
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	MB841000 -80/10/12		MB841000 -80L/10L/12L		Unit
			Min	Max	Min	Max	
Standby Supply Current	$CS_2 \leq 0.2V$ or $\overline{CS_1} \geq V_{CC}-0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{CC}-0.2V$)	I_{SB1}		1		0.2	mA
	$\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$	I_{SB2}		3		3	mA
Active Supply Current	$V_{IN}=V_{IH}$ or V_{IL}, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ $I_{OUT}=0mA$	I_{CC1}		5		5	mA
Operating Supply Current	Cycle=Min. Duty=100%, $I_{OUT}=0mA$	I_{CC2}		80		80	mA
Input Leakage Current	$V_{IN}=0V$ to V_{CC}	I_{LI}	–1	1	–1	1	µA
Output Leakage Current	$V_{I/O}=0V$ to V_{CC} $\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	$I_{LI/O}$	–2	2	–2	2	µA
Input High Voltage		V_{IH}	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	–0.3*	0.8	–0.3*	0.8	V
Output High Voltage	$I_{OH}=-1.0mA$	V_{OH}	2.4		2.4		V
Output Low Voltage	$I_{OL}=2.1mA$	V_{OL}		0.4		0.4	V

Note : All voltages are referenced to GND.
*** :** –3.0V min. for pulse width less than 20 ns. (V_{IL} min. = –0.3V at DC level.)

Fig.2 – AC TEST CONDITIONS



- Output Load
- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : $V_{IL}=0.8V, V_{IH}=2.2V$
  Output : $V_{OL}=0.8V, V_{OH}=2.0V$

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	MB841000–80/80L		MB841000–10/10L		MBM841000–12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		120		ns
Address Access Time *2	t_{AA}		80		100		120	ns
$\overline{CS_1}$ Access Time *3	t_{AC1}		80		100		120	ns
CS_2 Access Time *3	t_{AC2}		80		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select to Output Low–Z *4	t_{CLZ}	10		10		10		ns
Output Enable to Output Low–Z *4	t_{OLZ}	5		5		5		ns
Chip Select to Output High–Z *4	t_{CHZ}		30		35		40	ns
Output Enable to Output High–Z *4	t_{OHZ}		30		35		40	ns

Note: *1 $\overline{WE}$ is high for Read cycle.

*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.

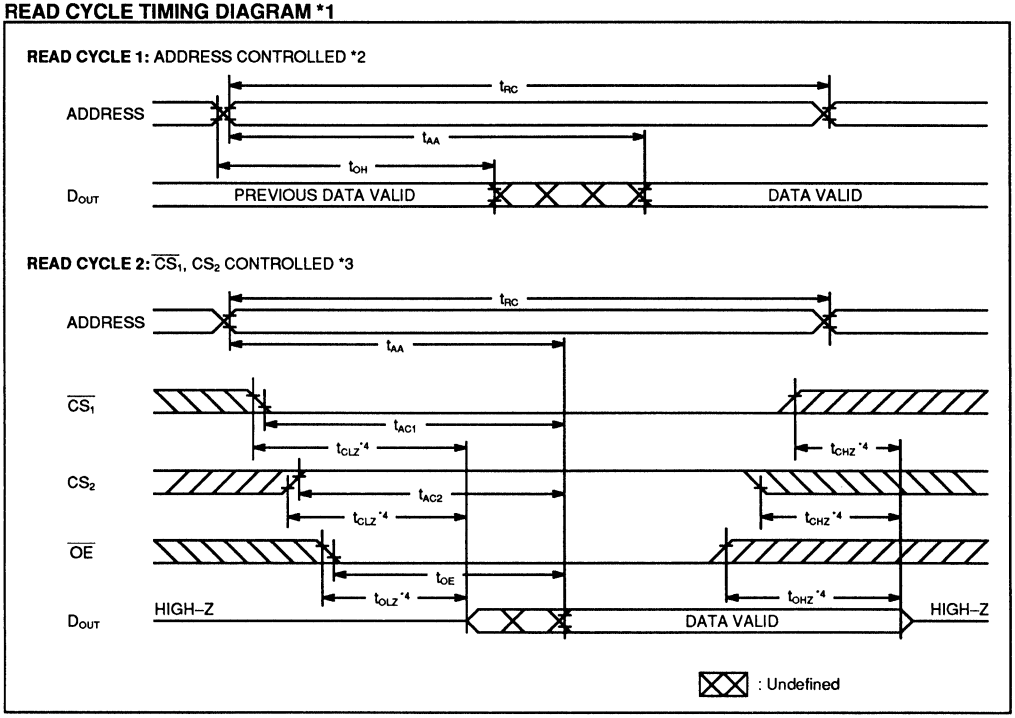
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig.2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.

*2 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=V_{IH}.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	MB841000–80/80L		MB841000–10/10L		MBM841000–12/12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	80		100		120		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Data Valid to End of Write	t_{DW}	30		40		45		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	50		60		70		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time *4	t_{WR}	5		5		5		ns
Write Enable to Output Low–Z *5	t_{WLZ}	5		5		5		ns
Write Enable to Output High–Z *5	t_{WHZ}		30		35		40	ns

Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

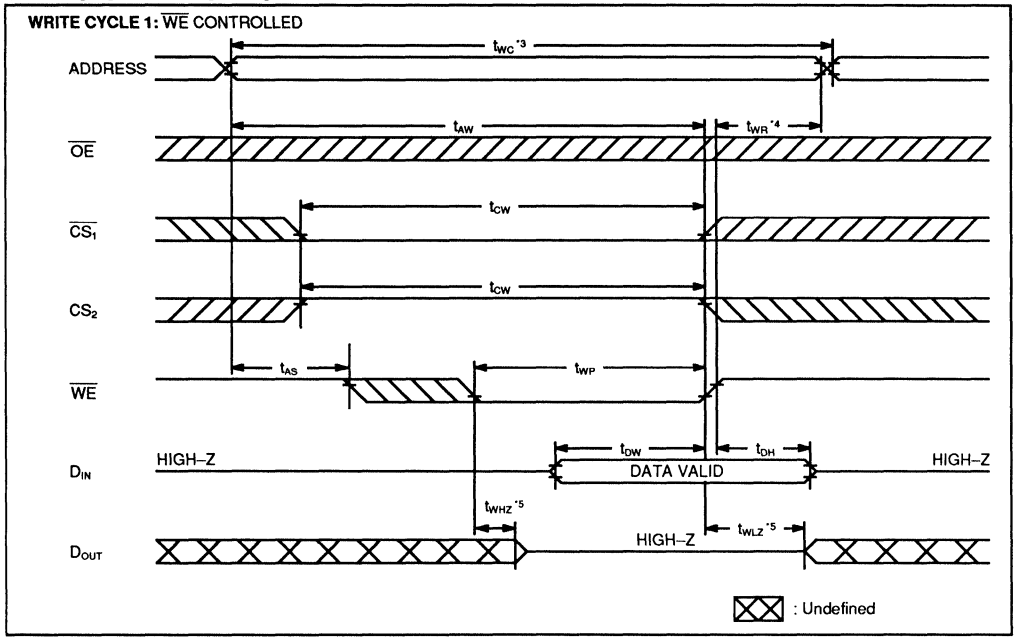
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig.2.

3

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

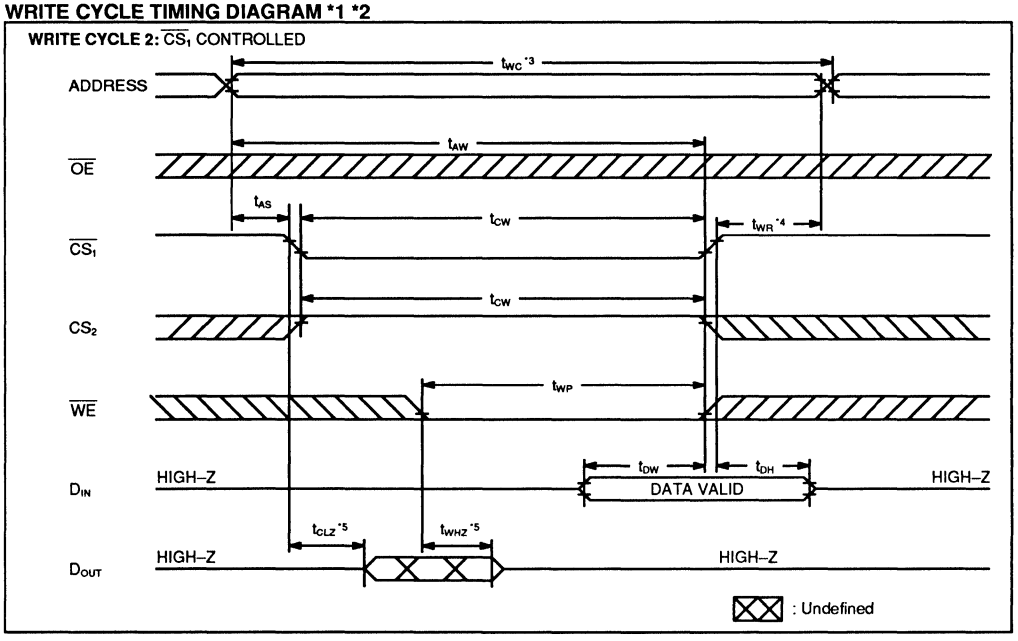
*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

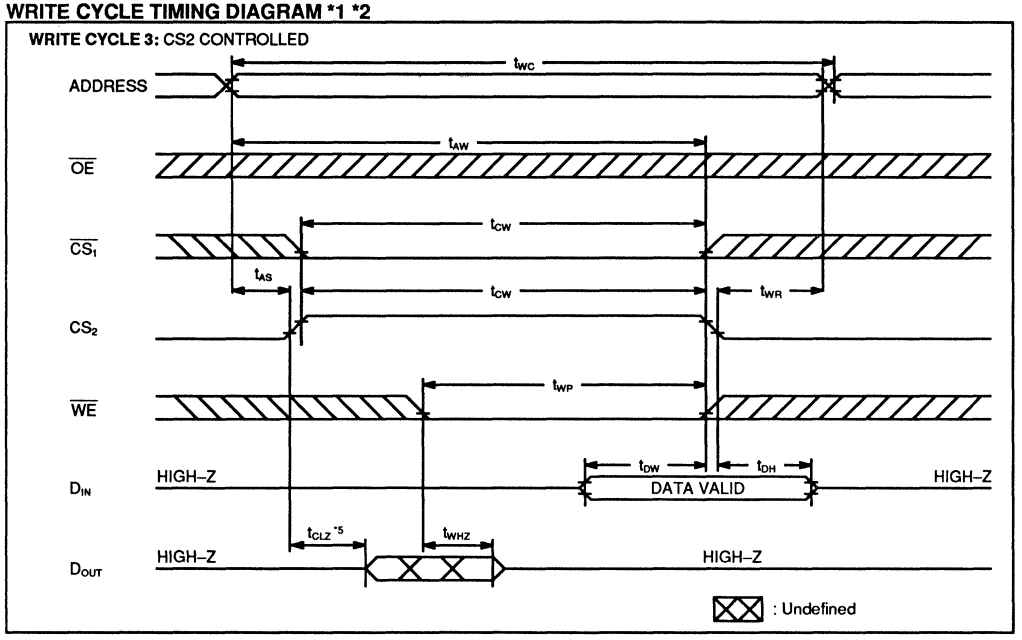
*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Note: *1 If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycle are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode.

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

DATA RETENTION CHARACTERISTICS

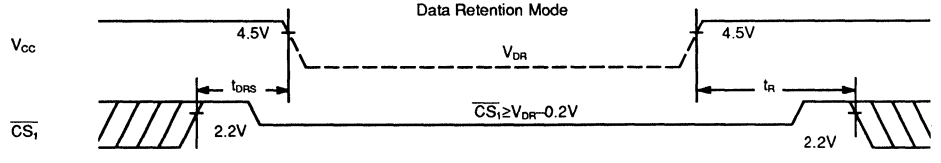
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			0.5	mA
	L-Version				0.1 *2	mA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time *2		t_R	t_{RC}			ns

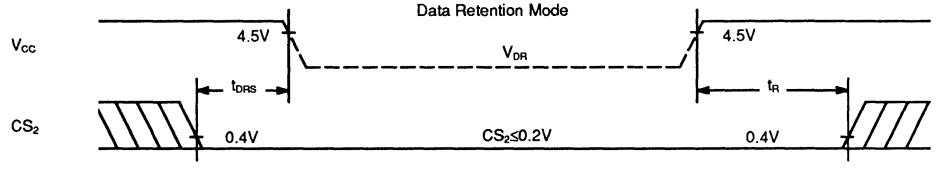
Note: *1 V_{CC}=V_{DR}=3.0V
$\overline{CS_1} \geq V_{DR} - 0.2V$, $CS_2 \geq V_{DR} - 0.2V$ or $CS_2 \leq 0.2V$ (at $\overline{CS_1}$ CONTROLLED)
$CS_2 \leq 0.2V$ (at CS_2 CONTROLLED)
*2 t_{RC}: Read Cycle Time

DATA RETENTION TIMING

$\overline{CS_1}$ CONTROLLED



CS_2 CONTROLLED

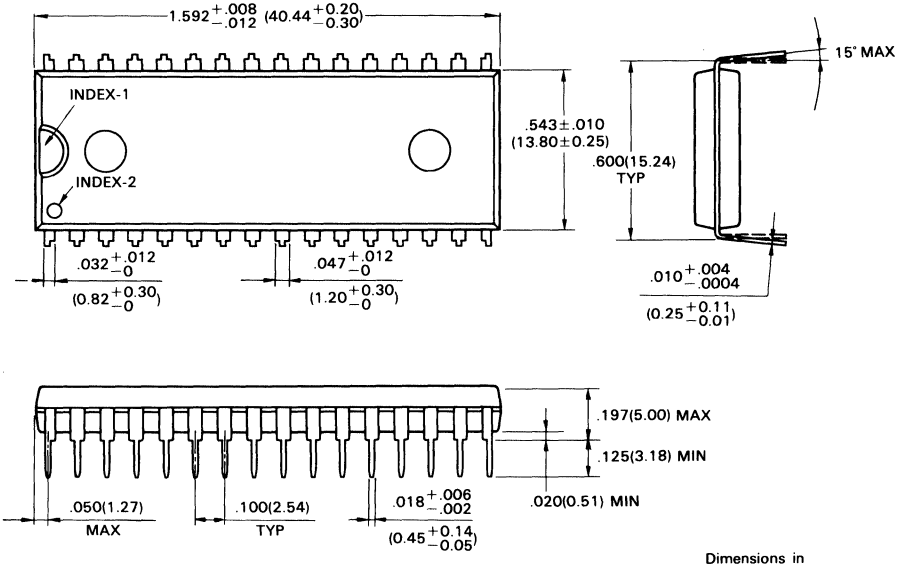


PACKAGE DIMENSIONS

(Suffix: P)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-32P-M01)

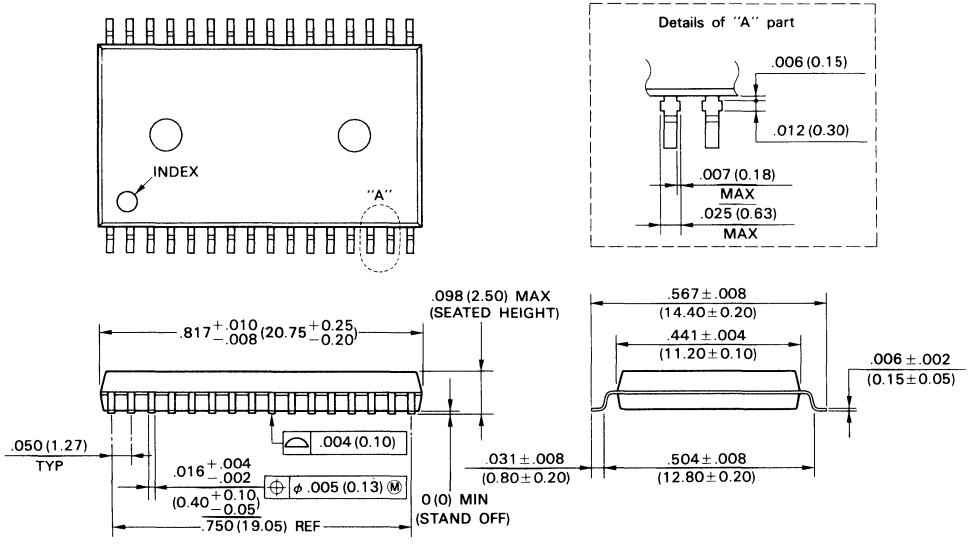


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

32-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-32P-M03)



Dimensions in
inches (millimeters)

3

Section 4

Application Specific CMOS SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity (Organization)	Package Options
4–3	MB81C51–25	25	2048 bits	64-pin Ceramic PGA
	–30	30	(512 x 4-way) or (1024 x 2-way)	
4–17	MB81C79B–35	35	73728 bits	28-pin Plastic DIP, SOP
	–45	45	(8192 x 9)	
4–29	MB8279RT–20	20	73728 bits	32-pin Plastic DIP, SOP
	–25	25	(8192 x 9)	
4–41	MB8287–25	25	262144 bits	32-pin Plastic DIP, SOP
	–35	35	(32768 x 8)	
4–53	MB8421–90, –90L and LL	90	16384 bits	48-pin Plastic DIP
	–12, –12L and LL	120	(2048 x 8)	52-pin Plastic DIP
				64-pin Plastic SOP
	MB8422–90, –90L and LL	90		
	–12, –12L and LL	120		
4–67	MB8431–90, –90L and LL	90	16384 bits	48-pin Plastic DIP
	–12, –12L and LL	120	(2048 x 8)	52-pin Plastic DIP
				64-pin Plastic SOP
	MB8432–90, –90L and LL	90		
	–12, –12L and LL	120		
4–85	MB8441–45	45	65536 bits	64-pin Plastic QFP
	–55	55	(8192 x 8)	

4

4

February 1990
Edition 2.0

FUJITSU

DATA SHEET

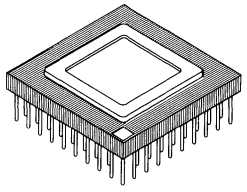
MB81C51-25/-30
CMOS TAG RANDOM ACCESS MEMORY

CMOS Tag Random Access Memory

The Fujitsu MB81C51 is a 512 entry x 4 way or 1024 entry x 2 way tag random access memory (Tag RAM) fabricated with CMOS technology.

The MB81C51 is ideal for use in cache memory systems with other RAMs. This device offers the advantages of compact design and high performance in cache systems for use with 32-bit CPUs.

- Organization: 512 Entry x 4 way or 1024 Entry x 2 way
- Access time: 30 ns max from Address Inputs 18 ns max from Compare Data Inputs
- Power consumption: 1375 mW max.
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- LRU (Least Recently Used) replacement logic
- Purge function (All-purge and partial-purge)
- Internal parity generator/checker
- Standard 64-pin Ceramic Pin Grid Array Package:
  PGA MB81C51-xxCR



PGA-64C-A02
(PIN GRID ARRAY)

4

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.0 to +7	V
Output Voltage on any pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB81C51 BLOCK DIAGRAM 1

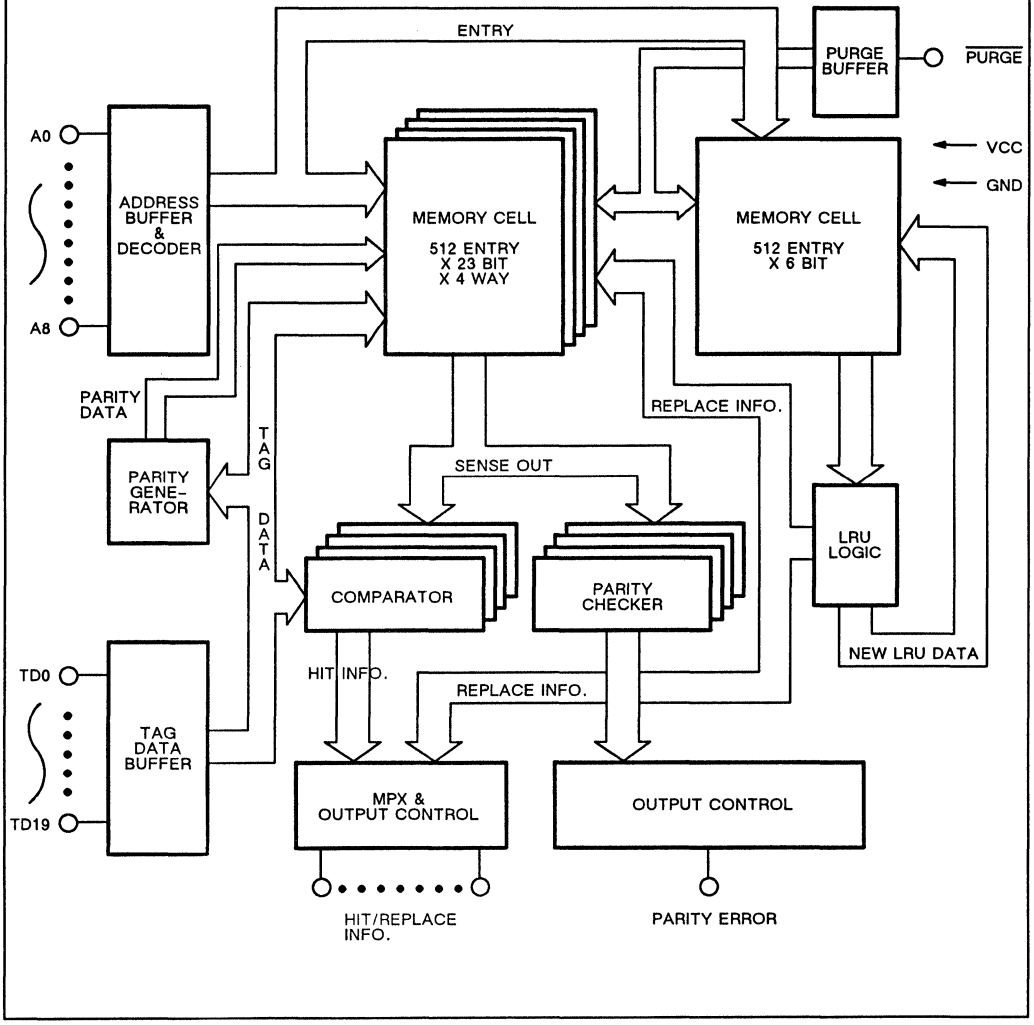
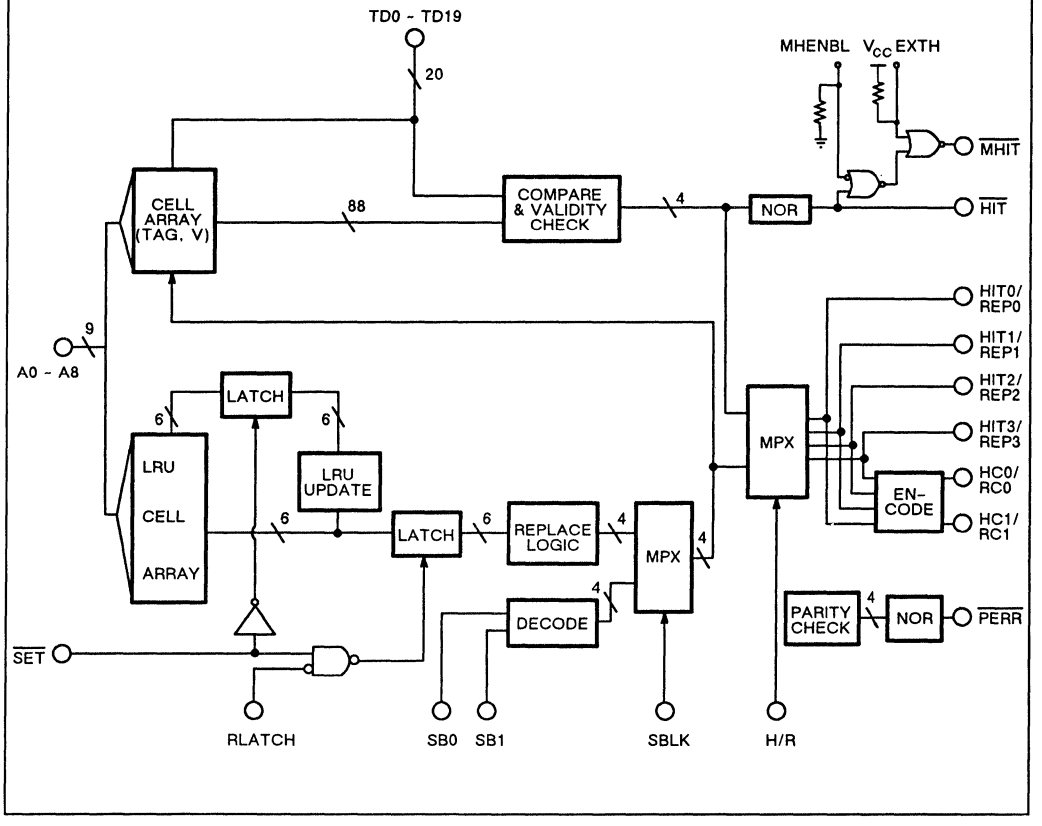


Fig. 2 — MB81C51 BLOCK DIAGRAM 2



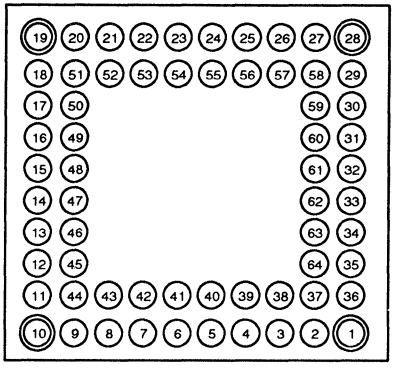
4

CAPACITANCE (T_A = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		10	pF

PIN ASSIGNMENT

64 PIN PIN GRID ARRAY(PGA-64C-A02)



BOTTOM VIEW

4

PIN FUNCTION

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A4	45	TD6
2	$\overline{\text{MHIT}}$	24	A5	46	TD9
3	HIT0/REP0	25	A7	47	Vcc
4	HIT2/REP2	26	A9	48	TD13
5	HIT3/REP3	27	N.C.	49	TD15
6	TD0	28	N.C.	50	TD17
7	TD2	29	$\overline{\text{PINV}}$	51	TD19
8	EXTH	30	SBLK	52	A0
9	MHENBL	31	SB1	53	A2
10	N.C.	32	$\overline{\text{INH}}$	54	GND
11	TD7	33	$\overline{\text{INVL}}$	55	A6
12	TD8	34	$\overline{\text{SET}}$	56	A8
13	TD10	35	H/R	57	$\overline{\text{PURGE}}$
14	TD11	36	$\overline{\text{HIT}}$	58	MODE
15	TD12	37	HC0/RC0	59	$\overline{\text{VINV}}$
16	TD14	38	HC1/RC1	60	SB0
17	TD16	39	HIT1/REP1	61	Vcc
18	TD18	40	GND	62	$\overline{\text{WRITE}}$
19	N.C.	41	TD1	63	RLATCH
20	N.C.	42	TD3	64	$\overline{\text{PERR}}$
21	A1	43	TD4		
22	A3	44	TD5		

PIN DESCRIPTION

OUTPUTS

$\overline{HIT}$	HIT OUTPUT. "NOR" OF HIT0 TO HIT3
HCn/RCn	CODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 1)
HITn/REPn	UNCODED OUTPUTS OF HIT OR REPLACE INFORMATION (n = 0 ~ 3)
$\overline{PERR}$	PARITY ERROR
$\overline{MHIT}$	HIT OUTPUT MODIFIED BY MHENBL AND EXTH

INPUTS

MODE	MODE SELECTION MODE = 1 : 512 Entry x 4 Way MODE = 0 : 1024 Entry x 2 Way
A0–A9	ADDRESS INPUTS (A9 is not used for 4 way)
TD0–19	TAG INFORMATION INPUTS
$\overline{PURGE}$	ALL-PURGE TIMING PULSE
$\overline{INVL}$	PARTIAL-PURGE. V-BIT FORCED TO "0". LRU IS REVERSIVELY UPDATED
SBLK	ENABLE WAY-SELECTION EXTERNALLY AT REPLACEMENT AND INVALIDATION
SB0, SB1	EXTERNAL WAY-ADDRESS INPUTS
$\overline{WRITE}$	WRITE CYCLE SIGNAL
$\overline{SET}$	TIMING PULSE Write : Registrate TAG, V-bit "H", LRU update Read : LRU updated PARTIAL PURGE : LRU reversively update, V-bit "L"
$\overline{INH}$	ALL FUNCTIONS EXCEPT PURGE ARE INHIBITED
H/R	OUTPUT SELECTION H/R = 1 : Hit Information H/R = 0 : Replace Information
RLATCH	LATCH CONTROL FOR REPLACE INFORMATION
$\overline{PINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
$\overline{VINV}$	USE FOR "TESTING" ONLY (GENERALLY "H")
MHENBL	ENABLE $\overline{MHIT}$ OUTPUT
EXTH	FORCE $\overline{MHIT}$ OUTPUT TO "L"

FUNCTION TABLE

1) BASIC FUNCTION (Any combination except below are inhibited.)

Input					TAG Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	TAG	P bit	V bit	LRU	Function Mode
L	H	X	X	X	N-CNG	N-CNG	N-CNG	N-CNG	INHIBIT[3]
H	H	H	X	X	N-CNG	N-CNG	N-CNG	N-CNG	TAG READ
H	H	⊓	H	H	N-CNG	N-CNG	N-CNG	N-CNG[1] or UP-D	TAG READ
H	H	⊓	L	H	TD0 to TD19	SET	H	UP-D	TAG WRITE
X	L	H	X	X	UNDEFINED	UNDEFINED	L (All)	INCLZ	ALL PURGE
H	H	⊓	H	L	N-CNG	N-CNG	N-CNG/L[2]	N-CNG[1] or RUP-D	PARTIAL PURGE

X : "H" or "L"
N-CNG : No Change INCLZ : INITIALIZE
UP-D : Up Dated RUP-D : Reversively Updated
1. When SBLK = "L" and no-HIT, then LRU is no change (N-CNG).
2. When SBLK = "L" and no-HIT, then V-Bit is no change (N-CNG).
3. During INHIBIT mode, $\overline{HIT}$ and $\overline{PERR}$ outputs are "H" but the other outputs are "L".

2) OUTPUT PIN FUNCTION

Input		Internal Info.[1, 2]				Output							
Mode	A9	hit0/ rep0	hit1/ rep1	hit2/ rep2	hit3/ rep3	HIT0/ REP0	HIT1/ REP1	HIT2/ REP2	HIT3/ REP3	HC0/ RC0	HC1/ RC1	$\overline{\text{HIT}}$[3]	Mode
H	X	L	L	L	L	L	L	L	L	L	L	H	
H	X	H	L	L	L	H	L	L	L	L	L	L	4
H	X	L	H	L	L	L	H	L	L	H	L	L	W
H	X	L	L	H	L	L	L	H	L	L	H	L	A
H	X	L	L	L	H	L	L	L	H	H	H	L	Y
L	L	L	X	L	X	L	L	L	L	L	L	H	
L	L	H	X	L	X	H	L	L	L	L	L	L	2
L	L	L	X	H	X	L	L	H	L	L	H	L	W
L	H	X	L	X	L	L	L	L	L	L	L	H	A
L	H	X	H	X	L	L	H	L	L	H	L	L	Y
L	H	X	L	X	H	L	L	L	H	H	H	L	

X: "H" or "L"

1. Internal information, rep0 to rep3 are determined by on-chip LRU logic when SBLK = "L". When SBLK = "H", the internal information are determined by external signal of SB0 & SB1.
2. Correct operation is not guaranteed if 2 ways or more become HIT at the same time.
3. Output of $\overline{\text{HIT}}$ is valid when H/R = "H".

3) PARTIAL PURGE ($\overline{\text{INVL}}$ = "L")

INPUT					INTERNAL INFO.				PURGE BLOCK				$\overline{\text{SET}}$	
					HIT				BLOCK					
MODE	A9	SBLK	SB0	SB1	0	1	2	3	0	1	2	3	LRU	MODE
H	X	L	X	X	L	L	L	L	—	—	—	—	---	
H	X	L	X	X	H	L	L	L	Q	—	—	—	RUP-D	4
H	X	L	X	X	L	H	L	L	—	Q	—	—	RUP-D	
H	X	L	X	X	L	L	H	L	—	—	Q	—	RUP-D	W
H	X	L	X	X	L	L	L	H	—	—	—	Q	RUP-D	A
H	X	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	Y
H	X	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
H	X	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	
H	X	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	
L	L	L	X	X	L	X	L	X	—	—	—	—	---	
L	L	L	X	X	H	X	L	X	Q	—	—	—	RUP-D	
L	L	L	X	X	L	X	H	X	—	—	Q	—	RUP-D	2
L	L	H	L	L	X	X	X	X	Q	—	—	—	RUP-D	
L	L	H	L	H	X	X	X	X	—	—	Q	—	RUP-D	W
L	H	L	X	X	X	L	X	L	—	—	—	—	---	A
L	H	L	X	X	X	H	X	L	—	Q	—	—	RUP-D	Y
L	H	L	X	X	X	L	X	H	—	—	—	Q	RUP-D	
L	H	H	H	L	X	X	X	X	—	Q	—	—	RUP-D	
L	H	H	H	H	X	X	X	X	—	—	—	Q	RUP-D	

Note: Correct operation is not guaranteed if 2 ways or more become HIT at the same time.

4) PARITY ERROR & V-BIT[1] (n : 0 to 3)

pen	vn0	vn1	PEn	HIT Info.[2]
L	L	L	L	---
L	L	H	H	HIT
L	H	L	H	HIT
L	H	H	L	HIT
H	L	L	L	---
H	L	H	H	HIT
H	H	L	H	HIT
H	H	H	H	HIT

1. $\overline{\text{PERR}}$ is "NOR" of PE0 to PE3
2. Output information when internal "HIT" is valid.

pen : Internal parity error of way "n"
vn0/vn1 : Duplicate validity bits.
PEn : Determined by the following equation.

$$PEn = (vn0 + vn1) \cdot pen + (vn0 \oplus vn1)$$

BASIC FUNCTIONS

TAG READ

A comparison between the TAG input data (TD0-19) and the contents of the addressed location is performed. If both data are the same, that is "FOUND". Then $\overline{\text{HIT}}$ will be "LOW" and outputs of HCn, HITn indicate hitted "Associative way". In the case of "NOT-FOUND", the TAG RAM will specify the "way", which should be replaced, by using the LRU logic automatically.

The replacement information will be presented at the outputs of RCn and REPn by forcing the H/R input into "LOW". These signals will be latched and used for the data Memory move-in operation.

TAG WRITE

When "NOT-FOUND" is occurred, the TAG-RAM also should be updated. The write operation is performed by $\overline{\text{WRITE}}$ "LOW" and $\overline{\text{SET}}$ pulse input. The TAG data will be written into the proper "way" by the internal LRU logic.

TAG-WRITE mode, V-bit (Validity bit) and the parity are set, and LRU logic is updated.

On the other hand, it will be able to specify the "way" externally by using SBLK, SB0 and SB1 inputs.

ALL PURGE

By asserting $\overline{\text{PURGE}}$ input "LOW", the V-bit are reset and LRU logic is initialized.

In this operation, the contents of each TAG and its parity will not be identified.

PARTIAL PURGE

The partial purge operation is performed by $\overline{\text{INVL}}$ "LOW" and $\overline{\text{SET}}$ pulse input.

The V-bit, which is specified by the address inputs, will be reset, and LRU logic will be reversively updated.

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	-10	10	µA
Operating Supply Current	D_{OUT} = Open, Cycle = min.	I_{CC}		250	mA
Input Low Voltage		V_{IL}	-0.5*	0.8	V
Input High Voltage		V_{IH}	2.2	6.0	V
Output Low Voltage	I_{OL} = 8mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = -4mA	V_{OH}	2.4		V

Note:
*-3.0V min. for pulse width less than 20ns.

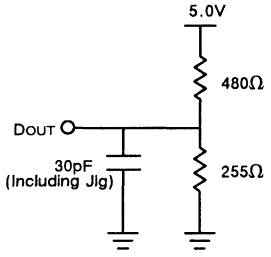
Fig. 3 — AC TEST CONDITION

INPUT PULSE LEVELS : 0.0V to 3.0V

INPUT PULSE RISE AND FALL TIMES : 5ns (Transient time between 0.8V and 2.2V)

TIMING REFERENCE LEVELS : Input : 1.5V
Output : 1.5V

OUTPUT LOAD:



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

4

TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H", or "L", $\overline{\text{VINV}}$ = "H" or "L", $\overline{\text{INH}}$ = "H")						
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	50		50		ns
Address Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{AH}		25		30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}		27		32	ns
TAG Data Valid to $\overline{\text{HIT}}$, HCn, HITn	t_{TH}		18		18	ns
TAG Data Valid to $\overline{\text{MHIT}}$	t_{TMH}		20		20	ns
$\overline{\text{HIT}}$, HCn, HITn Hold Time	t_{HH}	0		0		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
RCn, REPn Hold Time for RLATCH	t_{RH}	0		0		ns
SBLK, SB0, SB1 Setup Time for RCn, REPn	t_{SBR}		25		25	ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns
RCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0		0		ns
H/R to Multiplex output change	t_{HR}		10		12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ output	t_{MMH}		10		12	ns

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", H/R = "L", $\overline{\text{INH}}$ = "H")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	50		50		ns
Address Valid to RCn, REPn	t_{AR}		35		40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
RLATCH Setup Time	t_{RLS}	10		10		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Setup Time for PCn, REPn	t_{SBR}		25		25	ns
PCn, REPn Hold Time for SBLK, SB0, SB1	t_{SH}	0		0		ns
SBLK Hold Time	t_{SBH}	5		5		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Setup Time for $\overline{\text{SET}}$	t_{IS}	25		25		ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Hold Time	t_{IR}	5		5		ns

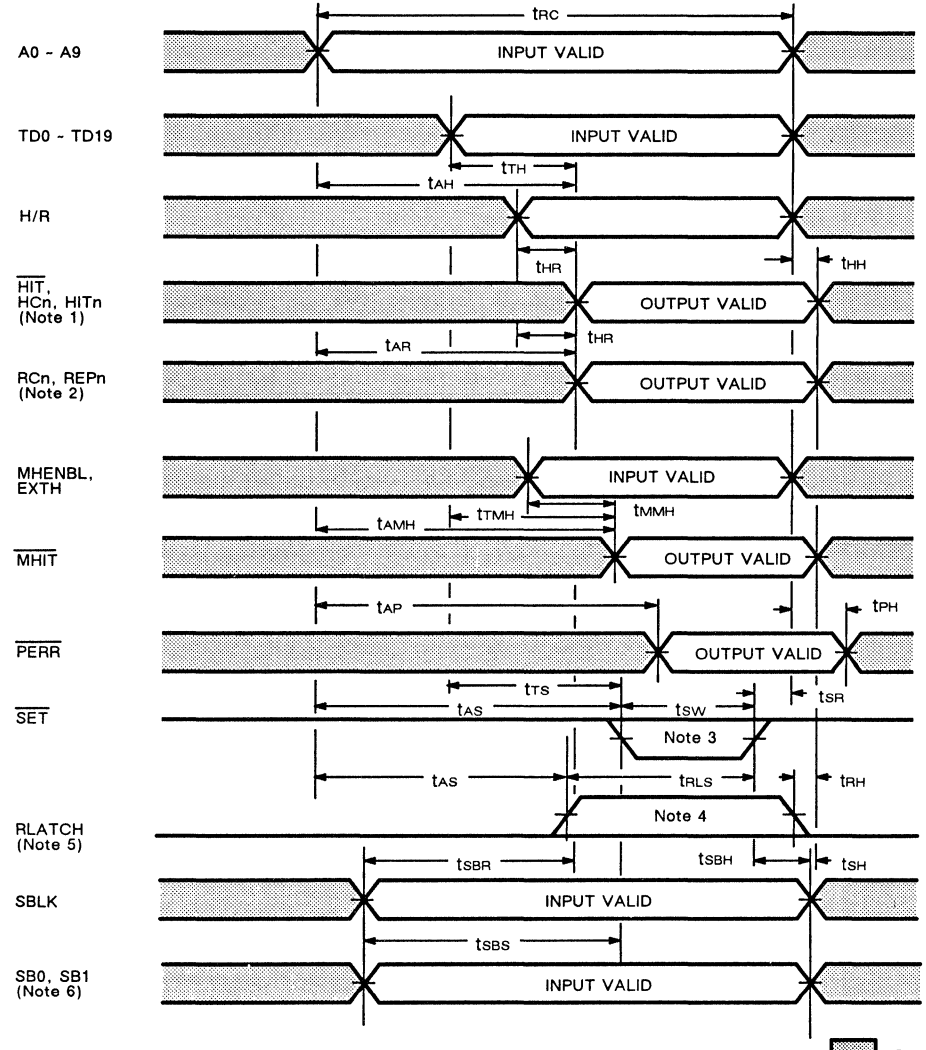
PERTIAL PURGE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$= "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")

Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
Pertial Purge Cycle	t_{PPC}	50		50		ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25		25		ns
TAG Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25		25		ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20		20		ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5		5		ns
SBLK, SB0, SB1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25		25		ns
SBLK, SB0, SB1 Hold Time	t_{SBH}	5		5		ns

ALL PURGE ($\overline{\text{SET}}$ = "H", Other control inputs are "H" or "L")

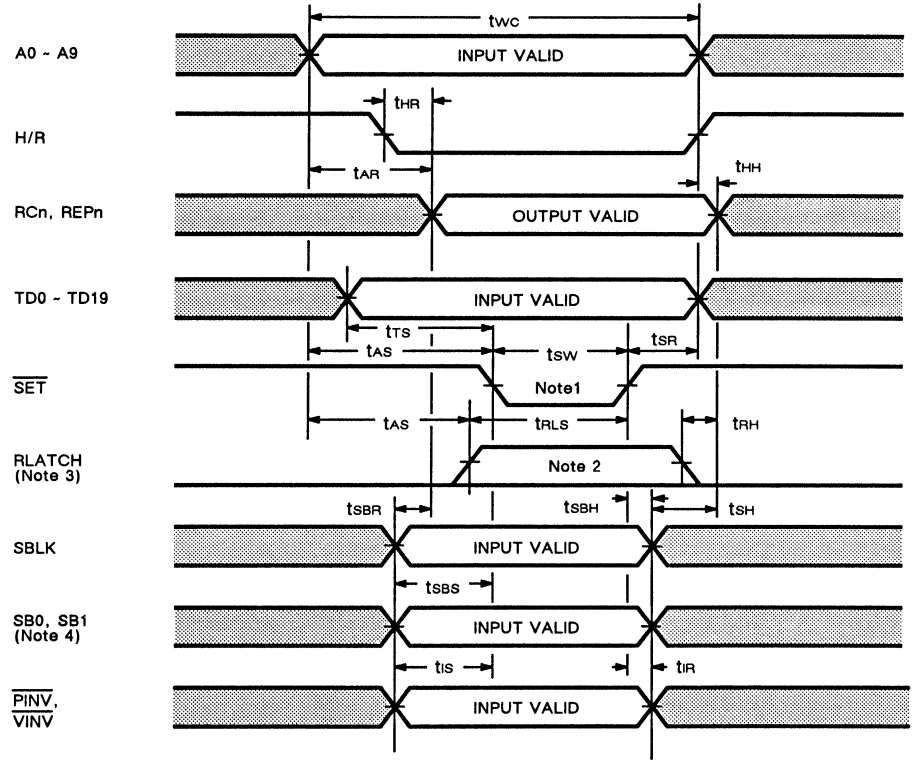
Parameter	Symbol	MB81C51-25		MB81C51-30		Unit
		Min	Max	Min	Max	
All Purge Cycle Time	t_{APC}	100		100		ns
Purge Pulse Width	t_{PPW}	50		50		ns
Purge Recovery Time	t_{PR}	50		50		ns

TAG READ CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "H", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L", INH = "H")



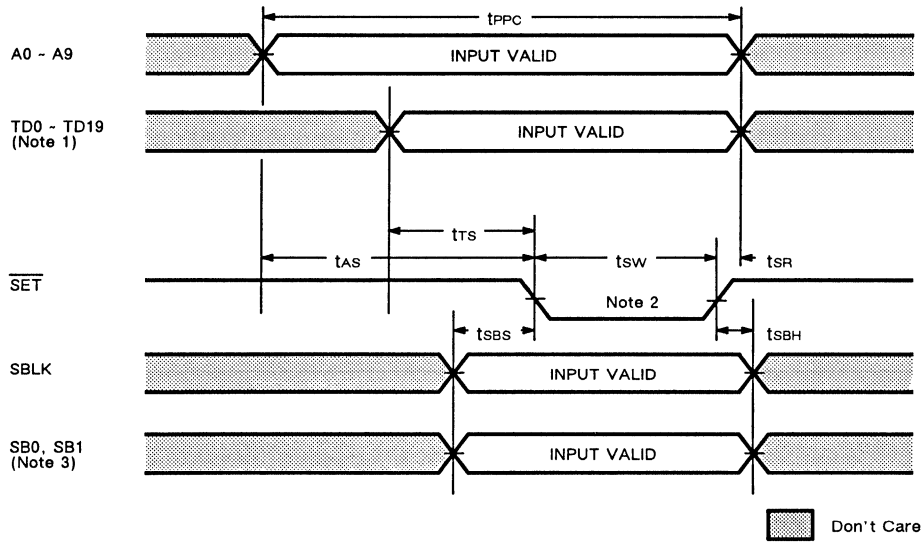
Notes 1: Valid at H/R = "H".
2: Valid at H/R = "L".
3: LRU is updated at $\overline{\text{SET}}$ = "L".
4: Replace latched at RLATCH = "H".
5: Valid at SBLK = "L".
6: Valid at SBLK = "H".

TAG WRITE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "L", $\overline{\text{INVL}}$ = "H", $\overline{\text{INH}}$ = "H")



Notes 1. Registrate TAG, V-bit "H", LRU update.
2. Replace latched at $\overline{\text{RLATCH}}$ = "H".
3. Valid at SBLK = "L".
4. Valid at SBLK = "H".

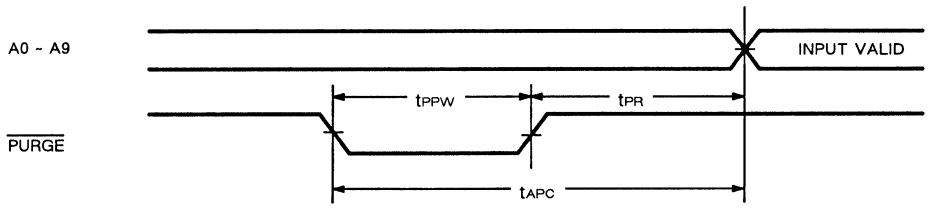
PARTIAL PURGE CYCLE (MODE = "H" or "L", $\overline{\text{PURGE}}$ = "H", $\overline{\text{WRITE}}$ = "H", $\overline{\text{INVL}}$ = "L", H/R = "H" or "L", $\overline{\text{INH}}$ = "H", RLATCH = "L", $\overline{\text{PINV}}$ = "H" or "L", $\overline{\text{VINV}}$ = "H" or "L")



Notes:

1. Valid at SBLK = "L".
2. LRU is reversively updated, V-bit "L".
3. Valid at SBLK = "H".

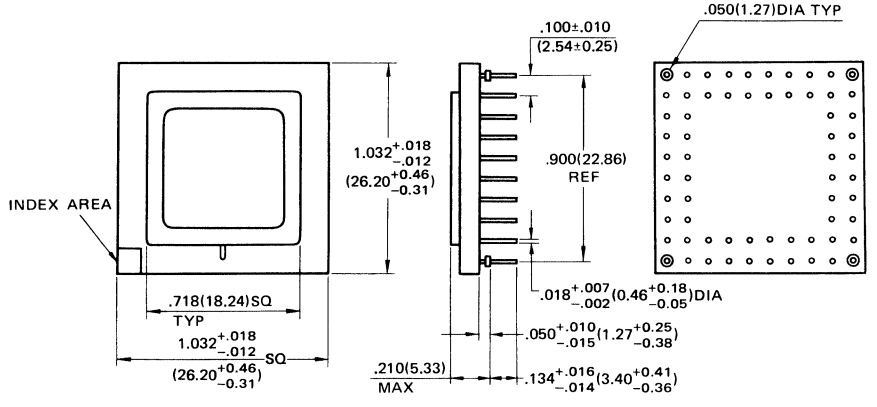
All purge ($\overline{\text{SET}}$ = "H", OTHER CONTROL INPUTS ARE "H" or "L")



PACKAGE DIMENSIONS

(Suffix: -CR)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-64C-A02)



Dimensions in
inches (millimeters)

4

October 1989
Edition 1.0

FUJITSU

DATA SHEET

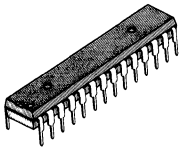
MB81C79B-35/-45
CMOS 72K-BIT HIGH-SPEED SRAM

8K Words x 9 Bits High-Speed CMOS Static Random Access Memory with Automatic Power Down

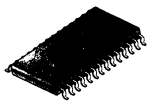
The Fujitsu MB81C79B is a 8,192 words x 9 bits static random access memory fabricated with CMOS technology. The 9-bit organization of this device is desirable for use in a parity check function. This device also has two fast column addresses, making it very suitable to use as cache buffers. To make power dissipation lower, peripheral circuits use CMOS technology, and to obtain smaller chip size, cells use NMOS transistors and resistors. All pins are TTL compatible and a single +5 V power supply is required.

The MB81C79B offers low power dissipation, low cost, and high performance.

- Organization: 8,192 words x 9 bits
- Static operation: no clock or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 35$ ns max, $t_{OE} = 10$ ns max.
  A11, A12 access time = 12 ns max. (MB81C79B-35)
  $t_{AA} = t_{ACS1} = 45$ ns max, $t_{OE} = 15$ ns max.
  A11, A12 access time = 15 ns max. (MB81C79B-45)
- Low power consumption: 550 mW max. (Operation)
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state inputs and outputs
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB81C79B-xxPSK
  SOP (450 mil) MB81C79B-xxPF



PLASTIC PACKAGE
DIP-28P-M04



PLASTIC PACKAGE
FPT-28P-M02

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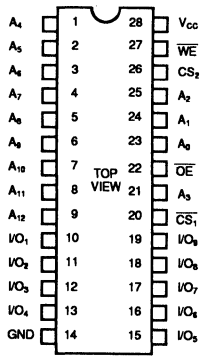
PIN ASSIGNMENT



Absolute Maximum Ratings (See Note)

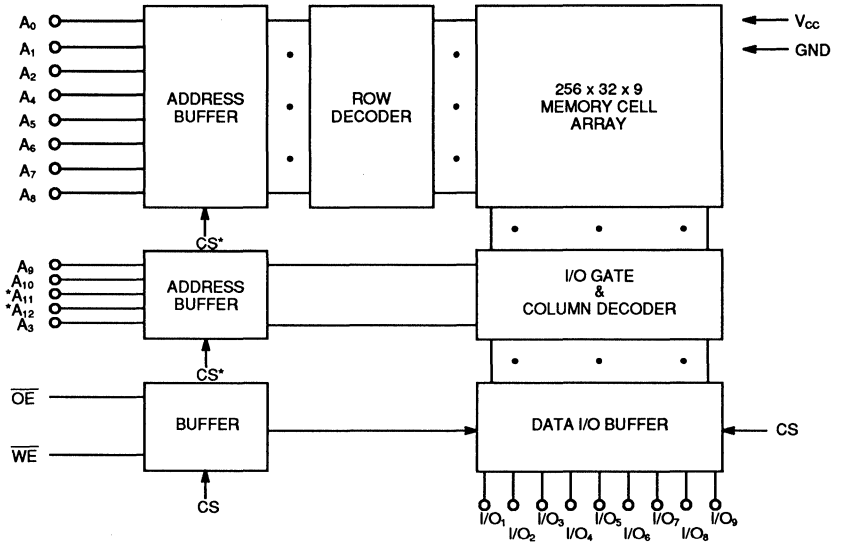
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

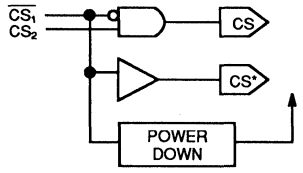
Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 — MB81C79B BLOCK DIAGRAM





TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O STATE
H	X	X	X	STANDBY	I_{SB}	HIGH–Z
L	L	X	X	DESELECT	I_{CC}	HIGH–Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH–Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

* Fast address

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V) ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	C_{I1}		7	pF
Input Capacitance (V_{IN}=0V) (Other Inputs)	C_{I2}		6	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$		8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−2.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

* −2.0V Min. for pulse width less than 20ns. (V_{IL} Min=−0.5V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	−10	10	µA	V_{IN}=0V to V_{CC}
Output Leakage Current	I_{LO}	−10	10	µA	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC}		130	mA	$\overline{CS_1}$=V_{IL} I/O=Open, Cycle=Min
Standby Supply Current	I_{SB1}		15	mA	V_{CC}=Min to Max. $\overline{CS_1}$=V_{CC}−0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}−0.2V
	I_{SB2}		25	mA	$\overline{CS_1}$=V_{IH}
Output Low Voltage	V_{OL}		0.4	V	I_{OL}=8mA
Output High Voltage	V_{OH}	2.4		V	I_{OH}=−4mA
Peak Power-on Current	I_{PO}		50	mA	V_{CC}=0V to V_{CC} Min. $\overline{CS_1}$=Lower of V_{CC} or V_{IH} Min.

4

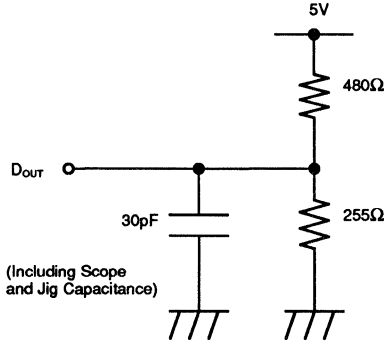
AC TEST CONDITIONS

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise And Fall Times:	5ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 1.5V

Fig. 2

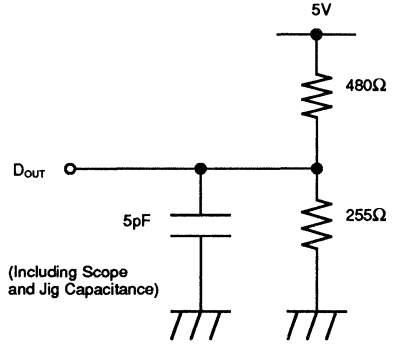
Output Load I.

For all except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



Output Load II.

For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, and t_{OHZ}.



4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

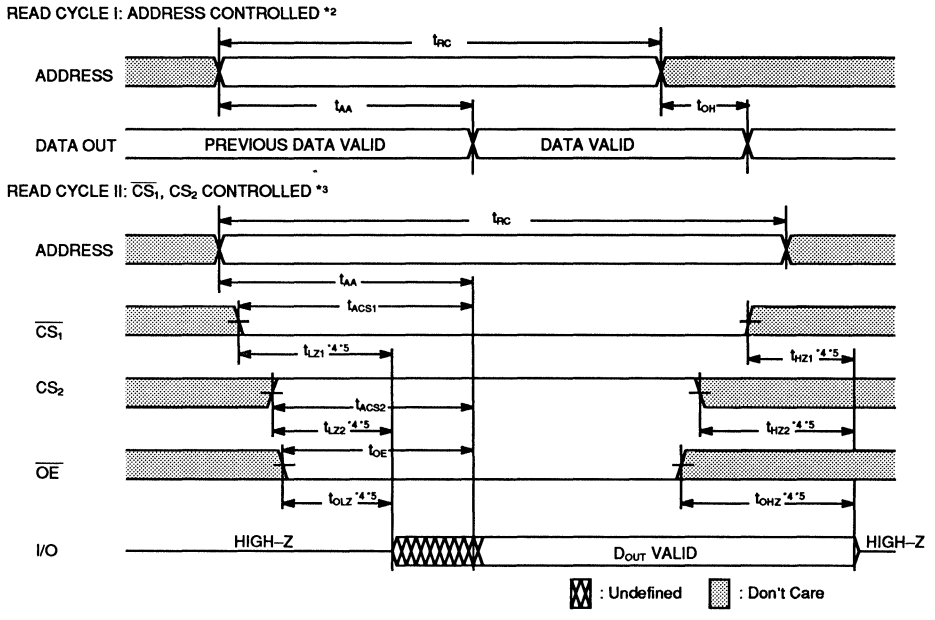
READ CYCLE*1

Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Address Access Time *2	t_{AA}		35#1		45#2	ns
$\overline{CS_1}$ Access Time *3	t_{ACS1}		35		45	ns
CS_2 Access Time *3	t_{ACS2}		15		20	ns
Output Hold from Address Change	t_{OH}	3		3		ns
$\overline{OE}$ Access Time	t_{OE}		10		15	ns
Output Active from $\overline{CS_1}$ *4 *5	t_{LZ1}	5		5		ns
Output Active from CS_2 *4 *5	t_{LZ2}	2		2		ns
Output Active from $\overline{OE}$ *4 *5	t_{OLZ}	2		2		ns
Output Disable from $\overline{CS_1}$ *4 *5	t_{HZ1}		20		25	ns
Output Disable from CS_2 *4 *5	t_{HZ2}		20		25	ns
Output Disable from $\overline{OE}$ *4 *5	t_{OHZ}		20		25	ns

Note : *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.
#1 A11, A12 address access time is 12ns max.
#2 A11, A12 address access time is 15ns max.

4

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

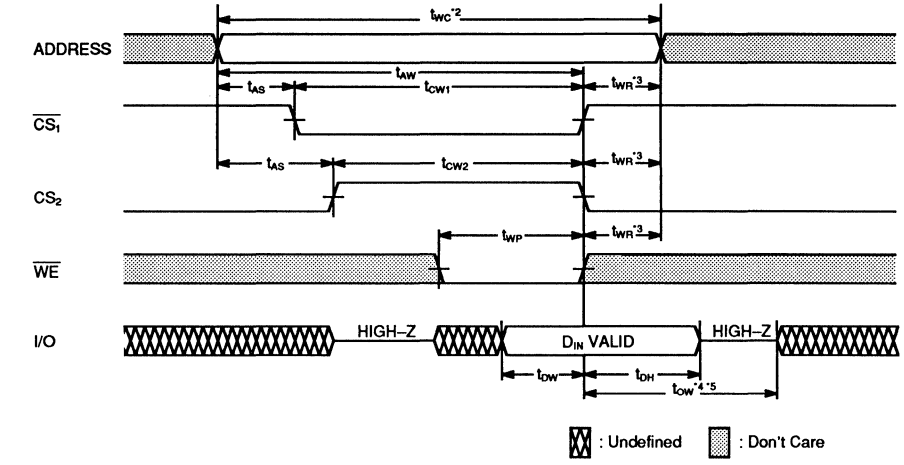
WRITE CYCLE*1

Parameter	Symbol	MB81C79B-35		MB81C79B-45		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	35		45		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	30		40		ns
CS_2 to End of Write	t_{CW2}	20		25		ns
Address Valid to End of Write	t_{AW}	30		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	20		25		ns
Data Setup Time	t_{DW}	17		20		ns
Write Recovery Time *3	t_{WR}	3		3		ns
Data Hold Time	t_{DH}	0		0		ns
Output High-Z from $\overline{WE}$ *4*5	t_{WZ}		15		20	ns
Output Low-Z from $\overline{WE}$ *4*5	t_{OW}	0		0		ns

Note: *1 If $\overline{CS_1}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage.
*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE I: $\overline{CS_1}$, CS_2 CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

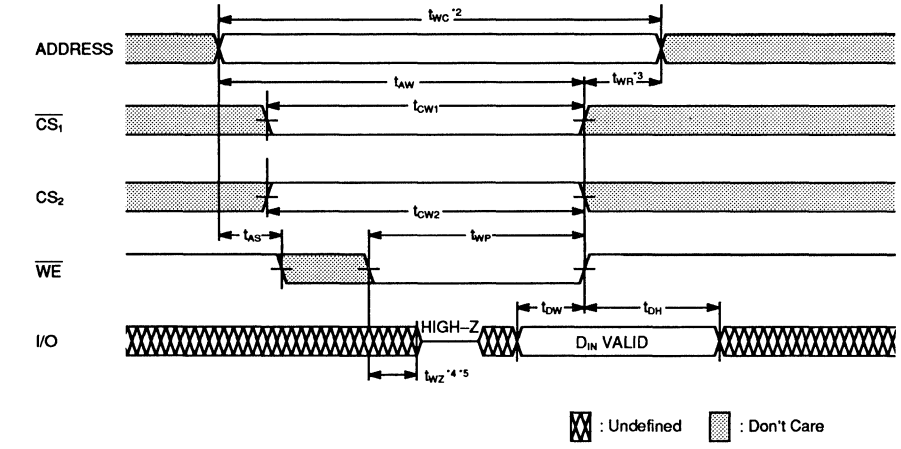
*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

*5 This parameter is specified with Load II in Fig. 2.

WRITE CYCLE TIMING DIAGRAM *1

WRITE CYCLE II: $\overline{WE}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS_1}$, and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 All write cycles are determined from the last address transition to the first address transition of next address.

*3 t_{WR} is defined from the end point of WRITE Mode.

*4 Transition is specified at the point of ±500mV from steady state voltage.

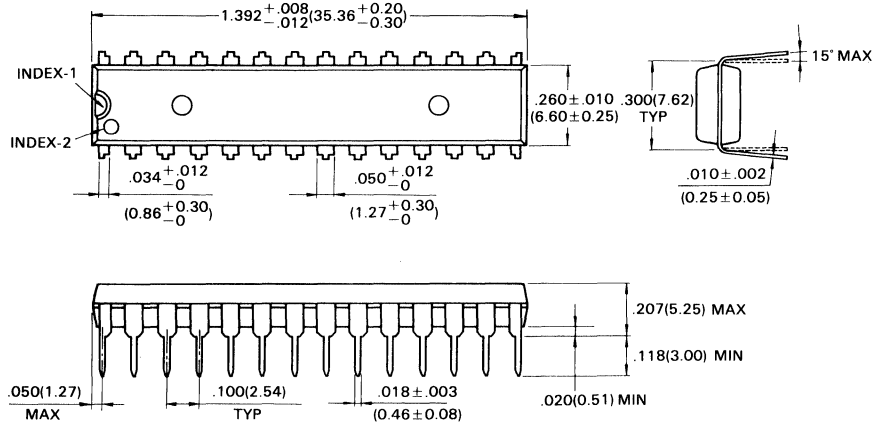
*5 This parameter is specified with Load II in Fig. 2.

4

PACKAGE DIMENSIONS

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)

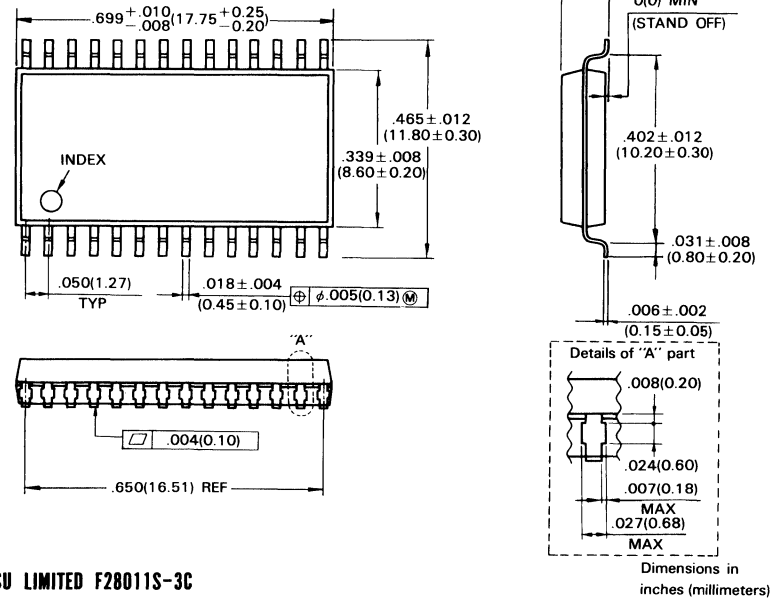


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M02)



Dimensions in inches (millimeters)

4

April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB8279RT-20/-25
CMOS 72K-BIT HIGH-SPEED SRAM

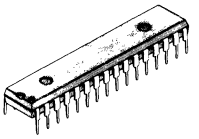
8K Words x 9 Bits Synchronous CMOS Static Random Access Memory with Automatic Power Down

The Fujitsu MB8279RT is a 8,192 words x 9 bits static random access memory fabricated with a CMOS silicon gate process.

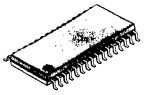
Write operation is initiated by an internal write pulse generator, which is driven by the CLK input; therefore, external control of write pulse width is not necessary. Compared to the traditional RAM, the MB8279RT provides improved system level cycle time because signal skews are not involved.

The MB8279RT is housed in 32-pin plastic skinny DIP and SOP packages. All pins are TTL compatible and a single +5 V power supply is required.

- Organization: 8,192 words x 9 bits
- Access time: t_{ACL} = 20 ns max. (MB8279RT-20)
  $t_{ACS2} = t_{PE2}$ = 10 ns max.
  t_{ACL} = 25 ns max. (MB8279RT-25)
  $t_{ACS2} = t_{PE2}$ = 12 ns max.
- Registered addresses, $\overline{CS_1}$, $\overline{WE}$ and data inputs
- Write cancel function by asynchronous CS_2 pin
- On-chip write pulse generator
- On-chip parity checker
- CMOS peripheral circuits
- Single +5 V power supply ±10% tolerance with low current drain:
  120 mA max. Active operation
  30 mA max. Standby operation
- Common data inputs and outputs
- TTL compatible inputs and outputs
- Three-state data outputs and open drain parity error outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8279RT-xxPSK
  SOP MB8279RT-xxPF



PLASTIC PACKAGE
DIP-32P-M02

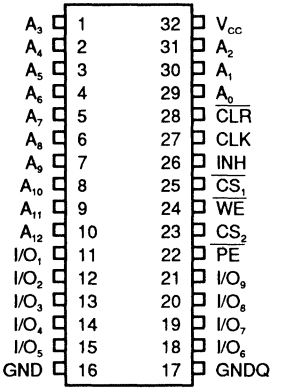


PLASTIC PACKAGE
FPT-32P-M02

4

PIN ASSIGNMENT

(TOP VIEW)



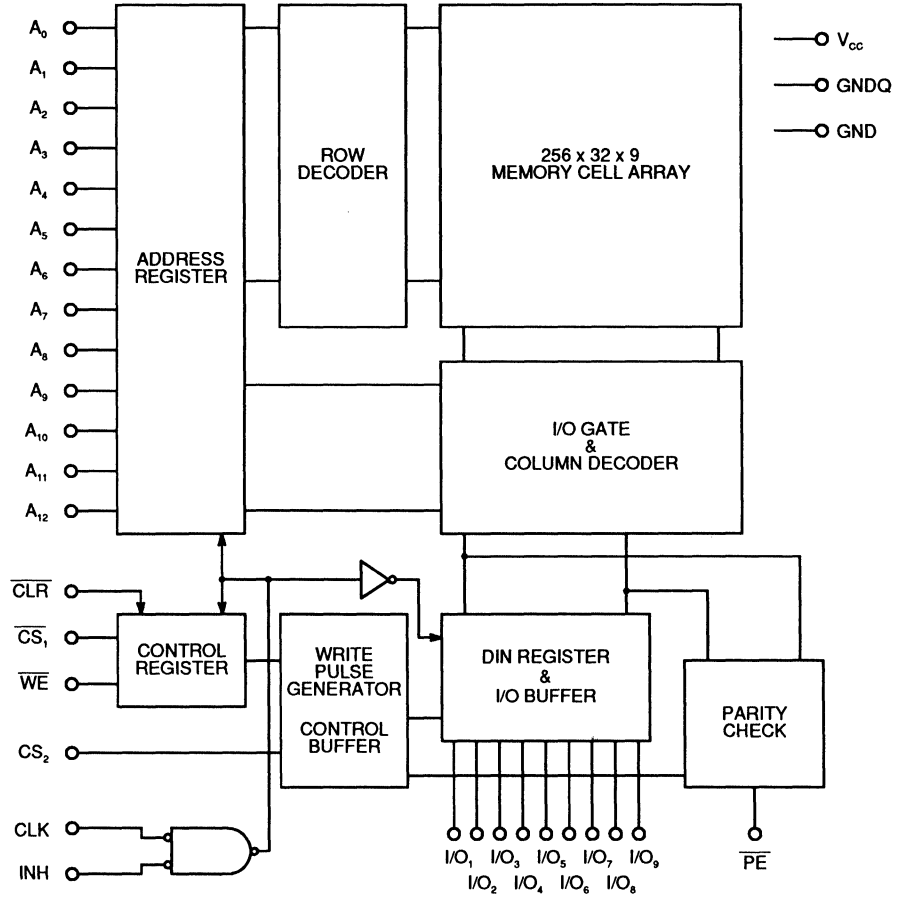
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Output Voltage	$V_{I/O}$	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB8279RT BLOCK DIAGRAM



4

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN}=0V)	C_{IN}			6	pF

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CLK	Clock	Input	Address, $\overline{CS}$, and $\overline{WE}$ are fetched at the rising edge of the CLK, and D_{IN} is fetched at falling edge of the CLK.
INH	Inhibit	Input	While INH="H", a low level of CLK is disabled.
$\overline{CLR}$	Clear	Input	When $\overline{CLR}$="L", the contents of $\overline{CS}$, and $\overline{WE}$ register are cleared to standby.
A_0 to A_{12}	Address Input	Input	Synchronous address inputs.
$\overline{CS_1}$	Chip Select 1	Input	Synchronous Chip Select 1 ($\overline{CS_1}$) input. (This pin can be used as power down.)
CS_2	Chip Select 2	Input	Asynchronous high-speed Chip Select 2 (CS_2) input. (This pin can be used as write cancel.)
$\overline{WE}$	Write Enable	Input	Synchronous Write Enable ($\overline{WE}$) input.
I/O_1 to I/O_9	Data Input/Output	Input/ Output	Data inputs/outputs. (Synchronous data input/Asynchronous data outputs)
PE	Parity Error	Output	Asynchronous parity error output: $\overline{PE}$ output remains High-Impedance state through undefined area.
V_{CC}	Power Supply	–	+5V ±10% power supply.
GNDQ	Ground for Output	–	Ground for output circuits.
GND	Ground for Others	–	Ground for other circuits.

4

TRUTH TABLE

$\overline{CLR}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	MODE	I/O PIN	$\overline{PE}$ OUTPUT PIN	SUPPLY CURRENT
L	X	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	H	X	X	STANDBY	HIGH-Z	HIGH-Z	STANDBY
H	L	L	X	CHIP DISABLE	HIGH-Z	HIGH-Z	ACTIVE
H	L	H	H	READ	D_{OUT}	$\overline{PE}$ OUTPUT	ACTIVE
H	L	H	L	WRITE	D_{IN}	HIGH-Z	ACTIVE

Legend: H=High level, L=Low level, X=Don't care.
Notes: $\overline{CS_1}$, and $\overline{WE}$ are input at the rising edge of the CLK.
$\overline{PE}$ output remains High-Impedance state through undefined area.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

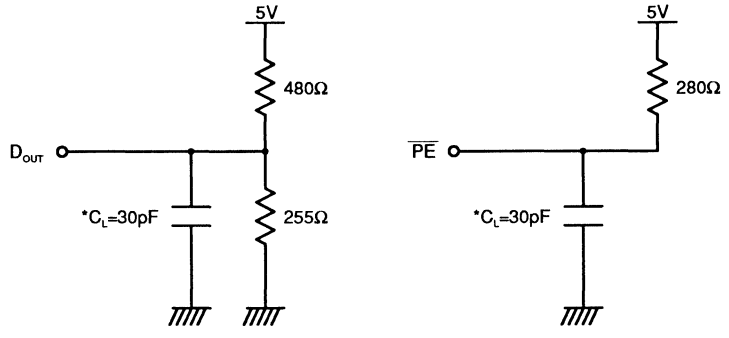
(Recommended operating conditions otherwise noted)

Parameter		Test Conditions	Symbol	Min	Max	Unit
Standby Supply Current		$\overline{CS_1}$=V_{IH}	I_{SB}		30	mA
Operating Supply Current		$\overline{CS_1}$=V_{IL}, I/O=Open Cycle=min.	I_{CC}		120	mA
Input Leakage Current		V_{IN}=GND to V_{CC}	I_{IL}	−10	10	µA
Output Leakage Current		$\overline{CS_1}$=V_{IH}, or CS_2=V_{IL} V_{OUT}=GND to V_{CC}	$I_{LI/O}$	−10	10	µA
Input Low Voltage			V_{IL}	−2.0*1	0.8	V
Input High Voltage			V_{IH}	2.2	6.0	V
Output High Voltage		I_{OH}=−4mA	V_{OH}	2.4		V
Output Low Voltage	D_{OUT}	I_{OL}=8mA	V_{OL}		0.4	V
	$\overline{PE}$	I_{OL}=16mA				
Peak Power-on Current*2		V_{CC}=GND to 4.5V $\overline{CLR}$=GND	I_{PO}		120	mA

Note: *1 −2.0V Min. for pulse width less than 20ns. (V_{IL}=−0.5V at DC level)
*2 The $\overline{CLR}$ input should be connected to GND to keep the device deselected.

Fig. 2 – AC TEST CONDITIONS

- INPUT PULSE LEVELS: 0.6V TO 2.4V
- INPUT PULSE RISE & FALL TIMES: 5ns (Transient between 0.8V and 2.2V)
- TIMING REFERENCE LEVELS: INPUT: V_{IL}=0.8V, V_{IH}=2.2V
  OUTPUT: V_{OL}=0.8V, V_{OH}=2.2V
- OUTPUT LOAD



*INCLUDING JIG AND STRAY CAPACITANCE.
(C_L=5pF for t_{LZ}, t_{HZ}, t_{LZ2}, t_{HZ2} and t_{CRHZ}) (C_L=5pF for t_{PLZ}, t_{PHZ}, t_{PLZ2}, t_{PHZ2} and t_{CRHZ})

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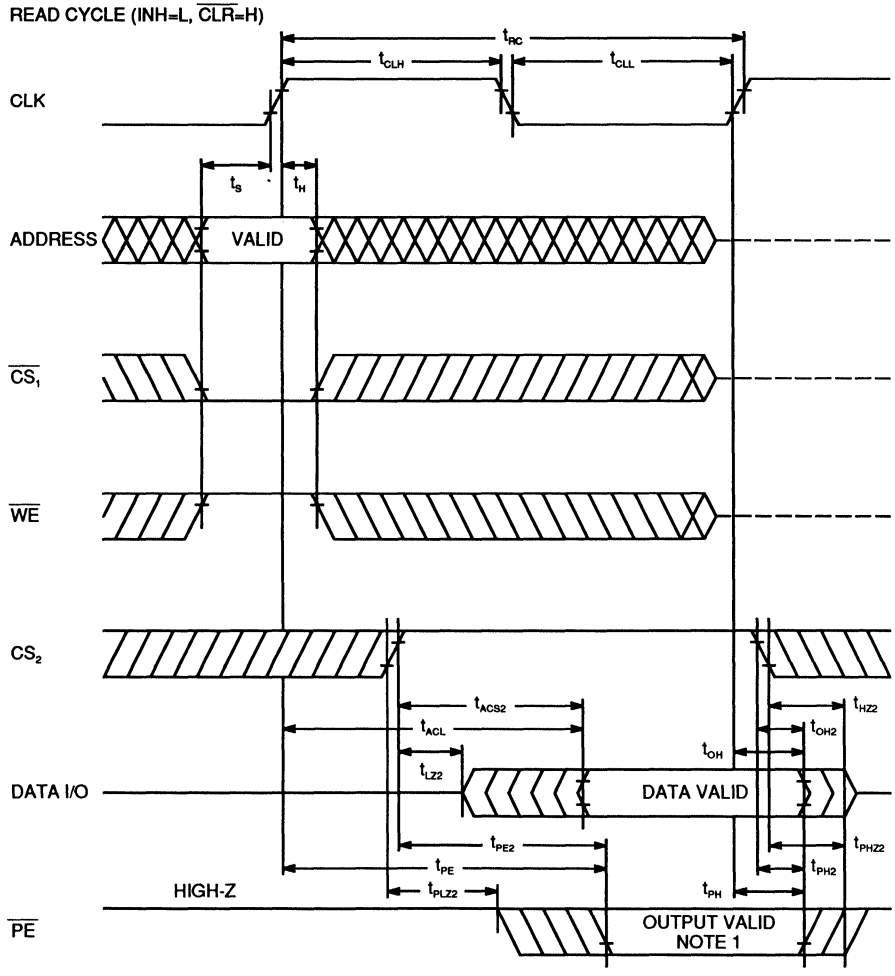
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Read Cycle Time	When on uses $\overline{PE}$	t_{RC}	20		25		ns
	When uses $\overline{PE}$	t_{RC}	25		30		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
Clock Access Time	D_{OUT}	t_{ACL}		20		25	ns
	$\overline{PE}$	t_{PE}		25		30	ns
CS_2 Access Time	D_{OUT}	t_{ACS2}		10		12	ns
	$\overline{PE}$	t_{PE2}		10		12	ns
CS_2 to Output Low-Z	D_{OUT}	t_{LZ2}	2		2		ns
	$\overline{PE}$	t_{PLZ2}	2		2		ns
CS_2 to Output High-Z	D_{OUT}	t_{HZ2}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ2}	2	8	2	10	ns
Output Hold from Clock	D_{OUT}	t_{OH}	2		2		ns
	$\overline{PE}$	t_{PH}	2		2		ns
Output Hold from CS_2	D_{OUT}	t_{OH2}	2		2		ns
	$\overline{PE}$	t_{PH2}	2		2		ns

READ CYCLE TIMING DIAGRAM



Note 1: $\overline{PE}$ output remains High-Impedance state through undefined area.

WRITE CYCLE

Parameter		Symbol	MB8279RT-20		MB8279RT-25		Unit
			Min	Max	Min	Max	
Write Cycle Time		t_{WC}	20		25		ns
Clock "H" Level Pulse Width		t_{CLH}	8		10		ns
Clock "L" Level Pulse Width		t_{CLL}	8		10		ns
Input Setup Time		t_S	4		4		ns
Input Hold Time		t_H	2		2		ns
CS_2 Setup Time		t_{CS}	2		2		ns
CS_2 Hold Time		t_{CH}	8		10		ns
Data Setup Time		t_{DS}	0		0		ns
Data Hold Time		t_{DH}	6		6		ns
CLK to Output High-Z	D_{OUT}	t_{HZ}	2	8	2	10	ns
	$\overline{PE}$	t_{PHZ}	2	8	2	10	ns
CLK to Output Low-Z	D_{OUT}	t_{LZ}	2		2		ns
	$\overline{PE}$	t_{PLZ}	2		2		ns

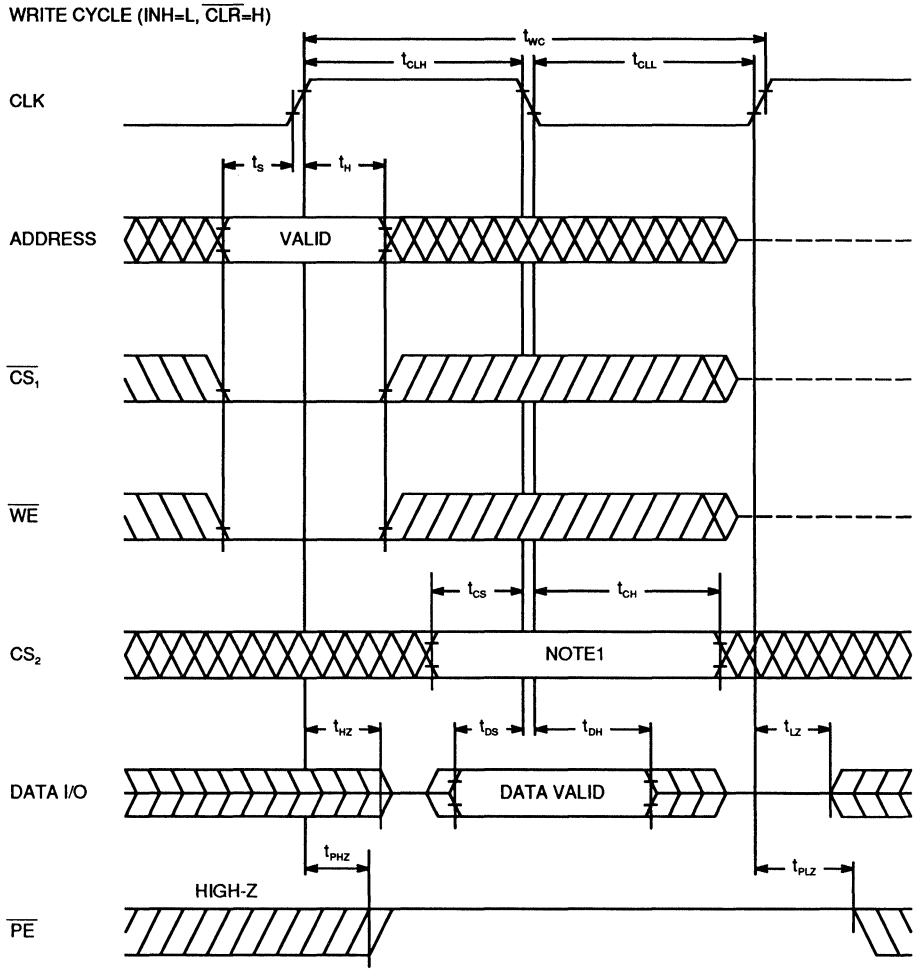
CLOCK INHIBIT TIMING

Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clock Inhibit Setup Time	t_{CLIS}	2		2		ns
Clock Inhibit Hold Time	t_{CLIH}	2		2		ns
Clock Enable Setup Time	t_{CLES}	2		2		ns
Clock Enable Hold Time	t_{CLEH}	0		0		ns

REGISTER CLEAR TIMING

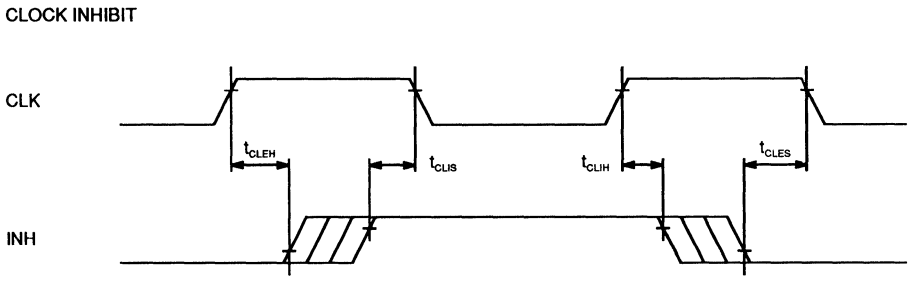
Parameter	Symbol	MB8279RT-20		MB8279RT-25		Unit
		Min	Max	Min	Max	
Clear Pulse Width	t_{CRW}	7		7		ns
Clear Hold Time	t_{CRH}	10		10		ns
Clear Recovery Time	t_{CRR}	10		10		ns
Clear to Output High-Z	t_{CRHZ}	2	8	2	10	ns

WRITE CYCLE TIMING DIAGRAM

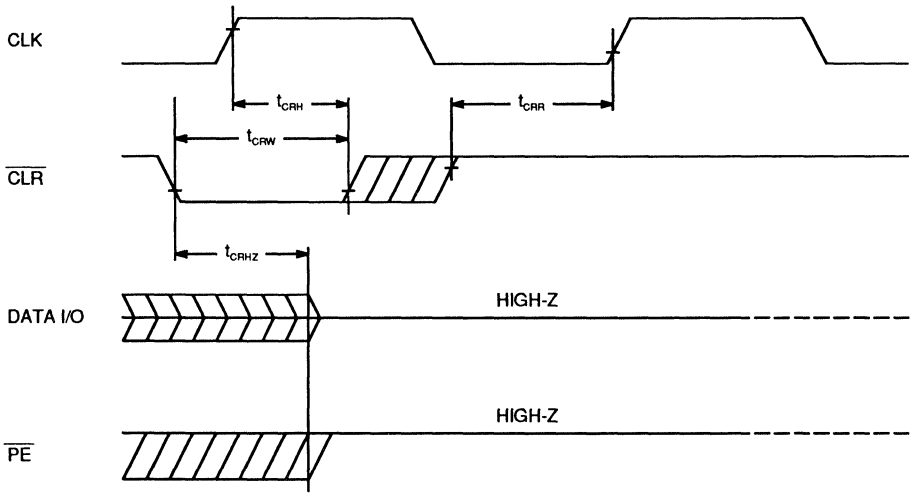


Note 1: When CS_2 = "H" level, write operation is excuted and when CS_2 = "L" level, write operation is cancelled.

CLOCK INHIBIT TIMING DIAGRAM



REGISTER CLEAR TIMING



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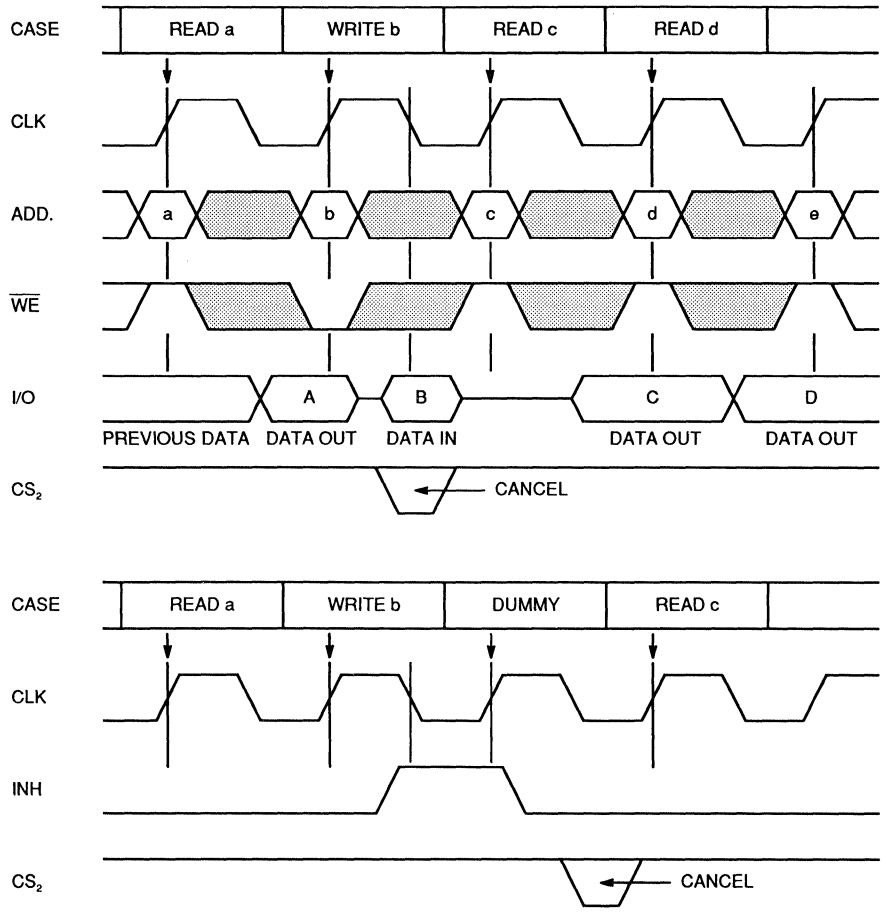
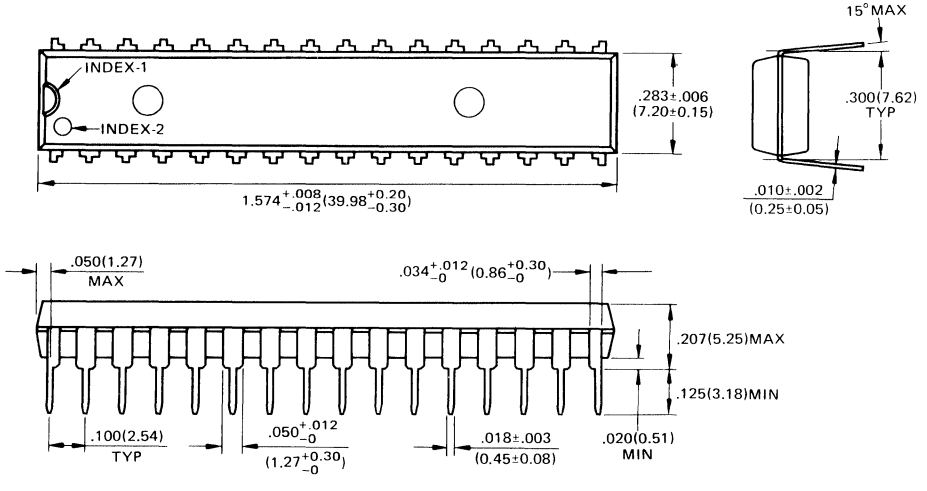
EXAMPLE OF MB8279RT BASIC FUNCTION



PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)

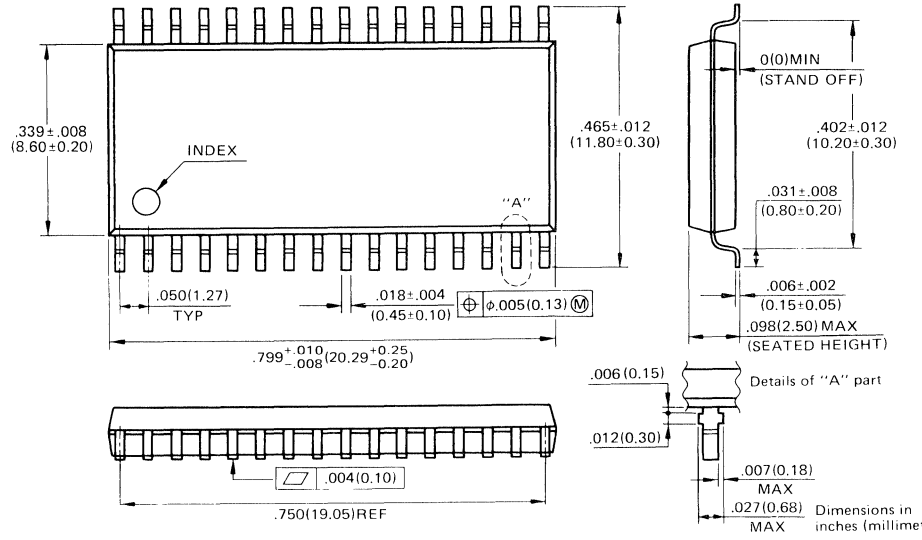


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M02)



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April 1990
Edition 2.0

FUJITSU

DATA SHEET

MB8287-25/-35
CMOS 288K-BIT HIGH-SPEED SRAM

32K Words x 8 Bits Static Random Access Memory with Automatic Power Down

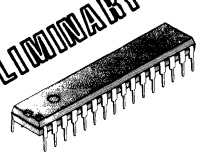
The Fujitsu MB8287 is a 32,768 words x 8 bits static random access memory with parity generator and checker, and fabricated with CMOS technology. To obtain a smaller chip size, the cell uses NMOS transistors and resistors. This device is housed in a 300 mil DIP package with low (605 mW max.) power dissipation. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select ($\overline{CS_1}$) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

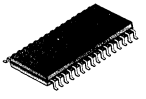
The MB8287 offers low power dissipation, low cost, and high performance.

- Organization: 32,768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 25$ ns max, $t_{ACS2} = 14$ ns max. (MB8287-25)
  $t_{AA} = t_{ACS1} = 35$ ns max, $t_{ACS2} = 15$ ns max. (MB8287-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  83 mW max. (CMOS Standby)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion
- Electrostatic protection for all inputs and outputs
- Standard 32-pin Plastic Packages:
  Skinny DIP (300 mil) MB8287-xxPSK
  SOP (450 mil) MB8287-xxPF

PRELIMINARY

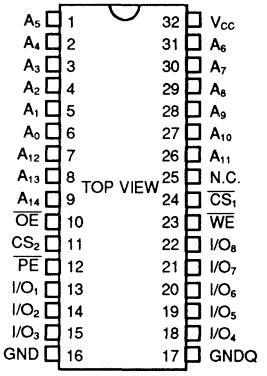


PLASTIC PACKAGE
(DIP-32P-M02)



PLASTIC PACKAGE
(FPT-32P-M02)

PIN ASSIGNMENT



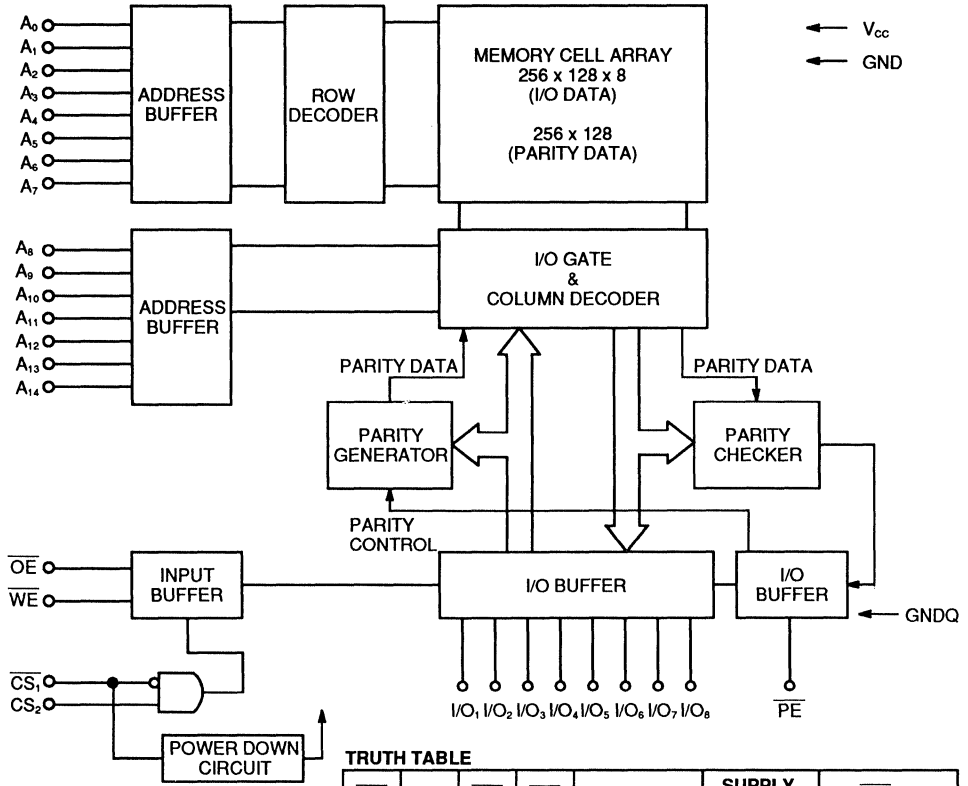
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7.0	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – MB8287 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O, $\overline{PE}$ STATE
H	X	X	X	STANDBY	I_{SB}	HIGH-Z
L	L	X	X	DESELECT	I_{CC}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	H	L	READ	I_{CC}	D_{OUT}
L	H	L	X	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS_1}$, CS_2, $\overline{OE}$, $\overline{WE}$)	V_{IN}=0V	C_{I1}			8	pF
Input Capacitance (Other Input)	V_{IN}=0V	C_{I2}			7	pF
I/O Capacitance (with $\overline{PE}$)	$V_{I/O}$=0V	$C_{I/O}$			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

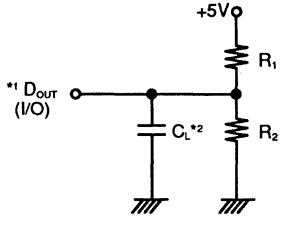
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		I_{SB1}	$\overline{CS_1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		15	mA
		I_{SB2}	$V_{IN} \leq 0.2V$ $\overline{CS_1} = V_{IH}$		25	mA
Operating Supply Current	25ns	I_{CC}	I_{OUT}=0mA, $\overline{CS_1}=V_{IL}$ Cycle=Min.		130	mA
	35ns				110	
Input Leakage Current		I_{LI}	V_{IN}=0V to V_{CC}, V_{CC}=Max.	–5	5	µA
Output Leakage Current		$I_{LI/O}$	$\overline{CS_1}=V_{IH}$ or $\overline{CS_2}=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=0V to V_{CC}	–5	5	µA
Input Low Voltage		V_{IL}		–2.0*1	0.8	V
Input High Voltage		V_{IH}		2.2	6.0	V
Output High Voltage		V_{OH}	I_{OH}=–4mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL}=8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20ns. (V_{IL} min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input : V_{IL}=0.8V, V_{IH}=2.2V
  Output : V_{OL}=0.8V, V_{OH}=2.2V
- Output Load:



	R_1	R_2	C_L	Parameters Measured
Load I	480kΩ	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}
Load II	480kΩ	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}, t_{OLZ}, t_{OHZ}, t_{PHZ} and t_{POHZ}

*1 $\overline{PE}$ pin is included.
*2 Including Scope and Jig Capacitance

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

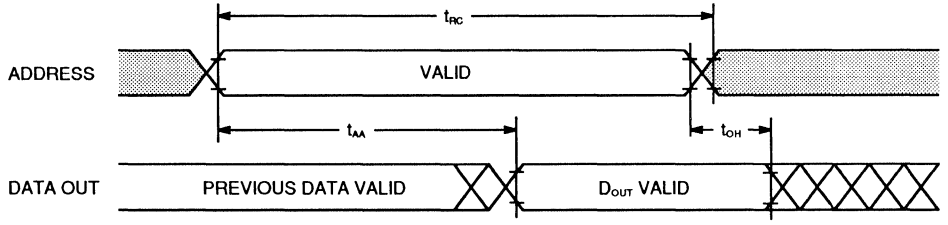
READ CYCLE*1

Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time*2	t_{AA}		25		35	ns
$\overline{CS_1}$ Access Time*3	t_{ACS1}		25		35	ns
CS_2 Access Time*3	t_{ACS2}		14		15	ns
$\overline{OE}$ Access Time	t_{OE}		12		14	ns
Output Hold from Address Change	t_{OH}	3		3		ns
Output Active from $\overline{CS_1}$*4	t_{LZ1}	5		8		ns
Output Active from CS_2*4	t_{LZ2}	2		3		ns
Output Active from $\overline{OE}$*4	t_{OLZ}	2		3		ns
Output Disable from $\overline{CS_1}$*4	t_{HZ1}	1	15	1	15	ns
Output Disable from CS_2*4	t_{HZ2}	1	15	1	15	ns
Output Disable from $\overline{OE}$*4	t_{OHZ}	1	15	1	15	ns
Parity Error Access from Address*2	t_{APA}		28		40	ns
Parity Error Access from $\overline{CS_1}$*3	t_{APCS1}		28		40	ns
Parity Error Access from CS_2*3	t_{APCS2}		14		15	ns
Parity Error Access from $\overline{OE}$	t_{APOE}		12		14	ns
Parity Error Hold from Address Change	t_{POH}	3		3		ns
Parity Error Disable from Address Change*4	t_{PHZA}		20		25	ns
Parity Error Disable from $\overline{CS_1}$*4	t_{PHZ1}	1	15	1	15	ns
Parity Error Disable from CS_2*4	t_{PHZ2}	1	15	1	15	ns
Parity Error Disable from $\overline{OE}$*4	t_{POHZ}	1	15	1	15	ns

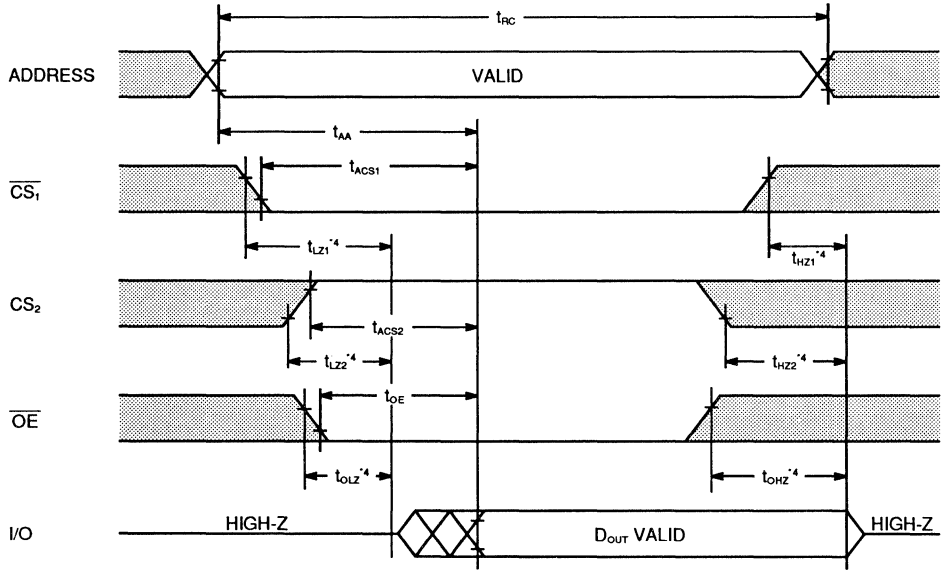
Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ and $\overline{OE}=V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

READ CYCLE TIMING DIAGRAM*1

READ CYCLE : ADDRESS CONTROLLED*2



READ CYCLE : $\overline{CS_1}$, CS_2 CONTROLLED*3

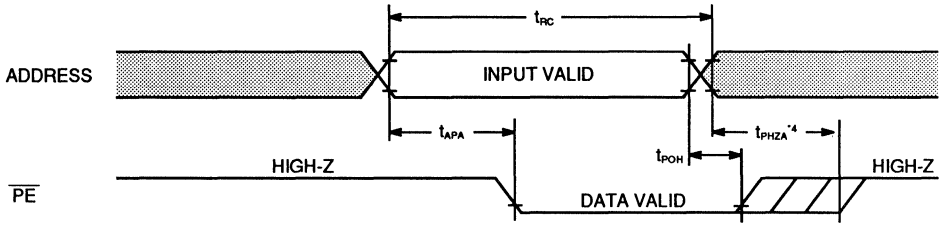


Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

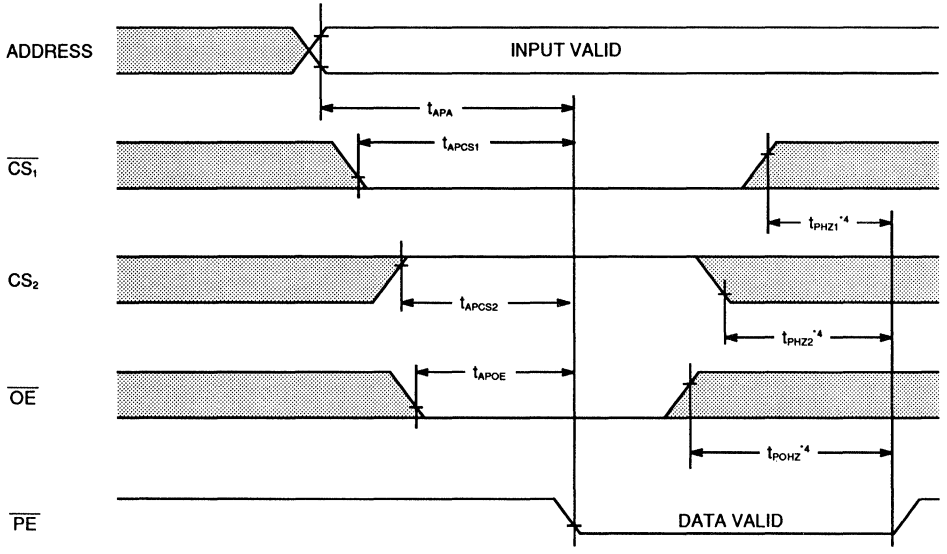
4

PARITY READ FUNCTION TIMING DIAGRAM*1, 5

1) ADDRESS CONTROLLED*2



2) $\overline{CS_1}$, CS_2 CONTROLLED*3



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS_1}$ = "L", CS_2 = "H" and $\overline{OE}$ = "L"
*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 When error occurred, $\overline{PE}$ pin outputs "L". But when no error, $\overline{PE}$ pin is in High-Z state.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1, *5, *6

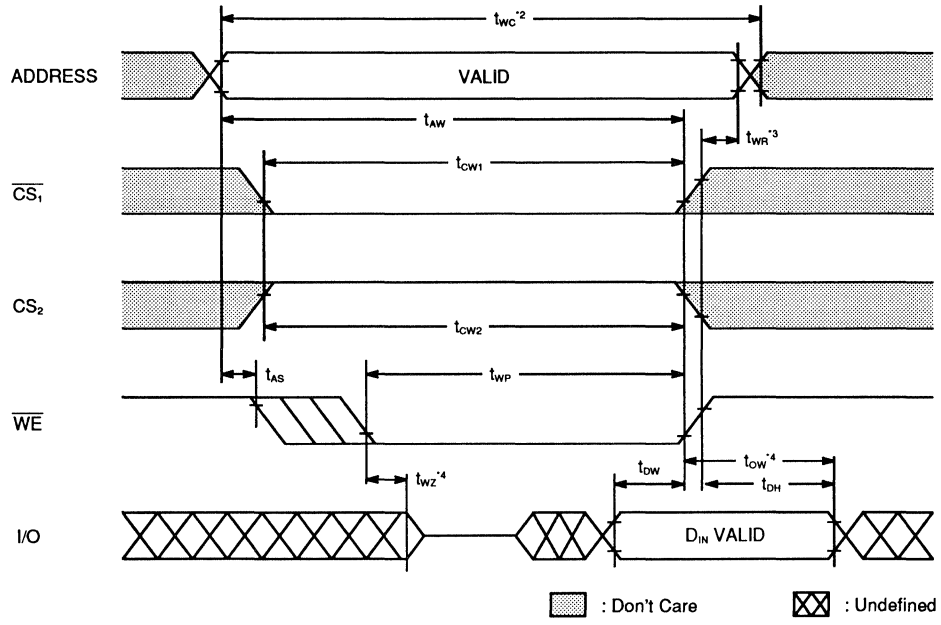
Parameter	Symbol	MB8287-25		MB8287-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	t_{WC}	25		35		ns
Address Valid to End of Write	t_{AW}	18		28		ns
$\overline{CS_1}$ to End of Write	t_{CW1}	16		26		ns
CS_2 to End of Write	t_{CW2}	13		20		ns
Data Setup Time	t_{DW}	8		12		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	15		20		ns
Write Recovery Time*3	t_{WR}	0		0		ns
Address Setup Time	t_{AS}	0		0		ns
Output Low-Z from $\overline{WE}$*4	t_{OW}	0		0		ns
Output High-Z from $\overline{WE}$*4	t_{WZ}	0	8	0	14	ns

Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycle are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*6 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

4

WRITE CYCLE TIMING DIAGRAM*1, *5 *6

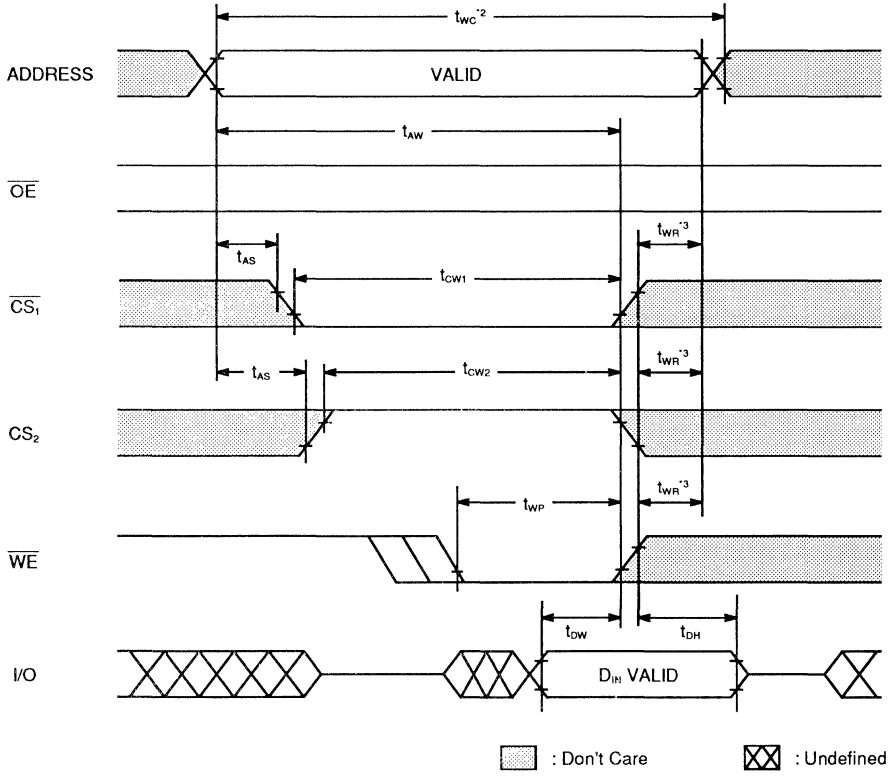
WRITE CYCLE No. 1 ($\overline{WE}$ CONTROLLED)



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.
*5 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*6 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

WRITE CYCLE TIMING DIAGRAM*1, *4, *5

WRITE CYCLE No. 2 ($\overline{CS_1}$, CS_2 CONTROLLED)

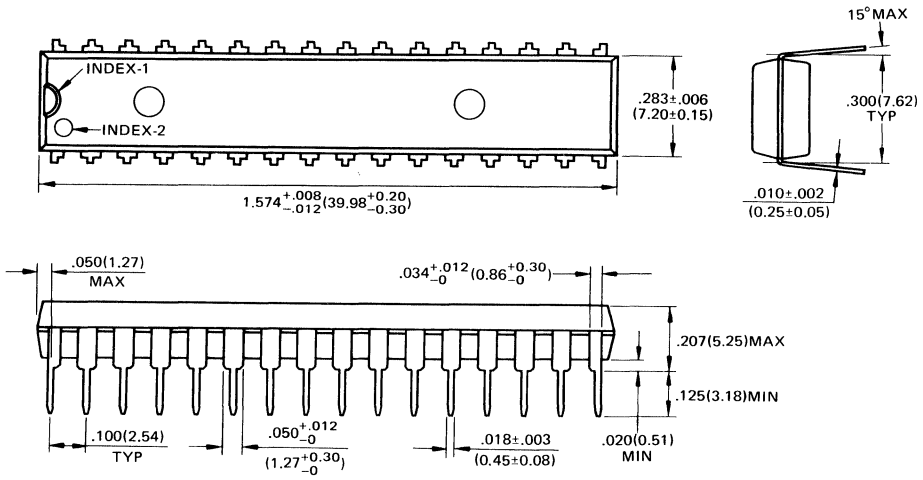


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 t_{WR} is defined from the end point of Write Mode.
*4 In normal Write Cycle, $\overline{PE}$ pin must be pulled-up to High.
*5 If data "L" is written in $\overline{PE}$ pin under the same timing as data input on I/O pins, "Error" information is written in the parity bit addressed forcibly.

4

PACKAGE DIMENSIONS

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M02)

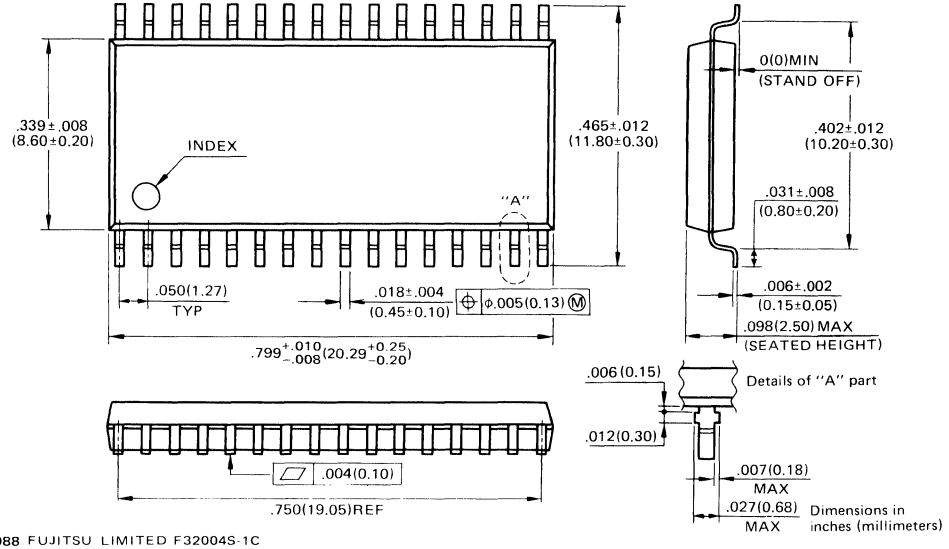


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M02)



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July 1990
Edition 3.0

FUJITSU

DATA SHEET

MB8421/8422-90/-90L/-90LL/-12/-12L/-12LL
CMOS 16K-BIT DUAL-PORT SRAM

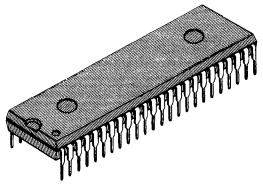
2K x 8 Bits CMOS Dual-Port Static Random Access Memory

The Fujitsu MB8421 and MB8422 are 2,048 words x 8 bits dual-port high-performance static random access memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus, no external clocks are required. MB8421 and MB8422 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation – a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$.

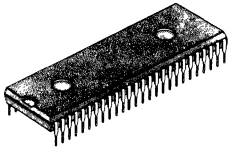
To avoid data contention on the same address, a $\overline{BUSY}$ input is provided for address arbitration; in addition, MB8421 utilizes an interrupt ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. Both devices use a single +5 V power supply and all pins are TTL-compatible.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.

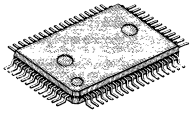
- Organization: 2,048 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 90$ ns max. (MB8421/22-90) (MB8421/22-90L) (MB8421/22/-90LL)
  $t_{AA} = t_{ACS} = 120$ ns max. (MB8421/22-12) (MB8421/22-12L) (MB8421/22/-12LL)
- Power consumption for the standard version:
  660 mW max. (Both ports active)
  385 mW max. (One port active)
  38.5 mW max. (Both ports standby, TTL)
  11 mW max. (Both ports standby, CMOS)
- Power consumption for the L and LL-versions:
  495 mW max. (Both ports active)
  275 mW max. (One port active)
  27.5 mW max. (Both ports standby, TTL)
  1.1 mW max. (Both ports standby, CMOS)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Address arbitration function: $\overline{BUSY}$ flag
- Interrupt function for communication between systems (*MB8421 only*): $\overline{INT}$ flag
- Data retention voltage: 2 V min.
- Standard Plastic Packages:
  48-pin DIP MB8422-xx(L/LL)P
  52-pin DIP MB8421-xx(L/LL)P
  64-pin QFP MB8421-xx(L/LL)PFQ



DIP–48P–M02
(MB8422)



DIP–52P–M01
(MB8421)



FPT–64P–M06
(MB8421)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS [1, 2]

Parameter	Designator	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	VIN	-0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	VOUT	-0.5 to V_{CC} +0.5	V
Output Current	IOUT	± 20	mA
Power dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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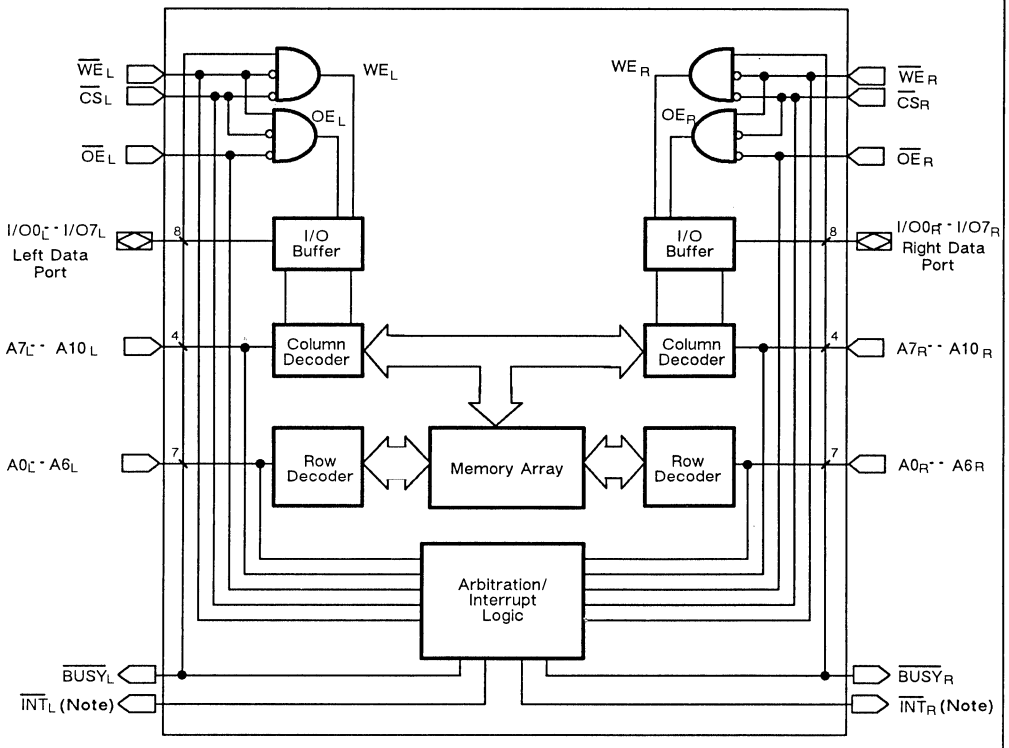
Fig. 1 — BLOCK DIAGRAM OF MB8421/22



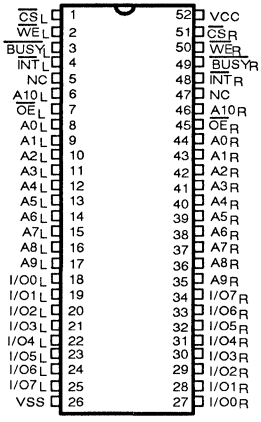
NOTES: MB8421 only.

I/O CAPACITANCE (T_A = 25 °C, f = 1 MHz)

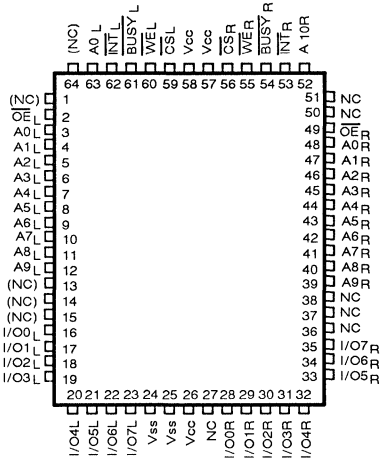
Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN		10	pF
I/O Capacitance (VI/O = 0V)	CI/O		10	pF

PIN ASSIGNMENTS

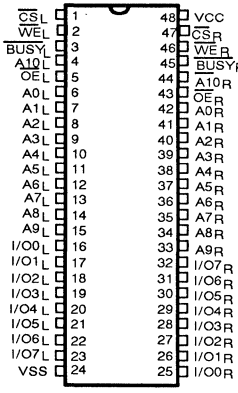
MB8421 - Top View
(DIP-52P-M01)



MB8421 - Top View
(FPT-64P-M01)



MB8422 - Top View
(DIP-48P-M02)



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PIN DESCRIPTIONS

Left Port	Right Port	Function	Left Port	Right Port	Function
$\overline{WE}_L$	$\overline{WE}_R$	Write Enable	$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select	$A0_L$ -- $A10_L$	$A0_R$-- $A10_R$	Address
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable	$I/O0_L$-- $I/O7_L$	$I/O0_R$-- $I/O7_R$	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag			
Vcc					Power (Common)
Vss					Ground (Common)

FUNCTIONAL OPERATION

The MB8421 and MB8422 provide two ports with separate control signals, address inputs, and input/output data pins that allow asynchronous read and write operations to any memory location. Each device has an on-chip automatic power-down feature controlled by $\overline{CS}$ that places the respective port in the standby mode when the chip is deselected ($\overline{CS}$ is HIGH).

When a port is enabled, access to the entire memory array is permitted. Each port has an independent Output Enable ($\overline{OE}$) control that is active in the read mode and enables the output drivers. Non-contention Read/Write conditions are shown in the following Truth Table; a simplified block diagram of the dual-port SRAM is shown in Fig. 1.

NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS[1]			RIGHT PORT INPUTS[1]			FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. $A0_L$-$A10_L \neq A0_R$ - $A10_R$
2. H = HIGH, L = LOW, X = Don't Care

ARBITRATION LOGIC

The arbitration logic resolves an address match or chip-enable match and determines the access priority. In both cases, an active $\overline{BUSY}$ flag is set for the port-in-waiting. Since both ports are asynchronous, there is the possibility of accessing the same memory location from both sides. In the read mode, this condition is not a problem. However, this is a problem when both ports are in a write mode with different data words or when one port is reading and the other is writing. When both ports access the same memory location, the on-chip arbitration logic determines which port has access and the $\overline{BUSY}$ flag for the delayed port is set active LOW and all operations on that port are inhibited. The delayed port can be accessed when the $\overline{BUSY}$ flag becomes inactive. Basic modes of abitration are described in subsequent paragraphs.

1. When addresses for both the left and right ports match and are valid before $\overline{CS}$ is active, the on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for device access. Refer to the following Truth Table for signal states; timing detail is shown later in this data sheet under "Data Contention Cycle No. 2 ($\overline{CS}$ controlled)."
2. When $\overline{CS}_L$ and $\overline{CS}_R$ are LOW before an address match, on-chip control logic arbitrates between the left and right addresses for device access. Signal states for this condition are shown in the following Truth Table; timing detail is shown under "Data Contention Cycle No. 1 (Address Controlled)."

ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Right Operation Permitted Left Operation Not Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, LST= Low Same Time, LBR = Low Before Right, LBL = Low Before Left

ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Right Operation Permitted Left Operation Not Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left

When both $\overline{CS}_L$ and $\overline{CS}_R$ are low at the same time ($\overline{CS}$ controlled) or when both left-and-right addresses are valid at the same time (address controlled), the $\overline{BUSY}_R$ flag for the right port is set to the active LOW state and access is granted to the left port.

For the Intel 8086 and Fujitsu's MBL8086 as well as most other microprocessors, the asynchronous $\overline{BUSY}$ signal can be directly tied to the READY input, providing setup-and-hold time requirements are met.

INTERRUPT FUNCTION

The Interrupt ($\overline{INT}$) function provides communication between systems on both sides of the dual-port RAM. $\overline{INT}_L$ is set LOW when the processor on the right port writes to address 7FE (A0 = L and A1-A10 = H). When the left port acknowledges by reading address 7FE, $\overline{INT}_L$ is then reset to HIGH. In essence, address 7FE serves as an 8-bit mailbox that transfers information from the right port to the left port. When $\overline{INT}_R$ is set LOW, the processor on the left port writes to address 7FF (A0-A10=H). When the right port acknowledges by reading address 7FF, $\overline{INT}_R$ is then reset to HIGH. Hence, address 7FF serves as a second 8-bit mailbox, transferring information from the left port to the right port.

On power-up, $\overline{INT}_L$ and $\overline{INT}_R$ are set to a HIGH state. However, if one port is in the standby mode, the standby port can still be interrupted by the processor on the other port. But if the $\overline{BUSY}$ flag is set to the LOW state, the port associated with that flag cannot set or reset the $\overline{INT}$ flag.

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	Vcc	4.5	5.0	5.5	V
Operating Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8421/ MB8422-90/12		MB8421/MB8422 -90L/-90LL/-12L/-12LL		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	ICC	Cycle = Min Duty = 100% IOUT = 0 mA		120		90	mA
Standby Supply Current	ISB1	Both ports at Standby $\overline{CS}_L$ & $\overline{CS}_R$ = VIH		7		5	mA
	ISB2	One port at Standby $\overline{CS}_L$ or $\overline{CS}_R$ =VIH, IOUT = 0 mA		70		50	mA
	ISB3	Both ports at Full Standby $\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc -0.2V		2		0.2	mA
	ISB4	One port at Full Standby $\overline{CS}_L$ or $\overline{CS}_R \geq$ Vcc -0.2V IOUT = 0 mA		70		50	mA
Input Leakage Current	ILI	VIN = 0V to Vcc	-10	10	-10	10	µA
Output Leakage Current	ILO	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	-10	10	-10	10	µA
Input High Voltage	VIH		2.2	Vcc +0.3	2.2	Vcc +0.3	V
Input Low Voltage	VIL		-0.3	0.8	-0.3	0.8	V
Output High Voltage	VOH (Note)	IOUT = -1.0 mA	2.4		2.4		V
Output Low Voltage	VOL	IOUT = 3.2 mA		0.4		0.4	V
Output Low Voltage for Open-Drain	VOL	IOUT = 8 mA		0.4		0.4	V

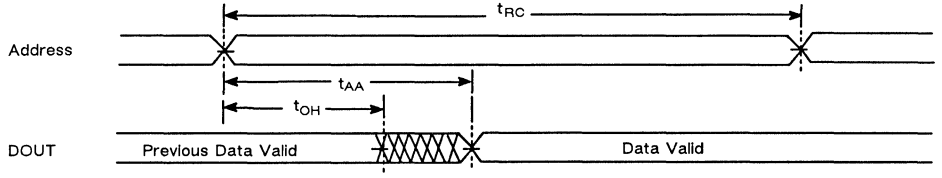
NOTE: The $\overline{BUSY}$ and $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC CHARACTERISTICS

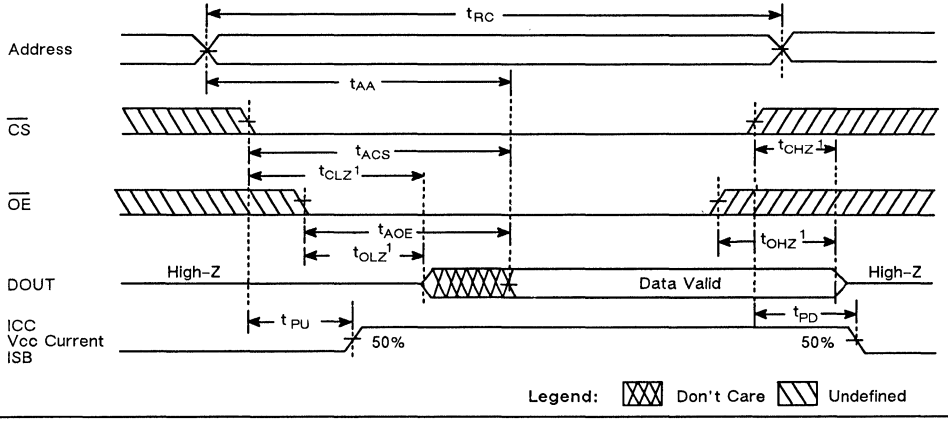
(Recommended Operations Conditions unless otherwise noted.)

Parameter	Symbol	MB8421-90/90L/90LL MB8422-90/90L/90LL		MB8421-12/12L/12LL MB8422-12/12L/12LL		Unit
		Min	Max	Min	Max	
Read Cycle Parameters & Timing Diagrams						
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z (Note 1)	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z (Note 1)	t_{OLZ}	5		5		ns
Chip Select to Output High-Z (Note 1)	t_{CHZ}		40		50	ns
Output Enable to Output High-Z (Note 1)	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

Read Cycle No. 1 [2, 3]:



Read Cycle No. 2 [2]:



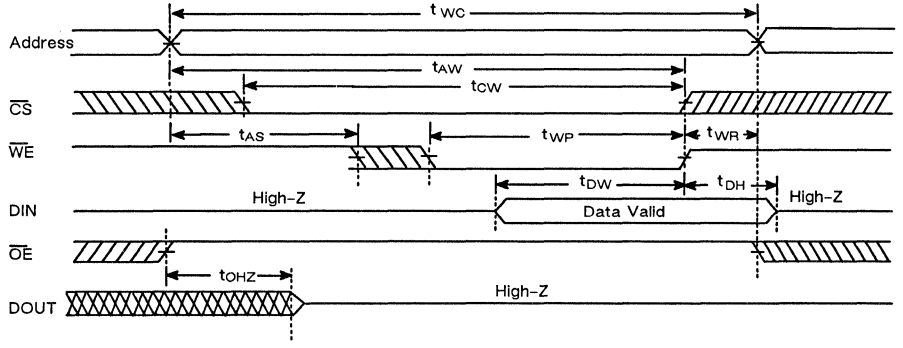
NOTES:

1. Transition is measured at a point of ± 500 mV from steady-state voltage with an output capacitance of 5pF.
2. $\overline{WE}$ is High during read cycle.
3. Device is continuously selected ($\overline{CS}$ = $\overline{OE}$ = VIL).

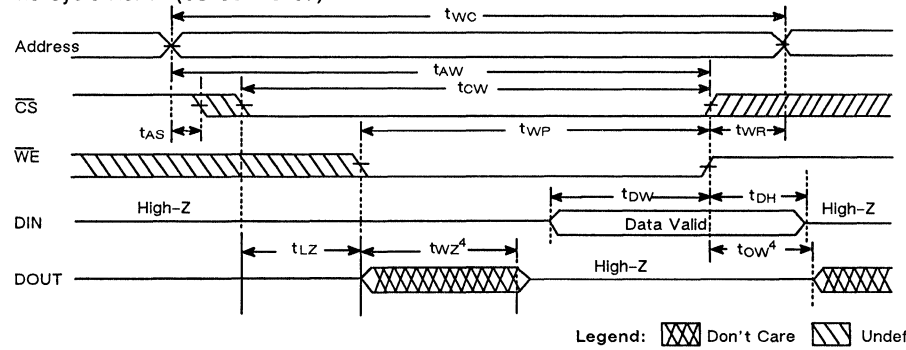
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L/90LL MB8422-90/90L/90LL		MB8421-12/12L/12LL MB8422-12/12L/12LL		Unit
		Min	Max	Min	Max	
Write Cycle Parameters & Timing Diagrams						
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z (Note 4)	t_{OW}	0		0		ns
Write Enable to Output High-Z (Note 4)	t_{WZ}		40		50	ns

Write Cycle No. 1 ($\overline{WE}$ Controlled) [1,2]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [1,2,3]



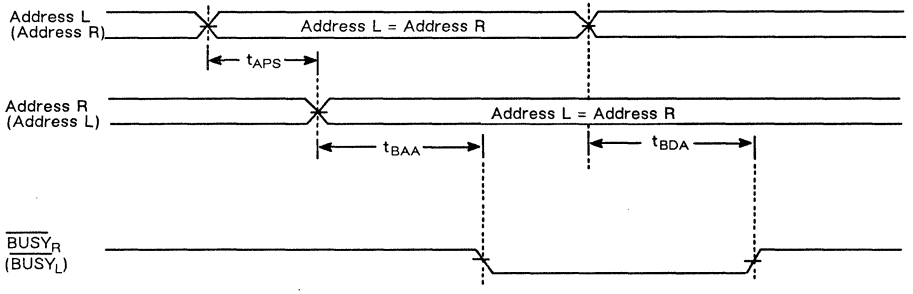
Legend: Don't Care, Undefined

NOTES:
1. The Write Enable ($\overline{WE}$) signal must be high during an address transition.
2. If the Output Enable ($\overline{OE}$) and Chip Select ($\overline{CS}$) signals are in the Read Mode, the associated I/O pins are in the output state; accordingly, input signals of opposite phase must not be applied to the outputs.
3. If $\overline{CS}$ goes high prior to or coincident with the low-to-high transition of $\overline{WE}$, the output remains in high-impedance state.
4. This parameter is specified at a point ± 500 mV from steady-state voltage with an output capacitance of 5 pF.

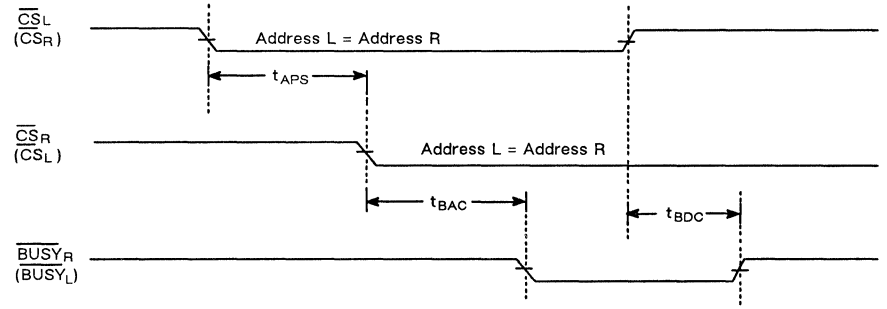
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
$\overline{BUSY}$ Parameters & Data Contention Timing						
$\overline{BUSY}$ Access Time from Address	t_{BAA}		45		60	ns
$\overline{BUSY}$ Output High-Z from Address	t_{BDA}		45		60	ns
$\overline{BUSY}$ Access Time from $\overline{CS}$	t_{BAC}		45		60	ns
$\overline{BUSY}$ Output High-Z from $\overline{CS}$	t_{BDC}		45		60	ns
Arbitration Priority Set up Time	t_{APS}	20		25		ns

Data Contention Cycle No. 1 (Address Controlled)[1, 2]:



Data Contention Cycle No. 2 ($\overline{CS}$ Controlled)[1, 3]:



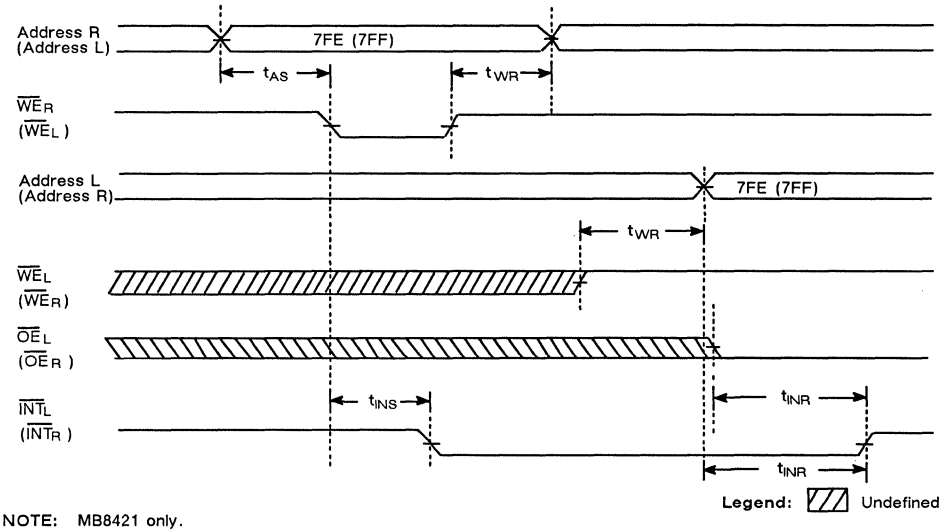
NOTES:

1. In case of dual-access at the same memory location, the port that accesses the RAM first sets the $\overline{BUSY}$ flag HIGH.
2. Chip Select ($\overline{CS}$) signal must be low before or coincident with an address transition.
3. Address is valid prior to or coincidence with the high-to-low transition of $\overline{CS}$.

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
Interrupt Parameters & Timing Diagram						
$\overline{INT}$ Set Time (Note)	t_{INS}		80		100	ns
$\overline{INT}$ Reset Time (Note)	t_{INR}		80		100	ns

Interrupt Cycle Timing

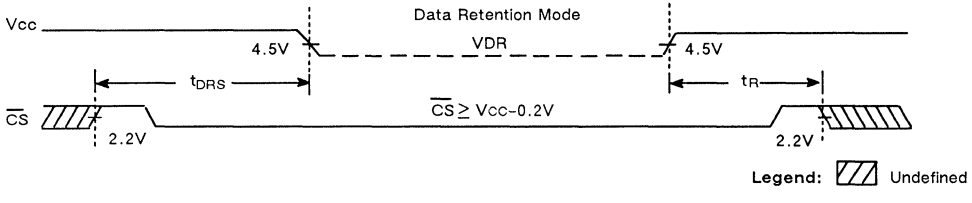


NOTE: MB8421 only.

AC CHARACTERISTICS (Continued)

DATA RETENTION PARAMETERS & TIMING

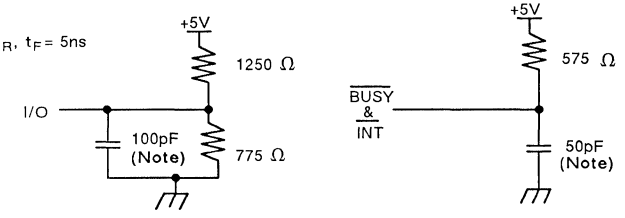
Parameter	Symbol	MB8421-90/12 MB8422-90/12		MB8421-90L/12L MB8422-90L/12L		Unit
		Min	Max	Min	Max	
Data Retention Parameters & Timing						
Data Retention Supply Voltage	VDR	2.0	5.5	2.0	5.5	V
Data Retention Supply Current (Note)	IDR		0.2		0.02	mA
Data Retention Setup Time	t_{DRS}	0		0		ns
Operation Recovery Time	t_R	t_{RC}		t_{RC}		ns



NOTE: Vcc = VDR = 3V
$\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc - 0.2

AC TEST CONDITIONS

Input Pulse Levels: 0 to 3.0V
Input Pulse Rise & Fall Times: t_R, t_F = 5ns
Timing Reference Levels: 1.5V
Output Loads:



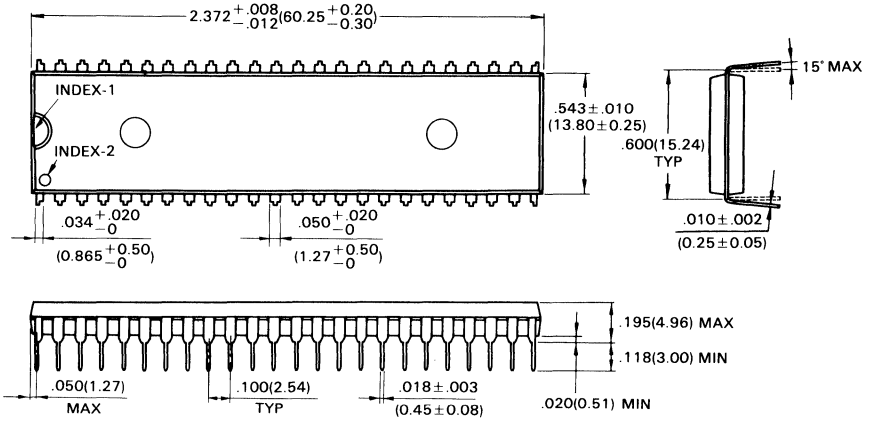
NOTE: Includes jig and stray capacitance.

PACKAGE DIMENSIONS

(Suffix: P)

48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M02)

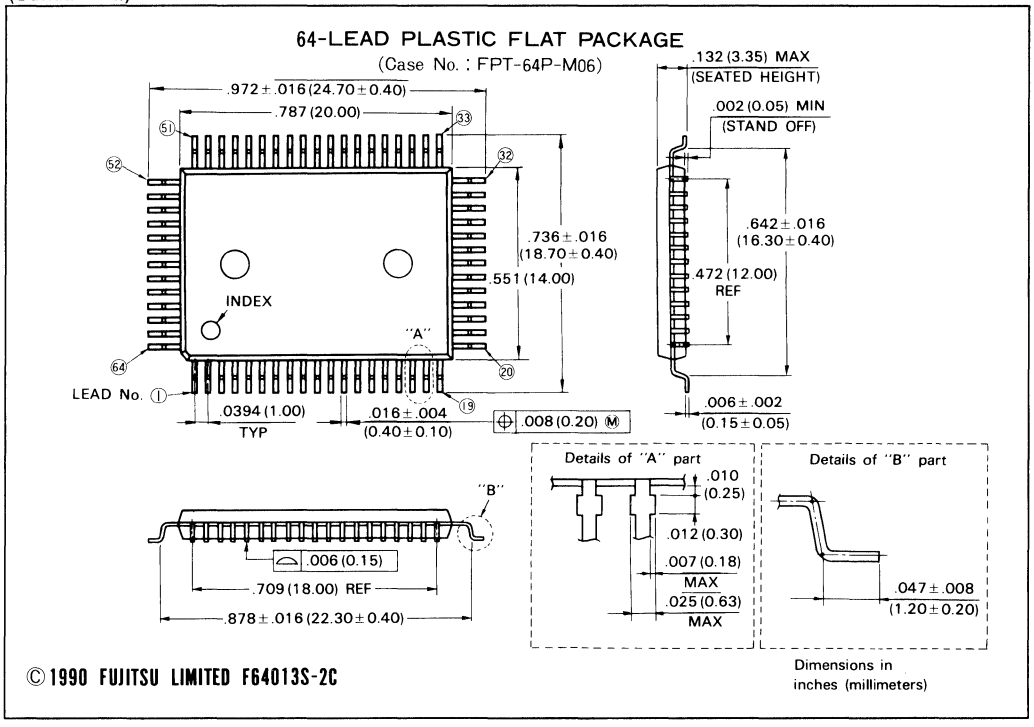


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

(Suffix: PFQ)



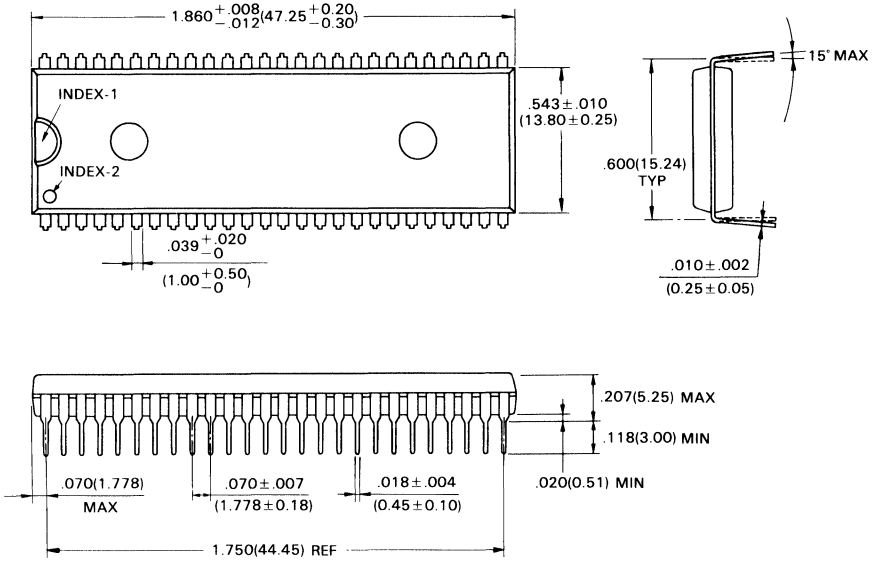
4

PACKAGE DIMENSIONS (Continued)

(Suffix: P)

52-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-52P-M01)



Dimensions in
inches (millimeters)

4

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB8431/32-90/-90L/-90LL/-12/-12L/-12LL
CMOS 16K-BIT DUAL-PORT SRAM

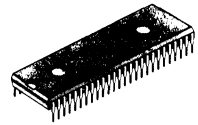
2K x 8 Bits CMOS Dual-Port Static Random Access Memory

The Fujitsu MB8431 and MB8432 are 2,048 words x 8 bits dual-port static high performance, random access memories fabricated with CMOS technology. MB8431 and MB8432 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation – a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$.

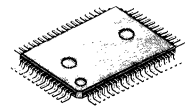
To avoid data contention on the same address, a $\overline{BUSY}$ input is provided for address arbitration; in addition, MB8431 utilizes an interrupt ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. Both devices use a single +5 V power supply and all pins are TTL-compatible. A simplified block diagram of the SRAM is shown in Figure 1.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.

- Organization: 2,048 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 90$ ns max. (MB8431/32-90)
  (MB8431/32-90L/-90LL)
  $t_{AA} = t_{ACS} = 120$ ns max. (MB8431/32-12)
  (MB8431/32-12L/-12LL)
- Power consumption for the standard version:
  660 mW max. (Both ports active)
  385 mW max. (One port active)
  38.5 mW max. (Both ports standby, TTL)
  11 mW max. (Both ports standby, CMOS)
- Power consumption for the L and LL-versions:
  495 mW max. (Both ports active)
  275 mW max. (One port active)
  27.5 mW max. (Both ports standby, TTL)
  1.1 mW max. (Both ports standby, CMOS)
- Single +5 V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Data retention voltage: 2 V min.
- Address arbitration function: $\overline{BUSY}$ input
- Interrupt function for communication between systems (*MB8431 only*): $\overline{INT}$ flag
- Expansion capability using MB8421/22 (Master) and MB8431/32 (Slave)
- Standard Plastic Packages:
  48-pin DIP MB8432-xx(L/LL)P
  52-pin DIP MB8431-xx(L/LL)P
  64-pin QFP MB8431-xx(L/LL)PFQ



DIP–52P–M01
(MB8431)



FPT–64P–M01
(MB8431)

DIP–48P–M02
(MB8432)

Pin Assignment

See page 4–81

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

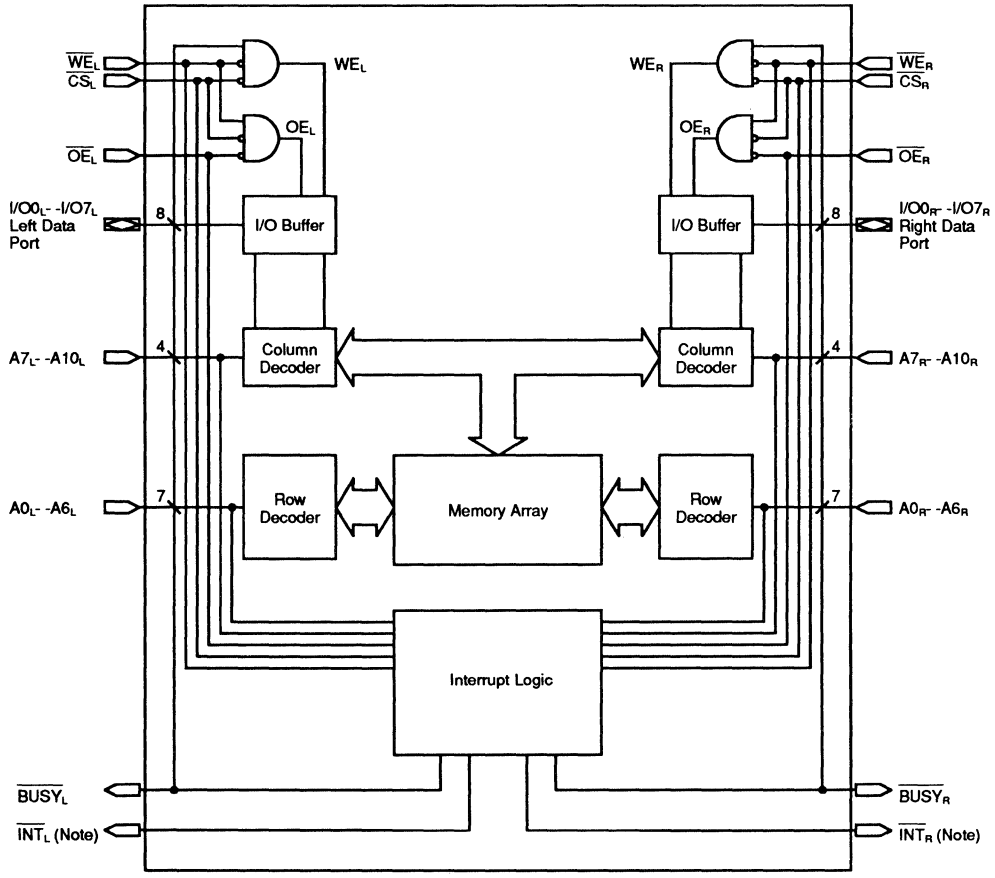
4

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS_L}$	$\overline{CS_R}$	Chip Select Input
$\overline{WE_L}$	$\overline{WE_R}$	Write Enable Input
$\overline{OE_L}$	$\overline{OE_R}$	Output Enable Input
$\overline{INT_L}$	$\overline{INT_R}$	Interrupt * Flag Output
$\overline{BUSY_L}$	$\overline{BUSY_R}$	Busy Flag Input
$A0_L$ to $A10_L$	$A0_R$ to $A10_R$	Address Input
$I/O0_L$ to $I/O7_L$	$I/O0_R$ to $I/O7_R$	Data Input/Output
V_{CC}		Power
GND		Ground

*: Applies to MB8431 only.

Fig. 1 — MB8431/32/31L/32L BLOCK DIAGRAM



Note: MB8431 only.

4

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN=0V)	C_{IN}		10	pF
I/O Capacitance (VI/O=0V)	$C_{I/O}$		10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS

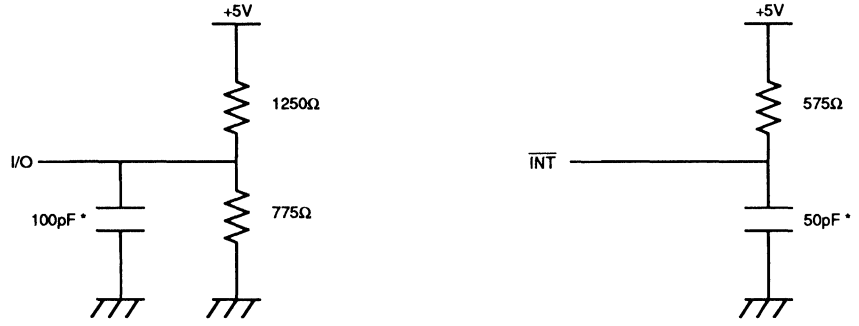
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8431/ MB8432-90/12		MB8431/ MB8432-90L/90LL/12L/12LL		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	I_{CC}	Cycle=Min. Duty=100% I_{OUT}=0mA		120		90	mA
Standby Supply Current	I_{SB1}	Both ports=Standby $\overline{CS_L}$ & $\overline{CS_R}$=V_{IH}		7		5	mA
	I_{SB2}	One port=Standby $\overline{CS_L}$ or $\overline{CS_R}$=V_{IH}, I_{OUT}=0mA		70		50	mA
	I_{SB3}	Both ports=Full standby $\overline{CS_L}$ & $\overline{CS_R}$≥V_{CC}–0.2V		2		0.2	mA
	I_{SB4}	One port=Full standby $\overline{CS_L}$ or $\overline{CS_R}$≥V_{CC}–0.2V, I_{OUT}=0mA		70		50	mA
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	–10	10	–10	10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, I/O=0V to V_{CC}	–10	10	–10	10	µA
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3 *1	0.8	–0.3 *1	0.8	V
Output High Voltage	V_{OH} *2	I_{OUT}=–1.0mA	2.4		2.4		V
Output Low Voltage	V_{OL}	I_{OUT}=3.2mA		0.4		0.4	V
Output Low Voltage for Open-Drain	V_{OL}	I_{OUT}=8mA		0.4		0.4	V

*1 Undershoot –3.0V min at less than 20ns pulse width.
*2 The $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: tR, tF=5ns
- Timing Reference Levels: 1.5V
- Output Load



* Including Jig and stray capacitance

4

AC CHARACTERISTICS

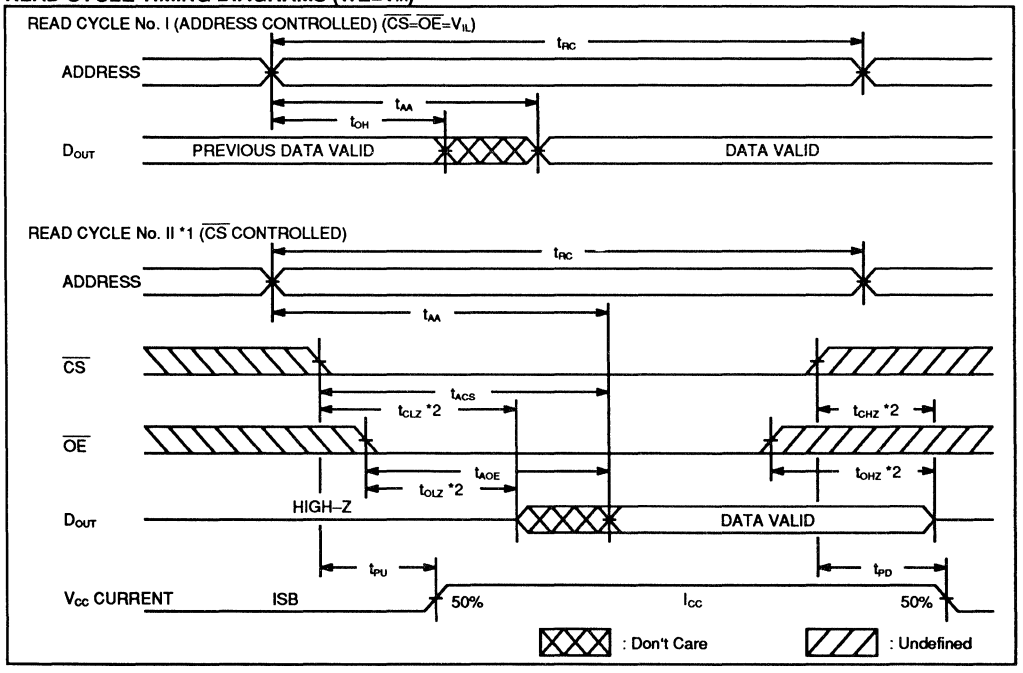
(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z *2	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z *2	t_{OLZ}	5		5		ns
Chip Select to Output High-Z *2	t_{CHZ}		40		50	ns
Output Enable to Output High-Z *2	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

4

READ CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

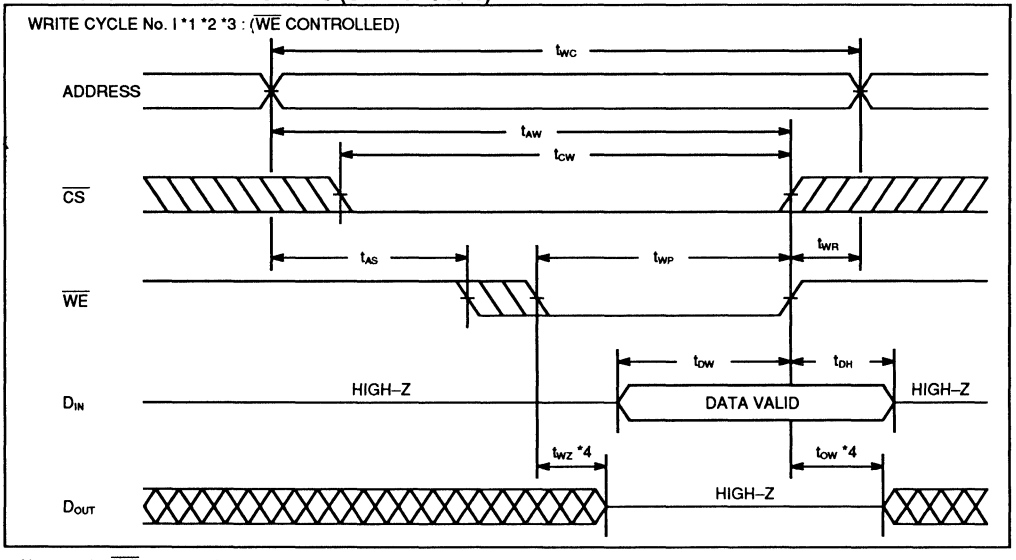


Note: *1 Address should be fixed before high-to-low transition of $\overline{CS}$.
*2 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

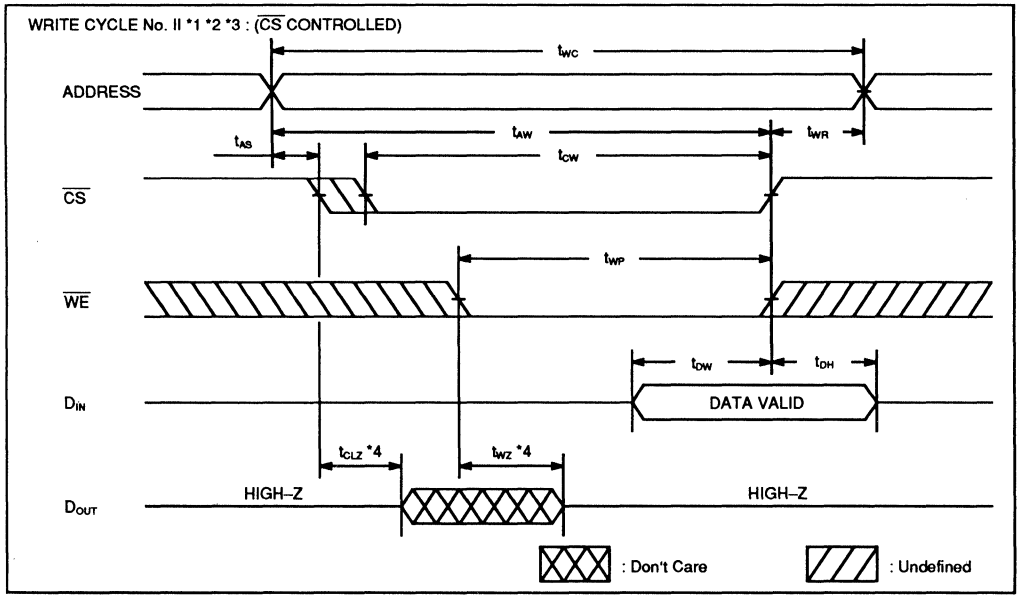
WRITE CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z *4	t_{OW}	0		0		ns
Write Enable to Output High-Z *4	t_{WZ}		40		50	ns

WRITE CYCLE TIMING DIAGRAMS ($\overline{OE}$=Don't care)



Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 Transition is measured at the point of ±500mV from steady state voltage with C_L=5pF.



Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

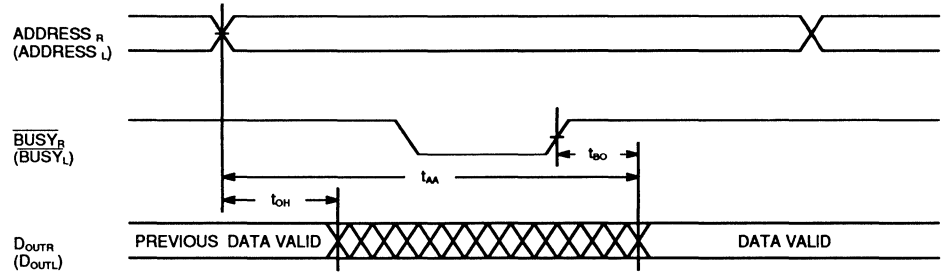
4

SLAVE BUSY TIMING

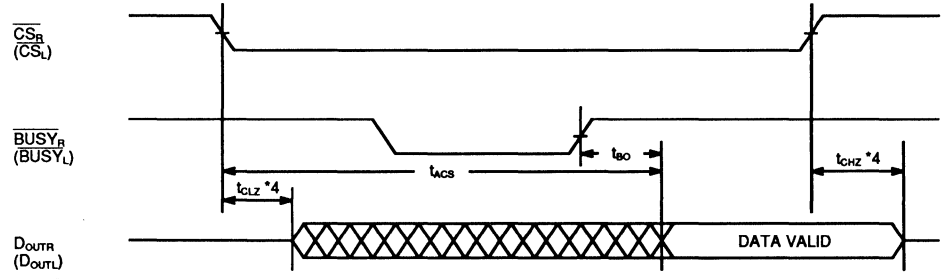
Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Busy Access Time	t_{BO}		0		0	ns
Write Set Up Time To Busy	t_{WS}	−10		−10		ns
Write Hold Time From Busy	t_{WH}	20		25		ns

CONTENTION CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

CONTENTION READ CYCLE No. I *1 *2 : (ADDRESS CONTROLLED) ($\overline{CS}$=$\overline{OE}$=V_{IL})



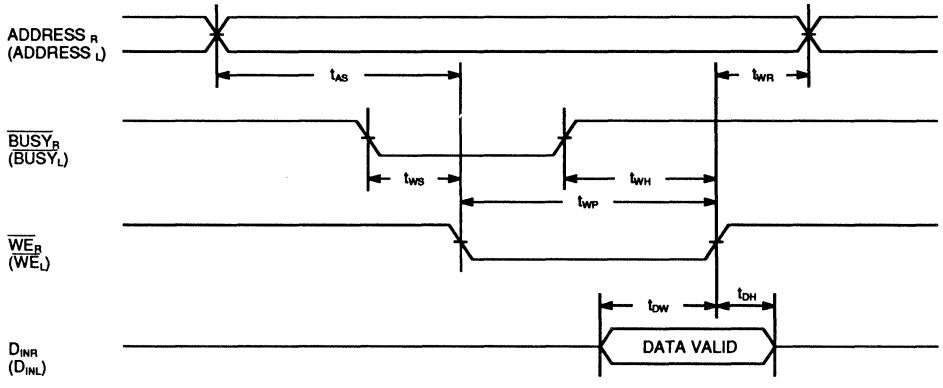
CONTENTION READ CYCLE No. II *1 *3 : ($\overline{CS}$ CONTROLLED)



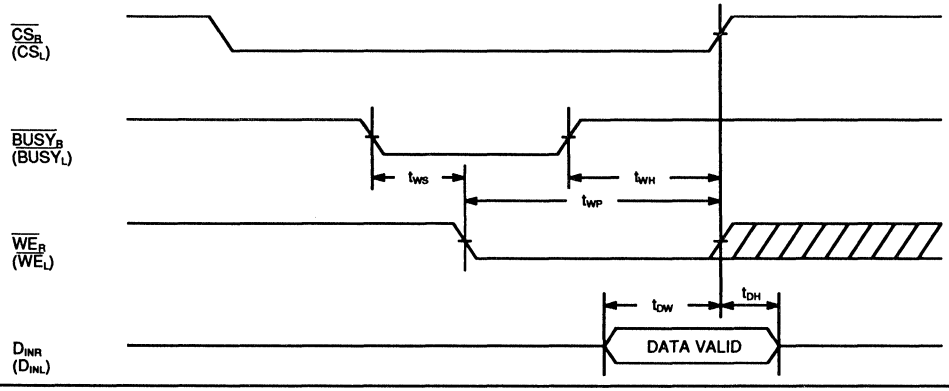
Note: *1 In case of dualaccess at the same memory location, the port that access the RAM first sets the $\overline{BUSY}$ flag high.
*2 $\overline{CS}$ must be low before or coincident with transition of address.
*3 Address is valid prior to cincident with high-to-low transition of $\overline{CS}$.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

CONTENTION CYCLE TIMING DIAGRAMS

CONTENTION WRITE CYCLE No. I *1 *2 *3 ($\overline{WE}$ CONTROLLED)



CONTENTION WRITE CYCLE No. II *3 : *1 *2 *3 ($\overline{CS}$ CONTROLLED)

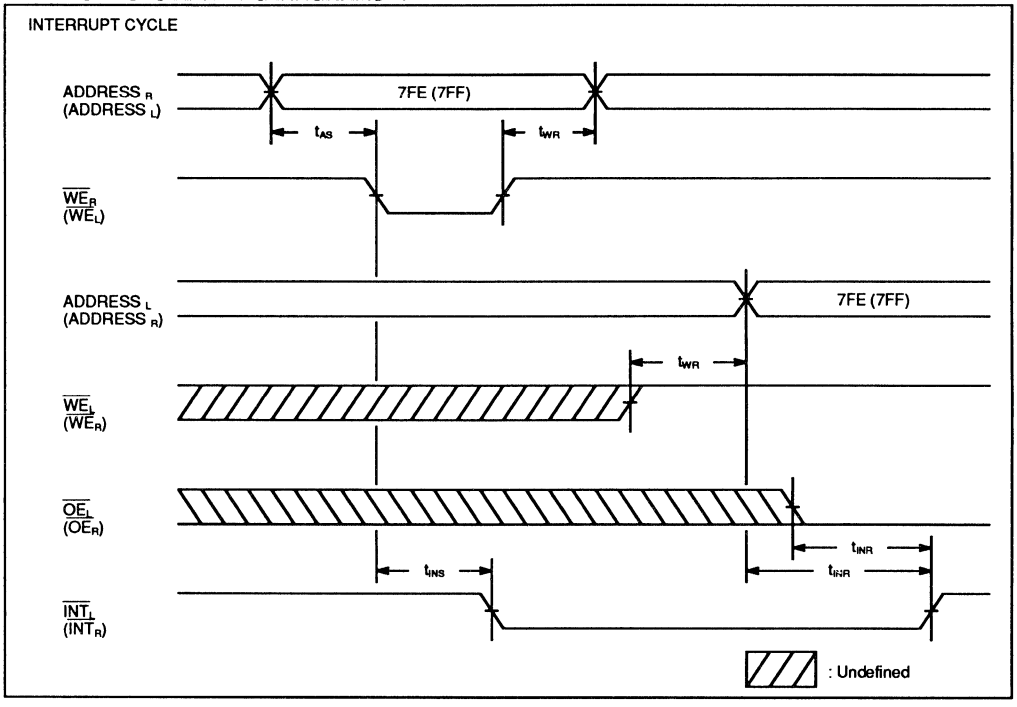


Note: *1 $\overline{WE}$ must be high during address transition.
*2 I/O pins are in the output state, so the input signals of opposite phase must not be applied.
*3 During $\overline{BUSY}$ input is low, write operation can not be excuted even if $\overline{WE}$ is low.

INTERRUPT TIMING *1

Parameter	Symbol	MB8431–90/90L/90LL MB8432–90/90L/90LL		MB8431–12/12L/12LL MB8432–12/12L/12LL		Unit
		Min	Max	Min	Max	
INT Set Time	t_{INS}		80		100	ns
INT Reset Time	t_{INR}		80		100	ns

INTERRUPT CYCLE TIMING DIAGRAMS *1



Note: *1 Applies to MB8431 only.

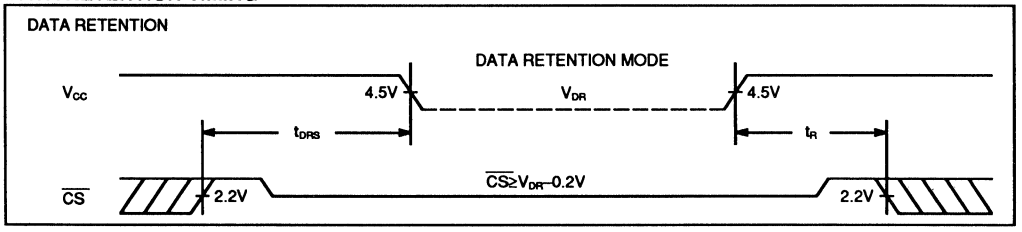
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			0.2	mA
	L-Version				20	μA
	LL-Version *2				2	μA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $V_{CC}=V_{DR}=3V$, $\overline{CS_L}$ & $\overline{CS_R}\geq V_{CC}-0.2V$
*2 $V_{DR}=3V$, $T_A=0°C$ to $40°C$

DATA RETENTION TIMING



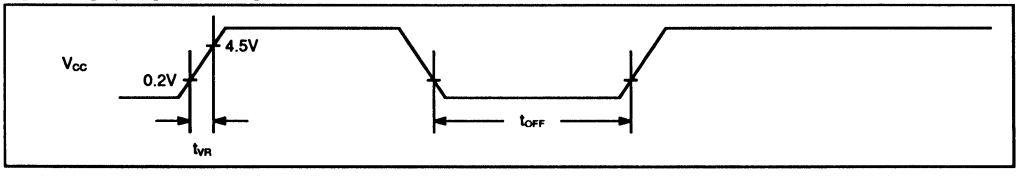
POWER ON/RESET CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Power Up Time *1	t_{VR}	0.05	50	0.05	50	ms
Power Off Time *2	t_{OFF}	1		1		S

*1 This is required to keep normal operation for power on/reset circuit which initialize $\overline{INT}$ output to "H" automatically when V_{CC} is applied.
*2 This is required to keep normal operation for power on/reset circuit which V_{CC} is repeatly turn on/off.

POWER ON/RESET TIMING

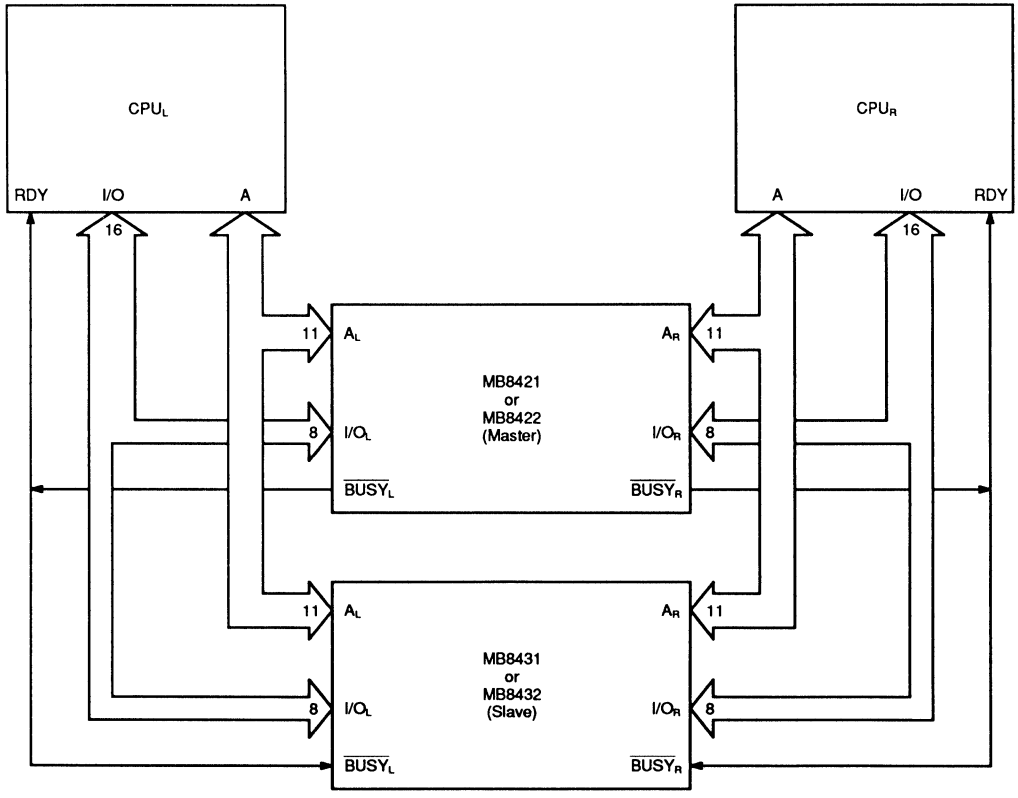


Function Description:

1. ORGANIZATION:
   MB8431/32 are 2K words x 8 bit Dual port Static Random Access Memory.
   Each port has independent addresses, chip select ($\overline{CS}$), write enable ($\overline{WE}$), output enable ($\overline{OE}$) and data input/output (I/O) functions.

2. SLAVE BUSY FUNCTION:
   In order to do bit expansion using 8 bit width dual port RAM such as MB8421/22, two or more parts should be connected paralel. But such case, there is a possibility, which depends on arbitration timing, of outputting $\overline{BUSY}$ signal to different ports and put both CPUs in waiting state. This causes a trouble. Using MB8431/32 which have slave busy function (busy input) is one of the solutaion for such trouble. Bit expansion is easily achievable to pair-use slave type dual port RAM such as MB8431/32 and master type dual port RAM such as MB8421/22.

(Example)
As an example, Fig1 shows 16 bit dual port memory system.
In this system, master type Dual port RAM (MB8421/22) judge arbitration for address contention and output result of the judgement from $\overline{BUSY}$ pin. This output returned to CPU and make the CPU in waiting state and also the output is applied to slave type dual port RAM (MB8431/32).
Though slave type dual port RAM (MB8431/32) do not judge for arbitration, they have $\overline{BUSY}$ input pin and inhibit write operation of the correspondent port during "L" signal form $\overline{BUSY}$ output of master type dual port RAM (MB8421/22) is applied to the $\overline{BUSY}$ input.
A system consists of one master dual port RAM (MB8421/22) and three slave dual port RAMs (MB8431/32) is harmonized for 32 bit application.



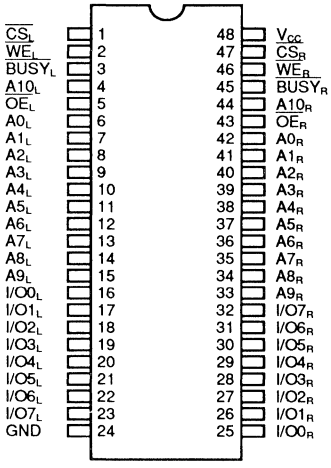
3. INTERRUPT FUNCTION:
The interrupt function ($\overline{INT}$) is provided to allow communication between the systems on either sides of the dual–port RAM. $\overline{INT}_L$ is set to low, when the processor on the right port writes to address 7FE (A0=L and A1 to A10=H). $\overline{INT}_L$ is then reset to High, when the left port acknowledges by reading the same address 7FE. Thus the address 7FE is like a 8 bit word mail–box transferring information from the right–port to the left–port.

$\overline{INT}_R$ on the other hand is set to low, when processor on the left port writes to the address 7FF (A=0 to A10=H). $\overline{INT}_R$ is reset to High, when the right port acknowledges by reading this address. Hence, the address 7FF is a second 8 bit word mail–box transferring information form the left port to the right port.

The $\overline{INT}_L$ and $\overline{INT}_R$ are set to High on power–up. If the port is in the standby mode, it can still get interrupted by the processor on the other side.

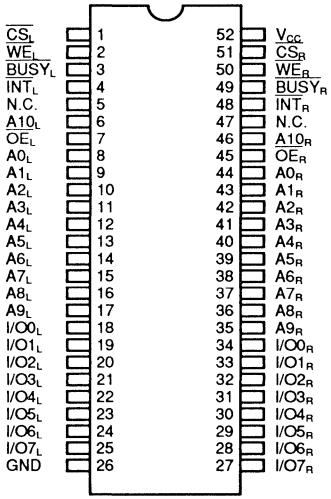
In case he $\overline{BUSY}$ flag is set to low, then the pertinent port can not set or reset the $\overline{INT}$ flag.

TOP VIEW

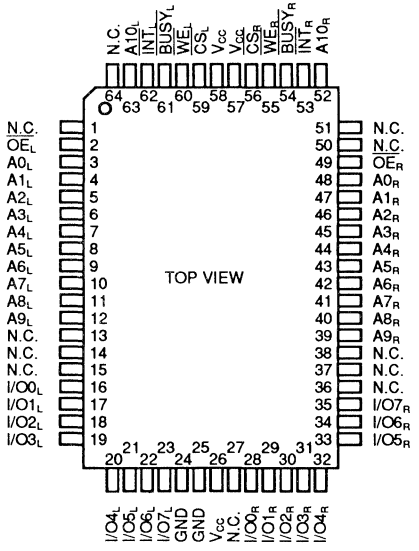


MB8432

TOP VIEW



MB8431

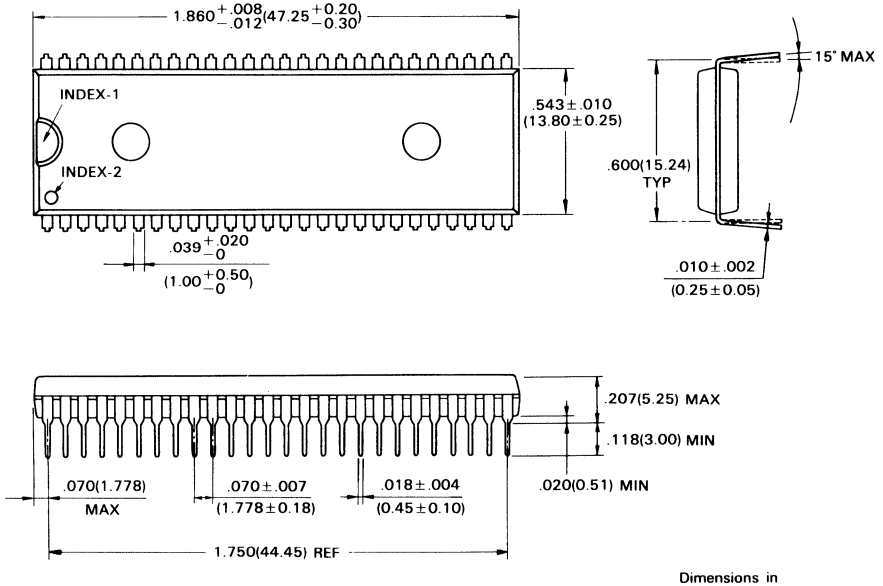


MB8431

4

52-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-52P-M01)

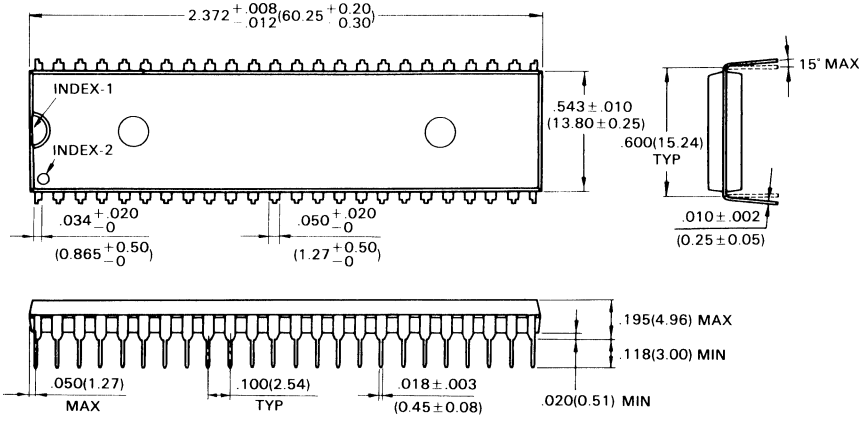


Dimensions in
inches (millimeters)

4

48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M02)

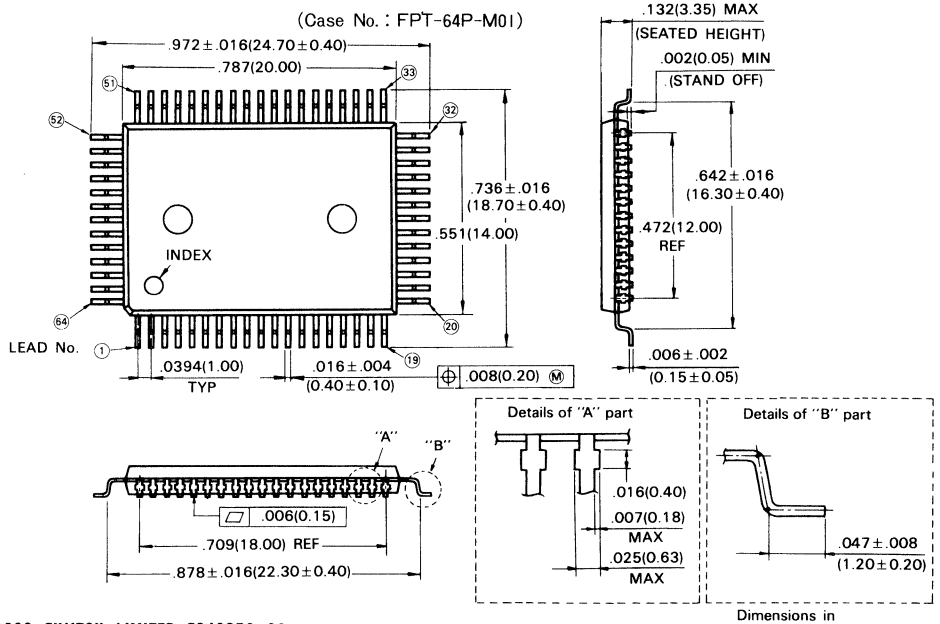


Dimensions in
inches (millimeters)

4

64-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-64P-M01)



Dimensions in
inches (millimeters)

4

September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB8441-45/-55
CMOS 64K-BIT DUAL PORT SRAM

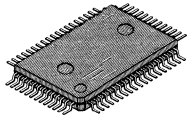
8K X 8 Bits CMOS Dual Port Static Random Access Memory

ADVANCE INFORMATION

The Fujitsu MB8441 is a dual-port high-performance static random access memory (SRAM) organized as 8,192 words x 8 bits and fabricated using CMOS technology. The SRAM uses asynchronous circuits; thus, no external clocks are required. The MB8441 provides the user with two separately controlled I/O ports with independent addresses: Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation — a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$. The MB8441 can be used in either a master or slave operation (controlled by the $\overline{BE}$ pin).

To avoid data contention on the same address, a $\overline{BUSY}$ flag is provided for address arbitration. In addition, the MB8441 utilizes an interrupt ($\overline{INT}$) flag which allows communication between systems that are on either side of the RAM. A single +5 V power supply is needed and all pins are TTL compatible.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.



(FPT-64P-M06)

Plastic Package
(FPT-64P-M05)

- Organization: 8,192 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 45$ ns max. (MB8441-45)
  $t_{AA} = t_{ACS} = 55$ ns max. (MB8441-55)
- Low power consumption: 660 mW max. (Both ports active/standby)
  1.1 mW max. (Both ports standby, CMOS)
  27.5 mW max. (Both ports standby, TTL)
- Single power +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Address Arbitration: ($\overline{BUSY}$) flag output (Master Operation: $\overline{BE}$ = L)
  ($\overline{BUSY}$) flag output (Master Operation: $\overline{BE}$ = H)
- Interrupt function for communication between systems: $\overline{INT}$ flag.
- Data retention voltage: 2.0 V min.
- Standard 64-pin Plastic Package:
  SOP MB8441-xxPF

Absolute Maximum Ratings (See Note)

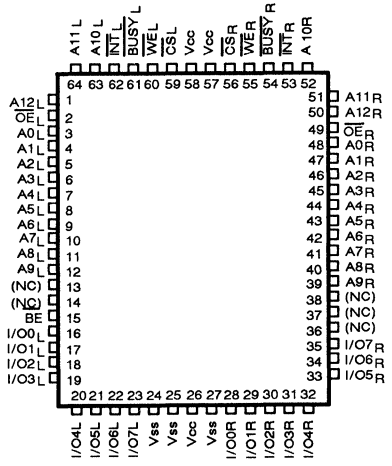
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

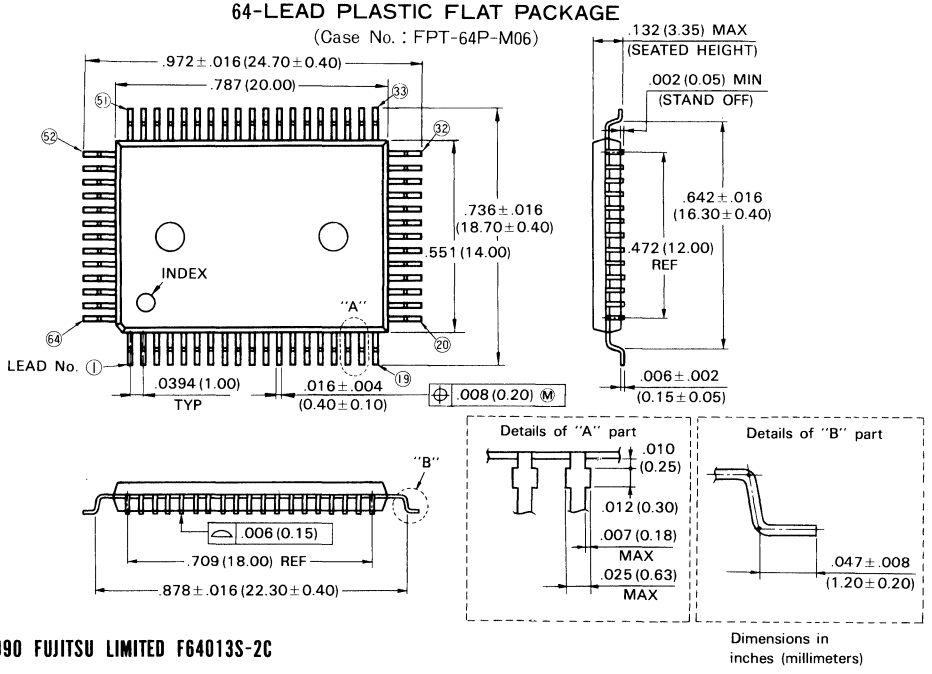
PIN ASSIGNMENTS

Top View
(FPT-64P-M06)



4

PACKAGE DIMENSIONS



Dimensions in
inches (millimeters)

4

Section 5

Extended Temperature Range SRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
5–3	MB8464A–10–X, –10LL-X	100	65536 bits	28-pin Plastic DIP, SOP
	–15–X, –15LL–X	150	(8192 x 8)	32-pad Ceramic LCC
5–15	MB84256A–70–X, –70LL-X	70	262147 bits	28-pin Plastic DIP, SOP
	–10–X, –10LL–X	100	(32768 x 8)	

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January1990
Edition 1.0

FUJITSU

DATA SHEET

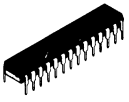
MB8464A-10-X/-10LL-X/-15-X/-15LL-X
CMOS 64K-BIT LOW-POWER SRAM

8K Words x 8 Bits CMOS Static RAM for Extended Temperature Operation

The Fujitsu MB8464A-X is an 8,192 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

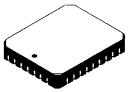
The MB8464A-X has low power dissipation, low cost and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

PLASTIC PACKAGE
DIP-28P-M02



PLASTIC PACKAGE
DIP-28P-M04

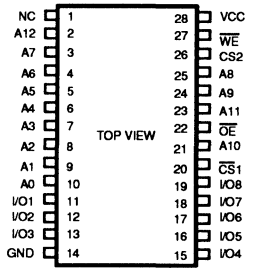
PLASTIC PACKAGE
FPT-28P-M02

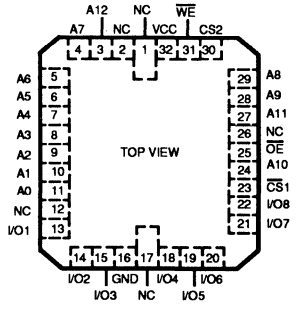


CERAMIC PACKAGE
LCC-32C-A02

- Organization: 8,192 words x 8 bits
- Access time: 100 ns max. (MB8464A-10-X/-10LL-X)
  150 ns max. (MB8465A-15-X/-15LL-X)
- Operating temperature: –40°C to +85°C
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V supply ±10% tolerance
- Low power consumption:
  1.1 mW max. (CMOS standby)
  27.5 mW max. (TTL standby)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
  DIP (600 mil) MB8464A-xx(LL)P-X
  Skinny DIP (300 mil) MB8464A-xx(LL)PSK-X
  SOP (300 mil) MB8464A-xx(LL)PF-X
- Standard 32-pad Ceramic Package:
  LCC (metal seal) MB8464A-xx(LL)CV-X

PIN ASSIGNMENT





Absolute Maximum Ratings (See Note)

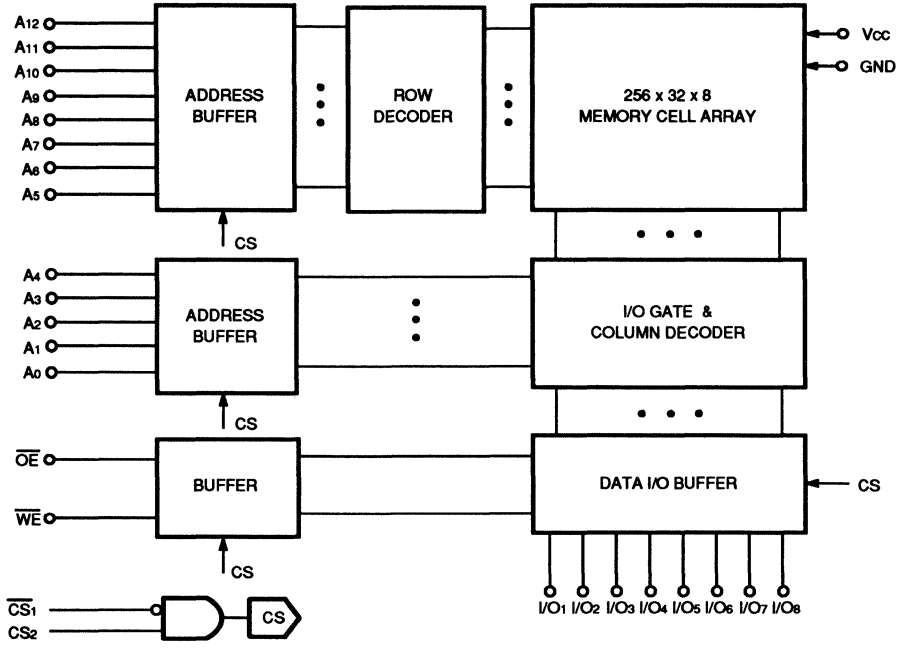
Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +7.0	V
Input Voltage		V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage		$V_{I/O}$	–0.5 to V_{CC} +0.5	V
Temperature Under Bias		T_{BIAS}	–50 to +95	°C
Storage Temperature Range	Ceramic	T_{STG}	–65 to +150	°C
	Plastic		–40 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 – MB8464A-X BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

5

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

RECOMMENDED OPERATING CONDITION (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	–40		85	°C

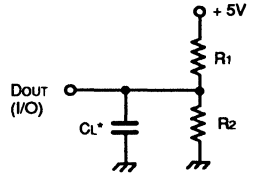
DC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB8464A-10-X/10LL-X MB8464A-15-X/15LL-X		Unit	Test Condition
		Min	Max		
Standby Supply Current	I_{SB1}		0.2	mA	$CS2 \le 0.2V$ or $\overline{CS1} \ge V_{CC}-0.2V$ (with $CS2 \le 0.2V$ or $CS2 \ge V_{CC}-0.2V$)
	I_{SB2}		5.0	mA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$
Active Supply Current	I_{CC1}		60	mA	$V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0mA $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$
Operating Supply Current	I_{CC2}		70	mA	Cycle = Min. Duty = 100%, I_{OUT} = 0mA
Input Leakage Current	I_{LI}	–10	10	µA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	I_{LVO}	–50	50	µA	$\overline{V_{IO}} = 0V$ to V_{CC} $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Input High Voltage	V_{IH}	2.4	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	–0.3 *	0.6	V	
Output High Voltage	V_{OH}	2.4		V	$I_{OH} = -1.0mA$
Output Low Voltage	V_{OL}		0.4	V	$I_{OL} = 2.1mA$

Note: All voltages are referenced to GND.
* : –3.0V min. for pulse width less than 20 ns. (V_{IL} min. = –0.3V at DC level.)

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.6V and 2.4V)
- Timing Reference Levels Input: V_{IL} = 0.6V, V_{IH} = 2.4V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V
- Output Load

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

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AC CHARACTERISTICS

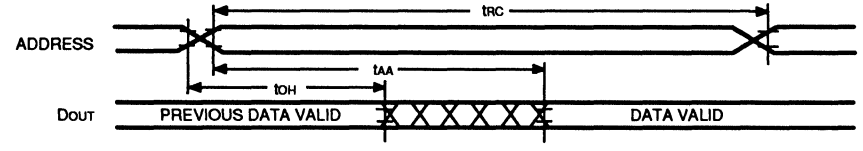
(Recommended operating conditions otherwise noted.)

READ CYCLE *1

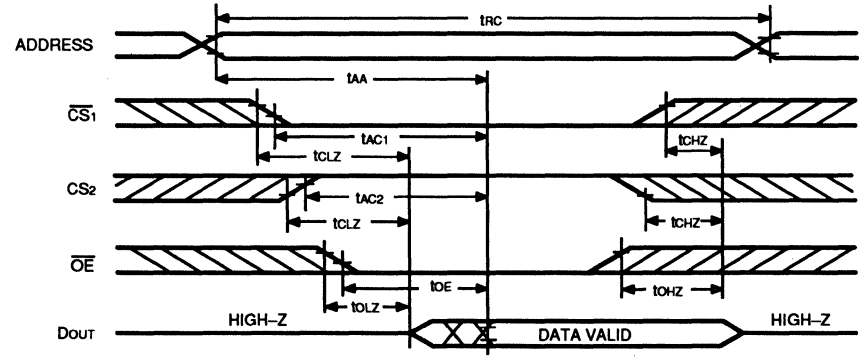
Parameter	Symbol	MB8464A-10-X/10LL-X		MB8464A-15-X/15LL-X		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	100		150		ns
Address Access Time	t_{AA}		100		150	ns
$\overline{CS1}$ Access Time	t_{AC1}		100		150	ns
CS2 Access Time	t_{AC2}		100		150	ns
Output Enable to Output Valid	t_{OE}		45		60	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z *4	t_{CLZ}	10		10		ns
Output Enable to Output Low-Z *4	t_{OLZ}	5		5		ns
Chip Select to Output High-Z *4	t_{CHZ}		40		50	ns
Output Enable to Output High-Z *4	t_{OHZ}		40		50	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2 : $\overline{CS1}$, CS2 CONTROLLED *3



Note: *1 $\overline{WE}$ is high for Read cycle.

*2 Device is continuously selected, $\overline{CS_1}$ = $\overline{OE}$ = V_{IL}, CS_2 = V_{IH}.

*3 Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.

*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

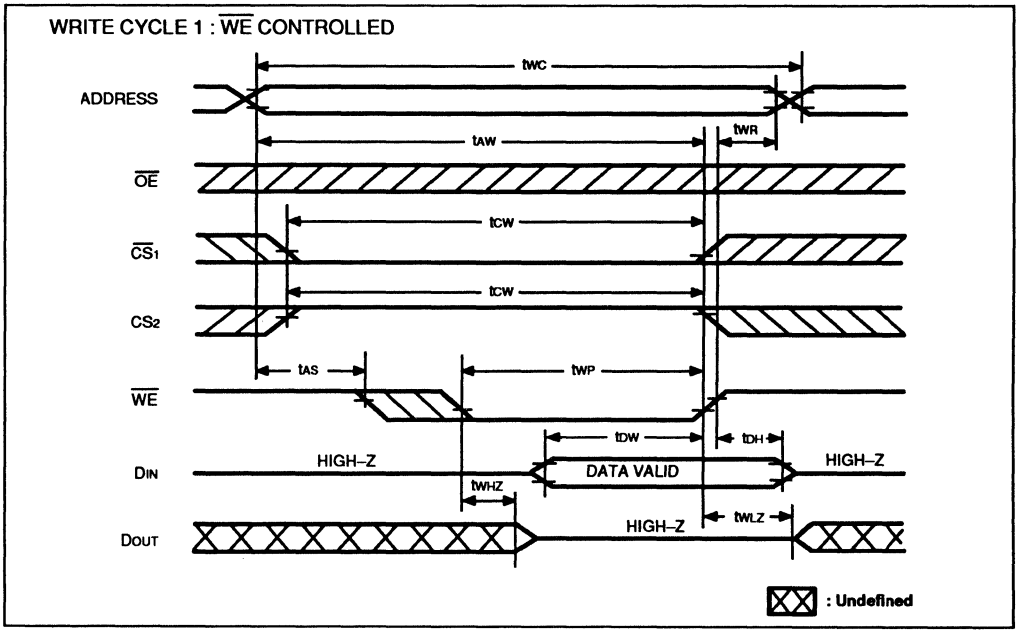
AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	MB8464A-10-X/10LL-X		MB8464A-15-X/15LL-X		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	tWC	100		150		ns
Address Valid to End of Write	tAW	80		100		ns
Chip Select to End of Write	tCW	80		100		ns
Data Valid to End of Write	tDW	40		50		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	60		90		ns
Address Setup Time	tAS	0		0		ns
Write Recovery Time *4	tWR	5		5		ns
Write Enable to Output Low-Z *5	tWLZ	5		5		ns
Write Enable to Output High-Z *5	tWHZ		40		50	ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: 1* If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

2* If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

3* All write cycle are determined from last address transition to the first address transition of the next address.

4* tWR is defined from the end point of WRITE Mode.

5* Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

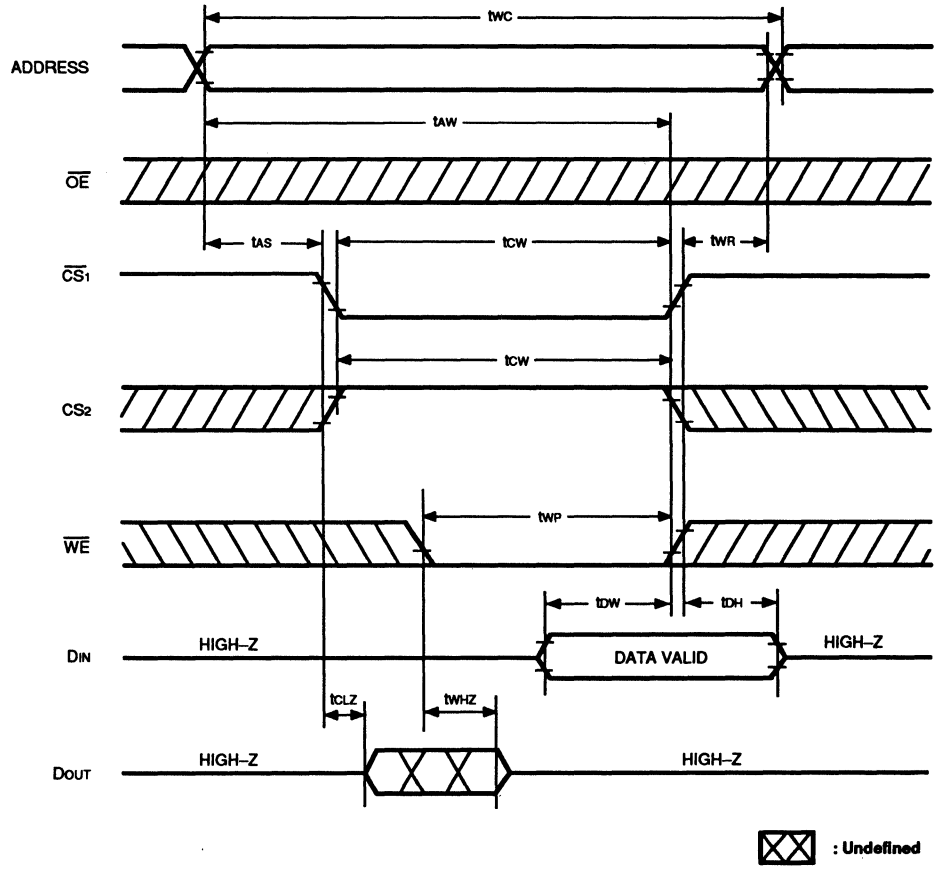
5

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE 2 : $\overline{CS_1}$ CONTROLLED *1



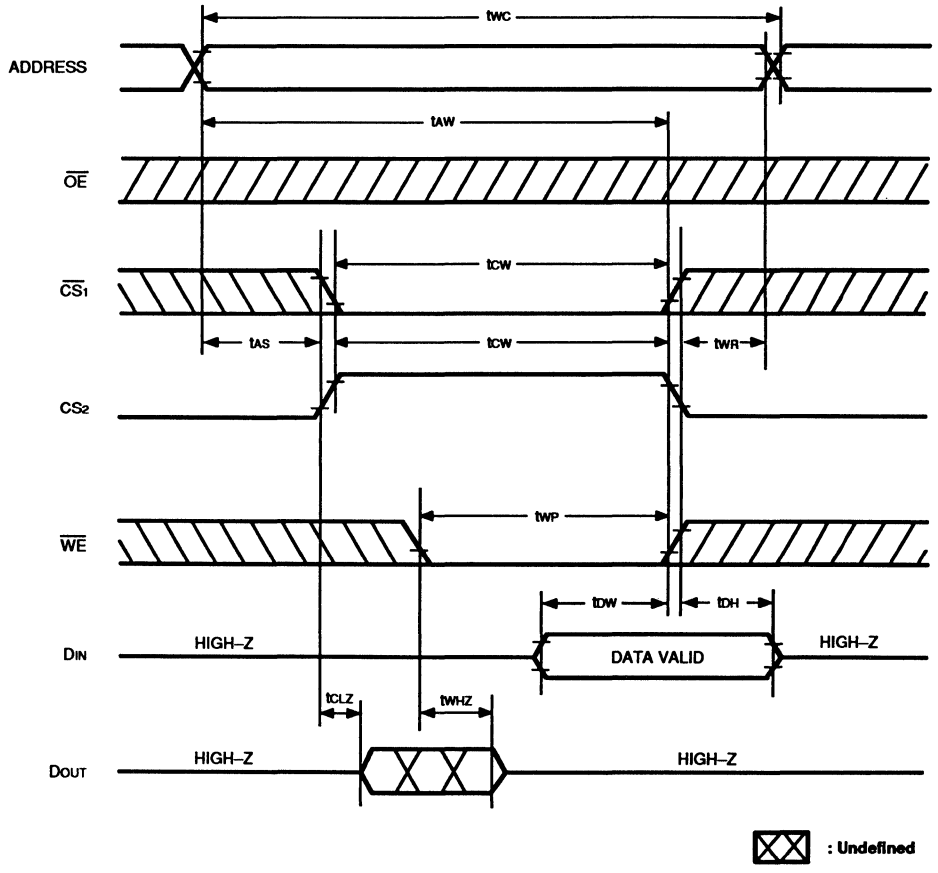
Note: *1 If $\overline{OE}$, CS_2 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

AC CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

WRITE CYCLE TIMING DIAGRAM

WRITE CYCLE 3 : $\overline{CS_2}$ CONTROLLED *1



Note: *1 If $\overline{OE}$, CS_1 and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			50	µA
	LL-Version *2				50	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $V_{CC} = V_{DR} = 3.0V$

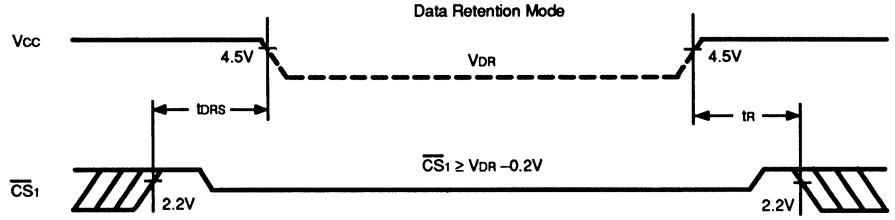
$\overline{CS_1} \geq V_{DR} - 0.2V$, $CS_2 \geq V_{DR} - 0.2V$ or $CS_2 \leq 0.2V$ (at $\overline{CS_1}$ CONTROLLED)

$CS_2 \leq 0.2V$ (at CS_2 CONTROLLED)

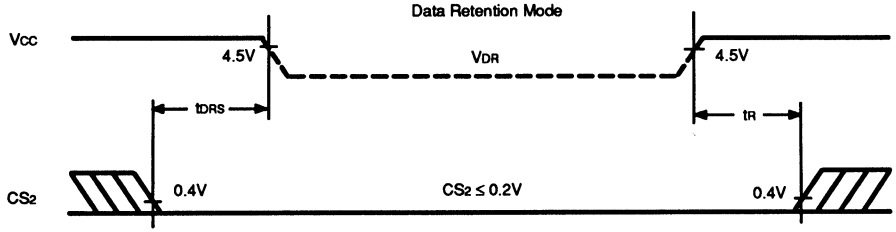
*2 I_{DR} max. = 2.0µA at $V_{DR} = 3.0V$, $T_A = -40°C$ to $+40°C$.

DATA RETENTION TIMING

$\overline{CS_1}$ CONTROLLED



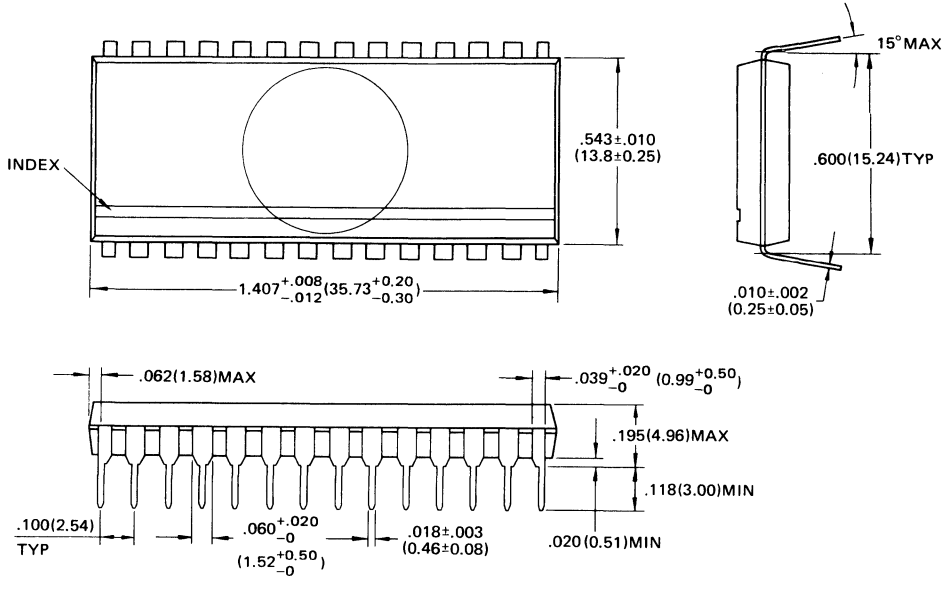
CS_2 CONTROLLED



PACKAGE DIMENSIONS

(SuffiX: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)



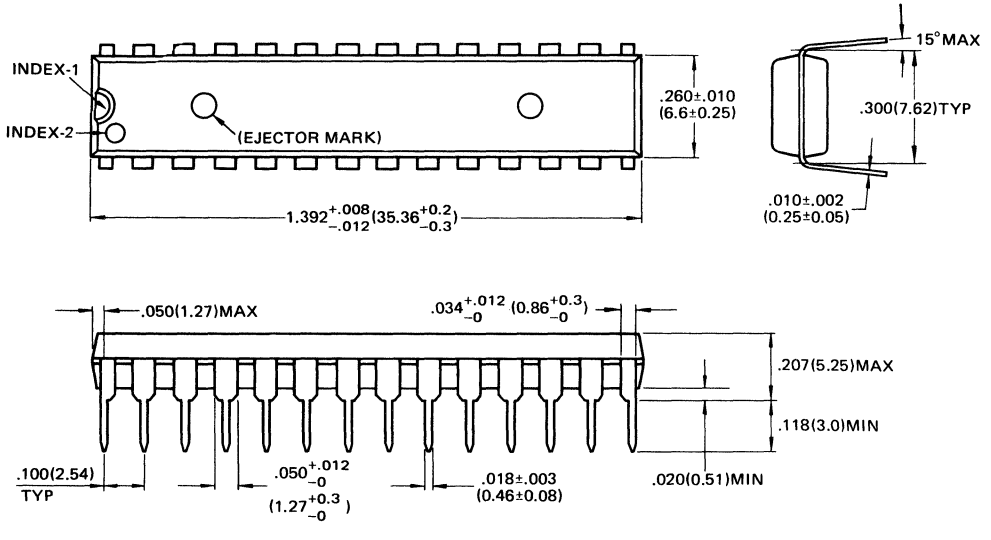
Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (Continued)

(SuffiX: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M04)



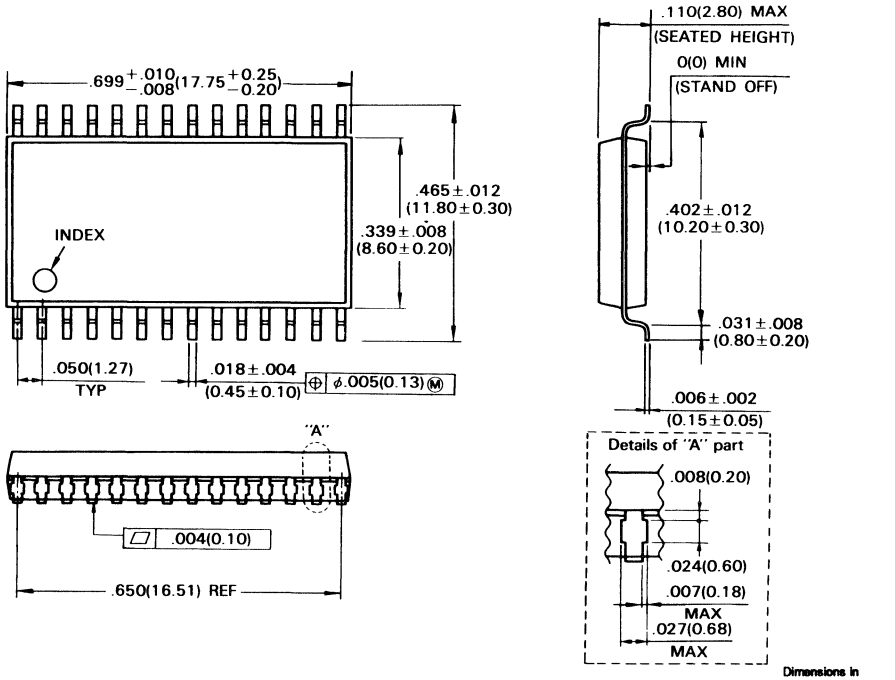
Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (Continued)

(SuffIX: PF)

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



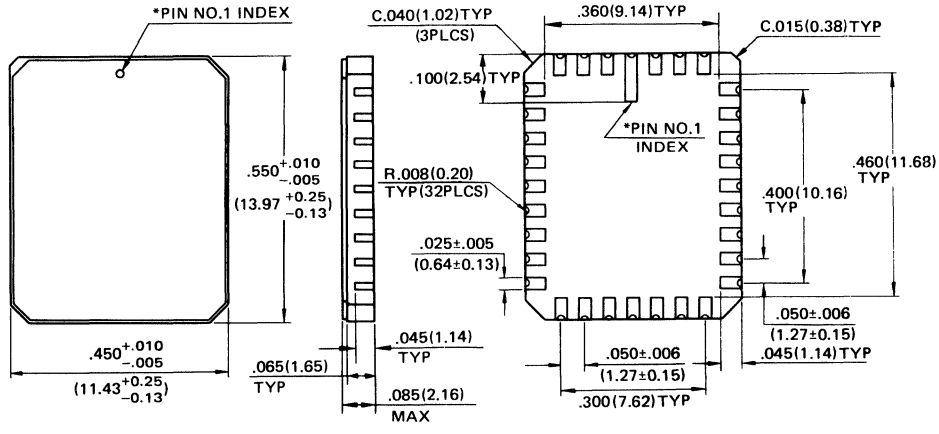
Dimensions in inches (millimeters)

5

PACKAGE DIMENSIONS (Continued)

(SuffiX: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

5

October 1990
Edition 1.0

FUJITSU

DATA SHEET

MB84256A-70-X/-70LL-X/-10-X/-10LL-X
CMOS 256K-BIT LOW-POWER SRAM

32K Words x 8 Bits CMOS Static RAM for Extended Temperature Operation

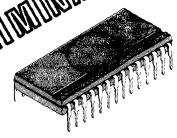
The Fujitsu MB84256A-X is a 32,768 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB84256A-X has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 8 bits
- Access time: 70 ns max. (MB84256A-70/-70LL-X)
  100 ns max. (MB84256A-10/-10LL-X)
- Operating temperature: –40°C to +85°C
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Single +5 V power supply ±10% tolerance
- Low power consumption:
  1.1 mW max. (CMOS standby)
  16.5 mW max. (TTL standby)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:

DIP	(600 mil)	MB84256A-xx(LL)P-X
Skinny DIP	(300 mil)	MB84256A-xx(LL)PSK-X
SOP	(450 mil)	MB84256A-xx(LL)PF-X
TSOP (Normal bend)		MB84256A-xx(LL)PFTN-X
TSOP (Reverse bend)		MB84256A-xx(LL)PFTR-X

PRELIMINARY

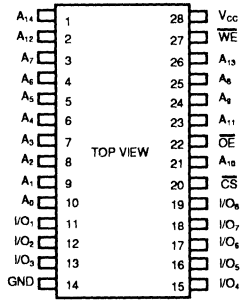


PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04

PLASTIC PACKAGE
FPT-28P-M02

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

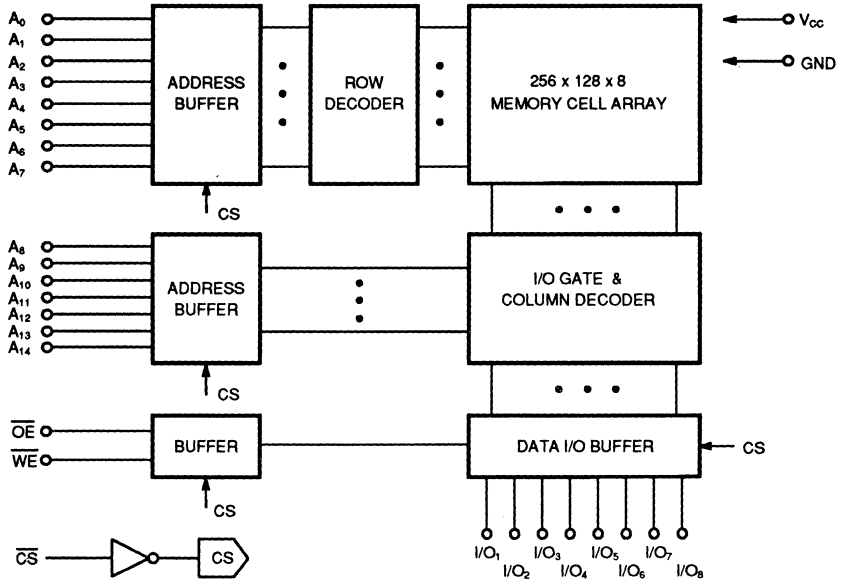
Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	–0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	–40 to +85	°C
Storage Temperature Range	T_{STG}	–40 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

Fig. 1 – MB84256A BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High–Z
L	H	H	D_{OUT} Disable	I_{CC}	High–Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

CAPACITANCE

(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	−40		+85	°C

DC CHARACTERISTICS

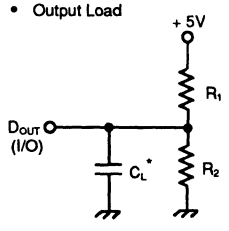
(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Condition	MB84256A-70/70LL/10/10LL-X		Unit
				Min	Max	
Standby Supply Current		I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$		0.2	mA
		I_{SB2}	$\overline{CS} = V_{IH}$		3	mA
Active Supply Current		I_{CC1}	$V_{IN} = V_{IH}$ or V_{IL} $\overline{CS} = V_{IL}$, I_{OUT} = 0mA		70	mA
Operating Supply Current	70ns	I_{CC2}	Cycle = Min. Duty = 100% I_{OUT} = 0mA		90	mA
	100ns				80	
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	−1	1	µA
Output Leakage Current		$I_{LI/O}$	$V_{I/O}$ = 0V to V_{CC} $\overline{CS} = V_{IH}$ $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	−1	1	µA
Input High Voltage		V_{IH}		2.4	V_{CC} +0.3	V
Input Low Voltage		V_{IL}		−0.3 *	0.6	V
Output High Voltage		V_{OH}	I_{OH} = −1.0mA	2.4		V
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA		0.4	V

Note: All voltages are referenced to GND.
*: −3.0V min. for pulse width less than 20 ns.

Fig. 2 – AC TEST CONDITIONS

- Output Load



- Input Pulse Levels: 0.4 to 2.6V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL}=0.6V, V_{IH}=2.4V
  Output: V_{OL}=0.8V, V_{OH}=2.0V

* Including Jig and stray capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}
Load II	1.8KΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ}, and t_{WHZ}

5

AC CHARACTERISTICS

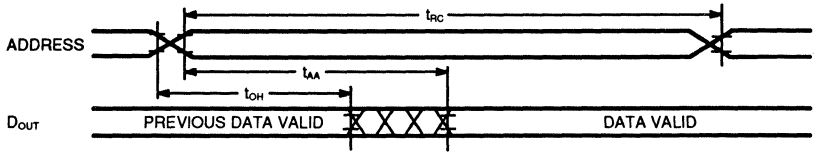
(Recommended operating conditions otherwise noted.)

READ CYCLE *1

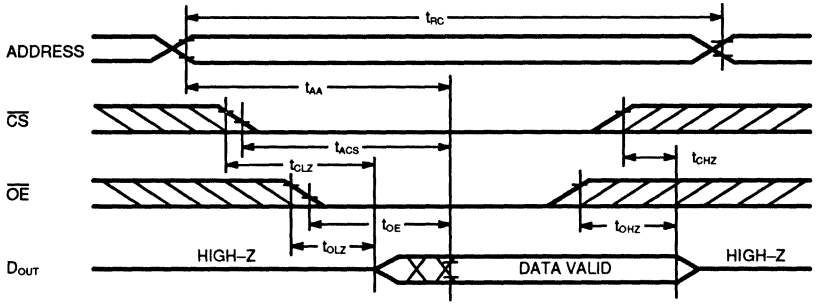
Parameter	Symbol	MB84256A-70/70LL-X		MB84256A-10/10LL-X		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time *2	t_{AA}		70		100	ns
$\overline{CS}$ Access Time *3	t_{ACS}		70		100	ns
Output Enable to Output Valid	t_{OE}		35		40	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low–Z *4	t_{CLZ}	10		10		ns
Output Enable to Output Low–Z *4	t_{OLZ}	5		5		ns
Chip Select to Output High–Z *4	t_{CHZ}		25		40	ns
Output Enable to Output High–Z *4	t_{OHZ}		25		40	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED*2



READ CYCLE 2: $\overline{CS}$ CONTROLLED*3



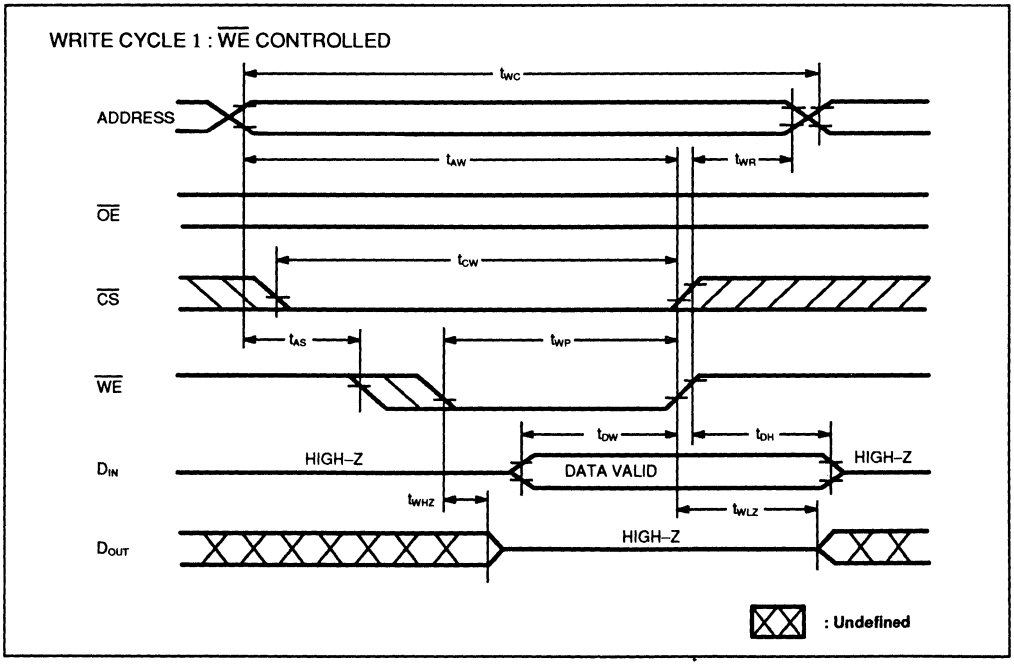
: Undefined

Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{CS}$ = $\overline{OE}$ = V_{IL}.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE *1*2

Parameter	Symbol	MB84256A-70/70LL-X		MB84256A-10/10LL-X		Unit
		Min	Max	Min	Max	
Write Cycle Time *3	t_{WC}	70		100		ns
Address Valid to End of Write	t_{AW}	50		80		ns
Chip Select to End of Write	t_{CW}	50		80		ns
Data Valid to End of Write	t_{DW}	25		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Pulse Width	t_{WP}	50		60		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time *4	t_{WR}	5		5		ns
$\overline{WE}$ to Output Low-Z *5	t_{WLZ}	5		5		ns
$\overline{WE}$ to Output High-Z *5	t_{WHZ}		25		40	ns

WRITE CYCLE TIMING DIAGRAM *1 *2

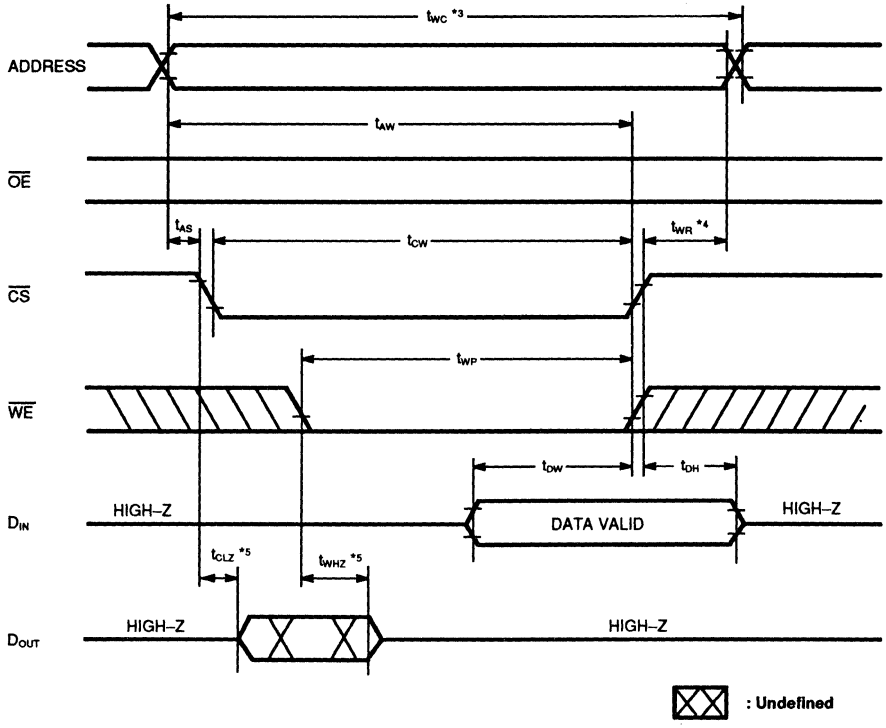


Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All write cycles are determined from last address transition to the first address transition of the next address.
*4 t_{WR} is defined from the end point of WRITE Mode..
*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load I in Fig. 2.

5

WRITE CYCLE TIMING DIAGRAM *1 *2

WRITE CYCLE 2 : $\overline{CS}$ CONTROLLED



Note: *1 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 All write cycles are determined from last address transition to the first address transition of the next address.

*4 t_{WR} is defined from the end point of WRITE Mode..

*5 Transition is measured at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

5

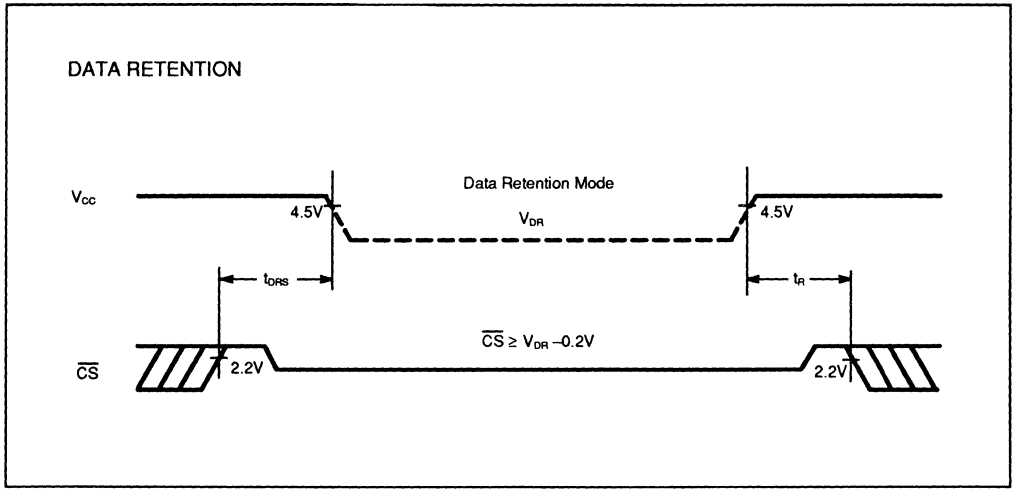
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1		V_{DR}	2.0		5.5	V
Data Retention Supply Current *2	Standard	I_{DR}		0.001	0.05	mA
	LL-Version *3			1	5.0	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 $\overline{CS} \geq V_{DR} - 0.2V$
*2 $V_{DR} = 3.0V$, $\overline{CS} \geq V_{DR} - 0.2V$
*3 $V_{DR} = 3.0V$, $T_A = 40°C$

DATA RETENTION TIMING

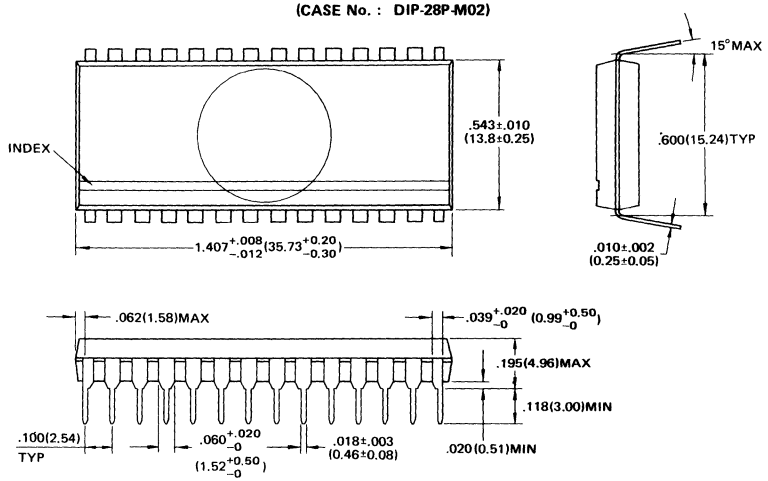


5

PACKAGE DIMENSIONS

(Suffix: P)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)

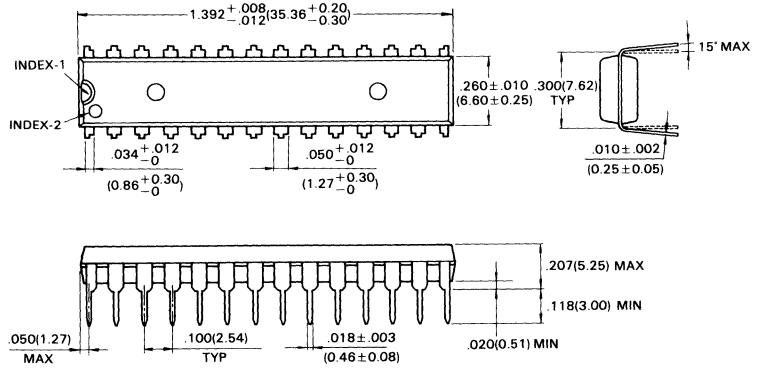


Dimensions in
inches (millimeters)

5

(Suffix: P-SK)

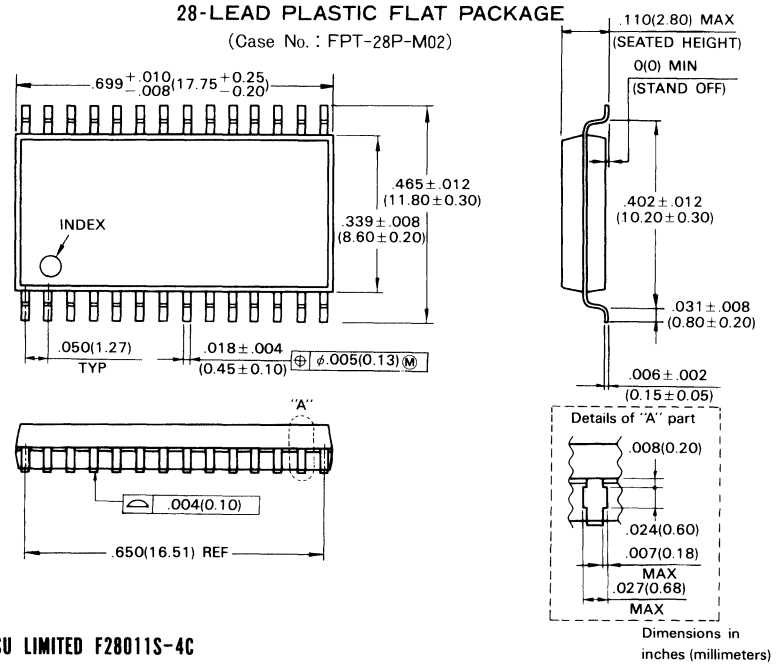
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)



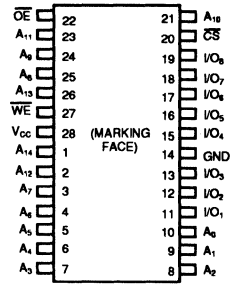
5

PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)

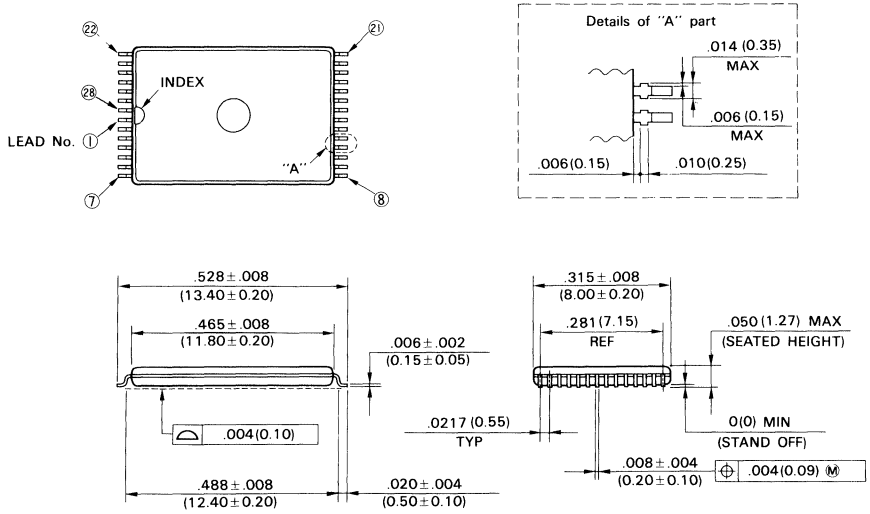
FPT-28P-M03

PIN ASSIGNMENT
(NORMAL BEND)



28-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-28P-M03)

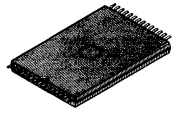


Dimensions in
inches (millimeters)

5

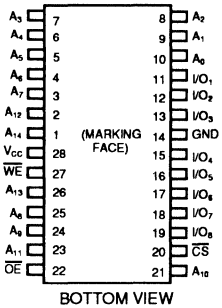
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



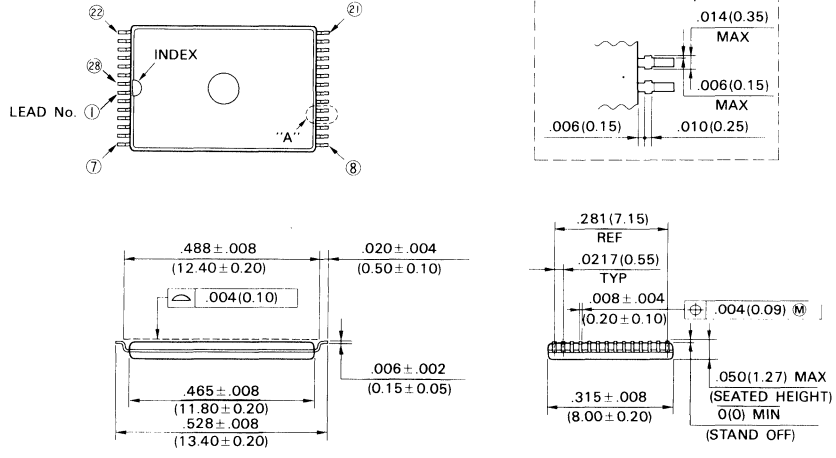
FPT-28P-M04

PIN ASSIGNMENT
(REVERSE BEND)



BOTTOM VIEW

28-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-28P-M04)



Dimensions in
inches (millimeters)

5

Section 6

Quality and Reliability — *At a Glance*

Quality Control at Fujitsu

Built-In Quality and Reliability

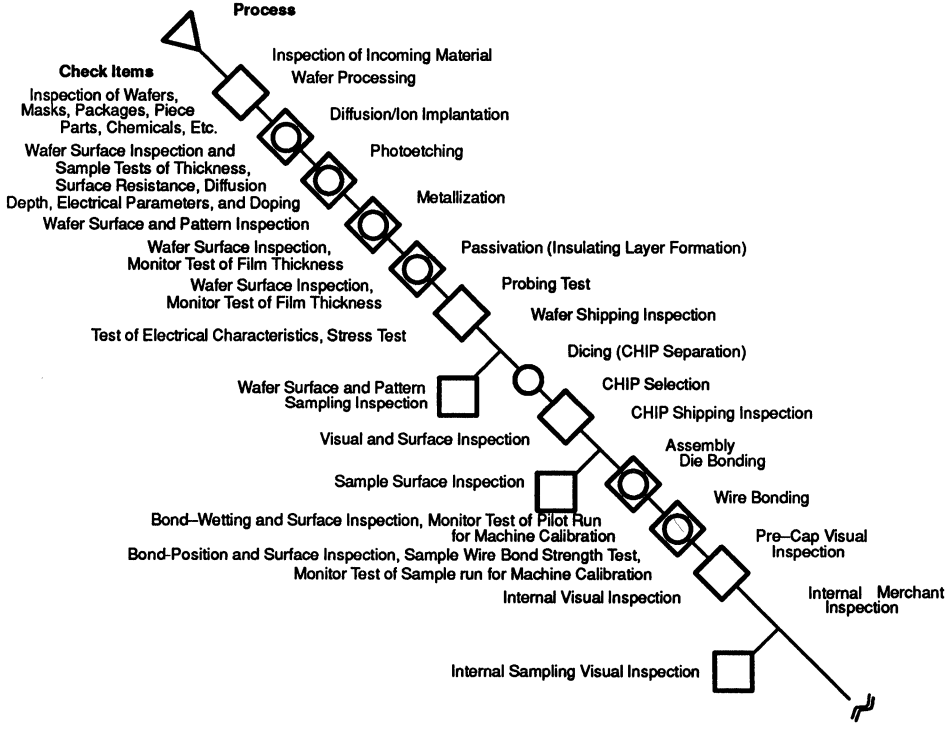
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

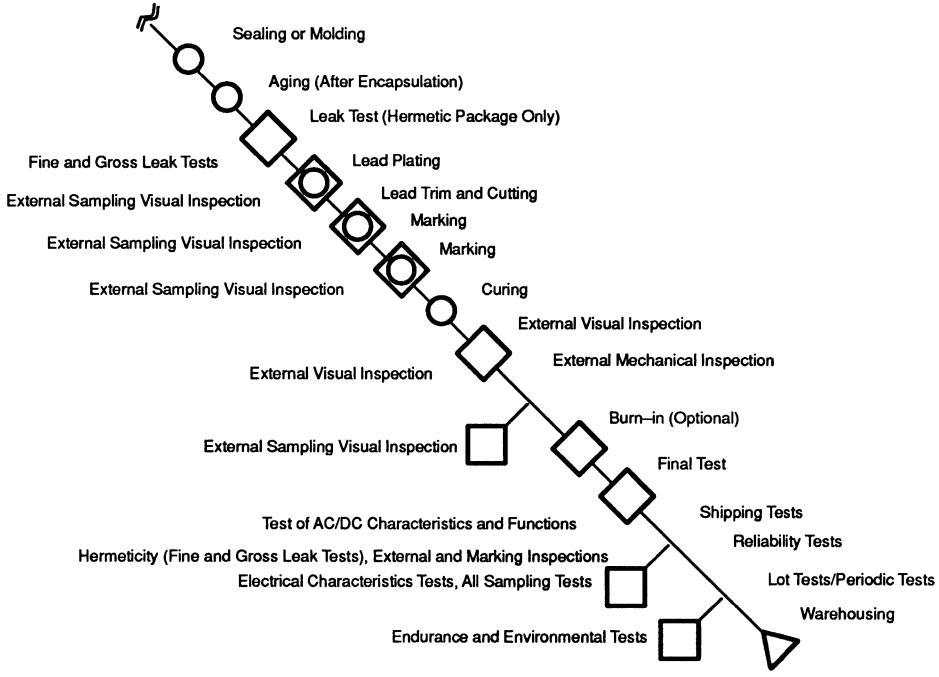
Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



Continued on next page

Quality Control Processes at Fujitsu (Continued)



Legend:

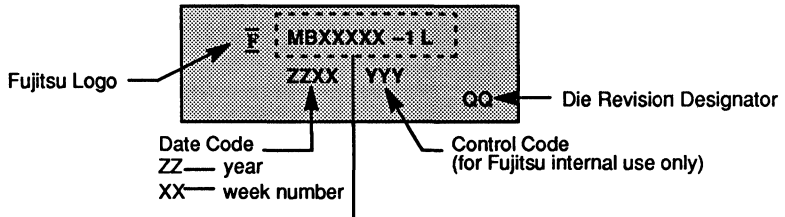
- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

Section 7

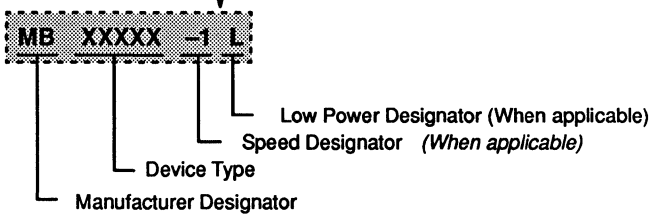
Ordering and Package Information — *At a Glance*

SRAM IC Package Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

Part Number



MB Identifies an IC designed and manufactured by Fujitsu with a Fujitsu-designated device number.

MBM Identifies an IC designed and manufactured by Fujitsu with a device number, designated by the industry, that is the industry standard number.

Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

7

IC Package Marking and Ordering Information

This ordering information is presented as a guide to Fujitsu's package options. The codes shown here indicate the current selections available for IC packaging. Since device packages are subject to changes and updates, you should contact your closest Fujitsu Sales Office or Representative for the latest package information.

Plastic Packages		
Description	**Type**	**Fujitsu Ordering Code[1,2]**
Dual In-line Package, 600 mil Wide	DIP	P or M[3]
Dual In-line Package, 300 mil Wide	Skinny DIP	P-SK or P
Dual In-line Package, 400 mil Wide	Slim DIP	P-SL or P
Dual In-line Package, 70 mil Lead Pitch	Shrink DIP	P-SH or P
Flatpack, 0.5 mm Lead Pitch	SSOP or SQFP	PFV
Leaded Chip Carrier	PLCC	PD or PV
Pin Grid Array Package	PGA	PR
Quad Flatpack	QFP	PFQ or PF
Single In-line Package	SIP	PS
Small Outline J-Leads	SOJ	PJ or PJN
Small Outline Package	SOP	PF or PNF
Thin Small Outline (with Normal Bend Leads) Package	TSOP	PFTN
Thin Small Outline (with Reverse Bend Leads) Package	TSOP	PFTR
Zig-zag In-line Package	ZIP	PSZ

[1]Package ordering code appears as a suffix to Fujitsu's part number and speed designator (MBXXXXX–XXPKG).
[2]Package codes in the U.S.A do not use the "–"; e.g., PSK is the same as P–SK.
[3]M is used on bipolar devices only.

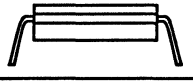
Continued on next page

IC Package Marking and Ordering Information (Continued)

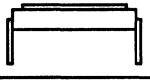
Ceramic Packages		
Description	**Type**	**Fujitsu Ordering Code[1,2]**
Dual In-line Package with CERDIP[3]	CERDIP	Z
Dual In-line Package with Frit Glass Seal	DIP	T
Dual In-line Package with Metal Seal (Side Brazed[4])	DIP	C
Dual In-line Package, 400 mil Wide	Slim DIP	Z-SL or Z T-SL or T C-SL or C
Dual In-line Package, 300 mil Wide	Skinny DIP	Z-SK or Z T-SK or T C-SK or C
Dual In-line Package, 1.778 mm Lead Pitch	Shrink DIP	Z-SH or Z T-SH or T C-SH or C
Flat Package with CERPACK	CERPACK	ZF
Flat Package with Frit Glass Seal	FPT	TF
Flat Package with Metal Seal	FPT	CF
Leadless Chip Carrier with Frit Glass Seal	LCC	TV
Leadless Chip Carrier with Metal Seal	LCC	CV
Pin Grid Array	PGA	CR
Quad Flat J-lead Package with CERPACK	QFJ	ZJ
Quad Flat, Gullwing Lead, Package with CERPACK	QFP	ZFL or ZF
Quad Flat, Gullwing Lead, Package with Metal Seal	QFP	CFL or CF
Small Outline, Gullwing Lead, Package with CERPACK	SOP	ZFL or ZF
Small Outline, Gullwing Lead, Package with Metal Seal	SOP	CFL or CF
Small Outline J-lead Package with Metal Seal	SOJ	CJ

[1]Package ordering code appears as a suffix to Fujitsu's part number and speed designator (MBXXXXX–XXPKG)
[2]Package codes in the U.S.A do not use the "–"; e.g., ZSK is the same as Z–SK.

3 CERDIP



4 Side Brazed



7

Section 8

Sales Information — *At a Glance*

8

Introduction to Fujitsu

Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

This leadership has resulted, at least in part, from the superb quality of the company's semiconductors and electronic components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one of the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie, and manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the U.S, Europe, and Asia also help to meet the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of a wide variety of customers. Backed by Fujitsu's extensive R&D commitment equal to over 10 percent of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

Continued on next page

Introduction to Fujitsu

Fujitsu Microelectronics, Inc. (U.S.A.)

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers throughout North and South America.

The Advanced Products Division (APD) is responsible for designing and selling a full line of SPARC processors, peripheral chips, and the EtherStar™ LAN controller that it designed. The EtherStar LAN controller is the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of a cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD) which markets the following standard devices, components, and ASICs.

Memory Products	DRAMs EPROMs EEPROMs NOVRAMs CMOS masked ROMs CMOS SRAMs BiCMOS SRAMs Bipolar PROMs ECL RAMs STRAMs (self-timed RAM) Hi-Rel PROMs and SRAMs Memory cards Memory modules
Telecommunication Products	PLLs Prescalers Piezoelectric devices CODECs VCOs Telephone ICs Modems

Continued on next page

Introduction to Fujitsu

Microprocessor Products	4-bit microcontrollers DSPs
Logic Products	Standard and ultra high-speed ECL Translator circuits Interface devices
Analog Products	Linear ICs Transistors
Hybrid Products	Thick- and Thin-film Custom modules Stepper motor drivers
Special Purpose Controller Products	SCSI controllers Serial protocol controllers Video controllers (TV text, CRT, and picture-in-picture)
ASIC Products	CMOS gate arrays ECL gate arrays BiCMOS gate arrays GaAs gate arrays CMOS standard cells ASIC Gallery™ (SuperMacros™, Compiled Cells) ASICOpen™ CAD Software Framework (ViewCAD™, a design and verification tool that integrates with third-party CAD tools) Third-party EWS (engineering workstation) support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division (SMD) assembles and tests memory devices. The Gresham Manufacturing Division (GMD) began manufacturing in 1988. GMD fabricates wafers, and produces ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Component of America**, markets connectors, keyboards, thermal printers, plasma displays, and relays.

Continued on next page

Introduction to Fujitsu

Fujitsu Electronic Devices Europe:

Fujitsu Mikroelektronik GmbH (FMG), West Germany
Fujitsu Microelectronics Limited (FML), U.K.
Fujitsu Microelectronics Italia S.R.L (FMIL), Italy
Fujitsu Microelectronics Ireland, Ltd. (FME), Ireland

Fujitsu Mikroelektronik GmbH (FMG) was established in June 1980 in Frankfurt, West Germany, as Fujitsu's European headquarters and is a totally owned subsidiary of Fujitsu Limited, Tokyo. Fujitsu Microelectronics Limited (FML) is a sister company based in Maidenhead, England and dedicated to serving the U.K., Ireland, and Scandanavia. Fujitsu Microelectronics Italia (FMIL) is based in Milan, Italy and serves Italy, Spain, Portugal, and the rest of Southern Europe. Together, FMG, FML, and FMIL supply the European market with a full range of semiconductors and electronic components. Sales offices are located in Munich, Frankfurt, Stuttgart, Paris, Eindhoven, Milan, Maidenhead, and Stockholm.

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in Dublin, Ireland, as Fujitsu's European Assembly Center for integrated circuits. FME produces DRAMs, EPROMs, and other LSI memory products.

Fujitsu has two European VLSI design centers, both in the U.K. The Manchester Design Center, in operation since 1983, is equipped with two mainframe computers and is linked by satellite to production plants in Japan and the U.S. Staffed with a team of experienced engineers, the center is involved in the design of VLSI standard products, SuperMacros, CAD tools and ASICs. A second design center was set up in London in 1990 for designing telecommunication ICs. Additionally, Fujitsu offers a network of 17 ASIC design centers in eight European countries.

Fujitsu has further demonstrated its commitment to the European market by commencing construction of a full wafer fabrication plant in Durham in the North of England. The new plant is due to start production of 4 megabyte DRAMs and ASICs in 1991.

Continued on next page

Introduction to Fujitsu

The range of semiconductor products offered by FMG, FML, and FMIL for the European market includes:

Memory Products	DRAMs SRAMs EPROMs EEPROMs Mask ROMs Bipolar PROMs Video RAMs ECL RAMs Memory modules Memory cards
ASIC Products	CMOS gate arrays BiCMOS gate arrays Bipolar (ECL) gate arrays Gallium Arsenide gate arrays CMOS standard cells ECL gate masterslice devices Wide range of ASIC design software
Microprocessor Products	4-Bit Microcontrollers 4- 8- and 16-bit F^2MC flexible Microcontrollers 32-Bit SPARC™ RISC microprocessors 32-Bit GMICRO™ TRON-based CISC microprocessors
Telecommunication Products	Prescalers PLLs CODECs LAN devices DSPs SCSI and LAN devices ISDN products Telecom devices for the GSM Pan-European digital cellular telephone system.
Analog Products	OP Amps Comparators A/D and D/A Converters Application Specific ICs

The range of electronic components offered by FMG, FML, and FMIL incudes relays, connectors, keyboards, thermal printers, plasma displays, liquid crystal displays, hybrid ICs, and piezoelectric devices.

Continued on next page

Introduction to Fujitsu

Fujitsu Microelectronics Asia PTE Ltd. (Singapore)

Fujitsu Microelectronics Asia PTE Ltd. (FMAP) opened in August 1986, in Hong Kong, as a wholly-owned Fujitsu subsidiary for sales of electronic devices to the Asian, Australian, and Southwest Pacific markets. In 1990, FMAP moved to a new location in Singapore.

FMAP offers memory, ASIC, microprocessor, and telecommunication products along with Fujitsu's wide range of electronic components.

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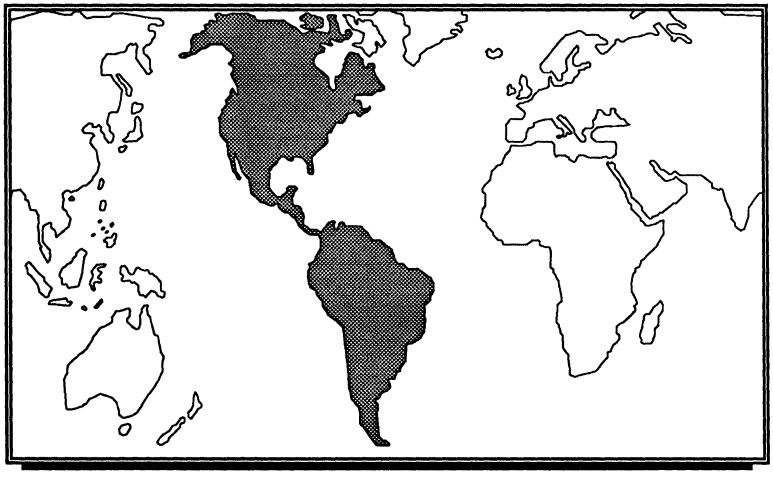

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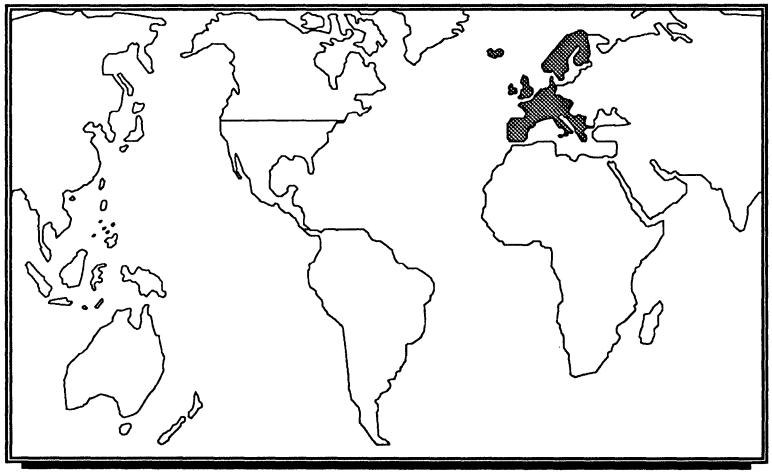

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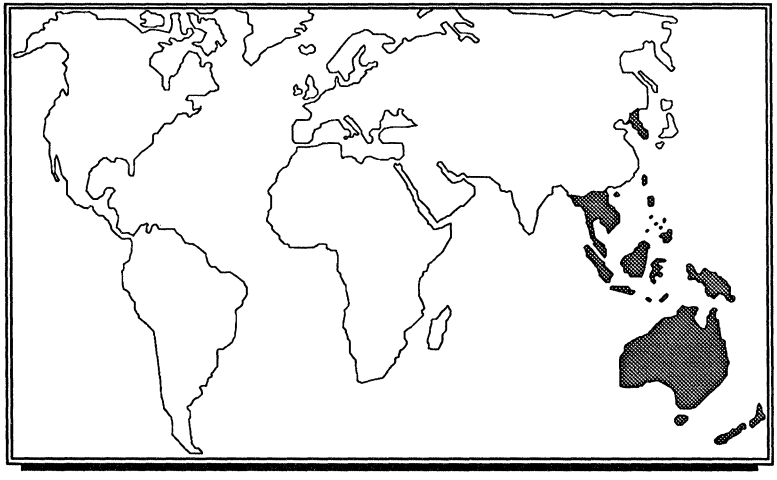

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Section 9

Design Information — *At a Glance*

Appendix 1

Self-Timed RAMs

Internally timed RAMs build fast writable control stores

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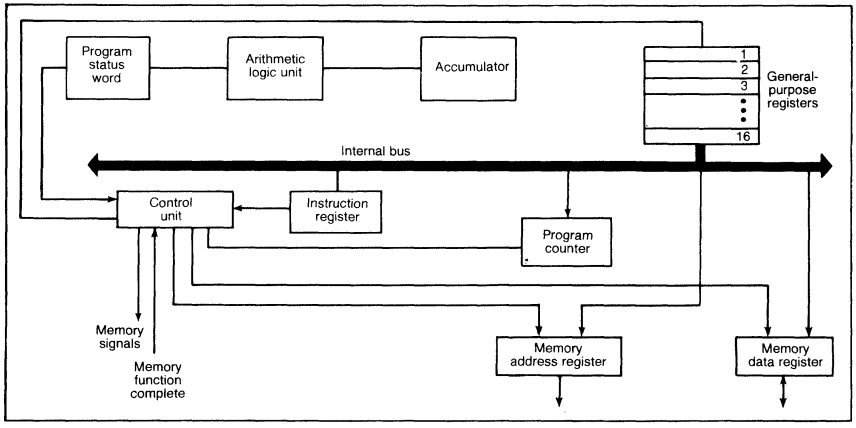
Create faster computers without sacrificing board space. Self-timed RAMs do the trick, replacing standard ECL RAMs in control memories.

The increasing speed of mainframes and minicomputers produces a need for memory access even faster than that supplied by ECL RAMs. One way to cut into 15-ns memory-access times is through process improvements, but this avenue quickly reaches its limits. Another method is to rework the architecture of the writable control store, which holds the microinstructions that implement the machine's assembly-language instructions. For instance, adding registers in the address and data lines to the control memory causes a pipeline effect that speeds up both read and write operations.

But the number of registers needed to process the size of control words in some of today's minicomputers can be prohibitive. The solution lies in the new self-timed RAMs (STRAMs)—pipelined memory devices containing on-board registers or latches, as well as a write-pulse generator. STRAMs not only shrink access times to 7 ns, but they also cut board space and reduce the number of lengthy connections between discrete parts. The latter is important because at ECL speeds these leads act as transmission lines, generating reflections and crosstalk.

To better understand how a STRAM can help a designer perform a specific task, consider a minicomputer's basic architecture. Both mainframes and minicomputers use microprogrammed processors in their CPUs. A microprogram is a flexible way to generate the control signals that implement assembly language. These control sequences or microinstructions reside in a control memory, usually a set of PROMs addressed by a microprogram counter.

In a microprogrammable machine, however, the control memory consists of fast RAMs, so a user can alter the control signals and modify the instructions. For example, a typical minicomputer CPU

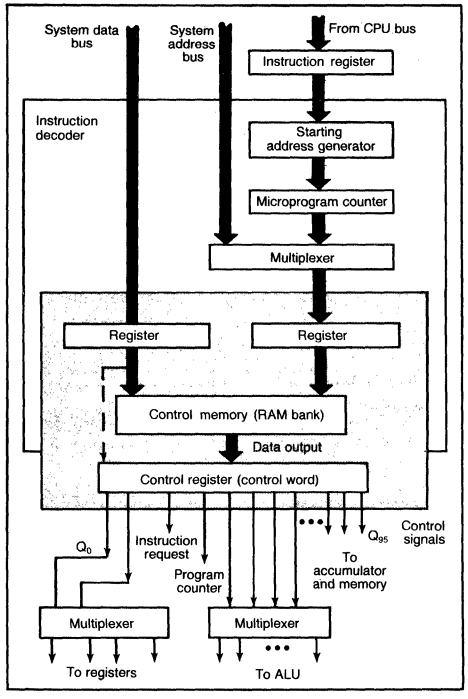


1. In a typical microprogrammed CPU, a control unit holds a control word employed for register loading, identification, and reading.

contains 12 kbytes of microprogrammable memory in its writable control store to diagnose problems, perform certain instructions, and change the microcode. For the sophisticated user, the CPU has an extra 12 kbytes of writable control store. This architecture lets a user change the way the computer responds to machine-language instructions.

A microprogrammable CPU usually contains general-purpose registers, an instruction register, a memory data register, a memory address register, a program counter, a 16-function arithmetic logic unit, a temporary register called an accumulator, and a control unit *(Fig. 1)*. The memory data register holds the data word to be sent to the memory, and the memory address register holds the address to the memory. The control unit sends a control word for register identification, loading, and reading. It generates signals like memory read and write, accumulator read and load, and ALU operations. The accumulator holds the ALU inputs and outputs.

The writable control store is implemented within the control unit *(Fig. 2)*. Its task is to generate the correct sequence of steps to execute the assembly-language instruction. Included in the controller are a starting address generator, microprogram counter, control memory, and control register. The control memory, addressed by the microprogram counter, stores the microinstructions. The control register holds the control word.



2. Adding registers to a writable control store's data and address paths speeds up the computer but at a steep price in board space. An alternative is to replace the components in the highlighted area with a self-timed RAM, which contains a write-pulse generator and registers.

The process begins when the CPU fetches a machine-language instruction from the main memory and loads it into the instruction register. Microprogramming then takes over. The instruction register puts the instruction into the starting address generator, which decodes the address of the first microinstruction in the control memory and loads this address into the microprogram counter. Next, the contents of the control memory pointed to by the microprogram counter are fetched and loaded into the control-word register. The microprogram counter is then updated to point to the next microinstruction in the desired sequence.

Minicomputers have control words 10 to 100 bits long. Each bit placed into the control-word register controls a part of the computer, including the instruction register, program counter, accumulator, memory, and ALU control. Hence, each bit is connected to a specific destination. The various control signals open or close data paths to these destinations or instruct the locations to perform an operation. For example, to transfer data between two registers, a control signal must instruct the source register to place the data on the bus, and a second signal must tell the destination register to read the data on the bus.

If the control store is writable, there must be a multiplexer between the microprogram counter and the control memory, because the address can come from either the microprogram counter or the system address bus. The system address bus's only task is to write to the control memory.

This is where a register between the counter and control memory input is beneficial. While the microprogram counter is generating an address during a read cycle (when it increments), the previous address can be in the register pointing to the control memory. That's the desired pipeline effect.

The computer gains a similar advantage during write cycles—that is, when the instructions in the microprogram are being altered. In this case, the new data is carried over the system bus and written in the control memory. If the memory consists of standard ECL RAMs and no registers, the address-hold time requirement will slow down the process.

Adding a register again creates a pipeline effect because the address and the data are both placed in the register. The address remains valid on the register's outputs until a new clock edge arrives, bringing a new address from the microprogram counter. The data and the address inputs are placed in the register on the true ongoing

edge of the clock. The Write Enable signal is also placed in the register *(Fig. 3a)*.

The several nanoseconds saved on each read and write cycle can add up to a considerable speed increase during normal computer operation. As noted, using STRAMs gives the designer this speed boost without the space penalty exacted by discrete registers.

In the example noted, a totally pipelined architecture was desired, so the registered STRAMs were used. This configuration yields the highest bit rate at the system level because the succeeding cycle can begin while the output signal is slewing and propagating. The data isn't available at the outputs until the next clock edge.

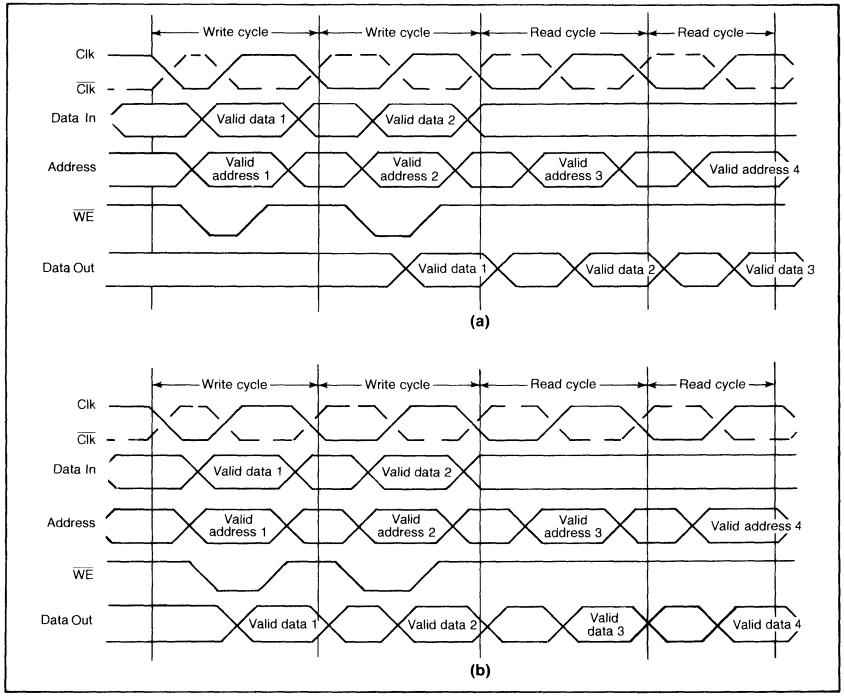
In some computers, however, the control store might have to read data from the RAM in one memory cycle. When this is the case, the control memory's inputs must have latches to hold the input data and address for saving the hold times. The output lines are also latched so that data can be placed on the data bus in one cycle. A latched STRAM fills the bill. This device's timing diagrams show that in read cycles the data is read in the same memory cycle *(Fig. 3b)*.

In a STRAM, the Address, Data In, Chip Enable, and Write Enable signals are latched into the on-chip registers or latches by the true-going edge or level of the clock pulse at the start of the memory cycle. All these signals remain valid throughout the memory cycle until the next true-going clock edge or level. As a result, signals need not be held stable during the entire cycle. They can slew down during one cycle to prepare for the next one.

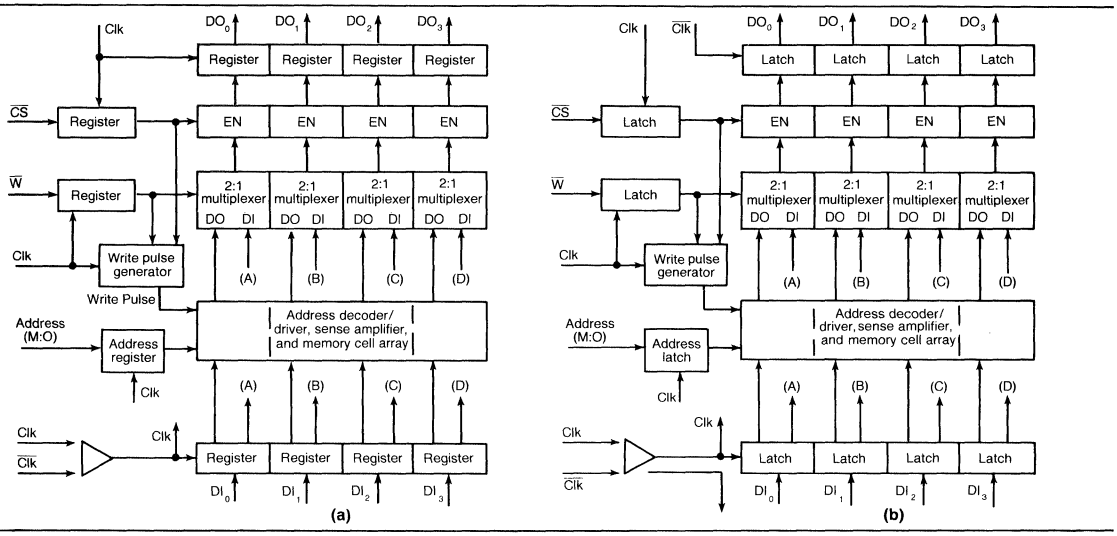
It's advantageous to trigger the write operation at the true going clock edge by latching the Address, Data, and Write Enable signals. Then the new Data and Address signals can be placed at the inputs while the old data is being written to the RAM cells. Also, this technique eliminates address skew because all the timing is clock-edge driven.

The basic difference between the registered and the latched STRAM, in fact, is that the former is clock-edge sensitive, while the latter is level sensitive *(Fig. 4)*. During a registered STRAM's read cycle, the data is available in the next clock cycle. For the latched STRAM, the data is available during the same memory cycle.

An advantage of both the latched and the register STRAM, however, is the built-in write-pulse generator, which eliminates an annoying problem associated with



3. Timing diagrams show that in a registered STRAM (a) the control word is read in the second clock cycle, while a latched STRAM (b) reads the data in the same clock cycle.



4. Both the registered (a) and latched versions (b) of the STRAM include a write-pulse generator. The devices have differential clock inputs—Clock and Clock—but single-ended operation is possible by connecting either clock line to an internal reference voltage.

fast ECL RAMs—the generation of a narrow write pulse. This on-board capability not only simplifies the designer's task, since creating very narrow pulses can be difficult, but it also speeds up the write cycle.

For instance, the length of a write cycle for a typical static RAM, MBM10474-15, employed without input and output latches is the sum of the minimum setup time, 2 ns; the write-pulse length, 12 ns; and the minimum hold time, 1 ns. That comes to 15 ns. For a latched STRAM with an internal write pulse generator, MBM10476LL-9, the write cycle time is the minimum setup time, 1 ns, plus the minimum high or low clock time, 6 ns—a total of 7 ns.

Another advantage of the STRAM is that the data written in the RAM is transparent to the outputs. This boosts the speed of the system for a cache write-through and improves the write-cycle timing for the writable control store. Also, the input data is transparent to the output in the same clock cycle for the latched STRAM and in the next cycle for the registered version. The transparent feature is helpful in diagnostic tasks and for writing back the data into the next location.

In both types of STRAMs the setup and hold times are identical for all inputs, simplifying the timing. The sum of the setup and hold times, also called the required valid window, is only 30% of the overall cycle time. For example, a 1k-by-4 latched STRAM, the MBM10476LL, has a clock cycle of 10 ns and a setup time plus hold time of 3 ns. This low ratio leaves enough time for the inputs to get ready for the next cycle.

The read and write cycles also have the same timing, because the data-input registers and latches are loaded at the start of each cycle, regardless of the type of cycle. This balanced read-write configuration is helpful for systems integration. When Write Enable is low at the beginning of a cycle, an internal write operation writes the data into memory and restores internal write lines to their original values.

The devices have differential clock inputs—Clock and $\overline{\text{Clock}}$—to increase timing accuracy. They can be connected in either the differential or single-ended mode. In the differential mode, data is latched at the cross point of the rising edge of Clock and at the falling edge of $\overline{\text{Clock}}$. Connecting either Clock or $\overline{\text{Clock}}$ to the internal reference voltage configures the STRAM in the single-ended mode, latching data at the true going edge of the clock. □

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Appendix 2

Static RAMs

November 1989
Edition 1.1

APPLICATION NOTE

FUJITSU

Static RAMs

Separate Data Inputs and Outputs SRAMs Provide New Architectural Solutions for System Designers

Applications Engineering Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

ABSTRACT

Traditionally, Static Random Access Memories (SRAMs) which can store greater than one-bit-wide words are available in packages with common data inputs and outputs. This is a consequence of the package size constraints for wider word widths. Fujitsu also offers byte wide and word-wide devices such as MB81C78A, MB81C79 and MB81C40. In the case of SRAMs with four-bit wide words or less, the increase in package size is not significant. Instead, the advantages of separate I/Os for system designers more than outweigh the slight increase in package size. The basic benefit of having separate data inputs and outputs is that it does not require the data bus direction to be changed during a read-modify write cycle. Thus, the need for multiplexing and demultiplexing in the data paths is eliminated. This application note deals with some specific usage areas which take advantage of the separate data input and output SRAMs.

A large variety of new applications, as well as some old memory designs have a need for separate data input and output pins on the SRAMs. Some of the key application areas are as follows: writeable microprogram control stores, cache memory systems, and deep FIFO data buffers for disks and LANs. The following discussion covers each of these application areas, highlighting the importance of the separate data input and output SRAMs.

Contents

Illustrations

Microprogramming and Writeable Control Store

Microprogramming has become one of the most powerful tools currently available to designers of high-speed, microprocessor-based systems. It provides a degree of flexibility previously unattainable in sophisticated processors and controllers.

Microprogramming is actually accomplished by execution of a machine language program that is made up of a sequence of microinstructions. This execution is performed at a microinstruction level by having each microinstruction interpreted on the host machine hardware through a microprogram[1].

Microprograms comprise a sequence of microinstructions that activate the control primitives of the host machine. Individual sequences contain all the elemental steps required to perform system function. The microprogram is kept in a high-speed, random access storage unit that is called a control store or control memory. Control storage is normally found implemented as a ROM. However, control storage may also exist as a dynamically alterable memory known as a writeable control store. A read only memory cannot be modified by an executing microprogram. The contents of the control ROM are unalterable and provide a fixed interpretation sequence for a given microinstruction set. On the other hand, the contents of the writeable control store can be modified by executing a microprogram. This allows the architecture of the host machine to be redefined under microprogram control since a different microprogram module may be loaded in the writeable control store under the control of the user program. A processor having this capability is called a flexible architecture machine.

A writeable control store memory provides the main application for the static RAM with separate data inputs and outputs. This will be evident from the arrangement of the control store as shown in Figure 1.

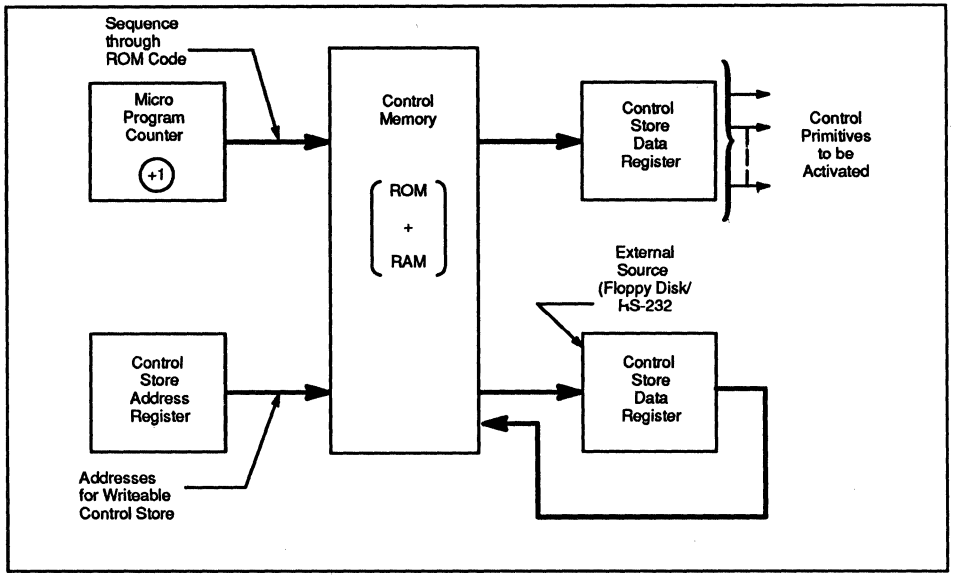

Figure 1. Arrangement of a Control Store Memory

The Main Parts of a Control Store

1. *Microprogram Counter*
   The microprogram counter contains the address of the next microinstruction which is loaded in the control store. Usually, it is incremented by one, and the program sequencing is done by adding one (1) to the current contents of the microprogram counter.

2. *Microprogram Instruction Register*
   The microinstruction register contains the current microinstruction being executed by the host machine. For a read only store, the microinstruction register would not provide leads for data to be written into the control memory — it would only receive data from the control store.

3. *Control Store Data Register*
   Since many microprogrammed machines use a combination of read only storage and writeable storage, another register must be provided to supply data to be written in the writeable control memory. This register can be called the control store data register.

4. *Control Store Address Register*
   Generally, the microcode which is loaded in the writeable control store is not written into the same location as that of the next instruction; therefore, a fourth register is needed. This register is called the control store address register. It points to the location in the writeable control store where the data word in the microcode is to be stored.

It is possible to combine the functions of the microprogram counter and the control address register as well as the functions of the microinstruction register and the control store data register. In general, these four registers will be kept separated, with the control store address register and

the control store data register forming a pair that references writeable control store and functions independently of the register pair formed by the microprogram counter and the microinstruction register. The microprogram counter and the microinstruction register, in turn, reference read-only control storage in terms of microprogram execution. Thus, a block of microcode could be loaded from a system peripheral, such as a floppy disk, into the writeable control store for usage by a specific microprogram. Similarly, data from either writeable control store or control ROM could be copied by control memory over into the main storage. The precise reasons for performing these operations would be dictated by the requirements of the user. In this application it is desirable to use an SRAM with separate data inputs and outputs to avoid the multiplexing and demultiplexing in the data paths.

Some systems use only writeable control store as control memory. In this case, the sequencer needs the addresses for read cycles of the RAM, while the microprocessor sends the addresses for the write cycle of the RAM. Typically the outputs of the writeable control store are to be configured in a very wide microword, anywhere between 64 to 96 bits wide. This is a horizontal microword implementation. The term horizontal here implies that the microword has enough bits to directly control all the significant machine resources without additional decoding, encoding, or other hardware interpretation. The inputs, however, are configured into an 8- or 16-bit wide data bus, in order to be loaded directly from the host microprocessor. Figure 2 shows the more detailed arrangement of a typical system which uses only a writeable control store.

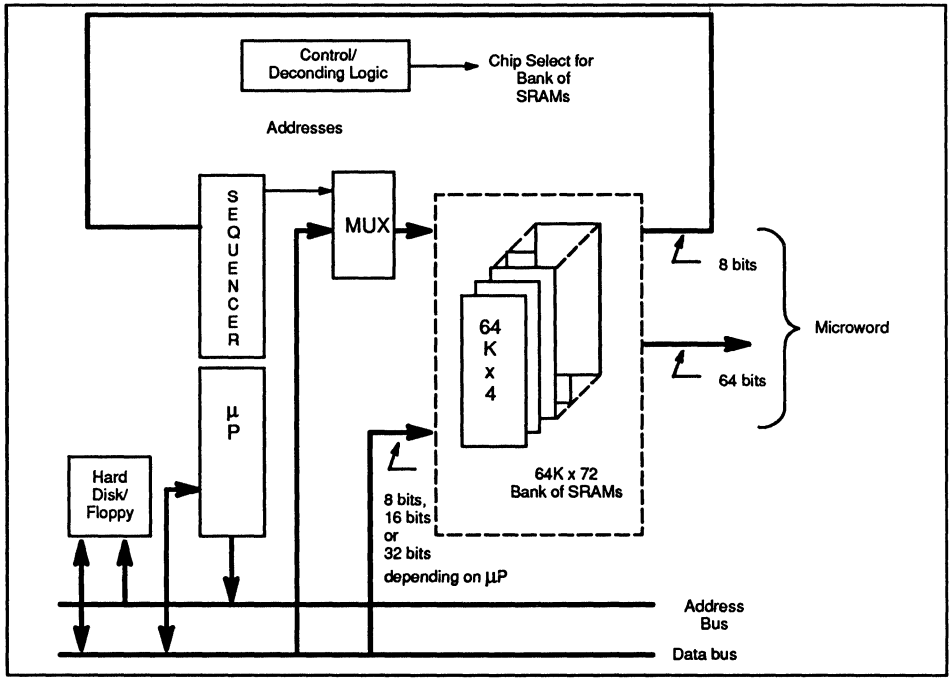

Figure 2. Writeable Control Store Memory

For this type of architecture, a static RAM with separate data inputs and outputs is required. If this design is implemented by devices having a common data input and output bus, then the design would require numerous buffers or transceivers to accomplish this function. Thus, by using a separate data input and output static RAM like the Fujitsu MB81C86, which is 64K x 4 bits wide, the designer realizes a significant savings in IC count, as well as PC board real estate.

Some Thoughts on Application Areas

Due to the flexibility and cost reductions throughout the design development and maintenance, microprogrammed (MP) systems extend across large product and application areas, ranging from simple control functions to complex real time control systems.

Aside from the more common applications, such as emulation of other systems, and upward/downward compatibility among series configured minicomputer systems, microprogram control units (because of their cost effectiveness) can be applied to functions previously performed only by special circuits or custom made devices. For example:

1. Process control systems (factory automation).
2. Instrumentation systems (signal generators, synthesizers etc.).
3. Intelligent terminal for off-line editing (supermarket checkouts, terminals of investment houses).
4. Real time data processing (spectral analysis, pattern recognition, etc.).
5. Data communications systems that have MP systems controlling polling, scheduling tasks, or buffer management (front end processors, communication processors, etc.).

Applications of MP systems are virtually unlimited because of their high performance, low cost implementation. Hence, the availability of static RAMs with separate data inputs and outputs has a substantial impact on the design of MP systems which, in turn, find their way into a wide variety of applications, as discussed previously. Another area of system architecture which benefits from the separate data inputs and outputs on the static RAMs is cache memory system design.

Cache Memory Systems

In a cache-based system, a small, fast memory known as the buffer or the cache, (with roughly the same speed as the processor registers) is interposed between the processor and the main memory. This cache serves as a transparent bridge between their speeds. The "cache bridge" is transparent in the sense that is is invisible, making it inaccessible to the users, since it is completely hidden from them and not directly addressable (cache means "a hiding place"). However, by providing the processor with all the current information it requires at a faster speed, the cache creates an illusion of having a large main memory operating.[3]

During the era of early computing, the main memory technology was quite slow compared to the speed of the CPU. In order to overcome the slow access of the main memory, a small high performance cache buffer memory was placed between the CPU and the main memory. Figure 3 shows two of the most common memory hierarchies.

The two-level cache has already been discussed; i.e., slow memory communicates with a fast CPU. The three-level case takes into account the advantages of having a cache. With this memory hierarchy scheme, the CPU executes data from the very fast cache buffer and only has to slow down when this buffer

requires new data from the slow main memory. Thus, with a small fast buffer, the overall performance of the large, slow main memory approaches that of the buffer.

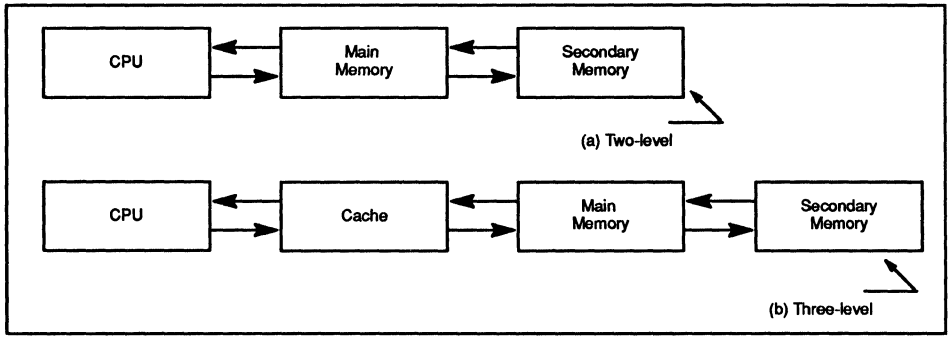

Figure 3. Common Memory Hierarchies: (a) Two-level, (b) Three-level

Basic Blocks of a Cache Memory

As already discussed, the philosophy behind the concept of buffering or caching is to use a fast, relatively small memory between the processor and the main memory. Figure 4 shows a typical way of implementing a cache memory system.

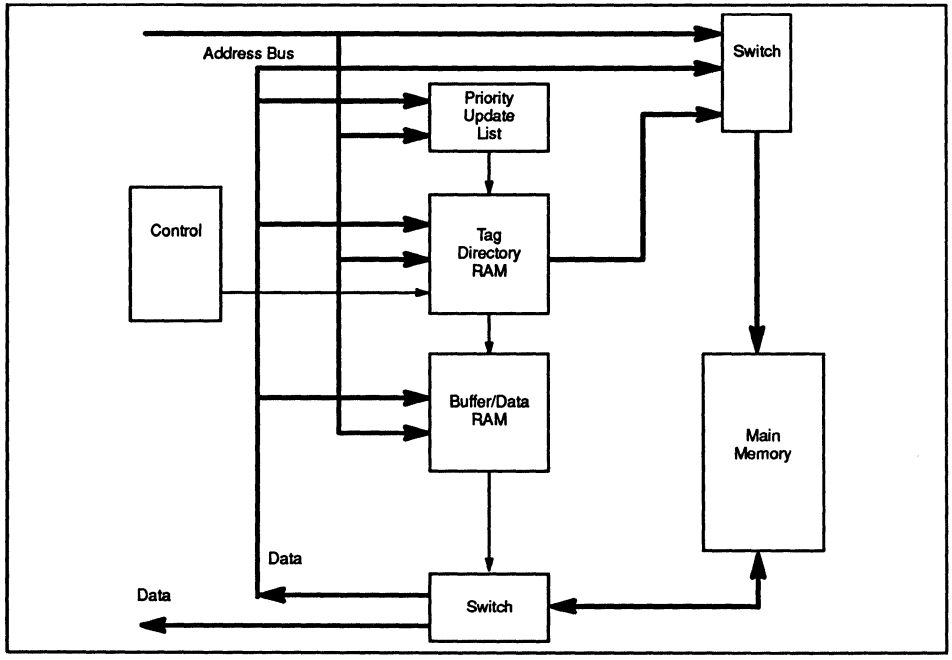

Figure 4. Typical Cache Memory Structure

Buffer Block

A cache memory is basically a small, high-speed memory with main memory information. This information may be addresses, data, or instructions. Hence, the cache can be an address cache, data cache, or an instruction cache. Its speed is typically an order of magnitude faster than that of the main memory, while its capacity is typically one or two orders of magnitude less than that of the main memory.

Tag/Directory Block

A cache memory system requires an identifier or tag store to indicate which entries of main memory have been copied into the cache store. Data in the large main memory has to be mapped into the smaller cache buffer, where it is partitioned or subdivided into small segments called blocks. Each block is identified with a label called the tag address. These tag addresses are stores in an associative RAM called the tag/directory RAM. It operates like a search memory.

Priority Update List

A buffered memory requires a logical network that selects words or blocks to be removed when the new entries (words or blocks) need to be brought into the cache. This structure is called the priority update list.

Control Logic

A cache memory system also requires control logic to generate all timing for synchronizing various activities; for example: searching the tag store, getting the data out of the cache, and replacing proper entries in the cache.

The operation of the total system is quite simple. Whenever the CPU requests the data from the main memory, the first operation that takes place is the matching of addresses coming from the CPU with the addresses inside the directory RAM. If this matches, then the data associated with this tag address is sent to the CPU. This is known as "hit" or address match. If the directory RAM does not contain the address being accessed by the CPU, then a "miss" takes place. When this happens, the data from the main memory is sent to the CPU. It will also be simultaneously stored in the buffer RAM. Hence, if this address is accessed again then the data will come from the cache.

The cache buffer design involves many parameters such as type of memory mapping schemes, (fully associative, direct and set associative), cache size, block size, data replacement algorithm, and a variety of other features which will not be covered in this paper.

In the earlier cache-based systems, the capacity and performance of main memory were modest in comparison to today's systems. Designers were using expensive bipolar RAM technology for performance considerations. Due to the improvements in semiconductor process technology, both bipolar and MOS, the size and performance of cache memories have continued to grow as shown in Figures 5 and 6.

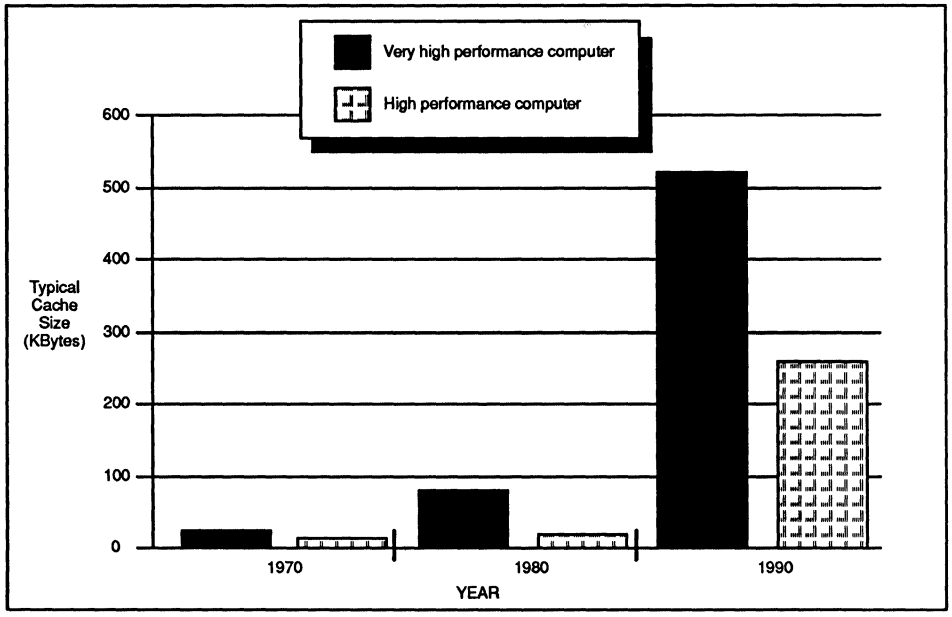

Figure 5. Cache Capacity Trends by Typical Cache Size

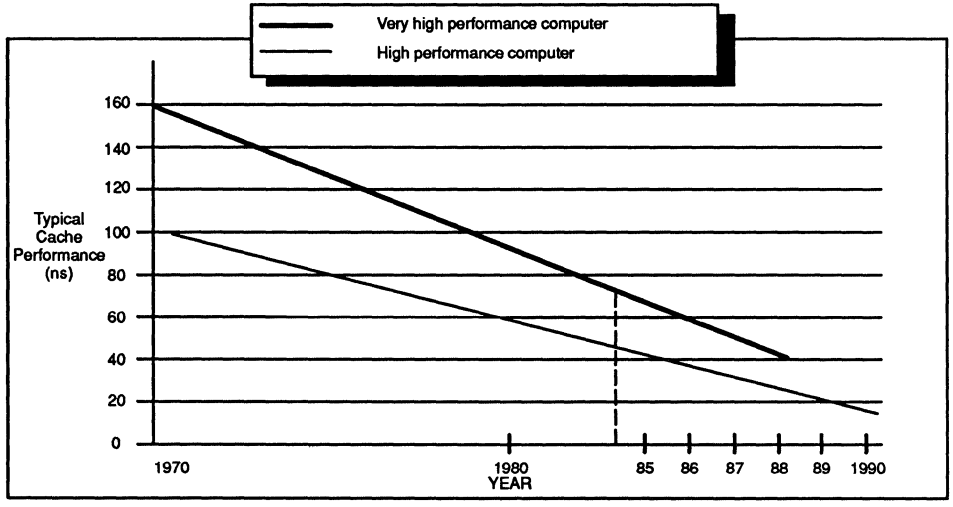

Figure 6. Cache Capacity Trends by Typical Cache Performance

As shown in Figure 6, the typical CPU cache times are approaching 55 ns or less. As far as the performance or hit rate of the cache is concerned, it is primarily determined by the buffer size. Consequently, if a cache buffer size is large, in the order of 256K or 512K, the miss rate is low (see Figures 5 and 6). Hence, a RAM 64K deep is an excellent choice.

Word width is another important consideration. Historically, a RAM with a large number of output drivers is slower than a device with fewer outputs because of high ground noise. Wider word widths, however, will give the system designer a large number of unused bits/word. A by-1-organization provides the highest performance and exact word widths' but it uses a large number of devices. Therefore, a by-4-organization usually provides a better alternative. This choice also affects the board layout.

The majority of by-4-bits and by-8-bits wide SRAMs have their inputs and outputs multiplexed over the same pins. This arrangement, however, increases turnaround and settling delays, thereby slowing system performance. As shown in Figure 4, if the tag and data RAM have a separate data input and output channel, then the glue logic for comparisons will not be followed by multiplexers and demultiplexers. Thus, a SRAM with a separate data input and output bus is ideal for this case. The Fujitsu MB81C86 is a CMOS 64K x 4 SRAM, with an access time of 55 ns, and a separate data input and output bus. For systems which require very high performance, and no board layout constraints, MB81C71A (the 64K x 1 CMOS SRAM with access times as fast as 25 ns) provides a unique solution. It is also useful for high-speed minicomputers and mainframe applications.

Building a Large Disk Cache

Real time interactive graphics and CAD systems are two high-speed computing applications which require a large on-line data base. Only mass storage can deal with such huge quantities of data. Disk drives, as well as mag tapes, are extremely slow, although their capacity is sufficient. These devices transfer data much too slowly for today's high performance mainframes, minicomputers, or microcomputers.

One solution to increase the transfer data rate is to place a semiconductor cache memory between the CPU and the disk subsystem. The cache should be large enough to hold a significant percentage of the data the CPU requires from an I/O device. This cache not only improves the disk data transfer rate, but also more closely matches the speed of the central processing unit of the host system. Incidentally, this cache does not place a heavy demand on the power from either the system or battery back-up.

The Fujitsu MB81C81A-35/45 is a prime candidate since the cache would be several megawords in size. This is a 256K x 1 CMOS SRAM. This device has separate data inputs and outputs. In order to design a 512K-byte disk cache for an 8-bit wide data bus, only 16 of these devices are needed. If the host's main memory access time is 80 ns, then a 45 ns device shortens the system throughput time. A typical system is shown in Figure 7.

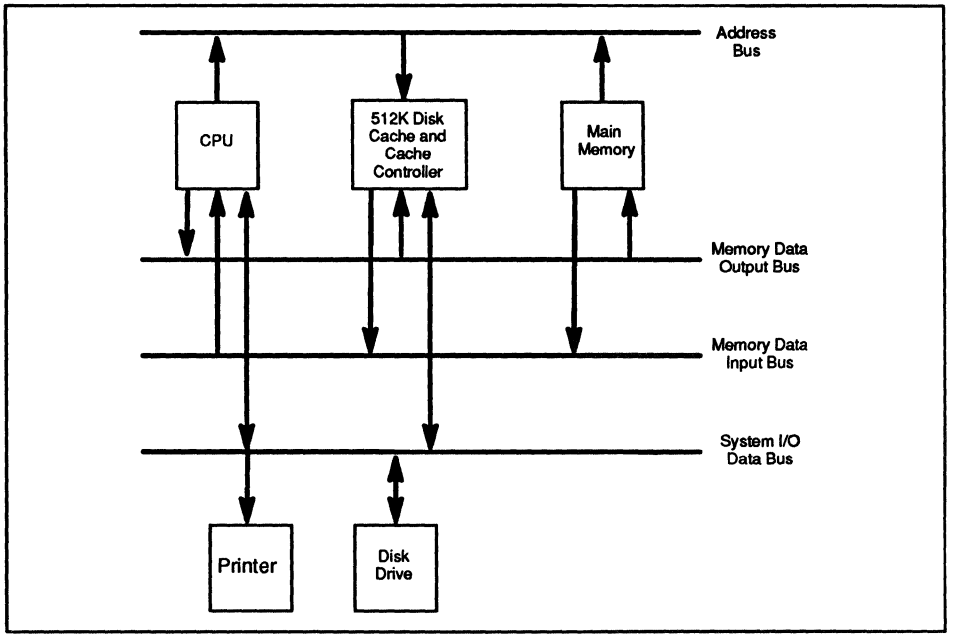

Figure 7. A Large Disk Cache for a Disk Drive Enhances System Performance

Building Deep FIFO Buffers

Separate data input and output SRAMs have a wide variety of applications. They are useful in building deep FIFO buffers. FIFO is a First-In-First-Out memory which can be implemented in different ways. The main function of this type of memory is to read out the data in the same order that it was written. The basic design of a FIFO implemented from the separate data input and output SRAM is shown in Figure 8.

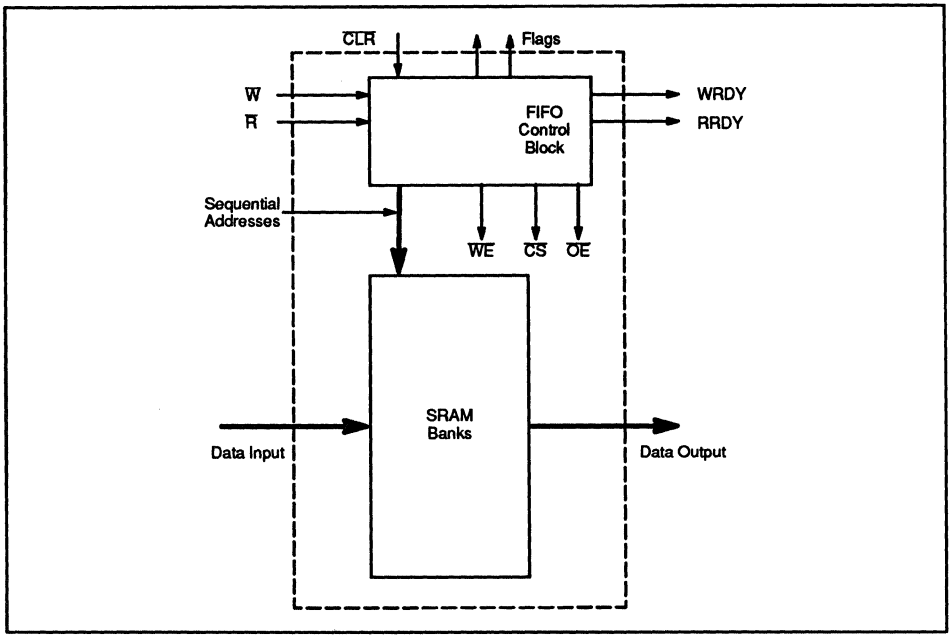

Figure 8. Basic FIFO Design

The FIFO control logic consists of two ring counters for generating read and write addresses. When the FIFO is empty, then both of these counters are initialized to location zero in the SRAM. In the case of a write to the SRAM, the write counter is incremented, thus pointing to the next empty location. The read counter always points to the full location i.e., the location which has data written into it. When all the data has been read, and the read and write counters point to the same location, the FIFO control logic generates an empty flag. A full flag is generated when the write counter points to an address that is less than the read counter. At this point no further data dumps are allowed in the FIFO. This FIFO control block is commercially available as FIFO RAM controller, which can easily create 64K deep buffers from the separate data input and output SRAMs.

FIFO devices are marketed with onboard RAMs. These commercially available FIFO devices provide asynchronous operation, but are not deep enough for such applications as buffers for disk systems, printers, and local area networks where the data usually comes in the form of large blocks. Designers cannot afford to lose the data; consequently, the FIFO buffer should be large enough to hold the complete block. The deepest commercially available devices are 2K words deep.

In order to implement a deep FIFO buffer, it is desirable to have a SRAM with separate data inputs and outputs. This avoids the turnaround delays and muxes/demuxes. Another advantage of using the SRAMs over commercially available devices is that the data can be accessed by the CPU. Therefore, in the disk environment the error correction can be done on the fly. This is not possible in commercially available FIFO devices because they do not have an address bus.

Conclusion

Fujitsu offers the following CMOS static RAMs with separate data inputs and outputs: a 64K x 4 SRAM, MB81C86 (with 55 ns access speed), a 64K x 1 SRAM, MB81C71A, (with 25 ns access speed), and a 256K x 1 SRAM, MB81C81A (with 35 ns access speed). These SRAMs help system designers develop not only an efficient system, but also a less expensive system because of smaller board space.

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2. Brunner, Dick. "High Performance Cache Memory." *IEEE Conference Proceedings*. WesCon 1986
3. Pohm, A.V. and O.P. Agrawal. *High Speed Memory Systems*. Reston Publishing Company.
4. Hartwig, Knorpp, Mears and Osman. "Large Disk Cache Uses Fast 64K by 1 SRAMs to Speed Database Accesses." *Electronic Design*. September 19, 1985.

Appendix 3

Fast SRAMs

November 1990
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APPLICATION NOTE

FUJITSU

Static RAMs

Fast SRAMs in Zero Wait-State Memory Interfaces

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Integrated Circuits Division

Abstract

With the introduction of high-speed microprocessors, running at up to 50 MHz and executing close to one instruction per clock cycle, the performance of state-of-the-art systems has become limited by memory access times. In order to harness the power available from these contemporary microprocessors, it is necessary to design systems capable of accessing memory without waiting for additional clock cycles. This capability is known as "zero wait-state" access, and it demands new techniques and devices in order to maximize system performance.

This Application Note discusses two approaches to maximizing system performance: first, the DRAMs-plus-SRAM cache, the choice for most current designs, and second, the SRAM bank, a choice that offers higher performance, albeit at a higher cost.

This Application Note will also show the choices that present and future high-performance SRAMs offer in terms of granularity (x1, x4, x8, x9) for high performance memory system designs.

High Performance Memory Interfaces

To implement a zero wait-state memory in a high-performance system, some use of SRAMs is necessary because DRAMs have access times that are much slower than a microprocessor cycle time. SRAMs, however, continue to stay with the fastest microprocessors (in terms of access time relative to one clock cycle).

The concept of a SRAM cache to reduce wait-states (first introduced in mainframes) is now commonly used in both workstations and high-performance personal computers. This demand for zero wait-state access has also reached the world of embedded control applications where, although data memory size requirements are generally smaller than in operating system applications, fast access to data is necessary in order to make critical, time-dependent decisions.

There are two possible configurations for a memory interface: (1) a zero wait-state memory could be composed of SRAMs only, or (2) a zero wait-state could have DRAMs (as the primary source) with a SRAM cache. The choice of options is normally dependent on relative cost and component count. Both memory interface options are described as follows.

1. DRAM Bank with SRAM Cache

This option interposes a fast SRAM cache between the processor and the DRAM memory to maintain high system performance (see Figure 1). The cache saves the most frequently used data and provides the processor with fast access to this data. If the processor could always access only the cache, then system performance would be maximized (zero wait-state). However, the prococessor cannot always access the cache because it inevitably requires additional data from the main memory. Thus, only a portion of memory accesses are with the (zero wait-state) cache itself, while the remaining portion is with the (non-zero wait-state) main memory.

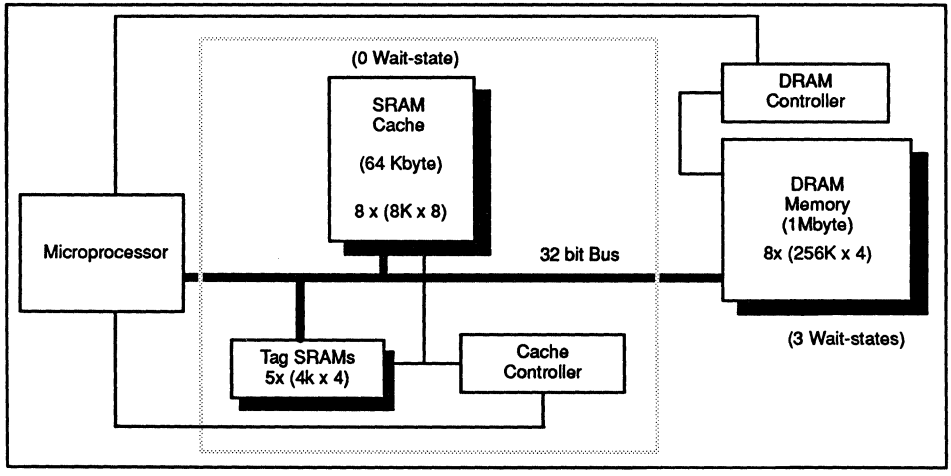

Figure 1. SRAM Cache Plus DRAM Memory Option

Given this mix of accesses, the system performance is dependent on the Hit Ratio of the cache, where the Hit Ratio is defined as:

$$Hit\ Ratio = \frac{Number\ of\ Cache\ Accesses}{Total\ Number\ of\ Memory\ Accesses}$$

To calculate the number of wait-states of this system, the following formula applies:

$$Number\ of\ wait\text{-}states = Hit\ Ratio \times number\ of\ wait\text{-}states\ (cache) + Miss\ Ratio \times number\ of\ wait\text{-}states\ (DRAM).$$

$$where\ the\ Miss\ Ratio = 1 - Hit\ Ratio$$

In a typical i486–VM33MHz system, a fast SRAM cache would have a zero wait-state access, while the much slower DRAM would have a three-wait-state access (based on 80 ns DRAM access time). In the i486–1M33MHz system, the Hit Ratio would quite likely be around 70 percent (this is dependent upon the size of the application program).

Using the preceding formula:

$$Number\ of\ wait\text{-}states = 0.70 \times 0 + 0.30 \times 3$$
$$= 0.90$$

Thus, on the average, the cache implementation adds 0.90 wait-states, or approximately one wait-state that substantially reduces overall system performance. A high-performance RISC, or even i486 processor, averages close to one clock per instruction. A wait-state representing an added clock cycle will reduce the performance of the system dramatically because it takes the processor twice as long to read an instruction from memory. In actual practice, one wait-state will typically reduce system performance by around 30 percent. The 30 percent compares well with the reduction of around 65 percent that occurs when using only DRAMs (wait-states) without the SRAM cache.

The addition of a SRAM cache to improve performance of a system has been the standard to improve performance because the cost impact is minimal. SRAMs cost more than DRAMs, but since the cache is normally around 10 percent of the size of the total memory size, the overall cost addition is modest. Thus, the DRAM plus SRAM cache provides a significant system performance improvement at a modest cost, but it still leaves a potential improvement of 43 percent [1/(1 - 0.3)] untapped. This potentially available improvement leads us to the SRAM-only option.

2. SRAM Bank Only

Whereas the cache plus DRAM performance is dependent on the Hit Ratio of the cache, and the number of wait-states it takes to access the DRAM bank, the SRAM Bank option offers a true 0 wait-state implementation. The straight SRAM Bank option does not limit the performance of the microprocessor, and it does pick up the 43 percent improvement that was left untapped with the DRAM plus SRAM cache option.

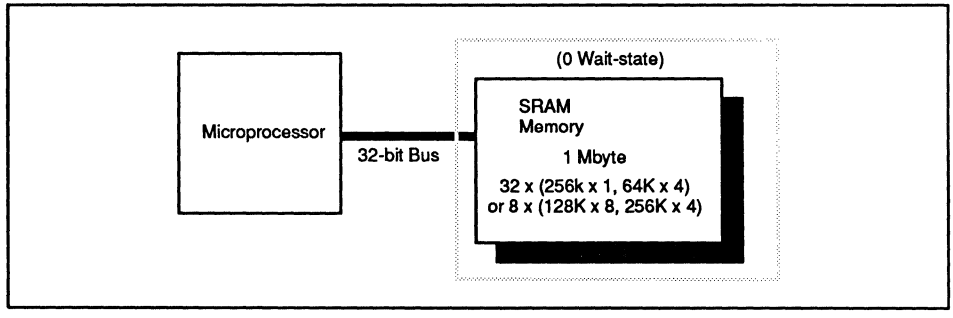

Figure 2. SRAM Memory Option

This option has been used rarely because the cost is significantly higher than for the cache scheme. However, with the current trend to smaller physical sizes in state-of-the-art SRAMs, along with the drive to extract maximum performance, it begins to look very attractive.

Let's take a look at the two approaches, the DRAM plus Cache with a SRAM Bank and the SRAM Bank, side by side.

Comparison of DRAM Plus Cache with the SRAM Bank

For a typical system with a microprocessor running a one clock memory access cycle, the access time requirement for the cache option is the sum of the Tag comparison and the SRAM data access. Since the SRAM memory option does not require a Tag comparison, the system has more time for SRAM memory access, and it can use slower SRAM devices than the DRAM plus cache that is only achieving a one wait-state interface. Clearly, if sheer system performance is the goal, the SRAM bank is the superior option.

Another consideration (when choosing which option to use) is the component count, and here too, the SRAM bank may well offer the optimum solution. Of course, the number of devices also impacts the board space requirement, as well as the power consumed by memory, and normally, it is desirable to make both as low as possible.

The cache plus DRAM option requires additional logic for two controllers (a cache controller and a DRAM controller), each commonly being implemented with three phase-lock demodulators (PLDs) each. In comparison, the SRAM bank option requires no additional devices.

Table 1 shows that if both options use 1 Mb devices, then the SRAM bank would use 8 devices compared to 27 for the DRAM plus cache option, with concomitant power dissipation reduction from 6.2W to 2W. Thus, in addition to a 42 percent performance improvement, the SRAM bank option significantly reduces both required board space and power dissipation.

It may be that in new high-performance systems the additional cost for SRAMs (as the complete memory) may be more than compensated for by the enhanced performance, simpler design, less power dissipation and less board space.

Table 1. System Characteristics

System Factors	Number of Wait-states	Number of Devices	Power Consumption
Option 1: Cache plus DRAM (64Kbyte plus 1Mbyte)	0.9 to 3.0	5 ea. Tag SRAMs 8 ea. Data SRAMs 8 ea. DRAMs 6 ea. PLDs 27 Total Devices	6.2 W
Option 2: SRAM (1mbyte) Bank	0	32 ea. (256Kb) SRAMs, or 8 ea. (1Mb) SRAMs	4.8 W 2 W

Memory Devices as Building Blocks

The traditional memory architectures in operating system-based applications, as well as embedded control systems, have been based on DRAMs. With advances in microprocessor speed, DRAMs are no longer fast enough to take advantage of the full performance of the leading microprocessors. The access

time of the DRAM is too long to satisfy a zero wait-state configuration, so SRAMs must be used in one of the configurations outlined here.

Fujitsu and other vendors are developing high density, high performance CMOS and BiCMOS SRAMs to provide design engineers with a variety of options in implementing these high-performance memory interfaces. Table 2 shows the memory size versus number and type of SRAMs needed in a typical application for a 32-bit bus system.

Table 2. Memory Size vs. Type and Number of SRAM Devices (32-bit Bus)

Memory Size	SRAM	Number of SRAMs
32 KB	8K x 8, 8K x 9*	4
64 KB	8K x 8, 8K x 9*, 16K x 4	8 or 9*
128 KB	32K x 8, 32K x 9*	4
256 KB	32K x 8, 32K x 9*, 64K x 4	8 or 9*
512 KB	32K x 8, 32K x 9* 64K x 4 128K x 8, 128K x 9*	16 or 18* 4

Memory Size	SRAM	Number of SRAMs
1 MB	128K x 8, 128K x 9* 256K x 4 256K x 1	8 or 9* 32 or 36
2 MB	128K x 8, 128K x 9* 256K x 4	16 or 18*
4 MB	128K x 8, 128K x 9* 256K x 4, 1M x 1	32 or 36*

*For Parity applications

The table shows the choices available for each memory configuration. The size of the memory places limitations on the individual memory architecture: a 128K memory cannot be built with a 64K by 4-bit device (since the width, which is 32 bits, dictates the depth to be 256K as a minimum). Obviously, the by 8-bit devices give most options; that is, they give better granularity than by 1-bit or by 4-bit devices.

Fujitsu's CMOS and BiCMOS Fast SRAMs

Current and future high-performance microprocessors demand faster and larger memory, and Fujitsu is continuing to develop memory devices that satisfy these requirements. The present Fujitsu asynchronous CMOS and BiCMOS SRAMs meet JEDEC standards to provide second source compatibility.

The variety of 64K bit, 256K bit, and 1M CMOS and BiCMOS fast SRAMs offered by Fujitsu are shown in Table 3. These SRAMs are the building blocks of memory interfaces, with BiCMOS technology evolving to speeds of 10 ns, and densities over 1Mbit.

From cache applications of 32K byte to 1 Megabyte SRAM memory banks, this choice of fast SRAMs gives design engineers maximum flexibility, whichever memory access technique is chosen.

Table 3. Fast CMOS and BiCMOS SRAMs from Fujitsu

64K	**64K x 1**	**16K x 4**	**16K x 4/OE**	**4K x 8**	**8K x 9**
CMOS	MB81C71A-35/-30/-25	MB81C74-35/-30/-25	MB81C75-35/-30/-25	MB81C78A-45/-35	MB81C79A-45/-35
BiCMOS				MB82B78-20/-15	MB82B79-20/-15
256K	**256K x 1**	**64K x 4**	**64K x 4/OE**	**32K x 8**	**32K x 9**
CMOS	MB81C81A-35/-25	MB81C84A-35/-25	MB81C85A-45/-35/-25	MB8298-35/-25	MB8299-35/-25
BiCMOS	MB82B81-20/-15	MB82B84-20/-15	MB82B85-20/-15	MB82B88-20/-15	MB82B89-20/-15
1M	**1M x 1**	**256K x 4**	**256K x 4/OE**	**128K x 8**	**128K x 9**
CMOS	MB81C81A-35/-25	MB81C84A-35/-25	MB81C85A-45/-35/-25	MB8298-35/-25	MB8299-35/-25
BiCMOS	MB82B001-35/-25	MB82B006-35/-25 20/-15	MB82B85-20/-15	MB82B88–20/-15	MB82B89-20/-15

Conclusion

Contemporary microprocessor-based systems are becoming faster and more powerful, demanding memory subsystems that ensure this power is achieved in real applications. Because traditional DRAM interfaces severely limit the system power actually achieved, cache architectures have become relatively common in high-performance systems. However, it may be that for some user applications, where maximum performance is desirable, the memory interface should be full-SRAM. SRAM devices are available to make that possible, with some impact on cost, but also with significant improvement in board space and power dissipation, in addition to performance.

In either case, Fujitsu offers fast SRAMs able to meet the system requirements.

Appendix 4

Cross Reference Guide for High-Speed (CMOS and BiCMOS) SRAMs

High-Speed CMOS SRAMs

64K Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB81C71A	64K x 1 Separate I/O	35 30 25	N/A	440	55	22 24	DIP[1] SOJ	P PJ
MB81C74	16K x 4 Common I/O	35 30 25	N/A	550	55	22	DIP[1]	P
MB81C75	16K x 4 Common I/O with OE	35 30 25	15 13 10	550	55	24 24	DIP[1] SOJ	P PJ
MB81C78A	8K x 8 Common I/O with OE	45 35	20 15	495	83	28 28 28	DIP[1] SOP SOJ	PSK PF PJ
MB81C79A	8K x 9 Common I/O with OE	45 35	20/15 15/10	495/550	83	28 28 28	DIP[1] SOP	PSK PF

[1]300-mil wide package: Skinny DIP

64K Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers				
	MB81C71A (64K x 1)	MB81C74 (16K x 4)	MB81C75 (16K x 4/OE)	MB81C78A (8K x 8/OE)	M81C79A (8K x 9)
Cypress	CY7C187	CY7C164	CY7C166	CY7C185	CY7C182
Hitachi	HM6287	HM6288	HM6289		
IDT	IDT7187	IDT7188	IDT7198	IDT7164	IDT7169
Micron	MT5C6401	MT5C6404	MT5C6405	MT5C6408	
Mitsubishi	M5M5187A	M5M5188A	M5M5189A	M5M5178	M5M5179
Motorola	MCM6287	MCM6288	MCM6290	MCM6264	MCM6265
NEC	µPD4361	µPD4362	µPD4363		
Performance	P4C187	P4C188	P4C198	P4C164	P4C163
Samsung	KM6165	KM6465	KM6466	KM6865	
Sharp	LH5261	LH5262	LH5267	LH5165 and 5164	
Sony	CXK5164	CXK5464	CXK5465	CXK5863	CXK5971
Toshiba	TC5562	TC55416	TC55417	TC5588	TC55389

High-Speed CMOS SRAMs (Continued)

256K Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB81C81A	256K x 1 Separate I/O	35 25	N/A	550	82.5	24 24	DIP[1] SOJ	PSK PJ
MB81C84A	64K x 4 Common I/O	35 25	N/A	550	82.5	24 24	DIP[1] SOJ	PSK PJ
MB8298	32K x 8 Common I/O with OE	35 25	14 12	605 715	27.5	28 28 28	DIP[1] SOP SOJ	PSK PF PJ
MB8299	32K x 9 Common I/O with OE	35 25	14 12	605 715	27.5	32 32 32	DIP[1] SOP SOJ	PSK PF PJ

[1]300-mil wide package, Skinny DIP

256K Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers			
	MB81C81A (256K x 1)	MB81C84A (64K x 4)	MB8298 (32K x 8/OE)	MB8299 (32K x 9/OE)
Cypress	CY7C197	CY7C194	CY7C199	
Hitachi	HM6207	HM6208	HM62832	
IDT	IDT71257	IDT71258	IDT71256	IDT71259
Micron	MT5C2561	MT5C2564	MT5C2568	
Mitsubishi	M5M5257	M5M5258		
Motorola	MCM6207	MCM6208	MCM6206	MCM6205
NEC		µPD43254		
Performance	P4C1257	P4C1258	P4C1256	
Samsung	KM61257	KM64257	KM68257	
Sharp	LH52251	LH52252 and 52255	LH52254 and 52258	
Sony	CXK51256	CXK54256	CXK58258	CXK58289
Toshiba		TC55464	TC55328	TC55929

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High-Speed BiCMOS SRAMs

64K Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB82B78	8K x 8 Common I/O with OE	20 15	10 8	660	82.5	28 28	DIP[1] SOJ[1] SOP	PSK PJ PF
MB82B79	8K x 9 Common I/O with OE	20 15	10 8	660	82.5	28 28	DIP[1] SOJ[1] SOP	PSK PJ PF

[1]300-mil wide package, Skinny DIP

64K Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers	
	MB82B78 (8K x 8)	MB82B79 (8K x 9)
Cypress	CY7B185	
Hitachi		
IDT	IDT7164	IDT7169
Micron	MT5C6408	
Mitsubishi	M5M5178A	M5M5179A
Motorola	MCM6264	MCM6265
Performance	P4C163	P4C164
Samsung		
Sony	CXK5863A	
Toshiba	TC5588	TC5589

High-Speed BiCMOS SRAMs

256K Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB82B81	256K x 1 Separate I/O	20 15	N/A	660	82.5	24 24	DIP[1] SOJ	PSK PJ
MB82B84	64K x 4 Common I/O	20 15	N/A	660	82.5	24 24	DIP[1] SOJ	PSK PJ
MB82B85	64K x 4 Common I/O with OE	20 15	10 8	660	82.5	28 28	DIP[1] SOJ	PSK PJ
MB82B88	32K x 8 Common I/O with OE	20 15	10 8	715	83	28 28	DIP[1] SOJ	PSK PJ
MB82B89	32K x 9 Common I/O with OE	20 15	10 8	715	83	32 32	DIP[1] SOJ	PSK PJ

[1]300-mil wide package, Skinny DIP

256K Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers				
	MB82B81 (256K x 1)	MB82B84 (64K x 4)	MB82B85 (64K x 4/OE)	MB82B88 (32K x 8/OE)	MB82B89 (32K x 9/OE)
Cypress	CY7C197	CY7C194	CY7C196	CY7C199	
Hitachi	HM6707/A	HM6708/A	HM6709/A		
IDT	IDT71257	IDT71258	IDT61298	IDT71256	IDT71259
Micron	MT5C2561	MT5C2564	MT5C2565	MT5C2568	
Mitsubishi	M5M5257B	M5M5258B			
Motorola	MCM6207	MCM6208	MCM6209	MCM6206	MCM6205
Performance	P4C1257	P4C1258	P4C1298	P4C1256	
Sony				CXK58258	CXK58289
Toshiba		TC55464	TC55465	TC55328	TC55329

High-Speed BiCMOS SRAMs

1M Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB82B001	1M x 1 Separate I/O	35 25	N/A	660	138	28	SOJ	PJ
MB82B006	256K x 4 Separate I/O	35 25	N/A	660	138	32	SOJ	PJ
MB82B005	256K x 4 Common I/O with OE	35 25		660	138	32	SOJ	PJ
MB82B008	128K x 8 Common I/O with OE	25		715	138	32	SOJ	PJ
MB82B009	128K x 9 Common I/O with OE	25		715	138	36	SOJ	PJ

1M Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers				
	MB82B001 (1M x 1)	MB82B005 (256K x 4)	MB82B006 (256K x 4)	MB82B008 (128K x 8)	M82B009 (128K x 9)
Hitachi	HM621100A	HM624256/A	HM624257		
Micron	MT5C1001	MT5C1005			
Mitsubishi	M5M51001	M5M51004			
Samsung	KM611001				
Sony					CXK581020

Low-Power CMOS SRAMs

64K, 256K, and 1M Static RAMs — Product Selection

Fujitsu Part No.	Description	Address Access Time Max. (ns)	Output Enable Access time Max. (ns)	Max. Power (mW)		Pin Count	Packages Available	Suffix
				Active	Standby			
MB8464A-L/-LL	8K x 8 Common I/O	150 100 80	55 45 35	330	11/0.55	28 28 28	DIP[1] DIP[2] SOP	PSK P PF
MB84256-L/-LL	32K x 8 Common I/O with OE	150 120 100 70	60 50 40 35	440	5.5/0.55	28 28 28 28	DIP[1] DIP[2] SOP TSOP	PSK P PF PFTN/ PFTR
MB841000-L	128K x 8 Common I/O	120 100 70	50 40 35	440	5.5/1.1	32 32	DIP[2] SOP SOJ TSOP	P PF PJ PFTN/ PFTR

[1]300-mil wide package: Skinny DIP
[2]600-mil wide package

64K, 256K, and 1M Static RAMs — Product Cross Reference

Vendors	Fujitsu Part Numbers		
	MB8464A (8K x 8)	MB84256A (32K x 8/OE)	MB841000 (128K x8/OE)
Hitachi	HM6264 and 6264A	HM62256	HM628128
Mitsubishi	M5M5165	M5M52256	M5M51008
Motorola	MCM6064	MCM60256	
NEC	µPD4464	µPD43256A	µPD431000A
OKI	MSM5165	MSM51256 and 51257	
Samsung	KM6264	KM62256	KM681000
Sharp	LH5164	LH51256	
Sony	CXK5864	CXK58257	CXK581000
Toshiba	TC5565 and 5563	TC55256 and 55257	TC551001

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