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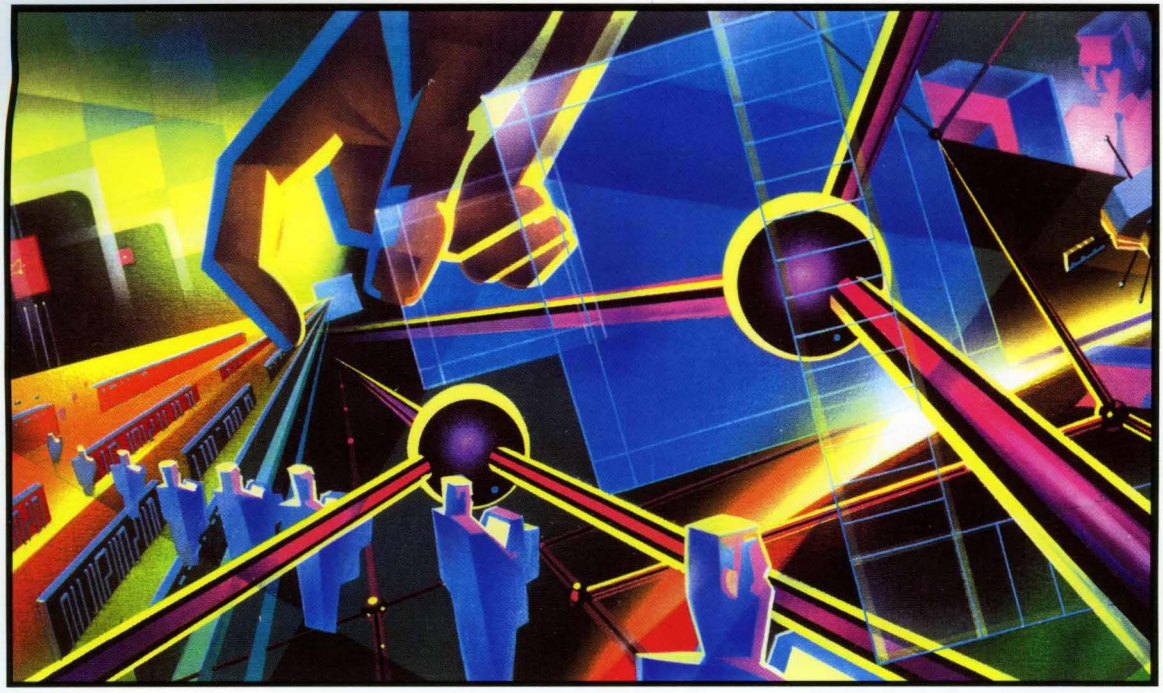

Local Area Network Products

Data Book
1993-1994

FUJITSU Local Area Network Products Data Book 1993-1994

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Local Area Network Products

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FUJITSU

LOCAL AREA NETWORK PRODUCTS

DATA BOOK

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Introduction

At Fujitsu, we work towards an important objective—keeping you one step ahead in a competitive market. As the American arm of Fujitsu Limited, FMI's Semiconductor Division does just that. Giving you a complete selection of sophisticated high-performance microprocessors and micro-peripheral solutions. And backing them with comprehensive documentation and design support.

In a global market, FMI is responsive to your particular needs. We work as your partner to keep pace with technological developments and worldwide market trends. And our success is a result of our values: devotion to technical excellence, insistence on the highest quality and reliability, dedication to outstanding customer service, and commitment to high ethical standards.

Our engineering team, built with heavy emphasis on systems expertise, specializes in developing products with high levels of integration and tight adherence to industry standards. In 1983, we introduced the first Ethernet LAN controller and Manchester encoder/decoder chip set. Building on that experience, we continue to bring you easy-to-use products with the highest performance and the lower system cost. Information on our current LAN products appears in this data book.

Using state-of-the-art design automation, we continue to develop and manufacture superior high-density integrated circuits. And we make sample designs and software available to you. So you can develop LAN systems more quickly and easily—getting them to market faster and more cost effectively than ever before.

Stay one step ahead in the worldwide distributed computing marketplace. Just take a look at our full line of LAN systems solutions—controllers, transceivers, bus interface chips and encoder/decoders. And get the competitive advantage today.

MB86953

PC BUS INTERFACE UNIT

FUJITSU

DATA SHEET

APRIL1993

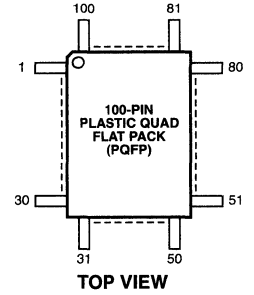
FEATURES

- Companion chip for MB86950 EtherStar™ and MB86960 NICE™ Ethernet LAN Controllers
- Provides interface between controller and IBM® PC, XT™ or AT® bus
- Substantially reduces parts count for LAN adapter
- 8- and 16-bit bus capability
- Supports 8 and 16 Kbyte static RAM and 16, 32 and 64 Kbyte DRAM buffer memory implementations
- Provides decoding for Ethernet node ID PROM
- Programmable adapter I/O address
- Programmable boot PROM address
- 100-pin plastic quad flat pack
- Low-power, high-speed CMOS technology

GENERAL DESCRIPTION

The MB86953 PC Bus Interface Unit (PCBIU) is a single-chip implementation of the logic necessary to interface a LAN adapter utilizing Fujitsu's MB86950 EtherStar or MB86960 NICE controllers to the bus of IBM or compatible PC, XT and AT computers. Implemented in CMOS technology, the PCBIU eliminates external SSI or MSI 'glue' logic for 8-bit adapters, and requires only one or two external parts for 16-bit adapters, depending on buffer memory configuration. Buffer memory may be implemented with static RAM for minimum cost, or with DRAM for larger buffer requirements. The PCBIU allows selection of eight different I/O port addresses and seven different boot EPROM base addresses via external switches or jumpers. Address decoding for an external Ethernet node ID PROM is also provided.

PIN CONFIGURATION



TOP VIEW

(For pin assignment, see pin assignment table)

PIN ASSIGNMENT – PQFP

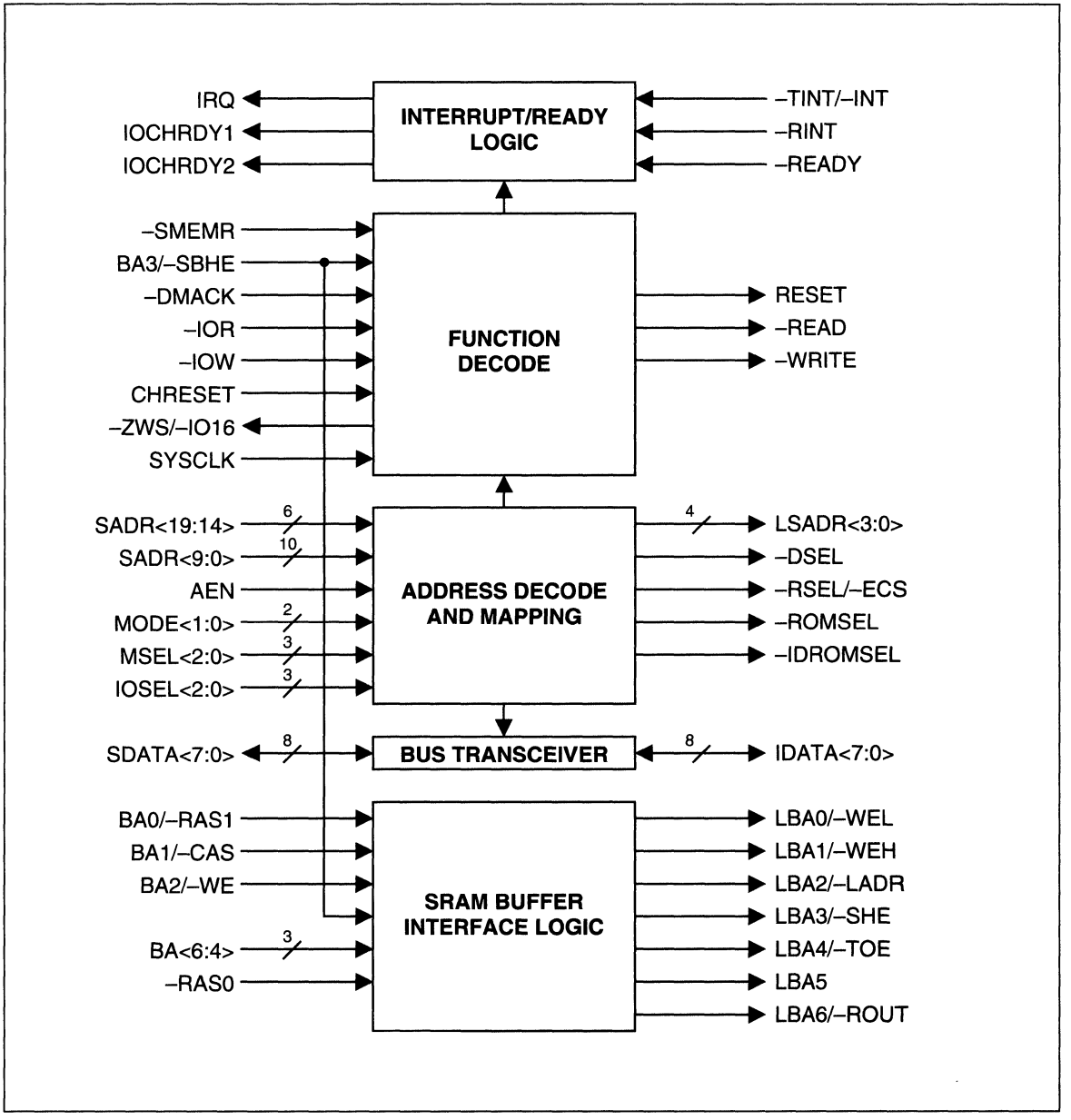
PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	SADR4	I	26	SDATA1	B24	51	N.C.	-	76	LSADR1	O3
2	SADR5	I	27	N.C.	-	52	SDATA7	B24	77	LSADR0	O3
3	VCC	-	28	VCC	-	53	VCC	-	78	VCC	-
4	GND	-	29	GND	-	54	GND	-	79	GND	-
5	IRQ	OD24	30	AEN	I	55	LBA6/–ROUT	O3	80	–DSEL	O3
6	SADR6	I	31	CHRESET	IS	56	LBA1/–WEH	O3	81	–RSEL/–ECS	O3
7	SADR7	I	32	SDATA2	B24	57	LBA0/–WEL	O3	82	–RINT	IP
8	SADR8	I	33	N.C.	-	58	LBA2/LADR	O3	83	–TINT/–INT	I
9	SADR9	I	34	SDATA3	B24	59	LBA5	O3	84	–READY	I
10	SYSCLK	IS	35	N.C.	-	60	LBA3/–SHE	O3	85	RESET	O3
11	–DMACK	IP	36	SDATA4	B24	61	LBA4/–TOE	O3	86	–ROMSEL	O3
12	SADR14	I	37	N.C.	-	62	BA6	IP	87	IDATA7	B3
13	IOCHRDY1	OD12	38	MODE0	IP	63	BA5	IP	88	IDATA6	B3
14	IOCHRDY2	OD12	39	MODE1	IP	64	–SMEMR	I	89	IDATA5	B3
15	GND	-	40	GND	-	65	GND	-	90	GND	-
16	SADR15	I	41	MSEL2	IP	66	BA4	IP	91	IDATA4	B3
17	SADR16	I	42	MSEL1	IP	67	BA3/–SBHE	I	92	IDATA3	B3
18	–IOR	I	43	MSEL0	IP	68	BA2/–WE	I	93	IDATA2	B3
19	SADR17	I	44	IOSEL2	IP	69	BA1/–CAS	I	94	IDATA1	B3
20	–IOW	I	45	IOSEL1	IP	70	BA0/–RAS1	I	95	IDATA0	B3
21	SADR18	I	46	IOSEL0	IP	71	–WRITE	O3	96	–IDROMSEL	O3
22	–ZWS/–IO16	OD24	47	N.C.	-	72	–READ	O3	97	SADR0	I
23	SADR19	I	48	SDATA5	B24	73	–RAS0	IP	98	SADR1	I
24	SDATA0	B24	49	N.C.	-	74	LSADR3	O3	99	SADR2	I
25	N.C.	-	50	SDATA6	B24	75	LSADR2	O3	100	SADR3	I

NOTE: I = Standard input
IS = Schmitt trigger input
IP = Input with pull-up resistor
B3 = 3.2 mA bidirectional I/O
B24 = 24 mA bidirectional I/O
O3 = 3.2 mA totem pole output
OD12 = 12 mA open drain output
OD24 = 24 mA open drain output
N.C. = No connect

ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5 V ±5% T_A = 0° to +70°C
100-Pin Plastic Quad Flat Pack	FPT-100P-M01	MB86953PF-G

BLOCK DIAGRAM



PIN DESCRIPTIONS[1]

PIN NO.	SYMBOL	TYPE	DESCRIPTION
23, 21, 19, 17, 16, 12	SADR<19:14>	I	**HIGH ORDER SYSTEM ADDRESS:** These inputs are connected to the corresponding signals from the system bus.
9 - 6, 2, 1, 100 - 97	SADR<9:0>	I	**LOW ORDER SYSTEM ADDRESS:** These inputs are connected to the corresponding signals from the system bus.
30	AEN	I	**ADDRESS ENABLE:** Input signal from the system bus. When low, indicates that an I/O slave may respond to addresses and I/O commands on the system bus.
39, 38	MODE<1:0>	IP	**MODE CONTROL:** These inputs set the operation mode of the MB86953. See Functional Description for additional information.
41 - 43	MSEL<2:0>	IP	**MEMORY ADDRESS:** These inputs set the base address at which the –ROMSEL output is asserted. See Functional Description for additional information.
44 - 46	IOSEL<2:0>	IP	**I/O ADDRESS:** These inputs set the base address at which the controller is located, and control the assertion of the –DSEL and –RSEL/–ECS outputs. See Functional Description for additional information.
74 - 77	LSADR<3:0>	O3	**LATCHED SYSTEM ADDRESS:** Latched outputs used as address inputs for the controller. These outputs may be modified as described in the Functional Description section.
80	–DSEL	O3	**DATA SELECT:** When operating in the MB86950 (EtherStar) mode, an active low output indicating that the current I/O access is to the BMP register set.
81	–RSEL/–ECS	O3	**REGISTER SELECT:** When operating in the MB86950 (EtherStar) mode, an active low output indicating that the current I/O access is to the DLC register set. When operating in the MB86960 (NICE) mode, an active low output indicating that the current I/O access is for the controller.
86	–ROMSEL	O3	**BOOT ROM SELECT:** Active low enable output indicating that the current memory access is in the range defined by the MSEL<2:0> inputs.
96	–IDROMSEL	O3	**ID ROM SELECT:** Active low enable output indicating that the current I/O access is in the space assigned for the ID ROM.
64	–SMEMR	I	**SYSTEM MEMORY READ:** Active low signal from the system bus which indicates that the current bus cycle is a memory read operation.
20	–IOW	I	**I/O WRITE:** Active low signal from the system bus which indicates that the current bus cycle is an I/O write operation.
18	–IOR	I	**I/O READ:** Active low signal from the system bus which indicates that the current bus cycle is an I/O read operation.
11	–DMACK	IP	**DMA ACKNOWLEDGE:** Active low signal from the system bus indicating that a DMA acknowledge cycle is in progress.
31	CHRESET	IS	**CHANNEL RESET:** Reset signal from the system bus used to generate a reset to the controller chip and other logic on the board.
22	–ZWS/–IO16	OD24	**ZERO WAIT STATE/IO CHANNEL SIZE 16:** In 8-bit mode this active low output is used to shorten the timing of the I/O cycle. In 16-bit mode this active low output indicates that the channel size is 16 bits.
10	SYSCLK	IS	**SYSTEM CLOCK:** Clock from the system bus which controls the timing of several signals from the PCBIU.

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

PIN DESCRIPTIONS (continued)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
85	RESET	O3	**RESET:** Reset output to the controller and other board logic. Produced in response to receipt of CHRESET.
72	–READ	O3	**READ STROBE:** Active low output to the controller which indicates that the current I/O operation is a read cycle.
71	–WRITE	O3	**WRITE STROBE:** Active low output to the controller which indicates that the current I/O operation is a write cycle.
52, 50, 48, 36, 34, 32, 26, 24	SDATA<7:0>	B24	**SYSTEM DATA BUS:** Bidirectional bus for the least significant byte of system data. In 8-bit mode, all data transactions take place over this bus. In 16-bit mode, an external transceiver is required for the upper byte of data.
87 - 89, 91 - 95	IDATA<7:0>	B3	**INTERNAL DATA BUS:** Internal, isolated, 8-bit bidirectional data bus corresponding to SDATA<7:0>.
13, 14	IOCHRDY1, 2	OD12	**I/O CHANNEL READY:** Active high outputs to the system bus indicating that the addressed I/O device is ready for the bus transaction. The outputs can be connected together for increased current sink capability.
5	IRQ	OD24	**INTERRUPT REQUEST:** This output to the system bus indicates that the controller chip is requesting an interrupt.
83	–TINT/–INT	I	**TRANSMIT INTERRUPT / INTERRUPT:** In MB86950 mode, an active low transmit interrupt request input from the controller. In MB86960 mode, an active low interrupt request input from the controller.
82	–RINT	IP	**RECEIVE INTERRUPT:** In MB86950 mode, an active low receive interrupt request input from the controller.
84	–READY	I	**READY:** An active low input from the controller indicating that it is ready to complete the requested bus transaction.
73	–RAS0	IP	**ROW ADDRESS STROBE 0:** In 8-bit MB86950 mode, an input for the RAS0 signal from the controller. Used to latch the buffer address BA<6:0> into the internal address latch to allow operation with static RAM.
70	BA0/–RAS1	I	**BUFFER ADDRESS 0 / ROW ADDRESS STROBE 1:** In 8-bit MB86950 mode, an input for the BA0 signal from the controller. In 16-bit MB86950 mode, an input for the –RAS1 signal from the controller.
69	BA1/–CAS	I	**BUFFER ADDRESS 1 / COLUMN ADDRESS STROBE:** In 8-bit MB86950 mode, an input for the BA1 signal from the controller. In 16-bit MB86950 mode, an input for the –CAS signal from the controller.
68	BA2/–WE	I	**BUFFER ADDRESS 2 / WRITE ENABLE:** In 8-bit MB86950 mode, an input for the BA2 signal from the controller. In 16-bit MB86950 mode, an input for the write enable signal from the controller.
67	BA3/–SBHE	I	**BUFFER ADDRESS 3 / SOURCE BYTE HIGH ENABLE:** In 8-bit MB86950 mode, an input for the BA3 signal from the controller. In 16-bit mode, an input for the active low –SBHE signal from the system bus.
62, 63, 66	BA<6:4>	IP	**BUFFER ADDRESS <6:4>:** In 8-bit MB86950 mode, inputs for the corresponding signals from the controller.
57	LBA0/–WEL	O3	**LATCHED BUFFER ADDRESS 0 / WRITE ENABLE LOW:** In 8-bit MB86950 mode, the latched BA0 output for the SRAM. In 16-bit MB86950 mode, the active low write enable output for the low byte of the buffer SRAM.

PIN DESCRIPTIONS (continued)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
56	LBA1/–WEH	O3	**LATCHED BUFFER ADDRESS 1 / WRITE ENABLE HIGH**: In 8-bit MB86950 mode, the latched BA1 output for the SRAM. In 16-bit MB86950 mode, the active low write enable output for the high byte of the buffer SRAM.
58	LBA2/LADR	O3	**LATCHED BUFFER ADDRESS 2 / LATCH ADDRESS STROBE:** In 8-bit MB86950 mode, the latched BA2 output for the SRAM. In 16-bit MB86950 mode, the control signal used to strobe the row address from the controller into an external latch to address the SRAM.
60	LBA3/–SHE	O3	**LATCHED BUFFER ADDRESS 3 / LATCHED SOURCE BYTE HIGH ENABLE:** In 8-bit MB86950 mode, the latched BA3 output for the SRAM. In 16-bit mode, the active low output to the controller corresponding to the –SBHE signal from the system bus. This signal is latched by the –READY input.
61	LBA4/–TOE	O3	**LATCHED BUFFER ADDRESS 4 / TRANSCEIVER OUTPUT ENABLE:** In 8-bit MB86950 mode, the latched BA4 output for the SRAM. In 16-bit mode, an active low output enable for the external transceiver for the high byte of data.
59	LBA5	O3	**LATCHED BUFFER ADDRESS 5:** In 8-bit MB86950 mode, the latched BA5 output for the SRAM.
55	LBA6/–ROUT	O3	**LATCHED BUFFER ADDRESS 6 / RAS OUT:** In 8-bit MB86950 mode, the latched BA6 output for the SRAM. In 16-bit mode, an active low output which is asserted whenever the –RAS0 or –RAS1 inputs are asserted.
3, 28, 53, 78	V_{CC}	–	**+5 VOLT POWER INPUT**
4, 15, 29, 40, 54, 65, 79, 90	GND	–	**POWER AND SYSTEM GROUND**

NOTE: I = Standard input
IS = Schmitt trigger input
IP = Input with pull-up resistor
B3 = 3.2 mA bidirectional I/O
B24 = 24 mA bidirectional I/O
O3 = 3.2 mA totem pole output
OD12 = 12 mA open drain output
OD24 = 24 mA open drain output

FUNCTIONAL DESCRIPTION

This section provides a detailed description of the operation of the MB86953 PCBIU. Reference should also be made to the timing diagrams in the Electrical Characteristics section of this data sheet for additional information.

The block diagram illustrates the major functional blocks of the MB86953. These are:

- Function decode
- Bus transceiver
- Address decode and mapping
- Interrupt and ready logic
- SRAM buffer interface logic

FUNCTION DECODE

This block converts system bus control and timing signals to appropriate signals to control read and write operations for the adapter logic. The –READ output is asserted whenever the system performs a valid read of the boot ROM, the ID ROM or the controller, and the –WRITE output is asserted whenever the system performs a valid write to the controller. This block also generates a RESET signal in response to a system write to any address in the range 0x18 - 0x1F or assertion of the CHRESET input by the system, and asserts the –ZWS and –IO16 signals with appropriate timing during 8- and 16-bit modes respectively.

BUS TRANSCEIVER

The PCBIU incorporates an 8-bit bus transceiver for the lower eight data bits of the system bus (SDATA<7:0>). This transceiver is capable of sinking 24 mA on the system bus side and 3.2 mA on the adapter logic side (IDATA<7:0>). The transceiver drives the system bus side when a read cycle is made to the boot ROM, the ID ROM or the controller, and drives the adapter logic side when a write cycle to the controller is performed. The enable timing for the transceiver is controlled by the –IOW and –IOR system bus inputs.

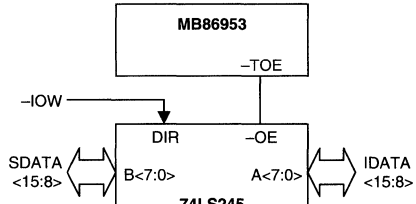


Figure 1. External Transceiver for Upper Data Bus

For 16-bit operation, an external transceiver for the upper eight data bits is required. The –TOE output, which is active in 16-bit mode, is used to control the enabling of the external transceiver, and –IOW from the system bus controls its data direction. See Figure 1.

INTERRUPT AND READY LOGIC

The IRQ output to the system is asserted whenever the controller requests an interrupt, as indicated by assertion of the –RINT or –TINT/–INT inputs from the adapter logic. Assertion of the IOCHRDY1 and IOCHRDY2 outputs to the system indicates that the controller has responded with its –READY output and is ready to complete the requested read or write cycle. The two IOCHRDY outputs may be tied together to provide 24 mA sink capability.

ADDRESS DECODE AND MAPPING

This functional block receives address inputs from the system bus and select inputs from switches or jumpers on the adapter board and generates the appropriate signals to select the boot ROM, the ID ROM or the controller. It also latches and outputs the four least significant bits of the system address for use by the controller. These outputs are remapped when certain registers of the controller are accessed to permit use of additional types of processor instructions, thus allowing greater flexibility in writing the driver for the controller.

The MODE<1:0> inputs select 8- or 16-bit operation with either the MB86950 (EtherStar) or MB86960 (NICE) LAN controllers. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 1.

The MB86953 provides for an optional boot ROM of up to 16 Kbytes on the adapter board. Address selection for this ROM is performed by the MSEL<2:0> inputs. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 2.

I/O address selection of the 32-byte address block for the controller and ID ROM is performed by the IOSEL<2:0> inputs. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 3. Table 4 shows the select output which is asserted and the address output at LSADR<3:0> whenever the system address lies within the address block selected by IOSEL<2:0>.

SRAM BUFFER INTERFACE LOGIC

The PCBIU provides interface logic to allow implementation of an 8 Kbyte or 8 Kword buffer memory with low-cost SRAM when using the MB86950 controller. In 8-bit mode, the PCBIU latches the upper 7 bits of the buffer memory address from the multiplexed buffer address lines (BA<6:0>) from the controller. The latched outputs are provided on LBA<6:0>. In 16-bit mode, the PCBIU generates control signals to control an external address latch and two 8Kx8 SRAMs. See Figures 2 and 3.

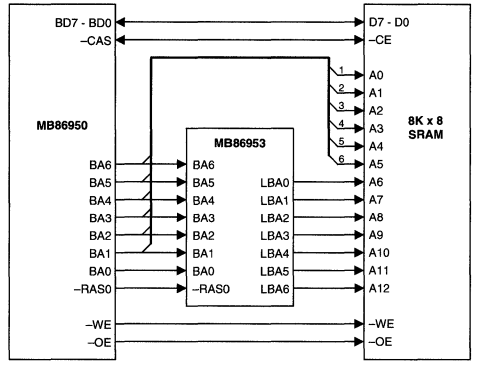


Figure 2. 8-Bit SRAM Buffer for MB86950 EtherStar

TABLE 1. Operating Mode Decoding

MODE 1	MODE 0	OPERATION MODE
0	0	8-bit NICE (MB86960)
0	1	16-bit NICE (MB86960)
1	0	8-bit EtherStar (MB86950)
1	1	16-bit EtherStar (MB86950)

TABLE 2. Boot ROM Address Decoding

MSEL2	MSEL1	MSEL0	ROM ADDRESS
0	0	0	0xC4000 - 0xC7FFF
0	0	1	0xC8000 - 0xCBFFF
0	1	0	0xCC000 - 0xCFFFF
0	1	1	0xD0000 - 0xD3FFF
1	0	0	0xD4000 - 0xD7FFF
1	0	1	0xD8000 - 0xDBFFF
1	1	0	0xDC000 - 0xDFFFF
1	1	1	Decode Disabled

TABLE 3. I/O Addressing

IOSEL2	IOSEL1	IOSEL0	I/O ADDRESS
0	0	0	0x260 - 0x27F
0	0	1	0x280 - 0x29F
0	1	0	0x2A0 - 0x2BF
0	1	1	0x2E0 - 0x2FF
1	0	0	0x300 - 0x31F
1	0	1	0x320 - 0x33F
1	1	0	0x380 - 0x39F
1	1	1	0x3E0 - 0x3FF

TABLE 4. System Address Translation to Select Outputs and Latched Address

SYSTEM ADDRESS	MODE = 00 (NICE 8)		MODE = 01 (NICE 16)		MODE = 10 (ES 8)		MODE = 11 (ES 16)	
	LSADR	SELECT	LSADR	SELECT	LSADR	SELECT	LSADR	SELECT
0x00[1]	0	–ECS	0	–ECS	0	–RSEL	0	–RSEL
|	|	|	|	|	|	|	|	|
0x0F	F	–ECS	F	–ECS	F	–RSEL	F	–RSEL
0x10	8	–ECS	8	–ECS	0	–DSEL	0	–DSEL
0x11	9	|	9	|	0	|	1	|
0x12	A	|	A	|	2	|	2	|
0x13	B	|	B	|	3	|	3	|
0x14	8	|	8	|	4	|	0	|
0x15	9	|	9	|	5	|	1	|
0x16	8	|	8	|	6	|	0	|
0x17	9	–ECS	9	–ECS	7	–DSEL	1	–DSEL
0x18[2]	8	–IDROM	8	–IDROM	8	–IDROM	8	–IDROM
|	|	|	|	|	|	|	|	|
0x1F	F	–IDROM	F	–IDROM	F	–IDROM	F	–IDROM

1. System address is relative to base I/O address selected by IOSEL<2:0>.
2. A write to any address in the range 0x18 - 0x1F will cause the PCBIU to reset the controller by asserting the reset pin. This feature provides a means for software resets.

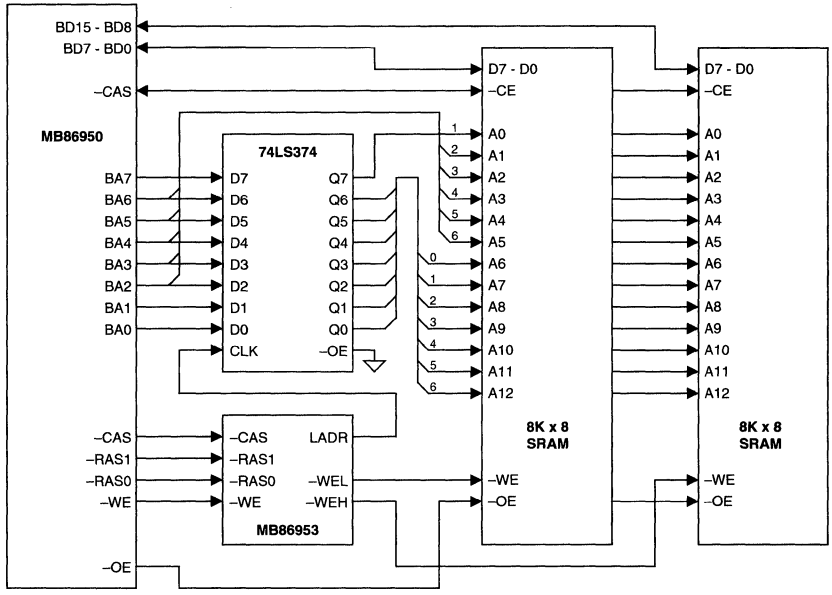


Figure 3. 16-Bit SRAM Buffer for MB86950 EtherStar

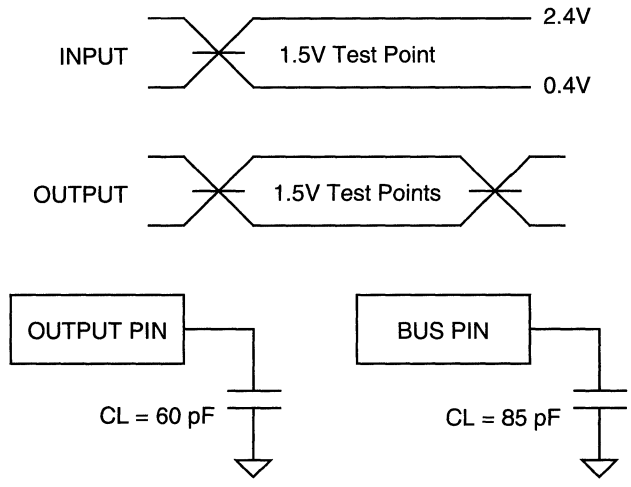


Figure 4. Test Conditions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1,4]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.5	6	V
V_I	Input voltage[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		-40	125	°C
T_{BIAS}	Temperature under bias		-25	85	°C
I_{OS}	Short circuit output current[5]	O3 output OD12 output OD24 output	-40 -60 -90	40 120 180	mA

DC SPECIFICATIONS[3,4] T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.2		V
V_{OL}	Output low voltage O3, B3 outputs OD12 outputs OD24, B24 outputs	 I_{OL} = 3.2 mA I_{OL} = 12 mA I_{OL} = 24 mA	 0 0 0	 0.4 0.4 0.5	 V V V
V_{OH}	Output high voltage O3, B3 outputs B24 outputs	 I_{OH} = -2 mA I_{OH} = -8 mA	 4.0 4.0	 V_{CC} V_{CC}	 V V
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{LZ}	3-state leakage current	V_{IN} = 0 to V_{CC} 3-state condition	-10	10	µA
I_{CC}	Operating power supply current	V_{IN} = 0 or V_{CC} V_{IN} = 0.8 V or 2. 2 V		6 75	mA mA
I_{CCS}	Steady state power supply current	V_{IN} = V_{CC}	0	500	µA
R_P	Input pull-up resistor, IP inputs	V_{IN} = 0 or V_{CC}	25	100	kΩ

CAPACITANCE

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input pin capacitance	T_A = 25°C V_{CC} = 0 V_{IN} = 0 f = 1 MHz		16	pF
C_{OUT}	Output pin capacitance O3, OD12 outputs OD24 outputs			 16 18	 pF pF
$C_{I/O}$	I/O pin capacitance B3 outputs B24 outputs			 16 23	 pF pF

AC CHARACTERISTICS[3,4,6] T_A = 0 °C to +70 °C, V_{CC} = 5 V ± 5%

Write Cycle Timing - Reference Figure 5.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t_1	t_{ADVIOH}	SADR, AEN valid to –IO16 high			53	ns
t_2	t_{ADVLAV}	SADR, AEN valid to LSADR<3:0> valid			22	ns
t_3	t_{WRLCRL}	–IOW low to IOCHRDY1, 2 low			22	ns
t_4	t_{WRLIDV}	–IOW low to IDATA<7:0> active and valid			36	ns
t_5	t_{WRLDSL}	–IOW low to –DSEL low			29	ns
t_6	t_{WRLRSL}	–IOW low to –RSEL/–ECS low			33	ns
t_7	t_{WRLTEL}	–IOW low to –TOE low			29	ns
t_8	t_{CKHWRL}	SYSCLK high to –WRITE low			29	ns
t_9	t_{RYLCRH}	–READY low to IOCHRDY1, 2 high			34	ns
t_{10}	t_{CKHZWL}	SYSCLK high to –ZWS low			35	ns
t_{11}	t_{WRHZWH}	–IOW high to –ZWS high			47	ns
t_{12}	t_{WRHIDF}	–IOW high to IDATA<7:0> three-state			38	ns
t_{13}	t_{WRHWRH}	–IOW high to –WRITE high			19	ns
t_{14}	t_{WRHDSH}	–IOW high to –DSEL high			23	ns
t_{15}	t_{WRHRSH}	–IOW high to –RSEL/–ECS high			23	ns
t_{16}	t_{WRHTEH}	–IOW high to –TOE high			21	ns
t_{17}	t_{ADIIOL}	SADR, AEN to –IO16 low			58	ns
t_{18}	t_{ADILAI}	SADR, AEN to LSADR<3:0> not valid			29	ns

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
4. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5 V. For testing, all inputs swing between 0.4 V and 2.4 V. See Figure 4.
5. Not more than one output may be shorted at a time for a maximum duration of one second.
6. See Figure 4 for test conditions for outputs.

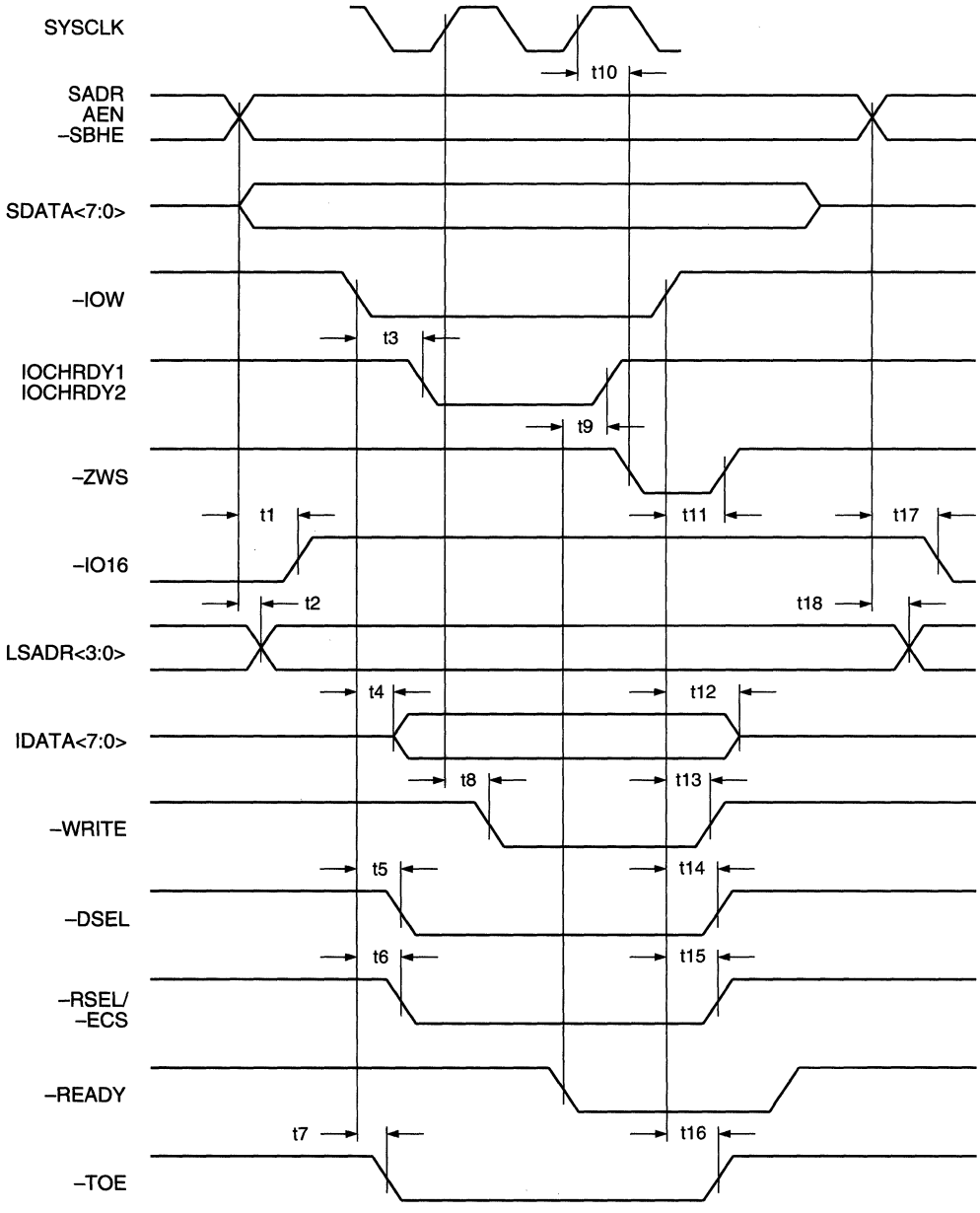


Figure 5. Write Cycle Timing

Read Cycle Timing - Reference Figure 6.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t_1	t_{ADVIOH}	SADR, AEN valid to –IO16 high			53	ns
t_2	t_{ADVLAV}	SADR, AEN valid to LSADR<3:0> valid			22	ns
t_3	t_{RDLSDA}	–IOR low to SDATA<7:0> enabled			39	ns
t_4	t_{RDLCRL}	–IOR low to IOCHRDY1, 2 low			22	ns
t_5	t_{RDLDSL}	–IOR low to –DSEL low			29	ns
t_6	t_{RDLRSL}	–IOR low to –RSEL/–ECS low			33	ns
t_7	t_{RDLTEL}	–IOR low to –TOE low			29	ns
t_8	t_{CKHRDL}	SYSCLK high to –READ low			29	ns
t_9	t_{RYLCRH}	–READY low to IOCHRDY1, 2 high			34	ns
t_{10}	t_{CKHZWL}	SYSCLK high to –ZWS low			35	ns
t_{11}	t_{RDHSDF}	–IOR high to SDATA<7:0> three-state			50	ns
t_{12}	t_{RDHZWH}	–IOR high to –ZWS high			47	ns
t_{13}	t_{RDHRDH}	–IOR high to –READ high			19	ns
t_{14}	t_{RDHDSH}	–IOR high to –DSEL high			22	ns
t_{15}	t_{RDHRSH}	–IOR high to –RSEL/–ECS high			25	ns
t_{16}	t_{RDHTEH}	–IOR high to –TOE high			21	ns
t_{17}	t_{ADIIOL}	SADR, AEN to –IO16 low			58	ns
t_{18}	t_{ADILAI}	SADR, AEN to LSADR<3:0> not valid			29	ns
t_{19}	t_{IDVSDV}	IDATA<7:0> valid to SDATA<7:0> valid			36	ns

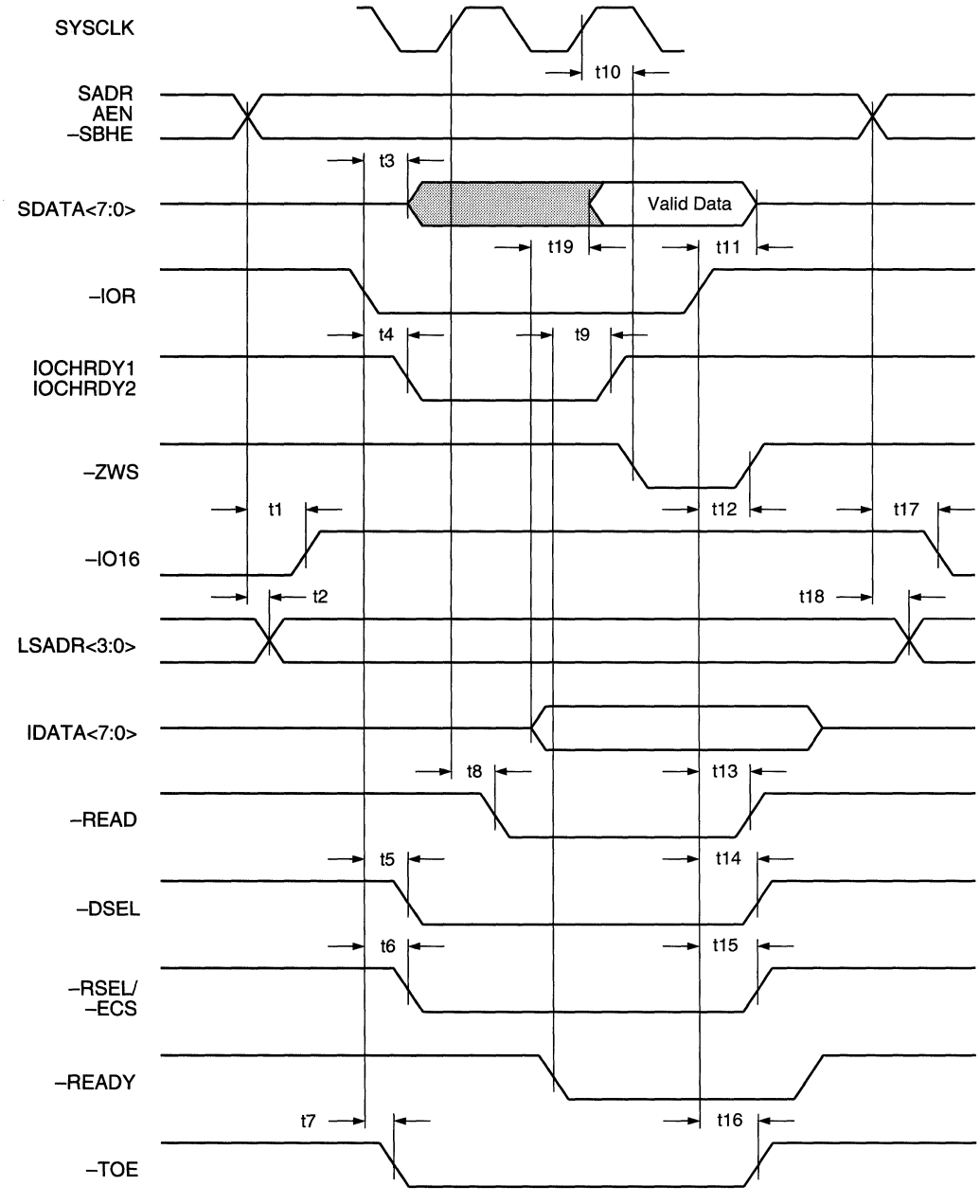


Figure 6. Read Cycle Timing

DMA Write Cycle Timing - Reference Figure 7.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t_1	t_{WRLIDV}	–IOW low to IDATA<7:0> active and valid			36	ns
t_2	t_{WRLTEL}	–IOW low to –TOE low			29	ns
t_3	t_{CKHWRL}	SYSCLK high to –WRITE low			29	ns
t_4	t_{WRHIDF}	–IOW high to –IDATA<7:0> three-state			38	ns
t_5	t_{WRHTEH}	–IOW high to –TOE high			21	ns
t_6	t_{WRHWRH}	–IOW high to –WRITE high			19	ns

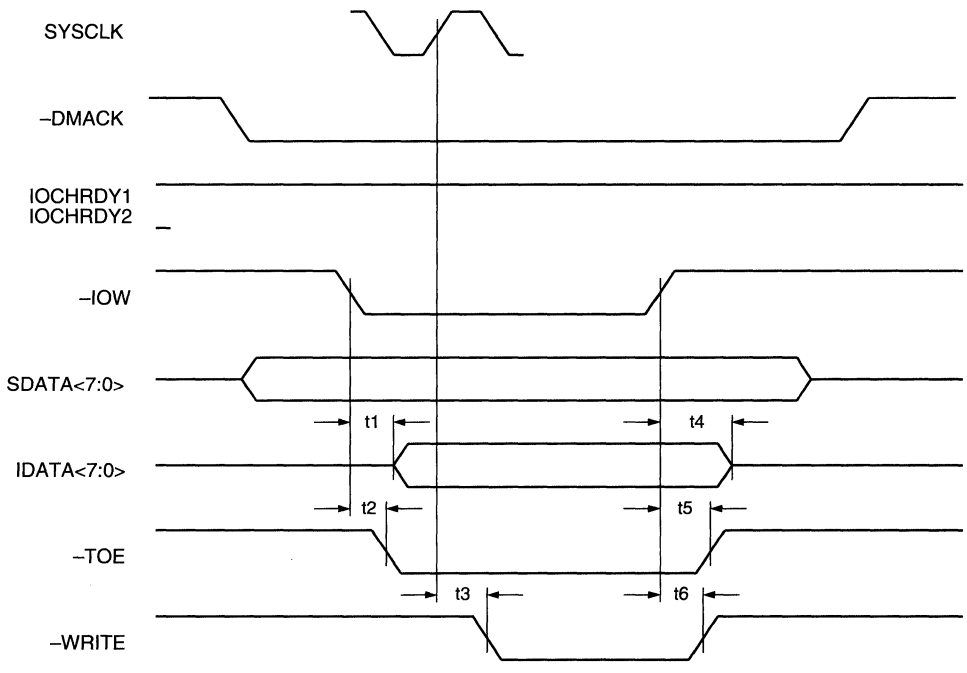


Figure 7. DMA Write Cycle Timing

DMA Read Cycle Timing - Reference Figure 8.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t_1	t_{RDLSDA}	–IOR low to SDATA<7:0> enabled			39	ns
t_2	t_{RDLTEL}	–IOR low to –TOE low			29	ns
t_3	t_{CKHRDL}	SYSCLK high to –READ low			29	ns
t_4	t_{RDHSDF}	–IOR high to –SDATA<7:0> three-state			50	ns
t_5	t_{RDHTEH}	–IOR high to –TOE high			21	ns
t_6	t_{RDHRDH}	–IOR high to –READ high			19	ns
t_7	t_{IDVSDV}	IDATA<7:0> valid to SDATA<7:0> valid			36	ns

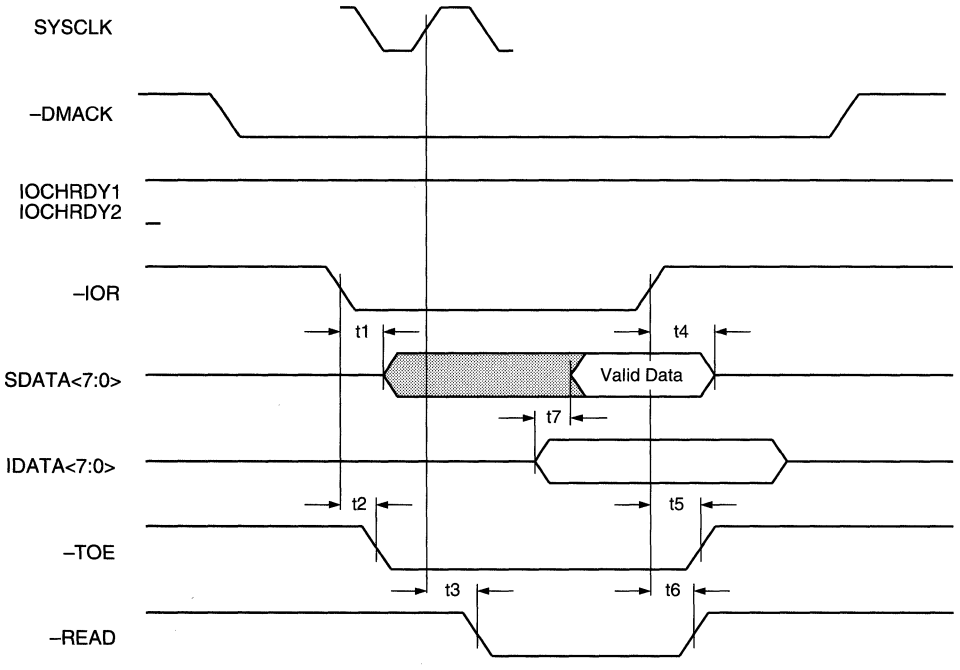


Figure 8. DMA Read Cycle Timing

DRAM to SRAM Signal Conversion Timing - Reference Figure 9.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t_1	t_{RALLAH}	–RAS0 or –RAS1 low to –LADR high			18	ns
t_2	t_{BAVRAL}	BA<6:0> valid to –RAS0 low	45			ns
t_3	t_{RALBAI}	–RAS0 low to BA<6:0> invalid	23			ns
t_4	t_{CALWLL}	–CAS low to –WEL low			28	ns
t_5	t_{CALWHL}	–CAS low to –WEH low			28	ns
t_6	t_{WRHWLH}	–WE high to –WEL high			19	ns
t_7	t_{WRHWHH}	–WE high to –WEH high			19	ns
t_8	t_{RAHLAL}	–RAS0 and –RAS1 low to –ROUT low			24	ns
t_9	t_{RALROL}	–RAS0 or –RAS1 low to –ROUT low			24	ns
t_{10}	t_{RAHROH}	–RAS0 and –RAS1 high to –ROUT high			16	ns

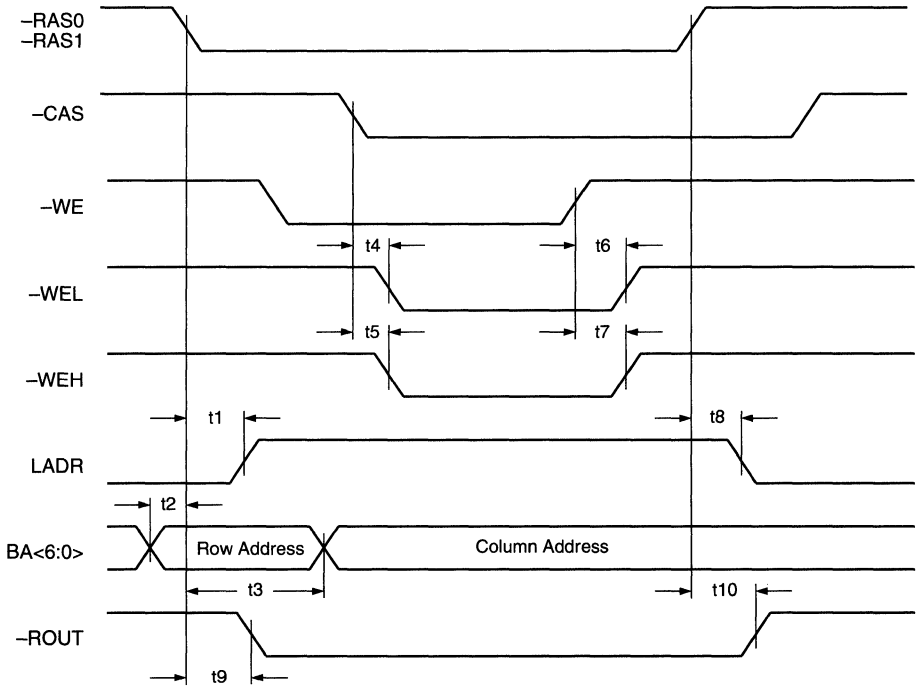
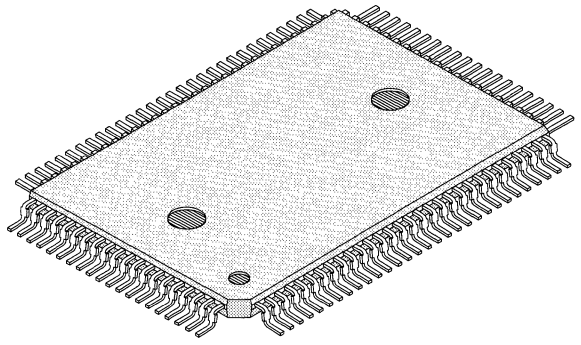


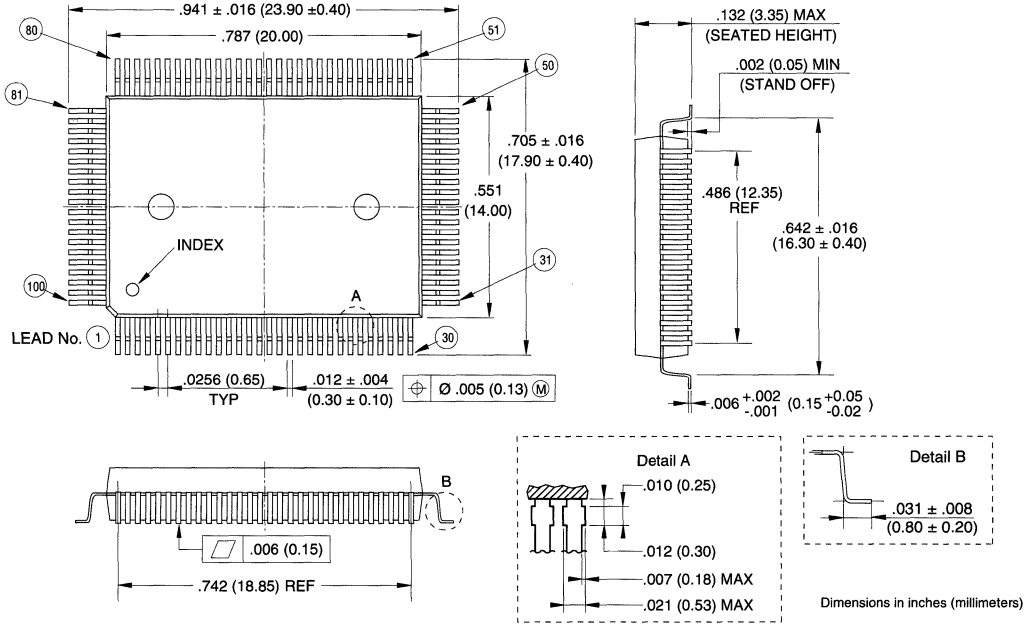
Figure 9. DRAM to SRAM Signal Conversion Timing

100-Pin Plastic Flat Package



Ordering Information: MB86960APF-G

100-Lead Plastic Flat Package
(Case No. FPT-100P-M06)



Dimensions in inches (millimeters)

MB86960

FUJITSU

NETWORK INTERFACE CONTROLLER with ENCODER/DECODER (NICE)

DATA SHEET

APRIL1993

FEATURES

- High-performance packet buffer architecture pipelines data for highest throughput
- 20 Mbyte/second data transfer rate to/from the system bus
- On-chip buffer controller manages pointers, reduces software overhead
- Efficient, configurable two bank transmit buffer and ring receive buffer
- Bus-compatible with most popular microprocessors, including RISC
- Complies with international standards for Ethernet, ISO/ANSI/IEEE 8802–3
- High-speed burst and single transfer DMA
- 64-element hash table for multicast address filtering
- High-speed, low-power CMOS technology
- Power down mode reduces power dissipation for battery-powered equipment
- Available in 100-pin plastic quad flat package

GENERAL DESCRIPTION

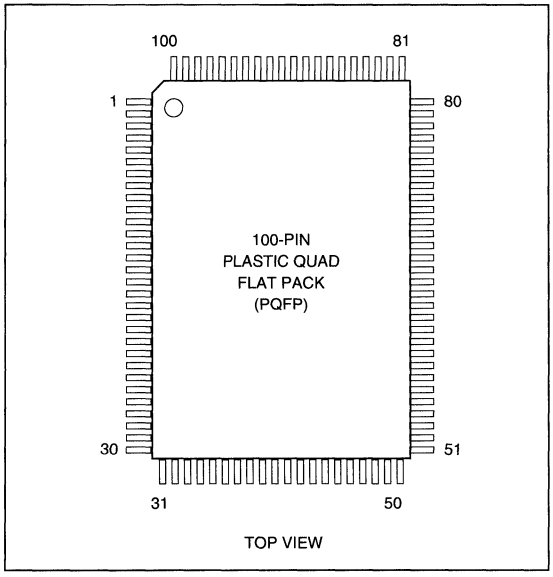
The MB86960 Network Interface Controller with Encoder/Decoder (NICE™) is a high-performance, highly integrated monolithic device which incorporates both network controller, complete with buffer management, and Manchester encoder/decoder. It allows implementation of a 7-chip solution for an Ethernet interface when used with either of Fujitsu's bus interface chips, the MB86953 for PC/XT/AT or the MB86954 for Micro Channel™, and either of Fujitsu's transceiver chips, the MBL8392A coaxial transceiver or MB86962 10BASE-T twisted-pair transceiver.

The unique buffer management architecture of the MB86960 allows packet data to access a buffer memory area from the host and from the network media simultaneously, with virtually no interaction. The network controller updates all receive and transmit pointers internally, thus reducing the software overhead required to control these operations, resulting in superior benchmark speed and application performance. The NICE device has a partitionable 2, 4, 8, or 16 kilobyte, two-bank, transmit buffer which allows multiple data packets to be "chained" together and transmitted to the network from a single transmit command, thus allowing greater design flexibility and throughput. Receive packets are captured in a ring buffer which can be configured in various sizes from 4 to 62 kilobytes, depending on memory equipped and amount used for the transmit buffer.

Possible configurations for the system bus interface include I/O mapping, memory mapping and DMA access, or a combination of these. With a 20 Mbyte/sec bandwidth, the NICE system bus interface allows you to use the full throughput capacity of its unique packet buffering architecture. The NICE controller's selectable bus modes provide both big- and little-endian byte ordering, permitting an efficient data interface with most microprocessors and higher-level protocols.

Implemented in Fujitsu's high-speed, low-power CMOS process, the MB86960 is supplied in a 100-pin plastic quad flat package for surface mounting.

PIN CONFIGURATION



PIN ASSIGNMENTS AND DESCRIPTIONS

Supplied in a 100-pin plastic quad flat pack, the NICE controller presents a small foot-print to the board design, and is surface-mountable with its gull-wing leads. See Pin Configuration and Pin Assignments for the pin numbering.

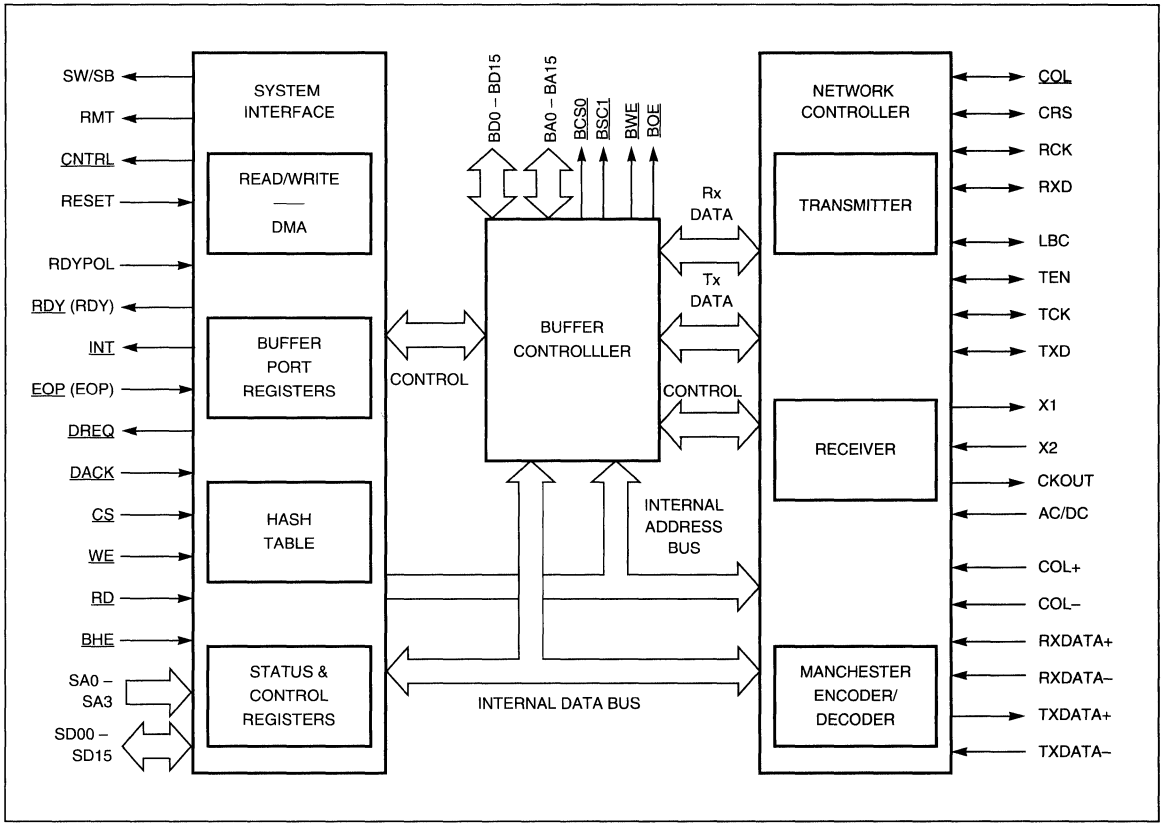
PIN ASSIGNMENTS

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	SD11	B	26	DREQ	O	51	BCS0	O	76	X1	I
2	SD10	B	27	DACK	I	52	BCS1	O	77	X2	O
3	V_{CC}	—	28	V_{CC}	—	53	V_{CC}	—	78	V_{CC}	—
4	GND	—	29	RD	I	54	BA0	O	79	GND	—
5	SD9	B	30	WE	I	55	BA1	O	80	TCK	B
6	SD8	B	31	RESET	I	56	BA2	O	81	RXDATA–	I
7	CS	I	32	BD0	B	57	BA3	O	82	RXDATA+	I
8	BHE	I	33	BD1	B	58	BA4	O	83	COL–	I
9	SW/SB	O	34	BD2	B	59	BA5	O	84	COL+	I
10	SA0	I	35	BD3	B	60	BA6	O	85	V_{CC}	—
11	SA1	I	36	BD4	B	61	BA7	O	86	LBC	B
12	SA2	I	37	BD5	B	62	BA8	O	87	AC/DC	I
13	SA3	I	38	BD6	B	63	BA9	O	88	RCK	B
14	RDY(RDY)	O	39	BD7	B	64	BA10	O	89	CKOUT	O
15	GND	—	40	GND	—	65	GND	—	90	GND	—
16	SD0	B	41	BD8	B	66	BA11	O	91	RXD	B
17	SD1	B	42	BD9	B	67	BA12	O	92	COL	B
18	SD2	B	43	BD10	B	68	BA13	O	93	CRS	B
19	SD3	B	44	BD11	B	69	BA14	O	94	RDYPOL	I
20	SD4	B	45	BD12	B	70	BA15	O	95	CNTRL	O
21	SD5	B	46	BD13	B	71	TEN	B	96	RMT	O
22	SD6	B	47	BD14	B	72	TXD	B	97	SD15	B
23	SD7	B	48	BD15	B	73	GND	—	98	SD14	B
24	EOP(EOP)	I	49	BOE	O	74	TXDATA–	O	99	SD13	B
25	INT	O	50	BWE	O	75	TXDATA+	O	100	SD12	B

Note: B = Bidirectional I/O
I = Standard Input
O = Totem Pole Output

Dual function pins have two names with the second in parentheses ( ).

BLOCK DIAGRAM



PIN DESCRIPTIONS

System Bus Interface Pins

SYMBOL	TYPE	DESCRIPTION
RESET	I	**HARDWARE RESET:** Active high. A minimum pulse of 300 nanoseconds in duration is required. This pin resets NICE's internal pointers and registers to the appropriate state. Note: NICE must be reset after power start before using.
RDY(RDY)	O	**READY:** This output is asserted to indicate to the host that NICE is ready to complete the requested read or write operation. It will also be asserted if the device is unable to respond to the request for a read or write within 2.4 microseconds. In that case, NICE will also assert INT and the bus read error status bit, DLCR1<6>, or bus write error status bit DLCR0<0>. RDY(RDY) may be an active low or active high signal as determined by RDYPOL, pin 94. If RDYPOL is a "1", RDY(RDY) will be active high. If RDYPOL is tied to a "0", RDY(RDY) will be an active low signal.
RDYPOL	I	**READY POLARITY SELECT:** Control input to select the polarity of RDY(RDY), pin 14. When this pin is tied high, RDY(RDY) will be active high. If RDYPOL is tied low, RDY(RDY) will be an active low signal.
WE	I	**WRITE:** The WE pin is an active low input that enables a write operation from the host system to the buffer memory port or to internal registers selected by system address inputs SA0–3.
RD	I	**READ:** Active low input which specifies that the current transfer between NICE and the host system is a read from one of NICE's internal registers or its data port as selected by SA0–3.
CS	I	**CHIP SELECT:** This active low input signal is the chip select for NICE.
BHE	I	**BYTE HIGH ENABLE:** Active low. This pin is the byte/word control line. It is used only when NICE is configured for a 16-bit data bus by the SB/SW bit of DLCR6. It allows word, upper byte only or lower byte only transfers. The address select pin SA0 is used with BHE for byte or word transfers as follows.
INT	O	**INTERRUPT:** Active low. Indicates that NICE requires host system attention after successful transmission or reception of a packet, or if any error conditions occur, or if an EOP (end of process) signal from the host occurs after the completion of the DMA cycle. The interrupt signal is maskable and can be disabled by writing a 0 to the appropriate mask bit.
EOP(EOP)	I	**END OF PROCESS:** Indicates to NICE that the DMA transfer is finished. When the host DMA controller asserts EOP(EOP), further assertions of NICE's bus request output, DREQ, will be discontinued.

SB/SW	BHE	SA0	Function
0	0	0	Word transfer
0	0	1	Byte transfer on upper half of data bus (SD15–8)
0	1	0	Byte transfer on lower half of data bus (SD7–0)
0	1	1	Reserved
1	X	X	Byte transfer (SD7–0)

Note: B = Bidirectional I/O
I = Standard Input
O = Totem Pole Output

Dual function pins have two names with the second in parentheses ( ).

PIN DESCRIPTIONS

System Bus Interface Pins (Continued)

SYMBOL	TYPE	DESCRIPTION
CNTRL	O	**CONTROL:** This pin is the complement of the register bit CNTRL, DLCR4<2>. It is used to control external functions.
RMT	O	**REMOTE CONTROL PACKET:** When DLCR5<2> is set high, this pin follows the RMT 0900H bit (DLCR1<4>) which indicates that a complete special packet with type field = 0900H has been received. This is intended for use as a remotely-controlled hardware function from other nodes in the network.
DREQ	O	**DMA REQUEST:** Issued to the DMA controller to indicate that NICE has data available to be read in its receive buffer, or is ready to accept data into its transmit buffer.
DACK	I	**DMA ACKNOWLEDGE:** Active low. Indicates that the DMA controller is ready to transfer data between the host system and NICE's buffer memory through BMPR8.
SA<3:0>	I	**SYSTEM ADDRESS LINES:** Specify which of the internal registers or ports of NICE is selected for read/write operations.
SD<15:0>	B	**SYSTEM DATA BUS:** All data, command and status transfers between the host system and NICE take place over this bidirectional, 3-state, bus. The direction of the transfer is controlled by RD and WE. The register or buffer port being accessed is selected by a combination of DACK (if active, selecting the Buffer Port), or the address pins SA3–0 and register bank select bits REG BANK 1 and REG BANK 0, DLCR7<3:2>. The portion of the data bus over which the transaction occurs is controlled by SB/SW, BHE, and SA0.
SW/SB	O	**SYSTEM WORD/SYSTEM BYTE CONFIGURATION:** This signal output reflects the inverse of DLCR6<5>, SB/SW. If SW/SB = 1, the system interface is configured for word transfers. If SW/SB = 0, the system interface is configured for byte-wide transfers on SD7–0, the lower byte.

Note: B = Bidirectional I/O
I = Standard Input
O = Totem Pole Output

Dual function pins have two names with the second in parentheses ( ).

PIN DESCRIPTIONS

Buffer Memory Interface Pins

SYMBOL	TYPE	DESCRIPTION
BCS0 BCS1	O O	**BUFFER CHIP SELECT:** BCS1 and BCS0 are the chip select lines, most significant byte and least significant byte respectively, of the dedicated buffer SRAMs. Active low.
BOE	O	**BUFFER OUTPUT ENABLE:** This active low signal is the output enable for the Buffer SRAM, and is asserted by NICE during buffer memory read cycles.
BWE	O	**BUFFER WRITE ENABLE:** Active low. Used as a write strobe to the buffer SRAM memory during write operations.
BD<15:0>	B B	**BUFFER DATA:** Data lines between the SRAM buffer memory and NICE. This SRAM data bus is configurable for an 8-bit or 16-bit data size by BUFFER BYTE/BUFFER WORD, BB/BW, in DLCR6<4>. The transfer byte order within a word, most-significant or least-significant byte first, is determined by DATA_ORDER, DLCR7<1>.
BA<15:0>	O O	**BUFFER ADDRESS:** These lines address up to 64 kilobytes of SRAM buffer memory.

Network Interface Pins

SYMBOL	TYPE	DESCRIPTION
TXDATA+ TXDATA–	O O	**TRANSMIT INTERFACE PAIR:** These are the differential outputs to the transceiver for transmitting.
RXDATA+ RXDATA–	I I	**RECEIVED DATA:** These are the Manchester differential inputs from the transceiver to the receiver.
COL+ COL–	I I	**COLLISION:** These differential inputs are driven with a 10 MHz signal when the transceiver detects a collision on the media.
AC/DC	I	**AC/DC COUPLING SELECT:** AC/DC = 1 selects AC coupling; 0 selects DC coupling for the TXDATA outputs. When AC coupling is selected, both TXDATA+ and TXDATA– are driven to the same output voltage level during the transmit idle period to prevent saturation of the isolation transformer. With DC coupling, these outputs remain at a 1 level during idle periods.

System Clock Pins

SYMBOL	TYPE	DESCRIPTION
X1	I	**CRYSTAL INPUT:** Connection for one side of the 20 MHz crystal, or input for an external 20 MHz clock source.
X2	O	**CRYSTAL OUTPUT:** Connection for the other side of the 20 MHz crystal. Leave unconnected if an external clock is used.
CKOUT	O	**CLOCK OUTPUT:** 20 MHz free-running clock output provided by the crystal oscillator circuit.

PIN DESCRIPTIONS

The following eight pins are provided for optional connection to an external encoder/decoder. They can also be used for test purposes, but are not used in a typical network interface application. Special encoder/decoder modes are selected by setting DLCR7<7:6>. Refer to the **MEDIUM CONNECTION** section under **SYSTEM CONFIGURATION** for a complete description of these modes.

Controller—Encoder/Decoder Interface Pins

SYMBOL	TYPE	DESCRIPTION
TXD	B	**TRANSMIT DATA:** NRZ transmit serial data. Normally not used. In "Encoder/Decoder Bypass" mode and "NICE + Monitor" mode, an output which can be fed to an external encoder. In "Encoder/Decoder Test" mode, an input to the on-chip encoder.
TCK	B	**TRANSMIT DATA CLOCK:** Clock synchronous with TXD serial data. Normally not used. In "Encoder/Decoder Bypass" mode, a 10 MHz data clock input used by the controller to synchronize the TXD data signal. In "NICE + Monitor" mode and "Encoder/Decoder Test" mode, an output from the on-chip encoder.
TEN	B	**TRANSMIT ENABLE:** Normally not used. In "NICE + Monitor" mode and "Encoder/Decoder Bypass" mode, this pin is an output which can be used to control an external encoder. When asserted high, TEN enables the encoding of the transmitted data. In "Encoder/Decoder Test" mode, an input to the on-chip encoder.
$\overline{\text{COL}}$	B	**COLLISION PRESENCE:** Normally not used. In "Encoder/Decoder Bypass" mode, an active low input which indicates that the collision inputs COL are active, signifying that the transceiver has detected a collision on the media. In "NICE + Monitor" mode and "Encoder/Decoder Test" mode, this is an output from the on-chip encoder/decoder section. $\overline{\text{COL}}$ is a normally high input which changes to a 10 MHz pulse stream during collision detection.
LBC	B	**LOOPBACK CONTROL:** Normally not used. In "Encoder/Decoder Bypass" mode and "NICE + Monitor" mode, this output should be connected to the loopback control pin of the external encoder/decoder. When this output is asserted high, the external encoder/decoder is placed in loopback mode. TEN enables the encoding of the transmitted data. In "Encoder/Decoder Test" mode, this is an input with the same function.
RXD	B	**RECEIVE SERIAL DATA:** Normally not used. In "Encoder/Decoder Bypass" mode, "NICE + Monitor" mode and "Encoder/Decoder Test" mode, an NRZ serial bit stream from a decoder or demodulator to the data link controller.
RCK	B	**RECEIVE DATA CLOCK:** Normally not used. In "Encoder/Decoder Bypass" mode, "NICE + Monitor" mode and "Encoder/Decoder Test" mode, this pin is an input for the serial data clock as recovered by the external decoder or demodulator.
CRS	B	**CARRIER SENSE:** Normally not used. In "Encoder/Decoder Bypass" mode, an input indicating the presence of incoming data on the network. In "NICE + Monitor" mode and "Encoder/Decoder Test" mode, an output from the on-chip encoder/decoder. Assertion of this active high input indicates that a carrier has been sensed at the RXDATA inputs.

PIN DESCRIPTIONS

Mode Configuration and Encoder/Decoder Pin Input/Output Table

CNF1	CNF0	MODE	TXD	TCK	TEN	LBC	RXD	RCK	CRS	COL
0	0	NORMAL NICE	Internal E/D is used with NICE controller, no signal appears on pins							
			none	none	none	none	none	none	none	none
0	1	NICE + MONITOR	Internal E/D is used with NICE controller, signal appears on output							
			O	O	O	O	O	O	O	O
1	0	E/D BYPASS	External E/D is used with NICE controller, internal E/D is shutdown							
			O	I	O	O	I	I	I	I
1	1	E/D TEST	Internal E/D is used only, NICE controller section is shutdown							
			I	O	I	I	O	O	O	O

Device Power Pins

SYMBOL	DESCRIPTION
V_{CC}	**POWER SUPPLY:** A +5 V_{DC} ±5% supply is required.
GND	**SYSTEM GROUND:**

Ordering Code

PACKAGE STYLE	PACKAGE CODE	ORDERING CODE
100-Pin Plastic Quad Flat Pack	FPT-100P–M01	MB86960APF–G

SYSTEM CONFIGURATION

A highly integrated system configuration can be achieved with the NICE controller. Figure 1 illustrates a low chip count LAN controller with NICE, a bus interface chip such as Fujitsu's MB86953 or MB86954, and either a coaxial transceiver such as Fujitsu's MBL8392A or a 10BASE-T twisted pair transceiver such as Fujitsu's MB86962. Because of its high integration and unique, innovative architecture, which handles all aspects of packet management and storage, a local microprocessor is not required.

The NICE controller connects to the host system bus to provide command and status interfaces as well as packet data access. Command and status registers can be directly accessed by the host processor when mapped into the I/O or memory space of the host. Through a port on the device, data packets to be transmitted to the media are transferred first from host memory to a dedicated buffer memory for temporary storage until transmitted. Received data packets are first stored in the buffer memory, then later transferred to the host memory.

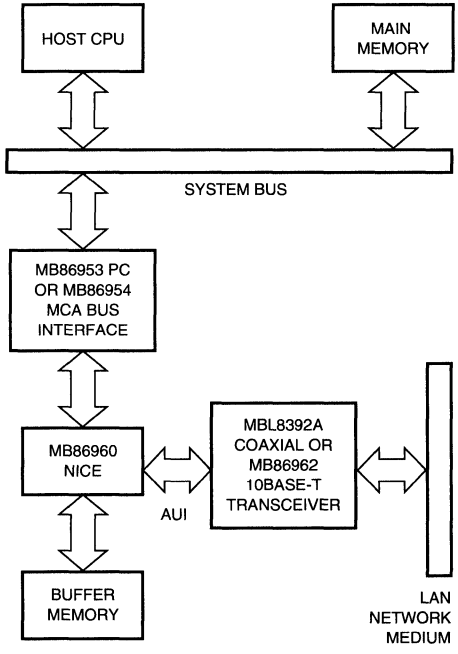


Figure 1.Typical System Configuration

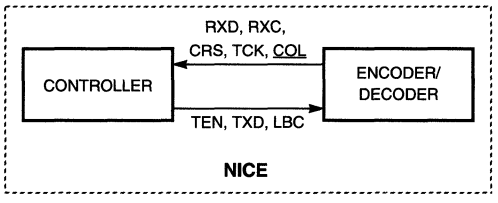
Medium Connection

Connection to the LAN medium can be accomplished with any of the popular connection methods: 1) on-board connection to unshielded twisted pair through a 10BASE-T transceiver, 2) on-board connection to a thin 50-Ohm coaxial cable through a 10BASE2 transceiver or 3) off-board connection to any other type of medium, such as standard Ethernet coaxial cable (10BASE5), through an Attachment Unit Interface (AUI) connector.

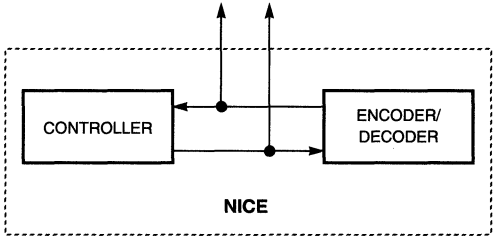
NICE has an encoder/decoder (E/D) on chip. An external encoder/decoder can be used by making the NICE chip act like a controller alone (depending on customer's needs). This option can be changed by using bits 7 and 6 of DLCR7.

Eight pins related to the on-chip E/D can be configured by DLCR7<7:6> (register DLCR7, bits 7 through 6) to operate in one of four modes. These pins are TXD, TCK, TEN, LBC, RXD, RCK, CRS, and COL. In the "Normal NICE" mode, an internal E/D is used. In this mode, the pins are all electrically isolated and no signals appear on the pins. In "NICE + Monitor" mode, all the pins listed above are outputs whose specific signals appear on the pins and can be monitored externally. In "Encoder/Decoder Bypass" mode, an external encoder/decoder is used with the NICE controller, its own internal E/D is shut down. In this mode, the pins are either outputs or inputs as needed to control the external encoder/decoder. In the "Encoder/Decoder Test" mode, only the E/D on NICE is active and accessible, the NICE controller section is shut down. In this mode, the pins are outputs or inputs for an encoder/decoder, with the opposite control direction of the outputs or inputs in the "Encoder/Decoder Bypass" mode. The various possibilities are shown in Figure 2 and the table below.

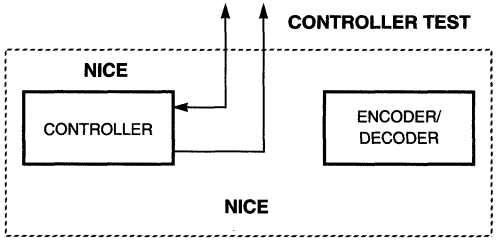
DLCR7 Bit 7	DLCR7 Bit 6	Function
0	0	Normal NICE
0	1	NICE plus Monitor
1	0	Encoder/Decoder Bypass
1	1	Encoder/Decoder Test



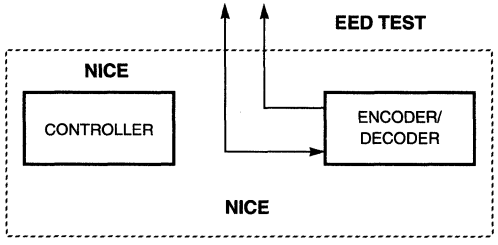
CASE 00: NORMAL NICE MODE



CASE 01: NICE + MONITOR



CASE 10: ENCODER/DECODER BYPASS



CASE 11: ENCODER/DECODER TEST

Figure 2. Encoder/Decoder Modes

CRYSTAL OSCILLATOR

The ISO/ANSI/IEEE 8802–3 international LAN standard specifies a bit clock rate of 10 Mbit/sec. This is obtained from a 20 MHz clock generated by the on-chip oscillator, which operates from an external crystal connected between pins X1 and X2 on the NICE chip. Crystal capacitance as specified by the manufacturer should be connected from X1 and X2 to ground, considering any stray capacitance which can vary the crystal's frequency. See Figure 3 for typical values. A crystal with the following specifications is recommended: quartz (AT-cut; 20 MHz; frequency/accuracy of ±50 ppm at 25°C to 70°C; parallel resonant with 20 pF load in a fundamental mode. Possible vendors include: Ecliptek Corp. (Costa Mesa, CA), p/n ECSM200-20.000; and M-tron Industries, Inc. (Yankton, SD), p/n MP-1 & MP-2, with 20MHz, 50ppm over 0°C to 70°C, and 18 pF fundamental load.

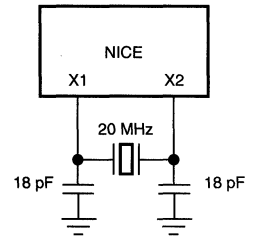


Figure 3. Crystal Connection

The clock also serves as a reference for an internal phase locked loop which is used for clock recovery in the decoder section. Internal clocks are shut down when DLCR7 bit 5, PWRDN, is invoked for Power Down Mode.

SRAM CONFIGURATIONS

Eight different configurations of SRAM for the packet buffer are possible as illustrated in Figure 4. First, the width of the SRAM data path can be 8 or 16 bits, selected by programming the Buffer Byte/Buffer Word (BB/BW) bit, bit 4 of DLCR6. If this bit is set to 1, byte-wide data is selected; if set to 0, the width is word-wide (16 bits). The SB/SW Bit, DLCR6 bit 5, selects the system bus width, while the BB/BW Bit, DLCR6 bit 4 selects the SRAM buffer width. Secondly, the depth of the SRAM is programmed by setting Buffer Size 1 and 0 (BS1 and BS0), bits 1 and 0 in DLCR6. Depth selections are 8, 16, 32 or 64 kilobytes.

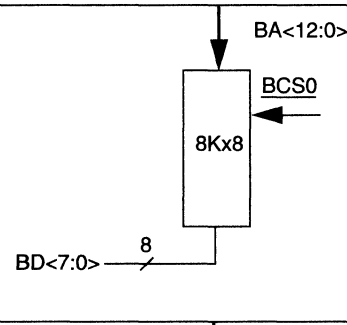
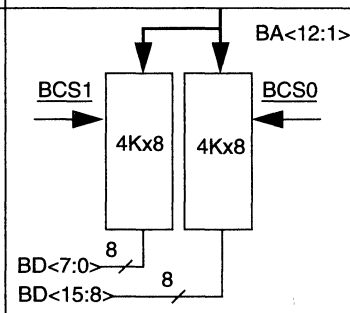
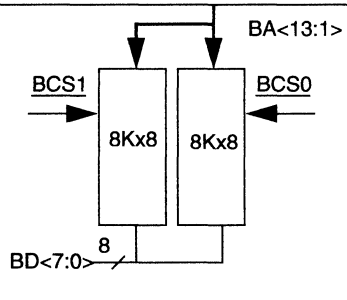
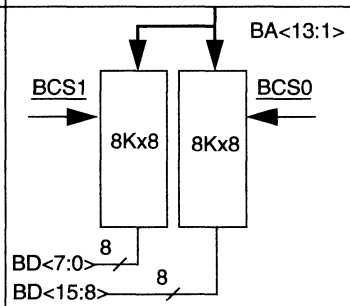
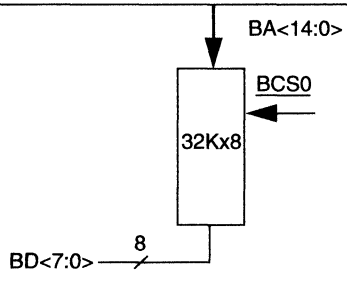
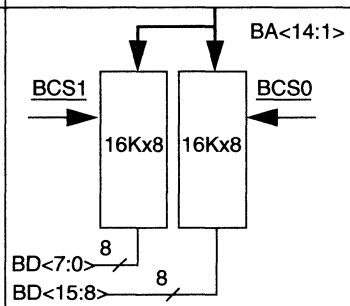
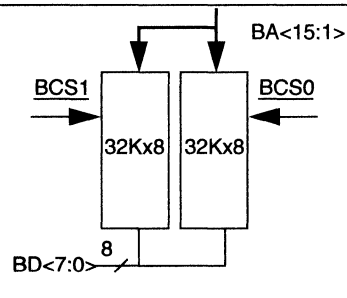
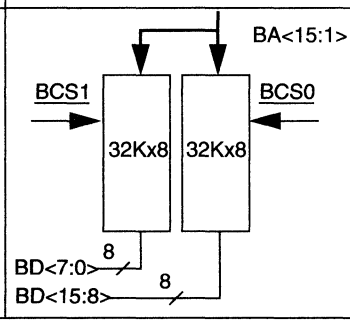
BS1 DLCR6<1>	BS0 DLCR<0>	8-BIT BUFFER BUS	16-BIT BUFFER BUS
0	0		
0	1		
1	0		
1	1		

Figure 4. SRAM Configuration

SB/SW	BB/BW	SYSTEM	BUFFER
0	0	word	word
0	1	word	byte
1	0	Do not use	
1	1	byte	byte

FUNCTIONAL DESCRIPTION

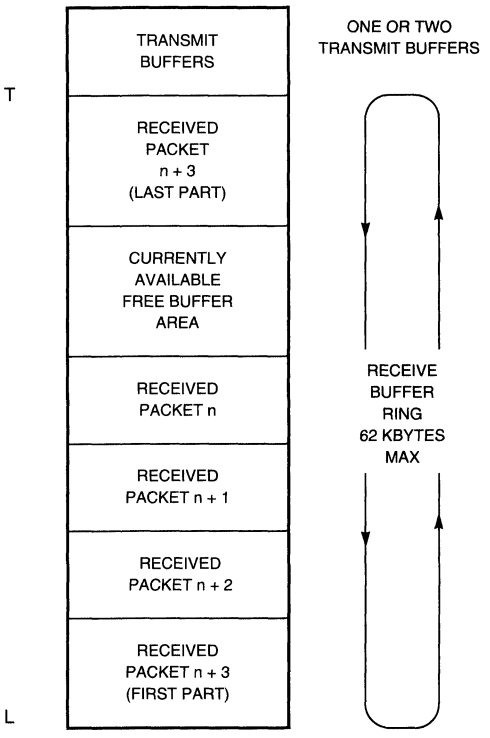
The MB86960 combines the functions of an Ethernet network controller with packet buffer management, and a 10 Mbit/s Manchester encoder/decoder. It consists of four major functional blocks: buffer controller, system interface, transmit controller with Manchester encoder, and receive controller with Manchester decoder.

The receive and transmit sections of the chip fully implement the ISO/ANSI/IEEE 8802–3 CSMA/CD specification for 10 Mbit/sec Ethernet. The transmitter assembles data packets for transmission and the receiver disassembles received data packets. Automatic generation and stripping of the 64-bit preamble, and generation and checking of the 32-bit CRC are provided on-chip. Other network functions provided on-chip include collision resolution by binary exponential backoff and re-transmission, several modes of address recognition, error detection and reporting, and serial/parallel and parallel/serial conversions.

BUFFER CONTROLLER

The MB86960 uses a dedicated buffer memory as shown in Figure 5 for intermediate storage of data packets to be transmitted, and of data packets received from the network. The buffer memory is connected directly to the controller rather than to a separate local microprocessor bus, thus eliminating the need for a local microprocessor. The buffer controller keeps track of buffer memory partitioning, allocation and updating of all receive and transmit pointers automatically, thus eliminating this task from software overhead. As a result of this automation and its high-performance packet buffering, the NICE controller can typically win benchmark performance tests over competing controllers.

Access to the buffer memory is managed by NICE's on-chip buffer controller. As required, it updates internal address pointers for the tasks of transmit, retransmit, receive, rejection of packets with errors and data transfers to and from the host. Thus the host is relieved of buffer management functions, making NICE easy to operate and substantially reducing software requirements. Packets with errors, such as CRC errors, are automatically rejected by NICE unless the host asserts the "accept bad packets" bit. When this bit is asserted, any packets received with alignment, CRC or short length errors are passed on to the host processor, and the appropriate error status bits are set to inform the host of the error. Similarly, by setting the "accept short packets" bit, reception of short packets down to 6 bytes in length is allowed. (Normal operation requires an IEEE minimum length packet of 60 bytes, excluding preamble and CRC.)



NOTES

1. Length (L) = 8, 16, 32, or 64 Kbytes.
2. Transmit Size (T) = 2 (one bank), 4 (two banks), 8 (two banks), or 16 (two banks) Kbytes.
3. Receive packets are aligned on an eight byte boundary.
4. Each received packet is preceded by a four byte packet header as follows:

   Byte 0 – Packet Status

   Byte 1 – Not Used

   Byte 2 – Packet Size LSB's

   Byte 3 – Packet Size MSB's

Figure 5. Buffer Memory Organization

As shown in Figure 5, the buffer memory is divided into transmit and receive buffer areas. The partitioning of the memory is programmable, allowing the system to be configured with different proportions of space available for the transmitter and receiver functions. By programming the proportions, an optimum usage of the memory can be selected, according to the demands of a particular application.

The section of the memory used by the transmitter can be configured as a single buffer 2 kilobytes long, or as a pair of banks, each either 2, 4 or 8 kilobytes long. Within each buffer or bank, one or more packets can be written by the system until the available space is too small for another packet. Once started, the transmitter will transmit all packets in the buffer automatically before finishing with a status update, and an interrupt if so enabled. With the two-bank configurations, one bank can be transmitted while the other is being loaded. Using dual buffers and loading multiple packets for "packet chaining" gives the highest rate of transmission. This will boost performance for systems that require high throughput transmission.

NICE can be configured to operate with 8, 16, 32 or 64 kilobytes of total buffer memory size, including both transmit and receive spaces. This memory partitioning into transmit and receive sections is allocated by the system software. The total size of the transmit buffer space can be either 2, 4, 8 or 16 kilobytes. Immediately following the transmit buffer space is the receive buffer space, using the balance of the available memory.

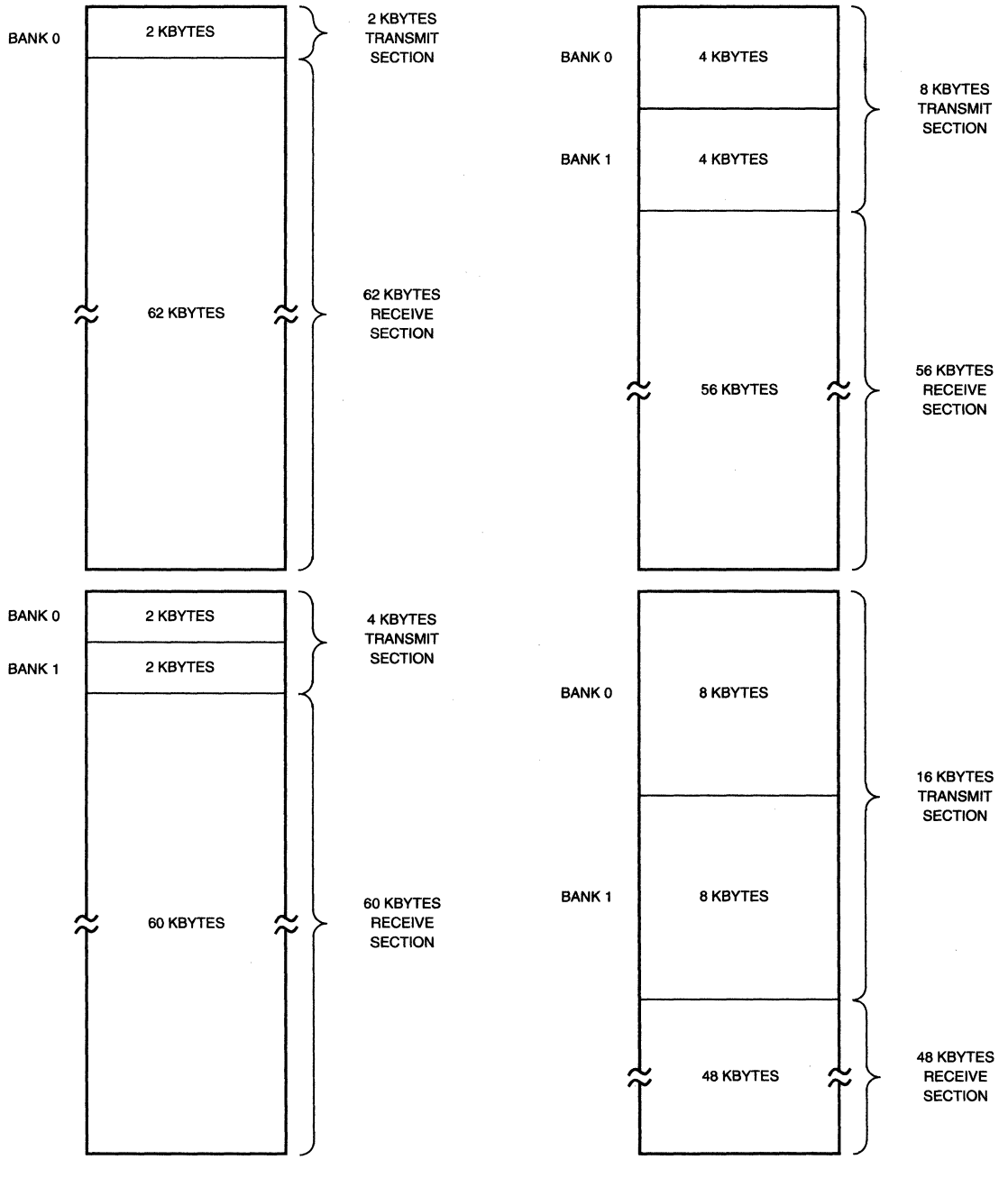


Figure 6. Transmit Buffer

As shown in Figure 6, the remaining memory not used for the transmitter is used for the receiver, and is automatically configured as a "ring buffer" by the chip. Packets are stored head-to-toe in the receive buffer, as they are in the transmit buffer. As packets are being stored in the receive buffer, as the end of the linear addressing space is reached, the chip's receive-write pointer automatically wraps around to the top of the receive addressing range to make a seamless ring. The receive-read pointer does the same as the packets are read out to the system. The MB86960 provides all the necessary buffer pointer management functions automatically, relieving the host system and its drivers of this time-consuming task. Since these tasks can be done faster in hardware than in software, this not only offloads the host system, but it also speeds up the communication processes giving higher throughput.

The buffer controller automatically prioritizes and services requests for access to the memory from the transmitter, the receiver, and the host system. It updates all buffer memory pointers, allocates memory space for incoming data packets, and controls pertinent bits within the status registers providing complete packet management functions.

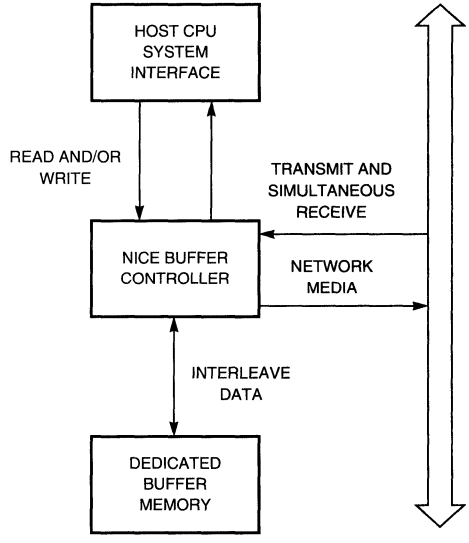


Figure 7. Simultaneous Operations and Buffer Control Capability of NICE

The NICE chip's arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory so that the operation appears to be "simultaneous": data can be written to or read from the buffer memory by the host via Buffer Memory Port Register 8 (BMPR8), while data packets are read out for transmission and/or written in for storage by the receiver. Each interface, whether host system or network access, appears to be served independently by the controller. Each interface has an associated FIFO to provide time for the buffer interleaving. Thus, packet data is "pipelined" through the system for highest performance and throughput, and the buffer controller supports all the cases of "simultaneous" access to the buffer memory, as illustrated in Figure 7 and as follows:

1. Data from the network is stored in the receive buffer.
2. The host retrieves packets from the receive buffer.
3. The host loads packet data into the transmit buffer.
4. The transmitter obtains data for transmission from the transmit buffer.
5. Any combination of the above can occur concurrently, including all four at once.

System Access to Buffer

NICE supports both programmed I/O, single cycle DMA and burst mode DMA transfers between the buffer memory and the host system. The host accesses the buffer memory by reading from or writing to NICE's Buffer Memory Port Register 8 (BMPR8). Data being read or written by the system passes through on-chip FIFO's to eliminate the effects of real-time interaction between the system, the transmitter and the receiver as they all access the buffer memory. All read and write operations to the external SRAM memory are controlled automatically by the NICE chip.

Transmitter Access to Buffer

The size of each of the transmit banks can be changed by programming the Buffer Size control bits, BS0 and BS1. The transmit buffer size is thus allocatable by the software to be a single 2-kilobyte transmit buffer, two 2-kilobyte transmit buffers, two 4-kilobyte transmit buffers, or two 8 kilobyte transmit buffers. In all configurations, a single packet or multiple packets can be loaded into the buffer at one time for transmission. When a single transmit buffer is used, the system and the transmitter time-share the use of the buffer. When two buffers are used, the system can load packets into one of the buffers while the contents of the other are being transmitted.

At reset, the pointers are initialized to point to the beginning of one of the transmit buffers. Each time the host writes data to the buffer via the Buffer Memory Port Register, an internal pointer is advanced to the next memory location within the transmit buffer. Once a data byte/word is written, it cannot be read and the internal pointer cannot be reversed.

Internal pointers managed by NICE control which of the two banks is selected for access by the host and which byte/word of the bank is accessed. NICE will switch banks as soon as the transmit start bit (TX START) of BMPR10 is written high by the host system. When this occurs, NICE will start transmitting at the earliest opportunity. Another automatically-managed pointer, the transmit-read pointer sequences through the bank being transmitted to read the packet data into the transmitter through its FIFO. If a collision occurs, the packet will be automatically retransmitted after a pseudo-random waiting interval called the backoff interval. If there are multiple packets in the bank, NICE will continue down the list, automatically transmitting them all. The details of this operation are described in the section on packet transmission.

NICE has the capability to transmit multiple back-to-back packets of varying legal Ethernet sizes to the LAN network. These packets may vary in length from 60 bytes to 1,514 bytes, excluding preamble and CRC fields. As shown in Figure 8, multiple packets can reside within one transmit bank, separated by a non-transmitted, two-byte header which provides the length of the packet in bytes. Upon reaching the end of the "list" or "chain" of packets, the transmitter will stop, update it's status bits and, if enabled, generate an interrupt.

Transmit Packet Data Formats

The packets to be transmitted, less preamble and CRC fields, are first loaded into the transmit buffer along with a two-byte header indicating the packet length in bytes. See Figure 8 for details. Multiple packets can be loaded at the same time provided there is room in the buffer. After the packets are loaded, the host initiates transmission by writing the number of packets just loaded into a register for this purpose on the chip. If the two-bank buffer configuration has been selected, the second bank can now be loaded with additional packets.

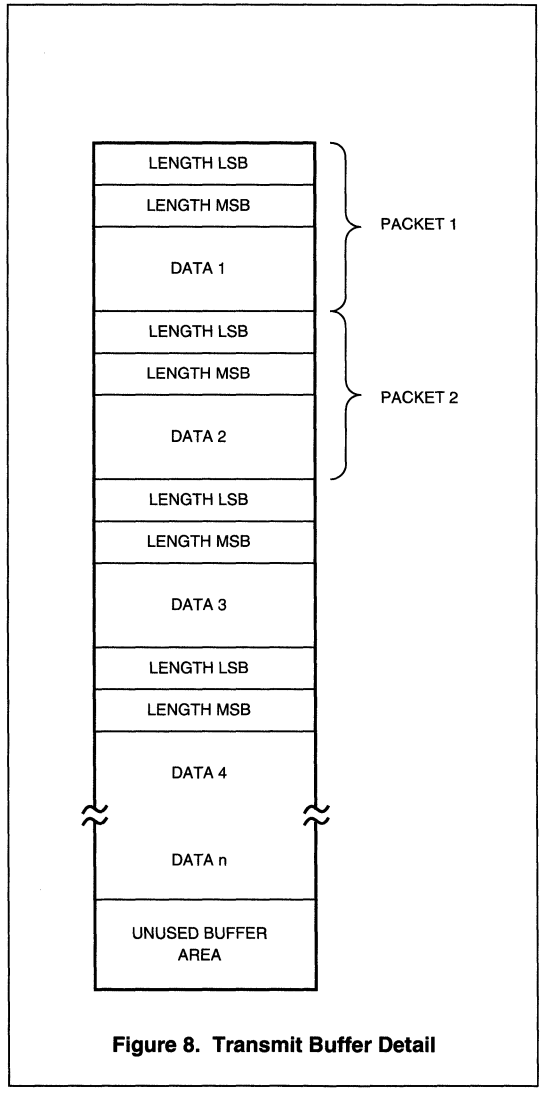


Figure 8. Transmit Buffer Detail

Receiver Access to Buffer

Once initialized and enabled, the receiver will automatically load any error-free incoming packets which pass the address filter into the receive buffer through an on-chip FIFO, appending a four-byte header to the front end which provides packet length and status. An interrupt can be provided to alert the host processor that a packet is available in the buffer. The host processor can read out receive packets as they become available. Continuous reception can continue as long as the receive buffer does not become full. If the host processor reads the receive packets from the buffer promptly, the buffer will not fill up. But if overflow does occur, an interrupt will be generated to indicate the problem. If this occurs, data should be read from the buffer to free space. As soon as space becomes available in the receive buffer, the receiver will automatically continue reception.

The receive buffer size can vary between a maximum of 62 kilobytes when 2 kilobytes is allocated for the transmit section and maximum memory size of 64 kilobytes is used, to a minimum of 4 kilobytes if 4 kilobytes is allocated for the transmit section and minimum memory size of 8 kilobytes is used. The receive section dynamically allocates space for each individual incoming data packet along an eight-byte "page" boundary. Each received packet is preceded by a four byte header which provides packet status and the length of that data packet. The data packets are linked or "chained" by internal pointers which use the length value in the packet header to calculate the length of the packet, and the starting address of the next packet. This buffer format is shown in Figure 9. Since NICE controls its dedicated buffer memory, FIFO size and depth are unimportant in this architecture, and need not be considered in system timing considerations.

A status bit in one of NICE's internal registers (RX BUF EMPTY) informs the host when one or more packets are resident in the receive buffer and available to be read. The host retrieves these packets from the buffer memory by successive reads of BMPR8. Once a data byte/word is read from the buffer memory, internal pointers are advanced to the next byte/word. As data is thus read by the system, that memory becomes available for reception of new packets. NICE automatically rejects an incoming packet if there is not enough buffer space to fully receive that packet. Therefore, there is no chance for packets already received to be "overrun" by incoming packets.

When DLCR5<5>, the ACPT BAD PKTS ("accept bad packets") bit is set to a "0" (disabled), a bad incoming packet causes NICE to release buffer space in which that packet is contained and reset its internal pointers so as to use that space for the next incoming packet. If this bit is set to a "1", the packet with a short length, alignment or CRC error will be accepted and the appropriate error bits in the status field of its header will be set. The same applies to DLCR5<3>, ACPT SHORT PKTS, which when high allows retention of packets below 60 bytes in length, excluding preamble and CRC (shorter than IEEE 802.3 minimum size).

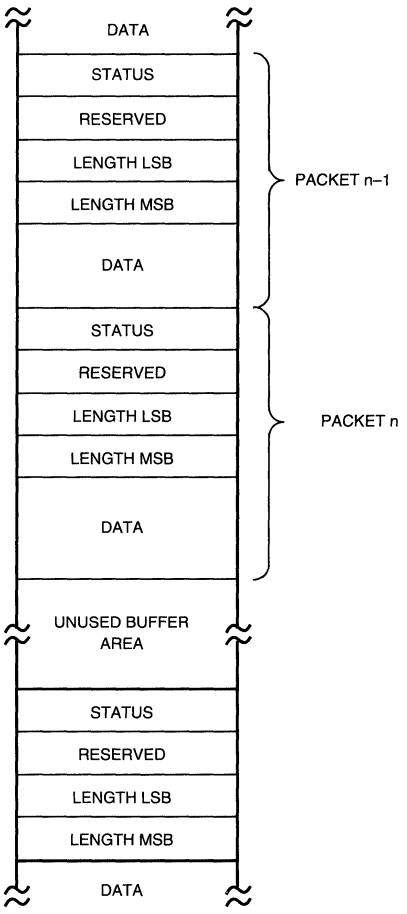


Figure 9. Receive Buffer Detail

Receive Packet Data Formats

Receive packets, less preamble and CRC fields, are stored in the buffer along with a four-byte header. The first byte gives status information, indicating errors, if any, that occurred during reception of the packet. Normally packets with errors are automatically discarded and eliminated from memory by the chip, but with a mode selection, the chip can allow reception of bad packets, with indication of their errors in the status byte of the header. The second byte of the header is reserved for possible future use. The last two bytes of the header give the byte count of the packet, less preamble and CRC. Refer to Figure 9.

SYSTEM INTERFACE

The system interface block provides the connection between NICE and the host CPU. NICE supports both 8-bit and 16-bit bus widths and byte or word transfers as determined by DLCR6<5>, SB/SW, the "system byte or system word" configuration bit. Depending on the type of host CPU, NICE will supply the data order, MSB or LSB first according to the setting of DCLR7<0> as described in the detailed register descriptions. NICE supports I/O-mapping, memory mapping, and burst or single transfer DMA modes. An interrupt output, INT, is provided which may be programmed by the user to inform the CPU of transmit and receive status conditions requiring host processing.

Three sets of user-accessible registers are contained within the MB86960. All registers are accessible as bytes or words.

Register Access

All control and status registers on the NICE chip are accessible through its bus interface port, which can be I/O or memory mapped in the system. Eight of the registers in the set, whose addresses are xxx0H through xxx7H, are always directly accessible. For the remaining physical addresses, three different banks of registers can be accessed through indirect addressing of the banks (bank switching). The bank switching bits are part of the first eight registers which are permanently resident.

The bank-switched register group consists of three sets or "banks" of registers. One of the sets is for Node ID (Ethernet Address) and TDR diagnostics, another is the Hash Table for multicast address filtering, and the third is for buffer memory access. This third bank is normally selected most of the time, except during initialization or diagnostic routines, as access to the other registers is not needed during normal operation.

Buffer Access

Buffer Memory Port Register 8 (BMPR<8>) of the buffer memory port register set provides serial access to the receive and transmit buffers through on-chip FIFO's. This port can be accessed with 8-bit or 16-bit wide data. There is a separate FIFO for each direction of data transfer, so there is no complicated direction control needed. Writes to the transmit buffer can be interleaved with reads from the receive buffer if desired. All buffer memory pointers are automatically maintained by the chip, eliminating software overhead normally needed for this.

This port can be accessed with I/O instructions using register address xxx8H, or by using DMA. In the latter case, assertion of the DACK input is sufficient to select the port. Thus data can be transferred from host memory to the transmit buffer, or from the receive buffer to host memory using CPU string moves, single-transfer programmed I/O moves, or DMA. The choice should be made according to which is most efficient at a system level, taking into account that a speedy transfer process will result in the best performance. A slow transfer process may not be satisfactory because it might result in poor throughput and performance, and might allow the receive buffer to overflow, losing packets.

DMA Operation

The MB86960 supports both single cycle and burst DMA operation for transfers of data between the host system and the dedicated buffer memory. The DREQ and DACK signals are used for handshaking between the external DMA and NICE. There is also an "end of process" input pin which, when asserted by the system DMA controller during a transfer cycle, will terminate the DMA activity after the current cycle completes. If enabled for DMA interrupt, upon completion of the DMA activity, the chip will generate an interrupt.

Usually only one DMA operation will be run at a time, although the NICE chip could run two interleaving operations, one reading and one writing. There is only one DMA EOP bit, and only one DREQ pin and one DACK pin, so most hosts could not support more than one DMA operation at a time with NICE.

DMA Write (Transmit)

Transmit DMA Enable, TX DMA EN, BMPR12<0>, is set high to enable DMA operation for transfers of data packets from the host memory to NICE's transmit buffer. Burst transfers can also be enabled by invoking the DMA burst control register BMPR13<1:0>. When NICE is ready to begin to accept data from the host, NICE will assert its DMA request output, DREQ. The host responds by asserting DMA Acknowledge, DACK, followed by write enable, WE, and placing the data on the data bus. NICE will assert its RDY(RDY) output when it is ready to complete the current data transfer cycle (polarity of RDY(RDY) and EOP(EOP) inputs are independently programmable). NICE accepts that data byte/word into its bus write FIFO, and later moves it into buffer memory. At the close of a transfer cycle, the host negates WE. In burst mode, NICE will negate DREQ two cycles before the end of the burst. The host DMA will then complete the last two transfer cycles, then negate DACK to close the burst. To start another burst, NICE will re-assert DREQ. The number of DMA write cycles within one burst can be 1, 4, 8, or 12 data transfers (bytes or words) depending on the burst control bits BURST1, BURST0, BMPR13<1:0>.

The DMA controller may assert the end-of-process input, EOP(EOP), concurrently with the last data transfer cycle to indicate that the entire transfer process has been completed. This sets the DMA EOP bit in NICE which causes NICE to discontinue making further data requests. If enabled, the EOP(EOP) signal assertion can also generate an interrupt. When the DMA EOP bit, DLCR1<5>, is set, the INT pin will assert if DLCR3<5>, interrupt enable for DMA EOP, is high. This interrupt can be used by the host to initiate the actions for closing the process. Upon servicing the interrupt, if DMA EOP is high, the host should close the DMA process, reset the NICE chip's DMA logic and clear the interrupt by writing 00H to BMPR12. *Note: Clearing TX DMA EN must be done to close the transmit DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, so it is not necessary to clear the interrupt separately.*

After finishing the loading of packets into the buffer, the host initiates packet transmission. This is done by loading the number of packets to be transmitted into the Transmit Packet Count Register, BMPR10<6:0>, and asserting the Transmit Start bit, TX START, of the same register, BMPR10<7>.

DMA Read (Receive)

NICE will indicate when it has receive packets to be read with status bits and/or interrupts. Before attempting to read a packet, the host processor first reads the RX BUF EMPTY bit, DLCR5<6>. If this bit is 0, there are one or more packets in the receive buffer to read. After reading each packet, the host will check this bit again to see if there are more.

Prior to beginning the transfer of a packet from NICE's receive buffer to host memory via DMA, the host must first read the four-byte receive packet header from the buffer to obtain the packet status and the length of the packet in bytes. Calculating from the packet length the number of DMA cycles needed to read the packet, the host will load that number into the cycle counter of the host DMA controller. The starting address in system memory will also be loaded into the DMA controller. Next, RX DMA EN, BMPR12<1>, is set high to enable DMA read operation to transfer the packet to host memory. When it is ready to begin, NICE asserts its DMA Request output, DREQ. The host responds by asserting DMA Acknowledge, DACK, followed by Read Enable, RD. NICE will assert its RDY output when it has placed the byte/word on the data bus and is ready to complete the data transfer cycle. The system memory will accept the data, then the host negates RD. NICE shifts the data down into its bus read FIFO, then moves its internal bus read pointer to point to the next byte/word in the buffer, moving it into the FIFO.

NICE will negate DREQ two cycles before the end of the burst. After the host negates DACK, if NICE can transfer more data, NICE will re-assert DREQ to repeat the process. The number of DMA read cycles in a burst can be 1, 4, 8, or 12 transfer cycles of data (bytes or words), depending on the burst control bits BURST1, BURST0, BMPR13<1:0>. The DMA controller may assert the end-of-process input, EOP(EOP), concurrently with the last byte/word data transfer to indicate that the entire process has completed. NICE will then discontinue making further data requests. RX DMA EN must be cleared when the DMA process is completed, and set again when the host desires to begin reading another packet from the receive buffer using DMA.

When EOP(EOP) is asserted by the host DMA controller, the DMA EOP bit, DLCR1<5>, will be set high, and an interrupt will also be generated, provided it is enabled by a high, DLCR3<5>. This interrupt can be used by the host to initiate the final actions to close the DMA process. The interrupt is cleared and the DMA is disabled and reset by writing 00H to the DMA Enable Register, BMPR12. *Note: Clearing RX DMA EN must*

be done to close the receive DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, so it is not necessary to clear the interrupt separately.

CONTROL AND STATUS REGISTERS

The control and status registers on the NICE chip are accessed through direct register addresses xxx0H through xxxFH, and indirect or bank-switching address bits RBS1, RBS0, DLCR7<3:0>. Table 1 summarizes the addressing scheme. In system word mode, data can be transferred 16-bits at a time on the system bus, or 8-bits at a time by using the byte lane controls of NICE. When transferring in 16-bit mode to/from the registers, even direct addresses are used to select the registers. For example, to access the Transmit/Receive Status Registers, address xxx0H would be used. The transmit status would be on the low byte and the receive status on the high byte. Separate access of high and low bytes is achieved by using the appropriate byte-access processor instructions.

Table 1. Internal Register Address Map

RBS1,RBS0	SA3	SA2	SA1	SA0	ADDRESS	DESCRIPTION
XX	0	0	0	0	DLCR0[1]	TRANSMIT STATUS
XX	0	0	0	1	DLCR1	RECEIVE STATUS
XX	0	0	1	0	DLCR2	TRANSMIT INT ENABLE
XX	0	0	1	1	DLCR3	RECEIVE INT ENABLE
XX	0	1	0	0	DLCR4	TRANSMIT MODE
XX	0	1	0	1	DLCR5	RECEIVE MODE
XX	0	1	1	0	DLCR6	CONFIG 0
XX	0	1	1	1	DLCR7	CONFIG 1
00	1	0	0	0	DLCR8	NODE ID 0
00	1	0	0	1	DLCR9	NODE ID 1
00	1	0	1	0	DLCR10	NODE ID 2
00	1	0	1	1	DLCR11	NODE ID 3
00	1	1	0	0	DLCR12	NODE ID 4
00	1	1	0	1	DLCR13	NODE ID 5
00	1	1	1	0	DLCR14	TDR 0 (LSB)
00	1	1	1	1	DLCR15	TDR 1 (MSB)
01	1	0	0	0	HT8	HASH TABLE 0
01	1	0	0	1	HT9	HASH TABLE 1
01	1	0	1	0	HT10	HASH TABLE 2
01	1	0	1	1	HT11	HASH TABLE 3
01	1	1	0	0	HT12	HASH TABLE 4
01	1	1	0	1	HT13	HASH TABLE 5
01	1	1	1	0	HT14	HASH TABLE 6
01	1	1	1	1	HT15	HASH TABLE 7
10	1	0	0	0	BMPR8[2]	BUFFER MEMORY PORT
10	1	0	0	1	BMPR9	RESERVED
10	1	0	1	0	BMPR10	TRANSMIT START
10	1	0	1	1	BMPR11	16 COLLISIONS
10	1	1	0	0	BMPR12	DMA ENABLE
10	1	1	0	1	BMPR13	DMA BURST
10	1	1	1	0	BMPR14	SKIP PACKET
10	1	1	1	1	BMPR15	RESERVED
11	X	X	X	X	—	RESERVED

1. All registers are both word and byte accessible. In word mode, register bytes are paired to form words starting with registers 0 and 1. The odd-addressed byte becomes the high byte of the word
2. In word mode, BMPR8 is a 16-bit port. In byte mode, it is an 8-bit port. The byte ordering Is determined by DLCR7<0>

Table 2. Summary of Control and Status Bits: DLCR0–7, BMPR8–15

Register	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX STATUS DLCR0	TX DONE	NET BSY	TX-RX	CR LOST	0	COL	16 COL	0
RX STATUS DLCR1	RX PKT	BUS RD ERR	DMA EOP	RMT 0900H	SHORT ERR	ALIGN ERR	CRC ERR	RX BUF OVERFLO
TX INT ENABLE DLCR2	INT EN	0	0	0	0	INT EN	INT EN	0
RX INT ENABLE DLCR3	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN
TX MODE DLCR 4	COL CTR 3	COL CTR 2	COL CTR 1	COL CTR 0	0	CNTRL	LBC	EN TX DEFER
RX MODE DLCR5	0	RX BUF EMPTY	ACPT BAD PKTS	40 BIT ADDR	ACPT SHORT PKTS	1	AF1	AF0
CONFIG0 DLCR6	DLC EN	1	SB/SW	BB/BW	TBS 1	TBS 0	BS 1	BS 0
CONFIG1 DLCR7	E/D CNF 1	E/D CNF 0	PWRDN	RDYPOL	RBS 1	RBS 0	EOPPOL	M..L/ L..M
BUF MEM PORT BMPR8	7	6	5	4	3	2	1	0
BUF MEM PORT BMPR9	15	14	13	12	11	10	9	8
TX START BMPR10	TX START	TX PKT CNT 6	TX PKT CNT 5	TX PKT CNT 4	TX PKT CNT 3	TX PKT CNT 2	TX PKT CNT 1	TX PKT CNT 0
16 COLLISIONS BMPR11	0	0	0	0	0	16 COL CNTRL 2	16 COL CNTRL 1	16 COL CNTRL 0
DMA ENABLE BMPR12	0	0	0	0	0	0	RX DMA ENABLE	TX DMA ENABLE
DMA BURST BMPR13	0	0	0	0	0	0	BURST 1	BURST 0
SKIP PACKET BMPR14	0	0	0	0	0	SKIP PKT	0	0
RESERVED BMPR15	0	0	0	0	0	0	0	0

Table 3. Summary of Control and StatusBits:DLCR8–15, HT8–15, Packet Buffer Headers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NODE ID 0 DLCR8	7	6	5	4	3	2	1	0
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
NODE ID 5 DLCR13	47	46	45	44	43	42	41	40
TDR 0 DLCR14	7	6	5	4	3	2	1	0
TDR1 DLCR15	N/A (0)	N/A (0)	13	12	11	10	9	8
HASH TABLE 0 HT8	7	6	5	4	3	2	1	0
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
HAST TABLE 7 HT15	63	62	61	60	59	58	57	56
TX LENGTH LSB (TX HEADER 0)	7	6	5	4	3	2	1	0
TX LENGTH MSB (TX HEADER 1)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8
PKT STATUS (RX HEADER 0)	N/A (0)	N/A (0)	GOOD PKT	RMT 0900H	SHORT ERR	ALIGN ERR	CRC ERR	RBUF OVRFLO
RESERVED (RX HEADER 1)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)
RX LENGTH LSB (RX HEADER 2)	7	6	5	4	3	2	1	0
RX LENGTH MSB (RX HEADER 3)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8

Type Descriptions (TYPE)

The following legend of descriptions applies to the type column of the register bit description tables:

R: Readable bit

W: Writable bit

C: Clears associated status bit and/or interrupt when 1 is written; no effect when 0 is written

N: Not used; reserved; write only 0 when written

0/1: Initial state after hardware reset

DATA LINK CONTROL REGISTERS

Status and control bits for the transmitter and receiver sections of the NICE chip are located in the first eight data link control registers, DLCR0–7. See Tables 4–11 for details.

Transmit Status Register

This register provides transmit status for the host processor. The system can enable interrupts based on the assertion (going high) of bits 7, 2, and/or 1 of this register by setting the corresponding enable bits in the Transmit Interrupt Enable register. See Table 4.

Bits 7, 2 and 1 in this register, the bits that can generate interrupts, are cleared by writing 1 to the bit. Writing 0 to the bit has no effect, only the NICE chip control logic can set these bits. Clearing the bit that caused the interrupt will clear both the bit itself and the interrupt. Since two or more status conditions can occur at one time, the interrupt routine must read all of them and act on all of those that are set.

One method for clearing interrupts is to read the contents of the status register, then write the same value back to the register, thus clearing all bits which were set. Another technique is to clear each status bit separately by writing its mask to the register. This might be done as the corresponding interrupt service is performed. *Note: Wholesale clearing of all status bits by writing FFH to the register is not recommended, since this may clear status which has just been set and not yet read by the system. The transmitter must be idle and TX DONE, DLCR0<7>, must be cleared by writing 1 to it before starting the transmitter (by writing 1 to TX START, BMPR10<7>).*

Table 4. DLCR0—Transmit Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX DONE	R C 0	**TRANSMIT DONE:** This bit is set high when all packets in the active transmit buffer have been successfully transmitted to the LAN media, or skipped due to excessive collisions. Can generate interrupt if enabled by DLCR2<7>.
6	NET BSY	R	**NET BUSY:** This is a real-time image of the Carrier Sense signal of the receiver.
5	TX-RX	R 0	**TRANSMIT PACKET RECEIVED:** Indicates that a good packet was received by NICE shortly after transmission was completed. This is used to indicate self-reception of the packet. This bit is cleared as each transmission begins.
4	CR LOST	R 0	**CARRIER LOST:** This bit is set if the receive carrier sense input is negated during a packet transmission. This can be caused by a collision or a shorted LAN medium. It is automatically cleared as each transmission begins.
3	0	N 0	**RESERVED:** Write 0.
2	COL	R C 0	**COLLISION:** This bit will assert during transmission of a data packet if a collision occurs on the network. The buffer controller will automatically retransmit the current packet after collisions up to 15 times. The user may read the number of consecutive collisions in the collision counter, DLCR4<7:4>. Can generate interrupt if enabled by DLCR2<2>.
1	16 COL	R C 0	**16 COLLISIONS:** This bit is set after the sixteenth unsuccessful transmission of the same packet. Can generate interrupt if enabled by DLCR2<1>.
0	0	R O	**RESERVED:** Write 0.

Receive Status Register

This register contains eight status bits which can generate interrupts if enabled by the corresponding bit in DLCR3. Five of these bits report the status of the most recently received packet that was accepted for storage in the receive buffer. Bit 7, RX PKT, is set whenever a new packet is successfully received and stored in the buffer. One bit reports reception of a special packet with 0900H in its 'type' field. Other bits in this register report buffer overflow, DMA end-of-process and bus read error. Bits 1, 2 and 3 indicate errors, if any, detected in the packet. If ACPT BAD PKTS, DCLR5<5> and/or ACPT SHORT PKTS, DLCR5<3> are set to 1 allowing acceptance of a bad packet, these error bits will be stored in the status byte of the receive packet header. If DLCR5<5> and DLCR5<3> are both 0, all packets with detected errors will be discarded automatically, and removed from the buffer.

The bits in this register are cleared by writing 1 to the bit. Writing 0 to the bit has no effect. Only the NICE chip control logic can set these bits. Clearing the bit that caused the interrupt will clear both the bit itself and the interrupt. Since two or more status conditions can occur at one time, the interrupt routine must read all of them and act on all of those that are set. See Table 5.

One method for clearing interrupts is to read the contents of the Transmit and Receive Status Registers, then write the same value back to the registers, thus clearing all bits which were set. Another technique is to clear each status bit separately by writing its mask to the register as the corresponding interrupt service is performed. *Note: Wholesale clearing of all status bits by writing FFH to the register is not recommended, since this may clear status which has just been set and not yet read by the system.*

Table 5. DLCR1—Receive Status Register

BIT	SRMBOL	TYPE	DESCRIPTION
7	RX PKT	R C 0	**RECEIVE PACKET:** Set when a new receive packet is stored in the Receive Buffer. Can generate interrupt if enabled by DLCR3<7>.
6	BUS RD ERR	R C 0	**BUS READ ERROR:** Set when a ready response cannot be issued within 2.4 s after the RD signal is asserted. Occurs when reading an empty buffer. Can generate interrupt if enabled by DLCR3<6>.
5	DMA EOP	R C 0	**DMA END OF PROCESS:** Set when the host DMA asserts the EOP pin indicating that the process is finished. When set, inhibits further assertion of DREQ. Cleared by writing 00H to BMPR12. *Do not clear by writing 1 to this bit as this may result in unwanted DREQ.* Can generate interrupt if enabled by DLCR3<5>.
4	RMT 0900H	R C 0	**REMOTE CONTROL PACKET RECEIVED:** This bit is set if a packet is received with 0900H in its Length/Type Field (two bytes following the source address, received MSB first). Can generate interrupt if enabled by DLCR3<4>.
3	SHORT ERR	R C 0	**SHORT PACKET ERROR:** Set when a packet is received with less than 60 bytes, excluding its Preamble and CRC fields. Such a packet usually indicates a collision has truncated its original length, since IEEE 802.3 minimum length is 60 bytes. Can generate interrupt if enabled by DLCR3<3>. See also Table 8.
2	ALIGN ERR	R C 0	**ALIGNMENT PACKET ERROR:** This bit will assert if a packet is received with an alignment error, meaning there were 1 to 7 extra bits at the end of the packet. Such an occurrence usually indicates a collision, or a faulty transceiver. Can generate interrupt if enabled by DLCR3<2>. See also Table 8.
1	CRC ERR	R C 0	**CRC PACKET ERROR:** This bit is set if a packet is received with a CRC error. This usually indicates a collision has corrupted the packet. Can generate interrupt if enabled by DLCR3<1>. See also Table 8.
0	RX BUF OVRFLO	R C 0	**RECEIVE BUFFER OVERFLOW:** This bit will be set if the receive buffer becomes full and must reject a packet for lack of space. Can generate interrupt if enabled by DLCR3<0>. Does not get set in loopback mode.

Transmit Interrupt Enable Register

This register contains the bits which enable or mask the status bits in DLCR0 from generating interrupts. Only bits 7, 2 and 1 can generate interrupts. The other bits are not used. See Table 6.

Table 6. DLCR2—Transmit Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables TX DONE to generate interrupt. See also DLCR0<7>.
6	0	N 0	**RESERVED:** Write 0.
5	INT EN	N 0	**RESERVED:** Write 0.
4	0	N 0	**RESERVED:** Write 0.
3	0	N 0	**RESERVED:** Write 0.
2	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables COL to generate interrupt. See also DLCR0<2>.
1	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables 16 COL to generate interrupt. See also DLCR0<1>.
0	0	N 0	**RESERVED:** Write 0.

Receive Interrupt Enable Register

This register provides control for enabling or masking interrupts based on the assertion of status bits in DCLR1, the Receive Status Register. See Table 7.

Transmit Mode Register

This register contains two control bits associated with transmission, a general-purpose control bit which drives a pin on the chip, and a collision counter. See Table 9.

Table 7. DLCR3—Receive Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables RX PKT to generate interrupt. See also DLCR1<7>.
6	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables BUS RD ERR to generate interrupt. See also DLCR1<6>.
5	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables DMA EOP to generate interrupt. See also DLCR1<5>.
4	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables RMT 0900H to generate interrupt. See also DLCR1<4>.
3	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables SHORT ERR to generate interrupt. See also DLCR1<3> and Table 8.
2	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables ALIGN ERR to generate interrupt. See also DLCR1<2> and Table 8.
1	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables CRC ERR to generate interrupt. See also DLCR1<1> and Table 8.
0	INT EN	R W 0	**INTERRUPT ENABLE:** When high, enables RBUF OVRFLO to generate interrupt. See also DLCR1<0>.

Table 8. Network Error Monitoring Modes

ACPT BAD PKTS DLCR5<5>	ACPT SHORT PKTS DLCR5<3>	INT EN SHORT ERRORS DLCR3<3>	INT EN ALIGN ERRORS DLCR3<2>	INT EN CRC ERRORS DLCR3<1>	Mode Description
0	0	0	0	0	Normal non-monitor mode.
0	0	1/0	1/0	1/0	Error interrupts only, if enabled.
0	1	0	1/0	1/0	Save short packets if otherwise error free in buffer; interrupts only for alignment and CRC errors, if enabled. RX PKT will be set high if short packet received.
1	0	0	0	0	Save packets with short, alignment and/or CRC errors in buffer; RX PKT will be set high if packet with error received.
All others					Do Not Use.

Note: Packet acceptance requires both error filter acceptance and address filter acceptance.

Table 9. DLCR4—Transmit Mode Register

BITF	SYMBOL	TYPE	DESCRIPTION
7	COL CTR 3	R 1	**COLLISON COUNT 3:** DLCR4<7:4> plus 1 indicates the number of consecutive collisions encountered by the current transmit packet. (Read only). See Table 10.
6	COL CTR 2	R 1	**COLLISON COUNT 2:** DLCR4<7:4> plus 1 indicates the number of consecutive collisions encountered by the current transmit packet. (Read only). See Table 10.
5	COL CTR 1	R 1	**COLLISON COUNT 1:** DLCR4<7:4> plus 1 indicates the number of consecutive collisions encountered by the current transmit packet. (Read only). See Table 10.
4	COL CTR 0	R 1	**COLLISON COUNT 0:** DLCR4<7:4> plus 1 indicates the number of consecutive collisions encountered by the current transmit packet. (Read only). See Table 10.
3	0	N 0	**RESERVED:** Write 0.
2	CNTRL	R W 1	**CONTROL OUTPUT:** The inverse of this bit is output for general use on pin 95.
1	LBC	R W 1	**LOOPBACK CONTROL:** This bit controls the loopback function of the NICE encoder/ decoder. A 0 in this bit places the chip in internal loopback mode.
0	EN TX DEFER	R W 0	**ENABLE TRANSMIT DEFER:** Program this bit low for normal network operation. When high, the transmitter will not defer to traffic on the network.

Table 10. Collision Count

Collision Count	16 COL DLCR0<1>	DLCR4<7>	DLCR4<6>	DLCR4<5>	DLCR4<4>	COL DLCR0<2>
0	0	0	0	0	0	0
1	0	0	0	0	1	1
2	0	0	0	1	0	1
3	0	0	0	1	1	1
. . .	. . .	. . .	. . .	. . .	. . .	. . .
15	0	1	1	1	1	1
16	1	0	0	0	0	1

Receive Mode Register

This register contains six bits which control receiver function, and one receive buffer status bit. See Table 11.

The status bit, RX BUF EMPTY (Receive Buffer Empty), is very important to the software routine which reads receive packets from the buffer. It tells the host routine whether there are any packets in the receive buffer which are complete and ready to read. In a multitasking system, this indicator would be used in conjunction with an interrupt when RX PKT asserts, which means a packet has arrived in memory. The interrupt would be used to start the routine which reads packets from the buffer. As this routine begins, the interrupt on RX PKT can be disabled to prevent unneeded interrupts. After the first packet is read from the buffer, the RX BUF EMPTY bit would be read to see if any more packets have come in (packets may, at times, arrive in bursts). If the buffer is not empty, another packet would be read out, and this procedure repeated until the buffer is empty. After emptying the buffer, the host clears RX PKT, then re-enables interrupts on RX PKT, checks the buffer status one more time (since a packet can come in at any time), then exits to do other tasks.

Two of the control bits allow reception of packets with certain types of errors. The ACPT BAD PKTS bit, when set, causes the receiver to retain and store in the buffer packets with CRC, alignment and/or short length errors provided there was no indication of collision during reception. Likewise, the ACPT SHORT PKTS bit, when set, allows the retention of short packets down to and including only six bytes in length, excluding preamble and CRC, provided there was no indication of collision during reception and no alignment or CRC error. Under normal operation, packets with less than 60 bytes, the IEEE 802.3 lower limit, would be discarded. These functions are provided for diagnostic purposes. Packets are accepted only if both the address filter and the error filter are passed. Packets with no content errors, i.e., short, alignment or CRC, are accepted without regard to collision indicators.

Table 11. DLCR5—Receive Mode Register

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>0</td><td>N
0</td><td>RESERVED: Write 0.</td></tr>
<tr><td>6</td><td>RX BUF EMTY</td><td>R
1</td><td>RECEIVE BUFFER EMPTY: Status bit which indicates that the receive buffer does not have any complete packets to read. (Read only).</td></tr>
<tr><td>5</td><td>ACPT BAD PKTS</td><td>R
W
0</td><td>ACCEPT PACKETS WITH ERRORS: When set high, allows packets with CRC, alignment and/or short length errors to be saved into the receive buffer for analysis, provided there was no indication of collision during reception. Otherwise such packets would be discarded automatically by the receiver and removed from the buffer. See also Table 8.</td></tr>
<tr><td>4</td><td>40 BIT ADDR</td><td>R
W
0</td><td>40 BIT ADDRESS: When set high, instead of the customary 48-bit NODE ID address filter, only the first 40 bits of the NODE ID are compared (NODE ID 0–4).</td></tr>
<tr><td>3</td><td>ACPT SHORT PKTS</td><td>R
W
0</td><td>ACCEPT SHORT PACKETS: When set high, allows short packets (packets with less than 60 bytes, excluding Preamble and CRC, i.e. below IEEE minimum length) down to 6 bytes, excluding preamble and CRC, to be saved into the receive buffer, provided there was no CRC or alignment error and no indication of collision during reception. Otherwise such packets would be discarded automatically by the receiver and removed from the buffer. See also Table 8.</td></tr>
<tr><td>2</td><td>1</td><td>N
0</td><td>RESERVED: Write 1.</td></tr>
<tr><td>1</td><td>AF1</td><td>R
W
0</td><td>ADDRESS FILTER MODE: AF1 and AF0, DLCR5<1:0>, control the address filtering on incoming packets. See table below under AF0.</td></tr>
<tr><td>0</td><td>AF0</td><td>R
W
1</td><td>ADDRESS FILTER MODE: AF1 and AF0, DLCR5<1:0>, control the address filtering on incoming packets:
<table>
<tr><th>AF1</th><th>AF0</th><th>Description of Addresses Accepted</th></tr>
<tr><td>0</td><td>1</td><td>NODE ID, Broadcast, Multicast & 2nd–24th bits of NODE ID</td></tr>
<tr><td>1</td><td>0</td><td>NODE ID, Broadcast, Multicast & Hash Table</td></tr>
<tr><td>0</td><td>0</td><td>Reject all packets</td></tr>
<tr><td>1</td><td>1</td><td>Accept all packets</td></tr>
</table>
Note: Self reception of broadcast and multicast packets prohibited except in “Accept all packets” mode. When LBC is low (loopback mode) broadcast packets can be self-received, except in “Reject all packets” mode.</td></tr>
</table>

Configuration Registers 0 and 1

Basic system configuration bits are found in these two registers. Among the configuration controls found here are physical packet buffer memory size, partitioning between transmit and receive buffers, widths of memory and system buses, byte lane control, chip configuration and power down control. Most of these configuration parameters will be programmed only during initialization after power start and hardware reset. See Tables 12 and 13.

Table 12. DLCR6—Configuration Register 0

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>DLC EN</td><td>R
W
1</td><td>ENABLE DATA LINK CONTROLLER: When low, enables the receiver and transmitter sections of the NICE chip. This bit must be set high during initialization and later set low to enable loopback testing and operation of the network. Program NODE ID only when this bit is high.</td></tr>
<tr><td>6</td><td>1</td><td>N
0</td><td>RESERVED: Write 1.</td></tr>
<tr><td>5</td><td>SB/SW</td><td>R
W
1</td><td>SYSTEM BYTE/WORD BUS WIDTH: When high, system bus will operate in 8-bit data mode; when low, 16-bit data mode is selected. See also BB/BW below.</td></tr>
<tr><td>4</td><td>BB/BW</td><td>R
W
1</td><td>BUFFER BYTE/WORK WIDTH: When high, buffer memory will operate in 8-bit data mode; when low, 16-bit data mode is selected. See table for allowable combinations with SB/SW:
<table>
<tr><th>SB/SW</th><th>BB/BW</th><th>SYSTEM</th><th>BUFFER</th></tr>
<tr><td>0</td><td>0</td><td>word</td><td>word</td></tr>
<tr><td>0</td><td>1</td><td>word</td><td>byte</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Do not use</td></tr>
<tr><td>1</td><td>1</td><td>byte</td><td>byte</td></tr>
</table></td></tr>
<tr><td>3, 2</td><td>TBS 1, 0</td><td>R
W
01</td><td>TRANSMIT BUFFER SIZE: Selects size of Transmit Buffer(s). See table:
<table>
<tr><th>TBS
1,0</th><th>No. TX
BUFS</th><th>Size each
TX BUF</th><th>Total Size
TX BUF</th></tr>
<tr><td>00</td><td>1</td><td>2KB</td><td>2KB</td></tr>
<tr><td>01</td><td>2</td><td>2KB</td><td>4KB</td></tr>
<tr><td>10</td><td>2</td><td>4KB</td><td>8KB</td></tr>
<tr><td>11</td><td>2</td><td>8KB</td><td>16KB</td></tr>
</table></td></tr>
<tr><td>1, 0</td><td>BS1, 0</td><td>R
W
10</td><td>BUFFER SIZE: Selects physical size of total SRAM buffer memory for both transmit and receive functions. See table:
<table>
<tr><th>BS1</th><th>BS0</th><th>SRAM size</th></tr>
<tr><td>0</td><td>0</td><td>8KB</td></tr>
<tr><td>0</td><td>1</td><td>16KB</td></tr>
<tr><td>1</td><td>0</td><td>32KB</td></tr>
<tr><td>1</td><td>1</td><td>64KB</td></tr>
</table></td></tr>
</table>

Table 13. DLCR7—Configuration Register 1

<table>
<tr><th>BIT</th><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>7, 6</td><td>E/D
CNF
1,0</td><td>R
W
00</td><td>ENCODER/DECODER CONFIGURATION: Selects the operating mode of the controller-encoder/decoder functions and their interface. See table below and pin descriptions for the monitor pins, TXD, TCK, TEN, LBC, RXD, RCK, CRS and COL:
<table>
<tr><th>E/D CNF 1</th><th>E/D CNF 0</th><th>Registers</th></tr>
<tr><td>0</td><td>0</td><td>Normal NICE: Internal encoder/decoder active. Monitor pins inactive.</td></tr>
<tr><td>0</td><td>1</td><td>NICE + Monitor: Internal encoder/decoder active. Monitor pins outputting all controller/encoder/decoder interface signals.</td></tr>
<tr><td>1</td><td>0</td><td>Encoder/Decoder Bypass: Internal encoder/ decoder not used. Monitor pins can be used to interface controller to external encoder/decoder.</td></tr>
<tr><td>1</td><td>1</td><td>Encoder/Decoder Test: Controller inactive, encoder/decoder active. Monitor pins used to test encoder/decoder.</td></tr>
</table></td></tr>
<tr><td>5</td><td>PWRDN</td><td>R
W
1</td><td>POWER DOWN: When set high, enables power to the chip for all functions; when set low, places chip in power down mode for power conservation.</td></tr>
<tr><td>4</td><td>RDYPOL</td><td>R
0/1</td><td>READY PIN POLARITY: Reads the state of the RDY POL pin 94.</td></tr>
<tr><td>3, 2</td><td>RBS 1, 0</td><td>R
W
00</td><td>REGISTER BANK SELECT: Provides the indirect address for selection of one of the three sets of registers to access when the physical register address is xxx8H–xxxFH. The lower 7 registers are not bank-selectable. See table:
<table>
<tr><th>RBS 1</th><th>RBS 0</th><th>Registers</th></tr>
<tr><td>0</td><td>0</td><td>DLCR0–7, DLCR8–F</td></tr>
<tr><td>0</td><td>1</td><td>DLCR0–7, HT8–F</td></tr>
<tr><td>1</td><td>0</td><td>DLCR0–7, BMR8–F</td></tr>
<tr><td>1</td><td>1</td><td>RESERVED</td></tr>
</table></td></tr>
<tr><td>1</td><td>EOPPOL</td><td>R
W
0</td><td>EOP PIN SIGNAL POLARITY: When high, the EOP pin is active-high; when low, EOP is active-low.</td></tr>
<tr><td>0</td><td>M..L/
L..M</td><td>R
W
0</td><td>BYTE ORDER CONTROL: Selects byte lane ordering for packet data in the buffer (applies only in System Word Mode). In both Most..Least and Least..Most modes, the first and second bytes of the packet will appear in the same word on the system bus. When this bit is high (M..L mode), the first and all odd-numbered bytes of a packet and its header will appear on the high byte of the system bus. Note that header bytes are also swapped.</td></tr>
</table>

Note to software engineers regarding NICE/EtherStar™ compatibility: If you desire to use the same node driver for Fujitsu's NICE and EtherStar controllers, the driver can determine which chip is being used by reading DLCR7 and/or DLCR6 after hardware reset. NICE will read 30B6H or 20BGH (30 or 20 for DLCR7 and B6 for DLCR6); EtherStar will read 0000H.

Power-down mode saves power when the device is not in use. When ready to place the NICE chip in Power Down Mode, first write 1 to DLCR6<7>, DLC EN, to turn the receiver and transmitter off, then write 0 to DLCR7<5>, PWRDN. To exit the power-down mode, write 1 to PWRDN. Register contents will be preserved, unless a hardware reset is issued. Hardware reset will also terminate the power-down mode.

Byte order control provided by the Most..Least/Least..Most bit, DLCR7<0>, provides compatibility with various higher-level protocols, such as TCP/IP and XNS. These protocols may have different transmission order of the bytes within a word. When M..L/L..M is low, the least significant byte of the word is transmitted first, followed by the most significant. When M..L/L..M is set high, the byte order is reversed. This feature applies only when the system bus is operated in 16-bit (word) mode.

The byte order control works by reversing or not reversing the bytes of all words as they pass between the buffer memory and the system bus. Thus all data stored in the transmit buffer or retrieved from the receive buffer is affected, including the nontransmitted headers. The NICE registers, other than the Buffer Memory Port, BMPR8:9, are not affected by this control bit. Care must be taken in the software driver code to reverse the header information as well as the packet data when using this feature. Examples follow.

Example of using Least..Most Byte Ordering:

System Bus

Transmit Packet:

High Byte	Low Byte
TX Length, high byte	TX Length, low byte
Destination Addr, 2nd byte	Destination Addr, 1st byte...
Source Addr, 2nd byte	Source Addr, 1st byte...
Length Field, low byte	Length Field, high byte
Data Field, 2nd byte	Data Field, 1st byte...

Receive Packet:

High Byte	Low Byte
Unused; reserved	Receive Packet Status
RX Length, high byte	RX Length, low byte
Destination Addr, 2nd byte	Destination Addr, 1st byte...
Source Addr, 2nd byte	Source Addr, 1st byte...
Length Field, low byte	Length Field, high byte
Data Field, 2nd byte	Data Field, 1st byte...

Example of using Most..Least Byte Ordering:

System Bus

Transmit Packet:

High Byte	Low Byte
TX Length, low byte	TX Length, high byte
Destination Addr, 1st byte	Destination Addr, 2nd byte...
Source Addr, 1st byte	Source Addr, 2nd byte...
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte...

Receive Packet:

High Byte	Low Byte
Receive Packet Status	Unused; reserved
RX Length, low byte	RX Length, high byte
Destination Addr, 1st byte	Destination Addr, 2nd byte...
Source Addr, 1st byte	Source Addr, 2nd byte...
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte...

Note: shaded items indicate numerically reverse byte ordering.

NODE ID REGISTERS

The Node ID Registers are accessed in register bank "0" at register addresses xxx8H–xxxDH. During initialization of the node, the unique Ethernet address assigned to the node is loaded into these registers. The first register at xxx8H corresponds to the first byte of the Node ID, which corresponds to the first address byte to be received as a packet arrives from the network. If the chip is configured to do so in its Address Filter mode bits, DLCR5<1:0>, the destination address field of an incoming packet will be compared to the Node ID stored in these registers. If there is a match, provided the packet passes the error filter, it will be accepted.

These registers are readable as well as writable, but they should not be accessed while the receiver is enabled. To avoid interaction with the receiver, access these registers only when DLC EN is 1. It is recommended that they be written and read only during initialization before enabling the receiver, i.e. before writing 0 to DLC EN, DLCR6<7>.

The address contained in these registers is used only for receive (destination) address filtering, not for the source address of outgoing packets. Outgoing packet addresses must be provided by the system as part of the packet data.

Within each byte, the bits are transmitted and received on the network least-significant bit first. See Table 3 for the transmission bit order, which follows the bit numbering in this table.

Time Domain Reflectometry (TDR) Counter

The TDR Counter can be used to get a rough indication of the location of a fault on the network, if one exists. When a node transmits, a short or open on the network would cause a reflected signal to the node's receiver which can sometimes be detected. The reflection will cause the carrier sense to fail and/or a false collision to be detected. This affect, time domain reflectometry, can be used to estimate the distance along the network cable from the node to the fault. The TDR Counter counts the number of bits transmitted before either a collision occurs, or carrier sense is lost, whichever comes first. If neither occur during transmission of the packet, the count is cleared. The amount of elapsed time this represents is two (2) times the signal delay from the node to the fault. An open on the network will usually cause a false collision, whereas a short is more likely to cause loss of carrier sense.

The TDR Count comes from DLCR14 and 15. DLCR14 is the least-significant byte, DLCR15 the most-significant. Only the lower 14 bits of the counter are equipped, which is more than is needed for an IEEE or Ethernet LAN. (The top two bits, DLCR15<7:6>, are always 0.)

To perform the TDR test for a fault, first enable interrupts for transmitter done (TX DONE). This is done by setting DLCR2<7> high. (An alternative to using the interrupt would be polling the TX DONE bit looking for a high level.) Set the 16 Collisions Register, BMPR11, to 07H for this test (no halt, skip failed packet). Clear all status bits by writing FF86H to the Receive and Transmit Status Registers. Next, transmit, or attempt to transmit, a packet of 600 bits or more in length. Up to 16 attempts may be made automatically if collisions are being indicated. Upon completion of the transmission attempt(s) TX DONE will go high, generating an interrupt if enabled. When this occurs, read the Transmit Status Register and the TDR Register.

Interpreting the results: If the count is zero, no fault was detected. If the count is greater than zero but smaller than the packet length, it may indicate a cable fault. If the count is less than 525, there may have been a real collision occurring during the test. Real collisions normally occur within the first 65 bytes of the packet, including preamble. Take note of the error messages, COL and CR LOST. COL high suggests a cable open, whereas CR LOST suggests a short. It is best to repeat the measurement several times, then throw out the anomalous values, if any, and average the rest. A cluster of readings at about the same value is a strong indicator of a valid fault measurement. If such a cluster of readings occurs, multiply the average of the cluster by 39 feet to estimate the distance from the node to the fault. (39 ft. = (100 ns x .8 x 186,282 mi/s x 5280 ft/mi)/ 2 ... this assumes the network is mostly coaxial cable with signal propagation speed of approximately .8 x C, the speed of light.)

HASH TABLE

The Hash Table provides a means for filtering incoming multicast packets so that the host processor does not have to process ones that are not of interest. The principle employed in this filtering scheme was originally developed by computer science to arrange a large number of elements of an array or database in such a way that facilitates searching for elements associated with a given key or datum. The 'hash function' is a mathematical or logical function which maps all possible elements in a domain onto a smaller domain called the 'hash table'.

As an example, suppose the following hashing function is used: "Treating the multicast address as a non-negative 48-bit integer, divide this number by 64 and take the remainder". This function will map all multicast addresses into a 64-element hash table since the remainder can be only the integer values 0 through 63. Applying this hashing function results in taking the least-significant 6 bits of the multicast address as an integer. In the hash table, for each element, 0 through 63, a single bit is stored which indicates whether the address is to be accepted (1) or rejected (0). If, for example, the node belongs to three multicast groups, only three or fewer of the hash table elements will store 1's, the rest 0's. The scheme allows the acceptance of any number of the addresses, including all of them. The limitation is that there may be addresses not of interest used on the network which also fall into the 'accept' elements, so in this case the filtering is imperfect. But in any case, most of the nonapplying addresses can be filtered out in this way.

The actual hashing function used in the NICE chip is this: "Calculate the CRC on the multicast address and take the high-order 6 bits of this calculation". The six bits are used to address the elements of the hash table. If a 1 is stored in an element of the table, associated packets are accepted. The hash filter criterium is only used on multicast addresses, which all start with a 1. Node ID's, which start with a 0, are not filtered by the hash filter. The broadcast address, a special case of the multicast set wherein all the bits are 1's, will be accepted anyway unless the "Reject all packets" mode is selected.

Figure 12 shows the register core, a modified shift-right register, used in generating and checking CRC's. Whereas some controllers share a single such core between transmitter and receiver, NICE has two of these, one for the generator and one for the checker, allowing both to operate concurrently for self-receive. To begin the calculation, the register is first set to all 1's. For the generator case, as the packet is transmitted, the data is clocked serially into the left-hand end of the register starting with the 48 bits of the destination address (the preamble is skipped). After the last bit of the 'data' field is clocked into the register, the CRC calculation is finished. The feedback line is then forced low and the register becomes a simple shift-right register. Its contents are then shifted out serially and transmitted, appending the CRC to the end of the packet. For the CRC checker, the calculation starts out the same way as for CRC generation feeding the incoming data into the register. But in this case, the CRC field of the packet is also fed into the calculation. The result is a fixed constant in the register if no CRC error has occurred.

For the Hash Filter, after the last bit of the destination address has been clocked into the register, the left-hand six register bits are stored in another register used to address the Hash Table elements. The left-most bit is most significant. The left-most three bits are used as the Hash Table register address and the right-most three as the bit address within a register byte. Having selected a Hash Table element in this way, a 1 in the table will indicate the packet is to be accepted, provided it is a multicast packet (first bit of destination address must be 1), and passes the error filters.

The hash filter is only employed when the address filter mode select bits, AF1, AF0 are 0, 1, selecting the "NODE ID, Broadcast, Multicast + Hash Table" mode. Like the NODE ID registers, the Hash Table registers should only be accessed when the receiver is disabled, i.e. when DLC EN is high, to avoid interaction with the receiver. There are eight bytes of registers in the Hash Table containing the 64 1-bit elements (refer to Table 1 for location). Source code software examples showing how to calculate entries for the Hash Table are available from Fujitsu Microelectronics', Semiconductor Division, in C and assembly language.

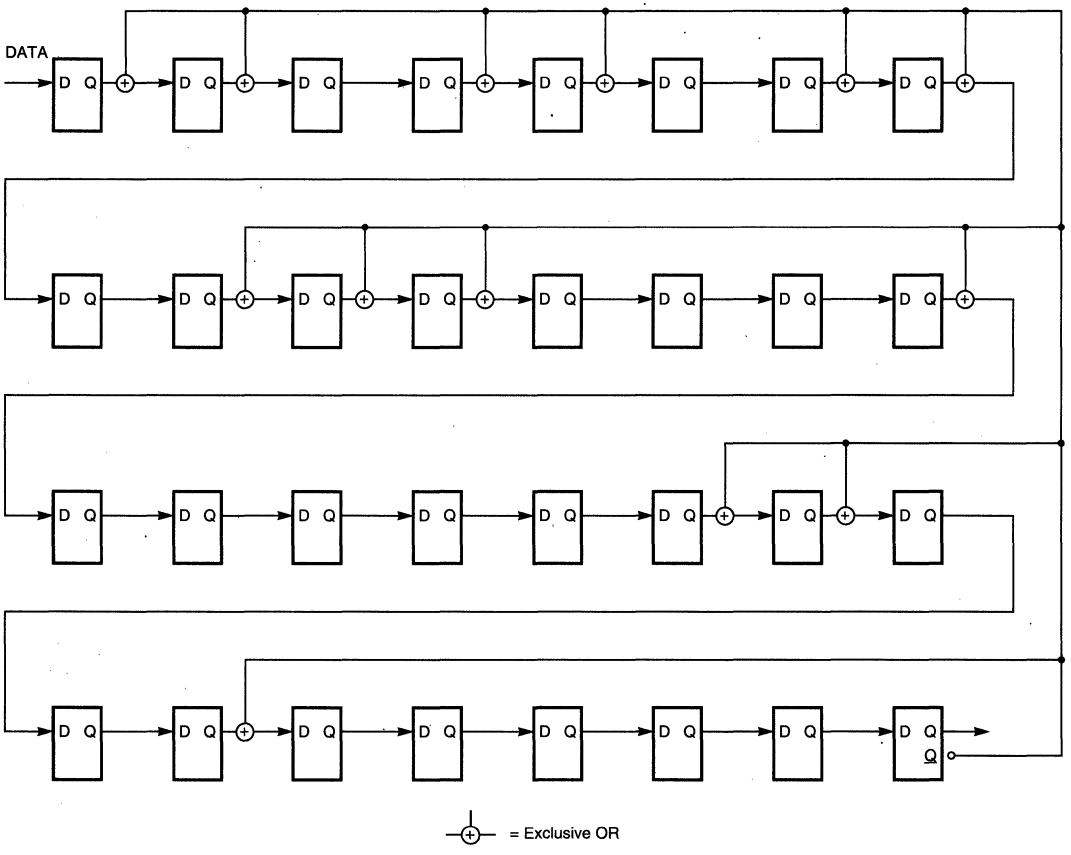


Figure 10. CRC Register Core

TRANSMIT AND RECEIVE PACKET HEADERS

Both transmit and receive packets have headers stored with them in the buffer memory which are not part of the transmitted packet. These headers precede the packet data.

Transmit Packet Length

An 11-bit integer indicating the number of bytes in the packet to be transmitted, excluding preamble and CRC fields which are generated by the NICE chip. See Table 3 for bit locations, and description for DLCR7<0>, M..L/L..M.

Receive Packet Status

The receive packet header consists of one byte of packet status, an unused byte and two bytes (11 bits) for packet length in bytes. See Table 3 for location of the bits, and description for DLCR7<0>, M..L/L..M. Bits 1, 2, 3 and 4 of the status byte are an image of the same bits in the Receive Status Register, DLCR1, with respect to the packet that follows. Bit 5 is the GOOD PKT bit. A 1 in this bit location indicates no errors were detected in the packet. Bits 0, 6 and 7 are unused and are always 0.

Receive Packet Length

The third and fourth bytes of the receive packet header indicate the total number of bytes in the stored packet data. See Table 3 for location of the bits, and description for DLCR7<0>, M..L/L..M.

BUFFER MEMORY PORT REGISTERS

The Buffer Memory Port Registers, BMPR8–15, provide the host access to the buffer memory and certain control functions. It is recommended that this bank be selected most of the time the chip is on the network for convenience in accessing the buffer memory and the control bits (Register Bank Select = 11 binary). Refer to Table 1 for location of these registers.

Writing a byte/word to BMPR8, the buffer port, transfers that data to the currently addressed location in the transmit buffer and increments the transmit buffer pointer to point to the next byte/word. Reading a byte/word from this port transfers the contents of the currently-addressed location in the receive buffer to the host and increments the receive buffer pointer to point to the next byte/word. BMPR9 is used only in word mode as the high byte of the word. In word mode, all transfers must be 16-bits wide, as the Buffer Port does not support byte-wide transfers in this mode. All other registers can be accessed word-wide, high byte only or low byte only as desired.

Table 14. BMPR10—Transmit Start Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX START	W 0	**TRANSMITTER START:** Writing 1 to this bit commands transmitter to start transmitting the packet(s) loaded into the transmit buffer. Before doing so, the transmitter must be idle (not busy with another buffer). The TX DONE bit is used to determine the required transmitter status, idle or busy.
6–0	TX PKT CNT	R W 0	**TRANSMIT PACKET COUNT:** A binary integer written by the system to indicate the number of packets contained in the transmit buffer for transmission. This information can be loaded at the same time the TX START bit is set high. As the transmitter finishes transmitting each packet, this counter is decremented. The value can be read by the system to see how many packets remain to be transmitted.

Transmit Start Register

The Transmit Start Register, BMPR10, contains the TX START bit and the TX PKT CNT. Writing 1 to the TX START bit immediately starts the transmitter. The Transmit Packet Count is a 7-bit binary integer written by the host to indicate the number of packets in the transmit buffer to be transmitted. See Table 14. This register should only be written when the transmitter is idle. It can be read at any time. TX START will always read as 1.

16 Collisions Control Register

This is a command register to control the actions taken when 16 consecutive attempts to transmit a packet are all met with collision. Table 15 summarizes the use of this register. It serves as both a mode setup register and an action command register. As a mode select register, two functions are selectable. Firstly, automatic continuation or halt after 16 collisions can be selected. If automatic continuation is selected, there is an option to continue attempting to transmit the same packet, or skip to the next packet. If halt is enabled, the Transmitter is restarted after a halt by writing any action code listed in Table 15 to this register.

DMA Enable Register

This is a write-only register which is used to enable and clear either Receive Read DMA or Transmit Write DMA. Refer to Table 14 for the codes.

DMA Burst Register (BMPR13)

This register is used to select the burst length for DMA operation. The burst length can be 1, 4, 8 or 12 transfers. Each transfer is one byte or one word, depending on the mode selected, System Byte or System Word (see SB/SW in DLCR6).

CODE	No. of Transfers
00H	1
01H	4
02H	8
03H	12

Table 15. 16 Collision Action Codes (written to BMPR11)

ACTION CODE	DESCRIPTION
02H or 03H	**MODE SETUP:** Halt after 16 Collisions.
02H	**COMMAND:** Resume transmitting, repeat failed packet (for use following a halt). Terminates the halt. Instructs transmitter to resume transmitting by repeating the failed packet. The collision counter is reset, allowing up to 16 additional attempts to be made. Halt after 16 collisions.
03H	**COMMAND:** Resume transmitting, skip failed packet (for use following a halt). Terminates the halt. Instructs transmitter to skip the failed packet and resume transmitting with the next packet in the buffer. The collision counter is reset, allowing up to 16 additional attempts to be made. If there is no next packet, the transmitter will deactivate, setting TX DONE as it does so. Halt after 16 collisions.
06H	**MODE SETUP:** Continue automatically after 16 collisions, repeat failed packet. Warning: If the network medium is disconnected, transmission attempts will usually result in false collision detection. Under this condition, this mode will cause the transmitter to continue re-attempting transmission of the same packet indefinitely. Interrupt or periodic polling of the status bits should be used to detect this condition.
07H	**MODE SETUP:** Continue automatically after 16 collisions, skip failed packet. Warning: This mode will result in failure to transmit some packets, since it skips a packet which has had 16 collisions. This condition is rare on a healthy network, but it does happen. To avoid this, use mode 06H.

Table 16. DMA Enable Register (BMPR12)

ACTION CODE	DESCRIPTION
01H	Enables Transmit Write DMA
02H	Enables Receive Read DMA
00H	Clear or terminate DMA activity, DMA EOP status bit and associated interrupt, if any. Normally used as response to End of Process (DMA EOP) interrupt.

Skip Packet Register (BMPR14)

Only one bit in this register is active, bit 2, the rest are 0. Writing 04H to this register commands the buffer controller to skip the balance of the current receive packet in memory. The bit can then be read to see when the skip process is complete (within 300 ns). The bit returns to 0 when the chip is ready to read the next packet, if there is another packet, or stop reading if there is not. Limitation of use: Do not use this feature before reading at least four (4) times from the beginning of the packet, nor if there are only eight (8) or fewer bytes left of the packet in the buffer. Doing so may corrupt the receive buffer pointers.

BMPR15 is unused and reserved for possible future use. Write only 0's to this register.

TRANSMITTER CIRCUITS

Circuits within the transmitter include a transmitter state machine, a small FIFO for pipe-lining the packet data, preamble generator, CRC generator, parallel to serial converter, backoff generator, inter-packet gap timer and a time domain reflectometer (TDR) counter.

The transmitter state machine provides sequencing of events for the transmitter, including idle, preamble, data, CRC, inter-packet gap, jam and backoff. It detects various transmit error conditions and sets appropriate bits within the DLCR registers.

The pipeline FIFO provides elastic buffering that the buffer controller can load with data to be transmitted. NICE's CRC generator calculates the Ethernet 32-bit CRC on the destination and source address, the length field and the data field as specified by the ISO/ANSI/IEEE 8802-3 specification for Ethernet. This value is appended to the end of the packet.

Transmit Error Processing

NICE has four transmit error status bits in its Transmit Status Register (DLCR0) for reporting the three possible transmit errors. The errors are: 1) loss of carrier during transmission, which usually indicates a medium fault or a collision, 2) collision, and 3) 16 consecutive collisions. The latter two can be enabled separately to generate interrupts.

If NICE detects a collision during transmission, it will automatically try to retransmit the packet until sixteen attempts have been made. Collision counter DLCR4<7:4>, automatically increments after each collision up to the sixteenth collision, at which time it rolls over to zero. (Bit 7 is the most-significant of the four bits.) Appropriate status bits in the Transmit Status Register and Transmit Mode Register are set in case of a collision-terminating transmission. Another status bit (16 COL) indicates that sixteen consecutive attempts to transmit a packet have been made and all have been terminated by collision. This case may indicate a network problem. For example, a disconnected cable or terminator will produce false collisions. But 16 collisions can occur normally, although rarely. A pseudo-random number generator provides the collision backoff function. This is clocked at the bit rate, 10 MHz, so that distances between stations become part of the randomizing function. It is sampled at the time of collision, masking all but the appropriate number of bits specified by the 8802–3 backoff algorithm. This value is then counted down at the slot-time rate (512 bits) to generate the backoff interval. For a first collision, only one bit is used, giving a backoff of either 51.2 microseconds or 0. For a second consecutive collision, two bits are used, and so forth, up to ten bits. From the tenth to the 16th collision, 10 bits are used. This gives a pseudo-random backoff interval of from 0 to 52.38 ms, the so-called 'binary exponential backoff' for collisions per 8802-3.

Time Domain Reflectometry

The TDR function provided counts the actual number of bits transmitted for each packet before an indication of either collision or carrier loss occurs, or the transmission completes. If a transmission completes without error indications, the TDR counter is cleared. See also the register description for DLCR14 and DLCR15.

Media Access Control

NICE's transmitter state machine implements the media access protocol for 8802–3 networks called CSMA/CD, Carrier Sense, Multiple Access with Collision Detection. The 'carrier sense' part means that the controller monitors the network for carrier from other nodes, and defers transmission while other nodes are transmitting (collision avoidance). But collisions can still occur when two nodes, perhaps separated on the network by several microseconds, start to transmit at nearly the same time. This is handled by the 'collision detection' part. All nodes are required to monitor the network for collisions and, when involved in one, transmit a 32-bit 'Jam' to reinforce the collision, then terminate transmission. Later, after waiting a pseudo-random backoff interval, the node automatically re-attempts to transmit the packet.

Between packets, there must be a gap of at least 9.6 microseconds during which time the trunk cabling is

idle. NICE's transmitter state machine measures this interval starting from the end of a packet on the network. It will not transmit until this interval has expired. During the first 2/3 of the interval, if for some reason carrier reappears on the network, NICE resets its interval timer to re-time the interval from the end of the new transmission. Such an event can occur during a collision, since data and carrier indications can be corrupted by the superimposition of the two packets. During the last 1/3 of the interval, NICE will ignore a carrier indication if it occurs. This is in accordance with 8802–3, intended to assure fairness and equality in access to the network. If one station starts to transmit slightly ahead of another, no advantage will be gained by the slightly earlier start. Both nodes will transmit, a collision will occur, and the media-access contention will be resolved by backoff interval differentials.

Data Encoder

NICE serializes the data for transmission, and converts each bit to Manchester Code, the format used on the network media. Manchester Code for '1' is a 100 ns interval starting with a low, ending with a high, with a low-to-high transition at the 50 ns point. Manchester Code for '0' is the inverse of this. See Figure 14 for a block diagram of the encoder/decoder section.

Operating with an External Encoder/Decoder

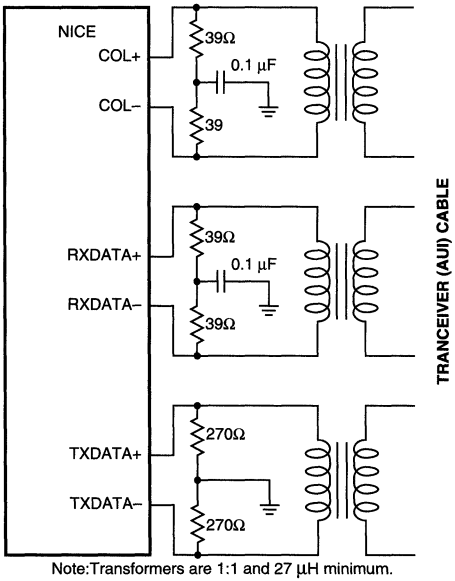
An option is provided on NICE to disable the on-chip encoder/decoder circuits and use an external encoder/decoder. Specific details are given in the register description section in Table 13, Configuration Register 1 (see DLCR7<7:6>).

Transmit Packet Processing

To transmit one or more packets, the host system first loads the packet(s), preceded by a 2-byte header giving their lengths, into a transmit buffer by writing the data to the Buffer Memory Port Register, BMPR<8:9>. Only the destination address, source address, length field and data field of the packets are loaded by the system, NICE generates the rest. When the packets are loaded, the system turns the transmitter on to initiate transmission. This enables NICE to transmit. Observing the media access protocol, NICE defers transmitting to carrier from other nodes, minimum inter-packet gap intervals and backoff intervals if any, then begins to transmit. NICE serializes the data and encodes it in Manchester Code. It generates the preamble field at the beginning, and calculates and appends the CRC field at the end, followed by the End-of-Packet Delimiter, which is a non-Manchester code. The Manchester-encoded signals are output through a differential driver to the TX DATA± pins to the external transceiver.

The driver is capable of driving a 50-meter segment of 78-Ohm transceiver cable, as specified in the 8802–3 standard. 270-Ohm resistors to GND are required externally to pull down TXDATA+ and TXDATA–. See Figures 11 and 12 for suggested cable interfacing.

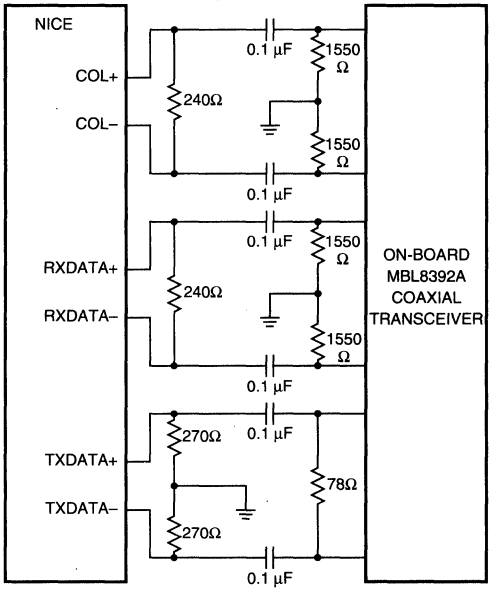
The host system activates the transmitter by writing 1 to the TX START bit and the packet count to TX PKT CNT. After this is done, the transmitter will transmit each packet in the buffer in the order that they were loaded. If a collision occurs, the transmitter automatically retransmits the packet until successful, or until 16 consecutive attempts have ended in collision. In the latter case, depending on the mode selection made at initialization time, the Transmitter will either 1) continue to try to transmit the same packet, starting again with a collision count of zero, 2) skip the current packet and try to transmit the next packet, starting with a collision count of zero, or 3) halt and wait for instruction from the host. In the third case the host can select to either 1) terminate by setting DLC EN high, 2) continue to attempt to transmit the same packet (collision counter gets reset) or 3) skip the current packet and try to transmit the next packet (collision count = 0).



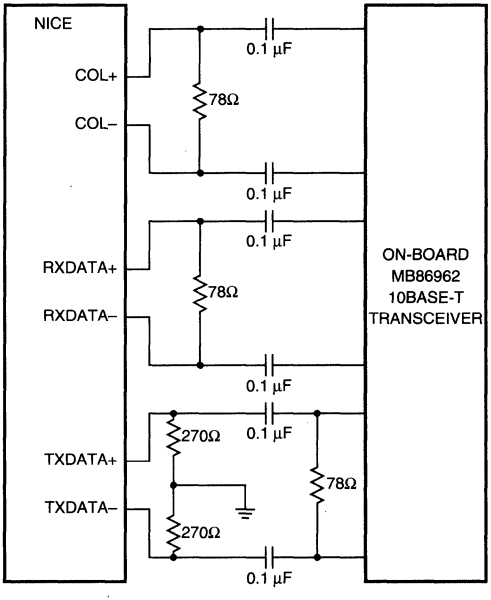
Note:Transformers are 1:1 and 27 µH minimum.

a. IEEE 802.3 AUI (Transceiver) Cable Termination

Figure 11. Transceiver Interface Termination



b. Simplified Termination for Coaxial Transceiver



c. Simplified Termination for on-board 10BASE-T Transceiver

Figure 12. Transceiver Interface Termination

Collision Signal Processing

As collisions are detected on the network media, the external transceiver generates a 10 MHz signal on the COL± differential inputs to the NICE's encoder/decoder section. When this signal is detected by NICE, it asserts the internal collision line, and in some modes the COL pin, pin 92, is also asserted.

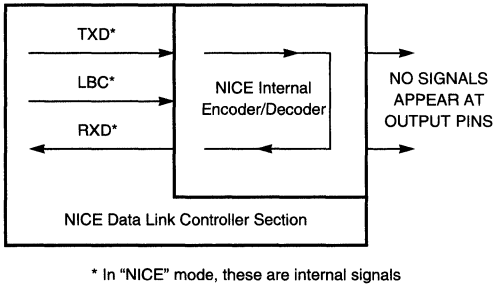
The COL± differential driver inputs require termination like that for the RXDATA± inputs. See Figures 11 and 12 for suggested cable termination.

Loopback

Loopback capability is provided to allow testing of NICE without sending signals onto the LAN media. The loopback function is invoked by clearing the LBC bit, DLCR4<1>. Loopback operation is illustrated in Figure 13.

Data is routed from the transmit buffer through a FIFO to the transmit section of the data link controller, through the internal Manchester encoder, back through the Manchester decoder, through the receiver section of the data link controller, and is then stored in a receive buffer. The test software can then read and check the received packet which has traveled through nearly all transmit and receive sections of the chip.

When an external encoder/decoder is used, the data is output on TXD and received at RXD. The external Manchester encoder/decoder should respond to assertion of its LBC input by looping its transmitter output to its receiver input internally, and should block the transmit data from appearing at its network output pin. Fujitsu's MB86951 and MB502A Encoder/Decoders, and MB86961 Encoder/Decoder with 10BASE-T Transceiver, for example, all respond in this way.



* In "NICE" mode, these are internal signals and no signals appear on the corresponding pins.

Figure 13. NICE in Loopback Mode

RECEIVER CIRCUITS

The receiver includes a receive state machine, serial to parallel conversion, pipe-line FIFO, preamble recognition, bit and byte framing, address filtering, CRC and other error checking and 'end-of-packet' symbol recognition.

The receiver state machine provides sequencing of events for the receiver, including idle, busy, address filtering, data storage, etc. It detects various receive error conditions and sets appropriate bits within the DLC Registers.

A small data FIFO provides elastic buffering for synchronization with the buffer controller timing, and buffering data while the buffer controller is servicing other buffer memory access requests.

All received bytes are delayed by four bytes before storing in the receive buffer so that the last four bytes of the packet can be stripped and checked for correct CRC. (The CRC bytes are not transferred to the receive buffer.)

During reception, packets are automatically rejected if space in the receive buffer is insufficient to hold the entire received packet. Status bits in the receive status register are set to indicate this and other errors. The receive errors are: 1) bus read error, which occurs if the host system attempts to read from an empty receive buffer (this need never occur if the RX BUF EMPTY bit is checked), 2) short packet error, 3) alignment error (incomplete byte fragment at end of packet), 4) CRC error and 5) buffer overflow. There is one additional possible receive error which the chip leaves to the software to check -- length error. When the length of the packet does not match the value in the Length Field of an 8802–3 packet, this is a length error. Some protocols use the length field for other purposes, for example, the DIX protocol uses it for a packet type code. In this case, allowed type codes do not overlap allowed packet length values, providing a means to distinguish which protocol is being used (if length value >1500, it's DIX type code). Length check can be made conditional on protocol type if necessary to support other protocols like DIX.

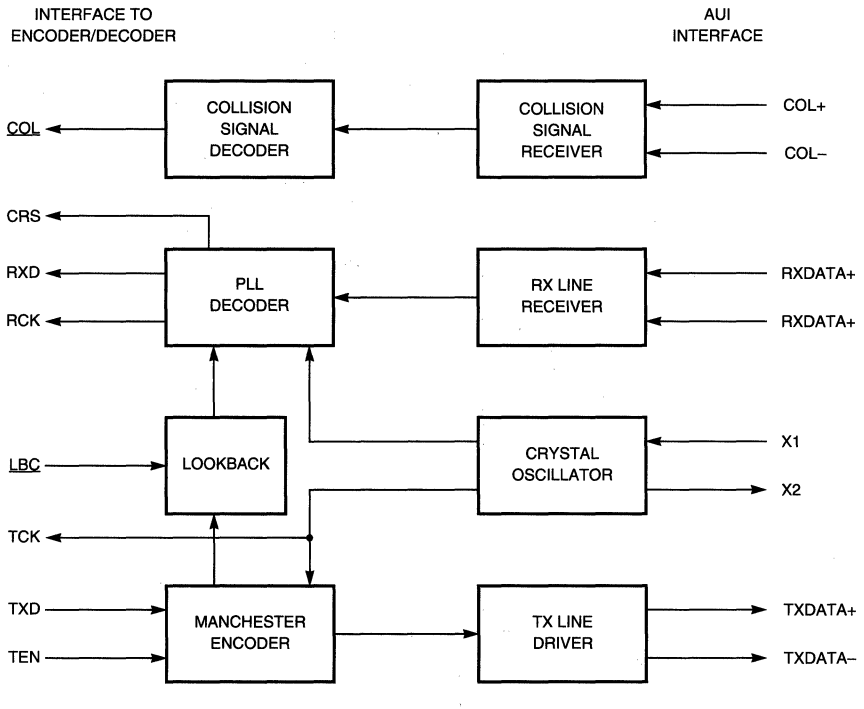


Figure 14. Encoder/Decoder Block Diagram

Decoder Functions

The data decoder section performs three functions on the data received at the differential receive inputs (RXDATA±) from the transceiver: clock recovery, carrier detection and Manchester data decoding.

Clock recovery and data separation are accomplished by the use of a phase locked loop. Use of proprietary techniques in the PLL allows lock-on to be accomplished within 6–7 bit times of the beginning of the preamble, and permits stable operation with input signal jitter of up to ±18 ns. Carrier detection is indicated to the controller by assertion of the CRS signal, which occurs shortly after a signal appears at RXDATA±.

The recovered clock is supplied to the controller on RCK, and is also used to convert the Manchester encoded data to NRZ format. NRZ data is output on RXD. Transitions in the state of RXD are synchronous with the falling edge of RCK. During idle periods, RCK is a free-running 10 MHz clock.

The RXDATA± differential inputs are usually terminated with two 39-Ohm resistors in series and an 0.1 µF bypass capacitor to ground at their junction, as shown in Figure 11.

Monitoring the Network

Whenever the data link section is enabled (DLC EN = 0), the receiver is constantly monitoring the network for carrier. Signals which exceed the AC and DC squelch thresholds of the RXDATA± input section cause the internal carrier sense (CRS) line to assert, which in turn causes the receiver to attempt to receive a packet. Refer to Figure 2 for a block diagram of the encoder/decoder section. (The carrier sense function is also used by the transmitter to defer to transmissions from other nodes, except when DLCR4<0> is high.)

After the PLL decoder acquires bit-synchronization with the incoming signal, the receiver monitors the data stream for the end-of-preamble bit pattern, two consecutive 1's ending the preamble's pattern of alternating 1's and 0's. This pattern gives the receiver byte and field synchronization, because the bit immediately following the two 1's is the first bit of the first byte of the packet's destination address field.

When packet transmission is unflawed, CRS will remain asserted for the duration of the packet, negating just after the last bit has been received. As a packet is coming in, the decoder's carrier sense function monitors the data stream for the end-of-packet symbol, a special non-Manchester code element at the end of the packet. Upon detecting this symbol, the carrier sense line will be negated. Loss of carrier will also result in negation of the carrier sense line, for example, when a collision occurs.

Receive Packet Processing

As a receive packet comes in from the network, its destination address field is tested for the various address filter criteria selected by the Address Filter Mode bits (AF1, AF0) and the Hash Table. See Figure 15 for 8802–3 packet format. Only if the address meets the filter criteria selected will the packet be accepted for storage in the receive buffer. In addition, the packet must be error-free, unless the chip has been enabled to receive flawed packets for diagnostic purposes. If these conditions are met, the packet reception results in the packet being stored in the buffer, its 4-byte header being updated at the end of reception, the RX BUF EMPTY bit being cleared, the RX PKT bit being set high and an interrupt being generated (if enabled). Otherwise the packet will be discarded and pointers will be reset to reuse the same portion of memory for the next packet to arrive. If a flawed packet is accepted for storage for diagnostic purposes, its error(s) will be reported in the PKT STATUS byte of its header (refer to Table 3 for byte and bit positions).

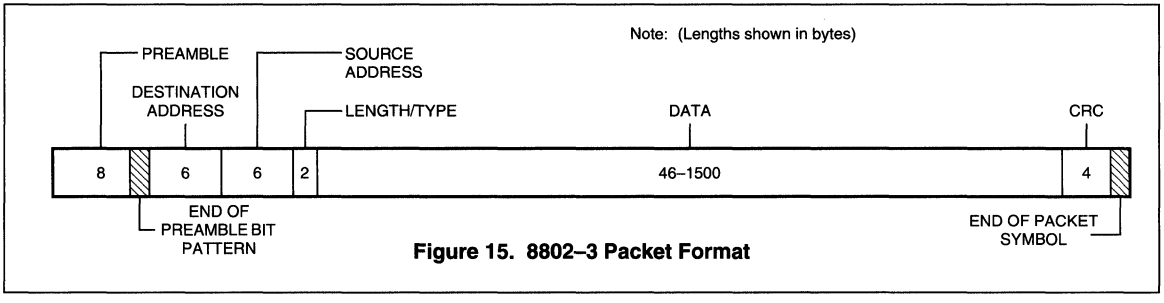


Figure 15. 8802–3 Packet Format

Network Management

Error, traffic and performance statistics can be collected continuously or on a sampled basis. The Receive Status Register and Transmit Status Register indicate any errors detected. Such data can be collected in two ways. Either interrupts can be used after each packet, and the status read from the status register by the interrupt service routine, or, for the receive case, the packets can be accepted for storage in the receive buffer, allowing their contents and error statuses (stored in the header) to be read later in batch mode. To get maximum statistics for the network, the "Accept all packets" mode can be used. In this mode, all packets can be counted, including their lengths. But of course, this use will maximize host overhead, so it should be used sparingly in user terminal equipment.

Carrier detection can be sampled as a means of estimating network bandwidth utilization. This bit is available in the Transmit Status Register (NET BSY).

An estimate of the average media-access waiting time can be calculated from the elapsed time between starting the Transmitter and TX DONE going high.

The transmit collision count (DLCR4<7:4>) can be used to determine the number of collisions encountered by the last outgoing packet. (The counter is reset at the start of transmitting each new packet.)

ELECTRICAL CHARACTERISTICS

Table 17. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter Description	Min.	Max.	Units
V_{CC}	Supply voltage	-0.5	6.0	V
V_{IN}	Input voltage	-0.5	V_{CC} + 0.5	V
V_{OUT}	Output voltage	-0.5	V_{CC} + 0.5	V
I_{ODF}	Differential output current on TXDATA± pins		-40	mA
V_{IDC}	Input DC voltage on RXDATA± and COL±	-0.5	16	V
V_{ODC1}	Output DC voltage on TXDATA± w/o transformer	-0.5	14	V
V_{ODC2}	Output DC voltage on TXDATA± with transformer	-0.5	16	V
T_{BIAS}	Temperature under bias	-25	+85	°C
T_{STG}	Storage temperature	-40	+125	°C
PWR	Power dissipation		425	mW

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Not more than one output may be shorted to ground or V_{CC} at a time for a maximum duration of one second.

Table 18. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	4.75		5.25	V
V_{IH}	Logic input high voltage	2.2			V
V_{IL}	Logic input low voltage			0.8	V
R_L	Driver load resistors on TXDATA± pins to ground	250	270	290	Ohm
R_T	Termination resistors (2 in series across RXDATA± and COL±)	38.6	39	39.4	Ohm
C_T	Termination bypass capacitors (between junction of termination resistors and ground)	0.1			µF
C_{OSC}	Oscillator load capacitance, including stray capacitance (see Figure 3)	12	20	38	pF
f_{XTAL}	Crystal oscillator frequency	19.999	20	20.001	MHz
T_A	Operating temperature	0		70	°C

Table 19. DC SPECIFICATIONS (At recommended operating conditions unless otherwise noted.)

Symbol	Parameter Description	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low level input voltage		0.0		0.8	V
V_{IH}	High level input voltage		2.2		V_{CC}	V
V_{OL1}	Low level output voltage, all outputs except DREQ	I_{OL} = -3.2 mA	0.0		0.4	V
V_{OL2}	Low level output voltage, DREQ only	I_{OL} = -12 mA	0.0		0.4	V
V_{OH1}	High level output voltage, all outputs except DREQ	I_{OH} = +2 mA	4.2		V_{CC}	V
V_{OH2}	High level output voltage, DREQ only	I_{OH} = +4 mA	4.2		V_{CC}	V
V_{OP}	TXDATA± peak output	R_L = 270 Ohms	±0.5		±1.3	V
V_{ACCM}	Output AC common mode on TXDATA±	R_L = 270 Ohms, R_T = 78 Ohms			±40	mV
V_{DCCM}	Output DC common mode on TXDATA±	R_L = 270 Ohms	2.4	3.4	4.4	V
V_{SQ}	Squelch threshold	AC/DC = 1 AC/DC = 0	-300 -80	-220 0	-140 +80	mV mV
I_L	Input leakage current	V_I = 0 - V_{CC}	-10		10	µA
I_{PWRDN}	Power down V_{CC} current	No output loads		6	10	mA
I_{CC}	Operating V_{CC} current	No output loads		40	85	mA

Table 20. GENERAL CAPACITANCE (T_A = 25° C, V_{DD} = V_I = 0 V, f = 1 MHz)

Symbol	Parameter Description	Min.	Max.	Units
C_{IN}	Input pin capacitance		16	pF
C_{OUT}	Output pin capacitance		16	pF
$C_{I/O}$	I/O pin capacitance		16	pF

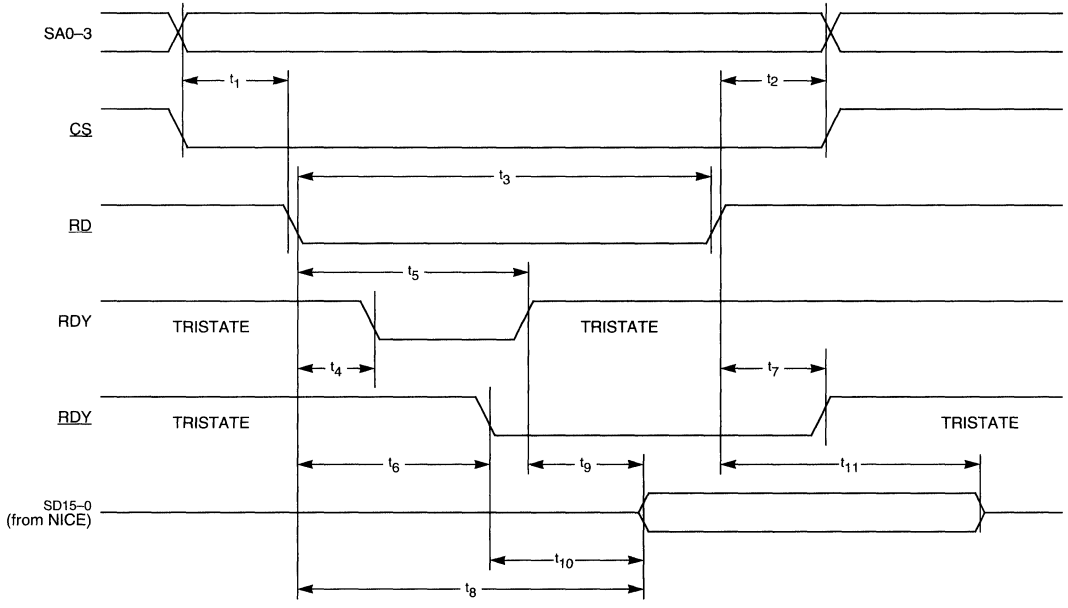


Figure 16. Read Cycle

Table 21. Read Cycle

Symbol	Parameter Description	Min.	Max.	Units
t_1	CS low to RD low; SA3–0 valid to RD low	3		ns
t_2	RD high to CS high; RD high to SA3–0 invalid	3		ns
t_3	RD low pulse width	30		ns
t_4	RD low to RDY low	0	26	ns
t_5	RD low to RDY TRISTATE[1]		175	ns
t_6	RD low to RDY low[2]	0	175	ns
t_7	RD high to RDY TRISTATE		28	ns
t_8	RD low to SD15–0 valid (except Buffer Memory Port)		44	ns
t_9	RDY TRISTATE to SD15–0 valid (buffer port)		8	ns
t_{10}	RDY low to SD15–0 valid		10	ns
t_{11}	RD high to SD15–0 invalid (data hold)	15		ns

1. 0 ns maximum for registers, and for Buffer Memory Port when port is ready before the read cycle begins. For port access only, 175 ns maximum may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception. 2.15 µs max for bus read error.

2. 28 ns maximum for all registers. For port access only, 175 ns maximum may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception. 2.15 µs max for bus read error.

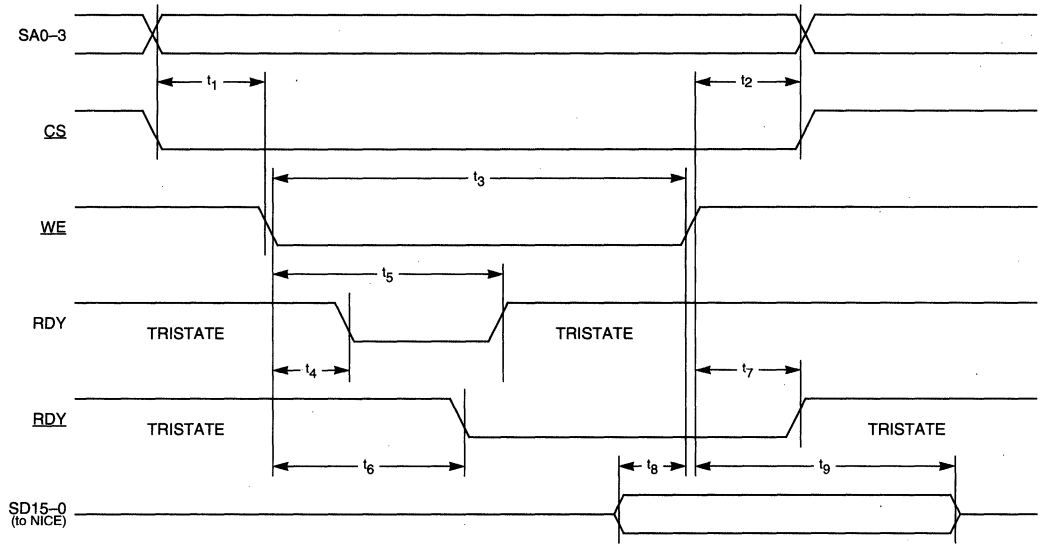


Figure 17. Write Cycle

Table 22. Write Cycle

Symbol	Parameter Description	Min.	Max.	Units
t_1	CS low to WE low; SA3–0 valid to WE low	3		ns
t_2	WE high to CS high; WE high to SA3–0 invalid	3		ns
t_3	WE low pulse width	36		ns
t_4	WE low to RDY low	0	26	ns
t_5	WE low to RDY TRISTATE[1]		175	ns
t_6	WE low to RDY low[2]	0	175	ns
t_7	WE high to RDY TRISTATE		28	ns
t_8	SD15–0 valid to WE high (data setup)	5		ns
t_9	WE high to SD15–0 invalid (data hold)	6		ns

1. 0 ns maximum for registers, and for Buffer Memory Port when port is ready before the write cycle begins. For port access only, 175 ns maximum may occur if system makes contiguous system write cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception.

2. 28 ns maximum for all registers. For port access only, 175 ns maximum may occur if system makes contiguous system write cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception.

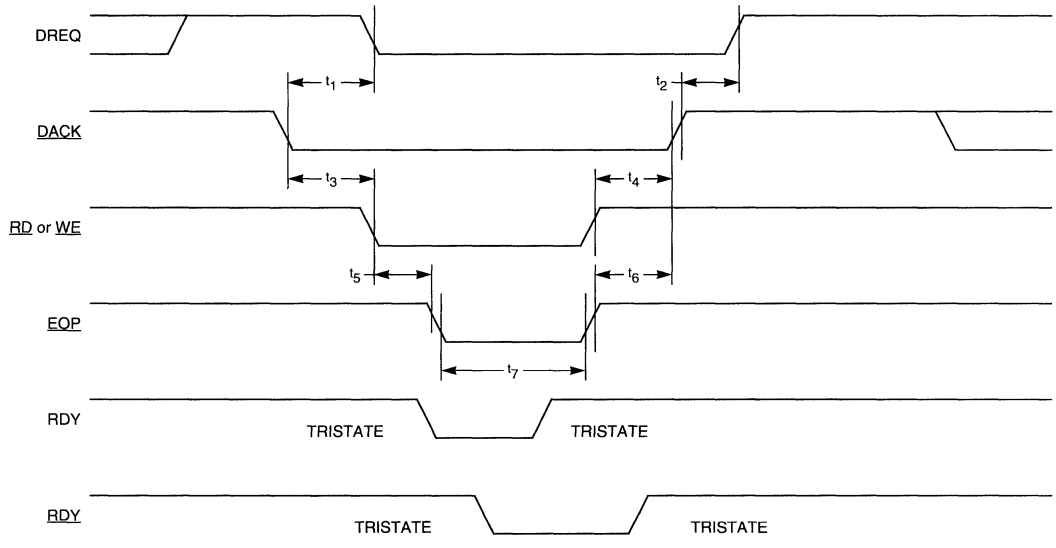


Figure 18. Single-Cycle DMA Timing

Table 23. Single-Cycle DMA Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	DACK low to DREQ low	0	21	ns
t_2	DACK high to DREQ high	0	19	ns
t_3	DACK low to RD or WE low	0		ns
t_4	RD or WE high to DACK high	3		ns
t_5	RD or WE low to EOP low	0		ns
t_6	EOP high to DACK high	3		ns
t_7	EOP low pulse width	10		ns

1. An asserted EOP terminates any further DREQ after DACK returns high.
2. The DMA cycle uses DACK as the chip select. DACK overrides CS and SA3–0 if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
3. For RDY(RDY) timing and SD15-0 timing, see Figure 16, t_4–t_{11}, and Figure 17, t_4–t_9.

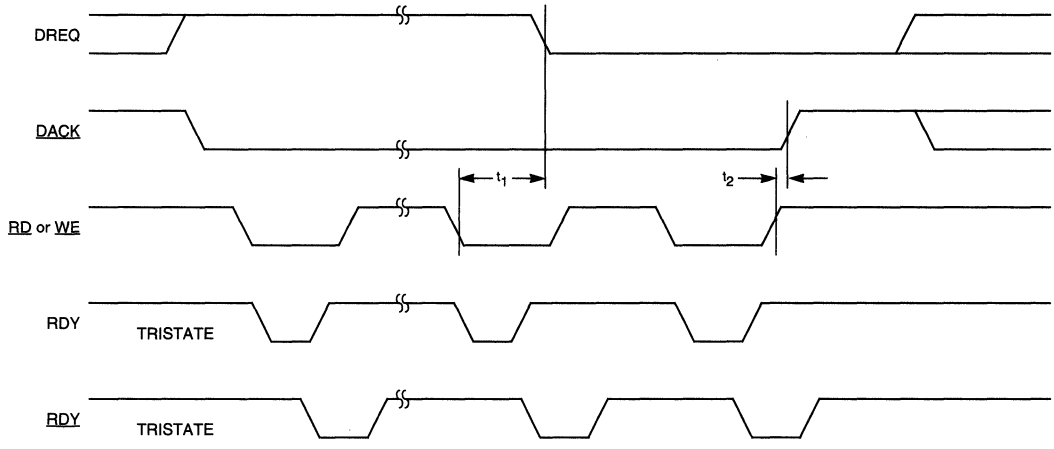


Figure 19. Burst DMA Timing

Table 24. Burst DMA Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	RD or WE low to DREQ low		32	ns
t_2	RD or WE high to DACK high	3		ns

1. DREQ goes low during the next-to-last transfer of the burst. DACK should not go high until after the RD or WE pulse of the last transfer cycle goes high.
2. The DMA cycle uses DACK as the chip select. DACK overrides CS and SA3–0 if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
3. For RDY(RDY) timing and SD15-0 timing, see Figure 16, t_4–t_{11}, and Figure 17, t_4–t_9.

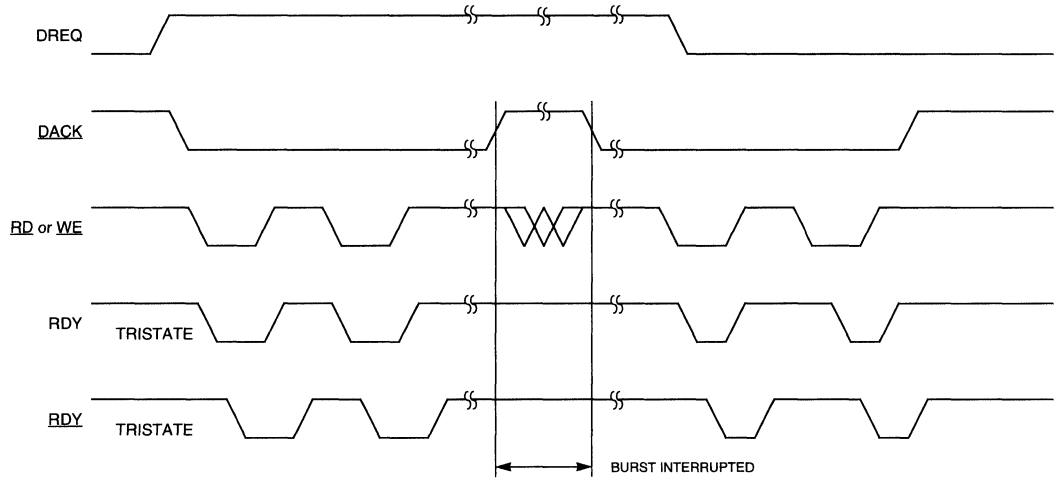


Figure 20. Burst DMA Interrupted by DACK

Note: Burst can be interrupted by DACK high-going pulse during the burst. Burst will resume when DACK returns low.

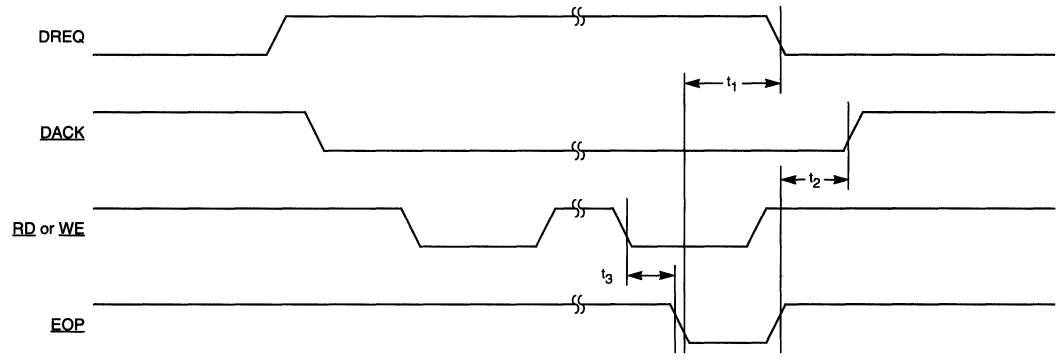


Figure 21. Burst DMA Terminated by EOP

Table 25. Burst DMA Terminated by EOP

Symbol	Parameter Description	Min.	Max.	Units
t_1	EOP low to DREQ low	4	28	ns
t_2	EOP high to DACK high	3		ns
t_3	RD or WE low to EOP low	0		ns

Note: EOP can be asserted during any transfer of the burst to terminate the process following that transfer.

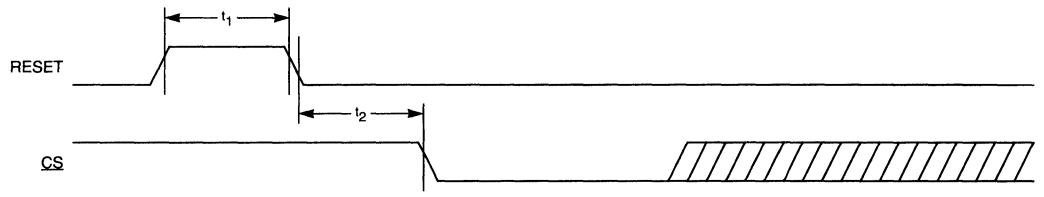


Figure 22. RESET Timing

Table 26. RESET Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	RESET pulse width	200		ns
t_2	RESET low to first CS low	300		ns

Note: Before enabling transmit and receive functions (DLC EN), wait 200 µs after reset pulse for stabilization of receiver PLL.

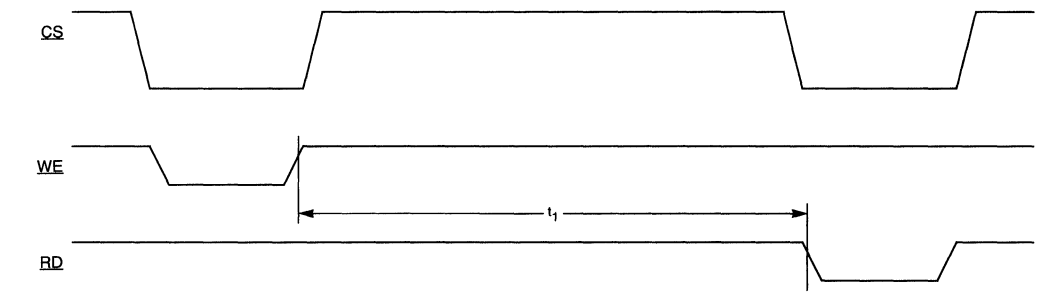


Figure 23. Skip Packet Timing

Table 27. Skip Packet Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	Writing Skip Packet high to next Buffer Memory Port read	300		ns

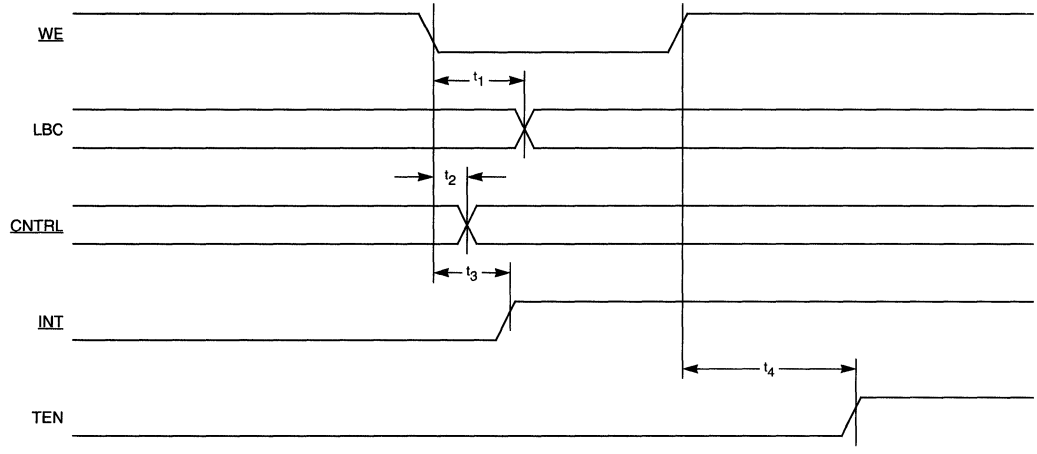


Figure 24. LBC, CNTRL and INT Timing

Table 28. LBC CNTRL and INT Timing

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Loopback Control (LBC) delay	20		60	ns
t_2	CNTRL delay	20		60	ns
t_3	INT signal clearing delay	20		60	ns
t_4	Transmit enable delay after setting TX START high (if network free)		2.3		µs

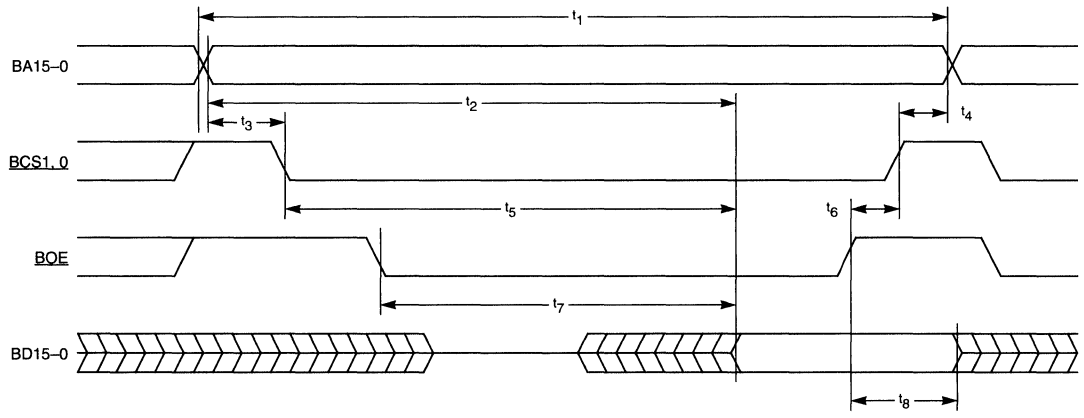


Figure 25. SRAM Read Timing

Table 29. SRAM Read Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	Read cycle	95		ns
t_2	Address access time		81	ns
t_3	Address valid to BCS1,0 low	0	8	ns
t_4	BCS1,0 high to address invalid	0		ns
t_5	Chip select access time		81	ns
t_6	BOE high to BCS1,0 high	0	2	ns
t_7	Output enable access time		49	ns
t_8	Data hold time	0		ns

Note: Use SRAM with address access time of 80 ns or less.

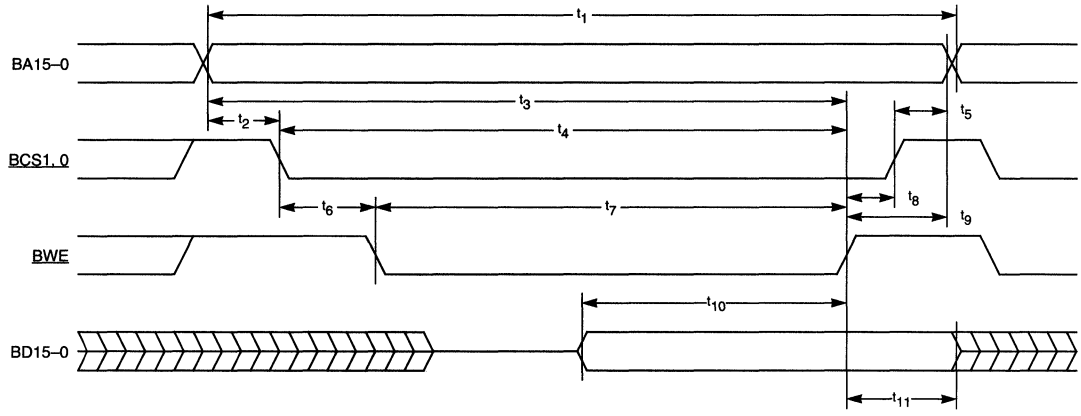


Figure 26. SRAM Write Timing

Table 30. SRAM Write Timing

Symbol	Parameter Description	Min.	Max.	Units
t_1	Write Cycle	95		ns
t_2	Address Valid to BCS1,0 low	2	8	ns
t_3	Address Valid to BWE high	71		ns
t_4	BCS1,0 low to BWE high	62		ns
t_5	BCS1,0 high to Address Invalid	0		ns
t_6	BCS1,0 low to BWE low	0		ns
t_7	BWE Pulse Width	60		ns
t_8	BWE high to BCS1,0 high	0		ns
t_9	BWE high to Address Invalid	12		ns
t_{10}	Data Setup Time	41		ns
t_{11}	Data Hold Time	14		ns

Note: Use SRAM with address access time of 80 ns or less.

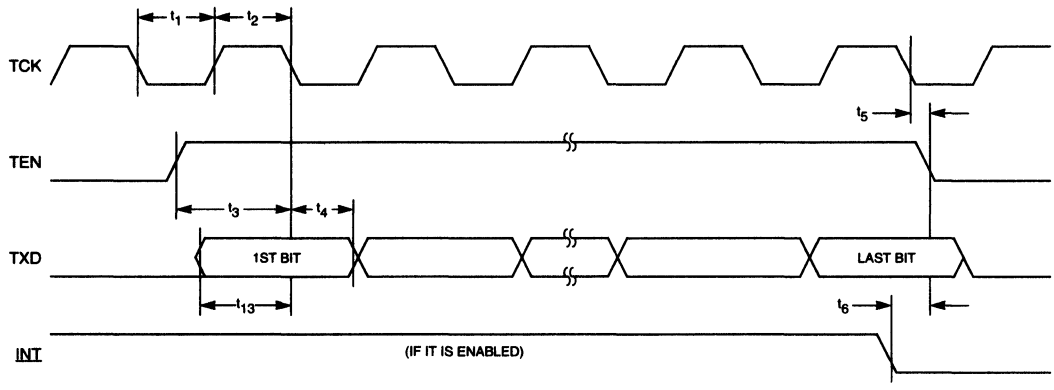


Figure 27. Transmit Timing

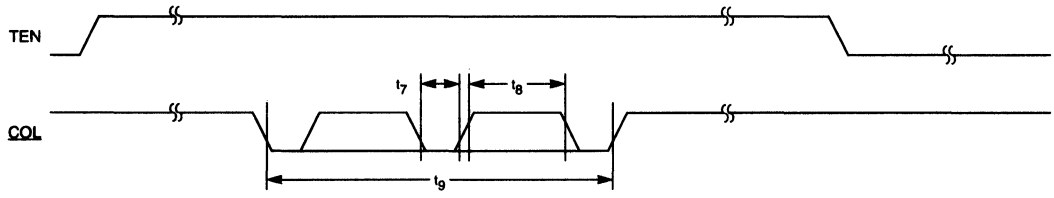


Figure 28. Transmit Timing

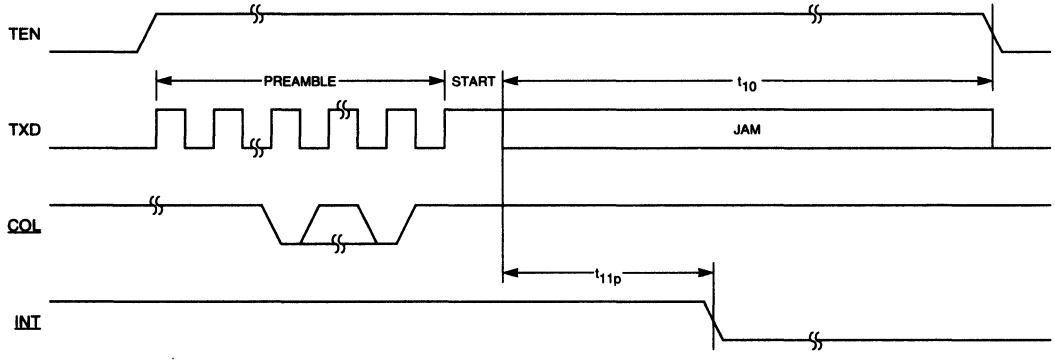


Figure 29. Transmit Timing

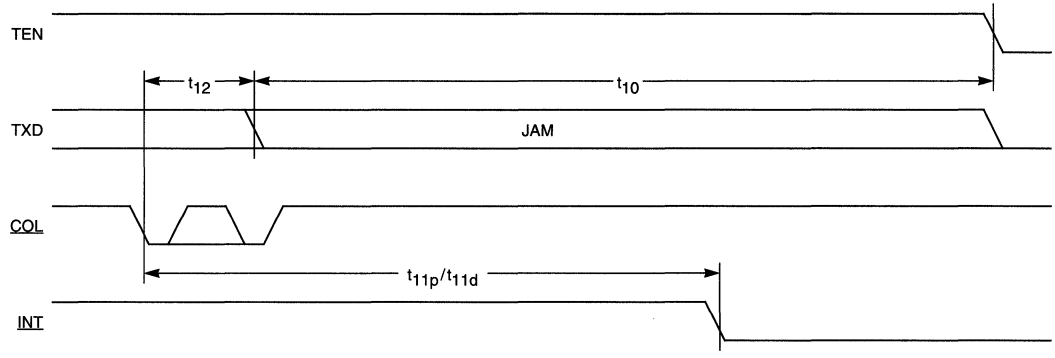


Figure 30. Transmit Timing

Table 31. Transmit Timing: Figures 27-30 (for Encoder/Decoder Bypass mode)

Symbol	Description	Min.	Typ.	Max.	Units
t_1	Transmit clock low width	40	50	60	ns
t_2	Transmit clock high width	40	50	60	ns
t_3	TEN high to TCK low	48	—	—	ns
t_4	Transmit data hold	12	—	—	ns
t_5	TCK low to TEN low	13	—	—	ns
t_6	Transmit interrupt low to transmit enable low	—	1	—	TCK cycles
t_7	Collision low pulse width	20	—	—	ns
t_8	Collision high pulse width	—	—	200	ns
t_9	Minimum collision length	520	—	—	ns
t_{10}	Jam period[1]	—	32	—	TCK cycles
t_{11p}	Transmit interrupt when collision at preamble	—	5	—	TCK cycles
t_{11d}	Transmit interrupt when collision at data field	—	16	—	TCK cycles
t_{12}	Collision to first jam bit	4	—	12	TCK cycles
t_{13}	Transmit data setup	40	—	—	ns

1. The 32 jam bits include eight data bits and 24 '0' bits.

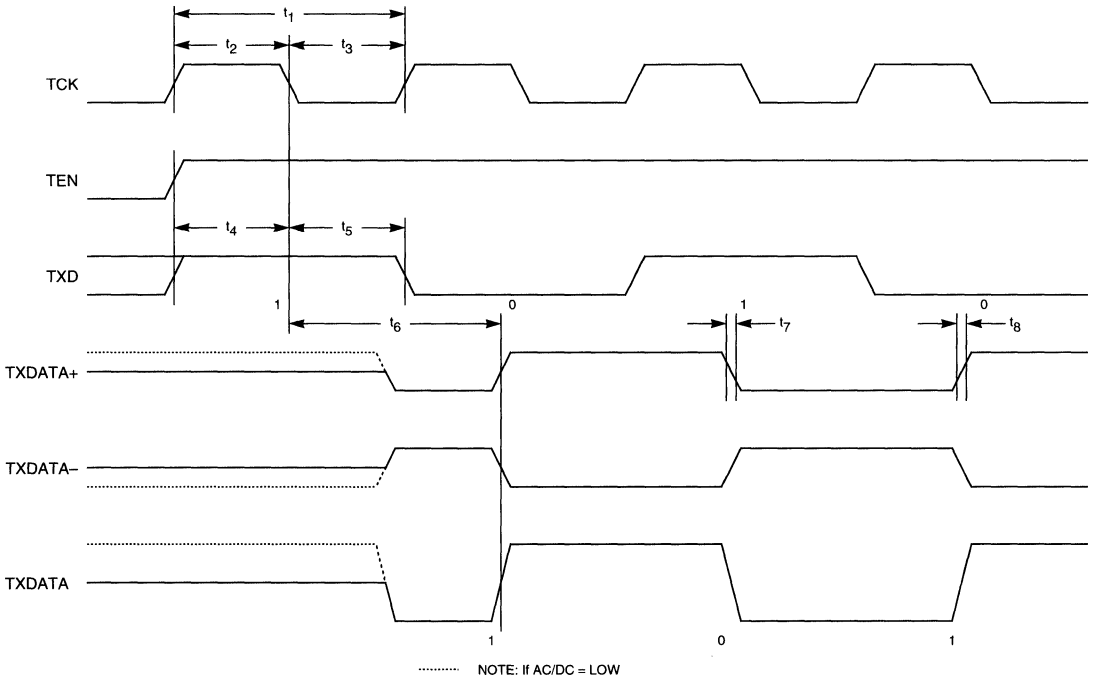


Figure 31. Transmit Start Timing

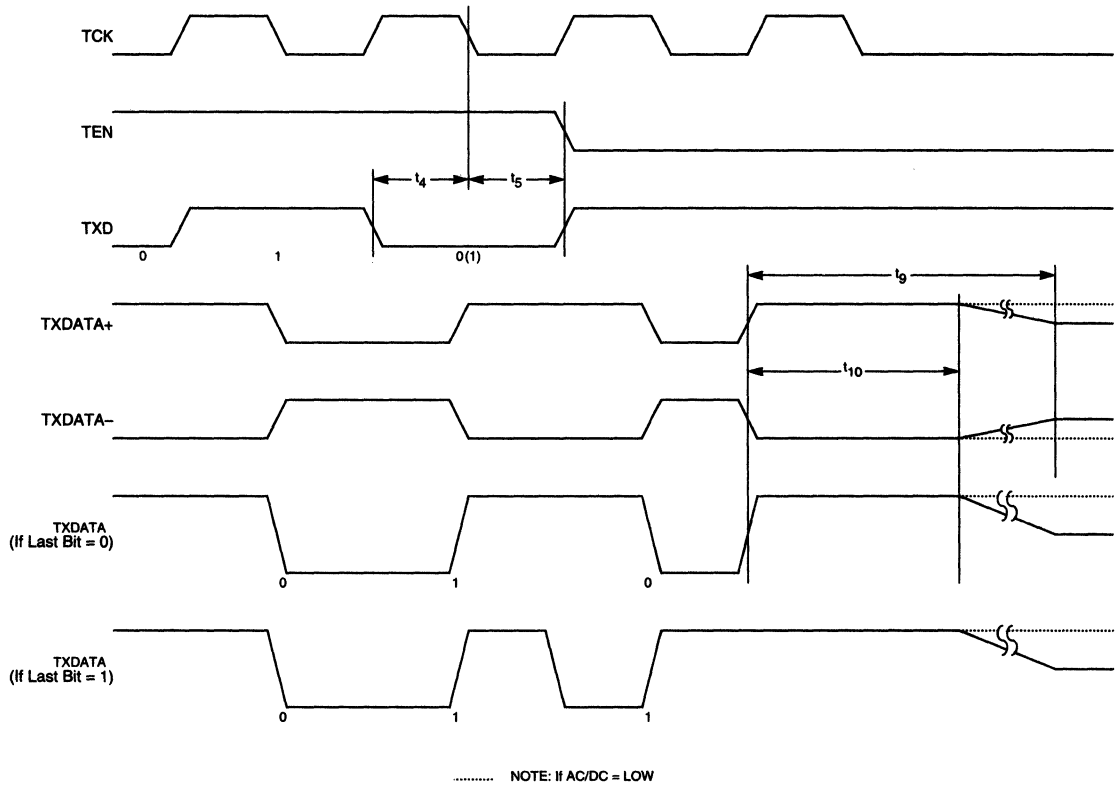


Figure 32. Transmit End Timing

Table 32. Transmit Start and End Timing: Figures 31-32 (for Encoder/Decoder Test mode)

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_1	31	TCK cycle time		99.99	100	100.01	ns
t_2	31	TCK high width		35	50	65	ns
t_3	31	TCK low width		35	50	65	ns
t_4	31, 32	TXD, TEN setup time to TCK		20	–	–	ns
t_5	31, 32	TXD, TEN hold time from TCK		10	–	–	ns
t_6	31	TXDATA± encode time		–	95	–	ns
t_7	31	TXDATA± fall time	20% to 80%	–	2	–	ns
t_8	31	TXDATA± rise time	20% to 80%	–	2	—	ns
t_9	32	TXDATA± line voltage transition	AC/DC = High	–	–	8000	ns
t_{10}	32	TXDATA± end-of-packet delimiter	AC/DC = High	200	–	–	ns

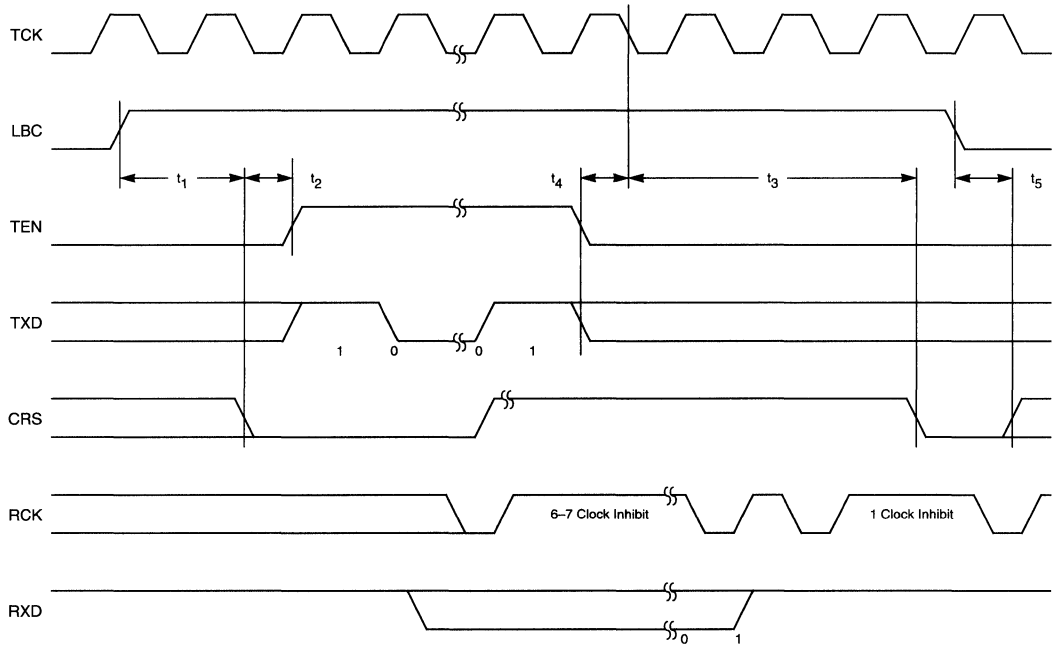


Figure 33. Loopback Timing

Table 33. Loopback Timing (for Encoder/Decoder bypass mode)

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	LBC receiving data purge time	–	260	–	ns
t_2	Wait time from CRS low to TEN high	9.6	–	–	s
t_3	Data through time	–	280	–	ns
t_4	TXD, TEN setup tome to TCK	0	–	–	ns
t_5	LBC receiving data accept time	–	80	–	ns

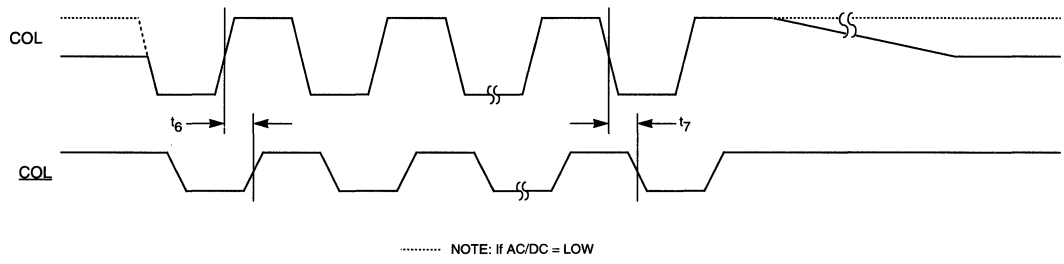


Figure 34. Collision Timing

Table 34. Collision Timing (for Encoder/Decoder Test mode)

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_6,t_7	COL± to COL propagation delay time	15	50	–	ns

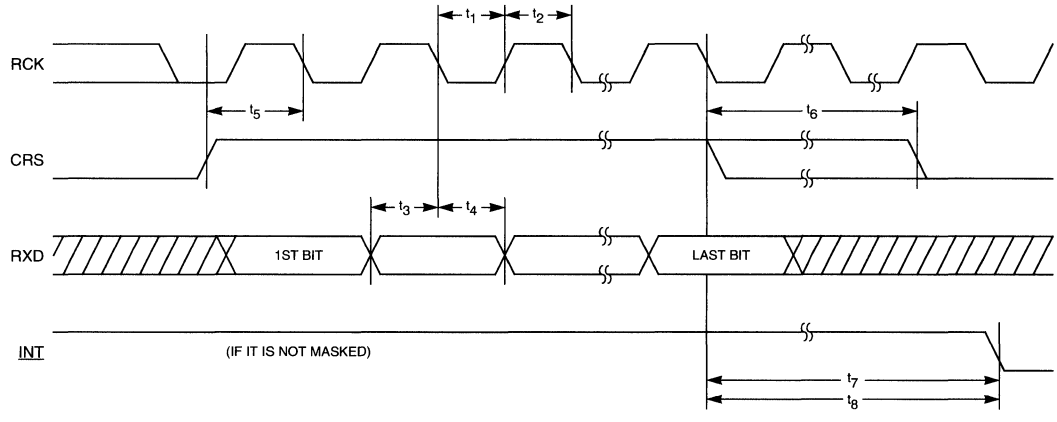


Figure 35. Receive Timing

Table 35. Receive Timing (for Encoder/Decoder Bypass mode)

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Receive clock low width	35			ns
t_2	Receive clock high width	35			ns
t_3	Receive data setup	10			ns
t_4	Receive data hold	10			ns
t_5	Receive carrier sense setup	10			ns
t_6	Receive carrier sense hold			7	RCK cycles
t_7	Last bit of good packet received to interrupt		40		RCK cycles
t_8	Receive interrupt after bad packet		15		RCK cycles

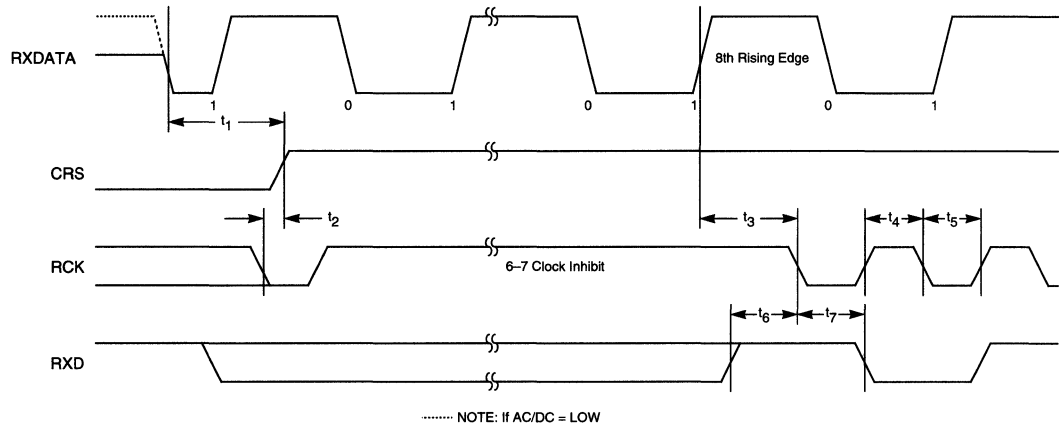


Figure 36. Receive Start Timing

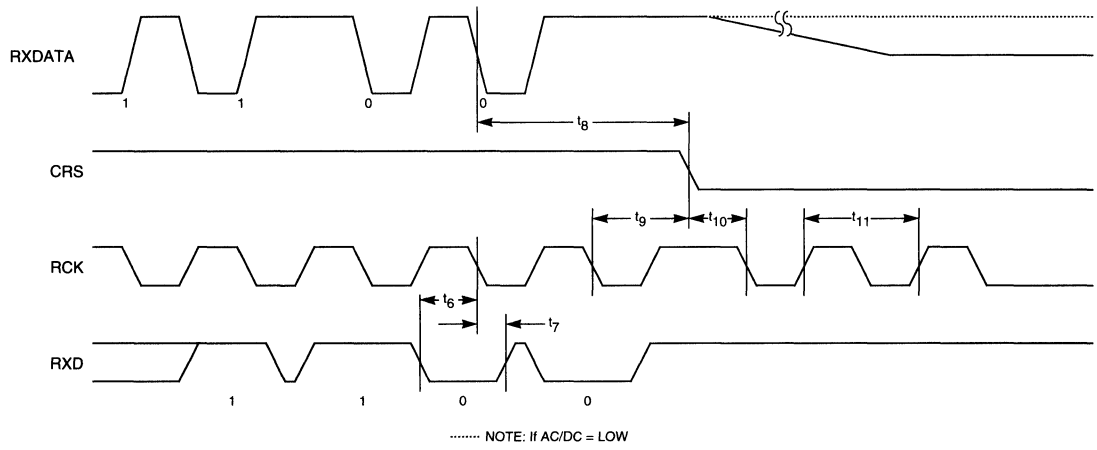


Figure 37. Receive End Timing

Table 36. Receive Timing: Figures 36-37 (for Encoder/Decoder Test mode)

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_1	36	CRS on delay time		–	90	120	ns
t_2	36	CRS low hold time		10	–	–	ns
t_3	36	RCK delay time		–	125	–	ns
t_4	36	RCK high time		35	50	–	ns
t_5	36	RCK low time		35	50	–	ns
t_6	36, 37	RXD setup time to RCK		20	60	–	ns
t_7	36, 37	RXD hold time from RCK		10	20	–	ns
t_8	37	CRS off delay time		–	260	–	ns
t_9	37	CRS high hold time		–	130	–	ns
t_{10}	37	CRS low setup time		–	70	–	ns
t_{11}	37	RCK cycle time during idle		99.99	100	100.01	ns

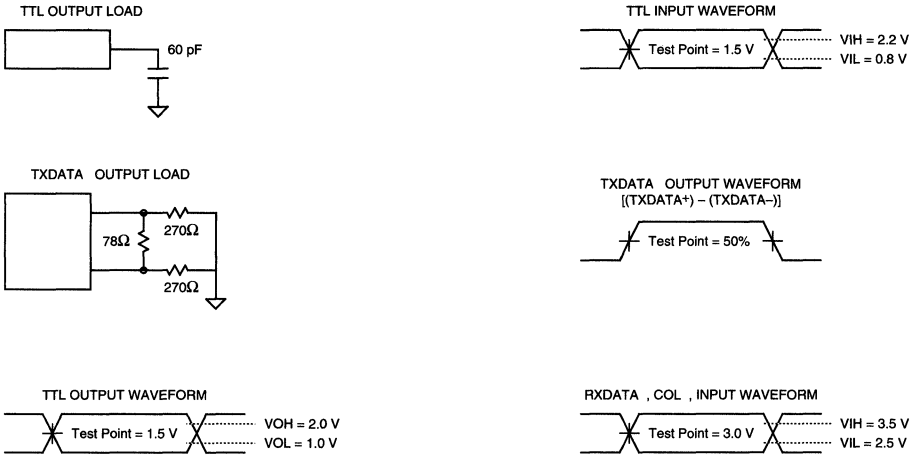
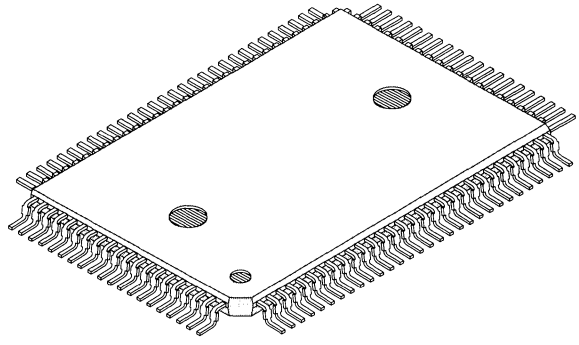


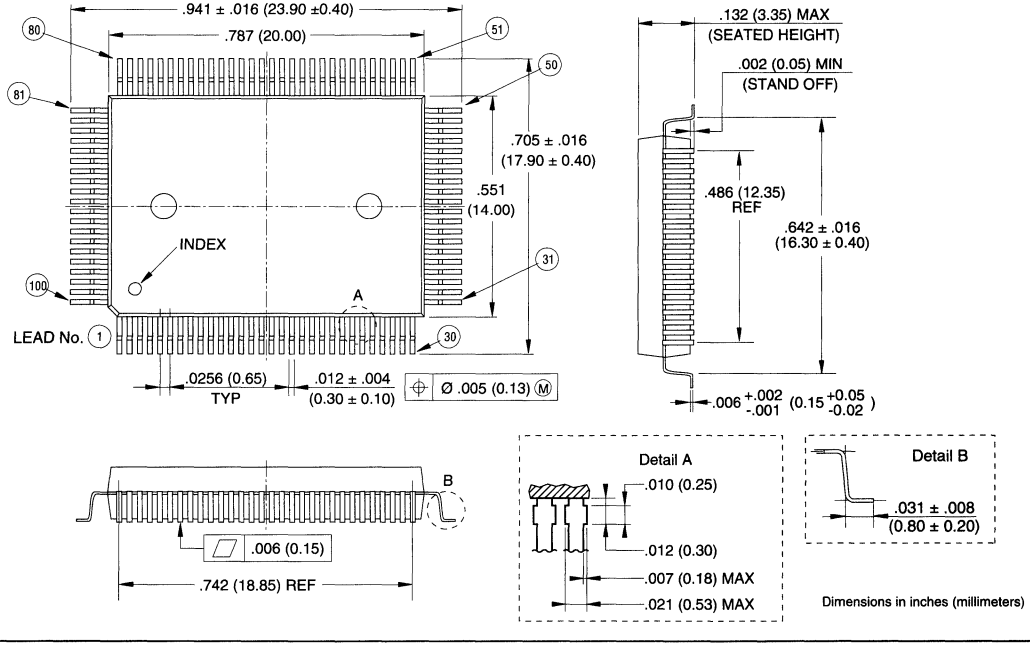
Figure 38. Test Conditions

100-Pin Plastic Flat Package



Ordering Information: MB86960APF-G

100-Lead Plastic Flat Package
(Case No. FPT-100P-M06)



MB86965

FUJITSU

ETHERCOUPLER SINGLE-CHIP ETHERNET CONTROLLER

DATA SHEET

APRIL1993

FEATURES

- Provides interface to the I/O bus of PC/XT™/AT® or compatible computers
- Optional, generic host interface to connect to industry-standard microprocessor buses
- Interface to serial EEPROM for Node ID and configuration option storage allows construction of jumperless, electronically configurable adapter cards
- Automatic polarity detection and correction on twisted-pair 10BASE-T cable
- Allows automatic selection of nonconflicting I/O address for self-installing under software control
- High-performance, packet-buffer architecture pipelines data for highest throughput
- On-chip buffer management controls buffer pointers to reduce software overhead and improve performance
- Hash filter for multicast packet reception
- Manchester encoder/decoder tolerates input jitter up to ±18 ns
- Fully compliant with ISO/ANSI/IEEE 8802-3 specifications
- Two network ports, AUI and 10BASE-T, with automatic port selection
- Integrated pulse shape, and transmit and receive filters
- Selectable 150Ω and 100Ω termination for shielded or unshielded twisted-pair cable, respectively
- Powerdown mode to reduce power dissipation in battery-powered equipment
- Low-power CMOS technology
- Single 5-volt power supply
- 160-pin plastic quad flat package (PQFP)

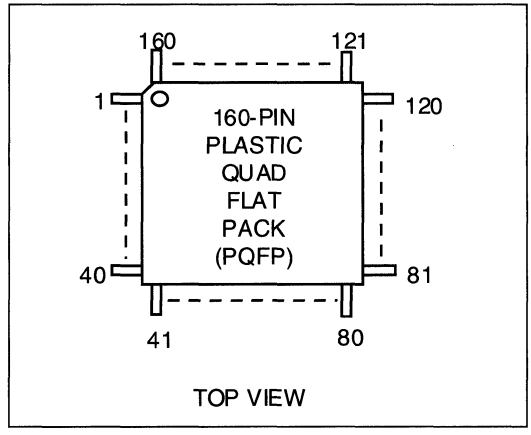
GENERAL DESCRIPTION

The MB86965 EtherCoupler™ Controller is a high-performance, highly integrated monolithic device that incorporates a network controller with buffer management, 10BASE-T transceiver with on-chip transmit and receive filters, Manchester encoder/decoder, and bus interface for a PC/XT/AT/ISA bus. EtherCoupler allows implementation of adapter solutions with as few as four chips. With its optional native bus mode for use directly on a microprocessor bus, it is ideal for use on daughter and motherboards, as well as expansion-bus adapter boards. An EEPROM can be interfaced to the chip for storage of Ethernet ID and configuration settings. EtherCoupler is designed to be configured electronically, thus eliminating the jumpers typically used to configure the system network adapters.

The buffer management architecture of the MB86965 allows packet data to access a buffer memory area simultaneously from the host and from the network media. The network controller updates all receive and transmit pointers automatically to reduce the software overhead needed to control these operations, which results in superior benchmark speed and application performance. EtherCoupler's transmit buffer is programmable as a single 2-kbyte bank or as two banks of 2, 4, or 8 kbytes each. This buffer chains multiple data packets and transmits them to the network from a single transmit command, thereby offering greater design flexibility and throughput. A ring buffer that can be sized from 4 to 62 kbytes, depending on the amount of available memory used for the transmit buffer, captures the receive packets.

The MB86965 performs pulse shaping and filtering internally, which eliminates the need for external filtering components and reduces overall system cost.

PIN CONFIGURATION



EtherCoupler is compatible with shielded and unshielded twisted-pair cables and provides outputs for receive, transmit, collision and link test LEDs. The twisted pair receive threshold can be reduced to allow an extended range between nodes in low-noise environments. Its wide range of features makes EtherCoupler the ideal device for 10BASE-T twisted-pair Ethernet.

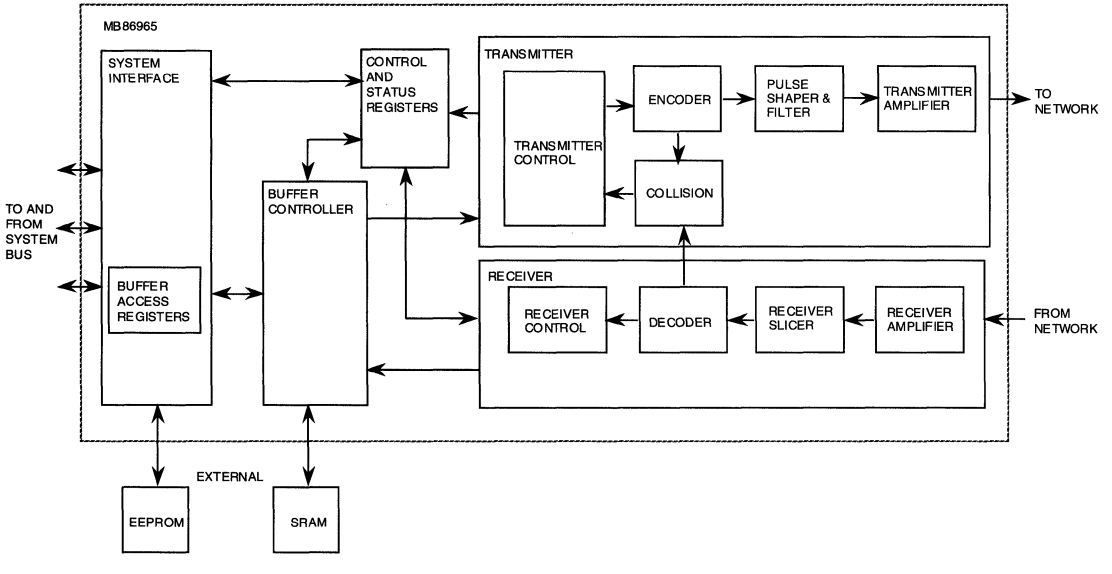
Possible configurations for the system bus interface include I/O mapping, memory mapping and DMA access, or a combination of these. With a 20 Mbyte/s bandwidth, the EtherCoupler system bus interface allows use of full throughput capacity of its packet-buffering architecture. EtherCoupler bus modes are selectable, thereby providing big or little endian byte-ordering, permitting efficient data interface with most microprocessors and higher-level protocols. The Fujitsu high-speed, low-power CMOS process is used to manufacture of the MB86965, which is furnished in a 160-pin plastic quad flat package.

FUNCTIONAL DESCRIPTION

As shown below, the MB86965 comprises five major functional blocks: System Interface, Buffer Controller, Control and Status Registers, Transmitter, and receiver. EtherCoupler's receive and transmit sections fully implement the ISO/ANSI/IEEE 8802-3 CSMA/CD specification for 10-megabit per second Ethernet. The transmitter assembles data packets for transmission and the receiver disassembles received data packets. On-chip Ethernet protocol functions include: automatic generation and stripping of the 64-bit preamble; generation and verification of 32-bit cyclic redundancy check (CRC); collision resolution by binary exponential back-off and retransmission; several modes of address recognition, error detection and reporting; and serial/parallel and parallel/serial conversions.

TYPICAL APPLICATION

Figure 1 is a block diagram illustrating the application of the MB86965 in an add-in adapter card for an ISA bus-based personal computer. The serial EEPROM provides storage for I/O base address, boot PROM address and interrupt channel as well as the Ethernet node ID. One or two 8-bit bidirectional transceivers provide data buffering between the Ethercoupler and the 8- or 16-bit system bus. A single SRAM, typically 8 or 32 kbytes, implements the local packet buffer, while an optional boot PROM allows use of the adapter in diskless environments, where the driver program must be loaded from the network. The EtherCoupler provides interfaces to 100- or 150-ohm twisted pair (10BASE-T) as



EtherCoupler Block Diagram

well as a direct AUI capability (10BASE5). An optional coaxial transceiver interface, such as Fujitsu's MBL8392A, provides additional capability for Thin Ethernet (10BASE2) networks. The MB86965 directly drives several LEDs which provide indication of adapter operational status.

For complete information on a typical adapter design, request the Hardware Reference Manual for the DK86965 EtherCoupler Designer Kit from your authorized Fujitsu Microelectronics sales representative or distributor. Schematics in electronic format, board layouts and Gerber tape for printed circuit card construction are also available for purchase as Hardware Design Kit HD86965.

PIN ASSIGNMENTS AND DESCRIPTIONS

LOGIC CONVENTION

Unless otherwise noted, a positive logic (active high) convention is assumed throughout this document, whereby the presence at a pin of a higher, more-positive voltage (nominally 5 VDC) causes assertion of the signal. An underscore, e.g., RDY indicates that the signal is asserted in the low state (nominally 0 volts). Dual-function pins have their alternate function enclosed in parentheses, e.g., RDY(RDY). Whenever a signal is separated into numbered bits, e.g., BD7, BD6, BD5, BD4, BD3, BD2, BD1 and BD0, the family of bits may also be shown collectively, e.g., as BD<7:0>.

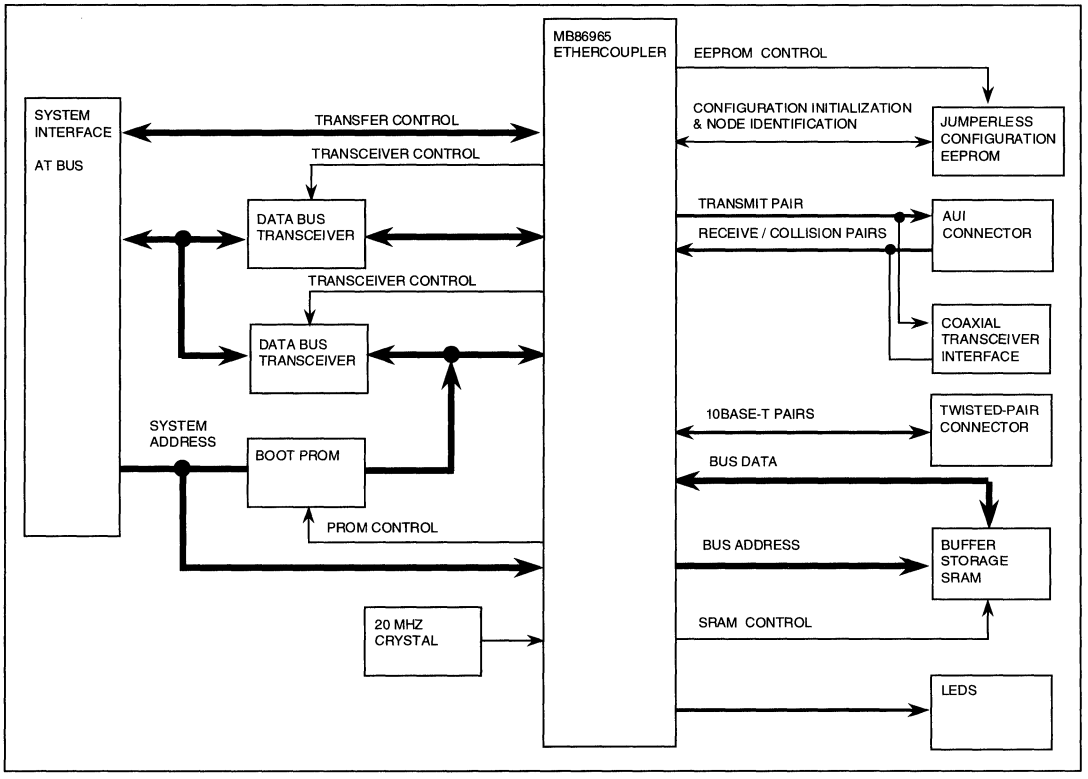


Figure 1. Typical Application, Block Diagram

PIN ASSIGNMENTS

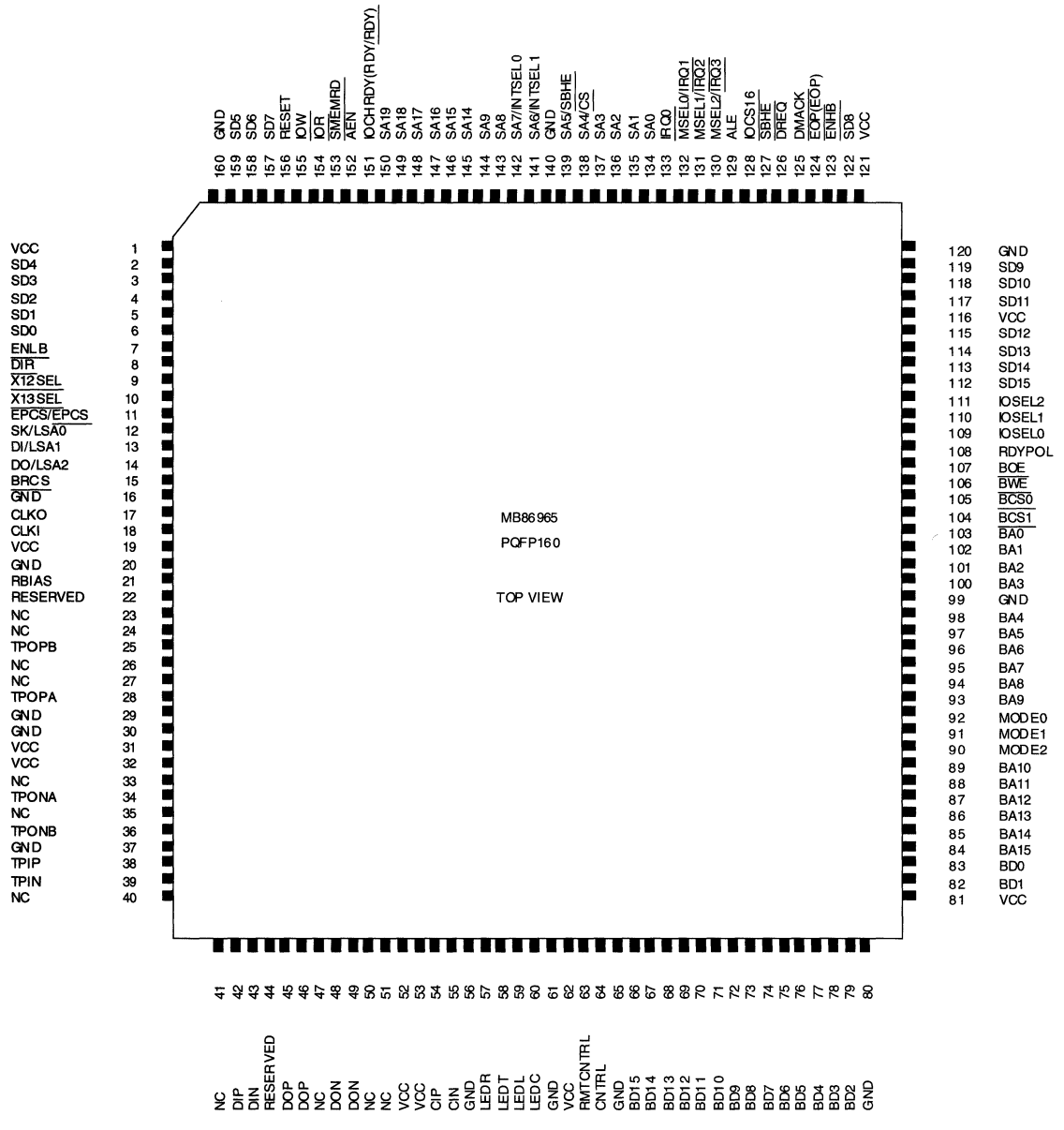


Figure 2. MB86965 Pin Assignments

PIN DESCRIPTIONS

Configuration Mode Selection

The MB86965 can be configured to match specific hardware environments, and pin functions vary according to Mode. Setting pins 90, 91 and 92 allows selection of EtherCoupler for operation in one of four predefined configurations. Operation is selectable as jumperless or requiring jumpers. Initial parameters can be stored in a bit-serial EEPROM or a byte-parallel PROM, depending on Mode. Operation as a NICE chip is also available.

CONFIGURATION PINS

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
90–92	MODE<2:0>	—	I pull-down	**MODE SELECT:** Allows selection of EtherCoupler configuration mode as shown in the **MODE** column in these tables.

No.	Bus	Pin 90	Pin 91	Pin 92	Operation	Initial Parameters
0	ISA	0	0	0	Jumperless	Stored in bit-serial EEPROM.
1	ISA	0	0	1	Jumpers	Stored in bit-serial EEPROM.
2	ISA	0	1	0	Jumpers	Stored in byte-parallel ID PROM.
3	Non-ISA	0	1	1	Jumpers	Functions identical to MB86960 NICE (Network Interface Controller with Encoder/ decoder) chip with MB86961 10BASE-T Interface.
X	–	1	X	X	–	Reserved.

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
111–109	IOSEL<2:0>	1, 2	I pull-up	**INPUT/OUTPUT BLOCK ADDRESS SELECT:** Sets the base address at which the controller is located, as follows:

IOSEL2	IOSEL1	IOSEL0	I/O BASE ADDRESS
0	0	0	260 – 27F
0	0	1	280 – 29F
0	1	0	2A0 – 2BF
0	1	1	240 – 25F
1	0	0	340 – 35F
1	0	1	320 – 33F
1	1	0	380 – 39F
1	1	1	300 – 31F

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
111–109	RESERVED	0, 3	I	**NOT USED.** These pins should be left floating, internally pulled high.

SYSTEM BUS TO INTERFACE PINS

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
112–115 117–119 122 157–159 2–6	SD<15:12> SD<11:9> SD<8> SD<7:5> SD<4:0>	0, 1, 2, 3	I/O	**SYSTEM DATA:** All data, command, and status transfers take place over this bus.
150–145 144–141 139–134	SA<19:14> SA<9:6> SA<5:0>	0, 1, 2	I	**SYSTEM ADDRESS:** Selects EtherCoupler internal register or port for read/write operations.
137–134	SA<3:0>	3	I	**SYSTEM ADDRESS:** Selects EtherCoupler internal register or port for read/write operations.
142 141	INTSEL0 INTSEL1	3	I	**INTERRUPT SELECT:** Selects the interrupt signal. Read only. Same as BMPR19<6:7>.
139 127	SBHE SBHE	3 0, 1, 2	I I	**SYSTEM BUS HIGH ENABLE:** Active low. This pin is the byte/word control line. It is used only when EtherCoupler is configured for a 16-bit data bus by the SB/SW bit, DLCR6<5>. It allows word, upper byte only or lower byte only transfers. The address select pin SA0 is used with SBHE for byte or word transfers as follows:

SB/SW	SBHE	SA0	FUNCTION
0	0	0	Word transfer
0	0	1	Byte transfer on upper half of data bus (SD15-8)
0	1	0	Byte transfer on lower half of data bus (SD7-0)
0	1	1	Reserved
1	X	X	Byte transfer (SD7-0)

138	CS	3	I	**CHIP SELECT:** Active low signal which, when set to 0, selects the EtherCoupler chip.
156	RESET	0, 1, 2, 3	I	**CHIP RESET:** Resets the chip internal pointers and initializes internal registers and logic.
154	IOR	0, 1, 2, 3	I	**INPUT/OUTPUT READ:** Active low signal from the system bus which indicates that the current bus cycle is a read operation.
155	IOW	0, 1, 2, 3	I	**INPUT/OUTPUT WRITE:** Active low signal from the system bus which indicates that the current bus cycle is a write operation.
153	SMEMRD	0, 1, 2	I	**SYSTEM MEMORY READ:** Active low signal from the system bus that indicates the current bus cycle is in a memory-read operation. Used for Boot ROM Chip Select (BRCS).
152	AEN	0, 1, 2	I	**ADDRESS ENABLE:** When asserted indicates that a DMA transfer is taking place.
124	EOP(EOP)	0, 1, 2, 3	I	**END OF PROCESS:** When asserted by the DMA controller, indicates that an entire packet has been transferred between buffer memory and the host system.
129	ALE	0, 1, 2	I	**ADDRESS LATCH ENABLE:** Provided by the system to latch valid addresses.
125	DMACK	0, 1, 2, 3	I	**DMA ACKNOWLEDGE:** Active low signal which indicates that the DMA controller is ready to transfer data between the host system and the EtherCoupler buffer memory.
15	BRCS	0, 1, 2	O	**BOOT ROM CHIP SELECT:** Active low signal which indicates that the current memory access is to Boot ROM.

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
133	IRQA	0, 1, 2, 3	O 24-ma tristate	**INTERRUPT REQUEST:** One of four interrupt request lines which indicate that EtherCoupler requires host attention after successful transmission or reception of a packet, or if any error conditions occur, including an EOP after the completion of the DMA cycle.
130–132	IRQD, IRQC, IRQB	0, 3	O 24-ma tristate	**INTERRUPT REQUEST:** In jumperless mode: three of four interrupt request lines which indicate that EtherCoupler requires host attention after successful transmission or reception of a packet, or if any error conditions occur, including an EOP after completion of DMA cycle.
130–132	MSEL<2:0>	1, 2	I	**MEMORY SELECT:** In jumper select mode: sets Boot ROM location base address.

MSEL2	MSEL1	MSEL0	ROM ADDRESS RANGE
0	0	0	C4000 – C7FFF
0	0	1	C8000 – CBFFF
0	1	0	CC000 – CFFFF
0	1	1	D0000 – D3FFF
1	0	0	D4000 – D7FFF
1	0	1	D8000 – DBFFF
1	1	0	DC000 – DFFFF
1	1	1	Decode disabled

126	DREQ	0, 1, 2, 3	O	**DMA REQUEST:** Issued to the DMA controller to indicate that EtherCoupler has data available to be read in its receive buffer, or is ready to accept data into its transmit buffer.
151	RDY(RDY)	3	O 24-ma tristate	**INPUT/OUTPUT CHANNEL READY:** This signal indicates to the host that EtherCoupler is ready to complete the requested read or write operation. Polarity of this pin is programmed by RDYPOL, pin 108. High-impedance to READY valid, or READy valid to high impedance (Tables 41 and 43). N-channel open drain.
151	IOCHRDY	0, 1, 2	O 24-ma tristate	**INPUT/OUTPUT CHANNEL READY:** This signal indicates to the host that EtherCoupler is ready to complete the requested read or write operation. RDYPOL pin must be tied to ground. N-channel open drain.
128	IOCS16	0, 1, 2	O 24-ma tristate	**INPUT/OUTPUT 16-BIT CHANNEL SIZE:** Active low signal which indicates that present data transfer is 16-bit I/O cycle. N-channel open drain.
123	ENHB	0, 1, 2	O	**ENABLE DATA HIGH BYTE:** Active low signal which enables the system data transceiver high byte.
7	ENLB	0, 1, 2	O	**ENABLE DATA LOW BYTE:** Active low signal which enables the system data transceiver low byte.
8	DIR	0, 1, 2	O	**TRANSCEIVER DIRECTION:** Active low signal sets the external transceiver direction, from chip to system (read operation). Active high signal sets the external transceiver direction from system to chip (write operation).
9	X12SEL	0, 1, 2	O	**SELECT CONFIGURATION REGISTER 1:** Active low signal pulse to read the jumper configuration register 1, located at address 0X12.

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
10	X13SEL	0, 1, 2	O	**SELECT CONFIGURATION REGISTER 2:** Active low signal pulse to read the jumper configuration register 2, located at address 0X13.
10	SB/SW	3	O	**SYSTEM BYTE / WORD BUS WIDTH:** When high, System Bus operates in 8-bit mode; when low,16-bit mode is selected. Same as DLCR6<5>.
12	SK	0, 1	O	**EEPROM SHIFT CLOCK:** With EEPROM option, this signal is generated from software, which shifts data in and out of the EEPROM.
12	LSA0	2	O	**LATCHED ADDRESS 0:** With ID PROM option, the pin provides one of three latched address lines to the ID PROM.
13	DI	0, 1	O	**EEPROM DATA IN:** With EEPROM option, this is serial data going to the EEPROM.
13	LSA1	2	O	**LATCHED ADDRESS 1:** With ID PROM option, the pin provides one of three latched address lines to the ID PROM.
14	DO	0, 1	I	**EEPROM DATA OUT:** With EEPROM option, this is serial data coming from the EEPROM.
14	LSA2	2	O	**LATCHED ADDRESS 2:** With ID PROM option, the pin provides one of three latched address lines to the ID PROM.
11	EPCS	0, 1	O	**PROM CHIP SELECT:** High signal selects EEPROM.
11	EPCS	2	O	**PROM CHIP SELECT:** Low signal selects ID PROM.
108	RDYPOL	0, 1, 2, 3	I	**READY LINE POLARITY SELECT:** Controls polarity of IOCHRDY signal at pin 151, where 0 is active low ready and 1 is active high ready.
63	RMTCNTRL	0, 1, 2, 3	O	**REMOTE CONTROL:** When RMT RST bit DLCR5<2> is set high, this pin follows RMT 0900H bit DLCR1<4>, which indicates that a complete special packet with type field = 0900H has been received. This is intended for use as a remotely controlled hardware function from other nodes in the network.
64	CNTRL	0, 1, 2, 3	O	**CONTROL:** This pin is intended as a hardware control pin programmable by the system software. Complement of CNTRL, DLCR4<2>.
127, 129, 143–150, 152, 153	RESERVED	3	I	**NOT USED.** These pins should be pulled low to ground.
7–9, 11–15, 123, 128	RESERVED	3	O	**NOT USED.** These pins should be left floating, internally pulled high.

BUFFER MEMORY INTERFACE PINS

PIN NO.	SYMBOL	MODE	TYPE	DESCRIPTION
66–79, 82–83	BD<15:2>, BD<1:0>	0, 1, 2, 3	I/O	**BUFFER MEMORY DATA BUS:** Data lines between SRAM buffer memory and EtherCoupler. This data bus configurable for 8-bit or 16-bit data size by BB/BW bit DLCR6<4>.
84–89, 93–98, 100-103	BA<15:10> BA<9:4> BA<3:0>	0, 1, 2, 3	O	**BUFFER MEMORY ADDRESS BUS:** These lines address up to 64 kbytes of buffer memory.
104	BCS1	0, 1, 2, 3	O	**BUFFER RAM CHIP SELECT 1:** Active low signal that is chip select for most significant byte of buffer memory.
105	BCS0	0, 1, 2, 3	O	**BUFFER RAM CHIP SELECT 0:** Active low signal that is chip select for least significant byte of buffer memory.
106	BWE	0, 1, 2, 3	O	**BUFFER WRITE ENABLE:** Active low, write-enable-to-buffer-memory signal output during memory write cycles.
107	BOE	0, 1, 2, 3	O	**BUFFER OUTPUT ENABLE:** Active low, output-enable-to-buffer-memory signal output during memory read cycles.

POWER AND TRANSCEIVER INTERFACE PINS

PIN NO.	SYMBOL	MODE	TYPE	
1, 19, 31, 32, 52, 53, 62, 81, 116, 121	V_{CC}	0, 1, 2, 3	I	**POWER SUPPLY:** +5 Volts ± 5%, for analog and digital circuits.
16, 20, 29, 30, 37, 56, 61, 65, 80, 99, 120, 140, 160	GND	0, 1, 2, 3	I	**GROUND:** digital and analog ground.
45, 46 48, 49	DOP DON	0, 1, 2, 3	O O	**AUI TRANSMIT PAIR:** Differential output driver pair for AUI transceiver DO circuits; output is Manchester-encoded.
42 43	DIP DIN	0, 1, 2, 3	I I	**AUI RECEIVE PAIR:** A differential input driver pair for the AUI transceiver DI circuits; input is Manchester-encoded.
54 55	CIP CIN	0, 1, 2, 3	I I	**AUI COLLISION PAIR:** A differential input driver pair for the AUI transceiver CI circuits. The input is collision signalling or signal-quality error (SQE).
28, 34 25, 36	TPOPA,TPONA TPOBP,TPONB		O	**TWISTED-PAIR OUTPUT:** Differential driver pair outputs to the twisted-pair cable. The output is pre-equalized so that no external filter is required.
38, 39	TPIP TPIN	0, 1, 2, 3	I	**TWISTED-PAIR INPUT:** A differential input pair from the twisted-pair cable.
60	LEDC	0, 1, 2, 3	O	**COLLISION LED:** Open-drain driver for the collision indicator. Output is pulled low during collision.
59	LEDL	0, 1, 2, 3	O	**LINK LED:** Open-drain driver for link integrity indicator. Output is pulled low during link test pass.
58	LEDT	0, 1, 2, 3	O	**TRANSMIT LED:** Open-drain driver for transmit indicator. Output is pulled low during transmit.
57	LEDR	0, 1, 2, 3	O	**RECEIVE LED:** Open-drain driver for the receive indicator. Output is pulled low during receive.
21	RBIAS	0, 1, 2, 3	I	**BIAS RESISTOR:** To control bias of operating circuit; pulled to ground with 12.4-kilohm ±1% pulldown resistor.
17 18	CLKO CLKI	0, 1, 2, 3	O	**CRYSTAL OSCILLATOR:** A 20-MHz crystal must be connected between these pins. [See figure 4.]
22–24, 26, 27, 33, 35, 40, 41, 44, 47, 50, 51	No Connection	0, 1, 2, 3	O	**NOT USED.** These pins should be left floating, internally pulled high.

SYSTEM CONFIGURATION

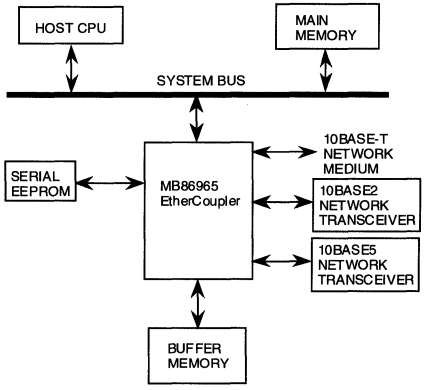


Figure 3. System Configuration, Simplified Block Diagram

As shown in Figure 3, EtherCoupler allows a highly integrated system configuration. EtherCoupler's architecture and high level of integration facilitate packet management and storage, and eliminate the need for a local microprocessor. EtherCoupler connects with the host system bus to provide command and status interfaces as well as packet data access. The host processor can directly access command and status registers when mapped into the host I/O or memory space. Data packets to be transmitted to the media initially transfer from host memory through an EtherCoupler port into a dedicated buffer memory where they are temporarily stored until transmitted. Buffer memory initially stores received data packets that are later transferred to the host memory. [Refer to the section on Control and Status Registers for identification of control and status bits of the data link control registers, DLCR0 through DLCR7, and buffer memory port register pair, BMPR8 and BMPR9.]

CONNECTION TO THE LAN MEDIA

Connection to the LAN media can be accomplished by on-board connection to a shielded or unshielded twisted pair, through the on-chip 10BASE-T transceiver.

CRYSTAL OSCILLATOR

The clock rate of 10 Mbits/s specified by the international LAN standard, ISO/ANSI/IEEE 8802-3, derives from an on-chip oscillator that is controlled by a crystal connected across pins 17 and 18 (CLKO and CLKI). Capacitance specified by the crystal manufacturer must

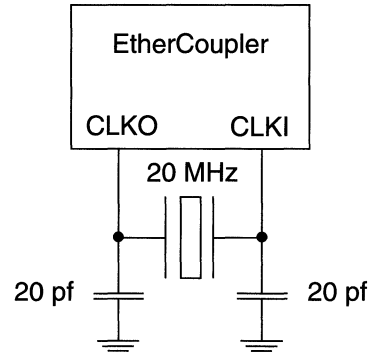


Figure 4. Crystal Oscillator Connection

be connected across pins 17 and 18 to ground, as shown in Figure 4, to stabilize the effects of stray capacitance that may vary crystal frequency. The 20-MHz clock also serves as an internal phase-locked loop (PLL) reference for decoder clock recovery. Internal clocks shut down when the PWRDN bit, DLCR7<5>, is asserted for power down mode. Use a crystal with the following specifications: quartz (AT-cut); 20-MHz; frequency/accuracy of ±50ppm at 25°C and 100ppm at 0°C to 70°C; parallel resonant with 20 pF-load in fundamental mode. Possible vendors include: Ecliptek Corp. (Costa Mesa, CA) p/n ECSM200-20.000; and M-tron Industries, Inc. (Yankton, SD) p/n MP-1 and MP-2, with 20-MHz, 50ppm over 0°C to 70°C, and 18 pF fundamental load.

SRAM CONFIGURATIONS

Figure 5 shows how to configure industry-standard SRAMs for memory implementation of packet buffers in byte and word modes. The Buffer Byte/Buffer Word (BB/BW) bit, DLCR6<4>, selects the width of the SRAM data path as 8 or 16 bits. Setting this bit to 1 selects byte-wide (8-bit) data; setting it to 0 selects word-wide (16-bit) data. The System Byte/System Word (SB/SW) bit, DLCR6<5>, selects the width of the system data path as 8 or 16 bits. Setting this bit to 1 selects byte-wide (8-bit) data; setting it to 0 selects word-wide (16-bit) data. Do not use the combination of SB/SW bit, DLCR6<5>, set to 1 (byte) and BB/BW bit, DLCR6<4>, set to 0 (word). The Buffer Size (BS1 and BS0) bits, DLCR6<1:0>, select SRAM size as 8, 16, 32 or 64 kbytes.

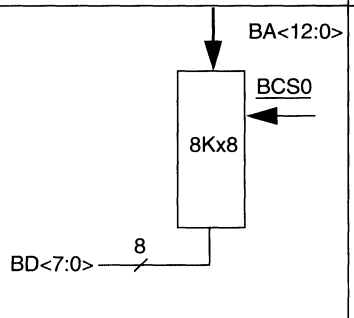
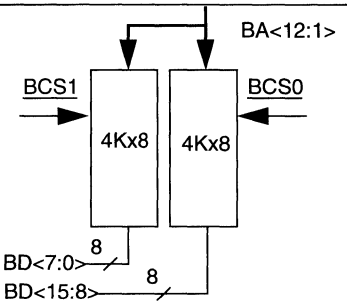
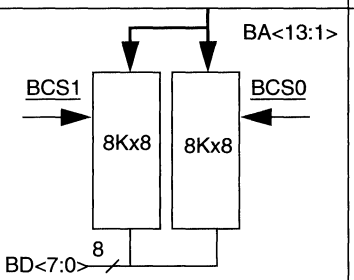
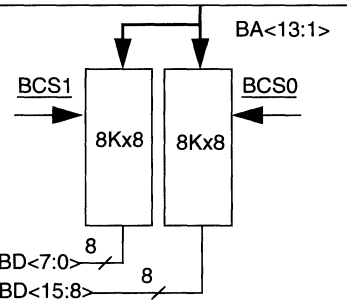
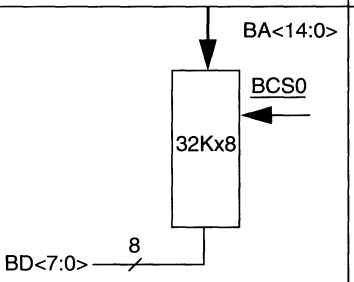
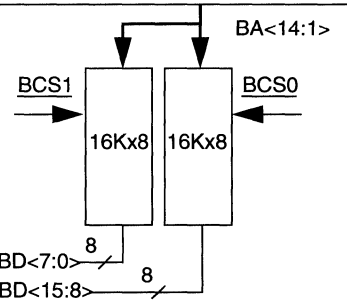
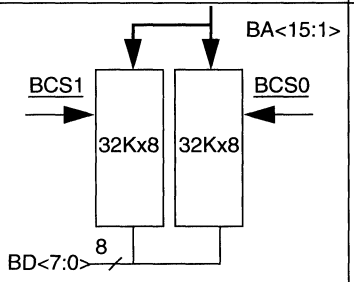
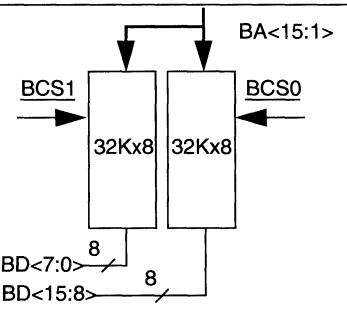
BS1 DLCR6<1>	BS0 DLCR<0>	8-BIT BUFFER BUS	16-BIT BUFFER BUS
0	0		
0	1		
1	0		
1	1		

Figure 5. SRAM Configurations

SYSTEM INTERFACE

GENERAL

The System Interface provides the interface logic necessary to connect to a PC/XT/AT/ISA bus and, via an alternate bus mode, to an x86, RISC or 680X0-type microprocessor bus. The interface supports 8- and 16-bit bus widths and byte or word transfers, as determined by the SB/SW bit, DLCR6<5>. Depending on the type of host CPU, EtherCoupler supplies the data order, MSB or LSB first (big or little endian), according to the setting of the M..LM..L/L..M bit, DLCR7<0>.

EtherCoupler supports I/O-mapping, and burst or single-transfer DMA modes. The user can select the active interrupt pin to inform the CPU of transmit and receive status conditions requiring host processing. EtherCoupler includes three sets of user-accessible registers, all of which are accessible as bytes or words.

Pins 90 to 92 allow selection and configuration of the mode in which the MB86965 operates. Specifically, when MODE<2:0> bits are set to 00H, the bus is in ISA mode with an EEPROM that stores initial parameters and jumperless operation. When MODE<2:0> bits are set to 01H the bus is set for operation with jumpers and EEPROM. When MODE<2:0> bits are set to 02H the bus is set for operation with jumpers and ID PROM. When MODE<2:0> bits are set to 03H the bus is set for generic bus operation.

REGISTER ACCESS

Direct access is available to eight registers in the device's register set, addresses xxx0H through xxx7H. Access to remaining physical addresses is through indirect addressing or bank-switching of three different register banks, for the address set XXX8H through XXXFH. Bank-switching bits reside in register 07H. The bank-switched register group comprises three sets or banks of registers: Node ID (Ethernet Address) and TDR Diagnostics; Hash Table for multicast address filtering; and Buffer Memory Access. During normal operation (excluding initialization or diagnostics), the Buffer Memory Access bank is selected, and access to other registers is not required.

BUFFER ACCESS

The Buffer Memory Port register pair BMPR8 and BMPR9 provide 8 or 16-bit data with access to the receive and transmit buffers through on-chip FIFOs. To eliminate the need for complicated directional control, FIFOs are dedicated to each direction of data transfer. Writing to the transmit buffer interleaves with reading from the receive buffer, with EtherCoupler automatically maintaining buffer memory pointers. The Buffer Memory port register pair is accessible via register address xxx8H, when bank I is selected. When using DMA, the buffer memory port is automatically selected when the DMA Acknowledge input, $\overline{\text{DMACK}}$ is asserted.

Data can transfer from the host memory to the transmit buffer, or from the receive buffer to host memory by using string moves, single-transfer programmed I/O moves, or DMA. Select the method that yields the highest system-level efficiency. A rapid transfer process results in best performance. Slow transfer could result in poor throughput and performance, and cause the receive buffer to overflow and lose packets.

I/O OPERATION

Write transmits data to BMPR10, and I/O Write will address the data to the Transmit Buffer. Read receives data on BMPR10 through I/O Read, which will load the data from the Receive Buffer.

DMA OPERATION

EtherCoupler supports single-cycle and burst DMA operation for data transfer between the host system and the dedicated buffer memory. Handshaking between EtherCoupler and external DMA is accomplished by the DREQ and DMACK signals. The end of process input, pin 124, when asserted by the system DMA controller during a transfer cycle, terminates DMA activity after completion of the current cycle. If a DMA interrupt (DLCR3<5>) is enabled, EtherCoupler generates an interrupt after completion of DMA activity.

DMA Write (Transmit)

Setting the TX DMA Enable bit, BMPR12<0>, enables DMA transfer of data packets from the host memory to the EtherCoupler transmit buffer. When invoked, DMA burst control bits BMPR13<1:0> enable burst transfers. EtherCoupler, when ready to accept data from the host, sets the DMA request output, DREQ, and the host responds by setting DMA acknowledge, DMACK, and write enable, WE, and placing data on the data bus. EtherCoupler sets the ± IOCHRDY output when ready to complete the current data-transfer cycle. (Polarity of the IOCHRDY signal and the EOP input are independently programmable.) EtherCoupler accepts the data byte/word into its Bus Write FIFO and later moves it into buffer memory. At the close of a transfer cycle, the host negates WE. In burst mode and depending on CNTRL bit, DLCR4<2>, at the next-to-last cycle,

EtherCoupler negates DREQ. The host DMA then completes the last two transfer cycles and negates DACK to close the burst. To start another burst, EtherCoupler re-asserts DREQ. The number of DMA write cycles within one burst can be 1, 4, 8, or 12 data transfers (bytes or words), depending on burst control bits BURST 1 and BURST 0, BMPR13<1:0>.

The DMA controller asserts the end of process input, EOP, concurrent with the last data-transfer cycle to indicate completion of the entire transfer process. This action sets the DMA EOP bit, DLCR1<5>, to discontinue further EtherCoupler data requests. Setting the EOP signal will also generate an interrupt. If the DMA EOP INT enable bit, DLCR3<5>, is high. The host can use this interrupt to begin action to close the process. The host should reset EtherCoupler DMA logic and clear the interrupt by resetting the DMA enable bit, BMPR12<0>.

The transmit DMA process must be closed by clearing BMPR12<0> before attempting another DMA process. Clearing the DMA EOP INT EN bit, BMPR3<5>, then automatically clears the EOP status and interrupt, removing the need to clear the interrupt separately. The host initiates packet transmission after loading packets into the buffer by loading the number of packets to be transmitted into the TX PKT CNT bits, BMPR10<6:0>, and asserting TX Start bit, BMPR10<7>.

DMA Read (Receive)

EtherCoupler indicates when it receives packets to be read with status bits or interrupts. Before reading a packet, the host processor can read the RX BUF EMPTY bit, DLCR5<6>, which if 0 indicates one or more packets in the receive buffer to read. After reading each packet, the host again checks this bit for more packets.

Before transferring a packet via DMA from the receive buffer to host memory, the host first reads the buffer four-byte receive packet header to obtain packet status and packet byte length. [Also refer to the discussion of Transmit and Receive Packet Headers.] The host calculates and loads the host DMA controller cycle counter with the number of DMA cycles needed to read the packet. The system memory starting address must also be loaded into the DMA controller. The RX DMA EN bit, BMPR12<1>, is next set to enable the DMA read operation and transfer the packet to host memory. When ready to begin this transfer, EtherCoupler sets the DMA request output DREQ, and the host responds by asserting DMA acknowledge bit, DMACK, and then I/O Read, IOR. EtherCoupler sets the IOCHRDY output when the byte/word is on the data bus, and the data transfer cycle is ready to be completed. After system memory accepts the data, the host negates IOR. EtherCoupler then "pops" the data in the Bus Read FIFO, and points the internal Bus Read pointer to the next buffer byte/word to move that data into the FIFO.

If programmed for burst operation and depending on CNTRL bit, DLCR4<2>, EtherCoupler negates DREQ two cycles before the end of the burst, then re-asserts DREQ to repeat the process, if it can transfer more data after the host negates DMACK. The number of DMA read cycles in a burst can be 1, 4, 8, or 12 data-transfer (byte or word) cycles, depending on burst control bits BURST1 and BURST0, BMPR13<1:0>. The DMA controller asserts the end of process input EOP concurrent with the last byte/word data transfer to indicate completion of the entire process. EtherCoupler then stops requesting more DMA cycles. After the DMA process, RX DMA enable must be cleared then re-asserted when the host wants to begin reading another packet from the Receive Buffer by using DMA.

When the host DMA controller asserts EOP, the DMA EOP bit, DLCR1<5>, is set and generates an interrupt, if so enabled by setting the associated int en bit, DLCR3<5>. The host can use this interrupt to close the receive DMA process. Writing 000H to the DMA En bits, BMPR12<1:0>, clears the interrupt and disables and resets the DMA, removing the need to clear the interrupt separately. The receive DMA process must be terminated before attempting another DMA process.

ETHERCOUPLER INTERFACE TO AT BUS

As shown in Figure 6, EtherCoupler provides jumpered (with ID PROM or serial ID EEPROM) and jumperless design solutions. Designed primarily for AT bus systems, EtherCoupler assumes that the program I/O mode is the most effective way to transfer data between controller and system resources.

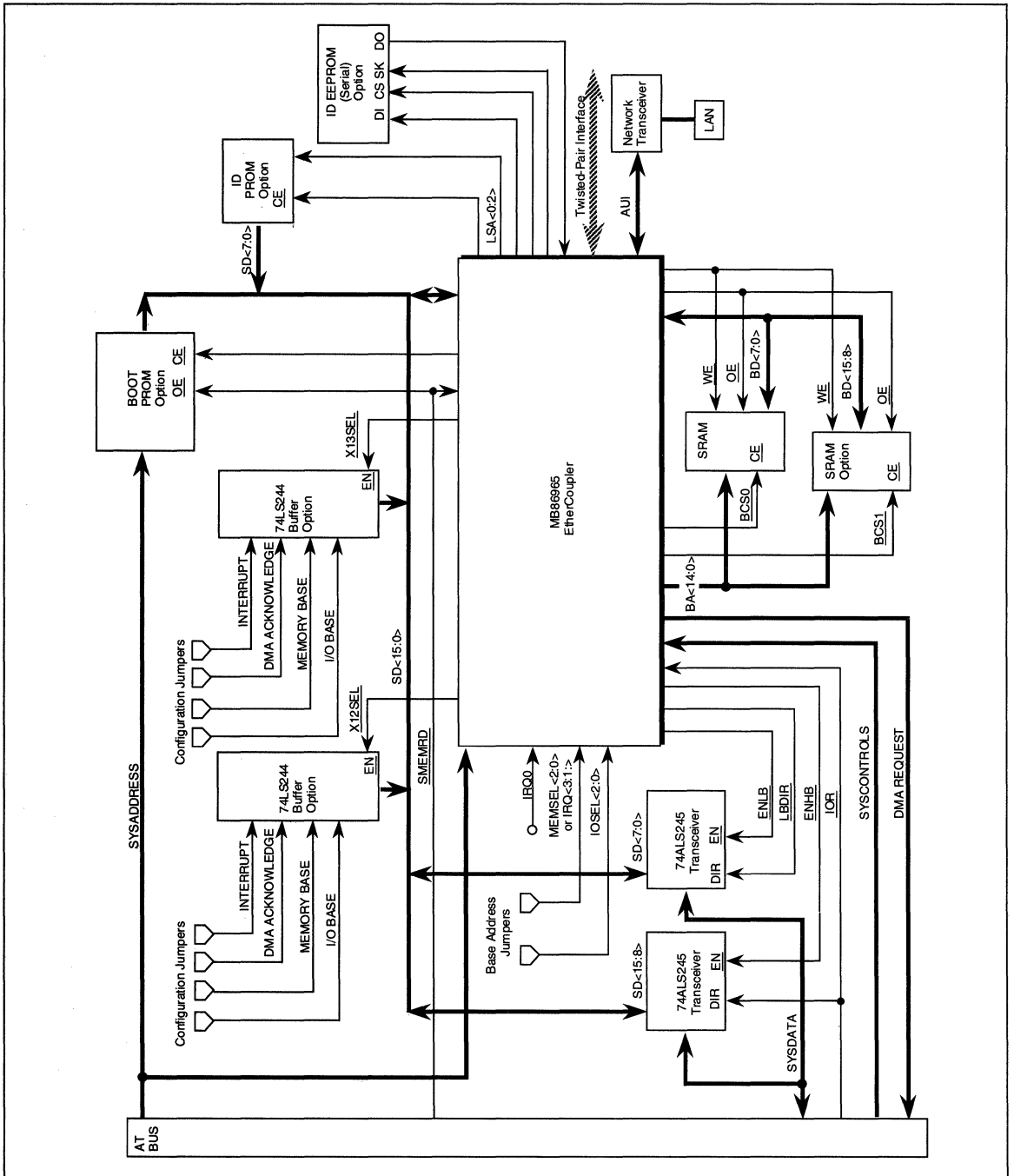


Figure 6. EtherCoupler Bus Operation Block Diagram

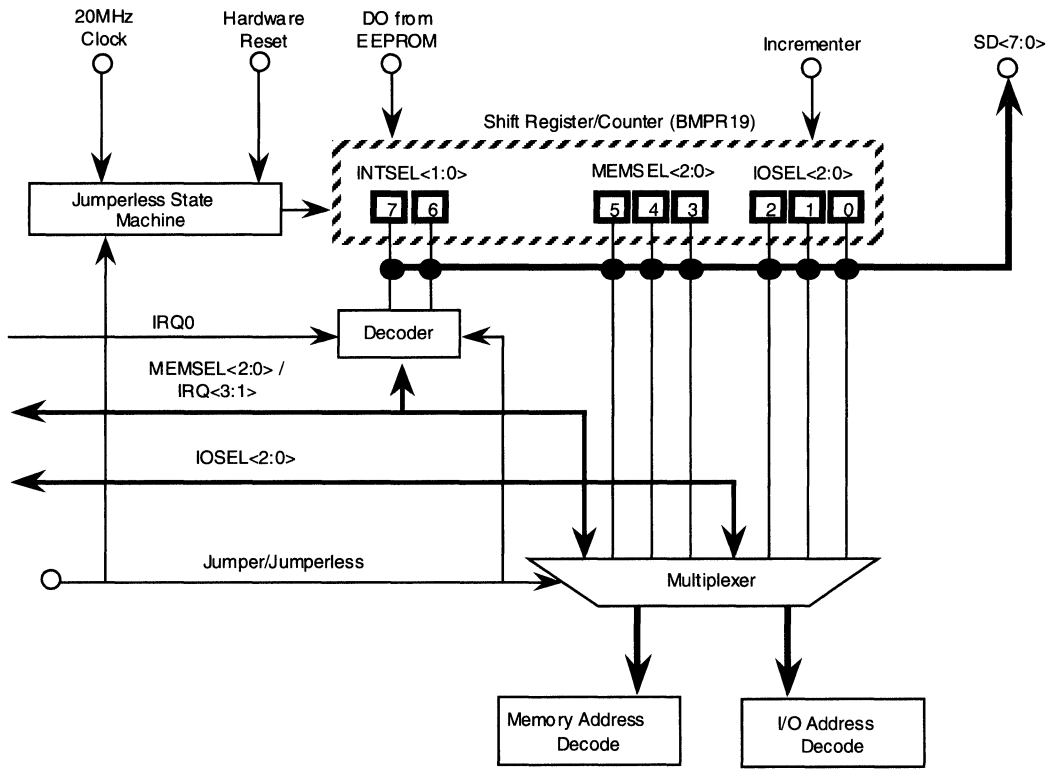


Figure 7. Jumperless/Jumpered Logic

Jumperless And Jumpered Mode Configuration And Control Registers

The jumperless EtherCoupler design approach assumes that an EEPROM is available for storage of I/O and memory base addresses, as well as system interrupt information in the first (Configuration) byte.

Jumperless/Jumpered Operation

The interrupt, I/O base address, and memory base address are set upon powerup and after system hardware reset, by first reading the configuration byte from the EEPROM into a special serial-in/parallel-out shift register/counter, as shown in Figure 7. Tables 1 through 4 provide detailed information about registers used for EtherCoupler Jumperless and Jumpered mode configuration and control.

Abbreviations that describe control and status bits are shown below.

Type	Description
R	Readable
W	Writable
N	Not used, reserved; write 0 when written.
C	Clears associated status bit and interrupt.
0/1	Initial state after hardware reset

Table 1. BMPR16 – EEPROM Control Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	0	0	**RESERVED:** Write 0.
6	ESK	W	**EEPROM SHIFT CLOCK:** Generates a shift clock signal for the EEPROM, by writing 1 or 0 from the software program. Write only.
5	ECS	W	**EEPROM CHIP SELECT:** When set to 1, generates a chip select signal for the EEPROM. Write only.
4 – 0	0	0	**RESERVED:** Write 0.

Table 2. BMPR17 – EEPROM Data Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	EDIO	W/R	**EEPROM INPUT/OUTPUT CLOCK:** When set to 1, indicates data is being input to the EEPROM. When set to 0, indicates that data is being output from the EEPROM.
6 – 0	0	0	**RESERVED:** Write 0.

Table 3. BMPR18 – IO Base Address Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 – 0	IOBA<7:0>	R	**I/O BASE ADDRESS:** When in Jumperless mode, enables storage and incrementing of IO base address. Read only.
7 – 0	X12SEL	R	**ADDRESS 12 SELECT:** When set to high in Jumpered mode, enables reading of jumpered information (address 0X12) from the board.

Register BMPR16 controls the selection and operation of the EEPROM and operates in Jumperless mode only.

Register BMPR 17 controls the input or output of the EEPROM and operates in Jumperless mode only.

Register BMPR18 temporarily stores, increments and reads out the I/O base address in Jumperless mode, when in Mode 3 operation with an EEPROM, and generates the X12SEL signal in Jumpered mode to enable reading of jumpered information from the board.

Register BMPR18 temporarily stores, increments and reads out the I/O base address in Jumperless mode, when in Mode 3 operation with an EEPROM, and generates the X12SEL signal in Jumpered mode to enable reading of jumpered information from the board.

Register BMPR19 reads the EtherCoupler jumperless configuration data in Jumperless mode, and generates the X13SEL signal in Jumpered mode to enable reading of jumpered information from the board.

Memory Base Address Configuration

Table 4 shows how BMPR19<5:3> defines the ROM Address read from the EEPROM. The process of reading the byte begins at system powerup, and is in parallel with system BIOS powerup initialization and checkout. This allows the BIOS to scan the ROM location for a valid boot ROM. If there are no memory address conflicts, the boot ROM initialization code then initializes its resources, replaces the required interrupt vectors, and returns control to system BIOS to complete system initialization.

If there are any memory address conflicts, the system may halt during powerup. If so, EtherCoupler should be removed from the system and installed in a system with no memory address conflict. This allows the user to reprogram the EEPROM with a different memory base address. An adapter card reprogrammed with a new base address can then be reinstalled in the original system. In case of I/O conflicts, EtherCoupler is software-configurable. In jumperless mode, removal of EtherCoupler from the system is unnecessary.

Table 4. BMPR19 – Jumperless Configuration Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 6	INTSEL 1 INTSEL 0	R R	**INTERRUPT SELECT:** In Jumperless mode, enables definition of the interrupt select signal. Read only.

BIT 7	BIT 6	DESCRIPTION
0	0	INT0
0	1	INT1
1	0	INT2
1	1	INT3

5 4 3	MEMSEL2 MEMSEL1 MEMSEL0	R R R	**MEMORY SELECT:** In Jumperless mode, enables ROM address decoding. Read only.

BIT 5	BIT 4	BIT 3	ROM ADDRESS DECODING
0	0	0	C4000 – C7FFF
0	0	1	C8000 – CBFFF
0	1	0	CC000 – CFFFF
0	1	1	D0000 – D3FFF
1	0	0	D4000 – D7FFF
1	0	1	D8000 – DBFFF
1	1	0	DC000 – DFFFF
1	1	1	Decode Disabled

2 1 0	IOSEL 2 IOSEL 1 IOSEL 0	R R R	**INPUT/OUTPUT SELECT:** In Jumperless mode, enables I/O Base Address decoding. Read only.
7 – 0	X13SEL	R	**ADDRESS 13 SELECT:** When set to high in Jumpered mode, enables reading of jumpered information (address 0X13) from the board.

BIT 2	BIT1	BIT 0	I/O BASE ADDRESS DECODING
0	0	0	260 – 27F
0	0	1	280 – 29G
0	1	0	2A0 – 2BF
0	1	1	240 – 25F
1	0	0	340 – 35F
1	0	1	320 – 33F
1	1	0	380 – 39F
1	1	1	300 – 31F

I/O Base Address Configuration

After successful system powerup, the software utility reads and compares the Product Signature or powerup value of the first eight registers to see if the controller is set with a nonconflicting I/O base address. Product Signature is the initial value of the first eight EtherCoupler registers.

The I/O base address is determined by bits 2–0 of the configuration byte read from EEPROM into the shift register/counter at the time of powerup. After reading from the EEPROM, hardware logic sets the shift register/counter to counter mode, and assigns a Counter Enable (Counter/Shift Register Select) bit within EtherCoupler registers to monitor the register and counter modes of this special three-bit block.

Table 4 also shows how BMPR19<2:0> defines the I/O Base Address read from the EEPROM. If the Product Signature read does match expected values, there is no conflict in the I/O address range. If there is a conflict in setting the address, the system may ignore the existence of EtherCoupler, although the software utility should continue reading the 0X12 register. Because the cell is set for counter mode (I/O Base Unlock bit, BMPR13<7>), every time the register is read, bits 2, 1 and 0 increment by one, moving the I/O base address to the next setting. The utility should read the chip for the correct Product Signature each time the register/counter counts up to the next base I/O address. This mechanism allows an adapter board to dynamically reconfigure itself to a nonconflicting I/O base address.

Once the right address is achieved, software locks the register/counter cell to register Address mode by resetting the designated Counter Enable bit. The software utility then reads the new configuration from the 0X13 register, and reprograms the EEPROM configuration byte with correct base addresses.

Interrupt Definition

Additionally, Table 4 indicates how BMPR19<7:6> defines the interrupt read from the EEPROM. Bits 6 and 7, which are used to configure interrupts, can be programmed to select any one of four interrupt lines offered at the system interface side of the EtherCoupler. The user may connect these lines to any four available system interrupt lines. The software utility tests the interrupt configuration for conflict and, if conflicting, reprograms the EEPROM bits with the next available interrupt option, and reboots the system to try again.

REGISTERS

CONTROL AND STATUS REGISTERS

The control and status registers on EtherCoupler are accessed through (direct) register addresses XXX0H through XXXFH, and (indirect) register bank-switching bits RBS1 and RBS0, DLCR7<3:2>.

Table 5. Internal Register Address Map

REGISTER BANK SWITCHING		SYSTEM ADDRESS					REGISTER	
RBS1	RBS0	SA4	SA3	SA2	SA1	SA0	Name	Description
X	X	0	0	0	0	0	DLCR0	Transmit Status
X	X	0	0	0	0	1	DLCR1	Receive Status
X	X	0	0	0	1	0	DLCR2	Transmit Interrupt Enable
X	X	0	0	0	1	1	DLCR3	Receive Interrupt Enable
X	X	0	0	1	0	0	DLCR4	Transmit Mode
X	X	0	0	1	0	1	DLCR5	Receive Mode
X	X	0	0	1	1	0	DLCR6	Configuration 0
X	X	0	0	1	1	1	DLCR7	Configuration 1
0	0	0	1	0	0	0	DLCR8	Node ID 0
0	0	0	1	0	0	1	DLCR9	Node ID 1
0	0	0	1	0	1	0	DLCR10	Node ID 2
0	0	0	1	0	1	1	DLCR11	Node ID 3
0	0	0	1	1	0	0	DLCR12	Node ID 4
0	0	0	1	1	0	1	DLCR13	Node ID 5
0	0	0	1	1	1	0	DLCR14	TDR 0 (LSB)
0	0	0	1	1	1	1	DLCR15	TDR 1 (MSB)
0	1	0	1	0	0	0	HT8	Hash Table 0
0	1	0	1	0	0	1	HT9	Hash Table 1
0	1	0	1	0	1	0	HT10	Hash Table 2
0	1	0	1	0	1	1	HT11	Hash Table 3
0	1	0	1	1	0	0	HT12	Hash Table 4
0	1	0	1	1	0	1	HT13	Hash Table 5
0	1	0	1	1	1	0	HT14	Hash Table 6
0	1	0	1	1	1	1	HT15	Hash Table 7
1	0	0	1	0	0	0	BMPR8	Buffer Memory Port (LSB)
1	0	0	1	0	0	1	BMPR9	Buffer Memory Port (MSB)
1	0	0	1	0	1	0	BMPR10	Transmit Start
1	0	0	1	0	1	1	BMPR11	16 Collisions
1	0	0	1	1	0	0	BMPR12	DMA Enable
1	0	0	1	1	0	1	BMPR13	DMA Burst, Transceiver Mode
1	0	0	1	1	1	0	BMPR14	Filter Self Receive, Transceiver Interrupt Enable
1	0	0	1	1	1	1	BMPR15	Transceiver Status
1	1	0	X	X	X	X	Reserved	Not used.
X	X	1	0	0	0	0	BMPR16	EEPROM Control. Write Only.
X	X	1	0	0	0	1	BMPR17	EEPROM Data. Read/Write.

REGISTER BANK SWITCHING		SYSTEM ADDRESS					REGISTER	
RBS1	RBS0	SA4	SA3	SA2	SA1	SA0	Name	Description
X	X	1	0	0	1	0	BMPR18	I/O Base Address. Read Only.
X	X	1	0	0	1	1	BMPR19	Jumperless Configuration. Read Only.
X	X	1	0	1	0	0	Reserved	Not used.
X	X	1	0	1	0	1	Reserved	Not used.
X	X	1	0	1	1	0	Reserved	Not used.
X	X	1	0	1	1	1	Reserved	Not used.
X	X	1	1	0	0	0	IDRB0	ID ROM Byte 0
X	X	1	1	0	0	1	IDRB1	ID ROM Byte 1
X	X	1	1	0	1	0	IDRB2	ID ROM Byte 2
X	X	1	1	0	1	1	IDRB3	ID ROM Byte 3
X	X	1	1	1	0	0	IDRB4	ID ROM Byte 4
X	X	1	1	1	0	1	IDRB5	ID ROM Byte 5
X	X	1	1	1	1	0	IDRB6	ID ROM Byte 6
X	X	1	1	1	1	1	IDRB7	ID ROM Byte 7

Table 5 summarizes the addressing scheme and provides functional selection criteria for system addressing. System address is relative to base I/O address selected by IOSEL<2:0>. Writing to a location within the optional IDROM space resets EtherCoupler internal registers and state machines. In System Word mode, data transfers 16 bits at a time on the system bus, or 8 bits at a time by using EtherCoupler byte lane controls. In 16-bit mode, even direct addresses select the registers when transferring to and from the registers. For example, address XXX0H accesses the Transmit/ Receive Status registers. Transmit Status would be on the low byte and Receive Status on the high byte. Appropriate byte-access processor instructions access high and low bytes separately.

Tables 6–11 describe control and status bits.

Table 6. Control and Status Bits, DLCR0–7

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX STATUS DLCR0	TX DONE	NET BSY	TX PKT RCD	CR LOST	JABBER	COL	16 COL	0
RX STATUS DLCR1	RX PKT	BUS RD ERR	DMA EOP	RMT 0900H	SHORT PKT ERR	ALIGN ERR	CRC ERR	RX BUF OVRFLO
TX INT ENABLE DLCR2	INT EN	0	0	0	INT EN	INT EN	INT EN	0
RX INT ENABLE DLCR3	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN	INT EN
TX MODE DLCR4	COL CTR 3	COL CTR 2	COL CTR 1	COL CTR 0	0	CNTRL & DREQ EXTND	LBC	EN TX DEFER
RX MODE DLCR5	0	RX BUF EMPTY	ACPT BAD PKTS	RX SHORT ADDR	ACPT SHORT PKTS	RMT RST	AF1	AF0
CONFIG 0 DLCR6	DLC EN	100NS / 150NS SRAM	SB/SW	BB/BW	TBS 1	TBS 0	BS 1	BS 0
CONFIG 1 DLCR7	ECID 1	ECID 0	PWRDN	RDYPN SEL	RBS 1	RBS 0	EOPPOL	M..L/L..M

Table 7. Control and Status Bits, BMPR8–15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BUF MEM PORT (LSB) BMPR8	7	6	5	4	3	2	1	0
BUF MEM PORT (MSB) BMPR9	15	14	13	12	11	10	9	8
TX START BMPR10	TX START	TX PKT CNT 6	TX PKT CNT 5	TX PKT CNT 4	TX PKT CNT 3	TX PKT CNT 2	TX PKT CNT 1	TX PKT CNT 0
16 COLLISIONS BMPR11	0	0	0	0	0	16 COL CNTRL 2	16 COL CNTR L 1	16 COL CNTRL 0
DMA ENABLE BMPR12	0	0	0	0	0	0	RX DMA EN	TX DMA EN
DMA BURST/ TXVR MODE BMPR13	I / O BASE UNLOCK	LOWER SQUELCH THRESH	LINK TEST EN	AUI / TP	AUTO PORT SEL	STP / UTP	BURST 1	BURST 0
FILTER SELF RX BMPR14	INT EN	INT EN	INT EN	0	0	SKIP PKT	INT EN	FILTER SELF RX
TXVR STATUS BMPR15	RLD	LLD	RJAB	RMT PORT	RXI POL REV	0	SQE	0

Table 8. Control and Status Bits, BMPR16–19

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EEPROM CONTROL BMPR16	0	ESK	ECS	0	0	0	0	0
EEPROM DATA BMPR17	EDIO	0	0	0	0	0	0	0
IO BASE ADDRESS INCREMENT & X12SEL BMPR18	0	0	0	0	0	0	0	0
JUMPERLESS & X13SEL BMPR19	INTSEL1	INTSEL0	MEMSEL2	MEMSEL1	MEMSEL0	IOSEL2	IOSEL1	IOSEL0

Table 9. Control and Status Bits, DLCR8–15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NODE ID 0 DLCR8	7	6	5	4	3	2	1	0
NODE ID 1 DLCR9	15	14	13	12	11	10	9	8
NODE ID 2 DLCR10	23	22	21	20	19	18	17	16
NODE ID 3 DLCR11	31	30	29	28	27	26	25	24
NODE ID 4 DLCR12	39	38	37	36	35	34	33	32
NODE ID 5 DLCR13	47	46	45	44	43	42	41	40
TDR 0 DLCR14	7	6	5	4	3	2	1	0
TDR 1 DLCR15	N/A (0)	N/A (0)	13	12	11	10	9	8

Table 10. Control and Status Bits, HT8–15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HASH TABLE 0 HT8	7	6	5	4	3	2	1	0
HASH TABLE 1 HT9	15	14	13	12	11	10	9	8
HASH TABLE 2 HT10	23	22	21	20	19	18	17	16
HASH TABLE 3 HT11	31	30	29	28	27	26	25	24
HASH TABLE 4 HT12	39	38	37	36	35	34	33	32
HASH TABLE 5 HT13	47	46	45	44	43	42	41	40
HASH TABLE 6 HT14	55	54	53	52	51	50	49	48
HASH TABLE 7 HT15	63	62	61	60	59	58	57	56

Table 11. Control and Status Bits, Packet Buffer Headers

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TRANSMIT PACKET HEADER								
TX LENGTH (LSB) TPH1	7	6	5	4	3	2	1	0
TX LENGTH (MSB) TPH2	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8
RECEIVE PACKET HEADER								
PKT STATUS RPH1	N/A (0)	N/A (0)	GOOD PKT	RMT 0900H	SHORT ERR	ALIGN ERR	CRC ERR	N/A (0)
RESERVED RPH2	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)
RXLENGTH (LSB) RPH3	7	6	5	4	3	2	1	0
RXLENGTH (MSB) RPH4	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8

DATA LINK CONTROL REGISTERS

Status and control bits for EtherCoupler Transmitter and Receiver sections are located in Data Link Control registers DLCR0 through DLCR7.

Transmit Status Register

As shown in Table 12, this register provides transmit status for the host processor. The system can enable interrupts based on setting (active high) of bits 7, 3, 2, or 1 of this register by setting the corresponding interrupt enable bits in the Transmit Interrupt Enable register, DLCR4.

Writing 1 to bits 7, 3, 2, and 1 clears this register, which can generate interrupts. Writing 0 to these bits has no effect; only EtherCoupler control logic can set these bits. Clearing the bit that causes an interrupt clears the bit and the interrupt. Because two or more status conditions may occur simultaneously, the interrupt routine must read and act on all status conditions that are set.

One method to clear interrupts is to read the contents of the status register, then write the same value back to the register, thus clearing all bits that were set. Another technique is to clear each status bit separately, by writing its mask (interrupt enable) to the register. This might be done as the corresponding interrupt service is performed. Note that wholesale clearing of all status bits by writing FFH to the register is not recommended, because this action may clear a just-set status that has not yet been read by the system. Note also that the Transmitter must be idle and TX DONE, DLCR0<7>, must be cleared by writing 1 to it, before starting the Transmitter by writing 1 to TX START bit, BMPR10<7>.

Table 12. DLCR0 — Transmit Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX DONE	RC0	**TRANSMIT DONE:** This bit is set high when all packets in the active TRANSMIT BUFFER have been successfully transmitted to the LAN media, or skipped due to excessive collisions. Can generate interrupts if enabled by DLCR2<7>.
6	NET BSY	R	**NET BUSY:** This is a real-time image of the Carrier Sense signal of the Receiver.
5	TX PKT RCD	RC0	**TRANSMIT PACKET RECEIVED:** Indicates that a good packet was received by EtherCoupler shortly after transmission was completed. This is used to indicate self-reception of the packet. This bit is cleared as each transmission begins, or by writing 1 to it.
4	CR LOST	R0	**CARRIER LOST:** This bit is set if the receive Carrier Sense input is negated during a packet transmission. This can be caused by a collision or a shorted LAN medium. It is automatically cleared as each transmission begins.
3	JABBER	RC0	**JABBER:** When active high, indicates excessive transmit length is detected by JABBER timer. Can generate interrupts if enabled by INT EN bit, DLCR2<3>.
2	COL	RC0	**COLLISION:** This bit will assert during transmission of a data packet if a collision occurs on the network. The Buffer Controller will automatically retirements the current packet after collisions up to 16 times. The user may read the number of consecutive collisions in collision counter, DLCR4<7:4>. Can generate interrupts if enabled by INT EN bit, DLCR2<2>.
1	16 COL	RC0	**16 COLLISIONS:** This bit is set after the sixteenth unsuccessful transmission of the same packet. Can generate interrupts if enabled by INT EN bit, DLCR2<1>.
0	0	R0	**RESERVED:** Write 0.

Receive Status Register

Table 13. DLCR1 — Receive Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	RX PKT	RC0	**RECEIVE PACKET:** Set when a new receive packet is stored in the Receive Buffer. Can generate interrupts if enabled by INT EN bit, DLCR3<7>.
6	BUS RD ERR	RC0	**BUS READ ERROR:** Set when a ready response cannot be issued within 2.4 milliseconds after the – SMEMRD signal is asserted. Occurs when reading an empty buffer. Can generate interrupts if enabled by INT EN bit, DLCR3<6>.
5	DMA EOP	RC0	**DMA END OF PROCESS:** Set when the host DMA asserts the EOP pin indicating that the process is finished. When set, inhibits further assertion of DREQ. Cleared by writing 00H to BMPR12, or by writing 1 to this bit. Can generate interrupts if enabled by INT EN bit, DLCR3<5>.
4	RMT 0900H	RC0	**REMOTE CONTROL PACKET RECEIVED:** This bit is set if a packet is received with 0900H in its Length/Type field (two bytes following the source address, received MSB first). Can generate interrupts if enabled by INT EN bit, DLCR3<4>.
3	SHORT PKT ERR	RC0	**SHORT PACKET ERROR:** This bit is set when a packet is received with less than 60 bytes, excluding its Preamble and CRC fields. Such a packet usually indicates a collision has truncated its original length, since IEEE 802.3 minimum length is 60 bytes. Can generate interrupts if enabled by INT EN bit, DLCR3<3>.
2	ALIGN ERR	RC0	**ALIGNMENT PACKET ERROR:** This bit will assert if a packet is received with an alignment error, meaning there were 1 to 7 extra bits at the end of the packet. Such an occurrence usually indicates a collision, or a faulty transceiver. Can generate interrupts if enabled by INT EN bit, DLCR3<2>.
1	CRC ERR	RC0	**CRC PACKET ERROR:** This bit is set if a packet is received with a CRC error. This usually indicates a collision has corrupted the packet. Can generate interrupts if enabled by INT EN bit, DLCR3<1>.
0	RX BUF OVRFLO	RC0	**RECEIVE BUFFER OVERFLOW:** This bit will be set if the Receive Buffer becomes full and must reject a packet for lack of space. Can generate interrupts if enabled by INT EN bit, DLCR3<0>.

As shown in Table 13, this register contains eight status bits which can generate interrupts if enabled by the corresponding bit in DLCR3. Five of these bits report the status of the most recently received packet accepted for storage in the Receive Buffer. Bit 7, RX PKT, is set whenever a new packet is successfully received and stored in the buffer. One bit reports reception of a special packet with 0900H in its type field. Other bits in this register report buffer overflow, DMA end of process, and bus read error. Bits 1, 2 and 3 indicate errors, if any, detected in the packet. If ACPT BAD PKTS bit, DLCR5<5> or ACPT SHORT PKTS bit, DLCR5<3> are set allowing acceptance of a bad packet, these error indicators will be stored in the Status Byte of the Receive Packet Header. If DLCR5<5> and/or DLCR5<3> are both 0, all packets with detected errors are automatically discarded and not stored in the buffer.

The bits in this register are cleared by writing 1 to the bit. Writing 0 to these bits has no effect; only EtherCoupler control logic can set these bits. Clearing the bit that causes an interrupt clears the bit and the interrupt. Because two or more status conditions can occur simultaneously, the interrupt routine must read and act on all status conditions that are set. One method to clear interrupts is to read the contents of the status register, then write the same value back to the register, thus clearing all bits that were set. Another technique is to clear each status bit separately, by writing its (interrupt enable) mask to the register. This might be done as the corresponding interrupt service is performed. Note that wholesale clearing of all status bits by writing FFH to the register is not recommended, because this action may clear a just-set status that has not yet been read by the system.

Transmit Interrupt Enable Register

Table 14. DLCR2 — Transmit Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables TX DONE to generate interrupt. Also see DLCR0<7>.
6	0	N0	**RESERVED:** Write 0.
5	0	N0	**RESERVED:** Write 0.
4	0	N0	**RESERVED**: Write 0.
3	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables JABBER to generate an interrupt. Also see DLCR0<3>.
2	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables COL to generate an interrupt. Also see DLCR0<2>.
1	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables 16 COL to generate interrupt. Also see DLCR0<1>.
0	0	N0	**RESERVED:** Write 0.

Receive Interrupt Enable Register

Table 15. DLCR3 — Receive Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables RX PKT to generate interrupt. Also see DLCR1<7>.
6	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables BUS RD ERR to generate interrupt. Also see DLCR1<6>.
5	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables DMA EOP to generate interrupt. Also see DLCR1<5>.
4	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables RMT 0900H to generate interrupt. Also see DLCR1<4>.
3	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables SHORT PKT ERR to generate and interrupt. Also see DLCR1<3>.
2	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables ALIGN ERR to generate interrupt. Also see DLCR1<2>.
1	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables CRC ERR to generate interrupt. Also see DLCR1<1>.
0	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables RX BUF OVERFLO to generate interrupt. Also see DLCR1<0>.

As shown in Table 14, this register contains the bits that enable the status bits in DLCR0 to generate interrupts. Bit 4 extends the DMA Request from the next-to-last to the last transfer cycle. Only bits 7, 3, 2, and 1 can generate interrupts; the other interrupt enable bits are not used.

As shown in Table 15, this register provides control for enabling interrupts based on the setting of status bits in DLCR1, the Receive Status register.

Table 16. Network Error Monitoring Modes

ACPT BAD PKTS DLCR5<5>	ACPT SHORT PKTS DLCR5<3>	INT EN SHORT PKT ERR DLCR3<3>	INT EN ALIGN ERR DLCR3<2>	INT EN CRC ERR DLCR3<1>	Mode
0	0	0	0	0	Normal, nominator mode.
0	0	X	X	X	Error interrupts only, if enabled.
0	1	0	X	X	Save short packets if otherwise error-free in buffer. Interrupts only for alignment and CRC errors, if enabled. RX PKT bit DLCR1<7> set high if short packet received.
1	0	0	0	0	Save packets with short, alignment or CRC errors in buffer. RX PKT bit DLCR1<7> set high if packet with error received.
All others					Not used.

Transmit Mode Register

Table 17. DLCR4 — Transmit Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	COL CTR 3	R*	**COLLISION COUNT 3 thru 0:** Indicate the number of consecutive collisions encountered by the current transmit packet. Read only. (* Initial value is not predictable until first packet transmits.)
6	COL CTR 2	R*	
5	COL CTR 1	R*	
4	COL CTR 0	R*	
3	0	N0	**RESERVED.** Write 0.
2	DREQ EXTEND	RW1	**DMA REQUEST EXTEND:** When high, extends DMA Request until last transfer cycle.
	CNTRL	RW0	**CONTROL OUTPUT:** When low, the complement to this bit is for general use as the CNTRL signal, available on EtherCoupler pin 64. When low, DMA Request extends until next-to-last transfer cycle.
1	LBC	RW1	**LOOPBACK CONTROL:** This bit controls encoder/decoder loopback function. A zero on this bit places EtherCoupler in internal loopback mode.
0	EN TX DEFER	RW0	**ENABLE TRANSMIT DEFER:** Program this bit low for normal network operation. When high, the transmitter will not defer to traffic on the network, and will ignore the collision indications.

Table 16 shows details on Network Error Monitoring modes.

As shown in Table 17, this register contains two control bits associated with transmission, a general-purpose control bit that drives an EtherCoupler pin, and extends the DMA request, and a collision counter.

Table 18. Collision Count

COLLISION COUNT	16 COL DLCR0<1>	COL CTR3 DLCR4<7>	COL CTR2 DLCR4<6>	COL CTR1 DLCR4<5>	COL CTR0 DLCR4<4>	COL DLCR0<2>
0	0	0	0	0	0	0
1	0	0	0	0	1	1
2	0	0	0	1	0	1
3	0	0	0	1	1	1
4	0	0	1	0	0	1
5	0	0	1	0	1	1
6	0	0	1	1	0	1
7	0	0	1	1	1	1
8	0	1	0	0	0	1
9	0	1	0	0	1	1
10	0	1	0	1	0	1
11	0	1	0	1	1	1
12	0	1	1	0	0	1
13	0	1	1	0	1	1
14	0	1	1	1	0	1
15	0	1	1	1	1	1
16	1	0	0	0	0	1

Table 18 shows details on collision counting.

Receive Mode Register

As shown in Table 19, this register contains six bits that control receiver function, and one Receive Buffer status bit. Status bit RX BUF EMPTY, DLCR5<6>, is necessary to the software routine, which reads receive packets from the buffer. It tells the host routine whether there are any packets in the Receive Buffer that are complete and ready-to-read. In a multitasking system, this indicator would be used in conjunction with an interrupt when RX PKT asserts, which means a packet has arrived in memory. The interrupt would be used to start the routine that reads packets from the buffer.

As this routine begins, the interrupt on RX PKT can be disabled to prevent unneeded interrupts. After the first packet is read from the buffer, the RX BUF EMPTY bit would be read, to see if more packets have come in (packets may, at times, arrive in bursts). If the buffer is not empty, another packet would be read out, and this procedure repeated until the buffer is empty. After emptying the buffer, the host clears RX PKT, then re-enables interrupts on RX PKT, checks the buffer status one more time (because a packet can arrive at any time), then exits to do other tasks. Note that the packet header can reflect acceptance of a short packet (bytes 3 to 59).

Two of the control bits allow reception of packets with certain types of errors. The ACPT BAD PKTS bit, when set, causes the Receiver to retain and store in the buffer packets with CRC, alignment or short-length errors, provided that there was no indication of collision during reception. Likewise, the ACPT SHORT PKTS bit, when set, allows the retention of short packets down to and including only six bytes in length, excluding Preamble and CRC, provided that there was no indication of collision during reception and no alignment or CRC error.

Under normal operation, packets with less than 60 bytes, the IEEE 802.3 lower limit, would be discarded. These functions are provided for diagnostic purposes. Packets are accepted only if both the address filter and error filter are passed. Packets with no content errors, i.e., short, alignment or CRC, are accepted without regard to collision indications. Normally Node ID is six bytes, except if RX SHORT ADDR bit DLCR5<4> is set high, in which case only the first five bytes of the Node ID are checked.

Table 19. DLCR5 — Receive Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	0	N0	**RESERVED:** Write 0.
6	RX BUF EMPTY	R1	**RECEIVE BUFFER EMPTY:** Status bit which indicates that the Receive Buffer does not have any complete packets to read. (Read only.)
5	ACPT BAD PKTS	RW0	**ACCEPT BAD PACKETS:** When set high, allows packets with CRC, and/or alignment errors or packets that are short, to be saved into the Receive Buffer for analysis. Otherwise such packets would be discarded automatically by the Receiver and removed from the buffer.
4	RX SHORT ADDR	RW0	**RECEIVE SHORT ADDRESS:** When set high, instead of customary 48-bit NODE ID address filter, only first 40 bits of NODE ID are compared.
3	ACCPT SHORT PKTS	RW0	**ACCEPT SHORT PACKETS:** When set high, allows short packets (with less than 60 bytes, excluding Preamble and CRC, i.e. below IEEE minimum length) to be saved into the Receive Buffer. Otherwise such packets would be discarded automatically by the Receiver and removed from the buffer.

ACPT BAD PKTS	ACPT SHORT PKTS	SHORT PKT ERR DLCR1<3>	ALIGN ERR DLCR1<2>	CRC ERR DLCR1<1>	ERROR INTERRUPT
0	0	—	—	—	Accept
0	1	Accept	—	—	Accept
1	X	Accept	Accept	Accept	—

2	RMT RST	RW0	**REMOTE RESET:** When set high, enables remote reset of Receiver.
1	AF1	RW1	**ADDRESS FILTER MODE:** These two bits control the address filtering on incoming packets. Note that self reception of broadcast and multicast packets is prohibited except in Accept all packets and loopback modes. When LBC is low (loopback mode), broadcast packets can be self-received, except in Reject All Packets mode.
0	AF0	RW0	

AF1	AF0	Acceptable Address Description
0	1	NODE ID, Broadcast, Multicast, and 2nd-24th bits of NODE ID.
1	0	NODE ID, Broadcast, Multicast, and Hash Table.
0	0	Reject all packets.
1	1	Accept all packets.

Table 20. Reception Destination Address Filtering

Receiving From Other Nodes								
AF1 DLCR5 <1>	**AF0** DLCR5 <0>	**LBC** DLCR4 <1>	**FILTER SELF RX** BMPR14 <0>	**Node ID Match*** Yes	**Node ID Match*** No	**Broadcast Address**	**Multicast (bit 0=1) and** Node ID <23:1>	**Multicast (bit 0=1) and** Hash Table
0	0	X	X	—	—	—	—	—
0	1	0	X	—	—	—	—	—
0	1	1	X	Accept	—	Accept	Accept	—
1	0	0	X	—	—	—	—	—
1	0	1	X	Accept	—	Accept	—	Accept
1	1	0	X	—	—	—	—	—
1	1	1	0	Accept	Accept	Accept	Accept	Accept
1	1	1	1	Accept	Accept	Accept	Accept	Accept
Receiving Own Transmission								
AF1 DLCR5 <1>	**AF0** DLCR5 <0>	**LBC** DLCR4 <1>	**FILTER SELF RX** BMPR14 <0>	**Node ID Match*** Yes	**Node ID Match*** No	**Broadcast Address**	**Multicast (bit 0=1) and** Node ID <23:1>	**Multicast (bit 0=1) and** Hash Table
0	0	X	X	—	—	—	—	—
0	1	0	X	Accept	—	Accept	Accept	—
0	1	1	X	Accept	—	—	—	—
1	0	0	X	Accept	—	Accept	—	Accept
1	0	1	X	Accept	—	—	—	—
1	1	0	X	Accept	Accept	Accept	Accept	Accept
1	1	1	0	Accept	Accept	Accept	Accept	Accept
1	1	1	1	—	—	—	—	—

* A NODE ID match occurs when the incoming packet has a destination address whose first bit is a zero, and whose second through forty-eighth bits match bits 1–47 respectively of EtherCoupler's Node ID Registers.

As shown in Table 20, packet destination address filtering depends on the programming of Address Filter bits AF1 and AF0, Loopback Control bit LBC, and self-receive filter bit, Filter Self RX. Received packet addresses can be filtered by Node ID, Broadcast, Multicast plus bits 23 through 1 of Node ID, and/or Multicast plus Hash Table. To be accepted, a packet must not only pass requirements for the address filter but also error filter requirements. [Also refer to Table 30 and the discussion of Filter Self Receive Register BMPR14.]

Configuration Registers 0 and 1

Table 21. DLCR6 — Configuration Register 0

BIT	SYMBOL	TYPE	DESCRIPTION
7	DLC EN	RW1	**DATA LINK CONTROL ENABLE:** When low, enables EtherCoupler Receiver and Transmitter sections. This bit must be set high during initialization, and set low to enable loopback testing and operation on the network. Program Node ID and Hash Table only when this bit is high.
6	100 NS/ 150 NS	RW0	**SRAM CYCLE TIME:** Controls the SRAM time cycle. When high, selects 100 ns; when low, selects 150 ns.
5	SB / SW	RW1	**SYSTEM BYTE/WORD BUS WIDTH:** When high, system bus will operate in 8-bit data mode; when low, 16-bit data mode is selected. Also see BB/BW below.
4	BB / BW	RW1	**BUFFER BYTE/WORD WIDTH:** When high, buffer memory will operate in 8-bit data mode; when low, 16-bit data mode is selected.

SB / SW	BB / BW	System	Buffer
0	0	word	word
0	1	word	byte
1	0	Do not use	Do not use
1	1	byte	byte

3 2	TBS1 TBS0	RW1 RW0	**TRANSMIT BUFFER SIZE:** Selects size of Transmit buffers.

TBS1	TBS0	Transmit Buffer Quantity	Size, each TX Buffer (kbytes)	Size, total TX Buffer (kbytes)
0	0	1	2	2
0	1	2	2	4
1	0	2	4	8
1	1	2	8	16

1 0	BS1 BS0	RW1 RW0	**BUFFER SIZE:** Selects physical size of total SRAM buffer memory for transmit and receive functions.

BS1	BS0	SRAM size (kbytes)
0	0	8
0	1	16
1	0	32
1	1	64

Table 22. DLCR7 — Configuration Register 1

BIT	SYMBOL	TYPE	DESCRIPTION
7 6	ECID1 ECID0	R1 R1	**ETHERCOUPLER IDENTIFICATION:** When both set high, indicates to software that EtherCoupler rather than another Fujitsu product is being used as controller.
5	PWRDN	RW1	**POWERDOWN:** When set high, enables power to the chip for all functions; when set low, places chip in powerdown mode for power conservation.
4	RDYPNSEL	R 0/1	**READY PIN SELECT:** Reads the state of RDY POL signal at EtherCoupler pin 108.
3 2	RBS1 RBS0	RW0 RW0	**REGISTER BANK SELECT:** Provides the indirect address for selecting one of three sets of registers to access when the physical register address is xxx8H - xxxFH. The lower seven registers are not bank-selectable.

RBS1	RBS0	Registers
0	0	DLCR0 thru DLCR7, DLCR8 thru DLCR15
0	1	DLCR0 thru DLCR7, HT8 thru HT15
1	0	DLCR0 thru DLCR7, BMPR 8 thru BMPR15
1	1	Reserved.

1	EOPPOL	RW0	**EOP PIN SIGNAL POLARITY:** When high, the EOP pin is active-high; when low, EOP is active-low.
0	M..L / L.M	RW0	**BYTE ORDER CONTROL:** Selects byte lane ordering for packet data in the buffer (applies only in System Word mode). In both Most.Least and Least.Most modes, the first and second bytes of the packet, as well as its non-transmitted buffer header, will appear in the same word on the system bus. When this bit is high (M..L mode), the first and all odd-numbered bytes of a packet and its header appear on the high byte of the system bus. When low, the first and all odd-numbered bytes of a packet appear on the low byte. Note that header bytes are also swapped.

As shown in Tables 21 and 22, system configuration bits are found in these two registers. Among the configuration controls found here are physical memory size, partitioning between transmit and receive buffers, widths of memory and system busses, byte lane control, and powerdown control. Most configuration parameters are programmed only during initialization, after power start and hardware reset.

Software engineers, who want to use the same node driver for EtherCoupler, NICE and EtherStar controllers from Fujitsu, should note that the driver can determine which chip is being used, by reading DLCR7 or DLCR6 after hardware reset. EtherCoupler reads E0B6H (E0H or F0H for DLCR7 and B6H for DLCR6, when in byte mode); NICE reads 30B6H or 20B6H; and EtherStar reads 0000H.

Powerdown mode saves power when EtherCoupler is not in use. When ready to place the EtherCoupler chip in Powerdown mode, first write 1 to DLC EN, DLCR6<7>, to turn off the Receiver and Transmitter, then write 0 to PWRDN, DLCR7<5>. To exit the Powerdown mode, write 1 to PWRDN. Register contents are preserved, unless hardware is reset. Hardware reset also terminates the Powerdown mode.

Byte-order control provided by Most..Least/Least..Most bit, DLCR7<0>, provides compatibility with various higher-level protocols, such as TCP/IP and XNS. These protocols may have a different order for transmission of the bytes within a word. When M..L/L..M is low, the least-significant byte of the word transmits first, followed by the most-significant. When M..L/L..M is set high, the byte order reverses. This feature applies only when the system bus operates in 16-bit (word) mode.

The byte-order control works by reversing, or not reversing, the bytes of all words as they pass between the buffer memory and the system bus. Thus all data stored in the Transmit Buffer or retrieved from the Receive Buffer is affected, including nontransmitted headers. This control bit does not affect EtherCoupler registers other than Buffer Memory Port registers, BMPR8 and BMPR9. When using this feature, ensure the reversal of header information as well as packet data in the software driver code. See Table 23 for examples of using least..most and most..least byte ordering.

Table 23. Byte Ordering

DATA <15:8>	DATA <7:0>
For Transmit Packet	
Least....Most	
Transmit Length, high byte	Transmit Length, low byte
Destination Address, 2nd byte	Destination Address, 1st byte...
Source Address, 2nd byte	Source Address, 2nd byte...
Length Field, low byte	Length Field, high byte
Data Field, 2nd byte	Data Field, 1st byte
Most....Least	
Transmit Length, low byte	Transmit Length, high byte
Destination Addr, 1st byte	Destination Addr, 2nd byte...
Source Addr, 1st byte	Source Addr, 2nd byte...
Length Field, high byte	Length Field, low byte...
Data Field, 1st byte	Data Field, 2nd byte...
For Receive Packet	
Least....Most	
Unused, reserved	Receive Packet Status
Receive Length, high byte	Receive Length, low byte...
Destination Address, 2nd byte	Destination Address, 1st byte...
Source Address, 2nd byte	Source Address, 1st byte...
Length Field, low byte	Length Field, high byte
Data Field, 2nd byte	Data Field, 1st byte
Most....Least	
Receive Packet Status	Unused; reserved
Receive Length, low byte	Receive Length, high byte
Destination Addr, 1st byte	Destination Addr, 2nd byte...
Source Addr, 1st byte	Source Addr, 2nd byte...
Length Field, high byte	Length Field, low byte...
Data Field, 1st byte	Data Field, 2nd byte
Shaded items in numerically reversed byte order.	

NODE ID REGISTERS

The Node ID Registers are accessed in register bank "0" at register addresses xxx8H - xxxDH. During node initialization, the unique Ethernet address assigned to the node loads into these registers. The first register at xxx8H corresponds to the first byte of the Node ID, or the first address byte to be received as a packet arrives from the network. If EtherCoupler is configured to do so via Address Filter bits, DLCR5<1:0>, the destination address field of an incoming packet compares with the Node ID stored in these registers. The packet is accepted, if it passes the error filter and there is a match.

The Node ID registers are readable and writable registers, and should not be accessed while the Receiver is enabled. To avoid interaction with the Receiver, access the Node ID registers only when DLC EN, DLCR6<7>, is 1. It is recommended that the Node ID registers be written and read only during initialization before enabling the Receiver, i.e., before writing 0 to DLC EN. The address contained in the Node ID registers is used only for receive (destination) address filtering, not for the source address of outgoing packets. The system provides outgoing packet addresses as part of the packet data. Within each byte, bits are transmitted and received on the network in a least-significant-bit-first order.

Time Domain Reflectometry (TDR) Counter

The TDR Counter approximately indicates the location of a fault on the network, if one exists. When a node transmits, a short or open on the network causes a reflected signal to the node receiver, which can sometimes be detected. The reflection causes failure of the carrier sense or detection of a false collision. Time domain reflectometry allows estimates of the distance along the network cable from the node to the fault.

The TDR Counter counts the number of transmitted bits before occurrence of a collision or loss of carrier sense, whichever comes first. If neither occurs during packet transmission, the count clears. The elapsed time represents twice the signal delay from node to fault. An open on the network may cause a false collision, whereas a short usually causes loss of carrier sense. The TDR Count comes from DLCR14 (the least-significant byte) and DLCR15 (the most-significant byte). Only the lower 14 bits of the counter are equipped, which is more than is needed for an IEEE or Ethernet LAN. The top two bits, DLCR15<7:6>, are always 0.

To perform the TDR fault test, first enable interrupts for TX DONE, by setting DLCR2<7> high. An alternative to use the interrupt is to poll the TX DONE bit, looking for a high level. Set the 16 Collisions register, BMPR11, to 07H for this test (no halt, skip-failed packet). Clear status bits by writing FF86H to the Receive and Transmit Status registers. Next, try to transmit a packet length of 600 or more bits. Up to 16 attempts may be made automatically, if collisions are indicated. Upon completion of the transmission attempts, TX Done goes high, generating an interrupt, if enabled. When this occurs, read the Transmit Status register and the TDR register.

Interpreting The Results

If the count is zero, no fault was detected. If the count is greater than zero, but smaller than the packet length, a cable fault my exist. If the count is less than 525, a real collision may have occurred during test. Real collisions normally occur within the first 65 bytes of the packet, including preamble. Note the error messages, COL and CR LOST. COL high suggests a cable open, whereas CR LOST suggests a short. Repeat the measurement several times, throw out any anomalous values, and average the rest. A cluster of readings at about the same value is a strong indicator of a valid fault measurement. If such a cluster of readings occurs, multiply the average of the cluster by 39 feet to estimate the distance from the node to the fault. [39 feet = (100 ns x 0.8 x 186,282 miles/second x 5280 feet/mile)/2; this assumes the network is mostly coaxial cable with signal propagation speed of approximately 0.8 x C, the speed of light.]

HASH TABLE

The Hash Table provides a way to filter incoming multicast packets so the host processor need not process packets that are not of interest. The principal behind this filtering process is based on the arrangement of a large number of elements of an array, or database, to facilitate searching for elements associated with a given key or datum. The hash function is a mathematical or logical function that maps all elements in a domain onto a smaller domain called the hash table.

Assume this hashing function as an example: treat the multicast address as a nonnegative 48-bit integer, divide this number by 64 and take the remainder. This function maps all multicast addresses into a 64-element hash table because the remainder must be integer values 0 through 63. Applying this hashing function results in taking the least-significant six bits of the multicast address as an integer. In the hash table, for each element, 0 through 63, a single bit is stored to indicate if the address is accepted (1) or rejected (0). If,

for example, the node belongs to three multicast groups, only three or fewer of the hash table elements store ones, and the rest store zeroes. The scheme allows the acceptance of any number of addresses, including all of them. However, while this filters out most nonspecific addresses, there may be addresses not of interest used on the network that also fall into the accept elements, so filtering may be imperfect.

The actual hashing function used in EtherCoupler is to calculate the CRC on the multicast address and take the most-significant six bits of this calculation. The six bits are used to address the elements of the hash table. If a one is stored in an element of the table, associated packets are accepted. The hash filter criteria are only used on multicast addresses, which all start with a one. Node IDs that start with a zero are not filtered by the hash filter. The broadcast address, a special case of the multicast set wherein all the bits are ones, are accepted anyway unless the Reject All Packets mode is selected.

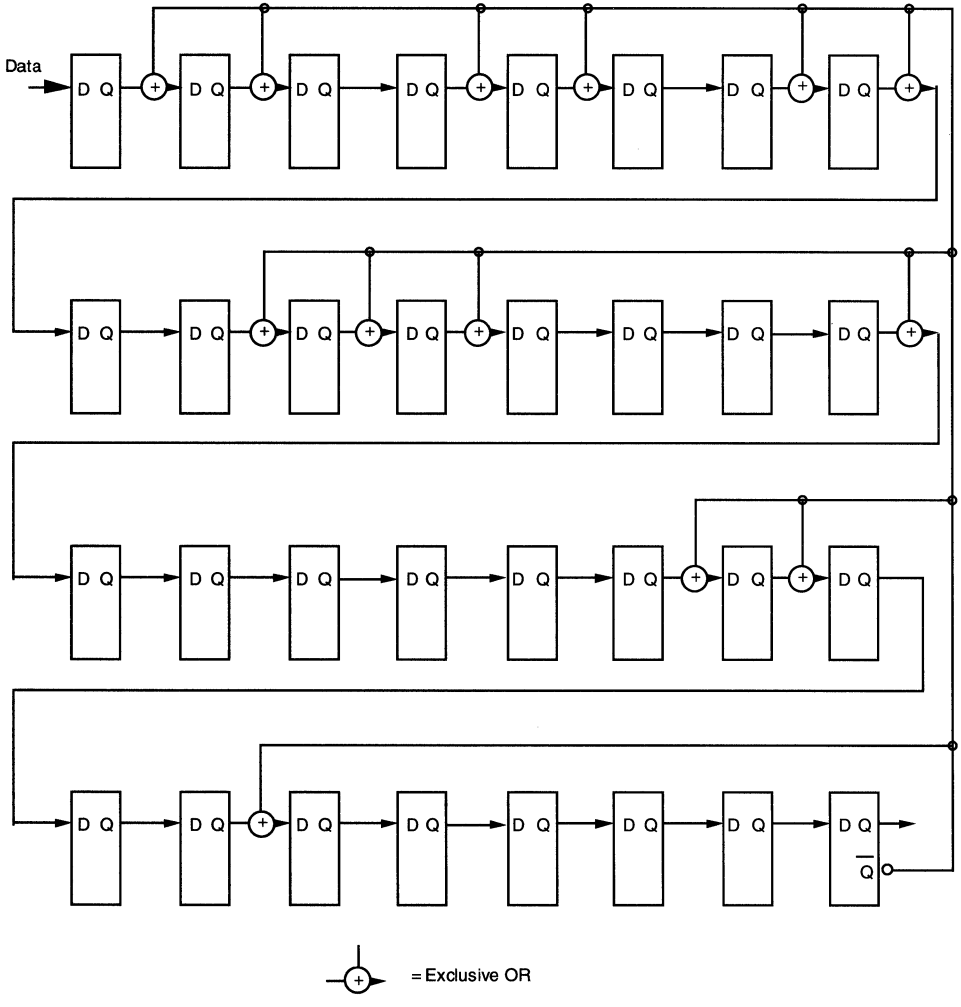


Figure 8. CRC Register Core

Figure 8 shows the Cyclical Redundancy Check (CRC) register core, which is a modified shift-right register used to generate and check CRCs. While some controllers share a single core between transmitter and receiver, EtherCoupler has one core for the generator and one core for the checker, thus allowing concurrent operation during self-receive.

To begin the calculation, the register is first set to all ones. For the generator case, as the packet transmits, data is clocked serially into the left-hand end of the register, starting with 48 bits of the destination address (the Preamble is skipped). After the last bit of the data field clocks into the register, the CRC calculation finishes. The feedback line is then forced low by the NOR gate, and the register becomes a simple shift-right register. Its contents then shift out serially, and are transmitted while appending the CRC to the end of the packet. Calculation for the CRC checker begins similar to CRC generation, by feeding the incoming data into the register. But the CRC field of the packet also feeds the calculation. The result is a fixed constant in the register, if no CRC error occurs.

For the Hash Filter, after the last bit of the destination address clocks into the register, the left-hand six register bits store in another register used to address the Hash Table elements. The left-most bit is most significant. The left-most three bits are used as the Hash Table register address, and the right-most three bits are used as the bit address within a register byte. Such selection of a Hash Table element yields a 1 in the table to indicate that the packet will be accepted, if it is a multicast packet (first bit of destination address equals 1), and passes the error filters.

The hash filter is used only when the Address Filter mode select bit AF1 is 1 and mode select bit AF0 is 0, selecting the Node ID, Broadcast, Multicast + Hash Table mode. Like the Node ID registers, Hash Table registers should only be accessed when the Receiver is disabled, i.e., when DLC EN is high, to avoid interaction with the Receiver. (Software code examples showing how to calculate entries for the Hash Table are available through Fujitsu sales offices.) There are eight bytes of registers in the Hash Table containing 64 one-bit elements, as shown in the Control and Status Table 11.

TRANSMIT AND RECEIVE PACKET HEADERS

Buffer memory is partitioned into Transmit and Receive sections, which store Packet Headers that precede associated outgoing and incoming packet information.

The Transmit Packet Header stored in the first two bytes of the Transmit Buffer reflects length characteristics of the current outgoing packet. Subsequent Transmit Buffer bytes store the contents of Destination ID, Source ID, Length, and Data fields of the outgoing packet.

The Receive Packet Header stored in the first four bytes of the Receive Buffer reflects packet conditions and length characteristics of the current incoming packet. (Refer to the discussion of Receive Status register DLCR1 for received errors.) Subsequent Receive Buffer bytes store the contents of Destination ID, Source ID, Length, and Data fields of the incoming packet.

Table 24. Receive Packet Header Conditions

CONDITION	N/A (bit 7)	NA (bit 6)	GOOD PKT (bit 5)	RMT 0900H (bit 4)	SHORT PKT ERR (bit 3)	ALIGN ERR (bit 2)	CRC ERR (bit 1)	NA (bit 0)
GOOD PACKET	0	0	1	X	X	X	X	X
GOOD PACKET WITH TYPE = 0900H	0	0	1	1	X	X	X	X
SHORT ERROR PACKET	0	0	0		1			
ALIGNMENT ERROR PACKET	0	0	0			1		
CRC PACKET ERROR	0	0	0				1	
RECEIVE BUFFER OVERFLOW ERROR	0	0	0					1
As indicated by shading in the table, EtherCoupler may detect multiple errors as they occur simultaneously, and then reflect their status in the Receive Packet Header.								

Table 24 identifies possible conditions for incoming packets and describes the contents of the Receive Packet Header byte under such conditions. [Also see Table 11, Control and Status Bits, Packet Buffer Headers.]

Transmit Packet Length

An 11-bit integer indicates the number of bytes in the packet to be transmitted, excluding Preamble and CRC fields generated by EtherCoupler.

Receive Packet Status

The receive packet header comprises one byte of packet status, an unused byte and two bytes (11 bits) for packet length in bytes. Bits 1 through 4 of the status byte are an image of the same bits in Receive Status register, DLCR1, with respect to the packet that follows. Bit 5 is the GOOD PKT bit, which when set to 1 indicates that no errors were detected in the packet. Bits 0, 6 and 7 are unused and are always set to 0.

Receive Packet Length

The third and fourth bytes of the receive packet header indicate the total number of bytes in the stored packet data.

BUFFER MEMORY PORT REGISTERS

Buffer Memory Port registers BMPR8 and BMPR9 provide the host with access to buffer memory. While EtherCoupler is on the network, Register Bank Select bits RBS1 and RBS0, DLCR7<3:2>, may be set to 1 and 0, respectively, to facilitate access to buffer memory.

Writing a byte/word to BMPR8 transfers that data to the currently addressed location in the transmit buffer, and increments the transmit buffer pointer to point to the next byte/word. Reading a byte/word from this port transfers the contents of the currently addressed location in the receive buffer to the host, and increments the receive buffer pointer to point to the next byte/word.

BMPR9 is used only in word mode as the high byte of the word. In word mode, all transfers must be 16-bits wide, as the Buffer Memory Port register does not support byte-wide transfers in this mode. As required, other registers can be accessed word-wide, high-byte-only or low-byte-only.

Transmit Start Register

Table 25 describes Transmit Start register, BMPR10, which contains the TX START bit and the TX PKT CNT bits. Writing a 1 to the TX START bit immediately starts the Transmitter. Transmit Packet Count is a seven-bit binary integer written by the host to indicate the number of packets in the transmit buffer to be transmitted. The Transmit Start register should be written only when the transmitter is idle, but can be read at any time. TX START is always read as a 1.

Table 25. BMPR10 – Transmit Start Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX START	W0	**TRANSMITTER START:** Writing 1 to this bit commands the Transmitter to start transmitting packets loaded into the transmit buffer. Before doing so, the Transmitter must be idle (not busy with another buffer).
6 – 0	TX PKT CNT 6 – 0	RW0	**TRANSMIT PACKET COUNT:** A binary integer written by the system to indicate the number of packets contained in the transmit buffer for transmission. This information can be loaded at the same time the TX START bit is set high. As the Transmitter finishes transmitting each packet, this counter is decremented. The value can be read by the system to see how many packets remain to be transmitted.

Table 26. BMPR11 – 16 Collisions Control Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 – 3	0	RW0	**RESERVED:** Write 0.
2	16 COL CNTRL 2	RW0	**16 COLLISIONS CONTROL:** Masks the internal logic for 16 COL CONTRL0 BMPR11<1>. If this bit is set to 0, EtherCoupler halts when the 16th collision occurs. If this bit is set to 1, EtherCoupler does not halt when the 16th collision occurs.
1	16 COL CNTRL1	RW0	**16 COLLISIONS CONTROL:** Restarts transmission when set to 1. Is set to 0 by EtherCoupler before transmitting a packet, when 16 COL CNTRL 2 set to 0.
0	16 COL CNTRL 0	RW0	**16 COLLISIONS CONTROL:** Retransmit or throw away this transmitted packet, when the 16th collision is met on the transmitted packet. When set to 0, retransmit this packet. When set to 1, throws away this packet.

16 COL CNTRL 2 (BIT 2)	16 COL CNTRL1 (BIT 1)	16 COL CNTRL 0 (BIT 0)	Description
0	0	X	Halt on 16 collisions.
0	1	0	Retransmit the packet, following a halt.
0	1	1	Throw away this packet and resume transmitting, following a halt.
1	X	0	Don't halt; retransmit current packet.
1	X	1	Don't halt; throw away current packet; and go to next packet.

16 Collisions Control Register

Table 26 describes 16 Collisions Control register, BMPR11, which controls action taken when each of 16 consecutive attempts to transmit a packet are met with collision. The 16 Collisions Control register serves as a mode-select register and an action command register. As a mode select register, two functions are selectable: automatic continuation, or halt after 16 collisions. If automatic continuation is selected, there is an option to continue attempting to transmit the same packet or skip to the next packet. If halt is enabled, Transmitter restarts after a halt by writing an action code listed in Table 27.

Table 27. Collision Action Codes Written to BMPR11

ACTION CODE	ACTIONS
02H or 03H	**MODE SETUP:** Halt after 16 collisions.
02H	**COMMAND:** Resume transmitting, repeat failed packet. For use following a halt. Terminates the halt. Instructs Transmitter to resume transmitting by repeating the failed packet. The collision counter is reset, allowing up to 16 additional attempts to be made. Transmitter will again halt after 16 collisions.
03H	**COMMAND:** Resume transmitting, skip failed packet. For use following a halt. Terminates the halt. Instructs Transmitter to skip the failed packet and resume transmitting with the next packet in the buffer. The collision counter is reset, allowing up to 16 additional attempts to be made. If there is no next packet, the Transmitter deactivates, setting TX DONE bit, DLCR0<7>, as it does so. Transmitter halts after 16 collisions.
06H	**MODE SETUP:** Continue automatically after 16 collisions, repeat failed packet. Note that if the network medium disconnects, transmission attempts usually result in false collision detection. Under this condition, this mode causes Transmitter to continue attempting transmission of the same packet indefinitely. Interrupt or periodic polling of the status bits could detect this condition.
07H	**MODE SETUP:** Continue automatically after 16 collisions, skip failed packet. Note that this mode results in failure to transmit some packets, because it skips a packet that has had 16 consecutive collisions. While this condition is rare on a healthy network, it does occur occasionally.

DMA Enable Register

Table 28. BMPR12 – DMA Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 – 2	0	0	**RESERVED:** Write 0.
1	RX DMA EN	WR0	**DMA RECEIVE ENABLE:** When set to 0, disables DMA read. When set to 1, enables DMA read.
0	TX DMA EN	WR0	**DMA TRANSMIT ENABLE:** When set to 0, disables DMA write. When set to 1, enables DMA write.

RX DMA EN	TX DMA EN	ACTIONS
0	0	Clear or terminate DMA activity, DMA EOP status bit and associated interrupt, if any. Normally used as response to End of Process (DMA EOP) interrupt.
0	1	Enable Transmit Write DMA.
1	0	Enable Receive Read DMA.

Table 28 describes DMA Enable register, BMPR12, a write-only register that enables or clears Receive Read DMA or Transmit Write DMA.

Table 29 describes DMA Burst and XVR Mode register, BMPR13, which selects the burst length for DMA operation, and programs the 10BASE-T Transceiver modes. Each burst is one word or one byte, depending on System Byte/System Word mode selected, DLCR6<5>. Writing code 00H, 01H, 02H or 03H to the register selects burst length as 1, 2, 4, or 12 transfers.

DMA Burst and Transceiver Mode Register (BMPR13)

Table 29. BMPR13 – DMA Burst and Transceiver Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	I / O BASE UNLOCK	WR1	**I/O BASE UNLOCK:** When set to 1, enables the I/O Counter for I/O space change. When the bit is set to 1, an I/O read address X12H increases the I/O space 32 bytes at a time. The I/O space change is between 260H and 3FFH. When set to 0, this I/O incremental function is disabled. Any I/O address read as X12H does not change the selected space.
6	LOWER SQLCH THRESH	WR0	**LOWER SQUELCH THRESHOLD:** When set to 1, reduces twisted-pair squelch threshold by 4.5 dB. When set to 0, twisted-pair squelch threshold is normal.
5	LINK TEST EN	WR0	**LINK TEST ENABLE:** When set to 1, disables transmit and receive link integrity test functions. When set to 0, enables link integrity test.
4	AUI / $\overline{TP}$	WR0	**AUI /TP PORT SELECT:** When AUTO PORT SELECT bit, BMPR13<3>, is set to 1, the Manual Port Select mode is in effect. When set to 1, the AUI port is selected. When set to 0, the TP port is selected.
3	AUTO PORT SEL	WR0	**AUTOMATIC PORT SELECTION:** When set to 0, Automatic Port Selection mode is in effect. EtherCoupler defaults to the AUI port if twisted-pair link integrity fails. When set to 1, allows manual port selection via AUI/TP bit, BMPR13<4>, which determines the active port.
2	STP / $\overline{UTP}$	WR0	**STP / UTP SELECT:** When set to 1, selects 150 Ω termination for shielded twisted pair. When set to 0, selects 100 Ω termination for unshielded twisted pair
1 0	BURST 1 BURST 0	WR0 WR0	**BURST CONTROL:** Selects the burst length for DMA operation. Each burst is one word or one byte, depending on System Byte/System Word mode selected, DLCR6<5>.

BURST 1	BURST 0	Burst Length (Transfers)
0	0	1
0	1	4
1	0	8
1	1	12

Filter Self Receive Register (BMPR14)

Table 30. BMPR14 – Filter Self Receive Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables RLD, DLCR15<7>, to generate an interrupt.
6	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables LLD, DLCR15<6>, to generate an interrupt.
5	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables RJAB, DLCR15<5>, to generate an interrupt.
4	0	0	**RESERVED:** Write 0.
3	0	0	**RESERVED:** Write 0.
2	SKIP PKT	WR0	**SKIP RECEIVE PACKET:** Flushes one receive packet. EtherCoupler adjusts the system read pointer to the beginning of the next received packet. The new pointer points to an empty buffer if there are no incoming packets, and remains unchanged if it points to an empty packet.
1	INT EN	RC0	**INTERRUPT ENABLE:** When high, enables SQE, DLCR15<1>, to generate an interrupt.
0	FILTER SELF RX	WR1	**FILTER SELF RECEIVE:** When set to 1, disables the Accept All Packets mode Self Receive function. When set to 0, enables the self receive function in Accept All Packets mode.

Table 30 describes Filter Self Receive register, BMPR14. [Also refer to Table 20 and the detailed description of Receive Mode register, DLCR5, for more information about the Filter Self Receive function.]

Writing 04H to this register commands the Buffer Controller to skip the balance of the current receive packet in memory. The bit can then be read to determine completion of the skip process is complete (within 300 ns). If there is another packet, the bit returns to 0 when the chip is ready to read the next packet or, if there is not another packet, to stop reading. Do not use this feature before reading at least four times from the beginning of the packet, nor if there are eight or fewer bytes left of the packet in the buffer; doing so may corrupt the receive buffer pointers.

Regardless of whether EtherCoupler is in byte or word mode, the system has to read four times from the receive buffer so that the SKIP PKT function can operate properly. The SKIP PKT function cannot be used when the receive packet contains only two bytes when the system in byte mode, or two words when the system in word mode. Those bytes or words move into system FIFO, and the System Read Pointer points at the next packet location.

As shown in Table 30, this register provides control for enabling interrupts based on the setting of status bits in BMPR15, the Transceiver Status Register.

Transceiver Status Register (BMPR15)

Table 31. BMPR15 –Transceiver Status Register

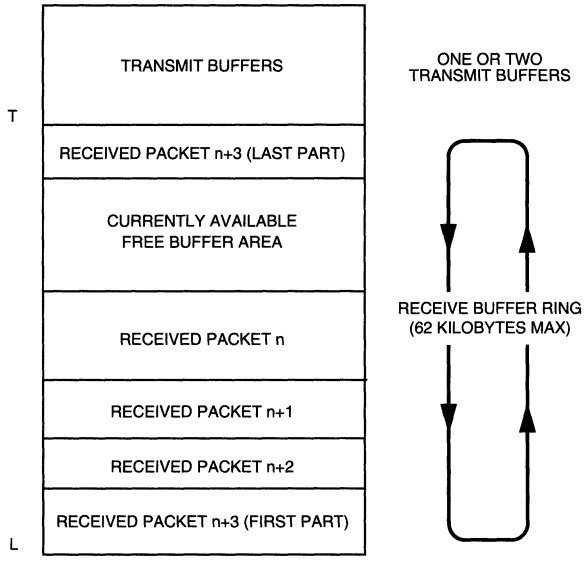
BIT	SYMBOL	TYPE	DESCRIPTION
7	RLD	WR0/1	**REMOTE LINKDOWN:** When set to 1, indicates that remote port is in linkdown condition. Can generate interrupts if enabled by Interrupt Enable bit BMPR14<7>.
6	LLD	WR0/1	**LOCAL LINKDOWN:** When set to 1, indicates that port is in linkdown condition. Can generate interrupts if enabled by Interrupt Enable bit BMPR14<6>.
5	RJAB	WR0/1	**REMOTE JABBER:** When set to 1, indicates that remote port is in Jabber condition. Can generate interrupts if enabled by Interrupt Enable bit BMPR14<5>.
4	RMT PORT	WR0/1	**REMOTE PORT:** When set to 1, indicates that remote port is compatible with and is using the same kind of TP chip.
3	RXI POL REV	WR0/1	**RXI POLARITY REVERSAL:** When set to 1, indicates reversed polarity.
2	0	0	**RESERVED:** Write 0.
1	SQE	WR0	**SIGNAL QUALITY ERROR:** When set to 1, indicates detection of SQE. Can generate interrupts if enabled by Interrupt Enable bit BMPR14<1>.
0	0	0	**RESERVED:** Write 0.

Table 31 describes Transceiver Status register, BMPR15. Note that when RMT PORT is set to 0, RLD, DLCR15<7>, and RJAB, DLCR17<5>, are meaningless.

POWERDOWN MODE

When EtherCoupler is not in use, the powerdown feature reduces power consumption by shutting off all internal clocks. This feature is invoked by first setting DLC EN bit, DLCR6<7>, high and disabling the Receiver and Transmitter, and then by setting PWRDN bit, DLCR7<5>, low. The powerdown mode terminates by setting the PWRDN bit high (writing a one to DLCR7<5>) or by implementing a hardware reset.

BUFFER CONTROLLER



1. Length (L) = 8, 16, 32, or 64 kilobytes.
2. Transmit Size (T) = 2 (one bank), 4 (two banks), 8 (two banks), or 16 (two banks) kilobytes.
3. Receive packets are aligned on eight-byte boundary.
4. Each received packet is preceded by a four-byte packet header as follows:

Byte 0	Packet Status
Byte 1	Not Used
Byte 2	Packet Size LSBs
Byte 3	Packet Size MSBs

Figure 9. Buffer Memory Organization

As shown in Figure 9, EtherCoupler uses dedicated buffer memory to store data packets to be transmitted to and received from the network. By direct connection to the EtherCoupler controller rather than a separate, local microprocessor bus, buffer memory eliminates the need for a local microprocessor. The Buffer Controller keeps track of buffer memory partitioning, as well as automatically allocating and updating receive and transmit pointers, eliminating these tasks from software overhead. Benchmark performance tests typically can surpass those of competing controllers because EtherCoupler provides a high level of automation and high-performance packet-buffering.

EtherCoupler on-chip Buffer Controller manages access to buffer memory by updating internal address pointers, which handle transmit, retransmit, receive, rejection of packets with errors, and data transfers to and from the host. The easy-to-operate EtherCoupler access-management feature relieves the host of buffer-management functions and substantially reduces software requirements. EtherCoupler automatically rejects packets with alignment, CRC or short-length errors. Packet rejection occurs unless the host sets the Acpt Bad Pkts bit, which passes packets received with errors to the host processor and sets appropriate error status bits to inform the host of the error. EtherCoupler allows reception of packets as small as six bytes by setting the Acpt short Pkts bit. Normal operation requires IEEE minimum packet length, excluding Preamble and CRC, of 60 bytes.

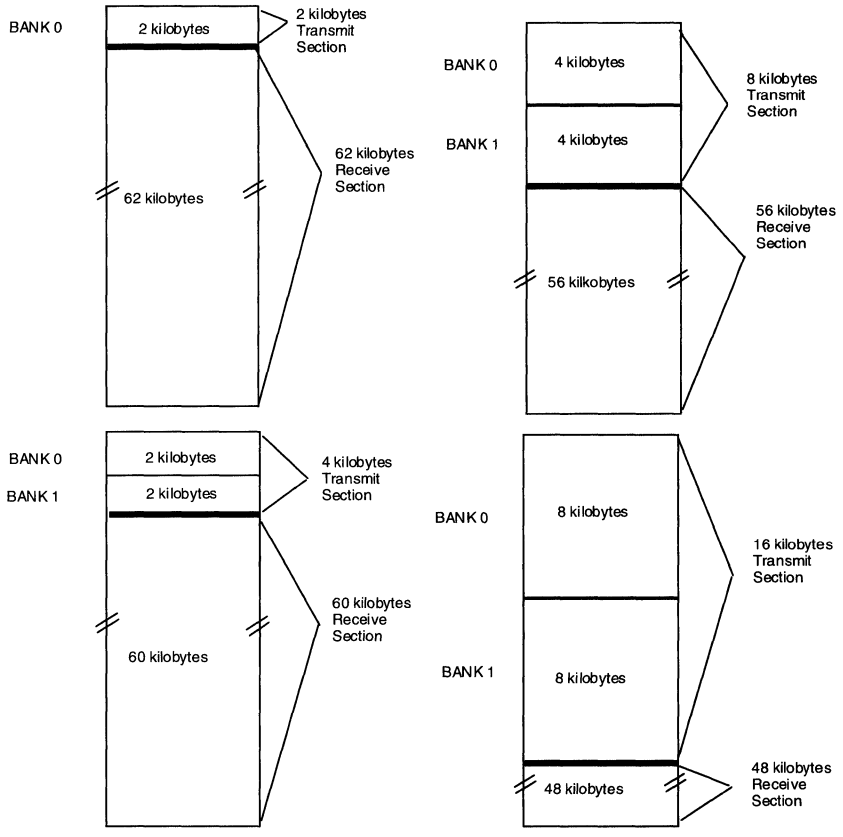


Figure 10. Transmit Buffer

As shown in Figure 10, system software can be used to program and partition buffer memory into transmit and receive buffer areas for optimum operation and for system configurations that accommodate a wide range of application demands. The transmit and receive buffer areas can allocate varying proportions of space to the transmit and receive functions.

Total EtherCoupler buffer memory size is configurable as 8, 16, 32 or 64 kbytes, including transmit and receive spaces. The buffer memory Transmitter section is configurable as a single, 2-kilobyte buffer or as a pair of 2, 4, or 8-kilobyte banks. Therefore, total size of the Transmit buffer space can be either 2, 4, 8 or 16 kbytes. Within each buffer or bank, the system writes one or more packets until available space is too small for another packet. Once begun, the Transmitter automatically transmits buffer packets, then finishes with a status update and interrupt. One bank of a two-bank configuration transmits while the other loads. The use of dual buffers, multiple-packet loading, and chaining produces the highest transmission rate, which boosts performance to accommodate systems that need high-throughput transmission.

EtherCoupler automatically configures memory as a ring buffer and allocates unused Transmitter memory to the Receiver. Like the Transmit buffer, the Receive buffer stores packets head-to-toe, but does so until reaching the end of the linear addressing space, where the EtherCoupler Receive-Write pointer then returns to the top of the receive addressing range, forming an apparently seamless ring with packets aligned on an 8-byte boundary. As packets read out to the system, the

Receive-Read pointer also forms a seamless ring. EtherCoupler automatically provides all necessary buffer-pointer management functions, to relieve host system drivers of this time-consuming task. Accomplished faster in hardware than software, this not only off-loads the host system but also speeds the communication process and increases throughput.

The Buffer Controller automatically prioritizes and services requests for access to memory from Transmitter, Receiver and host system. The Buffer Controller provides complete packet-management functions by updating buffer-memory pointers, allocating memory space for incoming data packets, and controlling pertinent bits within status registers.

The EtherCoupler arbitration mechanism provides packet management, by interleaving packet-data accesses to the buffer memory, so that operation appears to be simultaneous. The host writes data to or reads data from buffer memory via Buffer Memory Port register BMPR8 while the Receiver reads out data packets for transmission or writes in data packets for storage. EtherCoupler appears to independently serve the host system and network access interfaces, whose associated first-in, first-out (FIFO) circuits provide time for buffer interleaving.

As shown in Figure 11, packet data pipelines through the system to increase performance and throughput, with the Buffer Controller supporting all cases of simultaneous access to buffer memory, such as: (1) network data storage in the Receive buffer; (2) host retrieval of packets from the Receive buffer; (3) host loading of packet data into the Transmit buffer; (4) transmitter data acquisition for transmission from the Transmit buffer; and (5) any combination, including all of these, simultaneously.

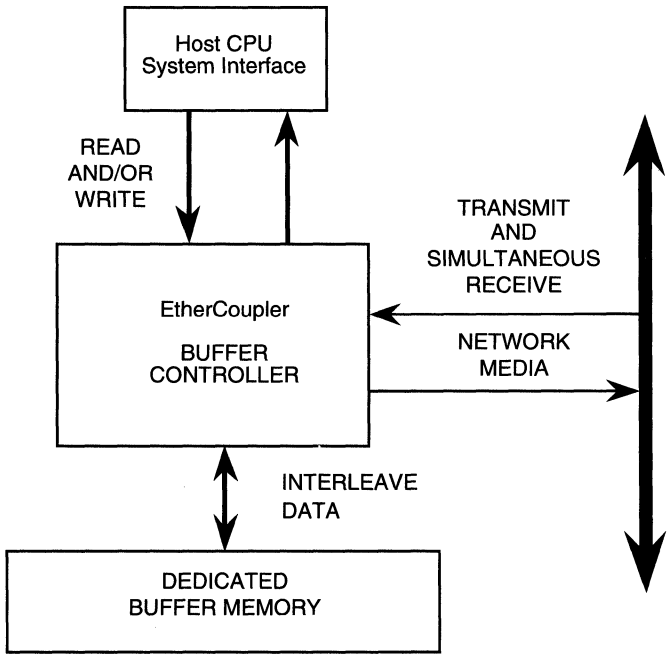


Figure 11. Simultaneous Access to Buffer Memory

System Access To Buffer

EtherCoupler supports programmed-I/O, Single-cycle and Burst mode DMA transfers between buffer memory and host system. The host accesses buffer memory by reading from or writing to EtherCoupler Buffer Memory Port register BMPR8. Data read or written by the system passes through on-chip FIFOs to eliminate effects of real-time interaction among the system, Transmitter and Receiver, as each accesses buffer memory. EtherCoupler also automatically controls read and write operations to external static random-access memory (SRAM).

Transmitter Access To Buffer

Programming Buffer Size bits BS1 and BS0, DLCR6<1:0>, changes the size of each transmit bank. Software allocates transmit buffer size as a single 2-kilobyte Transmit buffer, or as pairs of 2, 4 or 8-kilobyte Transmit buffers. A single packet or multiple packets simultaneously load into the buffer for transmission. The system and Transmitter time-share the buffer with a single Transmit buffer. The system utilizes two Transmit buffer sections to load packets into one of the buffers, while contents of the other buffer section are transmitted.

At reset, pointers initialize to set a beginning for one of the Transmit buffers. Each time the host writes data to the buffer via the Buffer Memory Port register, an internal pointer advances to the next memory location within the Transmit buffer. Once a data byte/word is written, it cannot be read and the internal pointer cannot be reversed.

EtherCoupler manages internal pointers that control access by the host to the two banks and selection of specific bank bytes and words. EtherCoupler switches banks as soon as TX START bit, BMPR10<7>, is set high by the host system, after which EtherCoupler begins transmitting at the earliest opportunity. The Transmit-Read pointer, which is also automatically managed, sequences through the transmitted bank to read packet data into the Transmitter through its FIFO. If a collision occurs, the packet automatically retransmit after a pseudo-random (backoff interval) waiting period. EtherCoupler continues down the list, automatically transmitting all multiple packets in the bank. EtherCoupler can transmit multiple, back-to-back packets of legal Ethernet sizes to the LAN network. Excluding preamble and CRC fields, these packets can be between 60 and 1514 bytes.

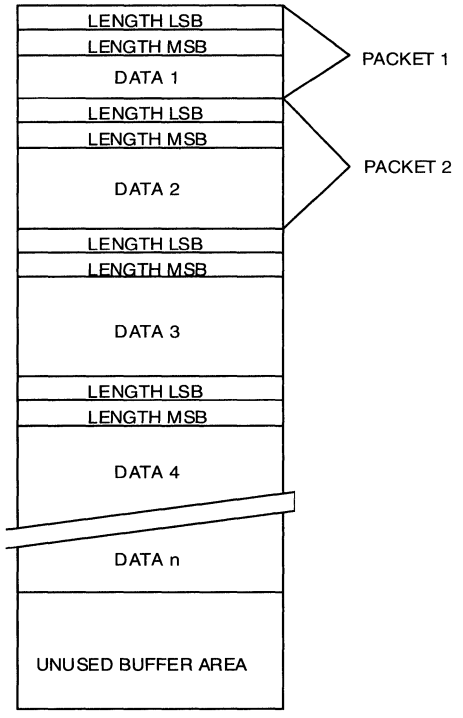


Figure 12. Transmit Buffer Detail

As shown in Figure 12, multiple packets can reside within one transmit bank, separated by a nontransmitted, two-byte header that provides packet byte-length information. At the end of a packet list or chain, the Transmitter stops, updates its status bits and, if enabled, generates an interrupt.

Transmit Packet Data Formats

Packets to be transmitted (minus preamble and CRC fields) first load into the Transmit buffer with a two-byte header indicating packet byte-length. If buffer space permits, multiple packets load simultaneously. After packet-loading, the host initiates transmission by writing the number of packets just loaded into TX PKT CNT bits, BMPR10<6:0>. If the two-bank buffer configuration is selected, the second bank now loads additional packets.

Receiver Access To Buffer

Once initialized and enabled, the Receiver automatically loads the Receive buffer (via address filter and EtherCoupler FIFO) with incoming, error-free packets, while inserting a four-byte packet-status and packet-length header. An interrupt alerts the host processor to the availability of packets in the buffer. As they become available, the host processor reads out receive packets. If an interrupt occurs to indicate when overflow occurs, buffer data writes to free space to resume reception. As soon as space is available in the Receive buffer, the Receiver automatically continues reception.

Receive buffer size varies between 62 kilobyte (with 2 kilobytes allocated for the transmit section with maximum memory size of 64 kilobyte) and 4 kbytes, if 4 kbytes are allocated for the Transmit section with minimum memory size of 8 kbytes. The Receive section dynamically allocates space along an eight-byte page boundary for each individual incoming data packet. A four-byte header that shows data packet status and length precedes each received packet. Internal pointers sense data packet length from the header and set a starting address for the next packet to link or chain with the previous packet. Figure 13 shows details of the Receive buffer. In this architecture, EtherCoupler controls a dedicated buffer memory, and FIFO size and depth are not relevant to system timing.

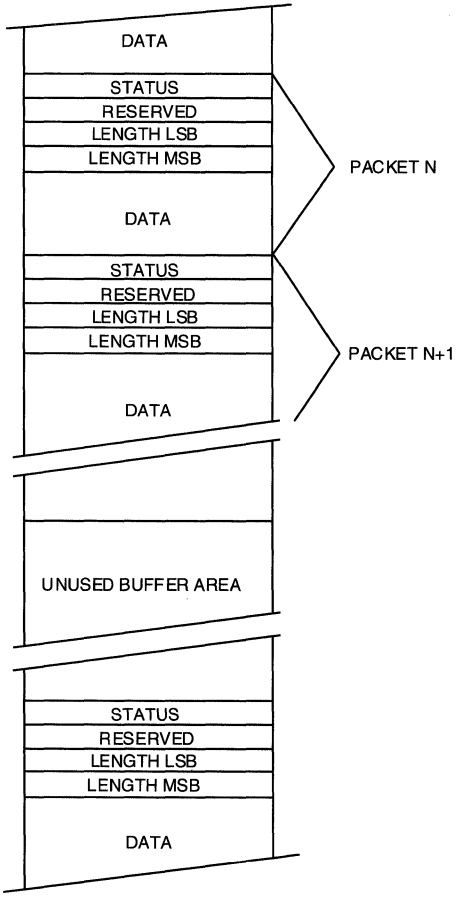


Figure 13. Receiver Buffer Detail

The RX BUF Empty status bit, DLCR5<6>, alerts the host that the Receive buffer holds one or more packets to be read. The host retrieves these packets from buffer memory by successively reading Buffer Memory Port register BMPR8. After a data byte/word is read from buffer memory, internal pointers advance to the next byte/word. As the system sequentially reads data, memory becomes available to receive new packets. EtherCoupler automatically rejects incoming packets if there is insufficient buffer space to fully receive that packet. Therefore, already received packets cannot be overrun by incoming packets.

When Acpt Bad Pkts bit, DLCR5<5>, is disabled (set to 0), a bad incoming packet causes EtherCoupler to release the buffer space containing that packet, and to reset internal pointers so the next incoming packet can use that space. When DLCR5<5> is set to a 1, the packet with a short-length, alignment or CRC error is accepted and appropriate error bits in the header status field are set. Similarly, when Acpt Short Pkts bit, DLCR5<3>, is set to a 1, packets shorter than IEEE 802.3 minimum size (less than 60 bytes excluding preamble and CRC) are accepted.

Receive Packet Data Formats

The buffer stores receive packets, less preamble and CRC fields, with a four-byte header. The initial header byte gives status information, such as errors that occurred during packet reception. Normally EtherCoupler automatically eliminates from memory and discards packets with errors. However, EtherCoupler offers mode selection to permit bad-packet reception, and indicates errors in the header status byte. While the second header byte is unused at this time, the last two header bytes provide packet byte count (less preamble and CRC).

TRANSMITTER CIRCUITS

Circuits within the Transmitter include a transmitter state machine, a small FIFO for pipe-lining the packet data, preamble generator, CRC generator, end-of-packet symbol generator, parallel-to-serial converter, Manchester encoder, waveform generator, transmit filter, twisted-pair line driver, backoff generator, inter-packet gap-timer, and time domain reflectometer (TDR) counter.

The transmitter state machine, which sequences Transmitter events (idle, preamble, data, CRC, inter-packet gap, jam and backoff), detects various transmit error conditions and sets appropriate bits within the DLCR registers.

The pipe-line FIFO provides elastic buffering that the Buffer Controller loads with data to be transmitted. The EtherCoupler CRC generator calculates the Ethernet 32-bit CRC on the destination and source address, the length field, and the (ISO/ANSI/IEEE 8802-3 Ethernet specification) data field that appends to the packet.

TRANSMIT ERROR PROCESSING

Transmit error status bits in Transmit Status register DLCR0 report possible transmit errors, the last two of which can be enabled separately to generate interrupts: 1) CR Lost, DLCR0<4>, loss of carrier during transmission, usually a medium fault or collision; 2) Col, DLCR0<2>, collision; and 3) 16 Col, DLCR0<1>, 16 consecutive collisions.

If it detects a collision during transmission, EtherCoupler automatically tries to retransmit the packet until sixteen attempts have been made. collision counter DLCR4<7:4> automatically increments after each Collision up to the sixteenth, at which time it rolls over to zero. (Bit 7 is the most-significant of the four bits.) Appropriate status bits in the Transmit Status register are set when a collision terminates transmission. The occurrence of 16 collisions may indicate a network problem, such as a disconnected cable or terminator, that produces false collisions. While rare, 16 collisions may normally occur.

A pseudo-random number generator, which provides collision backoff clocked at the 10-megahertz bit rate so that distances between stations become part of the randomizing function, is sampled at the time of collision, so as to mask all but the appropriate number of bits specified by the 8802-3 backoff algorithm. This value is then counted down at the slot-time rate (512 bits per second) to generate the backoff interval. Only one bit is used for a first collision, giving a backoff of either 0 or 51.2 microseconds. A second consecutive collision uses two bits, and so forth, up to ten bits. The tenth through 16th collisions use 10 bits to provide a pseudo-random backoff interval from 0 to 52.38 milliseconds that, per 8802-3, is the so-called binary exponential backoff for collisions.

TIME DOMAIN REFLECTOMETRY

The TDR function counts the actual number of bits transmitted for each packet before a collision indication, carrier loss indication or completion of transmission. A complete transmission with no error indications clears the TDR counter. [Refer to register descriptions for Time Domain Reflectometry registers, DLCR14 and DLCR15.]

MEDIA ACCESS CONTROL

The EtherCoupler transmitter state machine implements the 8802-3 networks media-access protocol, CSMA/CD (Carrier Sense, Multiple Access with Collision Detection). carrier sense means that EtherCoupler monitors the network for any other node carrier, and defers transmission (collision avoidance) while other nodes are transmitting. collision detection handles collisions that may still occur when two nodes separated on the network by several microseconds begin transmitting at nearly the same time. All nodes monitor the network for collisions and, when involved in one, transmit a 32-bit Jam to reinforce the collision and then terminate transmission. After waiting a pseudo-random backoff interval, the node automatically retries transmission of the packet.

Packets must be separated by at least 9.6 microseconds, a timing gap during which trunk cabling is idle. The EtherCoupler Transmitter state machine that measures this interval, starting from the end of a packet on the network, does not transmit until the end of this interval. If carrier reappears on the network during the first two-thirds of the interval, EtherCoupler resets the interval timer to re-time the interval from the end of the new transmission.

Superimposition of two packets corrupts data and carrier indications, such as during a collision. During the last one-third of the interval, EtherCoupler ignores the occurrence of a carrier indication, in accordance with 8802-3, and ensures fairness and equality in access to the network. If one station begins transmission slightly ahead of another, there is no advantage to the earlier start. Both nodes transmit, a collision occurs, and backoff interval differentials resolve the media-access contention.

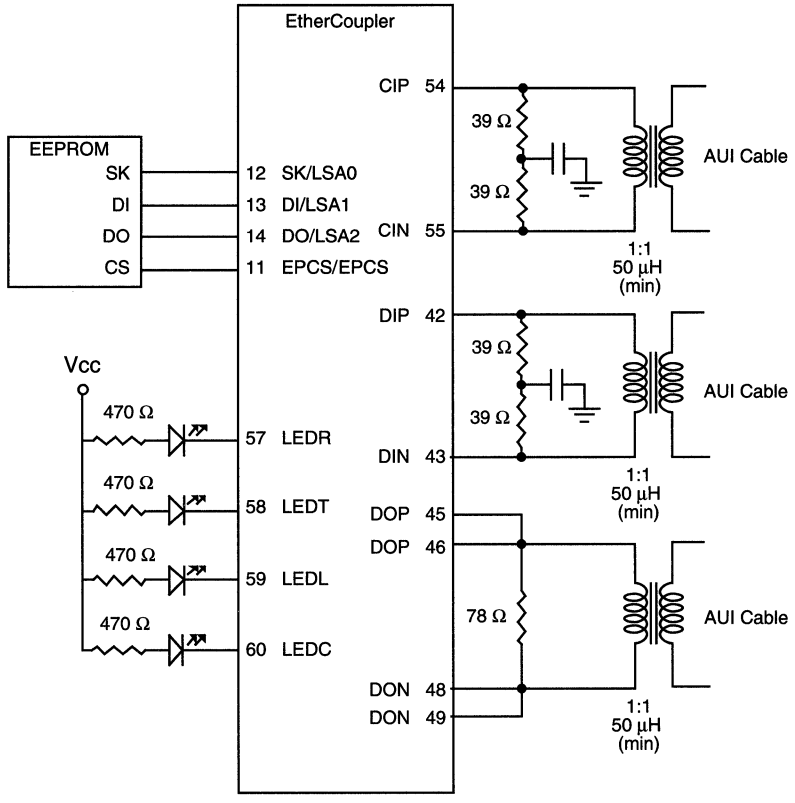


Figure 14. Typical Connections

DATA ENCODER

EtherCoupler serializes the data for transmission, and converts each bit to Manchester Code, the format used on the network media. Manchester Code for a one is a 100-nanosecond interval starting with a low, ending with a high, with a low-to-high transition at the 50-nanosecond point; Manchester Code for a zero is the inverse.

TRANSMIT PACKET PROCESSING

When transmitting one or more packets, the host system first loads the packets into a transmit buffer. The packets are preceded by a two-byte header giving their lengths, and are written to Buffer Memory Port registers BMPR8 and BMPR9. The system loads only packet destination address, source address, length field and data field; EtherCoupler generates the rest. When the packets load, the system turns on the Transmitter to initiate transmission, enabling EtherCoupler to transmit. Observing the media access protocol, EtherCoupler delays transmitting until the absence of carrier from other nodes or intervals for minimum interpacket gap and backoff, and then begins to transmit. EtherCoupler, which serializes and encodes data as Manchester code, generates the Preamble field at the beginning and calculates and appends the CRC field at the end, followed by the non-Manchester End-Of-Packet delimiter.

Figure 14, which shows typical connections to an EEPROM and the LEDs, also indicates typical interfacing to the AUI cable. The Manchester-encoded signals are output to transmitter data pins DOP and DON through a differential driver, which can drive a 50-meter segment of 78Ω transceiver cable as specified in the 8802-3 standard.

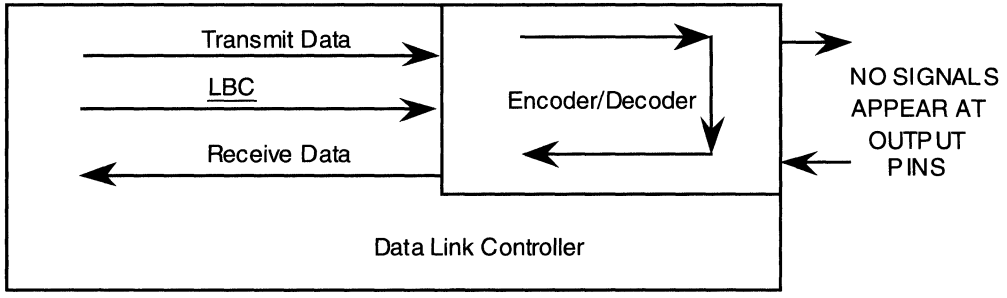


Figure 15. Loopback Operation

The host system activates the Transmitter by writing the packet count to TX PKT CNT register, BMPR10<6:0> and by writing one to the TX START bit, after which the Transmitter transmits each packet in the buffer in the order in which they were loaded. If a collision occurs, the Transmitter automatically retransmits the packet until successful or until 16 consecutive attempts have ended in collision. In the latter case, depending on the mode selection made at initialization time, the Transmitter continues to try to transmit the same packet starting again with a collision count of zero, or skips the current packet and tries to transmit the next packet starting with a collision count of zero, or halts and waits for instruction from the host. In the last case, the host terminates by setting DLC EN, DLCR6<7> to one, or continues to attempt to transmit the same packet (collision counter reset), or skips the current packet and tries to transmit the next packet (collision count is zero).

COLLISION SIGNAL PROCESSING

As collisions are detected on the network media, a 10-megahertz signal is generated on collision differential inputs, CIP and CIN. When EtherCoupler detects this signal, it asserts the internal collision line. The CIP and CIN differential driver inputs require termination similar to that for the DIP and DIN inputs, i.e., 39Ω resistors tied to ground through 0.1-microfarad capacitors.

LOOPBACK

As shown in Figure 15, loopback allows EtherCoupler testing without sending signals onto the LAN media. The loopback function is invoked by clearing LBC bit DLCR4<1>. Data is routed from the Transmit Buffer through a FIFO to the Transmit section of the data link controller, through the internal Manchester encoder, back through the Manchester decoder, through the Receiver section of the data link controller, and is then stored in a Receive Buffer. Software can then read and check the received packet that has traveled through the EtherCoupler Transmit and Receive sections. The Manchester encoder/decoder responds to assertion of the LBC input by internally looping the transmitter output to the receiver input, and blocks the transmit data from appearing at the network output pin.

RECEIVER CIRCUITS

The Receiver includes twisted-pair line receiver, receive squelch, receive filtering, a phase-locked loop (PLL) for clock and data separation (Manchester decoding), a receive state machine, serial-to-parallel conversion, pipe-line FIFO, preamble recognition, bit and byte-framing, address filtering, CRC and other error checking and end-of-packet symbol recognition.

The receiver state machine, which provides sequencing of events for the receiver, including idle, busy, address filtering, and data storage, detects receive error conditions and sets appropriate bits within the data link control registers. A small data FIFO provides elastic buffering for synchronization with Buffer Controller timing, and buffering data while the Buffer Controller is servicing other buffer memory access requests.

All received bytes are delayed by four bytes before storing in the Receive Buffer, so the last four bytes of the packet can be stripped and checked for correct CRC. (The CRC bytes are not transferred to the Receive Buffer.)

During reception, the controller automatically reject packets if Receive Buffer space is insufficient to hold the entire received packet. Status bits in the receive status register are set to indicate this and other errors. Receive errors are: 1) bus read error, which occurs if the host system attempts to read from an empty receive buffer (this need never occur if the RX BUF EMPTY bit is checked), 2) short packet error, 3) alignment error (incomplete byte fragment at end of packet), 4) CRC error and 5) Buffer Overflow. The software checks Length error, an additional possible receive error. When the length of the packet does not match the value in the Length Field of an 8802-3 packet, a length error occurs. Some protocols use the length field for other purposes, for example, the DIX protocol that uses it for a packet type code. In this case, allowed type codes do not overlap allowed packet length values, providing a means to distinguish which protocol is being used (if length value >1500, it is DIX type code). Length check can be made conditional on protocol type, if necessary to support other protocols such as DIX.

DECODER FUNCTIONS

The data decoder section performs three functions on the data received at the differential receive inputs from the transceiver: clock recovery, carrier detection, and Manchester data decoding. Clock recovery and data separation are accomplished by a phase-locked loop. Use of proprietary techniques in the PLL allows lock-on within 6 - 7 bit times of the beginning of the Preamble, and permits stable operation with input signal jitter of up to ±18 ns. Carrier detection is indicated to the controller by assertion of the internal CRS signal, which occurs shortly after the received data signals appear.

The recovered clock is supplied to the controller, and is also used to convert Manchester-encoded data to NRZ format. Transitions in the state of the NRZ data are synchronous with the falling edge of the receiver clock pulse. During idle periods, the receiver clock pulse is disabled. The DIP and DIN differential inputs are usually terminated with two 39Ω resistors in series and a 0.1-microfarad bypass capacitor to ground at their junction.

MONITORING THE NETWORK

Whenever the data link section is enabled (DLC EN bit, DLCR6<7>, is set to zero), the Receiver constantly monitors the network for carrier. Signals that exceed the AC and DC squelch thresholds of the received data input section cause the internal carrier sense line to assert, which in turn causes the Receiver to attempt to receive a packet. The Transmitter also uses the carrier sense function to defer to transmissions from other nodes, except when EN TX DEFER bit, DLCR4<0>, is high.

After the PLL decoder acquires bit-synchronization with the incoming signal, the Receiver monitors the data stream for the end-of-preamble bit pattern, a four-bit pattern of 1011 ending the Preamble's pattern of alternating ones and zeros. This pattern gives the Receiver byte and field synchronization, because the bit immediately following the four-bit pattern of 1011 ending the Preamble is the first bit of the first byte of the packet's destination address field.

When packet transmission is unflawed, carrier sense remains asserted for the duration of the packet, negating just after the last bit is received. As a packet comes in, the decoder carrier sense function monitors the data stream for the end-of-packet symbol, a special non-Manchester code element at the end of the packet. When detecting this symbol, the carrier sense line is negated. Loss of carrier may also result from negation of the carrier sense line during a collision.

RECEIVE PACKET PROCESSING

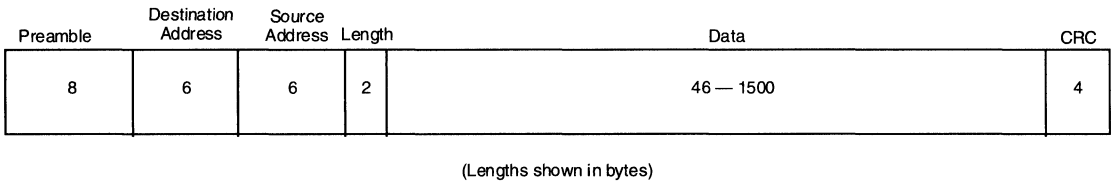


Figure 16. 8802-3 Packet Format

Figure 16 illustrates the 8802-3 packet format. When a received packet enters from the network, its destination address field is tested for address filter criteria selected by the Hash Table and Address Filter Mode bits AF1 and AF0, DLCR5<1:0>. If the address meets filter criteria, the Receive Buffer accepts the packet for storage. The packet must also be error-free unless the reception of flawed packets is allowed, e.g., for diagnostic purposes. If conditions are met, packet reception results in the Buffer storing the packet, updating the four-byte header at the end of reception, clearing the RX BUF EMPTY bit, setting the RX PKT bit high, and (if enabled) generating an interrupt. Otherwise the packet is discarded, and pointers reset to reuse the same portion of memory for the next arriving packet. A flawed packet accepted for storage for diagnostic purposes is reported as an error in the PKT STATUS byte of its header. The Receive Packet Header bit positions for PKT STATUS are shown in Table 24, Receive Packet Header Conditions.

NETWORK MANAGEMENT

Error, traffic and performance statistics may be collected continuously or on a sampled basis. The Receive Status register and Transmit Status register indicate detected errors. Such data can be collected in two ways: interrupts can be used after each packet, and the interrupt service routine reads the status from the status register; or packets are accepted for storage in the Receive Buffer in Accept Bad Packets mode, and content and error status stored in the header are later read in batch mode. Frequent selection of the Accept all packets mode to get maximum statistics for the network and to count all packets including their length, because it maximizes host overhead with user terminal equipment, is discouraged.

Sampling of carrier detection estimates network bandwidth utilization, via Transmit Status register NET BSY bit, DLCR0<6>. Average media-access waiting time is estimated by calculating the elapsed time between starting the Transmitter and TX DONE bit, DLCR0<7>, going high, and subtracting calculated transmit time. Collision counter bits COL CTR3 through COL CTR0, DLCR4<7:4>, determine the number of collisions encountered by the last outgoing packet. The counter resets at the start of transmission of each packet.

RECEIVE ERROR PROCESSING

Interrupts may optionally be generated by these receive error conditions: buffer overflow, CRC error, alignment error, and short packet. None of these errors requires special host processing or intervention, other than optional tallying of the error for network management purposes. EtherCoupler automa-tically discards any packet with errors. If a buffer overflow occurs, EtherCoupler automatically handles that as well. Packets already stored in the buffer are not lost. The host simply reads out some of the packet data, freeing space in the buffer for more packets. EtherCoupler then automatically resumes reception of packets, as long as there is buffer space. To prevent packet loss although EtherCoupler automatically recovers, avoid overflow by rapidly processing incoming packets.

TRANSCEIVER

The EtherCoupler Transceiver, which is fully compliant with IEEE 802.3 specifications for AUI (Attachment Unit Interface) and 10BASE-T (twisted-pair) interfaces, provides electrical interface to DB15 (AUI) and RJ45 (10BASE-T) connections to an Ethernet local area network. Its functions include Manchester encoding and decoding of serial data streams, level conversion, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted-pair input. Pulse-shaping and filtering functions eliminate the need for external filtering components and thus reduce overall system cost. Also provided are outputs for receive, transmit, collision and link test LEDs, and compatibility with shielded and unshielded twisted-pair cables. Receive threshold can be reduced to allow an extended range between nodes in low-noise environments.

TRANSMIT FUNCTION

The Transceiver Transmitter section receives from the controller section non-return zero (NRZ) data that passes through a Manchester encoder. Encoded data then transfers to either the AUI cable via the DO circuit or the twisted-pair network via the TPO circuit. Advanced integrated pulse-shaping and filtering produces on the TPON and TPOP pins an output signal that is predistorted and prefiltered to meet the 10BASE-T jitter template, which requires no external filters.

During idle periods, EtherCoupler transmits link integrity test pulses on the TPO circuit if Link Test Enable bit, LINK TEST EN, BMPR13<5>, is enabled and the AUI/TP port-select bit, BMPR13<4> is set low for twisted-pair (TP) mode. EtherCoupler is programmed for either shielded (150 Ω) or unshielded (100 Ω) twisted-pair through STP/UTP bit BMBR13<2>.

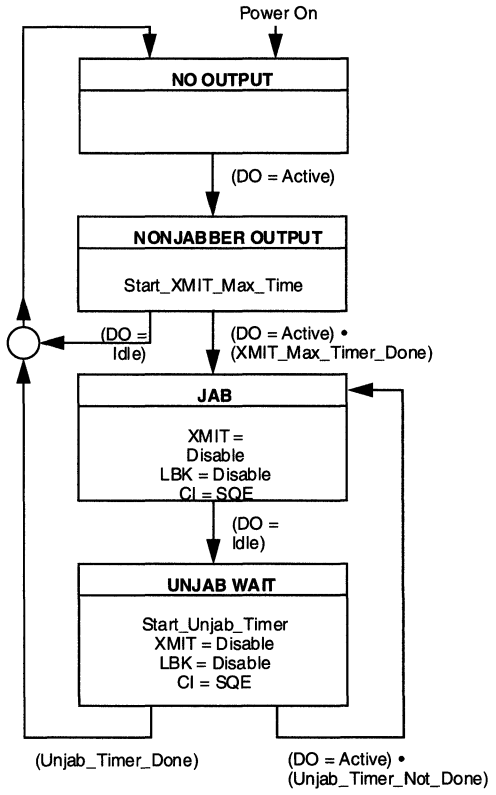


Figure 17. Jabber Control Function

Jabber Control Function

Figure 17 is a state diagram of the jabber control function. An on-chip watchdog timer prevents the data terminal equipment (DTE) from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JABBER signal. Before EtherCoupler can exit the jabber state, the transmit data circuit must remain idle for between 0.25 and 0.75 seconds.

SQE TEST FUNCTION

The Transceiver supports the signal quality error (SQE) test function as shown in Figure 18. After every successful transmission on the 10BASE-T network, EtherCoupler transmits the SQE signal to the DTE for 10±5 bit times over the internal CI circuit. Bit 1 of Transceiver Status register BMPR15 reflects the status of this SQE signal.

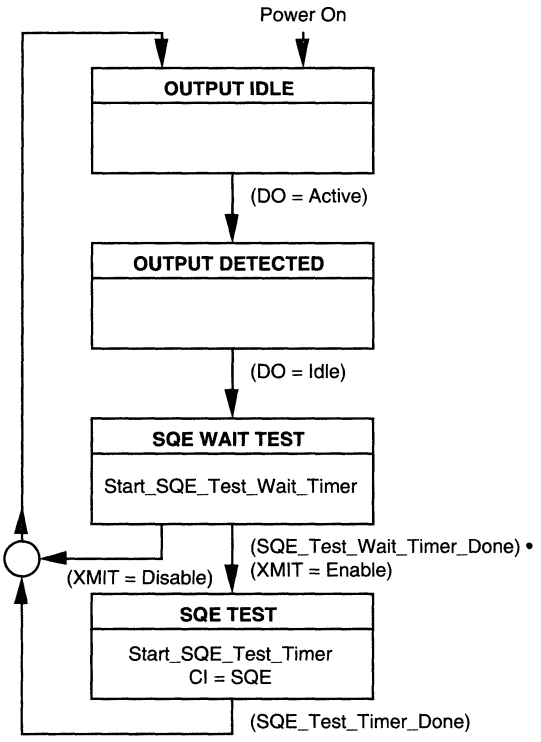


Figure 18. SQE Test Function

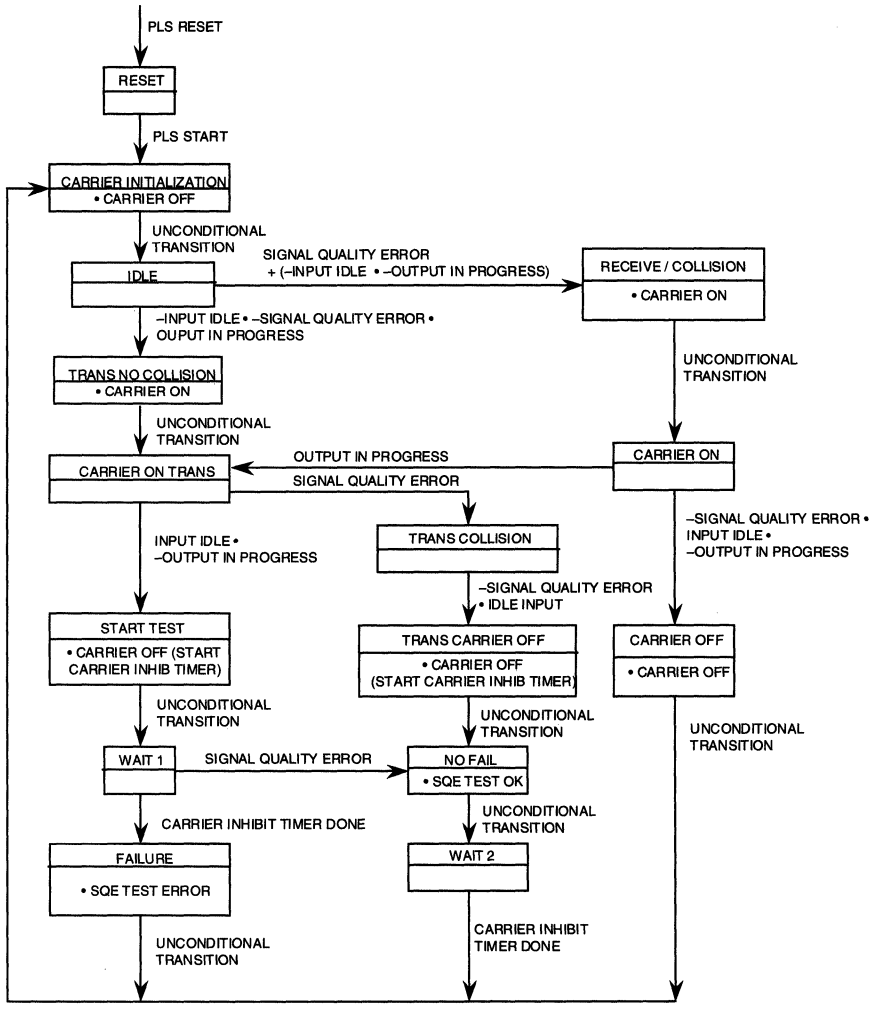


Figure 19. Carrier Sense Function

RECEIVE FUNCTION

The Transceiver receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI circuit). Valid received signals pass through the on-chip filters and Manchester decoder, and output as decoded NRZ data and receive timing on the Receiver Data and Receiver Clock to the Receiver State Machine. No external filters are required.

An internal intelligent squelch function discriminates noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the receive function enters the idle state. If polarity of the TPI circuit reverses, the Transceiver detects the polarity reversal and reports it via RXI POL REV bit, BMPR15<3>. The Transceiver automatically corrects reversed polarity. Figure 19 is a state diagram of the carrier sense function.

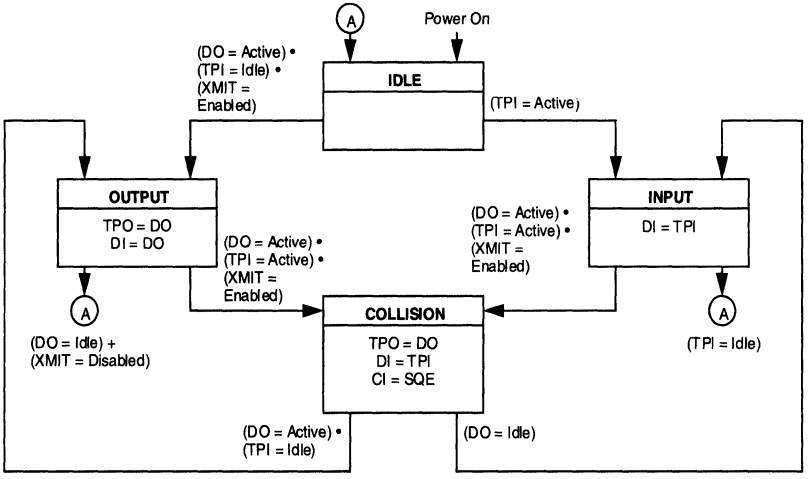


Figure 20. Collision Detection Function

POLARITY REVERSE FUNCTION

The Transceiver polarity reverse function uses link pulses and end-of-frame data to determine the polarity of received signals. A reversed polarity condition is detected when eight opposite receive link pulses are detected, without receiving of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the Transceiver enters the link fail state and no valid data or link pulses are received within 96 to 128 milliseconds, polarity resets to the default uninverted condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The Transceiver reports collisions to the back-end via the COL pin. If the TPI circuit is active while there is activity on the TPO circuit, the TPI data passes to the back-end as received data, disabling normal loopback. Figure 20 is a state diagram of the collision detection function.

TWISTED-PAIR LOOPBACK FUNCTION

EtherCoupler provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the Transmit State Machine is internally looped back within EtherCoupler before the TPO drivers to the Manchester decoder and returned to the Receive State Machine. The normal loopback function is disabled when a data collision occurs, clearing the received data circuit in the Transceiver for the twisted-pair input data. The normal loopback is also disabled during the link fail and jabber states.

EtherCoupler provides additional loopback functions controlled by LBC bit, DLCR4<1>. When the twisted-pair port is selected and LBC is set high, the twisted-pair loopback is forced to override collisions on the twisted-pair circuit. Normal loopback is in effect when LBC is set low. When the AUI port is selected and LBC is set high, data transmitted by the back-end internally loops back from the Transmit Data pin through the Manchester encoder/decoder to the Receive Data pin. When LBC is set low, no AUI loopback occurs.

AUTOMATIC PULSE-STRETCHING FUNCTION

EtherCoupler incorporates open-drain drivers to provide signals to each LED that indicates packet reception, transmission, collision, and linking. The chip provides automatic stretching of pulses to allow perception by the human eye of the presence of packets — as they are being processed for each function — despite true rates which would be too fast to visibly indicate state changes.

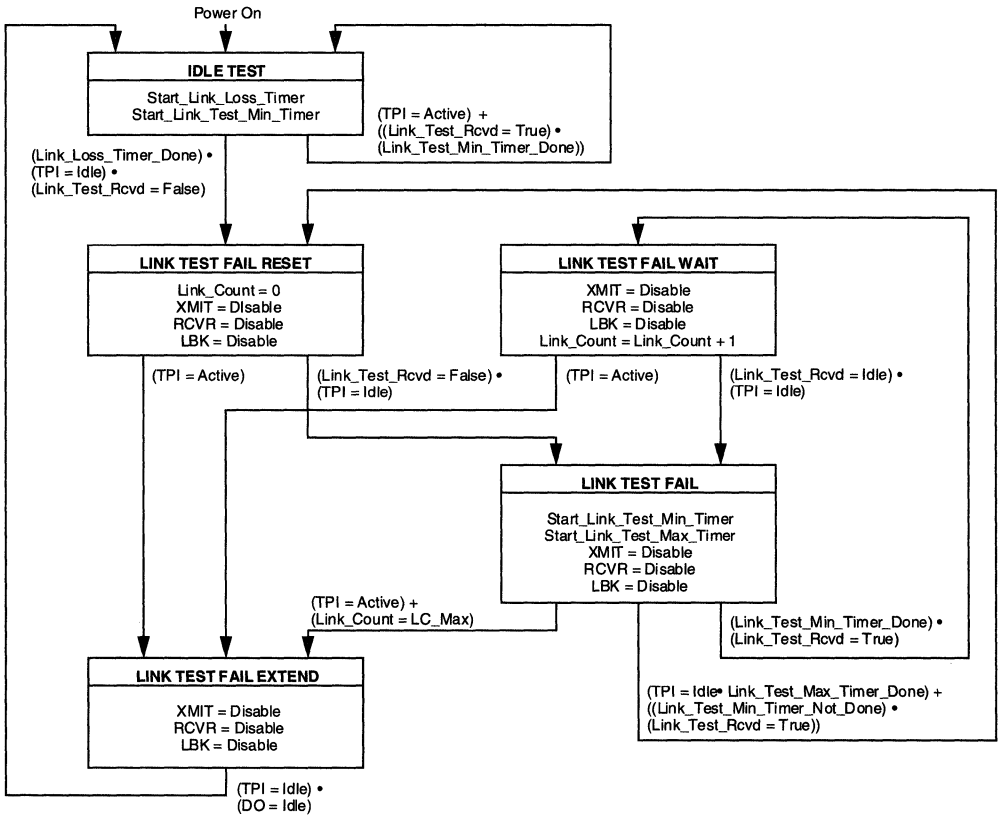


Figure 21. Link Integrity Function

LINK INTEGRITY TEST

Figure 21 is a state diagram of the link integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled when Link Test En bit BMPR13<5> is set low. When enabled, the Receiver recognizes the link integrity pulses transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 to 150 milliseconds, EtherCoupler enters a link-fail state and disables the transmit and normal loopback functions. EtherCoupler ignores any link integrity pulse with an interval less than 2 to 7 milliseconds. EtherCoupler remains in the link-fail state until it detects either a serial data packet or two or more link integrity pulses.

REMOTE SIGNALING

EtherCoupler transmits standard link pulses that meet the 10BASE-T specification. However, EtherCoupler encodes additional status information into the link pulse by varying the link-pulse timing; this is referred to as remote signaling. By using alternate pulse intervals, EtherCoupler signals three binary conditions: Remote Linkdown (RLD), Remote Jabber (RJAB), and Remote Signaling Capability (RFTN). EtherCoupler also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are sensed by the controller as RLD bit, BMPR15<7>, RJAB bit, BMPR15<5> and RFTN bit, BMPR15<4>.

SOFTWARE SUPPORT FOR POPULAR NETWORK OPERATING SYSTEMS

LAN NODE DRIVERS

The so-called driver is the hardware-dependent portion of the software complement for a network node. It's purpose is to marry a specific hardware configuration to a more-or-less generic interface provided by the networking software. Network software suppliers provide such generic interfaces for drivers to encourage universal support from a variety of hardware products. By partitioning or layering the software into a stack of components with standardized interfaces between the layers, the job of integrating various hardware and software offerings with a particular network operating system becomes easier. More drivers will become available, and everyone benefits.

As seen in Figure 22, which depicts a model of LAN node components, the driver sits between the generic network software and the hardware, and acts as a bridge between the system and the node hardware. The interface of the driver to the network software and its applications is a generic interface and virtually the same for all drivers running on a given operating system. But the driver comprehends the configuration and nuances of the hardware, and optimizes it's performance in the system. A good, well-written driver is a positive advantage to the system, allowing it to achieve its performance potential; whereas a poor driver will limit the performance and reliability of the system.

The best drivers have a certain intimacy with the hardware, which allows them to take full advantage of its features. High data throughput, data integrity, and reliable operation are the key goals for which every node-driver writer should strive. In addition, the final driver should be efficient, by requiring minimum host execution time. These are all things the end user will and should take for granted; if they are not supplied with the design, there will be no customer satisfaction.

Most network software suppliers offer technical support for third-party driver development. This often comes in the form of a developer's kit that includes a manual and software examples. Some suppliers also offer test suites and certification testing to verify the driver product, because they know that good drivers benefit both users and suppliers.

WHAT'S IN A DRIVER?

Typical node drivers manage the movement of packet data between system memory and the network, and vice versa, as well as providing diagnostic testing, error processing, and error statistics on-demand for the system.

The first thing a driver does when the system is powered up is system check-out, which may include buffer memory testing, and loopback testing of the transmit and receive circuits. If the network supports it, as does Ethernet, for example, the testing may include sending and receiving test packets on the network to verify the ability to communicate.

As shown in Figure 23, the driver provides control of the initialization, interrupt and branch control processes, supporting both the transmit and the receive functions.

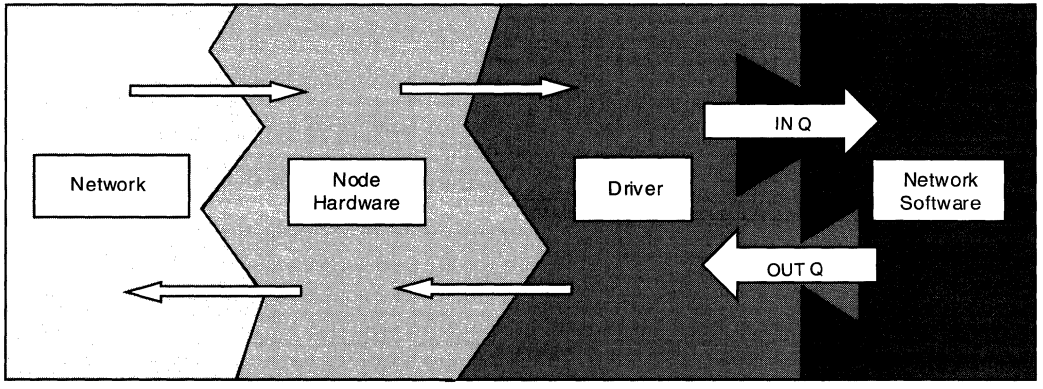


Figure 22. Model of LAN Node

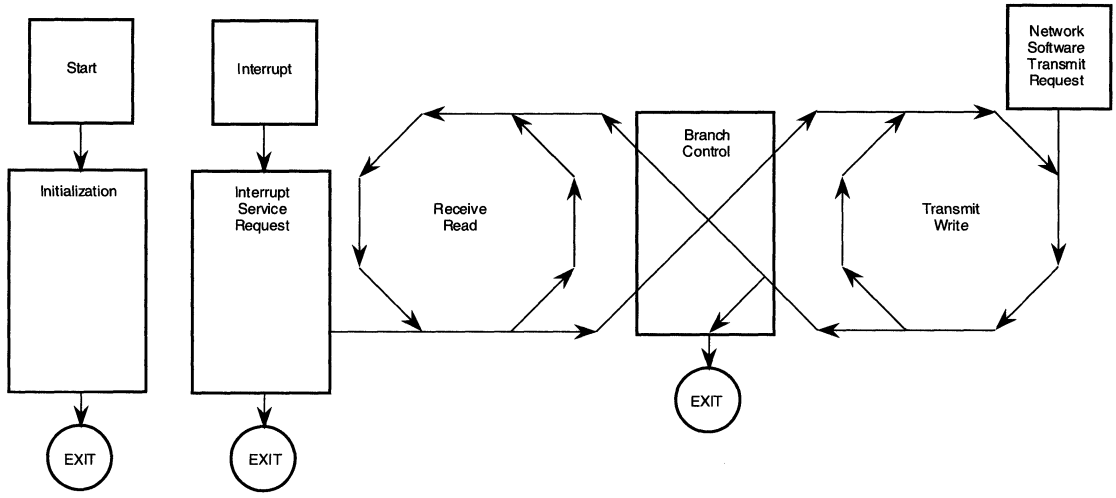


Figure 23. Software Driver Model

Figure 24 shows an example in flow chart form of a check-out routine written for the Fujitsu MB86965 Controller. The driver first initializes the control and status registers in the controller for memory and loopback testing. Loopback and memory testing are conducted simultaneously by transmitting memory test patterns from the transmit buffer area of memory to the receive buffer area using loopback. This test sequence simultaneously exercises and tests the transmitter, the receiver and the buffer memory.

The loopback/memory startup test is performed by first loading a test pattern in the form of several packets into the controller chip's transmit buffer, then transmitting the packets in loopback mode. The loopback transmission path through the chip exercises the data link controller as well as the encoder and decoder circuitry, but does not affect the network.

The EtherCoupler controller has a unique buffer memory architecture which pipelines packets through the system in both directions, optimizing data throughput. EtherCoupler's buffer controller provides all the pointer management for accessing the buffer automatically, greatly reducing the complexity of the driver and minimizing the software overhead. Receive packets with errors are automatically purged by EtherCoupler. When a collision occurs, EtherCoupler automatically re-transmits without host interaction. These features provide high data throughput while minimizing the host and memory overhead. At the successful conclusion of the tests, the driver starts up the EtherCoupler chip for regular service on the network.

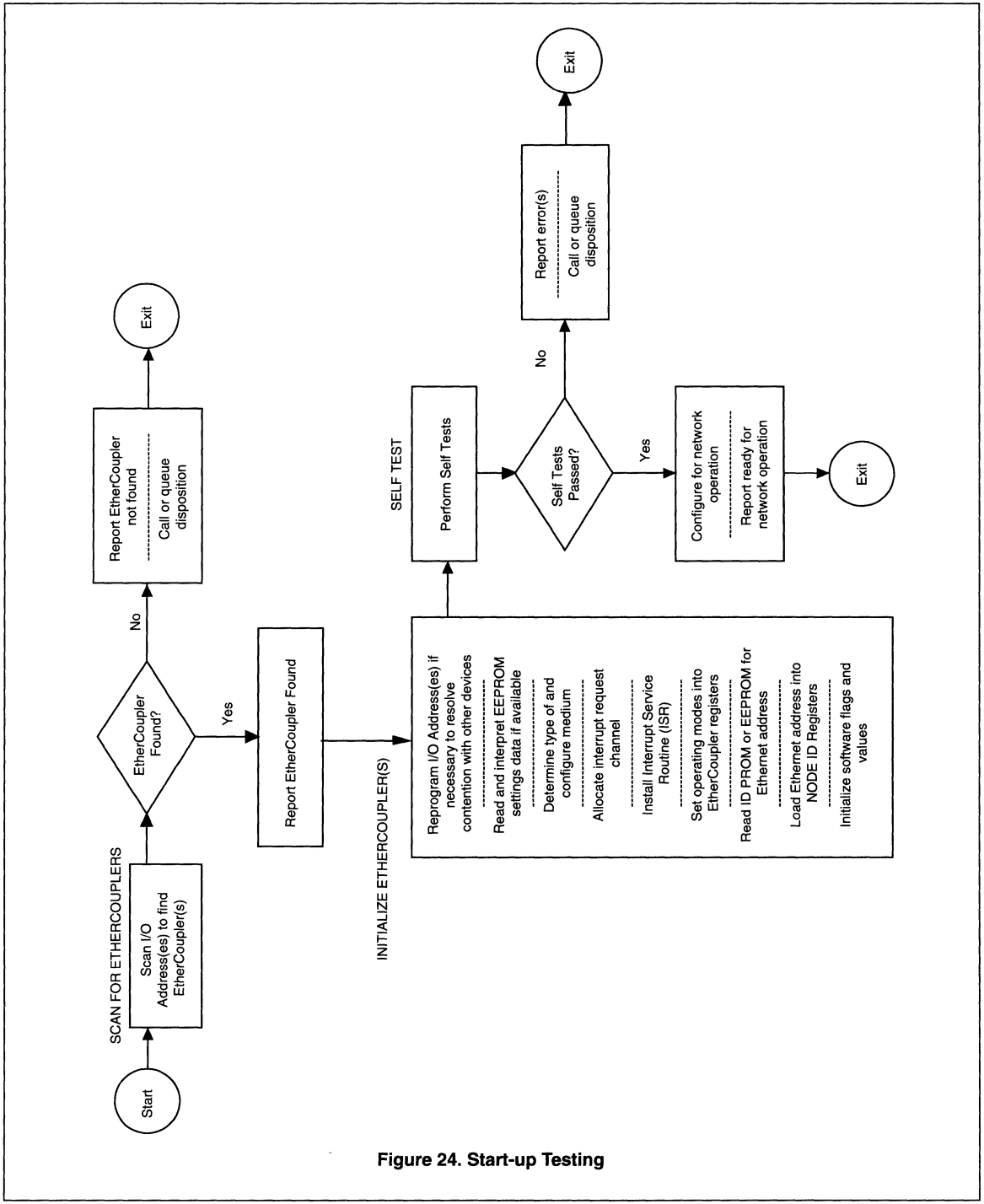


Figure 24. Start-up Testing

OPERATING ON THE NETWORK

Driver code for operating on the network might be partitioned into three main modules as shown in the example for the EtherCoupler controller in this section. The modules, shown in Figures 25, 26, and 27 are Transmit Packet Write, in which packets to be transmitted are moved from host memory to the point marked TX PKT WRITE.

Transmission takes place in two steps. First, packets to be transmitted are loaded into the transmit buffer. Secondly, when the transmitter is not busy, it will be started to transmit the stored packets. Each of these steps may have to wait for resources. The packets cannot be loaded unless there is buffer space available. EtherCoupler provides the option of a single or two independent transmit buffers. With two buffers there is usually no waiting. The transmitter cannot transmit but one buffer full of packets at a time. To manage these resources, two software flags are used, TBUF STAT and TX STAT, the status of the transmit buffer and the transmitter respectively. TBUF STAT refers to the current buffer which might be available to the driver for loading. Its status can be Busy if no buffer is available, Loading when in the process of being loaded, in Standby if ready to transmit, but not full, ready and Full or Empty. The transmitter status can be either Busy or Idle.

Packet length is checked during the loading process to assure that the ISO/ANSI/IEEE 8802-3 length requirements are met. Packets ready to be loaded can be loaded into an Empty or Standby buffer, the latter being a buffer with packets waiting for the transmitter to become idle. If a standby buffer has more room for packets, additional packets can be loaded until it is full. The Empty buffer is available for loading and has no packets. The driver takes ownership of an Empty or Standby buffer by changing its status to Loading.

After the packets are loaded, the transmit status flag is checked for an idle transmitter. If idle, it can be immediately started to transmit the contents of either a Full or Standby buffer. When the transmitter of the EtherCoupler chip is started, buffer status also changes. In single buffer mode, starting the transmitter makes the single buffer unavailable to the system. In dual buffer mode, starting the transmitter re-allocates its previously-transmitted buffer as an empty buffer, available for loading. If the transmitter is busy, the routine will suspend execution at that point pending an idle transmitter.

Two key interrupts used in this example are the receive packet interrupt (RX PKT), indicating that one or more packets has been received since the interrupt was last enabled, and the transmitter done interrupt (TX DONE), indicating that the transmitter has finished transmitting the contents of its current buffer. The interrupt service routine for network operation, illustrated in Figure 26, is short and sweet. If the receive packet interrupt has occurred, it calls or queues the routine for reading packets (RX PKT READ). Further receive interrupts are masked until the driver has emptied the receive buffer. This prevents redundant interrupts which would otherwise occur if packets come in during the read sequence. If the transmitter done interrupt has occurred, the status flags are updated, and appropriate action is taken to satisfy pending activity, if any, with the newly available buffer and/or transmitter resource.

The driver is structured to read all receive packets in the buffer whenever one or more packets arrive. A status bit in EtherCoupler (RBUF EMPTY) indicates whether the receive buffer is empty or not (indicating whole packets only). The packet read routine, shown in Figure 27, starts by masking further receive interrupts until it has emptied the buffer and suspended execution. This prevents redundant interrupts which would otherwise occur if packets come in during the read sequence. As each packet is read, it can be read in parts. If after reading the first part the packet is not of interest, the rest can be discarded without being moved to host memory using EtherCoupler's Skip Packet feature. Reading will continue until the buffer is empty, as indicated by RBUF EMPTY bit.

The Transmit Packet Write Routine, shown in Figure 25, and the Receive Packet Read Routine, shown in Figure 27, together comprise the driver core, which can be called by the network software or from the Network Interrupt Service Routine, shown in Figure 26. Once called, this core routine transfers both transmit and receive packets until there are no more to be transferred, then exits or returns. If packets are transferring, this core routine avoids locking out either the transmitter or the receiver while the other is very busy, by alternating between the two after a fixed number of packets, set by TX MAX and RX MAX. While in operation, the core routine polls key status bits. Interrupts are disabled to prevent unnecessary interrupts while the core is executing.

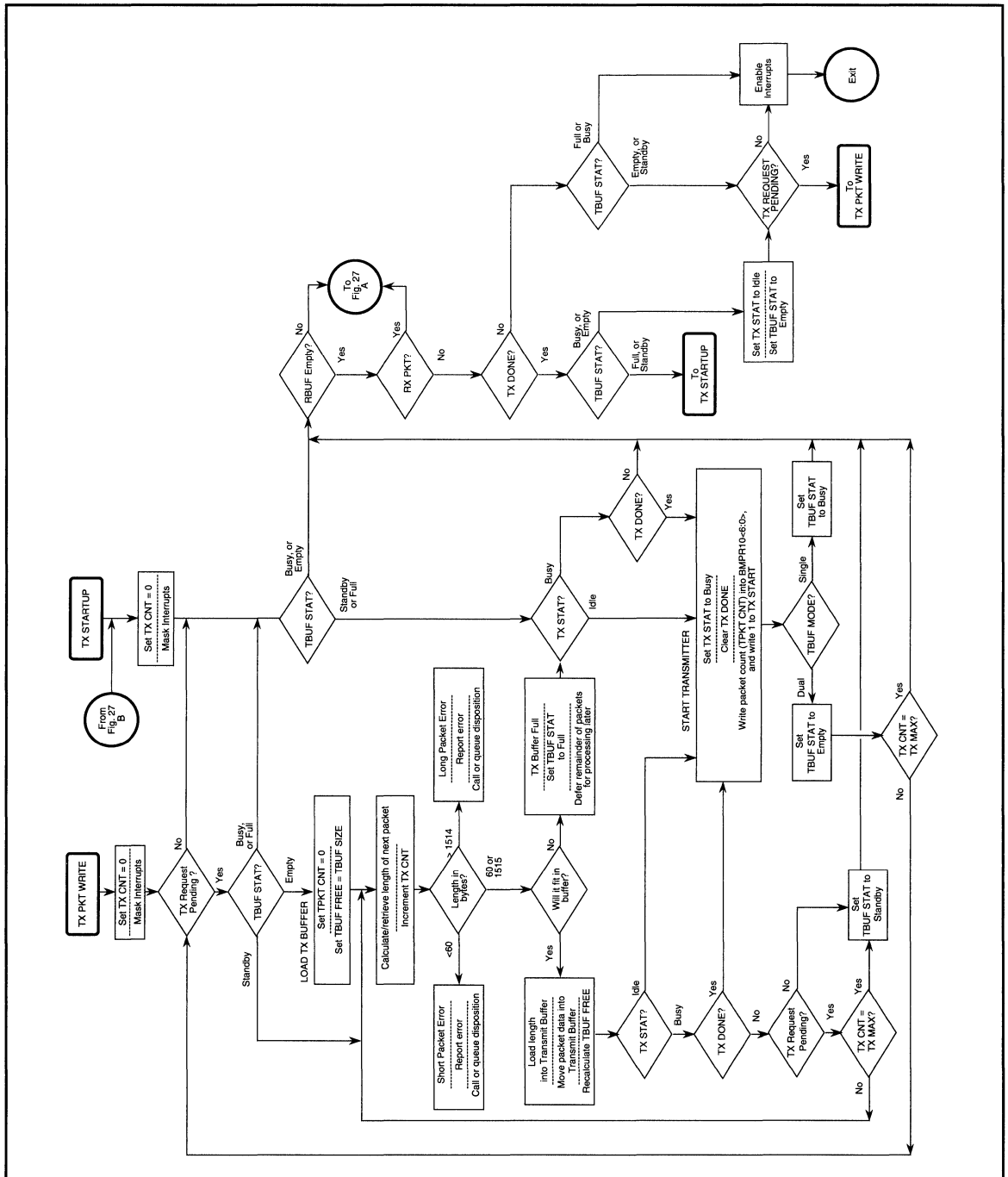


Figure 25. Transmit Packet Write Routine

A driver such as the one illustrated in this section might typically occupy 4 to 6 kilobytes on its distribution diskette. The host-resident portion, when loaded for network operation, might use typically 2 to 3 kilobytes of host memory. A set of quality software drivers bundled with the hardware is well worth providing to LAN equipment customers. By providing better performance and reliability, good drivers will enhance both customer satisfaction and sales, while reducing customer service calls.

Table 32 represents typical control and status parameters used in EtherCoupler Network Drivers.

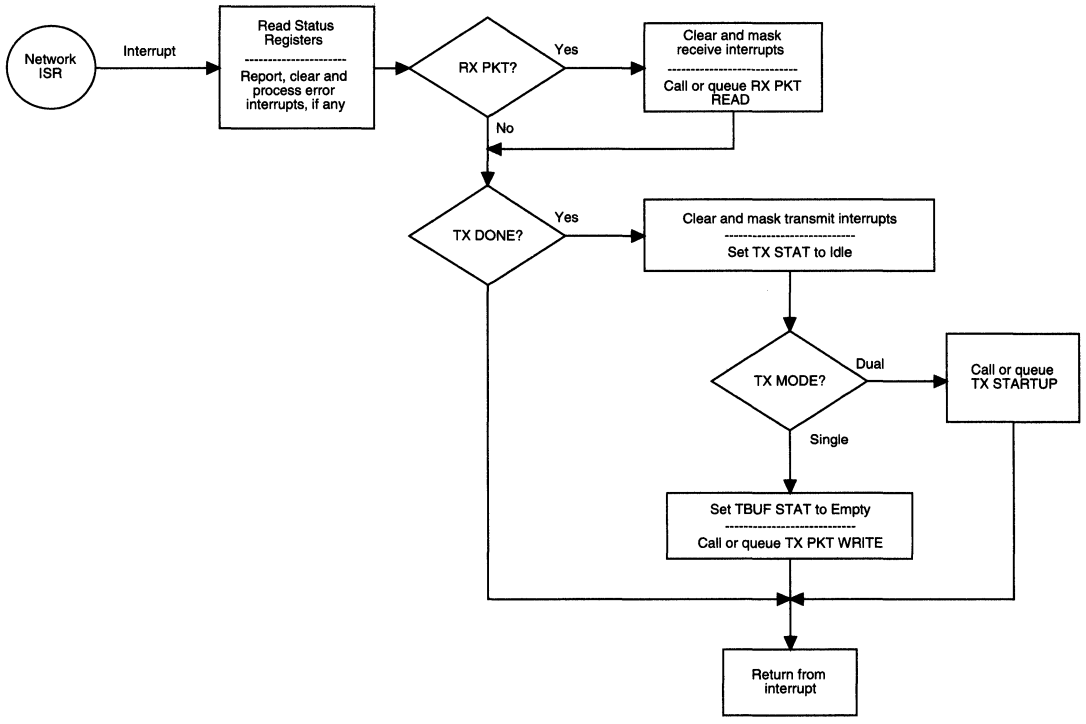


Figure 26. Network Interrupt Service Routine

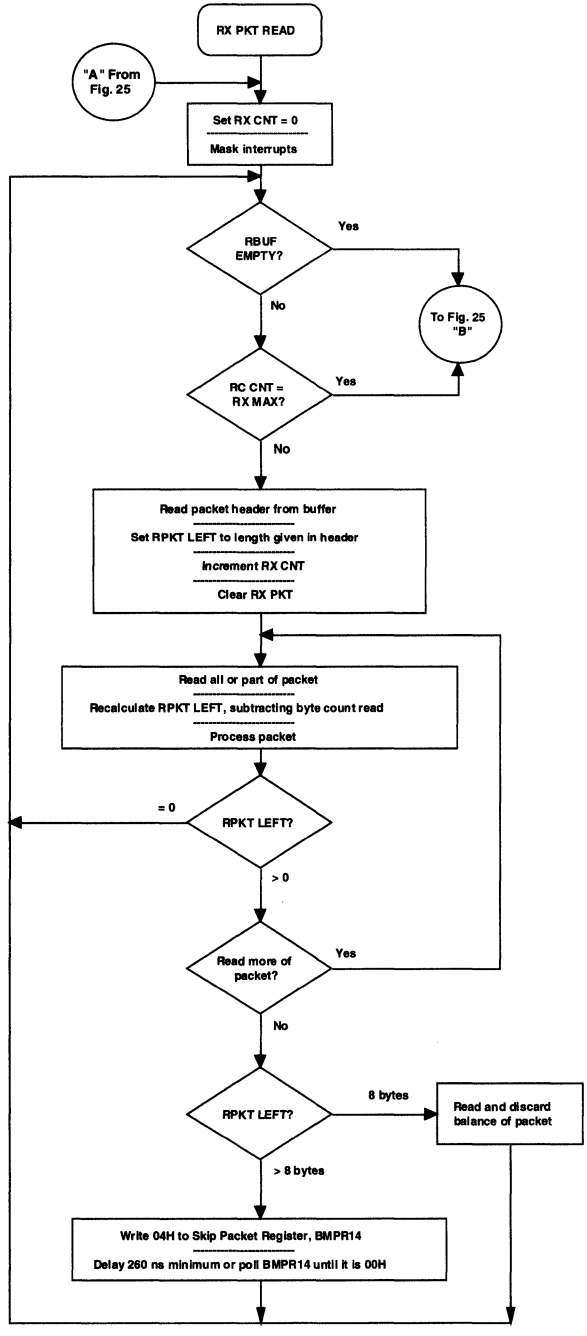


Figure 27. Receive Packet Read Routine

Table 32. Control and Status Parameters

SYMBOL	TYPE	NAME	DESCRIPTION
DLC EN	Register Bit	DATA LINK CONTROL ENABLE	When high, resets all buffer memory pointers and disables both the transmitter and the receiver circuits. When low, enables buffer memory, transmitter and receiver.
LBC	Register Bit	LOOPBACK CONTROL	When set low, places EtherCoupler in internal loopback mode.
RBUF EMPTY	Register Bit	RECEIVE BUFFER EMPTY	When high, indicates that there is at least one complete packet stored in the receive buffer, ready to read. When low, indicates there are no packets ready to read in the receive buffer.
RPKT LEFT	Software Value	RECEIVE PACKET LENGTH LEFT	The number of bytes remaining in the receive packet being read from the buffer. Calculated by the driver from the original length given by Ether-Coupler in the 3rd and 4th bytes of the receive packet header, less the number of bytes already read out.
RX CNT	Software Value	RECEIVE TRANSFER COUNT	A running count of the number of packets transferred from the receive buffer to system memory since entering the Receive Packet Read Routine. This parameter can share the same memory location with TX CNT, because both are not used concurrently in the same subroutine.
RX MAX	Software Value	MAXIMUM VALUE FOR RX CNT	The maximum number of packets that may be processed in the Receive Packet Read Routine.before passing control to the Transmit Packet Write Routine. This parameter can be fixed or allowed to vary according to need. Typical range for this parameter is 15 - 32.
TBUF FREE	Software Value	TRANSMIT BUFFER FREE SPACE	The number of available bytes remaining in the transmit buffer being loaded with packets by the driver. Calculated by driver.
TBUF MODE	Register Bits	TRANSMIT BUFFER MODE	The configuration of the transmit buffer space, SINGLE buffer or DUAL buffers.
TBUF SIZE	Software Value	TRANSMIT BUFFER SIZE	The size in bytes of each transmit buffer, which depends on initial configuration parameters for the buffer memory.
TBUF STAT	Software Value	TRANSMIT BUFFER STATUS	Current status of the transmit buffer available for loading packets. Maintained by the driver.

TBUF STAT	VALUE DESCRIPTION
Empty	Current transmit buffer available to system bus is completely empty.
Busy	No buffer is currently available to the system bus because a) EtherCoupler is in single-buffer mode and b) the transmitter is using the buffer.
Standby	The buffer currently available to the system bus has one or more packets in it, but may still have room for additional packet(s).
Full	The buffer currently available to the system bus has one or more packets in it, and does not have room for the next packet presented to the driver from the transmit queue.

SYMBOL	TYPE	NAME	DESCRIPTION
TPKT CNT	Software Value	TRANSMIT PACKET COUNT	The number of packets loaded into the current transmit buffer by the driver. Value is counted by driver. This value is written into EtherCoupler register BMPR10<6:0> at the time transmitter is started.
TX CNT	Software Value	TRANSMIT TRANSFER COUNT	A running count of the number of packets transferred from system memory to the transmit buffer since entering the Transmit Packet Write Routine. This parameter can share the same memory location with RX CNT, because both are not used concurrently in the same subroutine.
TX DONE	Register Bit	TRANSMITTER DONE	When transmitter finishes transmitting, EtherCoupler sets this bit high. Normally cleared by driver prior to starting transmitter. Hardware reset or DLC EN being set high also clears this bit.
TX MAX	Software Value	MAXIMUM VALUE FOR TX CNT	The maximum number of packets that may be processed in the Transmit Packet Write Routine before passing control to Receive Packet Read Routine. This parameter can be fixed or allowed to vary according to need. Typical range for this parameter is 15-32.
TX START	Register Bit	START TRANSMITTER	When set high, activates transmitter to transmit all packets in the current transmit buffer. See also TPKT CNT.
TX STAT	Software Value	TRANSMIT BUFFER STATUS	Current status of the- transmitter, maintained by driver.

TX STAT	VALUE DESCRIPTION
Busy	Transmitter has not finished transmitting packets previously given to it to transmit.
Idle	Transmitter has finished transmitting all packets in its buffer.

ELECTRICAL CHARACTERISTICS

OPERATIONAL SPECIFICATIONS

Table 33. Absolute Maximum Ratings

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
V_{CC}	Supply voltage	– 0.5	6.0	V
V_{IN}	Input voltage	– 0.5	V_{CC}+ 0.5	V
V_{OUT}	Output voltage	– 0.5	V_{CC} + 0.5	V
I_{ODF}	Differential output current on DOP pins		– 4 0	ma
V_{IDC}	Input DC voltage on DIP and CIP	– 0.5	16	V
V_{ODC1}	Output DC voltage on DOP without transformer	– 0.5	14	V
V_{ODC2}	Output DC voltage on DOP with transformer	– 0.5	16	V
T_{BIAS}	Temperature under bias	– 2 5	+85	°C
T_{STG}	Storage temperature	– 40	+125	°C
PWR	Power dissipation		787.5	mw

Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. No more than one output may be shorted to ground of V_{CC} at a time for a maximum duration of one second.

Table 34. Recommended Operating Conditions

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{DD}	Supply Voltage	4.75		5.25	V
V_{IH}	Logic input high voltage	2.2			V
V_{IL}	Logic input low voltage			0.8	V
R_L	Driver load resistors (across DOP and DON)	77	78	79.5	Ω
R_T	Termination resistors (two in series across DIP and CIP)	38.6	39	39.4	Ω
C_T	Termination bypass capacitors (between junction of termination resistors, ground)		0.1		µF
C_{OSC}	Oscillator load capacitors	12	20	38	pF
f_{XTAL}	Crystal oscillator frequency	19.999	20	20.001	MHz
T_A	Operating temperature	0		70	°C

Table 35. DC Specifications

SYMBOL	PARAMETER DESCRIPTION	CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IL}	Low-level input voltage		0.0		0.8	V
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{OL1}	Low-level output voltage, all outputs except DREQ	I_{OL} = 3.2 ma	0.0		0.4	V
V_{OL2}	Low-level output voltage, DREQ only	I_{OL} = 12 ma	0.0		0.4	V
V_{OL3}	Low-level output voltage, pins 130 – 132, 151, and 128	I_{OL} = 24 ma	0.0		0.4	V
V_{OH1}	High-level output voltage, all outputs except DREQ	I_{OH} = –2 ma	4.2		V_{CC}	V
V_{OH2}	High-level output voltage, DREQ only	I_{OH} = –4 ma	4.2		V_{CC}	V
V_{OH3}	High-level output voltage, pins 130 – 132, 151, and 128	I_{OH}= –8 ma	4.2		V_{CC}	V
V_{OP}	DOP peak output	R_L = 270	±0.5		±1.3	V
V_{ACCM}	Output AC common mode on DOP	R_T = 78			±40	mV
V_{DCCM}	Output DC common mode on DOP	R_L = 270	2.4	3.4	4.4	V
V_{SQ}	Squelch threshold	AC/DC = 1 AC/DC = 0	–300 –80	–220 0	–140 +80	mV
I_L	Input leakage current	V_I = 0 – V_{CC}	–10		10	µa
I_{PWRDN}	Powerdown V_{CC} current	No output loads		4	10	ma
I_{IDLE}	Idle V_{CC} current	No output loads		83	100	ma
I_{CC}	Operating V_{CC} current	No output loads		110	150	ma

Table 36. General Capacitance

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
C_{IN}	Input pin capacitance		16	pF
C_{OUT}	Output pin capacitance		16	PF
$C_{I/O}$	I/O pin capacitance		16	pF
T_A = 25°C, V_{DD} = V_I = 0 volts, and f = 1 megahertz				

Table 37. AUI Electrical Characteristics

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
IIL	Input low current			–700	ma
IIH	Input high current Figures for design aid only; not guaranteed and not subject to production testing.			500	µa
VOD	Differential output voltage	±550		±1200	mV
VDS	Differential squelch threshold		220		mV
Typical figures are at 25°C and are used for design aid only; not guaranteed and not subject to production testing. TA = 0°C to +70°C, VCC = 5 V±5%					

Table 38. Twisted-pair Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	MAXIMUM	UNITS
Z_{OUT}	Transmit output impedance		5		
V_{OD}	Peak differential output voltage	Load = 100 ohms at TPOP and TPON	3.5		V
J_{OUT}	Transmit timing jitter addition Parameter is guaranteed by design; not subject to product testing.	0 line length After line model specified by IEEE 802.3 for 10BASE-T		±8 ±3.5	ns
Z_{IN}	Receive input impedance	Between TPIP/TPIN, CIP/CIN and DIP/ DIN	20	0	k
V_{DS}	Differential squelch threshold		420		mV
V_{DSL}	Lower squelch threshold		250		mV
Typical figures are at 25°C and are used for design aid only; not guaranteed and not subject to production testing. T_A = 0°C to +70° C, V_{CC} = 5 V ±5%					

Table 39. Switching Characteristics

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
Jabber Timing	Maximum transmit time	20		150	ms
	Unjab time	250		750	
Link Integrity Timing	Time link loss	55		66	ms
	Time between link integrity pulses	8		24	
	Interval for valid receive link integrity pulses	4.1		65	
General	Receive startup delay	0		500	ns
	Transmit startup delay	0		200	
	Loopback startup delay	0		500	
	(These parameters are guaranteed by design and not subject to product testing.)				
T_A = 0°C to +70°C, V_{CC} = 5 V±5%					

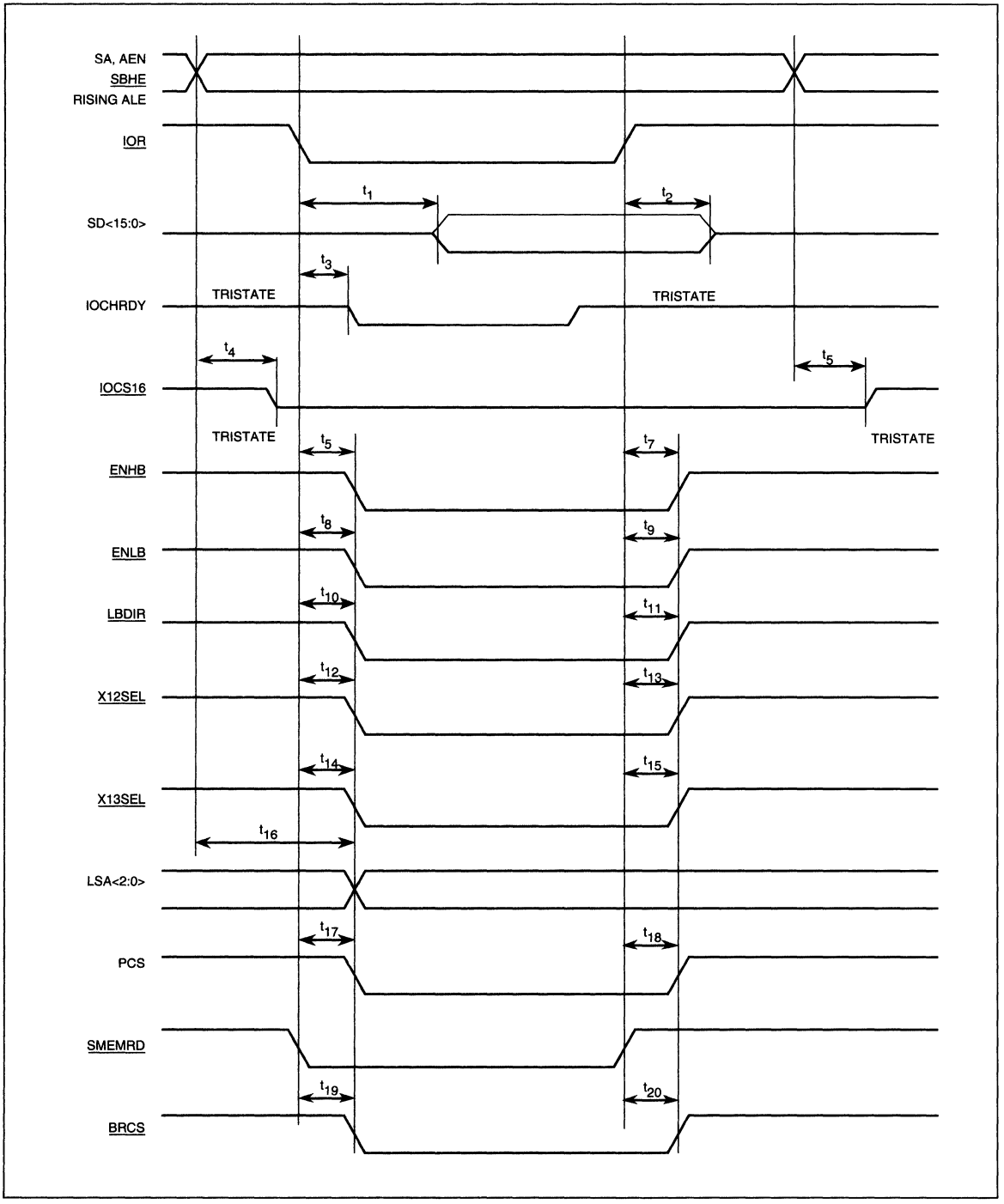
TIMING DIAGRAMS

Table 40. lists operational modes in which EtherCoupler may operate, and for which timing diagrams are specified in Tables 41-57.

Table 40. Operational Modes

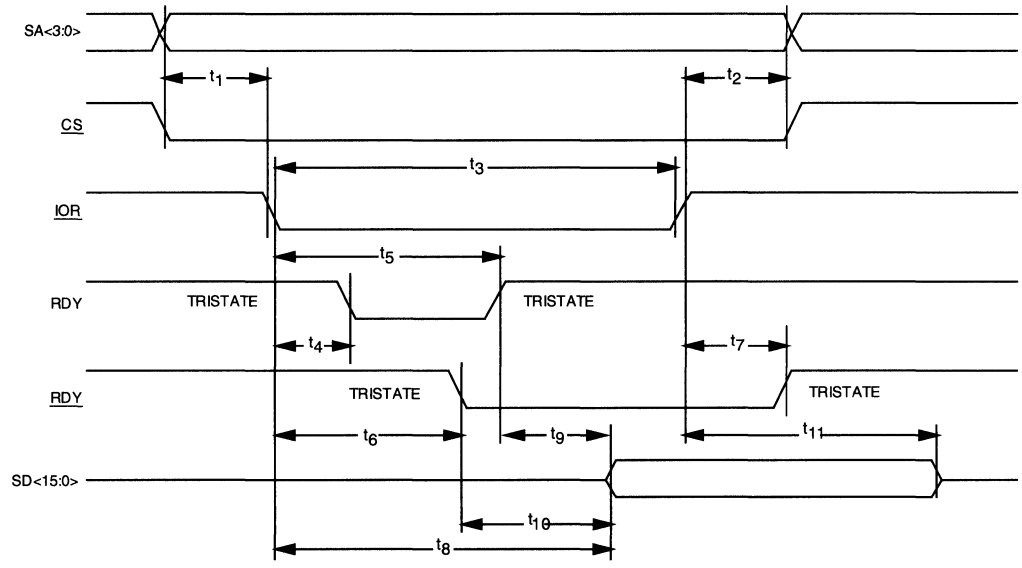
MODE NO.	BUS	PIN 90	PIN 91	PIN 92	OPERATION	INITIAL PARAMETERS
0	ISA	0	0	0	Jumperless	Stored in bit-serial EEPROM.
1	ISA	0	0	1	Jumpers	Stored in bit-serial EEPROM.
2	ISA	0	1	0	Jumpers	Stored in byte-parallel ID PROM.
3	Non-ISA	0	1	1	Jumpers	Functions identical to MB86960 NICE (Network interface Controller with Encoder/ decoder) chip.
X	—	1	X	X	—	Reserved.

Table 41. Read Cycle (Mode 0–2)



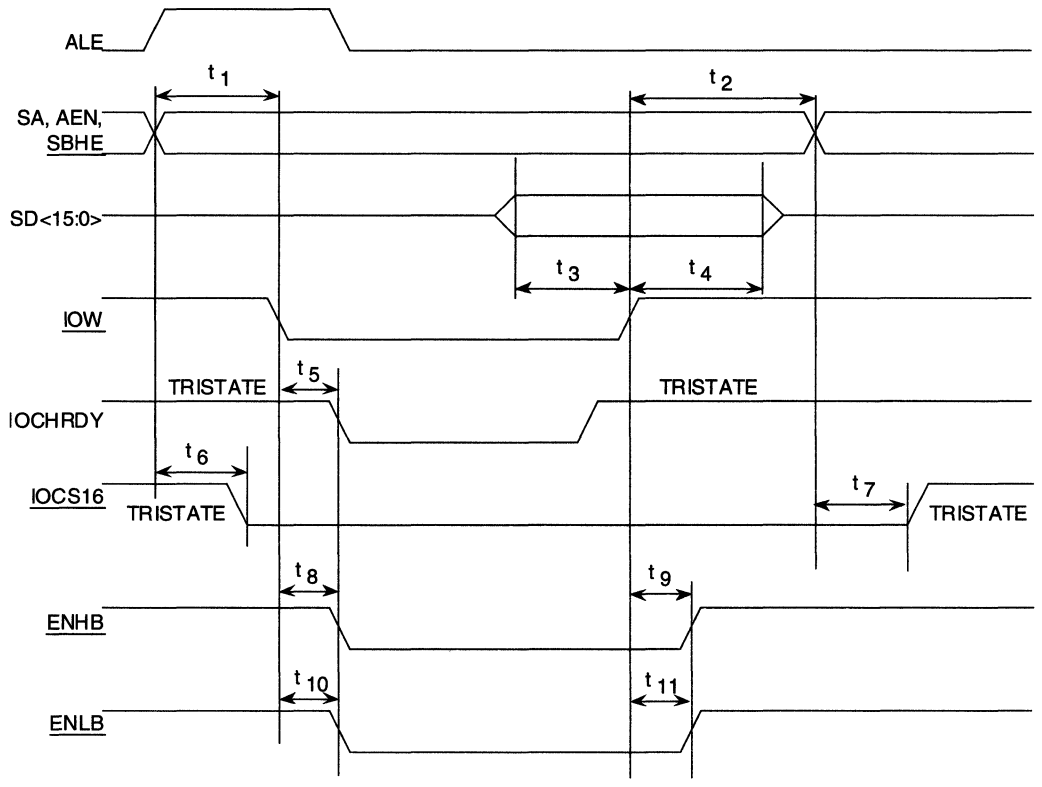
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	IOR to SD<15:0> enable			38	ns
t_2	IOR to SD<15:0> tristate			38	ns
t_3	IOR to IOCHRDY not ready		14	—	ns
t_4	SA, AEN, SBHE to IOCS16 Tristate to low			28	ns
t_5	SA, AEN to IOCS16 low to Tristate			71	ns
t_6	IOR to ENHB active			46	ns
t_7	IOR to ENLB active			24	ns
t_8	IOR to ENLB inactive			45	ns
t_9	IOR to LBDIR active			24	ns
t_{10}	IOR to ENLB inactive			42	ns
t_{11}	IOR to LBDIR inactive			21	ns
t_{12}	IOR to X12SEL active			44	ns
t_{13}	IOR to X12SEL inactive			23	ns
t_{14}	IOR to X13SEL active			45	ns
t_{15}	IOR to X13SEL inactive			24	ns
t_{16}	SA, AEN, rising ALE to LSA<2:0> stable (Mode 2)			21	ns
t_{17}	IOR to EPCS active (Mode 2)			45	ns
t_{18}	IOR to EPCS inactive (Mode 2)			23	ns
t_{19}	SMEMRD to BRCS active			44	ns
t_{20}	SMEMRD to BRCS inactive			20	ns

Table 42. Read Cycle (Mode 3)



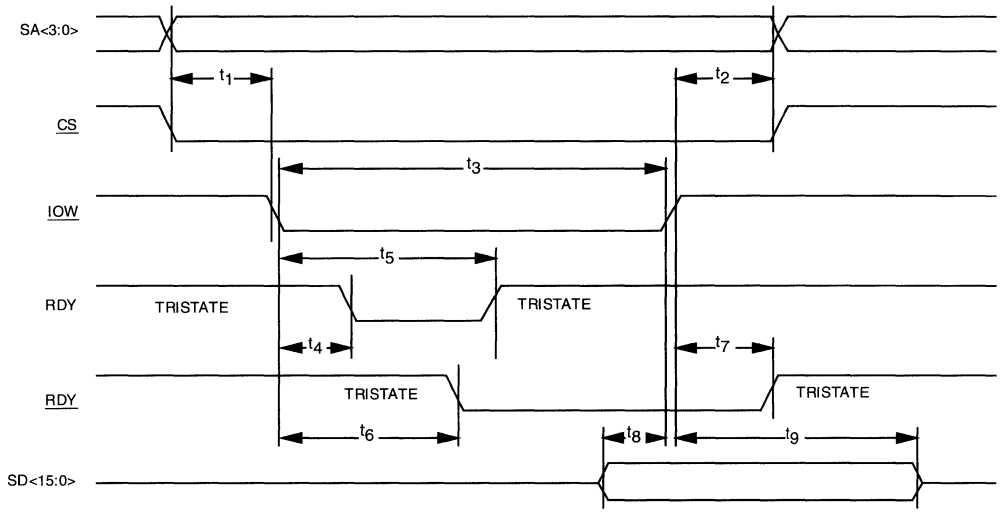
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	SA<3:0> valid to IOR low; CS low to IOR low.	3		ns
t_2	IOR high to SA<3:0> invalid; IOR high to CS high.	3		ns
t_3	IOR low pulse width.	30		ns
t_4	IOR low to RDY low.	0	26	ns
t_5	IOR low to RDY Tristate.		175	ns
	For registers and Buffer Port when port is ready before the read cycle begins.	0	7	ns
	For port access only, if system makes contiguous system read cycles at less than 100 ns intervals, and the network is busy.		175	ns
	For bus read error.		2.15	µs
t_6	IOR low to RDY low.	0	175	ns
	For all registers.		28	ns
	For port access only, if system makes contiguous system read cycles at less than 100 ns intervals, and the network is busy.		175	ns
	For bus read error.		2.15	µs
t_7	IOR high to RDY Tristate.		28	ns
t_8	IOR low to SD<15:0> valid (registers).		44	ns
t_9	RDY Tristate to SD<15:0> valid (buffer port).		8	ns
t_{10}	RDY low to SD<15:0>valid.		10	ns
t_{11}	IOR high to SD<15:0> invalid (data hold).	15		ns

Table 43. Write Cycle (Mode 0–2)



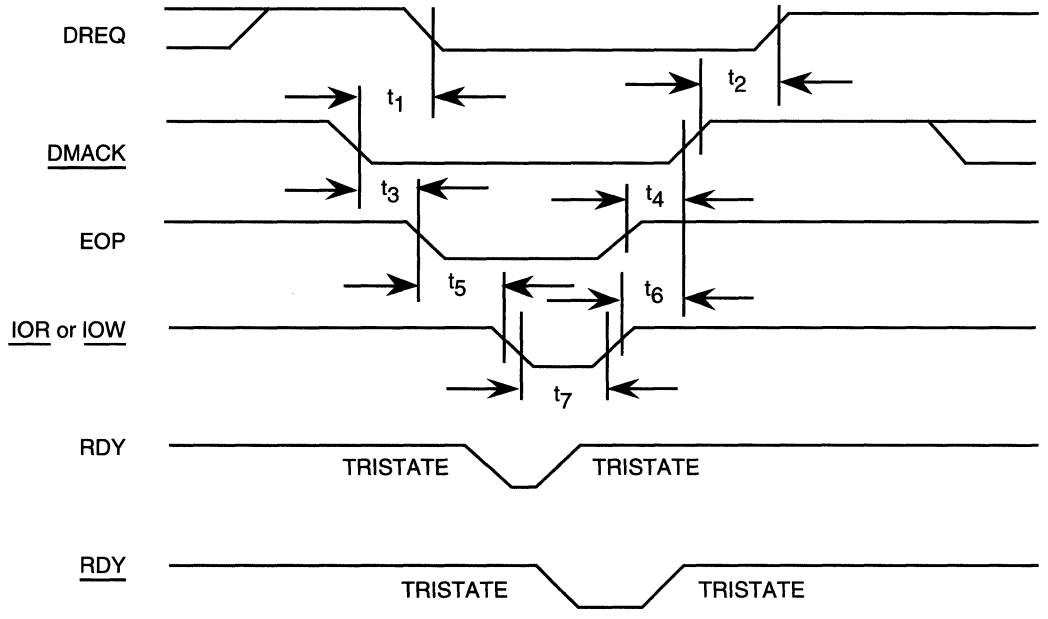
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	SA, SBHE and AEN setup time to IOW low	15			ns
t_2	Hold time of SA, SBHE and AEN after IOW high (up to leading edge of next cycle ALE)	21			ns
t_3	Setup time of SD to IOW high	5			ns
t_4	Hold time of SD after IOW low	33			ns
t_5	IOW to IOCHRDY not ready		14		ns
t_6	SA, AEN, SBHE to IOCS16 low to Tristate			38	ns
t_7	SA, AEN to IOCS16 Tristate to low			71	ns
t_8	IOW to ENHB active			47	ns
t_9	IOW to ENHB active			24	ns
t_{10}	IOW to ENLB inactive			45	ns
t_{11}	IOW to ENLB inactive			25	ns
AC characteristics: V_{CC} = 5.0 ±5%; T_A = 0°C to +70°C					

Table 44. Write Cycle (Mode 3)



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	SA<3:0> valid to IOW low; CS low to IOW low.	3		ns
t_2	IOW high to SA<3:0> invalid; IOW high to CS high.	3		ns
t_3	IOW low pulse width.	36		ns
t_4	IOW low to RDY low.	0	26	ns
t_5	IOW low to RDY Tristate.		175	ns
	For registers and Buffer Port when port is ready before the write cycle begins.	0	7	ns
	For port access only, if system makes contiguous system write cycles at less than 100-ns intervals, and both the transmitter and receiver are active in loopback reception.		175	ns
t_6	IOW low to RDY low.	0	175	ns
	For all registers.		28	ns
	For port access only, if system makes contiguous system write cycles at less than 100-ns intervals, and transmitter and receiver are active in loopback reception.		175	ns
t_7	IOW high to RDY Tristate.		28	ns
t_8	SD<15:0> invalid (data setup).	5		ns
t_9	IOW high to SD<15:0> invalid (data hold).	6		ns

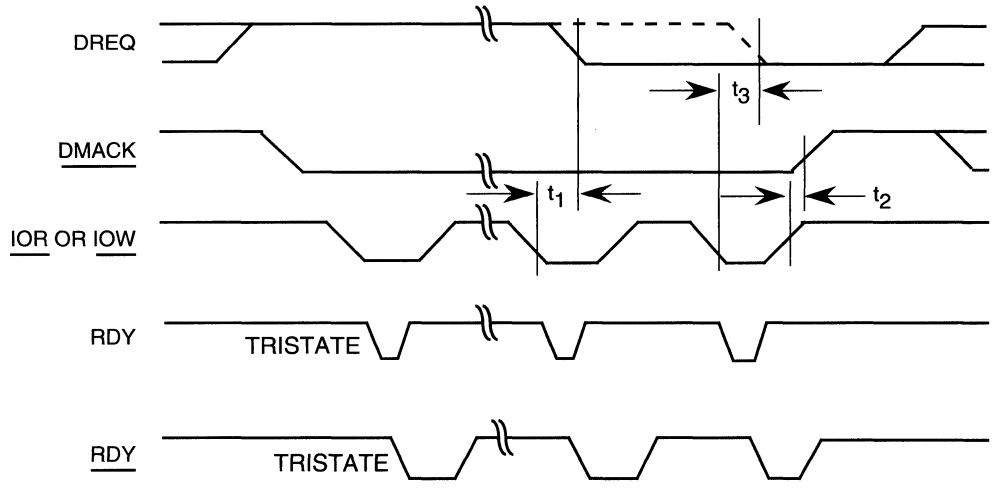
Table 45. Single–cycle DMA Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	DMACK low to DREQ low	0	21	ns
t_2	DMACK high to DREQ high	0	19	ns
t_3	DMACK low to IOR or IOW low	0		ns
t_4	IOR or IOW high to DMACK high	3		ns
t_5	IOR or IOW low to EOP low	0		ns
t_6	EOP high to DMACK high	3		ns
t_7	EOP low pulse width	10		ns

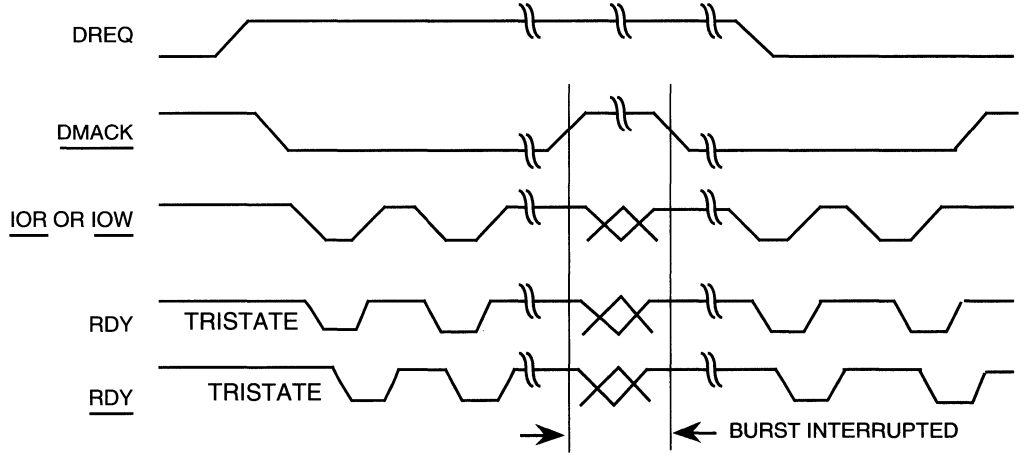
All of the IOR, IOW and EOP low–going pulses must fall inside of the DMACK low–going pulse. An asserted EOP terminates any further DREQ after DMACK returns high. The DMA cycle uses DMACK as the chip select. DMACK overrides SA<3:0>, forcing selection of the Buffer Memory Port as in a DMA cycle.

Table 46. Burst DMA Timing



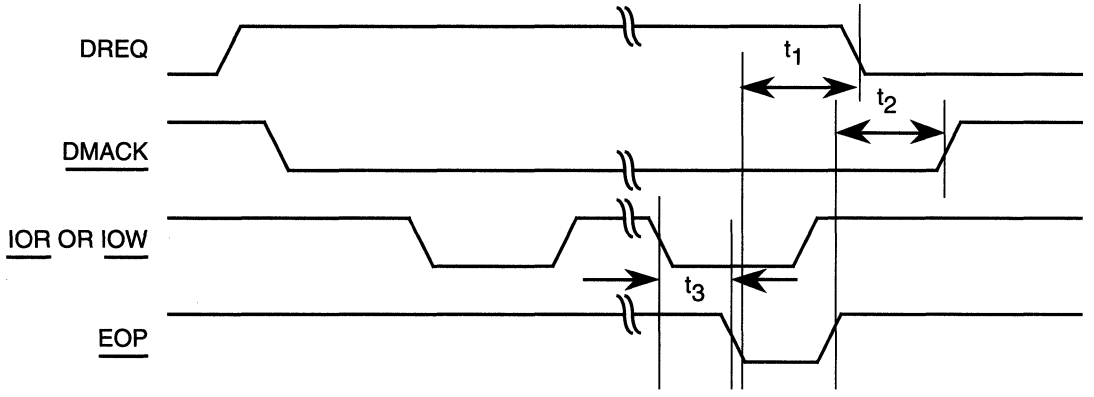
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	IOR or IOW low to DREQ low		32	ns
t_2	IOR or IOW high to DACK high	3		ns
t_3	IOR or IOW low to DREQ low, if DREQ EXTND (DLCR4<2>) is set to 1 (default).		32	ns

All of the IOR or IOW low–going pulse must fall inside of the DMACK low–going pulse. The DMA cycle uses DMACK as the chip select. DMACK overrides SA<3:0>, forcing selection of the Buffer Memory Port as in a DMA cycle. DREQ goes low during the next–to–last transfer of the burst, and can be extended from the next-to-last transfer cycle when DREQ EXTND, DLCR4<2>, is low to the last transfer cycle when DREQ EXTND is high.



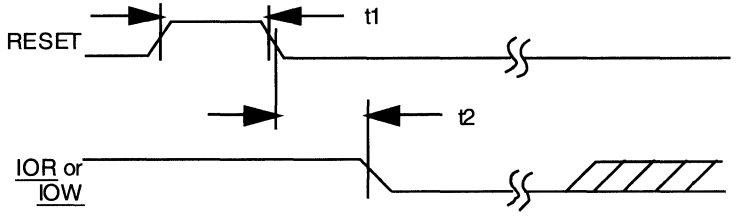
Burst can be interrupted by DMACK high-going pulse during the burst. Burst will resume when DMACK returns low. DREQ goes low during the next-to-last transfer of the burst

Table 47. Burst DMA terminated by EOP



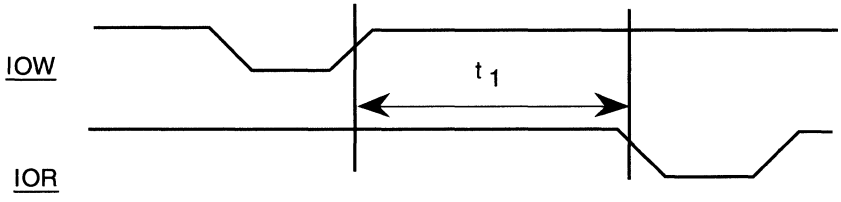
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	EOP low to DREQ low	4	28	ns
t_2	EOP high to DMACK high	3		ns
t_3	IOR or IOW low to EOP low	0		ns

Table 48. RESET Timing



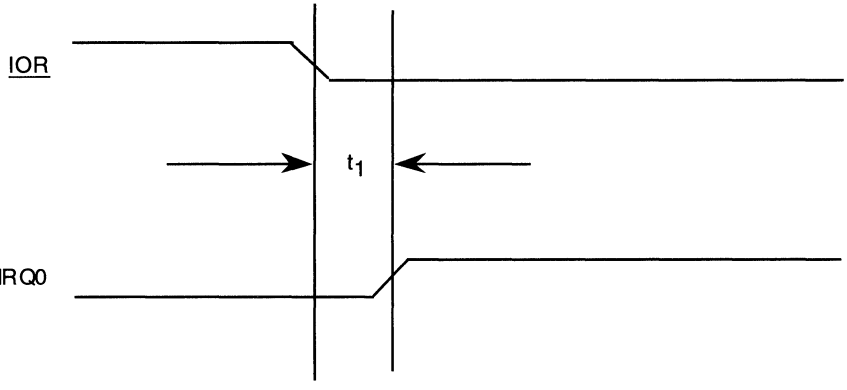
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	RESET pulse width	200		ns
t_2	RESET low to first IOR or IOW low	300		ns
Before enabling Transmit and Receive functions, wait 200μ sec after reset pulse for stabilization of receiver PLL.				

Table 49. Skip Packet Timing



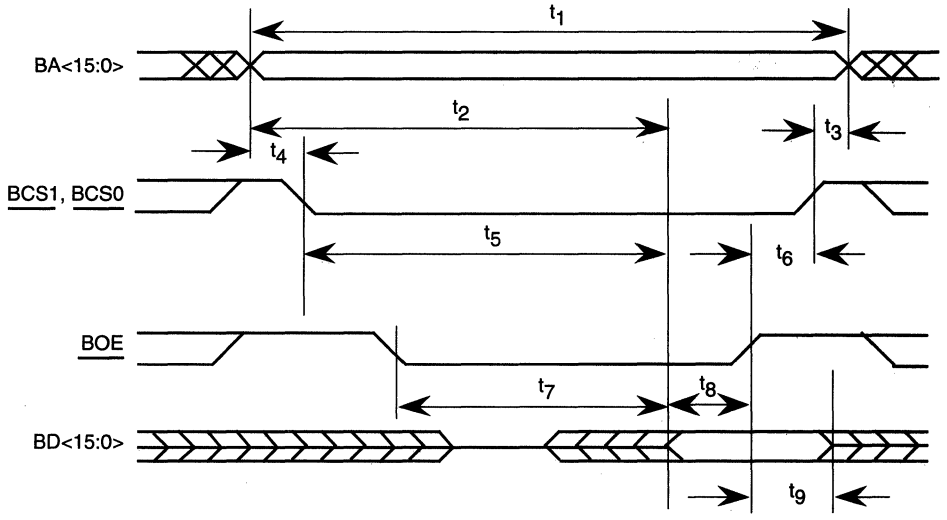
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	Writing skip packet high to next Buffer Memory Port read	300		ns

Table 50. IRQ Timing



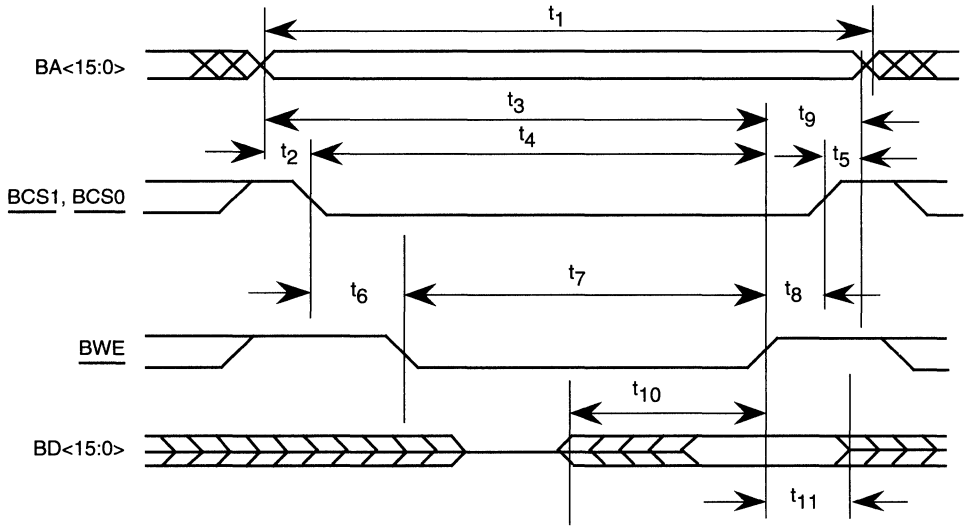
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_3	IRQ0 signal-clearing delay	30		80	ns

Table 51. SRAM Read Timing



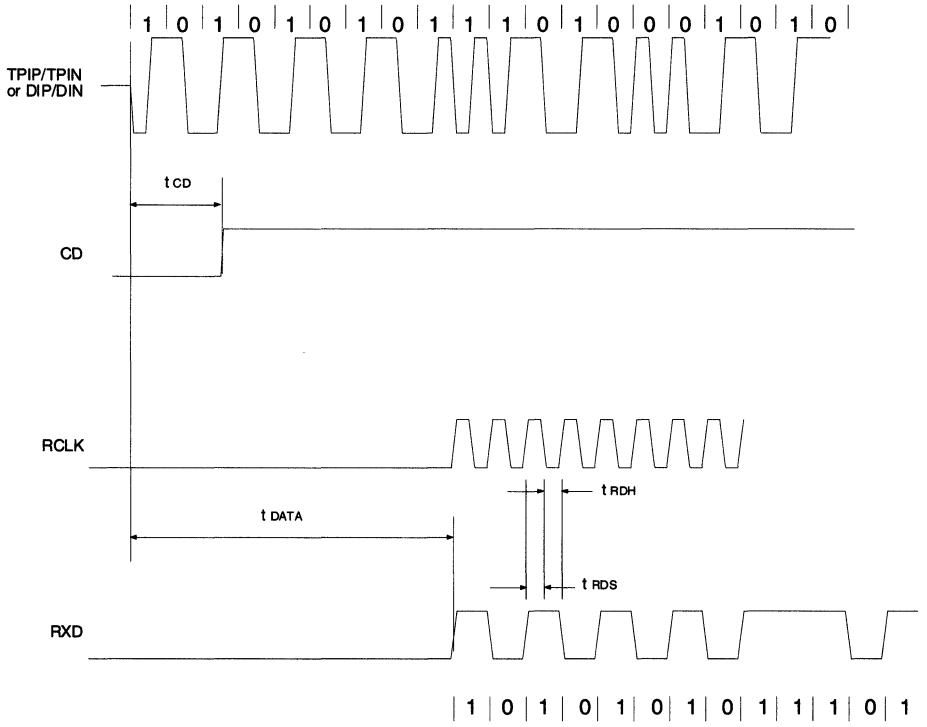
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	Read cycle, 100 ns	95	100	105	ns
	Read cycle, 150 ns	145	150	155	ns
t_2	T_{AA}, address access time			81	ns
t_3	BCS1, BCS0 high to address invalid	0			ns
t_4	Address valid to BCS1, BCS0 low	0		8	ns
t_5	T_{AC} chip select access time			81	ns
t_6	BOE high to BCS1, BCS0 high	0		2	ns
t_7	T_{OE} output enable access time			49	ns
t_8	Data setup time	15			ns
t_9	Data hold time	0			ns
Use SRAM with T_{AA} of 80 ns or less.					

Table 52. SRAM Write Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	Write cycle, 100 ns	95	100	105	ns
	Write cycle, 150 ns	145	150	155	ns
t_2	Address valid to BCS1, BCS0 low	2		8	ns
t_3	Address valid to BWE high	71			ns
t_4	BCS1, BCS0 low to BWE high	62			ns
t_5	BCS1, BCS0 high to address invalid	0			ns
t_6	BCS1, BCS0 low to BWE low	0			ns
t_7	BWE Pulse Width	60			ns
t_8	BWE high to BCS1, BCS0 high	0			ns
t_9	BWE high to address invalid	12			ns
t_{10}	Data setup time	41			ns
t_{11}	Data hold time	14			ns
Use SRAM with T_{AA} of 80 ns or less					

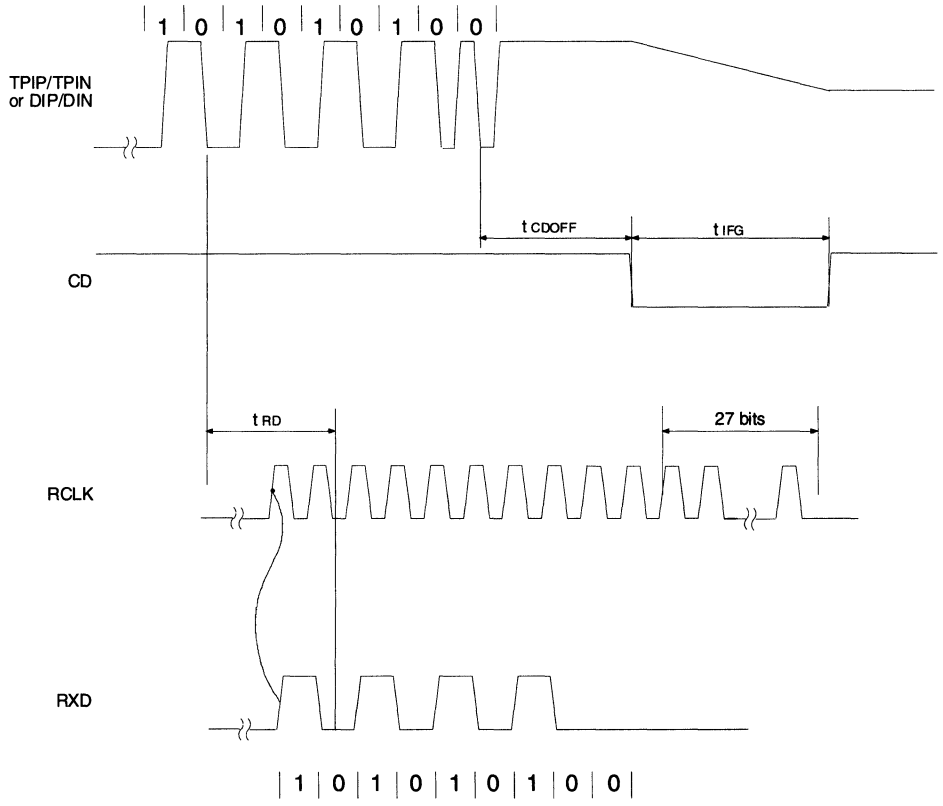
Table 53. RCLK/Start of Frame Timing (Mode 3) — For Reference Only



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{CD}	CD turn-on delay - AUI	—	900	—	ns
t_{CD}	CD turn-on delay - TP	—	1300	—	ns
t_{DATA}	Decoder acquisition time - AUI	—	50	—	ns
t_{DATA}	Decoder acquisition time - TP	—	400	—	ns
t_{RDH}	Receive data hold from RCLK	30	—	—	ns
t_{RDS}	Receive data setup from RCLK	30	—	—	ns

The CD, RCLK and RXD signals are internal to the EtherCoupler chip, and are provided for reference only. The RXD signal changes at the rising edge of RCLK. The controller is sampled at the falling edge.

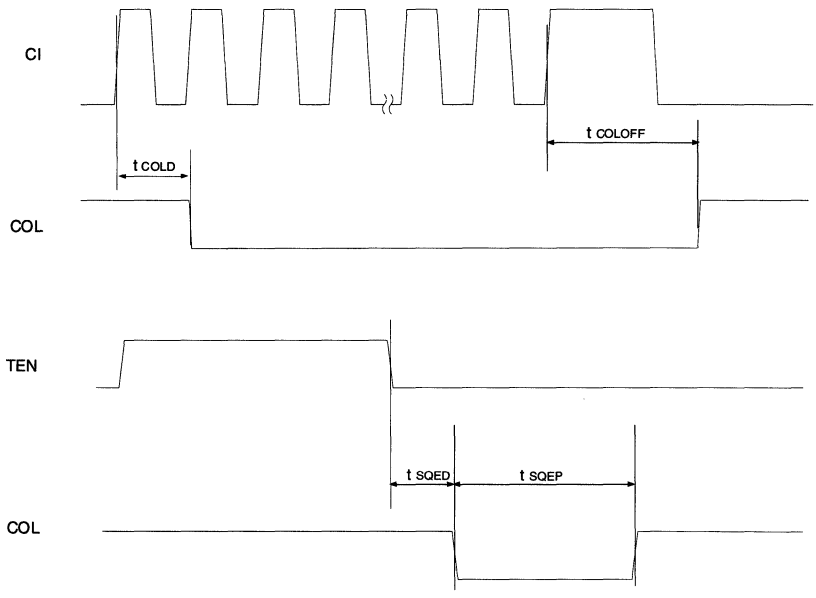
Table 54. RCLK/End of Frame Timing (Mode 3) — For Reference Only



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{RCH}	RCLK hold after CD low	27	—	—	bit time
t_{RD}	RCV data throughput delay	—	275	—	ns
t_{CDOFF}	CD turn-off delay, measured from middle of last bit, so that timing specification is unaffected by the value of the last bit.	—	375	—	ns
t_{IFG}	Receive block out	—	2	—	bit time

The CD, RCLK and RXD signals are internal to the EtherCoupler chip, and are provided for reference only. The RXD signal changes at the rising edge of RCLK. The controller is sampled at the falling edge. Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

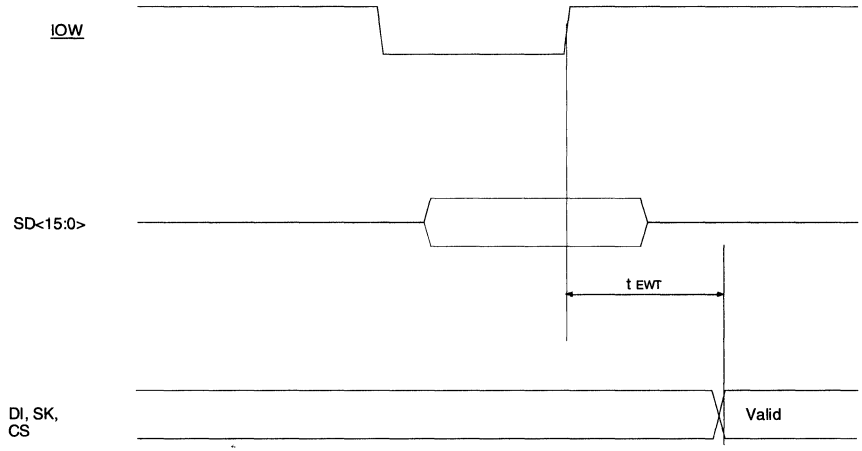
Table 55. Collision Detect and COL/CI Output Timing (Mode 3) — For Reference Only



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{COLD}	COL turn-on delay	—	50	—	ns
t_{COLOFF}	COL turn-off delay	—	160	—	ns
t_{SQED}	SQE delay	0.65	—	1.6	ns
t_{SQEP}	SQE pulse duration	500	—	1500	ns

The CI, COL and TEN signals are internal to the EtherCoupler chip, and are provided for reference only. Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

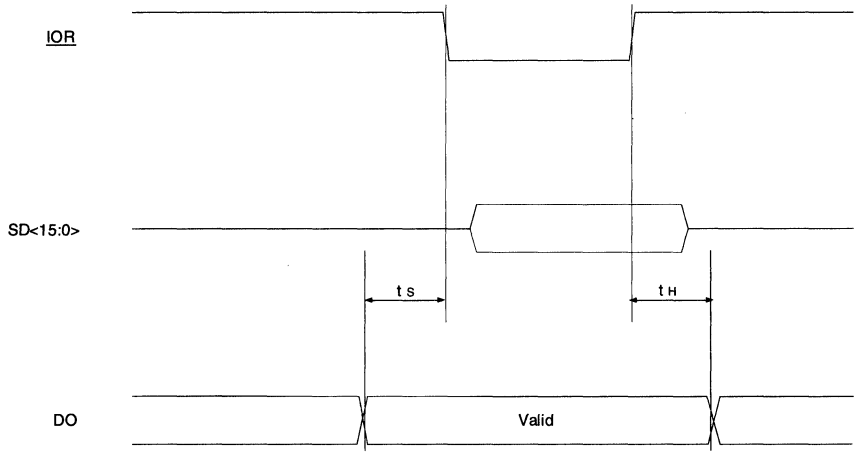
Table 56. EEPROM Write Timing (Mode 0 – 2)



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_{EWT}	IOW to DI, SK CS valid	9	—	24	ns

The SD signal is for reference only.

Table 57. EEPROM Read Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_S	DO valid to IOR	2	—	—	ns
t_H	IOR to DO invalid	2	—	—	ns

The SD signal is for reference only.

ETHERCOUPLER BOARD

INTRODUCTION

The EtherCoupler Ethernet adapter card is an I/O board that provides a reliable, high-performance networking interface between an IBM XT or AT-compatible personal computer and Ethernet. It supports three types of cables: standard Ethernet (10BASE5), thin Ethernet (10BASE2), and twisted-pair Ethernet (10BASE-T). 10BASE5 is supported by use of an external remote transceiver unit; 10BASE2 is supported on board directly by the MBL8392A transceiver chip; 10BASE-T is supported on board directly by the MB86965 EtherCoupler chip.

The EtherCoupler board occupies 32 bytes of the 1 kilobyte I/O space of the PC, and 16 kilobytes of the memory space for the Boot PROM. The EtherCoupler controller is completely I/O mapped, and occupies 16 of the 32 I/O addresses. Eight of the other 16 addresses are used to read the Ethernet ID PROM: one is used for jumperless operation control, while the remaining seven are reserved for future use. When using the board in 8-bit mode, all I/O is presented to the bus as 8-bit transfers on the lower byte of the data bus. When using the 16-bit mode, the EtherCoupler controller is presented as a 16-bit device, while the ID PROM and boot PROM are still 8-bit devices. The boot PROM is the only device on the board that resides in the memory space of the bus, and is only used in special applications.

Figure 28 illustrates the location of EtherCoupler board components, and Table 58 lists EtherCoupler board parts.

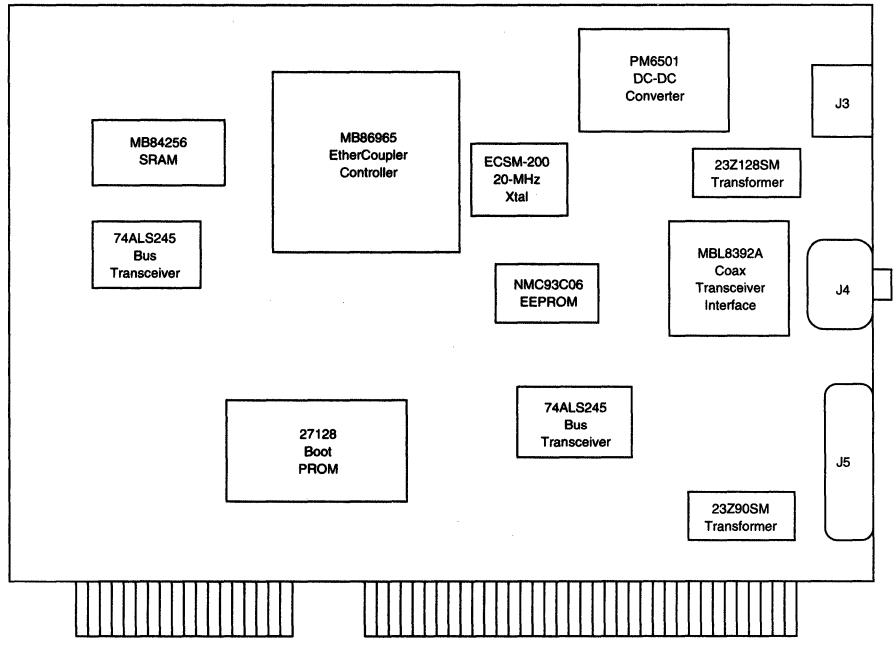


Figure 28. Ethercoupler Board Component Locations

Table 58. EtherCoupler Board Parts List

Item	Quantity	Reference	Value/PART	Vendor Part Number
1	3	C1, C4, C8	22 mF	
2	8	C2, C3, C5, C10, C11, C12, C13, C14	0.1 mF	
3	2	C6, C7	20 pF	
4	1	C9	10mF	
5	2	C15, C16	.001 mF	
6	1	C17	0.01 mF	
7	1	C18	0.01 mF	
8	2	DS1, DS2	LED	
9	1	F1	2.5 A	
10	1	J1	CON AT62	
11	1	J2	CON AT36	
12	1	J3	RJ45	
13	1	J4	BNC	
14	1	J5	CON DB15	
15	2	R1, R2	120 kilohms	
16	1	R3	12.4 kilohms ± 1%	
17	2	R4, R6	75 ohms ± 1%	
18	2	R5, R7	37.5 ohms ± 1%	
19	2	R8, R9	50 ohms ± 1%	
20	4	R10, R11, R12, R13	470 ohms	
21	1	R14	82 ohms	
22	4	R15, R16, R17, R18	1.5 kilohms	
23	1	R19	1 kilohm ± 1%	
24	1	R20	1 megohm	
25	4	R21, R22, R23	78 ohms	
26	1	R24	60 ohms	
27	1	SA1	Spark Arrestor	
28	1	T1	Transformer	Fil-Mag 23Z90SM
29	1	T2	Transformer	Fil-Mag 23Z128SM
30	1	U1	SRAM	Fujitsu MB84256
31	2	U2, U7	Bus Transceiver	74ALS245
32	1	U3	EtherCoupler Controller	Fujitsu MB86965
33	1	U4	Boot PROM	27128
34	1	U6	EEPROM	NMC93C06
35	1	U8	10BASE2 Transceiver	Fujitsu MBL8392A
36	1	U9	DC-DC CONverter	Valor PM6501
37	1	Y1	20 MHz Crystal	Ecliptek ECSM-200

ETHERCOUPLER PC BOARD LAYOUT INSTRUCTIONS

Guidelines

When laying out a PC board which uses the Fujitsu EtherCoupler chip set, the following guidelines should be observed:

1. Use a 0.1-microfarad bypass capacitor at the top or bottom of every IC. Bypass 12V and 5V. Include several bypass capacitors for the MB86965; this devices has many output drivers. The trace length from the device VCC and ground pins to the associated bypass capacitor should be as short as possible.
2. Use several 22-mF tantalum filter capacitors on +5V, and space these evenly throughout the board.
3. For two layer boards, use a 50-mil traces for both VCC and ground. Be sure that they are well grounded throughout the board. (However, we don't recommend building a two-layer board)
4. Ensure that there are no traces or feedthroughs under crystals or crystal oscillators. Provide adequate clearance for components around crystals and crystal oscillators. Also, put a ground pad under the crystals and associated resistors and capacitors. Do not put a solder mask over the ground pad that is under the crystal.
5. Crystals and associated discrete components should be placed as close as possible to the corresponding oscillator IC.
6. Due to a lack of ground signals on the PC bus connector, the CHRESET signal is susceptible to crosstalk from the data bus. Two-layer boards are especially vulnerable to this problem. To eliminate glitches on this signal, use a 50-mil trace, put a ground trace next to it, and put a 0.1-mF capacitor near the CHRESET receiver. An RC filter next to the bus connector is recommended.
7. The RBIAS resistor is used as a reference by the MB86965's analog section. It should be 12.4 KΩ ± 1% tolerance, and care must be taken to tie it to a low-noise point on the ground plate.
8. Keep digital signals away from the Thinnet BNC signals.
9. The 8392 COAX Transceiver should be placed as close to the BNC connector as possible to minimize stray capacitance and inductance on the tap.

Checklist

1. Check IC pack placement.
2. Do a preliminary mechanical check for board size, connector locations, and mounting-hole locations.
3. Check the wire list.
4. Check the IC pin numbers on the schematics.
5. Verify that the above layout instructions have been followed.
6. Check pinouts of special devices on the layout (PLCCs).
7. Check orientation, pinouts, and pin spacing of all connectors.
8. Check the silkscreen.
9. Check the clearance of special components, e.g., connectors, capacitors, CPU.
10. Check the clearance around mounting holes.
11. Check mechanical dimensions shown in the layout specification drawing.
12. Check the orientation of polarized capacitors. The position of pin 1 should be consistent.
13. Check the orientation of three-pin jumpers. The position of pin 1 should be consistent.
14. Check the VCC and ground grid.
15. Visually inspect plots for each layer. Check for air gaps, pad sizes, and cross-net shorts.

ETHERCOUPLER PC BOARD SCHEMATICS

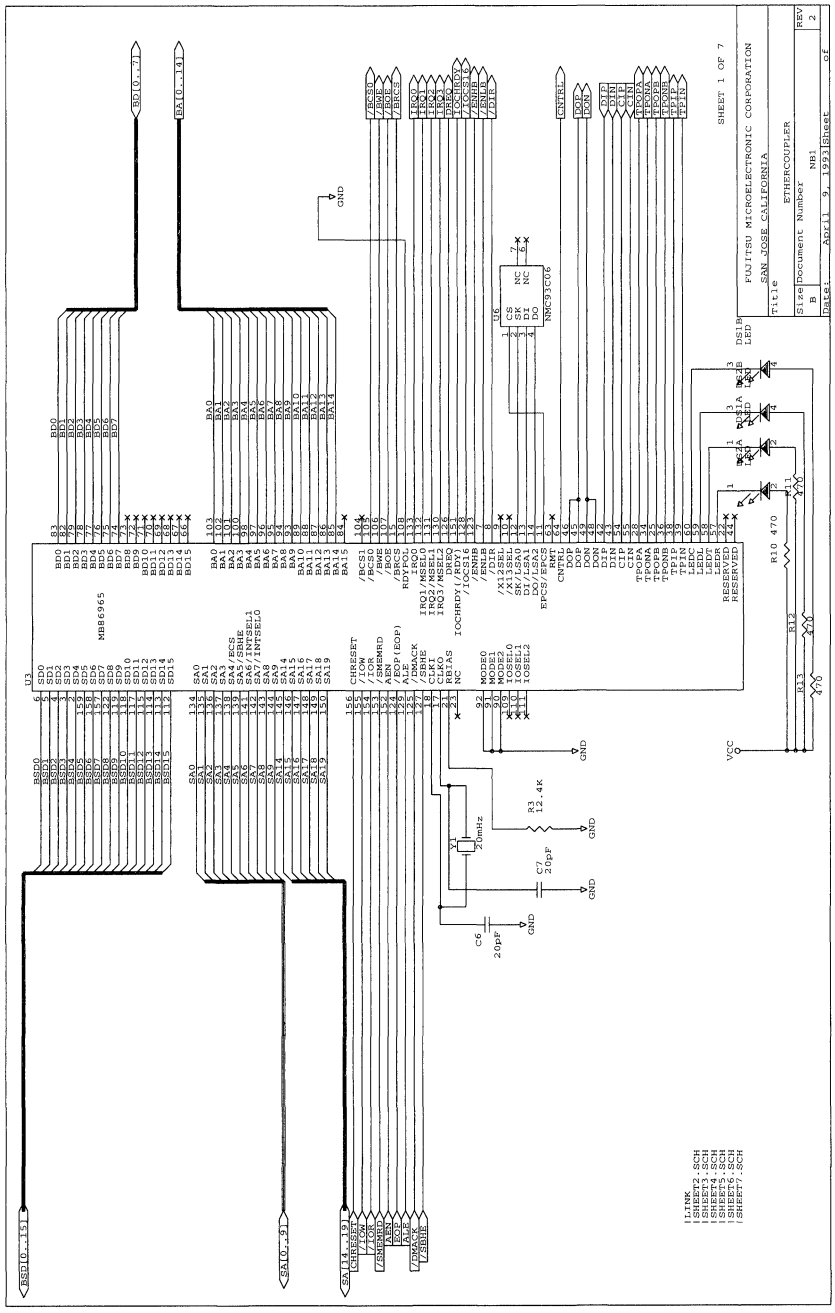


Figure 29. EtherCoupler, EEPROM and Crystal

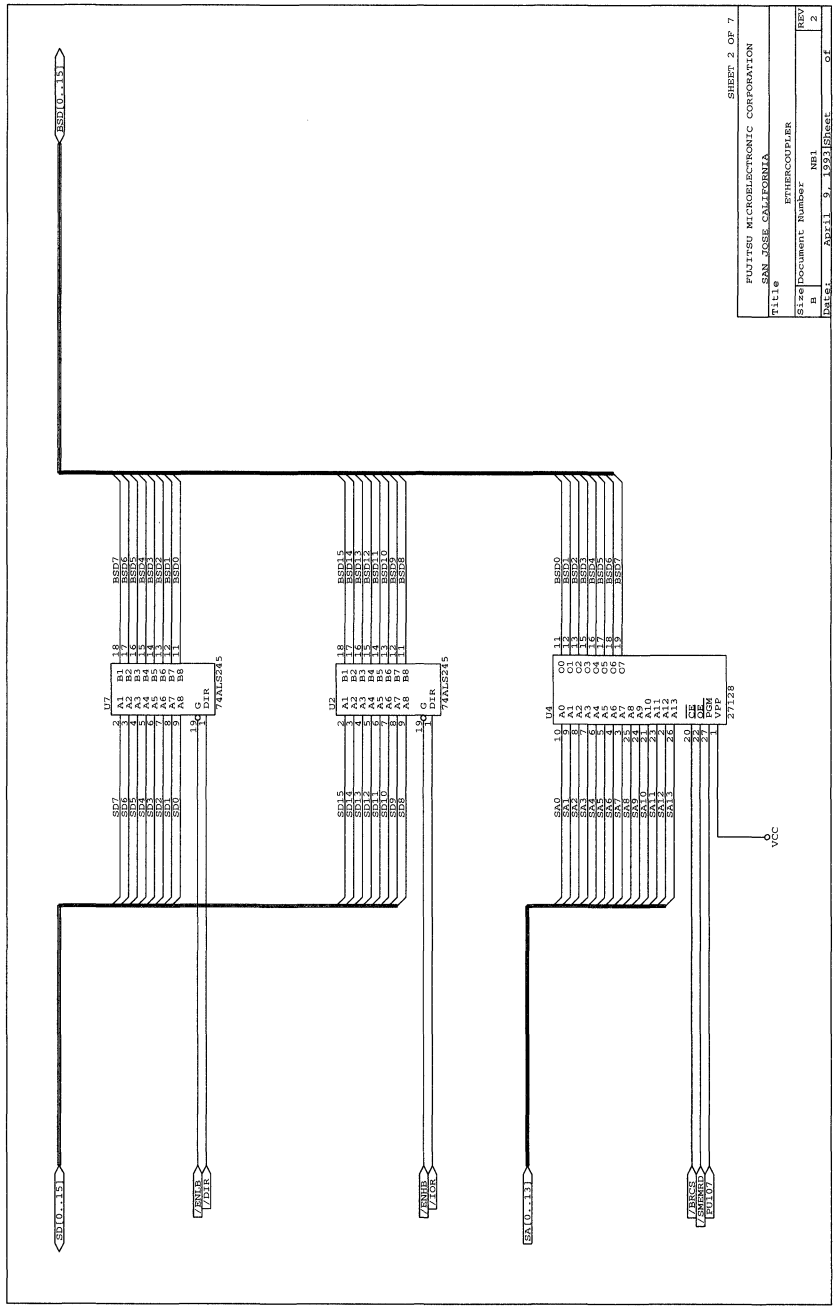


Figure 30. Boot PROM and Bus Transceivers

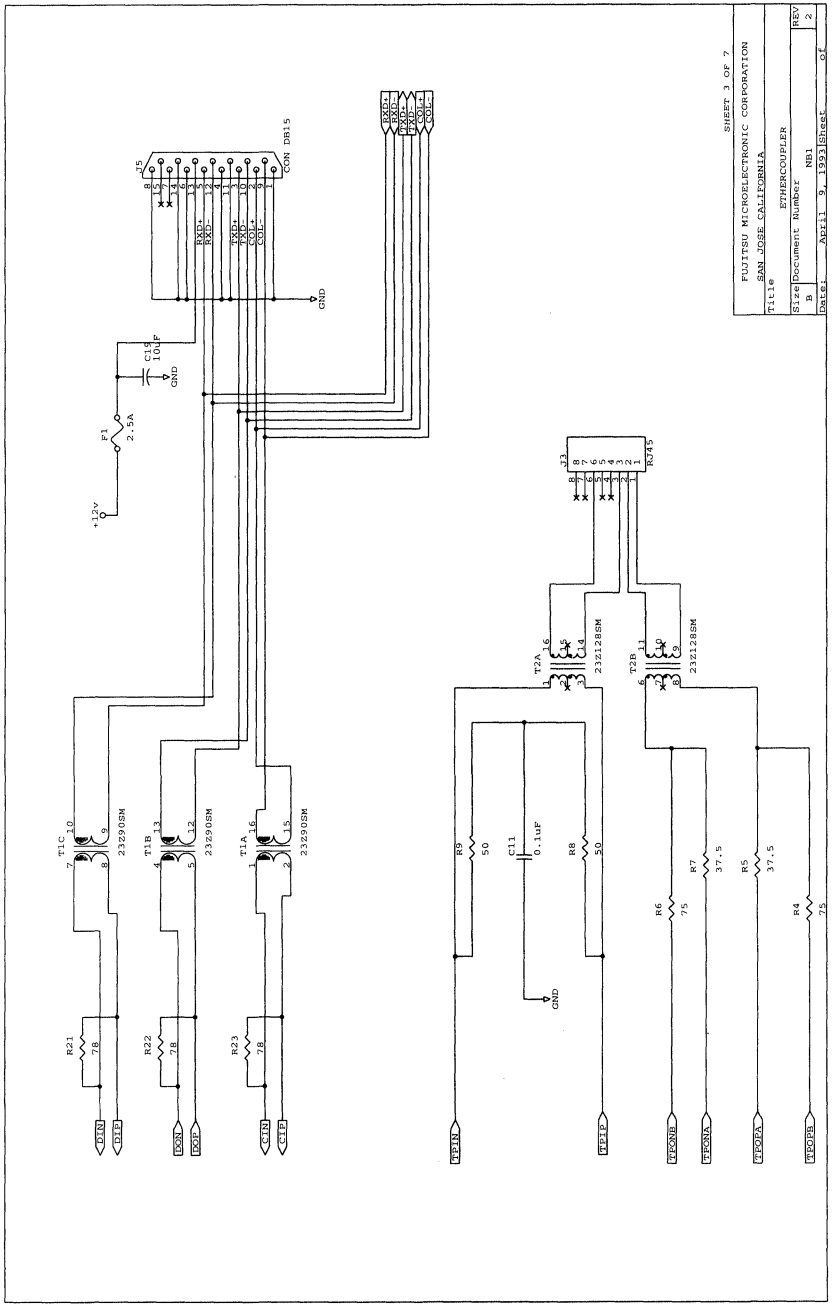


Figure 31. Transformers

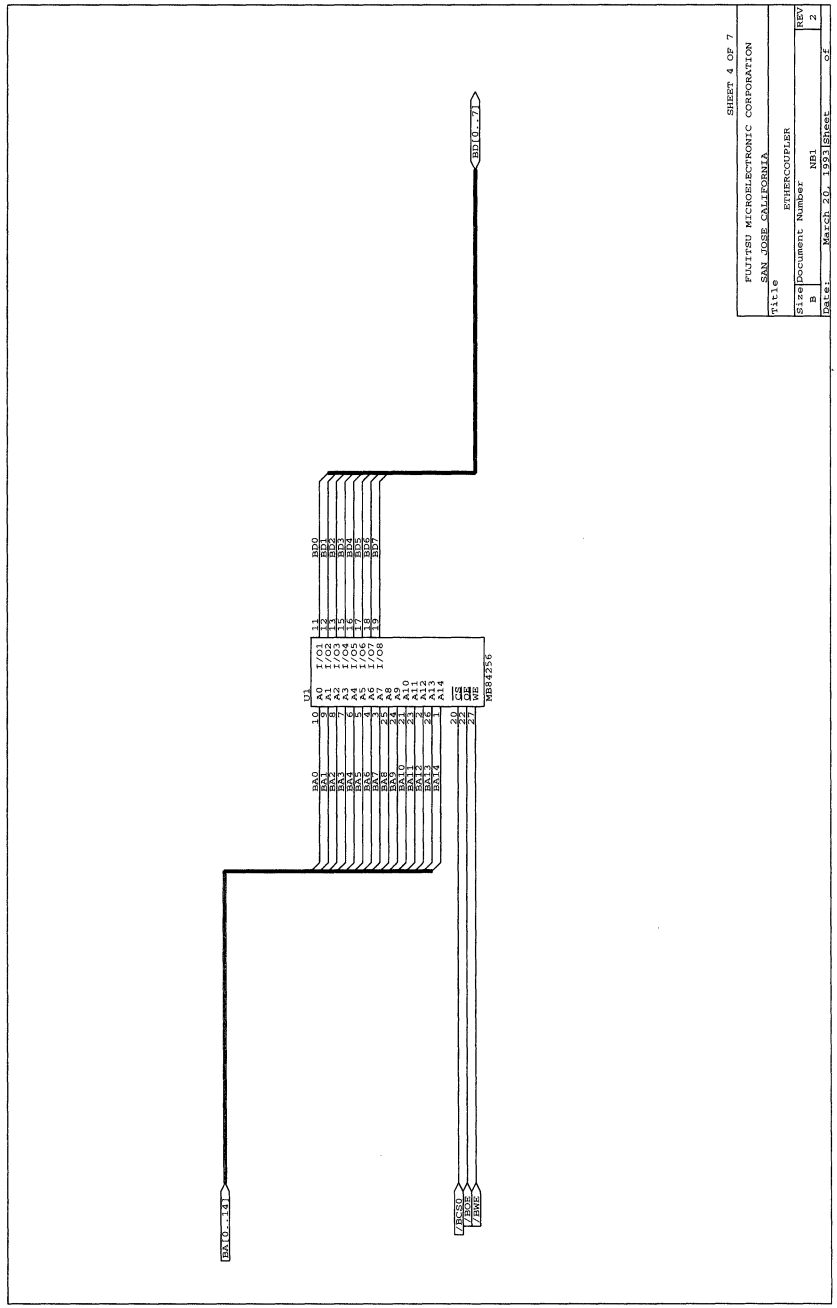


Figure 32. SRAM

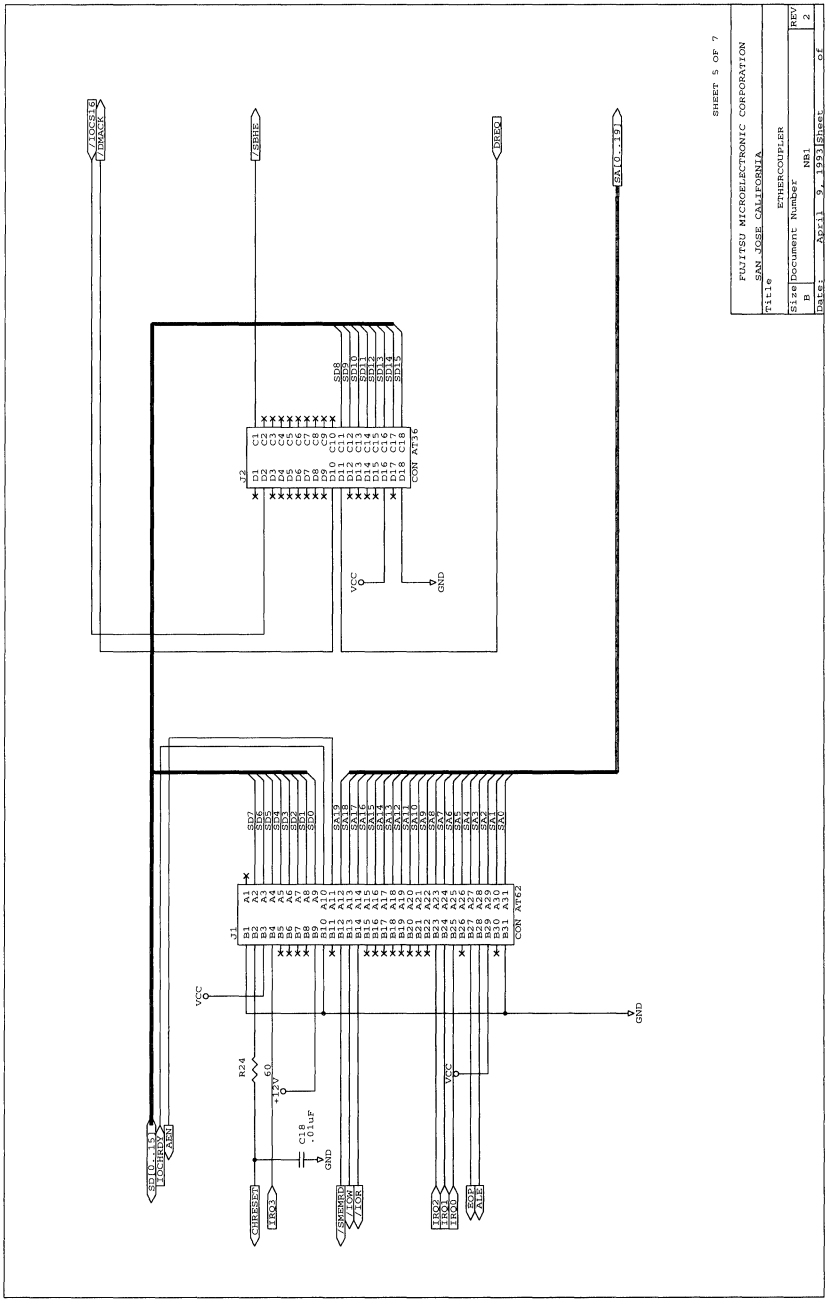


Figure 33. Connectors

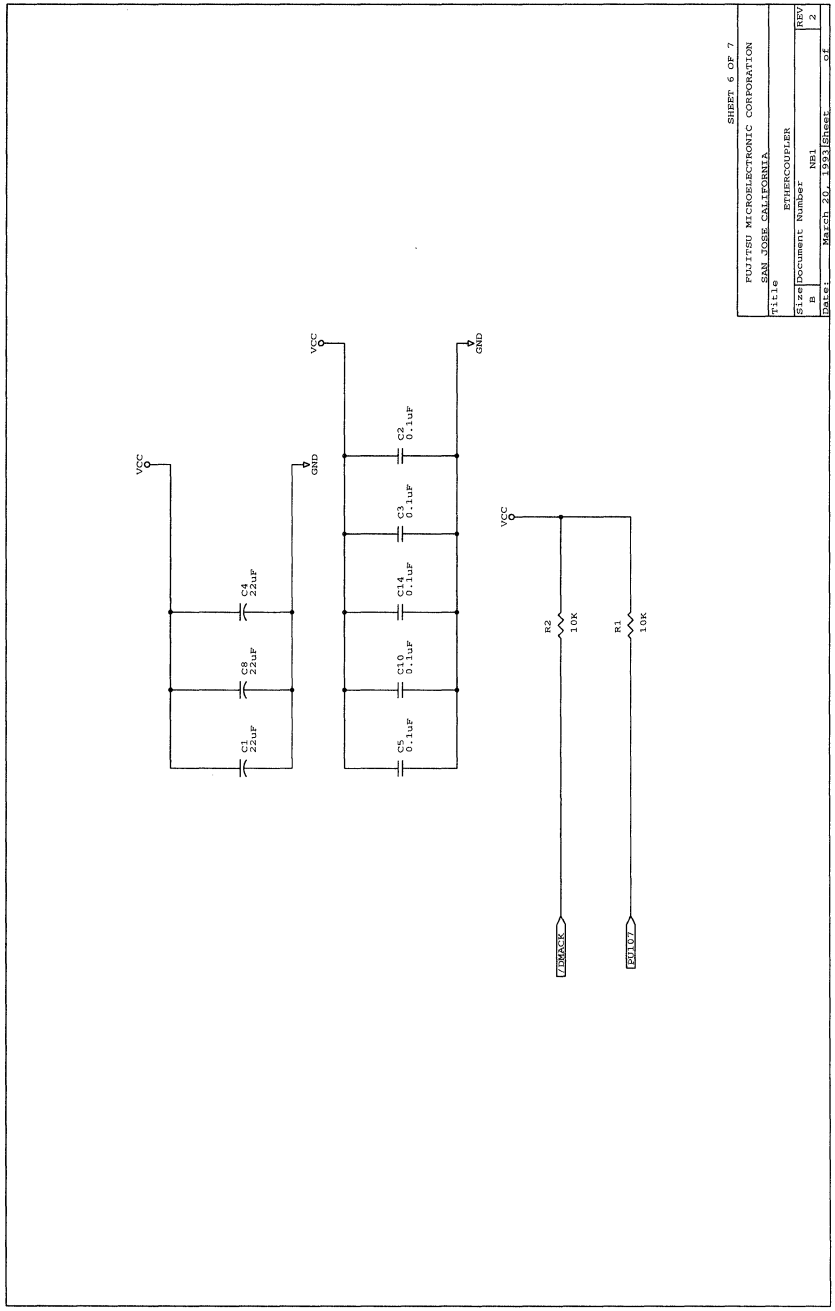


Figure 34. Capacitance

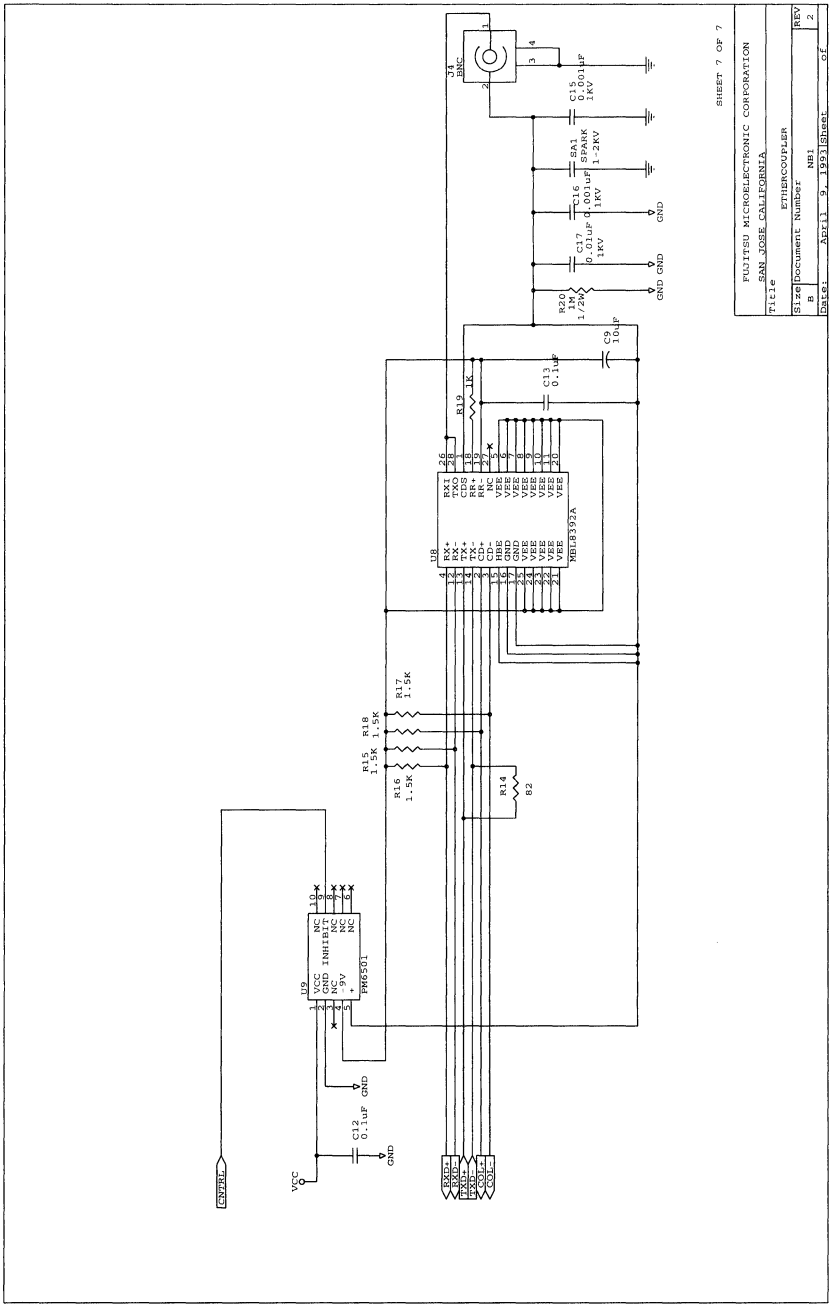
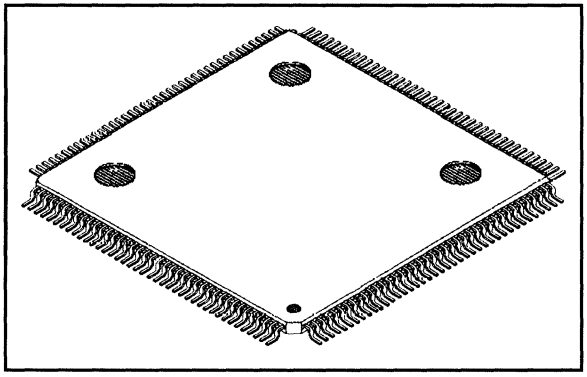
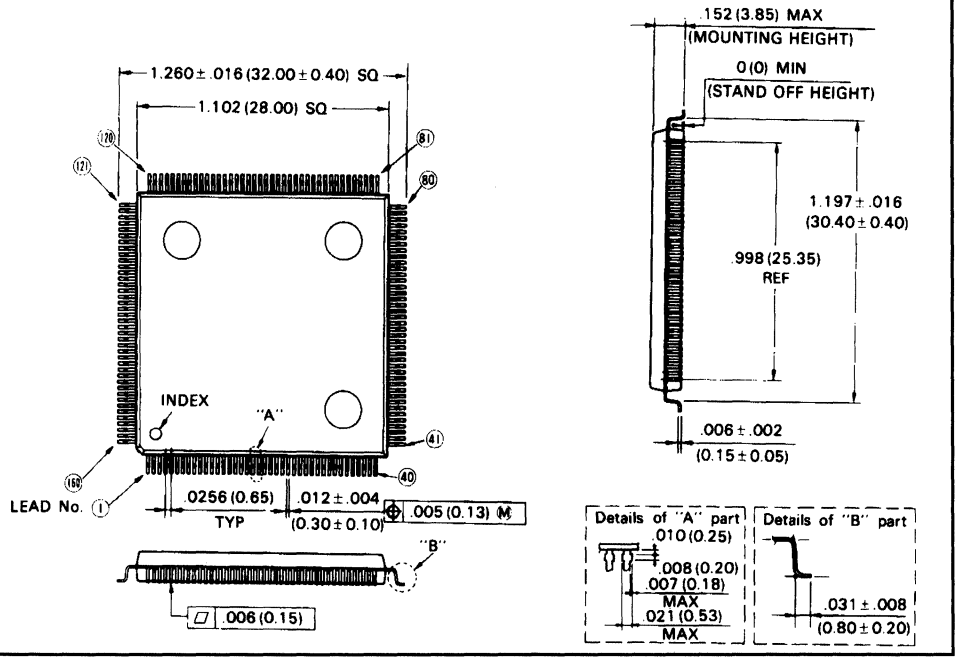


Figure 34. DC/DC Converter and 10BASE2 Transceiver

ORDERING INFORMATION



160-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-160P-M03)



Dimensions in inches (millimeters)

MB86970

FUJITSU

INTELLIGENT CONTROLLER FOR ETHERNET WITH 10BASE-T

APRIL1993

FEATURES

Host Interface Features

- LANCE-compatible architecture and buffer management structure with enhancements to ease programming, improve performance, and enhance flexibility
- Selectable 32-bit EISA or 486-compatible bus modes
- Non-multiplexed 32-bit address and data buses
- Operation as 32-bit bus master or 16/32-bit bus slave
- Supports bus preemption with preemption time programmable up to 64 bus clocks
- Page-boundry detection in bus master mode for page accesses to DRAM
- Generates chip select and read signals to access external ID PROM and boot PROM
- Direct and indirect (LANCE-compatible) addressing of all internal registers
- Initialization via direct access to initialization register set, or via initialization block in shared memory
- 33 Mbyte/sec data throughput in EISA mode and 80 Mbyte/sec data throughput in 486 mode

Ethernet Controller Features

- Transmit and receive descriptor rings each support up to 512 entries
- Enhanced transmit buffer descriptor includes collision count, enable/disable CRC and carrier sense status
- Enhanced receive buffer descriptor identifies packet as Broadcast, Multicast, Runt or Loopback type
- 128-byte FIFO auto-configured for most efficient use during transmit and receive operations
- Programmable transmit and receive FIFO threshold and burst size
- Four 16-bit counters with programmable interrupt level to allow automatic gathering of statistics on any of 15 events
- 32-bit programmable timer with interrupt
- Hash filter for multicast packet reception

Media Interface Features

- Direct interface to AUI and 10BASE-T outputs
- Fully compliant with IEEE 802.3 specifications
- Automatic AUI /10BASE-T selection
- Integrated pulse shaper and transmit and receive filters
- Selectable 100/150 ohm termination permits operation with shielded or unshielded twisted-pair cable
- Reverse-polarity detection and correction
- On-chip jabber logic, link test and SQE test with enable/disable options
- Output drivers for LEDs to indicate receive, transmit, collision and link-test pass

General Features

- Powerdown mode reduces power dissipation
- Low-power CMOS technology
- Single 5-volt power supply
- 160-pin, plastic quad flat package

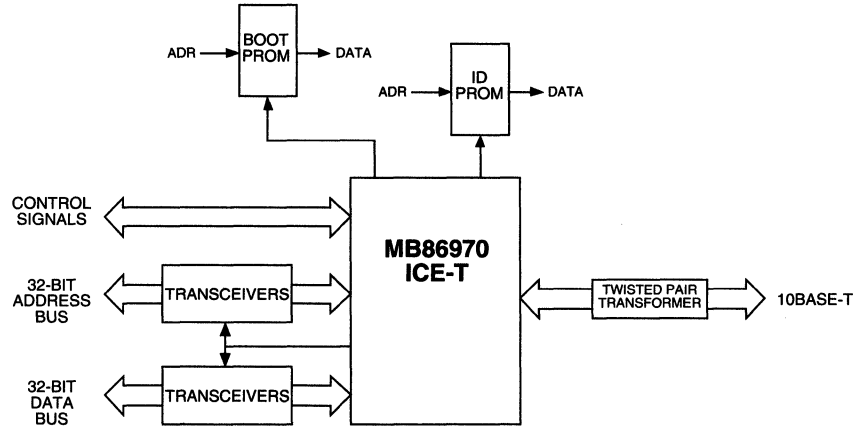
DESCRIPTION

Fujitsu's MB86970 Intelligent Controller for 10BASE-T Ethernet (ICE-T), is a single-chip, high performance, 16-/32-bit Ethernet controller for adapter card and motherboard applications. It incorporates a fully IEEE 802.3 compliant Ethernet encoder/decoder, 10BASE-T transceiver and pulse shaper and filters and features two selectable bus interface modes. In the EISA-compatible mode it provides 32-bit bus master operation with both single cycle and burst read and write capability or 16-/32-bit bus slave access to all internal registers. In its 486-compatible mode, useful for the construction of motherboards or other systems with integrated Ethernet capability, the MB86970 can operate as a 32-bit bus master or 16-/32-bit bus slave at a bus clock rate of up to 40 MHz.

The programming model for the MB86970 is based on the LANCE architecture, which allows previously developed software to be used with little or no modification. Numerous enhancements have been incorporated to ease programming, improve performance and enhance flexibility. For example, the size of the transmit and receive buffer descriptor rings are

increased to support up to 512 entries each and previously unused bits in the descriptors have been defined to provide additional status information. All registers within the MB86970 can be accessed indirectly (LANCE-compatible) or directly, and the initialization register set can be programmed either directly or via a LANCE-compatible initialization block in shared memory. Additional features in the ICE-T include a programmable 32-bit timer, counters which can be used to automatically gather statistics on any four of fifteen events such as collisions, various types of errors and received packets, packet TYPE filter to accept or reject packets based on the contents of the TYPE field, edge or level triggered interrupt outputs and generation of chip select and read strobes for external ID and boot PROMs. These features reduce the software overhead required to control internal operations, and also result in superior data throughput and application performance.

Twisted pair pulse shaping and filtering functions are performed by the MB86970 to eliminate the need for additional external components and thus reduce overall system cost. The device also provides outputs for receive, transmit, collision and link test LEDs and provides compatibility with both shielded and unshielded twisted pair cables, as well as an AUI output to allow interfacing to 10BASE5 and 10BASE2 coaxial networks with an external transceiver. Its wide range of features and its interface flexibility make the MB86970 the ideal device for constructing high-performance Ethernet adaptors.



EISA Adapter Using the MB86970 Controller, Block Diagram

MB86951

CMOS ETHERNET ENCODER/DECODER

FUJITSU

DATA SHEET

APRIL1993

FEATURES

- 10 Mbit/sec Manchester encoder/decoder
- Compatible with IEEE 802.3 10BASE2, 10BASE5 and 10BASE-T specifications
- Receiver clock recovery with dual phase locked loop for high stability
- Decodes Manchester data with up to ±20 ns of jitter.
- Loopback capability for diagnostics
- TTL compatible host interface
- Interfaces directly to the AUI (transceiver) cable
- High speed CMOS technology with a single 5 V supply
- Low power consumption, typically 16 mA
- Power Down Mode: I_{CC} = 5 mA typ
- Available in 24-pin plastic DIP and SOP packages

GENERAL DESCRIPTION

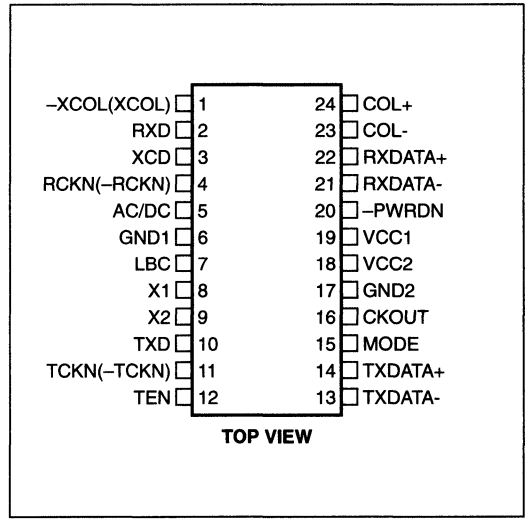
The MB86951 is a 10 Mbit/sec Manchester encoder/decoder that is designed to meet the requirements for Ethernet local area networks. This device, when used with companion chips such as Fujitsu's MB86950 EtherStar™ Controller and either the MBL8392A Coaxial Transceiver or the MB86962 Twisted Pair Transceiver (see Figure 1), forms a complete chip set that meets the requirements of the ISO/ANSI/IEEE 8802-3 international standard for Ethernet, Thin Net, and 10BASE-T networks.

The encoder/decoder interfaces with the network controller on the system side and with the transceiver on the network side. It contains a receiver with phase locked loop, a driver, a collision signaling detector, and an oscillator.

During transmit operation, the MB86951 receives NRZ (non-return-to-zero) data from the controller and converts the serial binary data stream into a Manchester encoded stream which is transmitted out on a balanced differential pair to the transceiver. During receive operation it converts Manchester encoded data on a balanced differential pair from the transceiver into NRZ data and forwards it to the controller, together with a 10 MHz synchronous receive data clock. A phase locked loop is used for clock recovery to allow a worst case jitter of ±20 ns.

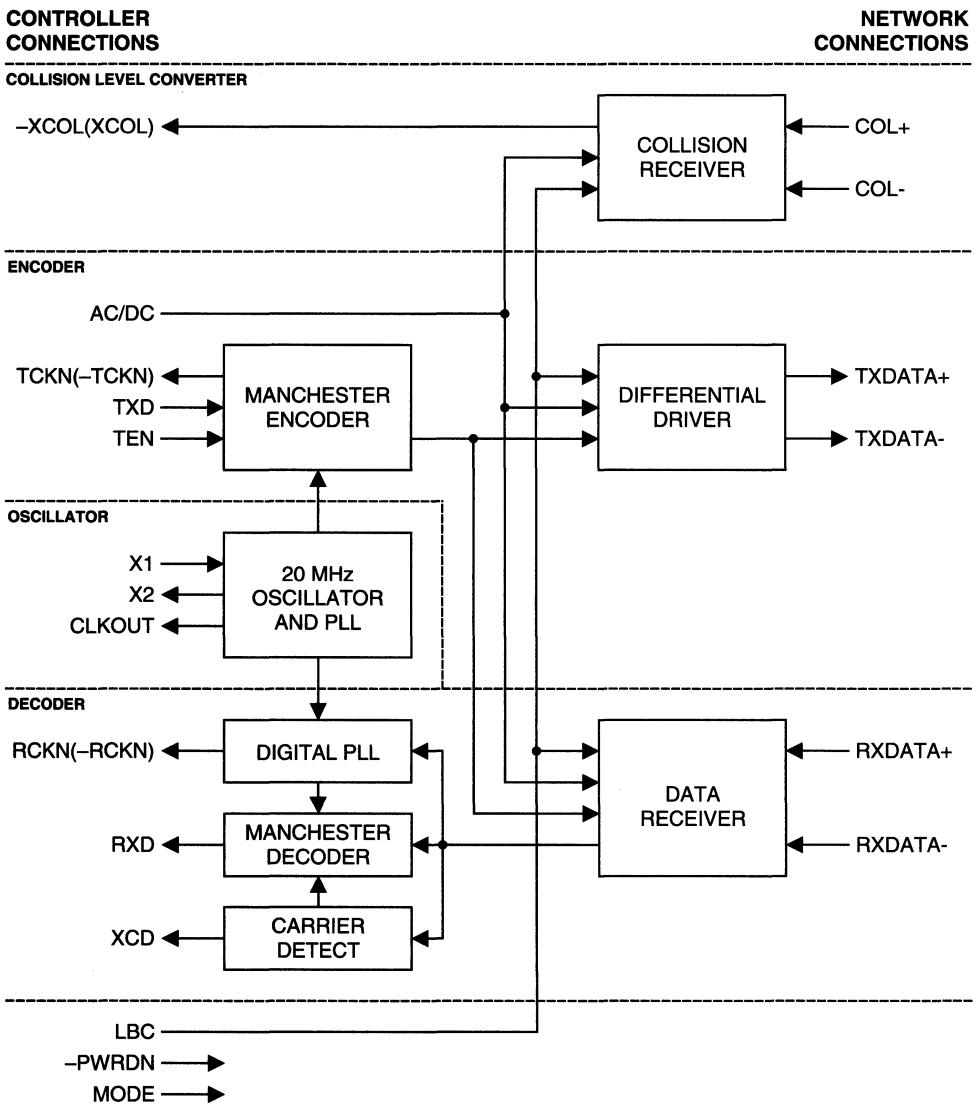
The MB86951 is fabricated using Fujitsu's high speed, low power, CMOS technology and is supplied in 24-pin plastic DIP and small outline (SOP) packages.

PIN CONFIGURATION



TOP VIEW

BLOCK DIAGRAM



ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5 V ± 5%, T_A = 0 to +70°C
24-Pin Plastic Dual In-line	DIP-24P-M03	MB86951P-G
24-Pin Plastic Small Outline	FPT-24P-M02	MB86951PF-G

SIGNAL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
–XCOL(XCOL)	O	**COLLISION PRESENCE:** This output indicates that the collision inputs to the MB86951 (COL±) are active, signifying that the transceiver has detected a collision on the media. If MODE = 0, –XCOL(XCOL) is a normally low output which changes to a high state during collision detection. If MODE = 1, –XCOL(XCOL) is a normally high output which changes to a 10 MHz pulse stream during collision detection. See also Mode Control section.
RXD	O	**RECEIVED SERIAL DATA:** Output NRZ serial bit stream from the Manchester decoder. Changes in the state of RXD are synchronous with the rising edge of RCKN if MODE = 0, and synchronous with the falling edge of RCKN if MODE = 1.
XCD	O	**RECEIVED CARRIER DETECT**: Assertion of this active high output indicates that a carrier has been detected at the RXDATA± inputs.
RCKN(–RCKN)	O	**RECEIVED DATA CLOCK:** The data clock recovered by the DPLL within the MB86951 while data is being received. RCKN(–RCKN) is a free running 10 MHz clock when the receive inputs are idle. See also Mode Control and Data Decoder sections.
AC/DC	I	**AC/DC COUPLING SELECT:** AC/DC = 0 selects DC coupling, AC/DC = 1 selects AC coupling for the TXDATA outputs. When AC coupling is selected, both TXDATA+ and TXDATA– are driven to the same output voltage level during transmit idle periods to prevent saturation of the isolation transformer.
LBC	I	**LOOPBACK CONTROL:** When this input is asserted (high) the MB86951 is placed in the loopback mode.
X1	I	**CRYSTAL INPUT:** Connection for one side of the 20 MHz crystal or input for an external 20 MHz clock.
X2	O	**CRYSTAL OUTPUT:** Connection for the other side of the 20 MHz crystal. Leave unconnected if an external clock is used.
TXD	I	**TRANSMIT SERIAL DATA INPUT:** NRZ serial data stream which is fed to the Manchester encoder. Changes in TXD should be synchronized to the rising edge of TCKN(–TCKN) if MODE = 0 and to the falling edge of TCKN(–TCKN) if MODE = 1.
TCKN(–TCKN)	O	**TRANSMIT DATA CLOCK:** 10 MHz clock output used by the controller to synchronize the TXD input to the MB86951. See also Mode Control and Data Encoder sections.
TEN	I	**TRANSMIT ENABLE:** When asserted (high) TEN enables encoding of the transmitted data.
TXDATA+ TXDATA-	O	**TRANSMIT DATA:** These are the Manchester encoded differential outputs to the transceiver. They require 270Ω pulldown resistors and are capable of driving a 78Ω differential transmission line.
MODE	I	**MODE:** MODE = 1 selects the normal (Fujitsu-controller compatible) mode. When MODE = 0, the part is functionally and electrically compatible with the National DP83910 and AMD Am7992B. See also Mode Control section.
CKOUT	O	**CLOCK OUTPUT:** 20 MHz free running clock output.

Signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

SIGNAL DESCRIPTIONS (continued)

SYMBOL	TYPE	DESCRIPTION
–PWRDN	I	**POWER DOWN:** Active low input for selecting power down mode. Note: LBC (pin 7) must be 0 during power down, otherwise the device will enter a test mode used by the factory. Tie –PWRDN high for normal operation.
RXDATA+ RXDATA-	I	**RECEIVED DATA:** These are the Manchester encoded differential inputs to the MB86951 from the transceiver.
COL+ COL-	I	**COLLISION:** These differential inputs are driven with a 10 MHz signal when the transceiver detects a collision on the medium.
V_{CC}		**POWER SUPPLY:** A nominal +5 V_{DC} supply is required.
GND		**GROUND**

Signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names with the second enclosed in parentheses ( ).

FUNCTIONAL DESCRIPTION

The block diagram highlights the major functional blocks of the MB86951: oscillator, data encoder, data decoder, collision signal detector, and loopback control. Figure 1 illustrates a typical interface for the device when driving an AUI (transceiver) cable on the network side and connected to Fujitsu's MB86950 EtherStar controller on the system side.

OSCILLATOR

The IEEE 802.3 standard specifies a clock rate of 10 Mbits/sec. This is obtained from a 20 MHz clock generated by the oscillator, which operates from an external crystal reference connected between pins X1 and X2 of the MB86951. Crystal capacitance as specified by the manufacturer should be connected from X1 and X2 to ground, considering any stray capacitance which can vary the crystal's frequency. If an external 20 MHz clock is available, it may be applied to X1 with X2 left unconnected.

The 20 MHz oscillator output is provided on CKOUT for external use. It is also divided by two to produce the required 10 MHz clock, which is used internally and furnished on TCKN(–TCKN) for use by the network controller. The 20 MHz clock also serves as a reference for an internal phase locked loop used for clock and data recovery in the decoder section.

DATA ENCODER

Manchester encoding is used for the transmission of data from the MB86951. Manchester encoding is a binary signaling mechanism that combines data and clock into bit symbols. Each bit symbol is split into two halves, with the signal polarity of the second half being the inverse of that of the first half. A transition always occurs in the middle of each bit symbol, with logic '0' and '1' encoded as 1-to-0 and 0-to-1 transitions respectively. See Figure 2. In the case of the

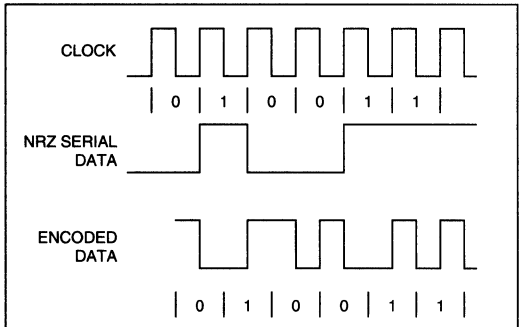


Figure 2. Manchester Encoding

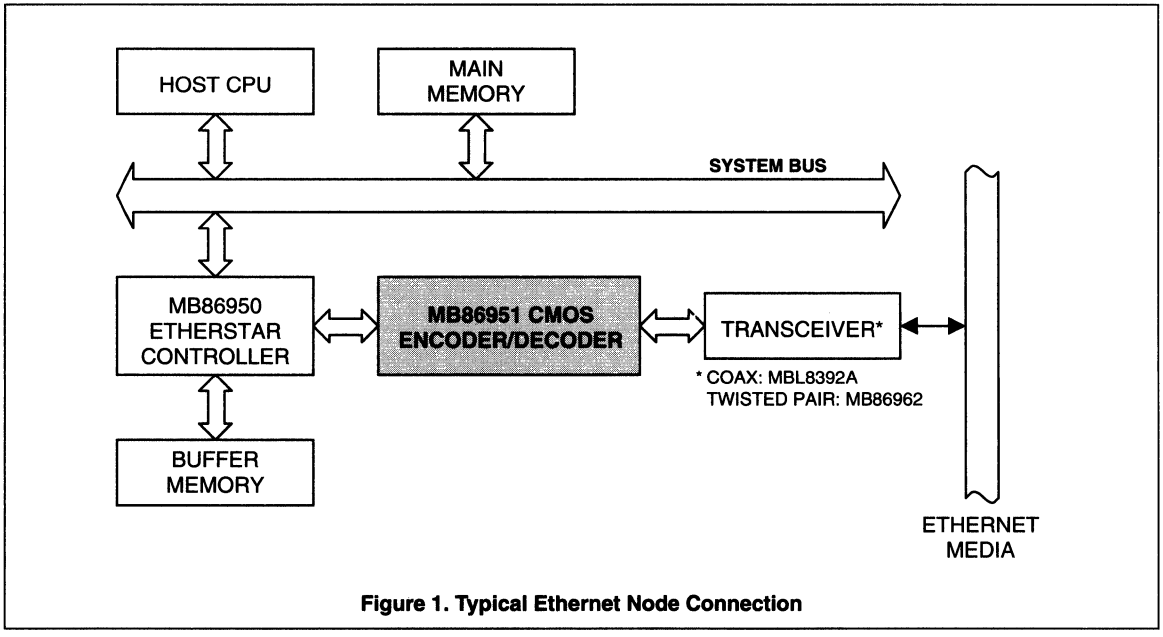


Figure 1. Typical Ethernet Node Connection

MB86951, the controller asserts transmit enable (TEN) to indicate that the outgoing packet on TXD is valid data. This NRZ serial data input must be supplied synchronously with the TCKN(–TCKN) clock as required by the setting of MODE. If MODE=1, TXD is valid during the rising edge of TCKN(–TCKN); if MODE=0, TXD is valid during the falling edge. The Manchester-encoded signals are output through a differential driver to the transceiver through TXDATA+ and TXDATA-, and are present as long as the TEN pin remains affirmed.

The differential driver is capable of driving a 50 meter segment of 78Ω interface cable, as specified in the ISO/ANSI/IEEE 8802-3 standard. 270Ω resistors are required externally to pull down TXDATA+ and TXDATA-. See Figure 3.

DATA DECODER

The data decoder section performs three functions on the data received at the differential receive inputs (RXDATA+ and RXDATA-) from the transceiver: carrier detection, clock recovery, and Manchester data decoding.

Clock recovery is accomplished by use of phase locked loop circuitry which uses the crystal oscillator as a reference. Use of a PLL provides the most reliable and robust clock recovery. It allows signal acquisition to be accomplished within six bit times from first detection of the signal, and permits stable operation with input signal jitter of up to ±20 ns. Carrier detection is indicated to the controller by affirmation of the XCD output, which occurs shortly after a signal appears at the differential inputs.

The recovered clock is supplied to the controller on RCKN(–RCKN), and is also used to convert the Manchester encoded data to NRZ format, which is then output on RXD. The phase relationship between RCKN(–RCKN) and RXD is controlled by the MODE input. Transitions in the state of RXD are synchronous with the rising edge of RCKN(–RCKN) if

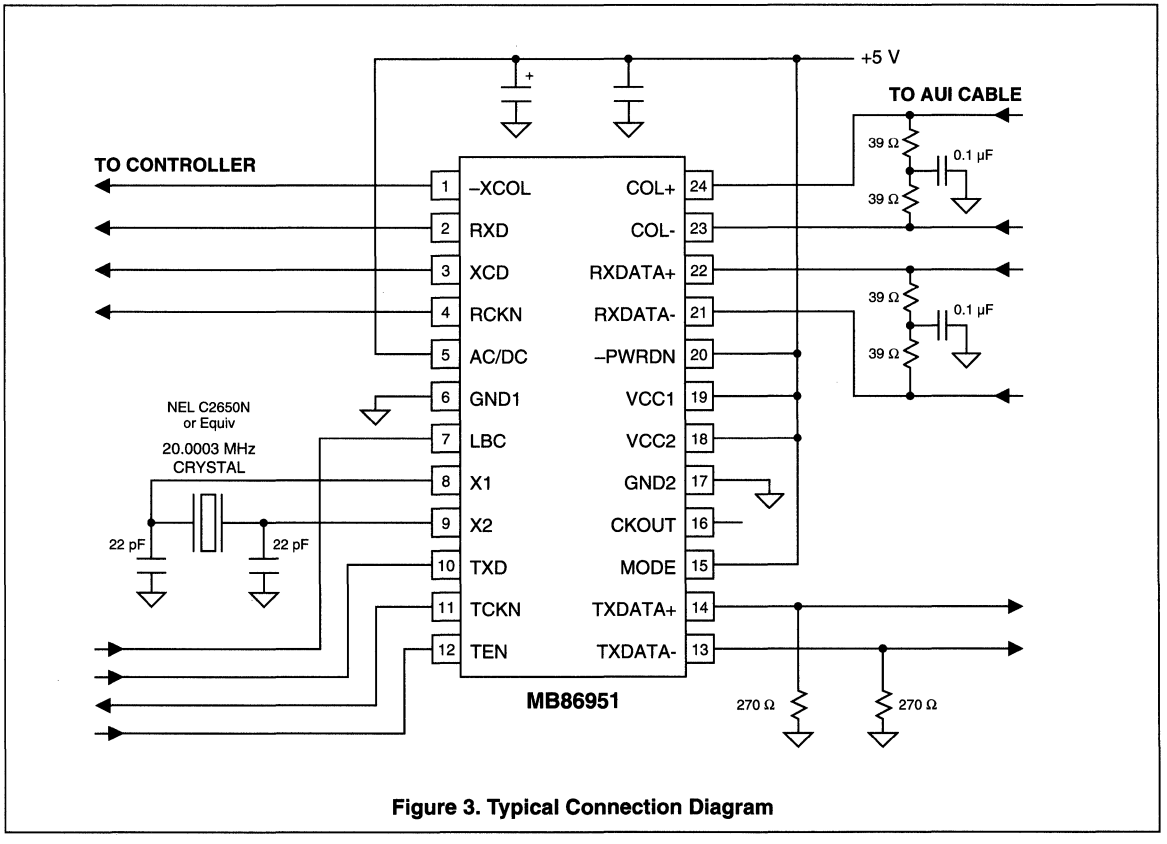


Figure 3. Typical Connection Diagram

MODE = 0, and synchronous with the falling edge of RCKN(–RCKN) if MODE = 1. RCKN(–RCKN) is a free running 10 MHz clock when no receive signal is present.

The RXDATA+ and RXDATA- differential inputs must be terminated with two 39Ω resistors in series with a 0.1 µF bypass capacitor at their junction, as illustrated in Figure 2.

COLLISION SIGNALING DETECTOR

As collisions are detected on the network media, the transceiver generates a 10 MHz signal on the COL+ and COL- differential inputs to the MB86951. This signal is detected by the MB86951, converted to a logic-level signal appropriate for the controller and output on –XCOL(XCOL). If MODE = 0, –XCOL(XCOL) is normally low and changes to a high state during collision detection. If MODE = 1, –XCOL(XCOL) is normally high and changes to a 10 MHz pulse stream during collision detection.

The COL+ and COL- differential inputs require 78Ω termination like that for the RXDATA+ and RXDATA- inputs. See Figure 2.

LOOPBACK

The loopback control input (LBC) causes transmitted data from the controller to be routed through the internal circuits of the MB86951 and back to the received data output to test for proper system operation. While LBC is affirmed, the encoded transmit data is supplied to the data decoder instead of the receive data from the RXDATA+ and RXDATA- inputs. Also, the differential transmit drivers and the collision signal detector are disabled. Note that changes in LBC while data is being received may cause errors in the received data output.

MODE CONTROL

The MODE input selects one of two modes of operation for the MB86951. The setting of this input changes the phase relationship between certain clocks and signals, and the format of the –XCOL(XCOL) output. The three signal pins which are affected are –XCOL(XCOL), RCKN(–RCKN) and TCKN(–TCKN). MODE =1 selects the normal mode in which these signals are compatible with Fujitsu controllers such as the MB86950. When MODE = 0 the MB86951 is functionally and electrically compatible with the National DP83910 and the AMD Am7992. Polarity of the three signal pins shown in their names in parentheses corresponds to MODE = 0. See the Pin Descriptions section and the timing diagrams at the end of this data sheet for additional information.

POWER DOWN

The power down mode is selected by driving both –PWRDN (pin 20), and LBC (pin 7) low. In this mode, power consumption is reduced to 6 mA typical.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1,2,3]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.5	6.0	V
V_{ITL}	TTL level input voltage		-0.5	V_{CC} + 0.5	V
I_{ODF}	Differential output current			-40	mA
T_{STG}	Storage temperature		-40	125	°C
T_{OP}	Operating temperature		-25	85	°C
V_{DCI}	RxDATA± / COL± DC input voltage		0.5	16	V
V_{DCO}	TxDATA± / COL± DC output voltage	with transformer without transformer	-0.5 -0.5	16 10	V V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Operating ambient temperature	0 to +70	°C
V_{CC}	Supply voltage	5.0 ± 5%	V
I_{OH}	Maximum TTL high level output current	-2.0	mA
I_{OL}	Maximum TTL low level output current	3.2	mA
R_L	Driver load resistor (see Figure 4)	270	Ω
R_T	Differential termination resistor (see Figure 4)	78	Ω
C_{OSC}	Oscillator capacitors[5]	22	pF
f_{XTAL}	Oscillator crystal frequency	20.000 ± 0.005%	MHz

DC SPECIFICATIONS[3,4] (Recommended Operating Conditions Unless Otherwise Indicated)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Operating power supply current	no output load	-	30	60	mA
I_{CCPD}	Power down supply current	no output load –PWRDN=0, LBC=0	-	6	10	mA
V_{IH}	TTL high level voltage		2.2	-	V_{CC}	V
V_{IL}	TTL low level input voltage		0	-	0.8	V
V_{OH}	TTL high level output voltage	I_{OH} = -2.0 mA	4.2	-	V_{CC}	V
V_{OL}	TTL low level output voltage	I_{OL} = 3.2 mA	0	-	0.4	V
I_{LI}	TTL input leakage current	V_{IN} = 0 or V_{CC}	-10	-	10	µA
V_{OP}	TxDATA± peak output voltage	R_L = 270Ω	±0.5	-	1.3	V
V_{OB}	TxDATA± output voltage imbalance	R_T = 78Ω	-	-	40	mV
V_{CMO}	TxDATA± DC common mode output		2.4	3.4	4.4	V
V_{IT1}, V_{IT2}	RxDATA± squelch threshold	AC/DC=0 AC/DC=1	-80 -300	0 -220	80 -140	mV

DC SPECIFICATIONS[3,4] (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IP}	RxDATA ± peak input voltage		0.3	-	1.5	V
V_{IB}	RxDATA ± DC input bias voltage		2.2	3.2	4.2	V
I_{IHD}	RxDATA ± input high level current	$V_{IN} = V_{CC}$	-	-	250	µA
I_{ILD}	RxDATA ± input low level current	$V_{IN} = 0$	-	-	-400	µA
V_{ITD1}	RxDATA ± input threshold	AC/DC = Low	-80	0	80	mV
V_{ITD2}		AC/DC = High[6]	-300	-220	-140	mV
I_{CCS}	Static power supply current	–PWRDN = 0, X_1=V_{CC}, dIfferential inputs open, TTL inputs = 0 or V_{CC}, no output loads	-	-	100	µA
I_{CC}	Operating power supply current	No output loads	-	25	50	mA

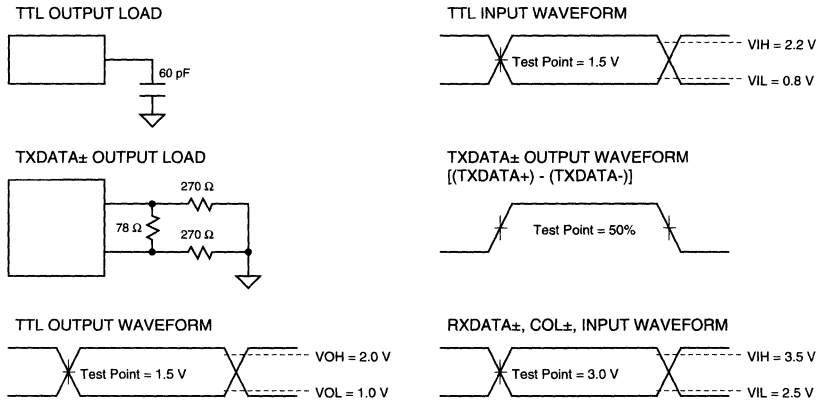


Figure 4. Test Conditions

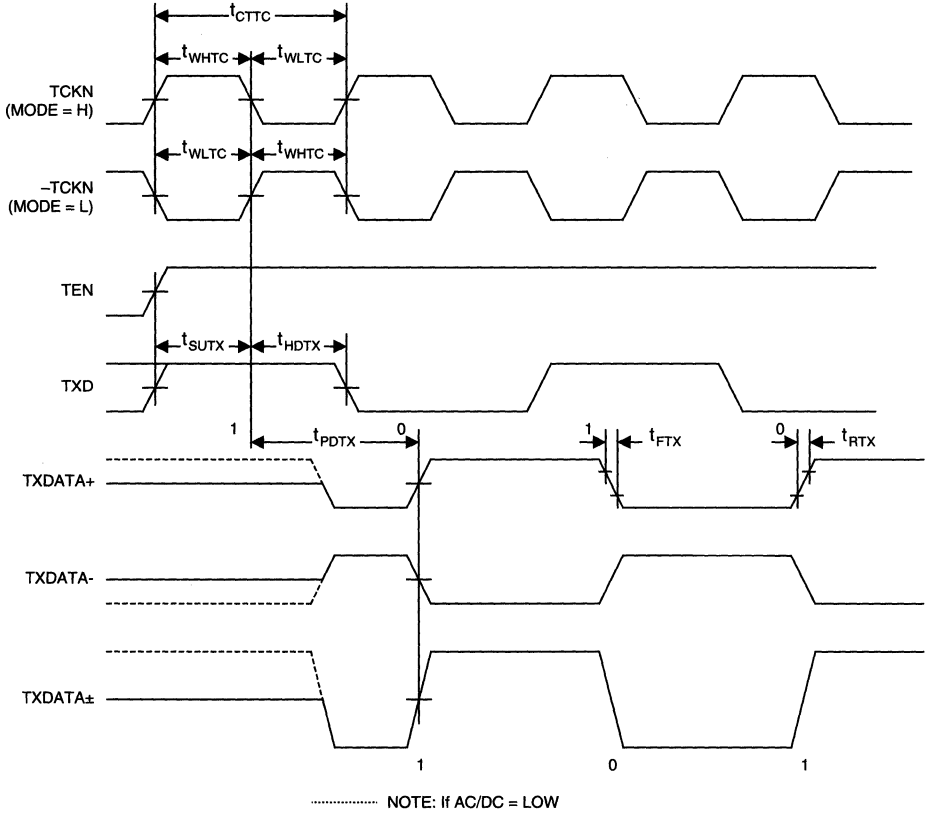


Figure 5. Transmit Start Timing

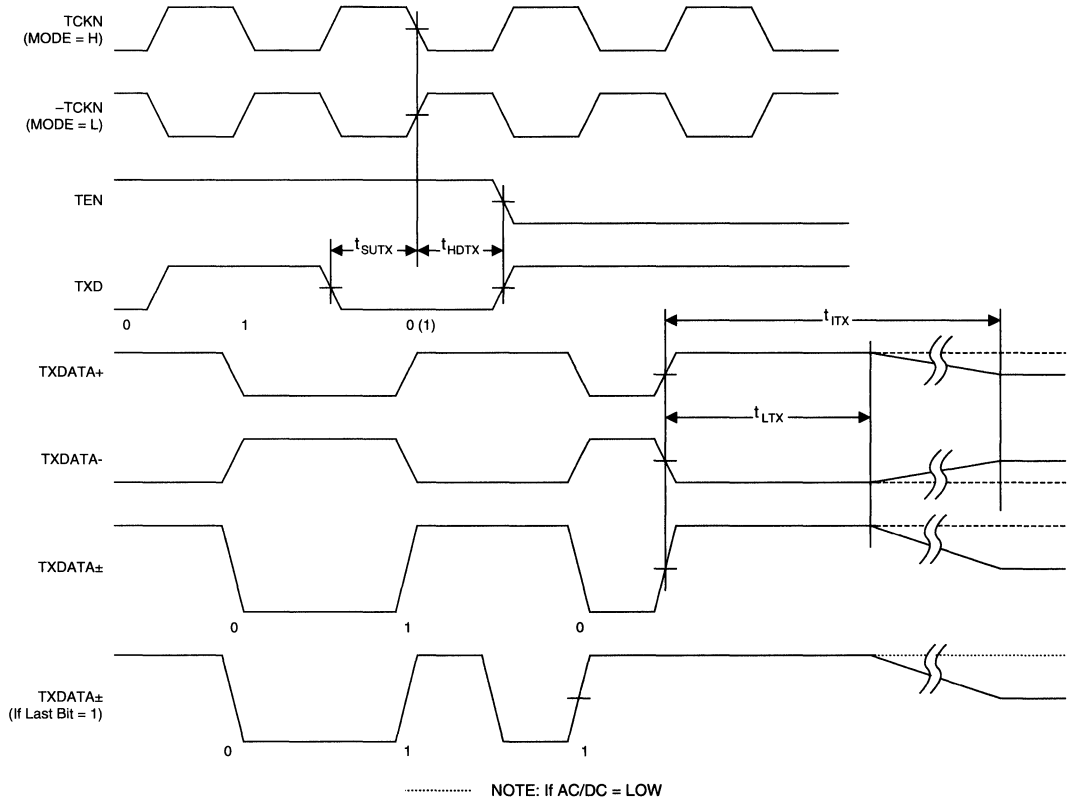


Figure 6. Transmit End Timing

AC CHARACTERISTICS[3,4] (Recommended Operating Conditions Unless Otherwise Indicated)

Transmit Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{CTTC}	5	TCKN cycle time		99.99	100	100.01	ns
t_{WLTC}	5	TCKN low time		40	50	60	ns
t_{WHTC}	5	TCKN high time		40	50	60	ns
t_{PDTX}	5	TXDATA ± encode time		-	95	-	ns
t_{RTX}	5	TXDATA ± rise time	20% to 80%	-	2	-	ns
t_{FTX}	5	TXDATA ± fall time	20% to 80%	-	2	-	ns
t_{LTX}	6	TXDATA ± level hold time	AC/DC = High	200	-	-	ns
t_{ITX}	6	TXDATA ± idling time	AC/DC = High	-	-	8000	ns
t_{SUTX}	5,6	TXD, TEN setup time to TCKN		20	-	-	ns
t_{HDTX}	5,6	TXD, TEN hold time from TCKN		10	-	-	ns

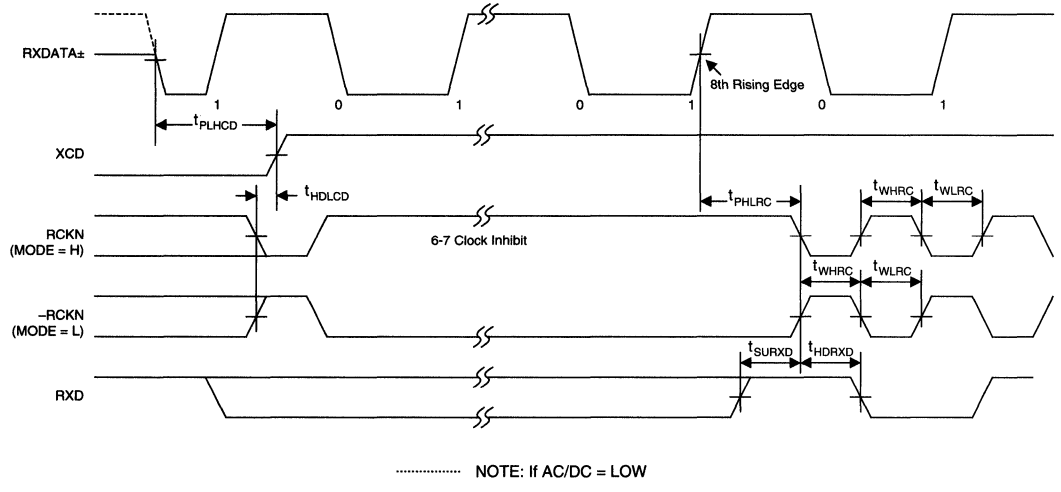


Figure 7. Receive Start Timing

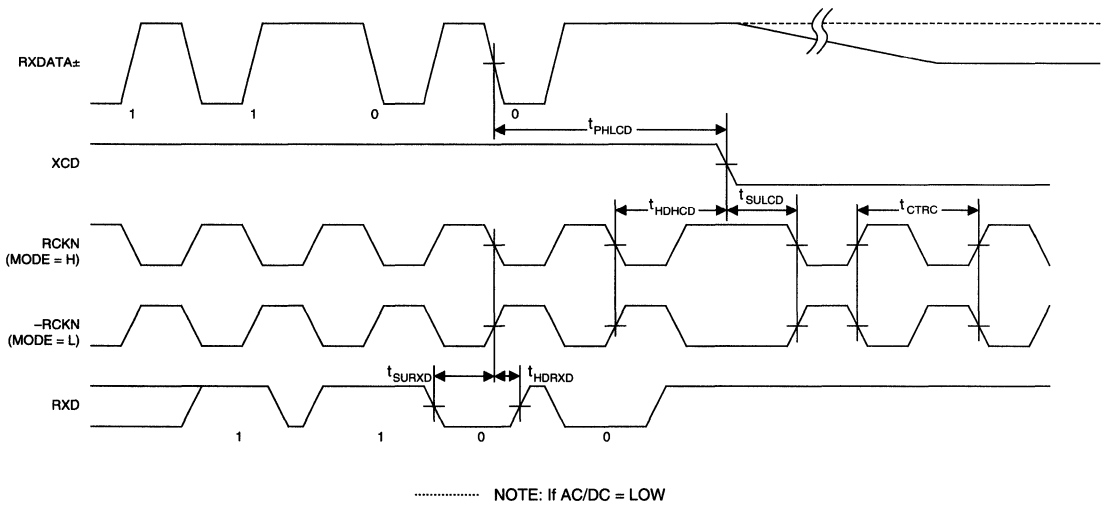


Figure 8. Receive End Timing

Receive Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{CTRC}	8	RCKN cycle time during idle		99.99	100	100.01	ns
t_{WLRC}	7	RCKN low time		35	50	-	ns
t_{WHRC}	7	RCKN high time		35	50	-	ns
t_{PHLRC}	7	RCKN delay time		-	125	-	ns
t_{PLHCD}	7	XCD on delay time		-	90	120	ns
t_{PHLCD}	8	XCD off delay time		-	260	-	ns
t_{HDLCD}	7	XCD low hold time		10	-	-	ns
t_{HDHCD}	8	XCD high hold time		-	130	-	ns
t_{SULCD}	8	XCD low setup time		-	70	-	ns
t_{SURXD}	7,8	RXD setup time to RCKN		20	60	-	ns
t_{HDRXD}	7,8	RXD hold time from RCKN		10	20	-	ns

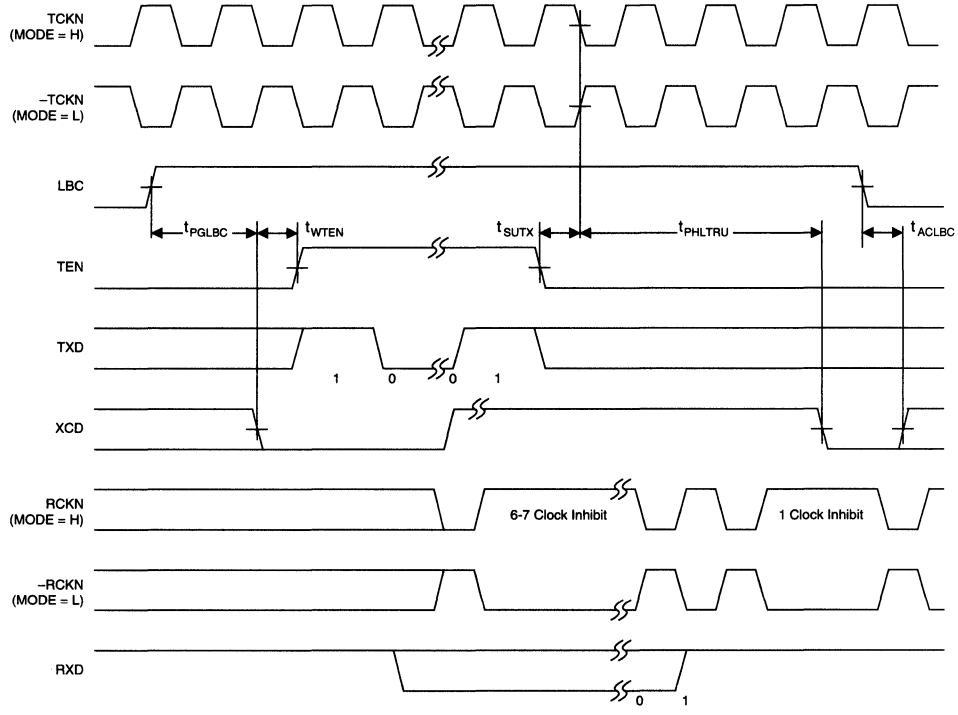


Figure 9. Loopback Timing

Loopback Timing[7]

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{PGLBC}	9	LBC receiving data purge time		-	260	-	ns
t_{ACLBC}	9	LBC receiving data accept time		-	80	-	ns
t_{PHLTRU}	9	Data through time		-	280	-	ns
t_{WTEN}	9	Wait time from XCD low to TEN high		0	-	-	ns

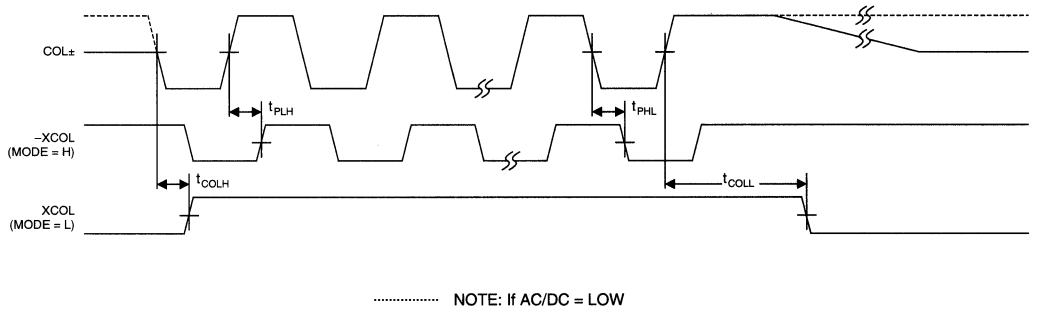


Figure 10. Collision Timing

Collision Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	10	COL± to –XCOL(XCOL) propagation delay time	MODE = High	-	15	50	ns
t_{PHL}	10		MODE = High	-	15	50	ns
t_{COLH}	10		MODE = Low	-	-	50	ns
t_{COLL}	10		MODE = Low	-	-	350	ns

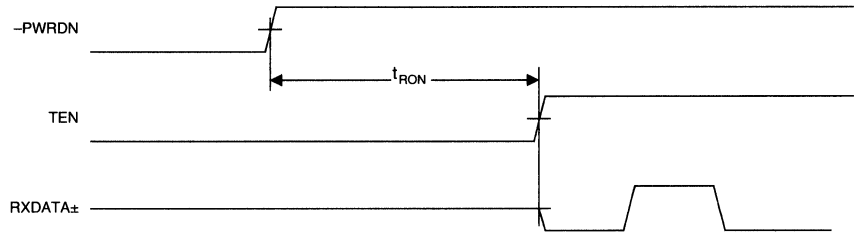


Figure 11. Reset Timing

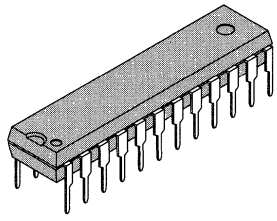
Reset Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{RON}	11	Start-up time after reset		200	-	-	µs

Notes:

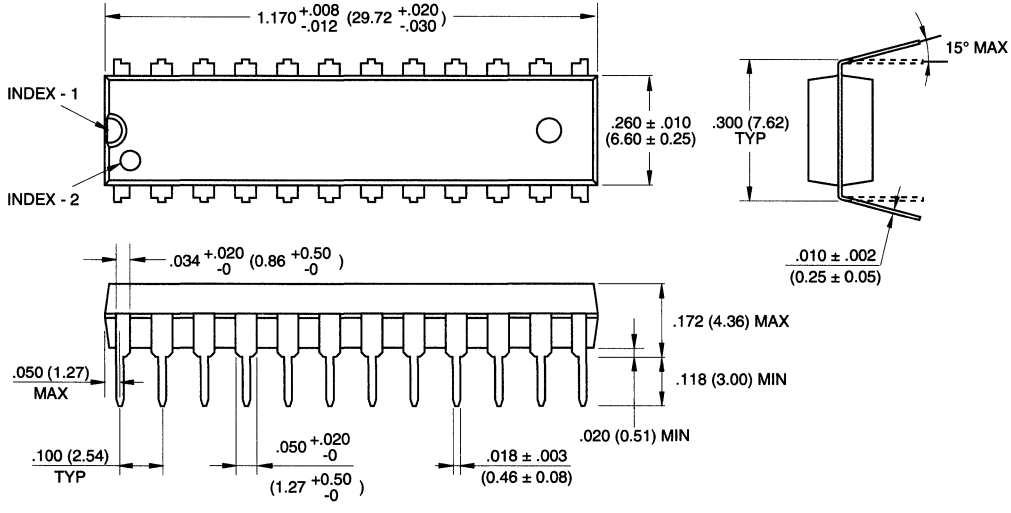
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. All voltage measurements are referenced to ground. See Figure 4 for test conditions.
4. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
5. The values of the oscillator capacitors may have to be tuned for a particular component layout. However, once the correct values are determined for that layout, tuning for each board is not required. Both capacitors should be adjusted for maximum voltage at X1.
6. The threshold of RXDATA± is changed to V_{ITD2} while AC/DC = High. (See DC Specifications for V_{ITD2}.)
7. During loopback operation, the COL± and RXDATA± inputs are ignored and the TXDATA± outputs are idle. XCD remains at a High level if MODE = Low.

24-Pin Plastic Dual In-Line Package



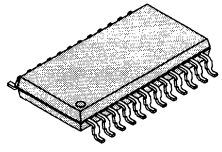
Ordering Information: MB86951P-G

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-24P-M03)



Dimensions in inches (millimeters)

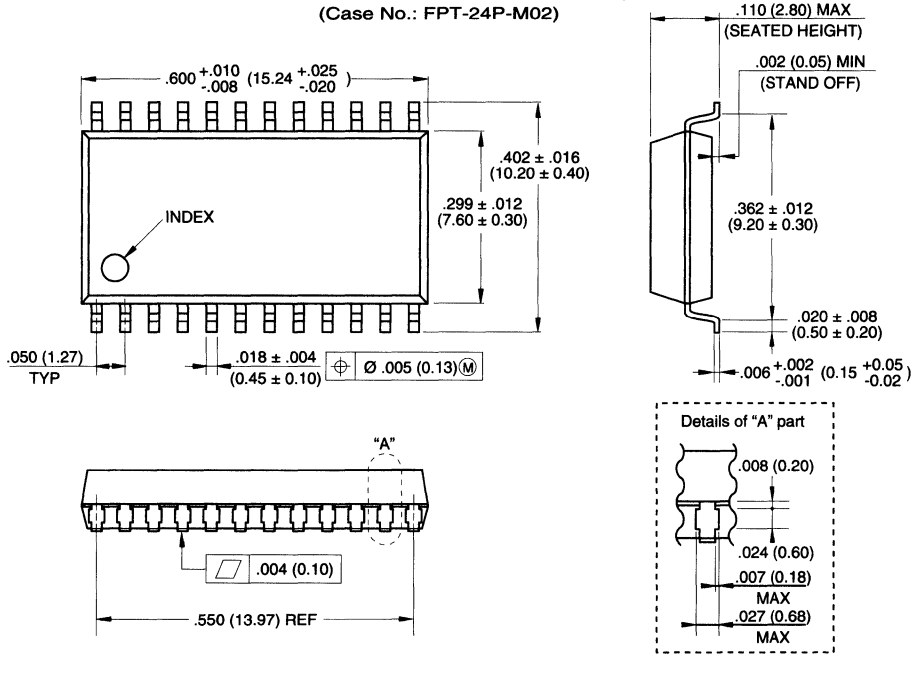
24-Pin Plastic Small Outline Package



Ordering Information: MB86951PF-G

24-LEAD PLASTIC FLAT PACKAGE

(Case No.: FPT-24P-M02)



Dimensions in inches (millimeters)

MBH10302

PCMCIA ETHERNET CARD

FUJITSU

DATA SHEET

APRIL1993

FEATURES

10 BASE-T Ethernet Interface

- 32 kilobytes Internal SRAM Buffer
- Ethernet ID and Card Descriptor in EEPROM
- Emulated Memory Map (optional)

Drivers Available

- NetWare® IPX/ODI
- Other Drivers in Development

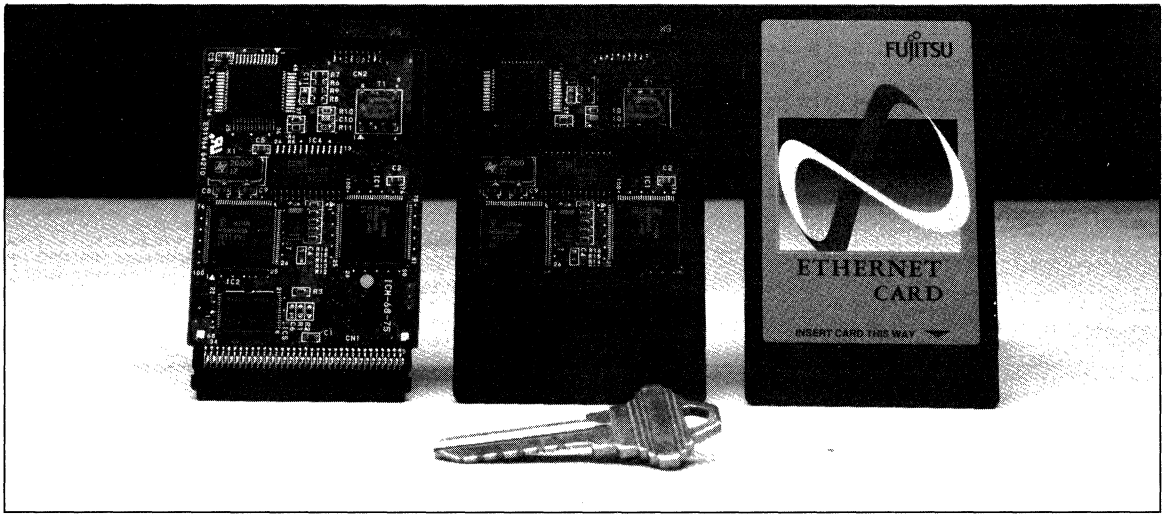
Miscellaneous

- 8- or 16-bit System Host
- Powerdown Mode
- Complies with PCMCIA 2.0 and JEIDA Standards
- Requires no External Power

DESCRIPTION

The Fujitsu MBH10302 Ethernet Card is a PCMCIA-compatible card that provides an Ethernet 10BASE-T port to a system using a PCMCIA bus. The card provides LAN connectivity for current and future generations of portable, notebook, palmtop and pen-based computers and peripherals. The 68-pin card is a complete and highly reliable LAN solution. The card fully complies with Personal Computer Standard, Release 2.0, of the Personal Computer Memory Card International Association (PCMCIA) and with ISO/IEEE/ANSI 8802-3 specifications for 10BASE-T Ethernet.

The card connects to the network via a Fujitsu-designed nine-pin I/O connector that is being considered as a PCMCIA standard. Its on-card circuitry allows attachment to 10BASE-T twisted-pair networks without the need for external line-adapter modules. The card



provides on-chip buffer management of 32 kilobytes of local buffer memory for receive and transmit packets. Data throughput speed between the buffer and the host reaches 15 megabytes/second when operating in 16-bit mode and 7 megabytes/second in 8-bit mode. By providing LAN connectivity to users of portable computers, including notebooks and hand-held devices, the card directly addresses the needs of one of the fastest-growing computer-related markets. Many new portable computer designs include slots for PCMCIA cards, anticipating a broad range of computer, industrial, and medical systems applications.

The card's advanced design derives from Fujitsu's proven LAN products, including the MB86960 NICE™ Ethernet Controller and MB86961 Universal Interface for Twisted-pair Ethernet. The card also includes a custom interface device for the PCMCIA bus. Requiring no external filtering components, the card utilizes Fujitsu's advanced technology to include all circuitry necessary for full functioning as a controller and interface from the PCMCIA bus to the Ethernet bus.

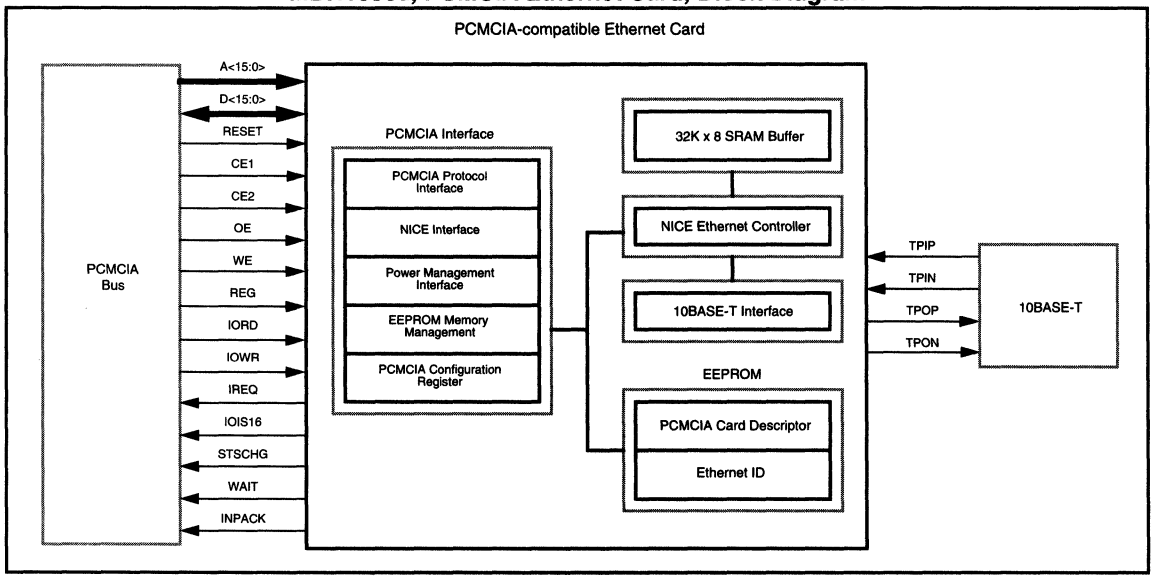
SPECIFICATIONS

- Height: 0.169 inches (4.3 mm) (Type II PC Card-compatible)
- Thickness: 0.197 inches (5.0 mm)
- Length: 3.370 inches (85.6 mm)
- Width: 2.126 inches (54.0 mm)
- Addressability: 64 megabytes
- Separate *Register* Attribute Memory Space selected by REG signal
- PCMCIA Bus Throughput with 16-bit Host: Ethernet Receive/Transmit Buffer 15 megabytes/second; I/O Space 4 megabytes/second; and Attribute Memory Space 7 megabytes/second
- Power Consumption: Active data transfer average of 700 milliwatts

Order Information -- For Sale to O.E.M. Customers Only

- Part Number: MBH10302
- Description: PCMCIA-compatible Ethernet Card

MBH10302, PCMCIA Ethernet Card, Block Diagram



MB86961/MB86961A

FUJITSU

UNIVERSAL INTERFACE FOR 10BASE-T (TWISTED-PAIR) ETHERNET

DATA SHEET

APRIL1993

Note: All descriptions apply to both MB86961 and MB86961A unless otherwise noted.

FEATURES

- Combines Manchester encoder/decoder and twisted pair transceiver functions
- Direct interface to all popular Ethernet controllers
- Direct interface to AUI and 10BASE-T outputs
- Manual or automatic AUI /10BASE-T selection
- Integrated pulse shaper and Tx/Rx filters
- Selectable 100 Ω/150 Ω termination permits operation with shielded or unshielded twisted pair cable
- Reverse-polarity detection for receiver with automatic correction
- On-chip jabber logic, SQE test and link test with enable/disable option
- Remote signaling of link down and jabber conditions
- Programmable receive threshold for extended range
- Power down mode for minimum power dissipation
- Output drivers for receive, transmit, collision and link test pass LED indicators
- Low power CMOS technology, single 5 volt power supply
- TP loopback disable for external loopback testing (MB86961A only)
- 44-pin PLCC package

Additional features in MB86961A only

- Automatic shut-down of unused port
- TP external loopback enable for testing

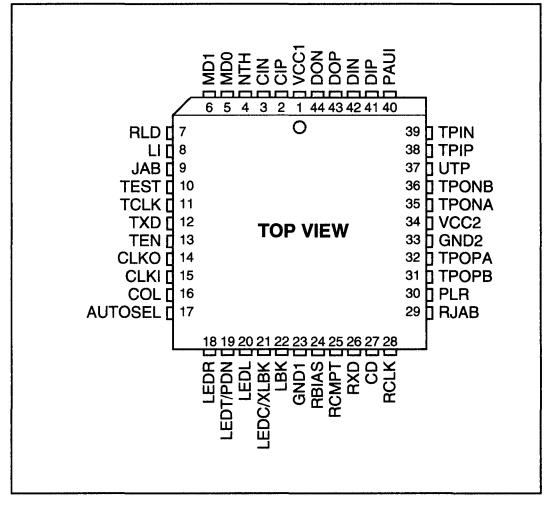
GENERAL DESCRIPTION

The MB86961(A) Universal Interface for 10BASE-T (Twisted-Pair) Ethernet is fully compliant with the IEEE 802.3 specifications for AUI (Attachment Unit Interface) and 10BASE-T (Twisted-Pair) interfaces and provides the electrical interface between an Ethernet controller and the DB15 (AUI) and RJ45 (10BASE-T) connections to an Ethernet local area network. Functions provided by the MB86961(A) include Manchester encoding and decoding of the serial data stream, level conversion, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted-pair input.

Pulse shaping and filtering functions are performed by the MB86961(A) to eliminate the need for external filtering components and thus reduce overall system cost. The device also provides outputs for receive, transmit, collision and link test LEDs and provides compatibility with both shielded and unshielded twisted pair cables. The receive threshold can be reduced to allow an extended range between nodes in low noise environments. Its wide range of features and its ability to interface to virtually all popular controllers make the MB86961(A) the ideal device for twisted pair Ethernet applications.

The MB86961(A) is part of a complete family of Ethernet devices available from Fujitsu. It is fabricated in a low-power CMOS technology and is supplied in a 44-pin PLCC package.

PIN CONFIGURATION



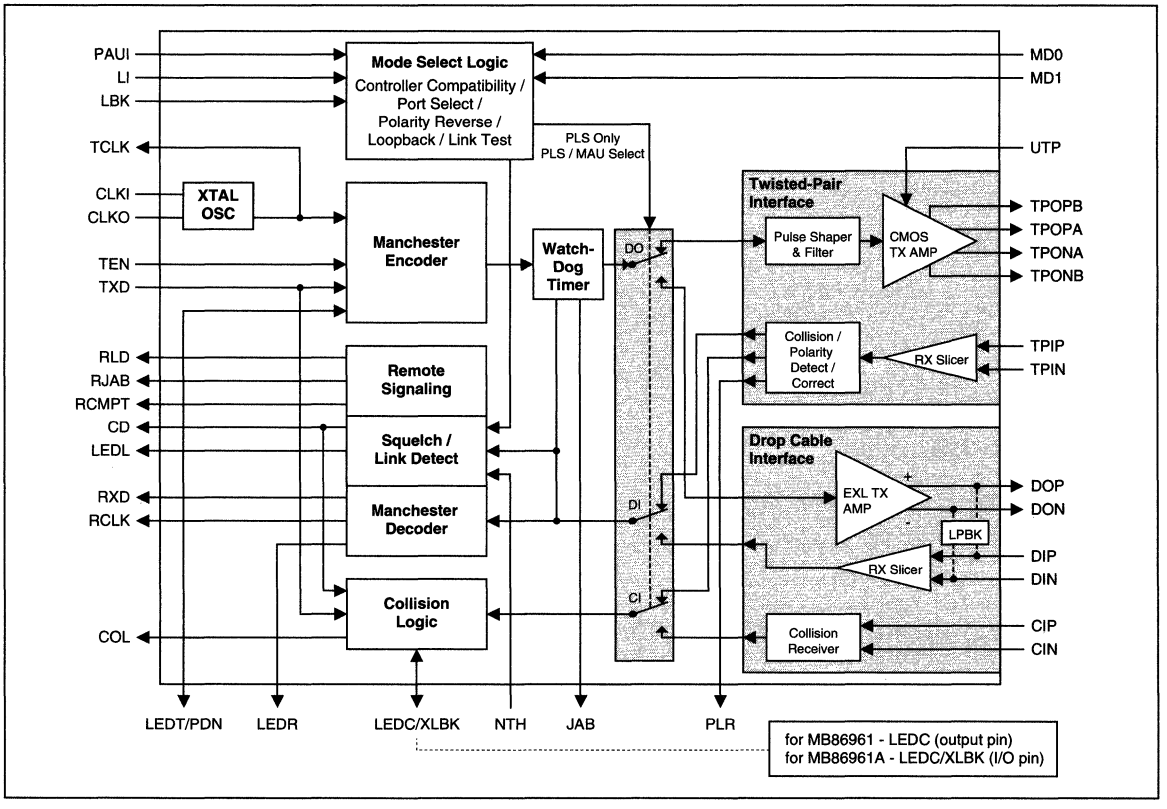
PIN ASSIGNMENT – 44-PIN PLCC

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	VCC1	-	12	TXD	I	23	GND1	-	34	VCC2	-
2	CIP	I	13	TEN	I	24	RBIAS	I	35	TPONA	O
3	CIN	I	14	CLKO	O	25	RCMPT	O	36	TPONB	O
4	NTH	I	15	CLKI	I	26	RXD	O	37	UTP	I
5	MD0	I	16	COL	O	27	CD	O	38	TPIP	I
6	MD1	I	17	AUTOSEL	I	28	RCLK	O	39	TPIN	I
7	RLD	O	18	LEDR	O	29	RJAB	O	40	PAUI	I
8	LI	I	19	LEDT/PDN	I/O	30	PLR	O	41	DIP	I
9	JAB	O	20	LEDL	I/O	31	TPOPB	O	42	DIN	I
10	TEST	I	21	LEDC/XLBK	I/O	32	TPOPA	O	43	DOP	O
11	TCLK	O	22	LBK	I	33	GND2	-	44	DON	O

ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5
44-Pin Plastic Leaded Chip Carrier	LCC-44P-M02	MB86961(A)PD-G

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Symbol	Type	Description
AUTOSEL	I	**AUTOMATIC PORT SELECT:** When AUTOSEL=1, automatic port selection is enabled (the MB86961(A) defaults to the AUI port only if TP link integrity = Fail). When AUTOSEL=0, manual port selection is enabled (the PAUI pin determines the active port).
CD	O	**CARRIER DETECT:** An output to notify the controller of activity on the network.
CIP CIN	I I	**AUI COLLISION PAIR:** Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
CLKO CLKI	O I	**CRYSTAL OSCILLATOR:** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI.
COL	O	**COLLISION DETECT:** Output which drives the collision detect input of the controller.
DIP DIN	I I	**AUI RECEIVE PAIR:** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
DOP DON	O O	**AUI TRANSMIT PAIR:** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.
JAB	O	**JABBER INDICATION:** Output goes high to indicate Jabber state.
LBK	I	**LOOPBACK:** When LBK=1, forced loopback is enabled. When LBK=0, normal loopback is enabled.
LEDC/XLBK	O	**COLLISION LED:** Open drain driver for the collision indicator. Output is pulled low during collision. For MB86961A only, if externally tied low, the MB86961A only disables the internal TP loopback and collision detection circuits in anticipation of external TP loopback. MB86961A is ready for loopback testing 16 ms after this pin goes low. No delay is needed when the pin goes high.
LEDL	I/O	**LINK LED:** Open drain driver for link integrity indicator. Output is pulled low during link test pass. If externally tied low, internal circuitry is forced to "Link Pass" state and the MB86961(A) will continue to transmit link test pulses.
LEDR	O	**RECEIVE LED:** Open drain driver for the receive indicator LED. Output is pulled low during receive.
LEDT/ PDN	O I	**TRANSMIT LED/POWER DOWN:** Open drain driver for the transmit indicator. Output is pulled low during transmit. If externally tied low, the MB86961(A) goes to power down state.
LI	I	**LINK TEST ENABLE:** When LI = 0, the Link Integrity Test function is disabled. When LI=1, the Link Integrity Test function is enabled.
MD0 MD1	I I	**MODE SELECT:** Mode select pins which determine controller compatibility mode. See Table 1.
NTH	I	**NORMAL THRESHOLD:** When NTH = 1, the normal TP squelch threshold is in effect. When NTH = 0, the normal TP squelch threshold is reduced by 4.5 dB.
PAUI	I	**PORT/AUI SELECT:** In Manual Port Select mode (AUTOSEL=0), PAUI selects the active port. When PAUI=1, the AUI port is selected. When PAUI=0, the TP port is selected. In Auto Port Select mode, PAUI is ignored.
PLR	O	**POLARITY REVERSE:** Output goes high to indicate reversed polarity.
RBIAS	I	**BIAS CONTROL:** A bias resistor at this pin controls the bias of the operating circuit.
RCLK	O	**RECEIVE CLOCK:** A recovered 10 MHz clock which is synchronous with the received data and connected to the controller receive clock input.

SIGNAL DESCRIPTIONS (Continued)

Symbol	Type	Description
RCMPT	O	**REMOTE COMPATIBILITY:** Output goes high to signal the controller that the remote port is compatible with the MB86961(A) remote signaling features.
RJAB	O	**REMOTE JABBER:** Output goes high to signal the controller that the remote port is in Jabber condition.
RLD	O	**REMOTE LINK DOWN:** Output goes high to signal to the controller that the remote port is in link down condition.
RXD	O	**RECEIVE DATA:** Output signal connected directly to the receive data input of the controller.
TCLK	O	**TRANSMIT CLOCK:** A 10 MHz clock output. This clock signal is directly connected to the transmit clock input of the controller.
TEN	I	**TRANSMIT ENABLE:** Enables data transmission and starts the watchdog timer. Synchronous with TCLK (see Figures 14, 20, 26 and 32 for details).
TEST	I	**TEST:** Input for factory test of the device. Leave open for normal operation.
TPIP TPIN	I I	**RECEIVE TWISTED-PAIR:** A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.
TPOPA/B TPONA/B	O O	**TRANSMIT TWISTED-PAIR:** Two differential driver pair outputs (A and B) to the twisted-pair cable. The output is pre-equalized, no external filter is required. Two pairs are used to provide compatibility with both 100 Ω load cable and 150 Ω load cable.
TXD	I	**TRANSMIT DATA:** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
UTP	I	**UTP/STP SELECT:** When UTP = 0, 150 Ω termination for shielded TP is selected. When UTP = 1, 100 Ω termination for unshielded TP is selected.
VCC1, VCC2	-	**POWER INPUTS:** +5 V power supply inputs.
GND1 GND2	– –	**GROUND RETURNS 1 & 2:** Grounds.

APPLICATIONS

Figure 1 shows the MB86961(A) in a typical application, interfacing between a controller and the RJ45 connector of the twisted-pair network. Figures 2 through 5 show detailed diagrams of various MB86961(A) applications.

AUTO PORT SELECT WITH LOOPBACK CONTROL PIN

With MD0 and MD1 both tied high, the MB86961(A) logic and framing are set to Mode 4 (compatible with National NS8390 controllers).

The AUTOSEL pin is tied high, allowing the MB86961(A) to automatically select the active port. The high at LI enables Link Testing.

The UTP and NTH pins are both tied high, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. (See Figure 2.)

MANUAL PORT SELECT WITH LINK TEST FUNCTION

With MD0 low and MD1 tied high, the MB86961(A) logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 and MB86960 controllers). As in Figure 2, the LI pin is tied high, enabling Link Testing, and the UTP and NTH pins are both tied high, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. However, in this application AUTOSEL is tied low, allowing external port selection through the PAUI pin. The remote status outputs are inverted and used to drive LED indicators. (See Figure 3.)

TWISTED-PAIR ONLY

Figure 4 shows the MB86961(A) in a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. (The AUI port is not used.) With MD0 tied high and MD1 grounded, the MB86961(A) logic and framing are set to Mode 2 (compatible with Intel 82586 controllers). The LI pin externally controls the link test function. The UTP and NTH pins are both tied low, selecting the reduced receiver threshold and 150 Ω termination for shielded TP cable. The switch at LEDT/PDN manually controls the power down mode. (See Figure 4.)

AUI ENCODER/DECODER ONLY

In this application the DTE is connected to a coaxial network through the AUI. AUTOSEL and PAUI are both tied to ground, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both grounded, the MB86961(A) logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied low, disabling the link test function. The LBK input controls loopback. A 20 MHz crystal connected across CLKI and CLKO provides the required clock signal. (See Figure 5.)

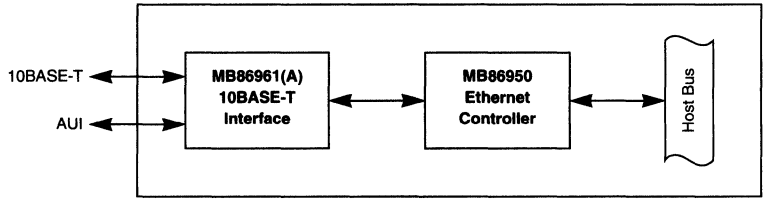
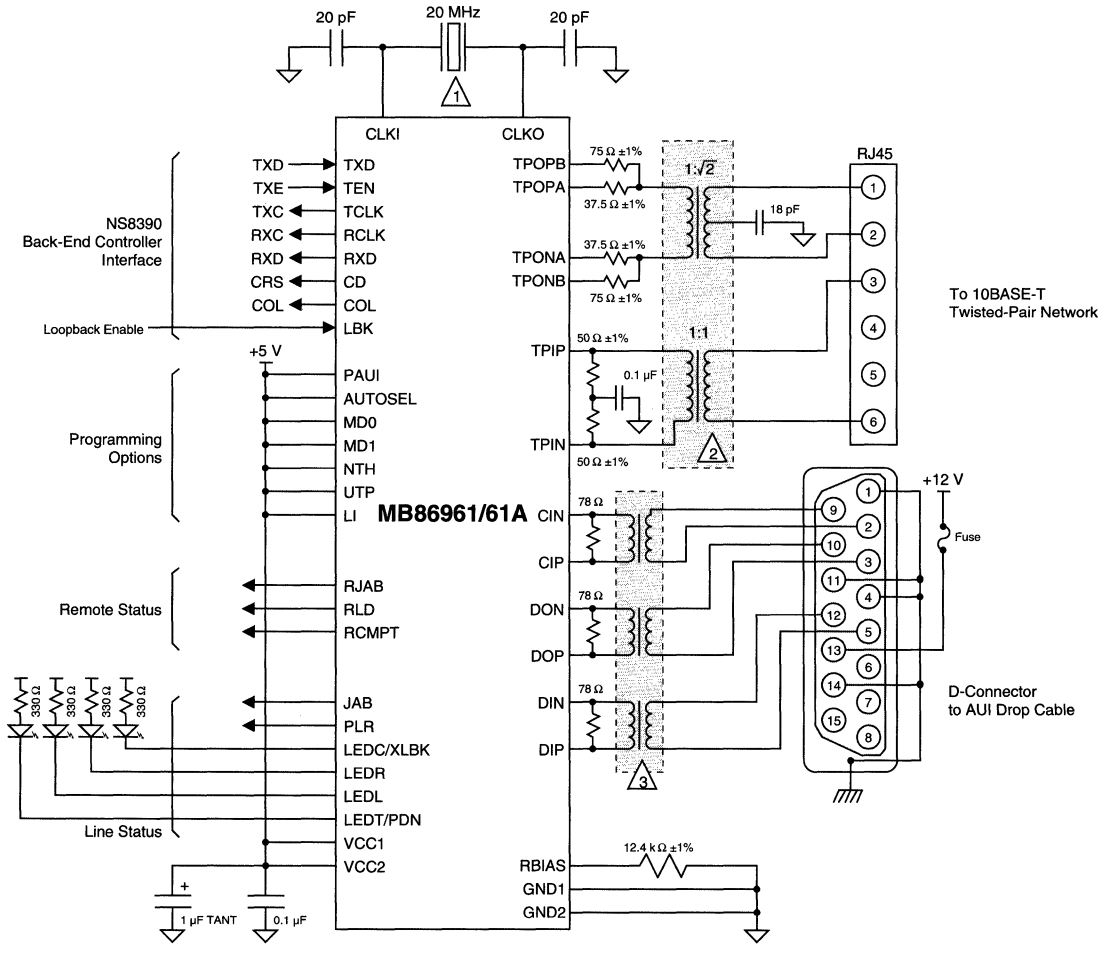


Figure 1. Typical System Diagram

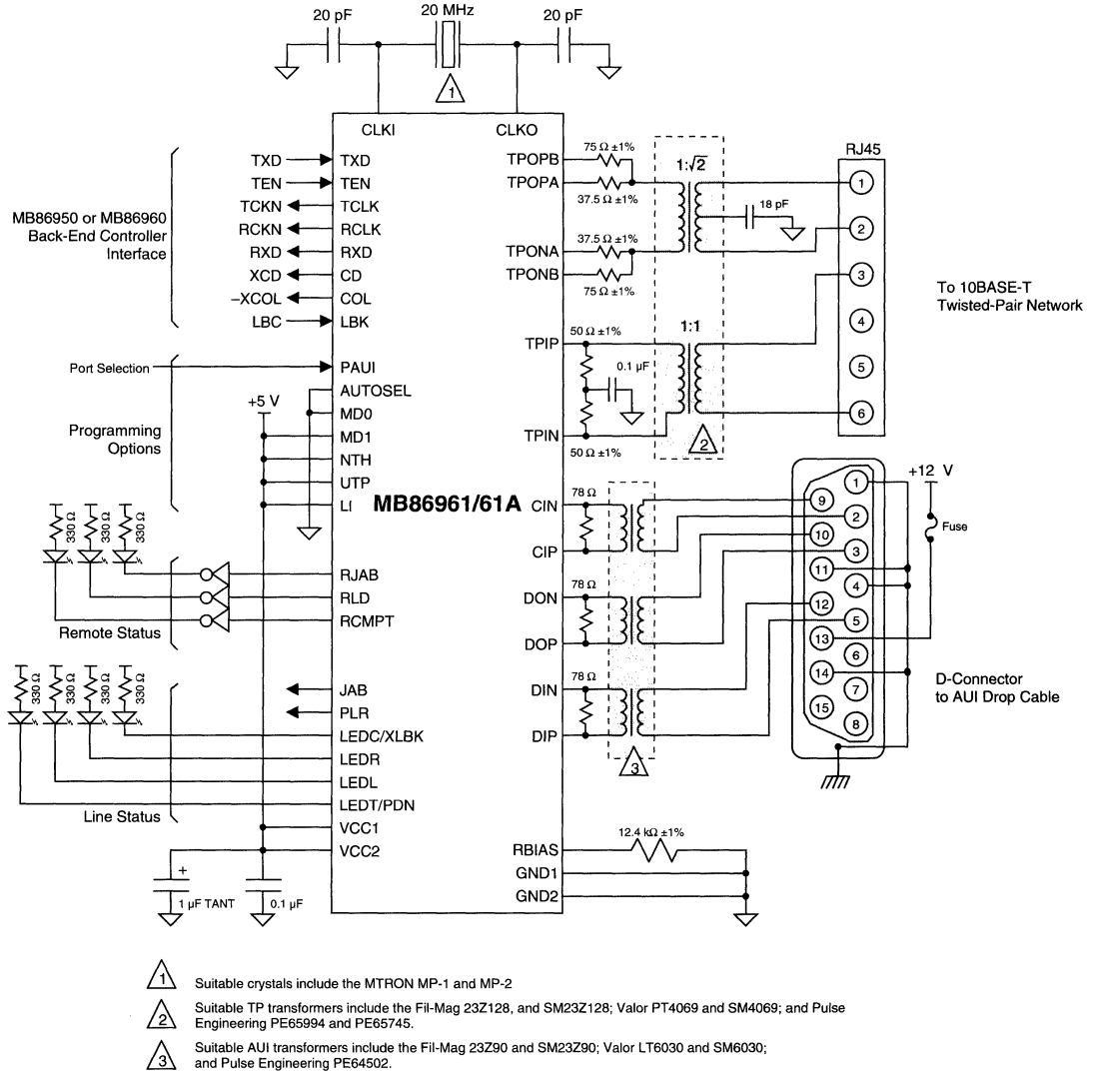


1 Suitable crystals include the MTRON MP-1 and MP-2

2 Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and SM4069; and Pulse Engineering PE65994, PE65745, PE65746, and PE65454.

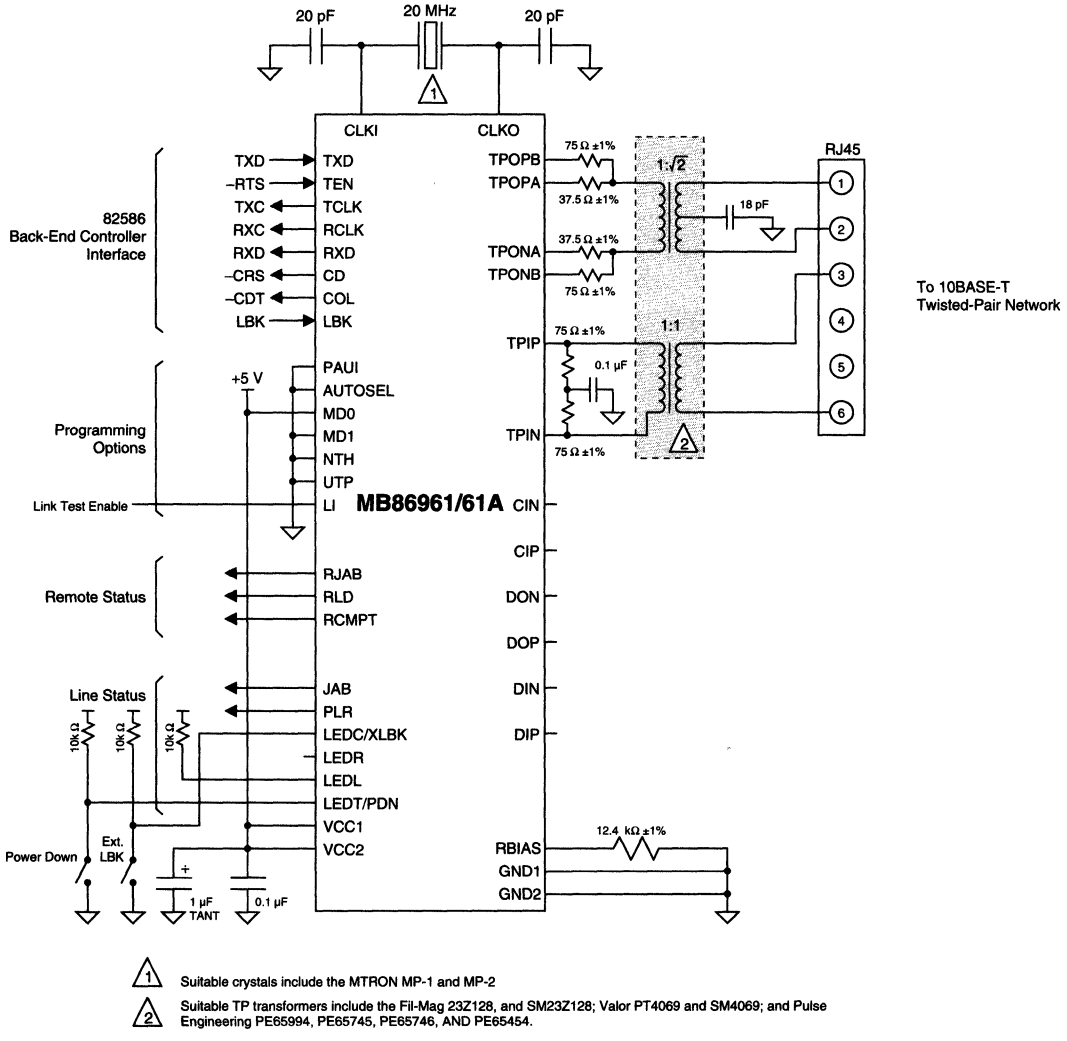
3 Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and SM6030; and Pulse Engineering PE64502.

Figure 2. LAN Adapter Board Application - Auto Port Select with External Loopback Control



1. Suitable crystals include the MTRON MP-1 and MP-2
2. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and SM4069; and Pulse Engineering PE65994 and PE65745.
3. Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and SM6030; and Pulse Engineering PE64502.

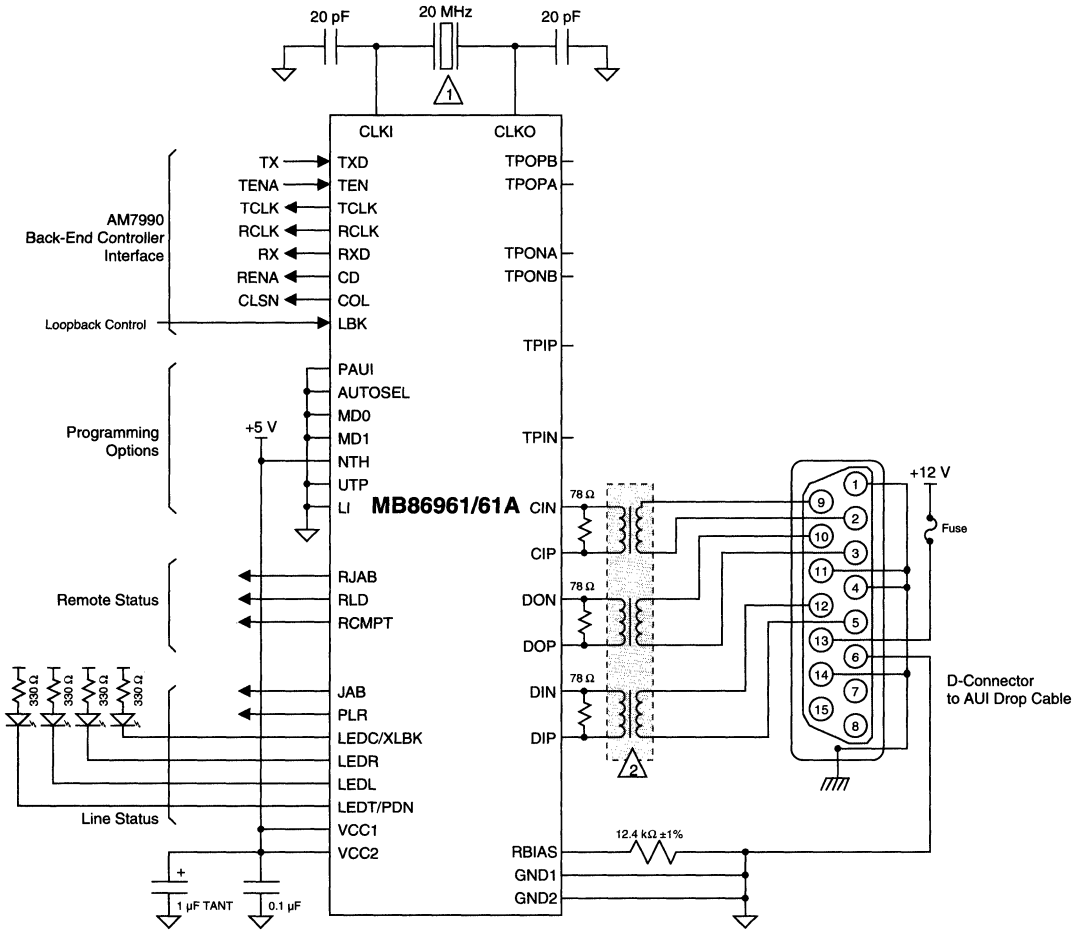
Figure 3. LAN Adapter Board Application - Manual Port Select with Link Test Function



1 Suitable crystals include the MTRON MP-1 and MP-2

2 Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and SM4069; and Pulse Engineering PE65994, PE65745, PE65746, AND PE65454.

Figure 4. Twisted-Pair Only Application



1 Suitable crystals include the MTRON MP-1 and MP-2

2 Suitable AUI transformers include the Fil-Mag 23Z90 and SM23Z90; Valor LT6030 and SM6030; and Pulse Engineering PE64502.

Figure 5. AUI Encoder/Decoder Only Application

FUNCTIONAL DESCRIPTION

The MB86961(A) Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as a PLS-only device (for use with 10BASE2 or 10BASE5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10BASE-T twisted-pair networks).

The MB86961(A) interfaces a back-end controller to either an AUI drop cable or twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the MB86961(A) contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The MB86961(A) Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The MB86961(A) Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the MB86961(A) performs all required MAU functions defined by the IEEE 802.3 10BASE-T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the MB86961(A) receives incoming signals from the AUI DI circuit with up to 18ns of jitter and drives the AUI DO circuit.

CONTROLLER COMPATIBILITY MODES

The MB86961(A) is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu and National Semiconductor. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins MD0 and MD1 determine controller compatibility modes as listed in table 1.

Table 1. MB86961(A) Compatibility Modes

MD1	MD0	Mode	
0	0	Mode 1:	Compatible with Advanced Micro Devices AM7990 controllers
0	1	Mode 2:	Compatible with Intel 82586 controllers
1	0	Mode 3:	Compatible with Fujitsu MB86950 and MB86960 controllers
1	1	Mode 4:	Compatible with National Semiconductor 8390 controllers

A complete set of timing diagrams is provided for each mode as follows:

- Mode 1: Figures 12-17
- Mode 2: Figures 18-23
- Mode 3: Figures 24-29
- Mode 4: Figures 30-35

The related timing specifications are provided in the electrical characteristics section of this data sheet.

TRANSMIT FUNCTION

The MB86961(A) receives NRZ data from the controller at the TXD input (see MB86961(A) block diagram), and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 6. The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. No external filters are required. During idle periods, the MB86961(A) transmits link integrity test pulses on the TPO circuit if LI is enabled and integrated PLS/MAU mode is selected. The MB86961(A) can be programmed for either shielded TP (150 Ω) or unshielded TP (100 Ω) through the UTP pin.

JABBER CONTROL FUNCTION

Figure 7 is a state diagram of the MB86961(A) Jabber control function. The MB86961(A) on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and activates the JAB pin. Once the MB86961(A) is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

SQE FUNCTION

In the integrated PLS/MAU mode, the MB86961(A) supports the signal quality error (SQE) function as shown in Figure 8. After every successful transmission on the 10BASE-T network, the MB86961(A) transmits the SQE signal to the DTE for 10 ±5 bit times over the internal CI Circuit.

RECEIVE FUNCTION

The MB86961(A) receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI Circuit). Valid received signals are passed through the on-chip filters and Manchester decoder and output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively. No external filters are required.

An internal intelligent squelch function discriminates noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the MB86961(A) receive function enters the idle state. If the polarity of the TPI circuit is reversed, the MB86961(A) detects the polarity reversal and reports it via the PLR output. The MB86961(A) automatically corrects reversed polarity.

POLARITY REVERSE FUNCTION

The MB86961(A) polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are

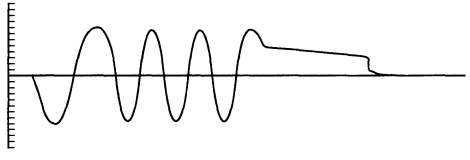


Figure 6. MB86961(A) TPO Output Waveform

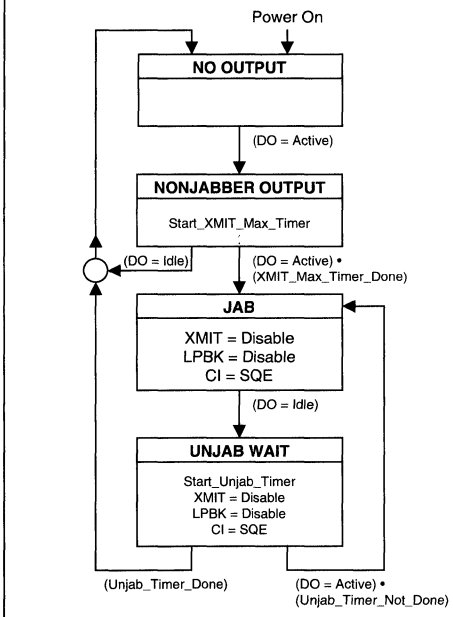


Figure 7. Jabber Control Function

reset to zero. If the MB86961(A) enters the link fail state and no valid data or link pulses are received within 96 to 128 ms the polarity is reset to the default non-flipped condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The MB86961(A) reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 9 is a state diagram of the MB86961(A) collision detection function. Refer to Electrical Characteristics for collision detection and COL/CI output timing.

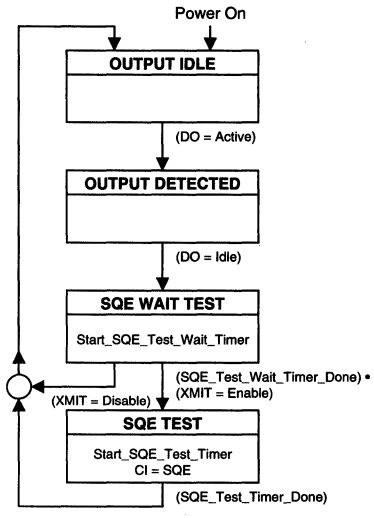


Figure 8. SQE Function

LOOPBACK FUNCTION

The MB86961(A) provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the MB86961(A) from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. The "normal" loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The MB86961A also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied low, the LXT901 disables the collision detection and internal loopback circuits, to allow external loopback. (This function is not implemented in the MB86961(A).) The MB86961(A) provides additional loopback functions controlled by pin 22 (LBK). When the TP port is selected and LBK=1, TP loopback is "forced," overriding collisions

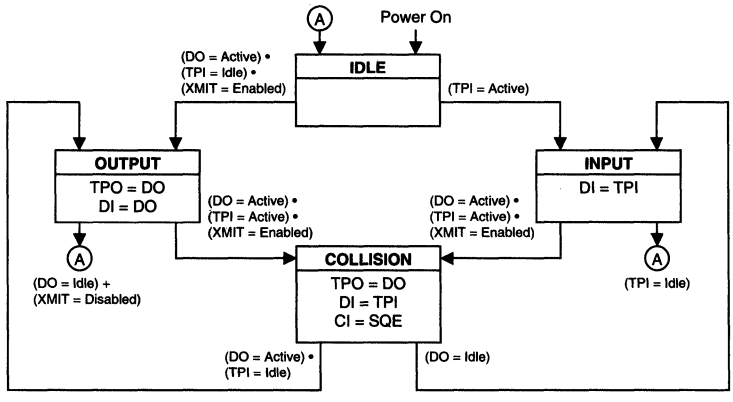


Figure 9. Collision Detection Function

on the TP circuit. When LBK=0, normal loopback is in effect.

When the AUI port is selected and LBK=1, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK=0, no AUI loopback occurs.

LINK INTEGRITY TEST

Figure 10 is a state diagram of the MB86961(A) Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50-150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The MB86961(A) ignores any link integrity pulse with an interval less than 2-7 ms. The MB86961(A) will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

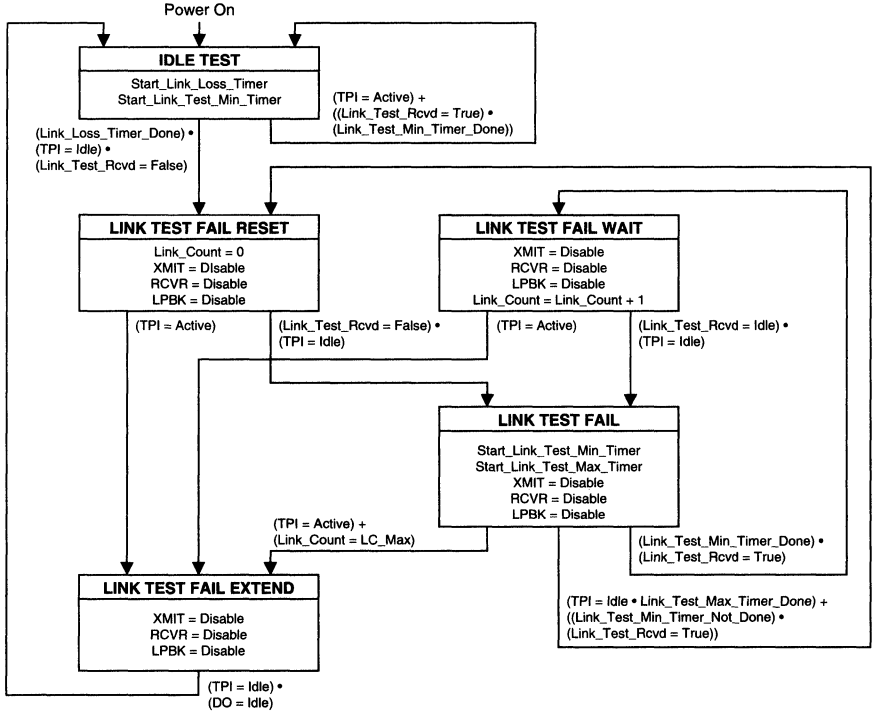
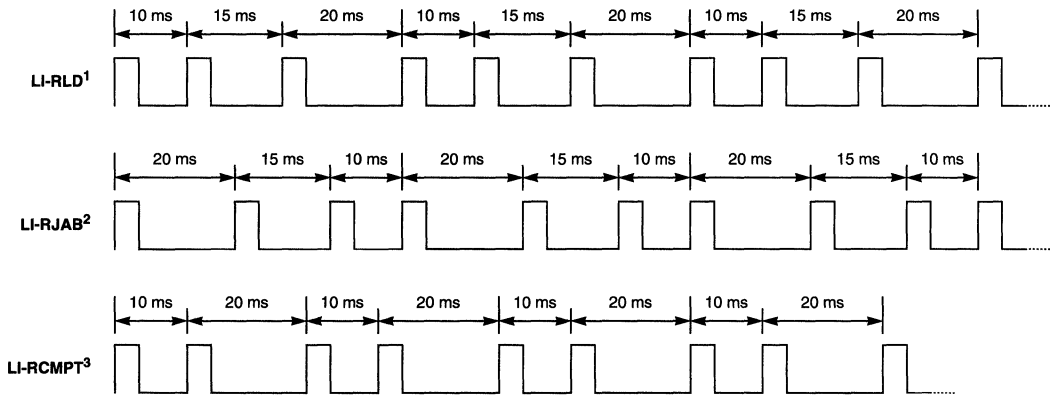


Figure 10. Link Integrity Test Function

REMOTE SIGNALING

The MB86961(A) transmits standard link pulses which meet the 10BASE-T specification. However, the MB86961(A) encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the MB86961(A) can signal three local conditions: link down, jabber, and remote signaling capability. Figure 11 shows the interval variations used to signal local status to the other end of the line. The MB86961(A) also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.



1. For Remote Link Down (RLD) signaling, the interval between LI pulses increments from 10 ms to 15 ms to 20 ms, and then the cycle starts over.
2. For Remote Jabber (RJAB) signaling, the interval between LI pulses decrements from 20 ms to 15 ms to 10 ms, and then the cycle starts over.
3. For Remote Compatibility (RCMPT) signaling, the interval between LI pulses continually switches between 10 ms and 20 ms.

Figure 11. Remote Signaling Link Integrity Pulse Timing

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.3	6	V
T_{OP}	Operating temperature		-40	85	C
T_{ST}	Storage temperature		-65	150	C

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

INPUT/OUTPUT CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5 V ±5%)

Symbol	Parameter		Condition	Min.	Typ.[1]	Max.	Units
V_{IL}	Input low voltage[2]			-	-	0.8	V
V_{IH}	Input high voltage[2]			2.0	-	-	V
V_{OL}	Output low voltage		I_{OL} =1.6 mA for MB86961	-	-	0.4	V
			I_{OL} =3.2 mA for MB86961(A)	-	-	0.4	V
			I_{OL} < 10 µA	-	-	10	%V_{CC}
V_{OH}	Output high voltage		I_{OH} = 40 µA	2.4	-	-	V
			I_{OH} < 10 µA	90	-	-	%V_{CC}
ICC	Supply current		Normal mode	-	90	-	mA
			Power-down mode	-	5	-	mA
t_R	Output rise time	CMOS	TCLK and RCLK	-	3	-	ns
		TTL	TCLK and RCLK	-	2	-	ns
t_F	Output fall time	CMOS	TCLK and RCLK	-	3	-	ns
		TTL	TCLK and RCLK	-	2	-	ns

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V.

AUI ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
I_{IL}	Input low current		-	-	-700	µA
I_{IH}	Input high current		-	-	500	µA
V_{OD}	Differential output voltage		±550	-	±1200	mV
V_{DS}	Differential squelch threshold		-	220	-	mV

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TP ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
Z_{OUT}	Transmit output impedance		-	5	-	Ω
V_{OD}	Peak differential output voltage	Load=100 Ω at TPOP and TPON	-	3.5	-	V
t_{JIT}	Transmit timing jitter addition[2]	0 line length	-	-	±8	ns
		After line model specified by IEEE 802.3 for 10BASE-T	-	-	±3.5	ns
Z_{IN}	Receive input impedance	Between TPIP/TPIN, CIP/CIN and DIP/DIN	-	20	-	kΩ
V_{DS}	Differential squelch threshold		-	420	-	mV
V_{DSL}	Lower squelch threshold		-	250	-	mV

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to product testing.

SWITCHING CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Jabber Timing						
t_{JAB}	Maximum transmit time		20	-	150	ms
t_{UJAB}	Unjab time		250	-	750	ms
Link Integrity Timing						
t_{LL}	Time link loss		55	-	66	ms
t_{LP1}	Time between Link Integrity Pulses		8	-	24	ms
t_{LP2}	Interval for valid receive Link integrity Pulses		4.1	-	65	ms
General						
t_{RST}	Receive start-up delay[1]		0	-	500	ns
t_{TST}	Transmit start-up delay[1]		0	-	200	ns
t_{LST}	Loopback start-up delay[1]		0	-	500	ns

1. Parameter is guaranteed by design; not subject to production testing.

RCLK/Start-of-Packet Timing

Symbol	Parameter		Min.	Typ.[1]	Max.	Units
t_{DATA}	Decoder acquisition time	AUI	-	900	-	ns
		TP	-	1300	-	ns
t_{CD}	CD turn-on delay	AUI	-	50	-	ns
		TP	-	400	-	ns
t_{RDS}	Receive data setup from RCLK	Mode 1	40	-	-	ns
		Modes 2, 3 and 4	30	-	-	ns
t_{RDH}	Receive data hold from RCLK	Mode 1	10	-	-	ns
		Modes 2, 3 and 4	30	-	-	ns

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

RCLK/End-of-Packet Timing

Symbol	Parameter	Type[1]	Mode 1	Mode 2	Mode 3	Mode 4	Units
t_{RCH}	RCLK hold after CD low	Min.	0	1	27	5	bt
t_{RD}	RCV data throughput delay	Typ.	300	275	275	275	ns
t_{CDOFF}	CD turn off delay[2]	Typ.	400	375	375	375	ns
t_{IFG}	Receive block out	Typ.	2	50	27	5	bt

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
2. CD Turn off delay measured from middle of last bit, so timing specification is unaffected by the value of the last bit.

Transmit Timing

Symbol	Parameter	Min.	Typ.[1]	Max.	Units
t_{EHCH}	TEN setup from TCLK	-	30	-	ns
t_{DSCH}	TXD setup from TCLK	-	30	-	ns
t_{CHEL}	TEN hold after TCLK	-	5	-	ns
t_{CHDU}	TXD hold after TCLK	-	5	-	ns

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Collision Detection, COL/CI Output and Loopback Timing

Symbol	Parameter	Min.	Typ.[1]	Max.	Units
t_{COLD}	COL turn on delay	-	50	-	ns
t_{COLOFF}	COL turn off delay	-	160	-	ns
t_{SQED}	SQE Delay	0.65	-	1.6	µs
t_{SQEP}	SQE Pulse Duration	500	-	1500	ns
t_{KHEH}	LBK setup from TEN	-	25	-	ns
t_{KHEL}	LBK hold after TEN	-	0	-	ns

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

MODE 1 (MD1=0, MD0=0) TIMING DIAGRAMS — FIGURES 12-17

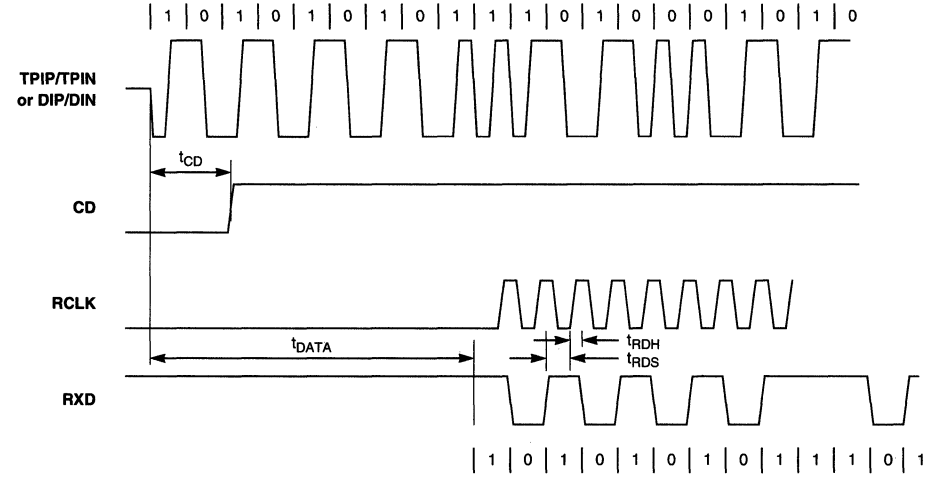
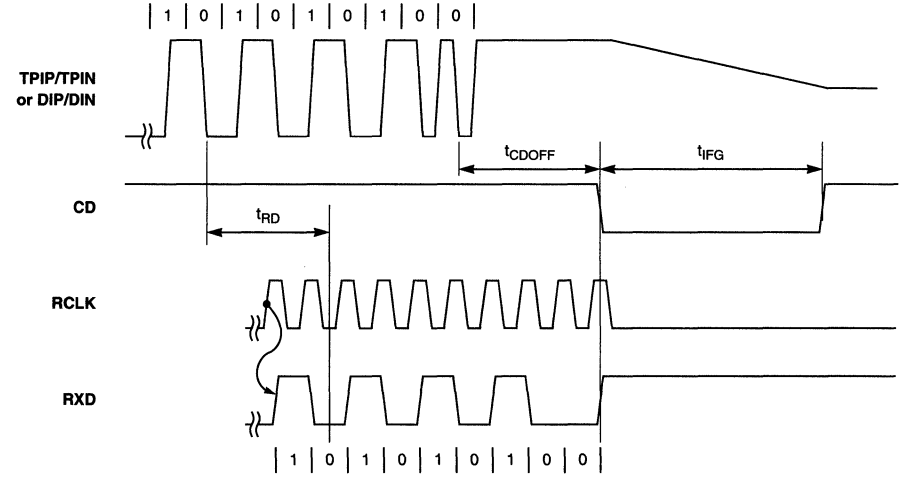


Figure 12. Mode 1 RCLK/SOP Timing



Note: RXD is triggered by the rising edge of RCLK, with RCLK advanced by 25 ns. The controller is sampled at the rising edge.

Figure 13. Mode 1 RCLK/EOP Timing

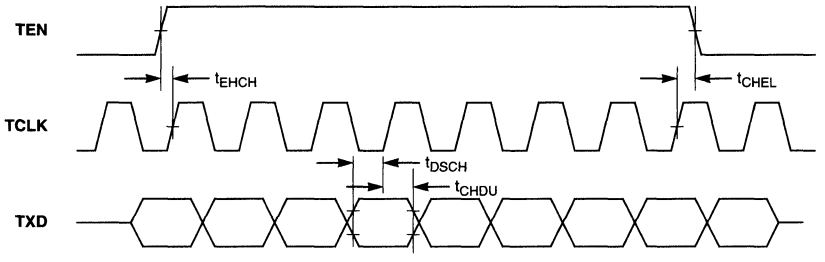


Figure 14. Mode 1 Transmit Timing

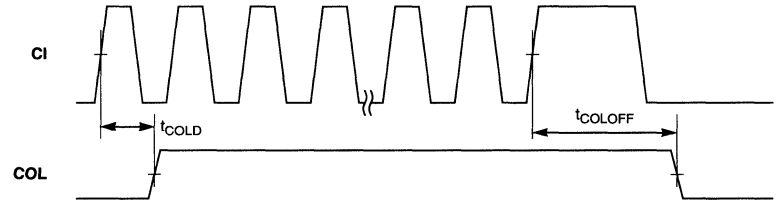


Figure 15. Mode 1 Collision Detect Timing

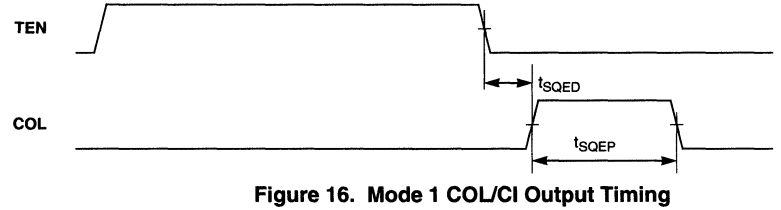


Figure 16. Mode 1 COL/CI Output Timing

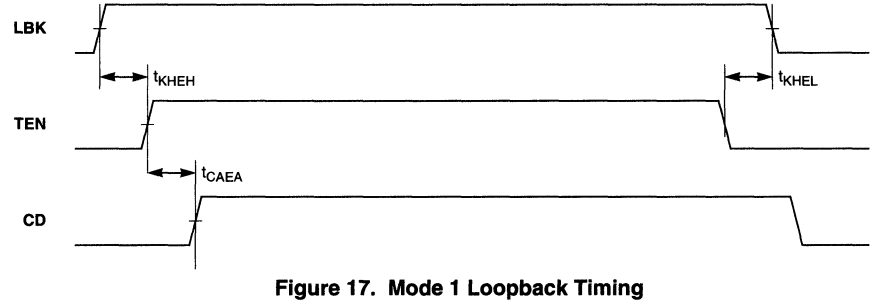
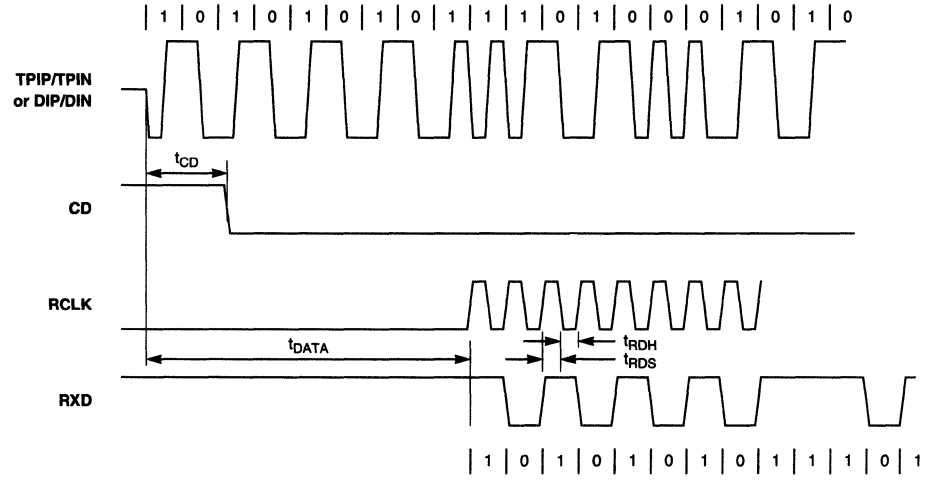


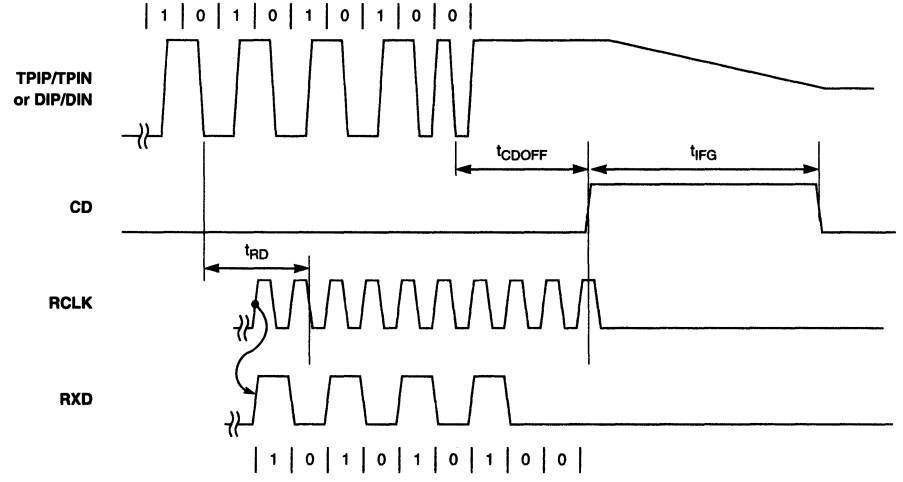
Figure 17. Mode 1 Loopback Timing

MODE 2 (MD1=0, MD0=1) TIMING DIAGRAMS — FIGURES 18-23



Note: RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 18. Mode 2 RCLK/SOP Timing



Note: RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 19. Mode 2 RCLK/EOP Timing

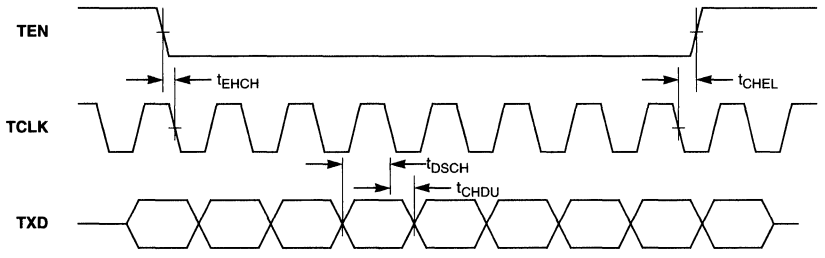


Figure 20. Mode 2 Transmit Timing

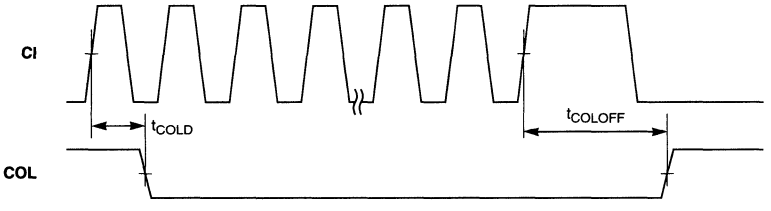


Figure 21. Mode 2 Collision Detect Timing

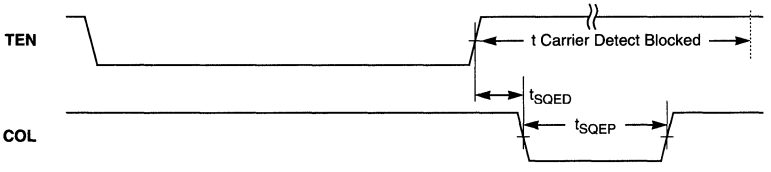


Figure 22. Mode 2 COL/CI Output Timing

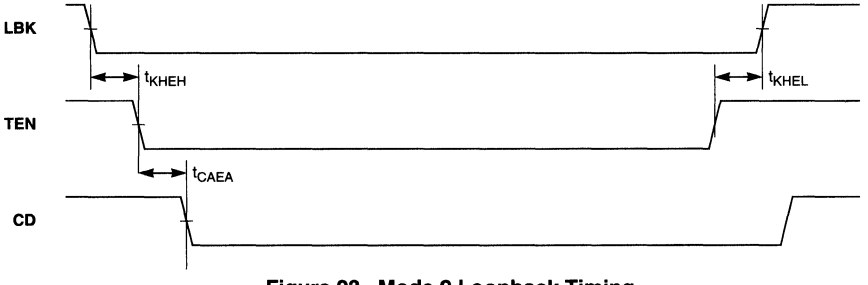
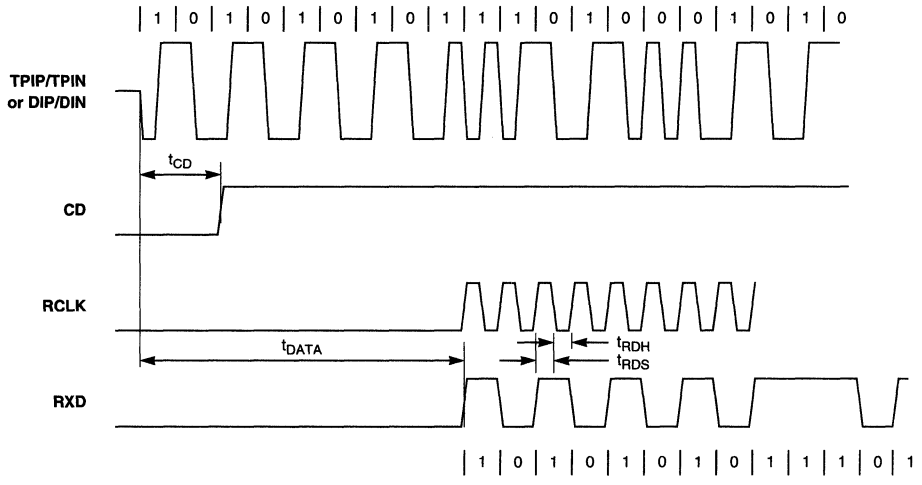


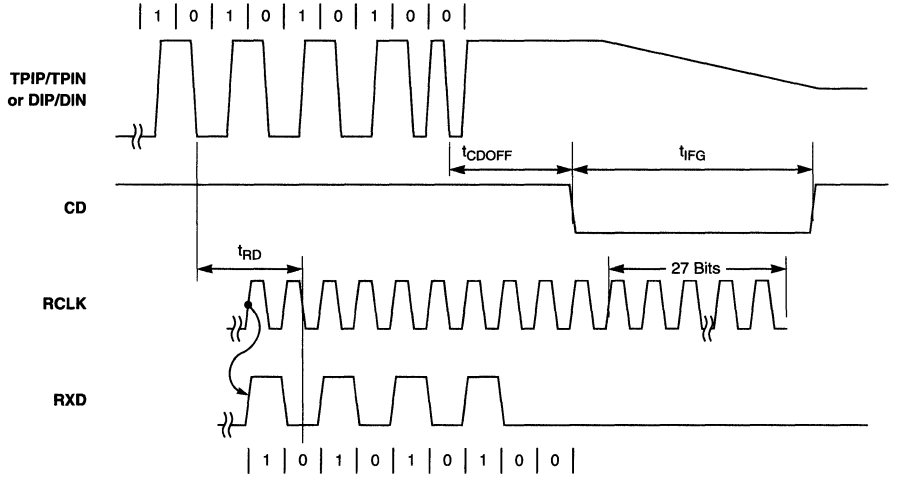
Figure 23. Mode 2 Loopback Timing

MODE 3 (MD1=1, MD0=0) TIMING DIAGRAMS — FIGURES 24-29



Note: RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 24. Mode 3 RCLK/SOP Timing



Note: RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 25. Mode 3 RCLK/EOP Timing

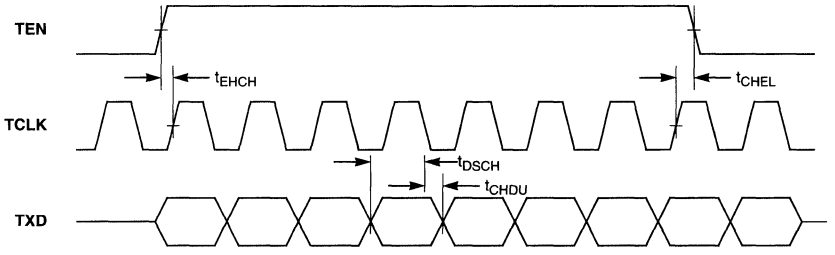


Figure 26. Mode 3 Transmit Timing

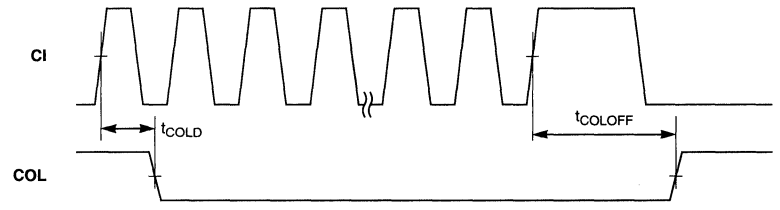


Figure 27. Mode 3 Collision Detect Timing

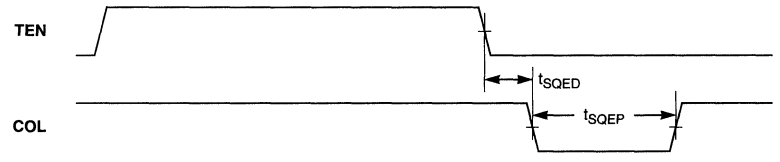


Figure 28. Mode 3 COL/CI Output Timing

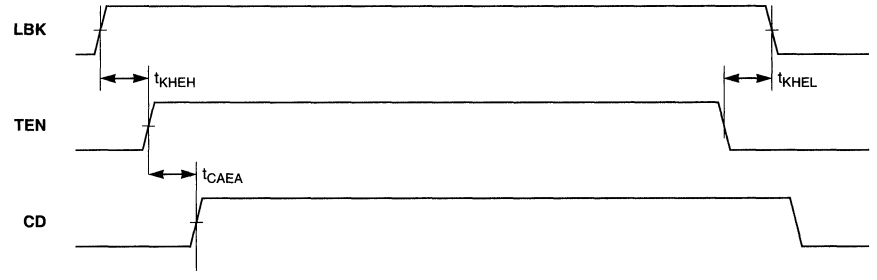
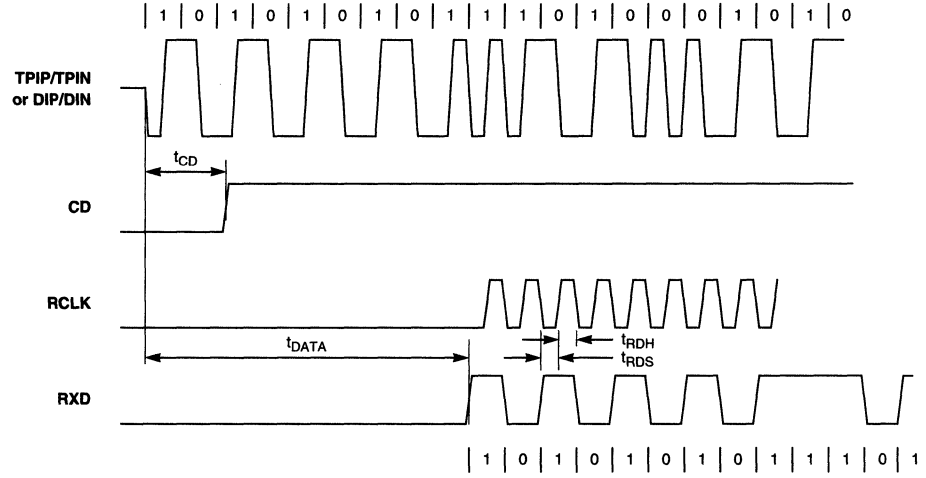


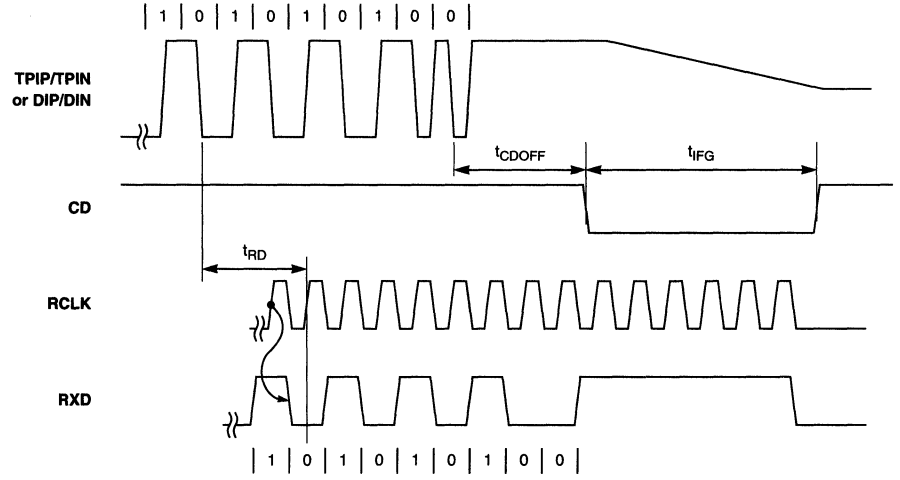
Figure 29. Mode 3 Loopback Timing

MODE 4 (MD1=1, MD0=1) TIMING DIAGRAMS — FIGURES 30-35



Note: RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 30. Mode 4 RCLK/SOP Timing



Note: RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 31. Mode 4 RCLK/EOP Timing

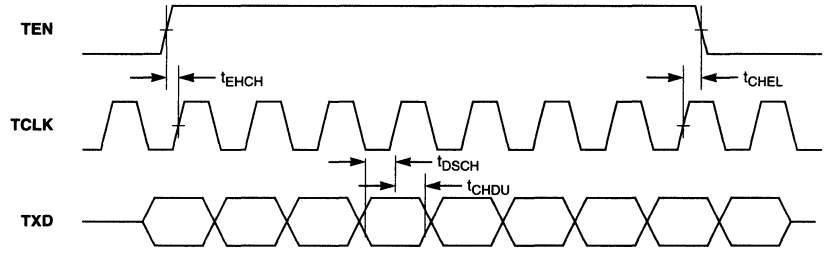


Figure 32. Mode 4 Transmit Timing

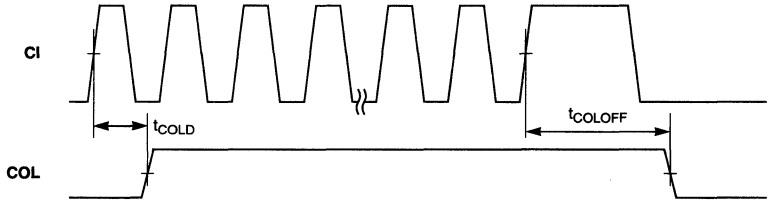


Figure 33. Mode 4 Collision Detect Timing

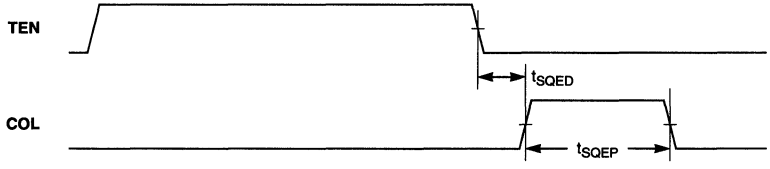


Figure 34. Mode 4 COL/CI Output Timing

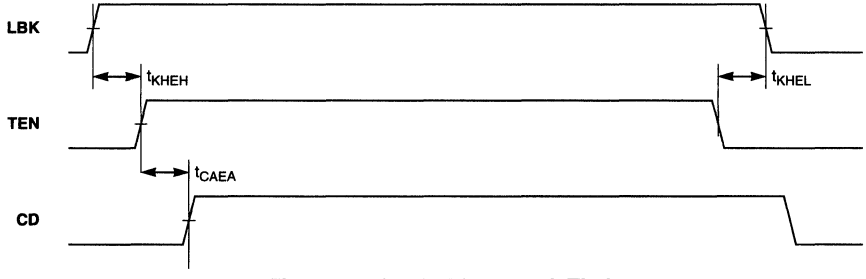
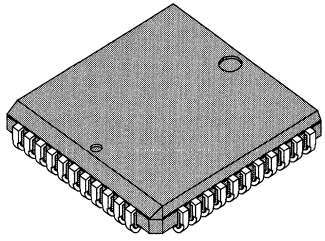


Figure 35. Mode 4 Loopback Timing

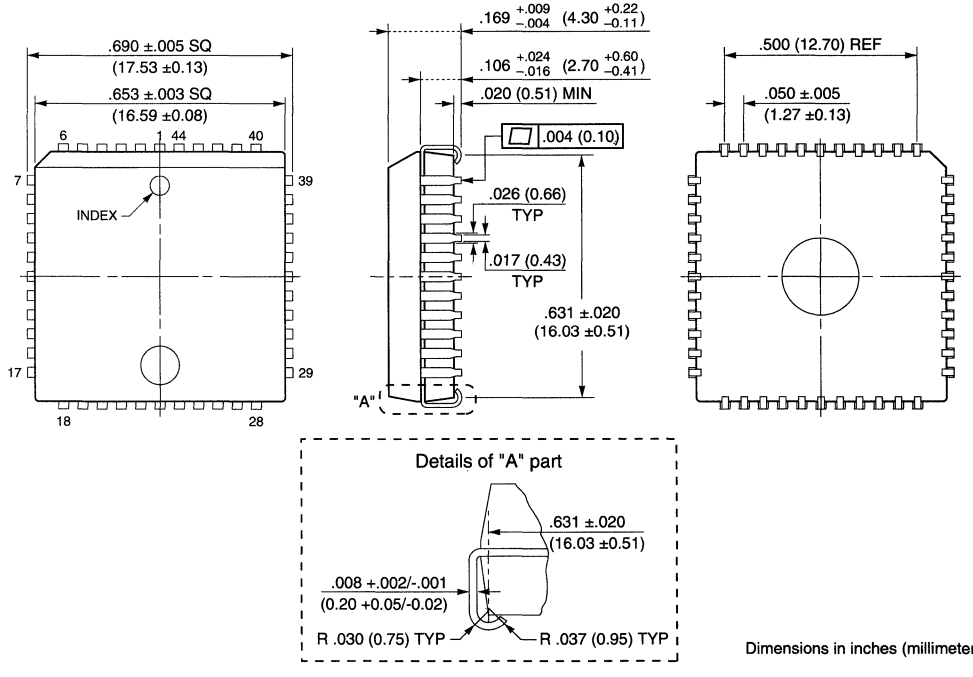
44-PIN PLASTIC LEADED CHIP CARRIER



Ordering Information: MB86961PD-G

44-LEAD PLASTIC LEADED CHIP CARRIER

(Case No.: LCC-44P-M02)



Dimensions in inches (millimeters)

MB86962

FUJITSU

10BASE-T TRANSCEIVER FOR TWISTED-PAIR ETHERNET

DATA SHEET

APRIL1993

FEATURES

- Complete implementation of IEEE 802.3 10BASE-T Medium Attachment Unit (MAU)
- Automatic AUI/10BASE-T selection
- Direct interface to AUI and RJ45 connectors
- Reverse polarity detection for receiver and selectable correction
- On-chip jabber logic, link test, and SQE Test with enable/disable options
- Programmable receive threshold for extended range
- LED drivers for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator
- Single 5 volt power supply, CMOS technology
- Available in 28-pin DIP and PLCC packages

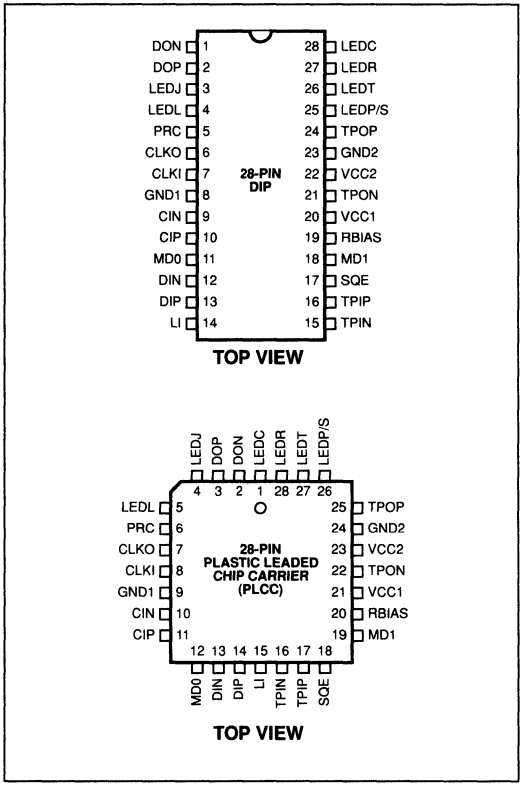
GENERAL DESCRIPTION

The MB86962 Twisted Pair Transceiver for Ethernet is fully compliant with the IEEE 802.3 10BASE-T specifications, and provides the electrical interface between the AUI (Attachment Unit Interface) and the twisted pair wiring. Functions provided by the MB86962 include level shifted data pass through from one transmission medium to another, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted pair input.

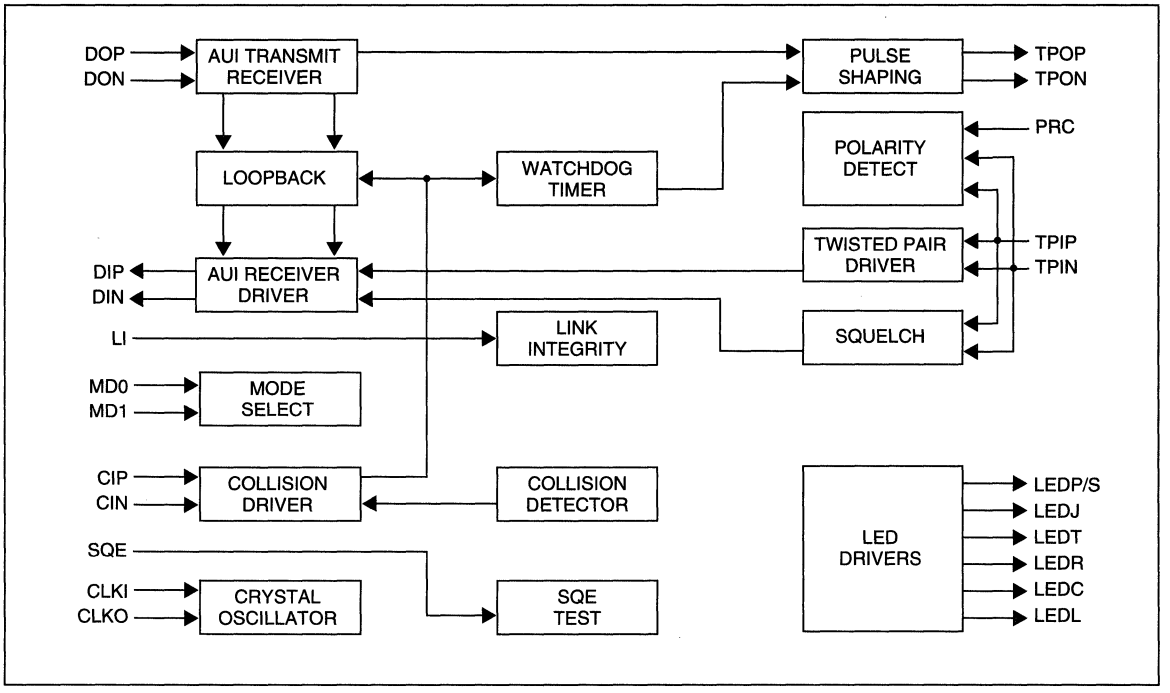
The transceiver uses a minimal number of external components and provides several unique features which make it an ideal device for both internal and external MAU (Medium Attachment Unit) applications. Its AUI/10BASE-T auto-sense circuity can automatically determine whether the local area network adapter is attached to an AUI cable or to twisted pair wiring, thus eliminating the need for jumpers to select between these two media. A high impedance AUI interface permits capacitive coupling to the external Manchester encoder/decoder, eliminating the isolation coupling transformer usually required at that interface. The receive threshold can be reduced to allow an extended range between nodes in low-noise environments. LED drivers are provided for transmit, receive, jabber, collision, link and reversed polarity indicators, or for a flashing status indicator.

The MB86962 is part of a complete family of Ethernet devices available from Fujitsu. It is fabricated in low-power CMOS technology and is available in 28-pin plastic DIP and PLCC packages.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING CODE

PACKAGE STYLE	TEMPERATURE RANGE	ORDERING CODE
28-Pin Plastic Dual In-Line	0 to +70°C	MB86962P-G
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	MB86962PD-G

SIGNAL DESCRIPTIONS[1]

SYMBOL	TYPE	DESCRIPTION
DON DOP	I	**DATA OUT NEGATIVE/POSITIVE:** Differential input pair connected to the AUI DO circuit.
LEDJ	I/O	**JABBER LED DRIVER:** Open drain driver for the Jabber indicator LED. Output goes active (low) when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function, blinking status indicator.
LEDL	O	**LINK LED DRIVER:** Open drain driver for the Link indicator LED. Output is active (low) except during Link Fail or when Link Integrity Test is disabled.
PRC	O	**POLARITY REVERSE CORRECTION:** The MB86962 automatically corrects reversed polarity at TPI when PRC is tied high. In Test mode, this pin is a 10 MHz output.
CLKO CLKI	-	**CRYSTAL OSCILLATOR:** The MB86962 requires either a 20 MHz crystal connected across these pins, or a 20 MHz clock applied at CLKI.
GND1 GND2	-	**GROUND.**
CIN CIP	O	**COLLISION NEGATIVE/POSITIVE:** Differential driver output pair tied to the collision presence pair of the Ethernet AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate that the transmit wire pair has been disabled.
MD0 MD1	I	**MODE SELECT:** Selects operating mode. MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
DIN DIP	O	**DATA IN NEGATIVE/POSITIVE:** Differential drive pair connected to the AUI DI circuit.
LI	I	**LINK INTEGRITY TEST ENABLE:** Link integrity testing is enabled when this pin is tied high. With link test enabled, the MB86962 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating that the receive wire pair is present in the absence of transmit traffic.
TPIN TPIP	I	**TWISTED PAIR RECEIVE INPUTS:** Differential receive inputs from the twisted pair input filter.
SQE	I/O	**SIGNAL QUALITY ERROR TEST ENABLE:** SQE is enabled when this pin is tied high. When enabled, the MB86962 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
RBIAS	-	**RESISTOR BIAS CONTROL:** Bias control pin for the operating circuit. Bias set by an external resistor to ground. External resistor value = 12.4KΩ ±1%.

MD1	MD0	MODE
0	0	10BASE-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
1	Clock	Test Mode, Jabber enabled
0	Clock	Test Mode, Jabber disabled

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

SIGNAL DESCRIPTIONS (CONTINUED)

SYMBOL	TYPE	DESCRIPTION
VCC1 VCC2	-	**+5 VOLT POWER SUPPLY.**
TPON TPOP	O	**TWISTED PAIR TRANSMIT OUTPUTS:** Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10BASE-T template.
LEDP/S	O	**POLARITY/STATUS LED DRIVER:** Open drain LED driver. In normal mode, LEDP/S is active (low) when reversed polarity is detected. If LEDJ is tied to ground, the output LEDP/S indicates multiple status conditions as shown in Figure 1. On solid = Normal, 1 blink = Link Down, 2 blinks = Jabber, 5 blinks = Polarity Reversed.
LEDT	O	**TRANSMIT LED DRIVER:** Open drain driver for the Transmit indicator LED. Output is active (low) during transmit.
LEDR	O	**RECEIVE LED DRIVER:** Open drain driver for the Receive indicator LED. Output is active (low) during receive from TPI.
LEDC	O	**COLLISION LED DRIVER:** Open drain driver for the Collision indicator LED. Output is active (low) during collision.

NOTE: I = Standard input
O = Standard output
I/O = Input or output

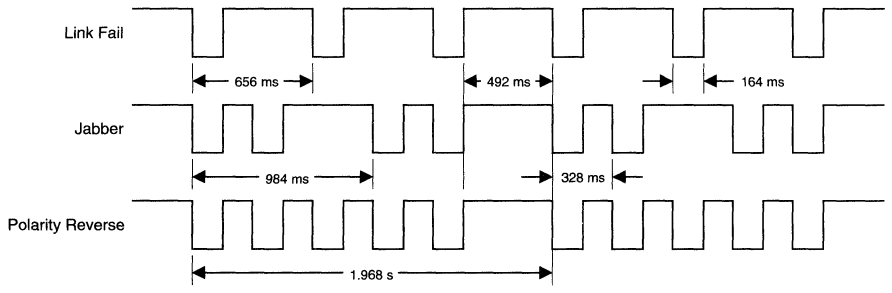
APPLICATIONS

Figure 2 shows the MB86962 in a typical external MAU application, interfacing between an AUI and the RJ45 connector of the twisted pair network. Figure 3 is the connection diagram for this application. A 20 MHz crystal or ceramic resonator connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of these filters are shown in Figures 4 and 5, respectively. (Differential filters are also recommended).

Figures 6 and 7 show an internal MAU application which takes advantage of the MB86962's unique AUI/10BASE-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10BASE-T). No termination resistors are used on the MB86962 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling.

MD1 is tied high so MD0 functions as the mode control switch. When MD0 is low, the half current drive mode is selected. When MD0 is high the MB86962 is effectively removed from the circuit. The transceiver's AUI ports (DO, DI and CI) are disabled, isolating the MB86962 from the AUI. The MB86962 DI and CI ports go to a high impedance state and the DO port is ignored.

To implement an auto-select function, LEDL can be tied to MD0. This activates the transceiver/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.



Note: LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity conditions are reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

Figure 1. LEDP/S Status indication Timing

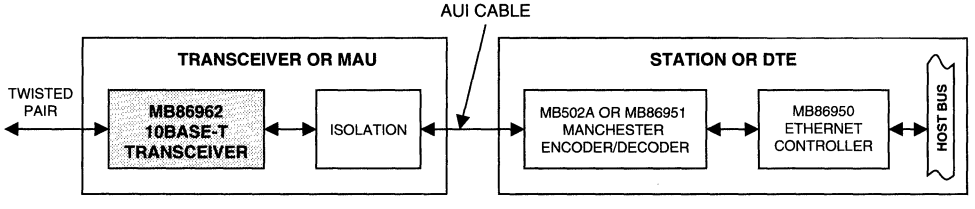
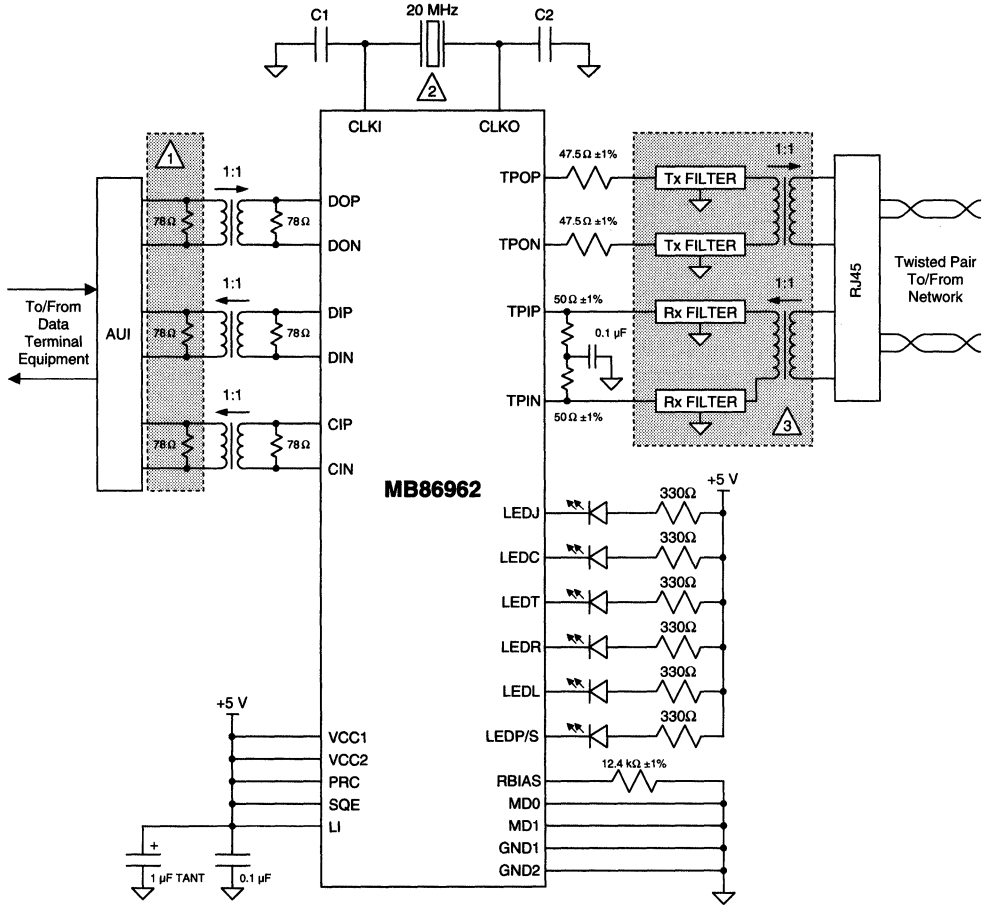


Figure 2. Typical System Diagram for External MAU



1 Typically, resistors on the AUI side of the transformer are already present in the terminal. If termination resistors are present in the terminal, these resistors are not required.

2 A 20 MHz (±1%) crystal or ceramic resonator may be used at CLKI/CLKO.

3 Suitable integrated filter/transformers include Pulse Engineering PE65421, FILMAG 781120B and Valor PT3877

Figure 3. Connection Diagram for External MAU

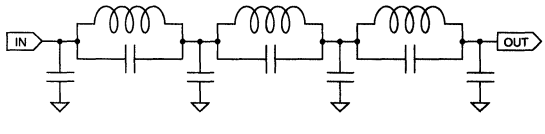


Figure 4. Transmit Filter Diagram

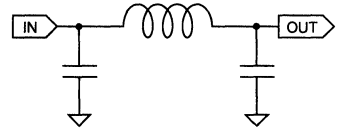


Figure 5. Receive Filter Diagram

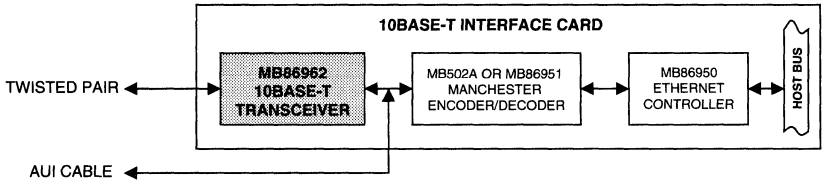


Figure 6. Typical System Diagram for Internal MAU

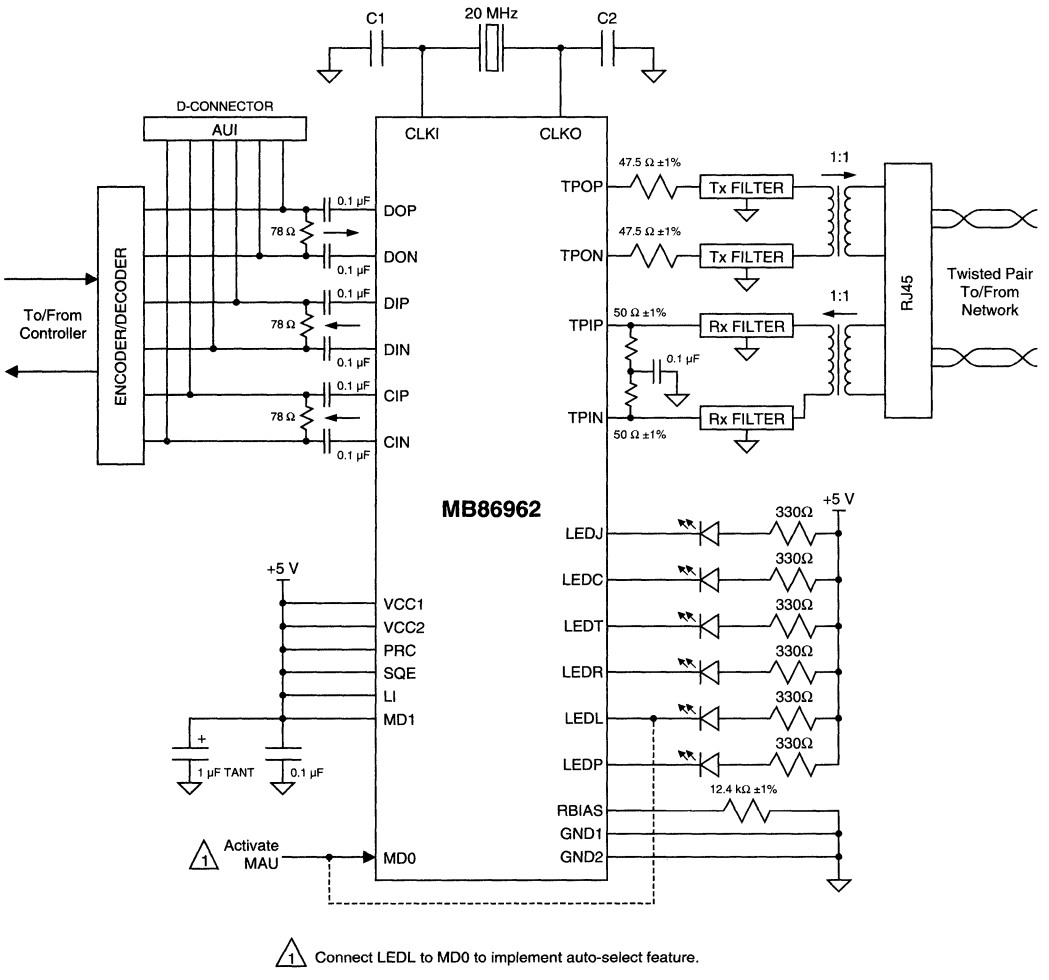


Figure 7. Connection Diagram for Internal MAU

FUNCTIONAL DESCRIPTION

The MB86962 interfaces the Attachment Unit Interface (AUI) to the unshielded twisted pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the MB86962 contains an internal crystal oscillator, separate power and ground pins for analog and digital circuits, various logic controls and six LED drivers for status indications.

Functions are defined from the AUI side of the interface. The Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted pair network. In addition to basic transmit and receive functions, the transceiver performs all required MAU functions defined by the IEEE 802.3 10BASE-T specifications such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

Several options are controlled by the MD0 and MD1 transceiver inputs. See Table 1 for a description of these functions.

TRANSMIT FUNCTION

The MB86962 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10BASE-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 8. If the differential inputs at the DO circuit fall below 75% of the threshold level for eight bit times (typical), the MB86962 transmit function will enter the idle state. During idle periods, the MB86962 transmits link integrity test pulses on the TPO circuit.

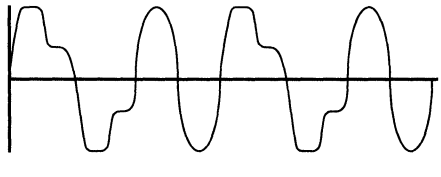


Figure 8. TPO Output Waveform

RECEIVE FUNCTION

The MB86962 receive function transfers serial data from the twisted pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for eight bit times (typical), the MB86962 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1=0 and MD0=1.

POLARITY REVERSE FUNCTION

The MB86962 polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the MB86962 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses).

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The MB86962 reports collisions to the AUI by sending a 10 MHz (CS0) signal over the CI circuit. The collision report signal is output no more than nine bit times after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO

Table 1. Mode Select Options

MD1	MD0	MODE
0	0	10BASE-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
Clock	0	Test Mode, Jabber enabled
Clock	1	Test Mode, Jabber disabled

circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 9 is a state diagram of the MB86962 collision detection function (refer to IEEE 802.3 10BASE-T specification).

LOOPBACK FUNCTION

The loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the transceiver from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE TEST FUNCTION

Figure 10 is a state diagram of the SQE test function. The SQE test function is enabled when the SQE pin is tied high. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10BASE-T network. When a successful transmission is completed, the MB86962 transmits the SQE signal to the AUI over the CI circuit for 10±5 bit times. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

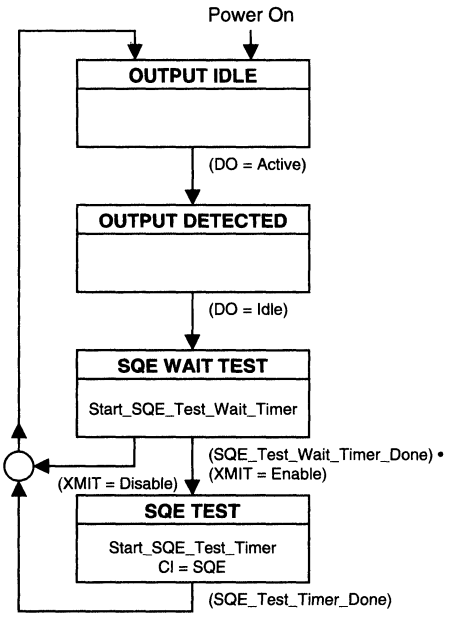


Figure 10. SQE Test Function

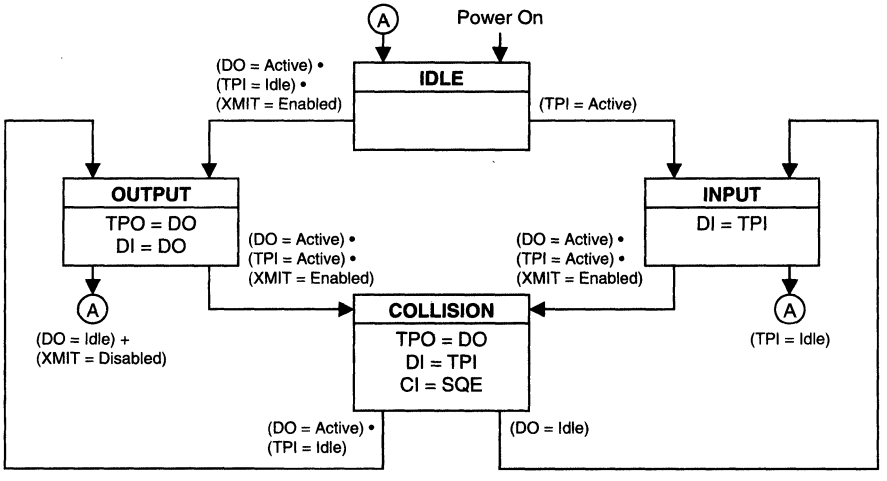


Figure 9. Collision Detection Function

JABBER CONTROL FUNCTION

Figure 11 is the state diagram for the MB86962 jabber control function. The MB86962 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the transceiver is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

LINK INTEGRITY TEST FUNCTION

Figure 12 is the state diagram of the MB86962 link integrity test function. The link integrity test is used to determine the status of the receive side twisted pair cable and is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 to 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The MB86962 ignores any link integrity pulse with an interval less than 2 to 7 ms. The MB86962 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

TEST MODE

The MB86962 test mode is selected when a 2 to 2.5 MHz clock is input on the MD1 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, link integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD0=1.

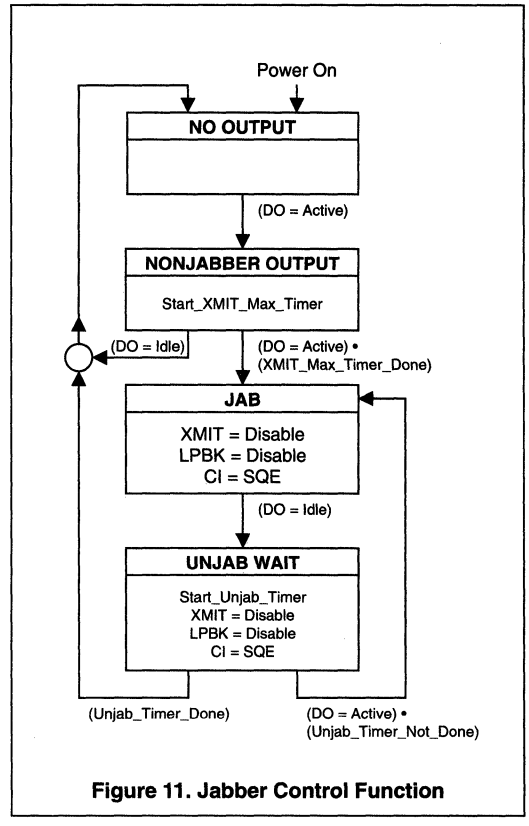


Figure 11. Jabber Control Function

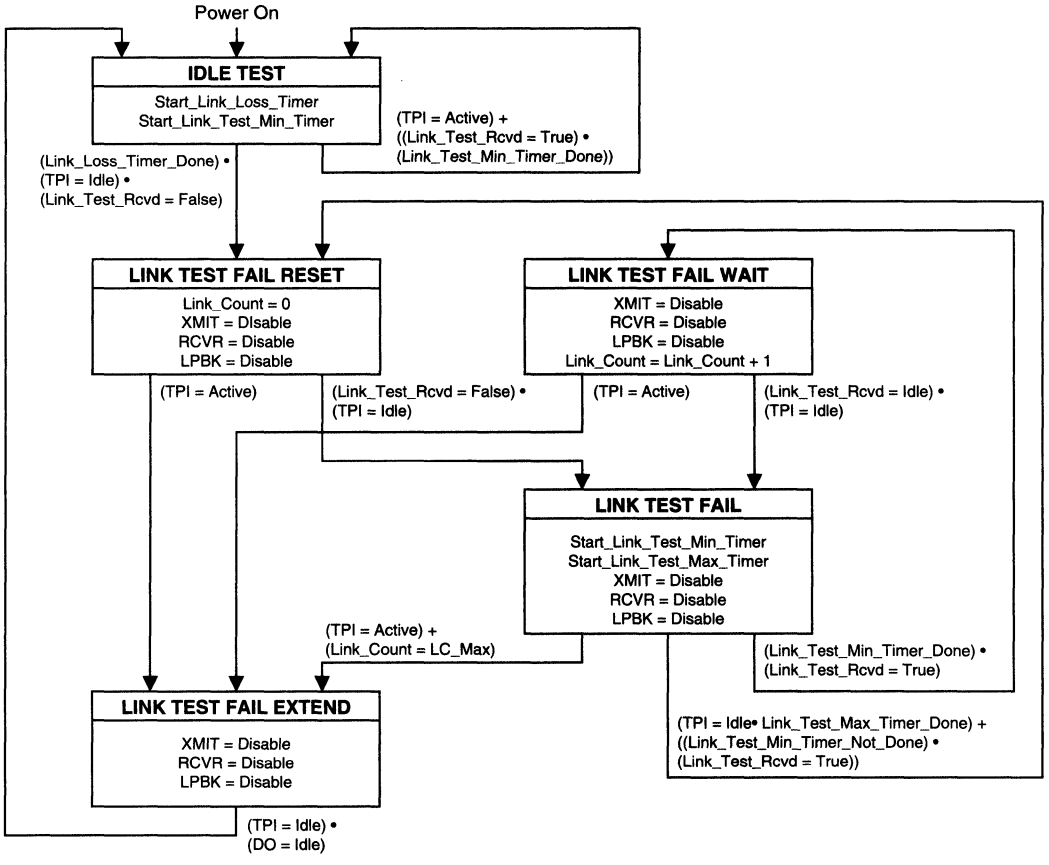


Figure 12. Link Integrity Test Function

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.3	6	V
V_I	Input voltage[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		-65	150	°C

I/O DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage[6]		-	-	0.8	V
V_{IH}	Input high voltage[6]		2.0	-	-	V
V_{OL}	Output low voltage (Open Drain LED Driver)[7]	R_{LOAD} = 2k Ω	-	-	0.13	V
I_{CC}	Power supply current (V_{CC1} = V_{CC2} = 5.25V)	Line Idle	-	60	69.3	mA
		Line Active, transmitting all ones	-	125	140	mA
I_{LI}	Input leakage current[8]	Input between V_{CC} and GND	-	±1	±10	µA
I_{LZ}	3-state leakage current	Output between V_{CC} and GND	-	±1	±10	µA

AUI DC SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input low current		-	-	-700	µA
I_{IH}	Input high current		-	-	500	µA
V_{OD}	Differential output voltage		±550	-	±1200	mV
V_{OB}	Differential voltage imbalance		-	-	±40	mV
V_{DS}	Differential squelch threshold		-	220	-	mV
R_Z	Receive input impedance	Between DOP and DON	-	20	-	kΩ

TRANSMIT SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{OUT}	Transmit output impedance		-	5	-	Ω
V_{OD}	Peak differential output voltage	Load = 200 Ω at TPOP and TPON	±4.5	-	±5.2	V
V_{OB}	Differential voltage imbalance	Load = 200 Ω at TPOP and TPON	-	-	±40	mV
t_{TTJ}	Transmit timing jitter addition	After Tx filter, 0 line length[9]	-	-	±8	ns
		After Tx filter, line model as shown in 10BASE-T draft #10[9]	-	-	±3.5	ns

RECEIVE SPECIFICATIONS T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{IN}	Receive input impedance	Between TPIP/TPIN	-	20	-	kΩ
V_{DS}	Differential squelch threshold		-	420	-	mV
V_{DSR}	Reduced squelch threshold		-	300	-	mV
t_{RTJ}	Receive timing jitter[9]		-	-	1.5	ns

JABBER TIMING T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Maximum transmit time[5]	98.5	-	131	ms
t_2	Unjab time[5]	491	-	525	ms
t_3	Time from Jabber to CS0 on CIP/CIN[9]	0	-	900	ns

LINK INTEGRITY TIMING T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Time link loss[5]	65	-	66	ms
t_2	Time between Link Integrity Pulses[5]	9	-	11	ms
t_3	Interval for valid receive Link Integrity Pulses[5]	4.1	-	65	ms

COLLISION TIMING T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Simultaneous TPI/TPO to CS0 state on CIN/CIP	0	-	900	ns
t_2	DO loopback to TPI on DI	300	-	900	ns
t_3	CS0 state delay after TPI/DO idle	-	-	900	ns
t_3	CS0 high pulse width	40	-	60	ns
t_3	CS0 low pulse width	40	-	60	ns
t_3	CS0 frequency	-	10	-	MHz

SQE TIMING T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	SQE signal duration	500	-	1500	ns
t_2	Delay after last positive transition	0.6	-	1.6	µs

LED TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

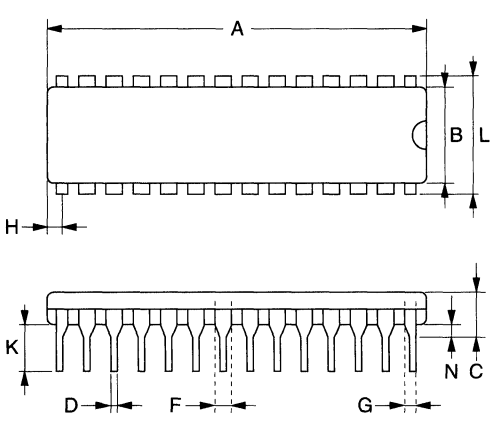
Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	LEDC, LEDT, LEDR on time[5]	100	-	-	ms
t_2	LEDP/S on time[5] (See Figure 1)	-	164	-	ms
t_2	LEDP/S period[5] (See Figure 1)	-	328	-	ms

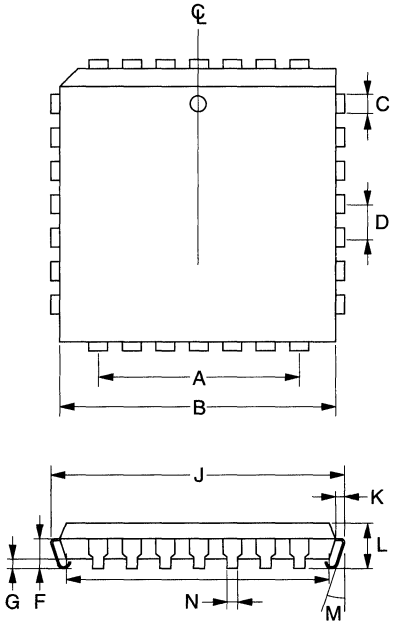
GENERAL TIMING T_A = 0°C to +70°C, V_{CC} = 5V ± 5%[3,4]

Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_1	Receive start-up delay	0	-	500	ns
t_2	Transmit start-up delay	0	-	200	ns
t_2	Loopback start-up delay	0	-	500	ns

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted. Typical parameters are at 25°C and are for design aid only.
4. Maximum voltage differential between V_{CC1} and V_{CC2} must not exceed 0.3 V.
5. Switching times reduced by a factor of 1024 in test mode.
6. Applies to MD0, MD1, SQE, PRC and LI pins.
7. LED drivers can sink up to 10 mA.
8. Not including TPIN, TPIP, DOP or DON.
9. This parameter is not production tested, but is guaranteed by design.





Dual In-Line Plastic Case

- Part Number MB86962P-G
- commercial temp. range
- 28 pin DIP

Dim.	Min.	Max.
A	1.440	1.470
B	.500	.550
C	.140	.160
D	.015	.023
F	.040	.065
G	.090	.110
H	.065	.085
J	.008	.015
K	.125	.150
L	.590	.610
M	0°	15°
N	.015	.035

Dimensions in inches

Plastic Leaded Chip Carrier

- Part Number MB86962PD-G
- commercial temp. range
- 28 pin PLCC

Dim.	Min.	Max.
A	.290	.310
B	.450	.460
C	.026	.036
D	.048	.052
F	.090	.120
G	.020	.030
H	.390	.430
J	.485	.495
K	.018	.022
L	.160	.185
M	0°	15°
N	.013	.021

Dimensions in inches

Package Dimensions

MBL8392A

FUJITSU

COAXIAL TRANSCEIVER INTERFACE FOR ETHERNET/THIN ETHERNET

DATA SHEET

APRIL1993

FEATURES

- Compatible with Ethernet II, IEEE 802.3 10BASE5 and 10BASE2, and ISO 8802/-3 interface specifications
- Integrates all active transceiver electronics
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection
- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP and 28-pin PLCC with special lead frames to minimize the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up

GENERAL DESCRIPTION

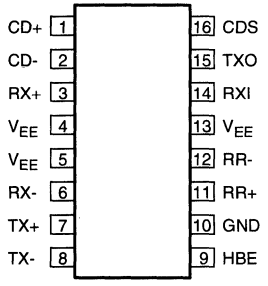
The MBL8392A Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10BASE5) and Thin Ethernet (10BASE2) local area networks. The CTI is part of a three chip set available from Fujitsu that fully implements IEEE 802.3 Ethernet specifications, as shown in the system diagram. The other chip is either the MB8696 NICE™ Ethernet controller or the MB8696S Ether Complexer. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50 Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer as shown in Figure 1.

During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heart- beat function can be disabled for repeater applications.

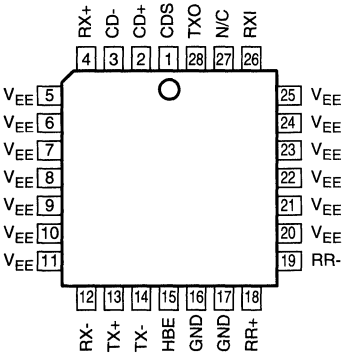
PIN CONFIGURATION

TOP VIEW

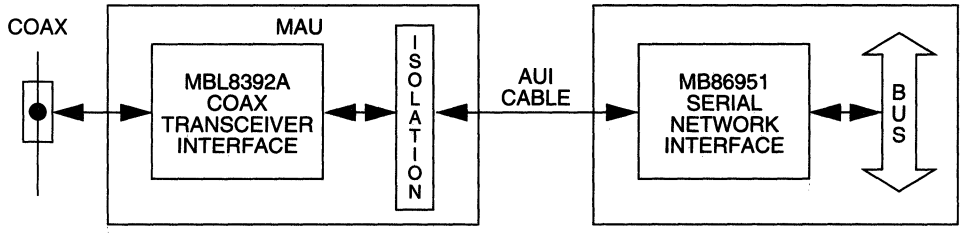
DIP PACKAGE



PLCC PACKAGE

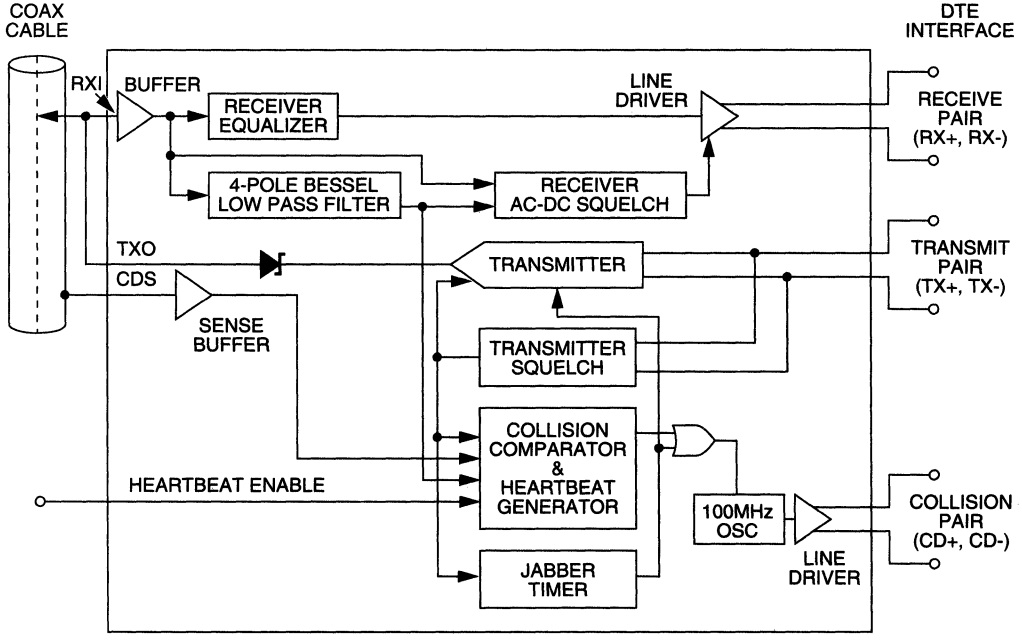


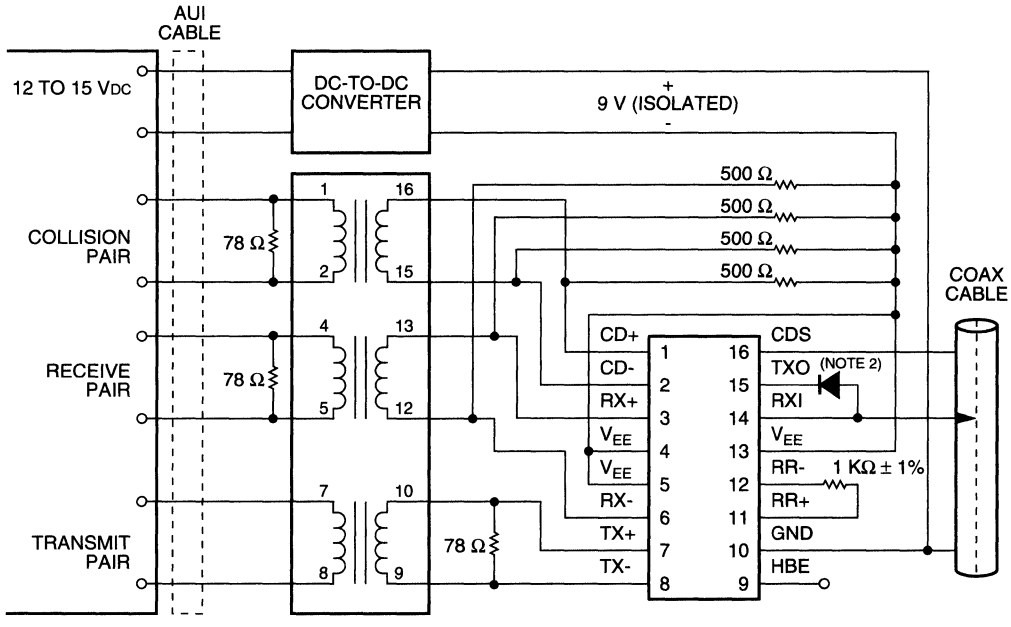
SYSTEM DIAGRAM



MAU = MEDIUM ATTACHMENT UNIT
AUI CABLE = ATTACHMENT UNIT INTERFACE CABLE (NOT USED IN THIN ETHERNET APPLICATONS)

BLOCK DIAGRAM





NOTES:
1. T1 IS A 1:1 PULSE TRANSFORMER, WITH AN INDUCTANCE OF 30 TO 150 μH.
2. 1N916 OR EQUIVALENT FOR ETHERNET, NOT REQUIRED FOR THIN ETHERNET.

Figure 1. Connection Diagram

PIN DESCRIPTIONS

PIN NO		SYMBOL	TYPE	DESCRIPTION
DIP	PLCC			
1 2	2 3	CD+ CD-	O	**COLLISION OUTPUTS:** Balanced differential line driver outputs which send a 10 MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX-	O	**RECEIVER OUTPUTS:** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX-	I	**TRANSMITTER INPUTS:** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	I	**HEARTBEAT ENABLE:** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR-		**EXTERNAL RESISTOR:** A 1 KΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR- is internally connected to V_{EE}.
14	26	RXI	I	**RECEIVER INPUT:** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.

PIN DESCRIPTIONS

PIN NO		SYMBOL	TYPE	DESCRIPTION
DIP	PLCC			
15	28	TXO	O	**TRANSMITTER OUTPUT:** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	I	**COLLISION DETECT SENSE:** Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16,17	GND	—	**POSITIVE SUPPLY PIN**
4, 5, 13	5 to 11 20 to 25	V_{EE}	—	**NEGATIVE SUPPLY PINS:** These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to 70°C	MBL8392AP-G
28-Pin PLCC	0 to 70°C	MBL8392APD-G

FUNCTIONAL DESCRIPTION

The MBL8392A, as illustrated in the block diagram, contains four main functional blocks. These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTF any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

RECEIVER FUNCTIONS

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500 ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250 ns and only enables the receiver again after approximately 1 µs. Receiver timing is shown in Figures 2 and 4.

The differential line driver provides typically ±900 mV signals to the DTE with less than 7 ns rise and fall times. When in idle state (no received signal) its

outputs provide less than 20 mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78 Ω transmission line, require 500 Ω pull-down resistors to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistors can be increased to 1.5 KΩ to reduce power consumption.

TRANSMITTER FUNCTIONS

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25 ns (±5 ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2 ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the MBL8392A meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225 mV in magnitude and 15 ns in duration. The transmitter will

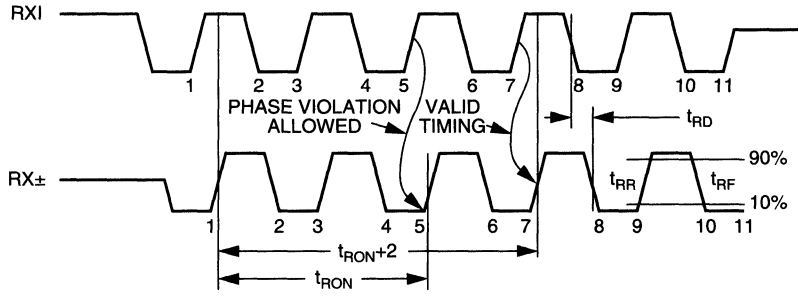


Figure 2. Receiver Timing

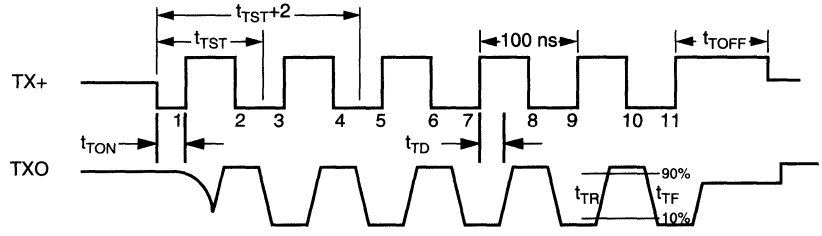


Figure 3. Transmitter Timing

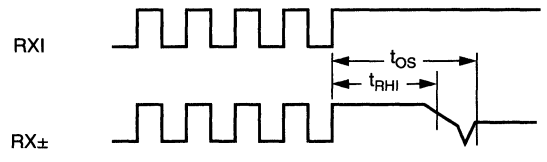


Figure 4. Receiver End-of-Packet Timing

be disabled at the end of a packet if there are no negative-going signals of greater than 225 mV for more than typically 250 ns, as shown in Figure 3.

COLLISION FUNCTIONS

The collision detection scheme implemented in the MBL8392A is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and nonrepeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10 MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10 MHz oscillation signal at the CD outputs and typically occurs within 700 ns of the onset of the collision. The collision signal begins with a negative going pulse and ends with a continuous high-to-idle state longer than 170 ns. Figure 5 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. The pseudo collision consists of a 1 µs burst of 10 MHz oscillation at the line driver outputs approximately 1 µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) input to V_{EE}. This allows the CTI to be used in repeater applications. Figure 6 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require pull down resistors to V_{EE} and maintain less than 20 mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

JABBER FUNCTIONS

The jabber timer monitors the transmitter and inhibits its transmission if it is active for longer than typically 30 ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450 ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 7 illustrates jabber timing.

DETECTION OF COAXIAL CABLE FAULTS

In the MBL8392A there is no internal loopback path from the TX inputs to the RX outputs. This means that when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX- if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of -1.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50 Ω, depending on the distance of the CTI from the fault. The upper limit of 50 Ω results from the fact that the coaxial cable is terminated in 50 Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.

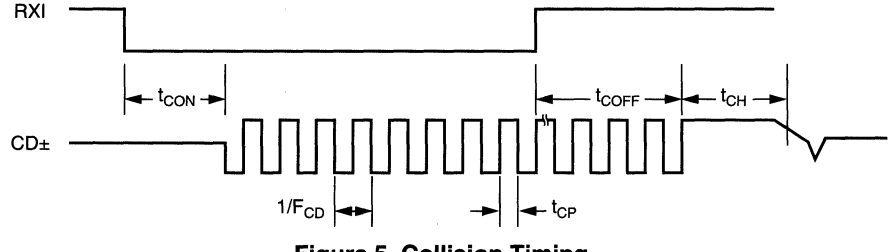


Figure 5. Collision Timing

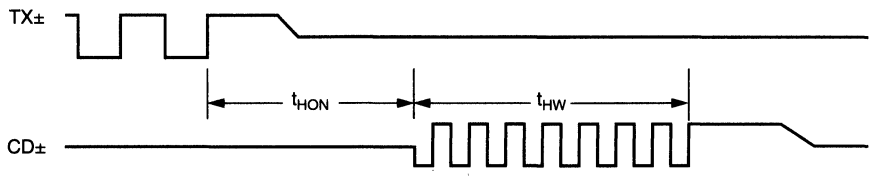


Figure 6. Heartbeat Timing

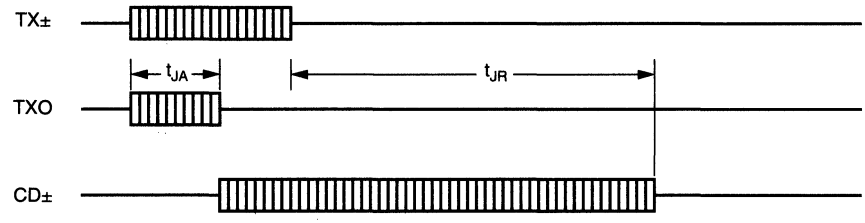


Figure 7. Jabber Timing

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Units
V_{EE}	Supply Voltage[2]	-12	V
V_{IN}	DC Input Voltage[2]	0 to -12	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOLD}	Lead Soldering Temperature (10 sec.)	+300	°C
T_J	Recommended Max Junction Temperature[3]	+130	°C
θ_{JA}	Thermal Impedance (PDIP and PLCC Packages)	60	°C/W

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. 100% measured in production.
3. The junction temperature is calculated from the following expression:
   $T_J = T_A + \theta_{JA} [V_{EE} (0.075 + n \times 0.05/100) + 8 (V_{EE} - 2) / R]$
   where
   T_A = Ambient temperature in °C
   θ_{JA} = Thermal resistance of package.
   V_{EE} = Normal operating supply voltage in volts.
   n = Percentage transmitter duty cycle.
   R = Pull down resistors on the RX and CD pins in ohms

The PDIP package is specially designed to have a low θ_{JA} by directly connecting the four center pins 4, 5,12, and 13 to the die attachment area These tour pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the PLCC package, pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} track.

DC SPECIFICATIONS

V_{EE} = -9V ±5% T_A = 0 to +70°C unless otherwise specified [1,2]. No external isolation diode on TXO.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power-on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			-6.5		V
I_{EE}	Supply current non-transmitting			-80	-130	mA
	Supply current transmitting			-125	-180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	-2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = VEE		-500	-1000	µA
I_{TDC}	Transmit output DC current level [3]		-37		-45	mA
I_{TAC}	Transmit output AC current level [3]		±28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	V_{TXO} = -10V	-250		+250	µA
V_{TCOM}	Transmitter output voltage compliance [4]				-3.7	V
V_{CD}	Collision threshold [5]	Measured by applying DC voltage at RXI	-1450	-1530	-1580	mV
V_{OD}	Differential output voltage - non idle at RX± and CD± [6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance - idle at RX± and CD± [7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±		-1.5	-2	-2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	-130	-250	-370	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} - V_{TX-}) peak	-175	-225	-300	mV
R_{RXI}	Shunt resistance at RXI non-transmitting		100			kΩ
C_{RXI}	Input Capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

Notes:

1. Currents flowing into device pins are positive All voltages are referenced to ground unless otherwise specified For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = -9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN}) / (2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TX0 with a 25 Ω load between TXO and GND.I_{TAC} is measured as (V_{MAX} - V_{MIN}) / (2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is -3.7 V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer as shown in the connection diagram, Figure 1 The transformer has a 1:1 turn ratio with an inductance between 30 and 100 µH at 5 MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = -9V ±5% T_A = 0 to +70°C unless otherwise specified [1]. No external isolation diode on TXO.

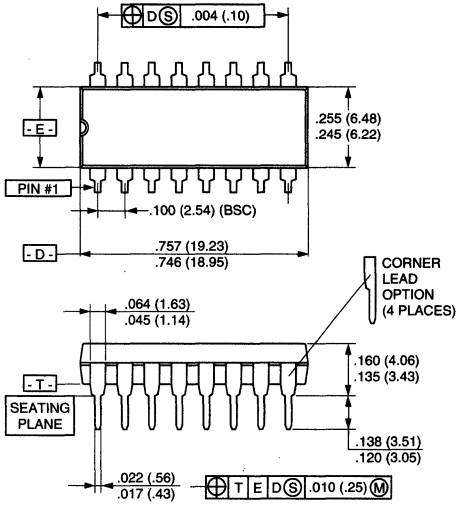
Symbol*	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{RON}(2)$	Receiver start up delay RXI to RX±: First received bit on RX±	V_{RXI} = -2V peak			5	bits
	First validly timed bit on RX±				t_{RON}+2	bits
$t_{RD}(2)$	Receiver prop. delay RXI to RXI±	V_{RXI} = -2V peak		35	50	ns
$t_{RR}(2)$	Differential output rise time on RX± and CD± [2,3]			5		ns
$t_{RF}(2)$	Differential output fall time on RX± and CD± [2,3]			5		ns
$t_{OS}(4)$	Differential output settling time on RX± and CD± to V_{OB} = 40 mV [2]			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
$t_{RHI}(4)$	Receiver high to idle time	Measured to +210 mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	t_{RF} - t_{RR}		0.4		ns
$t_{TST}(3)$	Transmitter start-up delay TX± to TXO First transmitted bit on TXO	$V_{TX±}$ = -1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
$t_{TD}(3)$	Transmitter prop delay TX± to TXO	$V_{TX±}$ = 1V peak		35	50	ns
$t_{TR}(3)$	Transmitter rise time 10% to 90%			25		ns
$t_{TF}(3)$	Transmitter fall time 10% to 90%			25		ns
t_{TM}	t_{TF} - t_{TR} mismatch			±2		ns
t_{TS}	Transmitter added skew [4]			±2		ns
$t_{TON}(3)$	Transmitter turn on pulse width	$V_{TX±}$ = 1V peak	10		40	ns
$t_{TOFF}(3)$	Transmitter turn off pulse width	$V_{TX±}$ = 1V peak	150	250	340	ns
$t_{CON}(5)$	Collision turn on delay	0V to -2V step at RXI			13	bits
$t_{COFF}(5)$	Collision turn off delay	-2V to 0V step at RXI			16	bits
$t_{CHI}(5)$	Collision high to idle time	Measured to +210 mV	150		850	ns
$f_{CD}(5)$	Collision frequency		8.0	10	12.5	MHz
$t_{CP}(5)$	Collision signal pulse width		35		70	ns
$t_{HON}(6)$	Heartbeat turn on delay		0.6		1.6	µs
$t_{HW}(6)$	Heartbeat test duration		0.5		1.5	µs
$t_{JA}(7)$	Jabber activation delay measured from TX± to CD±		20		60	ms
$t_{JR}(7)$	Jabber reset delay measured from TX± to CD±		250		750	ms

*** Numbers in parentheses indicate figure reference.**

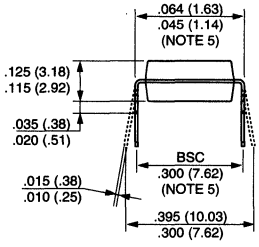
Notes:

1. All typicals are for V_{EE} = -9V and T_A=27°C
2. Measured on secondary side of isolation transformer as shown in the connection diagram, Figure 1. The transformer has a 1:1 turn ratio with an inductance between 30 and 100 µH at 5 MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from -225 mV to +225 mV, or +225 mV to -225 mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

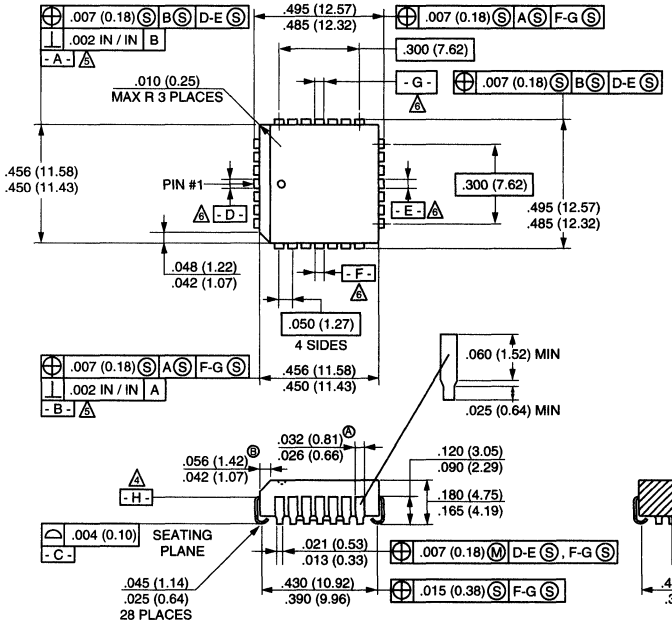
16-PIN PLASTIC DUAL IN-LINE



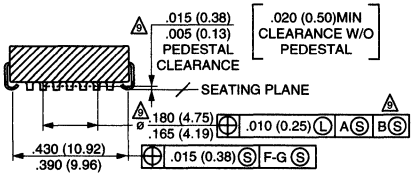
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85).
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm).
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwiseto pin #16 when viewed from the top.



28-PIN PLCC



NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB.
2. Controlling dimension: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. Datum plane -H- located at the top of mold parting line and coincident with top of lead where lead exits plastic body.
5. Location to datum -A- and -B- to be determined at plane -H-. These datum do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum D-E and F-G are determined where these center leads exit from the body at plane -H-.
7. Pin numbers continue counterclockwise to pin 28 (top view).
8. Fujitsu order code for product packaged PLCC is the suffix "PD".
9. Applicable to packages with pedestal only.



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