October 1993
Edition 1.0

FUJITSU

DATA SHEET

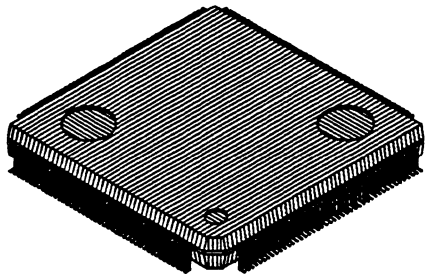
MB86683
Network Termination Controller (NTC)

Network Termination Controller

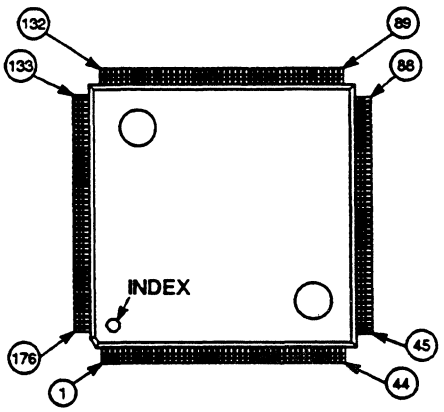
The FUJITSU MB86683 is a highly integrated termination controller for broadband ATM networks. It is designed to implement transmission convergence functions associated with physical media based on SONET,SDH, DS3, E3 and cell based protocols. The device includes a generic 8-bit parallel interface to an external transceiver, which is required only to provide serial / parallel conversion, and clock recovery.

The NTC is ideally suited to applications in ATM adapter cards and hubs. It can be used for UNI or NNI applications and conforms to the relevant CCITT, ANSI and ATM Forum specifications.

PLASTIC PACKAGE
SQFP-176



PIN ASSIGNMENT



FEATURES

- Implements TC sublayer functions associated with physical media based on SONET(SDH), DS3, E3 and cell based.
- Directly connects to external transceivers via a 20MHz 8-bit parallel interface.
- Implements framed and cell based physical layer OAM (PL-OAM) functions for F1, F2 and F3 flows.
- Supports F4/F5 OAM cell insertion / extraction.
- Maintains statistics for all active virtual circuits, including cell and error counts, and OAM statistics.
- Terminates serial switch statistics information provided by the MB86680 Self Routing switch Element (SRE).
- Includes an on-chip DMA controller for high speed transfer of statistics and inserted / extracted cells to/from system memory.
- Connects directly to the MB86689 Address Translation Controller (ATC) in order to provide real-time address translation in both directions.
- Microprocessor interface compatible with Motorola and Intel families of 16 and 32 bit processor.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

LIST OF FIGURES

AC TIMINGS

1. OVERVIEW

1.1. General

The NTC is a full duplex device which can be used to provide broadband termination functions in a variety of applications. Its primary use is for terminating the user or network ends of a user-network interface based in CCITT, ANSI, or ATM Forum UNI standards. Address translation functions, in conjunction with the MB86689 ATC, allows full flexibility for changing VPI and VCI values at either end of the link, and allows a 24 bit routing tag to be appended and removed. At the user end of a UNI connection, the address translation functions allow any incoming VPI / VCI combination to be mapped onto one of 1024 virtual connections supported by the Adaptation Layer Controller (MB86686). At the network end, address translation allows cell headers to be replaced with VPI and VCI values associated with the outgoing link, and routed to the appropriate output port by means of a routing tag.

Address translation can also be performed on the outgoing link of a network connection. This function may be required, for example, to replace outgoing multicast VPI/VCI values.
Some example system configurations are illustrated in Fig. 1

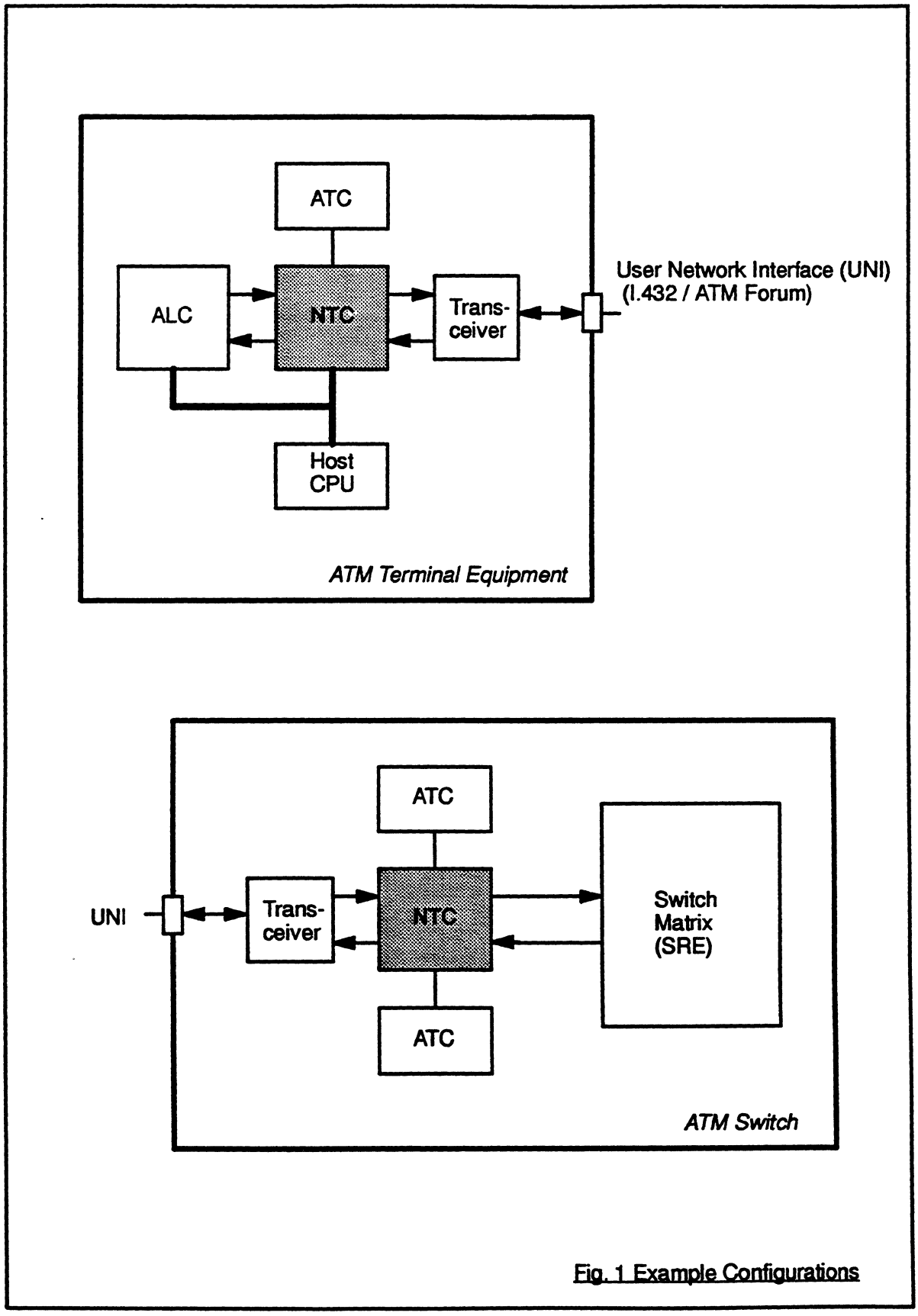


Fig. 1 Example Configurations

2. PIN DESCRIPTION

2.1. Logical Outline

A logical view of the NTC's external pins is illustrated in Fig. 2 below, and a physical pin assignment diagram is shown in Fig. 3.

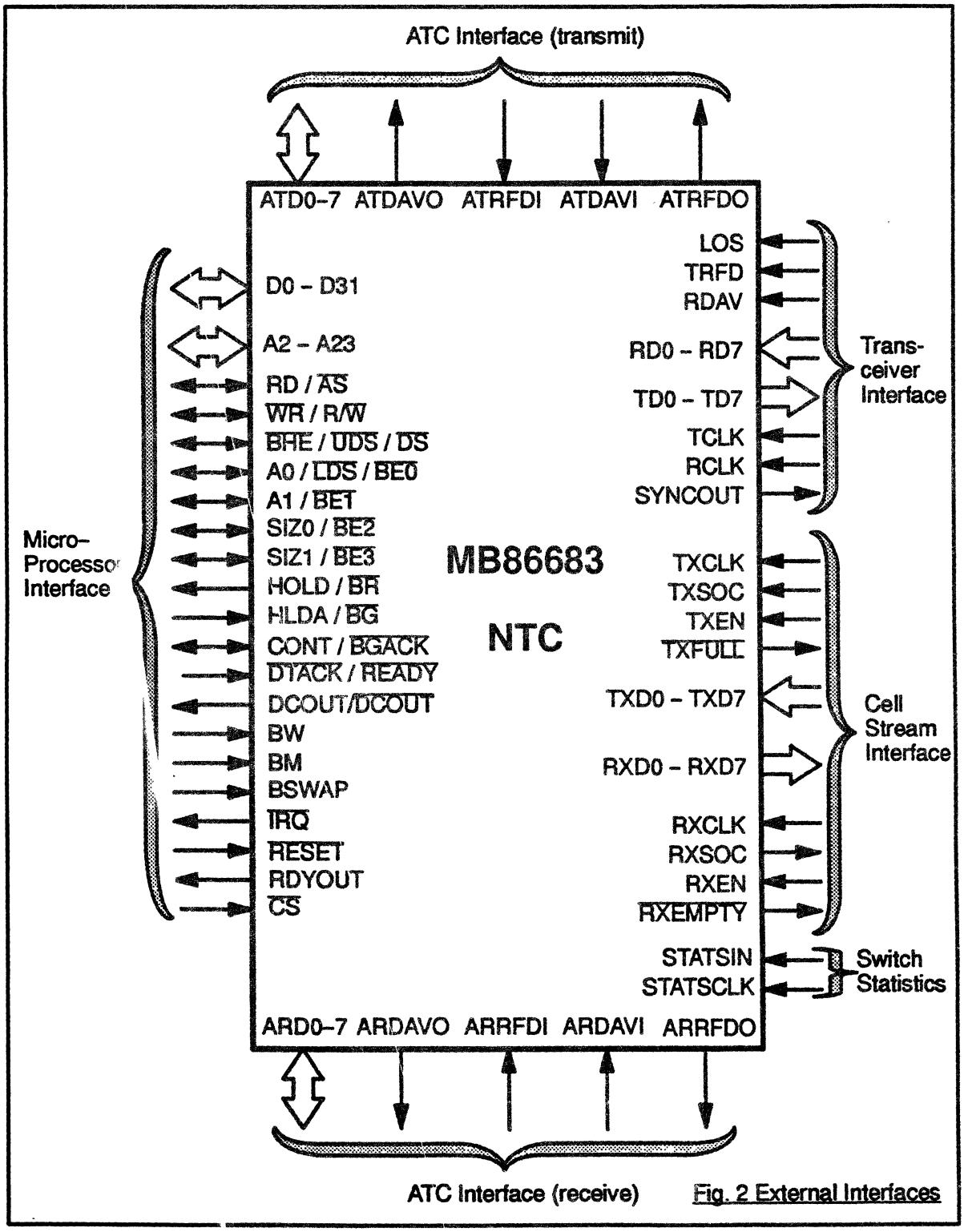


Fig. 2 External Interfaces

2.2. Pin Assignment

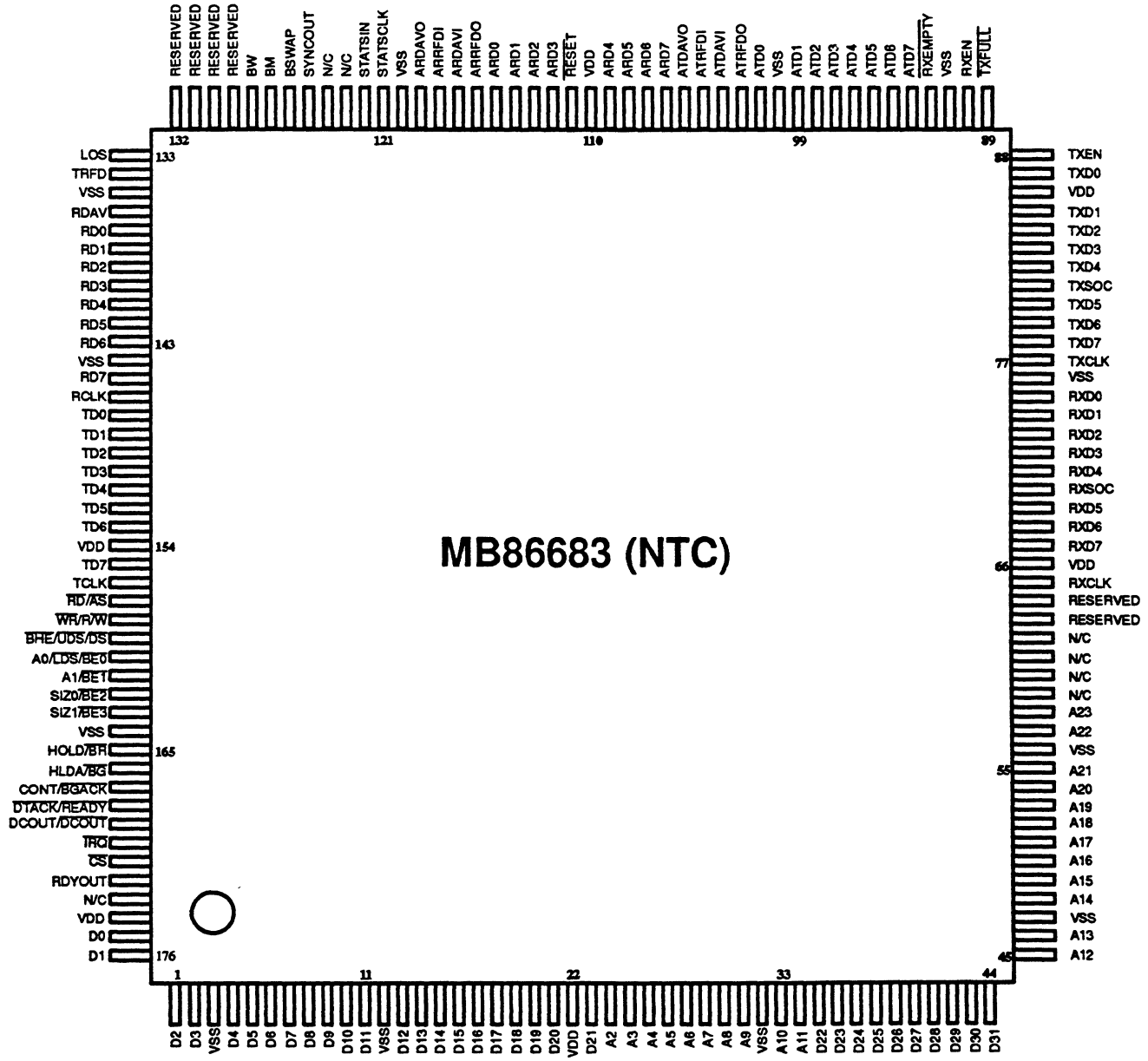


Fig. 3 NTC Pin Assignment

Pin No	Name	Type	Function
1	D2	I/O	Microprocessor data bus bit D2
2	D3	I/O	Microprocessor data bus bit D3
3	VSS	-	
4	D4	I/O	Microprocessor data bus bit D4
5	D5	I/O	Microprocessor data bus bit D5
6	D6	I/O	Microprocessor data bus bit D6
7	D7	I/O	Microprocessor data bus bit D7
8	D8	I/O	Microprocessor data bus bit D8
9	D9	I/O	Microprocessor data bus bit D9
10	D10	I/O	Microprocessor data bus bit D10
11	D11	I/O	Microprocessor data bus bit D11
12	VSS	-	
13	D12	I/O	Microprocessor data bus bit D12
14	D13	I/O	Microprocessor data bus bit D13
15	D14	I/O	Microprocessor data bus bit D14
16	D15	I/O	Microprocessor data bus bit D15
17	D16	I/O	Microprocessor data bus bit D16
18	D17	I/O	Microprocessor data bus bit D17
19	D18	I/O	Microprocessor data bus bit D18
20	D19	I/O	Microprocessor data bus bit D19
21	D20	I/O	Microprocessor data bus bit D20
22	VDD	-	
23	D21	I/O	Microprocessor data bus bit D21
24	A2	I/O	Microprocessor address bus bit A2
25	A3	I/O	Microprocessor address bus bit A3
26	A4	I/O	Microprocessor address bus bit A4
27	A5	I/O	Microprocessor address bus bit A5
28	A6	I/O	Microprocessor address bus bit A6
29	A7	O	Microprocessor address bus bit A7
30	A8	O	Microprocessor address bus bit A8
31	A9	O	Microprocessor address bus bit A9
32	VSS	-	
33	A10	O	Microprocessor address bus bit A10
34	A11	O	Microprocessor address bus bit A11
35	D22	I/O	Microprocessor data bus bit D22
36	D23	I/O	Microprocessor data bus bit D23
37	D24	I/O	Microprocessor data bus bit D24
38	D25	I/O	Microprocessor data bus bit D25
39	D26	I/O	Microprocessor data bus bit D26
40	D27	I/O	Microprocessor data bus bit D27
41	D28	I/O	Microprocessor data bus bit D28
42	D29	I/O	Microprocessor data bus bit D29
43	D30	I/O	Microprocessor data bus bit D30
44	D31	I/O	Microprocessor data bus bit D31

Pin No	Name	Type	Function
45	A12	O	Microprocessor address bus bit A12
46	A13	O	Microprocessor address bus bit A13
47	VSS	-	
48	A14	O	Microprocessor address bus bit A14
49	A15	O	Microprocessor address bus bit A15
50	A16	O	Microprocessor address bus bit A16
51	A17	O	Microprocessor address bus bit A17
52	A18	O	Microprocessor address bus bit A18
53	A19	O	Microprocessor address bus bit A19
54	A20	O	Microprocessor address bus bit A20
55	A21	O	Microprocessor address bus bit A21
56	VSS	-	
57	A22	O	Microprocessor address bus bit A22
58	A23	O	Microprocessor address bus bit A23
59	N/C	-	Not Connected
60	N/C	-	Not Connected
61	N/C	-	Not Connected
62	N/C	-	Not Connected
63	RESERVED	-	Reserved, should not be connected.
64	RESERVED	-	Reserved, should be connected to VSS
65	RXCLK	I	Cell stream receive clock (also system clock)
66	VDD	-	
67	RXD7	O	Cell stream received data, bit 7
68	RXD6	O	Cell stream received data, bit 6
69	RXD5	O	Cell stream received data, bit 5
70	RXSOC	O	Cell stream receive start of cell
71	RXD4	O	Cell stream received data, bit 4
72	RXD3	O	Cell stream received data, bit 3
73	RXD2	O	Cell stream received data, bit 2
74	RXD1	O	Cell stream received data. bit 1
75	RXD0	O	Cell stream received data, bit 0
76	VSS	-	
77	TXCLK	I	Cell stream transmit clock
78	TXD7	I	Cell stream transmit data bit 7
79	TXD6	I	Cell stream transmit data bit 6
80	TXD5	I	Cell stream transmit data bit 5
81	TXSOC	I	Cell stream transmit sync
82	TXD4	I	Cell stream transmit data bit 4
83	TXD3	I	Cell stream transmit data bit 3
84	TXD2	I	Cell stream transmit data, bit 2
85	TXD1	I	Cell stream transmit data bit 1
86	VDD	-	
87	TXD0	I	Cell stream transmit data bit 0
88	TXEN	I	Cell stream transmit enable

Pin No	Name	Type	Function
89	TXFULL	O	Cell stream transmitter full
90	RXEN	I	Cell stream receiver enable
91	VSS	-	
92	RXEMPTY	O	Cell stream receiver empty
93	ATD7	I/O	Transmit ATC data bus bit D7
94	ATD6	I/O	Transmit ATC data bus bit D6
95	ATD5	I/O	Transmit ATC data bus bit D5
96	ATD4	I/O	Transmit ATC data bus bit D4
97	ATD3	I/O	Transmit ATC data bus bit D3
98	ATD2	I/O	Transmit ATC data bus bit D2
99	ATD1	I/O	Transmit ATC data bus bit D1
100	VSS	-	
101	ATD0	I/O	Transmit ATC data bus bit D0
102	ATRFDO	O	Transmit ATC ready for data output
103	ATDAVI	I	Transmit ATC data available input
104	ATRFDI	I	Transmit ATC ready for data input
105	ATDAVO	O	Transmit ATC data available output
106	ARD7	I/O	Receive ATC data bus bit D7
107	ARD6	I/O	Receive ATC data bus bit D6
108	ARD5	I/O	Receive ATC data bus bit D5
109	ARD4	I/O	Receive ATC data bus bit D4
110	VDD	-	
111	RESET	I	NTC master reset input
112	ARD3	I/O	Receive ATC data bus bit D3
113	ARD2	I/O	Receive ATC data bus bit D2
114	ARD1	I/O	Receive ATC data bus bit D1
115	ARD0	I/O	Receive ATC data bus bit D0
116	ARRFDO	O	Receive ATC ready for data output
117	ARDAVI	I	Receive ATC data available input
118	ARRFDI	I	Receive ATC ready for data input
119	ARDAVO	O	Receive ATC data available output
120	VSS	-	
121	STATSCLK	I	Switch statistics clock input
122	STATSIN	I	Switch statistics serial data input
123	N/C	-	Not Connected
124	N/C	-	Not Connected
125	SYNCOUT	-	Transceiver transmitter Cell Sync Output
126	BSWAP	I	Bus swap; Little Endian[0],Big Endian[1]
127	BM	I	Bus mode; Intel[0], Motorola[1]
128	BW	I	Bus width select input 16[0], 32[1]
129	RESERVED	-	Reserved, should be connected to VSS
130	RESERVED	-	Reserved, should be connected to VSS
131	RESERVED	-	Reserved, should be connected to VSS
132	RESERVED	-	Reserved, should not be connected

Pin No	Name	Type	Function
133	LOS	I	Loss of signal input
134	TRFD	I	Transmit ready for data input
135	VSS	-	
136	RDAV	I	Receive data available input
137	RD0	I	Receive data bus bit 0
138	RD1	I	Receive data bus bit 1
139	RD2	I	Receive data bus bit 2
140	RD3	I	Receive data bus bit 3
141	RD4	I	Receive data bus bit 4
142	RD5	I	Receive data bus bit 5
143	RD6	I	Receive data bus bit 6
144	VSS	-	
145	RD7	I	Receive data bus bit 7
146	RCLK	I	Receive clock input
147	TD0	O	Transmit data bus bit 0
148	TD1	O	Transmit data bus bit 1
149	TD2	O	Transmit data bus bit 2
150	TD3	O	Transmit data bus bit 3
151	TD4	O	Transmit data bus bit 4
152	TD5	O	Transmit data bus bit 5
153	TD6	O	Transmit data bus bit 6
154	VDD	-	
155	TD7	O	Transmit data bus bit 7
156	TCLK	I	Transmit clock input
157	$\overline{RD}$/AS	I/O	µP Read / Address Strobe
158	$\overline{WR}$/RW	I/O	µP Write / Read/write
159	$\overline{BHE}$/$\overline{UDS}$/$\overline{DS}$	I/O	µP Byte High Enable / Upper Data Strobe / Data Stobe
160	A0/$\overline{LDS}$/$\overline{BE0}$	I/O	µP Address bit 0 / Lower Data Strobe / Byte Enable 0
161	A1/$\overline{BE1}$	I/O	µP Address bit 0 / Byte Enable 1
162	SIZ0/$\overline{BE2}$	I/O	µP Size 0 / Byte Enable 2
163	SIZ1/$\overline{BE3}$	I/O	µP Size 1 / Byte Enable 3
164	VSS	-	
165	HOLD/$\overline{BR}$	O	µP Hold / Bus Request
166	HLDA/$\overline{BG}$	I	µP Hold Acknowledge / Bus Grant
167	CONT/$\overline{BGACK}$	I/O	µP Cont / Bus Grant Acknowledge
168	$\overline{DTACK}$/READY	I	µP Data Transfer Acknowlege / Ready
169	DCOUT/$\overline{DCOUT}$	O	DMA daisy-chain out
170	$\overline{IRQ}$	O	Interrupt Request
171	$\overline{CS}$	I	Chip select
172	RDYOUT	O	Ready out, indicates R/W cycle can be terminated
173	N/C	-	Not connected
174	VDD	-	
175	D0	I/O	Microprocessor data bus bit D0
176	D1	I/O	Microprocessor data bus bit D1

2.3. Detailed Description

2.3.1. Microprocessor Interface

The microprocessor interface comprises the following signals:-

1 D0 - D31
Bi-directional 32 bit data bus.

2 A2 - A23
Most significant 22 bits of the 24 bit address bus. Bits A2 - A6 are bi-directional; all other lines are tri-state outputs.

3 $\overline{RD}$ / $\overline{AS}$
Multifunction bi-directional signal. Read signal (Intel mode), Address Strobe signal (Motorola mode).

4 $\overline{WR}$ / R/$\overline{W}$
Multifunction bi-directional signal. Write signal (Intel mode), Read / write signal (Motorola mode).

5 $\overline{BHE}$ / $\overline{UDS}$ / $\overline{DS}$
Bi-directional signals which indicate high byte enable / upper data strobe for Intel / Motorola 16 bit bus operation, and data strobe for Motorola 32 bit operation.

6 A0 / $\overline{LDS}$ / $\overline{BE0}$
Multifunction bi-directional signal. Functions are as follows:-
Motorola 32 bit mode:-
A0: Least significant address line

Motorola 16 bit mode:-
$\overline{LDS}$: Lower data strobe

Intel 32 bit mode:
$\overline{BE0}$: Lower byte enable signal

7 A1 / $\overline{BE1}$
Multifunction bi-directional signal. Functions as address line A1 in 16 bit modes and Motorola 32 bit mode. Functions as $\overline{BE1}$ in 32 bit Intel mode.

8 SIZ0 / $\overline{BE2}$
Used in 32 bit modes to enable long word transfers.

9 SIZ1 / $\overline{BE3}$
Used in 32 bit modes to enable long word transfers.

10 HOLD / $\overline{BR}$
Hold / bus request output signal used for DMA operations.

11 HLDA / $\overline{BG}$
Hold / bus grant acknowledge output signals used for DMA operations.

12 CONT / $\overline{BGACK}$
CONT signal in Intel mode, Bus grant acknowledge signal in Motorola mode.

13 $\overline{DTACK}$ / $\overline{READY}$
Input signal used to control data transfer operations in Motorola / Intel modes respectively.

14 DCOUT / $\overline{DCOUT}$
DMA daisy chain output. This output signal is activated by the NTC when it is releasing control of the system bus.

15 BW
Bus width input signal, Indicates whether bus is 16 bits (0) or 32 bits (1).

16 BM
Bus mode input signal, indicates whether bus is Intel (0) or Motorola (1).

17 BSWAP
Bus swap input signal, used to swap the higher and lower byte order. A '0' selects the low byte on pins D0–D7, and a '1' selects the low byte on D8–D15.

18 $\overline{IRQ}$
Interrupt request, open-drain output signal active when the NTC wishes to interrupt the processor.

19 $\overline{RESET}$
Reset input signal, places the NTC in a reset state. This signal must be active for at least 2 system clocks, and the clock must be active during this time. After reset, all internal control registers and most status registers will be cleared.

20 $\overline{CS}$
Chip select input. This pin must be set to '0' during read/write accesses to internal NTC registers.

21 RDYOUT
Ready output signal. Indicates that the current register access cycle may be terminated.

2.3.2. Switch Statistics Interface

This interface receives statistics information from the switch and comprises the following signals:-

1 STATSIN
Switch statistics in, this pin provides a serial data stream of switch statistic packets which have been formatted similar to HDLC.

2 STATSCLK
Statistics clock, this clock input is used to control the data on the STATSIN input. Data is sampled by the NTC on the rising edge of this clock. This input may be asynchronous to any other NTC clock input, but its frequency must be less than or equal to the system clock frequency (RXCLK).

2.3.3. Cell Stream Interface

This interface comprises the following signals:-

1 RXD0 - RXD7.
These 8 output signals provide 8 bit parallel receive path data.

2 RXSOC
Receive start of cell output. This output indicates that the first byte of an ATM cell (or routing tag) is available on the RXD0 - RXD7 data lines. This signal is not periodic, since its frequency is dependent on the assigned cell data rate.

3 RXCLK
Receive path data is clocked out on the falling edge of this clock. It can be of arbitrary frequency, but should be as close as possible to the value as determined by the physical data rate / protocol. It is also the system clock. A nominal frequency of 20MHz would be used.

4 RXEN
Receiver enable. This active high input signal is used to control data flow.

5 $\overline{\text{RXEMPTY}}$
This active low output signal is used to control data flow.

6 TXD0 - TXD7
These 8 input signals provide 8 bit parallel transmit path data.

7 TXSOC
Transmit start of cell input. This input is used to identify when the first byte of an ATM cell (or routing tag) is available on the TXD0 - TXD7 data lines. This signal is not periodic, since its frequency is dependent on the assigned cell data rate.

8 TXCLK
Transmit path data is sampled on the rising edge of this clock. It can be of arbitrary frequency, but should be as close as possible to the value as determined by the physical data rate / protocol. It should be the same nominal frequency as RXCLK, but no particular phase relationship is required.

9 TXEN
Transmitter enable. This active high input signal is used to control data flow.

10 $\overline{\text{TXFULL}}$
This active low output signal is used to control data flow.

2.3.4. Address Translation Controller Interface

The NTC comprises two separate interfaces for connecting to two ATCs. Each interface comprises the following signals:-

1 ATD0 - 7, ARD0 - 7.
Eight bi-directional data lines which provide the VPI/VCI values to the ATC, and also provide the NTC with the translated VPI/VCI values and routing tag from the ATC.
The data from these pins are clocked out of the NTC on the falling edge of the RXCLK pin.

2 ATDAVO, ARDAVO
Data available output signal.

Indicates that the NTC has VPI/VCI data available for translation.

3 ATRFDI, ARRFDI
Ready for data input signal. Indicates that the ATC is ready to accept new VPI/VCI data for translation.

4 ATDAVI, ARDAVI
Data available input signal. Indicates that the ATC has VPI/VCI and tag data available for transmission to the NTC.

5 ATRFDO, ARRFDO
Ready for data output signal. Indicates that the NTC is ready to accept new VPI/VCI and tag data from the ATC.

2.3.5. Transceiver Interface

This interface is used to transfer transmit and receive data between the NTC and an external transceiver. It comprises the following signals:-

1 RD0 - RD7
These 8 input signals are used to transfer data from a transceiver to the NTC.

2 RDAV
This signal is used to qualify data which is received on RD0 - RD7. Incoming data is ignored while RDAV is inactive.

3 TD0 - TD7
These 8 output signals are used to transfer data from the NTC to a transceiver.

4 TRFD
This input signal indicates that the transceiver is ready to receive data from the NTC. The NTC will not send any data until the transceiver indicates that it is ready by activating TRFD. When TRFD is inactive the TD0 - TD7 signals will retain their previous values.

5 RCLK
This input signal is used to synchronise all data received on the RD0-7 pins. Input data is sampled on the rising edge of this clock.

6 TCLK
This input signal is used to synchronise all data transmitted on the TD0-7 pins. Output data changes on the falling edge of this clock.

7 LOS
Loss of signal. This input signal is used to indicate to the NTC that the input signal has been completely lost. An internal alarm is set and an interrupt condition is generated.

8 SYNCOUT
Cell sync out signal. This output is active during the first byte of a cell to indicate the start of the cell on the transceiver transmit interface.
It is useful in cell-based modes to provide any external circuitry with cell boundary information.

3. FUNCTIONAL DESCRIPTION

This section describes the behavior of each major functional block within the NTC, as illustrated in Fig. 4. The descriptions contained in this section are from a user's perspective and are intended to give a detailed description of device functionality and mode of operation. The NTC comprises the following major components :-

1 Receive Framer

2 Transmit Framer

3 Cell Receiver

4 Cell Transmitter

5 Cell Stream Interface

6 Operations Administration and Maintenance Controller

7 Statistics Controller

8 Switch Statistics Handler

9 DMA Controller

10 Microprocessor Bus Interface

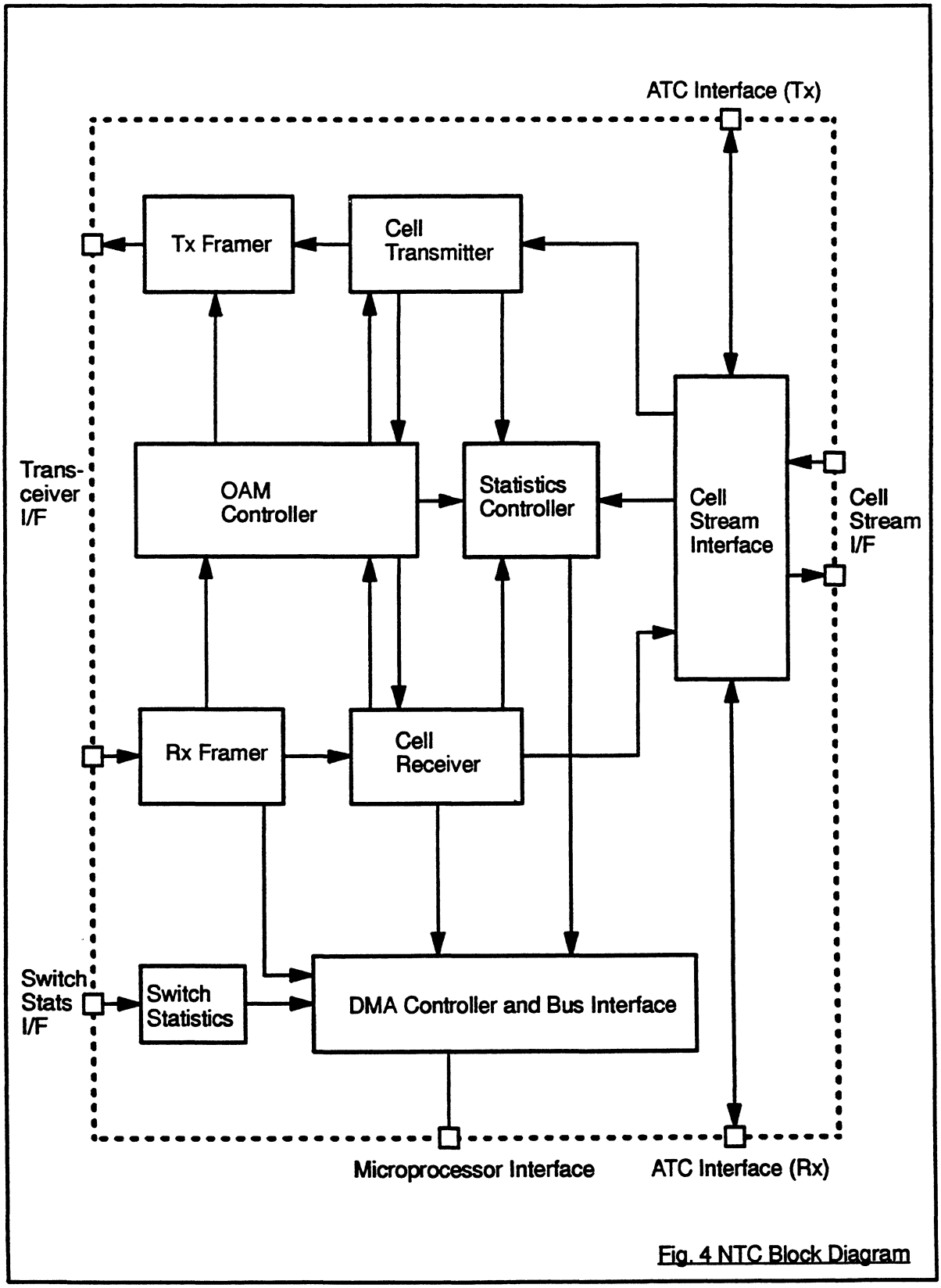


Fig. 4 NTC Block Diagram

3.1. Receive Framer

A simplified block diagram of the receive framer is shown in Fig. 5.

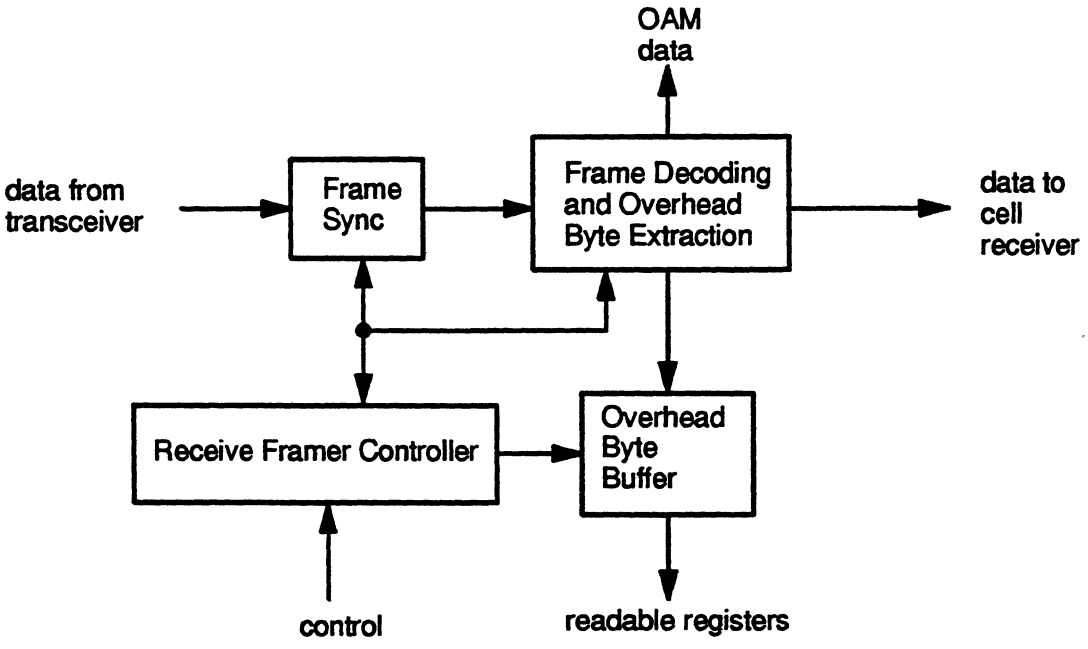


Fig. 5 Receive Framer Block Diagram

The receive framer has 5 modes of operation, namely:-

1 Cell Based (no external framing)

2 SDH STM-1

3 SONET STS-3c

4 DS3

5 E3

The required operating mode is selected via the NTC mode register. The functions associated with each operating mode are described in the following paragraphs.

3.1.1. Cell Based

In this mode of operation the receive framer acts as a transparent link between the transceiver interface and cell receiver section. This mode of operation allows an unframed ATM cell interface to be supported, and facilitates the use of an external framing device for physical interfaces not supported by the NTC. Physical layer OAM functions would be provided by using the F1 / F3 PLOAM cell capability of the NTC.

3.1.2. SDH STM-1

Frame alignment functions for STM-1 include detecting the start of an STM-1 frame, detecting the start of the VC-4 payload using the AU-4 pointer, and extracting a stream of ATM cells. The cells are then passed to the cell receiver function. An STM-1 frame is delimited by frame alignment bytes in the section overhead (A1, A2). The frame alignment bytes are repeated 3 times in the sequence A1, A1, A1, A2, A2, A2, as shown in Fig. 6. Frame alignment is assumed if the frame alignment sequence is detected in n consecutive frames, and frame alignment is assumed to be lost if the pattern is incorrect in p consecutive frames. The parameters n and p can be programmed by the user in the range 1 to 15.

After frame alignment has been detected, the data is de-scrambled using the polynomial : $1 + x^6 + x^7$ (except for the first 9 bytes of the SOH), and the AU-4 pointer value is used to identify the start of the VC-4 container. C-4 container bytes are extracted and passed to the cell receiver.

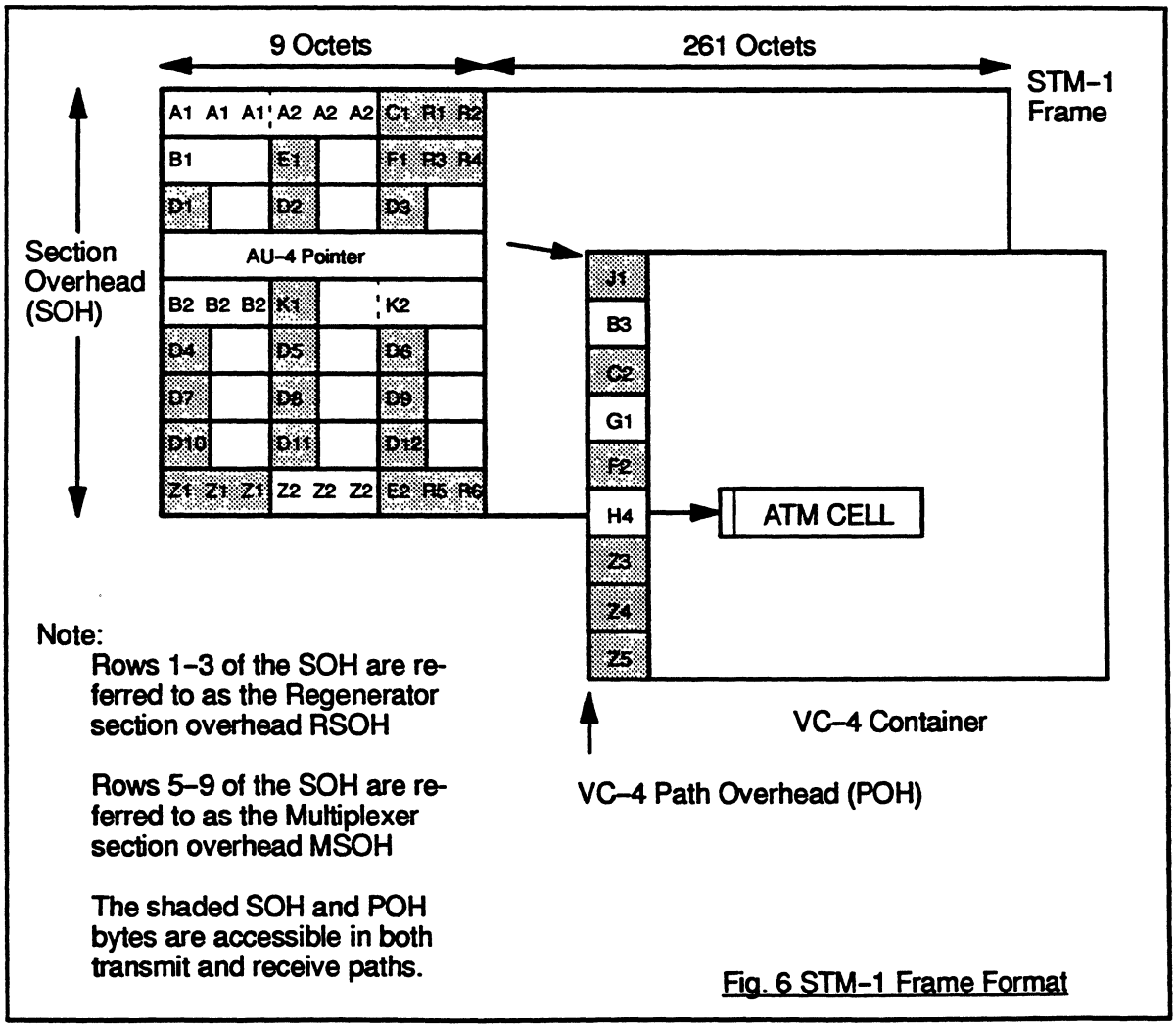


Fig. 6 STM-1 Frame Format

The SOH/POH bytes shown shaded in Fig. 6 are latched into registers within the receive framer and hence are available for reading directly by the processor. The SOH/POH bytes from one frame are latched at the start of the following frame.

The STM-1 receive framer performs performance monitoring and fault detection for STM-1 frames using the Bit Interleaved Parity (BIP) bytes.
These include the following :-

1 Regenerator Section error monitoring using a BIP-8 code in the B1 byte position.

2 Multiplex Section error monitoring using using a BIP-24 code in B2 byte positions.

3 Path error monitoring using a BIP-8 code in B3 byte position.

Any detected errors from the BIP checks are passed to the OAM controller and may be read by the processor using the "Physical Layer Alarms Received" status register (SR59).

In addition, the receive framer detects and reports the following fault conditions, which are also passed to the OAM controller and then made available in SR59 :-

1 MS-AIS (received K2 field)

2 MS-FERF (received K2 field)

3 Path AIS (all 1's in AU-4 pointer)

4 Path FERF (received G1 field)

The receive framer extracts the received Far End Block Error (FEBE) bytes from the frame and provides these to the statistics controller for recording. The B2 FEBE is contained in bits 20-24 of the Z2 field, and the B3 FEBE is contained in bits 1-4 of the G1 field.

The receive framer generates the following maskable interrupts to the microprocessor :-

1 Loss Of Signal (LOS)

2 Loss Of STM-1 Frame (LOF)

3 Loss Of AU-4 Pointer (LOP)

4 Start Of Frame (SOFRX)

5 Start Of VC-4 Container (SOVRX)

The SOFRX and SOVRX interrupts may be used to control the timing for reading the extracted SOH/POH bytes. For example, a SOFRX interrupt indicates that the previous frame SOH bytes have all been latched, and will be stable for 125μS, until the next frame. Similarly for the POH bytes.

3.1.3. SONET Mode

This mode is almost identical to the SDH STM-1 mode. The few differences are in the SOH and POH bytes, which are described in the transmit framer section.

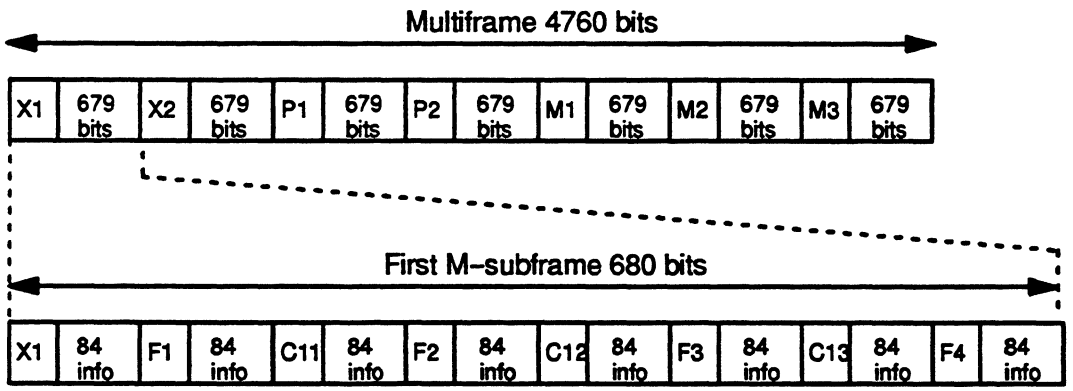
3.1.4. DS3 Mode

In this mode the receive framer first synchronises to the 44.736 kbps DS3 frame, as defined in CCITT G.752 and illustrated in Fig. 7, and then synchronises to the physical layer convergence protocol (PLCP) frame as defined in the ATM Forum UNI specification, illustrated in Fig. 8. ATM cells are then extracted and passed to the cell receiver. The Z1-Z6 PCLP frame overhead bytes are stored in registers and made available for reading by the processor.

Each DS3 multi-frame contains 4760 bits, and is divided into seven M-subframes of 680bits. Each M-subframe is further divided into 8 blocks of 85 bits, 1 bit for overhead and 84 bits for payload. The PCLP bytes are contained within the 84 information bits of each block in each subframe.

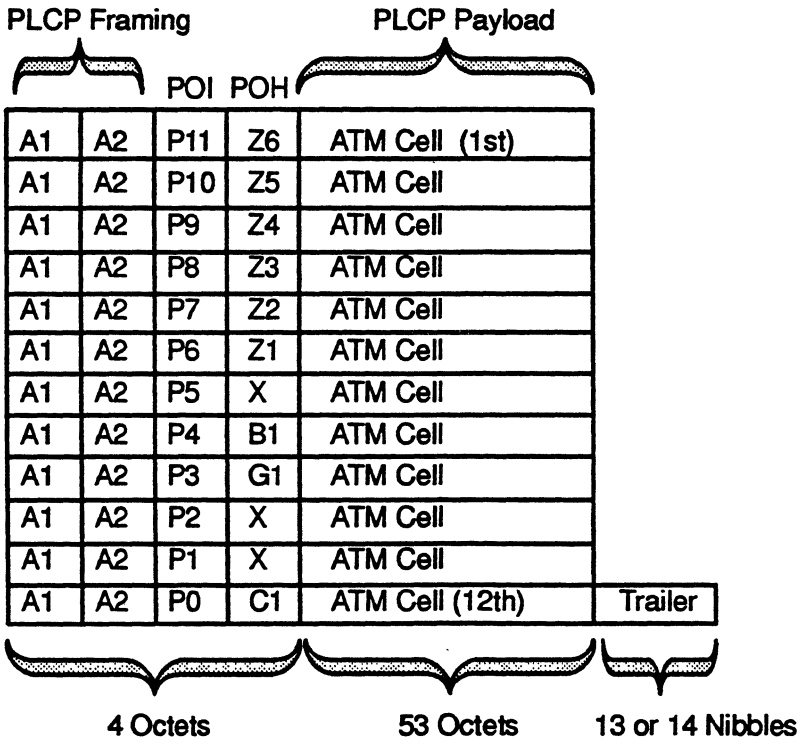
The 125µs PCLP frame occupies more than one 107µs DS3 frame, but the PCLP bytes are nibble aligned to the DS3 frame. Nibbles begin after the control bits X, F, P, C, M.

The receive framer checks the B1 field using a BIP-8 code and will report a BIP-8 error count to the OAM controller. The receive framer also detects PLCP path status using the G1 subfield, and will pass the associated data to the OAM controller.



56 Overhead bits sequential positions							
X1	F1	C11	F2	C12	F3	C13	F4
X2	F1	C21	F2	C22	F3	C23	F4
P1	F1	C31	F2	C32	F3	C33	F4
P2	F1	C41	F2	C42	F3	C43	F4
M1	F1	C51	F2	C52	F3	C53	F4
M2	F1	C61	F2	C62	F3	C63	F4
M3	F1	C71	F2	C72	F3	C73	F4

Fig. 7 DS3 Frame Format



Path Overhead Identifier Table :

POI	POI Code	POH
P11	00101100	Z6
P10	00101001	Z5
P9	00100101	Z4
P8	00100000	Z3
P7	00011100	Z2
P6	00011001	Z1
P5	00010101	X
P4	00010000	B1
P3	00001101	G1
P2	00001000	X
P1	00000100	X
P0	00000001	C1

Note:
The shaded POH bytes are processor accessible in both transmit and receive paths.

Fig. 8 PLCP Frame Format

The DS-3 receive framer performs the following functions :-

1 DS3 frame alignment through detection of the M-subframe alignment signal F1/F2/F3/F4 consisting of 1001, and detection of the multiframe alignment pattern M1/M2/M3 consisting of 010, and then extraction of each 84-bit information payload of every M-subframe.

2 Extraction of the PLCP payload and POH bytes by aligning to the PLCP framing and POI bytes. The framing bytes are A1=11110110 and A2=0010100. The POI indexes each of the 12 POH bytes.

3 B1 error and path status monitoring, together with FEBE and RAI reporting to OAM controller.

4 Extraction of the ATM cells, which will be forwarded to the cell receiver for cell delineation.

The DS-3 receive framer performs performance monitoring and fault detection using the B1 Bit Interleaved Parity (BIP) byte.

Any detected error from the BIP check is passed to the OAM controller and may be read by the processor using the "Physical Layer Alarms Received" status register (SR59).

In addition, the receive framer detects and reports the following fault conditions, which are also passed to the OAM controller and then made available in SR59 :-

1 RAI (received G1 field)

The receive framer extracts the received Far End Block Error (FEBE) byte from the frame and provides this to the statistics controller for recording. The FEBE is contained in the G1 field.

The receive framer generates the following maskable interrupts to the microprocessor :-

1 Loss Of Signal (LOS)

2 Loss Of DS-3 Frame (LOF)

3 Loss Of PLCP Frame (LOP)

4 Start Of DS-3 Frame (SOFRX)

5 Start Of PLCP Frame (SOVRX)

The SOVRX interrupt may be used to control the timing for reading the extracted POH bytes. For example, a SOVRX interrupt indicates that the previous PLCP POH bytes have all been latched, and will be stable for 125μS, until the next frame.

3.1.5. E3 Mode

In this mode, the data rate is defined as 34.368 kbps, and each 125μs frame contains 537 bytes consisting of 7 octets for generic path overhead and 530 octets of payload, as shown in Fig. 9.

The bytes within the ATM cells are octet aligned with the payload, but each received frame does not necessarily contain 10 complete cells, ie ATM cells may cross a 125μs boundary.

The shaded bytes shown are available for reading by the processor.

In this mode the framer performs the following functions:-

1 Frame alignment through detection of a frame delimiter pattern contained in FA1 / FA2

2 Extraction of the path overhead bytes for OAM error monitoring, performance monitoring, and network communication.

3 Extraction of the payload bytes, which will be forwarded to the cell receiver for cell delineation and descrambling.

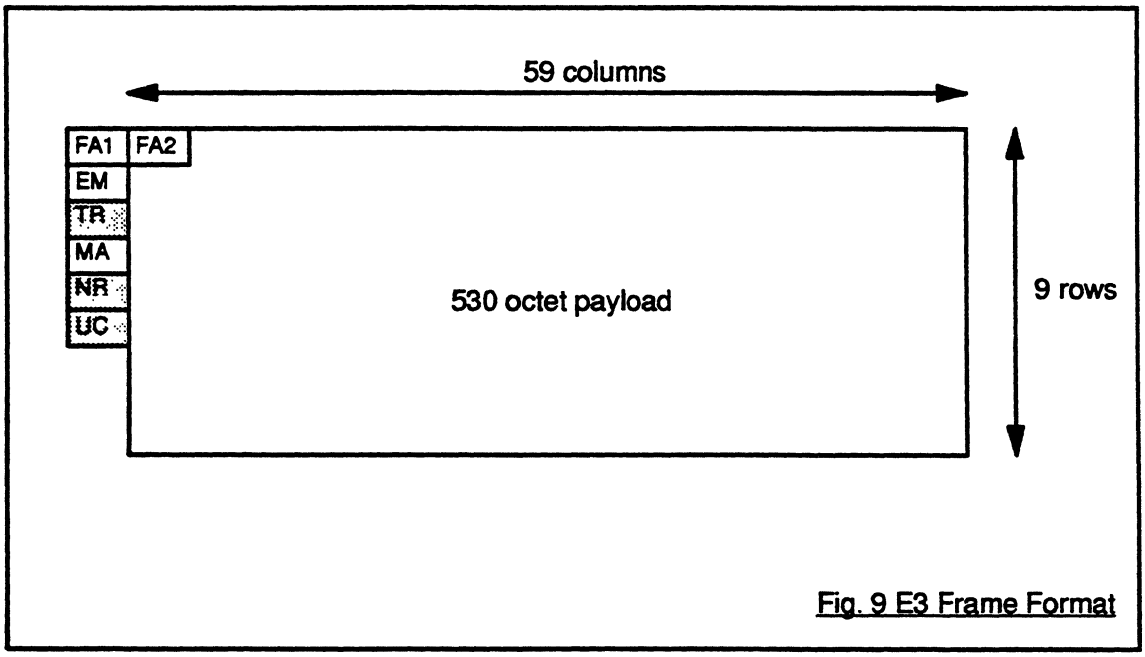


Fig. 9 E3 Frame Format

3.1.6. Transceiver Receive Interface

The transceiver receive interface allows the transfer of 8-bit parallel data from a transceiver to the receive framer of the NTC. The data is validated using the RDAV active high signal. If this signal is inactive, then no data will be clocked into the NTC. Input data will be sampled on the rising edge of RCLK. The frequency and phase of RCLK may be arbitrary, relative to the system clock RXCLK, but its frequency must be less than RXCLK in order to support the full data rate. The signals are internally synchronised to the system clock.

In addition to the data control signals, there is also a Loss of Signal (LOS) input. This signal would normally be generated by the opto-electrical device, to indicate that the received signal has been lost due to the power level of the signal being below a threshold. This active high signal may be used to generate an interrupt to the processor. Additionally, it will generate an alarm condition, which may be sent back to the transmitting device via the Transmit Framer.

The basic timing of these signals is illustrated in Fig. 10.

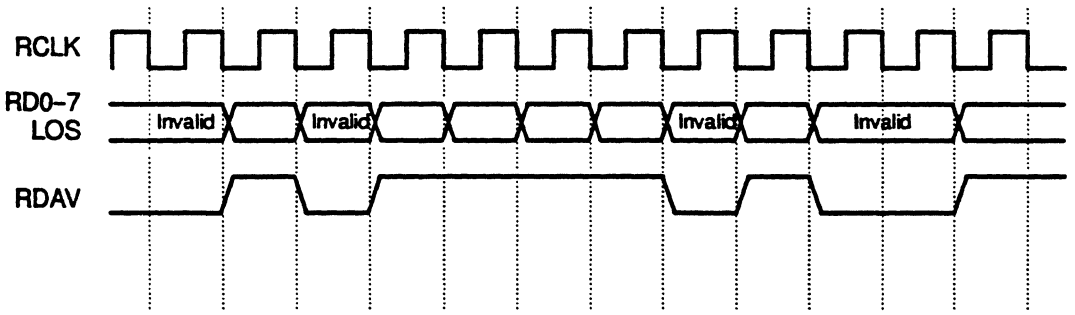


Fig. 10 Transceiver Receive Interface Timing

3.2. Transmit Framer

A simplified block diagram of the transmit framer is shown in Fig. 11.

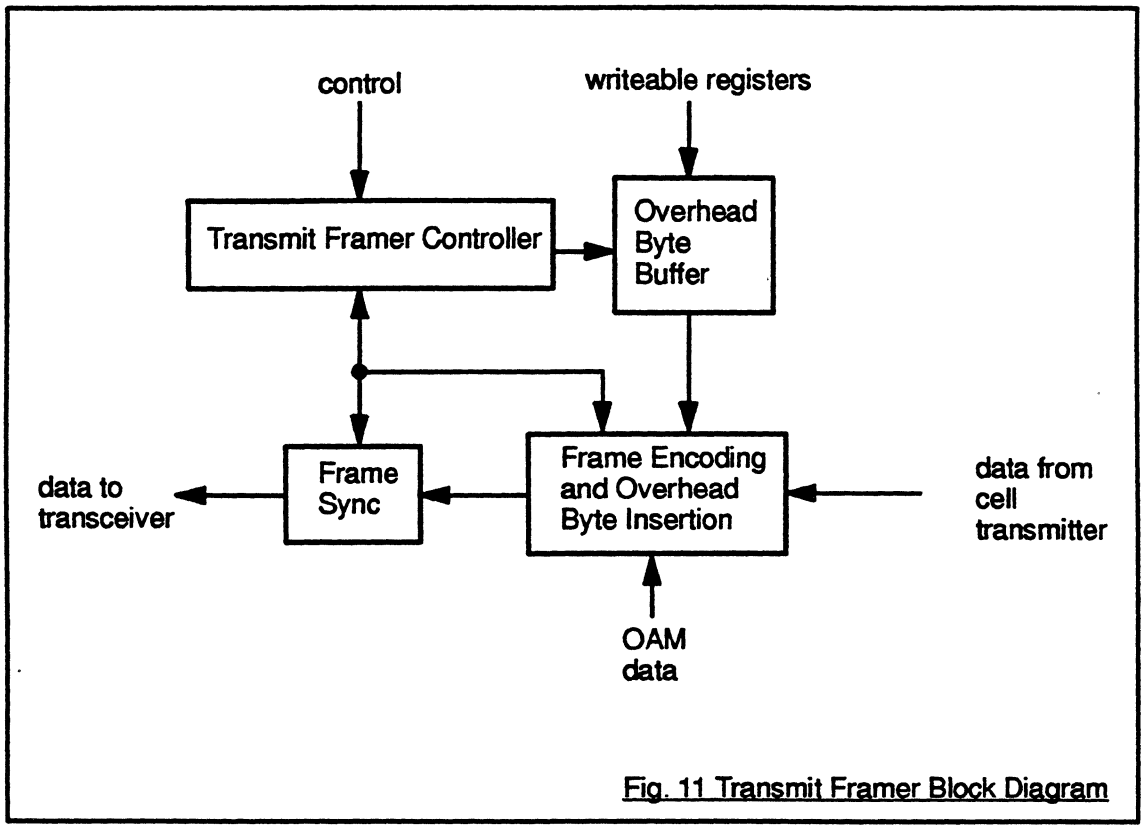


Fig. 11 Transmit Framer Block Diagram

The transmit framer operates in the same modes as the receive framer and generates outgoing frame patterns in accordance with the relevant framing mode. Various minor aspects appropriate to the various media are described below.

Some of the overhead bytes are controlled according to data obtained from the OAM controller. The other normally redundant bytes will take the values stored in processor accessible registers. The transmit framer will generate an interrupt to the processor to indicate start of frame. This signal may be used to synchronise the writing of the overhead bytes.

When used in framed modes, the transmit framer inserts outgoing alarms according to data received from the OAM controller. These alarms may optionally be ignored or accepted. Alarm conditions may also be forced, irrespective of the indication from the receive path.

3.2.1. SDH / SONET Modes

The transmit framer transmits data in STM-1 frames as illustrated in Fig. 6 However, transmitted data is synchronised to the SDH clock, and hence the AU-4 pointer will be set to 0, indicating that the VC-4 container will remain in a fixed position relative to the STM-1 payload. The H4 pointer within the VC-4 container is updated for each frame to indicate the position the next ATM cell header.

Section and path overhead bytes are controlled as detailed below:-

1 C1 byte :
Normally set to 00000001 (processor accessible).

2 R1-R2 bytes (Reserved) :
Normally set to 10101010 (processor accessible) (for SDH).

Note: C1,R1,R2 should be set to 00000001, 00000010, 00000011 (for SONET).

3 B1 byte :
This byte will be set according to a BIP-8 code calculated over all bits of the previous STM-1 frame after scrambling. The value will be inserted in the current STM-1 frame before scrambling.

4 E1 byte :
Normally set to 00000000 (processor accessible).

5 F1 byte :
Normally set to 00000000 (processor accessible).

6 R3-R6 bytes (Reserved) :
Normally set to 00000000 (processor accessible).

7 D1-D3 bytes :
Normally set to 00000000 (processor accessible).

8 24 bit AU-4 pointer value :
H1 (bits 1 to 4) set to 0110 (ie NDF = invalid).
H1 (5 & 6) set to 10 (ie SS = 10).
H1 - H2 (7 to 16) set to 0 (VC4 starts after last H3 byte).
H3 (17 - 24) set to 0.

9 B2 bytes :
These 3 bytes will be set according to a BIP-24 code calculated over all bits of the previous STM-1 frame, except for the first 3 rows of section overhead. The code will be calculated before scrambling, and will be inserted in the current STM-1 frame before scrambling.

10 K1 byte :
Normally set to 00000000 (processor accessible).

11 K2 byte :
This byte will be set to indicate line AIS and FERF conditions as indicated by the OAM controller. The byte will be encoded as follows. Bits 1 to 5 will be set to zero. Bits 6 to 8 will be set to 111 for line AIS, 110 for FERF, and 000 in all other cases.

12 D4-D12 bytes :
Normally set to 00000000 (processor accessible).

13 Z1 bytes :
Normally set to 00000000 (processor accessible).

14 Z2 bytes :
These bytes will be set to indicate the B2 FEBE error count as indicated by the OAM controller. (Bits 20-24). Other bits set to 0.

15 E2 byte :
Normally set to 00000000 (processor accessible).

16 J1 byte :
Normally set to 00000000 (processor accessible).

17 B3 byte :
This byte will be set according to a BIP-8 code calculated over all bits of the previous VC-4 container before scrambling, and will be inserted in the current VC-4 container before scrambling.

18 C2 Byte :
Normally set to 00000000 (processor accessible for SDH).

Normally set to 00010011 (processor accessible for SONET).

19 G1 byte :
This byte will be set according to information received from the OAM controller as follows :-
G1 (bits 1 - 4) FEBE error count (0 to 8).
G1 (bits 1 - 4) set to 1001 to indicate FERF (for SONET).
G1 (bit 5) set to 1 to indicate RAI (for SONET).
G1 (bit 5) set to 1 to indicate FERF (for SDH).

20 F2 byte :
Normally set to 00000000 (processor accessible).

21 H4 byte :
Set to indicate the offset from itself to the start of the next ATM cell. The value will be between 0 and 52. Bits 3-8 will be used for this purpose.

22 Z3 byte :
Normally set to 00000000 (processor accessible).

23 Z4 byte :
Normally set to 00000000 (processor accessible).

24 Z5 byte :
Normally set to 00000000 (processor accessible).

3.2.2. DS3 Mode

In this mode ATM cells are transmitted in PLCP frames having the following attributes :-

1 Data transmission rate is synchronised to the DS3 transmission rate and hence no justification is used (ie. no nibble stuffing).

2 B1 byte :
This byte will be set according to a BIP-8 code calculated over the PLCP payload and POH fields of the previous PLCP frame.

3 G1 byte :
G1 (bits 1 - 4) Set to indicate the FEBE count provided by the OAM controller
G1 (5) set to 1 when RAI is indicated by the OAM controller, otherwise set to 0.

4 C1 byte :
Set sequentially to 11111111, 00000000 and 01100110 to indicate the frame phase.

5 Z1-Z6 bytes :
Normally set to 00000000 (processor accessible).

6 X bytes :
Set to 00000000.

The PLCP frames will then be segmented and sent as DS3 frames.

3.2.3. E3 Mode

In this mode ATM cells are transmitted in E3 frames having the following attributes:-

1 Transmitted ATM cells will be byte aligned with the E3 frame. The first ATM cell will appear immediately after the FA2 byte. Hence, the 530 byte payload will contain 10 complete cells

2 EM byte :
This byte will be set according to a BIP-8 code calculated over all the bits of the previous 125µs frame.

3 MA byte :
This byte will contain FERF and FEBE information from the OAM controller.

4 TR byte :
Normally set to 00000000 (processor accessible).

5 NR byte :
Normally set to 00000000 (processor accessible).

6 UC byte :
Normally set to 00000000 (processor accessible).

3.2.4. Transceiver Transmit Interface

The transceiver transmit interface allows the transfer of 8-bit parallel data from the NTC to a transceiver. The output data is controlled using the TRFD active high signal. If this signal is inactive, then the output data will freeze. Output data will be clocked out of the NTC on the falling edge of TCLK. The frequency and phase of TCLK may be arbitrary, relative to the system clock RXCLK, but its frequency must be less than RXCLK in order to support the full data rate. The signals are internally synchronised to the system clock.

In addition to the data control signals, there is also a Cell Sync (SYNCOUT) output. This active high signal may be used to control an external device when used in cell-based modes. The signal will be active during the first byte of the header of a cell.

The signal is also operational during framed modes, but its use is limited in this case because of the overhead bytes being mixed with the cell bytes. An external device could not differentiate between these.

The basic timing of these signals is illustrated in Fig. 12.

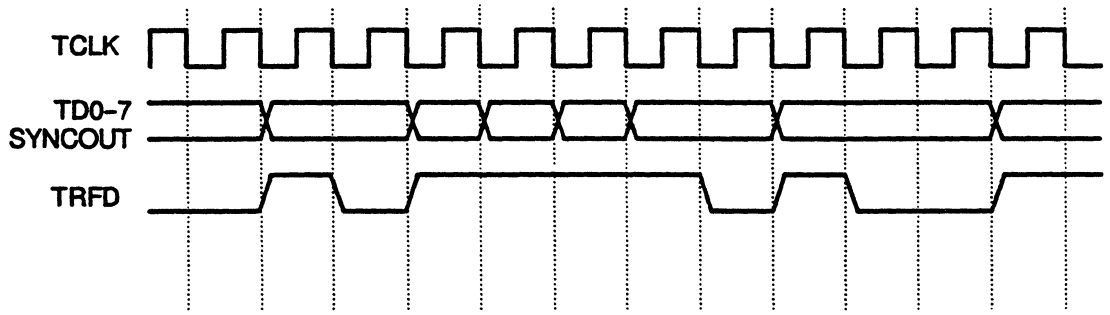


Fig. 12 Transceiver Transmit Interface Timing

3.3. Cell Receiver

A simplified block diagram of the cell receiver is shown in Fig. 13.

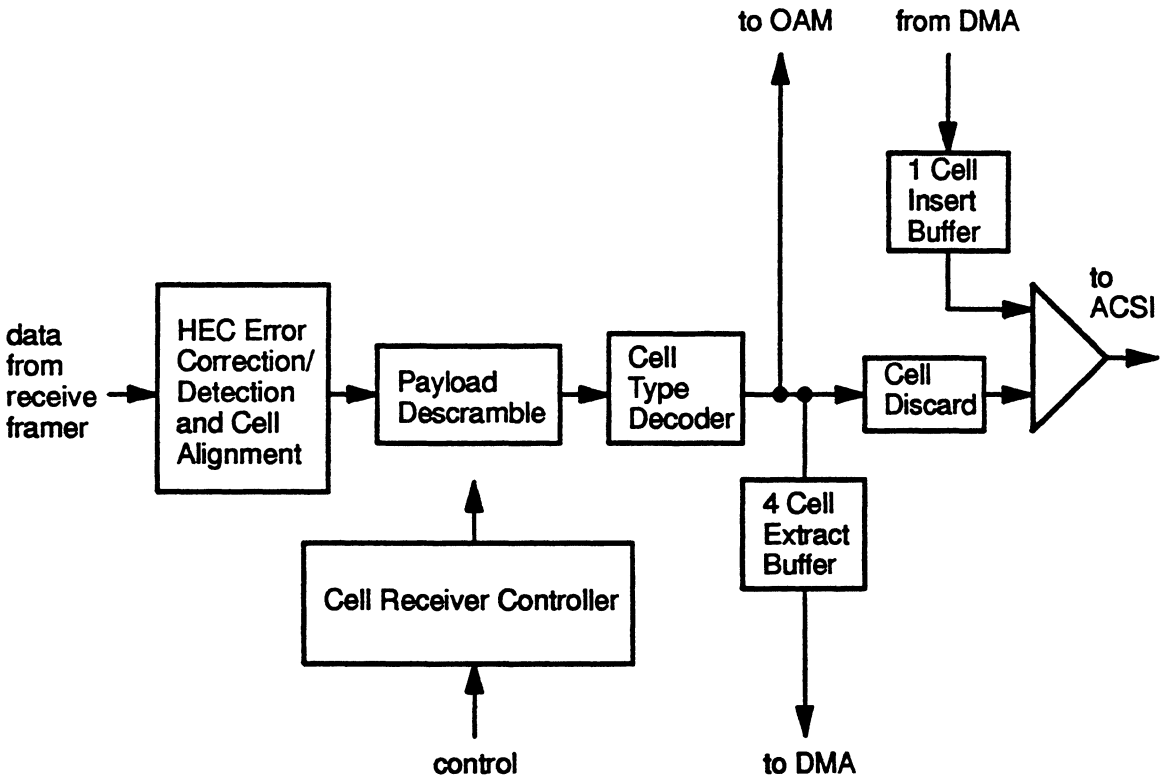


Fig. 13 Cell Receiver Block Diagram

3.3.1. Basic Features

The cell receiver takes data from the receive framer and performs the following functions, generally passing data on to the cell stream interface.

1. Cell delineation.
2. Cell header error detection and correction.
3. Cell payload descrambling.
4. Cell type recognition.
5. CRC-10 checking for received OAM cells.
6. Cell extraction (from the transceiver interface) via DMA.
7. Cell discard.
8. Cell insertion (towards the cell stream interface) via DMA.
9. Cells from the transceiver interface copied to the OAM Controller for cell-based OAM processing.

Data flow through the cell receiver is governed by the availability of data, clock-by-clock, from the transceiver interface via the receive framer.

3.3.2. Cell Reception

The cell delineation process will attempt to gain cell alignment continuously on the byte stream coming from the transceiver interface after being enabled. Cell alignment is gained by detecting DELTA correct results to the calculation of the HEC field residue at cell-spaced intervals. Cell alignment is assumed lost (and an interrupt generated to the host) when ALPHA incorrect results to the HEC calculation are detected. The parameters DELTA and ALPHA are programmed by the user to be between 0 and 15 inclusive. Suggested values in CCITT I.432 are DELTA = 6, ALPHA = 7 for all of the framed physical interfaces; and DELTA = 8, ALPHA = 7 for the unframed, cell-based physical interface. The values of DELTA and ALPHA are programmed in CR18.

The HEC calculation (using the polynomial $1 + x + x^2 + x^8$) is carried out over all 8 possible bit alignments of the data coming from the transceiver interface. It is possible to specify that the data provided at the transceiver interface is byte-aligned by setting the BALIGN bit in CR19.

The modulo-2 subtraction of the pattern "01010101" from the received HEC field before the calculation is applied is also under user control by programming the HECMASK bit in CR19.

Once cell alignment has been gained, the header error detection and correction process is capable of detecting most headers with multiple bit errors and correcting single bit errors in alternate frames. The single bit error correction may be not enabled by the user if it is not required by not setting the COREN bit in CR19. Error detection and correction events are recorded by the statistics controller.

The user must select the required descrambling algorithm to match the physical interface in use by setting the DESCR1-0 bits in CR19. For the STM-1 / STS-3c or E3 physical interfaces, the self-synchronous descrambler (with polynomial $1 + x^{43}$) is used. For the DS3 physical interface, no descrambling is required while for the unframed, cell-based physical interface. the distributed sample descrambler (with polynomial $1 + x^{28} + x^{31}$) is used.

3.3.3. Cell Type Recognition

The cell header VPI, VCI, PLT and CLP fields are examined to see if the cell is one of the following 12 types : -

1. Idle
   (VPI = 0, VCI = 0, PLT = 000, CLP = 1).
2. PL-OAM F1
   (VPI = 0, VCI = 0, PLT = 001, CLP = 1).
3. PL-OAM F3
   (VPI = 0, VCI = 0, PLT = 100, CLP = 1).
4. Other physical layer
   (VPI = 0, VCI = 0, PLT = XXX, CLP = 1).
5. Unassigned
   (VPI = 0, VCI = 0, PLT = XXX, CLP = 0).
6. Meta signalling
   (VPI = X, VCI = 1, PLT = 0X0, CLP = X).
7. Broadcast signalling
   (VPI = X, VCI = 2, PLT = 0XX, CLP = X).
8. Point-to-point signalling
   (VPI = X, VCI = 5, PLT = 0XX, CLP = X).

9. ATM-OAM F4 segment
(VPI = X, VCI = 3, PLT = 0X0, CLP = X).

10. ATM-OAM F4 end-to-end
(VPI = X, VCI = 4, PLT = 0X0, CLP = X).

11. ATM-OAM F5 segment
(VPI = X, VCI≠0, PLT = 100, CLP = X).

12. ATM-OAM F5 end-to-end
(VPI = X, VCI≠0, PLT = 101, CLP = X).

For ATM-OAM cells, the first byte of the payload is further examined to classify the cell as fault management (FM), activation / deactivation (AD) or performance management (PM).

In addition to these types, ILMI cells can also be identified :
(VPI = 0, VCI = 16, PLT = XXX, CLP = X).

The cell header is also compared to a user-programmed mask which may have any of the 32 header bits set to "0", "1" or "X". This allows cell headers to be matched which have either specific values or values in a range. The mask pattern bits are specified in CR22 & CR23 and the "don't care" bits are specified in CR20 & CR21.

3.3.4. OAM Cell CRC-10 Checking

If the recognised cell type for a received cell is one of the OAM cells, the CRC-10 field at the end of the payload may be checked. If an error is detected, the cell is discarded. This checking is controlled by the CRC10CHK bit in CR18.

3.3.5. Cell Extraction

Based on the recognised cell type, cells may be extracted (but not discarded from the data stream) to system memory using DMA. Cells may be extracted either by specific cell type or by explicitly matching (or not matching) the user mask. Cell extraction is controlled by CR24.

The extract buffer has space for four cells. Transfer of a cell by DMA will not start until the whole cell is in the buffer and the space will not be released until the whole cell has been transferred.

Extraction of OAM cells is subject to checking of the CRC-10 field. If this checking is enabled, a cell with a CRC-10 error in the payload will not be extracted.

3.3.6. Cell Discard

Also based on the recognised cell type, cells may be discarded from the data passed to the cell stream interface, again either by specific cell type or by explicitly matching (or not matching) the user mask. Cell discarding is controlled by CR25. In addition, any cell recognised as a physical layer cell (e.g. idle cells and F1 & F3 PL-OAM cells) will not be passed to the cell stream interface.

3.3.7. Cell Insertion

Insertion of cells into the data stream towards the cell stream interface via DMA is carried out through a single-cell insert buffer. The peak insertion rate is controlled by the PKIR bits in CR18. These give the number of cells which must be received from the transceiver interface for each cell which may be inserted (e.g PKIR3-0 = "1000" gives an insertion rate of 1 cell inserted per 32 cells (2^{13-8}) received or approximately 3.1% of the bandwidth).

It is important to note that, in order to insert a cell in the data going to the cell stream interface, the cell being received

from the transceiver interface must be deleted. This can occur if the cell being received is a physical layer cell or if the user has programmed the discard function to discard the cell, either as one of the pre-defined types or because it matches (or not matches) the user mask.

The peak insertion rate will therefore only be achieved if there are sufficient gaps (i.e. cells being discarded) in the data going to the cell stream interface, unless the INSPRI bit in CR18 is set. In this case, cells will be inserted at the maximum rate governed by the PKIR bits. When a cell is inserted, the cell being received will be lost, irrespective of whether or not it was supposed to be discarded.

The peak insertion rate will only be attained if the NTC's DMA latency can be satisfied by the host system bus.

3.3.8. OAM Cell CRC-10 Generation

If the cell inserted is recognised as an OAM cell, the CRC-10 field may be generated and placed at the end of the payload. If the CRC generation is not enabled, the data supplied from system memory will be transmitted transparently. This is controlled by the CRC10GEN bit in CR18.

3.3.9. Cell-based OAM Processing

If the unframed, cell-based physical interface is in use, the OAM controller handles F1 & F3 PL-OAM cells autonomously. Received cells of these types are therefore supplied to the OAM Controller (if they pass the CRC-10 check) for processing. All other received cells are copied to the OAM Controller in this mode to allow the calculation of the BIP error measurements.

3.4. Cell Transmitter

A simplified block diagram of the cell transmitter is shown in Fig. 14.

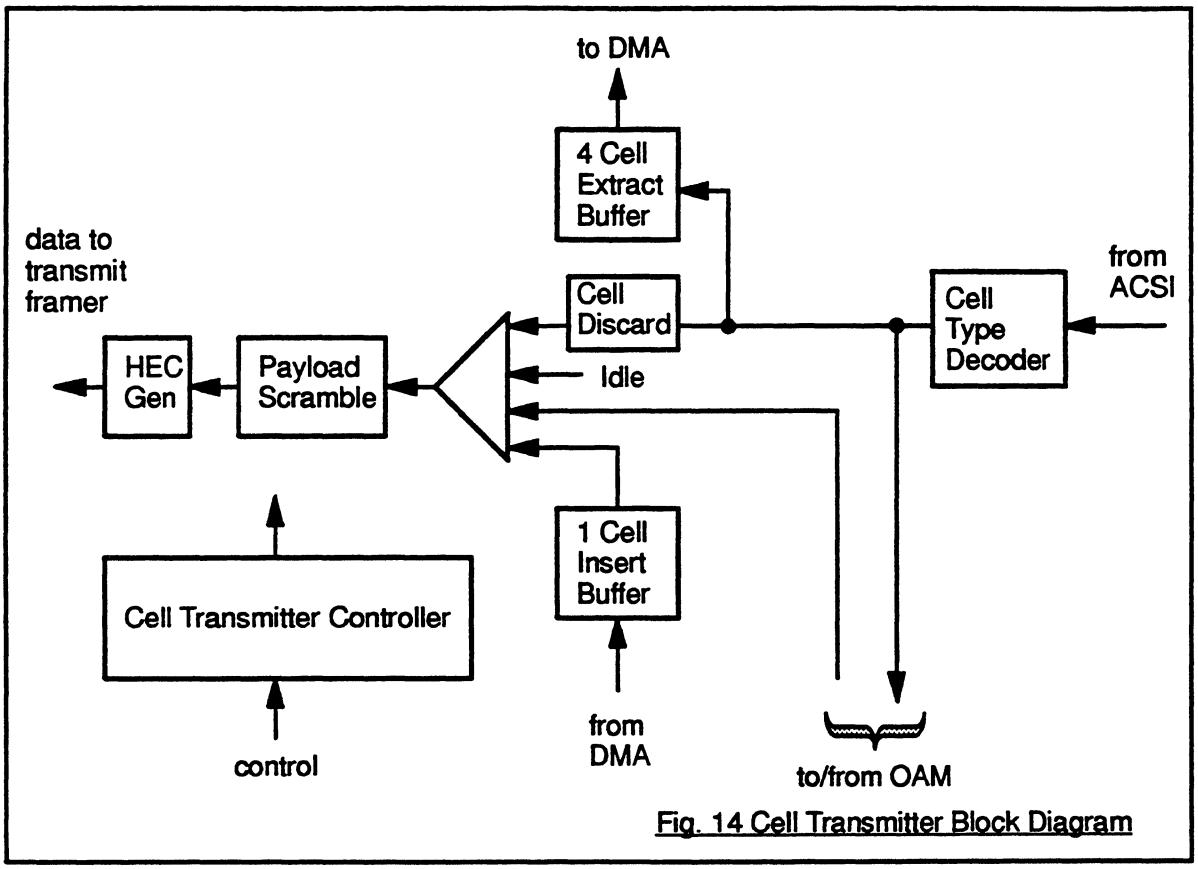


Fig. 14 Cell Transmitter Block Diagram

3.4.1. Basic Features

The cell transmitter takes data from the cell stream interface and performs the following functions. Data is always supplied to the transceiver interface via the transmit framer.

1. Cell type recognition.
2. Cell extraction (from the cell stream interface) via DMA.
3. Cell discard.
4. Cell insertion (towards the transceiver interface) via DMA.
5. Cells inserted from OAM Controller for PL-OAM processing.
6. Cells going to the transceiver interface copied to the OAM Controller for BIP calculations.
7. CRC-10 generation for transmitted OAM cells.
8. HEC field calculation.
9. Cell payload scrambling.

Data flow through the cell transmitter is governed by the ability of the transceiver interface via the transmit framer to accept data clock-by-clock.

If a received cell is recognised as either F4/F5 OAM, then the trailing 10-bit CRC may be optionally verified before being forwarded. If the cell is errored, then it will be discarded.

3.4.2. Cell Type Recognition

The cell header VPI, VCI, PLT and CLP fields are examined to see if the cell is one of the following 8 types : -

1. Unassigned
   (VPI = 0, VCI = 0, PLT = XXX, CLP = 0).

2. Meta signalling
   (VPI = X, VCI = 1, PLT = 0X0, CLP = X).

3. Broadcast signalling
   (VPI = X, VCI = 2, PLT = 0XX, CLP = X).

4. Point-to-point signalling
   (VPI = X, VCI = 5, PLT = 0XX, CLP = X).

5. ATM-OAM F4 segment
   (VPI = X, VCI = 3, PLT = 0X0, CLP = X).

6. ATM-OAM F4 end-to-end
   (VPI = X, VCI = 4, PLT = 0X0, CLP = X).

7. ATM-OAM F5 segment
   (VPI = X, VCI $\neq$ 0, PLT = 100, CLP = X).

8. ATM-OAM F5 end-to-end
   (VPI = X, VCI $\neq$ 0, PLT = 101, CLP = X).

For ATM-OAM cells, the first byte of the payload is further examined to classify the cell as fault management (FM), activation / deactivation (AD) or performance management (PM).

In addition to these types, ILMI cells can also be identified :
(VPI = 0, VCI = 16, PLT = XXX, CLP = X).

The cell header is also compared to a user-programmed mask which may have any of the 32 header bits set to "0", "1" or "X". This allows cell headers to be matched which have either specific values or values in a range. The mask pattern bits are specified in CR30 & CR31 and the "don't care" bits are specified in CR28 & CR29.

3.4.3. OAM Cell CRC-10 Checking

If the recognised cell type for a received cell is one of the OAM cells, the CRC-10 field at the end of the payload may be checked. If an error is detected, the cell is discarded. This checking is controlled by the CRC10CHK bit in CR26.

3.4.4. Cell Extraction

Based on the recognised cell type, cells may be extracted (but not discarded from the data stream) to system memory using DMA. Cells may be extracted either by specific cell type or by explicitly matching (or not matching) the user mask. Cell extraction is controlled by CR32.

The extract buffer has space for four cells. Transfer of a cell by DMA will not start until the whole cell is in the buffer and the space will not be released until the whole cell has been transferred.

Extraction of OAM cells can be subject to checking of the CRC-10 field. If this checking is enabled, a cell with a CRC-10 error in the payload will not be extracted.

3.4.5. Cell Discard

Also based on the recognised cell type, cells may be discarded from the data passed to the transceiver interface, again either by specific cell type or by explicitly matching (or not matching) the user mask. Cell discarding is controlled by CR33.

3.4.6. Cell Insertion

Insertion of cells into the data stream towards the transceiver interface via DMA is carried out through a single-cell insert buffer. The peak insertion rate is controlled by the PKIR bits in CR26.

These give the number of cells which must be transmitted towards the transceiver interface for each cell which may be inserted (e.g PKIR3-0 = "0100" gives an insertion rate of 1 cell inserted per 512 cells (2^{13-4}) transmitted or approximately 0.2 % of the bandwidth).

In order to insert a cell in the data going to the transceiver interface, there must be a gap in the cells coming from the cell stream interface. This will occur if the current cell is to be discarded or if there is no cell available. The peak insertion rate will therefore only be attained if there are sufficient gaps in the data going to the transceiver interface, unless the INSPRI bit in CR26 is set. In this case, cells will be inserted at the maximum rate governed by the PKIR bits and, each time a cell is inserted, the cell coming from the cell stream interface will be delayed by one cell time.

The higher peak insertion rates will only be attained if the NTC's DMA latency can be satisfied by the host system bus.

3.4.7. Cell-based OAM Processing

If the unframed, cell-based physical interface is in use, the OAM Controller handles F1 & F3 PL-OAM cells autonomously. Cells of these types are inserted periodically into the data stream going to the transceiver interface. All other transmitted cells are copied to the OAM Controller in this mode to allow the calculation of the BIP error measurements.

3.4.8. OAM cell CRC-10 generation

If the cell inserted is an OAM cell, the CRC-10 field may be generated and placed at the end of the payload. If the CRC generation is not enabled, the data supplied from system memory or from the OAM Controller will be transmitted transparently. This is controlled by the CRC10GEN bit in CR26.

3.4.9. Idle Cell Generation

An idle cell will be generated and sent to the transceiver interface for cell rate decoupling if there is no other cell to be sent. This can arise if there is no data coming from the cell stream interface or if the current cell is to be discarded, and if there is no cell to be inserted or if the current cell to be inserted is being held back to comply with the peak insertion rate.

3.4.10. Cell Transmission

When a cell is transmitted, the HEC residue is calculated (using the polynomial $1 + x + x^2 + x^8$) over the four header bytes. The modulo-2 addition of the pattern "01010101" to the result of the HEC calculation is under user control by programming the HECMASK bit in CR27.

The user must select the required scrambling algorithm to match the physical interface in use by setting the SCRAM1-0 bits in CR27. For the STM-1 / STS-3c or E3 physical interfaces, the self-synchronous scrambler (with polynomial $1 + x^{43}$) is used. For the DS3 physical interface, no scrambling is required while for the unframed, cell-based physical interface. the distributed sample scrambler (with polynomial $1 + x^{28} + x^{31}$) is used.

3.5. Cell Stream Interface

A block diagram of the cell stream interface is illustrated in Fig. 15.

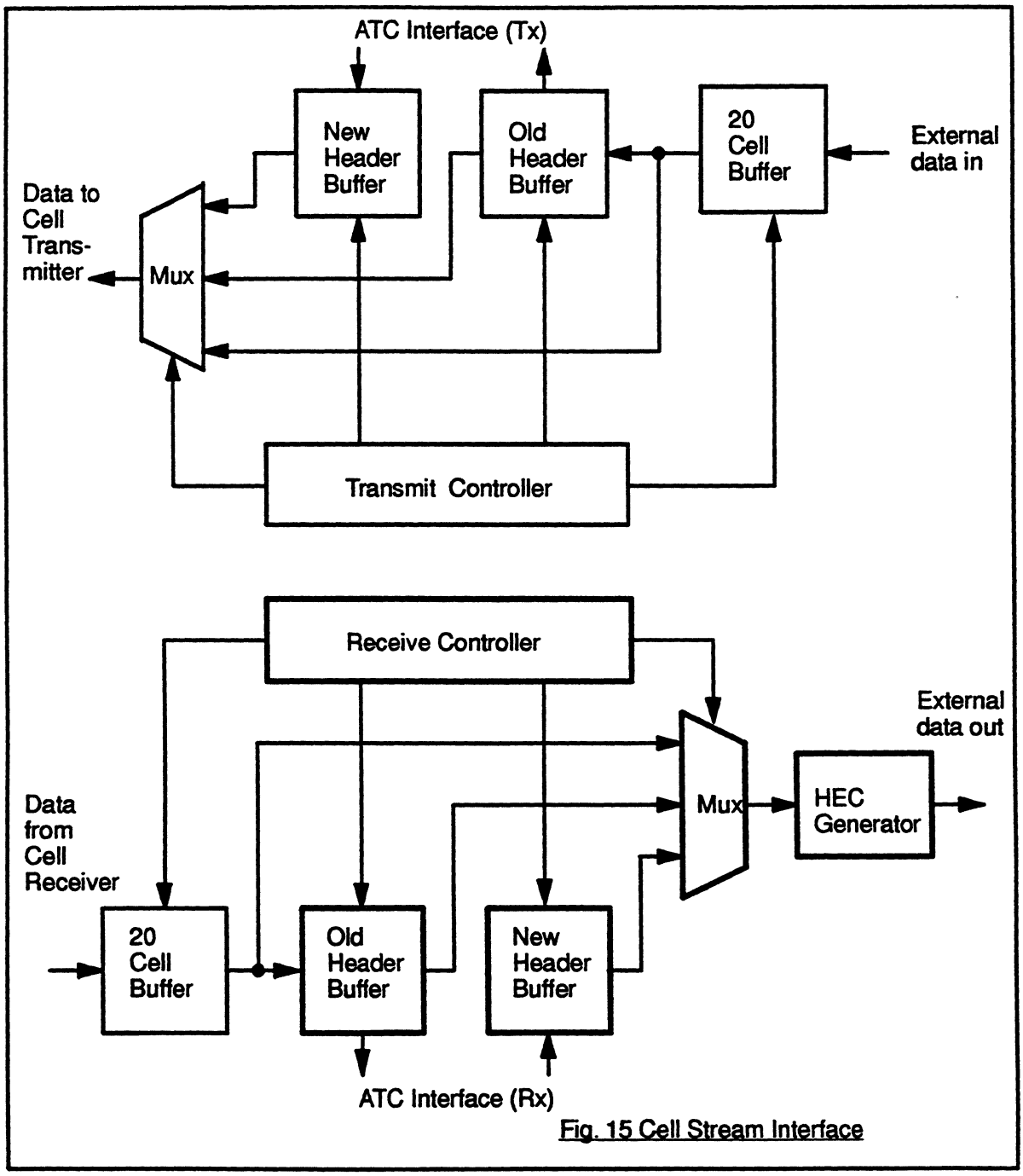


Fig. 15 Cell Stream Interface

3.5.1. CSI Basic Operation

The cell stream interface (CSI) transmits and receives a stream of ATM cells. Cells are transmitted and received in 8-bit parallel form with separate synchronisation inputs used to identify the start of a cell. Address translation may occur in either transmit and/or receive directions, or may be completely disabled.

Functions performed by the interface are:-

1 Cell reception initiated by start of cell indication.

2 FIFO buffering of 20 cells in both transmit and receive directions.

3 Receive path VPI/VCI address translation, optional tag generation (0, 1, 2, or 3 bytes) and HEC re-calculation.

4 Transmit path VPI/VCI address translation and tag removal, if present.

5 Congestion indication control for either receive or transmit paths.

6 Cell loss priority (CLP) indication for either receive or transmit paths.

7 Non-contiguous cell transmission.

The user has control over both the congestion indication bit contained within the payload type bits of the header, and the cell loss priority bit (CLP), for both transmit and receive directions.
There are 4 possible actions for each bit; use the bits returned from the address translation controller, use the original bits contained in the header, force to 0, or force to 1.

Multicasting is also supported in both directions. If the ATC finds more than one match for a particular header, the payload for that header is repeated for each new header.

Timing associated with both the transmit and receive asynchronous cell stream interfaces, with regard to basic function of the SOC signal and the tag length is illustrated in Fig. 16.

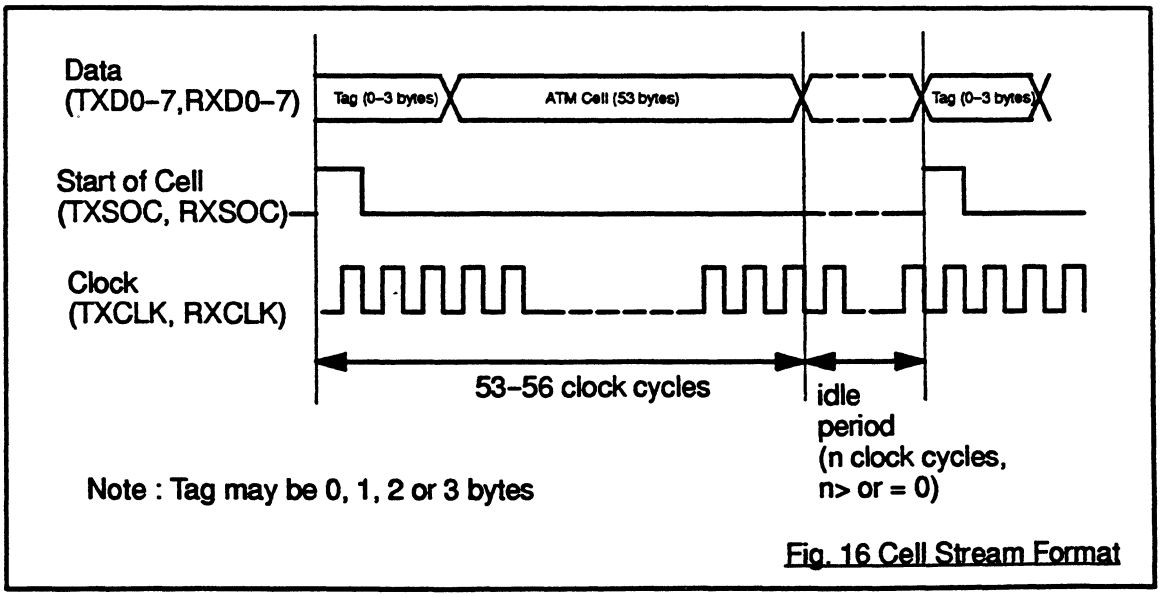


Fig. 16 Cell Stream Format

3.5.2. CSI Flow Control

Each of the interfaces include flow control signals, so that an external FIFO may be used to increase the effective buffer capacity from the current 20 cells. The basic function of these signals is shown below in Fig. 17 and Fig. 18. If flow control is not used, then RXEN and TXEN pins should be tied high, and the $\overline{\text{RXEMPTY}}$ and $\overline{\text{TXFULL}}$ outputs left unconnected.

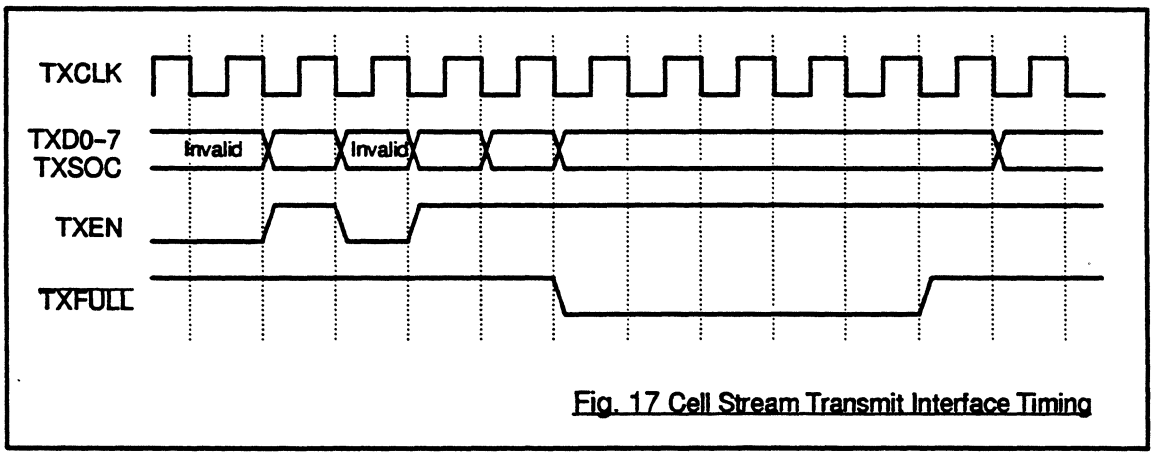


Fig. 17 Cell Stream Transmit Interface Timing

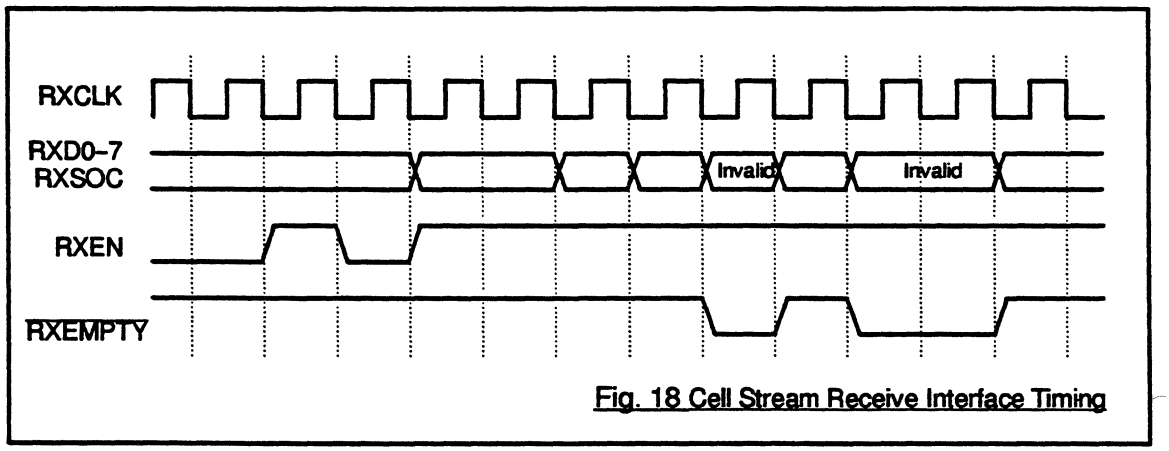


Fig. 18 Cell Stream Receive Interface Timing

3.5.3. ATC Interfaces

The Cell Stream Interface also includes interfaces to connect directly to two MB86689 Address Translation Controller (ATC) devices, one in the receive and one in the transmit directions. Either of these interfaces may be independently disabled if not required.

The purpose of the interfaces is to pass a VPI/VCI combination to the ATC where an address translation will be performed, and then receive the new cell header back from the ATC. The cell with its new header will then be passed on to either the Cell Stream, or to the cell transmitter. In addition to the basic address translation, an ATC in the receive path will attach a 3 byte routing tag to the beginning of the header. This tag is used for routing with the switch matrix. Full explanations of the translation capabilities of the ATC, and of the routing tag allocation for the SRE, are available in the respective MB86689 and MB86680 datasheets.

Both interfaces are identical in function. All transfers are timed to the NTC system clock (RXCLK). Outputs change on the positive edge of this clock, and input data is sampled on the rising edge. The data is transferred using a bi-directional bus. There are 4 hand-shaking signals used to control the data flow. The basic timing of the ATC interface is illustrated in Fig. 19 and Fig. 20.

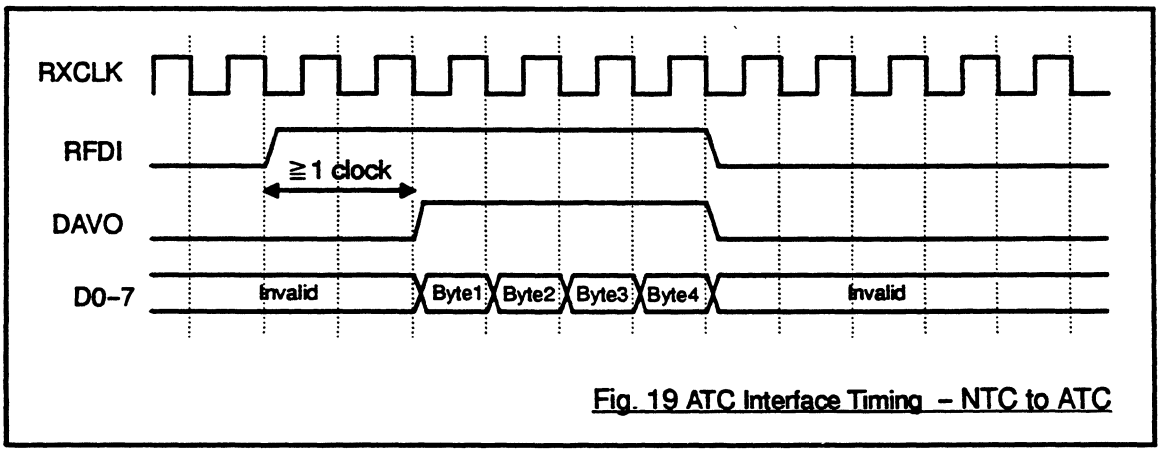


Fig. 19 ATC Interface Timing - NTC to ATC

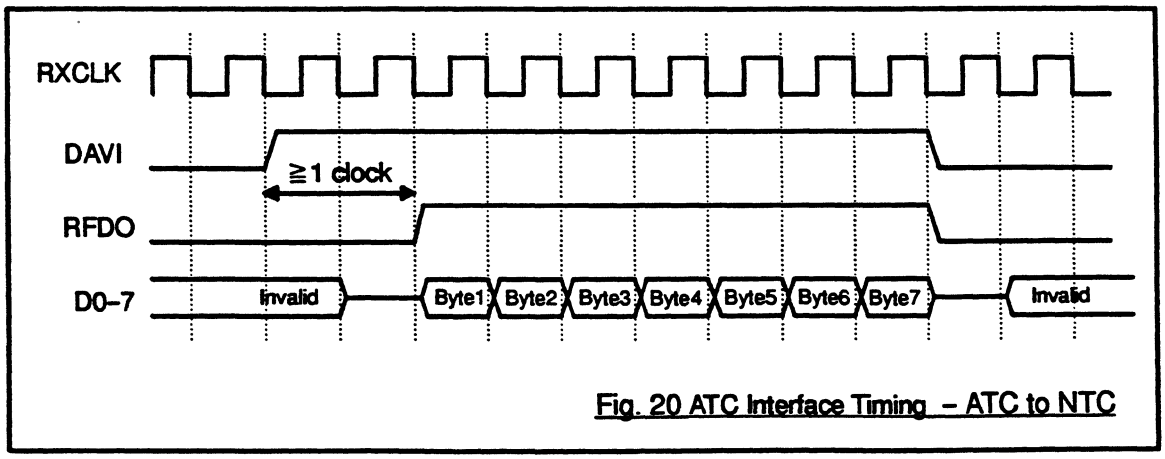


Fig. 20 ATC Interface Timing - ATC to NTC

The format of the data transferred over the ATC interface is illustrated in Fig. 21. The complete cell header (excluding the HEC byte) is transferred from the NTC to the ATC . When data is transferred from the ATC to the NTC, then the data includes a 3 byte routing tag together with 4 bytes of header. The ATC only sends 1 bit of the 3-bit PLT field to indicate congestion. The NTC places this bit in the second PLT bit position, as long as the first PLT bit is zero. If the first PLT bit is a one, then this indicates a non user-data cell, and hence the congestion indication bit is not applicable.

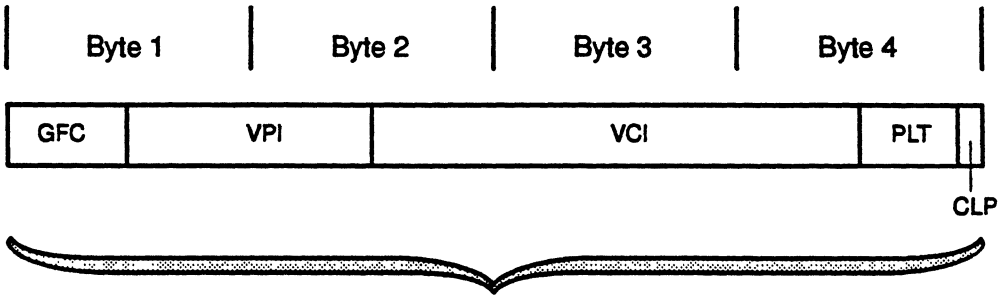


Fig. 21 ATC Interface Data Format - NTC to ATC

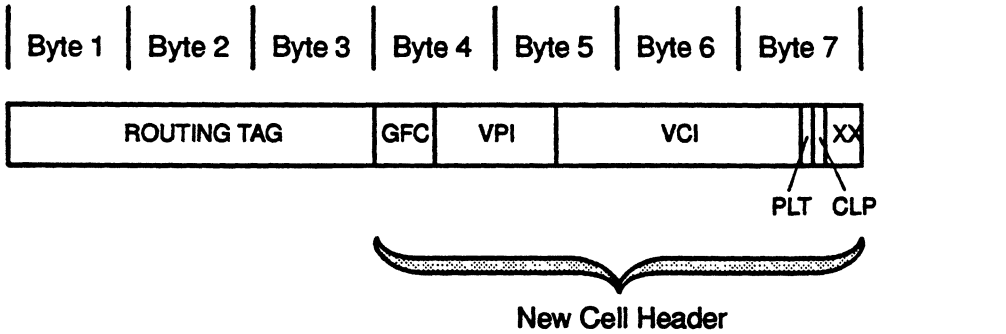


Fig. 22 ATC Interface Data Format - ATC to NTC

3.6. OAM Controller

A simplified block diagram of the OAM controller is shown in Fig. 23.

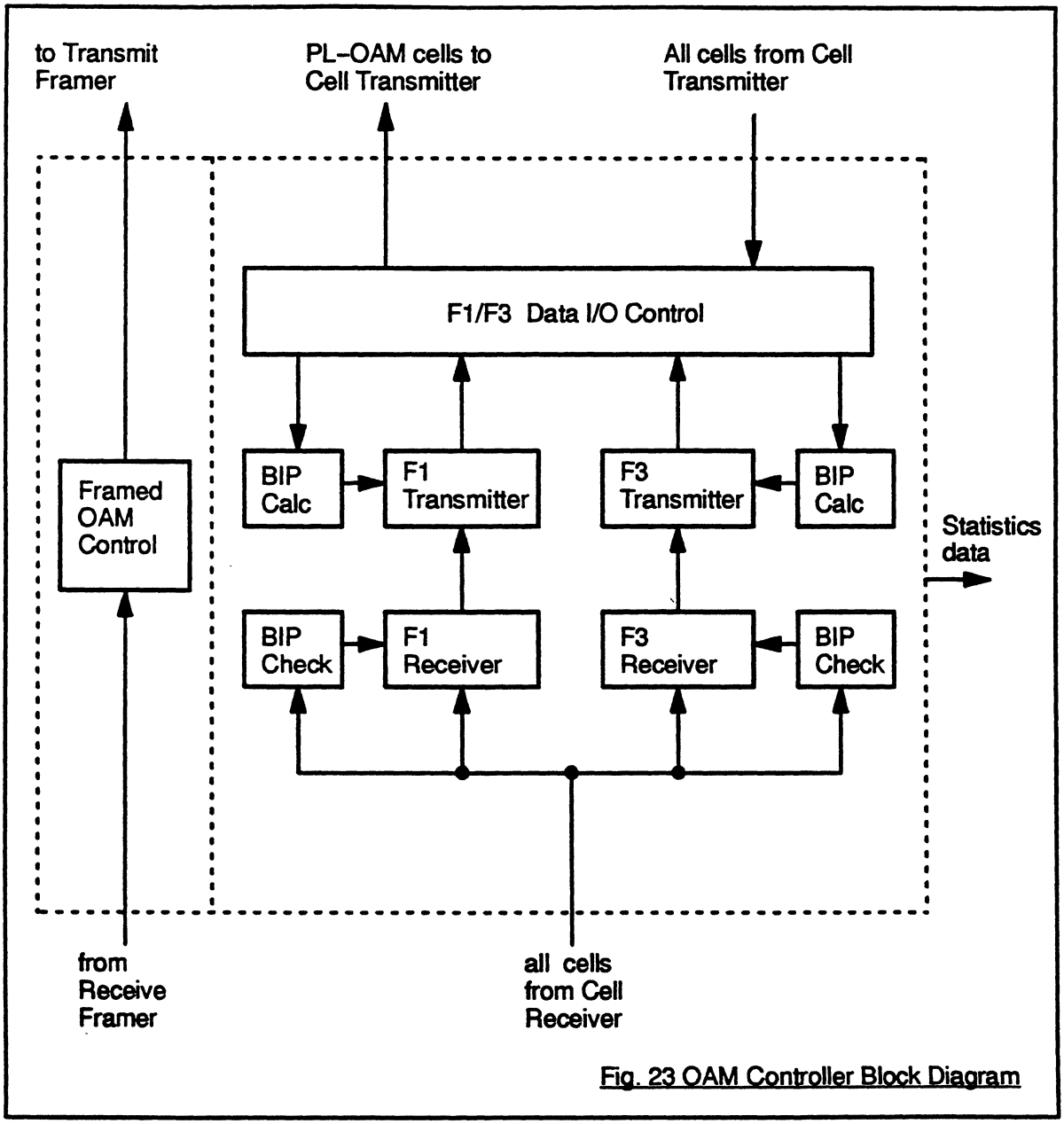


Fig. 23 OAM Controller Block Diagram

3.6.1. Basic Operation

The Operation, Administration and Maintenance (OAM) controller is divided into two main sections. One section controls the physical layer OAM (PL-OAM) functions associated with framed modes such as STM-1, SONET, DS-3 and E3. The other section controls PL-OAM functions when used in an unframed cell-based mode, as defined in CCITT I.432. In this mode, additional cells are used to carry the overhead information.

In both cases, received physical layer alarms are indicated in a status register.

3.6.2. Framed PL-OAM

An example of framed PL-OAM would be with STM-1 frames. In this mode, the error monitoring and reporting is performed by using overhead bytes which carry the B1/B2/B3 BIP calculations and FEBE/FERF results. The BIPs are calculated in the receive framer on receive data. These BIPs are then verified with the BIPs which are extracted from the received overhead bytes. Any resulting difference is indicated using a FEBE (Far End Block Error) which is passed over to the transmit framer for inclusion in outgoing frames.
Similarly for DS3 and E3 frames, the error monitoring and reporting information is carried in overhead bytes.

The OAM controller receives the following information from the receive framer, some of which may only be relevant to certain modes of operation:-

1 Section alarm indication signal (MS-AIS).

2 Section far end receive failure indication (MS-FERF).

3 Path alarm indication signal (P-AIS).

4 Path far end receive failure indication (P-FERF).

5 RAI indication.

6 Calculated section far end block error count (B2 FEBE).

7 Calculated path far end block error count (B3 FEBE).

8 Extracted section far end block error count (B2 FEBE).

9 Extracted path far end block error count (B3 FEBE).

10 Received B1/B2/B3 error indications.

11 Loss of pointer indication.

12 Loss of frame indication.

The OAM controller sends the following information to the transmit framer for inclusion into outgoing frames :-

1 Section alarm indication signal (MS-AIS).

2 Section far end receive failure indication (MS-FERF).

3 Path alarm indication signal (P-AIS).

4 Path far end receive failure indication (P-FERF).

5 RAI indication.

6 Calculated section far end block error count (B2 FEBE).

7 Calculated path far end block error count (B3 FEBE).

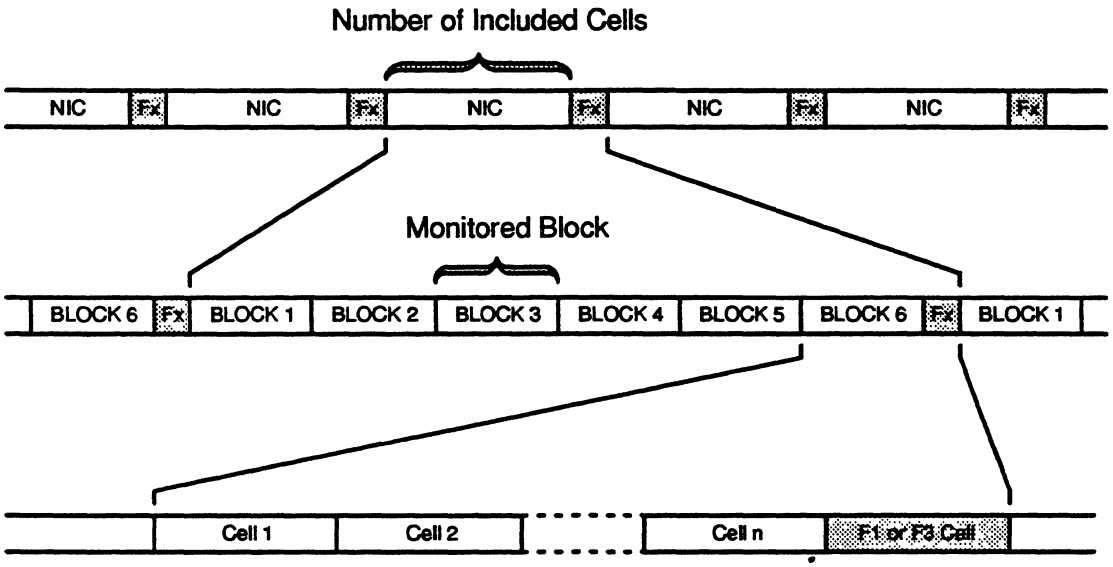
The OAM controller provides the FEBE counts extracted from the receive data to the statistics controller for recording into the Network Statistics Record (NSR).

3.6.3. Unframed PL-OAM

For cell based transmission systems, there is no inherent error monitoring/reporting because there are no overhead bytes. In this case, error monitoring/reporting is performed by inserting additional cells into the stream which are used only by the physical layer and are termed F1 or F3 PL-OAM cells.

F1 cells carry regenerator level OAM functions (same as B1 for STM-1), and F3 cells carry transmission path OAM functions (same as B3 for STM-1). F2 OAM flow is not used, but the functions are supported in F3 flow.

The principle of F1 and F3 PL-OAM flow is illustrated in Fig. 24.



Notes :

There can be between 1 and 8 monitored blocks.
This is known as the Number of Monitored Blocks (NMB)

Each monitored block can contain between 15 and 47 cells.
This is known as the Monitored Block Size (MBS)

Number of Included Cells (NIC) is derived by multiplying the Monitored Block Size by the Number of Monitored Blocks.

For F3 flow, the monitored block may contain ATM layer and Idle cells.

For F1 flow, the monitored block may contain ATM layer, Idle and F3 cells.

Both F1 and F3 flows are independent, and may have different NMB, MBS and NIC values.

Fig. 24 F1 and F3 PL-OAM Principle

F1 and F3 PL-OAM cells are recognised by unique cell header values as shown in Fig. 25.

The OAM controller sends F1 and F3 PL-OAM cells to the transceiver interface via the cell transmitter, at a selected rate, ie there will be a certain number of user (non-OAM) cells between successive F1/F3 cells. The rate is independently programmable between 26-512 user cells. The user may also specify that the data is partitioned into blocks of data, up to a maximum of 8 blocks. In this case 8 separate BIP-8 calculations will be performed on 8 continuous blocks of data between 2 successive F1 and/or F3 OAM cells. Any resulting FEBE/FERF errors will be reported and transmitted in outgoing frames. In common with the framed modes, the FEBE counts are extracted from the received F1 and F3 cells, and provided to the statistics controller, for recording into the NSR.

Any received F1/F3 cell may optionally have its CRC-10 checked, and if in error, the cell will be discarded. If the CRC checker is disabled, then all F1/F3 cells will be processed. Transmitted F1/F3 cells may have an appropriate CRC-10 field included.

FLOW	OCTET 1	OCTET 2	OCTET 3	OCTET 4
F1	00000000	00000000	00000000	00000011
F3	00000000	00000000	00000000	00001001

Fig. 25 F1 and F3 PL-OAM Cell Header Identification

The format of a PL-OAM cell payload as used for F1 and F3 flow is shown in Fig. 26.

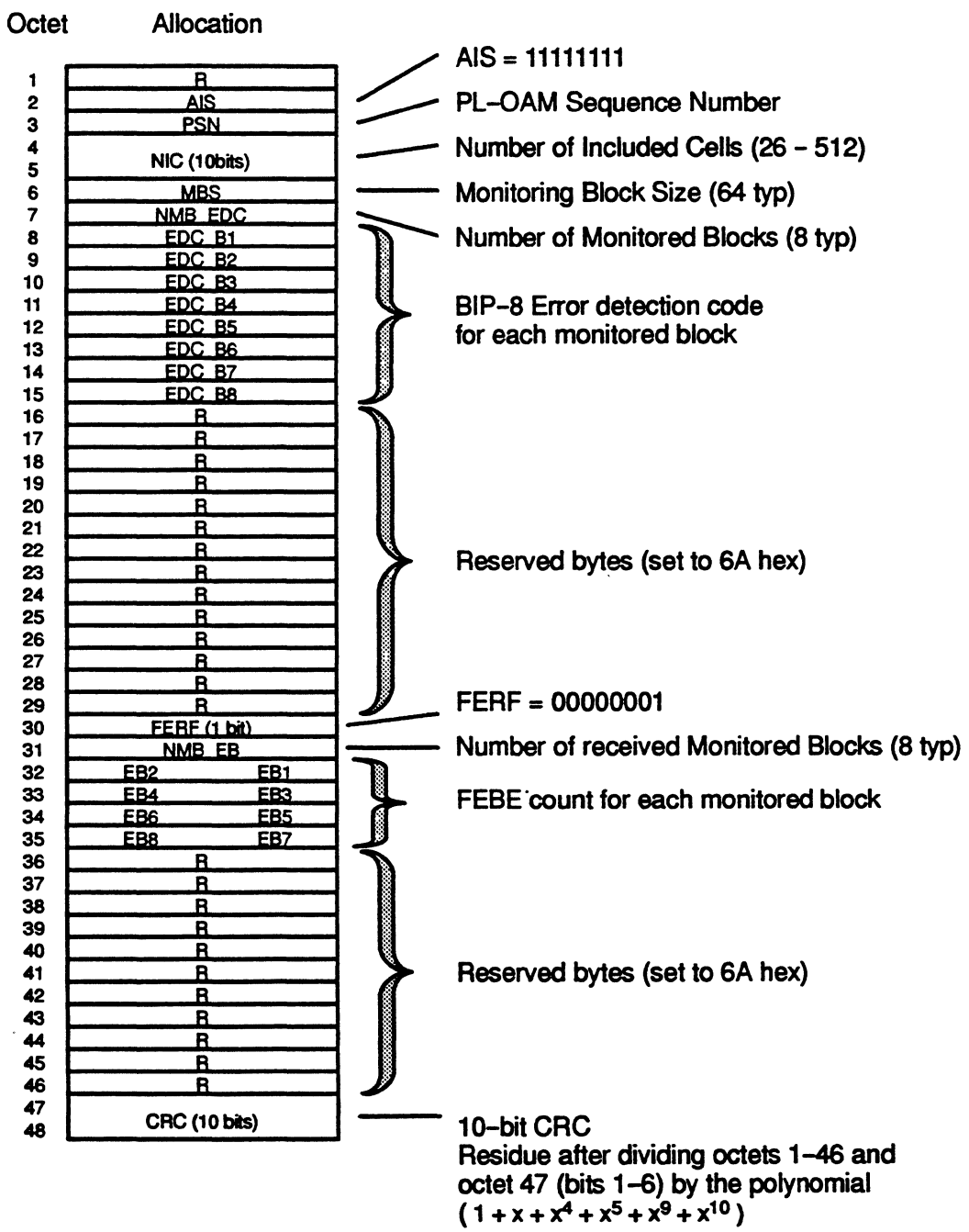


Fig. 26 F1 and F3 PL-OAM Cell Payload Format

3.7. Statistics Controller

The statistics controller maintains a record of the various events in a network statistics record (NSR), which is maintained in internal RAM, and will be transferred to system memory by DMA under certain conditions.

The NSR general format is illustrated in Fig. 27 along with the format of each user statistics entry. The format of the NSR header will be different for various physical interfaces and is shown in Fig. 28.

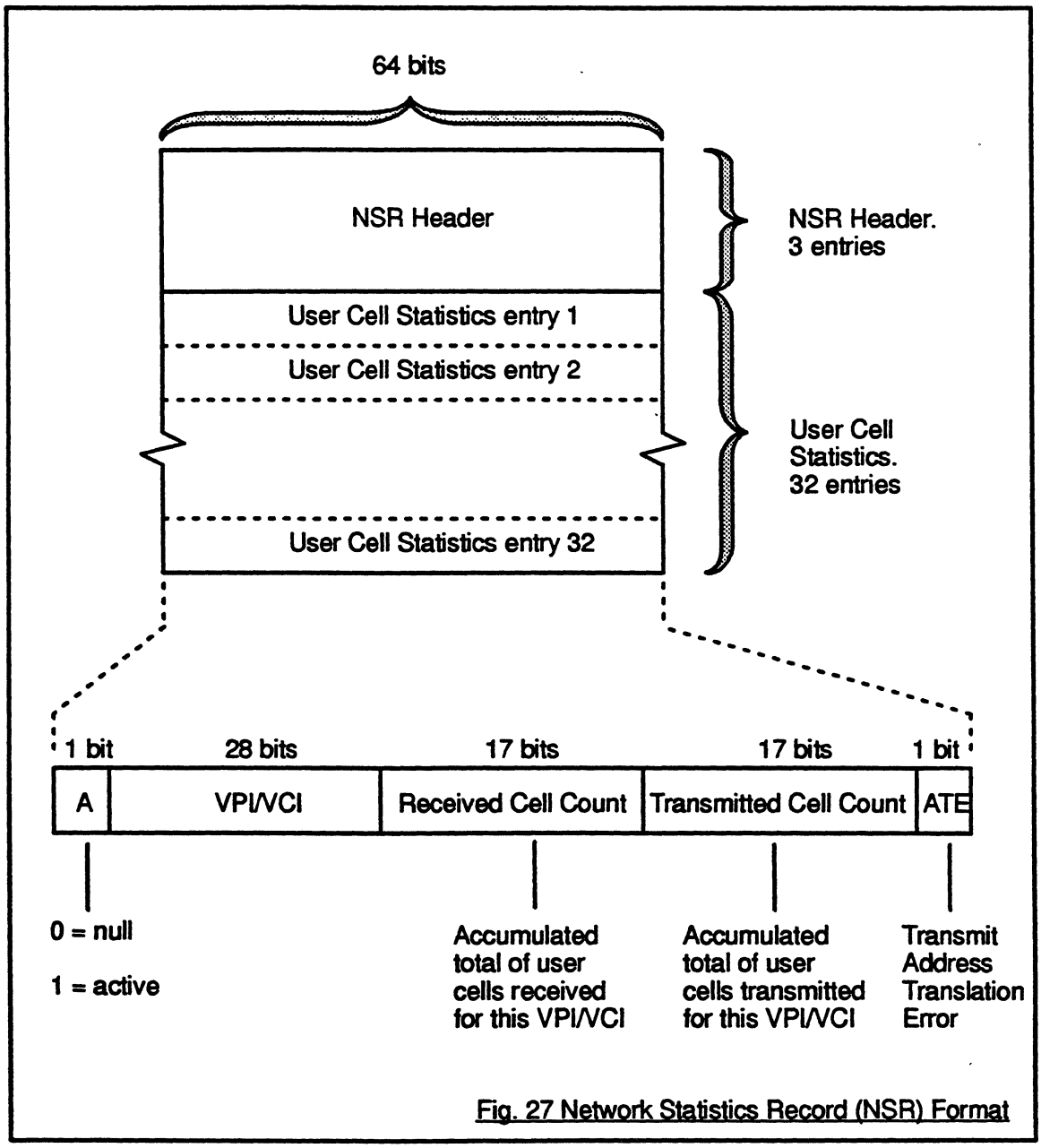


Fig. 27 Network Statistics Record (NSR) Format

NSR Header Format (STM-1)

32 bit timestamp		HEC detected count	HEC corrected count
Idle cell count (rx)	Idle cell count (tx)	B2 FEBE count	B3 FEBE count
Unassigned cell (rx)	Unassigned cell (tx)	User cell insert (rx)	User cell insert (tx)

NSR Header Format (DS-3 / PCLP)

32 bit timestamp		HEC detected count	-
Idle cell count (rx)	Idle cell count (tx)	-	G1 FEBE count
Unassigned cell (rx)	Unassigned cell (tx)	User cell insert (rx)	User cell insert (tx)

NSR Header Format (E3)

32 bit timestamp		HEC detected count	HEC corrected count
Idle cell count (rx)	Idle cell count (tx)	-	MA FEBE count
Unassigned cell (rx)	Unassigned cell (tx)	User cell insert (rx)	User cell insert (tx)

NSR Header Format (Cell based)

32 bit timestamp		HEC detected count	HEC corrected count
Idle cell count (rx)	Idle cell count (tx)	F1 FEBE count	F3 FEBE count
Unassigned cell (rx)	Unassigned cell (tx)	User cell insert (rx)	User cell insert (tx)

Fig. 28 NSR Header Formats

3.7.1. Basic Operation

Initially, all NSR header counters are set to zero. The timestamp counter is incremented on each transition of the system clock (RXCLK). Two different types of data may be received by the statistics controller. This is used to initiate updating of either the header section or the user cell entry section. This data is received from either the cell receiver, cell transmitter, OAM controller, or the ACSI.

Header Updating

Received data is used to update counts for :-

1. Number of HEC errors detected and corrected for received cells.
2. Physical layer received FEBE counts.
3. Number of idle cells received and transmitted.
4. Number of unassigned cells received (from transceiver or Cell Stream).
5. Number of user cells inserted (via cell receiver or transmitter).

User Cell Statistics Updating

All statistics entries will initially be set to their null state. A statistics entry will be set to its active state when a cell reception event is indicated by either the cell receiver or transmitter. On receiving such an event, the statistics controller will first check all active statistics entries to find whether an entry is active for the indicated VPI/VCI. If an entry is active then it will be updated accordingly, by incrementing the receive or transmit cell count. If no statistics entry is active, then a null entry will be activated and the appropriate information recorded. If no null entries are available, then the entire NSR will be transferred to the DMA controller for subsequent transfer to system memory, all active statistics entries will be set to null and a new entry will be recorded.

Statistics DMA Events

Several events will cause the NSR to be transferred and re-initialised as listed below:-

1 Programmable timeout based on a count from the last DMA transfer.

2 Reception of a new VPI/VCI event when no null entries are available.

3 Any counter reaching its maximum value.

After the NSR has been transferred, all counters will be set to zero.

Note that the 32-bit timestamp counter will reach its maximum value in 214 seconds when clocked at 20 MHz. The maximum time of the programmable timeout is 2^{22} x clock period, which equals 3.14 seconds at 20 MHz. Hence, it will be possible to derive the time relation between successive NSR records, using the timestamp values.

3.7.2. Stats Controller DMA Format

The DMA transfer will take either 70 or 140 transfers, depending on the bus width being 32 or 16-bits. The DMA transfer should be completed before the buffer overflows. If this is not the case, then a buffer overflow interrupt will be generated. Data is transferred by reading the NSR from top to bottom, left to right.

3.8. Switch Statistics Handler

The Switch Statistics Handler (SSH) interfaces to the switch matrix, formed from SRE devices, via the serial statistics daisy chain mechanism. Its purpose is to collect any valid payload statistics from the serial data stream, remove any of the synchronisation flags and format the data into a 54 bit word ready for transfer to system memory via the NTC DMA controller. The host processor can then use this statistics data to control any congestion within the switch matrix.
A block diagram of the switch statistics handler is illustrated in Fig. 29

3.8.1. Switch Statistics Frame Format

The received serial data stream is formatted into packets, similar to HDLC frames. Each frame may be either carrying statistics data (BUSY), or may contain empty payload data (IDLE). Idle packets are used to ensure a constant stream of data. Each frame is fixed at 90 bits and consists of the following; an 8-bit synchronisation flag, a 1-bit flag to indicate an idle or busy frame, a statistics payload which can vary between 54-65 bits due to bit stuffing, an 8-bit closing flag, and an idle period which varies between 19-8 bits to accommodate the bit stuffing.
A diagram of the switch statistics frame without bit stuffing is shown in Fig. 30.

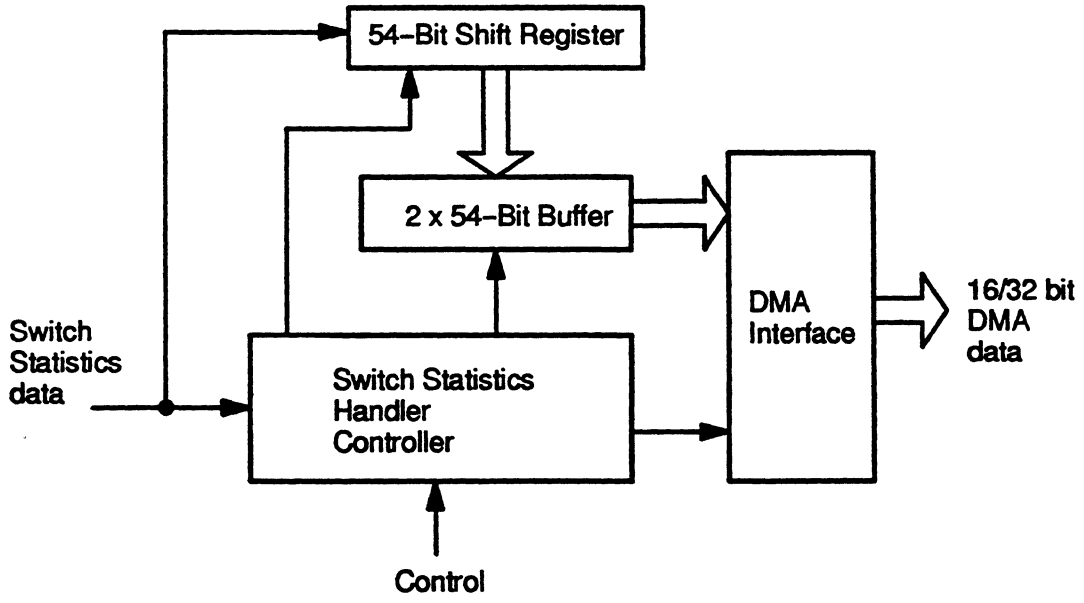
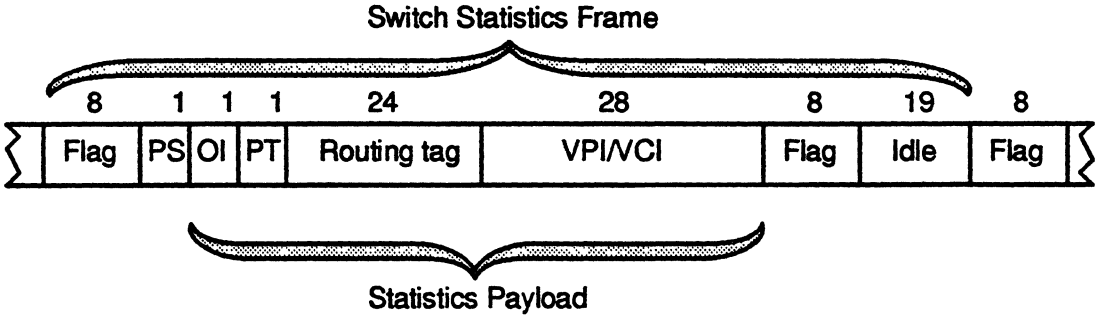


Fig. 29 Switch Statistics Handler Block Diagram



Flag	=	01111110	
PS	=	statistics payload status :	0 = IDLE 1 = BUSY
OI	=	statistics buffer overflow : indication	0 = Normal 1 = Multiple stats buffer overflow
PT	=	statistics payload type :	0 = Normal CLP discard 1 = SRE buffer overflow discard

Fig. 30 Switch Statistics Frame Format

3.8.2. Switch Statistics Operation

The statistics handler will clock data in on the rising edge of the STATSCLK clock input. This clock may be asynchronous to the other NTC clock inputs, but its frequency must be less than the system clock (RXCLK).

Initially, the switch statistics handler state machine will search for the 8-bit flag pattern. On detecting this, it will then expect a 1 to indicate a BUSY payload. If it detects a 0, then the frame is IDLE and contains no switch statistics information.

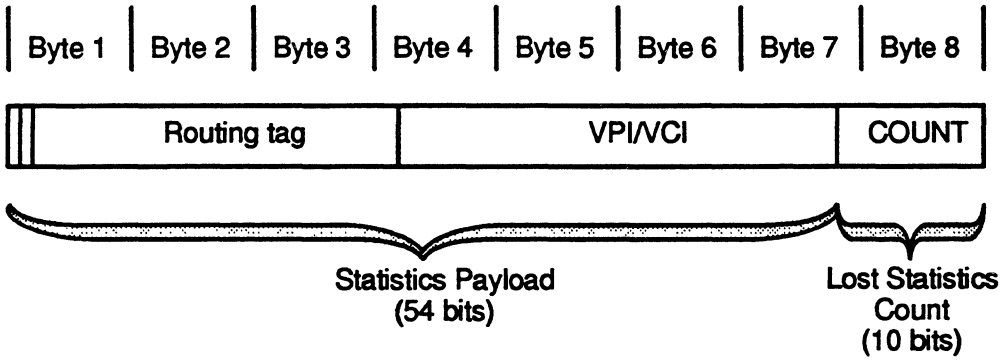
Once it has found a BUSY payload, the payload will be loaded into a 54-bit register. Any inserted zero bits will first be removed by counting for 5 consecutive 1's and removing the following 0. Once a complete 54-bit statistics payload has been received, the controller will latch this data into a buffer capable of storing up to 2 54-bit words. The controller will then indicate to the DMA controller that a transfer is requested.

3.8.3. Switch Statistics DMA Format

The DMA transfer will take either 2 or 4 transfers, depending on the bus width being 32 or 16-bits. The DMA transfer should be completed before the buffer overflows. If this is not the case, then a count of lost statistics payloads will be recorded and sent out in the next statistics transfer. All DMA transfers will be done as 64-bit blocks, and as only 54 bits are used for statistics, the lost payload count will be recorded in the remaining 10 bits of the statistics block.

It is expected that statistics data should not be lost because the statistics clock rate will generally be much slower than the DMA clock.

The DMA byte format is illustrated in the Fig. 31. The data is passed to the DMA controller in this format, but the actual format which will be output from the NTC data pins may vary depending on the microprocessor mode (eg big or little endian etc).



msb lsb

Byte 1	Byte 2
Byte 3	Byte 4
Byte 5	Byte 6
Byte 7	Byte 8

16-bit mode

msb lsb

Byte 1	Byte 2	Byte 3	Byte 4
Byte 5	Byte 6	Byte 7	Byte 8

32-bit mode

Fig. 31 Switch Statistics DMA Format

3.9. DMA Controller

3.9.1. Basic Operation

The DMA controller allows data to be transferred between the NTC and system memory at high speed without processor intervention. The DMA controller comprises 6 separate channels which perform the following functions:-

0 NTC Statistics Channel. This channel facilitates the autonomous transfer of network statistics records (NSRs) to system memory.

1 Switch Statistics Channel. This channel facilitates the autonomous transfer of switch statistics payloads to system memory.

2 Cell Receiver General Purpose Cell Extract Channel (CRX Extract). This channel facilitates the transfer of 52 byte cells received from the NTC transceiver interface to system memory.

3 Cell Receiver General Purpose Cell Insert (CRX Insert). Channel. This channel facilitates the transfer of 52 byte cells from system memory to the NTC for transmission via the cell stream interface.

4 Cell Transmitter General Purpose Cell Extract Channel (CTX Extract). This channel facilitates the transfer of 52 byte cells received from the NTC cell stream interface to system memory.

5 Cell Transmitter General Purpose Cell Insert Channel (CTX Insert). This channel facilitates the transfer of 52 byte cells from system memory to the NTC for transmission via the transceiver interface.

In all cases automatic chaining is supported, which allows multiple system memory buffers to be allocated to each channel.

The above functions are mapped onto DMA channels 0 - 5 according to the following table:-

DMA Channel No.	Function	Direction	Burst Size
0	NTC Statistics	From NTC to memory	280 bytes
1	Switch Statistics	From NTC to memory	8 bytes
2	CRX Extract	From NTC to Memory	52 bytes
3	CRX Insert	From Memory to NTC	52 bytes
4	CTX Extract	From NTC to memory	52 bytes
5	CTX Insert	From memory to NTC	52 bytes

3.9.2. DMA Descriptors

Each DMA channel requires a descriptor which is held in system memory. The NTC maintains an address which identifies the position of a descriptor table which is also held in system memory. The descriptor location table comprises pointers to descriptors for each DMA channel. The descriptors themselves may contain a pointer to the address of a further descriptor which may be used to form a chain of descriptors.
The principle of the descriptor table, together with chained descriptors is illustrated in Fig. 32.

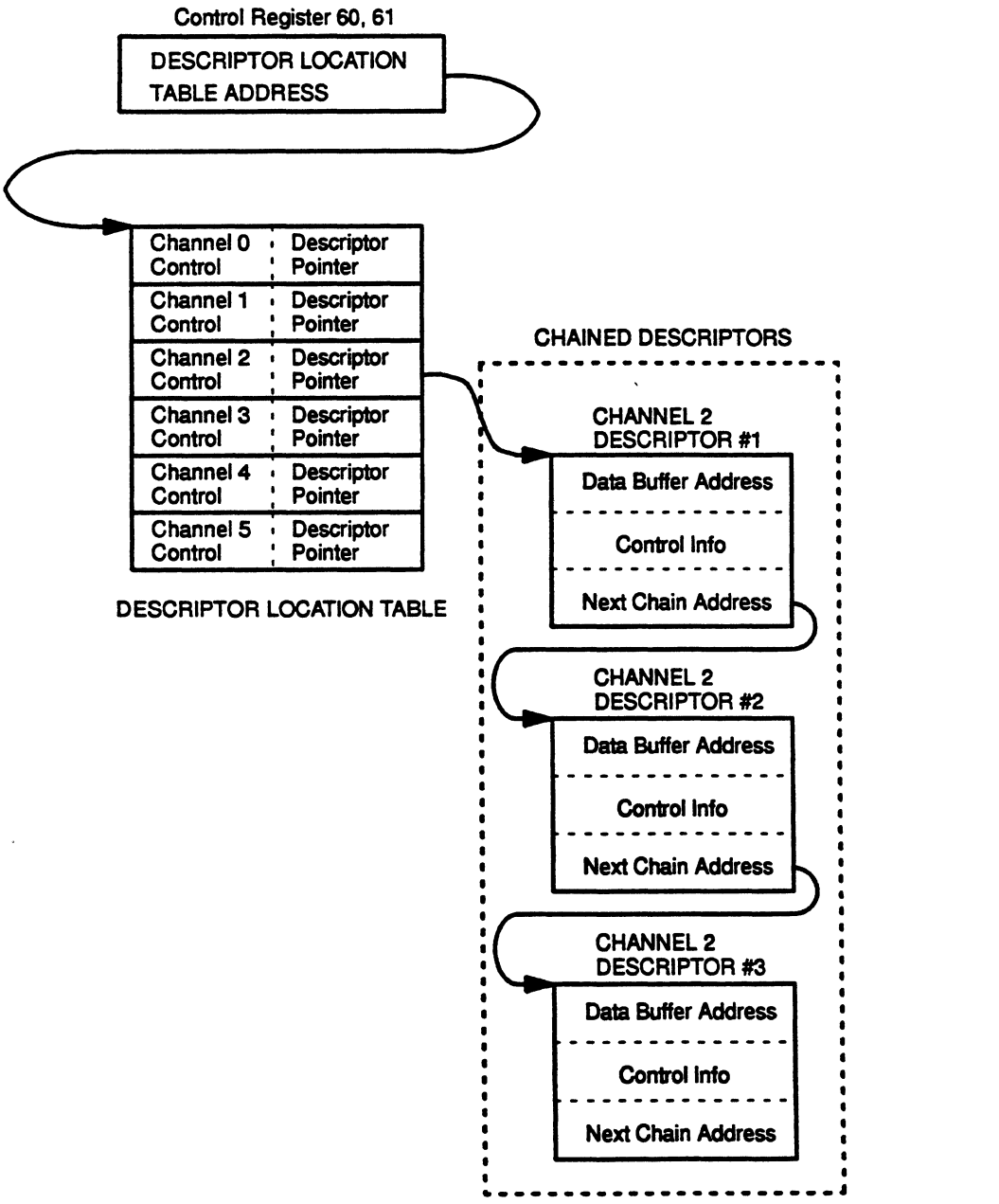


Fig. 32 Descriptor Principle

3.9.3. Descriptor Location Table

The format of the descriptor location table varies depending on whether the bus size is configured for 32 or 16 bits. In both cases, the table contains two main information fields for each of the 6 channels. These fields are an 8-bit Channel Control Register (CCR) and a 24-bit Descriptor Pointer (DP) address. This is illustrated in Fig. 33.

The value of the DP field should contain the physical address divided by two, since A0 is always assumed to be 0.

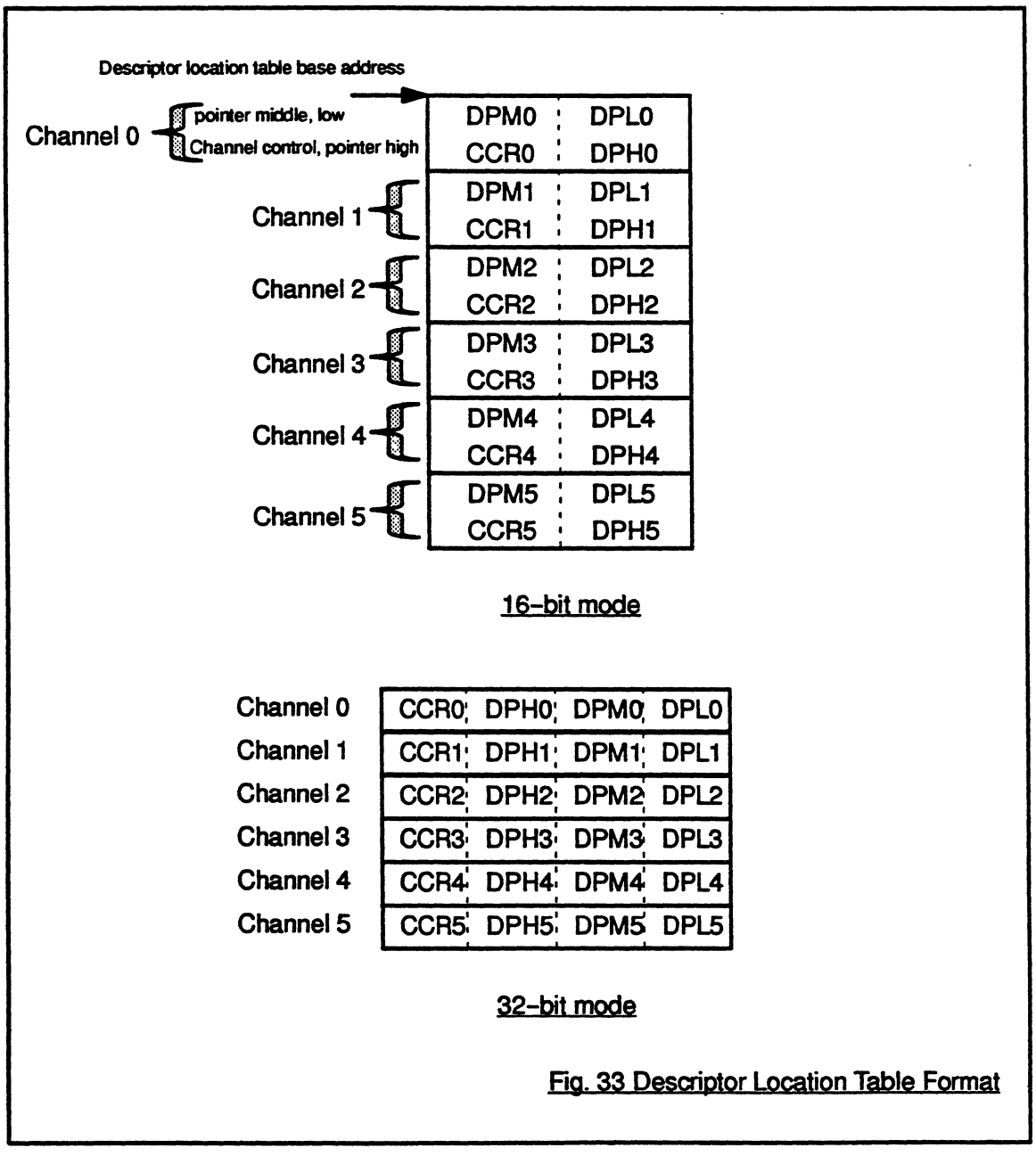
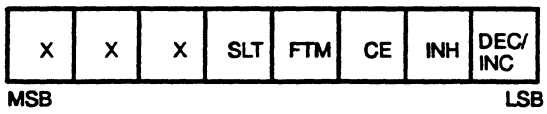


Fig. 33 Descriptor Location Table Format

3.9.4. Channel Control Register

Each channel has an associated channel control register (CCR) which is contained in the descriptor location table as illustrated in Fig. 33. This register will be loaded into the NTC when the channel is first enabled. The CCR has the following format:-



- Decrement / Increment (DEC/INC)
The DEC/INC bit determines whether the address register is incremented or decremented during data transfer. When this bit is "1" the address register will be incremented, and when this bit is "0" the address register will be decremented.

- Inhibit (INH)
The INH bit inhibits the address register from being incremented or decremented. When this bit is "1" data transfer will be performed at the initial block address only. When this bit is "0" the block address will be incremented or decremented as specified by the DEC/INC bit.

- Chaining Enable (CE)
The CE bit controls chaining operation. When this bit is "1" chaining is dependent on the CHE bit in the descriptor BCF field. When this bit is "0" chaining is disabled.

- Fast Transfer Mode (FTM)
The FTM bit is used to determine whether the READY input affects the DMA transfer cycle.
If this bit is set to "1", the READY input has no effect and the DMA transfer cycle is fixed at 4 system clock periods.
If this bit is set to "0", the READY input wil be sampled in every DMA transfer cycle and the cycle may be extended by any number of system clocks ($\geqq$ 0) to allow for slower memory systems.

- Select (SLT)
The SLT bit selects the direction of data transfer. When this bit is "1" NTC to memory transfers will occur. When this bit is set to "0" memory to NTC transfers will occur. This bit will be fixed for each particular channel, as the direction is fixed on a per channel basis.

3.9.5. Descriptor Format

For each DMA channel, the descriptor indicates the number of 16-bit words to be transferred, start address, and control information. When a channel is first enabled, the DMA controller will locate and load the associated descriptor address and control field using a burst mode transfer. When the DMA controller completes a block transfer, it will write status information into the current descriptor and will then read the start address of the next descriptor in the chain, if chaining is enabled. An interrupt will be generated on completion of a block transfer.

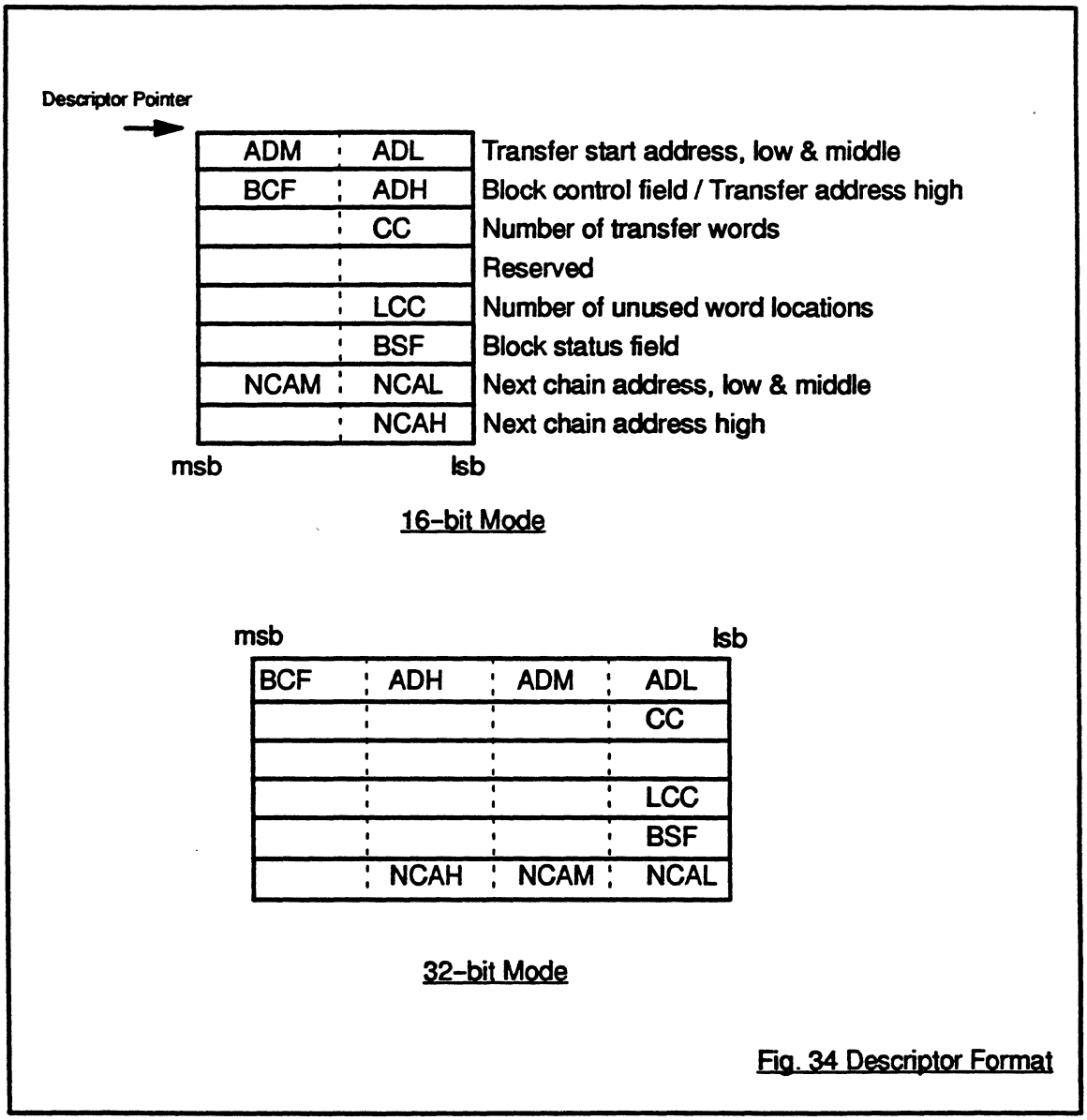


Fig. 34 Descriptor Format

3.9.6. Descriptor Control Fields

The meaning of each descriptor control field is given below. Any unused fields in the descriptor are ignored :-

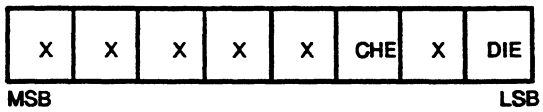
Start Address Field (ADL, ADM, ADH)
This field specifies the start address of a block. Data will be transferred with the address incrementing or decrementing or static, depending on the DEC/INC and INH bits of the CCR.
The value of the Start Address Field should contain the physical address divided by two.

Character Count Field (CC)
This field specifies the block size in 16-bit words. When the number of words specified by the character count field have been transferred, the current block transfer will be terminated.

Last Character Count Field (LCC)
This field will be used to indicate the number of remaining words in a block when a block transfer is terminated.

Next Chain Address (NCAL, NCAM, NCAH)
This field indicates the start address of the next DMA descriptor in a chain. This field will be read into the DMA controller at the end of a block transfer when chaining is enabled.
The value of the Next Chain Address Field should contain the physical address divided by two.

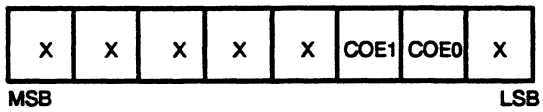
Block Control Field (BCF)
The block control field has the following format:-



- DMA Interrupt Enable (DIE)
This bit should be set to 1 to cause an interrupt to be generated after the associated block transfer has been completed.

- Chaining Enable (CHE)
This bit should be set to 1 to enable chaining at the end of a block transfer.

Block Status Field (BSF)
This field will be written by the DMA controller at the end of a block transfer operation. It has the following format:-



- COE0
This bit will be set when a block transfer operation has been terminated by the character count register reaching zero.
Hence, a successful transfer has occurred.

- COE1
This bit will be set when a block transfer operation has been terminated by the DMA channel enable bit being reset during operation.

3.9.7. Data Transfer Operations

A data transfer operation will be initiated when an internal function requires to transfer some data. The DMA controller will then request use of the system bus by activating the bus request output signal. The DMA controller will then wait for the external processor to grant it use of the bus, and it will then initiate a transfer cycle.

After it has been granted use of the system bus, the DMA controller will transfer the required data in a single burst. Hence ATM cells will be transferred in 52 byte bursts, and network statistics records will be transferred in 280 byte bursts (ie. 70 write cycles of 32 bits, or 140 write cycles of 16 bits). It is possible to reduce the time that the DMA holds the bus by chaining descriptors.

For example, the Network Statistics Record (NSR - channel 0) requires 280 bytes to be transferred. This could be done either as one block transfer of 140 16-bit words, or by breaking the transfer into 4 separate blocks by chaining 4 descriptors. The DMA will request the bus at the end of each block transfer, and hence the processor will have access at these points to accept or deny the request.

3.10. Microprocessor Interface

The microprocessor interface has two basic functions. One is to act as an asynchronous slave for microprocessor access to NTC internal registers, and the other is as an asynchronous master for the DMA transfer of data between the NTC and system memory.

3.10.1. Processor Register Access

The device is in slave mode when the NTC does not have control of the system bus, the data bus can be configured to be either 16 or 32-bits wide. All internal registers are 16-bits wide. A table showing the control and status registers is shown in section 5. Complete descriptions of all the register bits are given in section 6.

16-Bit Mode

In 16-bit mode, only word transfers are allowed in order that registers are not partially loaded or read. Read and write operations are made via the RD, WR, BHE, A0 and CS signals when in INTEL mode and AS, R/W, LDS, UDS and CS in MOTOROLA mode. In both modes the cycles are terminated by the NTC via the RDYOUT output pin.
In 16-bit mode register access, there is no difference in byte ordering between little endian and big endian systems, since the transfers are seen as single 16-bit words and not two 8-bit bytes.

32-Bit Mode

In 32-bit mode transfers can be either words (but only on word boundaries) or long words. In INTEL mode, read and write transfers are controlled via the RD, WR, BE0-3 and CS signals, and in MOTOROLA mode by the AS, R/W, DS A0-1, SIZ0-1 and CS signals. In common with 16-bit mode, the NTC terminates these cycles via the RDYOUT signal.

Since the bus size is now 32-bits wide and the registers are only 16-bits wide the difference between big endian and little endian needs to be considered. When in INTEL mode and the BSWAP pin (bus swap) is inactive, the configuration will be little endian and registers will be numbered right to left.
When in INTEL mode with BSWAP active, or in Motorola mode, the configuration is big endian with registers numbered left to right. This is illustrated in Fig. 35 and Fig. 36.

3.10.1.1. Cycle Termination - RDYOUT

Due to internal synchronisation, there is a minimum time in NTC clock cycles between consecutive write cycles and write read cycles. In order to allow software to be written independently of this, the RDYOUT signal is provided which is used by the host to insert wait cycles.

The RDYOUT signal is asynchronous and when high indicates to the host that the present cycle can be terminated, as long as the minimum cycle time has been satisfied. When the NTC is not being accessed the RDYOUT signal is always inactive.

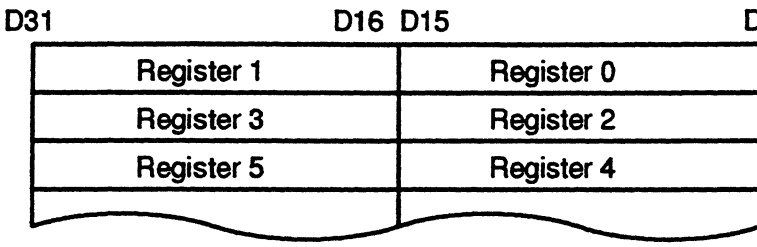


Fig. 35 Little Endian Configuration

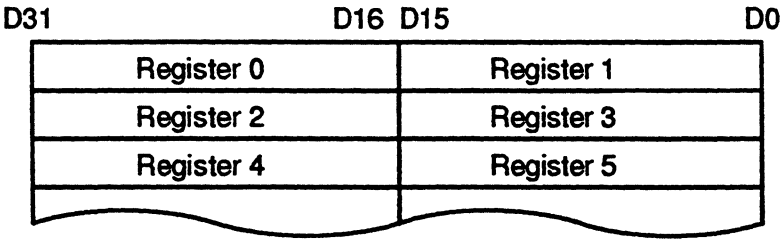


Fig. 36 Big Endian Configuration

3.10.2. DMA Arbitration and Chaining

DMA arbitration for control of the system bus is asynchronous, and is fully compliant with both INTEL and MOTOROLA bus cycles. Multiple NTC's can be chained together without the need of an external bus arbiter using proprietary signals. This is described below for both INTEL and MOTOROLA modes.

3.10.2.1. INTEL Mode Arbitration

When in INTEL mode, DMA arbitration is accomplished using the HOLD and HLDA signals, the HOLD signal is tristate when inactive to allow it to be connected in a wired OR configuration with other signals and therefore needs a pull down resistor of 2K7Ω. A DMA transfer can be suspended by negating the HLDA signal and forcing a control overide. The NTC will request the bus after two clock cycles and once it has gained control, it will continue from were it was suspended.

3.10.2.2. INTEL Mode Chaining

A number of NTC's can be chained together without the need of an external arbiter by using the DCOUT signal. This is illustrated in Fig. 37. To the host it appears as if there is only one device. During a DMA cycle with chained NTCs, the control of the bus is simply passed down the chain with NTC's individually controlling the bus if required. At the end of the chain, the bus will be released if a device has passed the token on. Further DMA transfers must will wait until the present chaining cycle has finished and the bus released before requesting the bus. This is to prevent chained NTCs from dominating the bus. If control overide cycles are required when using chains of NTC's the CONT signals must be connected together in a wired OR configuration and pulled low with a 2K7Ω resistor. This signal is used by the present bus master to inform other devices further down the chain that a control overide has occurred and they must cease requesting the bus.

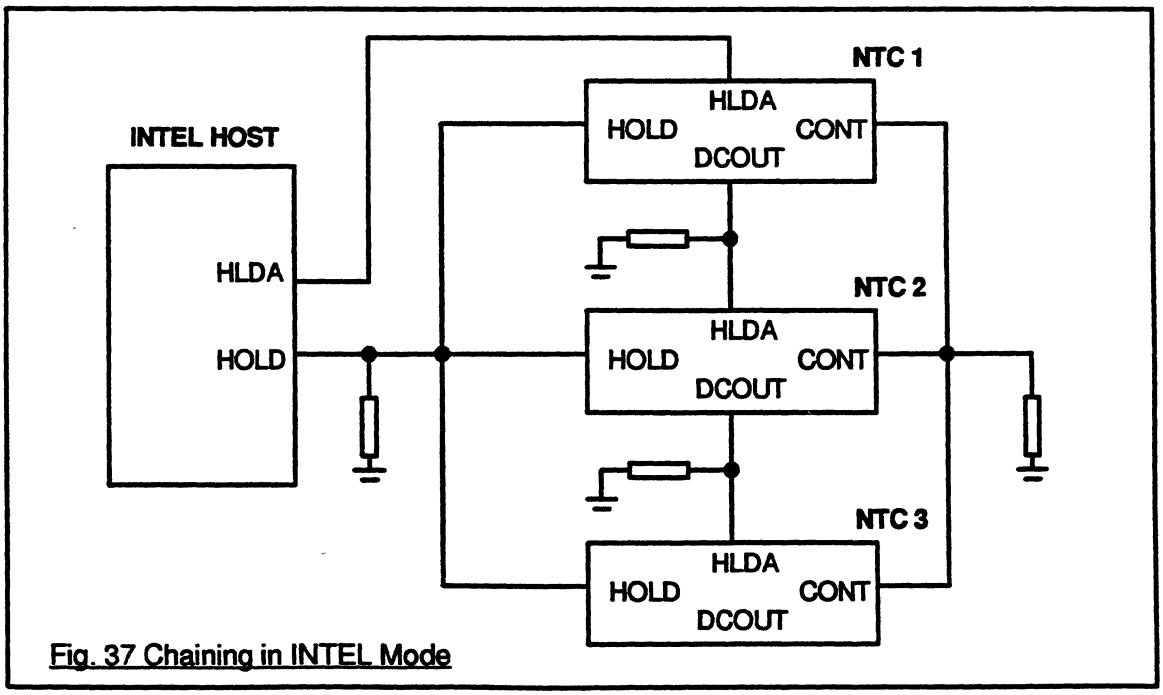


Fig. 37 Chaining in INTEL Mode

3.10.2.3.MOTOROLA Mode Arbitration

When in MOTOROLA mode, DMA arbitration is accomplished using the BR, BG and BGACK signals. AS and DTACK are also monitored to indicate the end of a cycle. Both BR and BGACK are tristate when inactive and thus need to be pulled high via a 2K7Ω resistor. The NTC will not assume control of the bus after receiving a BG active signal unless BGACK, AS and DTACK are all inactive.

3.10.2.4. MOTOROLA Mode Chaining

When NTCs are chained in MOTOROLA mode the BR signal is held active throughout the cycle until the last NTC in the chain is being serviced and then the BR signal will become inactive after detecting BG active. This indicates to the host that multiple bus requests are occurring and although the BGACK signal will be released between each NTC controlling the bus the host will not interrupt the DMA cycle. In this case, the DCOUT signal should be pulled up with a 2K7Ω resistor. This is illustrated in Fig. 38.

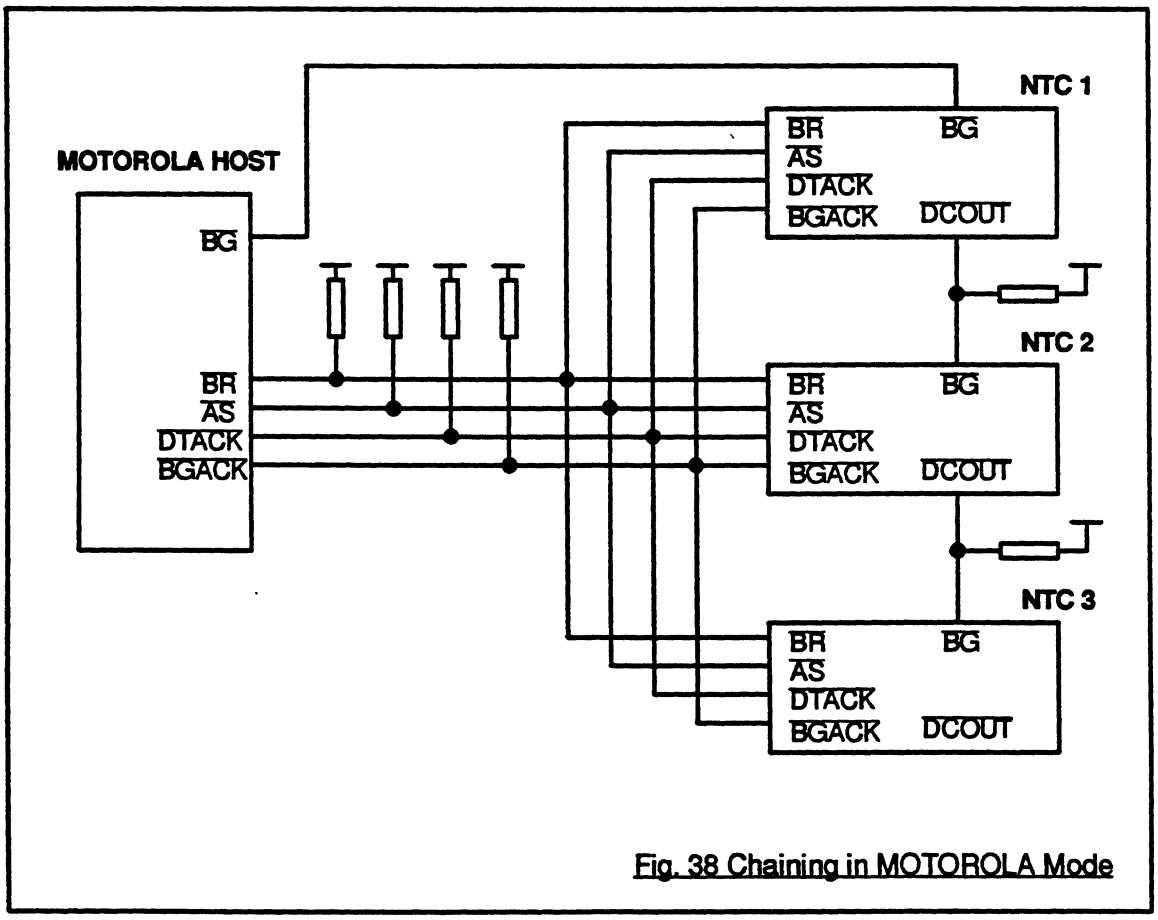


Fig. 38 Chaining in MOTOROLA Mode

3.10.3. DMA Transfer Cycles

When transferring data between the NTC and system memory, the full data bus width is always used, so in 16-bit mode only words are transferred and in 32-bit mode only long words are transferred. Wait states can be inserted by the use of the asynchronous READY/DTACK signal, if enabled. This is done in two stages. Fast transfer of DMA descriptor read/writes is done by setting the FTM bit in the DMA mode register. Fast transfer of the DMA data is done by setting the FTM bit in the Channel Control Register (CCR) within the descriptor location table.

INTEL 16-bit mode transfers are controlled by the RD, WR, BHE and A0 signals. 32-bit mode transfers are controlled by the RD, WR and BE0-3 signals. Wait states can be inserted by using the READY input.

MOTOROLA 16-bit mode transfers are controlled by the AS, R/W, LDS and UDS signals. In 32-bit mode transfers are controlled by the AS, R/W, DS, A0-1 and SIZ0-1 signals. Wait states can be inserted by using the DTACK input.

3.10.3.1. Little Endian / Big Endian

Since the data transferred is individual bytes in both 16-bit and 32-bit modes, the byte configuration is dependant on the system bus being configured as big endian or little endian.
The NTC DMA data conforms to little endian when in INTEL mode and BSWAP pin is inactive.
The NTC DMA data conforms to big endian when in INTEL mode and BSWAP pin is active, or when in MOTOROLA mode.
This is illustrated in Fig. 39 and Fig. 40.

3.10.4. Interrupt Handling

The NTC can generate an interrupt to the processor using the $\overline{IRQ}$ output pin. There are 10 sources of interrupts from within the NTC, all of which are maskable if not required.

The interrupts are are enabled by setting the appropriate bits in *Interrupt Enable* register (CR58). The procedure for handling the interrupts is as follows :-

- Enable Interrupts by setting bits in CR58.
- Wait for $\overline{IRQ}$ output going active.
- Read the *Interrupt Request* register (SR58).
- Write the value from SR58 back into Interrupt *Under Service Register* (CR59).
  This will clear the interrupt request, and will prevent further interrupts of the same type from being generated.
- Process the interrupt.
- Enable further interrupts by clearing the bits previously set in the *Under Service Register* (CR59).

3 of the interrupts provide further information as to the source of the interrupt. These are the OAM, OVERFLOW, and DMA interrupts. This information may be obtained by reading the interrupt indication registers (SR60, SR61, and SR63 respectively). Reading these registers will clear the indication only.

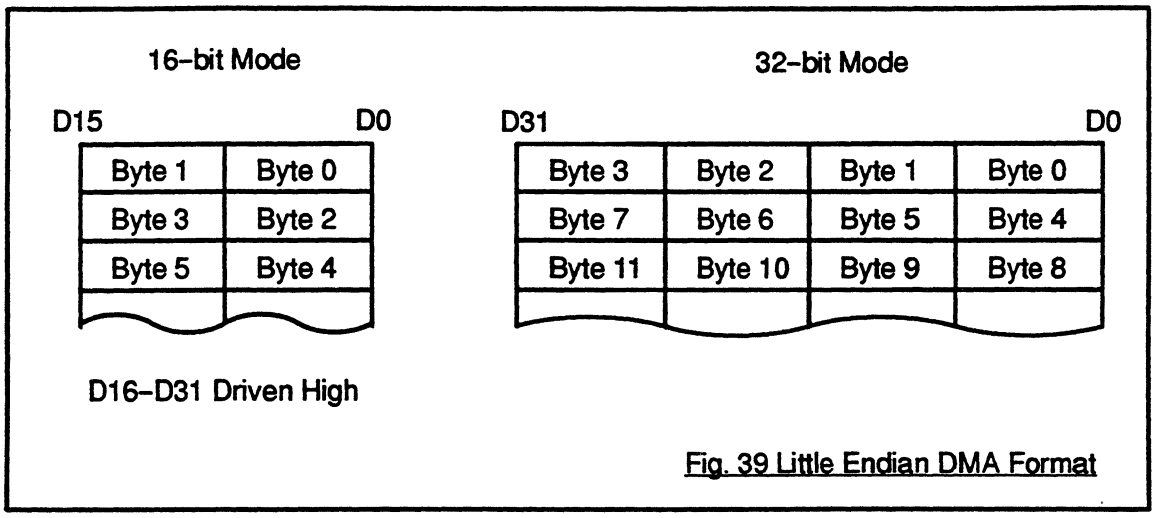


Fig. 39 Little Endian DMA Format

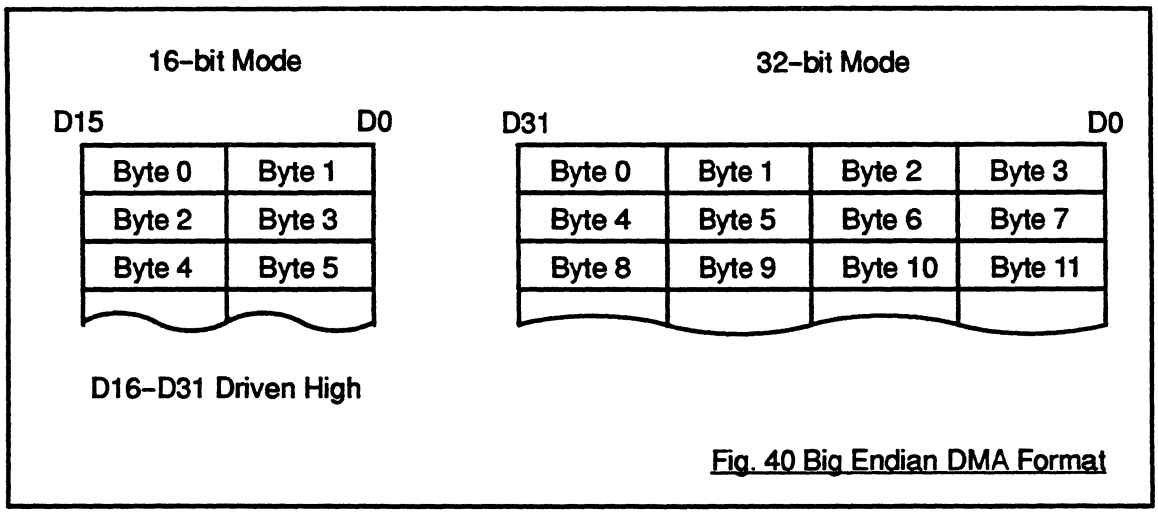


Fig. 40 Big Endian DMA Format

4. GENERAL INFORMATION

4.1. Loopback Modes

The NTC includes 2 loopback modes for in-line testing purposes. These modes are referred to as *transceiver loopback* and *CSI loopback*. The modes are set by setting the appropriate LOOPBACK bits in CR1 and CR56 respectively.
The dataflow is controlled as shown in Fig. 41 for transceiver loopback and Fig. 42 for CSI loopback.

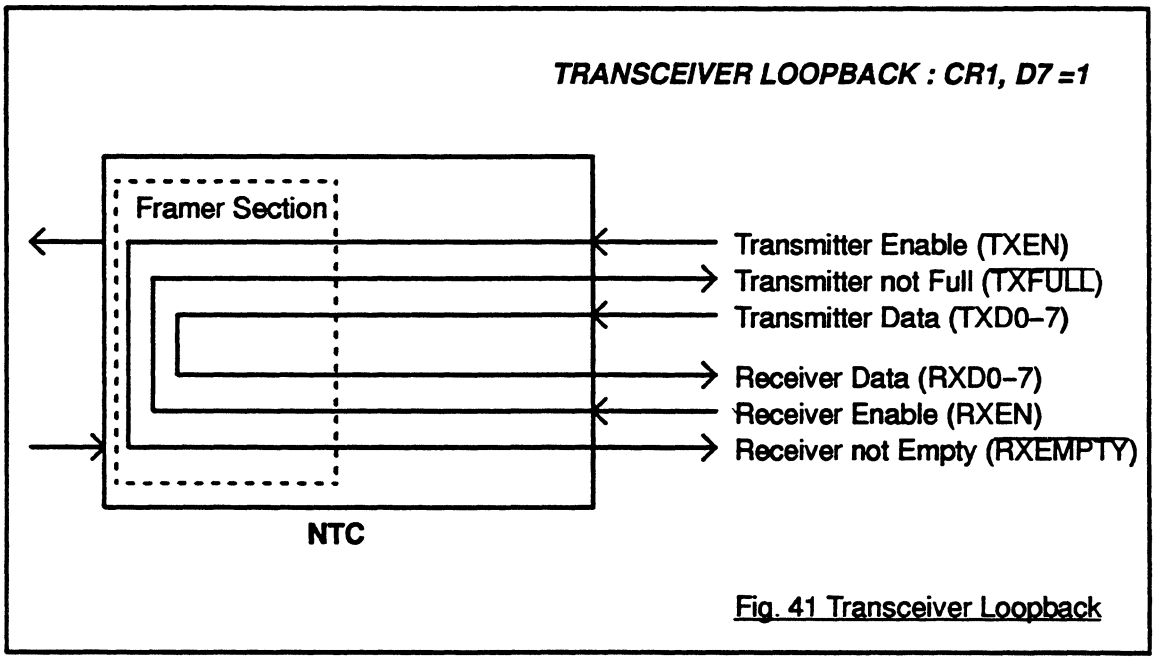


Fig. 41 Transceiver Loopback

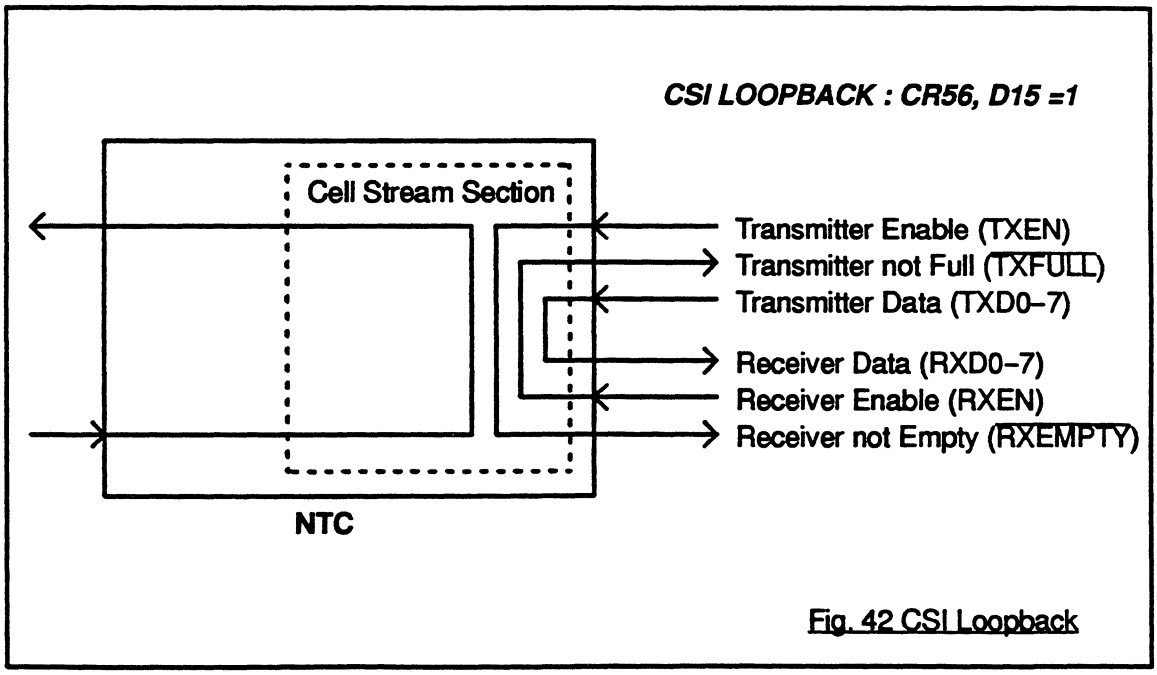


Fig. 42 CSI Loopback

4.2. Fujitsu Chipset Connections

The NTC is intended to connect to the other Fujitsu ATM chipset devices, which include the following :-

- MB86680 - Self-Routing switch Element (SRE)
- MB86689 - Address Translation Controller (ATC)
- MB86686 - Adaptation Layer Controller (ALC)

Recommended connection details to these devices is illustrated in the Fig. 43, Fig. 44, and Fig. 45 for the NTC-SRE, NTC-ALC, and NTC-ATC respectively.

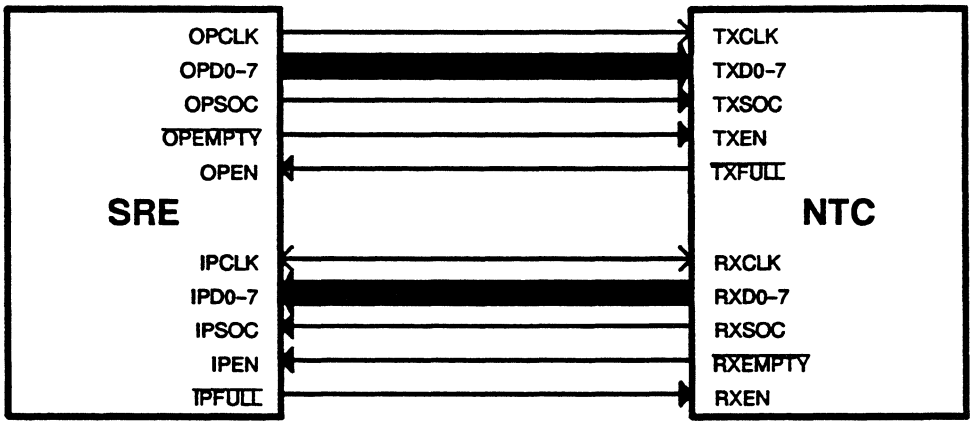


Fig. 43 NTC to SRE Connection

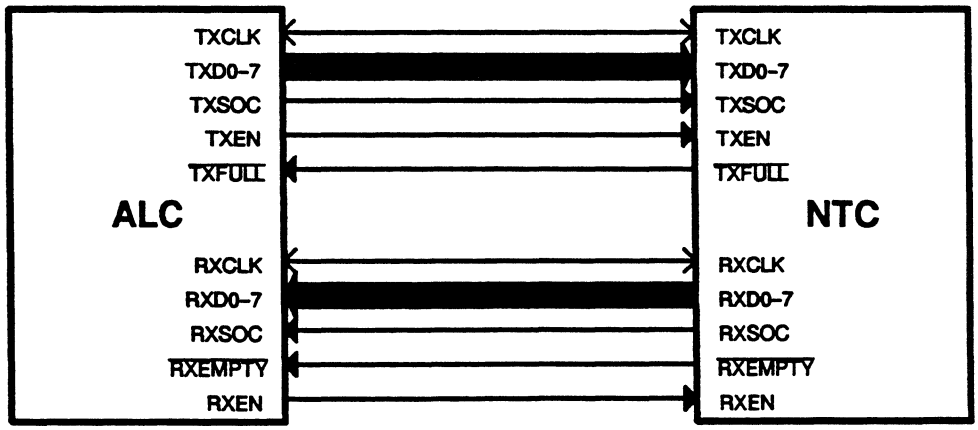
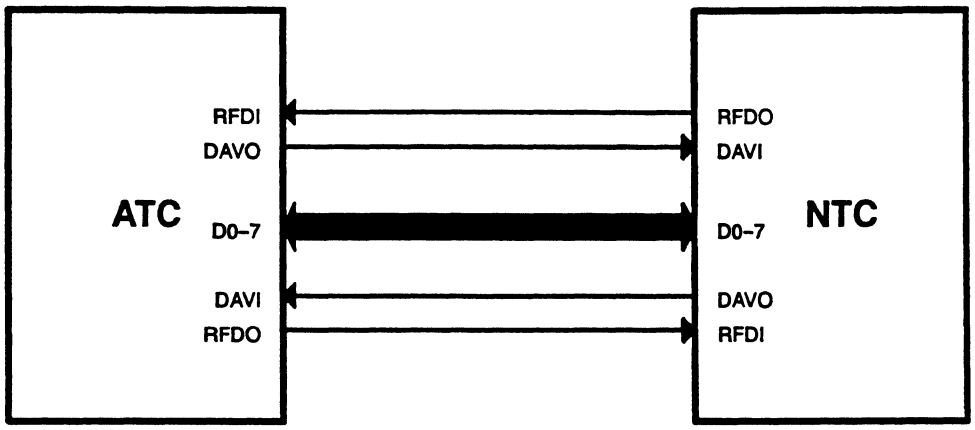


Fig. 44 NTC to ALC Connection



Note :
The NTC has 2 ATC interfaces, one in the transmit path and one in the receive. The pins are prefixed with either AR for the receive, and AT for the transmit path.

External pull-up resistors are required on the ATC databus pins.

Fig. 45 NTC to ATC Connection

4.3. Microprocessor Connections

The NTC is capable of interfacing to a variety of processors, including 16/32 bit INTEL or 16/32 bit MOTOROLA devices.
Some typical configurations are illustrated in Fig. 46 – Fig. 49

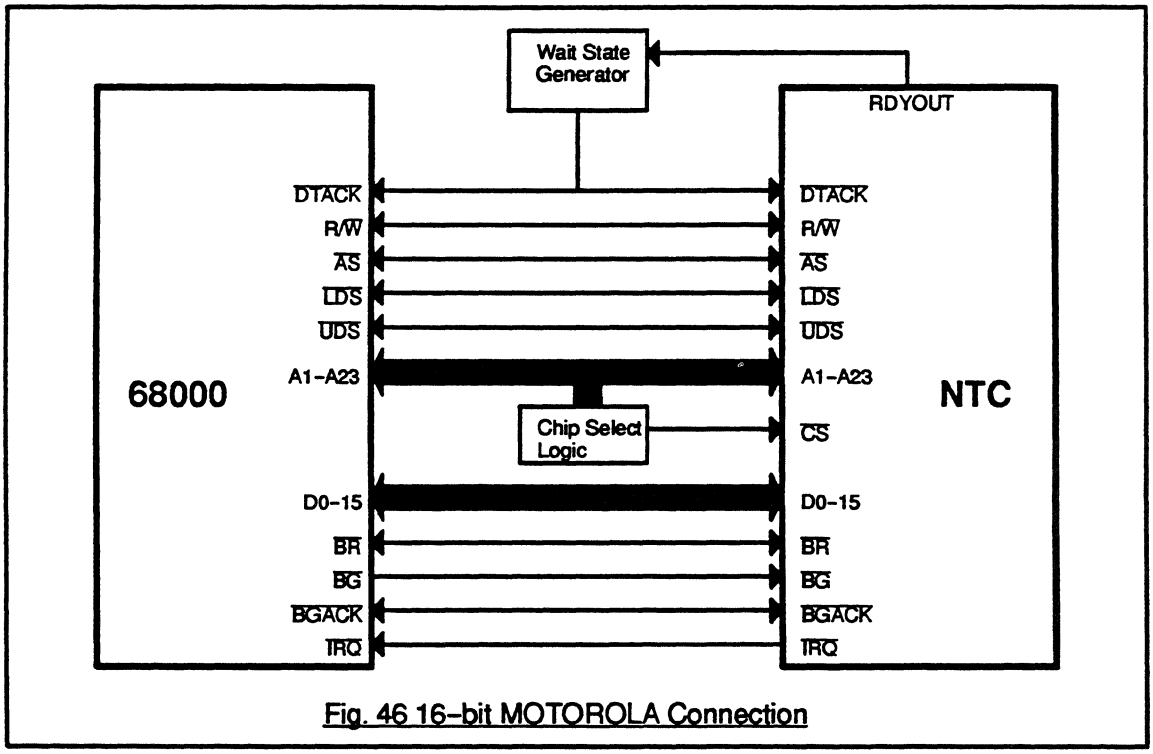


Fig. 46 16-bit MOTOROLA Connection

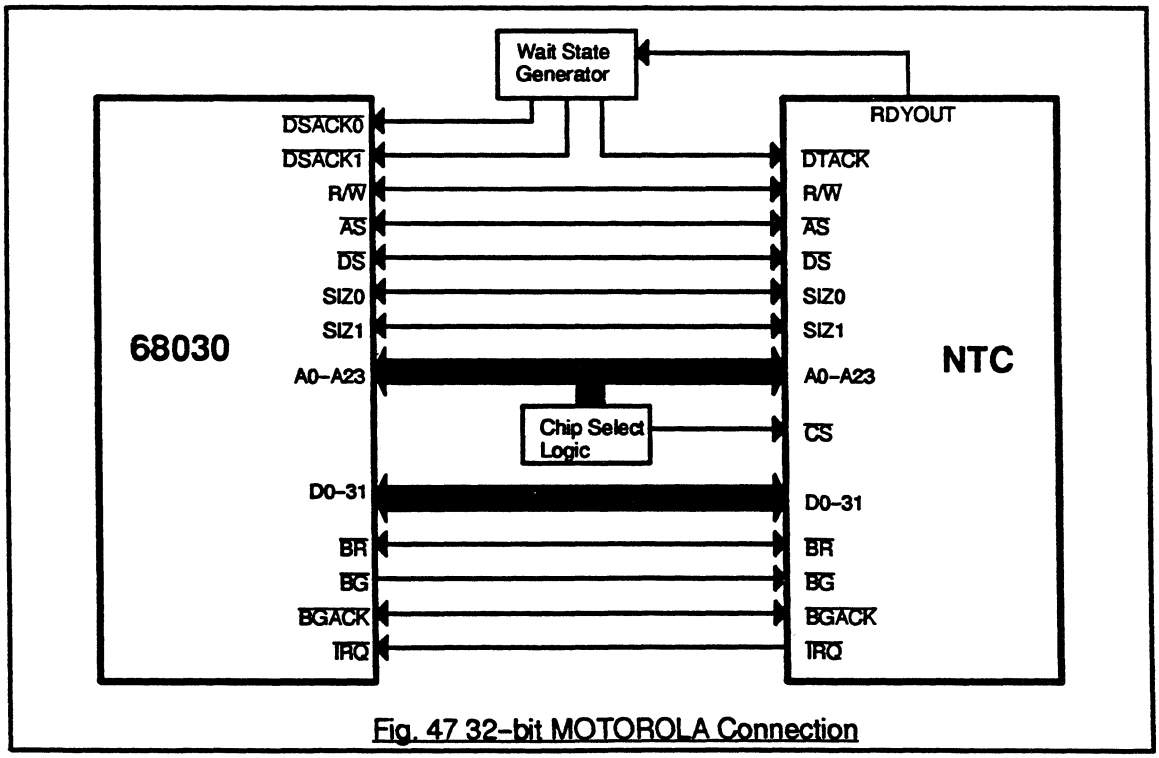


Fig. 47 32-bit MOTOROLA Connection

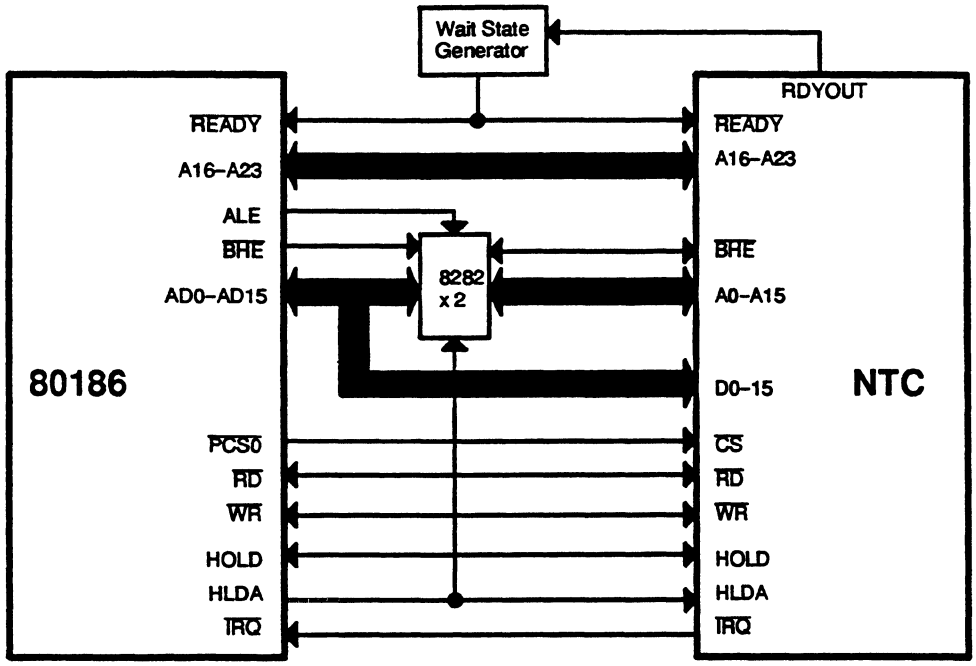


Fig. 48 16-bit INTEL Connection

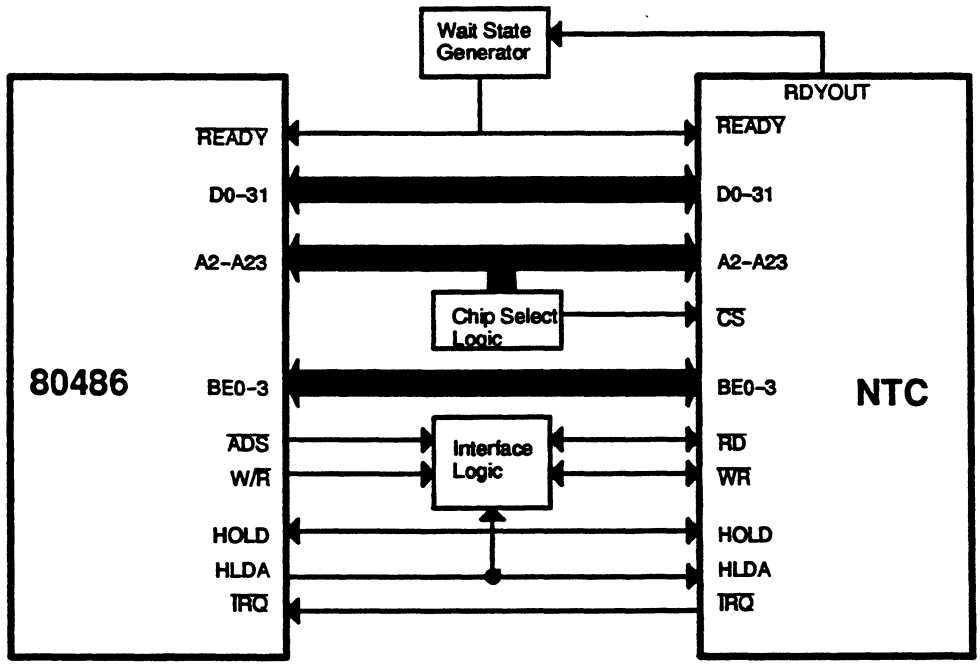


Fig. 49 32-bit INTEL Connection

5. REGISTER TABLE

5.1. Control Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	0	Not Used	
1	2	General Framer Control	Read/Write
2	4	Transmit Framer Overhead Access Bytes Block 1	Write
3	6	Transmit Framer Overhead Access Bytes Block 2	Write
4	8	Transmit Framer Overhead Access Bytes Block 3	Write
5	10	Transmit Framer Overhead Access Bytes Block 4	Write
6	12	Transmit Framer Overhead Access Bytes Block 5	Write
7	14	Transmit Framer Overhead Access Bytes Block 6	Write
8	16	Transmit Framer Overhead Access Bytes Block 7	Write
9	18	Transmit Framer Overhead Access Bytes Block 8	Write
10	20	Transmit Framer Overhead Access Bytes Block 9	Write
11	22	Transmit Framer Overhead Access Bytes Block 10	Write
12	24	Transmit Framer Overhead Access Bytes Block 11	Write
13	26	Transmit Framer Overhead Access Bytes Block 12	Write
14	28	Transmit Framer Overhead Access Bytes Block 13	Write
15	30	Transmit Framer Overhead Access Bytes Block 14	Write
16	32	Transmit Framer Overhead Access Bytes Block 15	Write
17	34	Transmit Framer Overhead Access Bytes Block 16	Write
18	36	Cell Receiver General Control	Read/Write
19	38	Cell Receiver HEC / Descrambler Control	Read/Write
20	40	Cell Receiver User Defined Extract/Discard XMASK #1	Read/Write
21	42	Cell Receiver User Defined Extract/Discard XMASK #2	Read/Write
22	44	Cell Receiver User Defined Extract/Discard SMASK #1	Read/Write
23	46	Cell Receiver User Defined Extract/Discard SMASK #2	Read/Write
24	48	Cell Receiver Extract Buffer Control	Read/Write
25	50	Cell Receiver Discard Control	Read/Write
26	52	Cell Transmitter General Control	Read/Write
27	54	Cell Transmitter HEC / Scrambler Control	Read/Write
28	56	Cell Transmitter User Defined Extract/Discard XMASK #1	Read/Write
29	58	Cell Transmitter User Defined Extract/Discard XMASK #2	Read/Write
30	60	Cell Transmitter User Defined Extract/Discard SMASK #1	Read/Write
31	62	Cell Transmitter User Defined Extract/Discard SMASK #2	Read/Write

Status Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	64		
33	66		
34	68		
35	70		
36	72		
37	74		
38	76		
39	78		
40	80		
41	82		
42	84		
43	86		
44	88		
45	90		
46	92		
47	94		
48	96		
49	98		
50	100		
51	102		
52	104		
53	106		
54	108		
55	110		
56	112	CSI Receive Buffer Fill Level	Read
57	114	CSI Transmit Buffer Fill Level	Read
58	116	Interrupt Status	Read
59	118	Physical Layer Alarms Received	Read
60	120	OAM Interrupt Indication	Read
61	122	Internal Buffer Overflow Interrupt Indication	Read
62	124	DMA Channel Activity Status	Read
63	126	DMA Interrupt Indication	Read

6. REGISTER MAP

Control Register 0 – Not Used

Control Register 1 – General Framer Control

D15 D8

P3	P2	P1	P0	N3	N2	N1	N0
LOOPBACK	STMDESC	STMSCR		XMODE2	XMODE1	XMODE0	FRMENB

D7 D0

Description :-

FRMENB : Rx/Tx Framer Enable
0 : Disabled
1 : Enabled

XMODE2–0 : Transceiver mode
000 : Cell based
001 : SDH (STM-1)
010 : SONET (STS-3c)
011 : DS3
100 : E3

STMSCR : $1+x^6+x^7$ frame scrambler
0 : Disabled
1 : Enabled

STMDESC : $1+x^6+x^7$ frame descrambler
0 : Disabled
1 : Enabled

LOOPBACK : TX to RX framer loopback
0 : Disabled
1 : Enabled

N3–N0 : Frame sync found count (1 – 15)

P3–P0 : Frame sync lost count (1 – 15)

Note : N3–0 and P3–0 are used on the following framing bytes :-

SDH & SONET : A1, A2
DS3 : F1, F2, F3, F4
E3 : FA1, FA2

Control Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	64	Cell Transmitter Extract Buffer Control	Read/Write
33	66	Cell Transmitter Discard Control	Read/Write
34	68	OAM Framed Alarm Control	Read/Write
35	70	F1 PL-OAM Control	Read/Write
36	72	F3 PL-OAM Control	Read/Write
37	74	Not Used	
38	76	Not Used	
39	78	Not Used	
40	80	Not Used	
41	82	Not Used	
42	84	Not Used	
43	86	Not Used	
44	88	Not Used	
45	90	Not Used	
46	92	Not Used	
47	94	Not Used	
48	96	Not Used	
49	98	Not Used	
50	100	Not Used	
51	102	Not Used	
52	104	Not Used	
53	106	Not Used	
54	108	Not Used	
55	110	Statistics Control	Read/Write
56	112	Cell Stream Interface Control #1	Read/Write
57	114	Cell Stream Interface Control #2	Read/Write
58	116	Interrupt Enable	Write
59	118	Interrupt Under Service	Write
60	120	DMA Descriptor Pointer Table Low	Write
61	122	DMA Descriptor Pointer Table High	Write
62	124	DMA Channel Activity	Write
63	126	DMA Mode	Write

5.2. Status Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	0		
1	2		
2	4	Receive Framer Overhead Access Bytes Block 1	Read
3	6	Receive Framer Overhead Access Bytes Block 2	Read
4	8	Receive Framer Overhead Access Bytes Block 3	Read
5	10	Receive Framer Overhead Access Bytes Block 4	Read
6	12	Receive Framer Overhead Access Bytes Block 5	Read
7	14	Receive Framer Overhead Access Bytes Block 6	Read
8	16	Receive Framer Overhead Access Bytes Block 7	Read
9	18	Receive Framer Overhead Access Bytes Block 8	Read
10	20	Receive Framer Overhead Access Bytes Block 9	Read
11	22	Receive Framer Overhead Access Bytes Block 10	Read
12	24	Receive Framer Overhead Access Bytes Block 11	Read
13	26	Receive Framer Overhead Access Bytes Block 12	Read
14	28	Receive Framer Overhead Access Bytes Block 13	Read
15	30	Receive Framer Overhead Access Bytes Block 14	Read
16	32	Receive Framer Overhead Access Bytes Block 15	Read
17	34	Receive Framer Overhead Access Bytes Block 16	Read
18	36		
19	38		
20	40		
21	42		
22	44		
23	46		
24	48		
25	50		
26	52		
27	54		
28	56		
29	58		
30	60		
31	62		

Control Register 2 – Transmit Framer Overhead Access Bytes Block 1

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : C1
D7 - D0 : R1

E3 :-
D15 - D8 : TR
D7 - D0 : NR

Control Register 3 – Transmit Framer Overhead Access Bytes Block 2

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : R2
D7 - D0 : E1

E3 :-
D15 - D8 : UC

Control Register 4 – Transmit Framer Overhead Access Bytes Block 3

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : F1
D7 - D0 : R3

Control Register 5 – Transmit Framer Overhead Access Bytes Block 4

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : R4
D7 - D0 : D1

Control Register 6 – Transmit Framer Overhead Access Bytes Block 5

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : D2
D7 - D0 : D3

Control Register 7 – Transmit Framer Overhead Access Bytes Block 6

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : K1
D7 - D0 : D4

Control Register 8 – Transmit Framer Overhead Access Bytes Block 7

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : D5
D7 – D0 : D6

Control Register 9 – Transmit Framer Overhead Access Bytes Block 8

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : D7
D7 – D0 : D8

Control Register 10 – Transmit Framer Overhead Access Bytes Block 9

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : D9
D7 – D0 : D10

Control Register 11 – Transmit Framer Overhead Access Bytes Block 10

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : D11
D7 – D0 : D12

Control Register 12 – Transmit Framer Overhead Access Bytes Block 11

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z1A
D7 – D0 : Z1B

Control Register 13 – Transmit Framer Overhead Access Bytes Block 12

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z1C
D7 – D0 : E2

Control Register 14 – Transmit Framer Overhead Access Bytes Block 13

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : R5
D7 – D0 : R6

Control Register 15 – Transmit Framer Overhead Access Bytes Block 14

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : J1
D7 – D0 : C2

DS3 (PCLP) :-
D15 – D8 : Z6
D7 – D0 : Z5

Control Register 16 – Transmit Framer Overhead Access Bytes Block 15

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : F2
D7 – D0 : Z3

DS3 (PCLP) :-
D15 – D8 : Z4
D7 – D0 : Z3

Control Register 17 – Transmit Framer Overhead Access Bytes Block 16

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z4
D7 – D0 : Z5

DS3 (PCLP) :-
D15 – D8 : Z2
D7 – D0 : Z1

Control Register 18 - Cell Receiver General Control

D15							D8
ALPHA3	ALPHA2	ALPHA1	ALPHA0	DELTA3	DELTA2	DELTA1	DELTA0
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CRXENB
D7							D0

Description :-

CRXENB :	Cell Receiver Enable	0 : Disabled 1 : Enabled
CRC10CHK :	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN :	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell Insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3–0 :	Peak cell insertion rate (from insert buffer)	0–11 : See Note below.
DELTA3–0 :	Cell sync found count (1 - 15)	
ALPHA3–0 :	Cell sync lost count (1 - 15)	

Note :

PKIR3-0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship :

1 inserted cell in $2^{(13-PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps) :

PKIR = 0 :- Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :- Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

Control Register 19 – Cell Receiver HEC/Descrambler Control

D15							D8
			BALIGN	COREN	HECMASK	DESCR1	DESCR0
D7							D0

Description :-

DESCR1,0 :	Descramble Control	00 : disable 01 : $1 + x^{43}$ 10 : $1 + x^{28} + x^{31}$ 11 : reserved
HECMASK :	HEC Receive Mask	0 : Mask disabled 1 : Mask enabled (01010101)
COREN :	Error Correction enable	0 : Disabled 1 : Enabled
BALIGN :	Byte Alignment	0 : Byte aligned data 1 : Non-byte aligned data

Control Register 20 – Cell Receciver User Defined Extract/Discard XMASK #1

D15							D8
VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12
D7							D0

Control Register 21 – Cell Receciver User Defined Extract/Discard XMASK #2

D15							D8
VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP
D7							D0

Control Register 22 – Cell Receciver User Defined Extract/Discard SMASK #1

D15							D8
VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12
D7							D0

Control Register 23 – Cell Receciver User Defined Extract/Discard SMASK #2

D15							D8
VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP
D7							D0

Description :–

These registers are used for user defined cell extraction/discard within the cell receiver.

Each bit of the first 4 bytes of the cell header may be defined as X, 0, or 1.

The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the user defined cell extraction/discard will take the state defined in the SMASK.

Control Register 24 – Cell Receiver Extract Buffer Control

D15							D8
				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
F1F3	F4F5PM	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0
D7							D0

Description :-

USERDEF1,0 :	User Defined Cell	00 : Extract disabled 01 : Extract all cells defined by mask 11 : Extract all cells not defined by mask 10 : Invalid
METASIG :	Meta Signalling	0 : Extract disabled 1 : Extract enabled
BROADSIG :	Broadcast Signalling	0 : Extract disabled 1 : Extract enabled
PPSIG :	Point-Point Signalling	0 : Extract disabled 1 : Extract enabled
ILMISIG :	ILMI Signalling	0 : Extract disabled 1 : Extract enabled
F4F5PM :	F4/F5 Performance Man	0 : Extract disabled 1 : Extract enabled
F1F3 :	F1/F3 PLOAM	0 : Extract disabled 1 : Extract enabled
F4SGFMAD:	F4 Segment (FM and AD)	0 : Extract disabled 1 : Extract enabled
F4EEFMAD:	F4 End-End (FM and AD)	0 : Extract disabled 1 : Extract enabled
F5SGFMAD:	F5 Segment (FM and AD)	0 : Extract disabled 1 : Extract enabled
F5EEFMAD:	F5 End-End (FM and AD)	0 : Extract disabled 1 : Extract enabled

Control Register 25 – Cell Receiver Discard Control

D15 D8

				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	UNASS	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0

D7 D0

Description :-

USERDEF1,0 : User Defined Cell
00 : Discard disabled
01 : Discard all cells defined by mask
11 : Discard all cells not defined by mask
10 : Invalid

METASIG : Meta Signalling
0 : Discard disabled
1 : Discard enabled

BROADSIG : Broadcast Signalling
0 : Discard disabled
1 : Discard enabled

PPSIG : Point-Point Signalling
0 : Discard disabled
1 : Discard enabled

ILMISIG : ILMI Signalling
0 : Discard disabled
1 : Discard enabled

UNASS : Unassigned Cell
0 : Discard disabled
1 : Discard enabled

F4SGFMAD: F4 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F4EEFMAD: F4 End-End (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5SGFMAD: F5 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5EEFMAD: F5 End-End (FM and AD)
0 : Discard disabled
1 : Discard enabled

Control Register 26 – Cell Transmitter General Control

D15							D8
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CTXENB
D7							D0

Description :-

CTXENB :	Cell Transmitter Enable	0 : Disabled 1 : Enabled
CRC10CHK :	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN :	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3–0 :	Peak cell insertion rate (from insert buffer)	0–11 : See Note below.

Note :

PKIR3–0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship :

1 inserted cell in $2^{(13-PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps) :

PKIR = 0 :- Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :- Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

Control Register 27 – Cell Transmitter HEC/Scrambler Control

D15							D8
					HECMASK	SCRAM1	SCRAM0
D7							D0

Description :–

SCRAM1,0 : Scramble Control

00 : disable
01 : $1 + x^{43}$
10 : $1 + x^{28} + x^{31}$
11 : reserved

HECMASK : HEC Transmit Mask

0 : Mask disabled
1 : Mask enabled (01010101)

Control Register 28 – Cell Transmitter User Defined Extract/Discard XMASK #1

D15							D8
VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12
D7							D0

Control Register 29 – Cell Transmitter User Defined Extract/Discard XMASK #2

D15							D8
VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP
D7							D0

Control Register 30 – Cell Transmitter User Defined Extract/Discard SMASK #1

D15							D8
VPI11/GFC3	VPI10/GFC2	VPI9/GFC1	VPI8/GFC0	VPI7	VPI6	VPI5	VPI4
VPI3	VPI2	VPI1	VPI0	VCI15	VCI14	VCI13	VCI12
D7							D0

Control Register 31 – Cell Transmitter User Defined Extract/Discard SMASK #2

D15							D8
VCI11	VCI10	VCI9	VCI8	VCI7	VCI6	VCI5	VCI4
VCI3	VCI2	VCI1	VCI0	PLT2	PLT1	PLT0	CLP
D7							D0

Description :-

These registers are used for user defined cell extraction/discard within the cell transmitter.

Each bit of the first 4 bytes of the cell header may be defined as X, 0, or 1.

The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the user defined cell extraction/discard will take the state defined in the SMASK.

Control Register 32 – Cell Transmitter Extract Buffer Control

D15							D8
				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	F4F5PM	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0
D7							D0

Description :-

USERDEF1,0 : User Defined Cell
00 : Extract disabled
01 : Extract all cells defined by mask
11 : Extract all cells not defined by mask
10 : Invalid

METASIG : Meta Signalling
0 : Extract disabled
1 : Extract enabled

BROADSIG : Broadcast Signalling
0 : Extract disabled
1 : Extract enabled

PPSIG : Point-Point Signalling
0 : Extract disabled
1 : Extract enabled

ILMISIG : ILMI Signalling
0 : Extract disabled
1 : Extract enabled

F4F5PM : F4/F5 Performance Man
0 : Extract disabled
1 : Extract enabled

F4SGFMAD: F4 Segment (FM and AD)
0 : Extract disabled
1 : Extract enabled

F4EEFMAD: F4 End-End (FM and AD)
0 : Extract disabled
1 : Extract enabled

F5SGFMAD: F5 Segment (FM and AD)
0 : Extract disabled
1 : Extract enabled

F5EEFMAD: F5 End-End (FM and AD)
0 : Extract disabled
1 : Extract enabled

Control Register 33 – Cell Transmitter Discard Control

D15							D8
				F5EEFMAD	F5SGFMAD	F4EEFMAD	F4SGFMAD
	UNASS	ILMISIG	PPSIG	BROADSIG	METASIG	USERDEF1	USERDEF0
D7							D0

Description :-

USERDEF1,0 : User Defined Cell
00 : Discard disabled
01 : Discard all cells defined by mask
11 : Discard all cells not defined by mask
10 : Invalid

METASIG : Meta Signalling
0 : Discard disabled
1 : Discard enabled

BROADSIG : Broadcast Signalling
0 : Discard disabled
1 : Discard enabled

PPSIG : Point-Point Signalling
0 : Discard disabled
1 : Discard enabled

ILMISIG : ILMI Signalling
0 : Discard disabled
1 : Discard enabled

UNASS : Unassigned Cell
0 : Discard disabled
1 : Discard enabled

F4SGFMAD: F4 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F4EEFMAD: F4 End-End (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5SGFMAD: F5 Segment (FM and AD)
0 : Discard disabled
1 : Discard enabled

F5EEFMAD: F5 End-End (FM and AD)
0 : Discard disabled
1 : Discard enabled

Control Register 34 – OAM Alarm Control

D15							D8
				MSFERF1	MSFERF0	PFERF1	PFERF0
		MSAIS	PAIS	RAI	MSFEBE	PFEBE	OAMENB
D7							D0

Description :-

OAMENB :	OAM Controller Enable	0 : Disabled 1 : Enabled
PFEBE :	Tx Path FEBE (B3)	0 : Disabled 1 : Enabled
MSFEBE :	Tx Section FEBE (B2)	0 : Disabled 1 : Enabled
RAI :	Tx Sextion RAI	0 : Disabled 1 : Enabled
PAIS :	Tx Path AIS	0 : Disabled 1 : Enabled
MSAIS :	Tx Section AIS	0 : Disabled 1 : Enabled
PFERF1,0 :	Tx Path FERF	00 : disable 01 : auto 10 : always active
MSFERF1,0 :	Tx Section FERF	00 : disable 01 : auto 10 : always active

Note1 : For cell based transceiver mode,

Section AIS and FERF is supported by F1 PLOAM cells
Path AIS and FERF is supported by F3 PLOAM cells

Note2 :

For *auto* modes, PFERF and MSFERF will be set depending on various received conditions, such as LOS, LOP, LOC, PAIS, etc, in accordance with specification I.610.

Control Register 35 – F1 PL-OAM Control

D15							D8
		MBS5	MBS4	MBS3	MBS2	MBS1	MBS0
				NMB2	NMB1	NMB0	ENBL
D7							D0

Description :-

ENBL : F1 PL-OAM enable 0 : Disabled
1 : Enabled

NMB2–0 : Number of Monitored Blocks (less 1)
(1 – 8)

MBS5–0 : Monitored Block Size (less 1)
(15 – 47)

Note : Number of included cell (NIC) value is given by (MBS x NMB)

eg For NIC = 376, then NMB = 8, and MBS = 47

Hence, set NMB2–0 = 7, and MBS5–0 = 46

Control Register 36 – F3 PL-OAM Control

D15							D8
		MBS5	MBS4	MBS3	MBS2	MBS1	MBS0
				NMB2	NMB1	NMB0	ENBL
D7							D0

Description :-

ENBL : F3 PL-OAM enable 0 : Disabled
1 : Enabled

NMB2–0 : Number of Monitored Blocks (less 1)
(1 – 8)

MBS5–0 : Monitored Block Size (less 1)
(15 – 47)

Note : Number of included cell (NIC) value is given by (MBS x NMB)

eg For NIC = 376, then NMB = 8, and MBS = 47

Hence, set NMB2–0 = 7, and MBS5–0 = 46

Control Register 37 – Not Used

Control Register 38 – Not Used

Control Register 39 – Not Used

Control Register 40 – Not Used

Control Register 41 – Not Used

Control Register 42 – Not Used

Control Register 43 – Not Used

Control Register 44 – Not Used

Control Register 45 – Not Used

Control Register 46 – Not Used

Control Register 47 – Not Used

Control Register 48 – Not Used

Control Register 49 – Not Used

Control Register 50 – Not Used

Control Register 51 – Not Used

Control Register 52 – Not Used

Control Register 53 – Not Used

Control Register 54 – Not Used

Control Register 55 – Statistics Control

D15							D8
				TIME3	TIME2	TIME1	TIME0
			TXVP	RXVP	TXSTAT	RXSTAT	STATENB
D7							D0

Description :-

STATENB : Statistics Controller Enable (also switch statistics block) 0 : Disabled 1 : Enabled

RXSTAT : Receive Statistics 0 : Disabled 1 : Enabled

TXSTAT : Transmit Statistics 0 : Disabled 1 : Enabled

RXVP : Receive Statistics Update 0 : Update on VPI and VCI value 1 : Update on VPI value only

TXVP : Transmit Statistics Update 0 : Update on VPI and VCI value 1 : Update on VPI value only

TIME3–0 : Statistics DMA transfer timeout (see note)

Note :

The TIME3–0 bits are used to provide a programmable timeout for the statistics data (NSR) to be sent to memory via DMA, for the situation where no other event has caused this to happen, ie no counter has reached its maximum value, or the table is not yet full.

The timeout event will happen after a predefined time has elapsed since the previous NSR DMA transfer. This time is set by the TIME3–0 bits, and is a function of the main timestamp counter.

The relationship is : Timeout Event = $2^{(26-TIMEOUT)}$ x clock period

Hence, at 20MHz :

TIMEOUT = 0 implies timeout event will be approximately 3.4 secs after previous DMA

TIMEOUT = 15 implies timeout event will be approximately 102 μs after previous DMA

Control Register 56 – Asynchronous Cell Stream Interface Control #1

D15							D8
LOOPBACK	HECMASK						
RXPLT1	RXPLT0	RXCLP1	RXCLP0	RXATE	RXATC	RXHEC	CSENB
D7							D0

Description :-

CSENB :	Cell Stream Enable	0 : Disabled 1 : Enabled
RXHEC :	HEC Generator enable (Receive)	0 : Disabled 1 : Enabled
RXATC :	Receive ATC enable	0 : ATC not present 1 : ATC present
RXATE :	Address translation error (Receive)	0 : discard 1 : forward
RXCLP1,0 :	CLP bit option (Receive)	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
RXPLT1,0 :	PLT congestion bit option (Receive)	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
HECMASK :	ACSI Rx path HEC Mask	0 : Mask disabled 1 : Mask enabled (01010101)
LOOPBACK :	ACSI Rx/Tx Loopback	0 : loopback disabled 1 : loopback enabled

Note :

For RXPLT bits, these will only change congestion bit (2nd PLT bit) if first PLT bit = 0 (ie indicating user cell).

Control Register 57 – Asynchronous Cell Stream Interface Control #2

D15							D8
TXPLT1	TXPLT0	TXCLP1	TXCLP0	TXATE	TXATC	TAG1	TAG0
D7							D0

Description :-

TAG1,0 :	Routing Tag Byte Size	00 : 0 01 : 1 10 : 2 11 : 3
TXATC :	Transmit ATC enable	0 : ATC not present 1 : ATC present
TXATE :	Address translation error (Transmit)	0 : discard 1 : forward
TXCLP1,0 :	CLP bit option (Transmit)	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
TXPLT1,0 :	PLT congestion bit option (Transmit)	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1

Note :

For TXPLT bits, these will only change congestion bit (2nd PLT bit) if first PLT bit = 0 (ie indicating user cell).

Control Register 58 – Interrupt Enable

D15							D8
INTTEST					SOFTX	SOVRX	SOFRX
	BUFFOVF	LOM	LOC	LOP	LOF	LOS	DMA
D7							D0

Description :-

DMA :	DMA Channel 0–5 Interrupt	0 : Interrupt masked 1 : Interrupt enabled
LOS :	Loss Of Signal	0 : Interrupt masked 1 : Interrupt enabled
LOF :	Loss Of Frame	0 : Interrupt masked 1 : Interrupt enabled
LOP :	Loss Of Pointer (STM–1)	0 : Interrupt masked 1 : Interrupt enabled
LOC :	Loss Of Cell Delineation	0 : Interrupt masked 1 : Interrupt enabled
LOM :	Loss Of OAM	0 : Interrupt masked 1 : Interrupt enabled
BUFFOVF :	Internal Buffer Overflow	0 : Interrupt masked 1 : Interrupt enabled
SOFRX :	Start Of Frame (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOVRX :	Start Of VC–4 (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOFTX :	Start Of Frame (transmit)	0 : Interrupt masked 1 : Interrupt enabled
INTTEST :	Internal Test	This bit is used for internal test purposes and must be set to zero.

Control Register 59 – Interrupt Under Service

D15							D8
					SOFTX	SOVRX	SOFRX
	BUFFOVF	LOM	LOC	LOP	LOF	LOS	DMA
D7							D0

Description :-

These bits are set by the processor to indicate that the associated exception condition is being dealt with. This has two effects :

1. It will clear the associated interrupt request, and
2. Will inhibit any further interrupt requests of the associated type from being generated.

The associated bits should be set back to zero in order to enable further interrupts to be generated. The interrupt sources are identical to those shown in the Interrupt Enable Register.

Control Register 60 – DMA Descriptor Pointer Table Low

D15							D8
AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9
AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1
D7							D0

Description :-

Data written into this register form the least significant 16 bits of the DMA descriptor pointer table.

Control Register 61 – DMA Descriptor Pointer Table High

D15							D8
	AD23	AD22	AD21	AD20	AD19	AD18	AD17
D7							D0

Description :-

Data written into this register form the most significant 7 bits of the DMA descriptor pointer table.

Note :

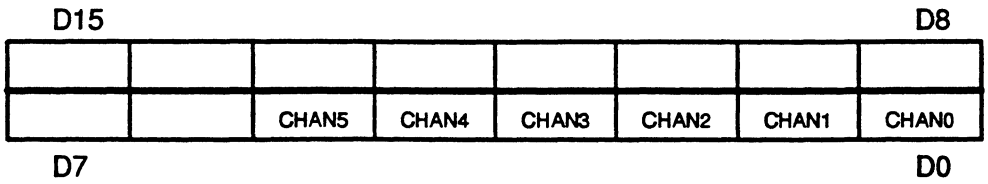
The 23 bit value written into these registers represents the byte address of the Descriptor Pointer Location Table (divided by 2)

eg

If the table resides at 1EF042 (hex), then these registers should be loaded with the following values :-

CR60 = 0821 (hex)
CR61 = 000F (hex)

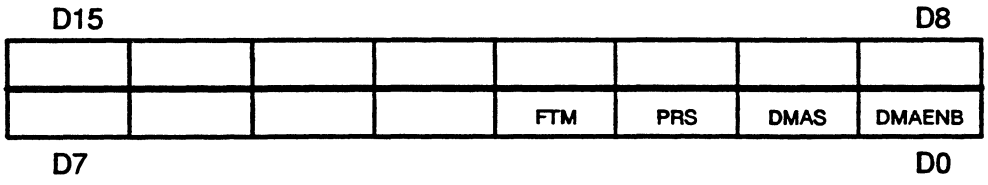
Control Register 62 – DMA Channel Activity



Description :-

CHAN5–0 : DMA Channel Enable
0 : Disabled
1 : Enabled

Control Register 63 – DMA Mode



Description :-

DMAENB : DMA Controller Enable
0 : Disabled
1 : Enabled

DMAS : DMA Stop
0 : DMA not stopped
1 : DMA stopped

PRS : Priority Select
0 : Channel 0 has priority
1 : Channel 5 has priority

FTM : Fast Transfer Mode
0 : Descriptor DMA cycle dependent on READY input
1 : Fast DMA cycle for descriptor transfer

Status Register 0 – Not Used

Status Register 1 – Not Used

Status Register 2 – Receive Framer Overhead Access Bytes Block 1

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : C1
D7 – D0 : R1

E3 :-
D15 – D8 : TR
D7 – D0 : NR

Status Register 3 – Receive Framer Overhead Access Bytes Block 2

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : R2
D7 – D0 : E1

E3 :-
D15 – D8 : UC

Status Register 4 – Receive Framer Overhead Access Bytes Block 3

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : F1
D7 – D0 : R3

Status Register 7 – Receive Framer Overhead Access Bytes Block 4

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : R4
D7 - D0 : D1

Status Register 5 – Receiver Framer Overhead Access Bytes Block 5

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : D2
D7 - D0 : D3

Status Register 6 – Receive Framer Overhead Access Bytes Block 6

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : K1
D7 - D0 : D4

Status Register 8 – Receive Framer Overhead Access Bytes Block 7

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : D5
D7 - D0 : D6

Status Register 9 – Receive Framer Overhead Access Bytes Block 8

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : D7
D7 - D0 : D8

Status Register 10 – Receive Framer Overhead Access Bytes Block 9

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : D9
D7 - D0 : D10

Status Register 11 – Receive Framer Overhead Access Bytes Block 10

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : D11
D7 – D0 : D12

Status Register 12 – Receive Framer Overhead Access Bytes Block 11

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z1A
D7 – D0 : Z1B

Status Register 13 – Receive Framer Overhead Access Bytes Block 12

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z1C
D7 – D0 : E2

Status Register 14 – Receive Framer Overhead Access Bytes Block 13

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : R5
D7 – D0 : R6

Status Register 15 – Receive Framer Overhead Access Bytes Block 14

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : J1
D7 – D0 : C2

DS3 (PCLP) :-
D15 – D8 : Z6
D7 – D0 : Z5

Status Register 16 – Receive Framer Overhead Access Bytes Block 15

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : F2
D7 – D0 : Z3

DS3 (PCLP) :-
D15 – D8 : Z4
D7 – D0 : Z3

Status Register 17 – Receive Framer Overhead Access Bytes Block 16

D15							D8
D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
D7							D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 – D8 : Z4
D7 – D0 : Z5

DS3 (PCLP) :-
D15 – D8 : Z2
D7 – D0 : Z1

Status Register 18 – Not Used
Status Register 19 – Not Used
Status Register 20 – Not Used
Status Register 21 – Not Used
Status Register 22 – Not Used
Status Register 23 – Not Used
Status Register 24 – Not Used
Status Register 25 – Not Used
Status Register 26 – Not Used
Status Register 27 – Not Used
Status Register 28 – Not Used
Status Register 29 – Not Used
Status Register 30 – Not Used
Status Register 31 – Not Used
Status Register 32 – Not Used
Status Register 33 – Not Used
Status Register 34 – Not Used
Status Register 35 – Not Used
Status Register 36 – Not Used
Status Register 37 – Not Used
Status Register 38 – Not Used
Status Register 39 – Not Used
Status Register 40 – Not Used
Status Register 41 – Not Used
Status Register 42 – Not Used
Status Register 43 – Not Used
Status Register 44 – Not Used
Status Register 45 – Not Used
Status Register 46 – Not Used
Status Register 47 – Not Used
Status Register 48 – Not Used
Status Register 49 – Not Used
Status Register 50 – Not Used
Status Register 51 – Not Used
Status Register 52 – Not Used
Status Register 53 – Not Used
Status Register 54 – Not Used
Status Register 55 – Not Used

Status Register 56 – ACSI Receive Buffer Fill Level

D15							D8
X	X	0	RXBUFF4	RXBUFF3	RXBUFF2	RXBUFF1	RXBUFF0
X	X	X	X	X	X	X	X
D7							D0

Description :-

This register shows the fill level of the ACSI Receive cell buffer.
The count will be in cells (0–20)

The X bits will contain the settings of the control bits as set in CR56

Status Register 57 – ACSI Transmit Buffer Fill Level

D15							D8
0	0	0	TXBUFF4	TXBUFF3	TXBUFF2	TXBUFF1	TXBUFF0
X	X	X	X	X	X	X	X
D7							D0

Description :-

This register shows the fill level of the ACSI Transmit cell buffer.
The count will be in cells (0–20)

The X bits will contain the settings of the control bits as set in CR57

Status Register 58 – Interrupt Status Register

D15							D8
0	0	0	0	0	SOFTX	SOVRX	SOFRX
0	BUFFOVF	LOM	LOC	LOP	LOF	LOS	DMA
D7							D0

Description :-

This register shows the source of the interrupt. The bits are identical to CR58.

Status Register 59 – Physical Layer Alarms Received

D15							D8
0	0	0	0	0	0	0	0
B3ERR	B2ERR	B1ERR	RAI	P-FERF	P-AIS	MS-FERF	MS-AIS
D7							D0

Description :-

For SDH/SONET : As above

For DS3 : MS-FERF corresponds to RAI in G1 byte

For E3 : MS-FERF corresponds to FERF in MA byte

For Cell Based : MS-FERF corresponds to F1 FERF
MS-AIS corresponds to F1 AIS
P-FERF corresponds to F3 FERF
P-AIS corresponds to F3 AIS

Note :

B1ERR, B2ERR, and B3ERR are set on receiving a B1/B2/B3 BIP count that disagrees with the calculated BIP.

Status Register 60 – OAM Interrupt Indication

D15							D8
0	0	0	0	0	0	0	0
0	0	F3CRC	F1CRC	F3PSN	F1PSN	F3NRT	F1NRT
D7							D0

Description :-

This register shows why the LOM interrupt was generated.

F1NRT	F1 PL-OAM cell not received on time.
F3NRT	F3 PL-OAM cell not received on time.
F1PSN	F1 PL-OAM cell sequence number error.
F3PSN	F3 PL-OAM cell sequence number error.
F1CRC	F1 PL-OAM cell CRC error
F3CRC	F3 PL-OAM cell CRC error

Status Register 61 – Internal Buffer Overflow Interrupt Indication

D15							D8
0	0	0	0	0	0	0	0
0	0	STATS	RXEXT	TXEXT	SSHBUFF	RXFIFO	TXFIFO
D7							D0

Description :-

This register shows which buffer generated the BUFFOVF interrupt.

TXFIFO :	20 cell CSI transmit buffer
RXFIFO :	20 cell CSI receive buffer
SSHBUFF :	2 x 54-bit word switch statistics buffer
TXEXT :	cell transmitter 4 cell extract buffer
RXEXT :	cell receiver 4 cell extract buffer
STATS :	NSR RAM not available

Status Register 62 – DMA Channel Activity

D15							D8
0	0	0	0	0	0	0	0
0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
D7							D0

Description :-

This register shows which DMA channels are currently active

Status Register 63 – DMA Interrupt Indication

D15							D8
0	0	0	0	0	0	0	0
0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
D7							D0

Description :-

This register shows which DMA channel generated the DMA interrupt

7. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Values		Unit
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	4.5	5.5	V
Input Voltage	V_{DIN}	-0.5	$+V_{DD}$ +0.5	V
Output Voltage	V_{O1}	-0.5	$+V_{DD}$ +0.5	V
Input Current	I_{MAX}	-10.0	10.0	uA
Storage Temperature	T_{STG}	-40	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. DC CHARACTERISTICS

Parameter	Symbol	Pin	Test Condition	Value			Unit
				Min.	Typ.	Max.	
Positive Supply Voltage	V_{DD}		+4.75	+4.75	+5.0	+5.25	V
Positive Supply Current	$+I_{VS}$		Static no load	-	-	100	µA
Input High Voltage (TTL)	V_{IH}			2.2	-	$+V_{DD}$	V
Input Low Voltage (TTL)	V_{IL}			0	-	0.8	V
Input High Voltage (CMOS)	V_{IH}			V_{DD} x 0.7	-	$+V_{DD}$	V
Input Low Voltage (CMOS)	V_{IL}			0	-	V_{DD} x 0.3	V
Input Leakage Current	I_L		$0<=V_I<=+V_{DD}$	-10	-	10	µA
Output Low Voltage	V_{OL}		I_{OL}= 3.2mA	V_{SS}	-	0.4	V
Output High Voltage	V_{OH}		I_{OH}= -2mA	4.2	-	V_{DD}	V
Output Off Leakage Current	I_{LO}			-10	-	10	µA
Input Pin Capacitance	C_{in}			-	-	8	pF
Output Pin Capacitance	C_{out}			-	-	16	pF
I/O Pin Capacitance	$C_{i/o}$			-	-	21	pF
Operating Temperature	T_A			0		+70	°C
Power Dissipation (operating)	P_O				500		mW

9. AC CHARACTERISTICS

Fig. 1 Cell Stream Interface Transmit Port Timing

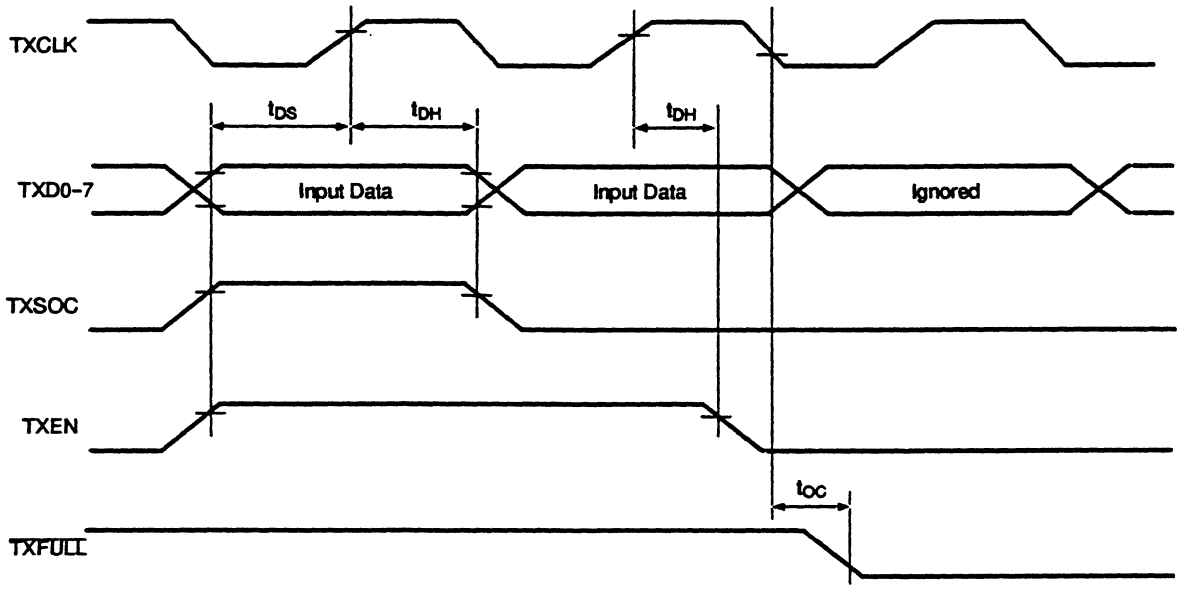


Fig. 2 Cell Stream Interface Receive Port Timing

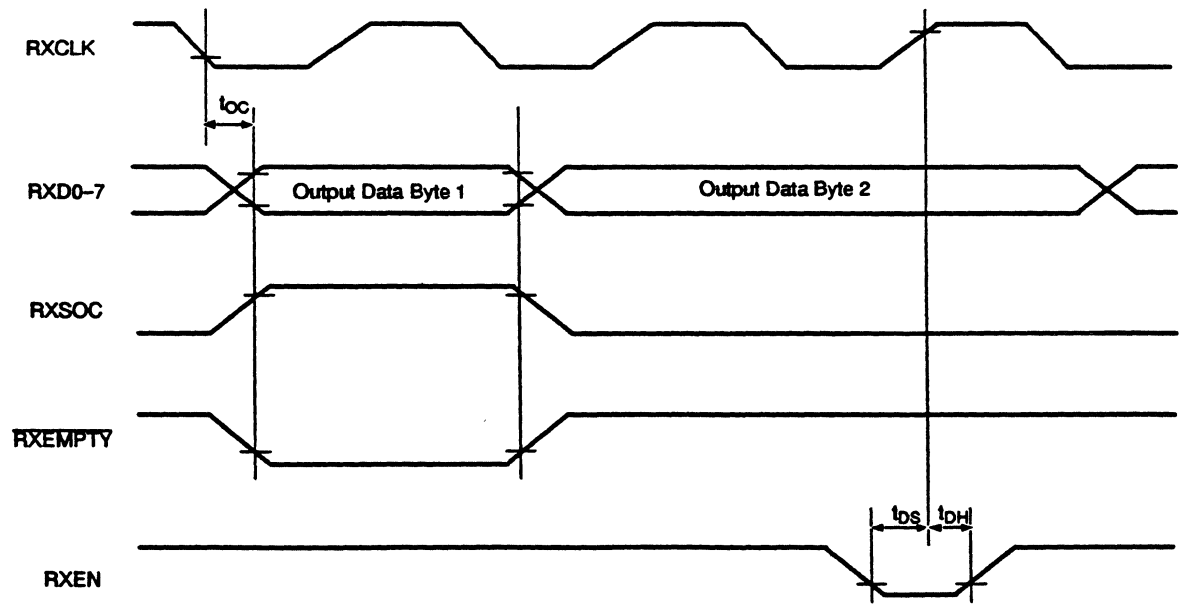


Fig. 3 Transceiver Interface Transmit Port Timing

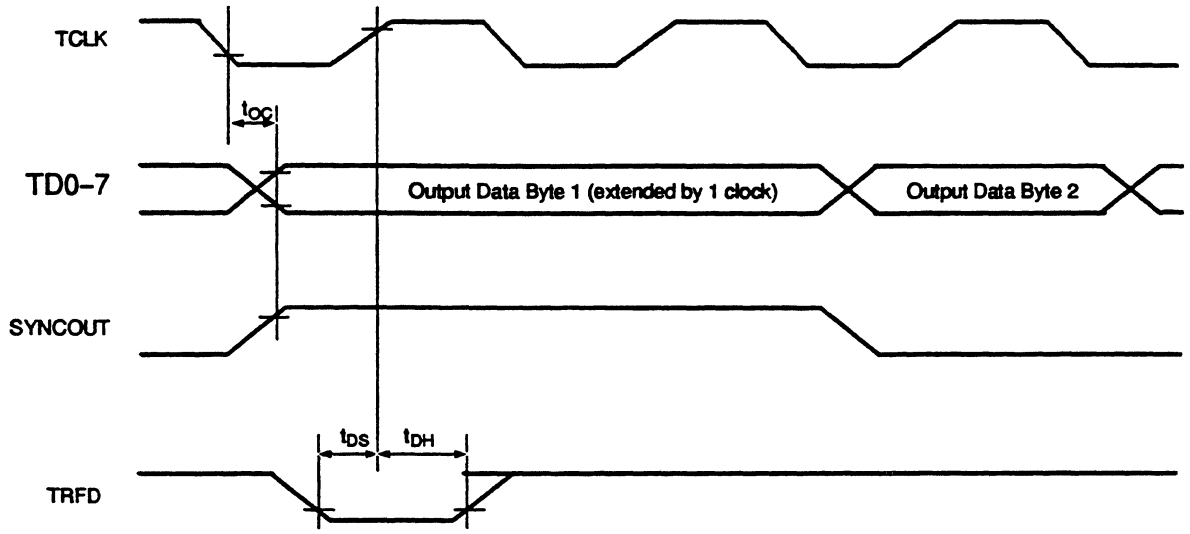


Fig. 4 Transceiver Interface Receive Port Timing

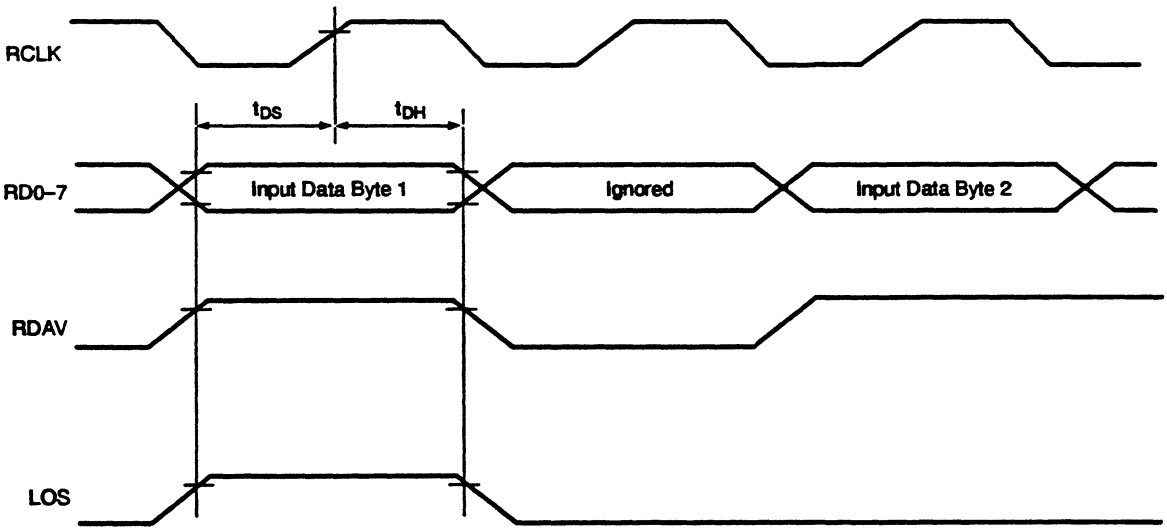


Fig. 5 ATC Interface Port Timing

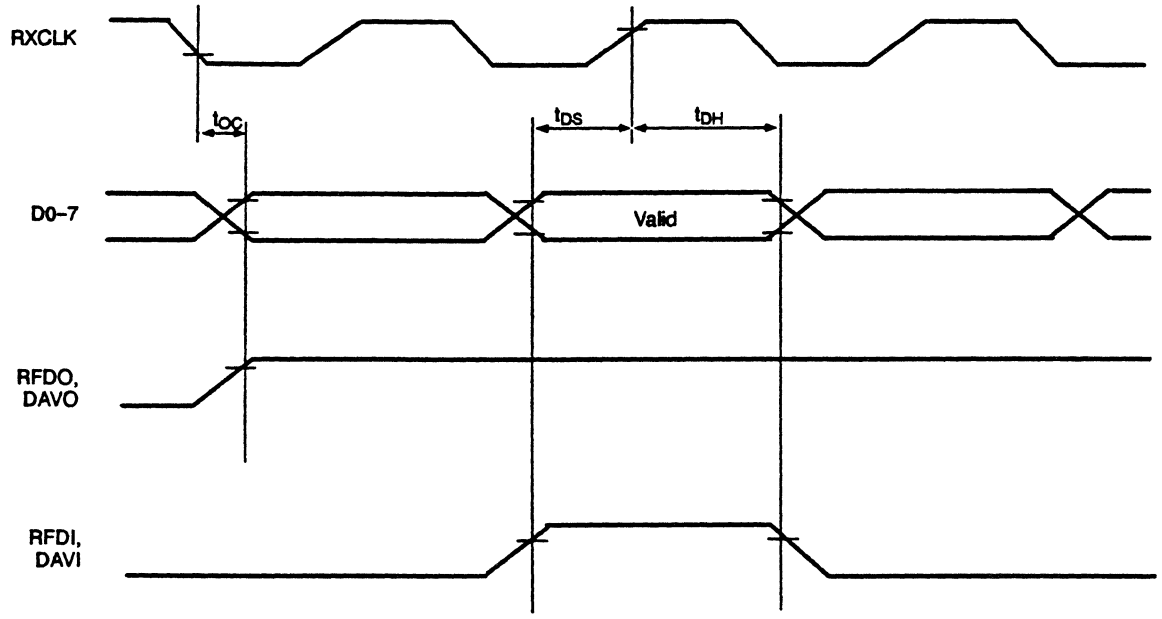


Fig. 6 Switch Statistics Interface Port Timing

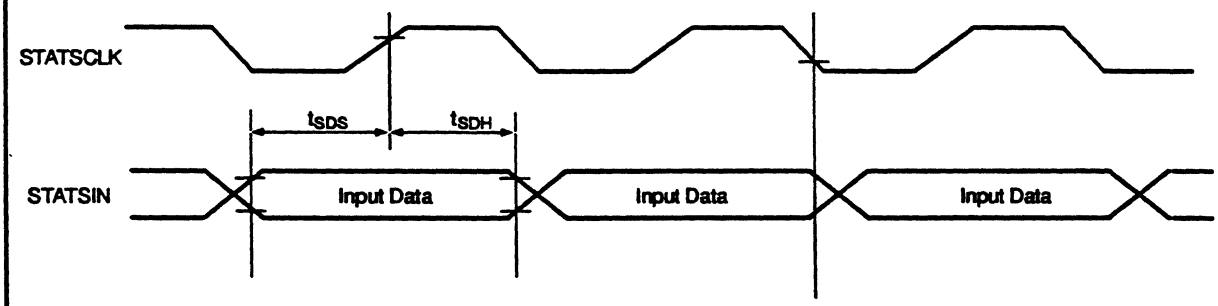


Fig. 7 Interrupt Timing

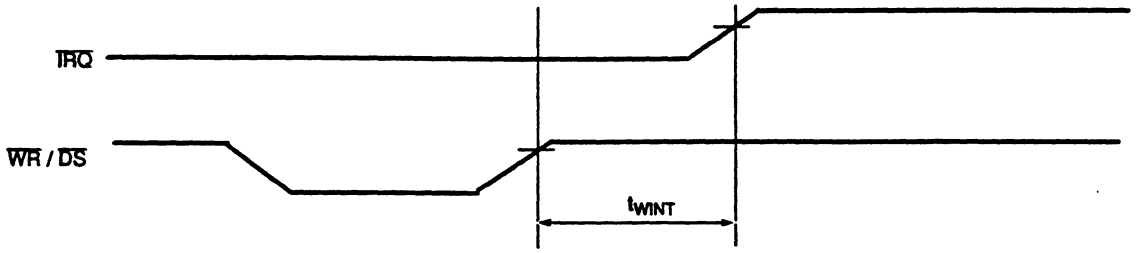


Fig. 8 System Clock Timing

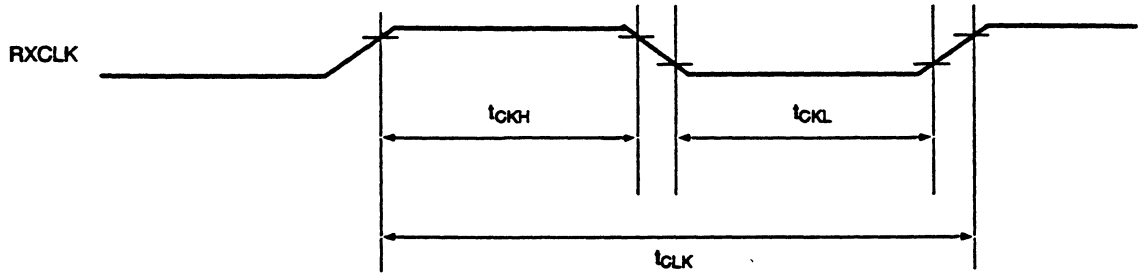


Fig. 9 Cycle to Cycle Timing

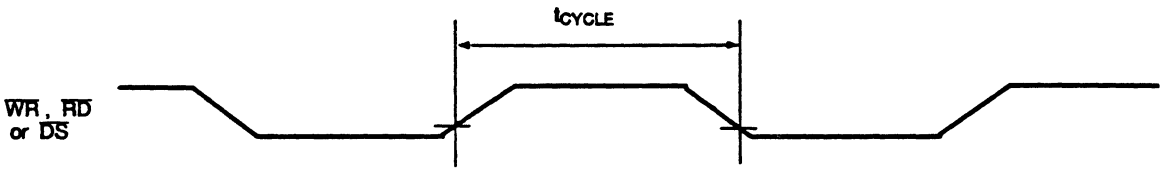
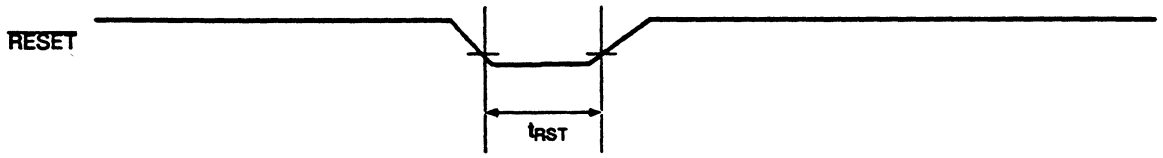


Fig. 10 Reset Timing



EXTERNAL INTERFACES – AC TIMING PARAMETERS

Parameter	Ref Signal	Abrev.	Values			Units
			Min	Typ	Max	
Input Data Setup Time	RCLK,RXCLK TCLK,TXCLK	t_{DS}	5			ns
Input Data Hold Time	RCLK,RXCLK TCLK,TXCLK	t_{DH}	5			ns
Data Out Delay	RCLK,RXCLK TCLK,TXCLK	t_{OC}			15	ns
Statistics Data Setup Time	STATSCLK	t_{SDS}	5			ns
Statistics Data Hold Time	STATSCLK	t_{SDH}	5			ns
Reset Pulse Width	$\overline{RESET}$	t_{RST}	300			ns

MISCELLANEOUS – AC TIMING PARAMETERS

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
Clock High Time	RXCLK	t_{CKH}	20			ns
Clock Low Time	RXCLK	t_{CKL}	20			ns
Clock Period	RXCLK	t_{CLK}	50			ns
Cycle Recovery Time Using Ready_Out	$\overline{WR}$, $\overline{RD}$ & $\overline{DS}$	t_{CYCLE}	30			ns
Cycle Recovery Time Ignoring Ready_Out	$\overline{WR}$, $\overline{RD}$ & $\overline{DS}$	t_{CYCLE}	4 t_{CLK}			ns
$\overline{WR}$ to $\overline{IRQ}$ Inactive	$\overline{WR}$, $\overline{DS}$	t_{WINT}			$20t_{CIK}$+40	ns

Fig. 11 INTEL Read Timing

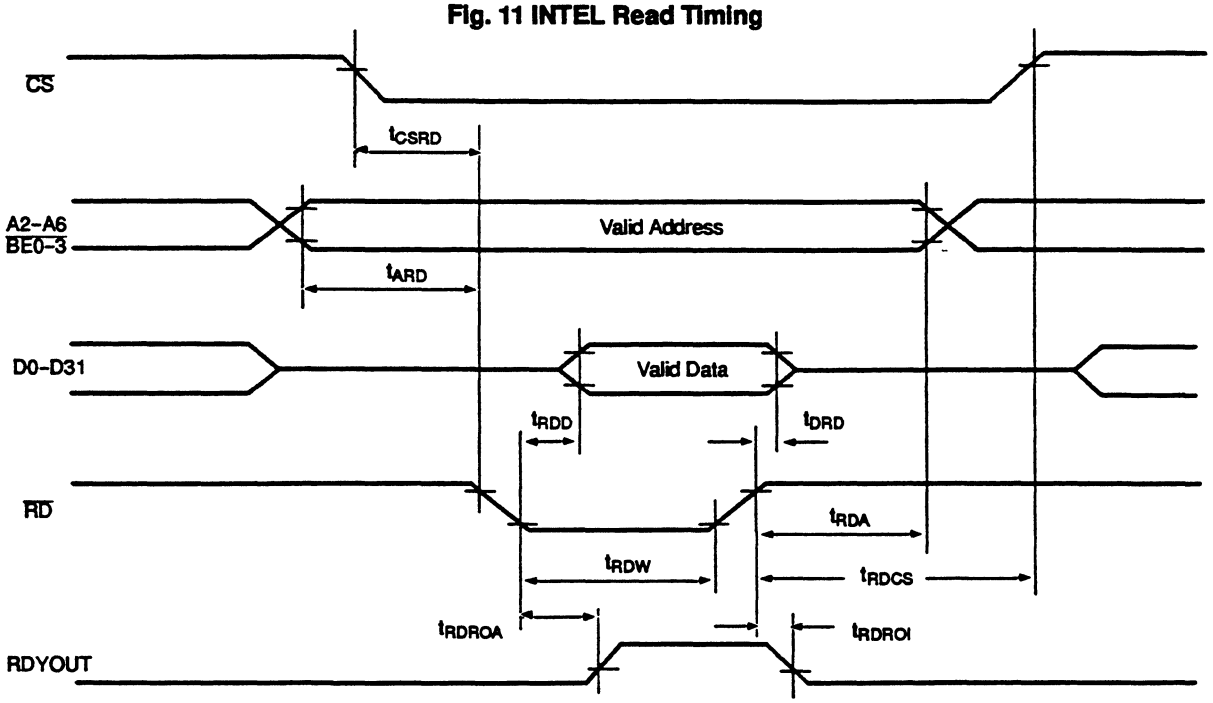
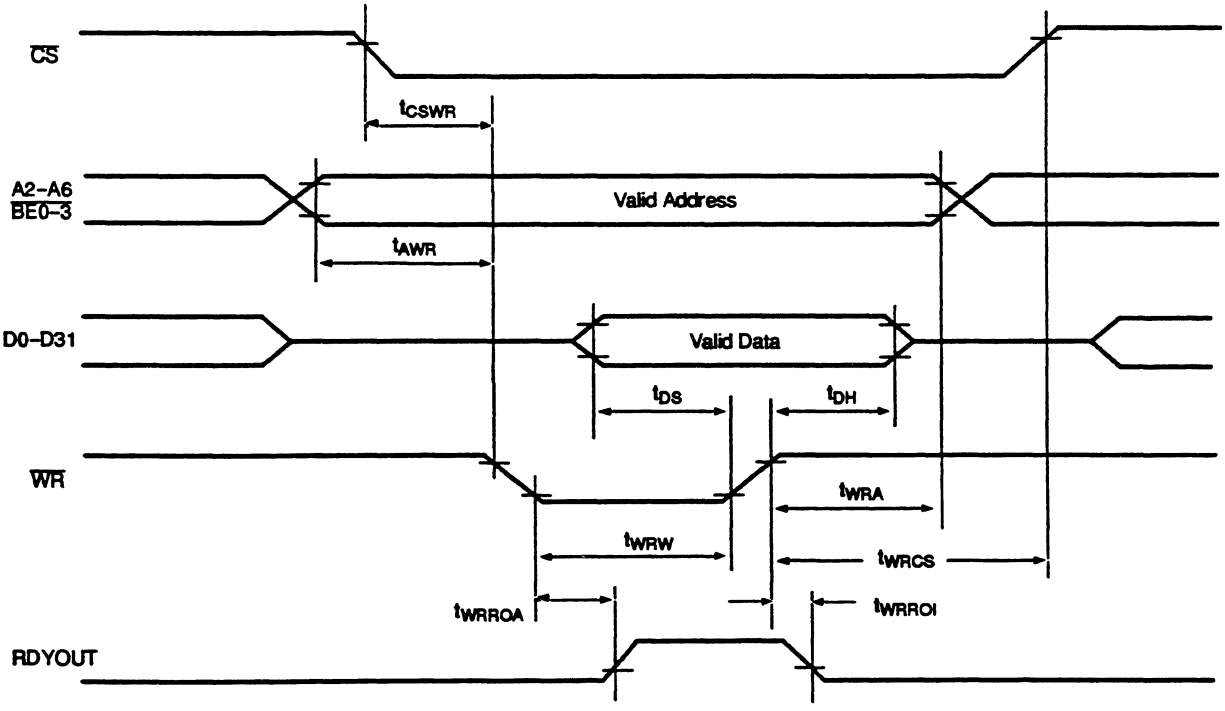


Fig. 12 INTEL Write Timing



MICROPROCESSOR INTERFACE – INTEL AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
$\overline{CS}$ active to $\overline{RD}$ active	$\overline{RD}$	t_{CSRD}	0			ns
Address Valid to $\overline{RD}$ Active	$\overline{RD}$	t_{ARD}	0			ns
$\overline{RD}$ Pulse Width	$\overline{RD}$	t_{RDW}	30			ns
$\overline{RD}$ Active to Valid Data	$\overline{RD}$	t_{RDD}			20	ns
$\overline{RD}$ active to RDYOUT active	$\overline{RD}$	t_{RDROA}			3 t_{CLK}	ns
$\overline{RD}$ Inactive to Invalid Data	$\overline{RD}$	t_{DRD}	5		30	ns
$\overline{RD}$ inactive to RDYOUT inactive	$\overline{RD}$	t_{RDROI}			10	ns
$\overline{RD}$ Inactive to Invalid Address	$\overline{RD}$	t_{RDA}	0			ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive	$\overline{RD}$	t_{RDCS}	0			ns
$\overline{CS}$ active to $\overline{WR}$ active	$\overline{WR}$	t_{CSWR}	0			ns
Address Valid to $\overline{WR}$ Active	$\overline{WR}$	t_{AWR}	0			ns
$\overline{WR}$ Pulse Width	$\overline{WR}$	t_{WRW}	30			ns
$\overline{WR}$ active to RDYOUT active	$\overline{WR}$	t_{WRROA}			3 t_{CLK}	ns
Data Setup Time	$\overline{WR}$	t_{DS}	10			ns
Data Hold Time	$\overline{WR}$	t_{DH}	0			ns
$\overline{WR}$ inactive to RDYOUT inactive	$\overline{WR}$	t_{WRROI}			10	ns
$\overline{WR}$ Inactive to Invalid Address	$\overline{WR}$	t_{WRA}	0			ns
$\overline{WR}$ Inactive to $\overline{CS}$ Inactive	$\overline{WR}$	t_{WRCS}	0			ns

Fig. 13 MOTOROLA Read Timing

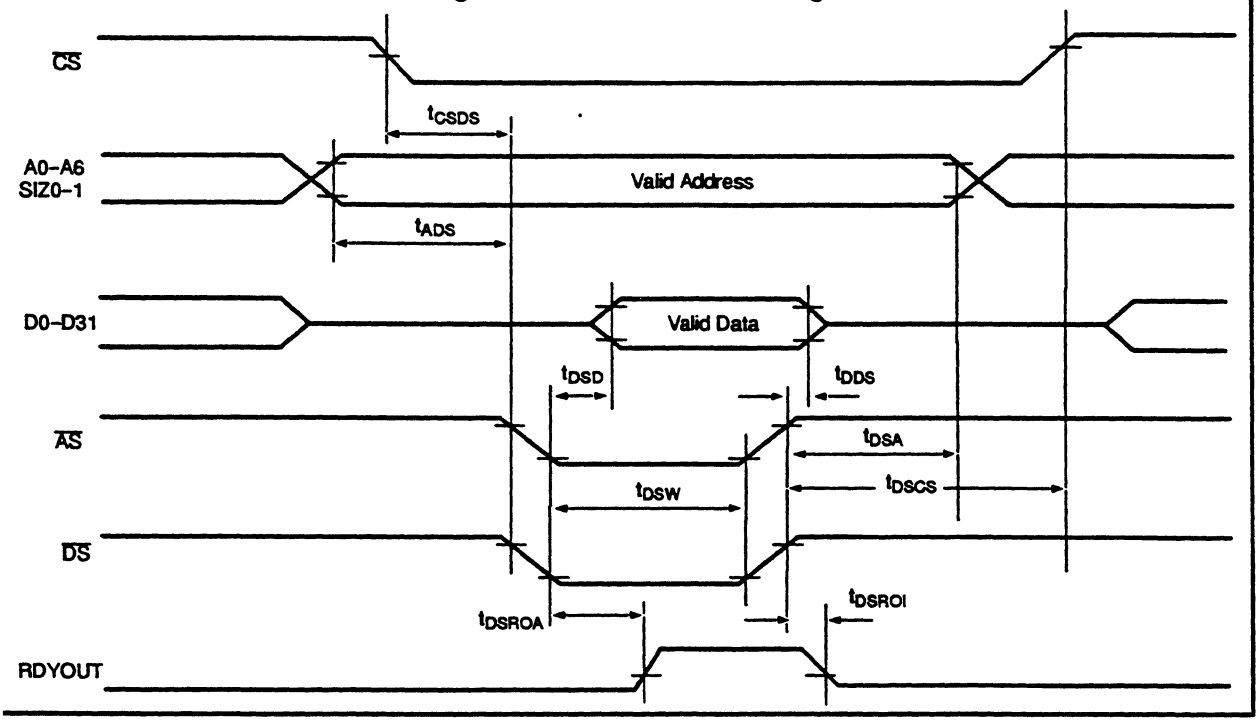
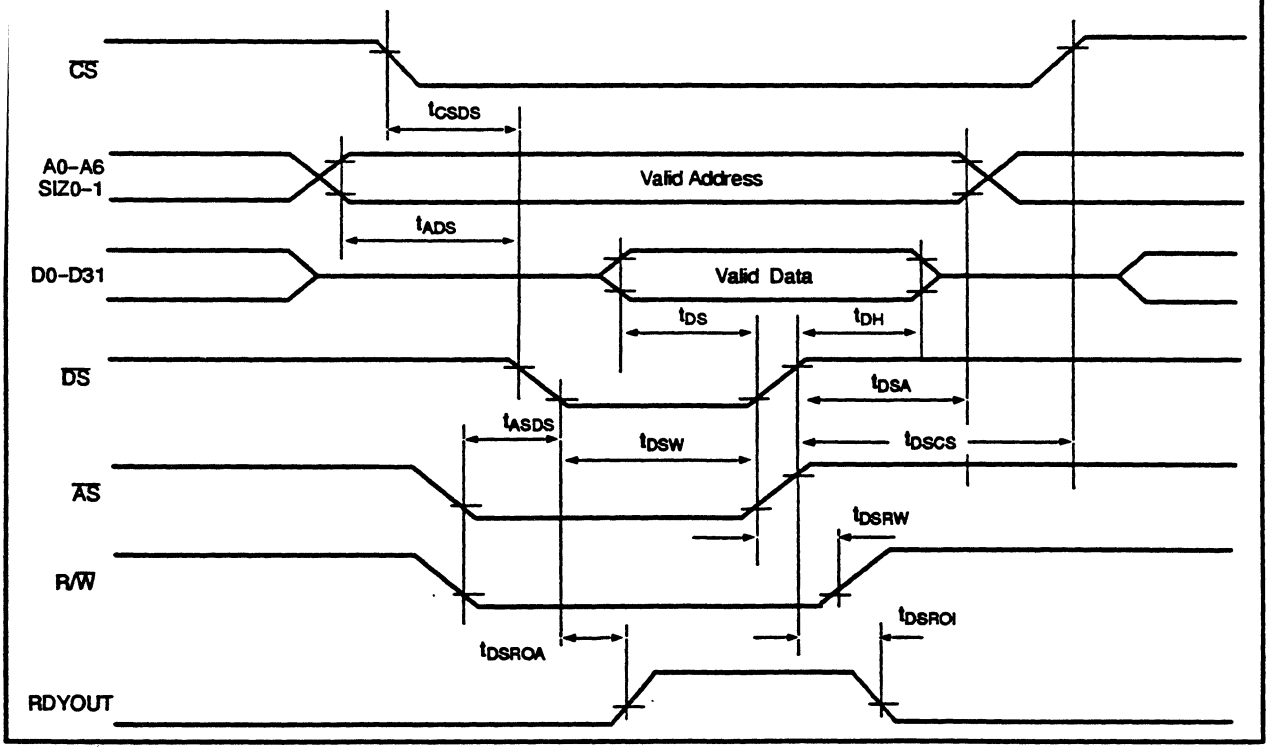


Fig. 14 MOTOROLA Write Timing



MICROPROCESSOR INTERFACE - MOTOROLA AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
$\overline{CS}$ active to $\overline{DS}$ active (Read)	$\overline{DS}$	t_{CSDS}	0			ns
Address Valid to $\overline{DS}$ Active (Read)	$\overline{DS}$	t_{ADS}	0			ns
$\overline{DS}$ Pulse Width (Read)	$\overline{DS}$	t_{DSW}	30			ns
$\overline{DS}$ Active to Valid Data (Read)	$\overline{DS}$	t_{DSD}			20	ns
$\overline{DS}$ active to RDYOUT active (Read)	$\overline{DS}$	t_{DSROA}			3 t_{CLK}	ns
$\overline{DS}$ Inactive to Invalid Data (Read)	$\overline{DS}$	t_{DDS}	5		30	ns
$\overline{DS}$ Inactive to Invalid Address (Read)	$\overline{DS}$	t_{DSA}	0			ns
$\overline{DS}$ inactive to RDYOUT inactive (Read)	$\overline{DS}$	t_{DSROI}			10	ns
$\overline{DS}$ Inactive to $\overline{CS}$ active (Read)	$\overline{DS}$	t_{DSCS}	0			ns
$\overline{CS}$ active to $\overline{DS}$ active (Write)	$\overline{DS}$	t_{CSDS}	0			ns
Address Valid to $\overline{DS}$ Active (Write)	$\overline{DS}$	t_{ADS}	0			ns
$\overline{AS}$ and R/$\overline{W}$ Active to $\overline{DS}$ Active	$\overline{AS}$/ R/$\overline{W}$	t_{ASDS}	0			ns
$\overline{DS}$ Pulse Width (Write)	$\overline{DS}$	t_{DSW}	30			ns
$\overline{DS}$ active to RDYOUT active (Read)	$\overline{DS}$	t_{DSROA}			3 t_{CLK}	ns
Data Setup Time (Write)	$\overline{DS}$	t_{DS}	10			ns
Data Hold Time (Write)	$\overline{DS}$	t_{DH}	0			ns
$\overline{DS}$ Inactive to Invalid Address (Write)	$\overline{DS}$	t_{DSA}	0			ns
$\overline{DS}$ Inactive to $\overline{CS}$ Inactive (Write)	$\overline{DS}$	t_{DSCS}	0			ns
$\overline{DS}$ Inactive to R/$\overline{W}$ Inactive (Write)	$\overline{DS}$ R/$\overline{W}$	t_{DSRW}	5			ns
$\overline{DS}$ inactive to RDYOUT inactive (Read)	$\overline{DS}$	t_{DSROI}			10	ns

Fig. 15 INTEL DMA Access Timing

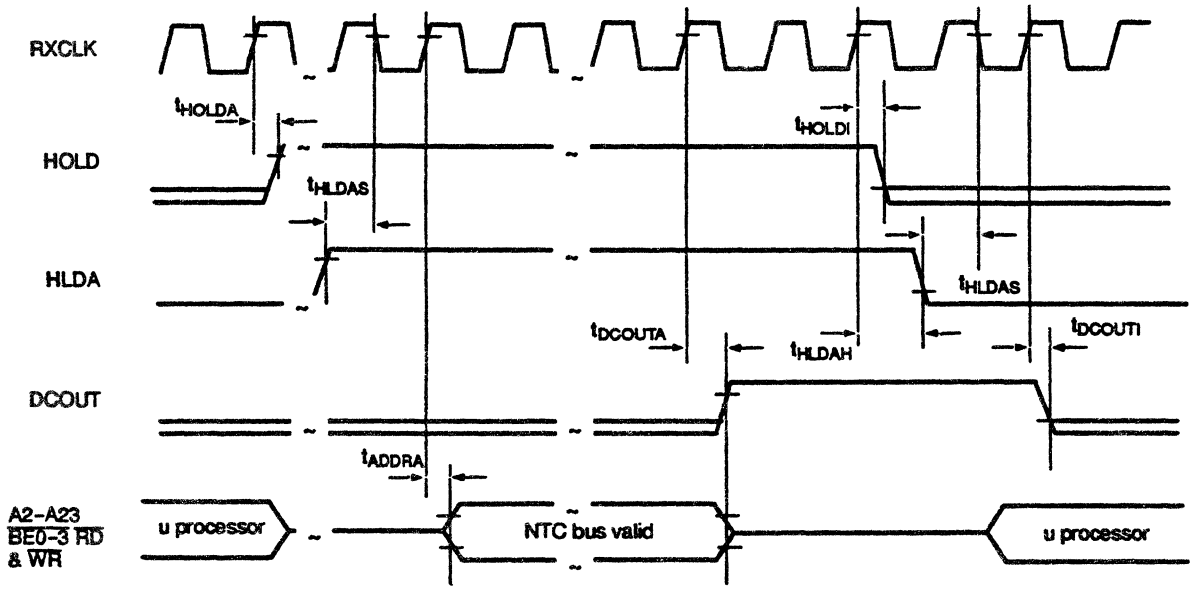
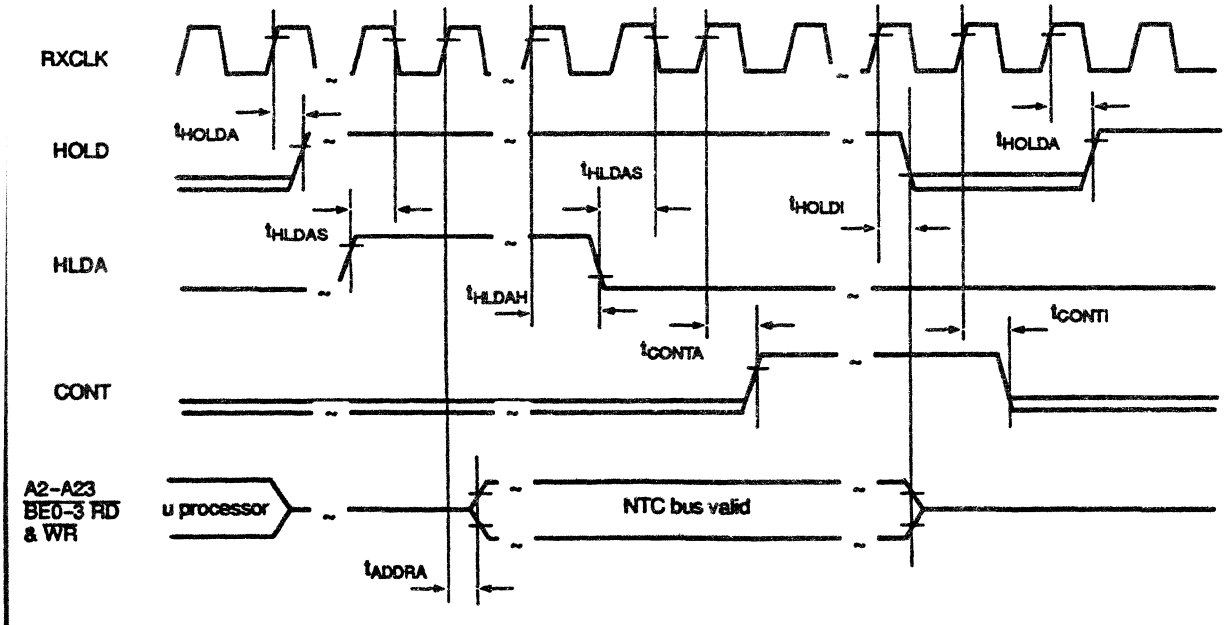


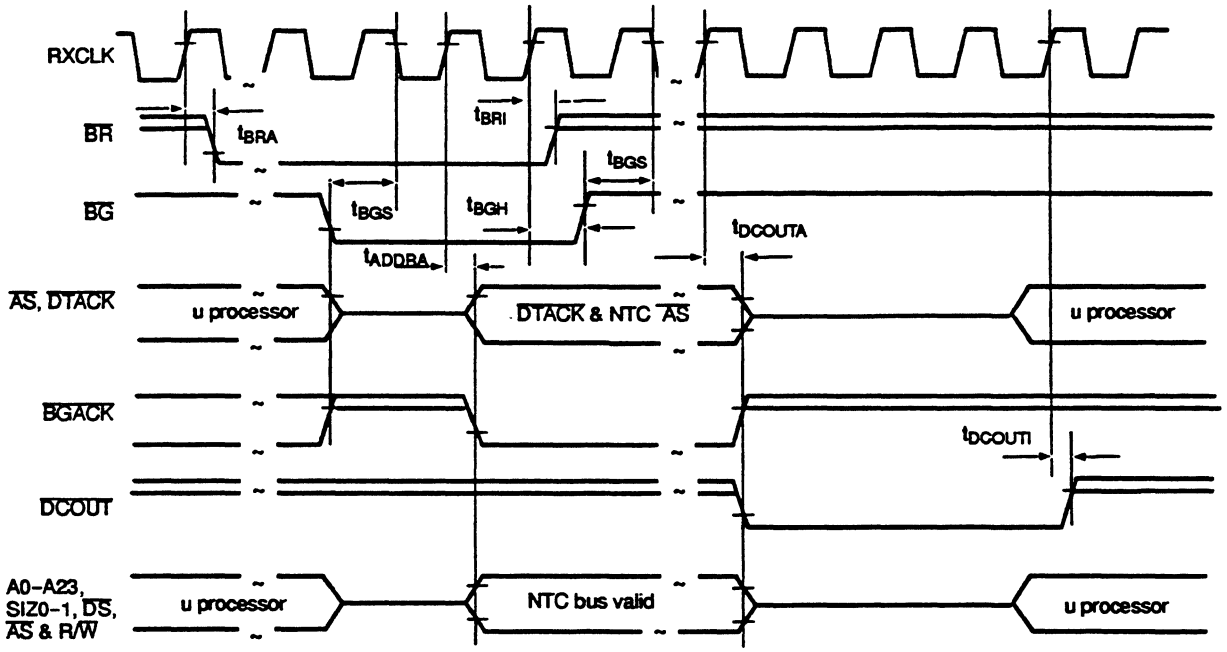
Fig. 16 INTEL DMA Access Control Overide Timing



MICROPROCESSOR INTERFACE – INTEL DMA ACCESS AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
HOLD Active delay	HOLD	t_{HOLDA}			20	ns
HOLD Inactive delay	HOLD	t_{HOLDI}			30	ns
Setup Time of HLDA Active	HLDA	t_{HLDAS}	10			ns
Hold Time of HLDA Invalid	HLDA	t_{HLDAH}	0			ns
DCOUT Active Delay	DCOUT	t_{DCOUTA}			20	ns
DCOUT Inactive Delay	DCOUT	t_{DCOUTI}			30	ns
ADDRESS Active Delay	A0–A7	t_{ADDRA}			20	ns
CONT Active Delay	CONT	t_{CONTA}			20	ns
CONT Inactive Delay	CONT	t_{CONTI}			30	ns

Fig. 17 MOTOROLA DMA Access Timing



MICROPROCESSOR INTERFACE – MOTOROLA DMA ACCESS AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
BR Active Delay	BR	t_{BRA}			20	ns
BR Inactive Delay	BR	t_{BRI}			30	ns
Setup Time of BG, AS & BGACK Active	BG	t_{BGS}	10			ns
Hold Time of BG, AS & BGACK Invalid	BG	t_{BGH}	0			ns
DCOUT Active Delay	DCOUT	t_{DCOUTA}			20	ns
DCOUT Active Delay	DCOUT	t_{DCOUTI}			30	ns
ADDRESS Bus Active Delay	A1-A7	t_{ADDRA}			20	ns

Fig. 18 INTEL DMA Read Cycle Timing

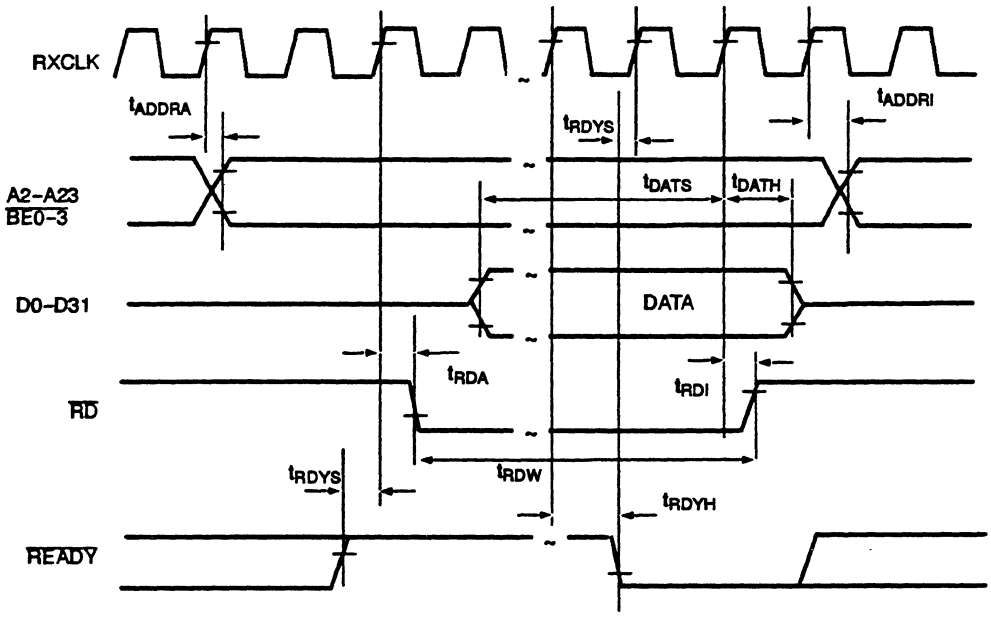
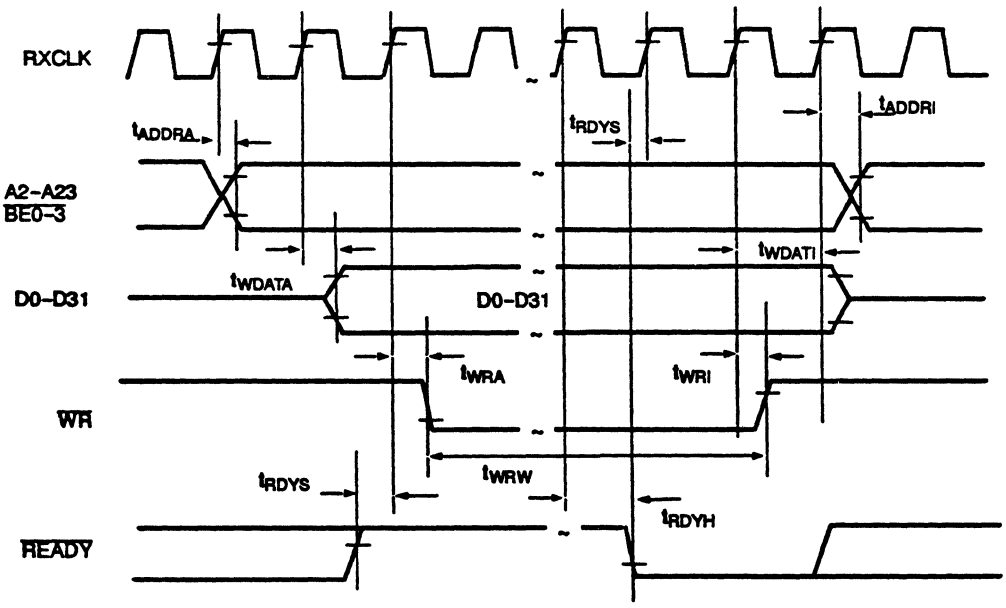


Fig. 19 INTEL DMA Write Cycle Timing



MICROPROCESSOR INTERFACE – INTEL DMA BUS CYCLE AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
Address Active Delay	A2–A23	t_{ADDRA}			10	ns
Address Inactive Delay	A2–A23	t_{ADDRI}			10	ns
Read Active Delay	$\overline{RD}$	t_{RDA}			10	ns
Read Inactive Delay	$\overline{RD}$	t_{RDI}			10	ns
Setup Time of Ready	$\overline{READY}$	t_{RDYS}	10			ns
Hold Time of Ready	$\overline{READY}$	t_{RDYH}	0			ns
Read Active Width	$\overline{RD}$	t_{RDW}	t_{CLK}			ns
Setup Time of Data	D0–D31	t_{DATS}	10			ns
Hold Time of Data	D0–D31	t_{DATH}	0			ns
Write Active Delay	$\overline{WR}$	t_{WRA}			10	ns
Write Inactive Delay	$\overline{WR}$	t_{WRI}			10	ns
Write Active Width	$\overline{WR}$	t_{WRW}	t_{CLK}			ns
Write Data Active Delay	D0–D31	t_{WDATA}			10	ns
Write Data Inactive Delay	D0–D31	t_{WDATI}	t_{CLK}			ns

Fig. 20 MOTOROLA DMA Read Cycle Timing

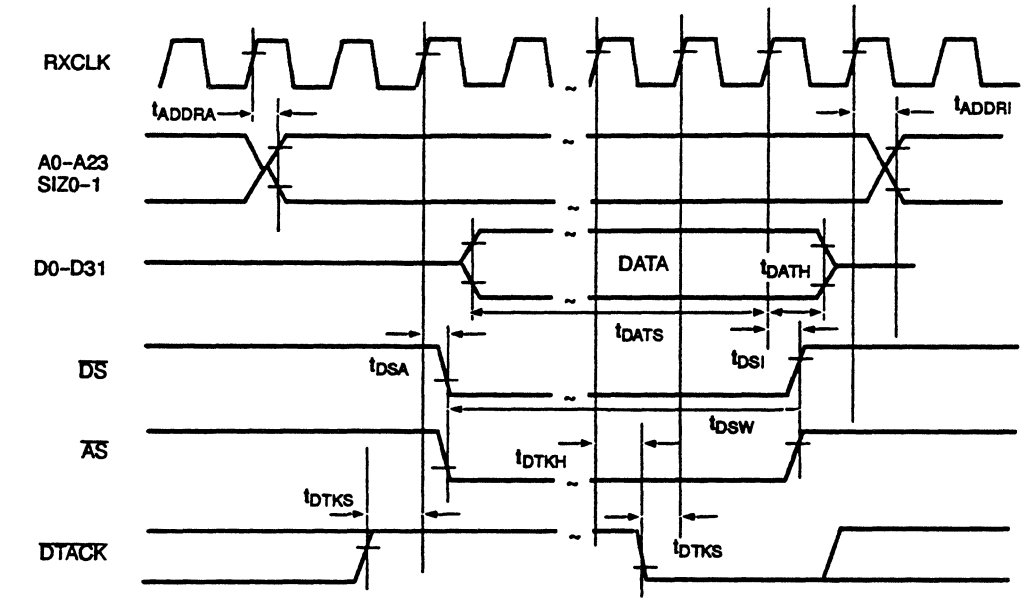
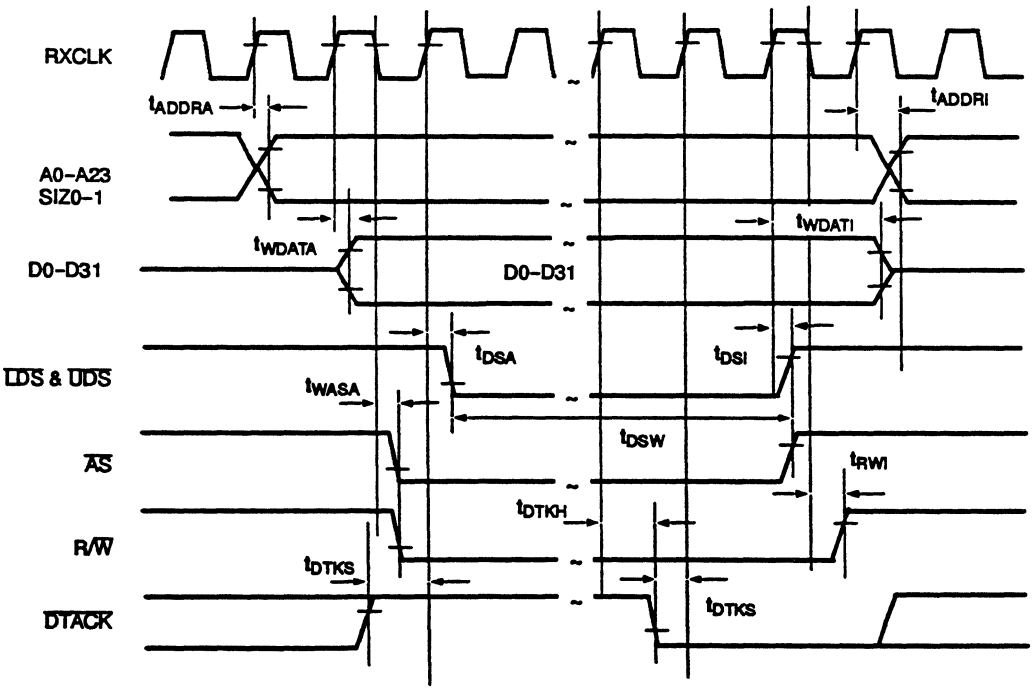


Fig. 21 MOTOROLA DMA Write Cycle Timing



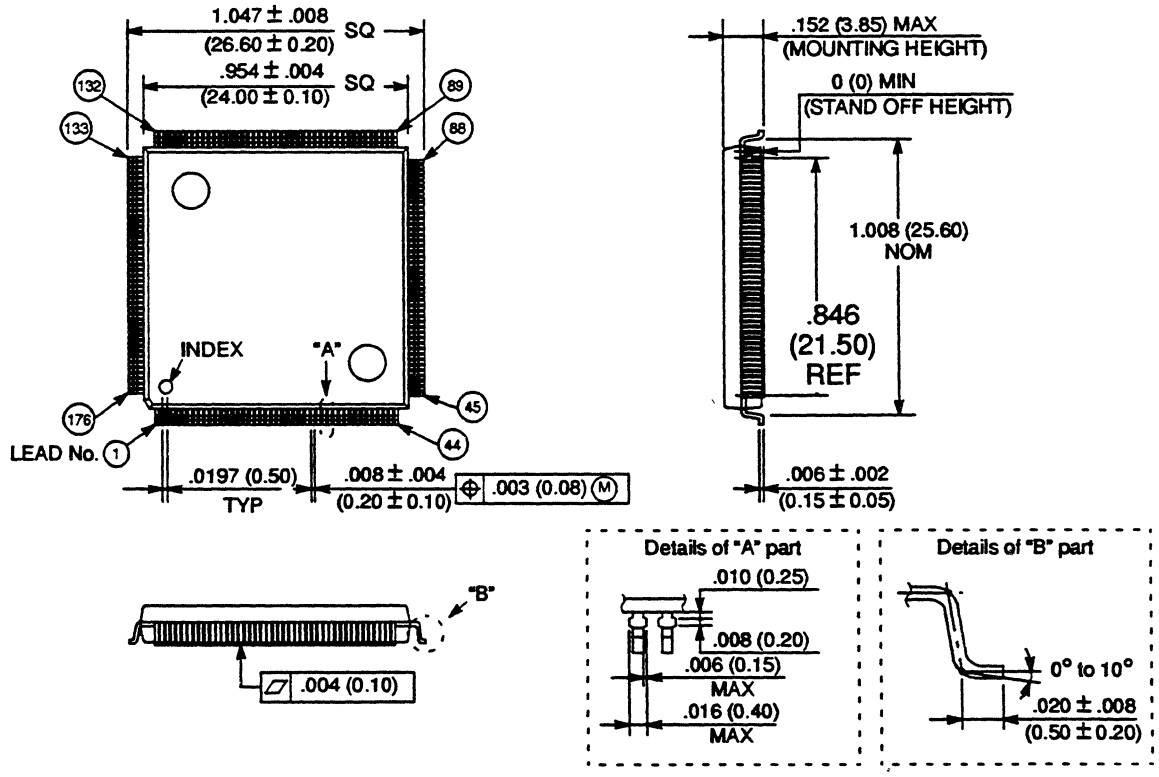
MICROPROCESSOR INTERFACE – MOTOROLA DMA BUS CYCLES AC TIMING

Parameter	Signal	Abbrev.	Values			Units
			Min	Typ	Max	
Address Active Delay	A0–A23	t_{ADSTBA}			10	ns
Address Inactive Delay	A0–A23	t_{ADSTBI}			10	ns
$\overline{DS}$ Active Delay	$\overline{DS}$	t_{DSA}			10	ns
$\overline{DS}$ Inactive Delay	$\overline{DS}$	t_{DSI}			10	ns
Setup Time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKS}	10			ns
Hold Time of $\overline{DTACK}$	$\overline{DTACK}$	t_{DTKH}	0			ns
Data Setup Time	D0–D31	t_{DATS}	10			ns
Data Hold Time	D0–D31	t_{DATH}	0			ns
$\overline{DS}$ Active Width (Read)	$\overline{DS}$	t_{DSW}	t_{CLK}			ns
Write Data Active Delay	D0–D31	t_{WDATA}			10	ns
Write Data Inactive Delay	D0–D31	t_{WDATI}	t_{CLK}			ns
$\overline{AS}$ Active Delay	$\overline{AS}$	t_{WASA}			10	ns
R/$\overline{W}$ Inactive Delay	R/$\overline{W}$	t_{RWI}			10	ns
$\overline{DS}$ Active Width (Write)	$\overline{DS}$	t_{DSW}	t_{CLK}			ns

10. PACKAGE DIMENSIONS

FPT-176P-M01

176-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-176P-M01)



F176001S-3C

Dimensions in
inches (millimeters)