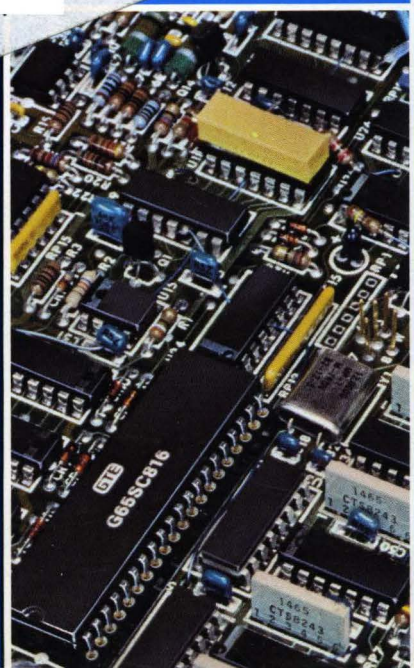
GTE Microcircuits

Data Book

Data Book



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Microcircuits

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2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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1 Microprocessors Microcomputers Peripherals

GTE Microcircuits

G65SCXX Series
G65SC1XX Series

Microcircuits

CMOS G65SCXXX 8-Bit Microprocessor Family

Features

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
  —64 microprocessor instructions
  —178 operational codes
  —15 addressing modes
- Choice of 4K, 8K or 65K-byte addressable memory
- 1, 2, 3 or 4 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Advanced memory access timing (ϕ4) on selected versions
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor designs

General Description

The G65SCXXX is a totally software-compatible microprocessor family manufactured using the state-of-the-art silicon gate CMOS process. The family consists of two series of devices: one series, designated G65SCXXX is pin-to-pin compatible with NMOS versions of the 6500 currently on the market; the other series, designated G65SC1XX includes several enhancements not available with other designs. The family provides the designer with a wide selection of addressable memory ranges, on-board or external clocks, and input interrupt options. All of the microprocessors are software compatible within the group and all are bus compatible with MC6800 products.

As shown in Table I, the family includes 18 microprocessors of which three have on-chip oscillators while the others require an external clock generator. The G65SC02, G65SC102 or G65SC112 clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The versions of the microprocessor which require an external clock source are generally intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

Ten of the microprocessors in the G65SCXX Series are pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users of the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption. (Continued on page 2)

TABLE I. G65SCXXX FAMILY MICROPROCESSOR CAPABILITIES

ITEM NO.	PART NUMBER	DIP PINS	ADDRESSABLE MEMORY (BYTES)	ON-BOARD CLOCK OSCILLATOR (SEE NOTE)	EXTERNAL CLOCK GENERATOR REQUIRED	ADVANCED MEMORY ACCESS (ϕ4)	$\overline{IRQ}$	$\overline{NMI}$	$\overline{SO}$	DBE	BE	SYNC	RDY	$\overline{ML}$	$\overline{RES}$
1	G65SC02	40	65K	•			•	•	•			•	•		•
2	G65SC03	28	4K		•		•	•							•
3	G65SC04	28	8K		•		•								•
4	G65SC05	28	4K		•		•						•		•
5	G65SC06	28	4K		•		•								•
6	G65SC07	28	8K		•								•		•
7	G65SC12	40	65K		•		•	•	•	•		•			•
8	G65SC13	28	4K		•		•	•							•
9	G65SC14	28	8K		•		•								•
10	G65SC15	28	4K		•		•						•		•
11	G65SC102	40	65K	•		•	•	•	•		•	•	•	•	•
12	G65SC103	28	4K		•	•	•	•							•
13	G65SC104	28	8K		•	•	•								•
14	G65SC105	28	4K		•	•	•						•		•
15	G65SC106	28	4K		•	•	•								•
16	G65SC107	28	8K		•	•							•		•
17	G65SC112	40	65K	•			•	•	•		•	•	•	•	•
18	G65SC115	28	4K		•		•						•	•	•

NOTE: These devices can operate in any of the following clock generation modes: 1. External crystal 2. External RC network 3. ϕ0(IN) from external clock source

General Description (Continued)

In addition to enhanced software programming, the use of CMOS processing also allows several hardware enhancements that are not available to users of the NMOS 6500 products. These hardware enhancements are listed and explained in Table II.

The G65SC1XX Series microprocessors (the "one-hundred" series) are a natural evolution of the 6500 product line. Basically, these products (G65SC102-107) have the same features as the G65SCXX Series, except these products also offer the designer the advantage of an on-board divide-by-four oscillator. The divide-by-four network permits the use of an economical television crystal (3.579545 MHz), plus the added advantage of increasing the access time (t_{ACC}) by approximately 25 percent.

On the G65SC102, additional features include memory lock output ($\overline{ML}$) and bus enable (BE), both of which will tend to simplify system applications. These functions are explained in the section of this data sheet entitled "Signal Description."

All versions of the G65SCXXX microprocessor family are available in plastic, ceramic, cerdip, or leadless chip carrier packaging. All versions are available in 1, 2, 3 and 4 MHz maximum operating frequencies.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

Parameter	Symbol	Min	Max	Unit
Input High Voltage				
ϕ0(IN), CLK (IN)		2.4	V_{DD} + 0.3	V
ϕ2 (IN)	V_{IH}	V_{DD} - 0.2	V_{DD} + 0.3	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		2.0	V_{DD} + 0.3	V
Input Low Voltage				
ϕ0 (IN), CLK (IN)		-0.3	0.4	V
ϕ2 (IN)	V_{IL}	-0.3	0.2	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD})				
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, $\overline{SO}$, DBE, BE (Internal Pull-Up),	I_{IN}			
CLK (IN) [10X]			1.0/-100	μA
ϕ2 (IN), ϕ0 (IN), CLK (IN) [0X, 1X, 11X]			±1.0	μA
Three-State Leakage Current				
Address, Data, R/$\overline{W}$	I_{TSI}		±10.0	μA
Output High Voltage (I_{OH} = -100 μA, V_{DD} = 4.75V)				
SYNC, Data, A0-A15, R/$\overline{W}$	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 1.6 mA, V_{DD} = 4.5V)				
SYNC, Data, A0-A15, R/$\overline{W}$	V_{OL}	—	0.4	V
Supply Current f = 1 MHz	I_{DD}	—	4	mA
(No Load) f = 2 MHz			8	
f = 3 MHz			12	
f = 4 MHz			16	
Standby Power Dissipation (ϕ2 = V_{IH}, Inputs = V_{SS} or V_{DD}	P_{SBY}		50.0	μW
Outputs Unloaded)				
Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz)				pF
Logic, ϕ0(IN), CLK (IN)	C_{IN}	—	10	
A0-A15, R/$\overline{W}$ Data (Three-State)	C_{TS}	—	15	
ϕ2 (IN)	C2 (IN)	—	40	

AC Characteristics, G65SC02-07, G65SC12-15, G65SC112, 115: V_{DD} = 5.0V ±5%, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, $\phi 0$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 0}$	—	40	—	40	—	40	—	40	nS
Delay Time, $\phi 2$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 2}$	—	35	—	35	—	35	—	35	nS
Delay Time, $\phi 1$ (OUT) to $\phi 2$ (OUT)	$t_{D\phi 1}$	—	50	—	50	—	50	—	50	nS
Delay Time, $\phi 2$ (OUT) to $\overline{OSC}$ (OUT)	t_{DOSC}	—	50	—	50	—	50	—	50	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	μS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	10000	240	10000	160	10000	115	10000	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	160	—	115	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	—	15	—	15	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	15	—	nS
Address Setup Time	t_{ADS}	—	225	—	140	—	110	—	90	nS
Access Time	t_{ACC}	675	—	310	—	170	—	110	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	100	—	50	—	50	—	50	—	nS
Write Data Delay Time	t_{MDS}	—	175	—	100	—	75	—	70	nS
Write Data Hold Time	t_{DHW}	15	—	15	—	15	—	15	—	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	225	—	140	—	110	—	90	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, t_{MLH}	—	0	—	0	—	0	—	0	nS
$\overline{SO}$ Setup Time	t_{SO}	100	—	50	—	35	—	25	—	nS
Processor Control Setup Time	t_{PCS}	200	—	200	—	150	—	120	—	nS

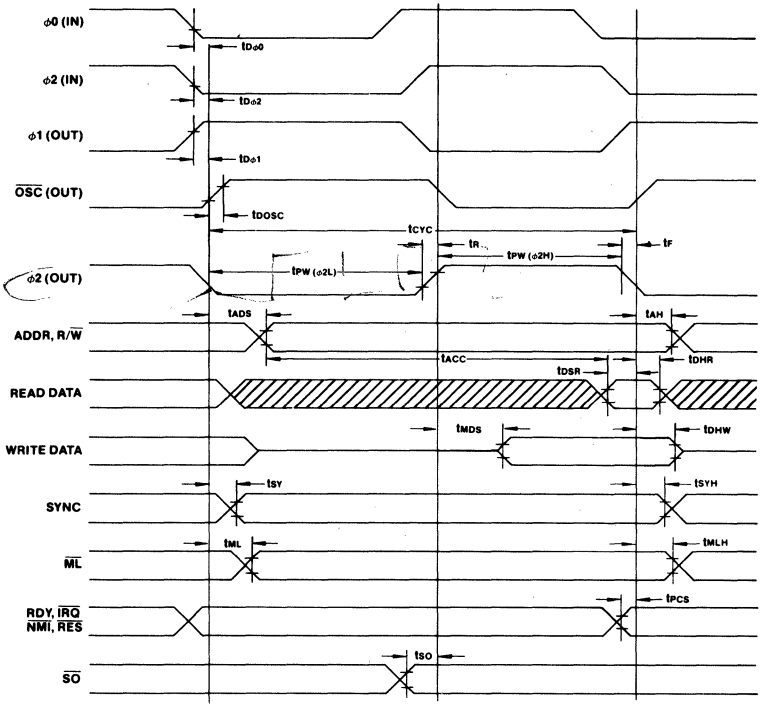
AC Characteristics, G65SC102-107: V_{DD} = 5.0V ±5%, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, CLK (IN) to $\phi 2$ (OUT)	t_{DCLK}	—	75	—	75	—	75	—	75	nS
Delay Time, $\overline{OSC}$ (OUT) to $\phi 2$ (OUT)	t_{DOSC}	—	70	—	70	—	70	—	70	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	μS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	10000	240	10000	160	10000	115	10000	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	160	—	115	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	—	15	—	15	nS
Delay Time, $\phi 2$ (OUT) to $\phi 4$ (OUT)	t_{AVS}	—	250	—	125	—	83	—	63	nS
Address Valid to $\phi 4$ (OUT)	$t_{A\phi 4}$	50	—	25	—	16	—	12	—	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	15	—	nS
Access Time	t_{ACC}	695	—	340	—	220	—	170	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	80	—	40	—	30	—	20	—	nS
Write Data Hold Time	t_{DHW}	15	—	15	—	15	—	15	—	nS
Write Data Delay Time	$t_{DD\phi 4}$	—	200	—	110	—	70	—	30	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	225	—	140	—	110	—	90	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, t_{MLH}	—	225	—	140	—	110	—	90	nS
$\overline{SO}$ Setup Time	t_{SO}	100	—	50	—	35	—	25	—	nS
Processor Control Setup Time	t_{PCS}	100	—	50	—	35	—	25	—	nS

TIMING DIAGRAM:

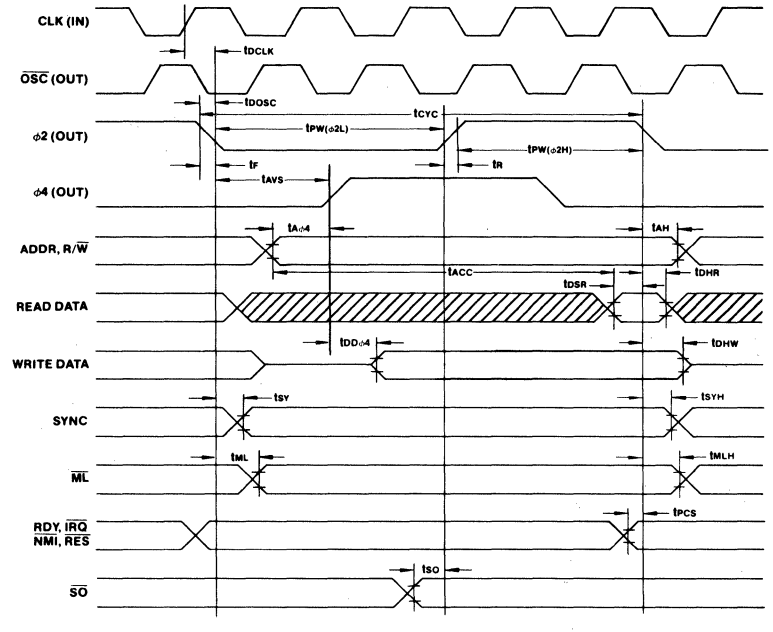
G65SC02, 03, 04, 05, 06, 07
G65SC12, 13*, 14*, 15*
G65SC112, 115*

*Variation of timing required. Contact factory for details.

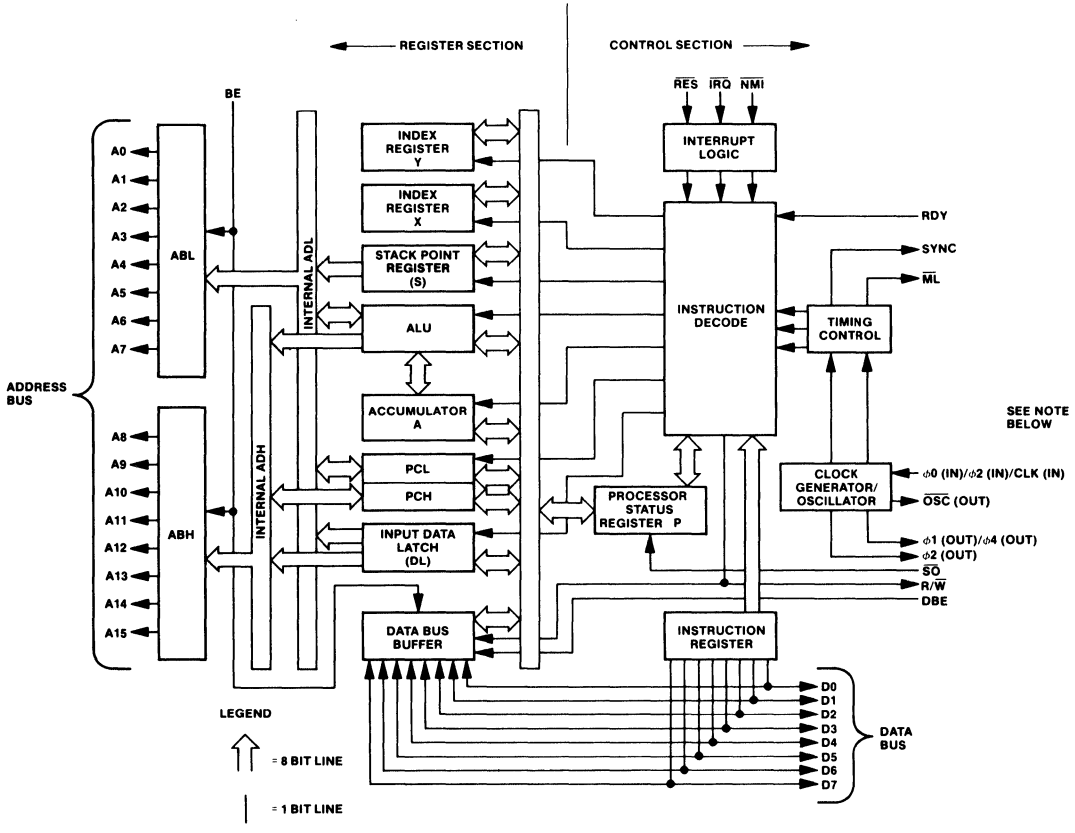


TIMING DIAGRAM:

G65SC102-107



Notes:
1. Load = 100 pF.
2. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.



Note: Refer to Table I for signal input/output applicability.

Figure 1. Internal Architecture Simplified Block Diagram

Functional Description

Timing Control
The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter
The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode
Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)
All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Functional Description (Continued)

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Signal Description

Address Bus (AO-AXX)

Refer to the particular package configuration for the respective number of address lines.

In both the 40-pin and 44-pin packages, A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The address lines are set (See BE below.) to the high impedance state by the bus enable (BE) signal. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

Bus Enable (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers.

Clock In (CLK (IN))

The 65SC10X Series is supplied with an internal clock generator operating at four times the $\phi 2$ frequency. The frequency of these clocks is externally controlled by the crystal or oscillator circuit shown in Figure 2.

Phase 0 In (ϕ0(IN))

This is the buffered clock input to the internal clock generator on the G65SC0X series. Clock outputs $\phi 1$(OUT) and $\phi 2$(OUT) are derived from this signal.

Phase 2 In (ϕ2(IN))

This is the unbuffered clock input to the internal clock generator on the G65SC1X and G65SC11X series. The clock output, $\phi 2$(OUT), is derived from this signal.

Data Bus Enable (DBE)

This TTL-compatible input allows external control of the three-state data output buffers. In normal operation, DBE would be driven by the phase two ($\phi 2$) clock, thus allowing data input from microprocessor only during $\phi 2$. During the read cycle, the data bus buffers are internally disabled, becoming essentially an open circuit. To disable the data bus externally, DBE should be held low.

Data Bus (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF. The data lines are set to the high impedance state by BE or DBE.

Interrupt Request ($\overline{IRQ}$)

This TTL compatible signal requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during $\phi 2$ operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during $\phi 1$. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire-OR operation.

Memory Lock ($\overline{ML}$)

In a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during $\phi 2$; the current instruction is completed and the interrupt sequence begins during $\phi 1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. However, it should be noted this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. Also, no interrupt will occur if $\overline{NMI}$ is low and negative-going edge has not occurred since the last non-maskable interrupt.

Oscillator Out ($\overline{OSC}$ (OUT))

On the G65SC102 microprocessor, an internal inverter and a resistor are connected between pins 35 and 37 on the DIP package and pins 39 and 41 on the PLCC package. The inverter has sufficient loop gain to provide oscillation using an external crystal.

Phase 1 Out (ϕ1(OUT))

This inverted $\phi 2$(OUT) signal provides timing for external R/$\overline{W}$ operations.

Phase 2 Out (ϕ2(OUT))

This signal provides timing for external bus R/$\overline{W}$ operations. Addresses are valid after the address setup time (t_{ADS}) from the falling edge of $\phi 2$(OUT).

Phase 4 Out (ϕ4(OUT))

This signal is delayed by t_{AVS} from $\phi 2$(OUT). The address output is valid prior to the rising edge of $\phi 4$(OUT).

Signal Description (Continued)

Ready (RDY)
This input signal allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\phi 2$) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

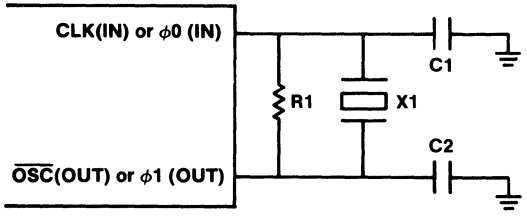
Reset ($\overline{RES}$)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. After the system has been operating, a low on this line of at least two cycles will cease microprocessing activity.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The previous program counter and status register values are written to the stack memory area. Then the interrupt mask flag is set, the decimal mode is cleared and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

Read/Write (R/$\overline{W}$)
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location. R/$\overline{W}$ is set to the high impedance state by BE.

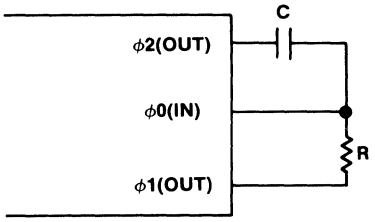
Set Overflow ($\overline{SO}$)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of $\phi 1$.

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.



C1, C2 = 51pF
R1 = 200KΩ
X1 = 1MHz

Figure 2(a). Crystal Circuit for Internal Oscillator



Suggested RC network configuration for internal oscillator.

1 MHz operation at V_{DD} = 5.0V:
C = 56pF
R = 5.6 KΩ

Figure 2(b). RC Circuit for Internal Oscillator

Table II. Microprocessor Hardware Enhancements

Function	NMOS 6500	G65SCXXX Family
Oscillator.	Requires external active components.	Crystal or RC network will oscillate when connected between $\phi 0$ (IN) and $\phi 1$ (OUT).
Assertion of Ready (RDY) during write operations.	Ignored.	Stops processor during $\phi 2$.
1X series clock inputs.	Two non-overlapping clock inputs ($\phi 1$ and $\phi 2$) are required.	$\phi 2$ (IN) is the only required clock.
Unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, $\overline{SO}$, DBE, BE).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 1 Megohm).

Addressing Modes

Fifteen addressing modes are available to the user of the GTE G65SCXXX family of microprocessors. The addressing modes are described in the following paragraphs:

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing
For absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Therefore, this addressing mode allows access to the total 65K bytes of addressable memory.

Zero Page Addressing
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing
Absolute indexed addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Zero Page Indexed Addressing
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

Relative Addressing
Relative addressing is used only with branch instruction; it establishes a destination for the conditional branch.

Zero Page Indexed Indirect Addressing
With zero page indexed indirect addressing (usually referred to as Indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Absolute Indexed Indirect Addressing (Jump Instruction Only)
With absolute indexed indirect addressing, the contents of the second and third instruction bytes are added to the X register. The result of this addition points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Zero Page Indirect Addressing
In this form of addressing, the second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits is always zero. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address.

Absolute Indirect Addressing (Jump Instruction Only)
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the 16 bits of the program counter.

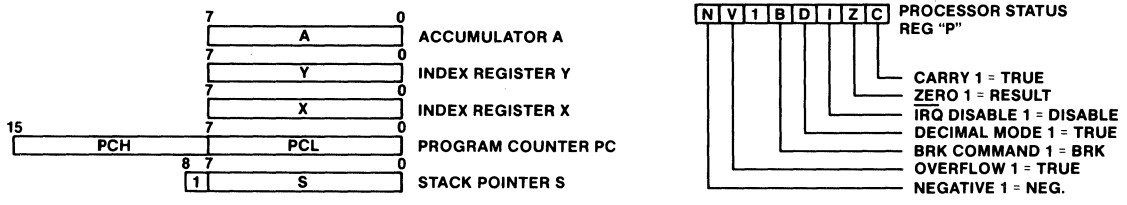


Figure 3. Microprocessor Programming Model

Table III. Instruction Set—Alphabetical Sequence

	ADC	Add Memory to Accumulator with Carry
	AND	"AND" Memory with Accumulator
	ASL	Shift One Bit Left
	BCC	Branch on Carry Clear
	BCS	Branch on Carry Set
	BEQ	Branch on Result Zero
	BIT	Test Memory Bits with Accumulator
	BMI	Branch on Result Minus
	BNE	Branch on Result Not Zero
	BPL	Branch on Result Plus
●	BRA	Branch Always
	BRK	Force Break
	BVC	Branch on Overflow Clear
	BVS	Branch on Overflow Set
	CLC	Clear Carry Flag
	CLD	Clear Decimal Mode
	CLI	Clear Interrupt Disable Bit
	CLV	Clear Overflow Flag
	CMP	Compare Memory and Accumulator
	CPX	Compare Memory and Index X
	CPY	Compare Memory and Index Y
	DEC	Decrement by One
	DEX	Decrement Index X by One
	DEY	Decrement Index Y by One
	EOR	"Exclusive-or" Memory with Accumulator
	INC	Increment by One
	INX	Increment Index X by One
	INY	Increment Index Y by One
	JMP	Jump to New Location
	JSR	Jump to New Location Saving Return Address
	LDA	Load Accumulator with Memory
	LDX	Load Index X with Memory
	LDY	Load Index Y with Memory
	LSR	Shift One Bit Right
	NOP	No Operation
	ORA	"OR" Memory with Accumulator
	PHA	Push Accumulator on Stack
	PHP	Push Processor Status on Stack
●	PHX	Push Index X on Stack
●	PHY	Push Index Y on Stack
	PLA	Pull Accumulator from Stack
	PLP	Pull Processor Status from Stack
●	PLX	Pull Index X from Stack
●	PLY	Pull Index Y from Stack
	ROL	Rotate One Bit Left
	ROR	Rotate One Bit Right
	RTI	Return from Interrupt
	RTS	Return from Subroutine
	SBC	Subtract Memory from Accumulator with Borrow
	SEC	Set Carry Flag
	SED	Set Decimal Mode
	SEI	Set Interrupt Disable Bit
	STA	Store Accumulator in Memory
	STX	Store Index X in Memory
	STY	Store Index Y in Memory
●	STZ	Store Zero in Memory
	TAX	Transfer Accumulator to Index X
	TAY	Transfer Accumulator to Index Y
●	TRB	Test and Reset Memory Bits with Accumulator
●	TSB	Test and Set Memory Bits with Accumulator
	TSX	Transfer Stack Pointer to Index X
	TXA	Transfer Index X to Accumulator
	TXS	Transfer Index X to Stack Pointer
	TYA	Transfer Index Y to Accumulator

Note: ● = New Instruction

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB zpg	ORA zpg	ASL zpg		PHP	ORA imm	ASL A		TSB abs	ORA abs	ASL abs		0
1	BPL rel	ORA ind, Y	ORA ind		TRB zpg	ORA zpg, X	ASL zpg, X		CLC	ORA abs, Y	INC A		TRB abs	ORA abs, X	ASL abs, X		1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg		PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs		2
3	BMI rel	AND ind, Y	AND ind		BIT zpg, X	AND zpg, X	ROL zpg, X		SEC	AND abs, Y	DEC A		BIT abs, X	AND abs, X	ROL abs, X		3
4	RTI	EOR ind, X				EOR zpg	LSR zpg		PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs		4
5	BVC rel	EOR ind, Y	EOR ind			EOR zpg, X	LSR zpg, X		CLI	EOR abs, Y	PHY			EOR abs, X	LSR abs, X		5
6	RTS	ADC ind, X			STZ zpg	ADC zpg	ROR zpg		PLA	ADC imm	ROR A		JMP ind	ADC abs	ROR abs		6
7	BVS rel	ADC ind, Y	ADC ind		STZ zpg, X	ADC zpg, X	ROR zpg, X		SEI	ADC abs, Y	PLY		JMP ind, X	ADC abs, X	ROR abs, X		7
8	BRA rel	STA ind, X			STY zpg	STA zpg	STX zpg		DEY	BIT imm	TXA		STY abs	STA abs	STX abs		8
9	BCC rel	STA ind, Y	STA ind		STY zpg, X	STA zpg, X	STX zpg, Y		TYA	STA abs, Y	TXS		STZ abs	STA abs, X	STZ abs, X		9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg		TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs		A
B	BCS rel	LDA ind, Y	LDA ind		LDY zpg, X	LDA zpg, X	LDX zpg, Y		CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y		B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg		INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs		C
D	BNE rel	CMP ind, Y	CMP ind			CMP zpg, X	DEC zpg, X		CLD	CMP abs, Y	PHX			CMP abs, X	DEC abs, X		D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg		INX	SBC imm	NOP		CPX abs	SBC abs	INC abs		E
F	BEQ rel	SBC ind, Y	SBC ind			SBC zpg, X	INC zpg, X		SED	SBC abs, Y	PLX			SBC abs, X	INC abs, X		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note: ▨ = New Op Codes

Figure 4. Microprocessor Op Code Table

Table IV. Operational Codes, Execution Time, and Memory Requirements

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND, X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3												N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3												M7 M6 • • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																								• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																								• • • • • • 0	CLC
CLD	0 → D										D8	2	1																								• • • 0 • • •	CLD
CLI	0 → I										58	2	1																								• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																								• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3												N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																								N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																								N • • • • Z •	DEY
EOR	A ∀ M →A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3												N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																								N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																								N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3															6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																														• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3												N • • • • Z •	LDY
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3												0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																								• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A→Ms S-1→S										48	3	1																								• • • • • • •	PHA
PHP	P→Ms S-1→S										08	3	1																								• • • • • • •	PHP
PHX	X→Ms S-1→S										DA	3	1																								• • • • • • •	PHX
PHY	Y→Ms S-1→S										5A	3	1																								• • • • • • •	PHY
PLA	S+1→S Ms→A										68	4	1																								N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																								N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																								N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																								N • • • • Z •	PLY
ROL	[← [7 0] ←C]				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3												N • • • • Z C	ROL
ROR	[→C→ [7 0]]				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3												N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																								N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																								• • • • • • •	RTS
SBC	A-M-C̄→A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																								• • • • • • 1	SEC
SED	1 → D										F8	2	1																								• • • 1 • • •	SED
SEI	1 → I										78	2	1																								• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																											96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																	• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3												• • • • • • •	STZ
TAX	A → X										AA	2	1																								N • • • • Z •	TAX
TAY	A → Y										A8	2	1																								N • • • • Z •	TAY
TRB	A̅∧M → M (6)				1C	6	3	14	5	2																												• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																												• • • • • Z •	TSB
TSX	S → X										BA	2	1																								N • • • • Z •	TSX
TXA	X → A										8A	2	1																								N • • • • Z •	TXA
TXS	X → S										9A	2	1																								• • • • • • •	TXS
TYA	Y → A										98	2	1																								N • • • • Z •	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates A∧M result (same as BIT instruction).

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
\- Subtract
∧ And
V Or
∀ Exclusive or

n No. Cycles
No. Bytes
M6 Memory Bit #6
M7 Memory Bit #7

Enhanced Operational Characteristics

The GTE G65SCXXX family of microprocessors is a complete series of devices designed for building state-of-the-art microcomputer systems. Each member of the family is carefully designed to be hardware compatible, utilize the same basic software instruction set, and to be bus compatible with the MC6800 product line. Accordingly, the G65SCXX series is pin compatible with existing NMOS 6500 type microprocessors.

However, as stated previously, the CMOS design allows several operational enhancements to be incorporated in the current product. These operational enhancements are explained in Table V.

Table V. Microprocessor Operational Enhancements

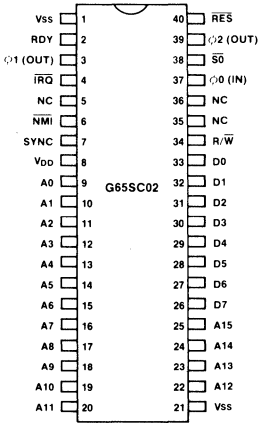
Function	NMOS 6500 Microprocessor	G65SCXXX Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code — Bytes — Cycles X2 — 2 — 2 X3, X7, XB, XF — 1 — 1 44 — 2 — 3 54, D4, F4 — 2 — 4 5C — 3 — 8 DC, FC — 3 — 4
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments, one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags. One additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded; BRK vector is ignored.	BRK is executed, then interrupt is executed.
Reset	Reads three stack locations.	Writes program counter and status register to stack
Read/Modify/Write instructions absolute indexed in same page.	Seven cycles.	Six cycles.

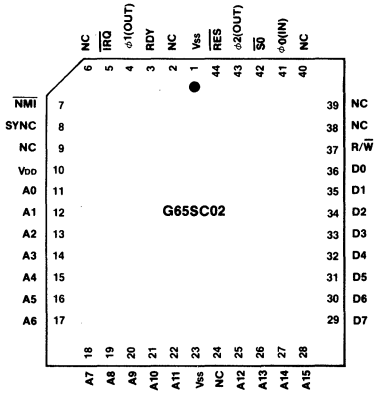
Pin Function

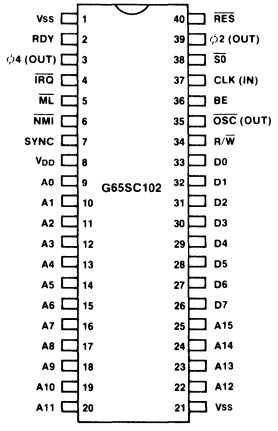
Pin	Description
A0-Axx	Address Bus
BE	Bus Enable
CLK (IN)	Clock Input
ϕ0(IN)	Phase 0 In
ϕ2(IN)	Phase 2 In
DBE	Data Bus Enable
D0-D7	Data Bus
$\overline{IRQ}$	Interrupt Request
$\overline{ML}$	Memory Lock
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt

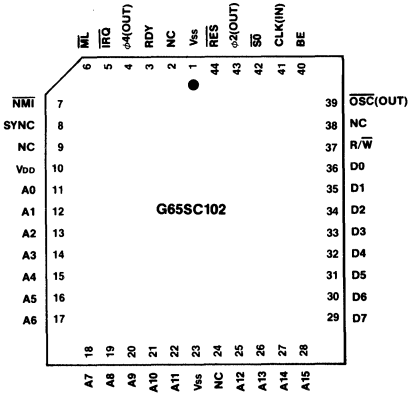
Pin	Description
$\overline{OSC}$ (OUT)	Oscillator Output
ϕ1(OUT)	Phase 1 Out
ϕ2(OUT)	Phase 2 Out
ϕ4(OUT)	Phase 4 Out
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
V_{DD}	Positive Power Supply (+5.0 Volts)
V_{SS}	Internal Logic Ground

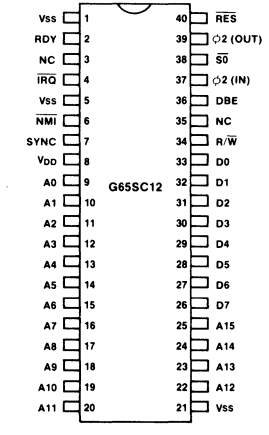
Pin Configuration

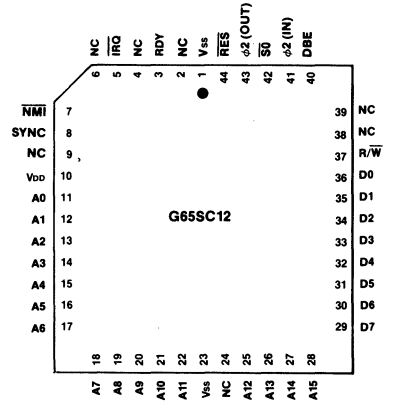












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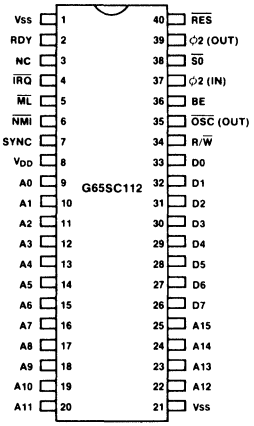

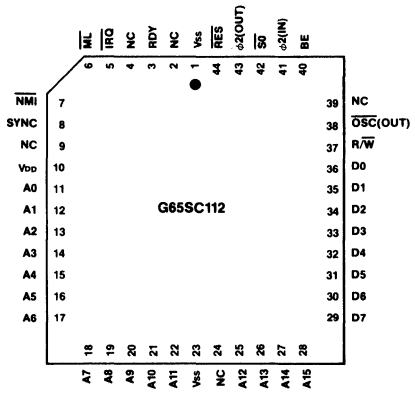

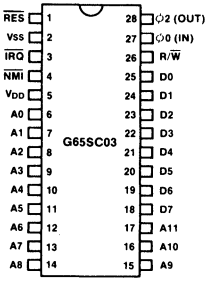

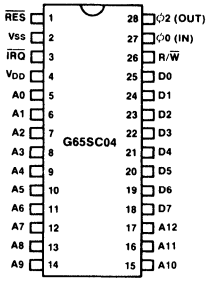

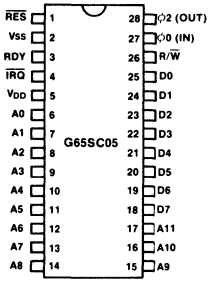

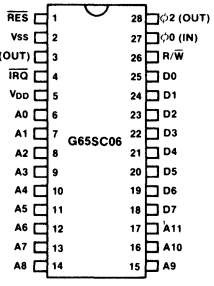

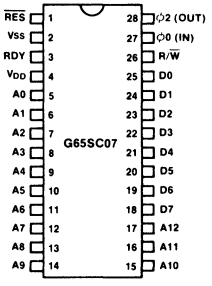

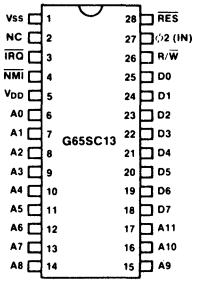

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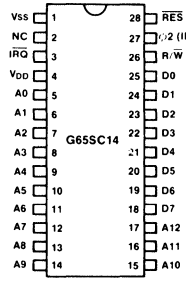
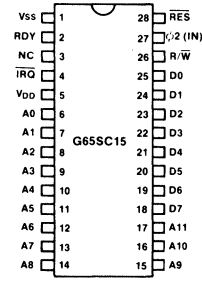
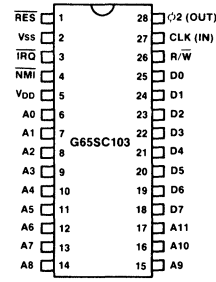
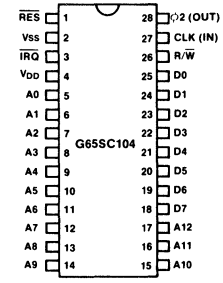
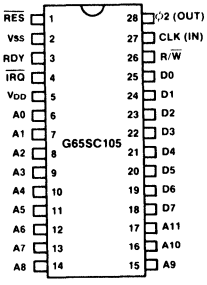
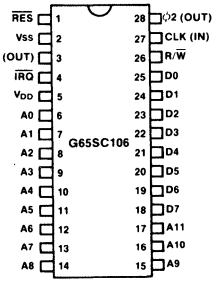


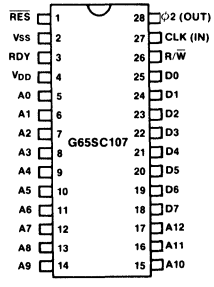


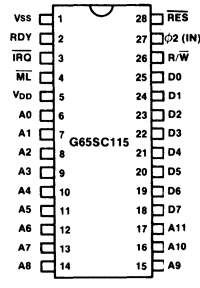












Ordering Information

G 65SCXXX A P I -2

Description

C—Special G—Standard

Product Identification Number

Version

Package

P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing

None— 0°C to +70°C, ± 5% P.S. Tol. S— 0°C to +70°C, ± 10% P.S. Tol.
I— -40°C to +85°C, ± 5% P.S. Tol. W— -40°C to +85°C, ± 10% P.S. Tol.

Performance Designator

Designators selected for speed and power specifications

—1 1MHz —3 3 MHz
—2 2 MHz —4 4 MHz

G65SC21

Microcircuits

CMOS Peripheral Interface Adapter

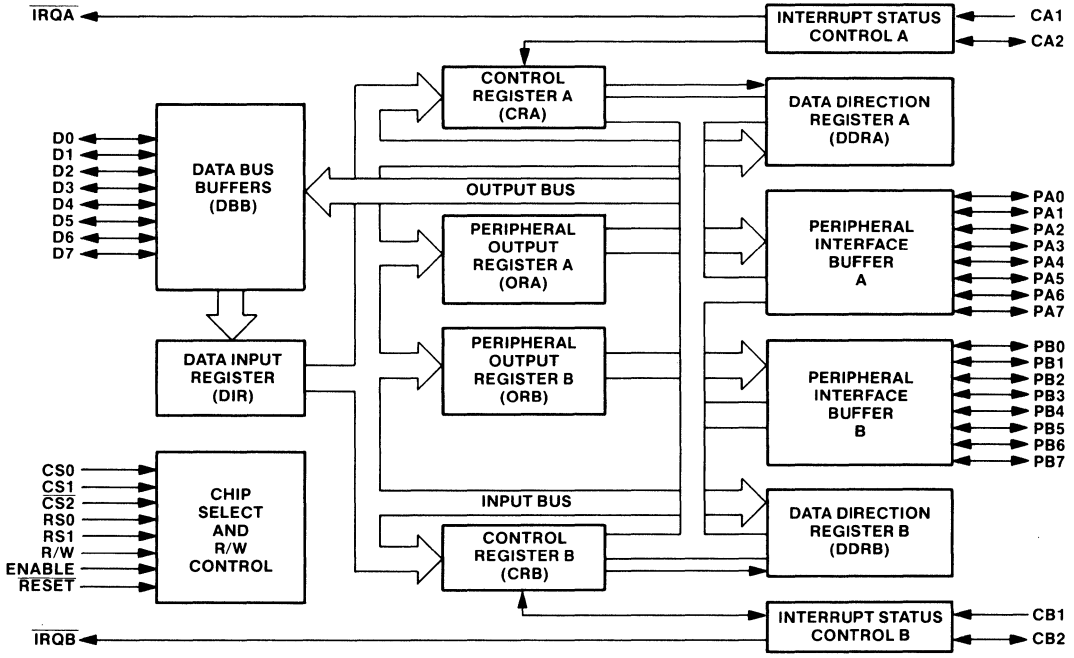
Features

- CMOS process technology for low power consumption
- Direct replacement for NMOS 6521 and 6821 devices manufactured by others
- Low power consumption (2 mA at 1MHz) allows battery powered operation
- Two programmable 8-bit bidirectional I/O Ports for peripheral device interfacing
- Individual Data Direction Registers for each I/O Port
- Microprocessor/peripheral "handshake" interrupt feature for enhanced data transfer control
- Programmable interrupt capability
- Four operating frequencies—1, 2, 3 and 4 MHz
- Automatic power-up initialization
- Single +5 volt power supply
- Available in 40-pin dual-in-line or 44-pin PLCC package

General Description

The GTE G65SC21 is a very flexible Peripheral Interface Adapter for use with GTE and other 8-bit microprocessor families. The G65SC21 provides programmed microprocessor control of up to two peripheral devices (Port A and Port B). Peripheral device control is accomplished through two 8-bit bidirectional I/O Ports, with individually assigned Data Direction Registers. The Data Direction Registers allow selection of data flow direction (input or output) at each respective I/O Port. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. The "handshake" interrupt control feature is provided by four peripheral control lines. This capability provides enhanced control over data transfer functions between the microprocessor and peripheral devices, as well as bidirectional data transfer between G65SC21 Peripheral Interface Adapters in multiprocessor systems.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, ϕ2	I_{IN}		±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, PB0-PB7, CB2, $\overline{IRQA}$, $\overline{IRQB}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IL}		-2.4	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7, CB2	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	P_D P_{DSB}		11.0 11.0	mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

		G65SC21-1		G65SC21-2		G65SC21-3		G65SC21-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS

AC Characteristics: (Continued)

Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay (Port A)	t_{CPW}	—	1000	—	500	—	330	—	320	nS
(Port B)		—	1000	—	500	—	330	—	250	

Note: Measurement points 0.8V and 2.0V unless otherwise specified.

AC Characteristics—Peripheral Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
CA2 Delay Time, High-to-Low	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CA2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CA2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	μS
CB2 Delay Time, High-to-Low	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CB2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CB2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	μS
CB2 Delay Time from Data Valid	t_{DC}	20	—	20	—	20	—	20	—	nS
Interrupt Input Pulse Width	P_{WI}	500	—	500	—	330	—	250	—	nS
Interrupt Response Time	t_{RS3}	—	1.0	—	1.0	—	0.67	—	0.33	μS
Interrupt Clear Delay	t_{IR}	—	1.6	—	0.85	—	0.67	—	0.33	μS
Rise and Fall Times— CA1, CA2, CB1, CB2	t_R, t_F	—	1.0	—	1.0	—	0.67	—	0.33	μS

Timing Diagrams

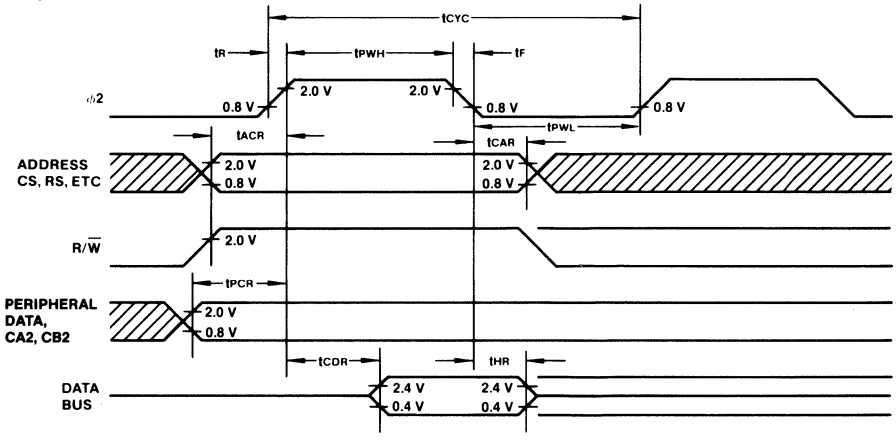


Figure 1. Read Timing

Timing Diagram (continued)

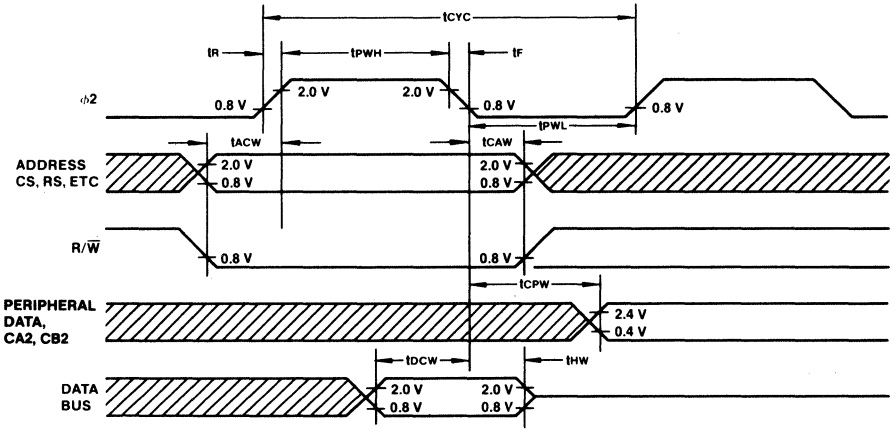


Figure 2. Write Timing

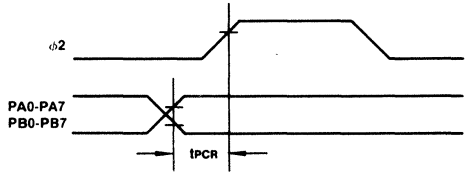


Figure 3. Peripheral Data Setup Time

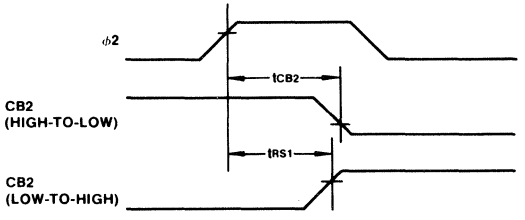


Figure 6. CB2 Timing

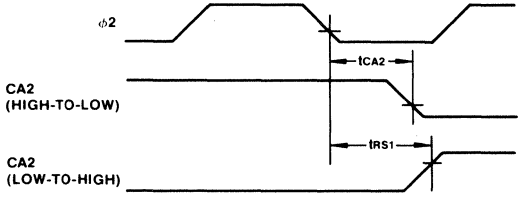


Figure 4. CA2 Timing

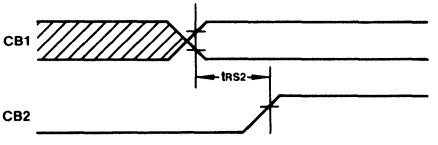


Figure 7. CB1/CB2 Handshake Timing

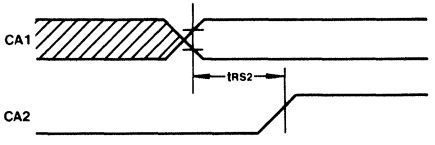


Figure 5. CA1/CA2 Timing

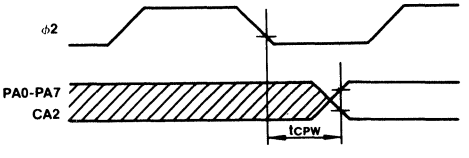


Figure 8. PA Port Delay Time

Timing Diagrams (continued)

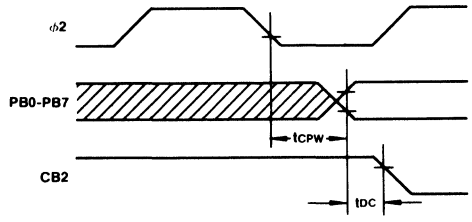


Figure 9. PB Port Delay Time

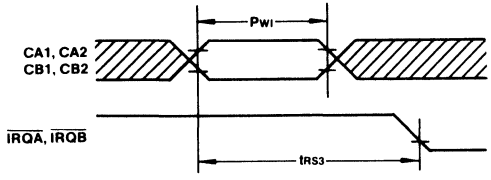


Figure 10. Interrupt Timing

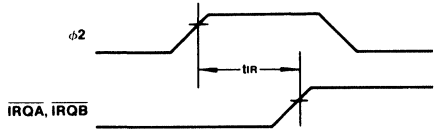
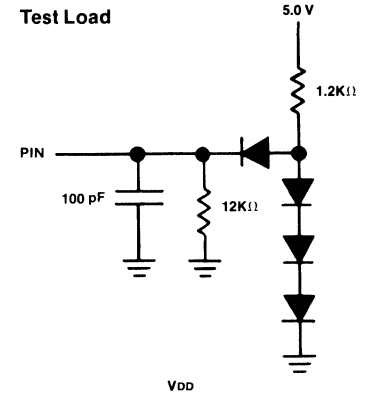
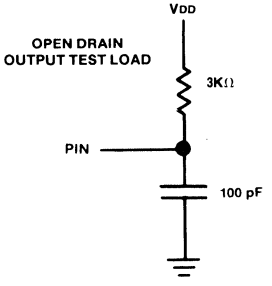


Figure 11. Interrupt Clear Timing





	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 12. Control Registers

REGISTER SELECT PIN		DATA DIRECTION REGISTER ACCESS CONTROL BIT		
RS1	RS0	CRA-2	CRB-2	REGISTER SELECTED
0	0	1	—	Peripheral Interface A
0	0	0	—	Data Direction Register A
0	1	—	—	Control Register A
1	0	—	1	Peripheral Interface B
1	0	—	0	Data Direction Register B
1	1	—	—	Control Register B

Figure 13. Register Addressing

Signal Description

Data Bus (D0-D7)
The eight bidirectional data bus lines are used to transfer data between the G65SC21 and the microprocessor.

During a Read operation, the contents of the G65SC21 internal Data Bus Buffer (DBB) are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines represent high impedance inputs over which data is transferred from the microprocessor to the Data Input Register (DIR). The Data Bus lines are in the high impedance state when the G65SC21 is unselected.

Chip Select (CS0, CS1, $\overline{CS2}$)
Normally, the three Chip Select lines are connected to the microprocessor address lines. This connection may be either direct or through an external decoder. To access the G65SC21, CS0 and CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0, RS1)
The Register Select inputs allow the microprocessor to select G65SC21 internal registers as presented in Figure 13.

Read/Write (R/$\overline{W}$)
The Read/Write signal is generated by the microprocessor and is used to control the transfer of data between the G65SC21 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC21 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC21 internal register (Write operation). Read/Write must always be preceded by Chip Select (CS0, CS1 and $\overline{CS2}$).

Input Clock (ϕ2)
The system ϕ2 Input Clock controls all data transfers between the G65SC21 and the microprocessor.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)
The Interrupt Request ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B) output signals become true (Logic 0) whenever an internal interrupt condition is determined by Interrupt Status Control Registers A and B. These two signals are active low and have open-drain outputs. The open-drain configuration allows the Interrupt Request signals to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Reset ($\overline{RES}$)
A low signal (Logic 0) on the Reset line serves to initialize the G65SC21, clearing all internal registers and placing all peripheral interface lines (PA and PB) in the input state.

Peripheral Data Port A (PA0-PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Each data port bus line may be individually programmed as either an input or output under control of the Data Direction Register (DDRA). Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port.

Peripheral Data Port B (PB0-PB7)
Peripheral Data Port B is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Functional operation is identical to Peripheral Data Port A, thus allowing the G65SC21 to independently control two peripheral devices.

Interrupt Status Control—
CA1, CA2 (Port A) and CB1, CB2 (Port B)
The two Interrupt Status Control lines for each Data Port are controlled by the Interrupt Status Control logic (A and B). This logic interprets the contents of the corresponding Control Register (CRA and CRB), allowing the Interrupt Status Control lines to perform various peripheral control functions.

Functional Description

Organization of the G65SC21 consists of two independent control sections (A and B). Section A and Section B are identical—each consisting of a Control Register (CRA and CRB), Data Direction Register (DDRA and DDRB), Output Register (ORA and ORB), Interrupt Status Control (A and B) and Peripheral Interface Buffers (A and B). The Data Bus Buffers (DBB), Data Input Register (DIR) and the Chip Select and Read/Write control logic is common to both sections. Refer to the Block Diagram on Page 1.

Data Input Register (DIR)
During a Write data operation, the microprocessor writes data into the G65SC21 by placing data on the Data Bus. This data is then latched into the Data Input Register by the Phase Two (ϕ2) clock. Once in the Data Input Register, this data byte is transferred into one of six internal registers. This data transfer occurs after the trailing edge of the ϕ2 clock pulse that latched the data byte into the Data Input Register. This timing delay guarantees the data on the peripheral output lines (PA or PB) will make a smooth transition from low to high or high to low, and the output voltage will remain stable when there is to be no change in polarity.

Control Registers (CRA and CRB)
The individual Control Registers allow the microprocessor to program the operation of the Interrupt Control inputs (CA1, CA2, CB1, and CB2), and the Peripheral Control outputs (CA2 and CB2). Refer to Figure 4. Bit 2 in each Control Register controls the addressing of the Data Direction Registers (DDRA and DDRB) and also the Output Registers (ORA and ORB). Bits 6 and 7 are interrupt flag bits which indicate the status of the Interrupt Status Control input lines (CA1, CA2, CB1, and CB2). These two interrupt status flags are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These two interrupt lines drive the interrupt input ($\overline{IRQ}$ and $\overline{NMI}$) of the microprocessor.

Interrupt Status Control Logic (A and B)
The G65SC21 contains four interrupt/peripheral control lines (CA1, CA2, CB1, and CB2). These lines are controlled by the Interrupt Status Control logic (A and B). The Interrupt Status Control logic serves to interpret the contents of the corresponding Control Register, thus allowing these lines to perform various control functions as described in Figure 16.

Data Direction Registers (DDRA and DDRB)
By use of the Data Direction Registers (DDR), the microprocessor can program each individual peripheral I/O Port line as an input or output. Each bit within the register controls a corresponding line of the I/O Port, with DDRA controlling peripheral I/O Port A and DDRB controlling I/O Port B. A programmed "0" in any bit position of a DDR results in the corresponding I/O Port line being designated as an input. A "1" results in the line being an output.

Peripheral Output Registers (ORA and ORB)
All output data to a peripheral is stored in the corresponding Output Register (ORA or ORB). This data is then presented to the Peripheral Interface Buffer (A and B) and placed on the respective I/O Port lines. Writing a "0" into any bit position of ORA or ORB results in the corresponding peripheral I/O Port line going low (<0.4V), providing that particular line is programmed as an output. Writing a "1" into a bit position results in the corresponding output going high.

Register Access and Selection

Register Select lines RS0 and RS1 are used in combination with Chip Select to access the six function registers within the G65SC21. These lines are normally connected to the microprocessor address output lines. As can be seen from Figure 13, the Register Select lines are used in combination with bit 2 of the Control Registers (CRA and CRB) to access the Data Direction Registers (DDRA and DDRB) and the peripheral interface Output Registers (ORA and ORB). If bit 2 is a Logic 1, a Peripheral Output Register is selected, and if bit 2 is a Logic 0, a Data Direction Register is selected. Thus, with appropriate addressing the microprocessor can write directly into the Control Registers, the Data Direction Registers, and the peripheral interface Output Registers. Also, the microprocessor can read the contents of the Control Registers and the Data Direction Registers.

Data Access—Peripheral I/O Port A

Depending on the contents of Data Direction Register A, the eight lines of Peripheral I/O Port A may be programmed as either inputs or outputs. When a particular line(s) is programmed as an output, it will reflect the contents of the corresponding bit in peripheral Output Register A (ORA). When programmed as inputs, these lines will reflect the logic state of corresponding peripheral input data. Lines programmed as inputs are not affected by the peripheral Output Register (ORA). To perform a Read operation (RS1 = 0, RS0 = 0, and Data Direction Register Access Control bit (CRA-2) = 1), data on peripheral I/O Port A lines is directly transferred to the microprocessor via the Data Bus. The transferred byte will contain both input and output data from all eight I/O Port A lines. It is the responsibility of the microprocessor to recognize and interpret only those bits which are important to a particular peripheral operation being performed. Note that the microprocessor always reads the I/O Port A "pins" and not the contents of the ORA. This being the case, the actual data read into the microprocessor may differ from the contents of the peripheral ORA, i.e., for a particular data "output" line. This condition occurs when the I/O pin is not allowed to reach a full +2.4 volts DC for a Logic 1. When this occurs, the microprocessor will read a Logic 0, even though the corresponding bit in the peripheral ORA is a Logic 1.

Data Access—Peripheral I/O Port B

When reading peripheral I/O Port B, a combination of input and output data is read in a similar manner to peripheral I/O Port A above. The major difference is that for I/O Port B, data is read directly from peripheral Output Register B (ORB) for those lines programmed as outputs. This being the case, it is possible to load down I/O Port B lines without causing incorrect data to be transferred to the microprocessor during a Read operation.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)

Both Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$) lines are active low, and serve to interrupt the microprocessor either directly or through external interrupt priority circuitry. Each line is "open drain" and is capable of sinking 3.2 milliamps from an external source, thus allowing all interrupts to be tied together in a wired-OR configuration. Each Interrupt Request line is assigned to a particular Peripheral Interface I/O Port ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B). Two interrupt flag bits are used with each Interrupt Request line. When true, these flag bits cause the Interrupt Request line to go low. The flag bits (bits 6 and 7 in each of the two Control Registers) act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the microprocessor to enable or disable the interrupts from each of the four interrupt inputs, i.e., CA1, CA2, CB1 and CB2. Each interrupt flag is set by an active transition on the interrupt input (CA1, CA2, CB1 and CB2).

Interrupt A Control ($\overline{IRQA}$)

Bit 7 of Control Register A is always set by an active transition of the CA1 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 0 of Control Register A to a Logic 0. Bit 6 of Control Register A is always set by an active transition of the CA2 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 3 of Control Register A to a Logic 0.

Both bit 6 and bit 7 in Control Register A are reset by a "Read Peripheral Output Register A" operation. To perform this Read operation, the proper Chip Select and appropriate Register Select signals must be present.

Interrupt B Control ($\overline{IRQB}$)

The control of Interrupt Request B ($\overline{IRQB}$) is performed in the same manner as that described above for $\overline{IRQA}$, except that for I/O Port B, Control Register bit 7 is set by an active transition on CB1 and interrupt enable/disable is controlled by Control Register bit 0. Control Register bit 6 is set by CB2 and its enable/disable is controlled by Control Register bit 3. Here again, both bit 6 and bit 7 in Control Register B are reset by a "Read Peripheral Output Register B" operation. Note that the interrupt disable bits (CRB bits 0 and 3) allow the microprocessor to control the interrupt function.

Interrupt Control Summary

$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1

Peripheral I/O Ports

The G65SC21 provides two 8-bit bidirectional Data Ports (PA and PB) and four interrupt/control lines (CA1, CA2, CB1 and CB2) for interfacing to peripheral devices. Peripheral I/O Port A and I/O Port B allow the microprocessor to interface the peripheral device input lines by loading data into the corresponding Peripheral Output Register. The microprocessor interfaces the peripheral device output lines by reading data on the I/O Port input lines directly onto the Data Bus and into the internal registers of the microprocessor.

Peripheral I/O Port A (PA0-PA7)

Each Peripheral I/O Port line can be programmed to act as an input or an output, as determined by the corresponding bits in the Data Direction Register. Within the Data Direction Register, a Logic 1 in a particular bit position represents an output line. Likewise, a Logic 0 in a particular bit position represents an input line. The Data Buffers which drive the I/O Port A lines contain "active" pull-up transistors as shown in Figure 14. Since these pull-ups are p-channel transistors they allow the output voltage to go to V_{DD} for a Logic 1. Also, since these switches can sink a full 3.2 milliamp, the buffers are capable of driving one standard TTL load. In the input mode, the pull-up devices shown in Figure 14 remain connected to the I/O pin and continue to supply current to the pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral I/O Port B (PB0-PB7)

The lines of Peripheral I/O Port B function in a similar manner to the discussion of I/O Port A above. Programmed selection for input/output function is identical. There are, however, several characteristics of the buffers driving these lines which affect their use in peripheral interfacing. Peripheral I/O Port B buffers are push-pull devices as shown in Figure 15.

The active pull-up devices can source up to 3 milliamp at 1.5 volts. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows

convenient control of relays, lamps, etc. Because the I/O Port B outputs are designed to drive transistors directly, the output data is read directly from Peripheral Output Register B for those lines programmed as inputs. The I/O Port B push-pull buffers also provide a high impedance input state. When these lines are programmed as inputs, the output buffer enters the high impedance state.

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1 and CB2)

The G65SC21 contains four interrupt input/peripheral control lines (CA1, CA2, CB1 and CB2) which offer a number of special peripheral control functions. These functions greatly enhance the performance of the two I/O Ports. Refer to Figure 16 for a summary of control line operation.

I/O Port A Interrupt Input/Peripheral Control Lines (CA1, CA2)

Line CA1 is an interrupt input only. An active transition on this line will set bit 7 in Control Register A to a Logic 1. This flag bit (bit 7) can be programmed to set on either a positive or negative CA1 transition. Bit 7 will be set on a negative transition if bit 1 in the Control Register is set to a Logic 0. Likewise, bit 7 can be set on a positive transition if bit 1 in the Control Register is set to a Logic 1.

It should be noted that a negative transition is defined as a transition from high to low, and a positive transition is a transition from low to high.

Setting the interrupt flag (bit 7 or the Control Register) will interrupt the microprocessor via $\overline{IRQA}$ if bit 0 in Control Register A is a Logic 1 as described in earlier paragraphs.

Line CA2 can act as a totally independent interrupt input or as a peripheral control output. CA2 acts as an interrupt input when Control Register A bit 5 is a Logic 0. In this case, CA2 will set the interrupt flag (bit 6 of Control Register A) to a Logic 1 on the active transition as selected by bit 4 of the Control Register. The Control Register bits and interrupt inputs serve the same basic function as that described above for CA1. The input transition sets the interrupt flag which serves as the link between the microprocessor interrupt configuration and the peripheral device. The interrupt disable bit allows the microprocessor to exercise control over the system interrupts.

CA2 serves in the output control mode when Control Register A bit 5 is a Logic 1. In this case, CA2 can operate independently to generate a sample pulse each time the microprocessor reads data on I/O Port A. This mode is selected by setting bit 4 of the Control Register to a Logic 0 and bit 3 to a Logic 1. This pulse output is normally used to control counters, shift registers, etc. which provide sequential data to the peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the peripheral device and the microprocessor. With respect to I/O Port A, this "handshake" allows positive control of data transfers from the peripheral device into the microprocessor. The "handshake" function operates as follows:

The CA1 input signals the microprocessor that data is available by interrupting the microprocessor. The microprocessor then reads the data and sets CA2 to a Logic 0. This signals the peripheral device that it can now place new data on the I/O Port line.

A third output mode can be selected by setting Control Register bit 4 to a Logic 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of Control Register A to a Logic 1 or a Logic 0 respectively.

I/O Port B Interrupt Input/Peripheral Control Lines (CB1, CB2)

The CB1 line operates as an interrupt input only in the same manner as CA1 above. In this case, bit 7 of Control Register B is set by the active transition on CB1 as selected by bit 0 of the Control Register. The CB2 input modes operate identical to the CA2 input modes. However, the CB2 output modes (Control Register B bit 5 set to Logic 1) differ somewhat from those of CA2. That is, the pulse ouput occurs when the microprocessor writes data into Output Register B. Also, the "handshaking" operates on data transfers from the microprocessor into the peripheral device.

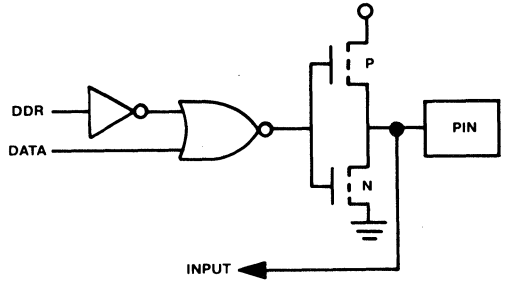


Figure 14. Port A Buffer Circuit (PA0-PA7)

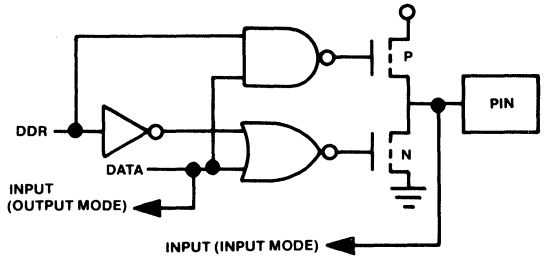


Figure 15. Port B Buffer Circuit (PB0-PB7)

CA1/CB1 CONTROL			
CRA (CRB) BIT 1	CRA (CRB) BIT 0	ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
0	0	Negative	Disable—remain high
0	1	Negative	Enable—goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable—remain high
1	1	Positive	Enable—as explained above

*Note: Bit 7 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES				
CRA (CRB) BIT 5	CRA (CRB) BIT 4	CRA (CRB) BIT 3	ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
0	0	0	Negative	Disable—remains high
0	0	1	Negative	Enable—goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable—remains high
0	1	1	Positive	Enable—as explained above

*Note: Bit 6 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2 OUTPUT MODES				
CRA BIT 5	CRA BIT 4	CRA BIT 3	MODE	DESCRIPTION
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES				
CRB BIT 5	CRB BIT 4	CRB BIT 3	MODE	DESCRIPTION
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

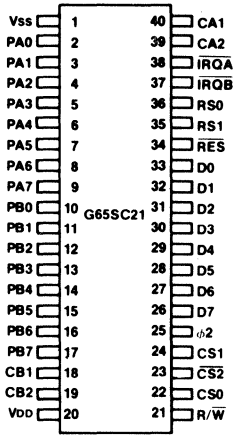
Figure 16. Interrupt Input/Peripheral Control Lines Operation

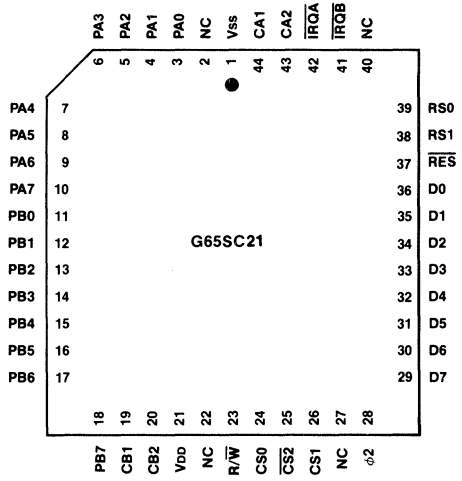
Pin Function Table

Pin	Description
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQA}$	Interrupt Request (Port A)

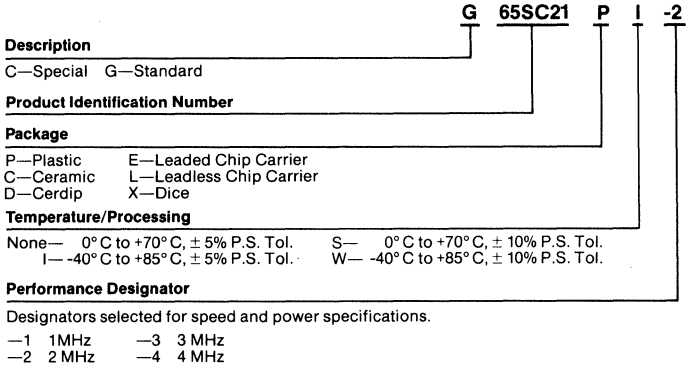
Pin	Description
$\overline{IRQB}$	Interrupt Request (Port B)
CS0, CS1, $\overline{CS2}$	Chip Select Inputs
RS0, RS1	Register Selects
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
VDD	Positive Power Supply (+5V)
VSS	Internal Logic Ground

Pin Configuration





Ordering Information



G65SC22

Microcircuits

CMOS Versatile Interface Adapter With Interval Timer/Counters

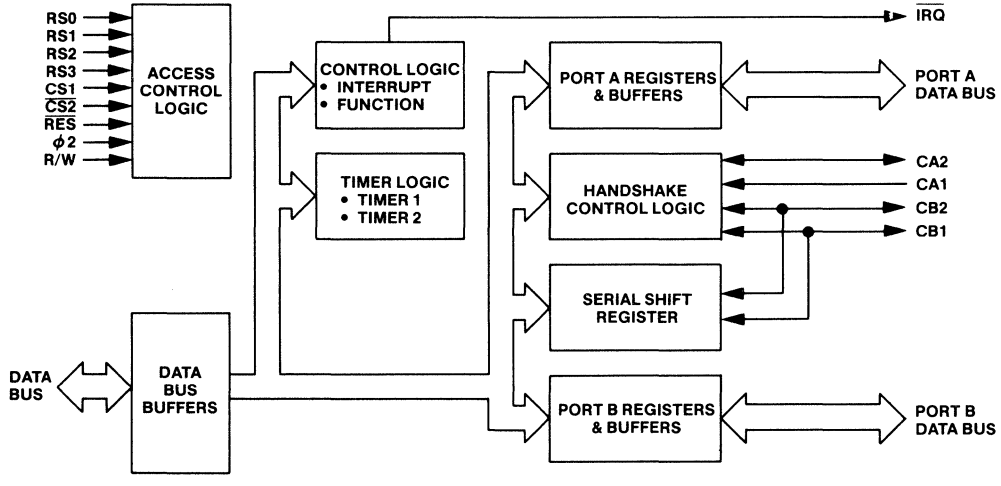
Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6522 devices
- Low power consumption allows battery-powered operation (2 mA at 1 MHz)
- Two 8-bit, bidirectional peripheral I/O Ports
- Two powerful 16-bit programmable Interval Timer/Counters
- Serial bidirectional peripheral I/O Port
- Enhanced "handshake" feature
- Latched Input/Output Registers on both I/O Ports
- Programmable Data Direction Registers
- Four operating frequencies—1, 2, 3 and 4 MHz
- TTL compatible I/O peripheral lines
- Single +5 volts power supply
- Available in 40-pin dual-in-line or 44-pin PLCC package

General Description

The GTE G65SC22 Versatile Interface Adapter (VIA) is a flexible I/O device for use with the GTE G65SCXXX series 8-bit microprocessor family. The G65SC22 includes functions for programmed control of up to two peripheral devices (Ports A and B). Two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis. Also provided are two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—an Interrupt Flag Register, an Interrupt Enable Register and two Function Control Registers.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0-RS3, CS1, $\overline{CS2}$, CA1, ϕ2	I_{IN}		±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IL}		-1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz	I_{DD}		2.0	mA
f = 2 MHz	I_{DD}		4.0	mA
f = 3 MHz	I_{DD}		6.0	mA
f = 4 MHz	I_{DD}		8.0	mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz)	P_D		11.0	mW
Standby (Static)	P_{DSB}		100	μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

		G65SC22-1		G65SC22-2		G65SC22-3		G65SC22-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 2)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS
Write Timing (Figure 3)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay (Port A)	t_{CPW}	—	1000	—	500	—	330	—	320	nS
(Port B)		—	1000	—	500	—	330	—	250	nS

AC Characteristics—Peripheral Interface Timing: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial.

(See Figures 4 through 12)

Parameter	Symbol	Min	Max	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	t_R, t_F	—	1.0	μS	—
Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)	t_{CA2}	—	1.0	μS	4,5
Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)	t_{RS1}	—	1.0	μS	4
Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)	t_{RS2}	—	2.0	μS	5
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	t_{WHS}		1.0	μS	6,7
Delay Time, Peripheral Data Valid to CA2 or CB2 Negative Transition	t_{DS}	40	—	nS	6,7
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)	t_{RS3}	—	1.0	μS	6
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)	t_{RS4}	—	2.0	μS	7
Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	t_{21}	400	—	nS	7
Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	t_{IL}	300	—	nS	8
Shift-Out Delay Time—Time from $\phi 2$ Falling Edge to CB2 Data Out	t_{SR1}	—	300	nS	9
Shift-In Set-up Time—Time from CB2 Data In to $\phi 2$ Rising Edge	t_{SR2}	300	—	nS	10
External Shift Clock (CB1) Set-up Time Relative to $\phi 2$ Trailing Edge	t_{SR3}	100	t_{CYC}	nS	10
Pulse Width—PB6 Input Pulse	t_{IPW}	2 x t_{CYC}	—		12
Pulse Width—CB1 Input Clock	t_{ICW}	2 x t_{CYC}	—		11
Pulse Spacing—PB6 Input Pulse	t_{IPS}	2 x t_{CYC}	—		12
Pulse Spacing—CB1 Input Pulse	t_{ICS}	2 x t_{CYC}	—		11
CA1, CB1 Set Up Prior to Transition to Arm Latch	t_{AL}	300	—	nS	8
Peripheral Data Hold After CA1, CB1 Transition	t_{PDH}	150	—	nS	8

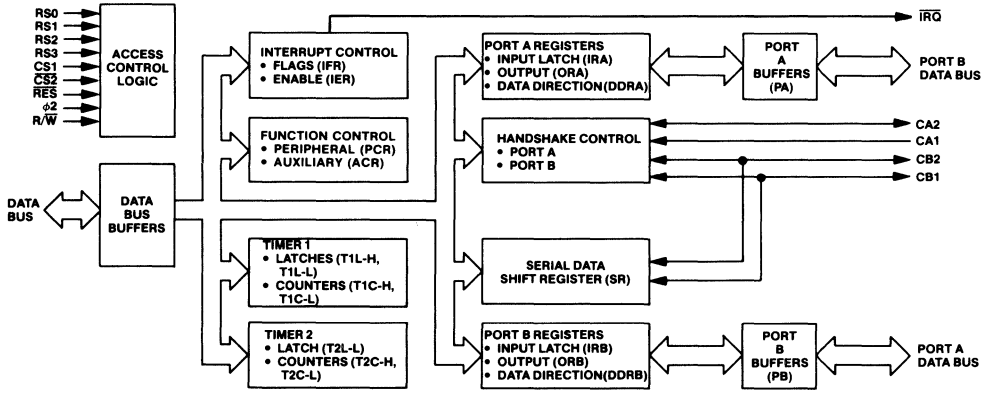


Figure 1. Functional Block Diagram

Timing Diagrams: Measurement points 0.8.V and 2.0V unless otherwise specified.

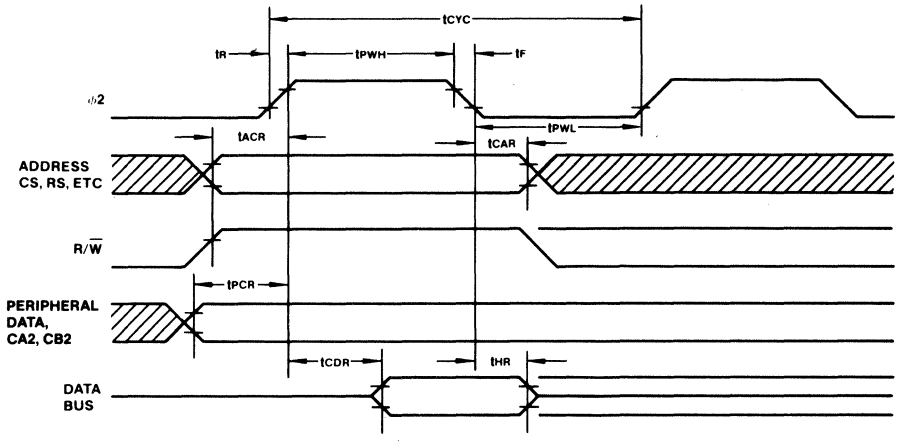


Figure 2. Read Timing

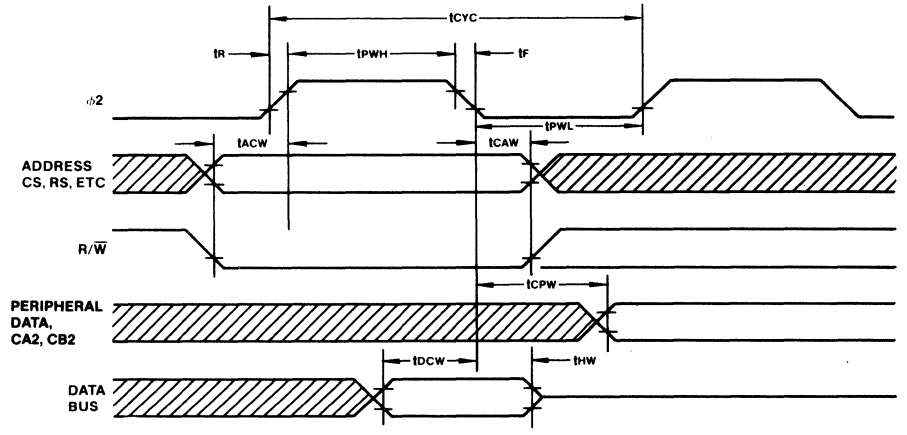


Figure 3. Write Timing

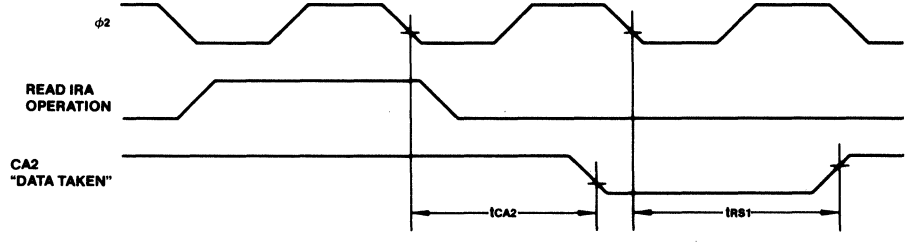


Figure 4. Read Handshake, Pulse Mode Timing (CA2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

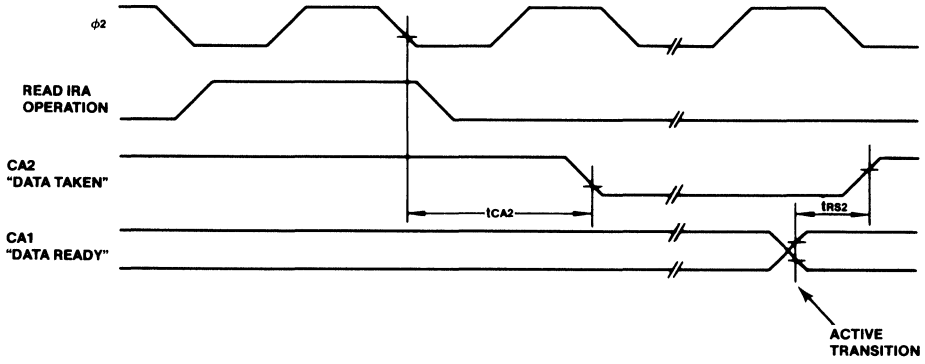


Figure 5. Read Handshake, Handshake Mode Timing (CA2)

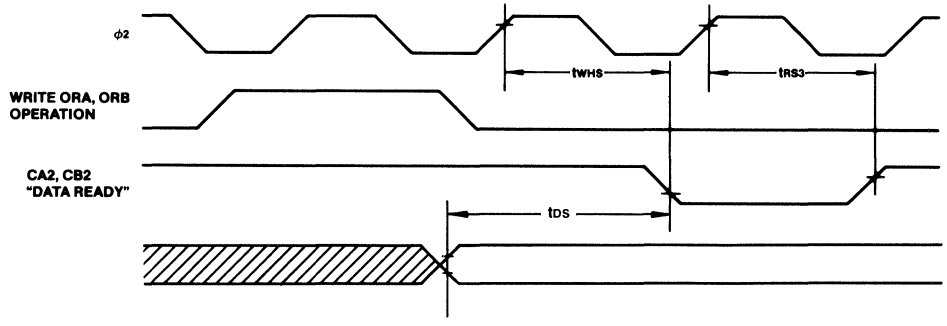


Figure 6. Write Handshake, Pulse Mode Timing (CA2, CB2)

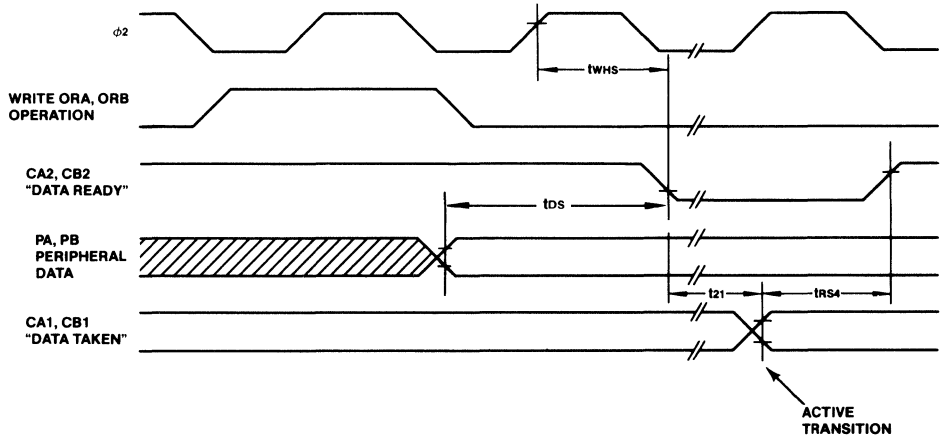


Figure 7. Write Handshake, Handshake Mode Timing (CA2, CB2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

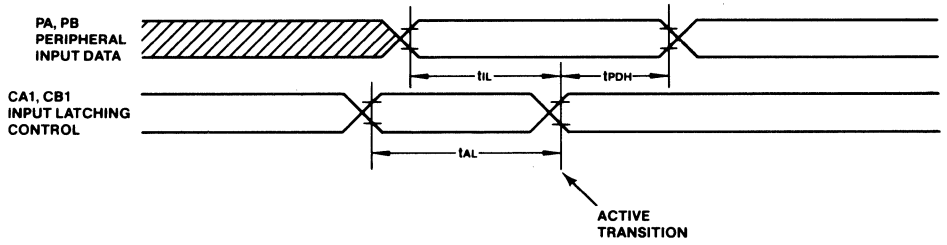


Figure 8. Peripheral Data, Input Latching Timing

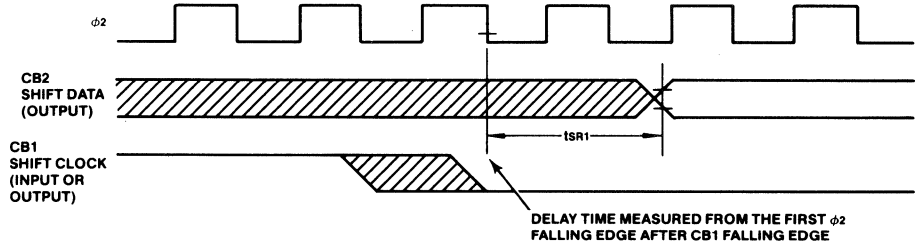


Figure 9. Data Shift Out, Internal or External Shift Clock Timing

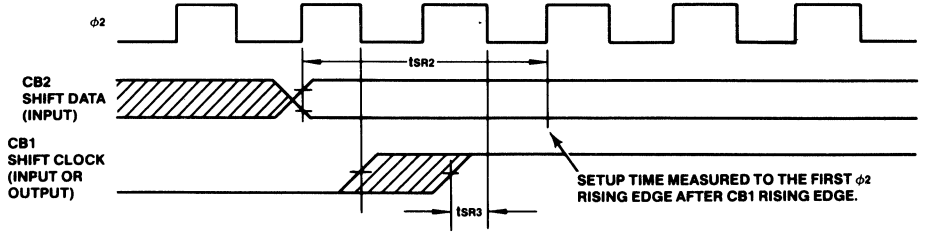


Figure 10. Data Shift In, Internal or External Shift Clock Timing

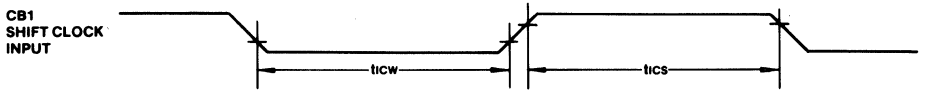


Figure 11. External Shift Clock Timing

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

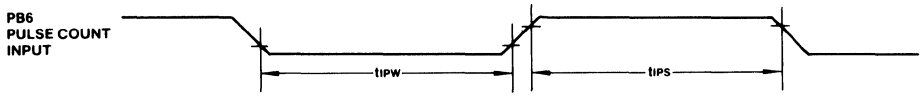


Figure 12. Pulse Count Input Timing

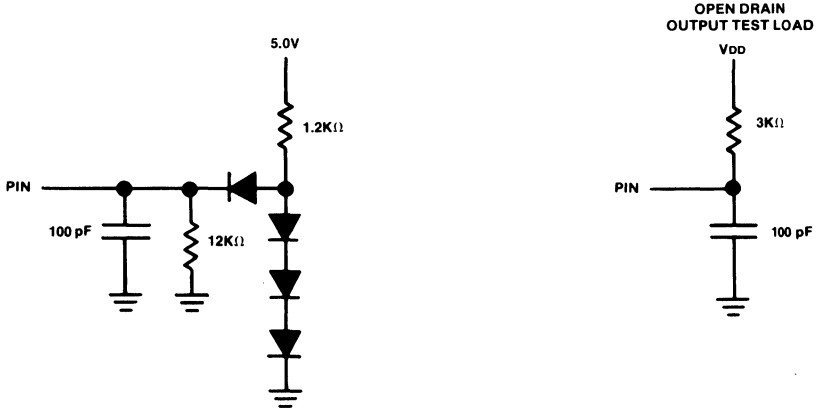


Figure 13. Test Load

Signal Description

Reset ($\overline{RES}$)
Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

Input Clock (ϕ2)
The system ϕ2 Input Clock controls all data transfers between the G65SC22 and the microprocessor.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the G65SC22 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC22 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC22 register (Write operation). Read/Write must always be preceded by a proper Chip Select (CS1, $\overline{CS2}$).

Data Bus (D0-D7)
The eight bidirectional Data Bus lines are used to transfer data between the G65SC22 and the microprocessor. During a Read operation, the contents of the selected G65SC22 internal register are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected G65SC22 register. The Data Bus lines are in the high impedance state when the G65SC22 is unselected.

Chip Select (CS1, $\overline{CS2}$)
Normally, the two Chip Select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected G65SC22 register, CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0-RS3)
The Register Select inputs allow the microprocessor to select one of 16 internal registers within the G65SC22. Refer to Table 1 for Register Select coding and a functional description.

Interrupt Request ($\overline{IRQ}$)
The Interrupt Request ($\overline{IRQ}$) output signal is generated (Logic 0) whenever an internal Interrupt Flag bit is set (Logic 1) and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Table 1. G65SC22 Internal Registers

Register Number	RS Coding				Register Designation	Description	
	RS3	RS2	RS1	RS0		Write ($R/\overline{W}$ = 0)	Read ($R/\overline{W}$ = 1)
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same As Reg 1 Except No "Handshake"	

Peripheral Data Port A (PA0-PA7)

Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the G65SC22's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 14.

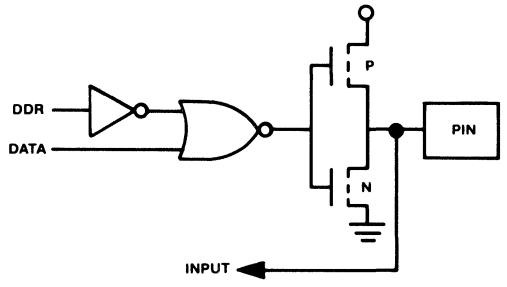


Figure 14. Port A Buffer Circuit (PA0-PA7, CA2)

Peripheral Data Port A Control Lines (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

Peripheral Data Port B (PB0-PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 3.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 15.

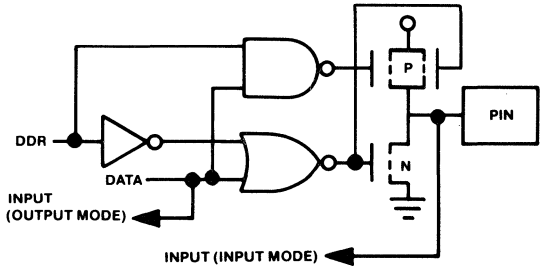


Figure 15. Port B Buffer Circuit (PB0-PB7, CB1, CB2)

Peripheral Data Port B Control Lines (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.

Functional Description

Peripheral Data Ports (Port A, Port B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA & ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) is transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates similar to Input Register A except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of Input Register A to result in the reading of a Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 16, 17 and 18. It should be noted that the input latching modes are controlled by the Auxiliary Control Register (See Figure 24).

Data Transfer—Handshake Control

A powerful feature of the G65SC22 is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

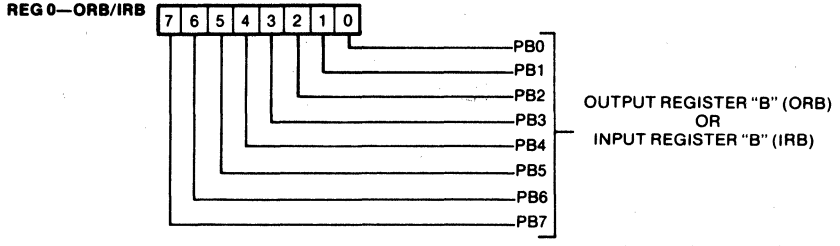
Read Handshake Control

Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the G65SC22 which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figure 19 for Read Handshake timing and operating sequence.

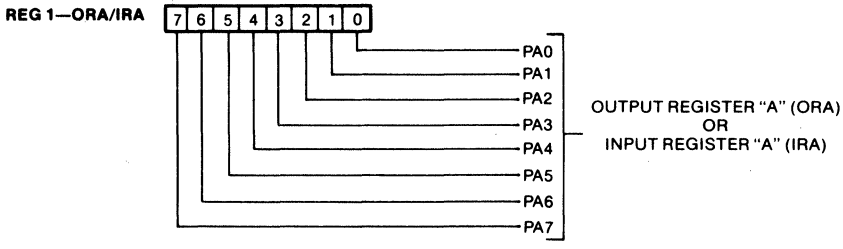
Write Handshake Control

The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the G65SC22 generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Refer to Figure 20 for Write Handshake timing and operating sequence. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1 and CB2) is accomplished by the Peripheral Control Register (PCR). See Figure 21.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 16. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 17. Output Register A (ORA), Input Register A (IRA)

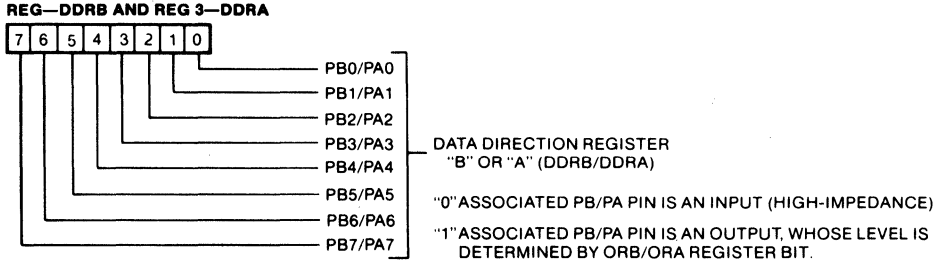


Figure 18. Data Direction Registers (DDRB, DDRA)

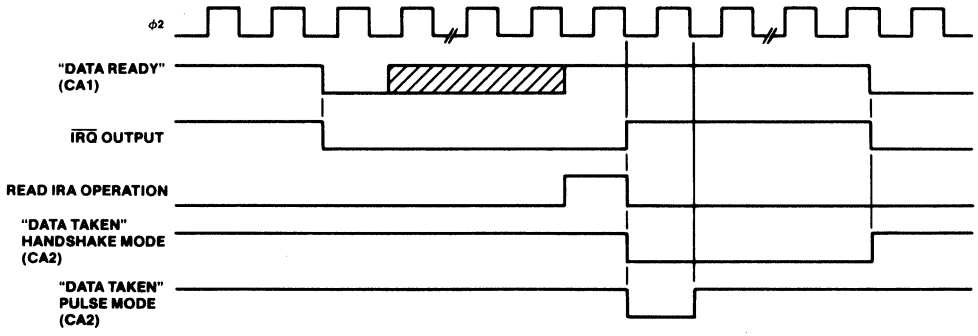


Figure 19. Read Handshake (Port A Only)

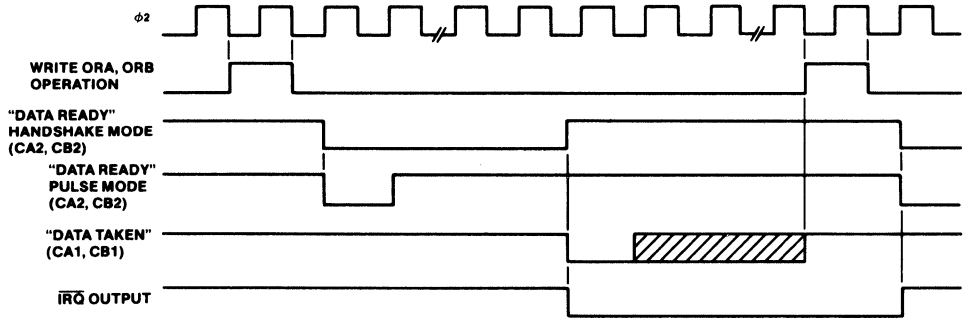


Figure 20. Write Handshake (Ports A and B)

REG 12—PERIPHERAL CONTROL REGISTER

7	6	5	4	3	2	1	0

CB2 CONTROL

7	6	5	Operation
0	0	0	Input-negative active edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

CB1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA2 CONTROL

3	2	1	Operation
0	0	0	Input-negative active edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

*See Note Accompanying Figure 37.

Figure 21. CA1, CA2, CB1, CB2 Control

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 ($\phi 2$) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request ($\overline{IRQ}$) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may also be programmed to invert the output signal on PB7 each time it reaches a count of zero. Each of these counter modes is presented below. The T1 counter format and operation is shown in Figure 22, with corresponding latch format and operation in Figure 23. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer T1 operating modes. The four available modes are shown in Figure 24.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode

Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port line PB7.

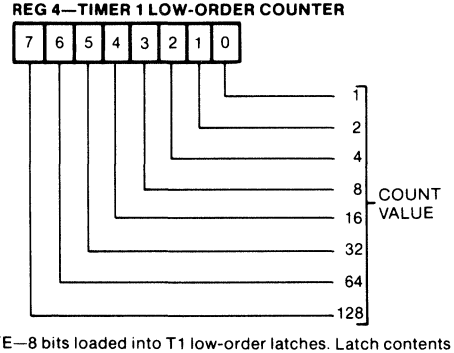
To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next $\phi 2$ clock following the load sequence into T1C-H, and will decrement at the $\phi 2$ clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count.

Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L. Refer to Figure 25 for One-Shot Mode timing information.

Timer 1 Free-Run Mode

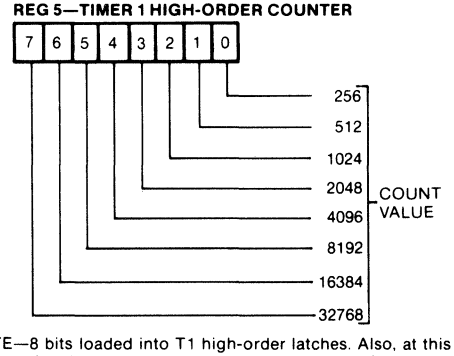
An important advantage within the G65SC22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers to contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated. Refer to Figure 26 for timing information on the Free-Run Mode.



WRITE—8 bits loaded into T1 low-order latches. Latch contents are transferred into low-order counter at the time the high-order counter is loaded (Reg. 5).

READ—8 bits from T1 low-order counter transferred to MPU. In addition, T1 interrupt flag is reset (bit 6 in interrupt flag register).

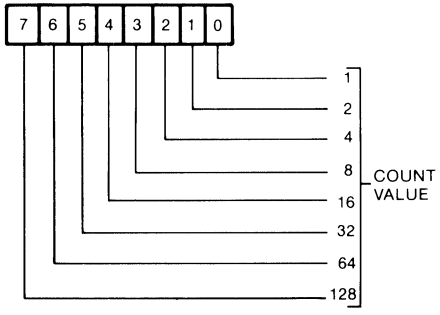


WRITE—8 bits loaded into T1 high-order latches. Also, at this time both high and low-order latches transferred into T1 counter, and initiates countdown. T1 interrupt flag also is reset.

READ—8 bits from T1 high-order counter transferred to MPU.

Figure 22. T1 Counter Format and Operation

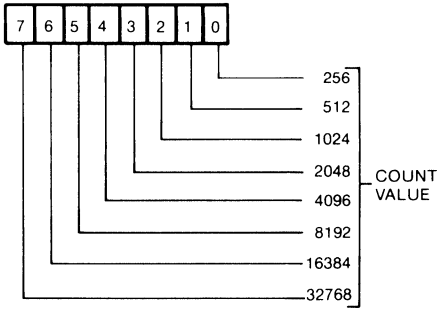
REG 6—TIMER 1 LOW-ORDER LATCHES



WRITE—8 bits loaded into T1 low-order latches. This operation is no different than a write into Reg. 4.

READ—8 bits from T1 low-order latches transferred to MPU. Unlike Reg. 4 operation, this does not cause reset of T1 interrupt flag.

REG 7—TIMER 1 HIGH-ORDER LATCHES

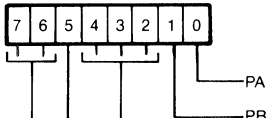


WRITE—8 bits loaded into T1 high-order latches. Unlike Reg. 4 operation no latch-to-counter transfers take place.

READ—8 bits from T1 high-order latches transferred to MPU.

Figure 23. T1 Latch Format and Operation

REG 11—AUXILIARY CONTROL REGISTER



T1 TIMER CONTROL

7	6	Operation	PB7
0	0	Timed interrupt each time T1 is loaded	Disabled
0	1	Continuous interrupts	
1	0	Timed interrupt each time T1 is loaded	One shot output
1	1	Continuous interrupts	Square wave output

T2 TIMER CONTROL

5	Operation
0	Timed interrupt
1	Count down with pulses on PB6

LATCH ENABLE/DISABLE

0 = Disable
1 = Enable Latching

SHIFT REGISTER CONTROL

4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk.
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk.

Figure 24. Auxiliary Control Register Format and Operation

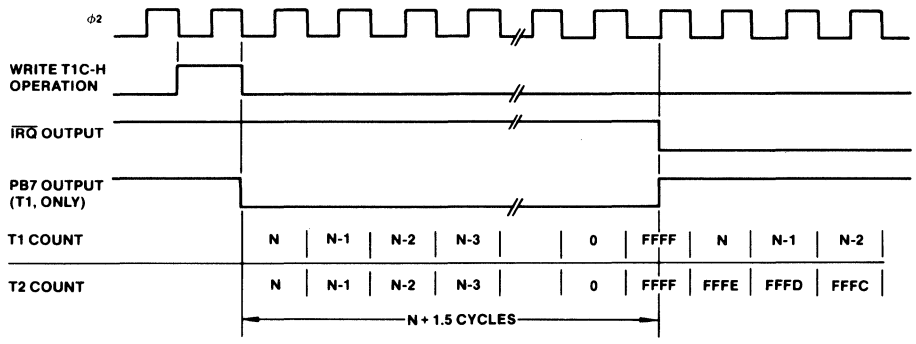
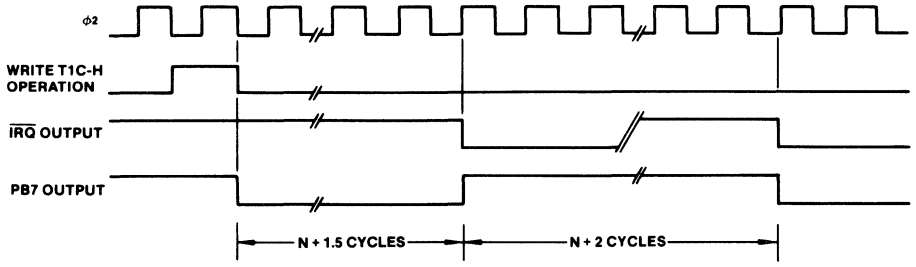


Figure 25. One-Shot Mode (Timer 1 and Timer 2)



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 26. Free-Run Mode (Timer 1)

Timer 2 Operation

Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for counting negative pulses on Data Port line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a $\phi 2$ clock rate. Refer to Figure 27 for T2 counter format and operation.

Timer 2 One-Shot Mode

Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1s ($FFFF_{16}$) and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H. Refer to Figure 25 for timing information on the One-Shot Mode.

Timer 2 Pulse Counting Mode

In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the $\phi 2$ clock. Refer to Figure 28 for timing information.

Shift Register Operation

The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line from an external source, or (with proper mode selection) shift pulses may be generated internally which will appear on the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register. Refer to Figure 29 for format and control bit information. Also refer to Figures 30 through 36 for operation of the various Shift Register modes.

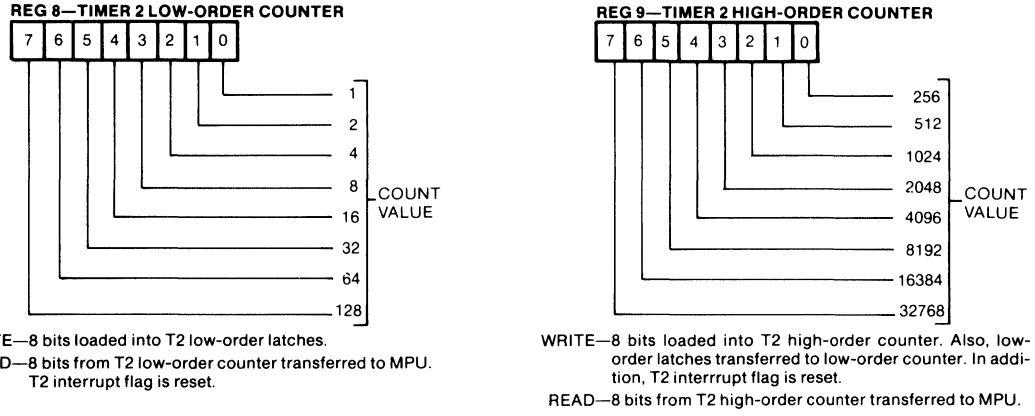


Figure 27. T2 Counter Format and Operation

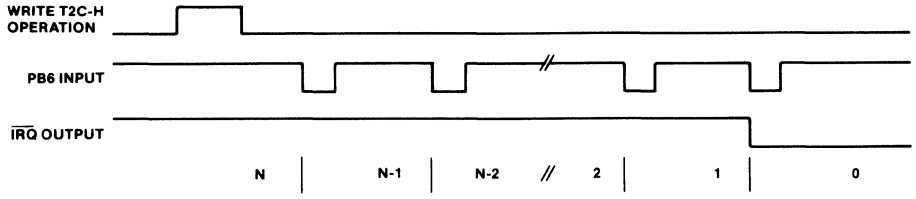


Figure 28. Pulse Counting Mode (Timer 2)

Shift Register Input Modes

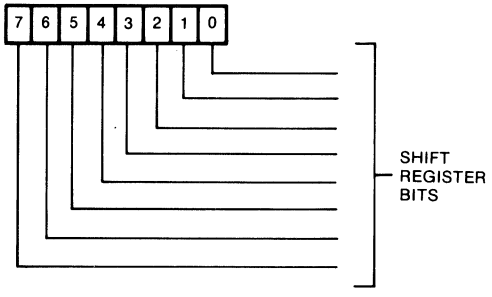
Shift Register Disabled (000)—In the 000 mode, the Shift Register is disabled from all operation. The microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In—Counter T2 Control (001)—In this mode, the shifting rate is controlled by the low order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the $\phi 2$ clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set and $\overline{IRQ}$ will go low (Logic 0). Refer to Figure 30.

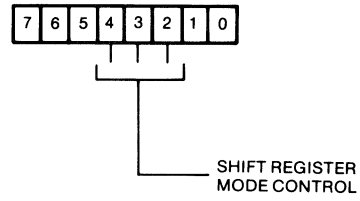
Shift In—$\phi 2$ Clock Control (010)—In this mode, the shift rate is controlled by the $\phi 2$ clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low order bit first, and is then shifted into the next higher order bit on the trailing edge of the $\phi 2$ clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set, and output clock pulses on the CB1 line will stop. Refer to Figure 31.

Shift In—External CB1 Clock Control (011)—In this mode, CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first $\phi 2$ clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Refer to Figure 32.

REG 10—SHIFT REGISTER



REG 11—AUXILIARY CONTROL REGISTER



4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk.

Notes:
1. When shifting out, bit 7 is the first bit out and simultaneously is rotated back into bit 0.
2. When shifting in, bits initially enter bit 0 and are shifted towards bit 7.

Figure 29. Shift Register and Auxiliary Control Register Control Bits

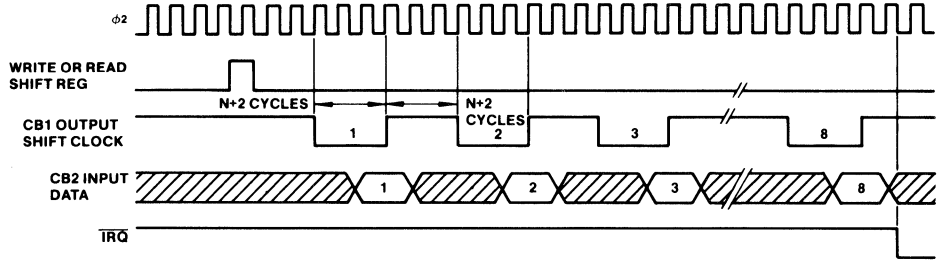


Figure 30. Shift In—Counter T2 Control

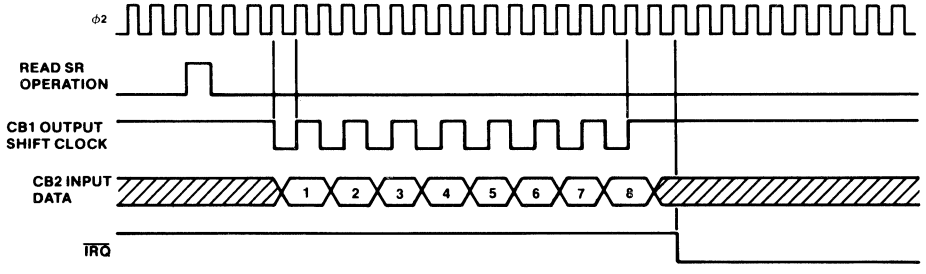


Figure 31. Shift In—$\phi 2$ Clock Control

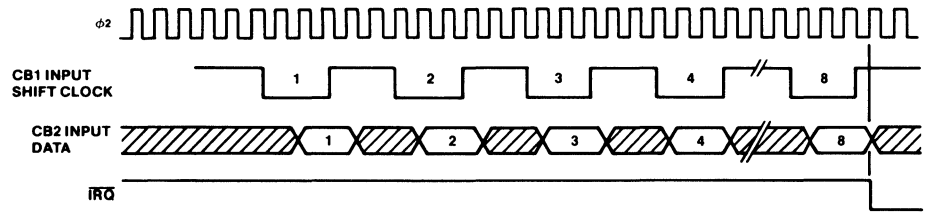


Figure 32. Shift In—External CB1 Clock Control

Shift Register Output Modes

Shift Out—Free Running at T2 Rate (100)—This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CB2 line repetitively. In this mode, the Shift Register Counter is disabled and $\overline{IRQ}$ is never set. Refer to Figure 33.

Shift Out—T2 Control (101)—In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level. Refer to Figure 34.

Shift Out—Φ2 Clock Control (110)—In this mode, the shift rate is controlled by the system Φ2 Clock. Refer to Figure 35.

Shift Out—External CB1 Clock Control (111)—In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data. Refer to Figure 36.

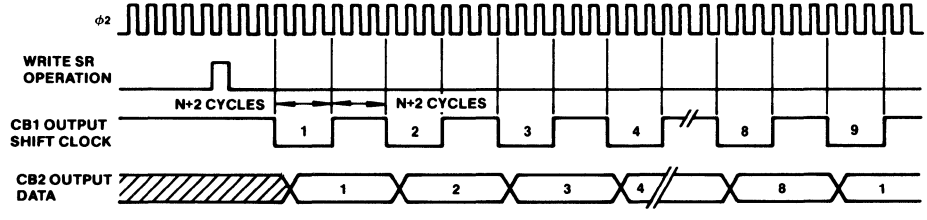


Figure 33. Shift Out—Free Running T2 Rate

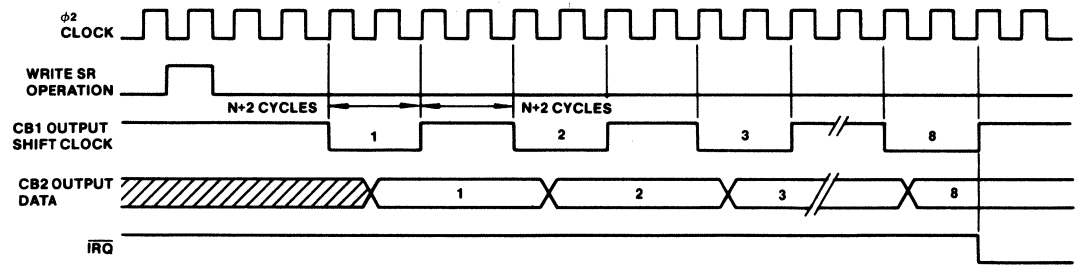


Figure 34. Shift Out—T2 Control

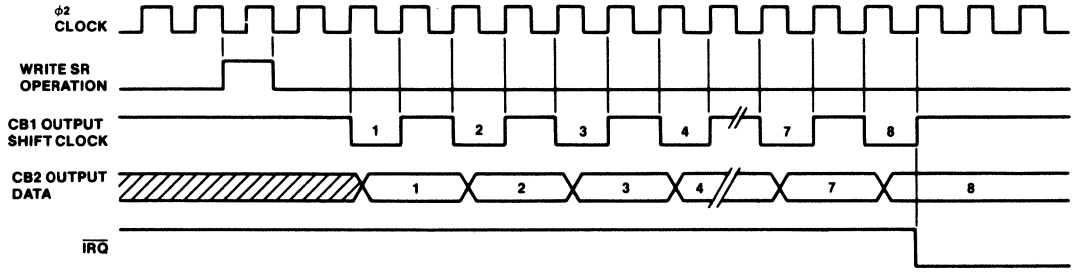


Figure 35. Shift Out—φ2 Control

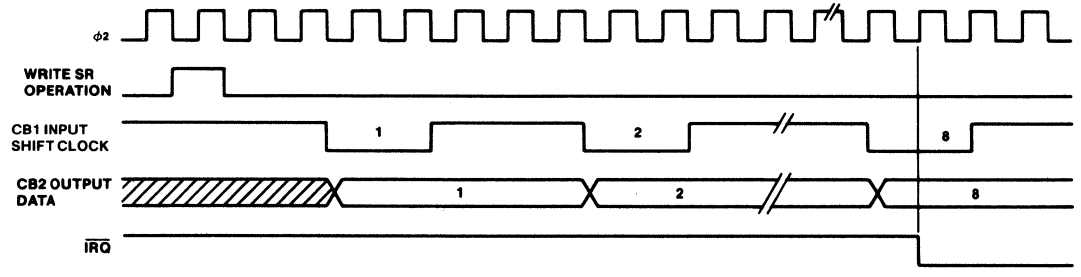


Figure 36. Shift Out—External CB1 Clock Control

Interrupt Operation

There are three basic interrupt operations, including: setting the interrupt flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request ($\overline{IRQ}$). An Interrupt Flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag will remain set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request ($\overline{IRQ}$) will go low (Logic 0). $\overline{IRQ}$ is an open-collector output which can be wire-ORed with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

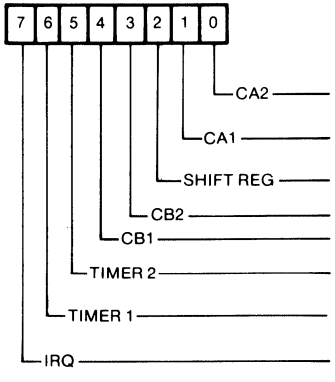
The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 37 and 38 respectively. The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request ($\overline{IRQ}$) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: x = Logic AND, + = Logic OR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts as presented in the next section.

Each Interrupt Flag within the IFR has a corresponding enable bit in the Interrupt Enable Register (IER). The microprocessor can set or clear selected bits within the IER. This allows the control of individual interrupts without affecting others. To set or clear a particular Interrupt Enable bit, the microprocessor must write to address 1110 (IER address). During this write operation, if bit 7 on the Data Bus is a "0", each "1" in bits 6 thru 0 will clear the corresponding bit in the Interrupt Enable Register. For each "0" in bits 6 thru 0, the corresponding bit in the IER will be unaffected.

Setting selected bits in the IER is accomplished by writing to the same address with bit 7 on the Data Bus set to a "1". In this case, each "1" in bits 6 thru 0 will set the corresponding bit to a "1". For each "0", the corresponding bit will be unaffected. This method of controlling the bits in the Interrupt Enable Register allows convenient user control of interrupts during system operation. The microprocessor can also read the contents of the IER by placing the proper address on the Register Select and Chip Select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a "1".

REG 13—INTERRUPT FLAG REGISTER

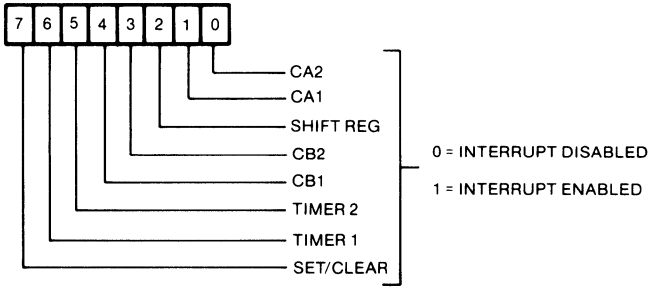


	SET BY	CLEARED BY
CA2	CA2 active edge	Read or write Reg. 1 (ORA)*
CA1	CA1 active edge	Read or write Reg. 1 (ORA)
SHIFT REG	Complete 8 shifts	Read or write Shift Reg.
CB2	CB2 active edge	Read or write ORB*
CB1	CB1 active edge	Read or write ORB
TIMER 2	Time-out of T2	Read T2 low or write T2 high
TIMER 1	Time-out of T1	Read T1 low or write T1 high
IRQ	Any enabled interrupt	Clear all interrupts

*If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

Figure 37. Interrupt Flag Register (IFR)

REG 14—INTERRUPT ENABLE REGISTER



Notes:
1. If bit 7 is a "0", then each "1" in bits 0-6 disables the corresponding interrupt.
2. If bit 7 is a "1", then each "1" in bits 0-6 enables the corresponding interrupt.
3. If a read of this register is done, bit 7 will be "1" and all other bits will reflect their enable/disable state.

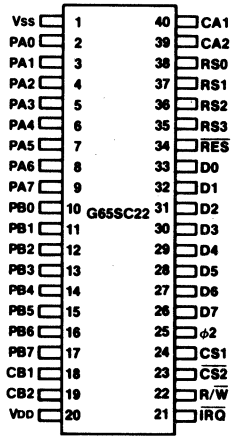
Figure 38. Interrupt Enable Register (IER)

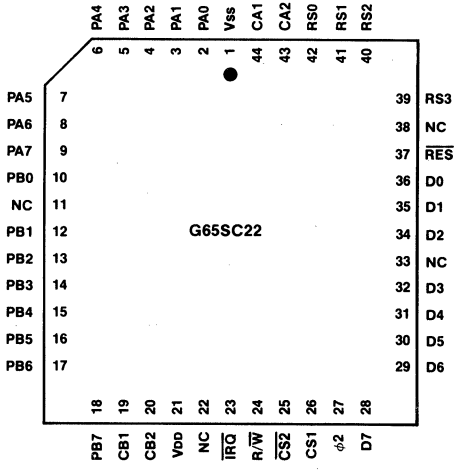
Pin Function Table

Pin	Description
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request

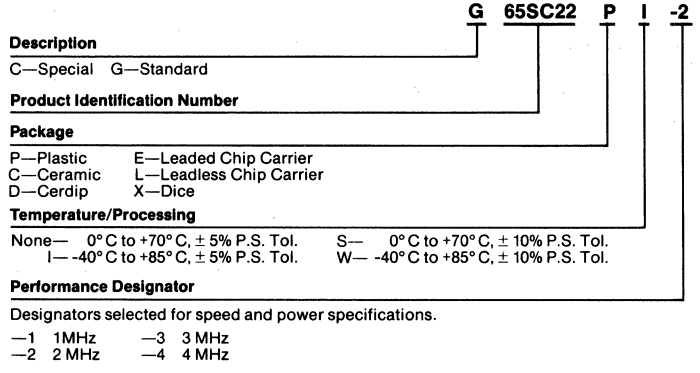
Pin	Description
CS1, $\overline{CS2}$	Chip Select
RS0-RS3	Register Select
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
VDD	Positive Power Supply (+5V)
VSS	Internal Logic Ground

Pin Configuration





Ordering Information



G65SC32

Microcircuits

CMOS RAM, I/O, Timer

Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6532 devices
- Bus compatible with 6500 and 6800 microprocessors
- Low power consumption (2 mA at 1 MHz)
- 128 X 8 bit static RAM
- Two 8-bit bidirectional peripheral data ports
- Two programmable Data Direction Registers
- Programmable Edge Sense Interrupt function
- Interrupt Timer with programmable interrupt intervals
- Peripheral I/O Port B allows direct transistor drive
- High impedance three-state Data Bus
- Available in 40-pin dual-in-line package or 44-pin PLCC

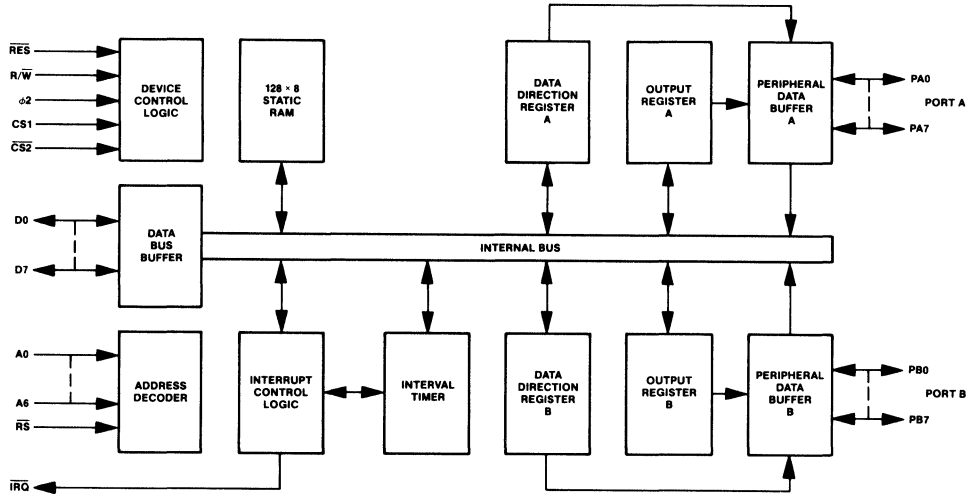
General Description

The G65SC32 is a programmable RAM, I/O, Timer device for use with the G65SCXXX series 8-bit microprocessor family. The G65SC32 includes functions for programmed control of up to two peripheral devices (Port A and Port B). These functions include:

- 128 X 8 bit static RAM for microprocessor scratch pad activity.
- Two program controlled 8-bit bidirectional Data Ports for direct interfacing between the microprocessor and selected peripheral units.
- Two programmable Data Direction Registers (A and B) for data direction control at each peripheral Data Port.
- A programmable Interrupt Timer with interrupt timing capability in intervals ranging from 1 to 262,144 clock periods.
- Edge-detect interrupt circuitry for interrupt generation on active edge transitions.

The G65SC32 offers the many advantages of GTE's leading edge CMOS technology, i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to V_{DD} + 0.3V
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these rating may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, A0-A6, ϕ2, CS1, $\overline{CS2}$, R/$\overline{W}$, $\overline{RES}$, $\overline{RS}$)	I_{IN}		±1.0	μA
Three-State, Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IL}		1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.25V, f = 1 MHz) Standby (Static)	P_D P_{DSB}		11.0 100	mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial

		G65SC32-1		G65SC32-2		G65SC32-3		G65SC32-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay (Port A) (Port B)	t_{CPW}	— —	1000 1000	— —	500 500	— —	330 330	— —	320 250	nS

Timing Diagrams

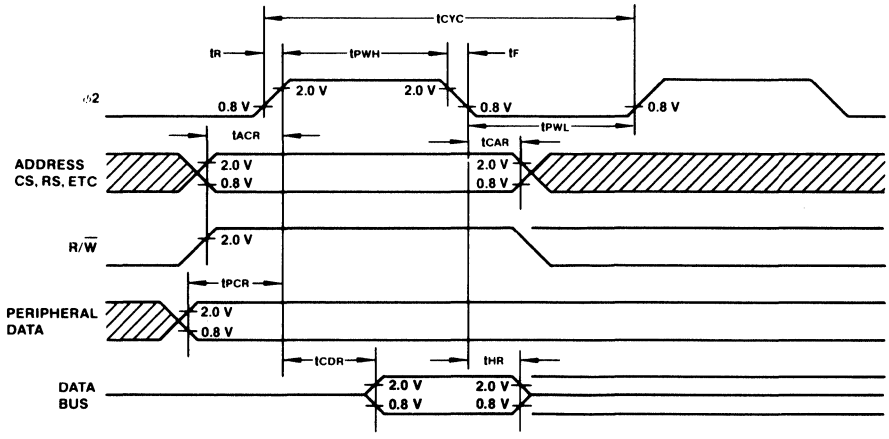


Figure 1. Read Timing

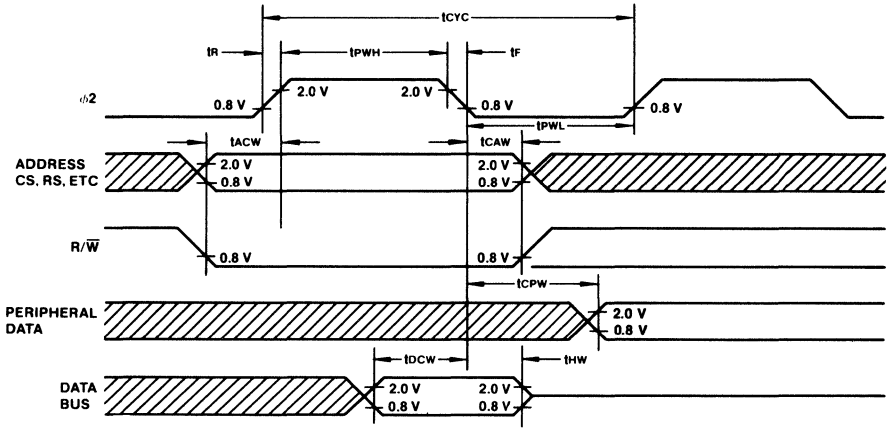
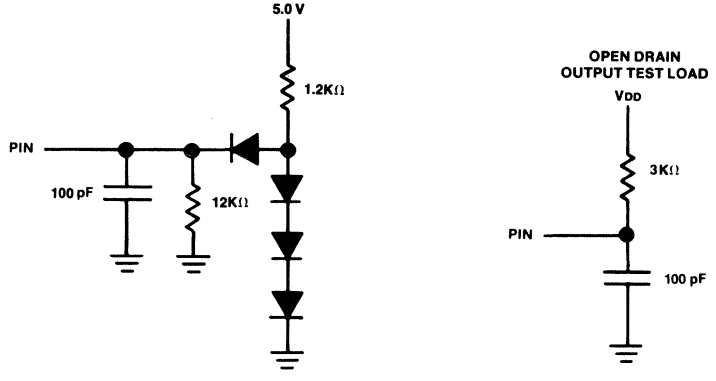


Figure 2. Write Timing

Test Load



Interface Signals

Input Clock ($\phi 2$)
The Input Clock consists of a system $\phi 2$ clock source. This clock can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{DD} + 0.3$ "or" $V_{DD} - 0.2$).

Reset ($\overline{RES}$)
During system initialization a Logic "0" on the $\overline{RES}$ input will cause all four I/O registers to be zeroed. This in turn will cause all lines within the I/O bus to serve as inputs. This arrangement protects external components from possible damage and/or erroneous data being written during system configuration under software control. Also, the Data Bus Buffers are placed in an Off-State during any $\overline{RES}$. Interrupt capability is disabled during $\overline{RES}$. The $\overline{RES}$ signal must be held low for a minimum of one clock period during a $\overline{RES}$ function.

Interrupt Request ($\overline{IRQ}$)
The $\overline{IRQ}$ output signal is derived from the Interrupt Control Logic, and is normally in the high state (Logic "1"). When in the low state (Logic "0"), $\overline{IRQ}$ indicates an interrupt exists within the G65SC32. This interrupt output may be activated (Logic "0") by a logical transition on line PA7 of peripheral I/O Bus A, or by timeout of the Interval Timer. Interrupt Request is an open-drain output, thus allowing several units to be wire-ORed to a common microprocessor $\overline{IRQ}$ input pin.

Data Bus (D0-D7)
The G65SC32 contains eight bidirectional data lines (D0-D7) for transfer of data to and from the microprocessor. The Data Buffer is active during a Read operation, and is held in the Off-State during all other operations.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data to and from the G65SC32. When R/$\overline{W}$ is in the high state (Logic "1"), the microprocessor is allowed to read data from the G65SC32. Conversely, when R/$\overline{W}$ is in the low state (Logic "0"), the microprocessor may write data to the G65SC32. Read/Write functions must always be preceded by proper addressing.

Peripheral Data Ports (PA0-PA7 and PB0-PB7)
The G65SC32 contains two 8-bit peripheral I/O Ports... Port A (lines PA0-PA7) and Port B (lines PB0-PB7). An important feature of the G65SC32 is that each peripheral port bus line is individually programmable as either an input or an output. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. This feature is accomplished by the Data Direction Registers. When a "0" is written to any bit position of the Data Direction Register (DDRA or DDRB), the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of DDRA or DDRB, the corresponding data line will serve as an output.

When an I/O Port line has been programmed as an input and its Output Register (ORA or ORB) is read by the microprocessor, the TTL level on the I/O Port line will be transferred to the Data Bus (D0-D7). When programmed as outputs, the I/O Port lines will reflect data as written by the microprocessor into the Output Registers. I/O Port line PA7 also serves an Edge Sense Interrupt function as described in the following sections.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)
Address lines A0-A6 serve to address the RAM, I/O Registers, Timer and Flag Register. CS1 and $\overline{CS2}$ are used to select (enable access to) the G65SC32.

Functional Description

In reference to the Block Diagram on page one, the G65SC32 is shown to consist of four basic functions; that is, RAM, I/O, Timer and Interrupt Control. RAM interfaces directly with the microprocessor by way of the Data Bus and Address Lines. The peripheral I/O functions consist of two 8-bit I/O Ports. Each port is supported by a Data Direction Register and an Output Register.

RAM (128 Bytes, 1024 Bits)
Within the G65SC32 is a 128 X 8 bit static RAM. This RAM is used as a scratch pad or special data buffer, and is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1 and $\overline{CS2}$.

Peripheral I/O Port Registers
The peripheral I/O Port Registers consist of two Data Direction Registers and two data Output Registers. The Data Direction Register (A and B) controls the direction of data into and out of the peripheral I/O Ports as described under the Peripheral Data Ports Section above. The voltage level on any I/O Port line which has been programmed as an output, is determined by the corresponding bit in the Output Register (ORA or ORB).

During a peripheral Read operation over I/O Port A, data is read directly from the I/O Port bus (PA0-PA7). During this Read operation, should a particular PA line be programmed as an output, data transferred into the microprocessor will be identical to the corresponding data in Output Register A providing that line loading is such that the line voltage is $\geq$ 2.4 volts for a Logic "1", and $\leq$ 0.4 volts for a Logic "0". Under severe loading conditions where these voltage limits cannot be guaranteed, the resulting Read operation may not match the contents of Output Register A.

The output buffer which services I/O Port B (PB0-PB7) is different from the buffers for I/O Port A. The buffers for Port B are push-pull devices capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To ensure valid data will be read during a peripheral Read operation, I/O Port B contains logic which allows the microprocessor to read the contents of Output Register B instead of reading directly from the Port B data bus.

Interval Timer
Figure 3 shows the three basic functions of the Interval Timer section. These functions include: a preliminary divide-down register, a programmable 8-bit register, and all necessary interrupt logic.

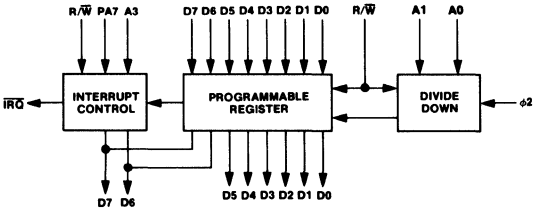


Figure 3. Basic Functions of Interval Timer

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be selected as 1T, 8T, 64T, or 1024T increments, where T is the system clock ($\phi 2$) period. When a full interval count has been reached, the interrupt flag is set to the Logic "1" state. Once the flag has been set, the internal clock starts counting down at a 1T rate to a maximum count of -255T. This arrangement allows the user to read the counter and thus determine the elapsed time since the interrupt was set.

The G65SC32's internal Data Bus is used to transfer data to and from the Interval Timer. For example, if a count of 52 time intervals is desired, the pattern 00110100 would be put on the Data Bus and written into the Interval Time Register. During the time when data is being written into the Interval Timer, timing intervals 1,8,64 and 1024T are decoded from address lines A0 and A1. During Read and Write operations, address line A3 controls the interrupt capability of $\overline{IRQ}$. That is, when A3=1, $\overline{IRQ}$ is enabled. When A3=0, $\overline{IRQ}$ is disabled. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read to or written from by the microprocessor. When $\overline{IRQ}$ is enabled by A3 and an interrupt occurs, $\overline{IRQ}$ will go low. Should the Timer be read prior to the interrupt flag being set, the number of remaining time intervals will be read, i.e., 51, 50, 49, etc.

Once the Timer has counted down to 00000000, an interrupt will occur on the next count time which will result in the Timer reading 11111111. Following the interrupt, the Timer registers decrements at a divide by "1" rate of the clock system. After interrupt, should the Timer read a value of 11100100, then the time since the last interrupt is 28T. The value read is in two's complement as follows:

Value read = 11100100
Complement = 00011011
Add 1 = 00011100 = 28T (28 $\phi 2$ clock periods)

Thus, to arrive at the total elapsed time since the Timer count was originally program set, simply perform a two's complement of the Timer value and add this to the original time value written into the Timer. For example, assume the original time written was 00110100 (=52). With a divide-by-8T, total time to interrupt would be (52 X 8) + 1 = 417T. In this case, total elapsed time would then be 416T + 28T = 444T, assuming the value read after interrupt was 11100100.

Following an interrupt, whenever the Timer is read or written the interrupt is reset. However, should the Timer be read at the same time the interrupt occurs, the interrupt flag will not reset. Figure 4 is an example of Timer Interrupt Timing.

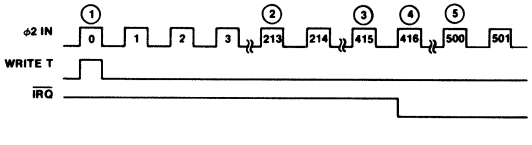


Figure 4. Timer Interrupt Timing

1. Data written into Interval Timers: 00110100 = 52_{10}
2. Data in Interval Timer: 000110100 = 25_{10}
   i.e., $52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$
3. Data in Interval Timer: 00000000 = 0_{10}
   i.e., $52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$
4. Interrupt occurred at $\phi 2$ clock pulse number 416
   Data in Interval Timer = 11111111
5. Data in Interval Timer: 10101100
   Two's complement: 01010100 = 84_{10}
   Therefore, 84 + (52 x 8) = 500_{10}

When reading the timer following an interrupt, address line A3 must be low such that $\overline{IRQ}$ will be disabled. This procedure prevents future interrupts until a future Write operation has occurred.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits ... the Timer interrupt flag (bit 7) and the PA7 Edge Sense Interrupt flag (bit 6). Whenever a Read operation is performed on the Interrupt Flag Register, the two bits are transferred to the microprocessor via the internal Data Bus. Figure 5 shows the Interrupt Flag Register bit configuration.

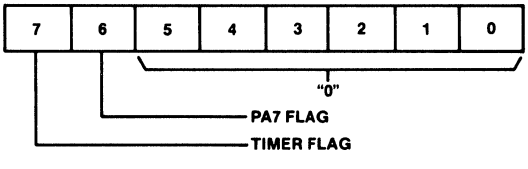


Figure 5. Interrupt Flag Register

It should be noted that the PA7 flag is cleared when the Interrupt Flag Register is read. Also, the Timer flag is cleared when the Timer is either read or written.

Addressing

The G65SC32 is addressed by way of the 7-bit Address Bus (A0-A6), the $\overline{RS}$ input, and the two Chip Select inputs (CS1 and $\overline{CS2}$). To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ both low. To address the I/O and Interval Timer, CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. It is apparent that in order to access the G65SC32 device, CS1 must be high and $\overline{CS2}$ must be low. The $\overline{RS}$ input is used to distinguish between the RAM and the I/O — Interval Timer Sections. When $\overline{RS}$ is low, RAM is addressed. When $\overline{RS}$ is high, the I/O — Interval Timer Section is addressed. To distinguish between Interval Timer and I/O, address line A2 is used. With A2 high, the Interval Timer is accessed. With A2 low, the I/O registers are accessed. Table 1 provides addressing requirements for the G65SC32.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can also function as an Edge Sense Interrupt input. In the interrupt mode, an active transition on line PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, providing the PA7 interrupt has been enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detection logic is accomplished by a Write operation to one of four addresses. The data lines for this Write operation are "don't care" and the addresses to be used can be found in Table 1.

Setting the internal interrupt flag by an active transition on PA7 is always enabled, independent of whether PA7 is set up as an input or output by the Data Direction Register.

The Reset signal ($\overline{RES}$) will disable the PA7 interrupt and at the same time set the active transition logic to the negative edge-detect state. During the $\overline{RES}$ operation, the interrupt flag may be set by a negative transition of PA7. This being the case, it may therefore be necessary to clear the interrupt flag prior to being enabled for its normal use as an edge detecting input. This special Reset can be achieved by reading the Interrupt Flag Register.

I/O Register—Timer Addressing

Table 1 provides the address decoding for all internal functions and Timer programming. Address line A2 distinguishes the I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 may be used to address the desired register.

With A2 high and $\overline{RS}$ high, the Timer is selected, and address lines A1 and A0 are available to decode the "divide-by" matrix as defined in Table 1. Address line A3 is used to enable the interrupt flag to the $\overline{IRQ}$ output.

Address Decoding

Table 1. G65SC32 Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

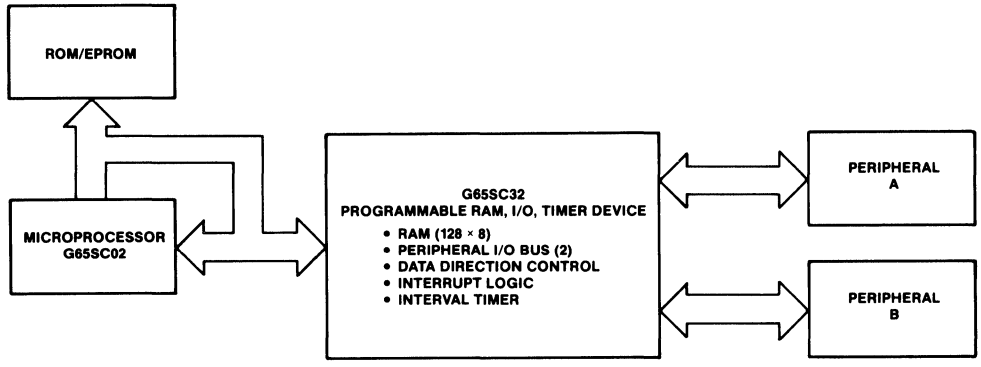
Notes: — = Don't Care, "1" = High Level ($\geq$ 2.4V), "0" = Low Level ($\leq$ 0.4V)

(a) A3 = 0 to Disable Interrupt from Timer to $\overline{IRQ}$
A3 = 1 to Enable Interrupt from Timer to $\overline{IRQ}$

(b) A1 = 0 to Disable Interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to Enable Interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for Negative Edge-Detect
A0 = 1 for Positive Edge-Detect

Application Diagram

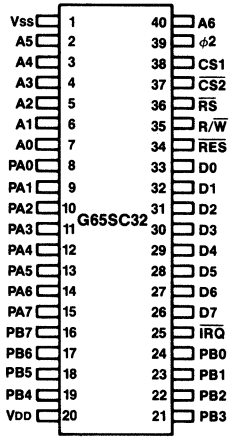


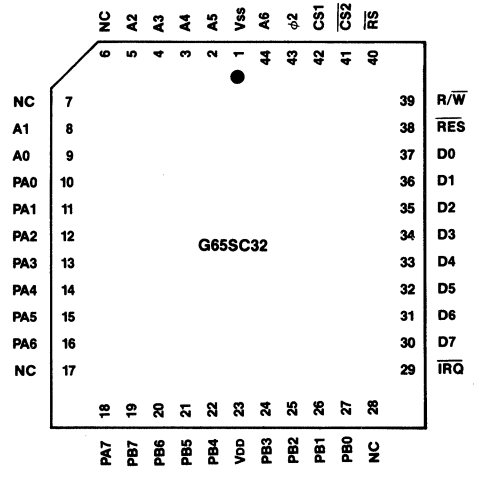
Pin Function Table

A0-A6	Address Bus
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
CS1/$\overline{CS2}$	Device Select

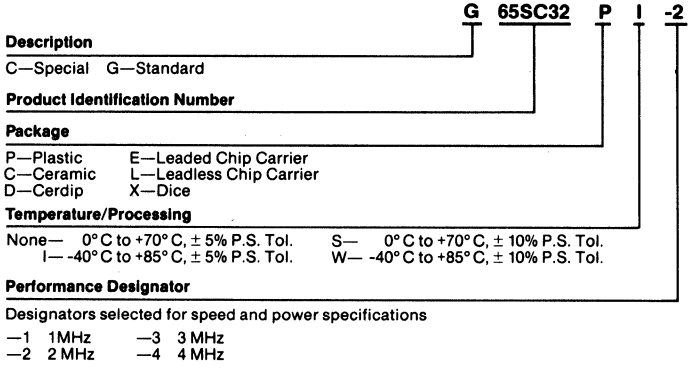
$\overline{RS}$	Function Select
R/$\overline{W}$	Read/Write
$\overline{RES}$	Reset
$\overline{IRQ}$	Interrupt
VDD	Power Supply (+5V)
VSS	Internal Logic Ground

Pin Configuration





Ordering Information



G65SC37

Microcircuits

CMOS Timing and Keyboard/Display Interface (TKDI)

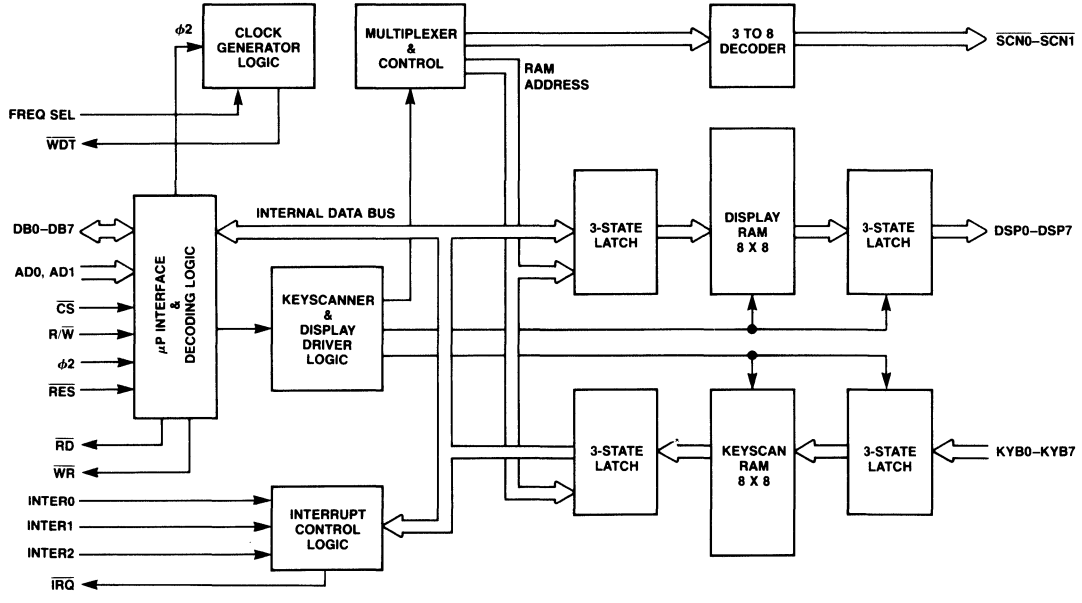
Features

- Advanced CMOS design for low power consumption
- Comprehensive Keyboard/Display Interface within a single chip
- Interface compatible with any 6500 or 6800 series microprocessor
- Internal Keyscanner and Display RAM
- Automatically scans and stores the status of up to 64 keys or switches
- Provides multiplex matrix drive for up to 64 display indicators (LEDs)
- Internally generated Real Time Clock, 10-Millisecond Interrupt and 1-Second Watch Dog Timer signals
- Provides detection, enabling, polling and servicing of up to three external interrupt signals
- Single +5 volt power supply
- Available in 68 pin PLCC package

General Description

GTE Microcircuits' G65SC37 Timing and Keyboard/Display Interface (TKDI) circuit provides a highly versatile interface between a keyboard and/or display unit and any 6500 or 6800 series microprocessor. The G65SC37 is manufactured using GTE's Advanced CMOS technology for low power consumption and precise data handling. The G65SC37 is a multifunction device. It provides automatic scanning of a matrix of up to 64 keys or switches, storing the status of each key into an internal Keyboard RAM. An internal Display RAM allows multiplex driving for an array of up to 64 display LED indicators. Internal Interrupt Control Logic provides for the polling and servicing of up to three external interrupts, plus an internal Real Time Clock interrupt. Internally generated timing signals consist of a Real Time Clock, 10-Millisecond Interrupt and a One-Second Watch-Dog Timer. A pin-select input clock feature allows the TKDI to operate from an external input clock frequency of either 1 MHz or 2.048 MHz. For new and future system designs. the G65SC37 TKDI is the ideal single-chip solution for keyboard/display applications.

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

G65SC51

Microcircuits

CMOS Asynchronous Communications Interface Adapter

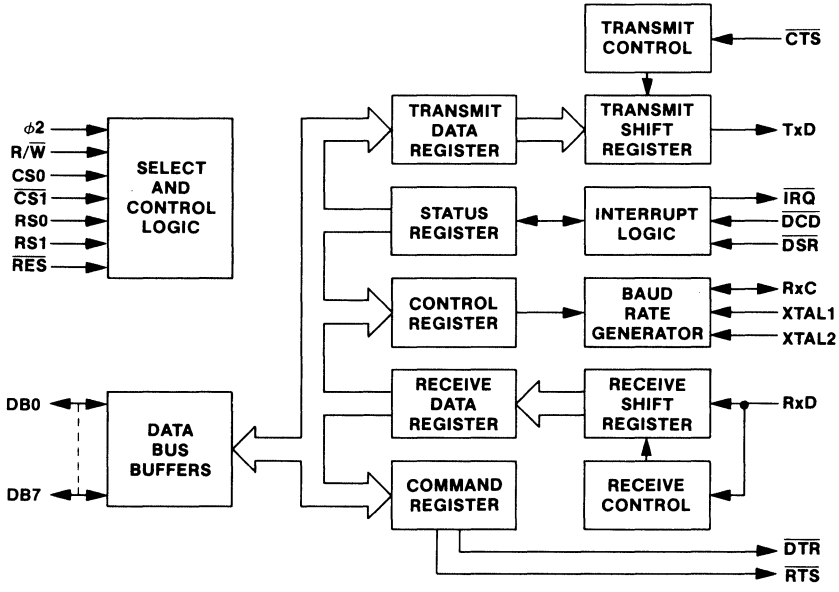
Features

- CMOS process technology for low power consumption
- 15 programmable baud rates (50 to 19,200 baud)
- External 16X clock input for nonstandard baud rates to 125,000 baud
- Programmable interrupt and status registers
- Full-duplex or half-duplex operating modes
- Selectable 5, 6, 7, 8 or 9 bit transmission rates
- Programmable word length, parity generation and detection, and number of stop bits
- Programmable parity options—odd, even, none, mark or space
- Includes data set and modem control signals
- False start bit detection
- Serial echo mode
- Four operating frequencies—1, 2, 3 and 4 MHz
- Available in 28-pin DIP or PLCC package

General Description

The GTE G65SC51 is an Asynchronous Communications Interface Adapter which offers many versatile features for interfacing 6500/6800 microprocessors to serial communication data sets and modems. The G65SC51's most significant feature is its internal baud rate generator, allowing programmable baud rate selection from 50 to 19,200 baud. This full range of baud rates is derived from a single standard 1.8432 MHz external crystal. For non-standard baud rates up to 125,000 baud, an external 16X clock input is provided. In addition to its powerful communications control features, the G65SC51 offers the advantages of GTE's leading edge CMOS technology, i.e., increased noise immunity, higher reliablity, and greatly reduced power consumption.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} + 0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum ratings.

NOTES:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Except XTAL1)	V_{IH}	2.0	V_{DD} + 0.3	V
Input High Voltage (XTAL1 only)	V_{IHX}	3.1		V
Input Low Voltage (Except XTAL1)	V_{IL}	-0.3	0.8	V
Input Low Voltage (XTAL1 only)	V_{ILX}		1.9	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins	I_{IN}		±1.0	μA
Three-State Leakage Current, (V_{IN} = 0.4 to 2.4V)	I_{TSI}		±10.0	μA
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA)	V_{OH}	2.4		V
Supply Current (No Loads) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	 PD PDSB		 11.0 300	 mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Write Timing										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS

AC Characteristics—Transmit/Receive Timing: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Transmit/Receive Clock Cycle Time (1)	tCCY	400	—	400	—	400	—	400	—	nS
Transmit/Receive Clock High Time	tCH	175	—	175	—	175	—	175	—	nS
Transmit/Receive Clock Low Time	tCL	175	—	175	—	175	—	175	—	nS
XTAL 1 to TxD Propagation Delay	tDD	—	500	—	500	—	330	—	250	nS
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	tDLY	—	500	—	500	—	330	—	250	nS
$\overline{IRQ}$ Propagation Delay (Clear) (2)	tIRQ	—	500	—	500	—	500	—	500	nS

1. The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$
2. Propagation Delay is a function of external RC time constant.

Timing Diagrams

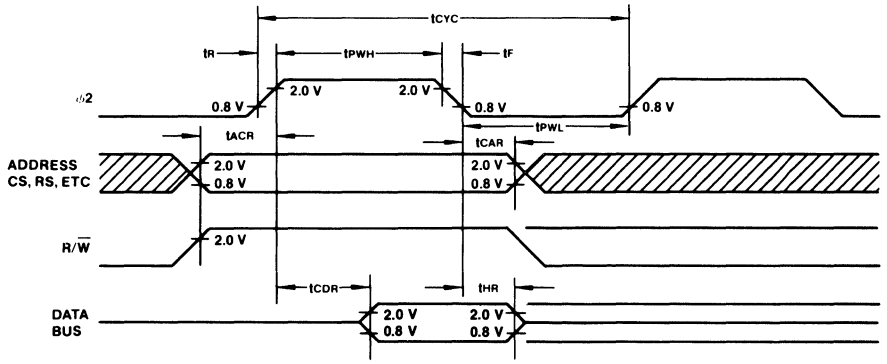


Figure 1. Read Timing

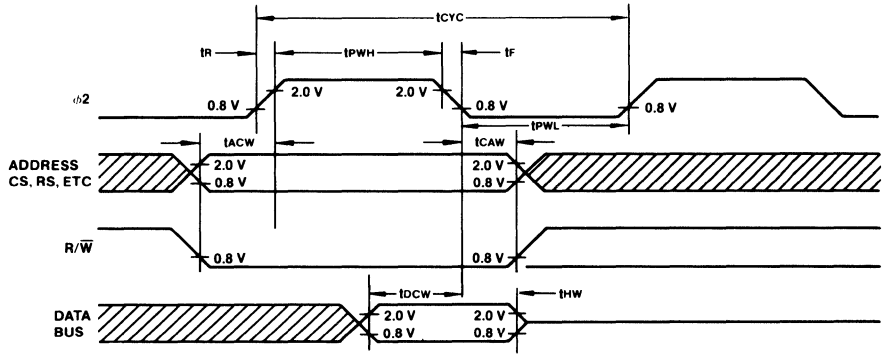
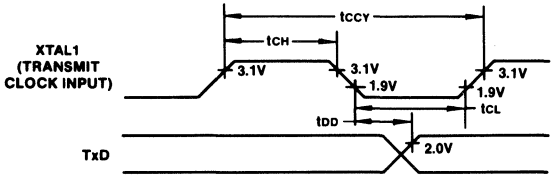


Figure 2. Write Timing

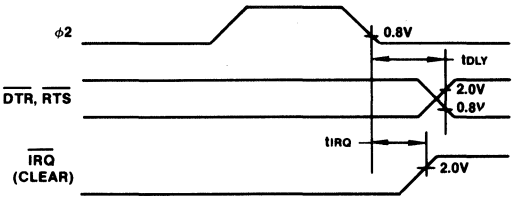
NOTE: Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

Timing Diagrams (Continued)



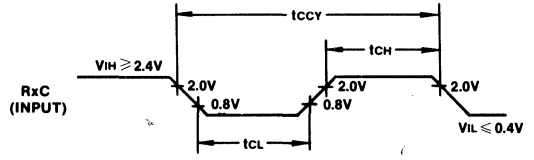
NOTE: 1. TxD is 1/16 TxC rate.
2. XTAL input voltage $V_{IL} \leq 1.5V$, $V_{IH} \geq 3.5V$.

Figure 3. Transmit Timing with External Clock



NOTE: 1. Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

Figure 4. Interrupt and Output Timing



NOTE: 1. RxD rate is 1/16 RxC rate.
2. Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

Figure 5. Receive External Clock Timing

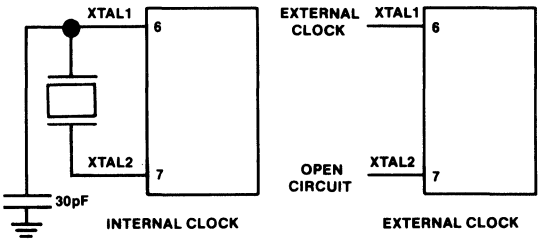
Test and Crystal Specifications

1. Temperature stability ± 0.01% (-40°C to +85°C)
2. Characteristics at 25°C ± 2°C

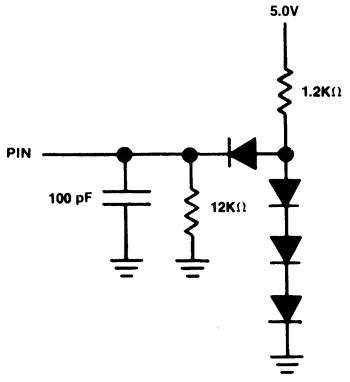
a.	Frequency (MHz)	1.8432
b.	Frequency tolerance (±%)	0.02
c.	Resonance mode	Series
d.	Equivalent resistance (ohm)	400 max.
e.	Drive level (mW)	2
f.	Shunt capacitance (pF)	7 max.
g.	Oscillation mode	Fundamental

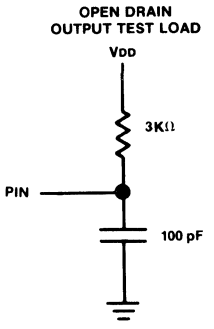
Clock Generation

G65SC51



Test Load





Signal Description (Microprocessor Interface)

Reset ($\overline{RES}$)
Reset clears all internal registers during system initialization.

Interrupt Request ($\overline{IRQ}$)
The Interrupt Request ($\overline{IRQ}$) output signal is generated by the Interrupt Control Logic. $\overline{IRQ}$ is normally held to a high level and goes low when an interrupt occurs. $\overline{IRQ}$ is an open-drain output, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor Interrupt input line.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the G65SC51 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC51 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the G65SC51 (Write operation).

Input Clock ($\phi 2$)
The $\phi 2$ clock is used to trigger all data transfers between the microprocessor and the G65SC51.

Data Bus (DB0-DB7)
The eight bidirectional Data Bus lines are used to transfer data between the G65SC51 and the microprocessor. During a Read operation, data is transferred from the G65SC51 to the microprocessor. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to the G65SC51. The Data Bus lines are in the high impedance state when the G65SC51 is unselected.

Chip Select (CS0, $\overline{CS1}$)
The two Chip Select lines are normally connected to the processor address lines either directly or through decoders. To access a selected G65SC51, CS0 must be high (Logic 1) and $\overline{CS1}$ must be low (Logic 0).

Register Select (RS0, RS1)
The two Register Select lines are normally connected to the processor address lines. This allows the processor to select the various G65SC51 internal registers. Refer to Table 1 for internal register select coding.

Table 1. Register Select Coding

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control Registers can be accessed during both Read and Write operations. Programmed Reset operation does not cause data transfer, but is used to clear (reset) all G65SC51 internal registers. Programmed Reset is used in a slightly different way as compared to the hardware Reset ($\overline{RES}$). These differences are described under each individual register description.

Signal Description (Communications Interface)

Transmit Data (TxD)
TxD is an output line used to transfer NRZ (Non-Return-to-Zero) data to a modem. The LSB (Least Significant Bit) of the Transmit Data Register is the first data bit transmitted. The rate of data transmission (baud rate) is determined by the selected baud rate.

Receive Data (RxD)
RxD is an input line used to receive NRZ input data from a modem. The LSB is always the first data bit received. Received data will always be at the G65SC51's internally programmed baud rate or the baud rate of an externally generated receiver clock. The baud rate is a selection which is made by programming the Control Register. See Figure 6, Control Register Format.

Receive Clock (RxC)
RxC serves as a bidirectional "pin" which can be either the 16X Clock Input or the receiver 16X Clock Output. The 16X Clock Output mode results if the internal baud rate generator is selected for External Receiver Clocking. See Figure 6, Control Register Format.

Request to Send ($\overline{RTS}$)
$\overline{RTS}$ is an output line used as a control function to the modem. The state of $\overline{RTS}$ is determined by the contents of the Command Register. Refer to Figure 7, Command Register Format.

Data Carrier Detect ($\overline{DCD}$)
$\overline{DCD}$ is an input line used to indicate carrier-detect output status from the modem. A low level indicates the modem carrier signal is present, and a high level indicates the modem carrier signal is not present. $\overline{DCD}$ is a high impedance input and must not be used as a no-connect. That is, if unused, this pin must be driven high or low, but not switched.

NOTE: If Command Register Bit 0 is a high (Logic 1) and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and the Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low (Logic 0) for the Receiver to operate.

Clear to Send ($\overline{CTS}$)
$\overline{CTS}$ is an input used to control Transmitter operation. The Transmitter is enabled when $\overline{CTS}$ is low (Logic 0), and is automatically disabled when $\overline{CTS}$ is high (Logic 1).

Data Terminal Ready ($\overline{DTR}$)
$\overline{DTR}$ is an output line used to indicate G65SC51 status to the modem, and is controlled by the processor via Bit 0 of the Command Register. $\overline{DTR}$ low (Logic 0) indicates the G65SC51 is enabled, while $\overline{DTR}$ high (Logic 1) indicates the device is disabled.

Data Set Ready ($\overline{DSR}$)
$\overline{DSR}$ is an input line used to indicate modem status to the G65SC51. $\overline{DSR}$ low (Logic 0) indicates the modem is "ready", while a high (Logic 1) indicates the modem is in a "not ready" state. Like $\overline{DCD}$, $\overline{DSR}$ is a high impedance input and must not be used as a no-connect. If unused, this line must be driven either high or low, but not switched.

NOTE: If Command Register Bit 0 is high (Logic 1) and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

*This allows for 9-bit transmission (8 data bits plus parity).

BAUD RATE GENERATOR

3	2	1	0	
0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	—	—	—	—	—	—	—	—

Figure 6. Control Register Format

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
—	—	0	Parity Disabled—No Parity Bit Generated—No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

NORMAL/ECHO MODE FOR RECEIVER

0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	—	—	—	0	0	0	0	0

Figure 7. Command Register Format

External Crystal Pins (XTAL1, XTAL2)

These two crystal pins are normally used to connect an external crystal (1.8432 MHz) to the internal baud rate generator. This crystal is used to derive the full range of available baud rates. For nonstandard baud rates, an externally generated clock may be connected to the XTAL1 pin. In this case, the XTAL2 pin must float.

Internal Functions

Figure 8 shows the Transmitter/Receiver sections of the G65SC51. Bits 0-3 of the Control Register are used to select the "divisor" which in turn generates the selected baud rate for the Transmitter. Should the Receiver clock be using the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the G65SC51.

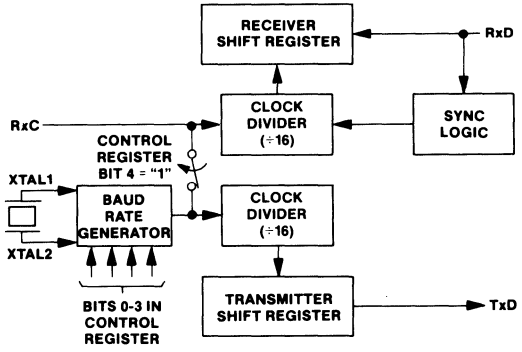


Figure 8. Transmitter/Receiver Clock Circuits

Control Register

The Control Register selects the various operating modes for the G65SC51. Note that the Baud Rate Generator, word length, number of stop bits and the Receiver Clock Source are all controlled by the Control Register. Refer to Figure 6, Control Register Format, for detailed operation and programming information.

Command Register

The Command Register is used to control Transmit/Receive functions. Refer to Figure 7, Command Register Format, for detailed operation and programming information.

Transmit and Receive Data Registers

The Transmit and Receive Data Registers are used as temporary data storage within the G65SC51. Transmit Data Register characteristics are as follows:

- Bit 0 is always the leading bit during any transmission.
- Unused data bits are always the high-order bits in the data word. These unused high-order bits are "don't care" during data transmission.

Receive Register characteristics are as follows:

- Bit 0 is always the leading bit received.
- Unused data bits are always the high-order bits and are "zeros" for the receiver.
- Parity bits are not stored in the Receive Register. The parity bits are stripped off after being used for external parity checking. Therefore, received data in the Receive Data Register will have all parity and unused high-order bits as "zeros."

Figure 9 shows an example of a transmitted or received data word which contains eight data bits, a parity bit and a single stop bit.

Status Register

The Status Register indicates to the processor the status of various G65SC51 functions. Refer to Figure 10 for detailed Status Register operation and programming information.

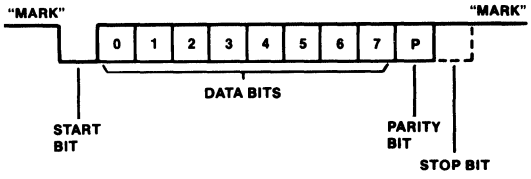
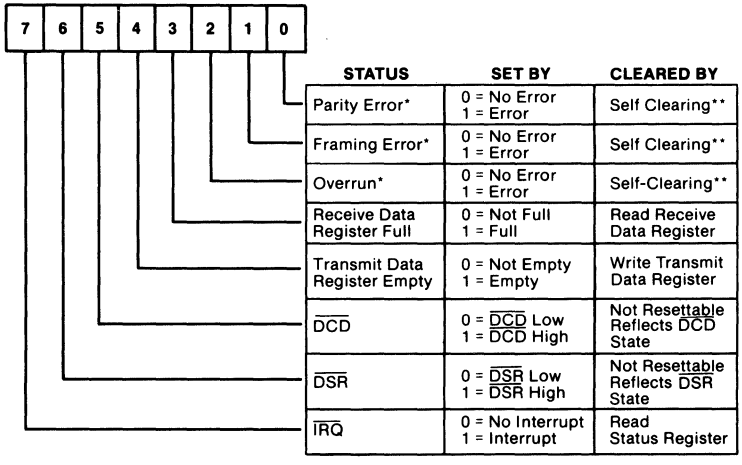


Figure 9. Serial Data Stream Example



*NO INTERRUPT GENERATED FOR THESE CONDITIONS
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR-FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

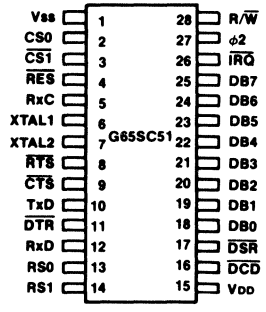
Figure 10. Status Register Format

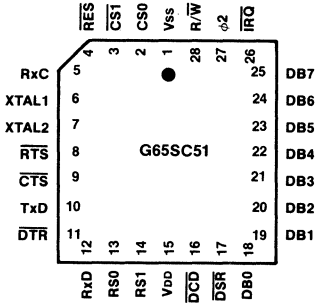
Pin Function Table

CS0, $\overline{CS1}$	Chip Select
$\overline{RES}$	Reset
$\phi 2$	Input Clock
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request
RS0, RS1	Register Selects
XTAL1, XTAL2	Crystal Inputs
TxD	Transmit Data
RxD	Receive Data

RxC	Receive Clock
$\overline{RTS}$	Request to Send
$\overline{CTS}$	Clear to Send
$\overline{DTR}$	Data Terminal Ready
$\overline{DSR}$	Data Set Ready
$\overline{DCD}$	Data Carrier Detect
DB0-DB7	Data Bus
VDD	Positive Power Supply (+5.0 volts)
VSS	Internal Logic Ground

Pin Configuration





Ordering Information

G 65SC51 P I -2

Description

C—Special G—Standard

Product Identification Number

Package

P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing

None— 0° C to +70° C, ± 5% P.S. Tol. S— 0° C to +70° C, ± 10% P.S. Tol.
I— -40° C to +85° C, ± 5% P.S. Tol. W— -40° C to +85° C, ± 10% P.S. Tol.

Performance Designator

Designators selected for speed and power specifications.

—1 1MHz —3 3 MHz
—2 2 MHz —4 4 MHz

G65SC150

Microcircuits

CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Features

- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 2K bytes ROM
  64 bytes RAM
- Standard DTMF and modem frequencies can be generated which are accurate to ±1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

General Description

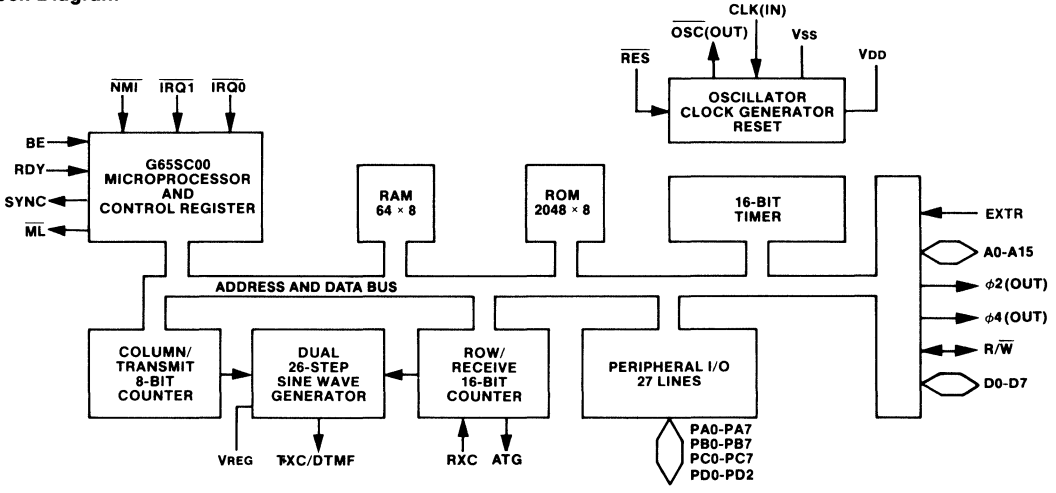
The GTE G65SC150 Communications Terminal Unit (CTU) is a single chip telecommunications microcomputer manufactured using state-of-the-art silicon gate CMOS process technology, which is optimized for telephone line signaling and data transmission applications. A functional block diagram is shown which illustrates the major system functions that are included on the integrated circuit.

The CTU uses the GTE G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 2K bytes of ROM and 64 bytes of RAM, the CTU operates as a single-chip microcomputer.

The internal bus interconnects all microcomputer functions. The address and data bus buffers permit expansion of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. A test and prototyping mode switches internal ROM addresses to external access. An on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-65 to +150	°C
Regulated Voltage	V_{REG}	-0.3 to V_{DD} + 0.3	V

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: All signals except TXC/DTMF, V_{DD} = 5.0V ± 10% unless otherwise stated, T_A = -40°C to +85°C

Parameter	Symbol	Min	Max	Units
Input High Voltage	V_{IH}			
CLK (IN)		2.4	V_{DD} + 0.3	V
All Other Inputs		2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			
CLK (IN)		-0.3	0.4	V
All Other Inputs		-0.3	0.8	V
Output High Voltage	V_{OH}	2.4		V
Address, Data, R/W (I_{OH} = -100μA)				
Peripheral I/O				
Option B (I_{OH} = -10 μA)				
Option C (I_{OH} = -200μA)				
Option D (I_{OH} = -1.0mA)				
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), No Pullup Option,	I_{IN}			
RES, NMI, IRQ0, IRQ1, RDY, BE, CLK(IN)			±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V),	I_{TSI}			
I/O Ports			±10.0	μA
Pull Down Current (Control Register Bit 5 = 0)	I_{PD}		20	μA
Input Pullup Current (Inputs with Pullup Option),	I_{PLP}			
RES, NMI, IRQ0, IRQ1, RDY, BE		-20.0		μA
Input High Current (V_{IH} = 2.4V)	I_{IH}			
Option A		0		μA
Option B		-10		μA
Option C		-200		μA
Input Low Current (V_{IL} = 0.4V)	I_{IL}			
Option B			-100	μA
Option C			-2.4	mA
Output Source Current (V_{OH} = 1.5V)	I_{OH}			
I/O Ports Option D		3.0		mA
Supply Current	I_{DD}			
Standby Mode (No Clock, V_{DD} = 3.0V)			300	μA
4 MHz (ϕ2 = 10 KHz — Bus Off)			1	mA
4 MHz (ϕ2 = 1 MHz — Bus Off)			4	mA
4 MHz (ϕ2 = 1 MHz — Bus On)			6	mA
8 MHz (ϕ2 = 2 MHz — Bus On)			11	mA
Supply Current (V_{REG} = V_{DD})	I_{REG}		1.7	mA
Capacitance (V_{IN} = 0V, T_A = 25°C, F = 1 MHz)				
A0-A15, R/W, Data (Off State)	C_{TS}		15	pF
All Other Signals	C_{IN}		10	pF

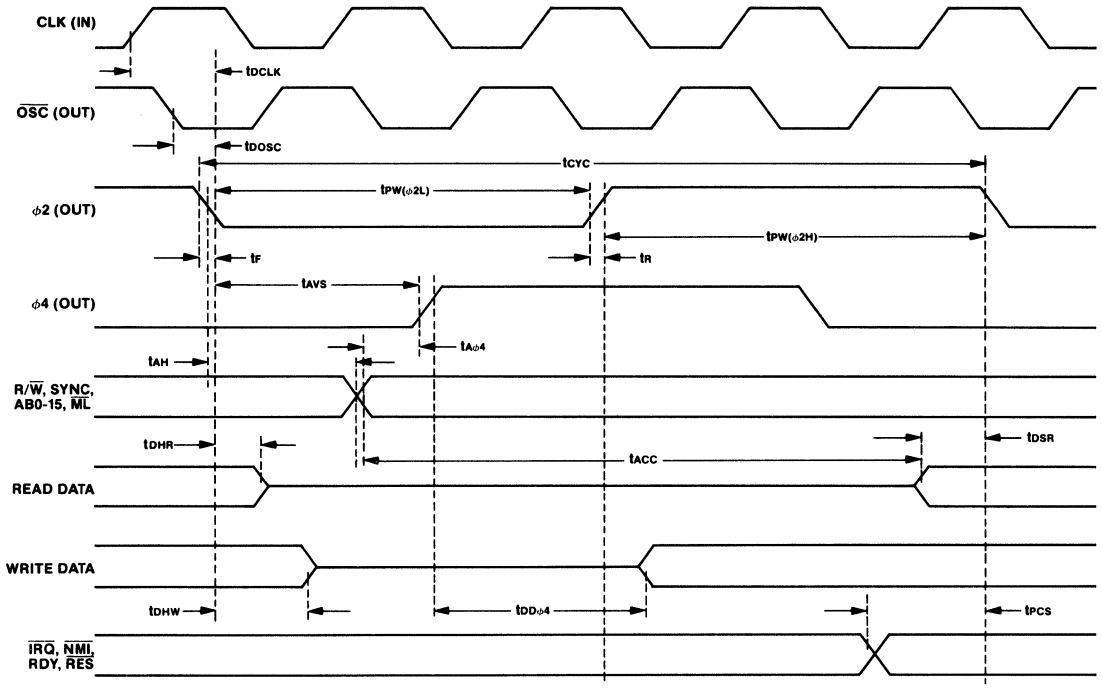
AC Characteristics: V_{DD} = 5.0V ± 10%, T_A = -40°C to +85°C

Parameter	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Delay Time, CLK(IN) to ϕ2(OUT)	t_{DCLK}	—	100	—	100	nS
Delay Time, OSC(OUT) to ϕ2(OUT)	t_{DOSC}	—	75	—	75	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	µS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	—	240	—	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	nS
Delay Time, ϕ2(OUT) to ϕ4(OUT)	t_{AVS}	—	250	—	125	nS
Address Valid to ϕ4(OUT)	$t_{A\phi 4}$	50	—	25	—	nS
Address Hold Time	t_{AH}	10	—	10	—	nS
Access Time	t_{ACC}	695	—	340	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	90	—	90	—	nS
Write Data Hold Time	t_{DHW}	30	—	30	—	nS
Write Data Delay Time	$t_{DD\phi 4}$	—	200	—	110	nS
Processor Control Setup Time	t_{PCS}	90	—	90	—	nS
Select, R/W Setup	t_{AC}	160	—	90	—	nS
Select, R/W Hold	t_{CA}	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	180	nS
Data Bus Hold	t_{HR}	10	—	10	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	nS

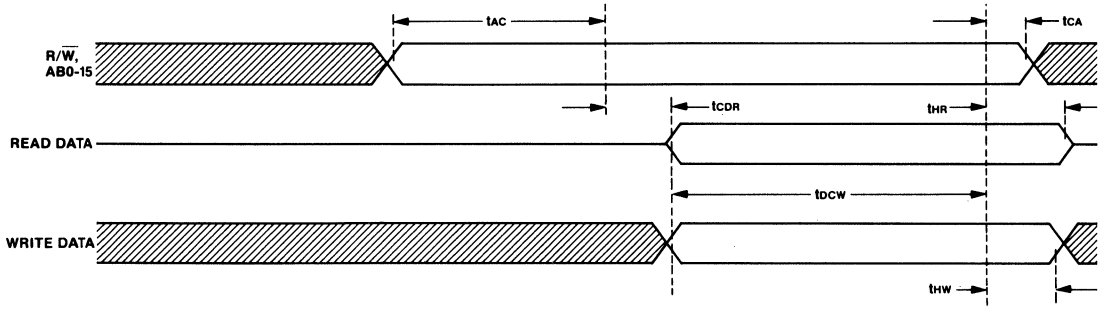
AC Characteristics, TXC/DTMF Output: V_{REG} = V_{DD}, R_L = 10KΩ, V_{DD} = 5.5V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Row Tone	V_{OR}	303	340	382	mVrms	
Column and Transmit Tone	V_{OC}	392	440	494	mVrms	
Pre-emphasis, DTMF High Group	PE_{HB}	1.0	2.0	3.0	dB	
DTMF Total Distortion	DIST			-25	dB	Total out-of-band power relative to sum of Row and Column fundamental power.
DTMF Single Frequency Distortion	DISs			-30	dB	0 to 3.4 KHz band. (Any spectral component.)
Idle Noise	V_{IDLE}			-80	dB	

Timing Diagram



Peripheral Mode Timing



Notes: 1. Load = 100 pF.
2. Voltage levels shown are $V_L < 0.4V$, $V_H > 2.4V$, unless otherwise specified.
3. Measurement points shown are 0.8V and 2.0V, unless otherwise specified.
4. T_{AH} measured at 1.5V.

Characteristic Curve

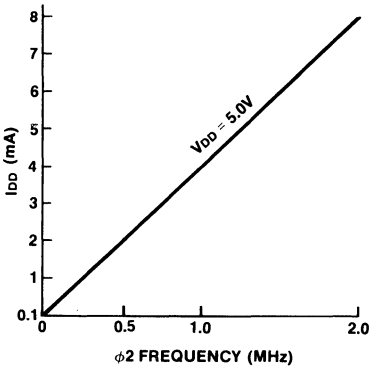


Figure 1(a). Typical Supply Current (IDD) Versus φ2 Frequency—Microprocessor Only

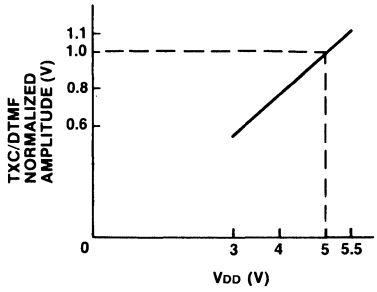


Figure 1(b). Normalized Output Amplitude (TXC/DTMF) Versus Supply Voltage, Unregulated Option

Test Circuits

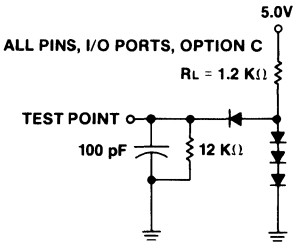


Figure 2(a). Test Load

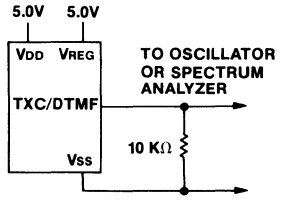


Figure 2(b). Audio Test Load

Signal Description

Microprocessor Signals

Interrupt Request ($\overline{IRQ0}$, $\overline{IRQ1}$)—These TTL compatible signals (bidirectional, active low—two lines) request that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ signals are sampled during φ2(OUT) operation. If the interrupt flag in the status register is zero, the current instruction is completed and the interrupt sequence begins when φ2(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no other maskable interrupts occur. The program counter is loaded with the interrupt vector thereby transferring program control to an interrupt routine. Interrupt and vector addresses are shown in Figure 3. Note that this is a level sensitive input. As a result, another interrupt will occur as soon as the interrupt flag is cleared if $\overline{IRQ}$ remains low. No interrupt will occur when the interrupt flag is cleared and $\overline{IRQ}$ is high but was low prior to clearing the flag. Also note that these are bidirectional signals which are "wire-ORed" with both internal and external interrupt sources. The signals are decoded to form three separate interrupt vector addresses as shown in Figure 3. Since these signals are "wire-ORed" for both internal and external interrupts, the generation of internal interrupts will cause high and low logic level swings at the $\overline{IRQ}$ pins. As outputs, these signals serve to indicate that a specific internal interrupt has occurred. This being the case, caution should be used to prevent connecting these signals to external circuitry which could falsely respond to an internal interrupt condition.

Vector Address	Description	Comment
FFFE, F	Break	Software Interrupt
FFF8, 9	Row/Receive Counter	Pulls $\overline{IRQ0}$ and $\overline{IRQ1}$ Low
FFFA, B	External	$\overline{IRQ1}$
FFFC, D	Timer/Counter	Pulls $\overline{IRQ0}$ Low
FFEE, F	Reset	$\overline{RES}$
FFEC, D	Non-Maskable	$\overline{NMI}$

Figure 3. Interrupt and Vector Addresses

Non-Maskable Interrupt ($\overline{NMI}$)—A negative-going edge on this input, active low signal unconditionally starts a non-maskable interrupt sequence within the microprocessor. The $\overline{NMI}$ signal is sampled during φ2(OUT) operation. The current instruction is completed and the interrupt sequence begins when φ2(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no maskable interrupts occur. The program counter is loaded with the interrupt vector from locations FFEC (low byte) and FFED (high byte), thereby transferring program control to the non-maskable interrupt routine. Note that this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. No interrupt will occur if $\overline{NMI}$ is low and a negative-going edge has not occured since the last non-maskable interrupt.

Bus Enable (BE)—When this input, active high signal is high, (R/$\overline{W}$) is an output, indicating internal control of read and write operations. When BE is low, the address/data bus is reversed allowing access to internal ROM, RAM and I/O from an external device. R/$\overline{W}$ becomes an input, controlling the internal read and write operations. The φ2(OUT) and φ4(OUT) outputs are used for system timing. BE is also used to switch the computer to the test and prototype mode. During processor initialization, BE is high before Reset ($\overline{RES}$) goes high for normal operation. When in the Test and Prototype Mode, internal ROM may be disabled, thus allowing the use of external memory addresses F800 through FFFF. To initiate the Test and Prototype Mode, BE must be held low while bringing Reset high. Note that BE must remain low for at least one clock cycle after Reset becomes high. For additional information, refer to the Test and Prototype Mode section under Operating Modes.

Synchronize (SYNC)—This output, active high signal identifies microprocessor op code fetches. Synchronize goes high after the start of an op code fetch cycle and stays high for the remainder of that cycle.

Ready (RDY)—This input, active high signal provides a single cycle stepping capability and allows operation with slow memory devices for read or write cycles. If this signal is low when φ2(OUT) is low, the processor will stop when φ2(OUT) goes high. The address and data lines remain at their current state. When RDY goes high, the processor resumes operation.

Memory Lock ($\overline{ML}$)—This signal is an active low output and, in a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB and TSB memory referencing instructions. This signal is low for two cycles: the modify and write cycles, and is available as a metal mask option in place of PD2.

Bus Signals

Address Bus (A0-A15)

Output (BE = 1)
A0-A15 forms a three-state, 16-bit, input/output, active high address bus (65,536 locations) for memory and I/O exchanges on the data bus. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Input (BE = 0)
These lines drive the internal address decoder to select internal ROM, RAM or I/O for external read and write cycles.

Clocks (ϕ2(OUT) and ϕ4(OUT))—These output, active high signals (2 lines) provide timing for external bus read and write operations. ϕ4(OUT) is a metal mask option in place of SYNC.

Data Bus (D0-D7)—D0-D7 constitute an 8-bit bidirectional active high, three-state data bus, used for data exchanges with memory and I/O. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Read/Write (R/$\overline{W}$)

Output (BE = 1)
This output, active low signal is normally in the high state indicating that the CPU is reading data from memory or I/O. In the low state the data bus has valid data from the CPU to be stored at the addressed memory or I/O location. If the TSC control register bit is set, this line is pulled to ground by a high resistance device.

Input (BE = 0)
In systems where this part is used as a peripheral controller, R/$\overline{W}$ is an input, active low signal which controls the output data buffers. When R/$\overline{W}$ is high, the buffers are active and internal data is read by the external microprocessor.

Telecommunications Signals

Transmit Carrier and Dual Tone Multifrequency (TXC/DTMF)—This output signal is connected to the output of an operational amplifier which mixes the two sine wave generator outputs. In a telecommunication application, these signals may be the row and column tones used in DTMF signaling. The level of the dual-tone output is the sum of the levels of a single row and single column output. The modem Transmit Carrier (TXC) is generated by the column/transmit counter and sine wave generator. This signal level is controlled by VREG voltage reference supply and is gated by CC0, CC1, and CC2 control register bits.

Audible Tone Generator (ATG)—This output signal is derived from the carry output of the row/receive counter. The square wave output is gated by the ATG control register bit.

Receive Carrier (RXC)—When the row/receive counter is in the pulse width timer mode, this input signal generates a maskable interrupt after both positive and negative transitions. At the same time, the counter contents are transferred to the row/receive register. In this way, the time between transitions can be measured by an interrupt servicing program.

Peripheral Signals

There are 27 peripheral input/output lines: PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD2. Four memory addressable registers are associated with these signals. Depending upon the mask option chosen, the output can source either 0, 10 or 400 μA at V_{OH} = 2.4 volts. The higher sourcing current may be used to directly drive the base of an external NPN transistor having a grounded emitter, or in a Darlington configuration.

Miscellaneous Signals

Reset ($\overline{RES}$)—A positive transition of this input, active low signal causes an initialization sequence to begin. Reset must be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition. After this time R/$\overline{W}$ is high. The I/O ports (PA, PB, PC and PD) are forced to the high state. All bits in the control register are set to zero. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The interrupt mask flag is set and the program counter is loaded with the restart vector from locations FFEE (low byte) and FFEF (high byte).

Clock In (CLK(IN))—The microcomputer contains an internal clock generator operating at four times the ϕ2 frequency. The frequency of these clocks is externally controlled by a crystal oscillator circuit as shown in Figure 4. The internal generator may also be controlled by an input signal from any external clock source.

Oscillator Out (OSC(OUT))—An inverter whose input is CLK(IN) and output is OSC(OUT) is connected between these two clock pins. This active low inverter has sufficient loop gain to provide oscillation using a crystal. Frequency deviation, usually less than 0.05%, will affect the tone output frequency. There is a bias resistor mask option between the two pins.

External ROM(EXTR—Normally PD1)—When in the Test and Prototype Mode, the PD1 pin assumes an additional function and becomes PD1/EXTR, where an active high input selects external memory and an active low input switches back to internal ROM only. For additional information, refer to the Test and Prototype Mode section under Operating Modes.

Regulated Supply Voltage (VREG)—The D-to-A resistor networks and summing amplifier are powered by connecting VREG. The TXC/DTMF output level is directly proportional to VREG.

Internal Logic Ground (Vss)—This connection is used for the power supply internal logic ground.

Positive Supply Voltage (VDD)—This connection serves as the positive power supply input. Reset (RES) should be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition.

Operating Modes

Normal Mode

In the normal mode, the internal microprocessor is operating and its memory map includes the internal 2K bytes of ROM, 64 bytes of RAM, four general purpose I/O registers, one control register and five timer/counter registers. The three-state control bit in the control register determines whether the external bus is active, thus allowing access to the full 65K addressing space.

Test and Prototype Mode

The Test and Prototype Mode provides a convenient means for system testing and debugging without the need for mask-programmed ROM. The Test and Prototype Mode enables the use of external memory at address locations normally occupied by internal ROM (F800 through FFFF), with internal ROM being disabled. In this mode, system programs can be developed using external memory for the prototype system. The program can then be developed using the same memory locations as reserved for internal ROM. Once the program has been debugged and tested, it can then be committed to internal ROM. The Test and Prototype Mode is initiated during the Reset sequence by holding Bus Enable (BE) low while bringing Reset high. Note that BE must remain low for at least one clock cycle after Reset becomes high. Also, BE must be high before the beginning of the first Vector Read cycle. During the Reset sequence, the Reset Vector will be accessed from external memory locations FFFC and FFFD. Note that the Control Register TSC bit has no effect in the Test and Prototype Mode. Also, in this mode the PD1 I/O line is assigned an additional function and becomes PD1/EXTR. An active high input on this I/O pin selects external memory, while an active low input disables external memory and places internal ROM back into the memory map.

Peripheral Mode

In the peripheral mode, internal ROM, RAM and I/O may be accessed from an external device. This mode is useful when the G65SC150 is used as a peripheral device in a microprocessor system. To enable this mode, the Bus Enable (BE) signal is held low. This stops the microprocessor and reverses the address and data buses. Read/Write becomes an input, thus allowing external control of internal read and write operations.

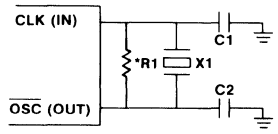
Low Power Mode

Since power consumption in CMOS circuits is directly related to operating frequency, this mode allows operation at greatly reduced power by reducing the microprocessor clock frequency. This mode is enabled by storing a value in the 16-bit Timer register and then setting the ϕ2 mode bit in the control register. The timer counter becomes a programmable clock divider. To further reduce power, the external address and data bus may be disabled by clearing the three-state control bit in the control register.

Functional Description

G65SC150 Microprocessor Unit

For a detailed functional and software programming description of the



C1, C2 = 51 pF
R1 = 1.5 Meg
X1 = 1, 4 or 8 MHz

*R1 is deleted if internal option (R ≈ 1.5 Meg) is selected.

Figure 4. Crystal Circuit for Internal Oscillator

microprocessor, refer to the data sheet for the G65SCXXX family of 8-bit microprocessors. Figure 17 (page 12) illustrates a microprocessor programming model, while a complete listing of operational codes, execution times and memory requirements is provided in Figure 19 (page 13). A brief functional description of the G65SCXXX microprocessor is as follows:

Timing Control—The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each $\phi 1$ clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter—The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode—Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)—All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator—The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers—There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer—The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register—The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Oscillator/Clock Generator

A functional block diagram of the oscillator/clock generator circuitry is shown in Figure 5. The circuits are described in the following three paragraphs:

Oscillator—The clock oscillator accommodates a crystal of up to 8 MHz. CLK(IN) and $\overline{OSC}$(OUT) are TTL compatible. An oscillator bias resistor between these pads is a mask option. With the resistor connected, the circuit requires only an external crystal. For an external oscillator, the resistor is disconnected to eliminate static current drain in low-power system.

Microcomputer Clock—In the maximum frequency mode ($\phi 2$ mode = 0) the oscillator frequency divided-by-four provides the microcomputer bus timing signals $\phi 2$(OUT) and $\phi 4$(OUT). The quadrature clock generator delays the $\phi 2$(OUT) signal by one oscillator period. The low-power mode ($\phi 2$ mode = 1) uses the timer counter as a programmable $\phi 2$(OUT) clock divider.

Timer and Counter Clock—A mask option determines whether a divide-by-two circuit is inserted in the counter and timer clocks. With the divider, a higher frequency crystal (8 MHz maximum) may be used to increase the microprocessor speed while the counter and timer speeds remain unchanged. The modem function is enabled by bits in the control register (CC2, CC1, CC0 = 101).

Random Access Memory (RAM)

The 64-byte memory resides in two ranges in the microcomputer address map. Address bit A8 is not decoded for the RAM, allowing addressing at both 01C0-01FF and 00C0-00EF (00F0-00FF is reserved for the telecommunication register set). In a typical program, the RAM would be partitioned for both stack addressing (01XX) and zero page addressing (00XX).

Read Only Memory (ROM)

The 2048-byte ROM is used for program and constant data storage in the microcomputer system. The ROM occupies addresses F800-FFFF in the microcomputer address map.

Control Register

The on-chip timer and counters with their associated interrupts are configured by setting bits in the control register at address 00F7 as shown in Figure 6.

A functional description of the various control register bits is contained in the following paragraphs:

Communication Mode Select—CC2, bit 2; CC1, bit 1; CC0, bit 0—These bits select one of eight operating modes for the row/receive and column/transmit registers and counters.

000—Idle Mode
Both the Row/Receive Counter (RRC) and Row/Receiver Register (RRR) are inactive, with no interrupt generated and no tone output.

001—Interval Timer Mode
In this mode, the row/receive counter is configured as an additional interval counter based on the contents of the row/receive register.

010—Pulse Width Timer Mode
In this mode, the row/receive counter is configured as a pulse width interval timer...measuring the period between transitions of the receive carrier input.

011—Single Tone Row/Tone Generator Mode
As determined by the ATG bit, a square wave is generated at the Audible Tone Generator (ATG), or a sine wave is generated which appears at the TXC/DTMF output.

100—Single Tone Column Mode
In this mode, a single frequency is generated at the TXC/DTMF output.

101—Modem
This mode is a concurrent application of the pulse width timer mode and the single tone column mode.

110—Modem—Divide-by-Two Prescaler Mode
This mode allows transmit and receive, plus low frequency transmit carrier generation.

111—Dual Tone Multifrequency Mode
This mode allows the generation of standard DTMF signaling tones.

Phase 2 Mode Select—Phase 2, Bit 3—This mode controls the frequency at which the microprocessor oscillator operates. Refer to Figure 5, Clock Functional Block Diagram.

0—Maximum Frequency Mode
The frequency at CLK (IN) divided by four is the microprocessor clock.

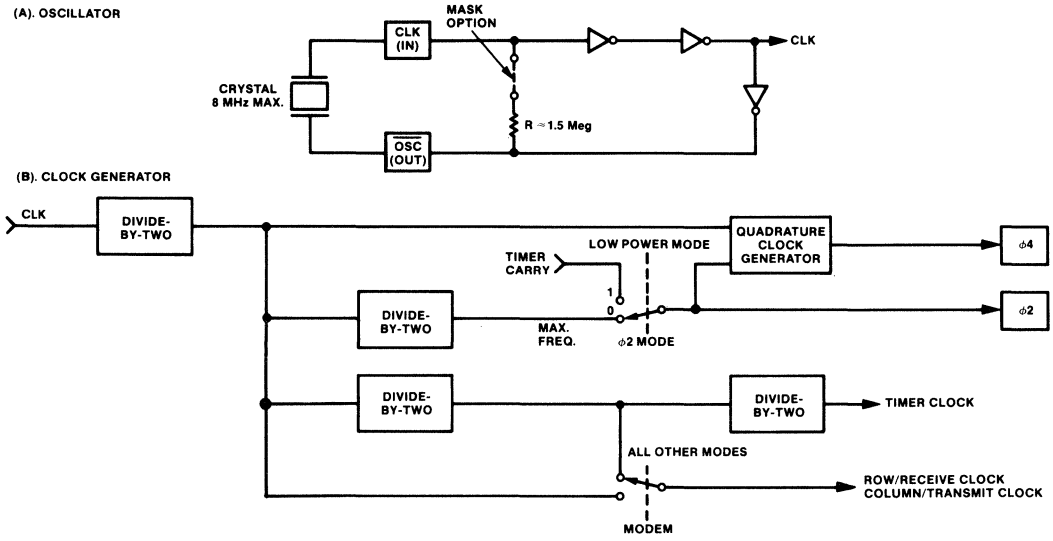


Figure 5. Clock Functional Block Diagram

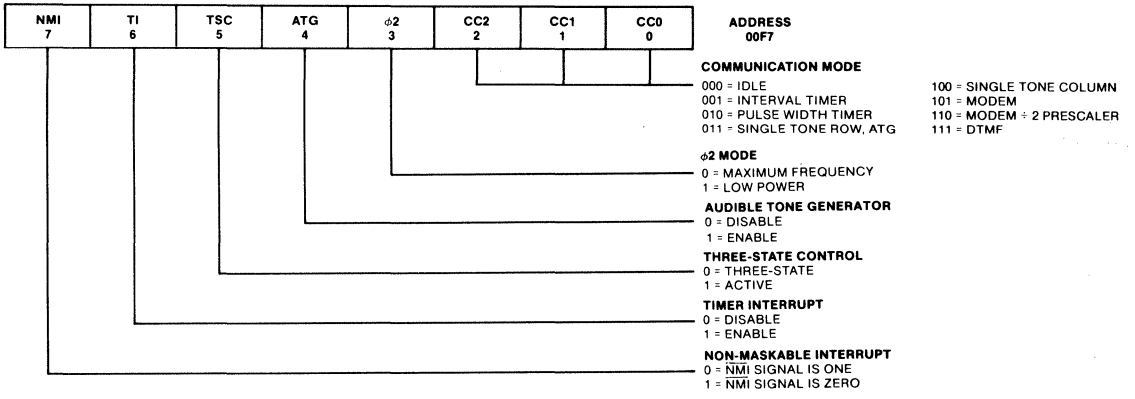


Figure 6. Control Register Functional Block Diagram

1—Low Power Mode
The timer overflow signal is the microprocessor clock. The timer clock input is the frequency CLK(IN) divided by either four or eight depending on a mask option in the clock circuitry. The timer divide ratio is the contents of the timer register plus two.

Audible Tone Generator Enable—ATG, Bit 4

0—Audible Tone Disabled

1—Audible Tone Enabled

Three-State Control Enable—TSC, Bit 5

0—Three-State
The external address and data buses and R/$\overline{W}$ are pulled to Vss by a high resistance device. In a typical application TSC is set to zero when operating in low or back-up power condition. The bus is powered down and not driven externally.

1—Bus Active

Timer Interrupt Enable—TI, Bit 6

0—Timer Interrupt Disabled
The timer register value is transferred to the counter when changing to the enabled interrupt state.

1—Timer Interrupt Enabled

Non-Maskable Interrupt Input—$\overline{NMI}$, Bit 7

0—$\overline{NMI}$ Signal = One (No Interrupt)

1—$\overline{NMI}$ Signal = Zero (Interrupt)
In a typical application this condition indicates low or back-up power system operation. The microprocessor program would monitor this condition to return to normal power operation.

Timer

The 16-bit free-running timer counter and register operates in one of two modes determined by timer interrupt signal and φ2 bits in the control register. Figure 7 illustrates the timer functional block diagram. With a 3.579545 MHz clock, the timer mode is capable of 1.1175 μS resolution. An interrupt is generated at intervals from 2.2349 μS to 73.234 mS. In the low power mode, the counter carry output becomes the microprocessor φ2(OUT) clock. Refer to Figure 18 (page 12), Microprocessor Clock Frequency and Timer Interval.

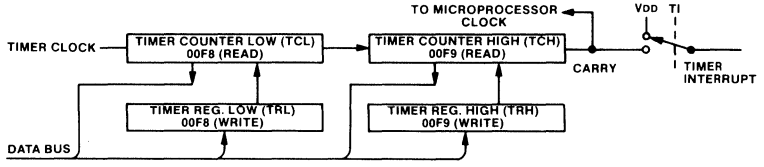


Figure 7. Timer Functional Block Diagram

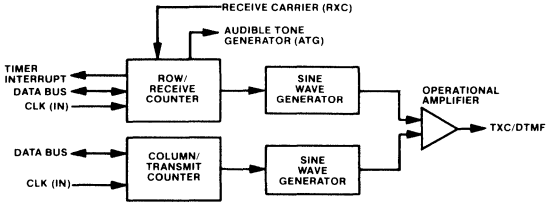


Figure 8. Frequency Detection/Generation Block Diagram

Timer Operation—The timer operating mode is enabled by setting the control register timer interrupt bit to one. The desired time interval is written in the 16-bit timer register (00F8,9). When the timer interrupt (TI) bit is set to one the timer carry interrupts the microprocessor; the counter decrements toward a zero value. When the counter generates a carry by counting past zero, the timer register is again transferred to the counter and interrupts the microprocessor if the interrupt bit in the status register is zero. A read operation will read the contents of the counter and reset the interrupt latch.

Low Power Operation—This mode is enabled by setting the control register $\phi 2$ mode bit to one. Since chip power consumption is directly related to operating frequency, power can be reduced by lowering the microprocessor clock frequency. The desired clock divide ratio is written in the 16-bit timer register at address 00F8 and 00F9. When the counter decrements from zero, the timer register is transferred to the counter. In this configuration, the counter carry output becomes the system $\phi 2$ clock (See Figure 5b).

Frequency Detection/Generation

The frequency detection/generation section of the G65SC150 contains the necessary circuitry to generate a wide range of sine waves, either singularly or in pairs. See Figure 8, Frequency Detection/Generation Block Diagram. In addition, a square wave may be generated as a separate frequency output. Furthermore, a frequency detection input (RXC) is provided for measurement or duplex communications. The row/receive counter and column/transmit counter operate independently or in conjunction with each other to perform the various communications modes as determined by bits CC0, CC1 and CC2 of the control register. The row/receive and column/transmit counters are programmable. Register values for typical applications are shown in Figure 16 (page 12).

Row/Receive Counter

The 16-bit Row/Receive Counter (RRC) and Row/Receive Register (RRR) (address 00F4, 5) operate as a tone generator, pulse width interval timer or interval timer as determined by CCX bits in the Control Register. Figure 9 illustrates the RRC/RRR functional block diagram for these three modes.

In the Idle Mode (CCX = 000), both the counter (RRC) and the register (RRR) are inactive, no interrupt is generated and there is no tone output. With the exception of the single tone column (CCX = 100), any change in CCX to any other state will cause the row/receive counter to be initialized with the current register value and the counter to begin counting.

In the Interval Timer Mode (CCX = 001), the row/receive counter serves as an additional interval timer. The counter interval is received from the row/receive register via the Data Bus. Upon generation of a carry, a timer interrupt is generated and the new contents of RRR is transferred to the counter (RRC). The counter continues counting and the process (cycle) continues until modified. In the interval timer mode, an interrupt is generated at intervals from 2.2349 microseconds to 73.234 milliseconds with a resolution of 1.1175 microseconds.

In the Pulse Width Timer Mode (CCX = 010), the row/receiver counter is used as a pulse width timer, measuring the period between Receive Carrier (RXC) transitions. In this case, both positive and negative transitions of the RXC input cause an interrupt and transfers the counter value to the row/receive register where it may be read by the microprocessor. Following each transfer, the counter continues counting. In telecommunications applications, receive carrier detect and dial tone detect functions can be accomplished.

In the Single Tone Row/Tone Generator mode (CCX = 011), a row/receive counter overflow reloads the counter from the row/receive register. No interrupt is generated. The overflow (carry signal) goes to either the ATG divide-by-two circuit, or to the sine wave generator and TXC/DTMF depending on the state of the ATG control register bit. With a clock frequency of 3.579545 MHz, a square wave with a frequency in the range of 13.7 Hz to 447 KHz may be generated at the Audible Tone Generator (ATG) output. For the same set of inputs, a sine wave with a frequency in the range of 1.05 Hz to 34.4 KHz appears at the TXC/DTMF output.

Column/Transmit Counter

The column/transmit counter circuit is enabled by the CC2 control register bit. A sine wave frequency in the range of 267.8 Hz to 34.4 KHz appears at the TXC/DTMF output. Figure 10 illustrates the column/transmit functional block diagram. For modem operation without the prescaler, the frequency range is 535.7 Hz to 68.8 KHz. A binary count is loaded into the register (CTR) at address location 00F6. The input is then transferred to the counter (CTC). As the counter continues to count, an overflow is generated which serves to reload the counter (CTC) from the contents of the register (CTR).

In the Single Tone Column Mode (CCX = 100), no interrupt is generated. In this mode, the overflow signal serves as one of the clock input signals to the sine wave generator. In this way, a single tone is generated at the TXC/DTMF output.

Combined Modes

In the Modem Mode (CCX = 101), both the pulse width timer mode of the row/receive counter and the single tone column mode are active. This allows simultaneous reception and transmission of data. In telecommunications applications such as duplex 300 bps modem, the row/receive circuitry demodulates the receive carrier at the RXC input while

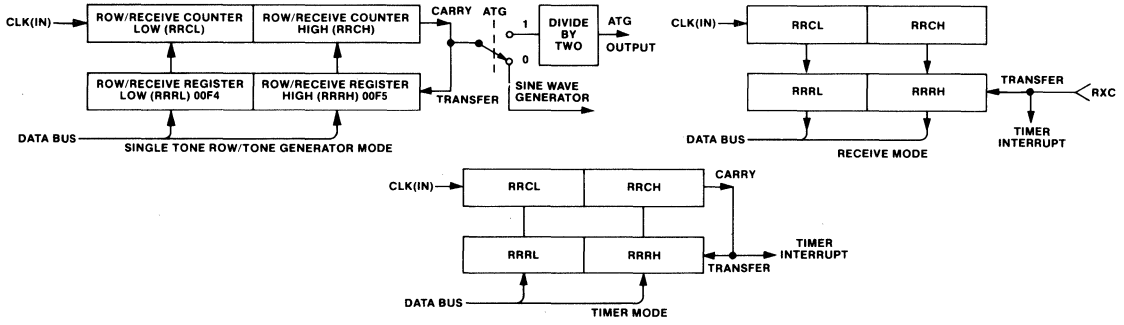


Figure 9. Row/Receive Functional Block Diagram

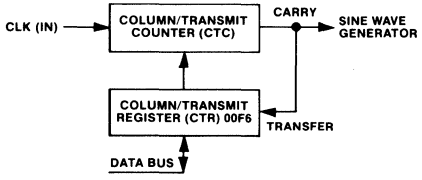


Figure 10. Column/Transmit Functional Block Diagram

the column/transmit circuitry generates the modulated transmit carrier at the TXC/DTMF output. Maximum clock frequency is applied to increase the precision of the transmit carrier frequencies.

In the Modem—Divide-by-Two Prescaler Mode (CCX = 110), operation is the same as the modem mode except that the divide-by-two prescaler is used. In this way, this mode allows low frequency transmit carrier generation.

In the Dual Tone Multifrequency Mode (CCX = 111), a combination of the single tone row mode and single tone column mode is used. In telecommunications applications, this arrangement allows standard DTMF signaling tones to be generated.

Sine Wave Generator

The modem and DTMF output signals are synthesized by the sine wave generator. An approximation of a sine wave is formed by a series of 26 voltage steps per cycle as shown in Figure 11. Figure 12 illustrates the sine wave generator functional block diagram. The two identical divide by 26 circuits are step counters that determine the fixed number of steps per cycle of the sine wave. The inputs to these counters are the outputs of the row/receive and column/transmit dividers that determine the variable step length, or frequency, of each sine wave.

A step select PLA translates the step number from the step counter to a number corresponding to the step voltage level. The D-to-A resistor networks convert these numbers to voltage levels to form the sine wave as shown in Figure 11. The column (high group) frequency amplitude is approximately 2.0 dB greater than the row frequency amplitude to compensate for the high frequency roll-off of the telephone circuit. The outputs of the two D-to-A converters are combined to drive the operational amplifier. V_{REG} is the power supply for the converters and amplifier to ensure a constant tone output level independent of V_{DD} variations. The amplifier output appears on the TXC/DTMF output depending on control register bits, CC0, CC1 and CC2.

To avoid transients when starting or stopping sine wave generation, the output remains at the voltage level defined by the step counters and D-to-A resistor networks when the step counters are stopped.

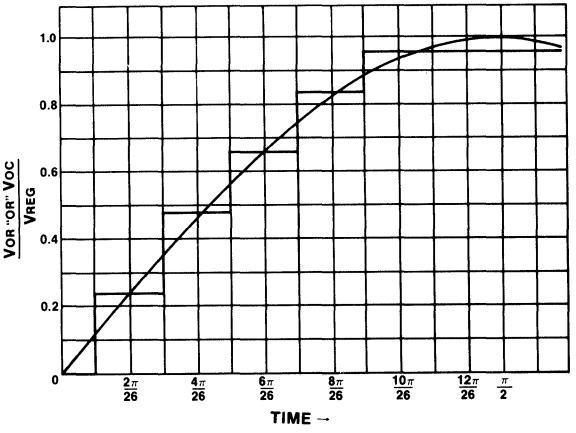


Figure 11. Sine Wave Generator Step Heights

General Formula for Determining Register Values

$$\text{Register Value} = \frac{OSC}{K \times F} - 2$$

$$\text{Register Value (Timer)} = \frac{OSC \times T}{K} - 2$$

OSC = Oscillator Frequency
F = Desired Frequency
T = Timer Period
K = Constant

		Desired Frequency (F) Limits
Modem	K = 26	Limit = 535.7 Hz to 68.8 KHz
DTMF and Modem with Prescaler	K = 52	Limit = 267.8 Hz to 34.4 KHz
ATG	K = 4	Limit = 13.7 Hz to 447 KHz
μP Clock	K = 4	Limit = 13.7 Hz to 447 KHz
Timer	K = 4	Limits = 2.2349 μS to 73.234 mS

F = 3.579545 MHz

Input/Output Registers

Figure 13 illustrates the I/O registers and their addresses. There are 27 I/O lines (PA0-PA7, PB0-PB7, PC0-PC7 and PD0-PD2) associated with four memory addressable registers (00F0-3).

Outputs are set by loading the desired bit pattern into the corresponding I/O register. A logic "1" selects a high output (or OFF), and a logic "0" selects a low output. A read operation always detects the logic state at the I/O pin, regardless of the previously loaded register value. When using the I/O pins as inputs, the I/O register should be loaded to provide the appropriate active level. When reset is active ($\overline{RES}$ = 0), all I/O registers and pins are initialized to a logic "1".

Figure 14 illustrates the circuitry associated with each I/O pin. Depending on the mask option chosen, the output can source either 0 μA, 10 μA, 200 μA, or 1.0mA at V_{OH} = 2.4 volts, or 3mA at 1.5 volts.

Address and Data Buffer

These buffers allow memory and I/O expansion of the microprocessor bus. Each buffer is TTL compatible. Control register bit TSC is set to one for normal operation (bus active). When TSC is set to zero, R/$\overline{W}$, and address lines AB0-AB15 and DB0-DB7 are pulled to ground by a high resistance device. In a typical application, TSC is set to zero when the external bus is not powered. Figure 15 illustrates a complete memory address map.

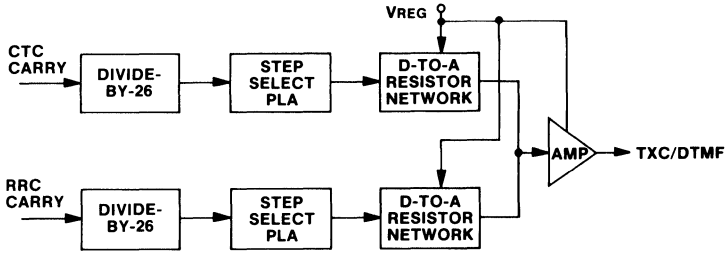


Figure 12. Sine Wave Generator Functional Block Diagram

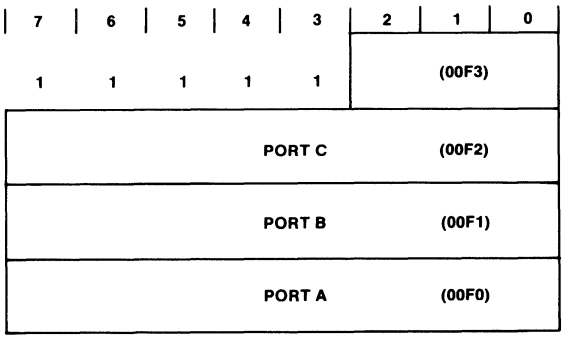


Figure 13. I/O Port Functional Block Diagram

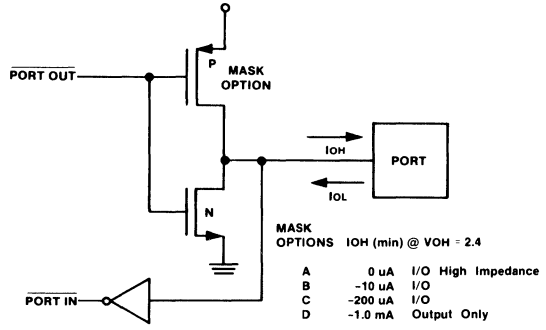


Figure 14. I/O Port Schematic

ADDRESS	DESCRIPTION		
FFFE, F	BREAK	INTERRUPT VECTORS	2048 BYTES ROM
FFFC, D	TIMER COUNTER		
FFFA, B	EXTERNAL		
FFF8, 9	ROW/RECEIVE COUNTER		
FFEE, F	RESET		
FFEC, D	NON-MASKABLE		
FFEB			
F800			
01FF			64 BYTES RAM
01C0			
00FF			TELECOM. REGS.
00F8, 9	TIMER		
00F7	CONTROL		
00F6	COLUMN/TRANSMIT		
00F4, 5	ROW/RECEIVE		
00F3	PD0-2 I/O		
00F2	PC0-7 I/O		
00F1	PB0-7 I/O		
00F0	PA0-7 I/O		
00EF	SEE RANDOM ACCESS MEMORY PARAGRAPH, PAGE 6.	(SAME AS 01C0 THRU 01EF, 48 BYTES)	
00C0			

Figure 15. Memory Map

Standard Frequency (Hz)	Oscillator 3.579545 MHz Register Value	Oscillator 3.579545 MHz Actual Frequency (Hz)	Oscillator 4.000000 MHz Register Value	Oscillator 4.000000 MHz Actual Frequency (Hz)
• DTMF Row				
697	98	695	109	699
770	88	773	99	769
852	80	850	89	855
941	72	943	81	938
• DTMF Column				
1209	56	1208	63	1202
1336	51	1324	57	1326
1477	46	1465	51	1479
1633	41	1639	46	1637
• Call Progress Tones				
350	196	349	219	350
440	155	441	174	440
480	142	481	159	481
620	110	620	123	620
• U.S. 110,300 Baud Modem				
1070	63	1076	71	1068
1270	53	1275	60	1261
2025	33	2025	37	2024
2225	30	2221	34	2198

Standard Frequency (Hz)	Oscillator 3.579545 MHz Register Value	Oscillator 3.579545 MHz Actual Frequency (Hz)	Oscillator 4.000000 MHz Register Value	Oscillator 4.000000 MHz Actual Frequency (Hz)
• European 110,300 Baud Modem				
980	69	983	77	986
1180	57	1187	64	1183
1650	41	1639	46	1637
1850	36	1860	41	1832
• Teletext				
390	176	389	196	390
450	152	450	170	450
1300	52	1299	58	1304
2100	32	2086	36	2079
• U.S. 1200 Baud Modem				
390	176	389	196	390
450	152	450	170	450
1200	56	1208	63	1202
2200	30	2221	34	2198

Figure 16. Communications Frequency Generated by Row/Receive and Column/Transmit Counters

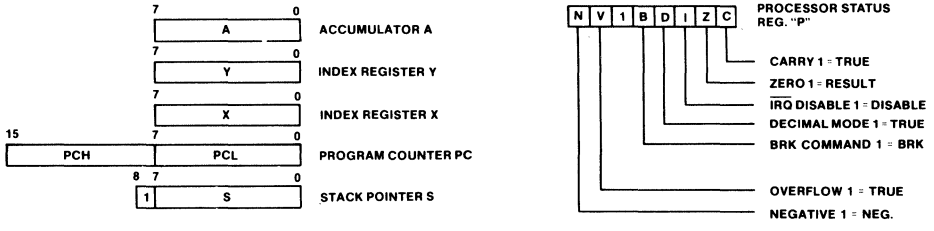


Figure 17. Microprocessor Programming Model

Maximum Frequency Mode (Phase 2, bit 3 is 0)			
Crystal Frequency		Microprocessor Clock	
8 MHz		2 MHz	
4 MHz		1 MHz	
3.579545 MHz		894.9 KHz*	
Lower Power Mode (Phase 2, bit 3 is 1)			
Crystal Frequency	Timer Count	Microprocessor Clock	Timer Interrupt Interval (max. freq. mode)
8 MHz	1	1.0 MHz	1 μS
	19	100 KHz	10 μS
	199	10 KHz	100 μS
	1999	1 KHz	1 mS
	19999	100 Hz	10 mS
	65535	30.5 Hz*	131.072 mS
4 MHz	1	500 KHz	2 μS
	9	100 KHz	10 μS
	99	10 KHz	100 μS
	999	1 KHz	1 mS
	9999	100 Hz	10 mS
	65535	15.3 Hz*	65.536 mS
3.579545 MHz	1	447.4 KHz*	2.2 μS*
	8	99.4 KHz*	10.1 μS*
	88	10.1 KHz*	99.5 μS*
	894	999.8 Hz*	1.0 mS*
	8948	100.0 Hz*	10.0 mS*
	65535	13.7 Hz*	73.2 mS*

*Approximate value

Figure 18. Microprocessor Clock Frequency and Timer Interval

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND, X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3													N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3													M7 M6 • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3													N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A ∀ M → A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3													N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3													0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A→Ms S-1→S										48	3	1																									• • • • • • •	PHA
PHP	P→Ms S-1→S										08	3	1																									• • • • • • •	PHP
PHX	X→Ms S-1→S										DA	3	1																									• • • • • • •	PHX
PHY	Y→Ms S-1→S										5A	3	1																									• • • • • • •	PHY
PLA	S+1→S Ms→A										68	4	1																									N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																									N • • • • Z •	PLY
ROL	[← [7 0] ←C]				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3													N • • • • Z C	ROL
ROR	[→C→ [7 0]]				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3													N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-C̄→A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																											96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																	• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	A∧M → M (6)				1C	6	3	14	5	2																													• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																													• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates A∧M result (same as BIT instruction).

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
\- Subtract
∧ And
∨ Or
∀ Exclusive or

n No. Cycles
No. Bytes
M5 Memory Bit #6
M7 Memory Bit #7

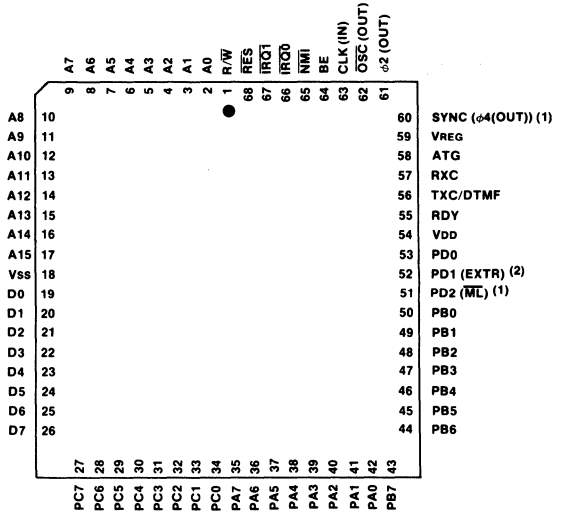
Figure 19. Operational Codes, Execution Times, and Memory Requirements

Pin Function Table

PIN	DESCRIPTION	PIN	DESCRIPTION
A0-Axx	Address Bus	PA0-PA7	Port A
ATG	Audible Tone Generator	PB0-PB7	Port B
BE	Bus Enable	PC0-PC7	Port C
D0-D7	Data Bus	PD0-PD2	Port D
TXC/DTMF	Transmit Carrier/Dual Tone Multifrequency	RDY	Ready
$\overline{IRQ}$	Interrupt Request	$\overline{RES}$	Reset
$\overline{ML}$	Memory Lock	RXC	Receive Carrier
EXTR	External ROM	R/$\overline{W}$	Read/Write
$\overline{NMI}$	Non-Maskable Interrupt	SYNC	Synchronize
CLK(IN)	Clock Input		
$\overline{OSC}$(OUT)	Oscillator Output	VDD	Positive Power Supply (+5.0 volts)
ϕ2(OUT)	Phase 2 Out	VREG	Regulated Supply Voltage
ϕ4(OUT)	Phase 4 Out	VSS	Internal Logic Ground

Pin Configuration

68-Pin Leaded Plastic and Ceramic Chip Carrier
(Top-side View)



NOTES:
1. ϕ4(OUT) AND ML ARE METAL MASK OPTIONS
2. EXTR SELECTED ONLY IN TEST AND PROTOTYPE MODE

G65SC150 Mask Options

The following mask options are available for the G65SC150, and must be specified before an order can be placed. To ensure that the proper options are selected, always contact the nearest GTE Microcircuits Sales Office prior to placing an order.

1. Oscillator feedback resistor
   - Feedback resistor between CLK(IN) and OSC(OUT)
   - No feedback resistor
2. The following signals are available with or without pull-up resistors:
   $\overline{BE}$ $\overline{NMI}$
   $\overline{IRQ0}$ $\overline{RDY}$
   $\overline{IRQ1}$ $\overline{RES}$
3. Pin 51 is available with the following signal option:
   PD2 or $\overline{ML}$
4. Pin 60 is available with the following signal option:
   SYNC or $\phi 4$
5. Three optional I/O source currents are available for the following signals. These source currents include: 0μA, 10μA, 200μA @ 2.4V, and 1mA @ 2.4V or 3mA @ 1.5V.
   PA0-PA7
   PB0-PB7
   PC0-PC7
   PD0-PD2
   ATG

Ordering Information

G 65SC150 PE W -2

Description
C—Special G—Standard

Product Identification Number

Package
P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing
W— -40° C to +85° C, ± 10% P.S. Tol.

Performance Designator
Designators selected for speed and power specifications.
—1 1 MHz —2 2 MHz

G65SC151
Standard Option

Microcircuits

ADV-CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Features

- Standard Option to the G65SC150 Communications Terminal Unit (CTU)
- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 64 bytes RAM, with facilities for external ROM or EPROM
- Standard DTMF and modem frequencies can be generated which are accurate to $\pm$1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

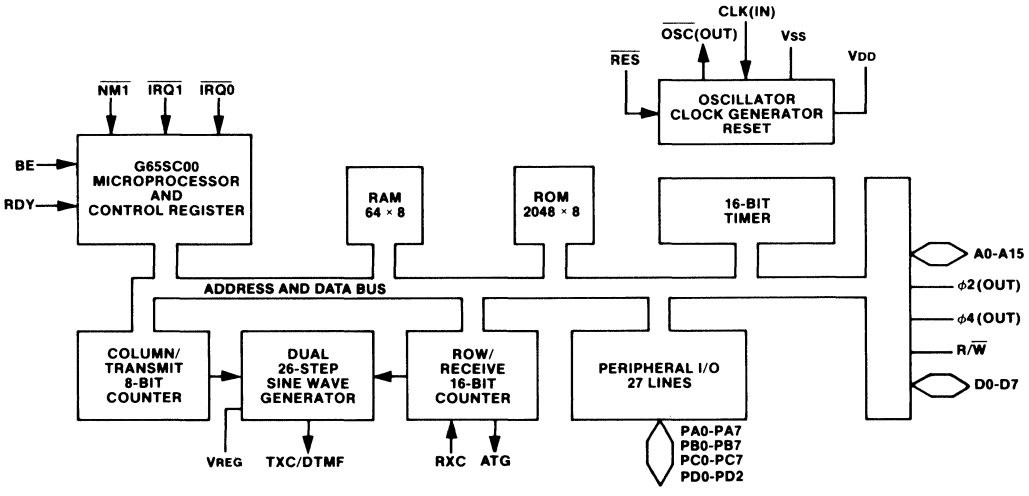
General Description

GTE Microcircuits' G65SC151 is configured as a **Standard Mask Option** to the G65SC150 Communications Terminal Unit (CTU). The G65SC150 CTU offers a variety of mask options which allow the user to configure a CTU that best suits the needs of a particular or unique design application. The G65SC151, however, is offered as a standard product (Standard Option) configuration which includes those options representing the general needs of most application requirements. Included options are detailed on page two. The G65SC151 is a single chip telecommunications microcomputer manufactured using GTE Microcircuits' Advanced CMOS (ADV-CMOS) processing technology. The G65SC151 has been optimized for telephone line signaling and data transmission applications. A functional block diagram is included to illustrate major system functions. For technical specifications and a detailed functional description, refer to the G65SC150 data sheet.

The G65SC151 CTU uses GTE Microcircuits' G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 64 bytes of internal RAM and bus expandable memory, the CTU operates as a single-chip microcomputer.

(continued)

Block Diagram



The CTU's internal bus interconnects all microcomputer functions. The address and data bus buffers permit expansion for the addition of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. The on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

Standard Options

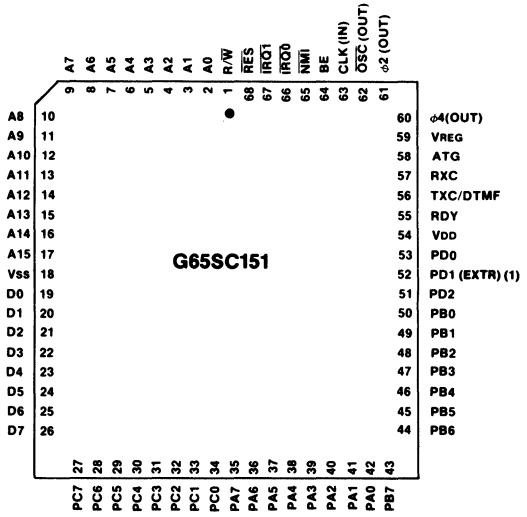
The following Standard Options have been implemented within the G65SC151 CTU. Note that the G65SC151 is identical to the G65SC150 CTU in technical specifications and functional operation. Refer to the G65SC150 CTU data sheet for detailed specifications and operation.

1. The oscillator feedback resistor (between CLK (IN) and $\overline{OSC}$ (OUT)) is **not** provided.
2. The following control signals are provided with pull-up resistors at 20 μA pull-up current:
   BE NMI
   $\overline{IRQ0}$ RDY
   $\overline{IRQ1}$ $\overline{RES}$
3. Pin 51 is provided with the Port D signal PD2.
4. Pin 60 is provided with the ϕ4 (OUT) clock signal.
5. Pin 59 (V_{REG}) requires an external connection to V_{DD}.
6. The following I/O source currents are provided:

PA0-PA7	200 μA pull-up	PD0-PD2	1 mA pull-up
PB0-PB7	200 μA pull-up	ATG	10 μA pull-up
PC0-PC7	**no** pull-up		

Pin Configuration

68-Pin Leaded Plastic and Ceramic Chip Carrier (Top View)



NOTES:
1. EXTR SELECTED ONLY IN TEST AND PROTOTYPE MODE.

Application Programs

The following program consists of two subroutines which will be of value in G65SC151 applications. Note that these subroutines will be included in internal ROM on future devices. These subroutines include:

External Interrupt Vector Table

During the "Normal Mode" startup sequence, this subroutine automatically directs the microprocessor to an Interrupt Vector Table located in external ROM. In this way, the external Reset circuit is no longer required to initiate the Test and Prototype Mode in order to access external ROM. The Reset circuit can now perform the normal reset function, thus greatly simplifying the Reset circuit requirement.

DTMF Frequency Generator

This subroutine generates DTMF frequencies for various oscillator frequencies. The DTMF frequencies are presented at the TXC/DTMF output (pin 56).

```
0020  0000          CTUROM START
0021  0000
0022  0000                ORG $FE00
0023  0000
0024  0000          * TABLE OF ACCUMULATOR VALUES
0025  0000          * FOR DUAL TONE FREQUENCIES
0026  0000          *  (same as 8860 and 8870 DTMF decoders)
0027  0000
0028  0000          * +-----+-----+-----+-----+
0029  0000          * |  1  |  2  |  3  |  D  | 697
0030  0000          * +-----+-----+-----+-----+
0031  0000          * |  4  |  5  |  6  |  E  | 770
0032  0000          * +-----+-----+-----+-----+
0033  0000          * |  7  |  8  |  9  |  F  | 852
0034  0000          * +-----+-----+-----+-----+
0035  0000          * |  B  |  A  |  C  |  0  | 941
0036  0000          * +-----+-----+-----+-----+
0037  0000          *  1209  1336  1477  1633
0038  0000
0039  0000          * EXTERNAL INTERRUPT VECTOR ADDRESSES
0040  0000          NMIV    EQU   $EFEC   Non-Maskable Interrupt
0041  0000          RSTV    EQU   $EFEE   Reset
0042  0000          RCVV    EQU   $EFF8   Row-Receive Counter
0043  0000          EXTV    EQU   $EFFA   External
0044  0000          TMCV    EQU   $EFFC   Timer
```

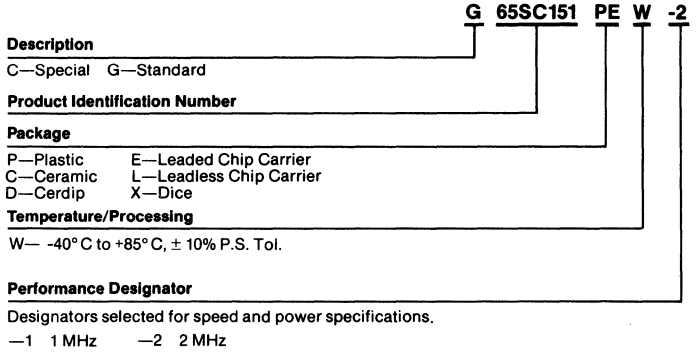
```
0045  0000                BRKV    EQU   $EFFE   Break Instruction
0046  0000
0047  0000                * CTU ON-CHIP I/O ADDRESSES
0048  0000                ROW     EQU   $F4     Row-Receive Counter
0049  0000                COL     EQU   $F6     Column-Transmit Counter
0050  0000                CNTRL   EQU   $F7     Control-Status Register
0051  0000
0052  0000                * CONSTANTS
0053  0000                TSC     EQU   $20     External Bus Three-State Control
0054  0000                DTMF    EQU   $07     DTMF Mode
0055  0000                        EJECT
0056  0000                * DTMF VALUES FOR ROW-RECEIVE COUNTER
0057  0000
0058  0000 486262       R358    DC    I1'72,98,98,98'  3.58 MHz
0059  0004 585858               DC    I1'88,88,88,80'
0060  0008 505048               DC    I1'80,80,72,72'
0061  000C 486258               DC    I1'72,98,88,80'
0062  0010
0063  0010 516D6D       R40     DC    I1'81,109,109,109' 4.0 MHz
0064  0014 636363               DC    I1'99,99,99,89'
0065  0018 595951               DC    I1'89,89,81,81'
0066  001C 516D63               DC    I1'81,109,99,89'
0067  0020
0068  0020 7AA5A5       R60     DC    I1'122,165,165,165' 6.0 MHz
0069  0024 959595               DC    I1'149,149,149,134'
0070  0028 86867A               DC    I1'134,134,122,122'
0071  002C 7AA595               DC    I1'122,165,149,134'
0072  0030
0073  0030 A2DCDC       R80     DC    I1'162,220,220,220' 8.0 MHz
0074  0034 C7C7C7               DC    I1'199,199,199,180'
0075  0038 B4B4A2               DC    I1'180,180,162,162'
0076  003C A2DCC7               DC    I1'162,220,199,180'
0077  0040
0078  0040                * DTMF Values for Column Divider
0079  0040
0080  0040 293833       C358    DC    I1'41,56,51,46'      3.58 MHz
0081  0044 38332E               DC    I1'56,51,46,56'
0082  0048 332E33               DC    I1'51,46,51,56'
0083  004C 2E2929               DC    I1'46,41,41,41'
0084  0050
0085  0050 2E3F39       C40     DC    I1'46,63,57,51'      4.0 MHz
0086  0054 3F3933               DC    I1'63,57,51,63'
0087  0058 393339               DC    I1'57,51,57,63'
0088  005C 332E2E               DC    I1'51,46,46,46'
0089  0060
0090  0060 465E55       C60     DC    I1'70,94,85,77'      6.0 MHz
0091  0064 5E554D               DC    I1'94,85,77,94'
0092  0068 554D55               DC    I1'85,77,85,94'
0093  006C 4D4646               DC    I1'77,70,70,70'
0094  0070
0095  0070 5D7E72       C80     DC    I1'93,126,114,103'  8.0 MHz
0096  0074 7E7267               DC    I1'126,114,103,126'
0097  0078 726772               DC    I1'114,103,114,126'
0098  007C 675D5D               DC    I1'103,93,93,93'
0099  0080                        EJECT
0100  0080                * Subroutine loads dividers with DTMF tone values
0101  0080
0102  0080 BD3000       D80     LDA   R80,X
0103  0083 BC7000               LDY   C80,X
0104  0086 8016                 BRA   SEND
0105  0088
0106  0088 BD2000       D60     LDA   R60,X
0107  008B BC6000               LDY   C60,X
0108  008E 800E                 BRA   SEND
0109  0090
0110  0090 BD1000       D40     LDA   R40,X
0111  0093 BC5000               LDY   C40,X
0112  0096 8006                 BRA   SEND
0113  0098
0114  0098 BD0000       D358    LDA   R358,X
0115  009B BC4000               LDY   C358,X
0116  009E
0117  009E 85F4         SEND    STA   ROW
0118  00A0 84F6                 STY   COL
0119  00A2 60                   RTS
0120  00A3
0121  00A3
0122  00A3 A907         DOFF    LDA   #DTMF   INITIALIZE TONES OFF
0123  00A5 04F7                 TSB   CNTRL
0124  00A7 64F5                 STZ   ROW+1
0125  00A9 64F4                 STZ   ROW
0126  00AB 64F6                 STZ   COL
0127  00AD 60                   RTS
0128  00AE
0129  00AE                * INTERRUPT VECTOR ROUTINES
0130  00AE 6CECEF       NMI     JMP   (NMIV)  Non-Maskable
0131  00B1
```

```
0132  00B1 A920      RST    LDA   #TSC     Reset
0133  00B3 85F7             STA   CNTRL    Set TSC bit to enable
0134  00B5 6CEEEF           JMP   (RSTV)       external bus
0135  00B8
0136  00B8 6CF8EF    RCV    JMP   (RCVV)   Row-Receive
0137  00BB 6CFAEF    EXT    JMP   (EXTV)   External
0138  00BE 6CFCEF    TMC    JMP   (TMCV)   Timer
0139  00C1 6CFEEF    BRK    JMP   (BRKV)   Break Instruction
0140  00C4                  EJECT
0141  00C4                  ORG   $FF80
0142  00C4
0143  00C4          * Set DTMF tone, oscillator frequency
0144  00C4 4CA300    DTMFOF JMP   DOFF     Tones off, and initialize
0145  00C7 4C9800    DTMF35 JMP   D358     3.579545 MHz
0146  00CA 4C9000    DTMF40 JMP   D40      4.000000 MHz
0147  00CD 4C8800    DTMF60 JMP   D60      6.000000 MHz
0148  00D0 4C8000    DTMF80 JMP   D80      8.000000 MHz
0149  00D3
0150  00D3                  ORG   $FFEC
0151  00D3
0152  00D3          * Interrupt Vectors
0153  00D3 AE10             DC    A'NMI' Non-Maskable
0154  00D5 B110             DC    A'RST' Reset
0155  00D7
0156  00D7                  ORG   $FFF8
0157  00D7
0158  00D7 B810             DC    A'RCV' Row-Receive
0159  00D9 BB10             DC    A'EXT' External
0160  00DB BE10             DC    A'TMC' Timer
0161  00DD C110             DC    A'BRK' Break Instruction
0162  00DF
0163  00DF                  END

Local  Symbol Table

BRK       00C1  BRKV      EFFE  C358      0040  C40       0050
C60       0060  C80       0070  CNTRL     00F7  COL       00F6
D358      0098  D40       0090  D60       0088  D80       0080
DOFF      00A3  DTMF      0007  DTMF35    00C7  DTMF40    00CA
DTMF60    00CD  DTMF80    00D0  DTMFOF    00C4  EXT       00BB
EXTV      EFFA  NMI       00AE  NMIV      EFEC  R358      0000
R40       0010  R60       0020  R80       0030  RCV       00B8
RCVV      EFF8  ROW       00F4  RST       00B1  RSTV      EFEE
SEND      009E  TMC       00BE  TMCV      EFFC  TSC       0020
```

Ordering Information



G65SC802
G65SC816

Microcircuits

CMOS 8/16-Bit Microprocessor Family

Features

- Advanced CMOS design for low power consumption and increased noise immunity
- Emulation mode for total software compatibility with 6502 designs
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Direct Register for "zero page" addressing
- 24 addressing modes (including 13 original 6502 modes)
- Wait for Interrupt (WAI) and Stop the Clock (STP) instructions for reduced power consumption and decreased interrupt latency
- 91 instructions with 255 opcodes
- Co-Processor (COP) instruction and associated vector
- Powerful Block Move instructions

Features (G65SC802 Only)

- 8-Bit Mode with both software and hardware (pin-to-pin) compatibility with 6502 designs (64 KByte memory space)
- Program selectable 16-bit operation
- Choice of external or on-board clock generation

Features (G65SC816 Only)

- Full 16-bit operation with 24 address lines for 16 MByte memory
- Program selectable 8-Bit Mode for 6502 coding compatibility.
- Valid Program Address (VPA) and Valid Data Address (VDA) outputs for dual cache and DMA cycle steal implementation
- Vector Pull ($\overline{VP}$) output indicates when interrupt vectors are being fetched. May be used for vectoring/prioritizing interrupts
- Abort interrupt and associated vector for interrupting any instruction without modifying internal registers
- Memory Lock ($\overline{ML}$) for multiprocessor system implementation

General Description

The G65SC802 and G65SC816 are ADV-CMOS (ADVanced CMOS) 16-bit microprocessors featuring total software compatibility with 8-bit NMOS and CMOS 6500 series microprocessors. The G65SC802 is pin-to-pin compatible with 8-bit 6502 devices currently available, while also providing full 16-bit internal operation. The G65SC816 provides 24 address lines for 16 MByte addressing, while providing both 8-bit and 16-bit operation.

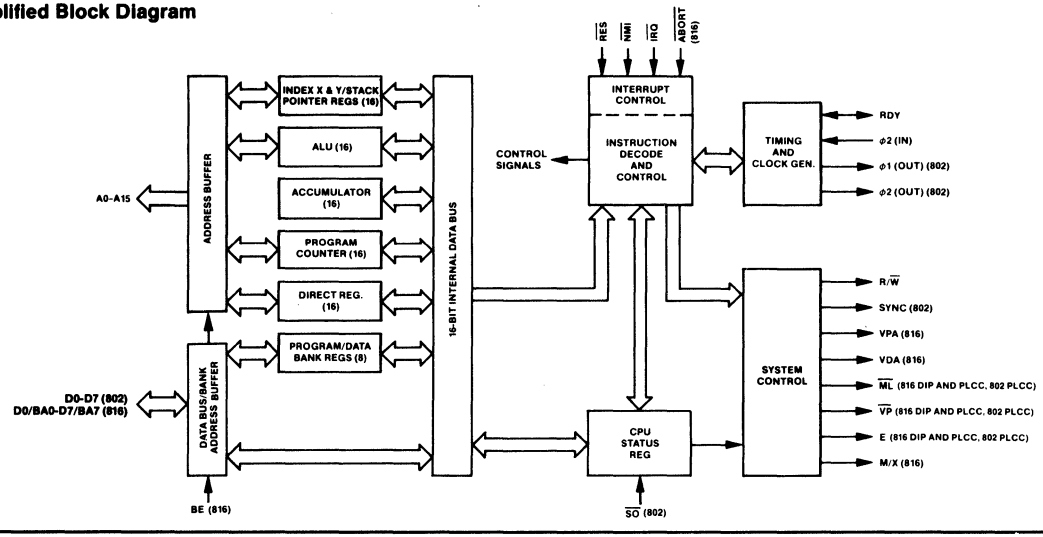
Each microprocessor contains an Emulation (E) mode for emulating 8-bit NMOS and CMOS 6500-Series microprocessors. A software switch determines whether the processor is in the 8-bit emulation mode or in the Native 16-bit mode. This allows existing 8-bit system designs to use the many powerful features of the G65SC802 and G65SC816.

The G65SC802 and G65SC816 provide the system engineer with many powerful features and options. A 16-bit Direct Page Register is provided to augment the Direct Page addressing mode, and there are separate Program Bank Registers for 24-bit memory addressing. Other valuable features include:

- An Abort input which can interrupt the current instruction without modifying internal registers.
- Valid Data Address (VDA) and Valid Program Address (VPA) outputs which facilitate dual cache memory by indicating whether a data or program segment is being accessed.
- Vector modification by simply monitoring the Vector Pull ($\overline{VP}$) output.
- Block Move instructions.

GTE Microcircuits' G65SC802 and G65SC816 microprocessors offer the design engineer a new freedom of design and application, and the many advantages of state-of-the-art ADV-CMOS technology.

Simplified Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	0°C to +70°C
Storage Temperature	T_S	-55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Characteristics (All Devices): V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}			
RES, RDY, IRQ, Data, SO, BE		2.0	V_{DD} + 0.3	V
ABORT, NMI, φ2 (IN)		0.7 V_{DD}	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			
RES, RDY, IRQ, Data, SO, BE		-0.3	0.8	V
ABORT, NMI, φ2 (IN)		-0.3	0.2	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	I_{IN}			
RES, NMI, IRQ, SO, BE, ABORT (Internal Pullup)		-100	1	μA
RDY (Internal Pullup, Open Drain)		-100	10	μA
φ2 (IN)		-1	1	μA
Address, Data, R/W (Off State, BE = 0)		-10	10	μA
Output High Voltage (I_{OH} = -100μA)	V_{OH}			
SYNC, Data, Address, R/W, ML, VP, M/X, E, VDA, VPA, φ1 (OUT), φ2 (OUT)		0.7 V_{DD}	—	V
Output Low Voltage (I_{OL} = 1.6mA)	V_{OL}			
SYNC, Data, Address, R/W, ML, VP, M/X, E, VDA, VPA, φ1 (OUT), φ2 (OUT)		—	0.4	V
Supply Current f = 2 MHz	I_{DD}	—	10	mA
(No Load) f = 4 MHz		—	20	mA
f = 6 MHz		—	30	mA
f = 8 MHz		—	40	mA
Standby Current (No Load; Data Bus = V_{SS} or V_{DD}; φ2(IN) = ABORT = RES = NMI = IRQ = SO = BE = V_{DD})	I_{SB}	—	10	μA
Capacitance (V_{IN} = 0V, T_A = 25°C, f = 2 MHz)				
Logic, φ2 (IN)	C_{IN}	—	10	pF
Address, Data, R/W (Off State)	C_{TS}	—	15	pF

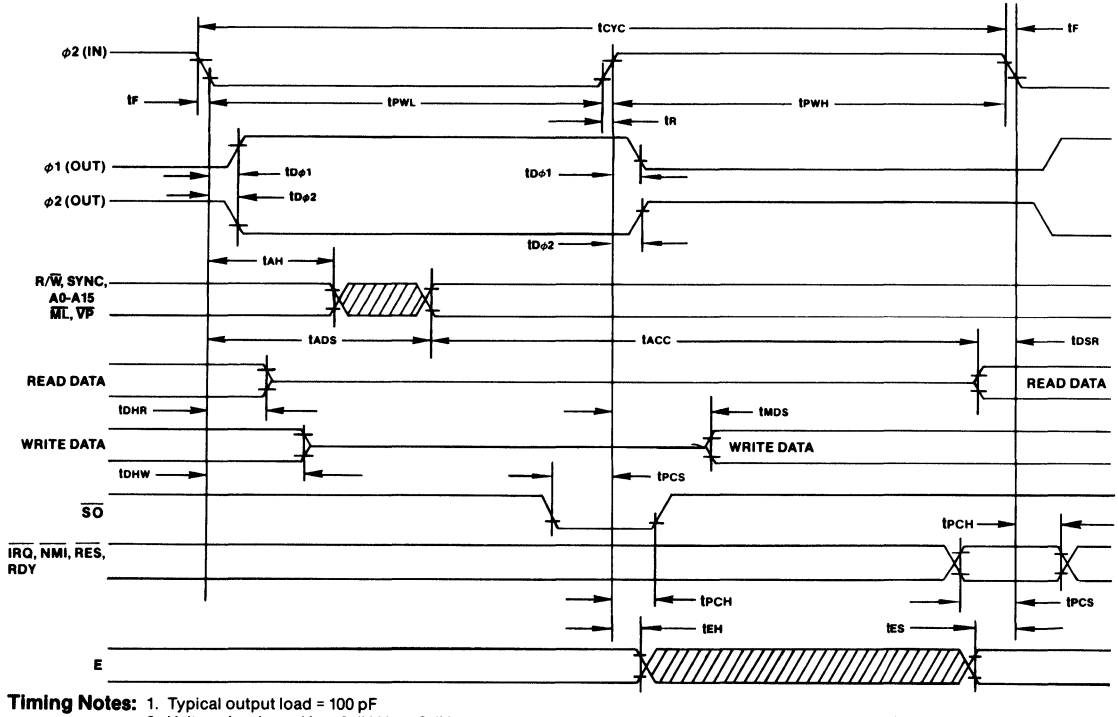
AC Characteristics (G65SC802): V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

		2 MHz		4 MHz		6 MHz		8 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	t_{CYC}	500	DC	250	DC	167	DC	125	DC	nS
Clock Pulse Width Low	t_{PWL}	0.240	10	0.120	10	0.080	10	0.060	10	μS
Clock Pulse Width High	t_{PWH}	240	∞	120	∞	80	∞	60	∞	nS
Fall Time, Rise Time	t_F, t_R	—	10	—	10	—	5	—	5	nS
Delay Time, φ2 (IN) to φ1 (OUT)	$t_{D\phi 1}$	—	40	—	40	—	40	—	40	nS
Delay Time, φ2 (IN) to φ2 (OUT)	$t_{D\phi 2}$	—	40	—	40	—	40	—	40	nS
Address Hold Time	t_{AH}	10	—	10	—	10	—	10	—	nS
Address Setup Time	t_{ADS}	—	100	—	75	—	60	—	40	nS
Access Time	t_{ACC}	365	—	130	—	87	—	70	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	40	—	30	—	20	—	15	—	nS
Write Data Delay Time	t_{MDS}	—	100	—	70	—	60	—	40	nS
Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	10	—	nS
Processor Control Setup Time	t_{PCS}	40	—	30	—	20	—	15	—	nS
Processor Control Hold Time	t_{PCH}	10	—	10	—	10	—	10	—	nS
E Output Hold Time	t_{EH}	10	—	10	—	5	—	5	—	nS
E Output Setup Time	t_{ES}	50	—	50	—	25	—	15	—	nS
Capacitive Load (Address, Data, and R/W)	C_{EXT}	—	100	—	100	—	35	—	35	pF

AC Characteristics (G65SC816): V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

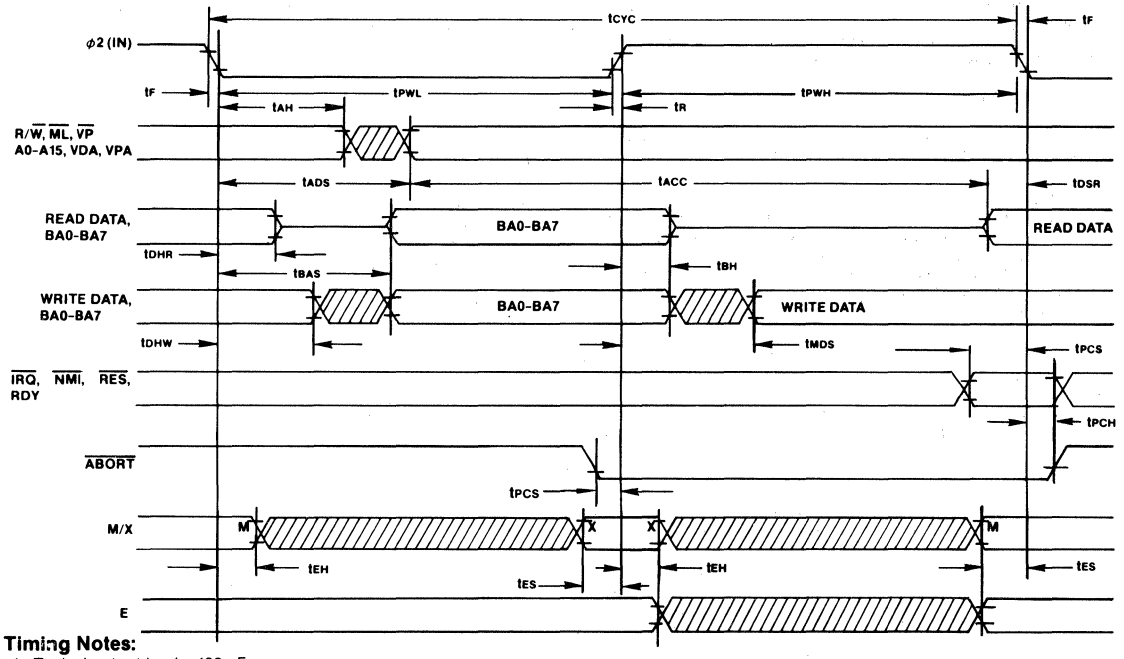
		2 MHz		4 MHz		6 MHz		8 MHz		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	500	DC	250	DC	167	DC	125	DC	nS
Clock Pulse Width Low	t_{PWL}	0.240	10	0.120	10	0.080	10	0.060	10	μS
Clock Pulse Width High	t_{PWH}	240	∞	120	∞	80	∞	60	∞	nS
Fall Time, Rise Time	t_F, t_R	—	10	—	10	—	5	—	5	nS
A0-A15 Hold Time	t_{AH}	10	—	10	—	10	—	10	—	nS
A0-A15 Setup Time	t_{ADS}	—	100	—	75	—	60	—	40	nS
BA0-BA7 Hold Time	t_{BH}	10	—	10	—	10	—	10	—	nS
BA0-BA7 Setup Time	t_{BAS}	—	100	—	90	—	65	—	45	nS
Access Time	t_{ACC}	365	—	130	—	87	—	70	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	40	—	30	—	20	—	15	—	nS
Write Data Delay Time	t_{MDS}	—	100	—	70	—	60	—	40	nS
Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	10	—	nS
Processor Control Setup Time	t_{PCS}	40	—	30	—	20	—	15	—	nS
Processor Control Hold Time	t_{PCH}	10	—	10	—	10	—	10	—	nS
E,MX Output Hold Time	t_{EH}	10	—	10	—	5	—	5	—	nS
E,MX Output Setup Time	t_{ES}	50	—	50	—	25	—	15	—	nS
Capacitive Load (Address, Data, and R/W)	C_{EXT}	—	100	—	100	—	35	—	35	pF
BE to High Impedance State	t_{BHZ}	—	30	—	30	—	30	—	30	nS
BE to Valid Data	t_{BVD}	—	30	—	30	—	30	—	30	nS

Timing Diagram (G65SC802)



Timing Notes:
1. Typical output load = 100 pF
2. Voltage levels are $V_L < 0.4V$, $V_H > 2.4V$
3. Timing measurement points are 0.8V and 2.0V

Timing Diagram (G65SC816)



Timing Notes:

1. Typical output load = 100 pF
2. Voltage levels are $V_L < 0.4V$, $V_H > 2.4V$
3. Timing measurement points are 0.8V and 2.0V

Functional Description

The G65SC802 offers the design engineer the opportunity to utilize both existing software programs and hardware configurations, while also achieving the added advantages of increased register lengths and faster execution times. The G65SC802's "ease of use" design and implementation features provide the designer with increased flexibility and reduced implementation costs. In the Emulation mode, the G65SC802 not only offers software compatibility, but is also hardware (pin-to-pin) compatible with 6502 designs... plus it provides the advantages of 16-bit internal operation in 6502-compatible applications. The G65SC802 is an excellent direct replacement microprocessor for 6502 designs.

The G65SC816 provides the design engineer with upward mobility and software compatibility in applications where a 16-bit system configuration is desired. The G65SC816's 16-bit hardware configuration, coupled with current software allows a wide selection of system applications. In the Emulation mode, the G65SC816 offers many advantages, including full software compatibility with 6502 coding. In addition, the G65SC816's powerful instruction set and addressing modes make it an excellent choice for new 16-bit designs.

Internal organization of the G65SC802 and G65SC816 can be divided into two parts: 1) The Register Section, and 2) The Control Section. Instructions (or opcodes) obtained from program memory are executed by implementing a series of data transfers within the Register Section. Signals that cause data transfers to be executed are generated within the Control Section. Both the G65SC802 and the G65SC816 have a 16-bit internal architecture with an 8-bit external data bus.

Instruction Register and Decode

An opcode enters the processor on the Data Bus, and is latched into the Instruction Register during the instruction fetch cycle. This instruction is then decoded, along with timing and interrupt signals, to generate the various Instruction Register control signals.

Timing Control Unit (TCU)

The Timing Control Unit keeps track of each instruction cycle as it is executed. The TCU is set to zero each time an instruction fetch is executed, and is advanced at the beginning of each cycle for as many cycles as is required to complete the instruction. Each data transfer between registers depends upon decoding the contents of both the Instruction Register and the Timing Control Unit.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place within the 16-bit ALU. In addition to data operations, the ALU also calculates the effective address for relative and indexed addressing modes. The result of a data operation is stored in either memory or an internal register. Carry, Negative, Overflow and Zero flags may be updated following the ALU data operation.

Internal Registers (Refer to Figure 2, Programming Model)

Accumulator (A)

The Accumulator is a general purpose register which stores one of the operands, or the result of most arithmetic and logical operations. In the Native mode (E=0), when the Accumulator Select Bit (M) equals zero, the Accumulator is established as 16 bits wide. When the Accumulator Select Bit (M) equals one, the Accumulator is 8 bits wide. In this case, the upper 8 bits (AH) may be used for temporary storage in conjunction with the Exchange AH and AL instruction.

Data Bank (DB)

During the Native mode (E=0), the 8-bit Data Bank Register holds the default bank address for memory transfers. The 24-bit address is composed of the 16-bit instruction effective address and the 8-bit Data Bank address. The register value is multiplexed with the data value and is present on the Data/Address lines during the first half of a data transfer memory cycle for the G65SC816. The Data Bank Register is initialized to zero during Reset.

Direct (D)

The 16-bit Direct Register provides an address offset for all instructions using direct addressing. The effective bank zero address is formed by adding the 8-bit instruction operand address to the Direct Register. The Direct Register is initialized to zero during Reset.

Index (X and Y)

There are two Index Registers (X and Y) which may be used as general purpose registers or to provide an index value for calculation of the effective address. When executing an instruction with indexed addressing, the microprocessor fetches the opcode and the base address, and then modifies the address by adding the Index Register contents to the address prior to performing the desired operation. Pre-indexing or post-indexing of indirect addresses may be selected. In the Native mode (E=0), both Index Registers are 16 bits wide (providing the Index Select Bit (X) equals zero). If the Index Select Bit (X) equals one, both registers will be 8 bits wide.

Processor Status (P)

The 8-bit Processor Status Register contains status flags and mode select bits. The Carry (C), Negative (N), Overflow (V), and Zero (Z) status flags serve to report the status of most ALU operations. These status flags are tested by use of Conditional Branch instructions. The Decimal (D), IRQ Disable (I), Memory/Accumulator (M), and Index (X) bits are used as mode select flags. These flags are set by the program to change microprocessor operations.

The Emulation (E) select and the Break (B) flags are accessible only through the Processor Status Register. The Emulation mode select flag is selected by the Exchange Carry and Emulation Bits (XCE) instruction. Table 2, G65SC802 and G65SC816 Mode Comparison, illustrates the features of the Native (E=0) and Emulation (E=1) modes. The M and X flags are always equal to one in the Emulation mode. When an interrupt occurs during the Emulation mode, the Break flag is written to stack memory as bit 4 of the Processor Status Register.

Program Bank (PB)

The 8-bit Program Bank Register holds the bank address for all instruction fetches. The 24-bit address consists of the 16-bit instruction effective address and the 8-bit Program Bank address. The register value is multiplexed with the data value and presented on the Data/Address lines during the first half of a program memory read cycle. The Program Bank Register is initialized to zero during Reset.

Program Counter (PC)

The 16-bit Program Counter Register provides the addresses which are used to step the microprocessor through sequential program instructions. The register is incremented each time an instruction or operand is fetched from program memory.

Stack Pointer (S)

The Stack Pointer is a 16-bit register which is used to indicate the next available location in the stack memory area. It serves as the effective address in stack addressing modes as well as subroutine and interrupt processing. The Stack Pointer allows simple implementation of nested subroutines and multiple-level interrupts. During the Emulation mode, the Stack Pointer high-order byte (SH) is always equal to 01. The Bank Address is 00 for all Stack operations.

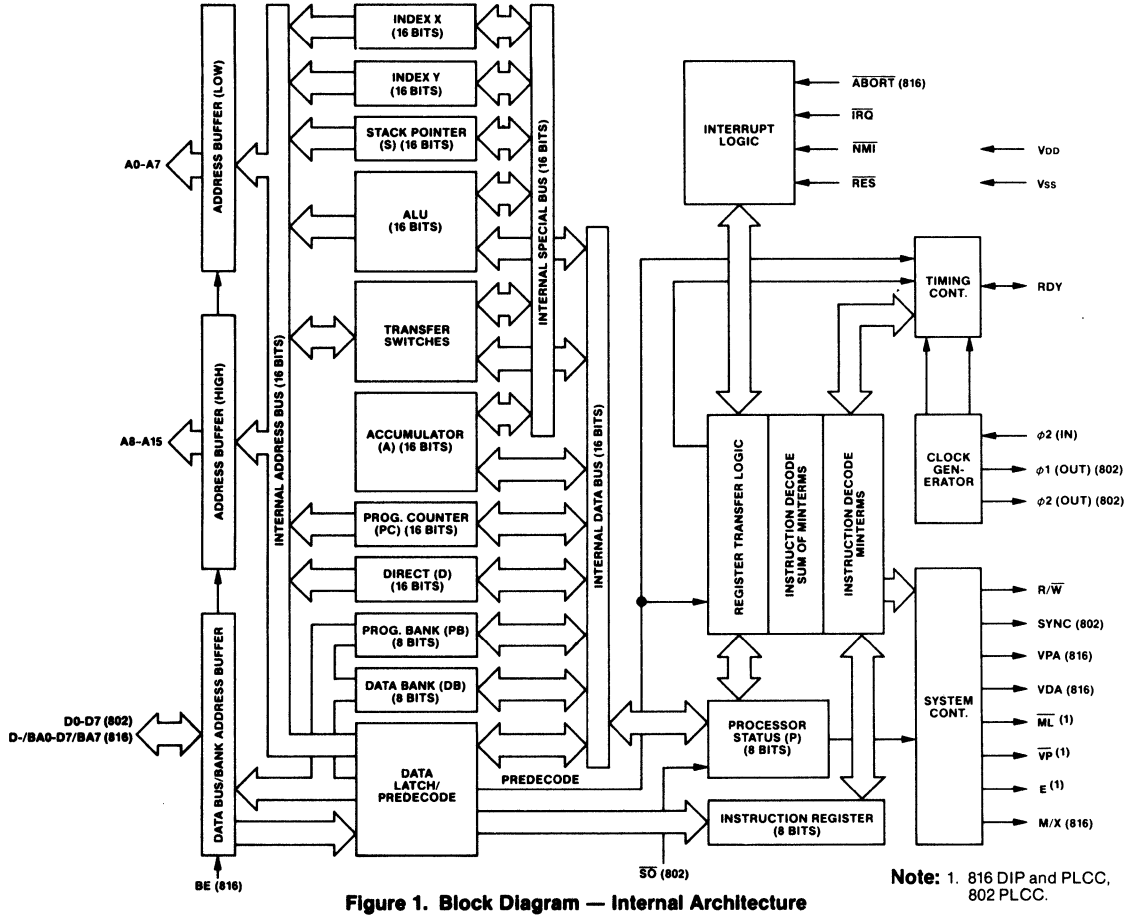


Figure 1. Block Diagram — Internal Architecture

Note: 1. 816 DIP and PLCC, 802 PLCC.

Signal Description

The following Signal Description applies to both the G65SC802 and the G65SC816 except as otherwise noted.

Abort ($\overline{ABORT}$)—G65SC816

The Abort input prevents modification of any internal registers during execution of the current instruction. Upon completion of this instruction, an interrupt sequence is initiated. The location of the aborted opcode is stored as the return address in Stack memory. The Abort vector address is 00FFF8, 9 (Emulation mode) or 00FFE8, 9 (Native mode). Abort is asserted whenever there is a low level on the Abort input, and the $\phi 2$ clock is high. The Abort internal latch is cleared during the second cycle of the interrupt sequence. This signal may be used to handle out-of-bounds memory references in virtual memory systems.

Address Bus (A0-A15)

These sixteen output lines form the Address Bus for memory and I/O exchange on the Data Bus. When using the G65SC816, the address lines may be set to the high impedance state by the Bus Enable (BE) signal.

Bus Enable (BE)

The Bus Enable input signal allows external control of the Address and Data Buffers, as well as the R/$\overline{W}$ signal. With Bus Enable high, the R/$\overline{W}$ and Address Buffers are active. The Data/Address Buffers are active during the first half of every cycle and the second half of a write cycle. When BE is low, these buffers are disabled. Bus Enable is an asynchronous signal.

Data Bus (D0-D7)—G65SC802

The eight Data Bus lines provide an 8-bit bidirectional Data Bus for use during data exchanges between the microprocessor and external memory or peripherals. Two memory cycles are required for the transfer of 16-bit values.

Data/Address Bus (D0/BA0-D7/BA7)—G65SC816

These eight lines multiplex bits BA0-BA7 with the data value. The Bank address is present during the first half of a memory cycle, and the data value is read or written during the second half of the memory cycle. The Bank address external transparent latch should be latched when the $\phi 2$ clock is high or RDY is low. Two memory cycles are required to transfer 16-bit values. These lines may be set to the high impedance state by the Bus Enable (BE) signal.

Emulation Status (E)—G65SC816 (Also Applies to G65SC802, 44-Pin Version)

The Emulation Status output reflects the state of the Emulation (E) mode flag in the Processor Status (P) Register. This signal may be thought of as an opcode extension and used for memory and system management.

Interrupt Request ($\overline{IRQ}$)

The Interrupt Request input signal is used to request that an interrupt sequence be initiated. When the IRQ Disable (I) flag is cleared, a low input logic level initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure the interrupt will be recognized immediately. The Interrupt Request vector address is 00FFFE,F (Emulation mode) or 00FFEE,F (Native mode). Since $\overline{IRQ}$ is a level-sensitive input, an interrupt will occur if the interrupt source was not cleared since the last interrupt. Also, no interrupt will occur if the interrupt source is cleared prior to interrupt recognition.

Memory Lock ($\overline{ML}$)—G65SC816 (Also Applies to G65SC802, 44-Pin Version)

The Memory Lock output may be used to ensure the integrity of Read-Modify-Write instructions in a multiprocessor system. Memory Lock indicates the need to defer arbitration of the next bus cycle. Memory Lock is low during the last three or five cycles of ASL, DEC, INC, LSR, ROL, ROR, TRB, and TSB memory referencing instructions, depending on the state of the M flag.

Memory/Index Select Status (M/X)—G65SC816

This multiplexed output reflects the state of the Accumulator (M) and Index (X) select flags (bits 5 and 4 of the Processor Status (P) Register). Flag M is valid during the $\phi 2$ clock positive transition. Instructions PLP, REP, RTI and SEP may change the state of these bits. Note that the M/X output may be invalid in the cycle following a change in the M or X bits. These bits may be thought of as opcode extensions and may be used for memory and system management.

Non-Maskable Interrupt ($\overline{NMI}$)

A high-to-low transition initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure that the interrupt will be recognized immediately. The Non-Maskable Interrupt vector address is 00FFFA,B (Emulation mode) or 00FFEA,B (Native mode). Since $\overline{NMI}$ is an edge-sensitive input, an interrupt will occur if there is a negative transition while servicing a previous interrupt. Also, no interrupt will occur if $\overline{NMI}$ remains low.

Phase 1 Out ($\phi 1$ (OUT))—G65SC802

This inverted clock output signal provides timing for external read and write operations. Executing the Stop (STP) instruction holds this clock in the low state.

Phase 2 In ($\phi 2$ (IN))

This is the system clock input to the microprocessor internal clock generator (equivalent to $\phi 0$ (IN) on the 6502). During the low power Standby Mode, $\phi 2$ (IN) should be held in the high state to preserve the contents of internal registers.

Phase 2 Out ($\phi 2$ (OUT))—G65SC802

This clock output signal provides timing for external read and write operations. Addresses are valid (after the Address Setup Time (T_{ADS})) following the negative transition of Phase 2 Out. Executing the Stop (STP) instruction holds Phase 2 Out in the High state.

Read/Write (R/$\overline{W}$)

When the R/$\overline{W}$ output signal is in the high state, the microprocessor is reading data from memory or I/O. When in the low state, the Data Bus contains valid data from the microprocessor which is to be stored at the addressed memory location. When using the G65SC816, the R/$\overline{W}$ signal may be set to the high impedance state by Bus Enable (BE).

Ready (RDY)

This bidirectional signal indicates that a Wait for Interrupt (WAI) instruction has been executed allowing the user to halt operation of the microprocessor. A low input logic level will halt the microprocessor in its current state (note that when in the Emulation mode, the G65SC802 stops only during a read cycle). Returning RDY to the active high state allows the microprocessor to continue following the next Phase 2 In Clock negative transition. The RDY signal is internally pulled low following the execution of a Wait for Interrupt (WAI) instruction, and then returned to the high state when a $\overline{RES}$, $\overline{ABORT}$, $\overline{NMI}$, or $\overline{IRQ}$ external interrupt is provided. This feature may be used to eliminate interrupt latency by placing the WAI instruction at the beginning of the $\overline{IRQ}$ servicing routine. If the $\overline{IRQ}$ Disable flag has been set, the next instruction will be executed when the $\overline{IRQ}$ occurs. The processor will not stop after a WAI instruction if RDY has been forced to a high state. The Stop (STP) instruction has no effect on RDY.

Reset ($\overline{RES}$)

The Reset input is used to initialize the microprocessor and start program execution. The Reset input buffer has hysteresis such that a simple R-C timing circuit may be used with the internal pullup device. The $\overline{RES}$ signal must be held low for at least two clock cycles after V_{DD} reaches operating voltage. Ready (RDY) has no effect while $\overline{RES}$ is being held low. During this Reset conditioning period, the following processor initialization takes place:

Registers

D = 0000		SH = 01	
DB = 00		XH = 00	
PB = 00		YH = 00	

	N	V	M	X	D	I	Z	C/E	
P =	*	*	1	1	0	1	*	*/1	* = Not Initialized

STP and WAI instructions are cleared.

Signals

E = 1		$\overline{VDA}$ = 0	
M/$\overline{X}$ = 1		$\overline{VP}$ = 1	
R/$\overline{W}$ = 1		VPA = 0	
SYNC = 0			

When Reset is brought high, an interrupt sequence is initiated:

- R/$\overline{W}$ remains in the high state during the stack address cycles.
- The Reset vector address is 00FFFC,D.

Set Overflow ($\overline{SO}$)—G65SC802

A negative transition on this input sets the Overflow (V) flag, bit 6 of the Processor Status (P) Register.

Synchronize (SYNC)—G65SC802

The SYNC output is provided to identify those cycles during which the microprocessor is fetching an opcode. The SYNC signal is high during an opcode fetch cycle, and when combined with Ready (RDY), can be used for single instruction execution.

Valid Data Address (VDA) and Valid Program Address (VPA)—G65SC816

These two output signals indicate the type of memory being accessed by the address bus. The following coding applies:

VDA	VPA	
0	0	Internal Operation—Address and Data Bus available. Address outputs may be invalid due to low byte additions only.
0	1	Valid program address—may be used for program cache control.
1	0	Valid data address—may be used for data cache control.
1	1	Opcode fetch—may be used for program cache control and single step control.

VDD and VSS

VDD is the positive supply voltage and VSS is system ground. When using only one ground on the G65SC802 DIP package, pin 21 is preferred.

Vector Pull (VP)—G65SC816 (Also Applies to G65SC802, 44-Pin Version)

The Vector Pull output indicates that a vector location is being addressed during an interrupt sequence. $\overline{VP}$ is low during the last two interrupt sequence cycles, during which time the processor reads the interrupt vector. The $\overline{VP}$ signal may be used to select and prioritize interrupts from several sources by modifying the vector addresses.

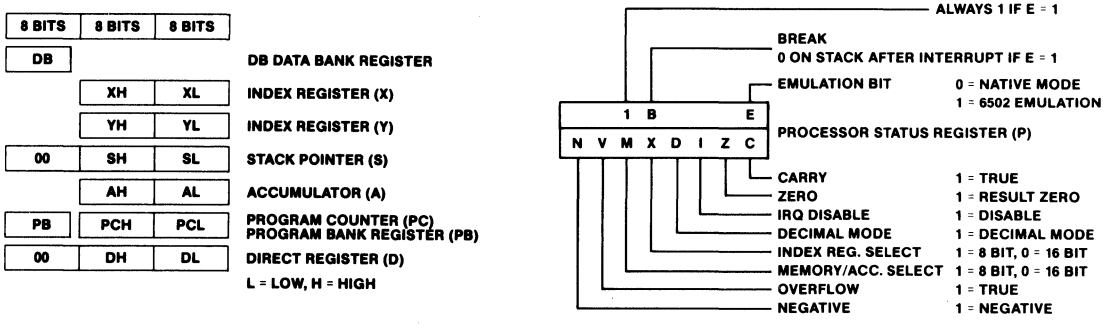


Figure 2. Programming Model

Table 1. G65SC802 and G65SC816 Compatibility

Function	G65SC802/816 Emulation	G65SC02	NMOS 6502
Decimal Mode: • After Interrupts • N, Z Flags • ADC, SBC	 0 → D Valid No added cycle	 0 → D Valid Add 1 cycle	 Not initialized Undefined No added cycle
Read-Modify-Write: • Absolute Indexed, No Page Crossing • Write • Memory Lock	 7 cycles Last 2 cycles Last 3 cycles	 6 cycles Last cycle Last 2 cycles	 7 cycles Last 2 cycles Not available
Jump Indirect: • Cycles • Jump Address, Operand = XXFF	 5 cycles Correct	 6 cycles Correct	 5 cycles Invalid
Branch or Index Across Page Boundary	Read last program byte	Read last program byte	Read invalid address
0 → RDY During Write	G65SC802: Ignored until read G65SC816: Processor stops	Processor stops	Ignored until read
Write During Reset	No	Yes	No
Unused Opcodes	No operation	No operation	Undefined
$\phi 1$ (OUT), $\phi 2$ (OUT), $\overline{SO}$, SYNC Signals	Available with G65SC802 only	Available	Available
RDY Signal	Bidirectional	Input	Input

Table 2. G65SC802 and G65SC816 Mode Comparison

Function	Emulation (E = 1)	Native (E = 0)
Stack Pointer (S)	8 bits in page 1	16 bits
Direct Index Address	Wrap within page	Crosses page boundary
Processor Status (P): • Bit 4 • Bit 5	 Always one, except zero in stack after hardware interrupt Always one	 X flag (8/16-bit Index) M flag (8/16-bit Accumulator)
Branch Across Page Boundary	4 cycles	3 cycles
Vector Locations: ABORT BRK COP IRQ NMI RES	 00FFF8,9 00FFFE,F 00FFF4,5 00FFFE,F 00FFFA,B 00FFFC,D	 00FFE8,9 00FFE6,7 00FFE4,5 00FFEE,F 00FFEA,B 00FFFC,D (1 → E)
Program Bank (PB) During Interrupt, RTI	Not pushed, pulled	Pushed and pulled
0 → RDY During Write	G65SC802: Ignored until read G65SC816: Processor stops	Processor stops
Write During Read-Modify-Write	Last 2 cycles	Last 1 or 2 cycles depending on M flag

G65SC802 and G65SC816 Microprocessor Addressing Modes

The G65SC816 is capable of directly addressing 16 MBytes of memory. This address space has special significance within certain addressing modes, as follows:

Reset and Interrupt Vectors

The Reset and Interrupt vectors use the majority of the fixed addresses between 00FFE0 and 00FFFF.

Stack

The Native mode Stack address will always be within the range 000000 to 00FFFF. In the Emulation mode, the Stack address range is 000100 to 0001FF. The following opcodes and addressing modes can increment or decrement beyond this range when accessing two or three bytes: JSL; JSR (a,x); PEA; PEI; PER; PHD; PLD; RTL; d,s; (d,s),y.

Direct

The Direct addressing modes are often used to access memory registers and pointers. The contents of the Direct Register (D) is added to the offset contained in the instruction operand to produce an address in the range 000000 to 00FFFF. Note that in the Emulation mode, [Direct] and [Direct],y addressing modes and the PEI instruction will increment from 0000FE or 0000FF into the Stack area, even if D=0.

Program Address Space

The Program Bank register is not affected by the Relative, Relative Long, Absolute, Absolute Indirect, and Absolute Indexed Indirect addressing modes or by incrementing the Program Counter from FFFF. The only instructions that affect the Program Bank register are: RTI, RTL, JML, JSL, and JMP Absolute Long. Program code may exceed 64K bytes although code segments may not span bank boundaries.

Data Address Space

The data address space is contiguous throughout the 16 MByte address space. Words, arrays, records, or any data structures may span 64 KByte bank boundaries with no compromise in code efficiency. As a result, indexing from page FF in the G65SC802 may result in data accessed in page zero. The following addressing modes generate 24-bit effective addresses.

- Direct Indexed Indirect (d,x)
- Direct Indirect Indexed (d),y
- Direct Indirect (d)
- Direct Indirect Long [d]
- Direct Indirect Indexed Long [d],y
- Absolute
- Absolute,x
- Absolute,y
- Absolute long
- Absolute long indexed
- Stack Relative Indirect Indexed (d,s),y

The following addressing mode descriptions provide additional detail as to how effective addresses are calculated.

Twenty-four addressing modes are available for use with the G65SC802 and G65SC816 microprocessors. The "long" addressing modes may be used with the G65SC802; however, the high byte of the address is not available to the hardware. Detailed descriptions of the 24 addressing modes are as follows:

1. Immediate Addressing—#

The operand is the second byte (second and third bytes when in the 16-bit mode) of the instruction.

2. Absolute—a

With Absolute addressing the second and third bytes of the instruction form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the operand address.

Instruction:	opcode	addrl	addrh	
Operand Address:	DB	addrh	addrl	

3. Absolute Long—al

The second, third, and fourth byte of the instruction form the 24-bit effective address.

Instruction:	opcode	addrl	addrh	baddr
Operand Address:	baddr	addrh	addrl	

4. Direct—d

The second byte of the instruction is added to the Direct Register (D) to form the effective address. An additional cycle is required when the Direct Register is not page aligned (DL not equal 0). The Bank register is always 0.

Instruction:	opcode	offset	
		Direct Register	
	+	offset	
Operand Address:	00	effective address	

5. Accumulator—A

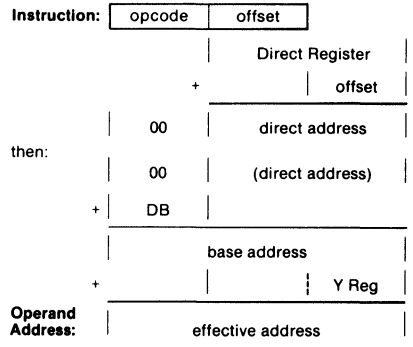
This form of addressing always uses a single byte instruction. The operand is the Accumulator.

6. Implied—.

Implied addressing uses a single byte instruction. The operand is implicitly defined by the instruction.

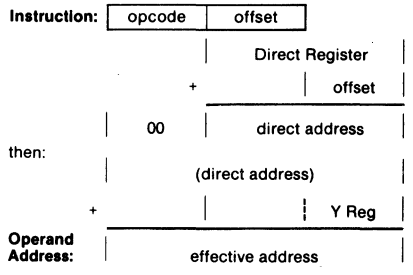
7. Direct Indirect Indexed—(d),y

This address mode is often referred to as Indirect,Y. The second byte of the instruction is added to the Direct Register (D). The 16-bit contents of this memory location is then combined with the Data Bank register to form a 24-bit base address. The Y Index Register is added to the base address to form the effective address.



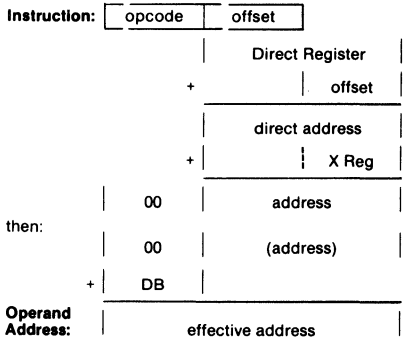
8. Direct Indirect Indexed Long—[d],y

With this addressing mode, the 24-bit base address is pointed to by the sum of the second byte of the instruction and the Direct Register. The effective address is this 24-bit base address plus the Y Index Register.



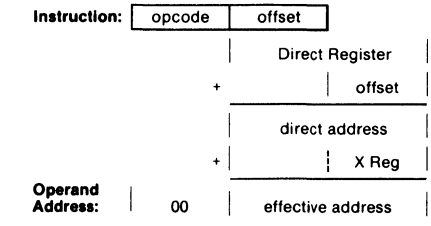
9. Direct Indexed Indirect—(d,x)

This address mode is often referred to as Indirect,X. The second byte of the instruction is added to the sum of the Direct Register and the X Index Register. The result points to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



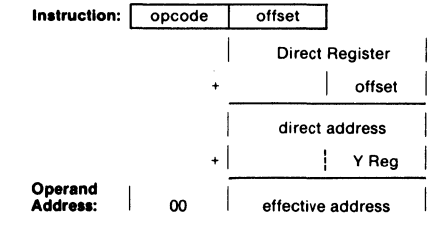
10. Direct Indexed With X—d,x

The second byte of the instruction is added to the sum of the Direct Register and the X Index Register to form the 16-bit effective address. The operand is always in Bank 0.



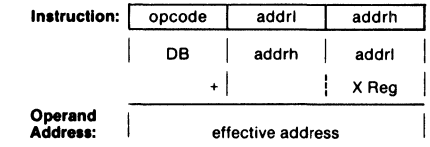
11. Direct Indexed With Y—d,y

The second byte of the instruction is added to the sum of the Direct Register and the Y Index Register to form the 16-bit effective address. The operand is always in Bank 0.



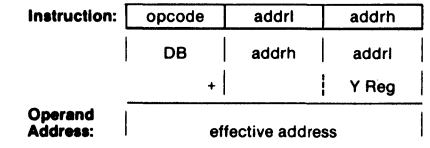
12. Absolute Indexed With X—a,x

The second and third bytes of the instruction are added to the X Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



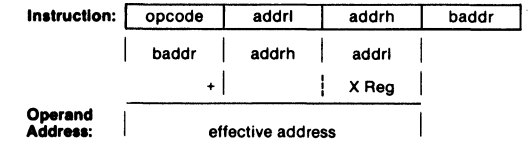
13. Absolute Indexed With Y—a,y

The second and third bytes of the instruction are added to the Y Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



14. Absolute Long Indexed With X—al,x

The second, third and fourth bytes of the instruction form a 24-bit base address. The effective address is the sum of this 24-bit address and the X Index Register.



15. Program Counter Relative—r

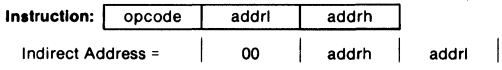
This address mode, referred to as Relative Addressing, is used only with the Branch instructions. If the condition being tested is met, the second byte of the instruction is added to the Program Counter, which has been updated to point to the opcode of the next instruction. The offset is a signed 8-bit quantity in the range from -128 to 127. The Program Bank Register is not affected.

16. Program Counter Relative Long—rl

This address mode, referred to as Relative Long Addressing, is used only with the Unconditional Branch Long instruction (BRL) and the Push Effective Relative instruction (PER). The second and third bytes of the instruction are added to the Program Counter, which has been updated to point to the opcode of the next instruction. With the branch instruction, the Program Counter is loaded with the result. With the Push Effective Relative instruction, the result is stored on the stack. The offset and result are both an unsigned 16-bit quantity in the range 0 to 65535.

17. Absolute Indirect—(a)

The second and third bytes of the instruction form an address to a pointer in Bank 0. The Program Counter is loaded with the first and second bytes at this pointer. With the Jump Long (JML) instruction, the Program Bank Register is loaded with the third byte of the pointer.



New PC = (indirect address)

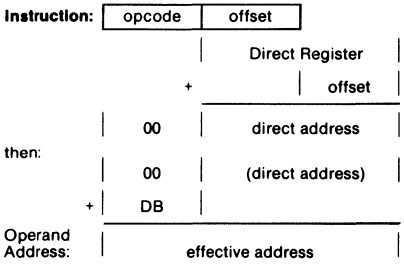
with JML:

New PC = (indirect address)

New PB = (indirect address +2)

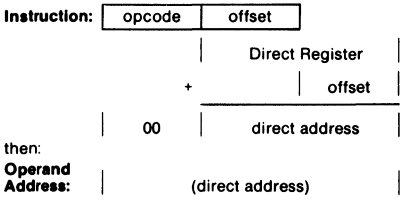
18. Direct Indirect—(d)

The second byte of the instruction is added to the Direct Register to form a pointer to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



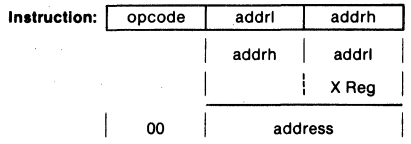
19. Direct Indirect Long—[d]

The second byte of the instruction is added to the Direct Register to form a pointer to the 24-bit effective address.



20. Absolute Indexed Indirect—(a,x)

The second and third bytes of the instruction are added to the X Index Register to form a 16-bit pointer in Bank 0. The contents of this pointer are loaded in the Program Counter. The Program Bank Register is not changed.



then:

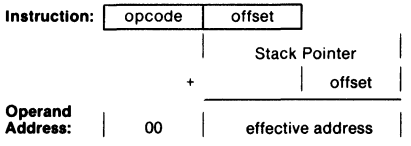
PC = (address)

21. Stack—s

Stack addressing refers to all instructions that push or pull data from the stack, such as Push, Pull, Jump to Subroutine, Return from Subroutine, Interrupts, and Return from Interrupt. The bank address is always 0. Interrupt Vectors are always fetched from Bank 0.

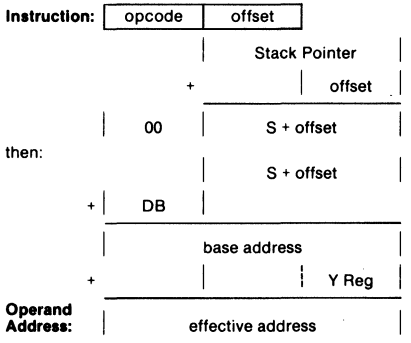
22. Stack Relative—d,s

The low-order 16 bits of the effective address is formed from the sum of the second byte of the instruction and the Stack Pointer. The high-order 8 bits of the effective address is always zero. The relative offset is an unsigned 8-bit quantity in the range of 0 to 255.



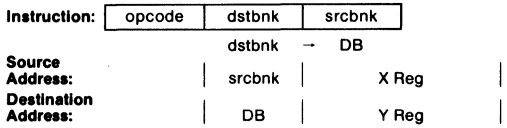
23. Stack Relative Indirect Indexed—(d,s),y

The second byte of the instruction is added to the Stack Pointer to form a pointer to the low-order 16-bit base address in Bank 0. The Data Bank Register contains the high-order 8 bits of the base address. The effective address is the sum of the 24-bit base address and the Y Index Register.



24. Block Source Bank, Destination Bank—xyc

This addressing mode is used by the Block Move instructions. The second byte of the instruction contains the high-order 8 bits of the destination address. The Y Index Register contains the low-order 16 bits of the destination address. The third byte of the instruction contains the high-order 8 bits of the source address. The X Index Register contains the low-order 16 bits of the source address. The Accumulator contains one less than the number of bytes to move. The second byte of the block move instructions is also loaded into the Data Bank Register.



Increment (MVN) or decrement (MVP) X and Y.

Decrement A, (if greater than zero), then PC-3 → PC.

Notes on G65SC802/816 Instructions

All Opcodes Function in All Modes of Operation

It should be noted that all opcodes function in all modes of operation. However, some instructions and addressing modes are intended for G65SC816 24-bit addressing and are therefore less useful for the G65SC802. The following is a list of instructions and addressing modes which are primarily intended for G65SC816 use:

JSL; RTL; [d]; [d],y; JMP al; JML; al; al,x

The following instructions may be used with the G65SC802 even though a Bank Address is not multiplexed on the Data Bus:

PHK; PHB; PLB

The following instructions have "limited" use in the Emulation mode:

- The REP and SEP instructions cannot modify the M and X bits when in the Emulation mode. In this mode the M and X bits will always be high (logic 1).
- When in the Emulation mode, the MVP and MVN instructions only move date in page zero since X and Y Index Register high byte is zero.

Indirect Jumps

The JMP (a) and JML (a) instructions use the direct Bank for indirect addressing, while JMP (a,x) and JSR (a,x) use the Program Bank for indirect address tables.

Switching Modes

When switching from the Native mode to the Emulation mode, the X and M bits of the Status Register are set high (logic 1), the high byte of the Stack is set to 01, and the high bytes of the X and Y Index Registers are set to 00. To save previous values, these bytes must always be stored before changing modes. Note that the low byte of the S, X and Y Registers and the low and high byte of the Accumulator AL and AH are not affected by a mode change.

WAI Instruction

The WAI instruction pulls RDY low and places the processor in the WAI "low power" mode. $\overline{NMI}$, $\overline{IRQ}$ or RESET will terminate the WAI condition and transfer control to the interrupt handler routine. Note that an $\overline{ABORT}$ input will abort the WAI instruction, but will not restart the processor. When the Status Register I flag is set ($\overline{IRQ}$ disabled), the $\overline{IRQ}$ interrupt will cause the next instruction (following the WAI instruction) to be executed without going to the $\overline{IRQ}$ interrupt handler. This method results in the highest speed response to an $\overline{IRQ}$ input. When an interrupt is received after an $\overline{ABORT}$ which occurs during the WAI instruction, the processor will return to the WAI instruction. Other than $\overline{RES}$ (highest priority), $\overline{ABORT}$ is the next highest priority, followed by $\overline{NMI}$ or $\overline{IRQ}$ interrupts.

STP Instruction

The STP instruction disables the $\phi 2$ clock to all circuitry. When disabled, the $\phi 2$ clock is held in the high state. In this case, the Data Bus will remain in the data transfer state and the Bank address will not be multiplexed onto the Data Bus. Upon executing the STP instruction, the $\overline{RES}$ signal is the only input which can restart the processor. The processor is restarted by enabling the $\phi 2$ clock, which occurs on the falling edge of the $\overline{RES}$ input. Note that the external oscillator must be stable and operating properly before $\overline{RES}$ goes high.

Tranfers from 8-Bit to 16-Bit, or 16-Bit to 8-Bit Registers

All transfers from one register to another will result in a full 16-bit output from the source register. The destination register size will determine the number of bits actually stored in the destination register and the values stored in the processor Status Register. The following are always 16-bit transfers, regardless of the accumulator size:

TCS; TSC; TCD; TDC

Stack Transfers

When in the Emulation mode, a 01 is forced into SH. In this case, the B Accumulator will not be loaded into SH during a TCS instruction. When in the Native mode, the B Accumulator is transferred to SH. Note that in both the Emulation and Native modes, the full 16 bits of the Stack Register are transferred to the Accumulator, regardless of the state of the M bit in the Status Register.

Interrupt Processing Sequence

The interrupt processing sequence is initiated as the direct result of hardware Abort, Interrupt Request, Non-Maskable Interrupt, or Reset inputs.

The interrupt sequence can also be initiated as a result of the Break or Co-Processor instructions within the software. The following listings describe the function of each cycle in the interrupt processing sequence:

Hardware Interrupt—$\overline{ABORT}$, $\overline{IRQ}$, $\overline{NMI}$, $\overline{RES}$ Inputs

Cycle No. E = 0	Cycle No. E = 1	Address	Data	R/$\overline{W}$	SYNC	VDA	VPA	$\overline{VP}$	Description
1	1	PC	X	1	1	1	1	1	Internal Operation
2	2	PC	X	1	0	0	0	1	Internal Operation
3	[1]	S	PB	0	0	1	0	1	Write PB to Stack, S-1 → S
4	3	S	PCH [2]	0 [3]	0	1	0	1	Write PCH to Stack, S-1 → S
5	4	S	PCL [2]	0 [3]	0	1	0	1	Write PCL to Stack, S-1 → S
6	5	S	P [4]	0 [3]	0	1	0	1	Write P to Stack, S-1 → S
7	6	VL	(VL)	1	0	1	0	0	Read Vector Low Byte, 0 → P_D, 1 → P_I,00 → PB
8	7	VH	(VH)	1	0	1	0	0	Read Vector High Byte

Software Interrupt—BRK, COP Instructions

Cycle No. E = 0	Cycle No. E = 1	Address	Data	R/$\overline{W}$	SYNC	VDA	VPA	$\overline{VP}$	Description
1	1	PC-2	X	1	1	1	1	1	Opcode
2	2	PC-1	X	1	0	0	1	1	Signature
3	[1]	S	PB	0	0	1	0	1	Write PB to Stack, S-1 → S
4	3	S	PCH	0	0	1	0	1	Write PCH to Stack, S-1 → S
5	4	S	PCL	0	0	1	0	1	Write PCL to Stack, S-1 → S
6	5	S	P	0	0	1	0	1	Write P to Stack, S-1 → S
7	6	VL	(VL)	1	0	1	0	0	Read Vector Low Byte, 0 → P_D, 1 → P_I, 00 → PB
8	7	VH	(VH)	1	0	1	0	0	Read Vector High Byte

Notes:
[1] Delete this cycle in Emulation mode.
[2] Abort writes address of aborted opcode.
[3] R/$\overline{W}$ remains in the high state during Reset.
[4] In Emulation mode, bit 4 written to stack is changed to 0.

Table 3. Vector Locations

Name	Source	Emulation (E = 1)	Native (E = 0)	Priority Level
$\overline{ABORT}$	Hardware	00FFF8,9	00FFE8,9	2
BRK	Software	00FFFE,F	00FFE6,7	N/A
$\overline{COP}$	Software	00FFF4,5	00FFE4,5	N/A
$\overline{IRQ}$	Hardware	00FFFE,F	00FFEE,F	4
$\overline{NMI}$	Hardware	00FFFA,B	00FFEA,B	3
$\overline{RES}$	Hardware	00FFFC,D	00FFFC,D (1 → E)	1

Table 4. G65SC802 and G65SC816 Instruction Set—Alphabetical Sequence

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift One Bit Left, Memory or Accumulator
BCC*	Branch on Carry Clear (Pc = 0)
BCS*	Branch on Carry Set (Pc = 1)
BEQ	Branch if Equal (Pz = 1)
BIT	Bit Test
BMI	Branch if Result Minus (PN = 1)
BNE	Branch if Not Equal (Pz = 0)
BPL	Branch if Result Plus (PN = 0)
BRA	Branch Always
BRK	Force Break
BRL	Branch Always Long
BVC	Branch on Overflow Clear (Pv = 0)
BVS	Branch on Overflow Set (Pv = 1)
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP*	Compare Memory and Accumulator
COP	Coprocessor
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC*	Decrement Memory or Accumulator by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive OR" Memory with Accumulator
INC*	Increment Memory or Accumulator by One
INX	Increment Index X by One
INY	Increment Index Y by One
JML**	Jump Long
JMP	Jump to New Location
JSL**	Jump Subroutine Long
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
MVN	Block Move Negative
MVP	Block Move Positive
NOP	No Operation
ORA	"OR" Memory with Accumulator
PEA	Push Effective Absolute Address on Stack (or Push Immediate Data on Stack)
PEI	Push Effective Indirect Address on Stack (add one cycle if DL ≠ 0)
PER	Push Effective Program Counter Relative Address on Stack
PHA	Push Accumulator on Stack
PHB	Push Data Bank Register on Stack
PHD	Push Direct Register on Stack
PHK	Push Program Bank Register on Stack
PHP	Push Processor Status on Stack
PHX	Push Index X on Stack
PHY	Push Index Y on Stack
PLA	Pull Accumulator from Stack
PLB	Pull Data Bank Register from Stack
PLD	Pull Direct Register from Stack
PLP	Pull Processor Status from Stack
PLX	Pull Index X from Stack
PLY	Pull Index Y form Stack
REP	Reset Status Bits
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTL	Return from Subroutine Long
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
SEP	Set Processor Status Bits
STA	Store Accumulator in Memory
STP	Stop the Clock
STX	Store Index X in Memory
STY	Store Index Y in Memory
STZ	Store Zero in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TCD*	Transfer Accumulator to Direct Register
TCS*	Transfer Accumulator to Stack Pointer Register
TDC*	Transfer Direct Register to Accumulator
TRB	Test and Reset Bit
TSB	Test and Set Bit
TSC*	Transfer Stack Pointer Register to Accumulator
TSX	Transfer Stack Pointer Register to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer Register
TXY	Transfer Index X to Index Y
TYA	Transfer Index Y to Accumulator
TYX	Transfer Index Y to Index X
WAI	Wait for Interrupt
XBA*	Exchange AH and AL
XCE	Exchange Carry and Emulation Bits

***Common Mnemonic Aliases**

Mnemonic	Alias
BCC	BLT
BCS	BGE
CMP	CPA
DEC A	DEA
INC A	INA
TCD	TAD
TCS	TAS
TDC	TDA
TSC	TSA
XBA	SWA

**JSL should be recognized as equivalent to JSR when it is specified with long absolute addresses.

JML is equivalent to JMP with long addressing forced.

Table 5. Arithmetic and Logical Instructions

Addressing Mode

MNE-MONIC	M/X	OPERATION E=1 or E=0 and M/X=1	OPERATION E=0 and M/X=0	immed	accum	dir	dir,x	dir,y	(dir)	(dir,x)	(dir),y	[dir]	[dir],y	abs	abs,x	abs,y	abs1	abs1,x	d,s	(d,s),y	STATUS N V M X D I Z C	MNEMONIC
ADC	Pm	AL+B+Pc→AL	A+W+Pc→A	69		65	75		72	61	71	67	77	6D	7D	79	6F	7F	63	73	N V . . . . Z C	ADC
AND	Pm	AL∧B →AL	A∧W →A	29		25	35		32	21	31	27	37	2D	3D	39	2F	3F	23	33	N . . . . . Z .	AND
ASL (2)	Pm	Pc←B←0	Pc←W←0		0A	06	16							0E	1E						N . . . . . Z C	ASL
BIT (1)	Pm	AL∧B	A∧W	89		24	34							2C	3C						N V . . . . Z .	BIT
CMP	Pm	AL-B	A-W	C9		C5	D5		D2	C1	D1	C7	D7	CD	DD	D9	CF	DF	C3	D3	N . . . . . Z C	CMP
CPX	Px	XL-B	X-W	E0		E4								EC							N . . . . . Z C	CPX
CPY	Px	YL-B	Y-W	C0		C4								CC							N . . . . . Z C	CPY
DEC (2)	Pm	B-1→B	W-1→W		3A	C6	D6							CE	DE						N . . . . . Z .	DEC
EOR	Pm	AL⊻B→AL	A⊻W→A	49		45	55		52	41	51	47	57	4D	5D	59	4F	5F	43	53	N . . . . . Z .	EOR
INC (2)	Pm	B+1→B	W+1→W		1A	E6	F6							EE	FE						N . . . . . Z .	INC
LDA	Pm	B→AL	W→A	A9		A5	B5		B2	A1	B1	A7	B7	AD	BD	B9	AF	BF	A3	B3	N . . . . . Z .	LDA
LDX	Px	B→XL	W→X	A2		A6		B6						AE		BE					N . . . . . Z .	LDX
LDY	Px	B→YL	W→Y	A0		A4	B4							AC	BC						N . . . . . Z .	LDY
LSR (2)	Pm	0→B→Pc	0→W→Pc		4A	46	56							4E	5E						0 . . . . . Z C	LSR
ORA	Pm	ALVB→AL	AVW→A	09		05	15		12	01	11	07	17	0D	1D	19	0F	1F	03	13	N . . . . . Z .	ORA
ROL (2)	Pm	Pc←B←Pc	PC←W←Pc		2A	26	36							2E	3E						N . . . . . Z C	ROL
ROR (2)	Pm	PC→B→Pc	Pc→W→Pc		6A	66	76							6E	7E						N . . . . . Z C	ROR
SBC	Pm	AL-B-P̄c→AL	A-W-P̄c→A	E9		E5	F5		F2	E1	F1	E7	F7	ED	FD	F9	EF	FF	E3	F3	N V . . . . Z C	SBC
STA (7)	Pm	AL→B	A→W			85	95		92	81	91	87	97	8D	9D	99	8F	9F	83	93	. . . . .	STA
STX	Px	XL→B	X→W			86		96						8E							. . . . .	STX
STY	Px	YL→B	Y→W			84	94							8C							. . . . .	STY
STZ (7)	Pm	0→B	0→W			64	74							9C	9E						. . . . .	STZ
TRB (8)	Pm	A∧B→B	Ā∧W→W			14								1C							. . . . . Z .	TRB
TSB (8)	Pm	AVB→B	AVW→W			04								0C							. . . . . Z .	TSB
			← add one cycle if DL ≠ 0 →																			
Emulation (E=1) or Native (E=0) Mode, 8 bit (M/X=1)		cycles		2	2	3	4	4	5	6	5 (3)	6	6	4	4 (3)	4 (3)	5	5	4	7		
		bytes		2	1	2	2	2	2	2	2	2	2	3	3	3	4	4	2	2		
Native Mode (E=0), 16 bit (M/X=0)		cycles		3	2	4	5	5	6	7	6	7	7	5	5	5	6	5	5	8		
		bytes		3	1	2	2	2	2	2	2	2	2	3	3	3	4	4	2	2		

V	logical OR	B	byte per effective address
∧	logical AND	W	word per effective address
⊻	logical exclusive OR	r	relative offset
+	arithmetic addition	A	Accumulator, AL low half of Accumulator
-	arithmetic subtraction	X	Index Register, XL low half of X register
≠	not equal	Y	Index Register, YL low half of Y register
•	status bit not affected	Pc	carry bit
		M/X	effective mode bit in Status Register (Pm or Px)
		Ws	word per stack pointer
		Bs	byte per stack pointer

Notes:

1. BIT instruction does not affect N and V flags when using immediate addressing mode. When using other addressing modes, the N and V flags are respectively set to bits 7 and 6 or 15 and 14 of the addressed memory depending on mode (byte or word).
2. For all Read/Modify/Write instruction addressing modes except accumulator—
   Add 2 cycles for E=1 or E=0 and Pm=1 (8-bit mode).
   Add 3 cycles for E=0 and Pm=0 (16-bit mode).
3. Add one cycle when indexing across page boundary and E=1 except for STA and STZ instructions.
4. If E=1 then 1→SH and XL→SL. If E=0 then X→S regardless of Pm or Px.
5. Exchanges the carry (Pc) and E bits. Whenever the E bit is set the following registers and status bits are locked into the indicated state: XH=0, YH=0, SH=1, Pm=1, Px=1.
6. Add 1 cycle if branch is taken. In Emulation (E=1) mode only—add 1 cycle if the branch is taken and crosses a page boundary.
7. Add 1 cycle in Emulation mode (E=1) for (dir),y; abs,x; and abs,y addressing modes.
8. With TSB and TRB instruction, the Z flag is set or cleared by the result of A∧B or A∧W.
   For all Read/Modify/Write instruction addressing modes except accumulator—
   Add 2 cycles for E=1 or E=0 and Pm=1 (8-bit mode).
   Add 3 cycles for E=0 and Pm=0 (16-bit mode).

Table 6. Branch, Transfer, Push, Pull, and Implied Addressing Mode Instructions

Mnemonic	Bytes	M/X	Cycles	Operation 8 Bit	Cycles	Operation 16 Bit	Implied	Stack	Relative	Status N V M X D I Z C	Mnemonic
BCC (6)	2	—	2	PC+r→PC	2	PC+r→PC			90	. . . . .	BCC
BCS (6)	2	—	2	PC+r→PC	2	PC+r→PC			B0	. . . . .	BCS
BEQ (6)	2	—	2	PC+r→PC	2	PC+r→PC			F0	. . . . .	BEQ
BMI (6)	2	—	2	PC+r→PC	2	PC+r→PC			30	. . . . .	BMI
BNE (6)	2	—	2	PC+r→PC	2	PC+r→PC			D0	. . . . .	BNE
BPL (6)	2	—	2	PC+r→PC	2	PC+r→PC			10	. . . . .	BPL
BRA (6)	2	—	2	PC+r→PC	2	PC+r→PC			80	. . . . .	BRA
BVC (6)	2	—	2	PC+r→PC	2	PC+r→PC			50	. . . . .	BVC
BVS (6)	2	—	2	PC+r→PC	2	PC+r→PC			70	. . . . .	BVS
CLC	1	—	2	0→Pc	2	0→Pc	18			 0	CLC
CLD	1	—	2	0→Pd	2	0→Pd	D8			. . . . 0 . .	CLD
CLI	1	—	2	0→Pi	2	0→Pi	58			. . . . 0 . .	CLI
CLV	1	—	2	0→Pv	2	0→Pv	B8			. 0	CLV
DEX	1	Px	2	XL-1→XL	2	X-1→X	CA			N . . . . Z .	DEX
DEY	1	Px	2	YL-1→YL	2	Y-1→Y	88			N . . . . Z .	DEY
INX	1	Px	2	XL+1→XL	2	X+1→X	E8			N . . . . Z .	INX
INY	1	Px	2	YL+1→YL	2	Y+1→Y	C8			N . . . . Z .	INY
NOP	1	—	2	no operation	2	no operation	EA			. . . . .	NOP
PEA	3	—	5	W→Ws, S-2→S	5	same		F4		. . . . .	PEA
PEI	2	—	6	W→Ws, S-2→S	6	same		D4		. . . . .	PEI
PER	3	—	6	W→Ws, S-2→S	6	same		62		. . . . .	PER
PHA	1	Pm	3	AL→Bs, S-1→S	4	A→Ws, S-2→S		48		. . . . .	PHA
PHB	1	—	3	DB→Bs, S-1→S	3	same		8B		. . . . .	PHB
PHD	1	—	4	D→Ws, S-2→S	4	same		0B		. . . . .	PHD
PHK	1	—	3	PB→Bs, S-1→S	3	same		4B		. . . . .	PHK
PHP	1	—	3	P→Bs, S-1→S	3	same		08		. . . . .	PHP
PHX	1	Px	3	XL→Bs, S-1→S	4	X→Ws, S-2→S		DA		. . . . .	PHX
PHY	1	Px	3	YL→Bs, S-1→S	4	Y→Ws, S-2→S		5A		. . . . .	PHY
PLA	1	Pm	4	S+1→S, Bs→AL	5	S+2→S, Ws→A		68		N . . . . Z .	PLA
PLB	1	—	4	S+1→S, Bs→DB	4	same		AB		N . . . . Z .	PLB
PLD	1	—	5	S+2→S, Ws→D	5	same		2B		N . . . . Z .	PLD
PLP	1	—	4	S+1→S, Bs→P	4	same		28		N V M X D I Z C	PLP
PLX	1	Px	4	S+1→S, Bs→XL	5	S+2→S, Ws→X		FA		N . . . . Z .	PLX
PLY	1	Px	4	S+1→S, Bs→YL	5	S+2→S, Ws→Y		7A		N . . . . Z .	PLY
SEC	1	—	2	1→Pc	2	1→Pc	38			 1	SEC
SED	1	—	2	1→Pd	2	1→Pd	F8			. . . . 1 . .	SED
SEI	1	—	2	1→Pi	2	1→Pi	78			. . . . 1 . .	SEI
TAX	1	Px	2	AL→XL	2	A→X	AA			N . . . . Z .	TAX
TAY	1	Px	2	AL→YL	2	A→Y	A8			N . . . . Z .	TAY
TCD	1	—	2	A→D	2	A→D	5B			N . . . . Z .	TCD
TCS	1	—	2	A→S	2	A→S	1B			. . . . .	TCS
TDC	1	—	2	D→A	2	D→A	7B			N . . . . Z .	TDC
TSC	1	—	2	S→A	2	S→A	3B			N . . . . Z .	TSC
TSX	1	Px	2	SL→XL	2	S→X	BA			N . . . . Z .	TSX
TXA	1	Pm	2	XL→AL	2	X→A	8A			N . . . . Z .	TXA
TXS	1	—	2	see note 4	2	X→S	9A			. . . . .	TXS
TXY	1	Px	2	XL→YL	2	X→Y	9B			N . . . . Z .	TXY
TYA	1	Pm	2	YL→AL	2	Y→A	98			N . . . . Z .	TYA
TYX	1	Px	2	YL→XL	2	Y→X	BB			N . . . . Z .	TYX
XCE	1	—	2	see note 5	2	see note 5	FB			 C	XCE

See Notes on page 13.

Table 7. Other Addressing Mode Instructions

Mnemonic	Addressing Mode	Op Code	Cycles	Bytes	Status N V M X D I Z C	Mnemonic	Function
BRK	stack	00	7/8	2	. . . . 0 1 . .	BRK	See discussion in Interrupt Processing Sequence section.
BRL	relative long	82	3	3	. . . . .	BRL	PC+r→PC where -32768<r<32767.
COP	stack	02	7/8	2	. . . . 0 1 . .	COP	See discussion in Interrupt Processing Sequence section.
JML	absolute indirect	DC	6	3	. . . . .	JML	W→PC, B→PB
JMP	absolute	4C	3	3	. . . . .	JMP	W→PC
JMP	absolute indirect	6C	5	3	. . . . .	JMP	W→PC
JMP	absolute indexed indirect	7C	6	3	. . . . .	JMP	W→PC
JMP	absolute long	5C	4	4	. . . . .	JMP	W→PC, B→PB
JSL	absolute long	22	8	4	. . . . .	JSL	PB→Bs, S-1→S, PC→Ws, S-2→S, W→PC, B→PB
JSR	absolute	20	6	3	. . . . .	JSR	PC→Ws, S-2→S, W→PC
JSR	absolute indexed indirect	FC	6	3	. . . . .	JSR	PC→Ws, S-2→S, W→PC
MVN	block	54	7/byte	3	. . . . .	MVN	See discussion in Addressing Mode section
MVP	block	44	7/byte	3	. . . . .	MVP	
REP	immediate	C2	3	2	N V M X D I Z C	REP	P∧$\overline{B}$→P
RTI	stack	40	6/7	1	N V M X D I Z C	RTI	S+1→S, Bs→P, S+2→S, Ws→PC, if E=0 then S+1→S, Bs→PB
RTL	stack	6B	6	1	. . . . .	RTL	S+2→S, Ws+1→PC, S+1→S, Bs→PB
RTS	stack	60	6	1	. . . . .	RTS	S+2→S, Ws+1→PC
SEP	immediate	E2	3	2	N V M X D I Z C	SEP	PVB→P
STP	implied	DB	3 +	1	. . . . .	STP	Stop the clock. Requires reset to continue.
WAI	implied	CB	3 +	1	. . . . .	WAI	Wait for interrupt. RDY held low until interrupt.
XBA	implied	EB	3	1	N . . . . Z .	XBA	Swap AH and AL. Status bits reflect final condition of AL.

See Notes on page 13.

Table 8. Opcode Matrix

MSD	LSD 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK s 2 8	ORA (d,x) 2 6	COP s 2 8	ORA d,s 2 4	TSB d 2 5	ORA d 2 3	ASL d 2 5	ORA [d] 2 6	PHP s 1 3	ORA # 2 2	ASL A 1 2	PHD s 1 4	TSB a 3 6	ORA a 3 4	ASL a 3 6	ORA al 4 5	0
1	BPL r 2 2	ORA (d),y 2 5	ORA (d) 2 5	ORA (d,s),y 2 7	TRB d 2 5	ORA d,x 2 4	ASL d,x 2 6	ORA [d],y 2 6	CLC i 1 2	ORA a,y 3 4	INC A 1 2	TCS i 1 2	TRB a 3 6	ORA a,x 3 4	ASL a,x 3 7	ORA al,x 4 5	1
2	JSR a 3 6	AND (d,x) 2 6	JSL al 4 8	AND d,s 2 4	BIT d 2 3	AND d 2 3	ROL d 2 5	AND [d] 2 6	PLP s 1 4	AND # 2 2	ROL A 1 2	PLD s 1 5	BIT a 3 4	AND a 3 4	ROL a 3 6	AND al 4 5	2
3	BMI r 2 2	AND (d),y 2 5	AND (d) 2 5	AND (d,s),y 2 7	BIT d,x 2 4	AND d,x 2 4	ROL d,x 2 6	AND [d],y 2 6	SEC i 1 2	AND a,y 3 4	DEC A 1 2	TSC i 1 2	BIT a,x 3 4	AND a,x 3 4	ROL a,x 3 7	AND al,x 4 5	3
4	RTI s 1 7	EOR (d,x) 2 6	reserve 2 2	EOR d,s 2 4	MVP xya 3 7	EOR d 2 3	LSR d 2 5	EOR [d] 2 6	PHA s 1 3	EOR # 2 2	LSR A 1 2	PHK s 1 3	JMP a 3 3	EOR a 3 4	LSR a 3 6	EOR al 4 5	4
5	BVC r 2 2	EOR (d),y 2 5	EOR (d) 2 5	EOR (d,s),y 2 7	MVN xya 3 7	EOR d,x 2 4	LSR d,x 2 6	EOR [d],y 2 6	CLI i 1 2	EOR a,y 3 4	PHY s 1 3	TCD i 1 2	JMP al 4 4	EOR a,x 3 4	LSR a,x 3 7	EOR al,x 4 5	5
6	RTS s 1 6	ADC (d,x) 2 6	PER s 3 6	ADC d,s 2 4	STZ d 2 3	ADC d 2 3	ROR d 2 5	ADC [d] 2 6	PLA s 1 4	ADC # 2 2	ROR A 1 2	RTL s 1 6	JMP (a) 3 5	ADC a 3 4	ROR a 3 6	ADC al 4 5	6
7	BVS r 2 2	ADC (d),y 2 5	ADC (d) 2 5	ADC (d,s),y 2 7	STZ d,x 2 4	ADC d,x 2 4	ROR d,x 2 6	ADC [d],y 2 6	SEI i 1 2	ADC a,y 3 4	PLY s 1 4	TDC i 1 2	JMP (a,x) 3 6	ADC a,x 3 4	ROR a,x 3 7	ADC al,x 4 5	7
8	BRA r 2 2	STA (d,x) 2 6	BRL rl 3 3	STA d,s 2 4	STY d 2 3	STA d 2 3	STX d 2 3	STA [d] 2 6	DEY i 1 2	BIT # 2 2	TXA i 1 2	PHB s 1 3	STY a 3 4	STA a 3 4	STX a 3 4	STA al 4 5	8
9	BCC r 2 2	STA (d),y 2 6	STA (d) 2 5	STA (d,s),y 2 7	STY d,x 2 4	STA d,x 2 4	STX d,y 2 4	STA [d],y 2 6	TYA i 1 2	STA a,y 3 5	TXS i 1 2	TXY i 1 2	STZ a 3 4	STA a,x 3 5	STZ a,x 3 5	STA al,x 4 5	9
A	LDY # 2 2	LDA (d,x) 2 6	LDX # 2 2	LDA d,s 2 4	LDY d 2 3	LDA d 2 3	LDX d 2 3	LDA [d] 2 6	TAY i 1 2	LDA # 2 2	TAX i 1 2	PLB s 1 4	LDY a 3 4	LDA a 3 4	LDX a 3 4	LDA al 4 5	A
B	BCS r 2 2	LDA (d),y 2 5	LDA (d) 2 5	LDA (d,s),y 2 7	LDY d,x 2 4	LDA d,x 2 4	LDX d,y 2 4	LDA [d],y 2 6	CLV i 1 2	LDA a,y 3 4	TSX i 1 2	TYX i 1 2	LDY a,x 3 4	LDA a,x 3 4	LDX a,y 3 4	LDA al,x 4 5	B
C	CPY # 2 2	CMP (d,x) 2 6	REP # 2 3	CMP d,s 2 4	CPY d 2 3	CMP d 2 3	DEC d 2 5	CMP [d] 2 6	INY i 1 2	CMP # 2 2	DEX i 1 2	WAI i 1 3	CPY a 3 4	CMP a 3 4	DEC a 3 6	CMP al 4 5	C
D	BNE r 2 2	CMP (d),y 2 5	CMP (d) 2 5	CMP (d,s),y 2 7	PEI s 2 6	CMP d,x 2 4	DEC d,x 2 6	CMP [d],y 2 6	CLD i 1 2	CMP a,y 3 4	PHX s 1 3	STP i 1 3	JML (a) 3 6	CMP a,x 3 4	DEC a,x 3 7	CMP al,x 4 5	D
E	CPX # 2 2	SBC (d,x) 2 6	SEP # 2 3	SBC d,s 2 4	CPX d 2 3	SBC d 2 3	INC d 2 5	SBC [d] 2 6	INX i 1 2	SBC # 2 2	NOP i 1 2	XBA i 1 3	CPX a 3 4	SBC a 3 4	INC a 3 6	SBC al 4 5	E
F	BEQ r 2 2	SBC (d),y 2 5	SBC (d) 2 5	SBC (d,s),y 2 7	PEA s 3 5	SBC d,x 2 4	INC d,x 2 6	SBC [d],y 2 6	SED i 1 2	SBC a,y 3 4	PLX s 1 4	XCE i 1 2	JSR (a,x) 3 6	SBC a,x 3 4	INC a,x 3 7	SBC al,x 4 5	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

symbol	addressing mode	symbol	addressing mode
#	immediate	[d]	direct indirect long
A	accumulator	[d],y	direct indirect indexed long
r	program counter relative	a	absolute
rl	program counter relative long	a,x	absolute indexed (with x)
i	implied	a,y	absolute indexed (with y)
s	stack	al	absolute long
d	direct	al,x	absolute indexed long
d,x	direct indexed (with x)	d,s	stack relative
d,y	direct indexed (with y)	(d,s),y	stack relative indirect indexed
(d)	direct indirect	(a)	absolute indirect
(d,x)	direct indexed indirect	(a,x)	absolute indexed indirect
(d),y	direct indirect indexed	xya	block move

legend	
instruction mnemonic	addressing mode
base number of bytes	base number of cycles

Table 9. Detailed Instruction Operation

	ADDRESS MODE		CYCLE	$\overline{VP}$	$\overline{ML}$	VDA	VPA	ADDRESS BUS	DATA BUS	R/$\overline{W}$
1.	Immediate—#		1.	1	1	1	1	PBR,PC	Op Code	1
	(LDY,CPY,CPX,LDX,ORA,		2.	1	1	0	1	PBR,PC+1	IDL	1
	AND,EOR,ADC,BIT,LDA,	(1)(8)	2a.	1	1	0	1	PBR,PC+2	IDH	1
	CMP,SBC REP,SEP)									
	(14 Op Codes)									
	(2 and 3 bytes)									
	(2 and 3 cycles)									
2a.	Absolute—a		1.	1	1	1	1	PBR,PC	Op Code	1
	(BIT,STY,STZ,LDY,		2.	1	1	0	1	PBR,PC+1	AAL	1
	CPY,CPX,STX,LDX,		3.	1	1	0	1	PBR,PC+2	AAH	1
	ORA,AND,EOR,ADC,		4.	1	1	1	0	DBR,AA	Data Low	1/0
	STA,LDA,CMP,SBC)	(1)	4a.	1	1	1	0	DBR,AA+1	Data High	1/0
	(16 Op Codes)									
	(3 bytes)									
	(4 and 5 cycles)									
2b.	Absolute (R-M-W)—a		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	AAL	1
	(ASL,ROL,LSR,ROR		3.	1	1	0	1	PBR,PC+2	AAH	1
	DEC,INC,TSB,TRB)		4.	1	0	1	0	DBR,AA	Data Low	1
	(8 Op Codes)	(1)	4a.	1	0	1	0	DBR,AA+1	Data High	1
	(3 bytes)	(3)	5.	1	0	0	0	DBR,AA+1	IO	1
	(6 and 8 cycles)	(1)	6a.	1	0	1	0	DBR,AA+1	Data High	0
			6.	1	0	1	0	DBR,AA	Data Low	0
2c.	Absolute (JUMP)—a		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)(4C)		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
	(3 bytes)		1.	1	1	1	1	PBR, NEW PC	New Op Code	1
	(3 cycles)									
2d.	Absolute (Jump to		1.	1	1	1	1	PBR,PC	Op Code	1
	subroutine)—a		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
	(JSR)		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
	(1 Op Code)		4.	1	1	0	0	PBR,PC+2	IO	1
	(3 bytes)		5.	1	1	1	0	0,S	PCH	0
	(6 cycles)		6.	1	1	1	0	0,S-1	PCL	0
	(different order from N6502)		1.	1	1	1	1	PBR,NEW PC	New Op Code	1
★3a.	Absolute Long—al		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC		2.	1	1	0	1	PBR,PC+1	AAL	1
	STA,LDA,CMP,SBC)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(8 Op Codes)		4.	1	1	0	1	PBR,PC+3	AAB	1
	(4 bytes)		5.	1	1	1	0	AAB,AA	Data Low	1/0
	(5 and 6 cycles)	(1)	5a.	1	1	1	0	AAB,AA+1	Data High	1/0
★3b.	Absolute Long (JUMP)—al		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
	(4 bytes)		4.	1	1	0	1	PBR,PC+3	NEW BR	1
	(4 cycles)		1.	1	1	1	1	NEW PBR,PC	New Op Code	1
★3c.	Absolute Long (Jump to		1.	1	1	1	1	PBR,PC	Op Code	1
	Subroutine Long)—al		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
	(JSL)		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
	(1 Op Code)		4.	1	1	1	0	0,S	PBR	0
	(4 bytes)		5.	1	1	0	0	0,S	IO	1
	(7 cycles)		6.	1	1	0	1	PBR,PC+3	NEW PBR	1
			7.	1	1	1	0	0,S-1	PCH	0
			8.	1	1	1	0	0,S-2	PCL	0
			1.	1	1	1	1	NEW PBR,PC	New Op Code	1
4a.	Direct—d		1.	1	1	1	1	PBR,PC	Op Code	1
	(BIT,STZ,STY,LDY,		2.	1	1	0	1	PBR,PC+1	DO	1
	CPY,CPX,STX,LDX,	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	ORA,AND,EOR,ADC,		3.	1	1	1	0	0,D+DO	Data Low	1/0
	STA,LDA,CMP,SBC)	(1)	3a.	1	1	1	0	0,D+DO+1	Data High	1/0
	(16 Op Codes)									
	(2 bytes)									
	(3,4 and 5 cycles)									
4b.	Direct (R-M-W)—d		1.	1	1	1	1	PBR,PC	Op Code	1
	(ASL,ROL,LSR,ROR		2.	1	1	0	1	PBR,PC+1	DO	1
	DEC,INC,TSB,TRB)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	0	1	0	0,D+DO	Data Low	1
	(2 bytes)	(1)	3a.	1	0	1	0	0,D+DO+1	Data High	1
	(5,6,7 and 8 cycles)	(3)	4.	1	0	0	0	0,D+DO+1	IO	1
		(1)	5a.	1	0	1	0	0,D+DO+1	Data High	0
			5.	1	0	1	0	0,D+DO	Data Low	0
5.	Accumulator—A		1.	1	1	1	1	PBR,PC	Op Code	1
	(ASL,INC,ROL,DEC,LSR,ROR)		2.	1	1	0	0	PBR,PC+1	IO	1
	(6 Op Codes)									
	(1 byte)									
	(2 cycles)									
6a.	Implied—i		1.	1	1	1	1	PBR,PC	Op Code	1
	(DEY, INY, INX, DEX, NOP,		2.	1	1	0	0	PBR,PC+1	IO	1
	XCE, TYA, TAY,TXA, TXS,									
	TAX,TSX,TCS,TSC,TCD,									
	TDC,TXY,TYX,CLC,SEC,									
	CLI,SEI,CLV,CLD,SED)									
	(25 Op Codes)									
	(1 byte)									
	(2 cycles)									
★6b.	Implied—i		1.	1	1	1	1	PBR,PC	Op Code	1
	(XBA)		2.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		3.	1	1	0	0	PBR,PC+1	IO	1
	(1 byte)									
	(3 cycles)									
								RDY		
● 6c.	Wait For Interrupt									
	(WAI)		1.	1	1	1	1	PBR,PC	Op Code	1
	(1 Op Code)	(9)	2	1	1	0	0	PBR,PC+1	IO	1
	(1 byte)		3.	1	1	0	0	PBR,PC+1	IO	1
	(3 cycles) $\overline{IRQ,NMI}$		1.	1	1	1	1	PBR,PC+1	IRQ(BRK)	1
● 6d.	Stop-The-Clock									
	(STP)		1.	1	1	1	1	PBR,PC	Op Code	1
	(1 Op Code)		2.	1	1	0	0	PBR,PC+1	IO	1
	(1 byte) $\overline{RES}$=1		3.	1	1	0	0	PBR,PC+1	IO	1
	(3 cycles) $\overline{RES}$=0		1c.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
	$\overline{RES}$=0		1b.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
	$\overline{RES}$=1		1a.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
	See 21a Stack		1.	1	1	1	1	1	PBR,PC+1	BEGIN	1
	(Hardware interrupt)									

	ADDRESS MODE		CYCLE	$\overline{VP}$	$\overline{ML}$	VDA	VPA	ADDRESS BUS	DATA BUS	R/$\overline{W}$
7.	Direct Indirect Indexed—(d),y		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(5,6,7 and 8 cycles)	(4)	4a.	1	1	0	0	DBR,AAH,AAL+	YL IO	1
			5.	1	1	1	0	DBR,AA+Y	Data Low	1/0
		(1)	5a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
8.	Direct Indirect		1.	1	1	1	1	PBR,PC	Op Code	1
	Indexed Long—[d],y		2.	1	1	0	1	PBR,PC+1	DO	1
	(ORA,AND,EOR,ADC,	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	STA,LDA,CMP,SBC)		3.	1	1	1	0	0,D+DO	AAL	1
	(8 Op Codes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(2 bytes)		5.	1	1	1	0	0,D+DO+2	AAB	1
	(6,7 and 8 cycles)		6.	1	1	1	0	AAB,AA+Y	Data Low	1/0
		(1)	6a.	1	1	1	0	AAB,AA+Y+1	Data High	1/0
9.	Direct Indexed Indirect—(d,x)		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	0	0	PBR,PC+1	IO	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+X	AAL	1
	(6,7 and 8 cycles)		5.	1	1	1	0	0,D+DO+X+1	AAH	1
			6.	1	1	1	0	DBR,AA	Data Low	1/0
		(1)	6a.	1	1	1	0	DBR,AA+1	Data High	1/0
10a.	Direct,X—d,x		1.	1	1	1	1	PBR,PC	Op Code	1
	(BIT,STZ,STY,LDY,		2.	1	1	0	1	PBR,PC+1	DO	1
	ORA,AND,EOR,ADC,	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	STA,LDA,CMP,SBC)		3.	1	1	0	0	PBR,PC+1	IO	1
	(12 Op Codes)		4.	1	1	1	0	0,D+DO+X	Data Low	1/0
	(2 bytes)	(1)	4a.	1	1	1	0	0,D+DO+X+1	Data High	1/0
	(4,5 and 6 cycles)									
10b.	Direct,X (R-M-W)—d,x		1.	1	1	1	1	PBR,PC	Op Code	1
	(ASL,ROL,LSR,ROR,		2.	1	1	0	1	PBR,PC+1	DO	1
	DEC,INC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(6 Op Codes)		3.	1	1	0	0	PBR,PC+1	IO	1
	(2 bytes)		4.	1	0	1	0	0,D+DO+X	Data Low	1
	(6,7,8 and 9 cycles)	(1)	4a.	1	0	1	0	0,D+DO+X+1	Data High	1
		(3)	5.	1	0	0	0	0,D+DO+X+1	IO	1
		(1)	6a.	1	0	1	0	0,D+DO+X+1	Data High	0
			6.	1	0	1	0	0,D+DO+X	Data Low	0
11.	Direct, Y—d,y		1.	1	1	1	1	PBR,PC	Op Code	1
	(STX,LDX)		2.	1	1	0	1	PBR,PC+1	DO	1
	(2 Op Codes)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(2 bytes)		3.	1	1	0	0	PBR,PC+1	IO	1
	(4,5 and 6 cycles)		4.	1	1	1	0	0,D+DO+Y	Data Low	1/0
		(1)	4a.	1	1	1	0	0,D+DO+Y+1	Data High	1/0
12a.	Absolute,X—a,x		1.	1	1	1	1	PBR,PC	Op Code	1
	(BIT,LDY,STZ,		2.	1	1	0	1	PBR,PC+1	AAL	1
	ORA,AND,EOR,ADC,		3.	1	1	0	1	PBR,PC+2	AAH	1
	STA,LDA,CMP,SBC)	(4)	3a.	1	1	0	0	DBR,AAH,AAL+	XL IO	1
	(11 Op Codes)		4.	1	1	1	0	DBR,AA+X	Data Low	1/0
	(3 bytes)	(1)	4a.	1	1	1	0	DBR,AA+X+1	Data High	1/0
	(4,5 and 6 cycles)									
12b.	Absolute,X (R-M-W)—a,x		1.	1	1	1	1	PBR,PC	Op Code	1
	(ASL,ROL,LSR,ROR,		2.	1	1	0	1	PBR,PC+1	AAL	1
	DEC,INC)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(6 Op Codes)		4.	1	1	0	0	DBR,AAH,AAL+	XL IO	1
	(3 bytes)		5.	1	0	1	0	DBR,AA+X	Data Low	1
	(7 and 9 cycles)	(1)	5a.	1	0	1	0	DBR,AA+X+1	Data High	1
		(3)	6.	1	0	0	0	DBR,AA+X+1	IO	1
		(1)	7a.	1	0	1	0	DBR,AA+X+1	Data High	0
			7.	1	0	1	0	DBR,AA+X	Data Low	0
★13.	Absolute Long,X—al,x		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	AAL	1
	STA,LDA,CMP,SBC)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(8 Op Codes)		4.	1	1	0	1	PBR,PC+3	AAB	1
	(4 bytes)		5.	1	1	1	0	AAB,AA+X	Data Low	1/0
	(5 and 6 cycles)	(1)	5a.	1	1	1	0	AAB,AA+X+1	Data High	1/0
14.	Absolute,Y—a,y		1.	1	1	1	1	PBR,PC	Op Code	1
	(LDX,ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	AAL	1
	STA,LDA,CMP,SBC)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(9 Op Codes)	(4)	3a.	1	1	0	0	DBR,AAH,AAL+	YL IO	1
	(3 bytes)		4.	1	1	1	0	DBR,AA+Y	Data Low	1/0
	(4,5 and 6 cycles)	(1)	4a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
15.	Relative—r		1.	1	1	1	1	PBR,PC	Op Code	1
	(BPL,BMI,BVC,BVS,BCC,		2.	1	1	0	1	PBR,PC+1	Offset	1
	BCS,BNE,BEQ,BRA)	(5)	2a.	1	1	0	0	PBR,PC+2	IO	1
	(9 Op Codes)	(6)	2b.	1	1	0	0	PBR,PC+2+OFF	IO	1
	(2 bytes)		1.	1	1	1	1	PBR,New PC	New Op Code	1
	(2,3 and 4 cycles)									
★16.	Relative Long—ri		1.	1	1	1	1	PBR,PC	Op Code	1
	(BRL)		2.	1	1	0	1	PBR,PC+1	Offset Low	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	Offset High	1
	(3 bytes)		4.	1	1	0	0	PBR,PC+2	IO	1
	(4 cycles)		1.	1	1	1	1	PBR,New PC	New Op Code	1
17a.	Absolute Indirect—(a)		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)		2.	1	1	0	1	PBR,PC+1	AAL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		4.	1	1	1	0	0,AA	NEW PCL	1
	(5 cycles)		5.	1	1	1	0	0,AA+1	NEW PCH	1
			1.	1	1	1	1	PBR,NEW PC	Op Code	1
★17b.	Absolute Indirect—(a)		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	AAL	1
	(JML)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(1 Op Code)		4.	1	1	1	0	0,AA	NEW PCL	1
	(3 bytes)		5.	1	1	1	0	0,AA+1	NEW PCH	1
	(6 cycles)		6.	1	1	1	0	0,AA+2	NEW PBR	1
			1.	1	1	1	1	NEW PBR,PC	New Op Code	1
● 18.	Direct Indirect —(d)		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(5,6 and 7 cycles)		5.	1	1	1	0	DBR,AA	Data Low	1/0
		(1)	5a.	1	1	1	0	DBR,AA+1	Data Low	1/0

Table 9. Detailed Instruction Operation (continued)

	ADDRESS MODE		CYCLE	VP	ML	VDA	VPA	ADDRESS BUS	DATA BUS	R/W
*19.	Direct Indirect Long —[d]		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(6,7 and 8 cycles)		5.	1	1	1	0	0,D+DO+2	AAB	1
			6.	1	1	1	0	AAB,AA	Data Low	1/0
		(1)	6a.	1	1	1	0	AAB,AA+1	Data High	1/0
20a.	Absolute Indexed Indirect —(a,x)		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)		2.	1	1	0	1	PBR,PC+1	AAL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		4.	1	1	1	0	PBR,PC+2	IO	1
	(6 cycles)		5.	1	1	0	1	PBR,AA+X	NEW PCL	1
			6.	1	1	0	1	PBR,AA+X+1	NEW PCH	1
			1.	1	1	1	1	PBR, NEW PC	New Op Code	1
*20b.	Absolute Indexed Indirect		1.	1	1	1	1	PBR,PC	Op Code	1
	(Jump to Subroutine Indexed		2.	1	1	0	1	PBR,PC+1	AAL	1
	Indirect) —(a,x)		3.	1	1	1	0	0,S	PCH	0
	(JSR)		4.	1	1	1	0	0,S-1	PCL	0
	(1 Op Code)		5.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		6.	1	1	0	0	PBR,PC+2	IO	1
	(8 cycles)		7.	1	1	0	1	PBR,AA+X	NEW PCL	1
			8.	1	1	0	1	PBR,AA+X+1	NEW PCH	1
			1.	1	1	1	1	PBR,NEW PC	New Op Code	1
21a.	Stack (Hardware		1.	1	1	1	1	PBR,PC	IO	1
	Interrupts) —s	(3)	2.	1	1	0	0	PBR,PC	IO	1
	(IRQ,NMI,ABORT,RES)	(7)	3.	1	1	1	0	0,S	PBR	0
	(4 hardware interrupts)	(10)	4.	1	1	1	0	0,S-1	PCH	0
	(0 bytes)	(10)	5.	1	1	1	0	0,S-2	PCL	0
	(7 and 8 cycles)	/10)(11)	6.	1	1	1	0	0,S-3	P	0
			7.	0	1	1	0	0,VA	AAVL	1
			8.	0	1	1	0	0,VA+1	AAVH	1
			1.	1	1	1	1	0,AAV	New Op Code	1
21b.	Stack (Software		1.	1	1	1	1	PBR,PC	Op Code	1
	Interrupts) —s	(3)	2.	1	1	0	1	PBR,PC+1	Signature	1
	(BRK,COP)	(7)	3.	1	1	1	0	0,S	PBR	0
	(2 Op Codes)		4.	1	1	1	0	0,S-1	PCH	0
	(2 bytes)		5.	1	1	1	0	0,S-2	PCL	0
	(7 and 8 cycles)		6.	1	1	1	0	0,S-3 (COP Latches)	P	0
			7.	0	1	1	0	0,VA	AAVL	1
			8.	0	1	1	0	0,VA+1	AAVH	1
			1.	1	1	1	1	0,AAV	New Op Code	1
21c.	Stack (Return from		1.	1	1	1	1	PBR,PC	Op Code	1
	Interrupt) —s		2.	1	1	0	0	PBR,PC+1	IO	1
	(RTI)	(3)	3.	1	1	1	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	P	1
	(1 byte)		5.	1	1	1	0	0,S+2	New PCL	1
	(6 and 7 cycles)		6.	1	1	1	0	0,S+3	New PCH	1
	(different order from N6502)	(7)	7.	1	1	1	0	0,S+4	PBR	1
			1.	1	1	1	1	PBR,New PC	New Op Code	1
21d.	Stack (Return from		1.	1	1	1	1	PBR,PC	Op Code	1
	Subroutine) —s		2.	1	1	0	0	PBR,PC+1	IO	1
	(RTS)		3.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	New PCL-1	1
	(1 byte)		5.	1	1	1	0	0,S+2	New PCH	1
	(6 cycles)		6.	1	1	0	0	0,S+2	IO	1
			1.	1	1	1	1	PBR,New PC	New Op Code	1
*21e.	Stack (Return from		1.	1	1	1	1	PBR,PC	Op Code	1
	Subroutine Long) —s		2.	1	1	0	0	PBR,PC+1	IO	1
	(RTL)		3.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	NEW PCL	1
	(1 byte)		5.	1	1	1	0	0,S+2	NEW PCH	1
	(6 cycles)		6.	1	1	1	0	0,S+3	NEW PBR	1
			1.	1	1	1	1	NEW PBR,PC	New Op Code	1
21f.	Stack (Push) —s		1.	1	1	1	1	PBR,PC	Op Code	1
	(PHP,PHA,PHY,PHX,		2.	1	1	0	0	PBR,PC+1	IO	1
	PHD,PHK,PHB)	(1)	3a.	1	1	1	0	0,S	Register High	0
	(7 Op Codes)		3.	1	1	1	0	0,S-1	Register Low	0
	(1 byte)									
	(3 and 4 cycles)									
21g.	Stack (Pull) —s		1.	1	1	1	1	PBR,PC	Op Code	1
	(PLP,PLA,PLY,PLX,PLD,PLB)		2.	1	1	0	0	PBR,PC+1	IO	1
	(Different than N6502)		3.	1	1	0	0	PBR,PC+1	IO	1
	(6 Op Codes)		4.	1	1	1	0	0,S+1	Register Low	1
	(1 byte)	(1)	4a.	1	1	1	0	0,S+2	Register High	1
	(4 and 5 cycles)									
*21h.	Stack (Push Effective		1.	1	1	1	1	PBR,PC	Op Code	1
	Indirect Address) —s		2.	1	1	0	1	PBR,PC+1	DO	1
	(PEI)	(2)	2a	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(6 and 7 cycles)		5.	1	1	1	0	0,S	AAH	0
			6.	1	1	1	0	0,S-1	AAL	0
*21i.	Stack (Push Effective		1.	1	1	1	1	PBR,PC	Op Code	1
	Absolute Address) —s		2.	1	1	0	1	PBR,PC+1	AAL	1
	(PEA)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(1 Op Code)		4.	1	1	1	0	0,S	AAH	0
	(3 bytes)		5.	1	1	1	0	0,S-1	AAL	0
	(5 cycles)									
*21j.	Stack (Push Effective		1.	1	1	1	1	PBR,PC	Op Code	1
	Program Counter Relative		2.	1	1	0	1	PBR,PC+1	Offset Low	1
	Address) —s		3.	1	1	0	1	PBR,PC+2	Offset High	1
	(PER)		4.	1	1	0	0	PBR,PC+2	IO	1
	(1 Op Code)		5.	1	1	1	0	0,S	PCH + Offset	0
	(3 bytes)								+ CARRY	
	(6 cycles)		6.	1	1	1	0	0,S-1	PCL, + Offset	0
*22.	Stack Relative —d,s		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADL,		2.	1	1	0	1	PBR,PC+1	SO	1
	STA,LDA,CMP,SBC)		3.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		4.	1	1	1	0	0,S+SO	Data Low	1/0
	(2 bytes)	(1)	4a.	1	1	1	0	0,S+SO+1	Data High	1/0
	(4 and 5 cycles)									

	ADDRESS MODE		CYCLE	VP	ML	VDA	VPA	ADDRESS BUS	DATA BUS	R/W
*23.	Stack Relative Indirect		1.	1	1	1	1	PBR,PC	Op Code	1
	Indexed —(d,s),y		2.	1	1	0	1	PBR,PC+1	SO	1
	(ORA,AND,EOR,ADC,		3.	1	1	0	0	PBR+PC+1	IO	1
	STA,LDA,CMP,SBC)		4.	1	1	1	0	0,S+SO	AAL	1
	(8 Op Codes)		5.	1	1	1	0	0,S+SO+1	AAH	1
	(2 bytes)		6.	1	1	0	0	0,S+SO+1	IO	1
	(7 and 8 Cycles)		7.	1	1	1	0	DBR,AA+Y	Data Low	1/0
		(1)	7a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
*24a.	Block Move Positive		1.	1	1	1	1	PBR,PC	Op Code	1
	(forward) —xyc		2.	1	1	0	1	PBR,PC+1	DBA	1
	(MVP)		3.	1	1	0	1	PBR,PC+2	SBA	1
	(1 Op Code)	N-2	4.	1	1	1	0	SBA,X	Source Data	1
	(3 bytes)	Byte	5.	1	1	1	0	DBA,Y	Dest. Data	0
	(7 cycles)	C=2	6.	1	1	0	0	DBA,Y	IO	1
	x = Source Address		7.	1	1	0	0	DBA,Y	IO	1
	y = Destination		1.	1	1	1	1	PBR,PC	Op Code	1
	c = Number of Bytes to Move -1		2.	1	1	0	1	PBR,PC+1	DBA	1
	x,y Decrement		3.	1	1	0	1	PBR,PC+2	SBA	1
	MVP is used when the	N-1	4.	1	1	1	0	SBA,X-1	Source Data	1
	destination start address	Byte	5.	1	1	1	0	DBA,Y-1	Dest. Data	0
	is higher (more positive)	C=1	6.	1	1	0	0	DBA,Y-1	IO	1
	than the source start address.		7.	1	1	0	0	DBA,Y-1	IO	1
	FFFFFF		1.	1	1	1	1	PBR,PC	Op Code	1
	Dest. Start	N Byte	2.	1	1	0	1	PBR,PC+1	DBA	1
	Source Start	Last	3.	1	1	0	1	PBR,PC+2	SBA	1
	Dest. End	C=0	4.	1	1	1	0	SBA,X-2	Source Data	1
	Source End		5.	1	1	1	0	DBA,Y-2	Dest. Data	0
	000000		6.	1	1	0	0	DBA,Y-2	IO	1
			7.	1	1	0	0	DBA,Y-2	IO	1
			1.	1	1	1	1	PBR,PC+3	New Op Code	1
*24b.	Block Move Negative		1.	1	1	1	1	PBR,PC	Op Code	1
	(backward) —xyc		2.	1	1	0	1	PBR,PC+1	DBA	1
	(MVN)	N-2	3.	1	1	0	1	PBR,PC+2	SBA	1
	(1 Op Code)	Byte	4.	1	1	1	0	SBA,X	Source Data	1
	(3 bytes)	C=2	5.	1	1	1	0	DBA,Y	Dest. Data	0
	(7 cycles)		6.	1	1	0	0	DBA,Y	IO	1
	x = Source Address		7.	1	1	0	0	DBA,Y	IO	1
	y = Destination		1.	1	1	1	1	PBR,PC	Op Code	1
	c = Number of Bytes to Move -1		2.	1	1	0	1	PBR,PC+1	DBA	1
	x,y Increment		3.	1	1	0	1	PBR,PC+2	SBA	1
	FFFFFF	N-1	4.	1	1	1	0	SBA,X+1	Source Data	1
	Source End	Byte	5.	1	1	1	0	DBA,Y+1	Dest. Data	0
	Dest.End	C=1	6.	1	1	0	0	DBA,Y+1	IO	1
	Source Start		7.	1	1	0	0	DBA,Y+1	IO	1
	Dest. Start		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
		N Byte	3.	1	1	0	1	PBR,PC+2	SBA	1
	000000	C=0	4.	1	1	1	0	SBA,X+2	Source Data	1
	MVN is used when the		5.	1	1	1	0	DBA,Y+2	Dest. Data	0
	destination start address		6.	1	1	0	0	DBA,Y+2	IO	1
	is lower (more negative)		7.	1	1	0	0	DBA,Y+2	IO	1
	than the source start		1.	1	1	1	1	PBR,PC+3	New Op Code	1
	address.									

Notes:

(1) Add 1 byte (for immediate only) for M=0 or X=0 (i.e. 16 bit data), add 1 cycle for M=0 or X=0.

(2) Add 1 cycle for direct register low (DL) not equal 0.

(3) Special case for aborting instruction. This is the last cycle which may be aborted or the Status, PBR or DBR registers will be updated.

(4) Add 1 cycle for indexing across page boundaries, or write, or X=0. When X=1 or in the emulation mode, this cycle contains invalid addresses.

(5) Add 1 cycle if branch is taken.

(6) Add 1 cycle if branch is taken across page boundaries in 6502 emulation mode (E=1)

(7) Subtract 1 cycle for 6502 emulation mode (E=1)

(8) Add 1 cycle for REP,SEP.

(9) Wait at cycle 2 for 2 cycles after $\overline{NMI}$ or $\overline{IRQ}$ active input.

(10) R/$\overline{W}$ remains high during Reset.

(11) BRK bit 4 equals "0" in Emulation mode.

Abbreviations:

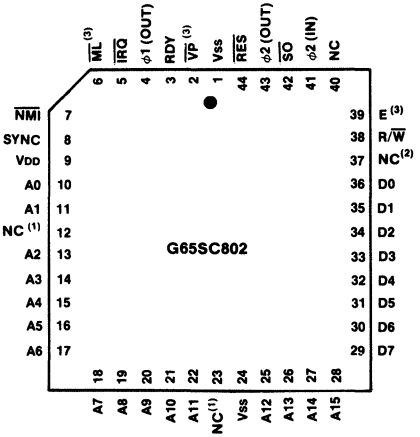
AAB Absolute Address Bank
AAH Absolute Address High
AAL Absolute Address Low
AAVH Absolute Address Vector High
AAVL Absolute Address Vector Low
C Accumulator
D Direct Register
DBA Destination Bank Address
DBR Data Bank Register
DO Direct Offset
IDH Immediate Data High
IDL Immediate Data Low
IO Internal Operation
P Status Register
PBR Program Bank Register
PC Program Counter
R-M-W Read-Modify-Write
S Stack Address
SBA Source Bank Address
SO Stack Offset
VA Vector Address
x,y Index Registers
* = New G65SC816/802 Addressing Modes
• = New G65SC02 Addressing Modes
Blank = NMOS 6502 Addressing Modes

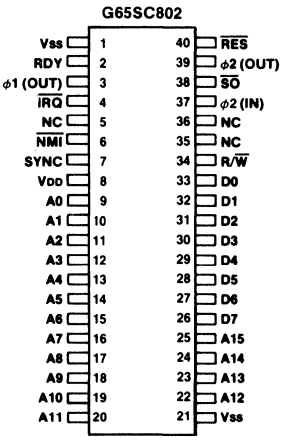
Pin Function Table

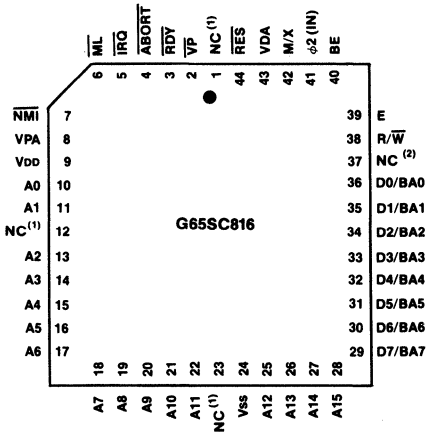
Pin	Description
A0-A15	Address Bus
$\overline{ABORT}$	Abort Input
BE	Bus Enable
ϕ2 (IN)	Phase 2 In Clock
ϕ1 (OUT)	Phase 1 Out Clock
ϕ2 (OUT)	Phase 2 Out Clock
D0-D7	Data Bus (G65SC802)
D0/BA0-D7/BA7	Data Bus, Multiplexed (G65SC816)
E	Emulation Select
$\overline{IRQ}$	Interrupt Request
$\overline{ML}$	Memory Lock
M/X	Mode Select (PM or Px)

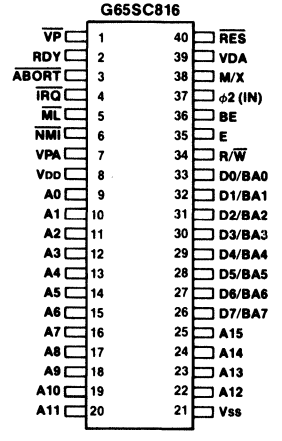
Pin	Description
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
VDA	Valid Data Address
$\overline{VP}$	Vector Pull
VPA	Valid Program Address
VDD	Positive Power Supply (+5 Volts)
VSS	Internal Logic Ground

Pin Configuration





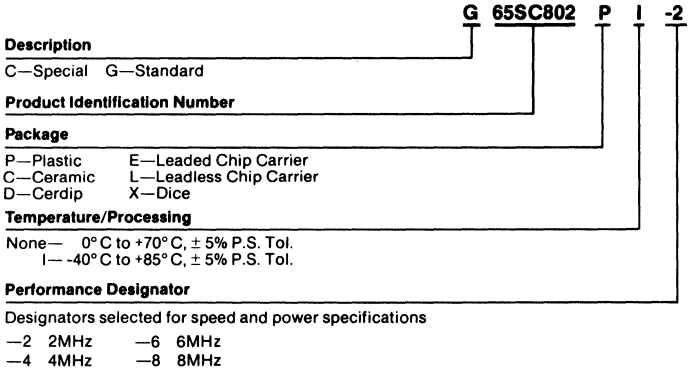




Notes:

1. Future G65SC802/816 PLCC devices will have VSS added to this pin.
2. Future G65SC802/816 PLCC devices will have VDD added to this pin.
3. New signal pins on G65SC802 not available on 40-pin DIP version.

Ordering Information



G65DS-150

Microcircuits

Evaluation Board for G65SC150 CTU

Features

- Emulates GTE's G65SC150 Communications Terminal Unit (CTU)
- Executes full G65SC150 instruction set
- Allows real-time G65SC150 emulation for in-circuit prototype debugging and program development when used with an In-Circuit Emulation system.
- Can be configured for stand-alone, full capability CTU emulation in designer's prototype system
- 2K × 8 EPROM or RAM for use during program development (RAM supplied)
- Crystal oscillator (3 to 16 MHz) for driving CTU clock input (3.58 MHz supplied)
- Vectored interrupt logic for vector address translation

General Description

GTE's G65SC150 Communications Terminal Unit (CTU) is a single-chip microcomputer which incorporates a G65SC00 Series microprocessor, RAM, ROM and several I/O functions. When developing a CTU-based system, the design engineer requires a convenient means for not only prototype development and debugging, but also software development. The G65DS-150 Evaluation Board serves this purpose by providing G65SC150 CTU emulation during the various phases of system and software development. The Evaluation Board's primary features include:

- G65SC150 CTU
- 2K × 8 EPROM or RAM
- Internal oscillator (3 to 16 MHz)
- Vector translation logic
- Configuration switches for function selection

(continued on page 2)

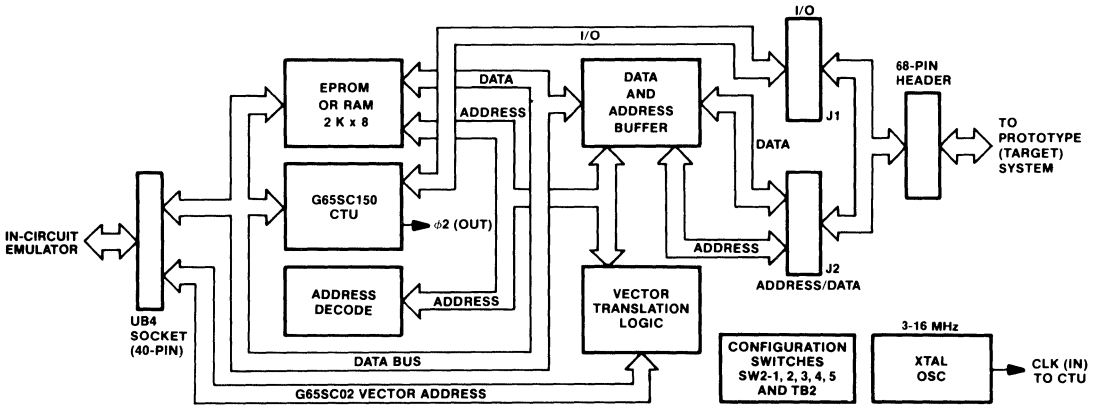
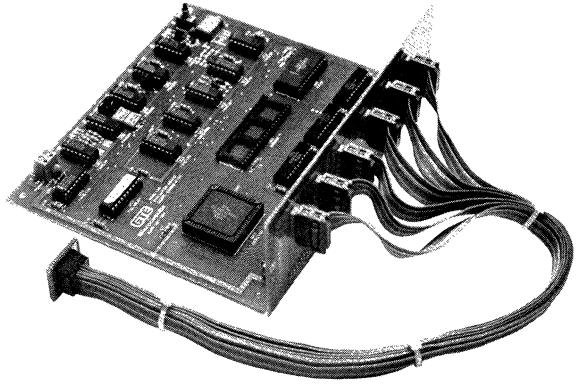


Figure 1. Evaluation Board Block Diagram



- 40-pin socket for connection to an In-Circuit Emulator
- 68-pin grid array header for connection to the prototype system

The G65SC150 CTU replaces the prototype system's CTU during the development and emulation phase. During initial hardware and software development, the Evaluation Board is normally used in conjunction with an In-Circuit Emulator. With the G65SC150 CTU operating in the peripheral mode, the In-Circuit Emulator serves to replace the CTU's internal microprocessor, thus allowing full emulation of all G65SC150 CTU functions—including its full instruction set. In this mode, the CTU's internal microprocessor is disabled. This way the In-Circuit Emulator's debugging and software development capabilities can be used on the designer's CTU-based system.

Furthermore, the on-chip CTU ROM can be disabled during software development and replaced by a 2K × 8 EPROM or RAM (designer's choice) on the Evaluation Board. This feature allows the designer's program to be easily debugged and modified prior to committing the code to the CTU's mask-programmed ROM. Normally, RAM storage is used in the memory location during the initial program development. Once the program is partially debugged, the RAM can be replaced with the less volatile EPROM for continued evaluation. Both RAM and EPROM plug into the same socket on the Evaluation Board.

Once the designer's prototype system and software has been partially debugged, the In-Circuit Emulator is normally disconnected, the CTU microprocessor is enabled, and the CTU is switched from the peripheral mode to the CTU mode. In this arrangement, the Evaluation Board appears as a full-functioning CTU to the designer's prototype system. The Evaluation Board's EPROM will continue to be used until development is complete and the CTU ROM is masked for final coding.

Functional Configurations

Tables 1 and 2 provide a description of the G65DS-150 Configuration Switches and the various system configurations available.

Table 1. G65DS-150 Configuration Switches

Switch	Name	Function
SW2-1	Off-Board Memory	**Open**—CTU ROM, or on-board EPROM or RAM at memory addresses $F800 through $FFFF. **Closed**—Memory at $F800 through $FFFF is in prototype system.
SW2-2	Processor Select	**Open**—CTU microprocessor is enabled for use without In-Circuit Emulator. **Closed**—CTU is in peripheral mode (BE = 0). In-Circuit Emulator microprocessor is in use, replacing CTU microprocessor.
SW2-3	CTU ROM Enable	**Open**—On-board EPROM or RAM is enabled at addresses $F800 through $FFFF. PD1 (EXTR) = 1. Program control of PD1 is enabled. **Closed**—CTU ROM is enabled. PD1 (EXTR) = 0. Program control of PD1 is disabled.
SW2-4	Oscillator	**Open**—Prototype system oscillator is used as CTU clock input at J1, pin 5, CLK (IN). **Closed**—On-board oscillator is used as CTU clock input, CLK (IN). This signal drives J1, Pin 5.
SW2-5	EPROM Or RAM	**Open**—Memory socket at UB7 contains EPROM or write-protected RAM at addresses $F800 through $FFFF. **Closed**—Memory socket at UB7 contains write-enabled RAM at addresses $F800 through $FFFF.
TB2	R/$\overline{W}$ Select (Jumper)	**A-B**—CTU microprocessor is in use. R/$\overline{W}$ is an output. **B-C**—CTU is in peripheral mode. R/$\overline{W}$ is an input.

Table 2. System Configurations

Configuration	SW2-1	SW2-2	SW2-3	SW2-4	SW2-5	TB2
Processor						
In-Circuit Emulator connected to socket UB4. CTU in peripheral mode.	X	Closed	X	X	X	B-C
Stand-alone CTU emulator mode. CTU microprocessor is in use. In-Circuit Emulator disconnected from UB4 socket.	X	Open	X	X	X	A-B
Memory at $F800 Through $FFFF						
CTU ROM in use.	Open	X	Closed	X	X	X
On-board EPROM or write-protected RAM in use.	Open	X	Open	X	Open	X
On-board write-enabled RAM in use.	Open	X	Open	X	Closed	X
Prototype system memory in use.	Closed	X	Open	X	X	X
Clock Source						
On-board oscillator in use.	X	X	X	Closed	X	X
Prototype system clock in use (J1, Pin 5).	X	X	X	Open	X	X

Specifications

Input Voltage	5.0 Vdc ±5%
Input Current	200 mA Max.
Height	0.6 inches
Length	7.0 inches
Width	6.0 inches
Weight	0.3 pounds
Operating Temp.	0° C to 50° C
Storage Temp.	-40° C to 85° C
Relative Humidity	20 to 80 percent

Ordering Information

Item	Part Number
Evaluation Board for G65SC150 (Assembly)	G65DS-150
Evaluation Board for G65SC150 (Board Only)	G65DS-151
In-Circuit Cable for Use with the G65DS-151	G65DS-152
Instruction Guide for G65DS-150	3003-02-00

2 Custom/ Semicustom

GTE Microcircuits

Custom/Semicustom

Custom/Semicustom Advantages

A custom integrated circuit solution becomes a major advantage when system volumes are high, board space is low, or when standard products are unable to offer a solution. When deciding on a custom/semicustom circuit the following advantages should be considered:

Reliability—As the total system size is reduced and the number of components is decreased, reliability increases. For the user, increased reliability means less down time, reduced cost and increased productivity.

Lower Cost—Custom/semicustom circuits can replace large numbers of components. This results in reduced inventory cost, less PC board assembly time and greatly reduced power supply requirements.

Design Features—Many design features which are not available in standard products can be cost-effectively designed into custom ICs.

Competitive Edge—Custom/semicustom circuits result in cost effective products with increased user value. Furthermore, custom circuits with special features are difficult to copy! This feature alone is a major consideration in maintaining a product's competitive edge.

Watch Your Custom Designs Come Alive

At GTE Microcircuits, we can make your custom designs come alive. We have a variety of custom/semicustom approaches to turn your most sophisticated designs into reality. Our Application Specific Integrated Circuit (ASIC) solutions include Gate Arrays, Standard Cells, Full Custom and CFT™ (Customer Furnished Tooling).

Engineer-To-Engineer

We have found the most effective way to assure the success of a custom/semicustom design. At GTE Microcircuits we stress the importance of our engineers interacting with your engineers. No matter how detailed the specification, all design considerations cannot be accounted for. We have found that this type of problem can best be eliminated through good engineering communications.

Cooperation

If your custom/semicustom circuit doesn't function, we have failed! To most customers, the decision to go with a custom/semicustom design is like sailing in uncharted waters. We at GTE Microcircuits can supply the maps. We are willing to do as much or as little of the work as necessary...it's your decision. For example, our engineering staff will do all the work, guide you through the process, or pick up the effort at any point you desire. Just let us know so we can provide the services you need for success.

Semicustom Design
GTE Gate Arrays

The Large Scale Integrated (LSI) circuit has become the state-of-the-art solution to highly complex electronic circuit design requirements. For compact individualized circuit designs, the custom LSI is the most cost-effective and reliable approach to high volume production requirements. The high cost of initial design and fabrication, however, makes the custom LSI circuit prohibitive for the low to moderate volume user.

The solution for the low to moderate volume user is GTE Gate Array technology; a matrix of uncommitted P-channel and N-channel transistors that allow the designer to obtain the economic benefits of volume manufacturing for relatively small runs while at the same time incorporating original or proprietary circuit designs.

GTE Gate Array wafers are prefabricated and banked (stored) at metal, with the user's metal interconnect pattern (mask) being the final processing step to personalizing the array. As non-personalized wafers can be banked in quantity, the user gains the benefits of a low parts count, reliability of proven technology, minimum development costs and a fast turnaround.

General Description

GTE Microcircuit's family of Gate Arrays are manufactured using high-performance CMOS technologies for higher speed and lower power operation. Inputs and outputs may be selected from 14 possible configurations. A growing library of macro cells, ranging from single 2-input gates to counters and static shift registers, are characterized and available.

GTE is attune to the changing requirements of the gate array user community and is continuously evolving their family of products to meet this changing need.

As your Total Resource Company, there are three reasons why GTE Microcircuits has become the industry's first choice for Gate Array design, fabrication and production.

1. Total Capability...From Logic to Devices

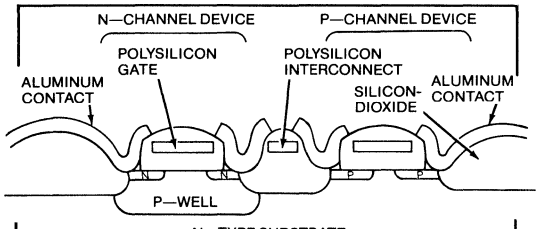
The designing and processing of a Gate Array chip is really quite simple. In fact, just provide us with your logic diagrams and interface specifications and GTE will do the rest. We will provide logic simplification or complexity reduction, simulation, timing analysis, interconnect place and route, prototype fabrication and testing, and final production integrated circuits. With this approach, you do what you do best and we'll do the rest. For minimum involvement, you do the logic and system design and we'll take it from there...reducing your design to an efficient, low cost and functionally equivalent integrated circuit.

2. Fully Automated Logic Integration System... It's a Step Ahead!

Once your logic design has been evaluated and reduced to macro logic functions, and a test plan developed, GTE's computerized system performs logic simulation, testing and pinout compatibility with the Gate Array macro structure. Your logic design is then ready for logic element placement and interconnection within the Gate Array matrix. Although this procedure can be accomplished by the customer, it can be performed much more efficiently by GTE's Automated Logic Integration System (ALIS). GTE's ALIS is a step ahead of the Gate Array industry. It not only relieves the burdensome job of manual logic element placement and interconnection, but also virtually eliminates the possibility of costly human error. Once the place and route is complete, the routed array is digitized and pattern generation tapes are produced for final mask tooling and prototype assembly.

3. Advanced CMOS Gate Array Technology...It's the Way of the Future!

GTE Microcircuits has the leading edge in Advanced CMOS Gate Array technology. Isolated Complementary Metal Oxide Semiconductors offers the speed and performance advantages of NMOS with the added benefits of increased reliability, greater noise immunity, and perhaps most important, significantly less power consumption. And furthermore, Advanced CMOS Gate Arrays are TTL/CMOS input/output compatible, and they require only a single supply voltage (+5V).



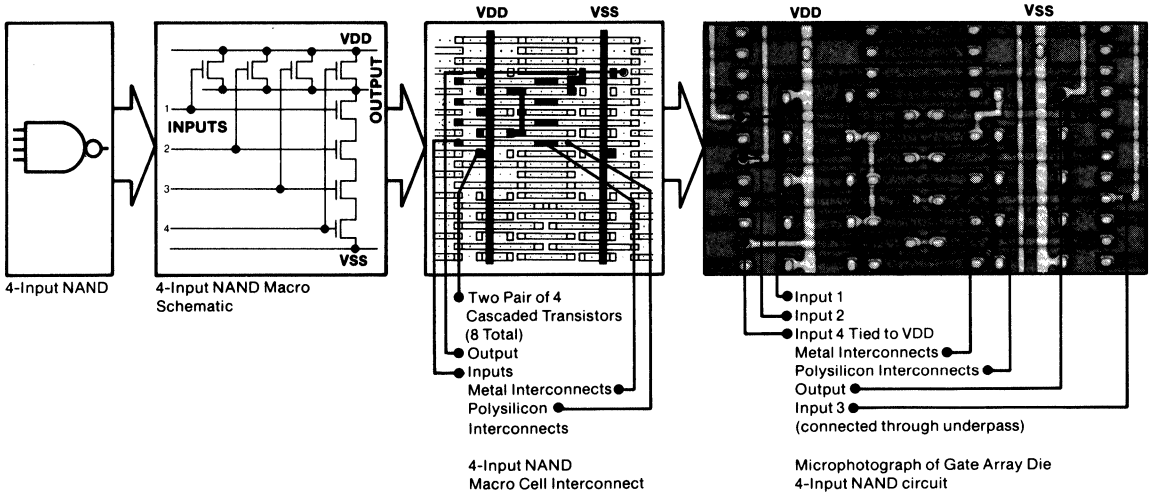
CMOS Topology

Technical Description

Features

- CMOS high speed, low power technology
- Gate propagation delay—2.9 nS (2-input NAND)

Gate Array Design Flow



- CMOS or TTL input configurations
- 4 to 6 week design turnaround
- Wide range of package options
- Specialized support during all phases of gate array designs
- Low NRE charges
- Above 90% array utilization

The Transistor Array

Each macro function is implemented within a cell or by grouping multiple cells. Each array is based on a matrix of uncommitted cells, where each cell consists of eight transistors...four cascaded N-channel and four cascaded P-channel devices. These cells are arranged in rows, and when appropriately connected, make up the various logic functions found in the Macro Cell Library.

Configuring a cell is accomplished by metal traces in the bus paths and by using polysilicon underpasses. These underpasses run horizontally between the cell rows as well as through the cells themselves. There are also vertical underpasses which serve to provide interconnection across a column of cells or bus paths without obstructing the bus paths. I/O pads, input protection circuitry, resistors, capacitors and output drivers are placed around the periphery of the array and are readily connected to the internal logic functions.

The Macro Cell Library

Table 1 provides a partial listing of currently available macro cell logic function. GTE offers over 88 different logic function configurations ranging from a simple 2-input NAND gate to cascadable shift registers. GTE's complement of macro logic functions will satisfy your most demanding system configuration and we're adding new functions all the time. As a special note, if you have a logic configuration which is not represented in our library, GTE will develop a custom macro cell for your requirement...and the cost is nominal.

Gate Array Configurations

GTE uses the "gate equivalent" method for describing the various array sizes. One "gate" is equivalent to a 2-input NAND/NOR gate. In this way, each macro cell function within the Macro Cell Library can be related to a "gate equivalent" (2-input NAND) requiring one-half cell, but an Edge-Triggered "D" Flip-Flop requires four cells. Therefore, the Flip-Flop requires array space equal to eight "gate equivalents". The "gate equivalent" method will help you in planning the array size needed for your application.

I/O Configurations

Your Gate Array I/O configuration will vary with the array size and to some degree with its complexity. All I/O pads except those predefined as power supply connection can be configured as Inputs or Outputs. I/O configuration characteristics include:

- Individually tailored input switching characteristics for either CMOS or TTL compatibility
- Low power Schottky output buffers for driving up to two "LS" TTL loads (CMOS level output)
- TTL output buffers for driving up to 1.5 standard TTL loads or six "LS" TTL loads (CMOS level outputs)
- All Gate Array output buffers can be configured for three-state or open-drain (open collector) operation

G50000B Series

Microcircuits

CMOS Gate Arrays

Features

- CMOS high speed, low power technology
- Gate propagation delay—2.9 nS (2-input NAND)
- Gate power dissipation—5 μW at 1 MHz typical
- CMOS or TTL interface
- Bus oriented interconnect paths
- On-chip resistors and capacitors
- Array sizes from 100 to 3000 gates
- Over 88 macro logic functions
- Single power supply (+5 Vdc)
- Wide range of packaging options

General Description

GTE's G50000B Series Gate Arrays are manufactured using CMOS high performance technology for higher speed and lower power operation. Each Gate Array cell consists of a matrix of four P-channel and four N-channel transistors which can be programmed for metal mask interconnection to provide virtually unlimited implementation of LSI logic designs. Within each logic cell and under the bus routes, polysilicon crossunders provide logic interconnection with the metal layer. These crossunders, combined with vertical bus routes, allow both vertical and horizontal interconnection, thus providing highly efficient chip utilization and circuit complexity. Macro logic functions are selected from a standard library of over 88 preconnected logic functions. Each array contains a number of resistors and capacitors which provide the circuits with limited analog capability. GTE offers arrays in sizes ranging from 100 to 3000 equivalent 2-input NANDS, with up to 94 I/O pads per array.

GTE Gate Array Configurations

Device	No. of Gates (1)	No. of Pads(2)	Chip Size	Package Pins Required
G50100B	120	24	92 x 118	14-24
G50500B	504	44	124 x 200	16-44
G51000B	960	54	175 x 223	24-68
G51500B	1512	70	228 x 247	24-68
G52000B	2024	82	245 x 289	24-84
G53000B	3000	100(3)	267 x 282	24-84

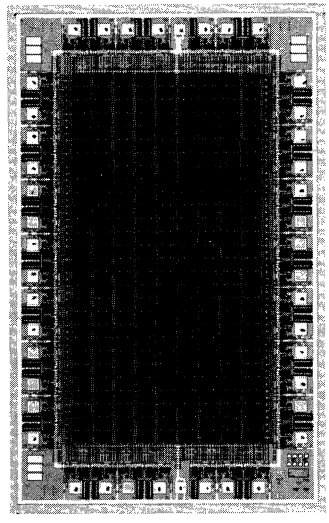
(1) Gates configured as 2-input NAND.
(2) Includes one V_{DD} pad and one V_{SS} pad.
(3) Includes three V_{DD} pads and three V_{SS} pads.

On-Chip Resistors and Capacitors

On-chip resistors and capacitors are positioned around the array to allow connection to either I/O cells or function cells.

Device	Resistors 40 K Ω (typ.)	Resistors 100 K Ω (typ.)	Capacitors 0.5 pF (typ.)
G50100B	0	31	0
G50500B	12	39	9
G51000B	12	53	9
G51500B	12	76	9
G52000B	12	90	9
G53000B	12	106	9

Array Configuration



Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{DD}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current, Any Output	I_O	±50 mA
Operating Temperature	T_A	-55°C to 125°C
Storage Temperature	T_S	-65°C to 150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics, Low Power Schottky Compatible Configurations: V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0		V	V_{CC} = 4.50
Low Level Input Voltage	V_{IL}		0.8	V	V_{CC} = 4.50
High Level Output Voltage (Type 2 Output)	V_{OH}	2.4		V	I_{OH} = 6.0 mA, V_{CC} = 4.50V
		4.5		V	I_{OH} = 2.0 mA, V_{CC} = 4.50V
Low Level Output Voltage (Type 2 Output)	V_{OL}		0.4	V	I_{OL} = 3.2 mA
High Level Input Current	I_{IH}		10	μA	V_I = 2.7V
Low Level Input Current	I_{IL}		-10	μA	V_I = 0.4V
Off-State Output Current, High-Level Voltage Applied	I_{OZH}		20	μA	V_O = 2.7V
Off-State Output Current, Low-Level Voltage Applied	I_{OZL}		-20	μA	V_O = 0.4V

DC Characteristics, CMOS Compatible Configuration: V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	3.5		V	
Low Level Input Voltage	V_{IL}		1.5	V	
High Level Output Voltage	V_{OH}	4.95		V	I_{OH} = 1μA
Low Level Output Voltage	V_{OL}		0.05	V	I_{OL} = -1μA
High Level Input Current	I_{IH}		1	μA	V_I = 5.0V
Low Level Input Current	I_{IL}		-1	μA	V_I = 0V
Off-State Output Current, High-Level Voltage Applied	I_{OZH}		20	μA	V_O = 5.0V
Off-State Output Current, Low-Level Voltage Applied	I_{OZL}		-20	μA	V_O = 0V

AC Characteristics: V_{DD} = 5.0V, V_{SS} = 0V, T_A = 27°C, R = 0Ω, C_L = 1 Unit Load, Input Rise/Fall = 5 nS

Parameter	Macro Cell	Min	Max	Unit	Test Conditions
Single Inverter	GTE5002		1.7	nS	
2-Input NAND	GTE5005		2.9	nS	
Output Buffer, Non-Inverting Stage With Three-State Output	GTE5208		13.1	nS	R = 4000Ω, C_L = 15 pF
Input Buffer, TTL (Inverting)	GTE5102		2.2	nS	

Standard Cells

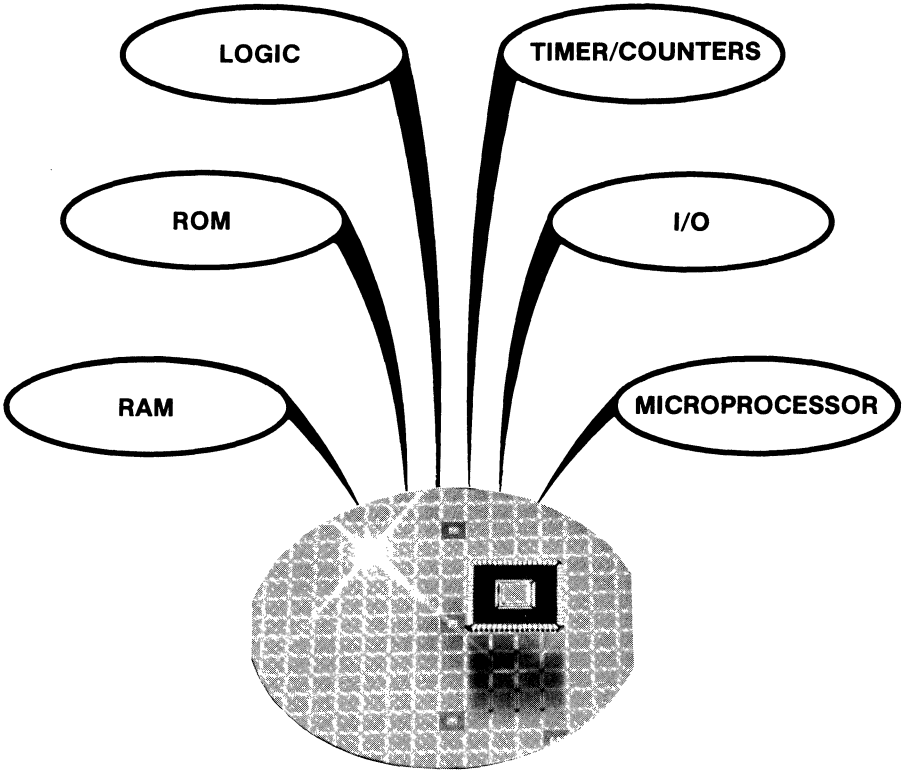
Building Blocks for Single Chip Designs

GTE Microcircuits offers a variety of Advanced CMOS Standard Cells. These cells are your building blocks for semicustom chip configurations. Many times, the needs of a particular application cannot support the expense and time of a full custom integrated circuit. When this is the case, GTE's Standard Cells provide the perfect solution...offering not only ease of implementation and design flexibility, but low cost and fast turnaround time. You'll find that your choice of internal functions and interface configurations is almost limitless...and it all takes place within a single chip. Internal design functions may include:

- Microprocessor—from the G65SC00 Microprocessor family
- ROM—for permanent data storage
- RAM—for temporary data storage
- I/O—special or expanded I/O configurations
- Logic—GTE Gate Array Macro Logic and other internal logic cells for logic control functions

So next time you have an application which requires multiple-chip functions, contact GTE Microcircuits. Chances are, we can put it ALL IN A SINGLE CHIP!

Semicustom Designs From Standard Cells



Custom Products
Customer Furnished Tooling (CFT™)

Make Your IC Designs Come Alive!

We're GTE Microcircuits, and we have what it takes to turn your IC designs into working silicon...from wafers to packaged and fully tested ICs ready for market or installation into your system's circuit boards. You can specify exactly what services you need and then get prototypes without committing to large production runs. In fact, you can enter the GTE Microcircuits program at any point in the process with just about any volume and we will work with you to ensure the highest possible quality and the best possible yield.

And make no mistake! We're serious about your requirements. We understand just how much you have put into your IC designs. You've invested many hours of design time and perhaps the allocation of Computer Aided Design (CAD) resources. Now it's time to implement your design into silicon and you want to use the best process available. You need look no further...you will find the best process is at GTE Microcircuits. Our state-of-the-art processing capabilities and ultra-modern facilities will guarantee you the ultimate in design performance and product reliability. So if you want the best, rely on GTE Microcircuits to make your IC designs come alive.

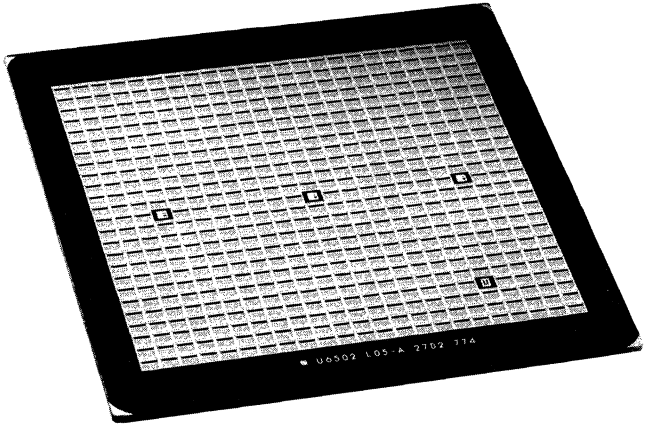
At GTE Microcircuits, we can process your designs in 3, 4 or 5 micron CMOS. We can also provide you with complete wafer fabrication through fully tested and packaged parts. In fact, you can enter the production process at any point and we'll take it from there. In this way, you can tailor your requirements to meet your specific needs. You'll find the GTE Microcircuits program is flexible and designed to help you gain the competitive edge.

GTE Provides The Total Solution

We call it the Customer Furnished Tooling (CFT™) program, and it's for those customers who have access to an integrated circuit design group and wish to design their own devices. It is also for those companies that have a design from another supplier and want to tool up a second source. GTE Microcircuits' CFT™ program is easy to use and contains a variety of options which allow you to enter the program at the point best suited to your needs. And remember, no challenge is too great ...we welcome your most complex designs. At GTE Microcircuits we offer the TOTAL SOLUTION to your integrated circuit processing requirements.

GTE Microcircuits Makes It Easy!

How easy? Let's take a look at an example of a basic entry level. In this case, the customer furnishes us with



working plates or masks. We will then manufacture ten or more wafers using CMOS technology.

Once processing is complete, these wafers will be returned to you for testing, or they can be tested by GTE Microcircuits using a customer-furnished test tape. Following test and evaluation, arrangements are made for volume processing, packaging, and shipment as originally specified.

It is highly recommended that GTE Microcircuits process monitors and alignment marks be incorporated into your masks and plates. These control monitors and alignment keys must be included during the digitizing process. The use of control monitors assures that all process controls are maintained throughout the wafer fabrication process.

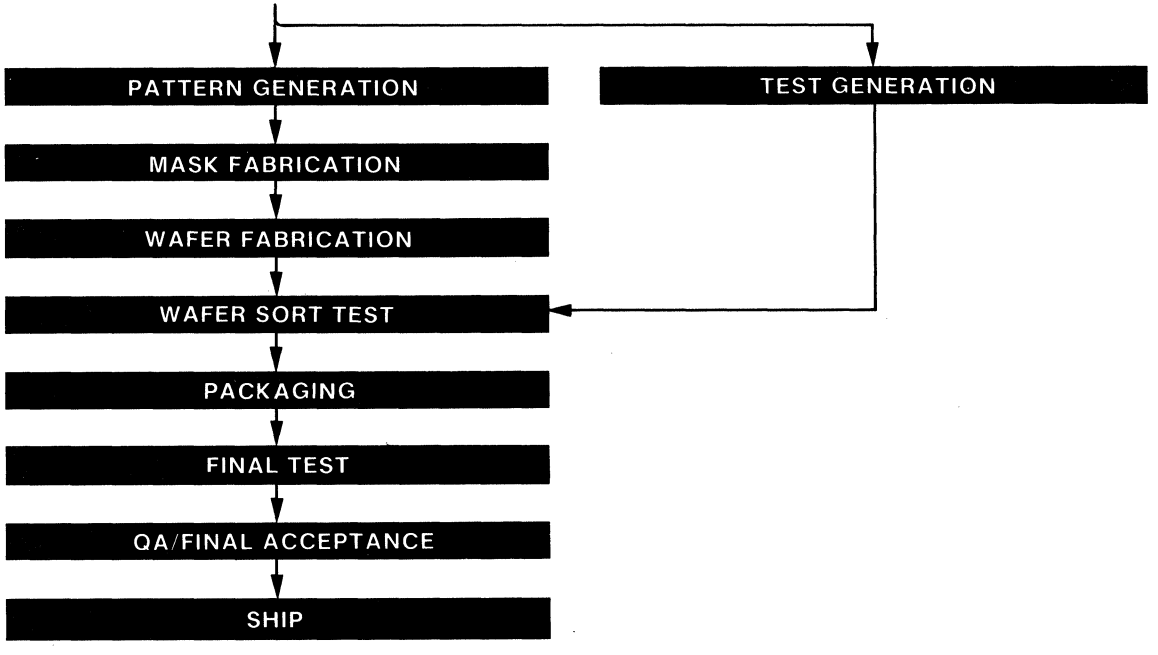
Although this example represents the most basic CFT™ program, it is quite typical of most processing requirements. But whatever your requirement, GTE Microcircuits will offer assistance for entry at any level of the manufacturing process as shown in the flow diagram. Remember, the entry point is your choice.

If you are engaged in a new design, we prefer to work with your design engineers at the earliest possible point in the design process. This approach allows us to provide you with appropriate specifications relative to design rules and process parameters. So, if you are considering a new design, or would like to establish a reliable, long term second source...GTE Microcircuits has the answer.

For Flexibility In Action, You Define The Interface

When working with GTE Microcircuits, you define the interface which best suits your program needs. In providing assistance, we will work closely with you to determine the best working arrangement for your specific program, or to put it another way: "Where is the best place for a customer to enter the CFT™ program?" This question depends on many factors, some of which are based on technical difficulty, circuit performance requirements, anticipated production volume, and the availability of your design engineers at the beginning of the program. The amount of time required for given tasks varies and this variance is in direct relation to the complexity of the circuits being processed. Nevertheless, before a program is started, realistic task ranges will be established and agreed upon. In this way, you will be fully aware of all tasks and worst case scheduling associated with performing these tasks.

Notice that the basic manufacturing flow diagram describes how the CFT™ program may be entered at any of several break points. The interfacing of any one of these entry points takes a mutual involvement by both GTE Microcircuits and the customer. Let's take a look!



Pattern Generation

GTE Microcircuits can accept a composite design and digitize it using computer-aided design techniques. The digitized information is then used to generate check plots which are used by the customer for comparison against the original composite design. It is at this stage that GTE Microcircuits' test monitors and alignment marks are incorporated. Overall, digitizing is an iterative procedure that requires several interactions before a data base tape can be approved for a total composite design.

The digitized information (data base tape) is then used for reticle generation (pattern generation). The reticle is normally generated 10X scale.

Mask Fabrication

If desired, you may enter the GTE Microcircuits CFT™ program at the mask fabrication stage. In this case, customer-generated data base tapes are used to produce a set of reticles from which a master plate will be produced. Before the master plate is produced, the reticles are used to photographically generate blow-backs for each layer. These blow-backs are compared to the composite design as a final check to ensure the reticles are correct. GTE Microcircuits test monitors and alignment marks can also be implemented at this step in the procedure. The approved reticle is then used to step-and-repeat a master plate which, in turn, is used to generate all working plates.

Wafer Fabrication

Wafer fabrication is performed using GTE's CMOS process. Geometric technology, wafer size and density will have been previously determined by the customer and GTE Microcircuits. It is important to note that the quality of wafers produced during wafer fabrication will reflect the quality of the customer-provided input. Customer-provided masks will be thoroughly inspected prior to wafer fabrication.

Each customer program is based on a two-phase approach. In Phase I, a wafer lot is processed. This lot is then process mapped, optically inspected, and delivered (untested) to the customer in the form requested. In Phase II, additional wafer lots are run. These wafers are delivered to the customer as prototype units. Upon customer approval of the prototype units, volume production will be initiated.

Wafer Sort Test

Wafers can be tested using state-of-the-art LSI testers. Each test unit contains its own minicomputer and is capable of extensive functional and parametric testing. All wafer testing is performed using customer-supplied test programs. Each program must be consistent with the appropriate GTE Microcircuits test format.

Packaging

Packaging can be included as a part of any CFT™ program. Or if you wish, customer-provided wafers or die can be supplied for packaging. In either case, each die is inspected before it is mounted into the package. Leads are then bonded to the pads, with a final visual inspection being performed prior to sealing. Sealed packages can then be tested by GTE Microcircuits or delivered to the customer untested.

Final Test

Final testing is performed using customer-supplied test programs. Most testing is conducted at 25°C and then correlated with temperature limits. Testing at extreme temperatures can also be accomplished upon request.

Quality Assurance And Final Acceptance

Quality Assurance is an integral part of the CFT™ program. Standard QA sampling is accomplished on all packaged products where each lot is sampled for acceptance testing. Completed packages are subjected to various environmental processes to ensure electromechanical integrity. Leak tests are performed on cavity packages to check hermeticity, and temperature cycling is performed to customer specifications. Additional environmental testing can be performed to satisfy individual customer requirements.

Quality Products From A Quality Program

The GTE Microcircuits Quality Assurance and Reliability program is designed to provide strong support to the CFT™ program. Quality measurement and appraisal activities encompass every facet of the company's operation. This objective ensures all products are manufactured to a high standard of quality...a quality level which meets or exceeds customer requirements.

Since wafer fabrication is a high technology operation, significant effort is exerted to guarantee the highest possible product quality and yields. For example, three critical inspection gates are maintained at the photomask stage. Each of these three gates involves visual inspections to not only guarantee correct mask alignment, but to ensure critical dimensions fall within specified limits.

Quality monitors are used during both diffusion implantation processes. These monitors provide Capacitance/Voltage (CV) analysis of ion implantation. The CV analysis is a useful tool, providing measurements of how much phosphorus or boron is being doped into each wafer. Furthermore, CV analysis is used during the diffusion process to monitor oxide quality and system cleanliness. Another means of ensuring quality involves sheet resistance and layer thickness measurements. These measurements are continuously monitored and compared against established criteria.

Quality Monitors During Test And Assembly

Wafer testing is performed prior to final assembly and consists of 100 percent functional and parametric test-

ing. During assembly, quality procedures require audit points, with each audit consisting of as many as 20 separate steps. At least three audit points involve optical inspections at critical stages within the assembly process. These inspections ensure that:

- Wafers have been correctly and fully probed.
- Damage did not occur as wafers were separated into individual dice.
- Quality is maintained during die attachment to the package and during bonding.

Once packaging has been completed, each ceramic and cerdip package is required to pass a 100 percent gross leak test. As a further check of package hermeticity, a sample fine leak test is conducted. At this point, each device is ready for final electrical testing during which worst case voltage and timing tests are performed. Temperatures and burn-in times vary with product type and individual product specifications. During burn-in, both voltage and temperature stresses are applied to weed out all possible infant mortalities.

In summary, the total GTE Microcircuits quality assurance program is designed to ensure product quality is built into the manufacturing process. This total quality concept is dedicated to making sure each step is done right the first time and every time.

A Total Resource In Capability And Dedication

GTE Microcircuits is your total resource for manufacturing capability. We are dedicated to the proposition that you must obtain advantages in both time and cost ...thus guaranteeing your competitive edge. To this end, GTE Microcircuits maintains continuing programs for the advancement of designs, technologies, and systems ...always striving to remain in the forefront of leading edge technology. This effort results in a better product, a better understanding of industry needs, and a keen insight into customer requirements.

Let Us Review Your Requirements

At GTE Microcircuits, we understand your processing needs, and we are prepared to help you find the necessary solutions. We're your Total Resource, derived not only from the industry's most advanced fully automated logic integration system, but also from dedicated engineers and system designers...and a project management concept that is unmatched in the industry.

In summary, GTE Microcircuits offers the Total Solution. You can be assured that your system performance and time-to-market requirements will be met...and at the lowest possible cost.

Table 1. Electrical Parameters

Electrical Parameters 25°C	5 Micron	4 Micron	3 Micron	Units
Vt N-Channel	0.4 to 0.9	0.4 to 0.9	0.4 to 0.9	V
KN (Conduction Factor)	60 to 180	70 to 180	39 to 47	$\mu A/V^2$
Bvdss N-Channel	>18	>18	>12	V
Field Threshold N-Channel Poly Si	>14	>12	>14	V
Vt P-Channel	0.4 to 0.9	0.4 to 0.9	0.4 to 0.9	-V
KP (Conduction Factor)	20 to 75	30 to 100	16 to 20	$\mu A/V^2$
Bvdss P-Channel	<-17	<-17	<-10	V
Field Threshold P-Channel Poly Si	<-12	<-10	<-10	V

Table 2. Process Parameters

Process Parameters	5 Micron	4 Micron	3 Micron	Units
Substrate				
Type	N100	N100	N100	
Resistivity	1.9 to 2.6	1.9 to 2.6	1.9 to 2.6	Ohm-cm
Tub				
Type	P-	P-	P-	
Xj	5.5	5.0	5.0	μm
Resistivity	1.9 to 3.2	1.6 to 3.0	2.0 to 4.0	Kohm/sq
Field Oxide Thickness	18,500	15,000	15,000	Angstrom
Gate Oxide Thickness	800	630	450	Angstrom
Polysilicon Thickness	4,400	4,400	4,400	Angstrom
Metal Thickness (A1-1.0% Si-0.5% Cu)	9,500	9,500	9,500	Angstrom
Final Passivation				
Thickness	11,000	11,000	11,000	Angstrom
Phos % wt	3.5 to 5.0	3.5 to 5.0	3.5 to 5.0	%

Table 3. Design Parameters

Design Parameters	5 Micron	4 Micron	3 Micron	Units
Diffusion				
Pitch	10	8	6	μm
Min. Space	5	4	2	μm
Min. Width	5	4	4	μm
Polysilicon				
Pitch	10	8	6	μm
Min. Space	5	4	3	μm
Min. Width	5	4	3	μm
Contact Size	5	4	3	μm
Metal				
Pitch	10	8	7	μm
Min. Space	5	4	3	μm
Min. Width	5	4	4	μm
Min. N-to-P Space				
P+ to P-	12.5	10	10	μm

Full Custom

Full custom designs are cost effective when the features required are not available in semicustom or standard product alternatives, or when the system volumes are large. Full custom circuits offer the advantages of reduced cost, expanded features, reliability and a competitive edge.

Resident at GTE Microcircuits is a staff of highly skilled designers. Our expertise spans the range of digital, analog, and mixed signal technology. The efforts of this staff have produced many high volume, cost effective custom integrated circuit solutions.

In designing a custom circuit our design staff will communicate often with your engineers and our test, process, packaging, manufacturing and quality assurance groups. This will ensure that you receive the product that you desire and that it is reliable, testable and takes full advantage of our advanced CMOS process.

3 Communications

GTE Microcircuits

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Glossary of Telecommunication Terms

Introduction

The following is a list of terms, and their definitions, commonly encountered in the telecommunications industry. Where possible, definitions have been based on the international recommendation of CCITT.

A-Law—European companding/encoding law commonly used in PCM systems.

A-Law/μ-Law Companded—Eight-bit PCM binary code; codes almost universally used for PCM digital switching and transmission. Where a reference is made to PCM, it is almost invariably these codes which are being referred to (A-Law version in Europe and μ-Law version in North America).

A/B Signaling—A special case of 8th-bit (LSB) signaling in a μ-Law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (Analog-to-Digital) Converter—Converts an analog signal sample to a digital representation suitable for digital processing and switching.

Address—In communications, a sequence of bits, a character, or a group of characters that identifies a network station, user, or application. The address is mainly used for routing purposes. In telephony, it is the number entered by the caller that identifies the party called.

ADI—Alternate Digit Inversion. ADI is used with A-Law to ensure sufficient 1-0/0-1 transitions for clock extraction (timing recovery) in PCM multiplex transmission equipment.

ADPCM—Adaptive Differential Pulse Code Modulation. ADPCM is an encoding technique, standardized by the CCITT, that allows an analog voice conversation to be carried within a 32-kbit/s digital channel. Three or four bits are used to describe each sample, which represents the difference between two adjacent samples. Sampling is performed 8,000 times a second.

Aliasing Noise—A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Alternate-Mark Inversion Signal (AMI or BAMI, Bipolar Signal)—A pseudo ternary signal, conveying binary digits, in which successive "marks" are normally of alternate, positive and negative polarity but equal in amplitude and in which "space" is of zero amplitude.

Alternate Routing—A feature of network switches, especially PBXs, where a call is completed over other circuit routes when first-choice routes are unavailable, not in service, or occupied.

Amplifier—Any electronic component that boosts the strength or amplitude of a transmitted signal (usually analog). It is functionally equivalent to a repeater in digital transmissions.

Amplitude Modulation (AM)—A transmission method in which variations in the voltage or current waveform of a carrier signal determine encoded information.

Analog—In communications, a transmission employing variable and continuous waveforms to represent information values, where interpretation by the receiver is an estimated approximation (quantization) of the encoded value (compare with digital).

Anti-Aliasing Filter—A filter (normally low-pass) that band limits an input signal before sampling to prevent aliasing noise.

ASCII—American Standard Code for Information Interchange. ASCII is the standard, and predominant, seven-bit (eight bits, with parity) character code used for data communications and data processing.

Asynchronous—A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Asynchronous Transmission—A mode of communication characterized by start/stop transmissions with undefined time intervals between transmissions.

Attenuation—Reduction or loss of signal strength, measured in decibels (opposite of gain).

Balanced-to-Ground—With a two-wire circuit, where the impedance-to-ground on one wire equals the impedance-to-ground on the other wire. Compare with unbalanced-to-ground, a preferable condition for data transmission.

Balancing Network—An arrangement of impedances connected to one branch of hybrid to match the impedance of a line connected to the opposite branch.

Bandwidth—The difference, expressed in Hertz (Hz), between the highest and lowest frequencies of a transmission channel.

Baseband—The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud—A unit of signaling speed equal to the number of discrete signal conditions or events per second. Baud refers to the physical symbols/second used within a transmission channel.

Binary Digit—A member selected from a binary set, e.g. 1, 0; V+, V–; H, L.

Bipolar—The predominant signaling method used for digital transmission services, such as DDS and T1, in which the signal carrying the binary value successively alternates between positive and negative polarities. Zero and one values

are represented by the signal amplitude at either polarity, while non-value "spaces" are at zero amplitude. Also in reference to polar transmission. Bipolar is also a type of integrated circuit (IC, or semiconductor) that uses both positively and negatively charged currents, characterized by high operational speed and cost.

Bisync—Binary Synchronous Communications (BSC) character-oriented data communications protocol developed by IBM. It is oriented toward half-duplex link operation. Bisync is still widely employed, though replaced in current IBM data communications products by the bit-oriented Synchronous Data Link Control (SDLC).

Bit—A binary digit, the representation of a signal, wave, or state, as either a binary zero or one.

Bit Duration—Equivalent to the time that it takes one encoded bit to pass a point on the transmission medium. In serial communications, a relative unit of time measurement, used for comparison of delay times (e.g., propagation delay, access latency) where the data rate of a transmission channel can vary.

Bit Error—The case where the value of an encoded bit is changed in transmission, and interpreted incorrectly by the receiver.

Bit Error Rate (BER)—The percentage of received bits that are in error, relative to a specific amount of bits received. It is usually expressed as a number referenced to a power of 10; e.g., 1 in 10^5.

Bit/s—Bits per second; basic unit of measure for serial data transmission capacity; Kbit/s, or kilobit/s, for thousands of bits per second; Mbit/s, or megabit/s, for millions of bits per second; Gbit/s, or gigabit/s for billions of bits per second; Tbit/s, or terabit/s for trillions of bits per second.

Bit Oriented—Describing a communications protocol or transmission procedure where control information is encoded in fields of one or more bits. Normally oriented toward full-duplex link operation. Bit orientation uses less overhead, and is therefore more efficient than character-, or byte-, oriented protocols.

Bit Rate—The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits per baud.

Bit Stuffing—A process, in bit-oriented data communications protocols, where a string of "one" bits is broken by an inserted "zero" which is added by the sender and removed by the receiver. Adding of "zero" bits is done to prevent user data from containing a series of "one" bits.

Blocking—A condition in a switching system in which no paths or circuits are available to establish a connection to the called party, even though it is not busy, thus resulting in a busy tone to the calling party.

BOC—Bell Operating Company. One of 22 local telephone companies spun off from AT&T as a result of divestiture, and now reorganized into seven regional Bell holding companies. They are among the largest of the 1,600 independent local phone companies in the U.S.

BORS(C)HT—Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband—A transmission facility whose bandwidth is greater than that available on voice-grade facilities.

Buffering—The process of temporarily storing data in a register or in RAM, which allows transmission devices to accommodate differences in data rates and to perform error checking and retransmission of data received in error.

Bus—A transmission path or channel. Typically an electrical connection, with one or more conductors, wherein all attached devices receive all transmissions at the same time. It can be a local-network topology, such as used in Ethernet and the token bus, where all network nodes "listen" to all transmissions, selecting certain ones based on address identification. A bus involves some sort of contention-control mechanism for accessing the bus transmission medium.

Byte—Generally an 8-bit quantity of information, used mainly in referring to parallel data transfer, semiconductor capacity, and data storage. In data communications it is generally referred to as an octet or character.

Byte Multiplexer Channel—A mainframe input/output channel that allows for the interleaving, or multiplexing, of data in bytes.

C-Message—A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background or impulse) on voice-grade data service.

Carrier—An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT—Consultative Committee for International Telephone and Telegraph; an international standards group of the European International Telecommunications Union.

Central Office (CO)—A main telephone office, usually within a few miles of a subscriber, that houses switching gear. The central office is commonly capable of handling about 10,000 subscribers.

Centrex—A widespread telephone company switching service that uses (typically digital) central office switching equipment, and to which customers connect via individual-extension access lines. Centrex central offices use telephone company equipment exclusively, with each phone set at the customer's premises connected via a separate and dedicated access line, while a Centrex Customer Unit involves the placement of some switching, contention, or concentration equipment on the customer's premises. Typical features include Direct Inward Dialing (DID), Direct Distance Dialing (DDD), and attendant switchboards.

CEPT—Conference of European Postal and Telecommunications administrations.

Channel—In communications, a physical or logical path allowing the transmission of information. Also, the path connecting a data source and a data sink, or receiver.

Channel Bank—Communications equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

Channel Time Slot—A time slot starting at a particular phase in a frame and allocated to a channel for transmitting a character signal and possibly in-slot signaling or other information.

Character—Standard bit representation of a symbol, letter, number, or punctuation mark. It generally takes on the same meaning as byte.

Character Code—One of several standard sets of binary representations for the alphabet, numerals, and common symbols, such as ASCII, EBCDIC, BCD.

Character Signal—A set of signal elements representing a character, or in PCM representing the quantizing value of a

sample. In PCM, the term "PCM word" may be used in this sense.

Circuit Switching—The process of establishing and maintaining a circuit between two or more users on demand, such that the users have exclusive use of the circuit until the connection is released.

Clock—An oscillator-generated signal that provides a timing reference for a transmission link. It is used to control the timing of functions such as sampling interval, signaling rate, and duration of signal elements.

Codec—COder-DECoder. Codec represents the A/D and D/A function on a subscriber line card within a telephone exchange.

Code Conversion—The process of changing the bit grouping for a character in one code into the corresponding bit grouping for the character in another.

COFIDEC—COder-FIlter-DECoder. This is the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common Channel Signaling—A signaling method using a link common to a number of channels for the transmission of signals necessary for the traffic via these channels.

Companding—Compressing/expanding; the process of reducing the bandwidth required for representation of an analog waveform for transmission, and then reconstructing (most of) the original waveform at the receiving end. This function is performed by electronic circuitry that applies a compression algorithm. Compression/expansion is generally associated with analog voice signals.

Companding Law (CCITT Encoding Law)—Mathematically defined non-linear transfer characteristic used for companding. This may be a smooth continuous function or a piecewise (commonly linear) approximation to a continuous function (CCITT segmented encoding law). The two commonly used laws in telecommunications are μ-Law (North America) and A-Law (Europe).

Compression—The application of any of several techniques that reduce the number of bits required to represent information in data transmission or storage, thus conserving bandwidth and/or memory, wherein the original form of the information can be reconstructed. May also be referred to as compaction.

CPE—Customer Premises Equipment. In telephony, equipment that interfaces to the telephone network and physically resides at the user's location. Normally includes most, but not all, of the gear referred to as network channel terminating equipment (NCTE).

CRC—Cyclic Redundancy Check. CRC is a characteristic link-level feature of bit-oriented data communications protocols, wherein data integrity of a received frame, or packet, is checked using a polynomial algorithm based on the content of the frame, and then matched with the result performed by the sender and included in a field appended to the frame. CRC is a basic error-checking method for link-level data transmissions.

Crosstalk—Unwanted transference of electrical energy from one transmission medium to another, usually an adjacent medium. Crosstalk usually occurs in the voice-grade frequency range and is typical of unshielded twisted pair wires in telephony.

CSDC—Circuit Switched Digital Capability. CSDC is an AT&T-designed service, implemented within the BOCs, that offers users a 56-Kbit/s digital channel on a user-switchable basis. It uses the same local loop as for analog voice, but without loading coils. The user first sets up the analog circuit, then switches to digital mode. CSDC employs time-compression multiplexing over a local loop.

CVSD—Continuous Variable-Slope Delta modulation. CVSD is a speech encoding and digitizing technique that uses a one-bit sample to encode the difference between two successive signal levels. Sampling is usually done at 32,000 times per second, though some implementations employ lower sampling rates.

D3—D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (Digital-to-Analog) Converter—Convert a digital word to an analog value.

dB (Decibel)—A power or voltage-level measurement unit.

dBm—The decibel signal level referred to one milliwatt, i.e., 0 dBm = 1 mW.

dBmO—Signal power measured at a point in a standard test tone level at the same point, i.e., dBmO = dBm - dBr, where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp—Circuit noise in dBmO, measured on a line with a noise measuring set having psophometric weighting.

dBr—Relative to point of zero transmission level.

dBrn—Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = -90 dBm.

dBrnC—Indicates dBrn measurement made with a C-message weighting filter. These units are most commonly used in the U.S., where psophometric weighting is rarely used.

dBrnc0—Noise measured in dBrnc referenced to zero transmission level.

Decoder (PCM Receiver)—A device which performs repeated D/A conversion, expansion and the sample-and-hold function necessary to convert a serial stream of PCM samples to a sample-and-hold equivalent of the originally encoded analog signal. See Codec and Decoding.

Decoding—A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Dedicated Line—A dedicated circuit, a nonswitched channel, or a private line.

Delay—In communications, the wait time between two events, such as from when a signal is sent until it is received.

Demodulator—A functional section of a modem that converts received analog line signals to digital form.

Dial-Up—Describes the process of, or the equipment or facilities involved in, establishing a temporary connection via the switched telephone network.

Digit—A member selected from a finite set. Note that in digital transmission, a digit may be represented by a signal element, being characterized by the dynamic nature, discrete condition and discrete timing of the element, e.g., it may be represented as a pulse of specified amplitude and duration.

Digital—Digital refers to communications procedures, techniques, and equipment where information is encoded as either

a binary "1" or "0". It is the representation of information in discrete binary form, discontinuous in time, as opposed to the analog representation of information in variable, but continuous, waveforms.

Digital Loopback—A technique for testing the digital processing circuitry of a communications device. It may be initiated locally, or remotely via a telecommunications circuit. The device being tested will echo back a received test message, after first decoding and then re-encoding it, the results of which are compared with the original message.

Digital Multiplex Equipment—Equipment for combining, by time division multiplexing (multiplexer), a defined integral number of digital input signals into a single digital signal at a defined digit rate and also for carrying out the inverse function (demultiplexer).

Digital Signal—A signal constrained to have a discontinuous characteristic in time and a set of permitted discrete values.

Digital Switching—The process of establishing and maintaining a connection, under stored program control, where binary-encoded information is routed between an input and an output port. Generally, a "virtual" through circuit is derived from a series of time slots (time-division multiplexing), which is more efficient than requiring dedicated circuits for the period of time that connections are set up.

Digital Telephone—A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. Note that it will normally multiplex 64 Kbps voice and separate data inputs at multiples of 8 Kbps.

Distortion—The failure to reproduce an original signal's amplitude, phase, delay, frequency, etc. characteristics accurately.

DPSK—Differential Phase Shift Keying. DPSK is a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180° and 270° to define the digital information.

Dry Line—A telephone line without battery voltage present.

DTMF—Dual Tone Multi-Frequency (dialing).

Duplex—A mode of operation permitting the simultaneous two-way independent transmission of telegraph or data signals.

Echo—In communications, the reflection back to the sender of transmitted signal energy. The amount of delay in an echo depends on the distance from the transmitter to the point of reflection.

Echo Cancellation—A technique being used in new higher-speed analog-line modems, that allows for the isolation and filtering out of unwanted signal energy resulting from echoes, from the main transmitted signal.

Echo Suppressor—A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM)—A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Envelope Delay Distortion—Envelope delay is the derivative of the circuit phase shift (in radians) with respect to frequency (radians per second). The deviation of this derivative at any frequency from the derivative's value at a prescribed frequency (usually 1800 Hz) is called envelope delay distortion (EDD).

Equalizer—An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

Equivalent Bit Rate—In a line-coded signal, the number of binary digits that can be transmitted in a unit of time.

Error Ratio—A measure for the distortion of a digital signal is the error rate which is defined as the number of wrongly received bits divided by the total number of received bits.

Expansion—Expansion of a compressed signal back to its original dynamic range. See Companding.

FDM—Frequency-Division Multiplex. A process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

FDX—Full duplex.

Flag—In communications, a bit pattern of six consecutive "1" bits (character representation is 01111110), used in many bit-oriented protocols to mark the beginning (and often also the end) of a frame.

Four-Wire Circuit—A circuit with two pairs of conductors, one pair for the "go" channel and one pair for the "return" channel.

Frame—A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Frame Alignment—The state in which the frame of the receiving equipment is correctly phased with respect to that of the received signal.

Frame Alignment Signal—The distinctive signal used to enable frame alignment to be secured.

Frame Alignment Time Slot—A time slot starting at a particular phase in each frame and allocated to the transmission of a frame alignment signal.

Frequency Modulation (FM)—A method used to encode a carrier wave by varying the frequency of the transmitted signal.

FSK—Frequency-Shift Keying. A modulation technique where two different tones represent either the "0" or the "1" state of binary information.

Full Duplex—A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain—The increase in signal amplitude realized when a signal passes through an amplifier or repeater (normally measured in decibels).

Gain Level Linearity (Gain Tracking)—A measurement of the dependence of a device gain on signal level. The output signal is compared to the input signal (assuming unity gain) over a range of input signals. The variation of gain from a constant gain (determined at 0dBm input level) is the gain tracking error.

Gaussian Noise—Undesirable random electrical energy that is introduced into a transmission channel from the environment. It is generally of low amplitude but may still occasionally interfere with a carrier signal. Also known as electrical background noise.

Ground Start—A telephony term describing a signaling method where one station detects that a circuit is grounded at the other end.

Half-Duplex—A mode of operation permitting transmission of information between two locations in only one direction at a time.

HDB-3 Code, High Density Bipolar 3 Code—In this code, two consecutive ones of the same polarity are permitted (interrupting a zero sequence which is too long). These violation bits, moreover, are arranged to form an AMI sequence in itself.

Highway—A common path or a set of parallel paths over which signals from a number of channels pass with separation achieved by time division.

Hybrid—A bridge-type circuit or connecting device that combines the function of providing impedance matching between certain circuits and isolation between other circuits. A hybrid is often used to connect four-wire lines to a two-wire line so that in both directions of transmission the four-wire lines are isolated from each other, but are connected to the two-wire line.

Idle Channel Noise (ICN)—The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide-band noise measurement using a C-message weighting filter to band-limit the output noise).

Interface—A shared boundary. A physical point of demarcation between two devices, where the electrical signals, connectors, timing and handshaking are defined. It is also the procedure, codes, and protocols that enable two entities to interact for the meaningful exchange of information.

Intermodulation—The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation Distortion—An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

ISDN—Integrated Services Digital Network. A future communication network intended to carry digitized voice and data multiplexed onto the public network.

IVDT—Integrated Voice/Data Terminal. One of a relatively new family of devices that features a terminal keyboard/display and voice telephone instrument. It may contain varying degrees of local processing power, ranging from full personal computer capacity to directory storage for automatic telephone dialing. May also be designed to work with a specific customer premises PBX, or else be PBX independent.

Jitter—A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission error, particularly at high speeds. The variation can be in amplitude, time, frequency or phase.

Justification (Pulse Stuffing)—A process of changing the rate of a digital signal in a controlled manner so that it can accord with a rate different from its own inherent rate, usually without loss of information.

Kbit/s—Kilobits per seconds; a standard measure of data rate and transmission capacity.

Key System—A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-Law—A companding law accepted as the North American standard for PCM based systems.

LAN—Local Area Network; a data-only communications network between data terminals using a standard interface to the network.

Line Code—A code chosen to suit the transmission medium and giving the equivalence between a set of digits generated in a terminal of other processing equipment and the pulses chosen to represent that set of digits for the line transmission.

Load Capacity (Overload Point)—In PCM, the level expressed in dBm0, of a sinusoidal signal the positive and negative peaks of which coincide with the positive and negative virtual decision values of the encoder.

Loading—A process of adding inductance to a transmission line to minimize amplitude distortion. It is generally accomplished with loading coils.

Local Loop—In telephony, the wire pair that connects a subscriber to a phone company end office. It typically contains two wires, though four-wire local loops are common, especially with leased voice-grade circuits.

Local Network—A type of high-speed data communications arrangement wherein all segments of the transmission medium (typically, coaxial cable, twisted-pair wire, or optical fiber) are under the control of the network operator. Also referred to as LAN for local-area network.

Longitudinal Balance—The common-mode rejection of a telephone circuit.

Loopback—Directing signals back toward the source at some point along a communication path.

Loop Resistance—The loop resistance of a cable pair is the dc resistance from the telephone office to a distant point. It may include a coil at the far end. If no coil is present, a short must be placed across the tip and ring. Corrections for temperature variations from 68°F must be made to the measured dc resistance in order to determine if the loop resistance is correct.

Loop Start—The most commonly used method of signaling an off-hook condition between an analog phone set and a switch, where picking up the receiver closes a wire loop, thus allowing DC current to flow, which is detected by a PBX or central office switch and interpreted as a request for service.

Loss—A reduction in signal strength, expressed in decibels. Also attenuation, opposite of gain.

Low Pass—A specific frequency level, below which an analog filter will allow all frequencies to pass; opposite of high-pass.

LRC—Longitudinal Redundancy Check.

Master Clock—A clock which generates accurate timing signals for the control of other clocks and possible other equipments.

MCU—MicroComputer Unit (Also MicroController Unit).

Modem—MOdulator-DEModulator. The modem is a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Modified Alternate Mark Inversion—An AMI signal which does not strictly conform with alternate mark inversion but includes violation in accordance with a defined set of rules.

MPU—MicroProcessor Unit.

Mu Law—A companding/encoding law commonly used in the U.S. (same as μ-Law).

Multiframe—A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal. The multiframe signal does not necessarily occur, in whole or in part, in each multiframe.

Multiplex—To simultaneously transmit two or more messages on a single channel.

Multiplexing—The process of combining multiple signals into a single channel for transmission over common facilities.

Mux—Multiplex or multiplexer.

Mux, 30-Channel (U.K. & Europe)—CCITT recommended form for PCM multiplex equipment. Consists of 8-digit A-Law, 30

speech channels plus two utility channels (32 time slots in all), and a transmission rate of 2,048 kbit/s.

Mux, 24-Channel (U.K.)—Early PCM multiplex equipment. Consists of 7-digit A-Law, one signaling bit associated with each time slot, 24 channels (time slots), and a transmission rate of 1536 Kbit/s.

Noise—Any extraneous and unwanted signal disturbances in a communications link (e.g., electromagnetic interference, or EMI). Usually experienced as random variations in signal voltage or current, or interfering signals.

Non-Synchronous Network (Asynchronous Network)—A network in which the clocks need not be synchronous or mesochronous.

Off-Hook—The circuit condition resulting when the handset is lifted from the hook switch of the telephone set; i.e., a low dc impedance is placed across the line causing loop current flow that is recognized by a relay at the central office as a request for service.

Off-Line—The condition in which a user, terminal, or other device is not connected to a computer, or is not actively transmitting via a network.

On-Hook—The circuit condition resulting when the handset of a telephone is replaced on its cradle (high dc impedance).

On-Line—The condition in which a user, terminal, or other device is actively connected with the facilities of a communications network or computer.

PABX—Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Packet—A sequence of data, with associated control elements, that is switched and transmitted as a whole. Packet refers mainly to the field structure and format defined within the CCITT X.25 recommendation. Multiple packets may be required to carry one complete document or a lengthy block of information.

PAD—Packet Assembler/Disassembler; a network interface device that allows multiple asynchronous and/or synchronous terminals or host computer ports to interface to a packet-switching network. It is also a protocol conversion device that allows user terminals not equipped for packet switching to communicate over an X.25-based channel. May also be used to allow connected user stations to open and close sessions with a remote host and to set specific transmission parameters. PAD operation and functions are fully delineated in CCITT recommendations.

PBX—Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM Binary Code—A pulse code in which the quantized values are identified by binary numbers taken in order. Note that this term should not be used for line transmission.

PCM Multiplex Equipment—Equipment for deriving a single digital signal at a defined digit rate from two or more analog channels by using a combination of pulse code modulation and time-division multiplexing (multiplexer), and also for carrying out the inverse function (demultiplexer). The description should be preceded by the relevant equivalent binary digit rate, e.g., 2048 Kbit/s PCM multiplex equipment.

Peak Limiting—In PCM, the effect caused by the application to an encoder of an input signal whose value exceeds the virtual decision values of the encoder.

Phase Jitter—In telephony, the measurement, in degrees out of phase, that an analog signal deviates from the referenced phase of the main data-carrying signal. Phase jitter is often caused by alternating current components in a telecommunications network.

Port—A point of access into a computer, a network, or other electronic device. It is also the physical or electrical interface through which one gains access, or the interface between a process and a communications or transmission facility.

Primary Block (American: Digroup)—A basic group of PCM channels assembled by time-division multiplexing.

Propagation Delay—The time interval between specified reference points on the input and output voltage waveforms.

Protocol—A formal set of rules which govern the format, timing, sequencing, and error control of exchanged messages on a data network. It may also include facilities for managing a communications link and/or contention resolution. A protocol may be oriented toward data transfer over an interface, between two logical units directly connected, or on an end-to-end basis between two end users over a large and complex network.

Psophometric Weighting—A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

Pulse Code Modulation (PCM)—A process in which an analog signal is sampled, and the magnitude of each sample with respect to a fixed reference is quantized and converted by coding to a digital signal. This is the prevalent technique for digital transmission in communications systems.

Pulse Dialer—A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

Quantizing—A process in which samples are classified into a number of adjacent intervals (amplitude steps), with each interval step being represented by a single value called the quantized value.

Quantizing Distortion—Due to the restriction of a finite number of produced amplitude steps, a difference occurs between the information which can be transmitted and the original information. This difference is called quantizing distortion.

Quantizing Distortion Power—The power of the distortion component of the output signal resulting from the process of quantizing.

Queuing—In telephony, a feature that allows calls to be "held" or delayed at the origination switch while waiting for a trunk to become available. It is also the sequencing of batch data sessions.

Regeneration—The process of recognizing and reconstructing a digital signal so that the amplitude, waveform and timing are constrained within stated limits.

Repeater—An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory Dialer—A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Return Loss (RL)—The return loss of a circuit is a measure of the amount of transmitting current which is transferred to the receiver at the same location due to impedance mismatches. The higher the ratio in dB, the better the return loss.

Sample—The value of a particular characteristic of a signal at a chosen instant.

Sampled Data System—A system that operates on samples of the analog input signals. It can be either analog (e.g.,

switched capacitor filter) or digital (speech coding/digital filter) processing or both.

SCU—Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Segmented Encoding Law—An encoding law where an approximation to a smooth law is obtained by a number of linear segments.

Signaling—The transmission of control or status information between switching systems in the form of dedicated bits or channels of information which is inserted on trunks with voice data.

Signaling Time Slot—A time slot starting at a particular phase in each frame and allocated to the transmission of signaling.

Signal-To-Distortion Ratio (S/D)—The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 KHz sinusoid) is eliminated from the output signal (e.g., by filtering).

Single Channel Codec—A codec which is designated to operate on a single signal source and not in a multiplexed mode which performs the codec function for more than one signal source.

Single Chip Codec—A single integrated circuit capable of performing all codec functions and in some cases providing an auxiliary signaling interface. It may be either single channel or multiplexable.

SLIC—Subscriber Line Interface Circuit; a device that performs the 2-4 wire conversion, battery feed and other line interface functions on a subscriber telephone line.

Smoothing (Decode or Reconstruction) Filter—Usually low pass. Restores the desired analog signal at the S & H, D/A or decoder output by blocking high frequency components produced by sampling.

Subscriber Line—The permanent connection between a station and the switching center that serves it.

Syn (Sync)—A bit or character used to synchronize a time frame in a time-division multiplexer. Also, a sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous—Two signals are synchronous if their corresponding significant instants have a specific phase relationship.

Synchronous Modem—A modem that uses a derived clocking signal to perform bit synchronization with incoming signals.

Synchronous Network—A network in which the clocks are controlled so as to run, ideally, at identical rates, or at the same mean rate with limited relative phase displacement.

Synchronous Transmission—A mode of digital transmission in which discrete signal elements (symbols) are transmitted at a fixed and continuous rate.

T Carrier—A time-division multiplexed, typically telephone company-supplied, digital transmission facility, usually operating at an aggregate data rate of 1.544 Mbit/s and above.

T1 Carrier—A PCM system operating at 1.544 Mbit/s and carrying 24 individual voice-frequency channels.

T1C—AT&T term for a digital carrier facility used to transmit a DS-1C formatted digital carrier signal at 3.152 Mbit/s.

T2—AT&T term for a digital carrier facility used to transmit a DS-2 formatted digital carrier signal at 6.312 Mbit/s.

Telco—Telephone Central Office, in most usages; but also, a generic abbreviation for telephone company.

Tie Line—A leased or private dedicated telephone circuit provided by common carriers that links two points together without using the switched telephone network.

Time Division Multiplexing (TDM)—Interleaving digital data from many users onto one or two serial communications links by dividing channel capacity into time slices.

Time Slot—Any cyclic time interval which can be recognized and defined uniquely.

Timing Recovery (Timing Extraction)—The derivation of a timing signal from a received signal.

Timing Signal—A cyclic signal used to control the timing of operations.

Tip (T) and Ring (R)—Terms used to identify the two conductors of a telephone circuit. These terms originate from switchboard terminology for cord circuits, in which a four-wire circuit is designated T1, T2, and R1 and R2.

Transceiver—Generic term describing any device, usually a terminal, that can both transmit and receive.

Transients—Intermittent, short-duration signal impairments.

Translator—In telephony, a central office device that converts dialed or tone digits into call-processing information.

Transmission—The dispatching of a signal, message, or other form of intelligence by wire, radio, telegraphy, telephony, facsimile, or other means (ISO). It consists of a series of characters, messages or blocks, including control information and user data. Also referred to as the signaling of data over communications channels.

Transmultiplexer—An equipment which transforms signals derived from frequency-division multiplex equipment to time-division multiplexed signals having the same structure as those derived from PCM multiplex equipment and vice versa.

Transparent Mode—Typically bisync data transmission where the recognition of control characters is suppressed. Also the operation (usually) of a digital transmission facility such that the user has complete and free use of the available bandwidth; generally implies out-of-band signaling.

Trunk—A telephone circuit or channel between two central offices or switching entities.

Trunk Exchange—A telephone exchange dedicated primarily to interconnecting trunks.

Trunk Group—Multiple trunk circuits between the same two switching centers that can be accessed by dialing a single trunk number and use the same multiplexing equipment at both ends.

T-Span—A telephone circuit or cable through which a T-carrier runs.

Twist—The amplitude ratio of a pair of DTMF tones. Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.

Two-Wire Circuit—A circuit with two conductors providing "go" and "return" channels.

Virtual Decision Value—Two hypothetical decision values, used in quantizing or encoding. Located at the ends of the working range used, and obtained by extrapolation from the real decision values. Effectively specifies the maximum input signal amplitude.

Voice Digitization—The conversion of an analog voice into digital symbols for storage or transmission.

Voice Frequency—A frequency within that part of the audio range that is used for the transmission of speech of commercial quality, i.e., 300-3400 Hz.

Voice-Grade Channel—A telecommunications circuit used primarily for speech transmission but suitable for the transmission of analog or digital data, or facsimile. It typically supports a frequency range of 300 to 3400 Hz.

Weighting Filters—Several different filters have been used to represent the transmission pass-band characteristics of different communications networks. The two most frequently used are C-message (North America) and Psophometric (Europe) weighting filters.

Wet Line—A telephone line with battery voltage present.

Working Range—The permitted range of values of an analog signal over which a transmission or other processing equipment can operate.

Zero Transmission Level Point (OTLP)—An arbitrary point in a transmission system to which all relative levels at other points in the system are referred. The OTLP is usually the transmitting toll switchboard or testboard.

G24002

Microcircuits

Subscriber Line Interface Circuit (SLIC) — Interface IC

Features

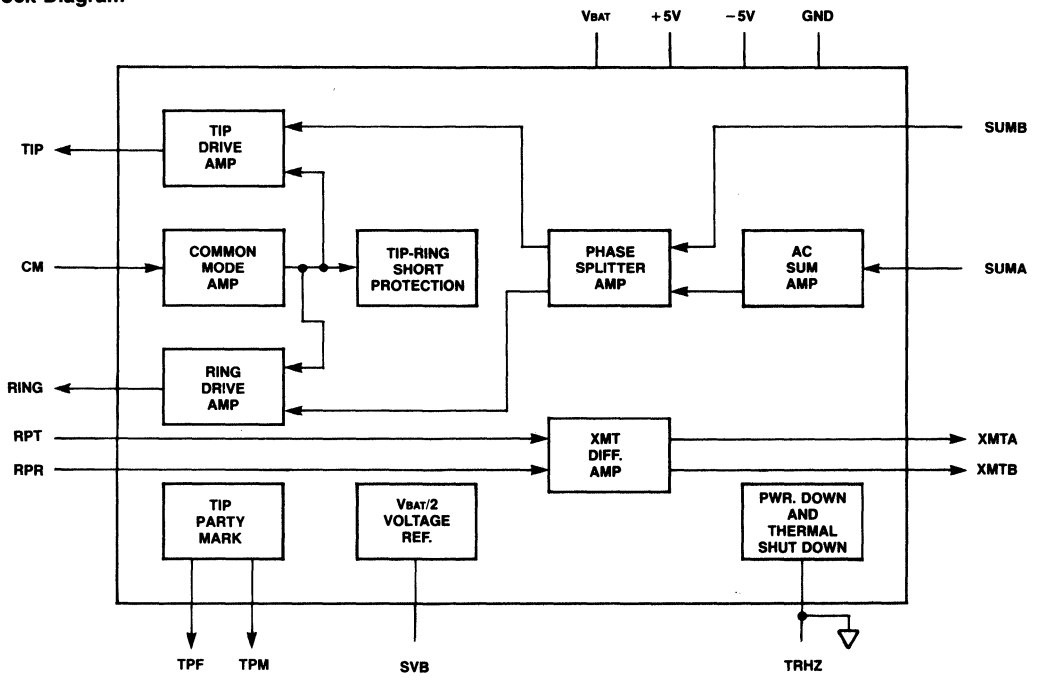
- Advanced Dielectrically Isolated Bipolar Monolithic technology
- Meets both North American and LSSGR Central Office Transmission and Signaling Standards
- Provides SLIC interface and BORSHT functions
- Longitudinal balance of 59 dB or greater
- Tip Party Mark detection
- Tip/Ring to ground or battery short circuit detection
- Thermal shutdown circuit
- Source/sink current capability (117 mA at Tip and Ring)
- Program-controlled power reduction in Idle mode
- Available in 28-pin DIP or PLCC package

General Description

GTE Microcircuits' G24002 SLIC Interface IC is a High Voltage Dielectrically Isolated Bipolar Monolithic LSI circuit designed to provide a direct interface to a telephone subscriber loop. The Interface IC is designed to function in combination with the GTE G24010 SLIC Control IC. This two-chip set, when combined with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications. The two-chip set provides BORSHT functions which include:

- Floating-polarity battery feed with controlled loop current
- Overvoltage protection (external)
- Ringing
- Supervision/signaling
- 2 to 4 wire hybrid conversion
- System testing
- Microcomputer control logic interface
- Hybrid software selectable networks (one-of-three)

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

The Interface IC provides battery feed, Tip and Ring current sourcing functions, Tip and Ring short protection, Tip Party Mark sensing, thermal shutdown, overvoltage protection and a direct interface to the telephone subscriber loop. Its companion IC, the G24010 Control IC, provides all necessary control outputs for driving Ringing and Testing relays, as well as other user-defined relay options. It also provides standard Ring-Trip, Loop Sense and Ground Start detection circuits, plus a DC Loop Control circuit which feeds the G24002 Interface IC to guarantee correct Tip and Ring voltages. The Control IC also contains a parallel I/O Logic Control Interface bus which can be interfaced to a system microcomputer or other control device. The Logic Interface allows external control of the various SLIC functions, including: Cut-Over functions, Tip Ground, Testing, Ringing, and Ring Trip Disable.

Absolute Maximum Ratings (Note 1)

Ratings	Symbol	Value
Supply Voltage	V_{DD} V_{SS} V_{BAT}	+6V −6V −60V
DC Loop Current	I_{LOOP}	65 mA
Operating Temperature	T_A	0°C to +70°C
Storage Temperature	T_S	−40°C to +85°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

Operating Characteristics: V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, V_{BAT} = −50V ±6V, TRHZ = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Units
Supply Current (THRZ = 0V, V_{BAT} = −50V)	I_{DD} I_{SS} I_{VB}	— — —	1.0 0.9 4.5	mA mA mA
Logic Interface				
Input Low Voltage (P_{IN} = TRHZ)	V_{IL}	—	0.8	V
Input High Voltage	V_{IH}	2.4	—	V
Input Low Current (0 ≤ V_{IN} ≤ 0.8V)	I_{IL}	—	100	μA
Input High Current (2.4 ≤ V_{IN} ≤ V_{DD})	I_{IH}	—	400	μA
Output Low Voltage (I_L = 10 μA)	V_{OL}	—	0.4	V
Output High Voltage (I_L = −10 μA)	V_{OH}	4.0	—	V
Battery Feed				
Feed Voltage (V_{BAT} = −50V)	V_T–V_R			
SUMB = 3.5V		33.5	35.8	V
SUMB = 1.0V		8.96	10.86	V
SUMB = 0.0V		−0.87	+0.87	V
SUMB = −1.0V		−10.8	−9.1	V
SUMB = −3.5V		−35.5	−33.9	V
DC Loop Control Output (V_{BAT} = −50V)	XMTB			
SUMB = 3.5V		−0.5	−0.4	V
SUMB = 1.0V		−1.27	−1.18	V
SUMB = 0.0V		−1.58	−1.48	V
SUMB = −1.0V		−1.88	−1.79	V
SUMB = −3.5V		−2.70	−2.55	V
V_{BAT}/2 Filter Output (V_{BAT} = −50V, SUMB = 0)	VBF	−25.15	−24.85	V
Scaled V_{BAT}/2 (V_{BAT} = −50V, SUMB = 0)	SVB	−3.4	−3.2	V
Common Mode DC Input (V_{BAT} = −50V, SUMB = 0)	VCM	−25.1	−24.9	V
Tip Overhead Voltage (V_{BAT} = −50V, SUMB = 0)	VAT	−2.2	—	V
Ring Overhead Voltage (V_{BAT} = −50V, SUMB = 0)	VAR	—	−47.8	V
Tip/Ring Short to Ground or V_{BAT} (V_{BAT} = −50V, SUMA = 1V, V_T and V_R connected to −25V thru 100 Ω)				
VCM = −18.7		−26	−24	V
VCM = −19.7		−40	−38	V
VCM = −30.3		−12	−10	V
VCM = −31.3		−26	−24	V

AC Transmission

Insertion Loss (R_{T-R} = 500 ohms, f = 1000 Hz)				
2-Wire to 4-Wire	G_{TX}	−6.22	−5.92	dBV
4-Wire to 2-Wire	G_{RCV}	−2.64	−2.34	dBV
Level Linearity	G_{LIN}			
+3 to −37 dBmO		—	±0.25	dB
−37 to −50 dBmO		—	±0.50	dB
2-Wire Return Loss	RL_{2W}			
200 Hz to 500 Hz		21	—	dB
500 Hz to 3400 Hz		27	—	dB
4-Wire Return Loss (Loaded/Non-Loaded 900/2.16 μF)	RL_{4W}			
200 Hz to 500 Hz		20	—	dB
500 Hz to 2500 Hz		25	—	dB
Longitudinal Balance (2-Wire, 200 Hz to 3000 Hz)	LB_{2W}	59	—	dB
Transfer Balance (4-Wire, 200 Hz to 3000 Hz)	LB_{4W}	59	—	dB
Idle Channel Noise (T-R Terminated 900/2.16 μF)	N_{TX}	—	2	dBrnc
Idle Channel Noise (RCV = GND)	N_{RC}	—	2	dB
Harmonic Distortion (f = 1000 Hz)	2nd HAR.	−48	—	dBv
	3rd HAR.	−52	—	dBv
Power Supply Rejection (f = 1000 Hz)	P_{SRR}	−50	—	dB

Functional Description

The G24002 SLIC Interface IC is designed to be used in combination with the G24010 SLIC Control IC. This two-chip set, when combined with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications.

The G24002 Interface IC provides battery feed, Tip and Ring current sourcing short protection, Tip Party Mark sensing, Thermal Shutdown and Overvoltage Protection, as well as a direct interface to the telephone subscriber loop. Its companion circuit, the G24010 Control IC, provides all remaining SLIC functions, including control outputs for driving Ringing, Testing and other user-defined relays, standard Ring-Trip, Loop Sense, and Ground Start detection circuits, plus a DC Loopback Control circuit to guarantee correct Tip and Ring voltages at the G24002 Interface IC. The Control IC also contains a parallel I/O Logic Control Interface bus for interfacing to a system microcomputer or other control device. The Logic Interface allows external control of various SLIC functions, including Cut-Over functions, Tip Ground, Testing, Ringing, and Ring-Trip Disable. Following is a description of the various SLIC Interface IC functions:

Subscriber Loop Environment

The subscriber loop consists of a 2-wire twisted pair (Tip and Ring), connected directly to the subscriber telephone set or other equivalent device. When the telephone is off-hook, the Interface IC applies a DC feed voltage across the Tip and Ring lines, resulting in DC loop current flow between the Tip and Ring feed connections. In this off-hook condition, both incoming and outgoing voice signals are superimposed on the DC feed voltage. In contrast, during an on-hook condition, the DC feed current path is opened, thus interrupting the flow of loop current. The Interface IC senses loop current status, and conveys any off-hook condition to the Central Office Switch or PABX via the G24010 Control IC.

In actual applications, the subscriber loop resistance may vary from 400 ohms (telephone set resistance) for short lines, to as much as 2000 ohms for long lines. To control power dissipation and loop current over short lines, a DC Loop control circuit (within the G24010 Control IC) is used. Depending on the loop length and its location with respect to AC power lines, undesirable longitudinal currents are often induced onto the subscriber line. These longitudinal currents are rejected by the Interface IC which transmits only the differential mode voice signal. Any common mode signal induced by the longitudinal currents are attenuated by 59 dB or better. The Interface IC is capable of accommodating up to 40 mA rms longitudinal induced currents on the Tip or Ring side of the loop.

The ringing function is performed by activating a Ring Relay which connects a ring generator to the loop, thus making the loop connection. This function is performed by the G24010 Control IC. Once the loop connection has been made and the subscriber answers the telephone, the Interface IC is ready for voice transmission. Voice transmission is accomplished by the Control IC, using a 2-wire to 4-wire switched-capacitor network. The switched-capacitor network selects from three different types of line networks, namely loaded, non-loaded and 9:2. This 2-wire to 4-wire conversion is referred to as the hybrid function.

To protect the SLIC circuits from lightning strikes, a bridged diode network is used across the Tip and Ring connections.

Tip Drive Amplifier

The Tip Drive Amplifier is a precision transconductance amplifier which provides DC and AC current feed to the Tip side of the subscriber loop. The Tip Drive Amplifier is capable of sinking or sourcing 117 mA and has a transconductance of 4 mA/V. The transconductance is set by an external resistor.

Ring Drive Amplifier

This amplifier functions identical to the Tip Drive Amplifier, except that it provides DC and AC current feed to the Ring side of the subscriber loop.

Common Mode Amplifier

The Common Mode Amplifier (biased at $V_{BAT}/2$) senses and amplifies the common mode voice signal across the Tip and Ring connections. This common mode signal, $(V_T + V_R)/2$, is amplified by a factor of 3.33 and fed to the Tip and Ring Drive Amplifiers. The function of this amplifier is to synthesize a longitudinal (common mode) input impedance of virtual AC ground at the Tip and Ring connections.

Tip/Ring Short Protection
This detector circuit monitors the output of the Common Mode Amplifier. Should the output become within 7.75 volts of either ground or VBAT, the Tip and Ring Drive Amplifiers are placed into a high-impedance state. This voltage threshold represents a short of Tip and/or Ring to ground or VBAT. When placed in the high-impedance state, drive current is removed from the loop.

AC Summing Amplifier
The function of this amplifier is to provide the sum of the received voice signal and the transmit voice signal. The transmit voice signal is fed back to the circuit in order to synthesize the Tip and Ring input impedance to 900: 2.16 μF. Signal SUMA represents the ground referenced summing voltage. Amplifier gain is set by the use of external resistors.

Phase Splitter Amplifier
The function of this amplifier is two-fold. First, it sums the DC signal SUMB with the voice signal, and second, it level shifts the combined (summed) signals and converts the single-ended input into two outputs (balanced around VBAT/2). These two outputs are equal in amplitude, but 180 degrees out of phase.

XMT Differential Amplifier
This amplifier is used to amplify the difference between the Tip line and Ring line voltages. The output (XMTA) is used to synthesize the input impedance (900 ohms) across the Tip and Ring lines, and to drive the transmit input (XMTA) of the G24010 Control IC. Note that the scaled-down output (XMTB) is used by the Control IC for DC loop control functions.

Tip Party Mark (TPM)
This detector circuit is used to sense a difference voltage between the Common Mode Amplifier output and VBAT/2. When a difference is sensed, it generates the logic output (TPM). Under normal operating conditions, the Common Mode Amplifier output is equal to VBAT/2. However, when a Tip Party Mark is placed on the line, Tip current will not be equal to Ring current, thus causing the Common Mode Amplifier output to deviate from VBAT/2. This deviation will trip the detector and produce a TPM output.

VBAT/2 Voltage Reference
This circuit generates the VBAT/2 reference voltage for use within the Interface IC.

Power-Down and Thermal Shut-Down
The Power-Down circuit controls power dissipation within the Interface IC. When the TRHZ input is true (logic 1), all internal amplifiers are placed into a high-impedance state. Output drive current and internal bias current is totally shut off, thus reducing power consumption to a minimum.

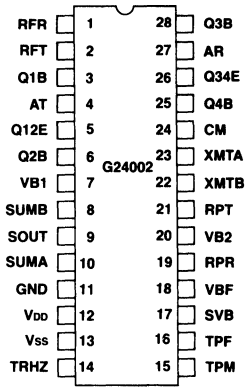
The Thermal Shut-Down circuit senses the temperature of the Interface IC. Should it reach 125°C, all internal amplifiers are shut down and power dissipation is reduced to a minimum.

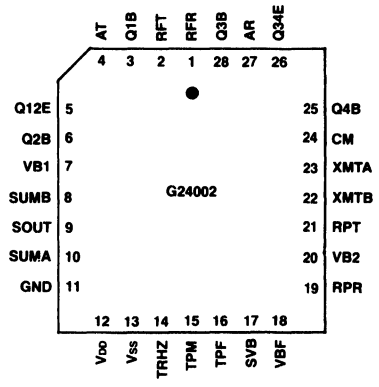
Pin Function Table

Pin	Description
AR	Output of Ring Drive Amplifier
AT	Output of Tip Drive Amplifier
CM	Common Mode Feedback Input from Tip and Ring
Q1B	Connection to Base of External NPN Transistor Q1
Q12E	Connection to Emitters of Transistors Q1 and Q2
Q2B	Connection to Base of Transistor Q2
Q3B	Connection to Base of Transistor Q3
Q34E	Connection to Emitters of Transistors Q3 and Q4
Q4B	Connection to Base of Transistor Q4
RFR	Connection to Ring Line Gm Setting Resistor
RFT	Connection to Tip Line Gm Setting Resistor
RPR	Ring Line Transmit Input
RPT	Tip Line Transmit Input
SUMA	Summing Amplifier Inverting Input

Pin	Description
SUMB	DC Loop Current Control Input
SOUT	Summing Amplifier Output
SVB	Scaled-Down VBAT/2 Output
THRZ	Logic Input to Place IC in High Impedance State
TPF	Tip Party Mark Filter Pin Source (Z = 110K ohms)
TPM	Tip Party Mark Detector Output
VB1	Battery Supply (−50V)
VB2	−50V Battery Supply for Input Protection Diodes
VBF	VBAT/2 Filter Pin (Source Z = 75K ohms)
XMTA	Transmit Output to SLIC Control IC
XMTB	Scaled-Down Transmit Output for DC Loop Control
GND	Ground
VDD	+5.0V Power Supply
VSS	−5.0V Power Supply

Pin Configuration





Applications

Figures 1 and 2 represent a typical application where the G24002 Interface IC is used in conjunction with the G24010 Control IC to form a Subscriber Loop Interface Circuit (SLIC). The addition of a PCM Codec/Filter to this circuit would result in a highly efficient Line Card for use at a Central Office or PABX station.

A description of the various external components is as follows:

Q1 through Q4
Since the G24002 Interface IC is a high voltage, low current device, four external emitter followers are required to drive the Tip and Ring terminals. For a 2000 ohm loop resistance, each transistor dissipates approximately 130 mW; for a loop resistance of 500 ohms, each transistor dissipates approximately 600 mW.

RF1 and RF2
These two resistors are used in conjunction with the Tip and Ring Drive Amplifier. These resistors, in combination with internal matched resistor pairs, serve to configure the Drive Amplifier into a transconductance amplifier with a transconductance of 4 mA/V.

RP1, RP2 and DB
RP1 and RP2, along with the Diode Bridge (DB), provide lightning protection.

RCM1 and RCM2
These two resistors serve to combine the Tip and Ring voltages, thus providing a common mode signal to an internal Common Mode Amplifier.

RIN1 and RIN2
These resistors, in combination with internal resistors, form the internal XMT Differential Amplifier.

RG1, RG2 and RSF
These are gain-setting resistors for the RCV signal, as received from the PCM Codec/Filter and XMTA signal.

CZIN
CZIN, along with RG1, provides a feedback path for the signal which appears across Tip and Ring. The purpose of this feedback is to synthesize ZIN "impedance locking" across Tip and Ring (approximately 900:2.16 μF).

CTPF and CVBF
CVBF filters out any power supply noise. CTPF filters out the AC signal components prior to the Tip Party Mark detector circuit within the G24002 Interface IC.

R1 through R4
These four resistors are used to scale down the Ring-Tip sensed signal such that it can be processed by CMOS circuits.

R5, R6 and C1, C2
These four components, in combination with an internal Op Amp, form a two-pole, low-pass filter to extract the DC component from the AC ringing voltage.

CHIT
This external capacitor, in conjunction with an internal resistor, forms a symmetrical integrator circuit. The purpose is to provide "Hit" protection, i.e., blocking pulses that are less than 10 mS in width.

CLF
This external capacitor serves as a loop-filter for the DC loop control circuit.

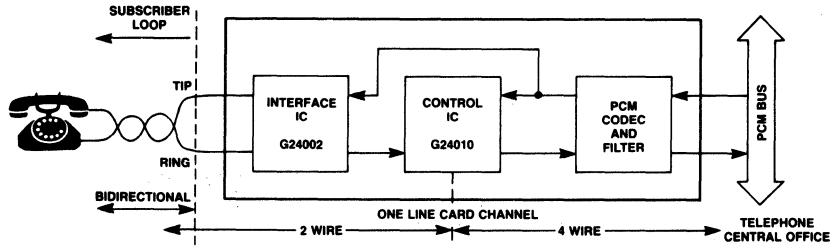


Figure 1. SLIC Line Card

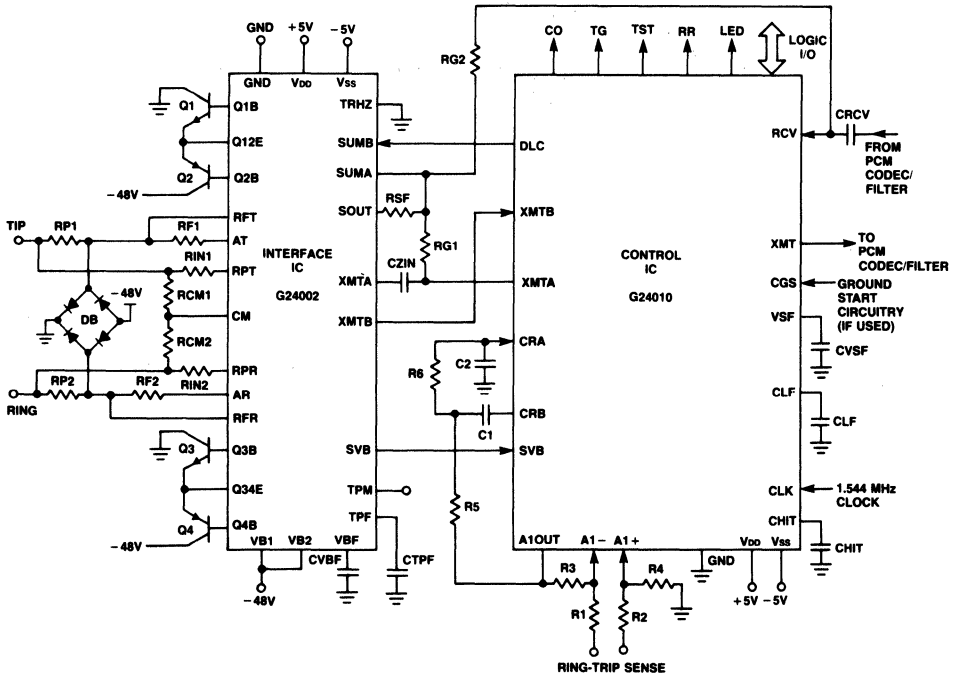


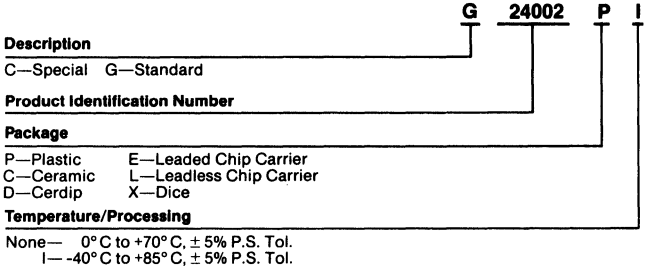
Figure 2. Typical SLIC Application

External Component List

Symbol	Value	Tolerance
R1, R2	5MΩ	±0.25% Ratio Match
R3, R4	81 14KΩ	±0.25% Ratio Match
R5, R6	237KΩ	±1%
RG1	200KΩ	±0.25%
RG2	263.3KΩ	±0.25%
RSF	110KΩ	±0.25%
RP1, RP2	24Ω	±5%
RF1, RF2	49.7Ω	±0.05% Ratio Match ±0.1% Absolute
RCM1, RCM2	150KΩ	±1%

Symbol	Value	Tolerance
RIN1, RIN2	4.42KΩ	±1%
Q1, Q3	Amperex	BSR41 Or Equivalent
Q2, Q4	Amperex	BSR31 Or Equivalent
DB1	Diode Bridge FD10290-BD	
CVBF, CTPF CHIT, CLF	0.22 μF	±10%
CZIN	0.01 μF	±1%
C1	0.47 μF	±5%
C2	0.22 μF	±5%
CRCV	0.0082 μF	±5%

Ordering Information



G24010

Microcircuits

Subscriber Line Interface Circuit (SLIC) — Control IC

Features

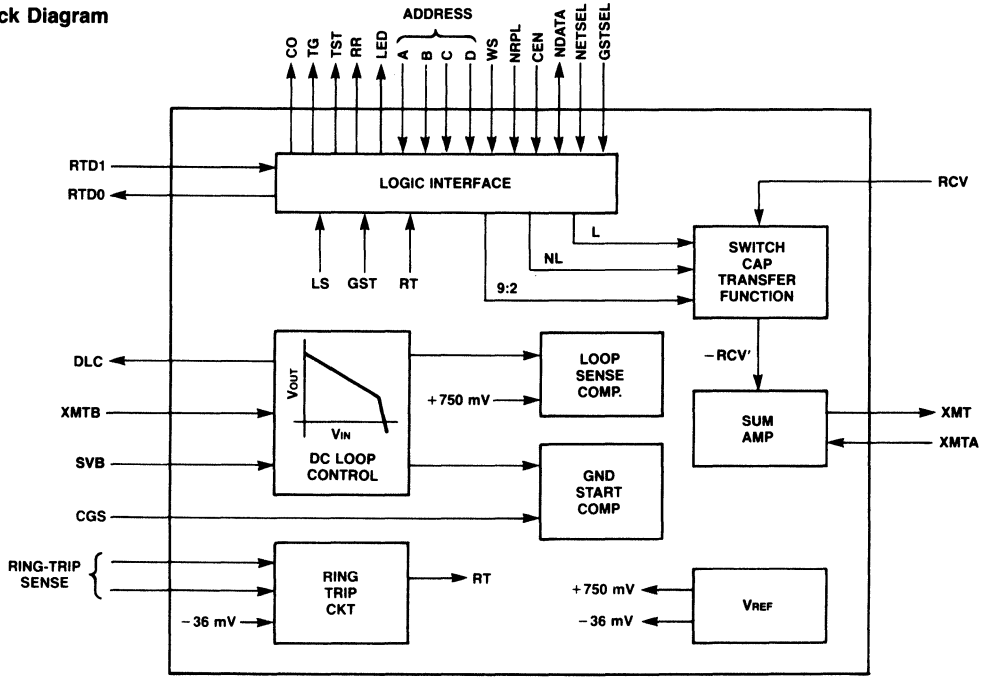
- Double-Poly CMOS Monolithic technology
- Meets both North American and LSSGR Central Office Transmission and Signaling Standards
- Provides SLIC control and BORSHT functions
- Performs 2 to 4 wire hybrid conversion with 9:2, loaded and non-loaded networks
- Logic Control Interface for off-chip microcomputer control function
- Interfaces with G24002 SLIC Interface IC and PCM Codec/Filter
- Ring-Trip Detection
- Ground Start Detection
- DC Loop Control
- Loop Sense Detection
- Available in 44-pin PLCC or 40-pin DIP package

General Description

GTE Microcircuits' G24010 SLIC Control IC is a Double-Poly CMOS Monolithic LSI integrated circuit designed to provide a three-way interface between GTE's G24002 SLIC Interface IC, a PCM Codec/Filter, and external microcomputer control. The G24010 Control IC is designed to function in combination with the GTE G24002 Interface IC. This two-chip set, in combination with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications. The combined two-chip set provides BORSHT functions which include:

- Floating-polarity battery feed with controlled loop current
- Overvoltage protection (external)
- Ringing
- Supervision/signaling
- 2 to 4 wire hybrid conversion
- System testing
- Microcomputer control logic interface
- Hybrid software selectable networks (1-of-3)

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

The G24010 Control IC provides all necessary control outputs for driving Ringing and Testing relays, as well as user-defined relay options. Standard Ring-Trip, Loop Sense and Ground Start Detection circuit functions are provided, in addition to a DC Loopback Control circuit which feeds the G24002 Interface IC to guarantee correct Tip and Ring voltages. A Line Card failure LED output is also provided, along with a special circuit for preventing false Loop Sense detection.

In addition to the above SLIC functions, a Digital Logic Control Interface is available for external control of the various G24010 internal functions, including: Cut-Over functions, Tip Ground, Testing, Ringing, and Ring-Trip Disable. SLIC operational status may also be read via the Logic Control Interface. This parallel I/O bus may be interfaced to a system microcomputer or other logic control device.

Absolute Maximum Ratings (Note 1)

Ratings	Symbol	Value
Supply Voltage	$V_{DD} - V_{SS}$	+14V
Input/Output Voltage	Vdc	V_{SS} −0.3, V_{DD} +0.3
Output Current	I_{OUT}	±50 mA
Operating Temperature	T_A	−40°C to +85°C
Storage Temperature	T_S	−65°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

Operating Characteristics: V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, SVB = −3.3V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Units
V_{DD} Supply Current (SVB = −3.3V, CLK = 1.544 MHz)	I_{DD}	—	5.0	mA
V_{SS} Supply Current	I_{SS}	—	−5.0	mA
Logic Interface				
Input Load Current (V_{IN} = 0 to V_{DD}, All Logic Inputs)	I_{LC}	−10	+10	μA
Input Low Voltage RTDI, A, B, C, D, WS, NRPL, CEN, CLK, NDATA (As Input)	V_{IL}	0	+0.8	V
Input High Voltage RTDI, A, B, C, D, WS, NRPL, CEN, CLK, NDATA (As Input)	V_{IH}	2.4	V_{DD}	V
Input Low Voltage NETSEL, GSTSEL	V_{IL1}	0	+0.3	V
Input High Voltage NETSEL, GSTSEL	V_{IH1}	V_{DD} −0.3	—	V
Output Low Voltage (I_{OL} = +0.5 mA) NDATA (Output)	V_{OL}	—	+0.4	V
Output High Voltage (I_{OH} = −0.3 mA) NDATA (Output)	V_{OH}	+2.7	—	V
Output Low Voltage (I_{OL} = +0.1 mA) TG, TST, RR, LED	V_{OL1}	—	+0.1	V
Output High Voltage (I_{OH} = −2.5 mA) TG, TST, RR, LED	V_{OH1}	+0.85	—	V
Output Low Voltage (I_{OL} = +0.25 mA) CO	V_{OL2}	—	−0.85	V
Output High Voltage (I_{OH} = −0.1 mA) CO	V_{OH2}	−0.1	—	V
Output Low Voltage (I_{OL} = +0.2 mA) RTDO	V_{OL3}	—	+0.4	V
Output High Voltage (I_{OH} = −20 μA) RTDO	V_{OH3}	+2.7	—	V

Ring-Trip Differential Gain Setting Amplifier

Input Leakage Current (V_{IN} = V_{SS} to V_{DD}) A1N, A1P, XMTB, CGS, CRA, SVB, XMTA, RCV	I_{AI}	−100	+100	nA
Input Resistance	R_{AI}	10	—	Mohms
Input Offset Voltage	V_{OS}	−10	+10	mV
Power Supply Rejection A1OUT	PSRR	50	—	dB
Common Mode Rejection (V_{IN} = −4.0V to +4.0V) A1(−), A1(+)	CMRR	60	—	dB
Common Mode Range A1(−), A1(+)	V_{CM}	−4.0	+4.0	V
DC Open Loop Gain	AVOL	65	—	dB
Output Voltage Swing (R_L = 10Kohm) A1OUT	V_{OA1}	±3.2	—	V
Load Capacitance A1OUT	C_{OA1}	—	50	pF
Load Resistance A1OUT	R_{OA1}	—	10	Kohms

Ring-Trip Detector

Ring-Trip Sensing DC Voltage (DC Differential Voltage Sensed at OP Amp A1 Output)	V_{RTDC}	−38.5	−33.5	mV

Ground Start Detector

Ground Start Sense Voltage at C_{GS}	V_{GS}	−1.4	−1.3	

Loop Sense Detector

Loop Sense Voltage at DLC Output (V_{DD} = +5V, V_{SS} = −5V, SVB = −3.3V)	V_{LS}	+0.7	+0.8	V
Spike Protection at Loop Sense Circuit	THIT	—	12	mS

DLC

DC Loop Control Transfer Function (Inputs at XMTB, Outputs DLC to High Voltage SLIC)	V_{DLC}			
V_{XMTB} = −1.6V		3.07	3.235	V
V_{XMTB} = −1.0V		2.095	2.26	V
V_{XMTB} = −0.4V		1.115	1.28	V
V_{XMTB} = −0.2V		0.05	0.5	V
V_{XMTB} = −0.1V		−1.15	−0.6	V

Transmission Characteristics

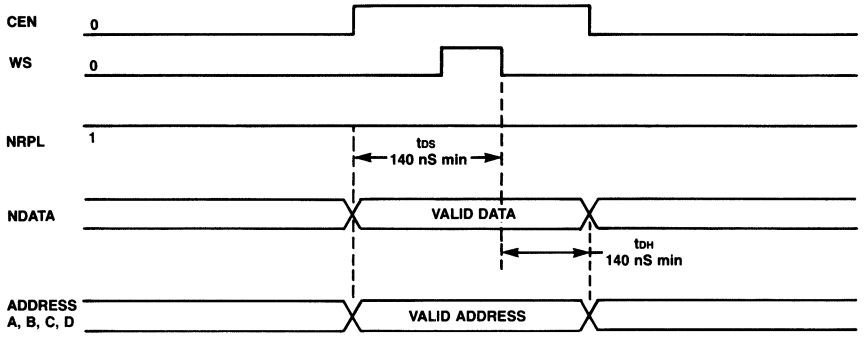
Transmit Gain at 1.02 KHz (Input −0.316 V_{RMS} at XMTA) XMT	G_{XMT}	8.003	8.135	dB
Transmit Freq. Response Relative to Gain at 1KHz (Input −0.316 V_{RMS} at XMTA)	G_{RXMT}	−0.066	+0.066	dB
4-Wire Return Loss: Loaded, Non-Loaded, 900 ohm/2.16 μF (When used with G24002)	R_{L4W}			
200 Hz to 500 Hz		20	—	dB
500 Hz to 2500 Hz		25	—	dB
2500 Hz to 3400 Hz		20	—	dB

Noise

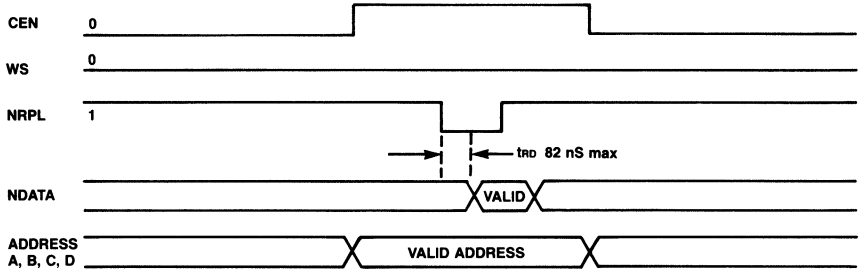
Total C-Message Noise at XMT Output (0 dBm0 = 1.2276 V_{RMS} at XMT)	N_{CXMT}	—	4	DBRNCO
Total C-Message Noise at DLC Output	N_{CDLC}	—	15	DBRNCO

Timing Diagrams (Logic Control Interface)

Write Cycle Timing



Read Cycle Timing



Functional Description

The G24010 Control IC is designed to provide a three-way interface between GTE's G24002 Interface IC, a PCM Codec/Filter, and external microcomputer control. The Control IC is designed to be used in combination with the G24002 Interface IC. This two-chip set, when combined with a PCM Codec/Filter, results in a highly versatile solid-state SLIC-based Line Card which is ideally suited for Central Office Switch or PABX applications. The SLIC-based Line Card provides interfacing between the 2-wire (high-voltage) subscriber loop twisted pair and the 4-wire (low-voltage) central office switch.

The SLIC Control IC provides all necessary control outputs for driving Ringing, Testing and other user-defined relay options. Standard Ring-Trip, Loop Sense and Ground Start Detection circuit functions are provided, in addition to a DC Loopback Control circuit which feeds the Interface IC to guarantee correct Tip and Ring voltages. A Line Card failure LED output is provided, along with a special circuit to prevent false Loop Sense detection.

Also included is a Digital Logic Control Interface for external control of the various G24010 internal functions, including; Cut-Over (CO) functions, Tip Ground (TG), Testing (TST), Ringing (RR), and Ring-Trip Disable (RTDI and RTDO). This parallel I/O bus may be interfaced to a system microcomputer or other logic control device. The following is a description of the various Control IC functions:

Logic Control Interface

The Logic Control Interface provides parallel bus interfacing to an external microcomputer or other control circuit, thus allowing external control of SLIC Control IC functions. SLIC control states are defined by the external control system. This is accomplished by using the 4-bit address (A, B, C and D) and bidirectional Data Line (NDATA), in combination with Chip Enable (CEN) and a Write Strobe (WS). SLIC control state Status is read using the same address and data line, along with Chip Enable (CEN) and Read Data Enable (NRPL). Refer to the previous Read and Write Timing Diagrams.

The control signals CO, TG, TST and RR are used to drive relays which provide Cut-Over, Tip Ground, Testing and Ringing functions. The LED output is used to drive an external system LED circuit, and serves to indicate a failed SLIC Line Card. The RTDI and RTDO signals provide external Ring-Trip Disable Input/Output functions. The Network Select (NETSEL) in conjunction with NDATA controls the selection of Loaded, Non-Loaded or 9:2 networks. This provides maximum 2 to 4-wire return loss in each case.

Table 1 provides an address map for the various Control IC functions, while Table 2 describes network selection (1-of-3) for 2-wire to 4-wire conversion.

Table 1. Functional Addressing Map

STATE	D	C	B	A	SELECTED FUNCTION
0	0	0	0	0	LS/GST (Read Only)
1	0	0	0	1	Not Used
2	0	0	1	0	Not Used
3	0	0	1	1	Not Used
4	0	1	0	0	Not Used
5	0	1	0	1	Not Used
6	0	1	1	0	Not Used
7	0	1	1	1	LED Indication
8	1	0	0	0	RR (Ring Relay)
9	1	0	0	1	RTDO (Ring-Trip Disable)
10	1	0	1	0	Not Used
11	1	0	1	1	CO (Cut-Over Relay)
12	1	1	0	0	TG (Tip Ground Relay)
13	1	1	0	1	NET (Network Selected)
14	1	1	1	0	Not Used
15	1	1	1	1	TST (Line Test Relay)

Notes:
1. At address 0 (state 0) "AND" GSTSEL is a logic 0, the external system reads the Control IC's Loop Sense (LS). When GSTSEL is a logic 1, address 0 reads Ground Start detection. All remaining functions operate in both read and write modes.
2. NDATA is a bidirectional data line, over which data can be read from or written to the SLIC Control IC.

Table 2. Network Selection

NETSEL	NDATA	NETWORK SELECTED
0	0	Loaded
0	1	Non-Loaded
1	0	900:2
1	1	900:2

DC Loop Control (DLC)

Since the subscriber loop resistance may vary from 400 ohms (telephone set resistance) for short lines, to as much as 2000 ohms for long lines, a DC Loop Control circuit is needed to control loop current (power dissipation) for short loop lengths. This circuit performs that function by generating a DLC transfer function using the scaled-down Transmit Output (XMTB) and scaled-down Battery Output (SVB) signals from the G24002 Interface IC. The resulting DLC output is used to drive the Phase Splitter Amplifier within the Interface IC. The transfer function, operating in a feedback loop with the interface IC, controls the loop current and follows a predetermined, smoothly decreasing curve for increasing loop resistance up to 2000 ohms. For long lines which may have a resistance greater than 2000 ohms, the transfer curve slope changes to allow sufficient overhead working voltage for the Tip and Ring Drive Amplifiers (current drivers) within the Interface IC.

Loop Sense Comparator

The Loop Sense Comparator is used to sense the condition of the subscriber loop, that is, loop closure due to an off-hook condition or rotary dial pulses. Since the DLC output is proportional to loop current, as described above, a Loop Sense (LS) output can be generated and compared against a 750 mV reference voltage. The LS output can then be communicated to the external system by way of the Logic Control Interface. Note that the LS output is "hit" protected by using symmetrical integration, consisting of an external RC circuit. "Hit" protection is defined as the blocking of detected pulses from the Loop Sense Comparator that are less than 10 mS in width.

Ground Start Comparator

This circuit detects a Ground Start condition, which in turn, generates the Ground Start (GST) signal. The GST signal is transferred to the external system by way of the Logic Control Interface. In practice, certain line circuits have Ground Start enabled for hotel/motel line service.

Ring-Trip Circuit

The Ring-Trip circuit is used to control ringing, as well as to remove ringing when the subscriber goes off-hook during a ringing period. When a command to ring a subscriber is received from the Logic Control Interface, the Ring-Trip circuit generates a Ring Relay (RR) signal which is current amplified to drive the Ringing Relay. This signal applies AC ringing voltage (in series with the DC battery voltage) to the subscriber loop through an external resistor. The voltage drop across the external resistor is sensed by the Ring-Trip circuit and applied to a two-pole filter circuit which filters out the AC component. When the subscriber is on-hook, the ringing current contains only AC components. When the subscriber goes off-hook, a DC voltage drop is sensed across the external resistor and compared against a -36 mV reference voltage. If the voltage drop is lower than the reference voltage, Ring-Trip is sensed and the Ring-Trip (RT) signal is generated. This signal resets the Ring Relay latch, thus stopping the ring function. The RT output is also sensed by the external system to detect the Ring-Trip.

Switched-Capacitor Filter Function

This function serves to reshape the RCV signal such that it is equal in amplitude but 180 degrees out of phase with the fed back signal received from the G24002 Interface IC. The filter adjusts the RCV signal to account for one of three different loads presented to Tip and Ring and the effects of the G24002 and external components. The resultant output is $-RCV'$. As discussed later, $-RCV'$ will be added to XMTA to form XMT. This serves to substantially reduce echo in the system.

Summing Amplifier

XMTA input signal contains two components: the transmitted signal from the subscriber connected to Tip-Ring at G24002 and a feedback signal (RCV') resulting from the other subscriber (RCV) through the G24002 and back. The output of the switched-capacitor Filter above is $-RCV'$. Thus by adding XMTA to $-RCV'$, the result is XMT signal which contains only the intended transmitted signal.

Simply put, the switched capacitor filter together with the summing amplifier isolate the RCV and XMT signals on the 4-wire side (4-wire return loss).

VREF

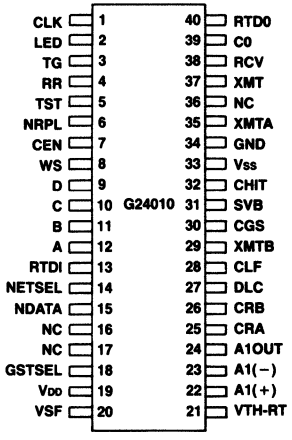
This circuit generates 750 mV and -36 mV reference voltages for use by the Loop Sense Comparator, DC Loop Control and Ring-Trip circuits. A fusible link technique is used to achieve the -36 mV precision reference, while the 750 mV reference is derived directly from the -5 volt source.

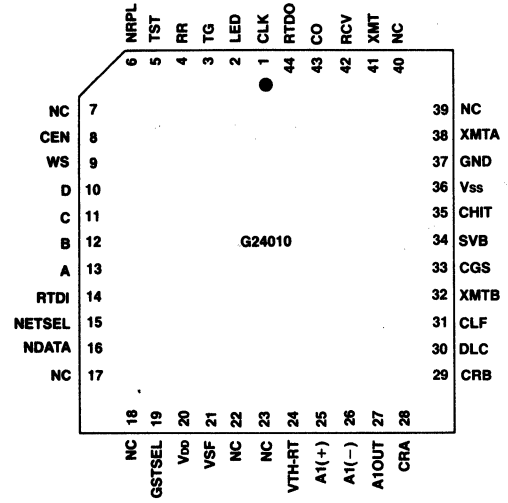
Pin Function Table

Pin	Description
A1(−)	Inverting Input to A1 Ring-Trip Op Amp
A1(+)	Non-Inverting Input to A1 Ring-Trip Op Amp
A1OUT	A1 Ring-Trip Op Amp Output
A, B, C, D	Address Input Lines for Logic Control
CEN	Circuit (Chip) Enable for Logic Control
CGS	Ground Start Comparator Input (−)
CHIT	"Loop Sense Hit" (External Capacitor)
CLF	DLC Loop Filter (External Capacitor)
CLK	1.544 MHz Input
CO	Cutoff Relay Output
CRA	Ring-Trip Circuit (External Capacitor A)
CRB	Ring-Trip Circuit (External Capacitor B)
DLC	DLC Output to G24002
GSTSEL	Ground Start Select
LED	LED Driver Output
NDATA	Bidirectional Data Line for Logic Control (Active Low)
NETSEL	Network Select Input

Pin	Description
NRPL	Read Data Enable (Active Low)
RCV	Receive Input from PCM Codec/Filter
RR	Ring Relay (RR) Output
RTDI	Ring-Trip Disable Input
RTDO	Ring-Trip Disable Output
SVB	Battery Input from G24002, Divided Down
TG	Tip-Ground (TG) Relay Driver Output
TST	Line Test Relay Output
VSF	Vss Noise Filter Pin (External Capacitor)
VTH-RT	Test Output Pin
WS	Write Strobe for Logic Control
XMT	Transmit Output to PCM Codec/Filter
XMTA	"Main" Input from G24002 Interface IC
XMTB	Input Signal from G24002, Divided Down
V_{DD}	Positive Supply Voltage
Vss	Negative Supply Voltage
GND	Ground

Pin Configuration





Applications

Figures 1 and 2 represent a typical application where the G24010 Control IC is used in conjunction with the G24002 Interface IC to form a Subscriber Loop Interface Circuit (SLIC). The addition of a PCM Codec/Filter to this circuit would result in a highly efficient Line Card for use at a Central Office or PABX station.

A description of the various external components is as follows:

Q1 through Q4
Since the G24002 Interface IC is a high voltage, low current device, four external emitter followers are required to drive the Tip and Ring terminals. For a 2000 ohm loop resistance, each transistor dissipates approximately 130 mW; for a loop resistance of 500 ohms, each transistor dissipates approximately 600 mW.

RF1 and RF2
These two resistors are used in conjunction with the Tip and Ring Drive Amplifiers. These resistors, in combination with internal matched resistor pairs, serve to configure the Drive Amplifiers into transconductance amplifiers with a transconductance of 4 mA/V.

RP1, RP2 and DB
RP1 and RP2, along with the Diode Bridge (DB), provide lightning protection.

RCM1 and RCM2
These two resistors serve to combine the Tip and Ring voltages, thus providing a common mode signal to an internal Common Mode Amplifier.

RIN1 and RIN2
These resistors, in combination with internal resistors, form the internal XMT Differential Amplifier.

RG1, RG2 and RSF
These are gain-setting resistors for the RCV signal, as received from the PCM Codec/Filter and XMTA signal.

CZIN
CZIN, along with RG1, provides a feedback path for the signal which appears across Tip and Ring. The purpose of this feedback is to synthesize ZIN "impedance locking" across Tip and Ring (approximately 900:2.16 μF).

CTPF and CVBF
CVBF filters out any power supply noise. CTPF filters out the AC signal components prior to the Tip Party Mark detector circuit within the G24002 Interface IC.

R1 through R4
These four resistors are used to scale down the Ring-Trip sensed signal such that it can be processed by CMOS circuits.

R5, R6 and C1, C2
These four components, in combination with an internal Op Amp, form a two-pole, low-pass filter to extract the DC component from the AC ringing voltage.

CHIT
This external capacitor, in conjunction with an internal resistor, forms a symmetrical integrator circuit. The purpose is to provide "Hit" protection for the output of the Loop Sense Comparator, i.e., blocking pulses that are less than 10 mS in width.

CLF
This external capacitor serves as a loop-filter for the DC loop control circuit.

External Component List

Symbol	Value	Tolerance
R1, R2	5MΩ	±0.25% Ratio Match
R3, R4	81.14KΩ	±0.25% Ratio Match
R5, R6	237KΩ	±1%
RG1	200KΩ	±0.25%
RG2	263.3KΩ	±0.25%
RSF	110KΩ	±0.25%
RP1, RP2	24Ω	±5%
RF1, RF2	49.7Ω	±0.05% Ratio Match ±0.1% Absolute
RCM1, RCM2	150KΩ	±1%
RIN1, RIN2	4.42KΩ	±1%
Q1, Q3	Amperex	BSR41 Or Equivalent
Q2, Q4	Amperex	BSR31 Or Equivalent
DB1	Diode Bridge FD10290-BD	
CVBF, CTPF CHIT, CLF	0.22 μF	±10%
CZIN	0.01 μF	±1%
C1	0.47 μF	±5%
C2	0.22 μF	±5%
CRCV	0.0082 μF	±5%

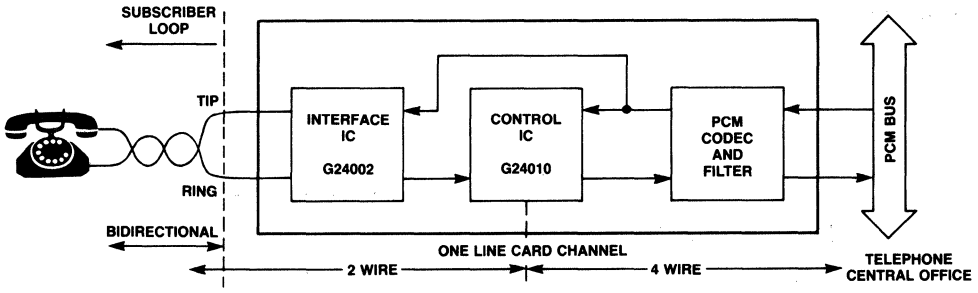


Figure 1. SLIC Line Card

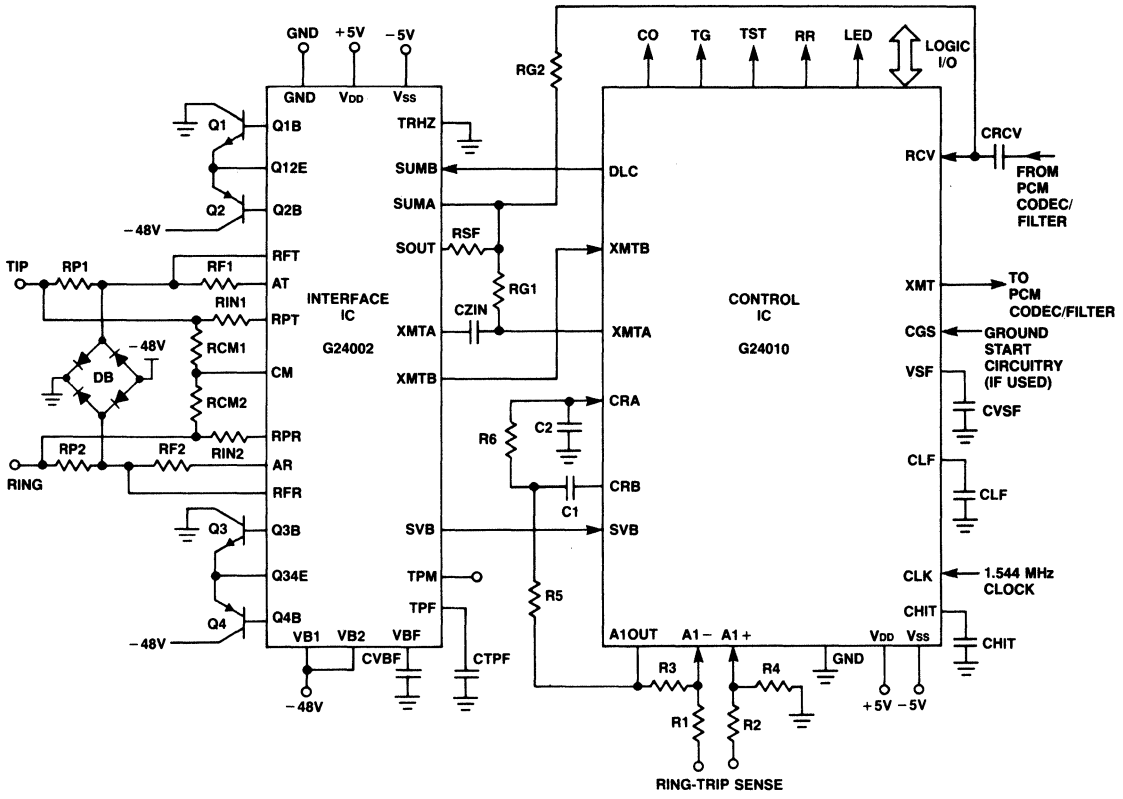
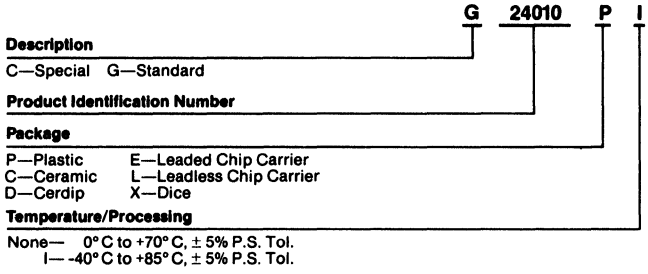


Figure 2. Typical SLIC Application

Ordering Information



G24020

Microcircuits

CMOS Subscriber Line Compensation Network

Features

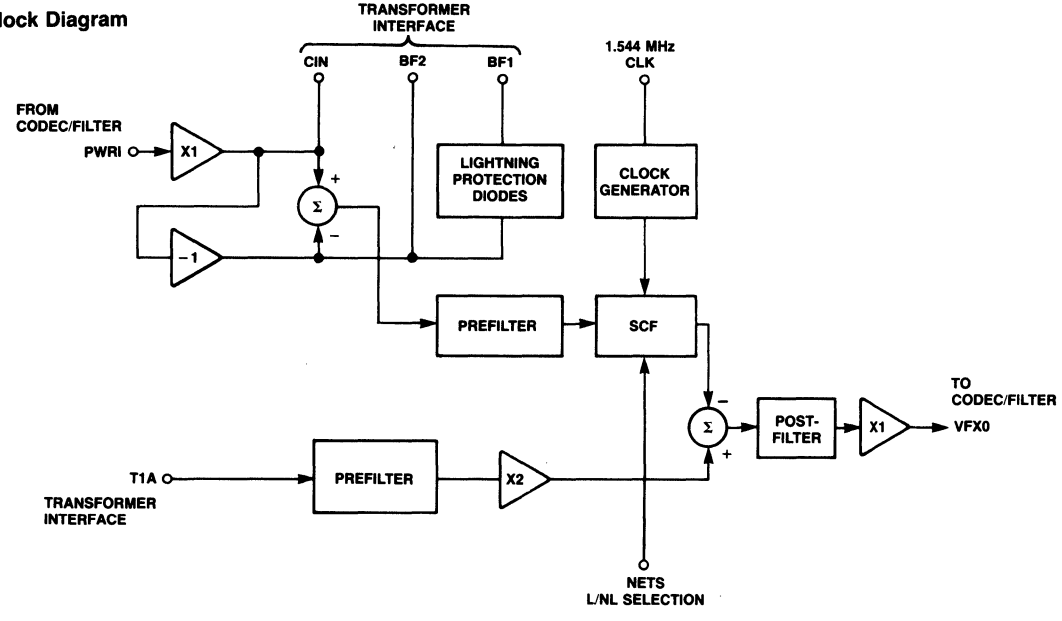
- Two-wire to four-wire converter
- 300 Ω power drivers for transformer and line drive
- 10K Ω transmit output driver
- Lightning protection circuitry
- Anti-alias and post-filters
- Low power consumption:
  - 20 mW typical without power amps
  - 30 mW typical with power amps
- Available in 14-pin DIP package

General Description

GTE Microcircuits' G24020 Subscriber Line Compensation Network is intended for use in telephone circuits. The G24020 serves as an interface between the line transformer and the codec/filter within a line card, and performs the tasks of a balanced hybrid. The primary purpose of the G24020 is to perform two-wire to four-wire conversion and provide lightning protection on the line coupling through the transformer.

To overcome the effects of variations in line impedances for different subscriber loops, the G24020 defines a statistical average loop, identifying two different line conditions, i.e., the loaded and the non-loaded conditions. In addition, isolation between the receive and transmit ports is provided for both the loaded and non-loaded conditions, with transformer bias current varying within the range of 20 mA and 85 mA. Switched capacitor filters are used for balancing the hybrid. The G24020 is manufactured using GTE's CMOS process technology for increased noise immunity, higher reliability and reduced power consumption.

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Microcircuits

G24352
G24353
G24354
G24357

CMOS Monolithic Serial Interface PCM Codec/Filter Family

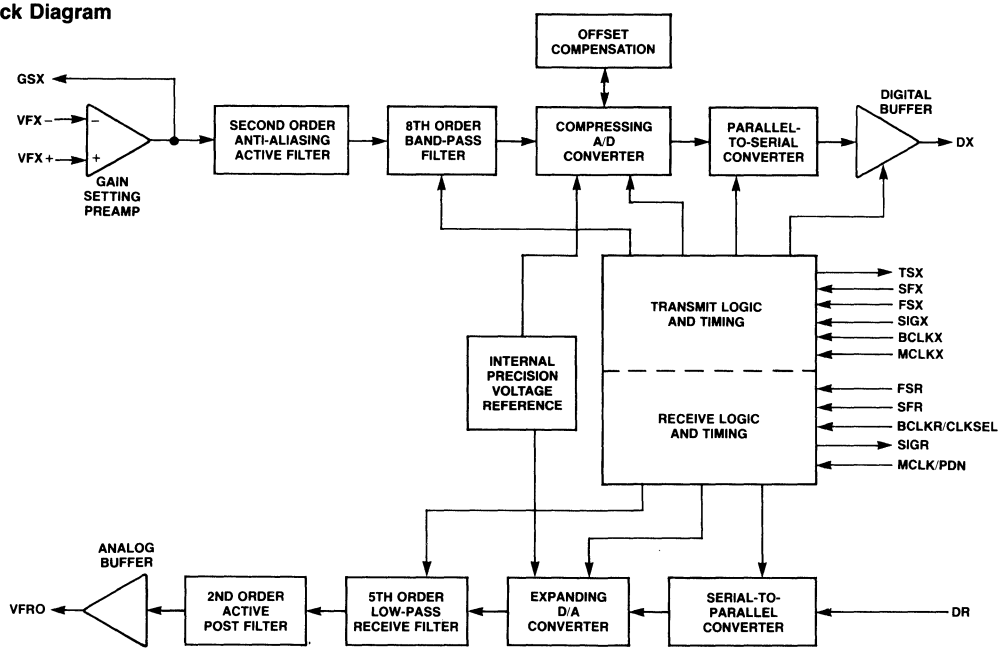
Features

- Four complete Codec/filtering systems:
  - — G24352 — μ-law with signaling (18-pin version)
  - — G24353 — μ-law with signaling (20-pin version)
  - — G24354 — μ-law without signaling (16-pin version)
  - — G24357 — A-law (16-pin version)
- Low power CMOS design: 60 mW operating (typ), 3 mW standby (typ)
- High-pass and low-pass transmit filtering
- Receive Sin x/x correction
- Resistor programmable gain for transmit section
- Synchronous or asynchronous transmit and receive operation
- Serial I/O interface
- Active RC anti-aliasing and post filters
- Precision internal voltage reference and auto-zero circuits
- Automatic power-down by removing frame Sync's and/or single-pin power-down
- Electrostatic discharge and improved latch-up protection on all inputs
- TTL or CMOS compatible logic
- ± 5V power input

General Description

GTE Microcircuits' family of μ-law and A-law Codec/filter circuits feature precision A/D and D/A signal conversion in combination with a serial PCM digital interface. Each device performs voice digitizing and recovery, as well as band limiting and signal restoration as required for companded PCM systems. Within each device, the encode section features an input gain adjust amplifier, active high-frequency RC filter, offset compensation circuitry and a switched-capacitor band-pass filter for rejecting frequencies outside a 200 to 3400 Hz band. Filtered signals are sampled and encoded into the companded μ-law or A-law format. The decode section features an expanding decoder for reconstructing the μ-law or A-law encoded signal, a low-pass filter including Sin x/x response corrections, and a low impedance power amplifier output stage. All devices within the GTE Codec/Filter family meet or exceed AT&T D3/D4 and CCITT specifications, and are manufactured using GTE's state-of-the-art CMOS process technology for increased noise immunity, higher reliability and reduced power consumption.

Block Diagram



ADVANCE INFORMATION

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G24800

Microcircuits

CMOS Mini-Packet Receiver/Transmitter (MPRT)

Features

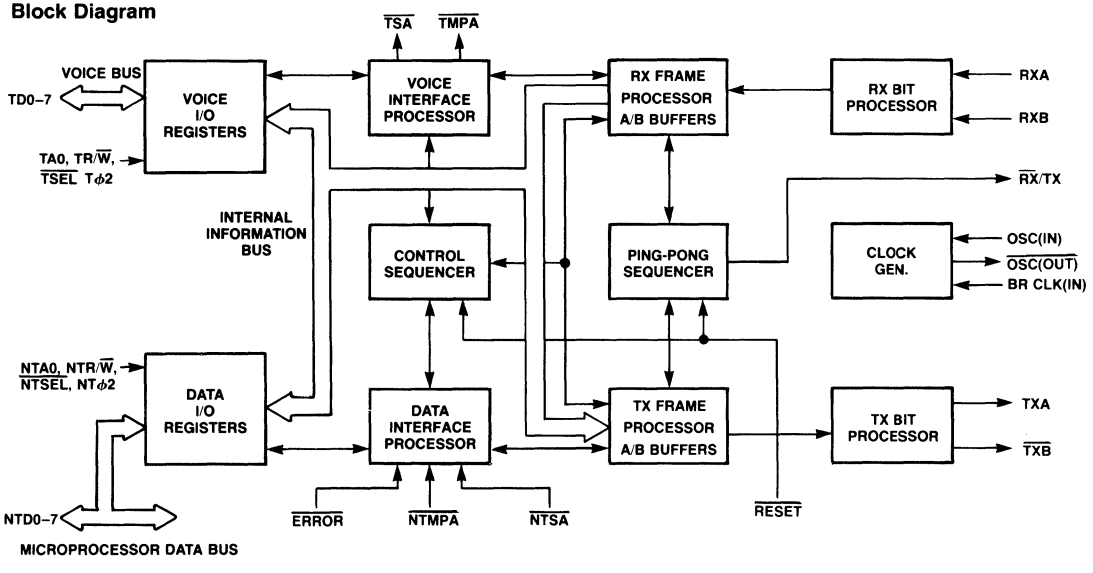
- Advanced CMOS design for low power consumption and increased noise immunity
- Voice/Data Mini-Packet (MP) protocol
- 10 or 12 bytes per Mini-Packet information field
- 4-bit Sync character per Mini-Packet frame
- 8-bit CRC character per Mini-Packet frame
- Bipolar AMI Return-to-Zero (RZ) transmit/receive format
- Digital Voice/Data communication
- Transparent (Voice) and Non-Transparent (Data) 8-bit microprocessor interfaces
- Digital subscriber loop interface (single twisted pair)
- Ping Pong half-duplex or full-duplex mode
- Program selectable baud rates (4, 16, 64, or 256 kb/s)
- Program selectable Master/Slave modes
- Automatic Bipolar Six-Zero Substitution (B6ZS) coding to prevent "line sag"
- Single +5 volt power supply
- Available in 40-pin DIP or 44-pin PLCC package

General Description

GTE Microcircuits' G24800 Mini-Packet Receiver/Transmitter (MPRT) is a single digital voice/data telecommunications chip designed to provide information management and control between one or two 8-bit microprocessors (Transparent Voice and Non-Transparent Data) and a 2-wire subscriber loop interface. The G24800 MPRT offers significant advantages in digital subscriber voice/data telephone operations, as well as remote data acquisition and control systems. Other advantages include GTE's silicon gate CMOS manufacturing process technology . . . providing reliable, low-power operation in a single-chip LSI configuration. The MPRT offers compatibility with existing, as well as future telephone switching hardware and software applications.

The MPRT information transmit and receive format is based on Mini-Packet protocol, with each Mini-Packet consisting of a 4-bit Sync character, 10 or 12 bytes of voice or data information, and an 8-bit CRC character. The Mini-Packet concept not only offers excellent data integrity, but also allows transmission of both voice and data packet information over a single digital subscriber loop. Bidirectional communication over a single twisted pair is achieved by use of a Ping Pong, half-duplex alternation of transmit/receive frames. Full-duplex capability requires two twisted pair lines. Program selectable baud rates, Master/Slave modes, and a versatile voice/data microprocessor interface allows the MPRT to be configured for a wide range of communication systems applications.

Block Diagram



ADVANCE INFORMATION

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Absolute Maximum Ratings (Note 1)

Ratings	Symbol	Value
Supply Voltage	V_{DD}	−0.3V to +7.0V
Input Voltage (All Inputs)	V_{IN}	−0.3V to V_{DD} + 0.3V
DC Current per Pin	I_{IN}	−10 mA to +10 mA
Operating Temperature	T_A	0°C to +70°C
Storage Temperature	T_S	−65°C to +150°C
Junction Temperature	T_J	+150°C

This device contains input protection against damage due to static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Supply Current (V_{DD} = 5.25V, OSC(IN) = 4.096 MHz, Bit 5 of NT Command Reg. High)	I_{DD}	—	10	mA
Input Low Voltage (V_{DD} = 4.75V) All inputs except OSC(IN) OSC(IN)	V_{IL}	 V_{SS} V_{SS}	 0.8 0.15V_{DD}	 V V
Input High Voltage (V_{DD} = 5.25V) All inputs except OSC(IN) OSC(IN)	V_{IH}	 2.0 0.7V_{DD}	 V_{DD} V_{DD}	 V V
Input Leakage Current, Low (V_{DD} = 5.25V, V_{IN} = 0V)	I_{IL}	—	−10	µA
Input Leakage Current, High (V_{DD} = 5.25V, V_{IN} = 5.25V)	I_{IH}	—	10	µA
Output Low Voltage (I_{SINK} = 2.5 mA) NTD0–NTD7, TD0–TD7	V_{OL}	 V_{SS}	 0.4	 V
Output Low Voltage (I_{SINK} = 800 µA) All Outputs Except NTD0–NTD7 & TD0–TD7	V_{OL}	 V_{SS}	 0.4	 V
Output High Voltage (I_{SOURCE} = −2.5 mA) NTD0–NTD7, TD0–TD7	V_{OH}	 2.4	 V_{DD}	 V
Output High Voltage (I_{SOURCE} = −400 µA) All Outputs Except NTD0–NTD7 & TD0–TD7	V_{OH}	 2.4	 V_{DD}	 V

AC Characteristics (General): V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Max	Unit
Clock Input (Oscillator Input)	OSC(IN)	—	4.096	MHz
Clock Input Pulse Width, Low	t_{WCL}	112	—	nS
Clock Input Pulse Width, High	t_{WCH}	112	—	nS
Baud Rate Clock Input Freq.	BR CLK	—	4.096	MHz
Baud Clock Input Pulse Width, Low	t_{WBCL}	112	—	nS
Baud Clock Input Pulse Width, High	t_{WBCH}	112	—	nS
Rise Time, Fall Time (All Clocks)	t_{CR}, t_{CF}	—	22	nS
$\overline{\text{RESET}}$ Input	t_{RST}	1	—	µS
Receive Input A & B Frequency	RXA,B	—	256	KHz
Transmit Output A & B Frequency	TXA,B	—	256	KHz
Receive Input A & B Pulse Width	t_{RXW}	6[1/16xCLK]	20[1/16xCLK]	nS
Receive Input A & B Rise/Fall Time	t_{RXR}, t_{RXF}	—	300	nS
Receive Input A & B Pos. Edge Spacing	t_{PES}	10[1/16xCLK]	25[1/16xCLK]	nS
Transmit Output A & B Pulse Width	t_{TXW}	1/[2(TX CLK)]	1/[2(TX CLK)]	nS

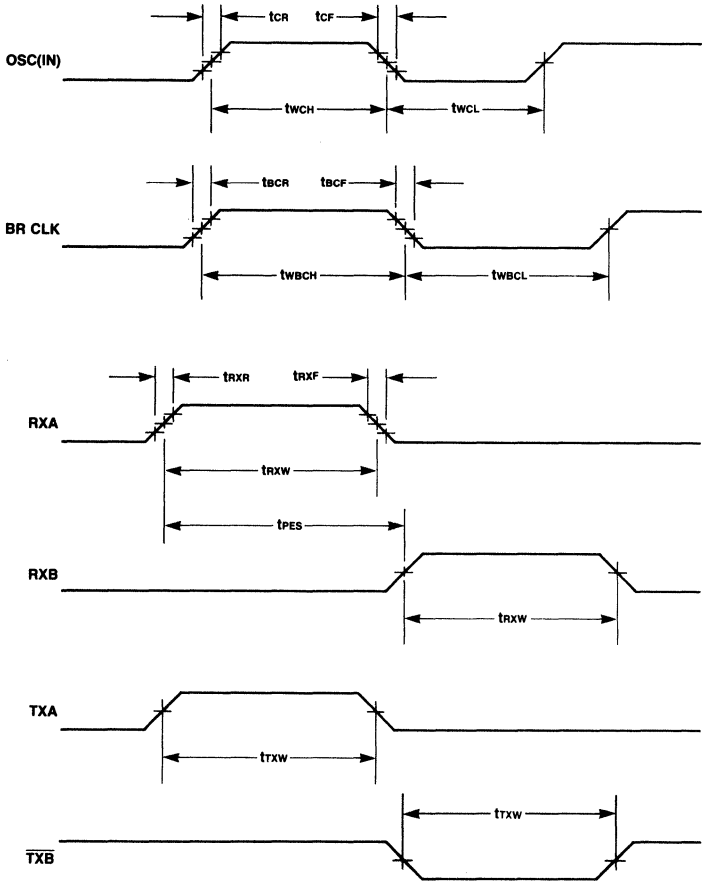
Note: The 16xCLK and Transmit Clock (TX CLK) signals are internally generated from the BR CLK input. The Baud Rate select logic provides one of four clock rates for use by the internal 16xCLK function. 16xCLK is further divided by 16 to generate TX CLK. The maximum 16xCLK frequency is 4.096 MHz and the maximum TX CLK frequency is 256 KHz.

AC Characteristics (Transparent/Non-Transparent Microprocessor Interface): V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C

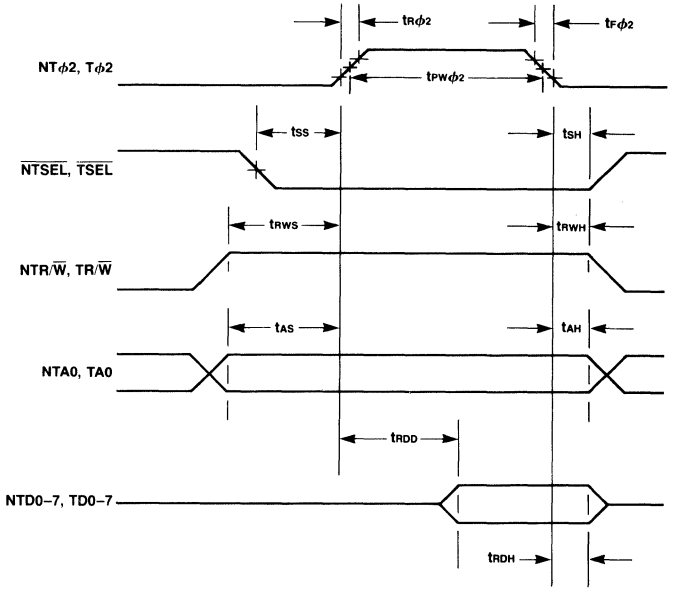
Parameter	Symbol	Min	Max	Unit
Tϕ2 & NTϕ2 Clock Frequency	Tϕ2, NTϕ2	—	2.048	MHz
Tϕ2 & NTϕ2 Pulse Width	$t_{PW\phi2}$	240	—	nS
Tϕ2 & NTϕ2 Rise, Fall Time	$t_{R\phi2}$, $t_{F\phi2}$	—	25	nS
Select Setup Time	t_{SS}	30	—	nS
Select Hold Time	t_{SH}	30	—	nS
R/$\overline{W}$ Setup Time	t_{RWS}	80	—	nS
R/$\overline{W}$ Hold Time	t_{RWH}	0	—	nS
Address Setup Time	t_{AS}	80	—	nS
Address Hold Time	t_{AH}	0	—	nS
Read Data Delay Time	t_{RDD}	—	150	nS
Read Data Hold Time	t_{RDH}	10	—	nS
Write Data Setup Time	t_{WDS}	60	—	nS
Write Data Hold Time	t_{WDH}	20	—	nS

Timing Diagrams

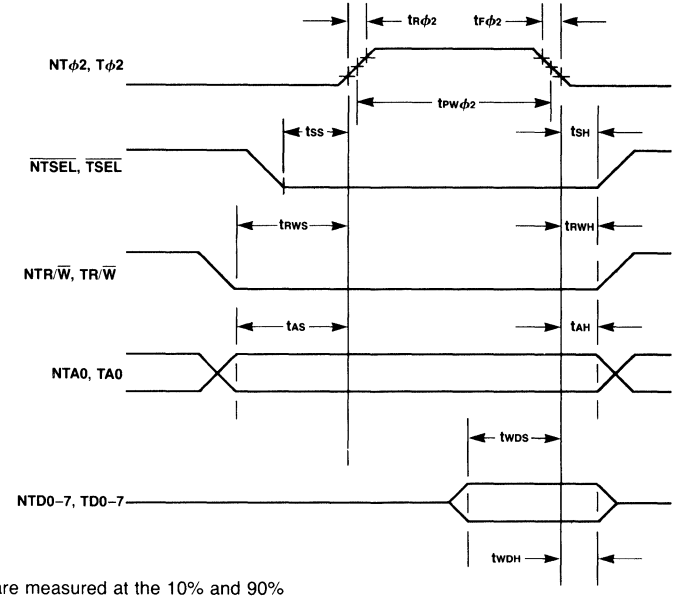
Input/Output Timing



Microprocessor Read from MPRT Timing



Microprocessor Write to MPRT Timing



Timing Notes:

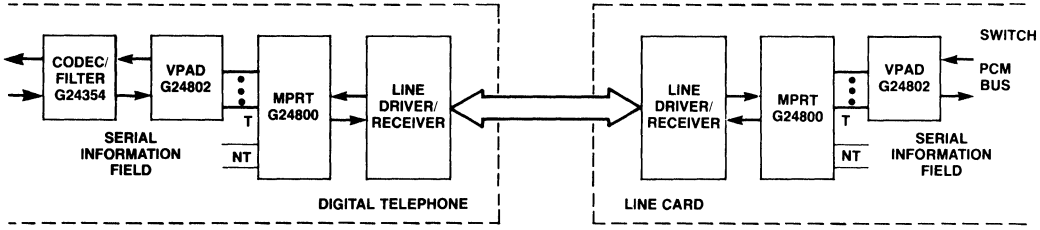
1. All rise and fall times are measured at the 10% and 90% points.
2. All other timing measurements are referenced at their DC Specification values.

Functional Description

The G24800 Mini-Packet Receiver/Transmitter (MPRT) is a single digital voice/data telecommunications chip designed to provide information processing and management between one or two 8-bit microprocessors (Transparent Voice and Non-Transparent data) and a 2-wire subscriber loop driver/receiver interface. Figure 1 shows a typical digital telephone application with GTE's G24802 VPAD interfacing the Transparent MPRT port. Information transmit and receive formatting is based on voice/data Mini-Packet protocol. Each Mini-Packet consists of a 4-bit Sync character, 10 or 12 bytes of voice or data information, and an 8-bit CRC character as shown in Figure 2. The Mini-Packet concept allows transmission by intermixing voice or data packet frames on a single subscriber loop twisted pair. The 4-bit Sync character is used to distinguish between "fill" frames (noninformation) and valid information frames. Sync character coding is shown in Figure 3.

The Most Significant Bit (MSB) of the first byte in the Mini-Packet information field designates Transparent (voice) or Non-Transparent (data) information, while the 8-bit CRC character provides an integrity check on the entire information field. Signals are transmitted over the subscriber loop in a bipolar AMI (Alternating Mark Inversion) Return-to-Zero (RZ) format with program selectable baud rates of 4, 16, 64 or 256 kb/s. Since the three-level bipolar AMI code requires two digital signals to implement, the MPRT provides two serial inputs (RXA and RXB) and two serial outputs (TXA and $\overline{TXB}$). In this case, consecutive "ones" on the loop are represented as alternating positive and negative pulses as defined in Figure 4.

Note that the Sync character and information field are always sent Least Significant Bit (LSB) first and the CRC character is sent Most Significant Bit (MSB) first.



T — TRANSPARENT PORT FOR VOICE APPLICATIONS
NT — NON-TRANSPARENT PORT FOR DATA APPLICATIONS

Figure 1. Digital Telephone Application

SYNC	INFORMATION FIELD	CRC CHARACTER
4 BITS	10 OR 12 BYTES	8 BITS

Figure 2. Mini-Packet Frame Format

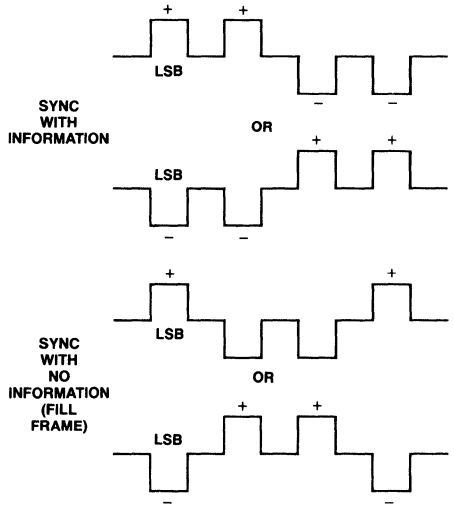


Figure 3. Sync Character Coding

Bidirectional communication over a single twisted pair is controlled by the MPRT using a Ping Pong half-duplex protocol. Ping Pong control provides for alternation of transmit and receive frames. In this way, there is always a continuous alternating flow of transmit and receive frames on the loop. That is, if voice or data information is not available for transmission, the Mini-Packet is transmitted with an "all zero" information field. This type of Mini-Packet is called a "fill" frame. Fill frames are generated by the MPRT using Bipolar Six-Zero Substitution (B6ZS) encoding. B6ZS encoding substitutes a recognizable pattern using no more than "Two Bipolar Rule Violation" for each group of six zeros in the information field. By definition, the occurrence of a Two Bipolar Rule Violation is the failure of a "mark" on the loop to alternate, which results in two adjacent positive marks or two adjacent negative marks. Normal pattern encoding always results in alternating positive and negative marks. A sample of B6ZS encoding, using Two Bipolar Rule Violation, is shown in Figure 5. Fill and valid information frames are identified by the Sync character as discussed above. In the event six contiguous zeros are detected within a valid information frame, as received from the microprocessor or other source, the Transmit Bit Processor will substitute B6ZS coding

RXA	RXB	BIPOLAR LOOP VOLTAGE
0	0	0
1	0	+1
0	1	−1
1	1	UNDEFINED

Figure 4. AMI Return To Zero Coding

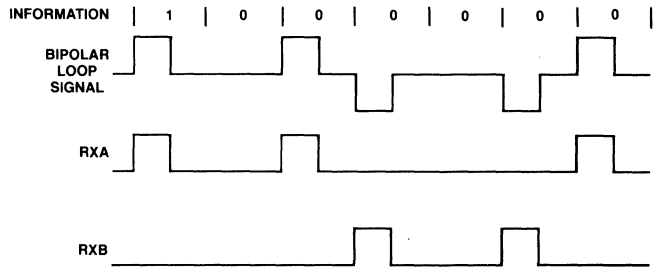


Figure 5. B6ZS Encoding Using Two Bipolar Rule Violation

for each set of six zeros. The Receive Bit Processor will then detect the B6ZS code and substitute the original six zeros for each B6ZS code. Note that the Two Bipolar Rule Violation is also used in encoding the Sync character. This unique Sync character allows the Receive Bit Processor to distinguish Sync coding from the information field. B6ZS coding is a valid method of preventing "line sag" when six contiguous zeros are transmitted.

The primary function of the MPRT is to receive and transmit asynchronous Mini-Packets over a subscriber loop and provide the necessary data buffering and control function for transferring information to and from corresponding microprocessors or other information processing devices such as the GTE VPAD (Voice Packet Assembler/Disassembler).

Microprocessor Interface

The MPRT contains two 8-bit microprocessor-compatible Input/Output (I/O) ports, a Transparent port and a Non-Transparent port. The microprocessor interface controls the transfer of Mini-Packet information fields between the Transmit and Receive Frame Processors and the Transparent or Non-Transparent I/O Registers. There are two Transmit Storage Buffers and two Receive Storage Buffers, with each buffer capable of storing 10 or 12 bytes of information.

The Microprocessor Interface consists of the following functions:

- Control Sequencer
- Transparent I/O Register Group
- Transparent Interface Processor
- Non-Transparent I/O Register Group
- Non-Transparent Interface Processor

Control Sequencer

The Control Sequencer is responsible for the initiation and control of both Transparent Port and Non-Transparent Port read/write functions for each byte of the information field being transferred, the decoding of I/O requests, the generation of Data Register read and write signals, and maintenance of the buffer status. The I/O read and write functions are initiated in accordance with a priority system. The priority system, from highest to lowest is:

Priority

1. Transparent Receive
2. Transparent Transmit
3. Non-Transparent Receive
4. Non-Transparent Transmit

Transparent I/O Register Group

The Transparent I/O Register Group contains an 8-bit bidirectional Voice Register, Voice Bus Transceivers, Control Register, Status Register and address decode and timing logic. Information transfers between the Receive and Transmit Storage Buffers and the microprocessor occur synchronously, one byte at a time, and are controlled by a standard microprocessor read/write interface. Note that the Address "0" bit, in combination with the read/write input, determines which function is to be performed by the Register Group. Refer to Figure 6 for Transparent Microprocessor Read/Write Functions.

Read/Write Functions

TA0	TR/$\overline{W}$	Function
0	0	Write byte into Voice Register
0	1	Read byte from Voice Register
1	0	Write Control Register
1	1	Read Status Register

Transparent Register Formats

B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0

Transparent Voice Register

B7	B6	B5	B4	B3	B2	B1	B0
SAIE	—	—	—	—	—	—	TB

Transparent Control Register

B7	B6	B5	B4	B3	B2	B1	B0
LB	VOICE RF	—	MPA	SA	—	—	TX INTEN

Transparent Status Register

Figure 6. Transparent Microprocessor Read/Write Functions

Transparent Interface Processor

The Transparent Interface Processor monitors and controls all voice packet transfers. The Interface Processor has three modes of operation; Idle, Receive and Transmit. In the Receive mode, and if the MSB of the first information byte is set to a logic "1", a packet is transferred from an RX Storage Buffer to the Transparent Voice Register, one byte at a time. When in the Transmit mode, a packet is transferred from the Transparent Voice Register to a TX Storage Buffer, one byte at a time. Note that when in the Receive or Transmit mode, 10 or 12 bytes must always be transferred to or from the microprocessor before returning to the Idle state. Also note that the Transparent microprocessor is not allowed to receive and transmit simultaneously.

Transparent Control Register Bit Definitions

SAIE (Space Available)	A logic "1" in the SAIE bit position (B7) of the Transparent Control Register will enable Transparent Space Available Interrupts.
TB (Test Bit)	The Test Bit (TB) must always be "zero" during normal MPRT operation.

Transparent Status Register Bit Definitions

LB (Last Byte)	The LB bit is set to a logic "1" after the last byte of a packet is read from or written to the Transparent Voice Register, and is reset by the next sequential Read or Write of the Transparent Voice Register.
VOICE RF (Voice Register Full)	The VOICE RF bit will be a logic "1" after a byte has been written into the Transparent Voice Register. This bit can be used as a Voice Available Flag during Read operations, and as a Ready Flag during Write operations.
MPA (Mini-Packet Available)	The MPA bit will be a logic "1" whenever Space Available (SA) is not asserted and a Receive packet from the subscriber loop is stored in one of the Receive Storage Buffers. The MPA bit is reset upon reading the first byte in the Transparent Voice Registers.
SA (Space Available)	The SA bit is set to a logic "1" whenever there is an empty Transmit Storage Buffer, Space Available Interrupt Enable (SAIE) is set, and MPA is not asserted. The SA bit is reset whenever SAIE is reset, or when the first byte is written to the Transparent Voice Register. The SA bit will always indicate the state of the Transparent Space Available Interrupt output.
TX INTEN (Transmit Interrupt Enable)	The TX INTEN bit will be a logic "1" when SAIE is set, and is reset when SAIE is reset.

The Receive mode is entered into whenever an RX Storage Buffer becomes full of Transparent voice information and there is no outstanding Space Available (SA). At this time, the first information byte is written into the Transparent Voice Register, thus setting the Transparent Voice Register Full flag. The Interface Processor then outputs the $\overline{MPA}$ signal and sets the MPA flag in the Transparent Status Register. The Transparent microprocessor then reads the contents of the Transparent Voice Register. Transfer of information bytes continues until the microprocessor has read the last byte from the Transparent Voice Register. Upon reading the last byte, the Last Byte (LB) flag is set in the Transparent Status Register. In this way, the microprocessor can verify that the packet transfer is complete by checking the Last Byte flag in the Status Register.

The Transmit mode is entered into whenever there is Space Available in one of the TX Storage Buffers, there is no Mini-Packet available (MPA) in a Receive Buffer, and the Transparent Transmit Interrupt Enable (TX INTEN) is set. In the Transmit Pending State, the Transparent Space Available ($\overline{TSA}$) signal is output to the microprocessor. When in the Transmit Pending State, should TX INTEN be reset, the Transparent Interface Processor will return to the Idle state. Also, in the Transmit Pending State, should the Transparent microprocessor write a byte into the Transparent Voice Register, the microprocessor must transfer a complete packet (10 or 12 bytes) to the MPRT. The Last Byte flag in the Transparent Status Register will be set when the last information byte has been read from the Transparent Voice Register.

Non-Transparent I/O Register Group

The Non-Transparent I/O Register Group is identical to the Transparent I/O Register Group except for Status and Control Register functions which are presented on the right.

Read/Write Functions

NTA0	NTR/$\overline{W}$	Function
0	0	Write byte into Data Register
0	1	Read byte from Data Register
1	0	Write Control Register
1	1	Read Status Register

Non-Transparent Register Formats

B7	B6	B5	B4	B3	B2	B1	B0
D7	D6	D5	D4	D3	D2	D1	D0

Non-Transparent Data Register

B7	B6	B5	B4	B3	B2	B1	B0
SAIE	DO	SWRST	RSA	RSB	M/S	H/F	10/12

Non-Transparent Control Register

B7	B6	B5	B4	B3	B2	B1	B0
LB	DATA RF	RXOVE	MPA	SA	BE	TO	TX INTEN

Non-Transparent Status Register

Figure 7. Non-Transparent Microprocessor Read/ Write Functions

Non-Transparent Control Register Bit Definitions

SAIE (Space Available Interrupt Enable)	A logic "1" in the SAIE bit position will enable Space Available Interrupts.
DO (Data Only)	When the DO bit is set to a logic "1", all received packets will be routed to the Transparent Interface.
SWRST (Software Reset)	When SWRST is set to a logic "0", the MPRT is reset to an initialized condition. SWRST is automatically set to a logic "0" whenever RESET is at a logic "0".
RSA (Rate Select A) and RSB (Rate Select B)	RSA and RSB select the appropriate divisor for generating the 16xCLK. The 16xCLK is equal to 16 times the serial loop data rate.
M/S (Master/Slave)	When the M/S bit is a logic "1" (Master mode), the MPRT will always begin transmitting a Mini-Packet. When the M/S bit is a logic "0" (Slave mode), and the MPRT is in the Receive mode, the MPRT will always begin by looking for a Sync character. Note that this bit has no effect during full-duplex operation.
H/F (Half/Full-Duplex)	When the H/F bit is a logic "1" (Full-Duplex), the MPRT Receiver and Transmitter operate independently. When a logic "0" (Half-Duplex), the Transmitter and Receiver alternate frames under Ping Pong control.
10/12 (Ten/Twelve)	When the 10/12 bit is a logic "1" (12 Byte mode), the MPRT transmits and receives packets containing 12 bytes of data. When a logic "0" (10 Byte mode), all packets contain 10 bytes of data.

Non-Transparent Status Register Bit Definitions

LB (Last Byte)	The LB bit is set to a logic "1" after the last byte of a Mini-Packet is read from or written to the Non-Transparent Data Register, and is reset by the next sequential Read or Write of the Non-Transparent Data Register.
DATA RF (Data Register Full)	The DATA RF bit will be a logic "1" after a byte has been written into the Transparent Data Register. This bit can serve as Data Available Flag during Read operations, and as a Ready Flag during Write operations.
RXOVE (Receive Overrun Error)	The Overrun Error bit will be set to a logic "1" whenever the MPRT receives a Mini-Packet and both Receive Storage Buffers are full. Note that this bit is reset upon reading the Non-Transparent Status Register.
MPA (Mini-Packet Available)	The MPA bit will be set to a logic "1" whenever Space Available (SA) has not been asserted and a Receive packet from the subscriber loop is stored in one of the Receive Storage Buffers. The MPA bit is reset upon reading the first data byte in the Non-Transparent Data Register.
SA (Space Available)	The SA bit is set to a logic "1" whenever there is an empty Transmit Storage Buffer, Space Available Interrupt Enable (SAIE) is set, and MPA is not asserted. The SA bit is reset whenever SAIE is reset, or when the first byte is written into the Non-Transparent Data Register. Note that the Status Register SA bit indicates the state of the Non-Transparent Space Available ($\overline{\text{NTSA}}$) output.
BE (Bit Error)	The BE bit is set to a logic "1" whenever a CRC error occurs, or when an illegal input pulse is detected. BE is reset by a Non-Transparent Status Register read.
TO (Timeout)	The TO bit is set to a logic "1" when a Mini-Packet Sync character has not been detected within 40 bit times of the loop data rate. The TO bit is reset by a Non-Transparent Status Register read.
TX INTEN (Transmit Interrupt Enable)	The TX INTEN bit will be a logic "1" when SAIE is set, and is reset when SAIE is reset.

Non-Transparent Interface Processor

The Non-Transparent Interface Processor performs identical functions as described for the Transparent Interface Processor.

Ping Pong Controller

The Ping Pong Controller contains a state machine which controls the alternation of subscriber loop receive and transmit Mini-Packet frames. The controller can operate in either the Master or Slave mode. The state machine is responsible for generating the Receive/Transmit ($\overline{\text{RX}}$/TX) output signal. The $\overline{\text{RX}}$/TX signal will indicate the Receive function when the state machine has initiated a Receive Mini-Packet, and the $\overline{\text{RX}}$/TX signal will indicate the Transmit function when the state machine has initiated a Transmit Mini-Packet. When the MPRT is configured for the Master mode, the Ping Pong Controller will always start by transmitting a Mini-Packet. After the Mini-Packet has been transmitted, the Ping Pong function will alternate to receive a Mini-Packet, reset a Timeout Counter, enter into a "Sync Hunt" state and wait for the Sync character. If a Sync character has not been received within 40 bit times, the Timeout Counter will roll over, set the Timeout (TO) bit in the Non-Transparent Status Register, and the Ping Pong Controller will alternate to the Mini-Packet transmit state. When the MPRT is configured for the Slave mode, the Ping Pong Controller will initiate to receive a Mini-Packet, reset a Timeout Counter, enter into a "Sync Hunt" state and wait for the Sync character. If a Sync character has not been received within 40 bit times, the Timeout Counter will roll over, set the TO bit in the Non-Transparent Status Register and remain in the Sync Hunt state until a Sync character has been received. Each time

the Timeout Counter rolls over, the Sync Error Counter will be incremented. If 128 timeouts occur before a Sync character is finally received, Sync Error is set and $\overline{\text{ERROR}}$ output is signaled. Synchronization can be recovered by having the microprocessor place the MPRT in a known state, i.e., software Reset. Note that Ping Pong timing is asynchronous with the microprocessor interface. In the full-duplex mode, the Ping Pong Controller is not active and both Receive and Transmit Frame Processors operate continuously.

Clock Generator

The MPRT Clock Generator contains the necessary dividing counters for establishing software-selected baud rates. The Baud Rate Clock input (BR CLK(IN)) will normally be 4.096 MHz, which is divided down to provide an internal 16xCLK. The 16xCLK is further divided by 16 to generate the internal TX CLK. The subscriber loop baud rate is selected by RSA and RSB. Figure 8 shows the four possible Baud Rates.

Baud Rate Select		Serial Loop	
RSA	RSB	Data Rate	16xCLK
0	0	256 kb/s	4.096 MHz
0	1	64 kb/s	1.024 MHz
1	0	16 kb/s	256 KHz
1	1	4 kb/s	64 KHz

Figure 8. Baud Rate Selection

Receive Bit Processor

The Receive Bit Processor receives serial Mini-Packet input from the subscriber loop. Its function is to extract the internal Receiver Clock, detect the Sync character, detect wide pulses, decode the Six-Zero Substitution (B6ZS) code, and generate NRZ data from the received RXA and RXB inputs. Since two signal inputs are required to represent B6ZS data, the serial line inputs RXA and RXB must be processed separately until the B6ZS information is decoded and the appropriate six logic zeros are returned to the information field. This Sync character decode determines whether the Mini-Packet contains valid information or "fill" information, since Mini-Packet protocol requires that there be continuous alternation of transmit and receive Mini-Packet frames as determined by the Ping Pong Controller.

Receive Frame Processor

The Receive Frame Processor converts NRZ serial data from the Receive Bit Processor into parallel data bytes, checks the CRC character, and stores the Mini-Packets into the Receive Storage Buffers. Upon receiving a valid Sync detect signal from the Receive Bit Processor, the subsequent serial NRZ data is received and the information field is stored in an available Receive Storage Buffer. Note that if the storage buffers are full and a new Mini-Packet is being received, data for that Mini-Packet is ignored and cannot be recovered. In this event, the Receive Overrun Error (RXOVE) is set in the Non-Transparent Status Register and an ERROR is asserted. When the entire Mini-Packet information field has been written into the RX Storage Buffer and the CRC character has been checked, an internal Buffer Full flag is set. The Receive Frame Processor thus provides Mini-Packet frame timing functions and buffer management to the Transparent or Non-Transparent Interface Processor.

Transmit Bit Processor

The Transmit Bit Processor contains Zero Detect logic and associated circuits for generating the Mini-Packet Return-to-Zero (RZ) transmit format. Following the internal Start Transmit signal from the Ping Pong Controller, the TX Storage Buffer is unloaded in parallel bytes and serially shifted through an internal shift register to outputs TXA and $\overline{\text{TXB}}$. The CRC character is generated by the Transmit Frame Processor from the serially shifted Transmit Buffer information field data. The SYNC character is generated and inserted first into the Mini-Packet, followed by the information field, with the CRC character being inserted following the last byte of the information field. During the data shift, if the Zero Detect logic detects six consecutive zeros, Six-Zero Substitution (B6ZS) is inserted into the data stream.

Transmit Frame Processor

The Transmit Frame Processor consists primarily of two TX Storage Buffers, a CRC character generator and parallel-to-serial data conversion logic. Once a Start Transmit signal is received from the Ping Pong Controller, and provided there is a Mini-Packet available to transmit, a parallel-to-serial register is loaded from one of the TX Storage Buffers. The CRC character is generated as NRZ data and is shifted out to the Transmit Bit Processor. The CRC character is appended following the last serial byte of the information field. Transmit conditions and priorities are as follows:

1. In the Idle state, that is, no Transparent or Non-Transparent data is available for transmission (buffers empty), "fill" data (B6ZS) is generated and transmitted as a noninformation Mini-Packet. Noninformation Mini-Packets will continue to be transmitted in response to each internal Start Transmit signal from the Ping Pong Controller, and will continue until valid Mini-Packet data is received by TX Storage Buffer.
2. Transparent Mini-Packets have priority and will be transmitted first over Non-Transparent packets.

Pin Function Table

Pin	Description
Transparent Processor Interface	
TD0–7	Transparent Voice I/O Bus
Tϕ2	Transparent Microprocessor ϕ2 Clock Input
$\overline{\text{TSEL}}$	Transparent Bus Select Input (Active Low)
TA0	Transparent Address Zero Bit Input
TR/$\overline{\text{W}}$	Transparent Read/Write Input (Write Active Low)
$\overline{\text{TMPA}}$	Transparent Mini-Packet Available Output (Active Low) A Transparent Mini-Packet is available to be read from an MPRT RX Buffer (A or B) when Buffer A or B is full and Space Available (TSA) is not asserted. TMPA is reset on the first byte read from the Transparent Voice Register.
$\overline{\text{TSA}}$	Transparent Space Available Output (Active Low) A TX Buffer (A or B) is available to be written into, i.e., Buffer A or B is empty and Transparent Space Available Interrupt Enable (TSAIE) is set, and TMPA is not asserted. TSA is reset when TSAIE is reset or when the first byte is written into the Transparent Voice Register.

Non-Transparent Processor Interface

NTD0–7	Non-Transparent Data I/O Bus
NTϕ2	Non-Transparent Microprocessor ϕ2 Clock Input
$\overline{\text{NTSEL}}$	Non-Transparent Bus Select Input (Active Low)
NTA0	Non-Transparent Address Zero Bit Input
NTR/$\overline{\text{W}}$	Non-Transparent Read/Write Input (Write Active Low)
$\overline{\text{NTMPA}}$	Non-Transparent Mini-Packet Available Output (Active Low) A Mini-Packet is available to be read from an MPRT RX Buffer (A or B) when Buffer A or B is full and NTSA is not asserted. NTMPA is reset when the first byte is read into from the Non-Transparent Data Register.
$\overline{\text{NTSA}}$	Non-Transparent Space Available Output (Active Low) Both TX Buffers are available to be written into, i.e., Buffers A and B are empty and NTSAIE is set, and NTMPA is not asserted. NTSA is reset when NTSAIE is reset or when the first byte is written into the Non-Transparent Data Register.
$\overline{\text{ERROR}}$	MPRT Error Output (Active Low) An MPRT error condition exists when either a Sync Error, CRC Error or Receive Overrun Error has occurred.

Subscriber Loop Line Driver Interface

RXA, RXB	Receiver Serial Inputs A and B The MPRT receives two digital Return-to-Zero signals from the Line Driver/Receiver interface.
TXA, $\overline{\text{TXB}}$	Transmit Serial Outputs A and B (TXA Active High, TXB Active Low) The MPRT transmits two digital Return-to-Zero signals to the Line Driver/Receiver interface.
$\overline{\text{RX}}$/TX	Receive/Transmit Control Output (TX Active High, RX Active Low)

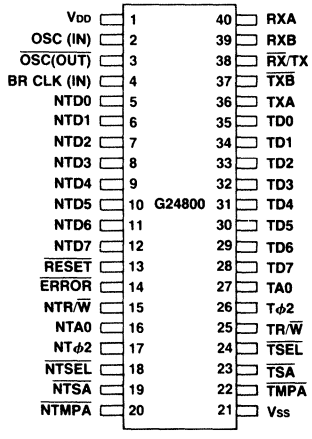
Interface Control Functions

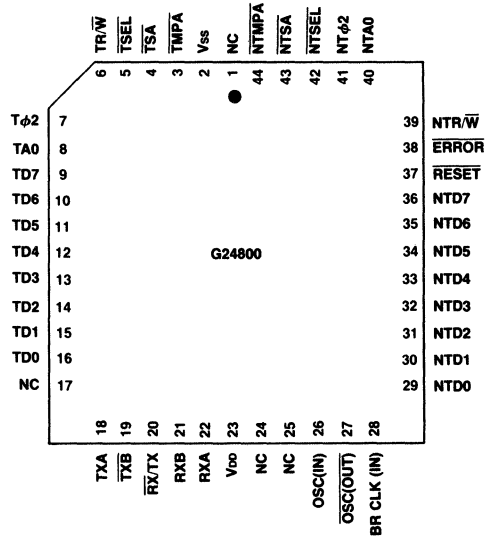
OSC(IN)	Oscillator or Clock Input
$\overline{\text{OSC(OUT)}}$	Oscillator or Clock Output
BR CLK(IN)	Baud Rate Clock Input
$\overline{\text{RESET}}$	Reset Input (Asynchronous MPRT Direct Reset Input) (Active Low)

POWER

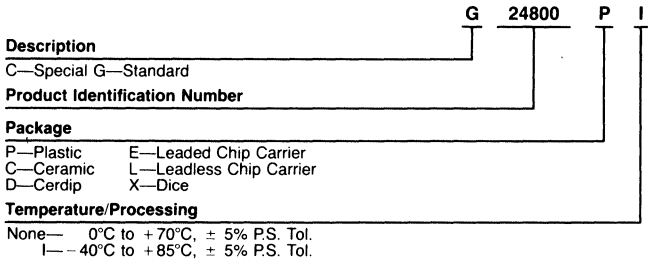
V_{DD}	+5 Volt Supply Voltage
V_{SS}	0 Volt Supply Voltage

Pin Configuration





Ordering Information



G24802

Microcircuits

CMOS Voice Packet Assembler/Disassembler (VPAD)

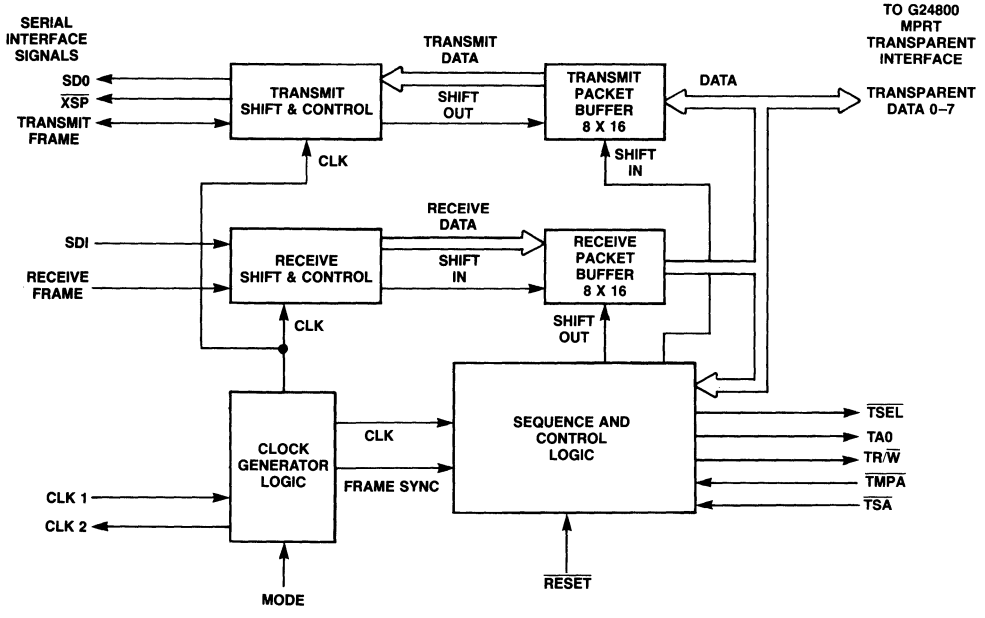
Features

- Advanced CMOS design for low power consumption
- Interfaces with G24800 MPRT Transparent 8-bit parallel microprocessor port
- Transparent serial output to Codec interface (Mode 0) for digital telephone applications
- Transparent serial output to Line Card interface (Mode 1) for other voice transmission applications
- Assembles 10 or 12-byte Mini-Packets from serial input device for transfer to the G24800 MPRT
- Receives 10 or 12-byte Mini-Packets from the G24800 MPRT for serial output devices
- Internal 1.544 MHz crystal controlled oscillator circuit
- Single +5 volt power supply
- Available in 24-pin DIP or 28-pin PLCC package

General Description

GTE Microcircuits' G24802 Voice Packet Assembler/Disassembler (VPAD) provides asynchronous, bidirectional digital data transfers between the GTE G24800 MPRT transparent parallel port and a serial I/O device. The serial I/O device may consist of either a Codec for digital telephone applications (Mode 0), or a Line Card for other digital voice transmission applications (Mode 1). VPAD operation is based on 10 or 12-byte Mini-Packet protocol, providing the Mini-Packet assembly function when transmitting data to the G24800 MPRT, and Mini-Packet disassembly when transmitting data to a serial I/O device. An internal clock generator provides all information clocking, slotting and framing signal functions. The G24802 VPAD is manufactured using state-of-the-art CMOS process technology for increased noise immunity, higher reliability and greatly reduced power consumption.

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

G8870

Microcircuits

CMOS DTMF Integrated Receiver

Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

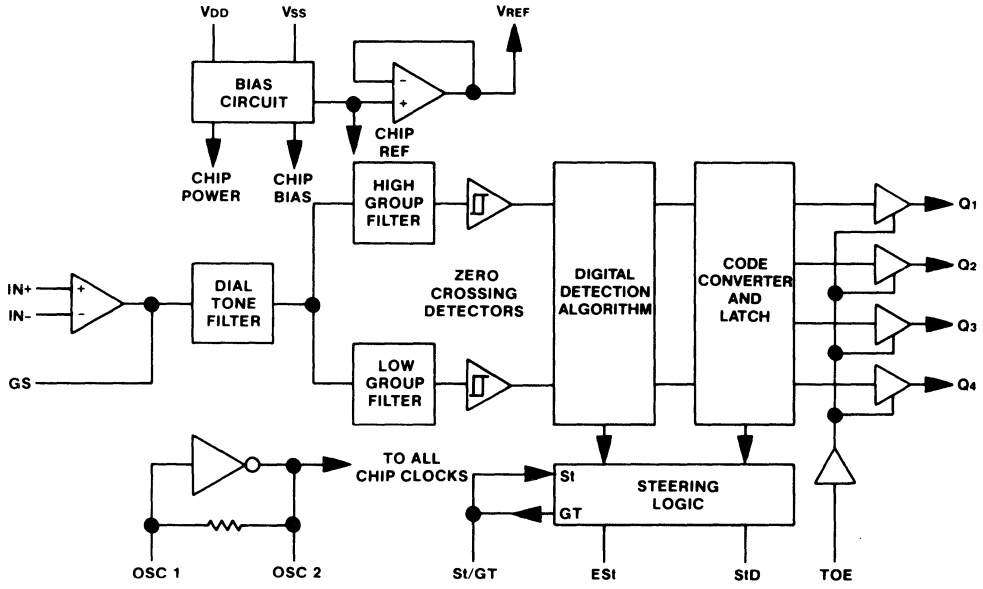
Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

General Description

The GTE G8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	V_{dc}	V_{SS}-0.3, V_{DD}+0.3
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-65° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltage	V_{DD}	4.75		5.25	V	
Operating Supply Current	I_{DD}		3.0	7.0	mA	
Power Consumption	P_o		15	35	mW	f = 3.579 MHz; V_{DD} = 5.0V
Low Level Input Voltage	V_{IL}			1.5	V	
High Level Input Voltage	V_{IH}	3.5			V	
Input Leakage Current	I_{IH}/I_{IL}			0.1	μA	V_{IN} = V_{SS} or V_{DD} (Note 11)
Pull Up (Source) Current on TOE	I_{SO}		6.5	15.0	μA	TOE = 0 V
Input Impedance, Signal Inputs 1,2	R_{IN}	8	10		Meg Ω	@ 1KHz
Steering Threshold Voltage	V_{Tst}	2.2		2.5	V	
Low Level Output Voltage	V_{OL}			0.03	V	No Load
High Level Output Voltage	V_{OH}	4.97			V	No Load
Output Low (Sink) Current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4 V
Output High (Source) Current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
Output Voltage (V_{REF})	V_{REF}	2.4		2.7	V	No Load
Output Resistance (V_{REF})	R_{OR}			10	KΩ	

Operating Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current	I_{IN}			±100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance	R_{IN}	10			MΩ	
Input Offset Voltage	V_{os}			±25	mV	
Power Supply Rejection	PSRR	50			dB	1 KHz (Note 12)
Common Mode Rejection	CMRR	55			dB	-3.0 V < V_{IN} < 3.0V
DC Open Loop Voltage Gain	A_{VOL}	60			dB	
Open Loop Unity Gain Bandwidth	f_c	1.2	1.5		MHz	
Output Voltage Swing	V_o	3.5			Vp-p	$R_L \geq$ 100KΩ to V_{SS}
Tolerable Capacitive Load (GS)	C_L			100	pF	
Tolerable Resistive Load (GS)	R_L			50	KΩ	
Common Mode Range	V_{cm}	2.5			Vp-p	No Load

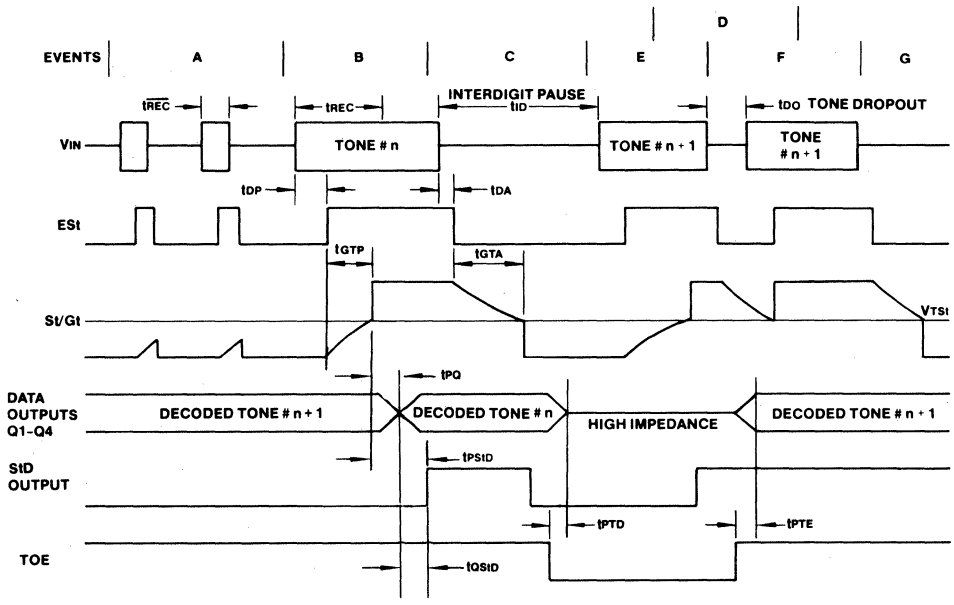
AC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C, f_{CLK} = 3.579545 MHz using test circuit (Fig. 1).

Parameter	Symbol	Min	Typ	Max	Units	Notes
Valid Input Signal Levels (each tone of composite signal)		-29		+1	dBm	1,2,3,4,5,8
		27.5		869	mVRMS	
Positive Twist Accept				10	dB	2,3,4,8
Negative Twist Accept				10	dB	
Freq. Deviation Accept Limit				1.5%±2 Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit		±3.5%			Nom.	2,3,5
Third Tone Tolerance		-25	-16		dB	2,3,4,5,8,9,13,14
Noise Tolerance			-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time	tDP	5	8	14	mS	Refer to Timing Diagram
Tone Absent Detection Time	tDA	0.5	3	8.5	mS	
Min. Tone Duration Accept	tREC			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1
Max. Tone Duration Reject	$t\overline{REC}$	20			mS	
Min. Interdigit Pause Accept	tID			40	mS	
Max. Interdigit Pause Reject	tDO	20			mS	
Propagation Delay (St to Q)	tPQ		6	11	µS	TOE = VDD
Propagation Delay (St to StD)	tPStD		9		µS	
Output Data Set Up (Q to StD)	tQStD	4.0			µS	
Propagation Delay (TOE to Q) Enable.	tPTE		50	60	nS	RL = 10KΩ
Propagation Delay (TOE to Q) Disable	tPTD		300		nS	CL = 50pF
Crystal/Clock Frequency	fCLK	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC2) Capacitive Load	CLO			30	pF	

NOTES:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of al 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.

Timing Diagram



Explanation of Events

A) Tone bursts detected, tone duration invalid, outputs not updated.

B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.

C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

D) Outputs switched to high impedance state.

E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

VIN	DTMF composite input signal.
ESt	Early Steering Output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4	4-bit decoded tone output.
StD	Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
tREC	Minimum DTMF signal duration required for valid recognition.
tID	Minimum time between valid DTMF signals.
tDO	Maximum allowable drop-out during valid DTMF signal.
tDP	Time to detect the presence of valid DTMF signals.
tDA	Time to detect the absence of valid DTMF signals.
tGTP	Guard time, tone present.
tGTA	Guard time, tone absent.

Functional Description

The GTE G8870 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP or 20-pin PLCC package configuration. The G8870's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The G8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTF}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \simeq 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the G8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and V_{REF} biasing the input at $\frac{1}{2}V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Pin Function Table

Name	Description	
IN+	Non-inverting input	Connections to the front-end differential amplifier
IN-	Inverting input	
GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.	
VREF	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.	
IC	Internal connection. Must be tied to VSS.	
IC	Internal connection. Must be tied to VSS.	
OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	Clock output	
VSS	Negative power supply (Normally connected to 0V).	
TOE	Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.	
Q1 Q2 Q3 Q4	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below VTSt.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2.)	
VDD	Positive power supply	

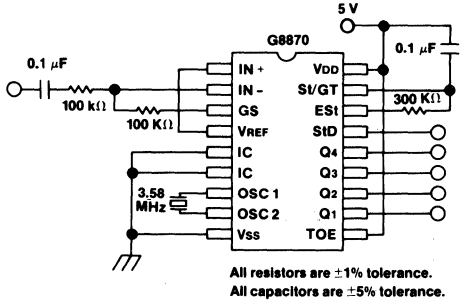
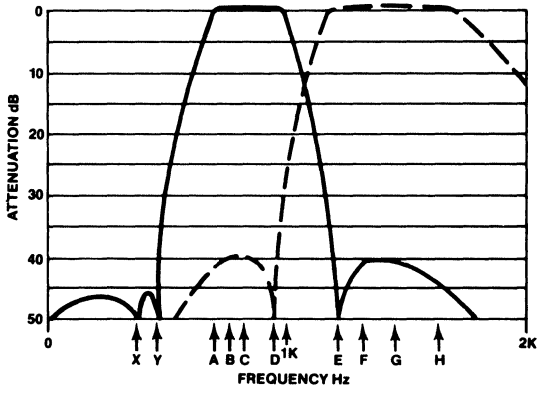


Figure 1. Single Ended Input Configuration

FLOW	FHIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
—	—	ANY	L	Z	Z	Z	Z
L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE							

Figure 2. Functional Decode Table



PRECISE DIAL TONES	DTMF TONES	
X = 350 Hz	A = 697 Hz	E = 1209 Hz
Y = 440 Hz	B = 770 Hz	F = 1336 Hz
	C = 852 Hz	G = 1477 Hz
	D = 941 Hz	H = 1633 Hz

Figure 3. Typical Filter Characteristic

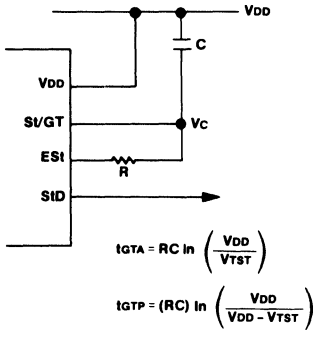


Figure 4. Basic Steering Circuit

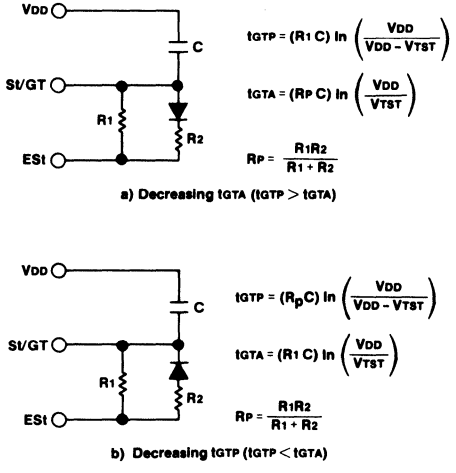


Figure 5. Guard Time Adjustment

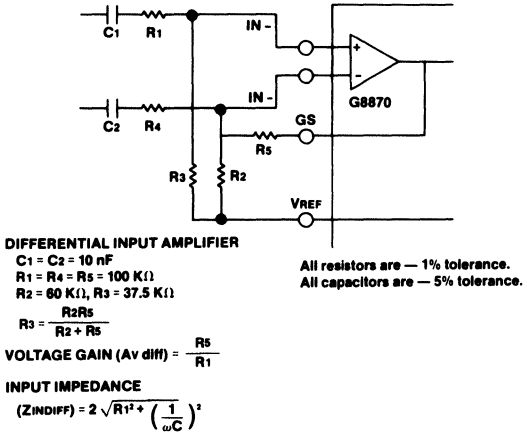


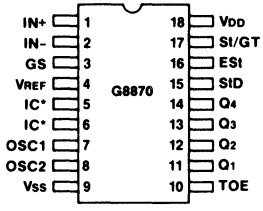
Figure 6. Differential Input Configuration

Pin Function

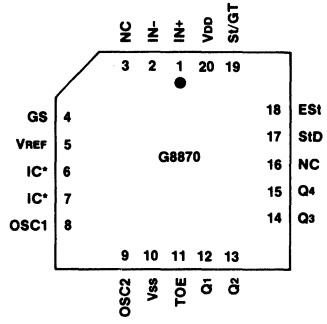
Pin	Description
IN+	Non-Inverting Input
IN-	Inverting Input
GS	Gain Select
IC	Internal Connection
OSC1	Clock Input
OSC2	Clock Output
TOE	Three-State Output Enable

Pin	Description
Q_{1-4}	Three-State Data Outputs
StD	Delayed Steering Output
ESt	Early Steering Output
St/GT	Steering Input/Guard Time Input
V_{REF}	Reference Voltage Output
V_{SS}	Negative Power Supply
V_{DD}	Positive Power Supply

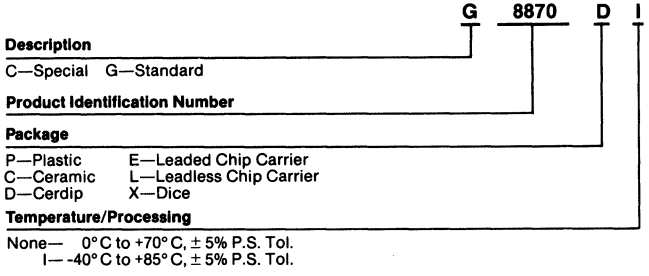
Pin Configuration



*CONNECT TO Vss



Ordering Information



G8870-1

Microcircuits

CMOS DTMF Integrated Receiver

Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

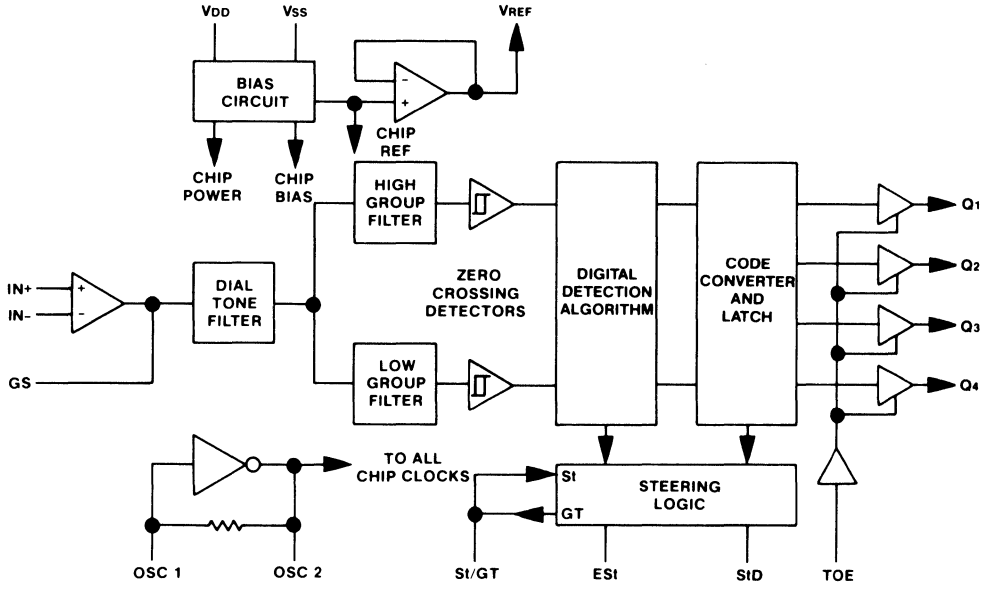
Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry
- Receiver system for Conference of European Postal and Telecommunications (CEPT), and British Telecom

General Description

The GTE G8870-1 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870-1 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870-1 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870-1 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	V_{dc}	V_{SS}-0.3, V_{DD}+0.3
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-65° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Parameter		Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltage		V_{DD}	4.75		5.25	V	
Operating Supply Current		I_{DD}		3.0	7.0	mA	
Power Consumption		P_o		15	35	mW	f = 3.579 MHz; V_{DD} = 5.0V
Low Level Input Voltage		V_{IL}			1.5	V	
High Level Input Voltage		V_{IH}	3.5			V	
Input Leakage Current		I_{IH}/I_{IL}			0.1	μA	V_{IN} = V_{SS} or V_{DD} (Note 11)
Pull Up (Source) Current on TOE		I_{SO}		6.5	15.0	μA	TOE = 0 V
Input Impedance, Signal Inputs 1,2		R_{IN}	8	10		Meg Ω	@ 1KHz
Steering Threshold Voltage		V_{Tst}	2.2		2.5	V	
Low Level Output Voltage		V_{OL}			0.03	V	No Load
High Level Output Voltage		V_{OH}	4.97			V	No Load
Output Low (Sink) Current		I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4 V
Output High (Source) Current		I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
Output Voltage	V_{REF}	V_{REF}	2.4		2.7	V	No Load
Output Resistance		R_{OR}			10	KΩ	

Operating Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current	I_{IN}			±100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance	R_{IN}	10			MΩ	
Input Offset Voltage	V_{os}			±25	mV	
Power Supply Rejection	PSRR	50			dB	1 KHz (Note 12)
Common Mode Rejection	CMRR	55			dB	-3.0 V < V_{IN} < 3.0V
DC Open Loop Voltage Gain	A_{VOL}	60			dB	
Open Loop Unity Gain Bandwidth	f_c	1.2	1.5		MHz	
Output Voltage Swing	V_o	3.5			V_{p-p}	$R_L \geq$ 100KΩ to V_{SS}
Tolerable Capacitive Load (GS)	C_L			100	pF	
Tolerable Resistive Load (GS)	R_L			50	KΩ	
Common Mode Range	V_{cm}	2.5			V_{p-p}	No Load

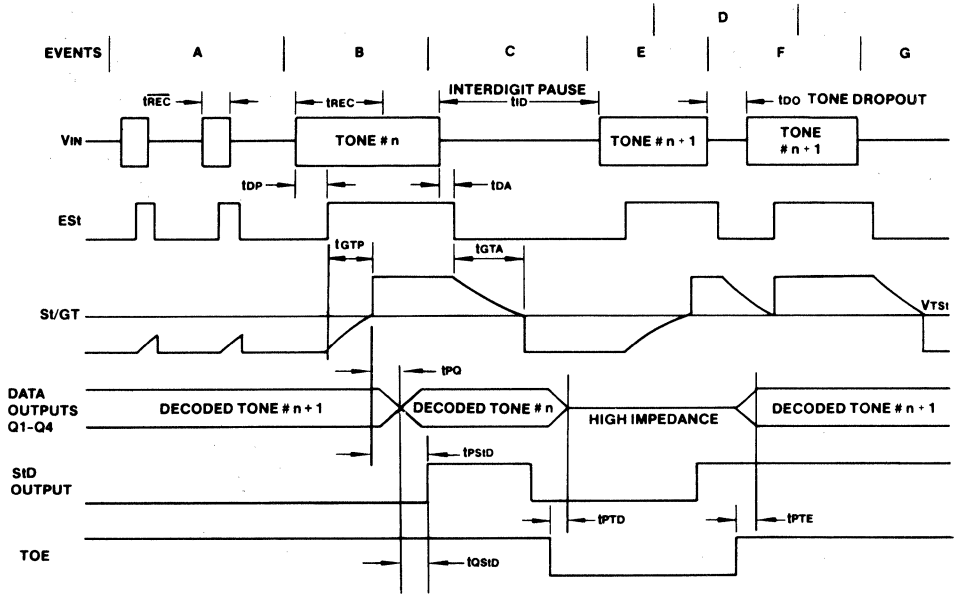
AC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C, f_{CLK} = 3.579545 MHz using test circuit (Fig. 1).

Parameter	Symbol	Min	Typ	Max	Units	Notes
Valid Input Signal Levels (each tone of composite signal)		-31		+1	dBm	1,2,3,4,5,8
		21.8		869	mV_{RMS}	
Input Signal Level Reject		-37			dBm	1,2,3,4,5,8
		10.9			mV_{RMS}	
Positive Twist Accept				10	dB	2,3,4,8
Negative Twist Accept				10	dB	
Freq. Deviation Accept Limit				1.5%±2 Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit		±3.5%			Nom.	2,3,5
Third Tone Tolerance		-18.5	-16		dB	2,3,4,5, 8, 9,13,14
Noise Tolerance			-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time	t_{DP}	5	8	14	mS	Refer to Timing Diagram
Tone Absent Detection Time	t_{DA}	0.5	3	8.5	mS	
Min. Tone Duration Accept	t_{REC}			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1
Max. Tone Duration Reject	$t_{\overline{REC}}$	20			mS	
Min. Interdigit Pause Accept	t_{ID}			40	mS	
Max. Interdigit Pause Reject	t_{DO}	20			mS	
Propagation Delay (St to Q)	t_{PQ}		6	11	µS	TOE = V_{DD}
Propagation Delay (St to StD)	t_{PStD}		9		µS	
Output Data Set Up (Q to StD)	t_{QStD}	4.0			µS	
Propagation Delay (TOE to Q) Enable	t_{PTE}		50	60	nS	R_L = 10KΩ
Propagation Delay (TOE to Q) Disable	t_{PTD}		300		nS	C_L = 50pF
Crystal/Clock Frequency	f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC2) Capacitive Load	C_{LO}			30	pF	

NOTES:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of al 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE .
12. External voltage source used to bias V_{REF}.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.

Timing Diagram



Explanation of Events

A) Tone bursts detected, tone duration invalid, outputs not updated.

B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.

C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

D) Outputs switched to high impedance state.

E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

VIN	DTMF composite input signal.
ESt	Early Steering Output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4	4-bit decoded tone output.
StD	Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
tREC	Minimum DTMF signal duration required for valid recognition.
tID	Minimum time between valid DTMF signals.
tDO	Maximum allowable drop-out during valid DTMF signal.
tDP	Time to detect the presence of valid DTMF signals.
tDA	Time to detect the absence of valid DTMF signals.
tGTP	Guard time, tone present.
tGTA	Guard time, tone absent.

Functional Description

The GTE G8870-1 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP or 20-pin PLCC package configuration. The G8870-1's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The G8870-1 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTF}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \simeq 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the G8870-1 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and V_{REF} biasing the input at $\frac{1}{2}V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Pin Function Table

Name	Description	
IN+	Non-inverting input	Connections to the front-end differential amplifier
IN-	Inverting input	
GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.	
VREF	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.	
IC	Internal connection. Must be tied to VSS.	
IC	Internal connection. Must be tied to VSS.	
OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	Clock output	
VSS	Negative power supply (Normally connected to 0V).	
TOE	Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.	
Q1 Q2 Q3 Q4	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below VTSt.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/GT	Steering input/guard time output (bidirectional). A voltage greater than VTSt detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTSt frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2.)	
VDD	Positive power supply	

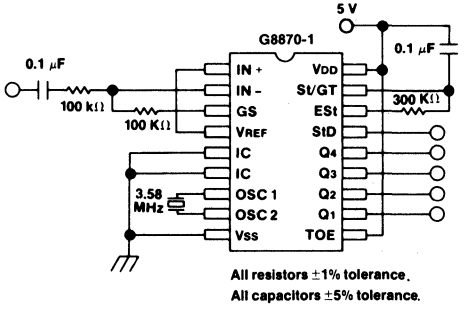
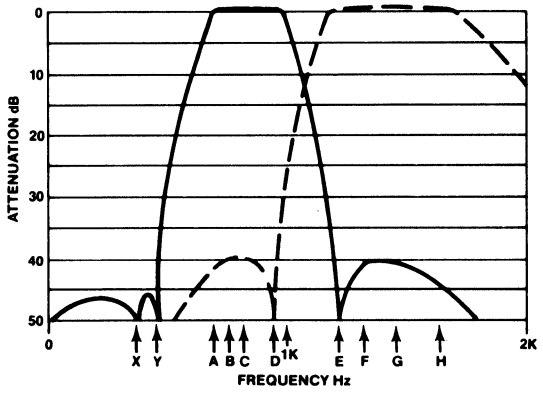


Figure 1. Single Ended Input Configuration Test Circuit

FLOW	FHIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
—	—	ANY	L	Z	Z	Z	Z
L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE							

Figure 2. Functional Decode Table



PRECISE DIAL TONES	DTMF TONES	
X = 350 Hz	A = 697 Hz	E = 1209 Hz
Y = 440 Hz	B = 770 Hz	F = 1336 Hz
	C = 852 Hz	G = 1477 Hz
	D = 941 Hz	H = 1633 Hz

Figure 3. Typical Filter Characteristic

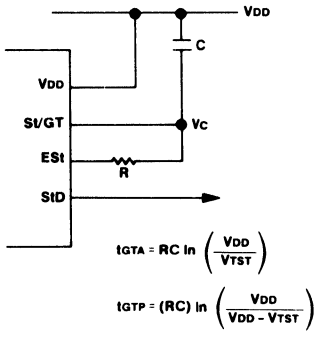
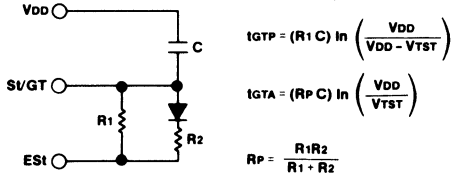
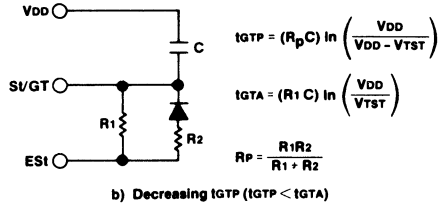


Figure 4. Basic Steering Circuit

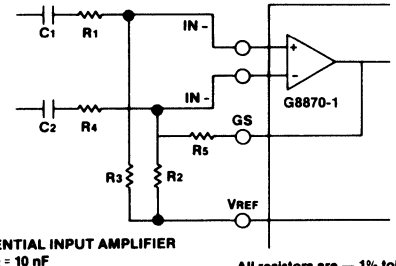


a) Decreasing tGTA (tGTP > tGTA)



b) Decreasing tGTP (tGTP < tGTA)

Figure 5. Guard Time Adjustment



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10$ nF

$R_1 = R_4 = R_5 = 100$ KΩ

$R_2 = 60$ KΩ, $R_3 = 37.5$ KΩ

$R_3 = \frac{R_2R_5}{R_2 + R_5}$

VOLTAGE GAIN (Av diff) = $\frac{R_5}{R_1}$

INPUT IMPEDANCE

$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$

All resistors are — 1% tolerance.
All capacitors are — 5% tolerance.

Figure 6. Differential Input Configuration

Application

Receiver System for British Telecom Spec PÖR 1151

The circuit shown in Fig. 8 illustrates the use of the G8870-1 device in a typical receiver system. The British Telecom specifications define the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing suitable values for R1 and R2 to provide 3 dB attenuation, such that the -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of the G8870-1. As shown in the diagram, the component values of R3 and C2 are the guard time requirement when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 7.

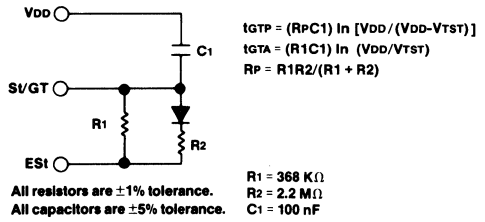


Figure 7. Non-Symmetric Guard Time Circuit

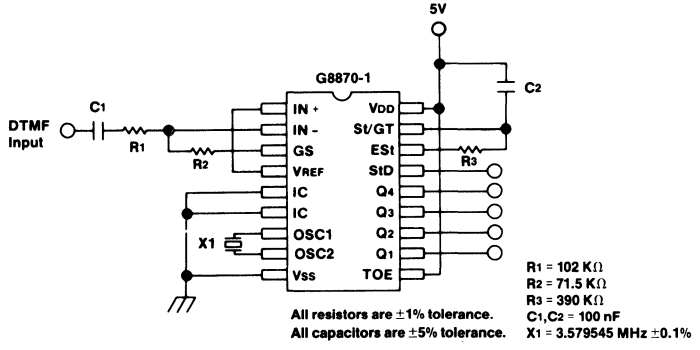


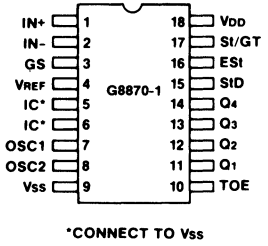
Figure 8. Single Ended Input Configuration for British Telecom or CEPT Specifications

Pin Function

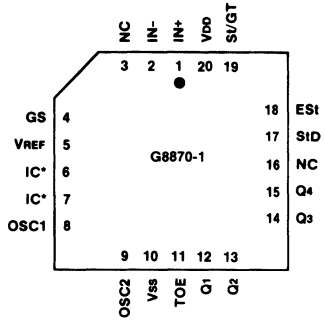
Pin	Description
IN+	Non-Inverting Input
IN-	Inverting Input
GS	Gain Select
IC	Internal Connection
OSC1	Clock Input
OSC2	Clock Output
TOE	Three-State Output Enable

Pin	Description
Q_{1-4}	Three-State Data Outputs
StD	Delayed Steering Output
ESt	Early Steering Output
St/GT	Steering Input/Guard Time Input
V_{REF}	Reference Voltage Output
V_{SS}	Negative Power Supply
V_{DD}	Positive Power Supply

Pin Configuration



*CONNECT TO V_{SS}



Ordering Information

G 8870-1 D I

Description

C—Special G—Standard

Product Identification Number

Package

P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing

None— 0°C to +70°C, ± 5% P.S. Tol.
I— -40°C to +85°C, ± 5% P.S. Tol.

G8880

Microcircuits

CMOS Integrated DTMF Transceiver

Features

- Advanced CMOS technology for low power consumption and increased noise immunity
- Complete DTMF Transmitter/Receiver within a single chip
- Standard 6500/6800 series microprocessor port
- Central office quality and performance
- Adjustable Guard Time
- Automatic Tone Burst mode
- Call Progress mode
- Single +5 volt power supply
- 20-pin DIP or 28-pin PLCC package

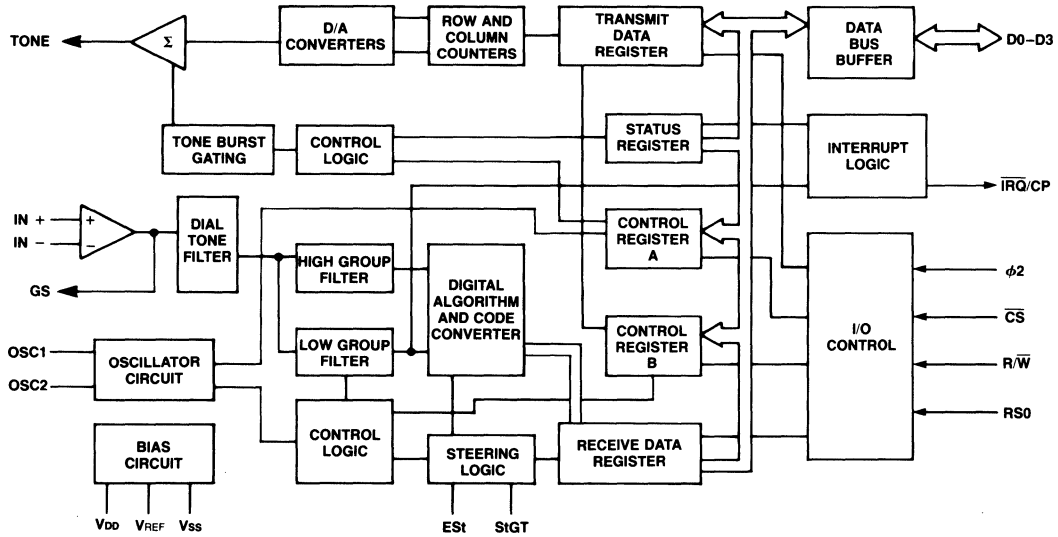
Applications

- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- PABX systems
- Computer systems

General Description

The GTE G8880 is a fully integrated DTMF Transceiver, featuring Adjustable Guard Time, Automatic Tone Burst mode, Call Progress mode and a fully compatible 6500/6800 microprocessor interface. The G8880 is manufactured using state-of-the-art Advanced CMOS technology for low power consumption and precise data handling. The G8880 is based on the industry standard G8870 DTMF Receiver, while the transmitter utilizes a switched-capacitor D/A converter for low distortion, highly accurate DTMF signalling. Internal counters provide an Automatic Tone Burst mode which allows tone bursts to be transmitted with precise timing. A Call Progress filter can be selected by an external microprocessor for analyzing Call Progress tones.

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Absolute Maximum Ratings (Note 1)

Ratings	Symbol	Value
Supply Voltage (V_{DD}–V_{SS})	V_{DD}	+6.0V Max
Voltage on any Pin	Vdc	−0.3V to V_{DD} + 0.3V
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	−40°C to +85°C
Storage Temperature	T_S	−65°C to +150°C

This device contains input protection against damage due to static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Characteristics All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, fc = 3.579545 MHz, $\phi 2$ = 1 MHz, T_A = 25°C

Parameter	Symbol	Min	Typ*	Max	Units
Operating Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Operating Supply Current	I_{DD}	—	10	—	mA
Power Consumption	P_O	—	50	—	mW
Inputs					
High Level Input Voltage OSC1	V_{IHO}	3.5	—	—	V
Low Level Input Voltage OSC1	V_{ILO}	—	—	1.5	V
Input Impedance (@ 1 KHz) IN+, IN−	R_{IN}	—	10	—	MΩ
Steering Threshold Voltage	V_{TSI}	2.2	—	2.5	V
Outputs					
High Level Output Voltage (No Load) OSC2	V_{OHO}	4.9	—	—	V
Low Level Output Voltage (No Load) OSC2	V_{OLO}	—	—	0.1	V
Output Leakage Current (V_{OH} = 2.4V) IRQ	I_{OZ}	—	1.0	10.0	μA
V_{REF} Output Voltage (No Load)	V_{REF}	2.4	—	2.7	V
V_{REF} Output Resistance	R_{OR}	—	10	—	KΩ
Data Bus					
Low Level Input Voltage	V_{IL}	—	—	0.8	V
High Level Input Voltage	V_{IH}	2.0	—	—	V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	—	—	0.4	V
High Level Output Voltage (I_{OH} = 400 μA)	V_{OH}	2.4	—	—	V
Input Leakage Current (V_{IN} = 0.4 to 2.4V)	I_{IZ}	—	—	10.0	μA

Electrical Characteristics — Gain Setting Amplifier: All voltages referenced to V_{SS} unless otherwise noted.
V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25°C

Parameter	Symbol	Min	Typ*	Max	Units
Input Leakage Current ($V_{SS} \leq V_{IN} \leq V_{DD}$)	I_{IN}	—	100	—	nA
Input Resistance	R_{IN}	—	10	—	MΩ
Input Offset Voltage	V_{OS}	—	25	—	mV
Power Supply Rejection (1 KHz)	PSRR	—	60	—	dB
Common Mode Rejection (−3.0V ≤ V_{IN} ≤ 3.0V)	CMRR	—	60	—	dB
DC Open-Loop Voltage Gain	A_{VOL}	—	65	—	dB
Unity Gain Bandwidth	BW	—	1.5	—	MHz
Output Voltage Swing ($R_L \geq$ 100 KΩ to V_{SS})	V_O	—	4.5	—	V_{PP}

Electrical Characteristics — Gain Setting Amplifier (continued)

Parameter	Symbol	Min	Typ*	Max	Units
Maximum Capacitive Load GS	C_L	—	100	—	pF
Maximum Resistive Load GS	R_L	—	50	—	KΩ
Common Mode Range (No Load)	V_{CM}	—	3.0	—	V_{PP}

AC Characteristics: All Voltages referenced to Vss unless otherwise noted. V_{DD} = 5.0V, Vss = 0V, fc = 3.579545 MHz, $\phi 2$ = 1 MHz

Parameter	Symbol	Min	Typ*	Max	Units
Receive Signal Conditions					
Valid Input Signal Levels (Each Tone of Composite Signal; Notes 1, 2, 3, 5, 6, 9)		−29 27.5	— —	+1 883	dBm mV_{RMS}
Positive Twist Accept (Notes 2, 3, 6, 9)		—	10	—	dB
Negative Twist Accept (Notes 2, 3, 6, 9)		—	10	—	dB
Freq. Deviation Accept (Notes 2, 3, 5, 9)		±1.5% ±2 Hz	—	—	Nom.
Freq. Deviation Reject (Notes 2, 3, 5)		±3.5%	—	—	Nom.
Third Tone Tolerance (Notes 2, 3, 4, 5, 9, 10)		—	−16	—	dB
Noise Tolerance (Notes 2, 3, 4, 5, 7, 9, 10)		—	−12	—	dB
Dial Tone Tolerance (Notes 2, 3, 4, 5, 8, 9, 11)		—	+22	—	dB
Call Progress					
Lower Frequency (@ −25 dBm) ACCEPT	f_{LA}	—	320	—	Hz
Upper Frequency (@ −25 dBm) ACCEPT	f_{HA}	—	510	—	Hz
Lower Frequency (@ −25 dBm) REJECT	f_{LR}	—	290	—	Hz
Upper Frequency (@ −25 dBm) REJECT	f_{HR}	—	540	—	Hz
Receive Timing					
Tone Present Detect Time	t_{DP}	5	11	14	mS
Tone Absent Detect Time	t_{DA}	0.5	4	8.5	mS
Tone Duration Accept (Ref. Fig. 9)	t_{REC}	—	—	40	mS
Tone Duration Reject (Ref. Fig. 9)	$t_{\overline{REC}}$	20	—	—	mS
Interdigit Pause Accept (Ref. Fig. 9)	t_{ID}	—	—	40	mS
Interdigit Pause Reject (Ref. Fig. 9)	t_{DO}	20	—	—	mS
Delay St to b3	t_{PStb3}	—	13	—	μS
Delay St to RX_0–RX_3	t_{PStRX}	—	8	—	μS
Transmit Timing					
Tone Burst Duration (DTMF Mode)	t_{BST}	50	—	52	mS
Tone Pause Duration (DTMF Mode)	t_{PS}	50	—	52	mS
Tone Burst Duration (Extended, Call Process Mode)	t_{BSTE}	100	—	104	mS
Tone Pause Duration (Extended, Call Process Mode)	t_{PSE}	100	—	104	mS
Tone Output					
High Group Output Level (R_L = 10 KΩ)	V_{HOUT}	−8	−5	—	dBm
Low Group Output Level (R_L = 10 KΩ)	V_{LOUT}	−10	−5	—	dBm
Pre-emphasis (R_L = 10 KΩ)	dBp	0	2	3	dB
Output Distortion (R_L = 10 KΩ, 3.4 KHz Bandwidth)	THD	—	−25	—	dB
Frequency Deviation (f = 3.5795 MHz)	f_D	—	±0.7	±1.5	%
Output Load Resistance	R_{LT}	10	—	50	KΩ

Microprocessor Interface

ϕ2 Cycle Period	t_{CYC}	—	1	—	μS
ϕ2 High Pulse Width	t_{CH}	450	—	—	nS
ϕ2 Low Pulse Width	t_{CL}	430	—	—	nS
ϕ2 Rise and Fall Time	t_R, t_F	—	—	25	nS
Address, R/$\overline{W}$ Hold Time	t_{AH}, t_{RWH}	10	—	—	nS
Address, R/$\overline{W}$ Setup Time (Prior to ϕ2)	t_{AS}, t_{RWS}	80	—	—	nS
Data Hold Time (Read)	t_{DHR}	20	—	100	nS
ϕ2 to Valid Data Delay (Read)	t_{DDR}	—	—	290	nS
Data Setup Time (Write)	t_{DSW}	165	—	—	nS
Data Hold Time (Write)	t_{DHW}	10	—	—	nS
Input Capacitance D0–D3	C_{IN}	—	5	—	pF
Output Capacitance $\overline{IRQ}$/CP	C_{OUT}	—	5	—	pF

DTMF Clock

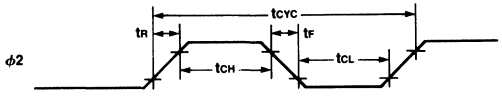
Crystal Clock Freq.	fc	3.5759	3.5795	3.5831	MHz
Clock Input Rise Time (External Clk)	t_{LHCL}	—	—	110	nS
Clock Input Fall Time (External Clk)	t_{HLCL}	—	—	110	nS
Clock Input Duty Cycle (External Clk)	DC_{CL}	40	50	60	%
Capacitive Load OSC2	C_{LO}	—	—	30	pF

*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

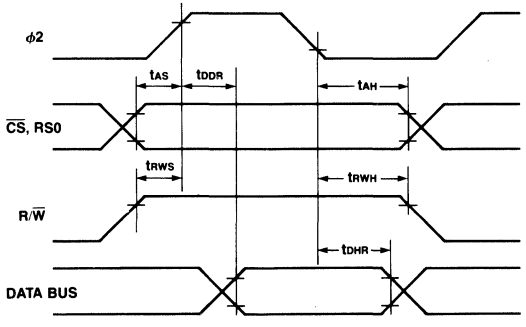
Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 KHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (±2%).
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

Timing Diagrams

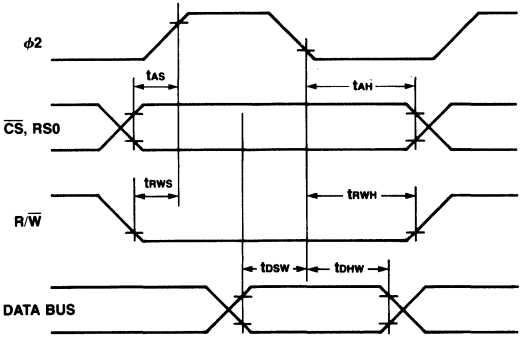
ϕ2 Pulse Timing



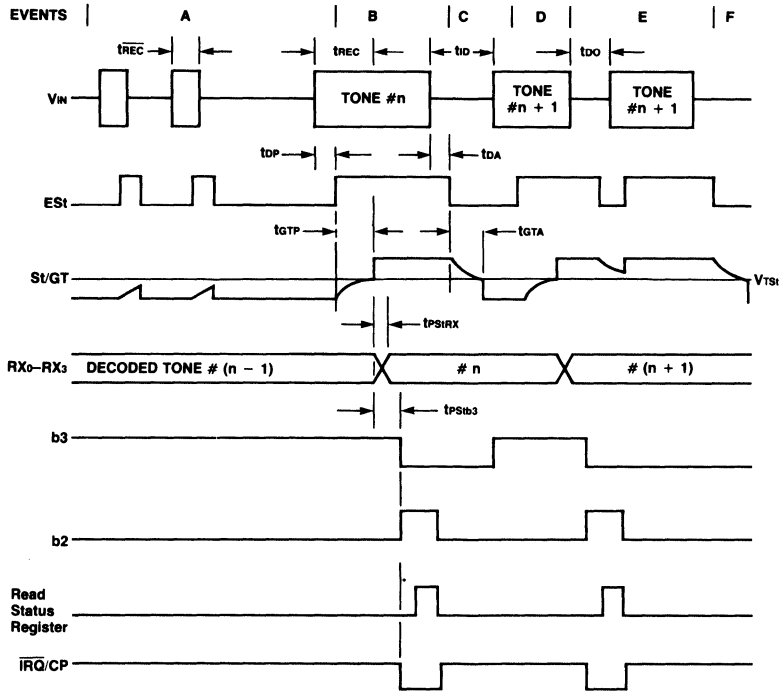
Microprocessor Read Cycle



Microprocessor Write Cycle



General Transceiver Timing

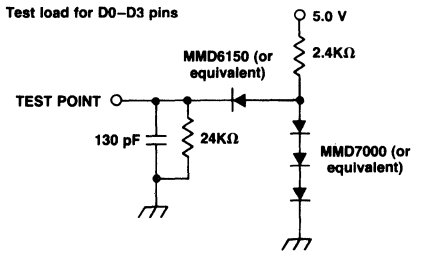


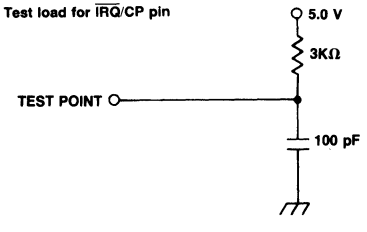
EXPLANATION OF EVENTS

A	Tone bursts detected, tone duration invalid, RX data register not updated.
B	Tone #n detected, tone duration valid, tone decoded and latched in RX data register.
C	End of tone #n detected, tone absent duration valid, information in RX data register retained until next valid tone pair.
D	Tone #n + 1 detected, tone duration valid, tone decoded and latched in RX data register.
E	Acceptable dropout of tone #n + 1, tone absent duration invalid, data remains unchanged.
F	End of tone #n + 1 detected, tone absent duration valid, information in RX data register retained until next valid tone pair.

EXPLANATION OF SYMBOLS

V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
RX_0–RX_3	4-bit decoded data in receive data register.
b3	Delayed steering. Indicates that valid frequencies have been present/absent for the required guard time thus constituting a valid signal. Active low for the duration of a valid DTMF signal.
b2	Indicates that valid data is in the receive data register. The bit is cleared after the status register is read.
$\overline{IRQ}$/CP	Interrupt is active indicating that new data is in the RX data register. The interrupt is cleared after the status register is read.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid sequential DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect valid frequencies present.
t_{DA}	Time to detect valid frequencies absent.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.





Functional Description

The G8880 Integrated DTMF Transceiver provides the design engineer with not only low power consumption, but Central Office quality performance within a single 20-pin DIP package. The G8880's internal architecture consists of a high performance DTMF receiver with an internal Gain Setting Amplifier and DTMF Generator. The DTMF Generator contains a Tone Burst Counter for generating precise tone bursts and pauses. The Call Progress mode, when selected, allows the detection of call progress tones. A standard 6500/6800 series microprocessor interface allows access to an internal Status Register, two Control Registers and two Data Registers within the G8880.

Input Configuration

The G8880 input arrangement consists of a differential input operational amplifier and bias source (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the Op Amp output (GS) for gain adjustment. In the single-ended configuration, the input pins should be connected as shown in Figure 1, while Figure 2 shows the necessary connections for a differential input configuration.

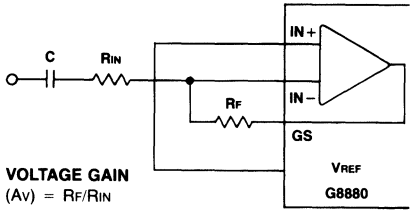
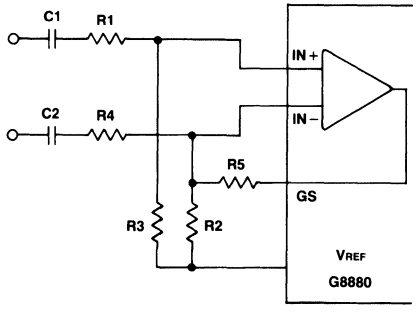


Figure 1. Single-Ended Input Configuration



DIFFERENTIAL INPUT AMPLIFIER
C1 = C2 = 10nF
R1 = R4 = R5 = 100KΩ
R2 = 60KΩ, R3 = 37.5KΩ
R3 = (R2R5)/(R2 + R5)
VOLTAGE GAIN
(Av diff) = R5/R1
INPUT IMPEDANCE
$(Z_{IN}\ diff) = 2\sqrt{R1^2 + (1/\omega C)^2}$

Figure 2. Differential Input Configuration

Receiver Section

Separation of the low and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high-group frequencies as shown in Figure 5. The low-group filter incorporates notches at 350 Hz and 440 Hz for excellent dial-tone rejection. Each filter output is followed by a single-order switched capacitor filter section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparators with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full-rail logic swings at the incoming DTMF signals frequencies.

Following the filter section is a decoder which employs digital counting techniques to determine the frequencies of the incoming tones, and to verify that the incoming tones correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals (e.g. voice), while still providing tolerance to small deviations in frequency. The averaging algorithm was developed to ensure an optimum combination of immunity to talk-off, as well as a tolerance to the presence of interfering frequencies (3rd tones) and noise. When the detector recognizes the presence of two valid tones (sometimes referred to as "signal condition" in industry publications), the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as Character Recognition Condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (See Figure 3) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (See Figure 5) into the Receive Data Register. At this point the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the Delayed Steering output flag goes high, signalling that a received tone pair has been registered. It is possible to monitor the status of the Delayed Steering flag by checking the appropriate bit in the Status Register. If Interrupt Mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the Delayed Steering flag is active.

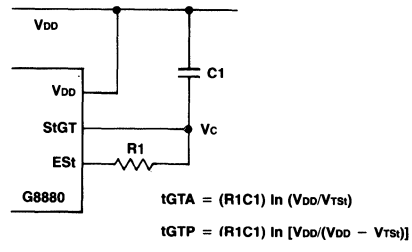


Figure 3. Basic Steering Circuit

The contents of the output latch are updated on an active Delayed Steering transition. This data is presented to the 4-bit bi-directional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the inter-digit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

The simple steering circuit shown in Figure 3 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard Time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for Guard Time adjustment is shown in Figure 4.

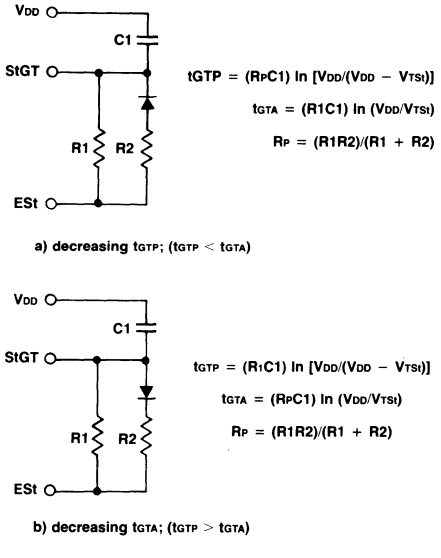


Figure 4. Guard Time Adjustment

FLOW	FHIGH	DIGIT	D4	D3	D2	D1
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = LOGIC LOW, 1 = LOGIC HIGH

Figure 5. Functional Encode/Decode Table

Call Progress Filter

A Call Progress (CP) Mode can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The Call Progress tone input and DTMF input are common, however, call progress tones can only be detected when the CP Mode has been selected. DTMF signals cannot be detected if the CP Mode has been selected (see Table 5). Figure 6 indicates the useful detect bandwidth of the Call Progress filter. Frequencies presented to the input (IN+ and IN−) which are within the 'accept' bandwidth limits of the filter are hard-limited by a high-gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the Call Progress tone being detected. Frequencies which are in the 'reject' area will not be detected, and consequently there will be no activity on $\overline{IRQ}$/CP as a result of these frequencies.

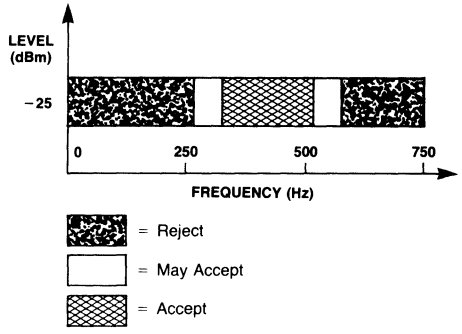


Figure 6. Call Progress Response

DTMF Generator

The DTMF transmitter employed in the G8880 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Figure 5 must be written to the Transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. As seen from Table 1, the Low-Group frequencies are 697, 770, 852 and 941 Hz; the High-Group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically the High-Group to Low-Group amplitude ratio (twist) is 2dB to compensate for High-Group attenuation on long loops.

DTMF Generator Operation

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register, 4-bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32; however, by varying the segment length as described above, the frequency can also be varied. The divider output clocks another counter which addresses the sinewave lookup ROM. The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously, thus providing a high degree of tone burst accuracy. Under conditions when there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typ). A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 4 KHz. It can be seen from Figure 7 that the distortion products are very low in amplitude.

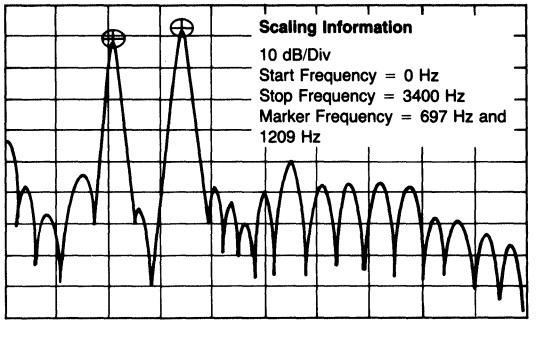


Figure 7. Spectrum Plot

Table 1. Actual Frequencies Versus Standard Requirements

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		
	SPECIFIED	ACTUAL	% ERROR
L1	697	699.1	+0.30
L2	770	766.2	−0.49
L3	852	847.4	−0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	−0.32
H3	1447	1471.9	−0.35
H4	1633	1645.0	+0.73

Burst Mode

In certain telephony applications it is required that DTMF signals being generated be of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 mS ± 1 mS which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register, indicating that the transmitter is ready for more data.

$$THD(\%) = 100\,\frac{\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + \ldots V^2_{nf}}}{V_{fundamental}}$$

Equation 1. THD(%) For a Single Tone

$$THD(\%) = 100\,\frac{\sqrt{V^2_{2L} + V^2_{3L} + \ldots V^2_{nL} + V^2_{2H} + V^2_{3H} + \ldots V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD(%) For a Dual Tone

The timing described above is available when the DTMF Mode has been selected. However, when CP Mode (Call Progress Mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 mS ± 2 mS. The extended interval is useful when precise tone bursts of longer than 51 mS duration and 51 mS pause are desired. Note that when CP Mode and Burst Mode have been selected, DTMF tones may be transmitted only and *not* received. In certain applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the Burst Mode is disabled by enabling and disabling the transmitter.

The G8880 is initialized on power-up sequence such that DTMF Mode and Burst Mode are selected.

Single Tone Generation

A Single Tone Mode is available whereby individual tones from the low-group or high-group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The G8880 is capable of producing precise tone bursts with minimal error in frequency (See Table 1). The internal summing amplifier is followed by a first-order low-pass switched-capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single* tone can be calculated using Equation 1 which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual* tone can be calculated using Equation 2. V_L and V_H correspond to the low-group amplitude and high-group amplitude, respectively, and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 7.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal having a resonant frequency of 3.579545 MHz. A number of G8880 devices can be connected as shown in Figure 8 such that only one crystal is required.

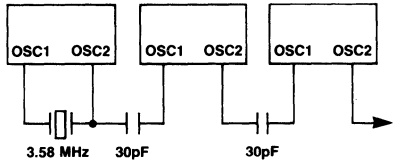


Figure 8. Common Crystal Connection

Table 2. Internal Register Functions

RS0	R/$\overline{W}$	Function
0	0	Write to Transmitter
0	1	Read from Receiver
1	0	Write to Control Register
1	1	Read from Status Register

Table 3. CRA Bit Positions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 4. CRB Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST

Microprocessor Interface

The G8880 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control and transceiver status.

There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read-only register. The data entered in the Transmit Data Register

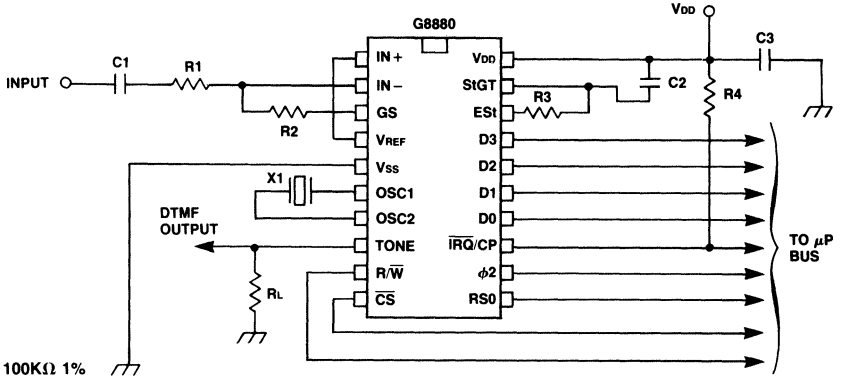
Table 5. Control Register A Description

Bit	Name	Function	Description
b0	TOUT	Tone Output	A logic '1' enables the Tone Output. This function can be implemented in either the Burst Mode or Non-Burst Mode.
b1	CP/$\overline{DTMF}$	Mode Control	In DTMF Mode (logic '0'), the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1'), a 6th-order bandpass filter is enabled to allow Call Progress tones to be detected. Call Progress tones which are within the specified bandwidth will be presented at the $\overline{IRQ}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and Burst Mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 mS (typ) duration. This signal duration is twice that obtained from the DTMF transmitter, if DTMF Mode had been selected. Note that DTMF signals cannot be decoded when the CP mode of operation has been selected.
b2	IRQ	Interrupt Enable	A logic '1' enables the Interrupt Mode. When this mode is active and the DTMF Mode has been selected (b1 = 0), the $\overline{IRQ}$/CP pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (Burst Mode only).
b3	RSEL	Register Select	A logic '1' selects Control Register B on the next write cycle to the Control Register address. Subsequent write cycles to the Control Register are directed back to Control Register A.

will determine which tone pair is to be generated (See Figure 5 for coding details). Data can only be written to the Transmit Data Register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. Internal reset circuitry will clear the control registers on power-up; however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Table 5 and Table 6 for details concerning the Control Registers. The $\overline{IRQ}$/CP pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals, or when the transmitter is ready for more data (Burst mode only). The $\overline{IRQ}$/CP pin is configured as an open-drain output device and as such requires a pull-up resistor (See Figure 9).

Table 6. Control Register B Description

Bit	Name	Function	Description
b0	BURST	Burst Mode	A logic '0' enables the Burst Mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Data Register, resulting in a tone burst of a specific duration (See AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Data Register is ready for further instructions, and an interrupt will be generated if the Interrupt Mode has been enabled. Additionally, if Call Progress (CP) Mode has been enabled, the burst and pause duration is increased by a factor of two. When the Burst Mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	Test Mode	By enabling the Test Mode (logic '1') the $\overline{IRQ}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to General Transceiver Timing (b3 waveform) for details concerning the output waveform. DTMF Mode must be selected (CRA b1 = 0) before Test Mode can be implemented.
b2	S/$\overline{D}$	Single/Dual Tone Generation	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single-tone generation is enabled (logic '1'), either row or column tones (low-group or high-group) can be generated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	Column/Row Tones	When used in conjunction with b2 (above) the transmitter can be made to generate single-row or single-column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.



Notes:
R1, R2 = 100KΩ 1%
R3 = 374KΩ 1%
R4 = 3KΩ 10%
RL = 10KΩ (min)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X1 = 3.579545 MHz

*Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the G8880 can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 9. Application Circuit (Single Ended Input)

Table 7. Status Register Description

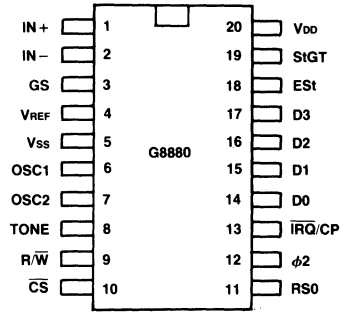
Bit	Name	Status Flag Set	Status Flag Cleared
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	Transmit Data Register Empty (Burst Mode Only)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in Non-Burst Mode.
b2	Receive Data Register Full	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{Delayed Steering}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

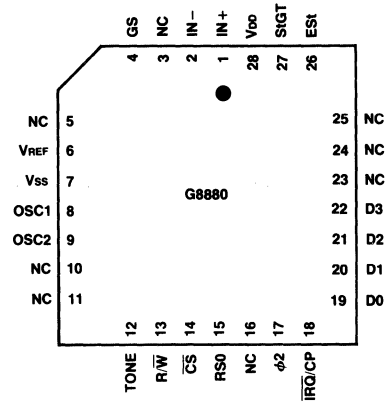
Pin Function Table

Name	Description
IN+	Non-inverting op-amp input.
IN−	Inverting op-amp input.
GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output. Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see application circuit).
V_{SS}	Negative power supply input.
OSC1	DTMF clock/oscillator input.
OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
TONE	Dual Tone Multi-Frequency (DTMF) output.
R/$\overline{W}$	Read/Write input. Controls the direction of data transfer to and from the microprocessor and the Receiver/ Transmitter. TTL compatible.
$\overline{CS}$	Chip Select. TTL input ($\overline{CS}$ = 0 to select the chip).
RS0	Register select input. See register decode table. TTL compatible.

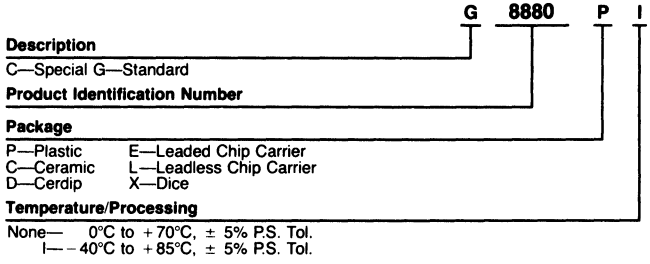
Name	Description
$\phi 2$	System clock input. TTL compatible.
$\overline{IRQ}$/CP	Interrupt request to microprocessor (open-drain output). Also, when Call Progress (CP) Mode has been selected and Interrupt enabled the $\overline{IRQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the Call Progress filter. See Figure 6.
D0–D3	Microprocessor data bus. TTL compatible.
ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
StGT	Steering input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	Positive power supply input.

Pin Configuration





Ordering Information



G8912B

Microcircuits

CMOS PCM Transmit/Receive Filters

Features

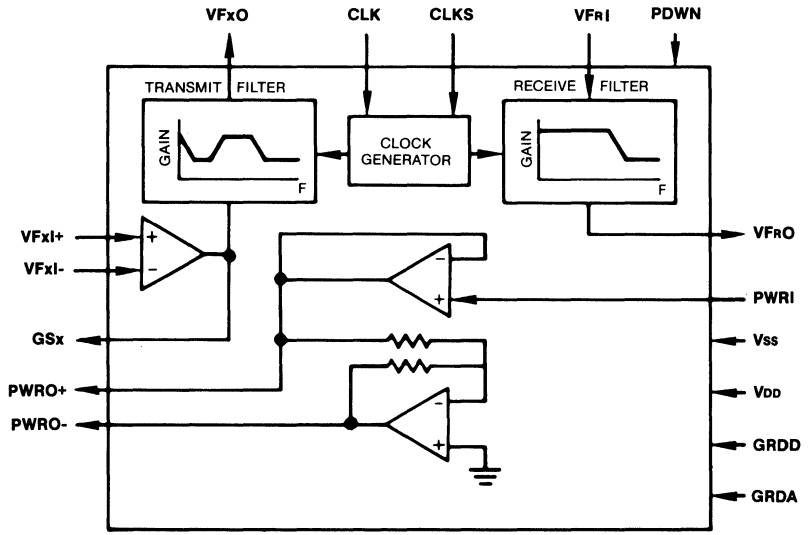
- Monolithic device includes both transmit and receive filters
- Compatible with Bell D3/D4 and CCITT G.712
- Transmit filter rejects 50/60Hz
- Receive filter includes Sin x/x correction
- External gain adjustment of both transmit and receive filters
- Direct interface with transformer or electronic 2-to-4 wire converters
- Low power consumption:
  20mW typical without power amps
  30mW typical with power amps
  0.4mW typical standby
- Anti-aliasing pre-filters on both transmit and receive filters
- Pin-for-pin compatible with Intel 2912

General Description

The GTE G8912B is a monolithic device containing both receive and transmit filters required for the analog termination of a PCM line or trunk. The transmit filter performs the 50/60 Hz power line frequency rejection and the antialiasing function needed for an 8KHz sampling system. The receive filter has a pre-filter to eliminate aliasable codec noise, a low pass transfer characteristic and provides the Sin x/x correction required after D/A signal conversion by a suitable codec.

The G8912B is fabricated using GTE double-poly CMOS technology. Switched capacitors are used for the filter design. The G8912B interfaces directly with an electronic or transformer 2-to-4 wire converter. When interfacing with an electronic converter, the on-chip power amplifiers may be deactivated, thus reducing power dissipation.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
V_{DD} With Respect to V_{SS}	Vdc	-0.3V to +14V
Input/Output Voltages With Respect to V_{SS}	Vdc	-0.3V to V_{DD}
All Output Currents	I_{DD}/I_{SS}	±50 mA
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-65°C to +150°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC and Operating Characteristics: GRDA = GRDD = 0V unless otherwise noted, V_{DD} = +5V, V_{SS} = -5V, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltages	V_{SS}	-5.25	-5	-4.75	V	Ref. to GRDA
	V_{DD}	4.75	5	5.25	V	
V_{DD} Standby Current	I_{DDO}		40	100	µA	PDWN = V_{DD}
V_{SS} Standby Current	I_{SSO}		10	100	µA	
V_{DD} Operating Current	I_{DD1}		2.0	4.0	mA	PWRI = V_{SS}
V_{SS} Operating Current	I_{SS1}		2.0	4.0	mA	Power Amps Inactive
V_{DD2} Operating Current	I_{DD2}		3.0	6.0	mA	With Power Amps
V_{SS2} Operating Current	I_{SS2}		3.0	6.0	mA	(Outputs Unloaded)
Input Load Current, CLK	I_{LIC}	-10	1	+10	µA	V_{IN} = 0 to V_{DD}
Input Load Current, CLKS	I_{LIS}	-10	1	+10	µA	V_{IN} = V_{SS} to V_{DD}
Input Load Current, PDWN	I_{LIP}	-100	-1	+100	µA	V_{IN} = 0 to V_{DD}
Input Low Voltage, CLK, PDWN	V_{IL}	0		0.8	V	
Input Low Voltage, CLKS	V_{ILS}	V_{SS}		V_{SS} + 0.5	V	
Input High Voltage, CLK, PDWN	V_{IH}	2.2		V_{DD}	V	
Input High Voltage, CLKS	V_{IHS}	V_{DD} -0.5		V_{DD}	V	
Input Intermediate Voltage, CLKS	V_{IIS}	-1.0		1.0	V	

Transmit Filter Gain Setting Amplifier

Input Leakage Current, VFxI +, VFxI-	I_{BXI}	-100		100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance, VFxI +, VFxI-	R_{IXI}	10			MΩ	
Input Offset Voltage, VFxI +, VFxI-	V_{OSXI}	-25		+25	mV	
Power Supply Rejection, GSx	$PSRR_1$	50	70		dB	
Common Mode Rejection, VFxI +, VFxI-	CMRR	55	65		dB	-2.5V ≤ V_{IN} ≤ +2.5V
DC Open Loop Voltage Gain, GSx	A_{VOL}	60	70		dB	
Open Loop Unity Gain Bandwidth, GSx	fc		1.0		MHz	
Output Voltage Swing, GSx	V_{OXI}	±2.5	±3.5		V	$R_L \geq 10$ KΩ
Load Capacitance, GSx	C_{LXI}			50	pF	
Minimum Load Resistance, GSx	R_{LXI}	10			KΩ	
Common-Mode Range, VFxI	V_{CM}	-2.5		+2.5	V	

Transmit Filter

Output Resistance, VFxO	R_{OX}		1	3	Ω	
Output DC Offset, VFxO	V_{OSX}	-150		+150	mV	VFxI + Connected to GRDA, Input Op Amp at unity gain
Power Supply Rejection of V_{DD} at 1KHz VFxO	$PSRR_2$	33	38		dB	
Power Supply Rejection of V_{SS} at 1KHz VFxO	$PSRR_3$	30	35		dB	
Load Capacitance, VFxO	C_{LX}			50	pF	
Minimum Load Resistance	R_{LX}	10			KΩ	
Output Voltage, 1KHz, VFxO	V_{OX}	±3.2	±3.8		V	$R_L \geq 10$ KΩ

DC and Operating Characteristics (Cont'd):

Receive Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current, VFRI	I_{BR}			100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance, VFRI	R_{IR}	10			MΩ	
Output Resistance, VFRO	R_{OR}		5	7	Ω	
Output DC Offset, VFRO	V_{OSR}	-150		+150	mV	VFRI Connected to GRDA
Power Supply Rejection of V_{CC} at 1KHz VFRO	$PSRR_4$	35	40		dB	
Power Supply Rejection of V_{BB} at 1KHz, VFRO	$PSRR_5$	35	40		dB	
Load Capacitance, VFRO	C_{LR}			50	pF	
Minimum Load Resistance, VFRO	R_{LR}	10			KΩ	
Output Voltage Swing, VFRO	V_{OR}	±3.2	±3.8		V	R_L = 10KΩ

Receive Filter Driver Amplifiers

Input Leakage Current, PWRI	I_{BRA}			3	μA	$V_{SS} < V_{IN} < V_{DD}$	
Input Resistance, PWRI	R_{IRA}	10			MΩ		
Output Resistance, PWRO +, PWRO–	R_{ORA}		1	2	Ω	$\lvert I_{OUT} \rvert < 5mA$ $-3.0V < V_{OUT} < 3.0V$	
Output DC Offset, PWRO +, PWRO–	V_{OSRA}	-50		+50	mV	PWRI Connected to GRDA	
Load Capacitance, PWRO +, PWRO–	C_{LRA}			100	pF		
Output Voltage Swing Across RL, PWRO+, PWRO–, Single Ended Connection	V_{ORA1}	±3.2			V	R_L = 10KΩ	R_L Connected to GRDA
		±2.9			V	R_L = 600Ω	
		±2.5			V	R_L = 300Ω	
Differential Output Voltage Swing, PWRO+, PWRO–, Balanced Output Connection	V_{ORA2}	±6.4			V	R_L = 20KΩ	R_L Connected Between PWRO+ and PWRO–
		±5.8			V	R_L = 1200Ω	
		±5.0			V	R_L = 600Ω	

AC Characteristics: GRDA = GRDD = 0V unless otherwise noted, V_{DD} = +5V, V_{SS} = -5V, T_A = 0°C to 70°C
Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLKS = V_{SS}
CLK = 1.544MHz ± 0.1%, CLKS = GRDD
CLK = 2.048MHz ± 0.1%, CLKS = V_{DD}

Transmit Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gain Relative to Gain at 1KHz	G_{RX}					0dBmO Input Signal Gain Setting Op Amp at Unity Gain
Below 50Hz				-10	dB	
50Hz				-20	dB	
60Hz				-26	dB	
200Hz		-1.5		-0.125	dB	0dBmO Signal = 1.1 V_{RMS} Input at VFXI +
300Hz to 3000Hz		-0.125		+0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	
4000Hz				-14	dB	
4600Hz and Above				-32	dB	
Absolute Passband Gain at 1KHz, VFXO	G_{AX}	2.9	3.0	3.1	dB	
Gain Variation with Temperature at 1KHz	G_{AXT}		0.0004		dB/°C	0dBmO Signal Level
Gain Variation with Supplies at 1KHz	G_{AXS}		0.01		dB/V	0dBmO Signal Level, Supplies ± 5%
Cross Talk, Receive to Transmit, Measured at VFXO. $20 \log \left[\frac{VFXO}{VFRO}\right]$	CT_{RT}		-85	-71	dB	VFRI = 2.20 V_{RMS}; Freq. = 200Hz -3.4KHz; VFXI+, VFXI- Connected to GSx; GSx Connected through 10KΩ to GRDA
Total C Message Noise at Output, VFXO	N_{CS1}		6	11	dBrncO	Gain Setting Op Amp at Unity Gain
Total C Message Noise at Output, VFXO	N_{CX2}		7	13	dBrncO	Gain Setting Op Amp at 20dB Gain

AC Characteristics: (Cont'd)

Transmit Filter (cont.)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Differential Envelope Delay, VFxO 1KHz to 2.6KHz	D_{DX}			70	μs	
Absolute Delay at 1KHz, VFxO	D_{AX}			185	μs	
Single Frequency Distortion Products	DP_{X1}		-55	-48	dB	0dBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at VFxO	DP_{X2}		-50	-48	dB	Gain Setting Op Amp at 20dB Gain. The +3dBmO signal at VFxO is 2.26 VRMS
Gaintracking Relative to G_{AX}	G_{AXX}	 -0.1 -0.05 -0.1		 +0.1 +0.05 +0.1	 dB dB dB	Input Signal at 1KHz +3 to +2 dBmO +2 to -40 dBmO -40 to -50 dBmO

Receive Filter

Gain Relative to Gain at 1KHz with Sin x/x Correction	G_{RR}					0dBmO Input Signal
Below 200Hz				0.125	dB	0dBmO Signal ≅ 1.6 VRMSX $\left[\frac{\text{Sin}\frac{\pi F}{8000}}{\frac{\pi F}{8000}}\right]$ Input at V_{FRI}
200Hz		-0.125		0.125	dB	
300Hz to 3000Hz		-0.125		0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	
4000Hz				-14	dB	
4600Hz and Above				-30	dB	
Absolute Passband Gain at 1KHz, V_{FRO}	G_{AR}	-0.1	0	+0.1	dB	
Gain Variation with Temperature at 1KHz	G_{ART}		0.0004		dB/°C	0dBmO Signal Level
Gain Variation with Supplies at 1KHz	G_{ARS}		0.01		dB/V	0dBmO Signal Level, Supplies ± 5%
Cross Talk, Transmit to Receive, Measured at V_{FRO}	CT_{TR}		-80	-71	dB	VFxO = 2.26 VRMS, Freq. = 300Hz -3.4KHz, V_{FRI} Connected to GRDA
Total C Messages Noise at Output, V_{FRO}	N_{CR}		5	8	dBrncO	V_{FRO} Output or PWRO+ and PWRO- Connected with Unity Gain
Differential Envelope Delay, V_{FRO} 1KHz to 2.6KHz	D_{DR}			85	μs	
Absolute Delay at 1KHz V_{FRO}	D_{AR}			110	μs	
Single Frequency Distortion Products	DP_{R1}		-55	-48	dB	0dBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at V_{FRO}	DP_{R2}		-50	-48	dB	+3dBmO Signal Level of 2.26 VRMS, 1KHz Output at V_{FRO}
Gaintracking Relative to G_{AR}	G_{ARR}	 -0.1 -0.05 -0.1		 +0.1 +0.05 +0.1	 dB dB dB	Input Signal at 1KHz +3 to +2 dBmO +2 to -40 dBmO -40 to -55 dBmO

Functional Description

Transmit Filter Input Stage

The input stage provides gain adjustment in the passband. The input operational amplifier has a common mode range of ±3.2 volts, a DC offset of less than 25mV, a voltage gain of typically 2000 and a unity gain bandwidth of 1.0 MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output must be greater than 10KΩ. The input signal on lead VFxI + can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of + 3dB in the pass band.

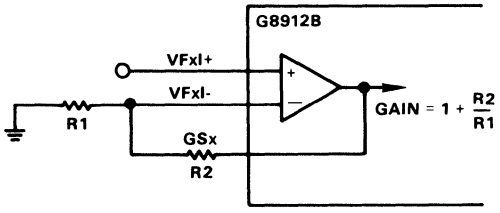


Fig. 1 Transmit Filter Gain Adjustment

50 Hz/60Hz Notch—Transmit Filter

The transmit filter has a notch section to reject 50Hz and 60Hz components of the input signal. A minimum attenuation of 26dB is provided at 60Hz. At 50Hz, the minimum attenuation is 20dB. The gain at 200Hz is between -0.125dB and -1.5dB. (All gain figures are relative to the gain at 1KHz.)

An active RC low pass anti-aliasing filter is included on chip immediately in front of the 50Hz/60Hz notch section. This filter provides greater than 35dB attenuation at 64KHz. As a result no external anti-aliasing components are required to provide the necessary anti-aliasing function for the switched capacitor sections of the transmit filter which operate at an internal sampling rate of 128KHz.

Transmit Filter Transfer Characteristics

The transmit section of filter provides a passband flatness and stopband attenuation which exceeds the Bell D3 and D4 specifications and the CCITT G.712 recommendations. The transmit filter transfer characteristics and specifications are shown in Fig. 2.

Transmit Filter Output Stage

The voltage range of the output signal on the VFxO lead is ±3.2 volts. The DC offset is less than 150mV. The output stage includes an active RC post-filter to attenuate clock noise.

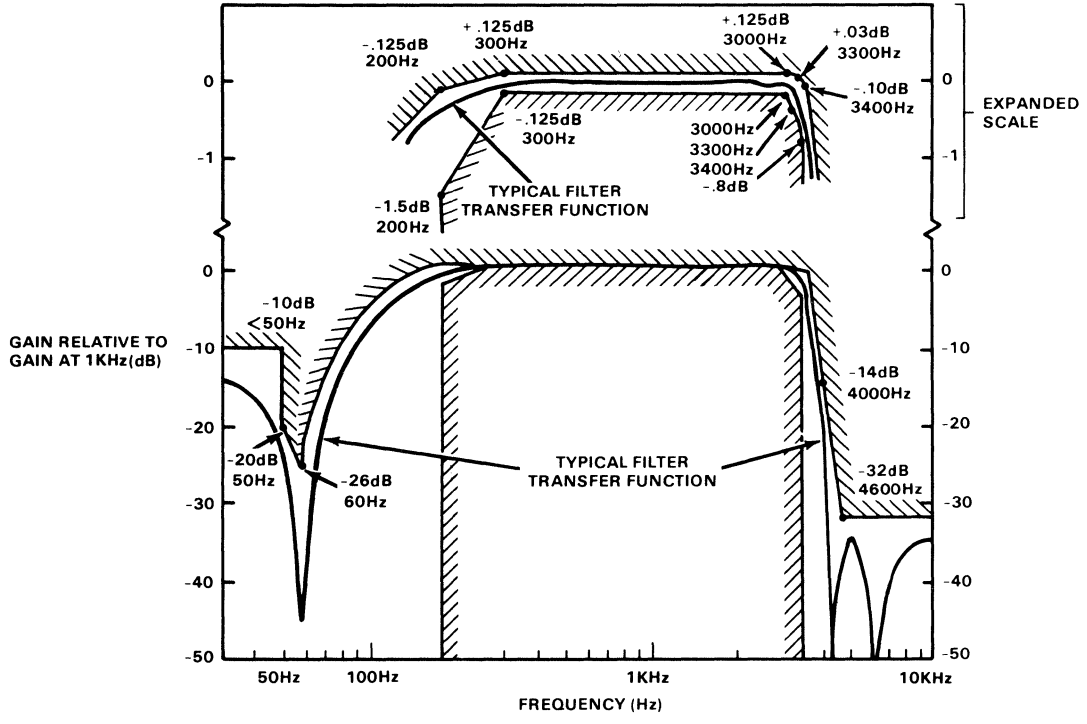


Fig. 2 Transmit Filter Transfer Characteristics

Receive Filter Anti-Aliasing Prefilter

An active RC low pass anti-aliasing filter is included on chip immediately preceding the receive filter section. This filter provides greater than 32dB rejection at 255KHz which is 1KHz below the receive filter effective sampling rate of 256KHz. This filter removes out-of-band noise generated by the codec which can be aliased in band by the filter. This results in significantly reduced harmonic distortion in the receive channel.

Receive Filter Transfer Characteristics

The receive section of the filter provides a passband flatness and stopband rejection which exceeds the Bell D3/D4 specifications and the CCITT G.712 recommendations, when used with a decoder which contains a sample/hold amplifier at its output. The filter contains the required compensation for the Sin x/x response of such decoders. The receive filter transfer characteristics and specifications, including the Sin x/x response of the decoder are shown in Fig. 3.

Receive Filter Output

The VFRO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VFRI TO VFRO is:

$$\frac{\left[\frac{\pi f}{8000}\right]}{\text{Sin}\left[\frac{\pi f}{8000}\right]}$$

which when multiplied by the output response of a suitable Codec results in a 0dB gain in the passband. The filter gain can be adjusted downward by a resistor voltage divider connected as shown in Fig. 4. The total resistive load RT on VFRO should not be less than 10KΩ. The output stage includes an active RC post filter to attenuate clock noise.

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VFRO is connected through gain setting resistors R1 and R2 to the amplifier input PWRI. The series combination of RS and the hybrid transformer must present a minimum AC load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown in Fig. 5. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it may be deactivated to save power. This is accomplished by tying the PWRI pin to VSS.

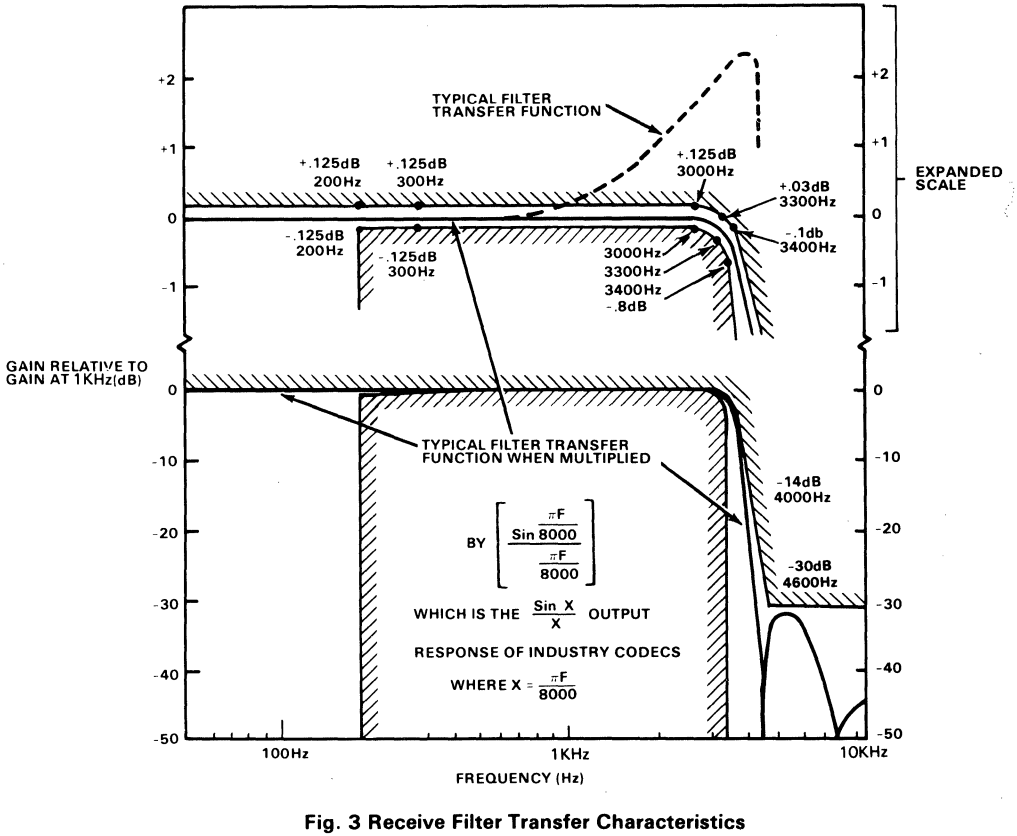


Fig. 3 Receive Filter Transfer Characteristics

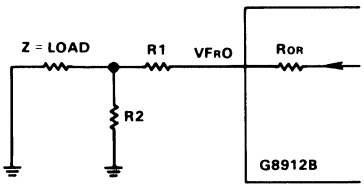


Fig. 4 Receive Filter Output Gain Adjustment

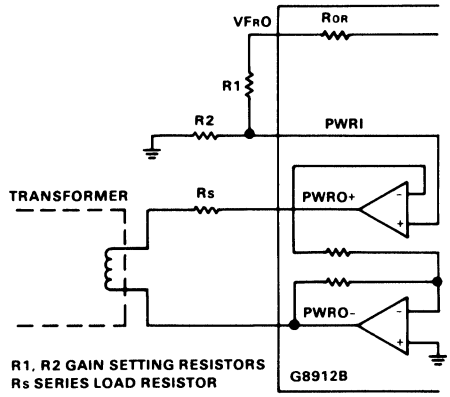


Fig. 5 Typical Connection of Output Driver Amplifier

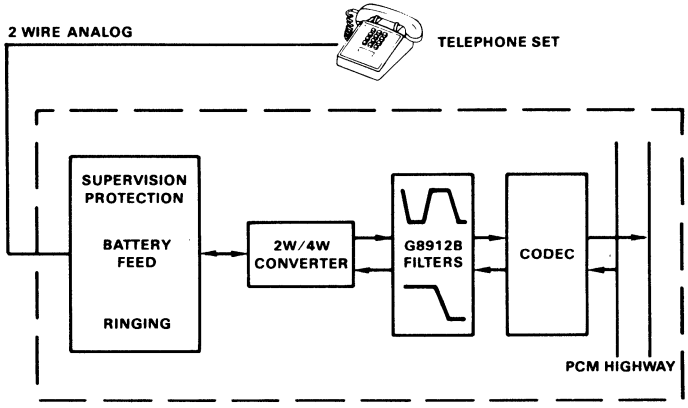
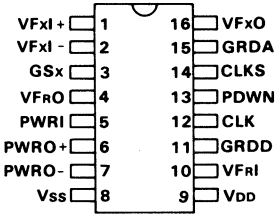


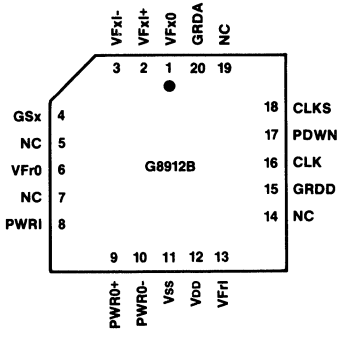
Fig. 6 Typical Line Termination

Pin Function Table

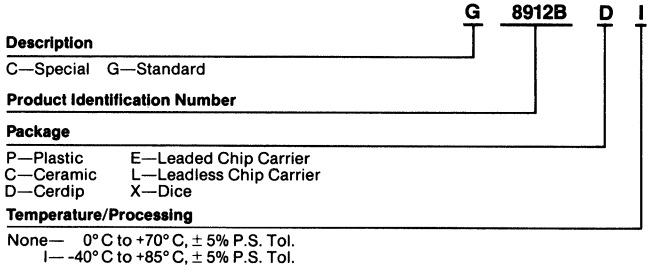
Name	Description
VFxI +	Analog input of the transmit filter from the 2 wire transmit output of a 2-to-4 wire converter
VFxI–	Inverting input of the gain adjustment op. amp on the transmit filter
GSX	Op. amp output used for gain setting of the transmit filter
VFRO	Analog output of the receive filter providing a direct interface to electronic 2-to-4 wire converter.
PWRI	Input to the power driver amplifiers. When tied to VSS these amplifiers are powered down.
PWRO+ PWRO–	Power amplifier outputs capable of directly driving transformer 2-to-4 wire converters.
VSS	Negative supply voltage (-5V)
VDD	Positive supply voltage (+5V)
VFRI	Analog input of the receive filter.
GRDD	Digital ground for internal clock generator.
CLK	Clock input. High impedance input. TTL-compatible voltage levels.
PDWN	Control input active high for the standby power down mode. Internal pull up to 5V. TTL-compatible voltage levels.
CLKS	Clock frequency select. CLK Input: 1.536MHz, 1.544MHz, 2.048MHz — CLKS Connection: VSS (-5V), GRDD, VDD (+5V)
GRDA	Analog ground for receive and transmit filters. Not internally connected to GRDD.
VFxO	Analog output of transmit filter.

Pin Configuration





Ordering Information



4 Applications

Application Note

G65SC00
Microprocessor

Microcircuits

GTE CMOS Brings New Life to 6500-Series Microprocessors

Introduction

GTE Microcircuits' CMOS family of G65SC00 microprocessors is not only pin compatible with NMOS versions currently available, but these new CMOS devices also offer several hardware and software enhancements that are not available in the older NMOS designs.

EXAMPLE—Low power consumption with significant new hardware and software features for ease of design and increased application flexibility.

GTE's CMOS process provides increased noise immunity, a wider operating voltage range, and a higher speed-to-power ratio. Furthermore, relaxed access time requirements allow a choice of either higher operating frequency or the use of slower memories and peripherals in existing systems.

EXAMPLE—Compatibility with NMOS versions.

GTE's G65SC00 microprocessor family provides an immediate system power savings when replacing the old NMOS processor. This feature may also lead to longer battery life, higher reliability, and greater immunity to transient-induced malfunctions.

EXAMPLE—GTE's new family members provide increased design flexibility.

New designs or simple modifications to existing designs can now take advantage of several hardware and software enhancements, such as:

- The on-chip oscillator and clock divider reduces the number of external oscillator components.
- The new Bus Enable input signal may eliminate the need for external address buffers, since the address bus can now be switched off internally.
- The enhanced functionality of the Ready input signal allows greater flexibility in the selection of memory and peripheral components.
- The new G65SC00 CMOS microprocessors are available in leadless chip carrier packages as well as dice, thus providing new system packaging options.

Hardware Improvements Save External Circuitry

Hardware improvements include:

An on-chip oscillator that requires no external active components—A crystal or R-C timing circuit are the only external components needed with the internal clock oscillator.

A single input clock that replaces two non-overlapping clock inputs—GTE's G65SC12 through G65SC15 circuits use only one clock phase when using an external clock generator.

The use of a slow RAM with a modified RDY input signal—GTE's CMOS processor can be halted during a write cycle due to an enhanced Ready input function. NMOS processors can only be stopped during a read cycle. This improvement enables the use of memories or peripherals which require an extended write cycle.

The use of slower memory and peripherals without extending the cycle time—Internal timing changes have significantly reduced the address setup delay, thus leaving a greater portion of the memory cycle for external data access.

Input pull-up resistors are no longer required—All input-only control signals have internal resistor pull-up devices connected to the positive supply. Unused or "wire-OR" inputs do not require external resistors.

Simple R-C circuit may be used with improved Reset input—The Reset input circuit has a Schmitt Trigger circuit to increase noise immunity and provide a positive reset function with a slowly varying signal. A simple resistor and capacitor circuit can be used as a reliable power-on-reset function.

An Enhanced Instruction Set Reduces Those Elusive Software Bugs

Software bugs and their solutions are as follows:

Invalid addresses—With the NMOS processor, an invalid memory location is read when the processor evaluates an indexed or relative address that crosses a page boundary. As an example, this problem will arise in systems using PIAs where reading the peripheral register resets the interrupt flags. If the read is unintentional, the interrupt condition may be ignored. **Solution**—To overcome this problem, GTE's G65SC00 Series CMOS microprocessor replaces the invalid address with a read of the last instruction byte. Figures 1 and 2 show this difference for both indexed and relative addressing.

Wrong jump address—When using the NMOS processor, an incorrect address is calculated by the Jump Indirect instruction if the low byte of the operand is FF hexadecimal. Most assemblers and loaders cannot check for this condition, so the error remains undetected until run time. Since the problem is "data dependent", the effects may be intermittent. **Solution**—This problem is corrected in the G65SC00 CMOS design by using an additional cycle to properly evaluate the effective address. Figure 3 illustrates the difference between the NMOS and CMOS processors for this instruction.

Undefined opcodes—With the NMOS processor, when a system "glitch" occurs and the microprocessor executes an undefined opcode, the results are always unpredictable. Recovery from this situation may require a system hardware reset, since the NMOS processor may not respond to a Non-Maskable interuupt. Data may be lost unnecessarily when only a software restart is required. **Solution**—GTE's CMOS processor defines all unused opcodes as No Operation, and a Non-Maskable interrupt is always recognized. Furthermore, the Reset signal functions the same as an interrupt, thus writing the program counter and status register in the stack before loading the Reset vector. This reset sequence is shown in Figure 4.

Invalid data—During a read-modify-write instruction (shift, rotate, increment, decrement), the previous data is always written to the effective address one cycle before writing the modified data. **Solution**—To prevent invalid data, GTE's CMOS processor substitutes another read cycle at the effective address. These instructions use one less cycle in the indexed addressing mode if a page boundary is not crossed. These differences are illustrated in Figure 5.

Invalid flags—The Z (Zero) and N (Negative) flags in the NMOS processor status register are not valid after a decimal add or subtract instruction. The Z Flag cannot be used to test for a zero result, and an extra instruction must be inserted to properly set the flag for testing. **Solution**—Within the CMOS processor, decimal add and subtract instructions use an extra "decimal adjust" cycle to set the Z and N flags using the same rules as in binary operations. Figure 6 shows the flag settings in both processors.

Undefined decimal mode—After reset, the NMOS processor status register Decimal Mode Bit is undefined. If a system uses interrupts and both decimal and binary modes, instructions must be used to initialize this mode after reset and in each interrupt servicing routine. **Solution**—GTE's CMOS processor treats this bit like the Interrupt Disable Bit, initializing to the binary mode during reset, during the Break instruction, and when servicing interrupts.

Unserviced interrupts—If an unmasked interrupt occurs during execution of a Break instruction, the interrupt is serviced and the Break instruction is ignored. Also, the program counter is not incremented on the stack, so the next Return From Interrupt instruction resumes execution at the byte following the Break opcode. Since the Break instruction normally skips this byte, the error also results in execution of an unforeseen instruction. **Solution**—The GTE CMOS processor completes the Break instruction before servicing the interrupt.

Additional OpCodes Reduce Program Size

New zero page indirect addressing mode—All arithmetic (ADC, AND, CMP, EOR, SBC) instructions have a zero page indirect addressing mode. The second instruction byte specifies the zero page memory word that contains the effective address. Figure 7 describes the bus status at each cycle for this new addressing mode.

Test and modify memory—The Test and Reset Bit (TRB) and the Test and Set Bit (TSB) instructions modify memory based on bits cleared or set in the accumulator. Both absolute and zero page addressing modes are available. The Z flag indicates the result of the accumulator "ANDed" with memory. Furthermore, the Memory Lock output signal is active during these instructions, thus allowing multiprocessor systems to operate with simplified bus arbitration. These read-modify-write instructions have the same cycle description as shown in Figure 5.

Unconditional branch—By using the relative addressing mode, the Branch Always (BRA) instruction saves program memory space compared to the Jump instruction. Refer to Figure 2 for the cycle description of this instruction.

Direct transfers between stack and index registers—Stack pushes and pulls for both index registers (PHX, PHY, PLX, PLY) not only reduce program memory space, but also reduce execution time. The bus cycles for these instructions are the same as the stack pushes and pulls for the accumulator and status registers.

Indexed indirect jump—This instruction facilitates the "computed go to" in high level language programs. Figure 8 shows the cycles used for this instruction.

Direct memory clear—The Store Zero (STZ) instruction clears memory without affecting register contents. Four addressing modes are available. The STZ instruction uses the same bus cycles as the STA instruction.

Other G65SC00 Series Advantages

4-X clock reduces crystal cost, boosts available access time—The divide-by-four circuit permits use of a higher frequency crystal. This means the widely used TV color burst crystal can be connected to the oscillator pins. The quadrature clock signals give an indication of a valid address earlier in the memory cycle, thus allowing an increase in access time available to the memory system.

Bus Enable signal reduces complexity in DMA applications—Address and data buffers may not be necessary in multiprocessor and Direct Memory Access (DMA) systems. The Bus Enable signal isolates both the address and data lines when the bus is controlled by another device.

Memory Lock signal is a must in multiprocessor systems—The Memory Lock output signal can be used in a multiprocessor system to ensure the integrity of read-modify-write instructions. During the time that Memory Lock is active, other processors are prohibited from accessing the shared memory area.

Explanation of Program Trace Column Headings

Program trace figures and listings within this Application Note provide a record of microprocessor activity during program execution. The state of address, data, and control signals is captured for each clock cycle.

Column Headings

FRAME—Represents the sequence number of the trace step in hexadecimal. The sequence is 0 to 7FF.
IFADDR—Represents the hexadecimal value on the address bus during an instruction fetch cycle.
ADDRESS—Represents the hexadecimal value on the address bus.
DATA—Represents the hexadecimal value on the data bus.
STATUS—Represents the type of processor activity:
R—memory read cycle (R/W = 1, SYNC = 0)
S—instruction fetch cycle (R/W = 1, SYNC = 1)
W—memory write cycle (R/W = 0, SYNC = 0)
MNEMONIC CODE—The value on the data bus during an instruction fetch cycle is translated into the assembly language mnemonic with the appropriate addressing mode.

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
0005	F885	F885	BD	S
0006		F886	47	R
0007		F887	F7	R
0008		F707	40	R - Invalid Address
0009		F807	AA	R

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
0005	F885	F885	BD	S
0006		F886	47	R
0007		F887	F7	R
0008		F887	F7	R - Read Last Instruction Byte
0009		F807	AA	R

Figure 1. Trace of LDA $F747, X
(X = $CO)

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
000A	F888	F888	D0	S
000B		F889	7A	R
000C		F88A	6C	R
000D		F804	4C	R - Invalid Address

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
000A	F888	F888	D0	S
000B		F889	7A	R
000C		F88A	6C	R
000D		F88A	6C	R - Read Last Instruction Byte

Figure 2. Trace of BNE $F904

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
0011	F88A	F88A	6C	S
0012		F88B	FF	R
0013		F88C	F8	R
0014		F8FF	01	R
0015		F800	F9	R - Wrong Indirect Address
0016	F901	F901	4C	S - Wrong Next Instruction

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
0011	F88A	F88A	6C	S
0012		F88B	FF	R
0013		F88C	F8	R
0014		F88C	F8	R - Extra Cycle
0015		F8FF	01	R
0016		F900	F8	R - Correct Indirect Address
0017	F801	F801	4C	S - Correct Next Instruction

Figure 3. Trace of JMP ($F8FF)

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS	RES	
07F2		0000	00	R	0	
07F3		0000	00	R	0	
07F4		0000	00	R	1	
07F5		0000	00	R	1	
07F6	0000	0000	00	S	1	- Start Reset Sequence
07F7		0000	00	R	1	
07F8		01FF	00	R	1	
07F9		01FE	66	R	1	
07FA		01FD	00	R	1	
07FB		FFFC	00	R	1	- Read PCL
07FC		FFFD	F8	R	1	- Read PCH
07FD	F800	F800	A2	S	1	- First Instruction

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS	RES	
07F3		F805	F8	R	0	
07F4		F805	F8	R	0	
07F5		F805	F8	R	1	
07F6	F805	F805	F8	S	1	- Start Reset Sequence
07F7		F805	F8	R	1	Write to Stack:
07F8		01FF	F8	W	1	- PCH
07F9		01FE	05	W	1	- PCL
07FA		01FD	A4	W	1	- Status
07FB		FFFC	00	R	1	- Read PCL
07FC		FFFD	F8	R	1	- Read PCH
07FD	F800	F800	A2	S	1	- First Instruction

Figure 4. Reset Sequence

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
001C	F88D	F88D	A2	S - LDX #$C0
001D		F88E	C0	R
001E	F88F	F88F	5E	S - LSR $F747, X
001F		F890	47	R
0020		F891	F7	R
0021		F707	40	R
0022		F807	AA	R
0023		F807	AA	W - Write Previous Data
0024		F807	55	W
0025	F892	F892	A2	S - LDX #$00
0026		F893	00	R
0027	F894	F894	3E	S - ROL $F807, X
0028		F895	07	R
0029		F896	F8	R
002A		F807	55	R
002B		F807	55	R
002C		F807	55	W - Write Previous Data
002D		F807	AA	W

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
001A	F88D	F88D	A2	S - LDX #$C0
001B		F88E	C0	R
001C	F88F	F88F	5E	S - LSR $F747, X
001D		F890	47	R
001E		F891	F7	R
001F		F891	F7	R
0020		F807	AA	R
0021		F807	AA	R - Reread Data
0022		F807	55	W
0023	F892	F892	A2	S - LDX #$00
0024		F893	00	R
0025	F894	F894	3E	S - ROL $F807, X
0026		F895	07	R
0027		F896	F8	R
0028		F807	55	R
0029		F807	55	R - Reread Data (one less cycle)
002A		F807	AA	W

Figure 5. Trace of Read-Modify-Write Instructions

(a.) NMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
002E	F897	F897	F8	S - SED
002F		F898	18	R
0030	F898	F898	18	S - CLC
0031		F899	A9	R
0032	F899	F899	A9	S - LDA #$99
0033		F89A	99	R
0034	F89B	F89B	69	S - ADC #$67 (2 cycles)
0035		F89C	67	R
0036	F89D	F89D	08	S - PHP
0037		F89E	18	R
0038		01FF	3F	W - Z Flag =1
0039	F89E	F89E	18	S - CLC
003A		F89F	A9	R
003B	F89F	F89F	A9	S - LDA #$99
003C		F8A0	99	R
003D	F8A1	F8A1	69	S - ADC #$01 (2 cycles)
003E		F8A2	01	R
003F	F8A3	F8A3	08	S - PHP
0040		F8A4	10	R
0041		01FE	BD	W - N Flag=1, Z Flag=0

(b.) CMOS processor

FRAME	IFADDR	ADDRESS	DATA	STATUS
002B	F897	F897	F8	S - SED
002C		F898	18	R
002D	F898	F898	18	S - CLC
002E		F899	A9	R
002F	F899	F899	A9	S - LDA #$99
0030		F89A	99	R
0031	F89B	F89B	69	S - ADC #$67 (3 cycles)
0032		F89C	67	R
0033		F89D	08	R
0034	F89D	F89D	08	S - PHP
0035		F89E	18	R
0036		01FF	3D	W - Z Flag=0
0037	F89E	F89E	18	S - CLC
0038		F89F	A9	R
0039	F89F	F89F	A9	S - LDA #$99
003A		F8A0	99	R
003B	F8A1	F8A1	69	S - ADC #$01 (3 cycles)
003C		F8A2	01	R
003D		F8A3	08	R
003E	F8A3	F8A3	08	S - PHP
003F		F8A4	10	R
0040		01FE	3F	W - N Flag=0, Z Flag=1

Figure 6. Trace of Decimal Add Instructions

FRAME	IFADDR	ADDRESS	DATA	STATUS
005F	F916	F916	12	S
0060		F917	C0	R
0061		00C0	04	R
0062		00C1	F8	R
0063		F804	4C	R

Figure 7. Trace of ORA ($C0)

FRAME	IFADDR	ADDRESS	DATA	STATUS
0056	F913	F913	7C	S
0057		F914	C0	R
0058		F915	00	R
0059		F915	00	R
005A		00C0	04	R
005B		00C1	F8	R

Figure 8. Trace of JMP ($00C0,X) (X = $00)

Appendix A

CMOS G65SC00 8-Bit Microprocessor Family

This assembly language program highlights the functional differences between the **old** 6500-Series and GTE's **new** CMOS G65SC00 family of microprocessors.

```
0012  0000              65C02 ON
0013  0000          *
0014  0000          ************************************************************
0015  0000          *                                                          *
0016  0000          *                                                          *
0017  0000          *                                                          *
0018  0000          *                                                          *
0019  0000          *                                                          *
0020  0000          *                    GTE Microcircuits                     *
0021  0000          *                    Applications Engineering              *
0022  0000          *                                                          *
0023  0000          *                    2000 West 14th Street                 *
0024  0000          *                    Tempe, Arizona  85281                 *
0025  0000          *                                                          *
0026  0000          *                    Author:  Peter L. Chapin              *
0027  0000          *                    Date:    June, 1983                   *
0028  0000          *                                                          *
0029  0000          *                                                          *
0030  0000          *                                                          *
0031  0000          *                                                          *
0032  0000          *                                                          *
0033  0000          ************************************************************
0034  0000          *
0035  0000          ITEST  START
0036  0000          *
0037  0000          * Program Constants
0038  0000          ZPG    EQU   $C0      PAGE ZERO ADDRESS
0039  0000          IND    EQU   $C0      INDIRECT ADDRESS
0040  0000          IMM    EQU   $AA      IMMEDIATE DATA
0041  0000          *
0042  0000                ORG   $F800
0043  0000 F9             DC    I1'$F9'  HIGH BYTE FOR NMOS JMP($XXFF) TEST
0044  0001 4C1500   JMPADR JMP   NEXT     RETURN FOR JMP($XXFF) TEST
0045  0004 4C4B00   JMPIND JMP   NEXT2    RETURN FOR JMP(IND,X) TEST
0046  0007 AA       ABS    DC    I1'$AA'  DATA FOR ABSOLUTE ADDRESSING MODES
0047  0008          *
0048  0008                ORG   $F880
0049  0008          *
0050  0008          ************************************************************
0051  0008          *                                                          *
0052  0008          *  PROGRAM STARTS HERE                                     *
0053  0008          *                                                          *
0054  0008          ************************************************************
0055  0008          *
0056  0008          * INITIALIZATION
0057  0008          RESET  ENTRY
```

Appendix A (Continued)

CMOS DEMO

```
0058  0008 A2FF            LDX   #$FF
0059  000A 9A              TXS
0060  000B                 EJECT
0061  000B           ************************************************************
0062  000B           *                                                          *
0063  000B           * An invalid memory location is read when the NMOS         *
0064  000B           *      processor evaluates an indexed address that         *
0065  000B           *      crosses a page boundary.                            *
0066  000B           *                                                          *
0067  000B           * The CMOS microprocessor replaces the invalid address    *
0068  000B           *      with a read of the last instruction byte.           *
0069  000B           *                                                          *
0070  000B           ************************************************************
0071  000B           *
0072  000B A2C0            LDX   #$C0
0073  000D BD47FF          LDA   ABS-$C0,X          CMOS REREADS LAST BYTE
0074  0010           *                              NMOS READS "ABS" - $100
0075  0010           *
0076  0010           ************************************************************
0077  0010           *                                                          *
0078  0010           * An invalid memory location is read when the NMOS         *
0079  0010           *      processor takes a relative branch across a          *
0080  0010           *      page boundary.                                      *
0081  0010           *                                                          *
0082  0010           * The CMOS microprocessor reads the next opcode.           *
0083  0010           *                                                          *
0084  0010           ************************************************************
0085  0010           *
0086  0010 D027            BNE   REL      CMOS READS NEXT OPCODE TWICE
0087  0012           *                     NMOS READS NEXT OPCODE,
0088  0012           *                           THEN "REL" - $100
0089  0012           *
0090  0012           ************************************************************
0091  0012           *                                                          *
0092  0012           * An incorrect address is calculated by the NMOS           *
0093  0012           *      Jump Indirect instruction if the low byte of        *
0094  0012           *      the operand is FF hexadecimal.                      *
0095  0012           *                                                          *
0096  0012           * The CMOS design uses an additional cycle to properly     *
0097  0012           *      evaluate the effective address.                     *
0098  0012           *                                                          *
0099  0012           ************************************************************
0100  0012           *
0101  0012 6C3400    BACK  JMP   (JMPOFR)           CMOS PC = "JMPADR"
0102  0015           *                              NMOS PC = "WRONG"
0103  0015           ************************************************************
0104  0015           *                                                          *
0105  0015           * During a read-modify-write instruction (shift, rotate,   *
0106  0015           *      increment, decrement), the NMOS processor writes    *
0107  0015           *      the current data, then the modified data in the     *
0108  0015           *      effective address.                                  *
0109  0015           *                                                          *
0110  0015           * The CMOS processor substitutes another read cycle        *
0111  0015           *      at the effective address.                           *
0112  0015           *                                                          *
0113  0015           ************************************************************
0114  0015           *
```

Appendix A (Continued)

CMOS DEMO

```
0115  0015 A2C0      NEXT   LDX    #$C0
0116  0017 5E47FF           LSR    ABS-$C0,X        CMOS REREADS "ABS"
0117  001A            *                           NMOS WRITES $AA AT "ABS"
0118  001A                   EJECT
0119  001A            ************************************************************
0120  001A            *                                                          *
0121  001A            * One less cycle is used by the CMOS processor for         *
0122  001A            *      read-modify-write instructions in the absolute      *
0123  001A            *      indexed addressing mode if a page boundary is       *
0124  001A            *      not crossed.                                        *
0125  001A            *                                                          *
0126  001A            ************************************************************
0127  001A            *
0128  001A A200             LDX    #$00
0129  001C 3E0700           ROL    ABS,X    CMOS = 6 CYCLES
0130  001F            *                     NMOS = 7 CYCLES
0131  001F            *
0132  001F            ************************************************************
0133  001F            *                                                          *
0134  001F            * The N (Negative) and Z (Zero) flags in the NMOS          *
0135  001F            *      processor are not valid after a decimal add         *
0136  001F            *      or subtract instruction.                            *
0137  001F            *                                                          *
0138  001F            * The CMOS processor uses an extra "decimal adjust"        *
0139  001F            *      cycle to correctly set the N and Z flags.           *
0140  001F            *                                                          *
0141  001F            * CMOS N FLAG = BIT 7 OF RESULT                            *
0142  001F            * NMOS N FLAG = BIT 7 OF RESULT OF DECIMAL OPERATION ON    *
0143  001F            *                  LOWER NIBBLE AND BINARY OPERATION ON    *
0144  001F            *                  UPPER NIBBLE                            *
0145  001F            *                                                          *
0146  001F            * CMOS Z FLAG = 1 IF RESULT IS ZERO                        *
0147  001F            * NMOS Z FLAG = 1 IF BINARY RESULT IS ZERO                 *
0148  001F            *                                                          *
0149  001F            ************************************************************
0150  001F            *
0151  001F F8               SED
0152  0020 18               CLC
0153  0021 A999             LDA    #$99
0154  0023 6967             ADC    #$67     RESULT = $66, CMOS Z = 0, 3 CYCLES
0155  0025            *                                  NMOS Z = 1, 2 CYCLES
0156  0025 08               PHP
0157  0026            *
0158  0026 18               CLC
0159  0027 A999             LDA    #$99
0160  0029 6901             ADC    #$01     RESULT = $00, CMOS N = 0, Z = 1,
0161  002B            *                                    3 CYCLES
0162  002B            *                                NMOS N = 1, Z = 0,
0163  002B            *                                  2 CYCLES
0164  002B 08               PHP
0165  002C            *
0166  002C            * THIS DIFFERENCE CAN BE USED TO TEST THE PROCESSOR TYPE
0167  002C 1003             BPL    AROUND
0168  002E            *
0169  002E 4C2E10           JMP    *        END OF PROGRAM FOR NMOS
0170  0031            *
0171  0031 4C3C00     AROUND JMP    NEWTST
```

Appendix A (Continued)

CMOS DEMO

```
0172  0034                    EJECT
0173  0034              *
0174  0034                    ORG    $F8FF
0175  0034              *                        OPERAND FOR JMP ($XXFF)
0176  0034 01F8        JMPOPR DC     A'$F801' "JMPADR"
0177  0036              *
0178  0036 4C0100      WRONG  JMP    JMPADR  NMOS WILL EXECUTE THIS
0179  0039              *
0180  0039 4C1200      REL    JMP    BACK
0181  003C              *
0182  003C              * SETUP INDIRECT ADDRESS FOR JMP (IND,X)
0183  003C A904        NEWTST LDA    #$04
0184  003E 85C0              STA    ZPG
0185  0040 A9F8              LDA    #$F8
0186  0042 85C1              STA    ZPG+1
0187  0044 A200              LDX    #$00
0188  0046              *
0189  0046              ************************************************************
0190  0046              *                                                          *
0191  0046              *       New opcodes                                        *
0192  0046              *                                                          *
0193  0046              ************************************************************
0194  0046              *
0195  0046 8000              BRA    NEXT1
0196  0048              *
0197  0048 7CC000      NEXT1  JMP    (IND,X)
0198  004B              *
0199  004B 12C0        NEXT2  ORA    (IND)
0200  004D 32C0              AND    (IND)
0201  004F 52C0              EOR    (IND)
0202  0051 72C0              ADC    (IND)
0203  0053 92C0              STA    (IND)
0204  0055 B2C0              LDA    (IND)
0205  0057 D2C0              CMP    (IND)
0206  0059 F2C0              SBC    (IND)
0207  005B              *
0208  005B 04C0              TSB    ZPG
0209  005D 14C0              TRB    ZPG
0210  005F 34C0              BIT    ZPG,X
0211  0061 64C0              STZ    ZPG
0212  0063 74C0              STZ    ZPG,X
0213  0065              *
0214  0065 89AA              BIT    #IMM
0215  0067              *
0216  0067 1A                INC    A        OR  INA
0217  0068 3A                DEC    A        OR  DEA
0218  0069 5A                PHY
0219  006A 7A                PLY
0220  006B DA                PHX
0221  006C FA                PLX
0222  006D              *
0223  006D 0C0700            TSB    ABS
0224  0070 1C0700            TRB    ABS
0225  0073 3C0700            BIT    ABS,X
0226  0076 9C0700            STZ    ABS
0227  0079              *
0228  0079 9E0700            STZ    ABS,X
```

Appendix A (Continued)

CMOS DEMO

```
0229  007C                    EJECT
0230  007C           ************************************************************
0231  007C           *                                                          *
0232  007C           * Unused opcodes - reserved for future 16- and 32-bit      *
0233  007C           *                  processors.                             *
0234  007C           *                                                          *
0235  007C           ************************************************************
0236  007C           *
0237  007C           *    2 BYTE, 2 CYCLE
0238  007C 020022          DC    H'0200 2200 4200 6200 8200 C200 E200'
0239  008A           *
0240  008A           *    1 BYTE, 1 CYCLE
0241  008A 031323          DC    H'03 13 23 33 43 53 63 73'
0242  0092 8393A3          DC    H'83 93 A3 B3 C3 D3 E3 F3'
0243  009A           *
0244  009A 071727          DC    H'07 17 27 37 47 57 67 77'
0245  00A2 8797A7          DC    H'87 97 A7 B7 C7 D7 E7 F7'
0246  00AA           *
0247  00AA 0B1B2B          DC    H'0B 1B 2B 3B 4B 5B 6B 7B'
0248  00B2 8B9BAB          DC    H'8B 9B AB BB CB DB EB FB'
0249  00BA           *
0250  00BA 0F1F2F          DC    H'0F 1F 2F 3F 4F 5F 6F 7F'
0251  00C2 8F9FAF          DC    H'8F 9F AF BF CF DF EF FF'
0252  00CA           *
0253  00CA           *    2 BYTE, 3 CYCLE
0254  00CA 4400            DC    H'4400'
0255  00CC           *
0256  00CC           *    2 BYTE, 4 CYCLE
0257  00CC 5400D4          DC    H'5400 D400 F400'
0258  00D2           *
0259  00D2           *    3 BYTE, 8 CYCLE
0260  00D2 5C0000          DC    H'5C0000'
0261  00D5           *
0262  00D5           *    3 BYTE, 4 CYCLE
0263  00D5 DC0000          DC    H'DC0000 FC0000'
0264  00DB           *
0265  00DB 4CDB10          JMP   *       END OF PROGRAM
0266  00DE           *
0267  00DE                 ORG   $FFFC
0268  00DE 0810            DC    A'RESET'        RESET VECTOR
0269  00E0                 END
```

```
Local  Symbol Table

ABS         0007  AROUND      0031  BACK        0012  IMM         00AA
IND         00C0  JMPADR      0001  JMPIND      0004  JMPOPR      0034
NEWTST      003C  NEXT        0015  NEXT1       0048  NEXT2       004B
REL         0039  RESET       0008  WRONG       0036  ZPG         00C0

0 macros expanded
```

Appendix B

Comparison of Program Instruction Trace—Old NMOS vs. New CMOS G65SC00 Microprocessors

Old NMOS Program Instruction Trace

FRAME	ADDRESS	DATA	MNEMONIC-CODE
0001	F882	9A	TXS
0003	F883	A2	LDX #C0
0005	F885	BD	LDA F747, X
000A	F888	D0	BNE F904
000E	F904	4C	JMP F88A
0011	F88A	6C	JMP (F8FF)
0016	F901	4C	JMP F801
0019	F801	4C	JMP F88D
001C	F88D	A2	LDX #C0
001E	F88F	5E	LSR F747, X
0025	F892	A2	LDX #00
0027	F894	3E	ROL F807, X
002E	F897	F8	SED
0030	F898	18	CLC
0032	F899	A9	LDA #99
0034	F89B	69	ADC #67
0036	F89D	08	PHP
0039	F89E	18	CLC
003B	F89F	A9	LDA #99
003D	F8A1	69	ADC #01
003F	F8A3	08	PHP
0042	F8A4	10	BPL F8A9
0044	F8A6	4C	JMP F8A6
0047	F8A6	4C	JMP F8A6

New CMOS G65SC00 Program Instruction Trace

FRAME	ADDRESS	DATA	MNEMONIC-CODE
0001	F882	9A	TXS
0003	F883	A2	LDX #C0
0005	F885	BD	LDA F747, X
000A	F888	D0	BNE F904
000E	F904	4C	JMP F88A
0011	F88A	6C	JMP (F8FF)
0017	F801	4C	JMP F88D
001A	F88D	A2	LDX #C0
001C	F88F	5E	LSR F747, X
0023	F892	A2	LDX #00
0025	F894	3E	ROL F807, X
002B	F897	F8	SED
002D	F898	18	CLC
002F	F899	A9	LDA #99
0031	F89B	69	ADC #67
0034	F89D	08	PHP
0037	F89E	18	CLC
0039	F89F	A9	LDA #99
003B	F8A1	69	ADC #01
003E	F8A3	08	PHP
0041	F8A4	10	BPL F8A9
0044	F8A9	4C	JMP F907
0047	F907	A9	LDA #04
0049	F909	85	STA C0
004C	F90B	A9	LDA #F8
004E	F90D	85	STA C1
0051	F90F	A2	LDX #00
0053	F911	80	BRA F913
0056	F913	7C	JMP (00C0, X)
005C	F804	4C	JMP F916
005F	F916	12	ORA (C0)
0064	F918	32	AND (C0)
0069	F91A	52	EOR (C0)
006E	F91C	72	ADC (C0)
0074	F91E	92	STA (C0)
0079	F920	B2	LDA (C0)
007E	F922	D2	CMP (C0)
0083	F924	F2	SBC (C0)
0089	F926	04	TSB C0
008E	F928	14	TRB C0
0093	F92A	34	BIT C0, X
0097	F92C	64	STZ C0
009A	F92E	74	STZ C0, X
009E	F930	89	BIT #AA
00A0	F932	1A	INC A
00A2	F933	3A	DEC A
00A4	F934	5A	PHY
00A7	F935	7A	PLY
00AB	F936	DA	PHX
00AE	F937	FA	PLX
00B2	F938	0C	TSB F807
00B8	F93B	1C	TRB F807
00BE	F93E	3C	BIT F807, X
00C2	F941	9C	STZ F807
00C6	F944	9E	STZ F807, X
00CB	F947	02	?
00CD	F949	22	?
00CF	F94B	42	?
00D1	F94D	62	?
00D3	F94F	82	?
00D5	F951	C2	?
00D7	F953	E2	?
00D9	F955	03	?
00DA	F956	13	?
00DB	F957	23	?
00DC	F958	33	?
00DD	F959	43	?
00DE	F95A	53	?
00DF	F95B	63	?
00E0	F95C	73	?
00E1	F95D	83	?
00E2	F95E	93	?
00E3	F95F	A3	?
00E4	F960	B3	?
00E5	F961	C3	?
00E6	F962	D3	?

Appendix B (Continued) CMOS DEMO

FRAME	ADDRESS	DATA	MNEMONIC-CODE
00E7	F963	E3	?
00E8	F964	F3	?
00E9	F965	07	?
00EA	F966	17	?
00EB	F967	27	?
00EC	F968	37	?
00ED	F969	47	?
00EE	F96A	57	?
00EF	F96B	67	?
00F0	F96C	77	?
00F1	F96D	87	?
00F2	F96E	97	?
00F3	F96F	A7	?
00F4	F970	B7	?
00F5	F971	C7	?
00F6	F972	D7	?
00F7	F973	E7	?
00F8	F974	F7	?
00F9	F975	0B	?
00FA	F976	1B	?
00FB	F977	2B	?
00FC	F978	3B	?
00FD	F979	4B	?
00FE	F97A	5B	?
00FF	F97B	6B	?
0100	F97C	7B	?
0101	F97D	8B	?
0102	F97E	9B	?
0103	F97F	AB	?
0104	F980	BB	?
0105	F981	CB	?
0106	F982	DB	?
0107	F983	EB	?
0108	F984	FB	?
0109	F985	0F	?
010A	F986	1F	?
010B	F987	2F	?
010C	F988	3F	?
010D	F989	4F	?
010E	F98A	5F	?
010F	F98B	6F	?
0110	F98C	7F	?
0111	F98D	8F	?
0112	F98E	9F	?
0113	F98F	AF	?
0114	F990	BF	?
0115	F991	CF	?
0116	F992	DF	?
0117	F993	EF	?
0118	F994	FF	?
0119	F995	44	?
011C	F997	54	?
0120	F999	D4	?
0124	F99B	F4	?
0128	F99D	5C	?
0130	F9A0	DC	?
0134	F9A3	FC	?
0138	F9A6	4C	JMP F9A6
013B	F9A6	4C	JMP F9A6

Appendix C

Comparison of Program Cycle Trace—Old NMOS vs. New CMOS G65SC00 Microprocessors

Old NMOS Program Cycle Trace

FRAME	1FADDR	ADDRESS	DATA	STATUS
0000		F881	FF	R
0001	F882	F882	9A	S
0002		F883	A2	R
0003	F883	F883	A2	S
0004		F884	C0	R
0005	F885	F885	BD	S
0006		F886	47	R
0007		F887	F7	R
0008		F707	00	R
0009		F807	AA	R
000A	F888	F888	D0	S
000B		F889	7A	R
000C		F88A	6C	R
000D		F804	4C	R
000E	F904	F904	4C	S
000F		F905	8A	R
0010		F906	F8	R
0011	F88A	F88A	6C	S
0012		F88B	FF	R
0013		F88C	F8	R
0014		F8FF	01	R
0015		F800	F9	R
0016	F901	F901	4C	S
0017		F902	01	R
0018		F903	F8	R
0019	F801	F801	4C	S
001A		F802	8D	R
001B		F803	F8	R
001C	F88D	F88D	A2	S
001D		F88E	C0	R
001E	F88F	F88F	5E	S
001F		F890	47	R
0020		F891	F7	R
0021		F707	00	R
0022		F807	AA	R
0023		F807	AA	W
0024		F807	55	W
0025	F892	F892	A2	S
0026		F893	00	R
0027	F894	F894	3E	S
0028		F895	07	R
0029		F896	F8	R
002A		F807	55	R
002B		F807	55	R
002C		F807	55	W
002D		F807	AA	W
002E	F897	F897	F8	S

Appendix C (Continued)

NMOS DEMO

FRAME	IFADDR	ADDRESS	DATA	STATUS
002F		F898	18	R
0030	F898	F898	18	S
0031		F899	A9	R
0032	F899	F899	A9	S
0033		F89A	99	R
0034	F89B	F89B	69	S
0035		F89C	67	R
0036	F89D	F89D	08	S
0037		F89E	18	R
0038		01FF	3F	W
0039	F89E	F89E	18	S
003A		F89F	A9	R
003B	F89F	F89F	A9	S
003C		F8A0	99	R
003D	F8A1	F8A1	69	S
003E		F8A2	01	R
003F	F8A3	F8A3	08	S
0040		F8A4	10	R
0041		01FE	BD	W
0042	F8A4	F8A4	10	S
0043		F8A5	03	R
0044	F8A6	F8A6	4C	S
0045		F8A7	A6	R
0046		F8A8	F8	R
0047	F8A6	F8A6	4C	S

New CMOS G65SC00 Program Cycle Trace

FRAME	IFADDR	ADDRESS	DATA	STATUS
0000		F881	FF	R
0001	F882	F882	9A	S
0002		F883	A2	R
0003	F883	F883	A2	S
0004		F884	C0	R
0005	F885	F885	BD	S
0006		F886	47	R
0007		F887	F7	R
0008		F887	F7	R
0009		F807	AA	R
000A	F888	F888	D0	S
000B		F889	7A	R
000C		F88A	6C	R
000D		F88A	6C	R
000E	F904	F904	4C	S
000F		F905	8A	R
0010		F906	F8	R
0011	F88A	F88A	6C	S
0012		F88B	FF	R
0013		F88C	F8	R
0014		F88C	F8	R
0015		F8FF	01	R
0016		F900	F8	R
0017	F801	F801	4C	S
0018		F802	8D	R
0019		F803	F8	R
001A	F88D	F88D	A2	S
001B		F88E	C0	R
001C	F88F	F88F	5E	S
001D		F890	47	R
001E		F891	F7	R
001F		F891	F7	R
0020		F807	AA	R
0021		F807	AA	R
0022		F807	55	W
0023	F892	F892	A2	S
0024		F893	00	R
0025	F894	F894	3E	S
0026		F895	07	R
0027		F896	F8	R
0028		F807	55	R
0029		F807	55	R
002A		F807	AA	W
002B	F897	F897	F8	S
002C		F898	18	R
002D	F898	F898	18	S
002E		F899	A9	R
002F	F899	F899	A9	S
0030		F89A	99	R
0031	F89B	F89B	69	S
0032		F89C	67	R
0033		F89D	08	R
0034	F89D	F89D	08	S
0035		F89E	18	R
0036		01FF	3D	W
0037	F89E	F89E	18	S
0038		F89F	A9	R
0039	F89F	F89F	A9	S
003A		F8A0	99	R
003B	F8A1	F8A1	69	S
003C		F8A2	01	R
003D		F8A3	08	R
003E	F8A3	F8A3	08	S
003F		F8A4	10	R
0040		01FE	3F	W
0041	F8A4	F8A4	10	S
0042		F8A5	03	R
0043		F8A6	4C	R
0044	F8A9	F8A9	4C	S
0045		F8AA	07	R
0046		F8AB	F9	R
0047	F907	F907	A9	S
0048		F908	04	R
0049	F909	F909	85	S
004A		F90A	C0	R
004B		00C0	04	W
004C	F90B	F90B	A9	S
004D		F90C	F8	R
004E	F90D	F90D	85	S
004F		F90E	C1	R

Appendix C (Continued)

CMOS DEMO

FRAME	IFADDR	ADDRESS	DATA	STATUS
0050		00C1	F8	W
0051	F90F	F90F	A2	S
0052		F910	00	R
0053	F911	F911	80	S
0054		F912	00	R
0055		F913	7C	R
0056	F913	F913	7C	S
0057		F914	C0	R
0058		F915	00	R
0059		F915	00	R
005A		00C0	04	R
005B		00C1	F8	R
005C	F804	F804	4C	S
005D		F805	16	R
005E		F806	F9	R
005F	F916	F916	12	S
0060		F917	C0	R
0061		00C0	04	R
0062		00C1	F8	R
0063		F804	4C	R
0064	F918	F918	32	S
0065		F919	C0	R
0066		00C0	04	R
0067		00C1	F8	R
0068		F804	4C	R
0069	F91A	F91A	52	S
006A		F91B	C0	R
006B		00C0	04	R
006C		00C1	F8	R
006D		F804	4C	R
006E	F91C	F91C	72	S
006F		F91D	C0	R
0070		00C0	04	R
0071		00C1	F8	R
0072		F804	4C	R
0073		F91E	92	R
0074	F91E	F91E	92	S
0075		F91F	C0	R
0076		00C0	04	R
0077		00C1	F8	R
0078		F804	53	W
0079	F920	F920	B2	S
007A		F921	C0	R
007B		00C0	04	R
007C		00C1	F8	R
007D		F804	53	R
007E	F922	F922	D2	S
007F		F923	C0	R
0080		00C0	04	R
0081		00C1	F8	R
0082		F804	53	R
0083	F924	F924	F2	S
0084		F925	C0	R
0085		00C0	04	R
0086		00C1	F8	R
0087		F804	53	R
0088		F926	04	R
0089	F926	F926	04	S
008A		F927	C0	R
008B		00C0	04	R
008C		00C0	04	R
008D		00C0	04	W
008E	F928	F928	14	S
008F		F929	C0	R
0090		00C0	04	R
0091		00C0	04	R
0092		00C0	04	W
0093	F92A	F92A	34	S
0094		F92B	C0	R
0095		F92B	C0	R
0096		00C0	04	R
0097	F92C	F92C	64	S
0098		F92D	C0	R
0099		00C0	00	W
009A	F92E	F92E	74	S
009B		F92F	C0	R
009C		F92F	C0	R
009D		00C0	00	W
009E	F930	F930	89	S
009F		F931	AA	R
00A0	F932	F932	1A	S
00A1		F933	3A	R
00A2	F933	F933	3A	S
00A3		F934	5A	R
00A4	F934	F934	5A	S
00A5		F935	7A	R
00A6		01FD	00	W
00A7	F935	F935	7A	S
00A8		F936	DA	R
00A9		01FC	FF	R
00AA		01FD	00	R
00AB	F936	F936	DA	S
00AC		F937	FA	R
00AD		01FD	00	W
00AE	F937	F937	FA	S
00AF		F938	0C	R
00B0		01FC	FF	R
00B1		01FD	00	R
00B2	F938	F938	0C	S
00B3		F939	07	R
00B4		F93A	F8	R
00B5		F807	AA	R
00B6		F807	AA	R
00B7		F807	AA	W
00B8	F93B	F93B	1C	S
00B9		F93C	07	R
00BA		F93D	F8	R
00BB		F807	AA	R
00BC		F807	AA	R
00BD		F807	AA	W
00BE	F93E	F93E	3C	S
00BF		F93F	07	R
00C0		F940	F8	R
00C1		F807	AA	R
00C2	F941	F941	9C	S
00C3		F942	07	R
00C4		F943	F8	R
00C5		F807	00	W
00C6	F944	F944	9E	S
00C7		F945	07	R
00C8		F946	F8	R
00C9		F807	00	R

Appendix C (Continued)

CMOS DEMO

FRAME	1FADDR	ADDRESS	DATA	STATUS
00CA		F807	00	W
00CB	F947	F947	02	S
00CC		F948	00	R
00CD	F949	F949	22	S
00CE		F94A	00	R
00CF	F94B	F94B	42	S
00D0		F94C	00	R
00D1	F94D	F94D	62	S
00D2		F94E	00	R
00D3	F94F	F94F	82	S
00D4		F950	00	R
00D5	F951	F951	C2	S
00D6		F952	00	R
00D7	F953	F953	E2	S
00D8		F954	00	R
00D9	F955	F955	03	S
00DA	F956	F956	13	S
00DB	F957	F957	23	S
00DC	F958	F958	33	S
00DD	F959	F959	43	S
00DE	F95A	F95A	53	S
00DF	F95B	F95B	63	S
00E0	F95C	F95C	73	S
00E1	F95D	F95D	83	S
00E2	F95E	F95E	93	S
00E3	F95F	F95F	A3	S
00E4	F960	F960	B3	S
00E5	F961	F961	C3	S
00E6	F962	F962	D3	S
00E7	F963	F963	E3	S
00E8	F964	F964	F3	S
00E9	F965	F965	07	S
00EA	F966	F966	17	S
00EB	F967	F967	27	S
00EC	F968	F968	37	S
00ED	F969	F969	47	S
00EE	F96A	F96A	57	S
00EF	F96B	F96B	67	S
00F0	F96C	F96C	77	S
00F1	F96D	F96D	87	S
00F2	F96E	F96E	97	S
00F3	F96F	F96F	A7	S
00F4	F970	F970	B7	S
00F5	F971	F971	C7	S
00F6	F972	F972	D7	S
00F7	F973	F973	E7	S
00F8	F974	F974	F7	S
00F9	F975	F975	0B	S
00FA	F976	F976	1B	S
00FB	F977	F977	2B	S
00FC	F978	F978	3B	S
00FD	F979	F979	4B	S
00FE	F97A	F97A	5B	S
00FF	F97B	F97B	6B	S
0100	F97C	F97C	7B	S
0101	F97D	F97D	8B	S
0102	F97E	F97E	9B	S
0103	F97F	F97F	AB	S
0104	F980	F980	BB	S
0105	F981	F981	CB	S
0106	F982	F982	DB	S
0107	F983	F983	EB	S
0108	F984	F984	FB	S
0109	F985	F985	0F	S
010A	F986	F986	1F	S
010B	F987	F987	2F	S
010C	F988	F988	3F	S
010D	F989	F989	4F	S
010E	F98A	F98A	5F	S
010F	F98B	F98B	6F	S
0110	F98C	F98C	7F	S
0111	F98D	F98D	8F	S
0112	F98E	F98E	9F	S
0113	F98F	F98F	AF	S
0114	F990	F990	BF	S
0115	F991	F991	CF	S
0116	F992	F992	DF	S
0117	F993	F993	EF	S
0118	F994	F994	FF	S
0119	F995	F995	44	S
011A		F996	00	R
011B		0000	02	R
011C	F997	F997	54	S
011D		F998	00	R
011E		F998	00	R
011F		0000	02	R
0120	F999	F999	D4	S
0121		F99A	00	R
0122		F99A	00	R
0123		0000	02	R
0124	F99B	F99B	F4	S
0125		F99C	00	R
0126		F99C	00	R
0127		0000	02	R
0128	F99D	F99D	5C	S
0129		F99E	00	R
012A		F99F	00	R
012B		FF00	00	R
012C		FFFF	00	R
012D		FFFF	00	R
012E		FFFF	00	R
012F		FFFF	00	R
0130	F9A0	F9A0	DC	S
0131		F9A1	00	R
0132		F9A2	00	R
0133		0000	02	R
0134	F9A3	F9A3	FC	S
0135		F9A4	00	R
0136		F9A5	00	R
0137		0000	02	R
0138	F9A6	F9A6	4C	S
0139		F9A7	A6	R
013A		F9A8	F9	R
013B	F9A6	F9A6	4C	S

GTE

Application Note

G65SC150
Telecommunication Microcomputer

Microcircuits

GTE 65SC150 Communications Terminal Unit (CTU) Offers Maximum Flexibility in 300 Baud Modem Designs

Introduction

GTE Microcircuits' G65SC150 Communications Terminal Unit (CTU) is a highly versatile and reliable single-chip telecommunications microcomputer, based on state-of-the-art silicon gate CMOS technology. The G65SC150 CTU reflects GTE's extensive telecommunications experience, thus providing the design engineer with not only a high level of performance, but many valuable functions which have been optimized for use in telephone line signaling and data transmission applications. The CTU generates signals compatible with either switched telephone networks or packet switched data networks. This makes it ideally suited for a wide range of telecommunications applications, including:

DTMF Dialing
Dial Pulse (DP) Signaling
Modems (0-600 baud)
UARTs
Keyboard Scan

Central to all CTU microcomputer operations is the GTE Microcircuits' G65SC00 8-bit microprocessor, complete with 2K bytes of ROM, 64 bytes of RAM, and an internal bus for interconnecting all microcomputer functions. Address and data bus buffers are included to allow convenient expansion of ROM, RAM and memory mapped I/O. This feature allows the design engineer to take advantage of the microprocessor's full 65K addressing space. Internal telecommunications functions include a 16-bit Timer, an 8-bit Column/Transmit Counter, a 16-bit Row/Receive Counter, and a Dual 26-Step Sine Wave Generator. There are also 27 Peripheral I/O Lines for use with keyboard, telephone Dial Pulse (DP) signaling, telephone line control, or for interfacing a variety of peripheral devices. In addition, the CTU Expansion Bus allows for external memory expansion.

The purpose of this Application Note is twofold... first to familiarize the design engineer with both hardware and software start-up procedures, and then to show the G65SC150 CTU in a typical Bell 103, 300 baud modem application. The discussion on start-up procedures includes Power Modes, Oscillator Requirements, Reset Options, using the Expansion Bus and Peripheral I/O Lines, memory expansion and mapping, and other subjects which may assist the user in developing his CTU application. The software section includes both discussions and listings (Appendix A). The program listings represent an Application Engineering Test Program to assist the system engineer in not only the development of application programs, but to achieve a better understanding of the CTU operation. The program contains many general purpose as well as modem-specific software routines which represent a variety of specific control or data handling functions, including: Reset Initialization, Page Zero Data Assignment, Clock Update, UART Parallel and Serial Data Conversion, and Modem Initialization... to name but a few.

To further assist the user in developing his CTU application, Appendix B provides a brief description of the GTE G65DS-150 Evaluation Board and its many advantages during CTU system prototype development and debugging, as well as during software development. A logic diagram and parts list has been included for those who may wish to develop their own CTU emulation system.

Please note that all topics within this Application Note assume the reader is familiar with or has access to the G65SCXX 8-Bit Microprocessor and G65SC150 CTU data sheets. It is intended that these data sheets be used in conjunction with the following CTU discussions. Should you have questions or require additional literature, please feel free to call your nearest GTE Microcircuits representative.

Getting Started

The G65SC150 CTU offers the design engineer a variety of options and modes from which to choose during the development of a CTU application. The following paragraphs and diagrams are included to assist the design engineer during the selection and implementation of these functions.

Oscillator Requirements

The G65SC150 CTU may be operated using its own internal oscillator or from an externally generated timing source.

Internal Oscillator—When using the internal CTU oscillator circuitry, an externally connected crystal is required. To assist in the specification and selection of this crystal, a diagram of the internal oscillator circuit is shown in Figure 1, followed by recommended crystal specifications and available manufacturers in Table 1. The CTU's internal oscillator circuit consists of three series-connected CMOS inverters which form a high-gain inverting amplifier. The crystal oscillator is formed by connecting a series resonant crystal between pin 62 ($\overline{OSC}$(OUT)) and pin 63 (CLK(IN)). Although a series resonant crystal should be specified, a parallel resonant crystal may be used. The parallel resonant crystal will function satisfactorily in a series resonant circuit, but at a slightly shifted frequency.

NOTE—Once the crystal has been selected, the "in-circuit" drive level of the crystal must be checked to ensure that overshoot above V_{DD} or below V_{SS} does not occur.

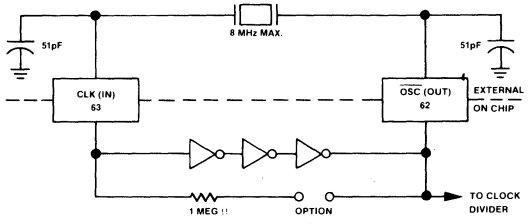
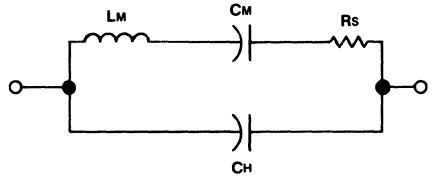


Figure 1. CTU Internal Oscillator Circuit

Table 1. Recommended Crystal Specifications

Crystal Equivalent Circuit



Recommended Crystal Specification

Frequency : 8.0 MHz MAX ±0.02%
Rs : ≤ 100 Ω
LM : 96 mHy
CM : 0.02 μF
CH : 5pF

Crystal Manufacturers

CRYSTEK
1000 Crystal Drive
Fort Myers, FL 33901
813-936-2109

UNITED STATES CRYSTAL CORP
3605 McCart St.
Fort Worth, TX 76110
817-921-3014

CTS KNIGHTS, INC.
400 Reimann Av
Sandwich, IL 60548
815-786-8411

External Timing—When external timing is to be used, the external timing source should be connected to pin 63 CLK (IN). Pin 62 may be left open or may be used as an inverted oscillator output. Note that a gated external timing source is required when the CTU Standby Mode is to be used (See discussion on Standby Mode).

A timing mask option provides a 1 Megohm feedback resistor between the CLK (IN) and $\overline{OSC}$ (OUT) pins. Alternatively, an external 1 Megohm resistor must be used if the mask option is not specified. This resistor biases the internal oscillator in the linear region and is required when an external crystal is used as a timing source for the internal oscillator. When an external clock is used, the resistor may be omitted to reduce power consumption.

Reset Considerations (Internal vs. External ROM)

Internal ROM—When the CTU's internal 2K byte ROM is to be used, system reset is accomplished by a simple external R-C circuit as shown in Figure 2. A Reset mask option provides a 200 Kohm pull-up resistor at the $\overline{RES}$ pin. Reset timing requires that Bus Enable (BE) (pin 64) remain high during the positive transition of the Reset signal (pin 68) as generated by the R-C network. After this positive transition, the internal processor will access the Reset Vector from ROM locations $FFFC and $FFFD. Note that the starting address stored at these locations must also be located within the internal ROM address space. Also, the internal firmware must always set the Control Register TSC (Three State Control) bit prior to accessing external memory or other devices via the Expansion Bus.

External ROM (Test & Prototype Mode)—During hardware and software development, the Test and Prototype Mode provides a convenient means for system testing and debugging without the need for mask-programmed ROM or other special emulation versions of ROM. The Test and Prototype Mode can also be used in the final application when using the G65SC151 "ROMless" CTU. The Test and Prototype Mode enables the use of external memory at the address locations normally occupied by internal ROM ($F800 through $FFFF), with internal ROM being disabled. In this mode, the software engineer can develop his program using external memory for the prototype system. The program can be developed using the same memory locations as reserved for internal ROM. Once the program has been debugged and tested, it can then be committed to internal ROM.

The Test and Prototype Mode is initiated during the Reset sequence by holding Bus Enable (BE) low while bringing Reset high. Figure 3 shows two examples of a Test and Prototype Mode External Reset Circuit, while Figure 4 shows the correct Bus Enable (BE) timing when placing the CTU in the Test and Prototype Mode. Note that BE must remain low for at least one clock cycle after $\overline{RES}$ becomes high. Also, BE must be high before the beginning of the first Vector Read cycle.

During the Reset sequence, the Reset Vector will be accessed from external memory locations $FFFC and $FFFD. Note that the Control Register TSC bit has no effect in the Test and Prototype Mode. Also, in this mode the PD1 I/O line is assigned an additional function and becomes PD1/EXTR. An active high input on this I/O pin selects external memory when in the Test and Prototype Mode. After Reset, this pin will be in the high state. A low level at this input disables external memory and places internal ROM back into the memory map.

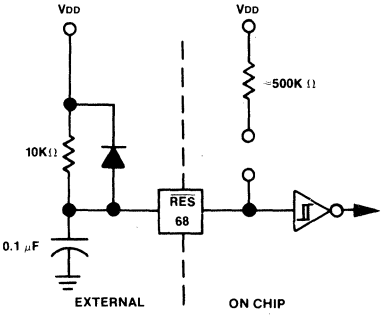


Figure 2. Reset Circuit, Internal ROM

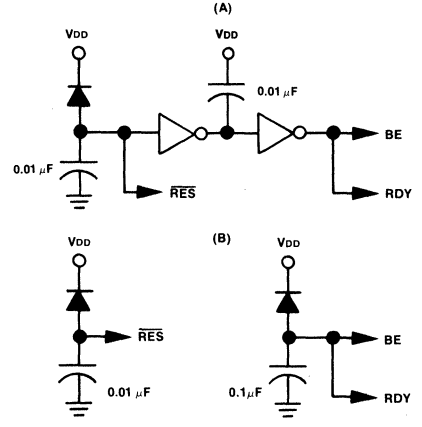


Figure 3. Reset Circuits for Test and Prototype Mode

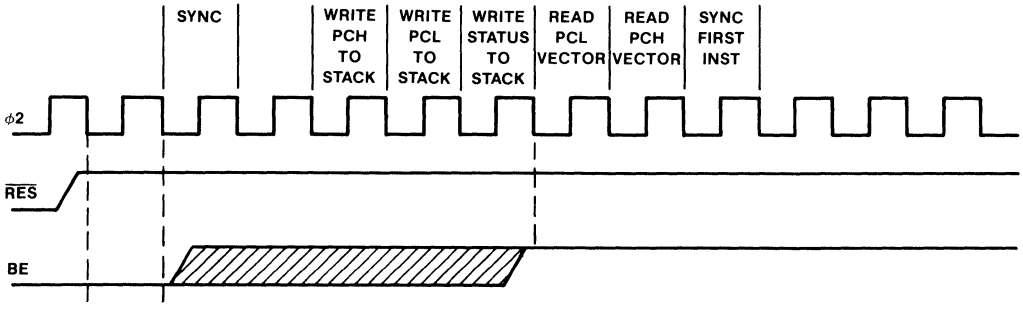


Figure 4. Bus Enable Timing for Test and Prototype Mode

Expansion Bus

When configuring a CTU system, additional memory (ROM or RAM) may be added by using the address (A0-A15), data (D0-D7), and control signals (R/$\overline{W}$, ϕ2 (OUT), ϕ4 (OUT)) provided at the CTU Expansion Bus. Figure 5 shows the CTU memory map addressing assignments. Note that the Control Register TSC bit must be set for the Expansion Bus to be active.

When in the Test and Prototype Mode, I/O signal PD1 becomes PD1/EXTR and is used to switch between internal ROM and external memory. A high level on this pin selects external memory. By holding PD1/EXTR low, internal ROM is switched back into the memory map. Note that this pin has no direct effect on the CPU operation. When addressing memory in the range $F800 through $FFFF, external memory is addressed in both cases. Data going to the CPU is switched between the external and internal buses. In systems where both internal and external program memory is used, the internal ROM will generally contain tables or routines that do not change. In this case, data which is subject to change or revision will be assigned to external memory. Systems using two or more CTUs will find the switchable memory feature a major advantage. As an example, in a PBX application, the program for the telephone set or line card can be entirely within the internal ROM. In this way, the same part can be used in the main control processor while the larger program is located in external EPROM.

It should also be noted that additional external memory can be "overlaid" in the Stack and Page Zero areas without affecting the I/O ports and Timer. In this case, internal RAM will continue to be "mirrored" in both pages, but the two 192-byte data segments will be independent. As an example, a 2K X 8 CMOS RAM can be accessed within the memory range $0000 through $0800. Furthermore, all of Page One can be used for Stack operations, while memory locations $0000 through $00BF are available for Page Zero. There is no bus contention problems associated with this arrangement.

Peripheral I/O Lines

The CTU's 27 Peripheral I/O Lines (as well as the ATG signal) are each independently mask programmed to one of four current sourcing options. The Design Engineer may assign each individual I/O line to be either input, output or bidirectional. Table 2 shows the available mask options for each of these lines. Reading the I/O ports accesses the state of the pin, not the output latch.

CTU Power Modes

Normal Power Mode—In the Normal Power Mode all CTU functions are available to the application. Note that switching between power modes may be accomplished under program control.

Low Power Mode—This mode is available for those applications which require operation at reduced power levels. Typical applications include:

- Systems operating from battery or telephone line power.
- Systems requiring fail-safe operation in the event of AC power loss.

Table 2. CTU Interface Current Source Options

OPTION	MIN I_{IH} @ 2.4V	MAX I_{IL} @ 0.4V	MIN I_{OH} @ 1.5V	COMMENT
A	0	—	—	WIRE-OR
B	-10 μA	-100 μA	—	KEYBOARD
C	-200 μA	-2.4 mA	—	TTL
D	—	—	3.0 mA	OUTPUT DRIVER

Source Current @ V_{DD} = 5.0V ± 10%

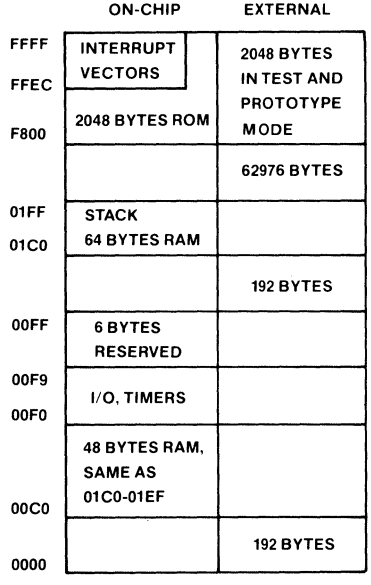


Figure 5. CTU Memory Map—Internal/External

When using the Low Power Mode and operating from the internal oscillator, the CTU operates at reduced speed using the 16-bit Timer to reduce the microprocessor clock rate, with the timer serving as a programmable clock divider. When operating from an external timing source, the Low Power Mode may be accomplished by using the 16-bit Timer as explained above or by reducing the external clock rate into the CTU. In either case, the CTU is capable of switching between power modes under program control; however, the CTU should not be switched from Low Power to Normal Power unless full power (V_{DD}) is available to the CTU.

In a typical fail-safe application, for example, the $\overline{NMI}$ Interrupt could be used to indicate the loss of AC power. Upon receiving the interrupt, the CTU would be switched to battery backup or telephone line power, depending on the application. The CTU will then shut down the system in an orderly manner...storing all critical values in internal RAM. At this point, the microprocessor continues to operate from the backup power source, but at a reduced clock rate, and at a resulting decrease in power requirements. The microprocessor clock rate was reduced by setting the Phase 2 Mode bit in the Control Register. To further reduce power, the CTU Expansion Bus may be disabled by clearing the TSC bit in the Control Register. When full power is restored, the CTU may be switched back to the Normal Power Mode with full operating capability. This again would be accomplished by monitoring the $\overline{NMI}$ bit in the Control Register. In this case, clearing of the $\overline{NMI}$ bit would indicate AC power had been restored.

Figure 6 is a sample program segment for executing the CTU Low Power Mode. In this sample, the clock rate is reduced to 10 KHz and the Expansion Bus will be disabled. Once in the Low Power Mode, the Control Register $\overline{NMI}$ bit will be monitored for return to Normal Power operation.

Standby Power Mode—During periods of system inactivity, the CTU may be placed in the Standby Mode to conserve power. In this mode, the CTU must be operated from an external clock source which can be gated "off" when the Standby Mode is selected (See Figure 7). In this case, the CTU firmware program sets the I/O PA0 bit to logic "zero", thus disabling the clock input until such time the Wake-Up signal becomes a logic "one". $\overline{RES}$ will restart the clock by setting PA0 to logic "one".

```
CONTROL  EQU  $F7          Status and Control Register
TIMER    EQU  $F8          Timer Register
TSC      EQU  $20          Bit 5 of Control Register
MODE     EQU  $08          Bit 3 of Control Register
           •
           •               (Save critical values here)
           •
         LDA  #98          Set Timer for 10 KHz Operation
         STA  TIMER
         STZ  TIMER + 1
         LDA  #MODE        Switch to Low Power mode
         TSB  CONTROL
         LDA  #TSC         Disable External Bus
         TRB  CONTROL
NOPWR    BIT  CONTROL      Is main power restored?
         BPL  PWRUP
           •
           •               (Low Power operating program)
           •
         JMP  NOPWR
PWRUP    LDA  #TSC         Enable External Bus
         TSB  CONTROL
         LDA  #MODE        Switch to MAXIMUM freq. mode
         TRB  CONTROL
           •
           •               (Restore critical values here)
           •
         RTI               Resume normal operation
```

Figure 6. Low Power Mode (NMI Power-Down Interrupt Routine)

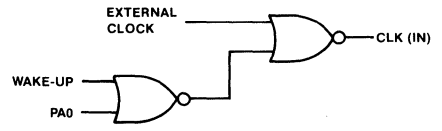


Figure 7. Standby Mode, External Clock Gating Circuit

Software—Application Engineering Test Program for the G65SC150 CTU

The following Application Engineering Test Program is included to assist the system engineer in not only the development of application programs, but also to achieve a better understanding of CTU operation as related to its various potential applications. This particular test program has been written for CTU evaluation as applied to Bell 103 modem applications. Included in the program listings are routines for Pulse and DTMF Dialing, Real-Time Clock, Asynchronous Serial Data Transmit and Receive, and Modem Transmit and Receive. The test program has been designed to test the CTU modem application capabilities by transmitting and receiving a message in a loopback configuration. The transmit message is looped back to the input and verified as a receive message. An error is indicated if data verification is incorrect. Bell 103 modem standards are used with a 300 baud signaling rate. Note that the G65SC150 CTU should be configured for 8 MHz operation. Individual program listings are contained in Appendix A.

Program Definitions and Initialization

CTU Internal Register Address (CTUDEF) (Listing A-1)—This data area establishes labels for the CTU I/O ports, Timers and Control Register.

Page Zero Data Assignment (PAGEZERO) (Listing A-2)—This data assignment is used to establish memory Page Zero address locations for variables used in the various program subroutines. Note that these assignments relate to the Bell 103 modem application.

Reset Initialization Routine (CTUINZ) (Listing A-3)—This routine serves to initialize CTU internal I/O registers. Any previous interrupts are cleared and the interrupt mask bit in the CPU Control Register is cleared, thus allowing subsequent interrupts to be recognized.

G65SC150 CTU Application Engineering Test Program (Listing A-4)

The Application Engineering Test Program is designed to test the Bell 103 modem application by transmitting and receiving serial data in a loopback configuration. Bell 103 modem standards are used with a 300 baud data transfer rate and the CTU configured for 8 MHz operation. Data transfer and the various modem subroutines are exercised by transmitting a character through the TXC/DTMF analog output and routing the character back to the RXC input. The transmitted and received characters are compared and the routine stops if there is an error. Also included within this program is a Timer Interrupt routine which handles the modem transmit, clock, and serial I/O functions. Note that this program may also be used as a "power on" modem operational test within the application software.

The following subroutines are called by the Engineering Test Program and the Timer Interrupt routine for the purpose of implementing the modem functions.

Real-Time Clock

Initialization Subroutine (CLKINZ) (Listing A-5)—This subroutine serves to initialize the CTU Timer for modem, DTMF and real-time clock routines. It also enables the Timer Interrupt. The Timer is set to interrupt at the transmit bit rate (3.33 mS).

Clock Update Subroutine (CLOCK) (Listing A-6—) This subroutine increments a counter which provides a 50 mS clock. A flag is set at 50 mS intervals to facilitate the addition of other real-time routines. The Clock Update Subroutine is called by the Timer Interrupt routine.

Parallel-To-Serial, Serial-To-Parallel Conversion

Initialization Subroutine (URTINZ) (Listing A-7)—This subroutine initializes both parallel-to-serial and serial-to-parallel data conversion for asynchronous serial data transmit and receive applications.

Asynchronous Serial Data Transmit Subroutine (CNVPS) (Listing A-8)—This subroutine provides parallel-to-serial data conversion for the modem transmit function and is called by the Timer Interrupt routine.

Asynchronous Serial Data Receive Subroutine (CNVSP) (Listing A-9)—This subroutine provides serial-to-parallel data conversion for the modem receive function. This subroutine is called by the Timer Interrupt routine.

Modem Routines

Bell 103 Standard Constants for Modem Transmit and Receive (MDMCON) (Listing A-10)—This listing establishes Bell 103 standard program constants for modem transmit and receive functions.

Modem Initialization Subroutine (MDMINZ) (Listing A-11)—This subroutine serves to initialize the modem receive buffer pointer.

Modem Bit Transmit Subroutine (TXMODM) (Listing A-12)—This subroutine is called by the Timer Interrupt servicing routine. It is used to transmit a bit from the modem by providing a frequency update at the CTU's TXC/DTMF output pin.

Row/Receive Interrupt Service Routine (RRCI) (Listing A-13)— This routine performs interrupt service for the CTU's Row/Receive Counter. It provides demodulation of the modem receive carrier as received at the CTU's RXC input pin.

DTMF and Pulse Dialing

Although these routines are not exercised by the modem test program, they can be inserted in a system application program to provide Pulse and/or DTMF Dialing.

Initialization Routine (DLINZ) (Listing A-14)—This routine clears the Row/Receive and Column/Transmit Counters to ensure no tones are generated when the DTMF mode is activated. Memory locations used by the Dialing routine (Listing A-15) are also cleared.

Interrupt Service Routine for Pulse and DTMF Dialing (DIAL) (Listing A-15)—This routine should be called at 50 mS intervals by the Real-Time Clock routine. A memory flag determines whether Pulse or DTMF dialing is used. DTMF tones are generated at the TXC/DTMF output by loading the Row/Receive and Column/Transmit Counters. Pulse dialing is accomplished by toggling the ON HOOK signal at I/O pin PB5.

Interrupt Vectors (VECTOR) (Listing A-16)

This data area provides the starting addresses for each interrupt service routine.

Program Global Symbol Table (Listing A-17)

This table is generated by the assembler and lists the value of each global symbol defined by the program.

Bell 103 Asynchronous Modem Applications for the G65SC150 CTU

The availability of low-cost microprocessor-based computer systems has created an increasing demand for data communications systems which operate by way of the dial-up telephone network...that is, the asynchronous Modem! For this application, the generally accepted standard for low-speed data communication has become the Bell 103 type modem, which uses Frequency Shift Keying (FSK) for transferring asynchronous binary data at speeds up to 300 baud. Frequency Shift Keying is simply a method for encoding digital data (logic ones and zeros) for transmission over telephone lines. As an example, for a logic one the modem transmits a specified frequency and for a logic zero the modem transmits a slightly different frequency. This type modem is well suited to computer-to-computer data communication. Not only does it have excellent reliability, but it is capable of providing full duplex transmission over voice grade, unconditioned telephones lines... and at extremely low error rates. Full duplex transmission actually employs four specified frequencies, that is, a logic one and zero frequency for "receive" and logic one and zero frequency for "transmit". In Bell 103 modem applications, the high frequency of the pair is referred to as a "mark" and the low frequency as a "space". These frequencies are specified by Bell 103 standards. Since communicating modems must never transmit or receive over the same band, a simple protocol must be followed. In this way, the calling (Originate) modem will normally transmit on the low band (1270 Hz for a one bit, and 1070 Hz for a zero bit) and receive on the high band (2225 Hz for a one bit, and 2025 Hz for a zero bit), while the called (Answer) modem transmits on the high band and receives on the low band.

GTE Microcircuits' G65SC150 CTU is ideally suited for a variety of low-cost modem applications, providing a design flexibility not normally found in single-chip modem configurations. In most modem applications, the modem function is accompanied by a single-chip microcomputer which provides the intelligence for off-loading the host computer system. In the G65SC150 CTU, GTE Microcircuits has incorporated a full 8-bit microprocessor which provides the necessary system intelligence, and at the same time, handles all the requirements of the modem. In most modem systems, the G65SC150 CTU is the only control element required, since its internal microprocessor and I/O can also handle keyboard scanning, display and call setup functions. In addition to the modem control, the CTU's internal dual sine wave generator performs both DTMF signal generation and the modem transmit carrier frequency, thus allowing full dial-up capabilities when coupled with pulse dialing via one of the 27 I/O ports.

The sine wave generation capabilities and the full bus access of the CTU allows the design engineer to configure systems with external EPROM for program modification without sacrificing any of the I/O capabilities of the device. This flexible bus structure allows the device to utilize external EPROM alone, internal masked ROM, or a combination of both.

In addition to dedicated applications, the G65SC150 CTU can also serve as a microprocessor-based intelligent peripheral control element to a "host" microcomputer system (See Figure 8). In this application, a single CTU chip is capable of providing intelligent control of LCD displays, ASCII keyboards and other peripheral functions, while at the same time providing the Bell 103 modem function as described in this Ap Note. When used as a peripheral device, the CTU memory is shared with the "host" microcomputer system, thus allowing the "host" system to modify and update the internal CTU memory. In turn, the CTU performs intelligent peripheral control in response to the updated memory contents.

In representing a typical modem application, the following paragraphs describe the G65SC150 CTU as used in a Bell 103, 300 Baud Intelligent Modem. A typical Block Diagram is shown in Figure 9, while Figure 10 presents the circuit diagram for a Bell 103 Intelligent modem with Auto-Answer, Ring Detection, Auto-Dialing, DTMF Dialing and Pulse Dialing. In configuring this modem, an FSK XR-2103 Modem Filter has been selected. The FSK filter is a switched-capacitor type filter, capable of performing both transmit and receive signal filtering as required by the

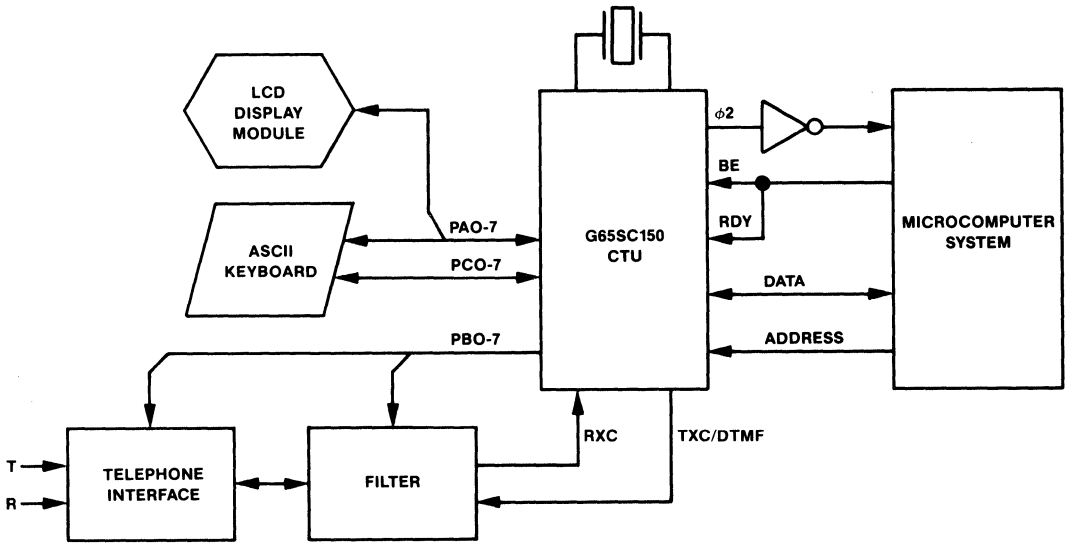


Figure 8. Intelligent Peripheral Control of Modem, Keyboard and Display

Bell 103 standards. Local communication with the CTU assumes the RS-232C interface.

The FSK Modem Filter (Exar XR2103)

The FSK modem filter is a switched-capacitor type with high and low bandpass filters, input/output multiplexers, duplexer, and a carrier detect circuit. The six-pole high and low bandpass filters provide precise bandpass filtering of both the receive and transmit carriers. The input/output multiplexer is used to route transmit and receive signals to the proper filter and signal output according to the CTU-selected operating mode (Originate, Answer, or Self-Test). The duplexer op amp serves as a two-to-four-wire converter which splits the phone line signal into transmit and receive components.

XIN (Filter Clock) Signal—The CTU $\phi 2$ (OUT) clock signal serves as the clock input to the modem filter. With an 8 MHz crystal, $\phi 2$ (OUT) runs at 2 MHz. The $\phi 2$ (OUT) clock is run through a D-Type flip-flop to provide the desired 1 MHz clock frequency input to the modem filter.

TXC/DTMF Signal—This CTU analog output signal provides the two DTMF tones when dialing and the modem transmit carrier when sending data. The TXC/DTMF pin is directly connected to TXIN of the modem filter. The CD4066 analog switch connects this signal to the phone interface when dialing with DTMF tones.

RXC Signal—The RXC Receive Carrier output signal from the modem filter is a square wave (approx. 50 percent duty cycle) with a frequency equal to the carrier received from the remote modem. The CTU is configured such that transitions on the RXC input will result in CPU interrupts. The interrupt servicing routine demodulates the receive carrier by detecting a "mark" or "space" frequency. The mark or space is detected by monitoring the difference between the RXC signal zero crossing times.

CARRIER DETECT (PB0) Signal—The modem filter generates a CARRIER DETECT signal when a receive carrier is detected. The signal is then used by the CTU modem software to determine whether valid data is being received at the RXC CTU input.

ORIGINATE/ANSWER (PB1) Signal—The ORIGINATE/ANSWER signal is generated by the modem firmware and sent to the FSK filter for selecting the high band (2025 Hz and 2225 Hz) and low band (1070 Hz and 1270 Hz) filters for transmit and receive operation. Band selection is as follows:

PB1	MODE	Tx	Rx
1	ORIGINATE	low	high
0	ANSWER	high	low

SELF-TEST (PB2) Signal—This input signal to the modem filter, when high, activates an analog loopback mode within the filter. In the Self-Test mode, the transmit carrier is routed through the proper filter and back through the receive limiter for transmit carrier verification. The CTU software Test Program activates the modem filter Self-Test mode as a verification of the CTU modem system.

The Telephone Line Interface Module (Cermetek CH1812)

The Direct Connect Protective Hybrid (DCPH) Telephone Line Interface Module (CH1812) provides the necessary circuit elements for Ring Detection and Hook Switch status, as well as line surge protection and signal coupling to the FSK filter. As shown in Figure 10, the CH1812 Telephone Line Interface Module combines with minimal external circuitry to form an FCC registrable telephone line interface.

Line Coupler—Surge protection circuitry and the coupling transformer both conform to all FCC Part 68 specifications for surge, hazardous voltage and leakage requirements at the RING and TIP telephone line connections. The LINE (+), LINE (-) and CT (Center Tap) signals all connect to the secondary side of the coupling transformer. The 390 ohm matching resistor assures a 600 ohm telephone line impedance match.

ON HOOK (PB5) Signal—The ON HOOK signal is used to initiate the modem handshake procedure in both the Answer and Originate modes. When the CTU brings this signal high, a relay within the Interface Module will "seize" the telephone line by allowing DC loop current to flow between the RING and TIP lines. This completed current flow path notifies the telephone company central office that this line is either originating or an-

swering a call. The general purpose 2N2222 transistor provides the necessary current drive for the relay coil. Note that the ON HOOK signal is also used during Pulse Dialing to interrupt the loop current at a specified 10 pps rate.

RING INDICATOR (PB4) Signal—Typically, an AC signal of 90 volts peak-to-peak and 20 Hz appears across the RING and TIP lines when ringing occurs. An optocoupler within the Interface Module is activated by this signal. This allows an NPN phototransistor to be turned on by an LED during part of each half cycle of the ringing waveform. The emitter (RI(-)) of this transistor is grounded, the base (BAL) is stabilized with a capacitor to ground, and the collector (RI(+)) is connected to PB4 of the CTU. A call setup software routine (not listed here) is used to detect the ringing signal. Although the Ring Detect circuit will not respond to audio signals on the line, it can sometimes be activated by pulse dialing and other switching transients. For this reason, when polling PB5 for a ring signal, it is important that the modem firmware detect that the signal is present for a minimum duration...normally one second for a ring ON interval.

Modem or DTMF Select Circuit

DTMF/MODEM (PB3) Signal—The DTMF/MODEM signal is set to the low state for modem operation. A CD4066 Quad Bidirectional Switch serves to connect the TXC/DTMF analog CTU output to the modem filter for the purpose of sending the transmit carrier signal. When the DTMF/MODEM signal is changed to the high state, the TXC/DTMF signal bypasses the modem filter and is sent directly to the telephone line interface.

RS-232C Interface

The RS-232C interface provides serial communication with a host computer, terminal or other information processing system. The MC1488 Line Driver and MC1489 Line Receiver are used to provide the voltage levels necessary to comply with the RS-232C serial interface standard. Note that the same Serial I/O subroutines used in the modem application can be used with the RS-232C interface.

TXD (PA0) Signal—This Transmit Data signal is the serialized data output signal as received from the modem and sent to the remote terminal device.

RTS (PA1) Signal—This is the Request to Send handshake signal. It informs the remote terminal that the modem is ready to receive data on the RXD line.

RXD (PA2) Signal—This is the serialized Receive Data input signal as received from the remote terminal and sent to the modem.

CTS (PA3) Signal—This is the Clear to Send handshake signal. It informs the modem that the remote terminal is ready to receive data over the modem TXD line.

Theory of Operation

Answer Mode

When receiving an incoming call, the ring voltage across telephone lines L1 and L2 activates the Ring Detect circuit. If the modem is enabled to receive incoming calls (Auto-Answer mode), a polling sequence within the modem firmware will detect the ring signal at I/O line PB5. On detecting the ring signal, the FSK filter is switched to the Answer mode by placing a low level on the Originate/Answer line (PB1). At this point, a Hook Switch signal is generated (high level) on I/O line PB4, activating the hook switch circuit within the telephone line interface module. This results in a DC current path between telephone lines L1 and L2, thus notifying the telephone company central office that a call is being answered. The received audio signal passes through a coupling transformer within the interface module and is applied to the duplexer input at the FSK filter. At this point, CTU modem firmware enables the TXC/DTMF output and transmits a high band "mark" tone (2225 Hz) to indicate acknowledgement of the call. The "calling" modem then transmits a low band "mark" tone (1270 Hz) in response, resulting in a Carrier Detect output (low level) from the FSK filter circuit on I/O Bus PB0. Once the Carrier Detect signal is received, full duplex data transfer can begin.

Originate Mode

The originate mode is used by the modem originating the data transfer. To originate a call, the ON HOOK signal (PB5) is changed to a high level. This activates a relay within the Telephone Line Interface Module, allowing DC current to flow between the TIP and RING lines. This current path results in a dial tone being returned by the telephone company central office. At this point, the telephone number is dialed by either Pulse Dialing through the ON HOOK signal, or DTMF Dialing (tone dialing) by setting DTMF/MODEM high and generating tones at the TXC/DTMF output. The CTU then switches the modem filter to the Originate mode by setting PB1 high. If the call is successful, a high-band modem carrier signal will be received from the answering device and the CARRIER DETECT signal will go low. If the call is unsuccessful, the call will be cancelled by ON HOOK going low. The CTU modem firmware responds to the high-band receive carrier by sending a low-band transmit carrier on the TXC/DTMF output line. At this point, full duplex data transfers can begin.

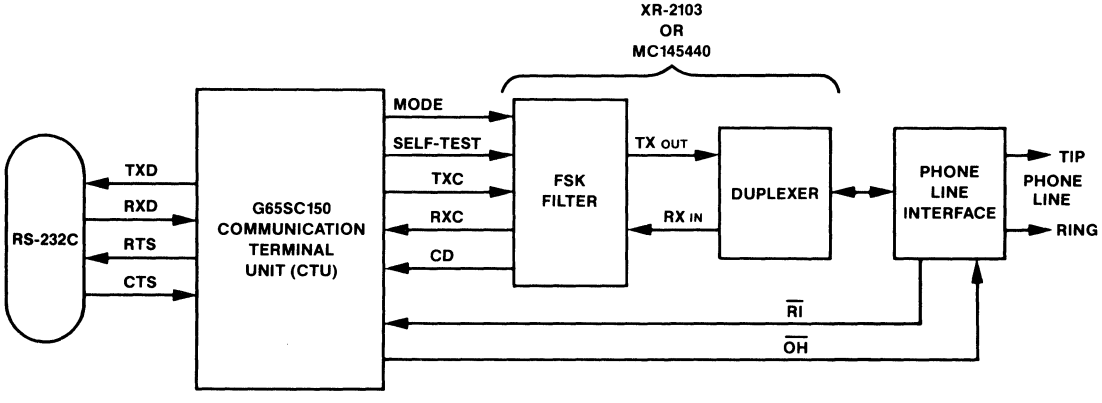


Figure 9. Bell 103, 300 Baud Intelligent Modem

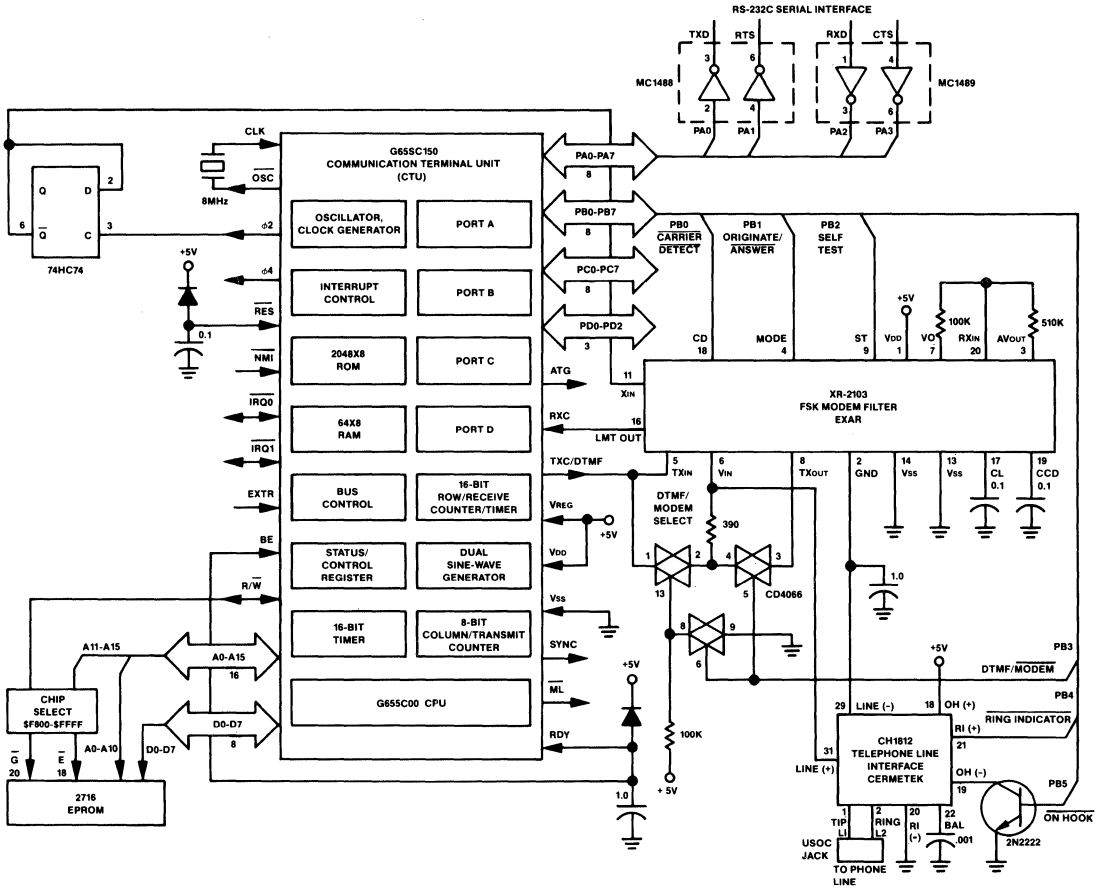


Figure 10. Bell 103, 300 Baud Modem, With Pulse Dialing, DTMF Dialing, Ring Detect, Auto Answer and Auto Dialing

Appendix A—Software Routine Listings

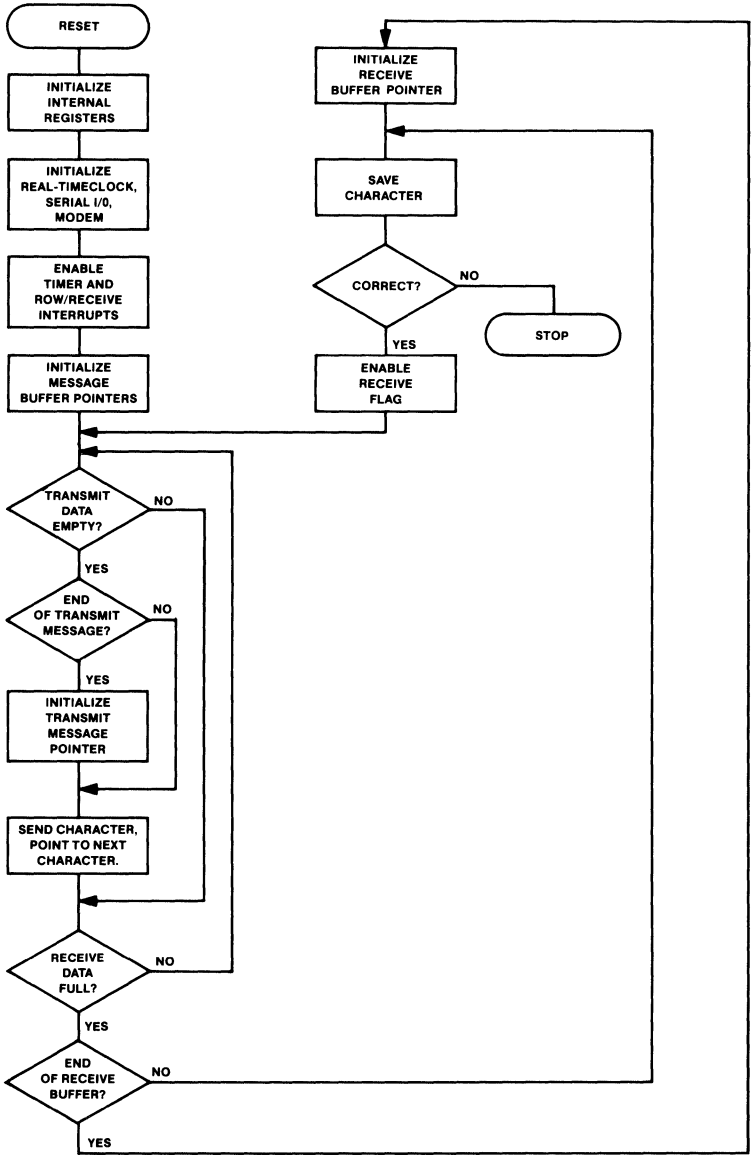


Figure A-1. Flow Chart, Modem Test Program

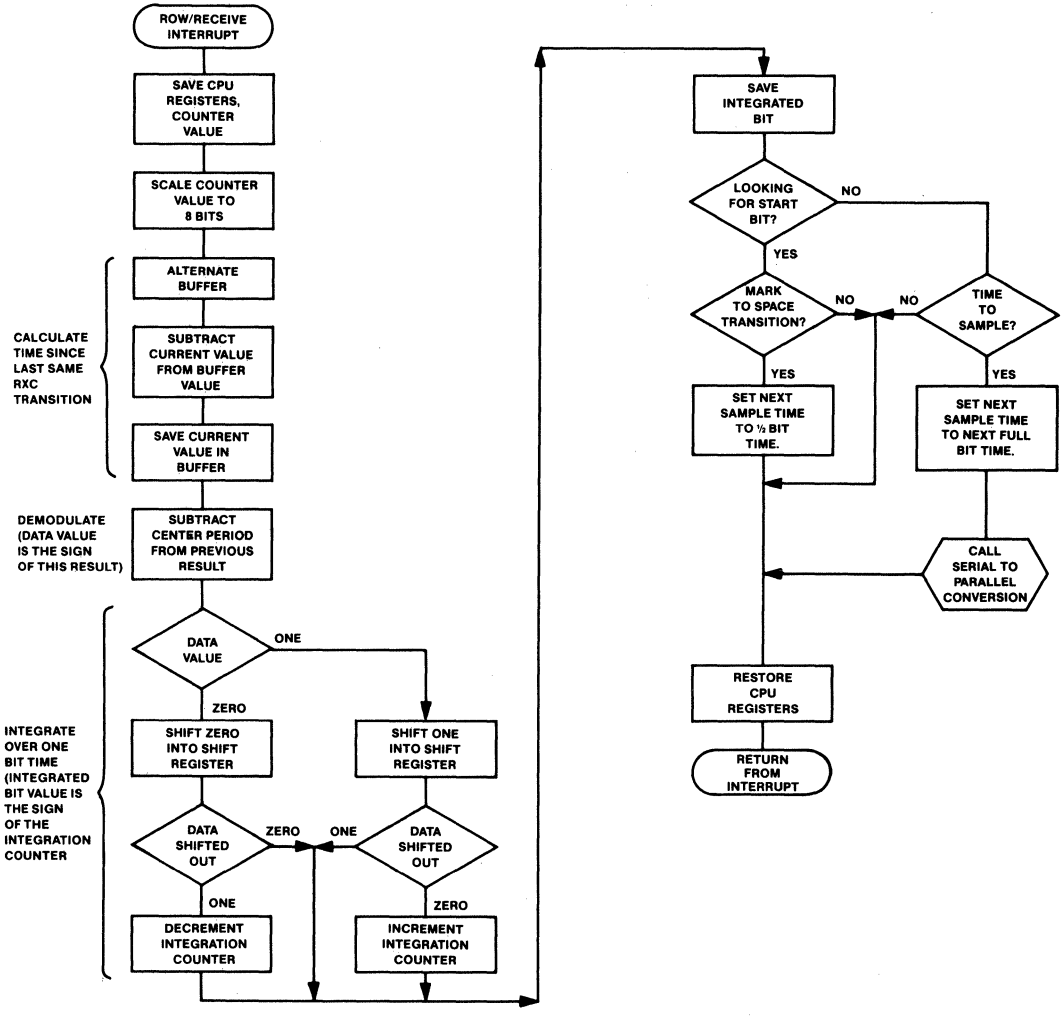


Figure A-2. Flow Chart, Modem Receive Routine

Program Definitions and Initialization

Listing A-1. CTU Internal Register Address (CTUDEF)

```
ORCA/M Assembler 3.5

0000            * FILE: TEST
0000            ************************************************************
0000            *                                                          *
0000            *       GTÉ MICROCIRCUITS                                  *
0000            *                                                          *
0000            *       2000 West Fourteenth Street                        *
0000            *       Tempe, Arizona  85281                              *
0000            *                                                          *
0000            *              G65SC150-CTU APPLICATION EXAMPLE            *
0000            *                                                          *
0000            *    GTE G65SC150-CTU App Note. 300 Baud Type 103 Modem    *
0000            *                                                          *
0000            *  This program tests the modem capabilities of the        *
0000            *  G65SC150 by sending and receiving serial data in        *
0000            *  a loopback configuration.  The Bell 103 modem           *
0000            *  standard is used, with a 300 baud signaling rate.       *
0000            *  The G65SC150 is configured for an 8 MHz oscillator      *
0000            *  and 2 MHz system clock.                                 *
0000            *                                                          *
0000            *       The assembler is ORCA/M, version 3.5               *
0000            *                                                          *
0000            ************************************************************
0000
0000                    KEEP  TESTOBJ,V10       Object file
0000
0000                    SYMBL OFF       Don't print local symbols
0000
0000                    65C02 ON        Enable enhanced instruction set
0000
0000            ORG     DATA            Set program starting address
0000
0000                    ORG   $F800     Beginning of G65SC150 ROM
0000


0000            * Program files
0000                    COPY  CTUDEF,V10        Define CTU registers
0000            * FILE: CTUDEF
0000            ************************************************************
0000            *                                                          *
0000            *  DEFINITION OF G65SC150 INTERNAL REGISTER ADDRESSES      *
0000            *                                                          *
0000            *       Connections between the CTU I/O ports and the      *
0000            *  RS-232 interface, filter, analog switch, and            *
0000            *  telephone interface are defined.                        *
0000            *                                                          *
0000            ************************************************************
0000
0000            CTUDEF DATA
0000
0000            PA      GEQU  $F0       I/O PORT A (8 BITS)
0000            *                       RS 232 INTERFACE
0000            *                       PA0 = TXD  (OUT)
0000            *                       PA1 = RTS  (OUT)
0000            *                       PA2 = RXD  (IN)
0000            *                       PA3 = CTS  (IN)
0000
0000            PB      GEQU  $F1       I/O PORT B (8 BITS)
0000            *                       FILTER
0000            *                       PB0 = CARRIER DETECT  (0 = CARRIER)
0000            *                       PB1 = ORIGINATE/ANSWER(1 = ORIGINATE)
0000            *                       PB2 = SELF TEST  (1 = SELF TEST)
0000            *                       ANALOG SWITCH
0000            *                       PB3 = DTMF/MODEM  (1 = DTMF)
0000            *                       TELEPHONE INTERFACE
0000            *                       PB4 = RING INDICATOR  (0 = RING)
0000            *                       PB5 = ON HOOK  (0 = ON HOOK (OPEN))
0000
0000            PC      GEQU  $F2       I/O PORT C (8 BITS)
0000            PD      GEQU  $F3       I/O PORT D (3 BITS, PD0, PD1, PD2)
0000
0000            RRC     GEQU  $F4       ROW/RECEIVE REGISTER (2 BYTES)
0000            CTC     GEQU  $F6       COLUMN/TRANSMIT REGISTER (1 BYTE)
0000            CSR     GEQU  $F7       CONTROL/STATUS REGISTER (1 BYTE)
0000            TIMER   GEQU  $F8       TIMER REGISTER (2 BYTES)
0000
```

Listing A-2. Page Zero Data Assignment (PAGEZERO)

```
0000                    COPY  PAGEZERO,V10     Page zero allocation
0000                  * FILE: PAGEZERO
0000                  ************************************************************
0000                  *                                                          *
0000                  * PAGE ZERO DATA ASSIGNMENT                                *
0000                  *                                                          *
0000                  *    This data area establishes locations in memory      *
0000                  * page zero for variables used in each subroutine.        *
0000                  *                                                          *
0000                  ************************************************************
0000
0000                  PAGEZERO      DATA
0000
0000                  * COPY OF G65SC150 I/O REGISTERS
0000                  CPA     GEQU  $C0       PORT A
0000                  CPB     GEQU  $C1       PORT B
0000                  CPC     GEQU  $C2       PORT C
0000                  CPD     GEQU  $C3       PORT D
0000                  CRRC    GEQU  $C4       ROW/RCV (TWO BYTES)
0000                  CCTC    GEQU  $C6       COL/XMIT
0000                  CCSR    GEQU  $C7       CTRL/STATUS
0000                  CTIMER  GEQU  $C8       TIMER (TWO BYTES)
0000
0000                  * MODEM
0000                  BUFPTR  GEQU  $CC       INDEX TO BUFFER
0000                  *                       FOR LAST ROW/RCV VALUE
0000                  NXTBIT  GEQU  $CD       NEXT BIT TIME
0000                  INTBIT  GEQU  $CE       BIT VALUE INTEGRATED
0000                  *                       OVER ONE BIT TIME
0000                  RXCB    GEQU  $CF       BUFFER FOR LAST
0000                  *                       ROW/RCV VALUE (TWO BYTES)
0000                  ANSORG  GEQU  $D1       ANSWER, ORIGINATE
0000                  *                       MODEM RECEIVE REQUIRES:
0000                  *                       0 = ANSWER
0000                  *                       1 = ORIGINATE
0000                  SLFTST  GEQU  $D2       SELF TEST
0000                  SR      GEQU  $D3       RECEIVE SHIFT REGISTER
0000                  *                       (TWO BYTES)
0000
0000                  * CLOCK
0000                  CLKREG  GEQU  $D5       50 mS Counter
0000
0000                  * UART
0000                  PSFLG   GEQU  $D6
0000                  PSDAT   GEQU  $D7
0000                  SEROUT  GEQU  $D8
0000                  SERIN   GEQU  $D9
0000                  SPFLG   GEQU  $DA
0000                  SPDAT   GEQU  $DB
0000
```

Listing A-3. Reset Initialization Routine (CTUINZ)

```
0000                    COPY  CTUINZ,V10      Reset initialization
0000                  * FILE: CTUINZ
0000                  ************************************************************
0000                  *                                                          *
0000                  * CTUINZ - Initialize CTU internal I/O registers           *
0000                  *                                                          *
0000                  ************************************************************
0000
0000                  CTUINZ START
0000
0000                  * PROGRAM STARTS HERE *
0000
0000                  * INITIALIZE CPU INTERNAL REGISTERS
0000                  RESET   ENTRY           RESET VECTORS HERE
0000 78               RESET   SEI             SET INTERRUPT MASK FLAG
0001 D8               RESET   CLD             CLEAR DECIMAL FLAG
0002 A2FF             RESET   LDX   #$FF      INITIALIZE STACK POINTER
0004 9A               RESET   TXS
0005                  *
0005                  * INITIALIZE CTU REGISTERS
0005 A20A             RESET   LDX   #10               Move 10 bytes
0007
0007 BD1800           MOVE10  LDA   INZTAB-1,X        from table
000A 95EF             MOVE10  STA   PA-1,X            to registers
000C 95BF             MOVE10  STA   CPA-1,X           and shadows
000E CA               MOVE10  DEX
000F D0F6             MOVE10  BNE   MOVE10
0011
0011                  * CLEAR INTERNAL INTERRUPT SOURCES
0011 24F5             RESET   BIT   RRC+1     RESET INTERRUPT BY READING
0013 24F9             RESET   BIT   TIMER+1
0015                  *
0015                  * ALLOW INTERRUPTS
0015 58               RESET   CLI
0016                  *
0016                  * GO TO MAIN PROGRAM
0016 4C0080           RESET   JMP   MAIN
0019
0019
0019                  * INITIAL CTU REGISTER VALUES
0019 FF04FF           INZTAB DC     H'FF 04 FF FF 55 55 55 20 55 55'
0023
0023
```

Test Program

Listing A-4. G65SC150 CTU Application Engineering Test Program

```
0000                    COPY  MAIN,V10          Test program
0000                * FILE: MAIN
0000                ************************************************************
0000                *                                                          *
0000                *  MAIN - ENGINEERING TEST PROGRAM -                       *
0000                *                                                          *
0000                *     Exercises the serial and modem subroutines by        *
0000                * transmiting a character through the TXC/DTMF analog      *
0000                * output and receiving through the RXC input.  The         *
0000                * transmitted and received characters are compared         *
0000                * and the program stops if there is an error.              *
0000                *                                                          *
0000                ************************************************************
0000
0000                MAIN    START
0000
0000 200080                 JSR   CLKINZ  Initialize Real-Time clock
0003 200080                 JSR   URTINZ  Initialize UART
0006 200080                 JSR   MDMINZ  Initialize Modem
0009 A946                   LDA   #%01000110        Enable interrupts
000B 85F7                   STA   CSR
000D 9C9A00                 STZ   TXBUFP  Initialize transmit message pointer
0010 9CA500                 STZ   RXBUFP  Initialize receive message pointer
0013
0013 24D6           MAIN2   BIT   PSFLG   Transmit data empty?
0015 3016                   BMI   MAIN1
0017
0017 AE8A00                 LDX   TXBUFP  End of message?
001A E01A                   CPX   #TXEND-TXBUF
001C 9002                   BLT   MAIN3
001E
001E A200                   LDX   #$00    Set pointer back to beginning
0020
0020 BD7000         MAIN3   LDA   TXBUF,X Send character
0023 85D7                   STA   PSDAT
0025 E8                     INX           Point to next character
0026 8E8A00                 STX   TXBUFP
0029
0029 A980                   LDA   #%10000000  Set flag to start transmiting
002B 04D6                   TSB   PSFLG
002D
002D 24DA           MAIN1   BIT   SPFLG   Receive data full?
002F 10E2                   BPL   MAIN2
0031
0031 AEA500                 LDX   RXBUFP  End of buffer?
0034 E01A                   CPX   #RXEND-RXBUF
0036 9002                   BLT   MAIN4
0038
0038 A200                   LDX   #$00    Set pointer back to beginning
003A                        EJECT
003A A5DB           MAIN4   LDA   SPDAT   Save character
003C 9D8B00                 STA   RXBUF,X
003F DD7000                 CMP   TXBUF,X Correct?
0042 D00A                   BNE   ERROR
0044
0044 E8                     INX
0045 8EA500                 STX   RXBUFP
0048 A980                   LDA   #%10000000  Reset receive flag
004A 14DA                   TRB   SPFLG
004C 80C5                   BRA   MAIN2
004E
004E
004E 80FE           ERROR   BRA   *       Infinite loop for receive errors
0050                *
0050                * INTERRUPT ROUTINES
0050                *
0050                IRQ     ENTRY         Infinite loop for external interrupt
0050 4C5010                 JMP   *
0053                *
0053                TMRI    ENTRY         Timer interrupt servicing routine
0053 24F9                   BIT   TIMER+1   Clear Timer interrupt source
0055 5A                     PHY           Save registers
0056 DA                     PHX
0057 48                     PHA
0058 58                     CLI           Allow other interrupts
0059 200080                 JSR   TXMODM  Update transmit carrier frequency
005C 200080                 JSR   CNVPS   Update transmit bit
005F 200080                 JSR   CLOCK   Update Real-time clock
0062 9008                   BCC   RETURN  50 mS interval?
0064                *
0064                * Insert 50 mS interrupt servicing routines here
0064                *
0064 8006                   BRA   RETURN
0066                *
0066                BREAK   ENTRY
0066 4C6610                 JMP   *       Infinite loop for software interrupt
0069                *
0069                NMI     ENTRY
0069 4C6910                 JMP   *       Infinite loop for non-maskable int.
006C                *
006C 68             RETURN  PLA           Restore all registers
006D FA                     PLX
006E 7A                     PLY
006F 40                     RTI
0070
0070                * Transmit message
0070 C1C2C3         TXBUF   DC    C'ABCDEFGHIJKLMNOPQRSTUVWXYZ'
008A                TXEND   DS    0
008A 00             TXBUFP  DS    1       Transmit pointer
008B
008B 000000         RXBUF   DS    26      Receive buffer
00A5                RXEND   DS    0
00A5 00             RXBUFP  DS    1       Receive pointer
00A6
```

Real-Time Clock

Listing A-5. Initialization Subroutine (CLKINZ)

```
0000                    COPY  CLOCK,V10         Real time clock
0000                * FILE: CLOCK
0000                ********************************************************
0000                *                                                      *
0000                * CLKINZ - Initializes timer for modem, DTMF and clock  *
0000                *      routines. Timer will interrupt at the transmit  *
0000                *      bit rate.                                       *
0000                *                                                      *
0000                ********************************************************
0000
0000                CLKINZ START
0000
0000                *  Clock constants
0000
0000                *  Oscillator frequency = 8 MHz
0000
0000                CLKCON GEQU  6667    8000000/(4*300)   Bit rate
0000
0000 A90B                  LDA   #<CLKCON          Set Timer
0002 85F8                  STA   TIMER
0004 A91A                  LDA   #>CLKCON
0006 85F9                  STA   TIMER+1
0008 64D5                  STZ   CLKREG  initialize 50 mS timer
000A 60                    RTS
000B
```

Listing A-6. Clock Update Subroutine (CLOCK)

```
0000
0000                ********************************************************
0000                *                                                      *
0000                * CLOCK - Updates clock. Indicates whether 50 mS has   *
0000                *  elapsed.                                            *
0000                *                                                      *
0000                ********************************************************
0000                *
0000                CLOCK  START
0000
0000 E6D5                  INC   CLKREG  50 mS elapsed?
0002 A5D5                  LDA   CLKREG
0004 C90F                  CMP   #15     15 times bit rate
0006 9002                  BCC   EXIT
0008
0008 64D5                  STZ   CLKREG
000A
000A 60             EXIT   RTS           C flag = 1 if 50 mS has elapsed
000B
```

Listing A-7. Initialization Subroutine (URTINZ)

```
0000                    COPY  UART,V10          Convert Parallel <--> Serial
0000                * FILE: UART
0000                ********************************************************
0000                *                                                      *
0000                *  URTINZ - Initialize asynchronous serial transmit and *
0000                *   receive.  This routine initializes flag registers  *
0000                *   that are used to communicate between the main      *
0000                *   program and the interrupt routines.                *
0000                *                                                      *
0000                ********************************************************
0000
0000                URTINZ START
0000
0000 A901                  LDA   #%00000001        Set transmit data to mark
0002 85D6                  STA   PSFLG             initialize transmit flags
0004 64DA                  STZ   SPFLG             initialize receive flags
0006 60                    RTS
0007
```

Listing A-8. Asynchronous Serial Data Transmit Subroutine (CNVPS)

```
0000
0000            ********************************************************
0000            *                                                      *
0000            * CNVPS - Asynchronous serial transmit. This routine is  *
0000            *  called after a timer interrupt. The next serial data  *
0000            *  bit to be sent is in bit 0 of the flag register.      *
0000            *                                                      *
0000            ********************************************************
0000
0000            CNVPS   START
0000
0000 A5D6               LDA     PSFLG   N FLAG = TDRE
0002 48                 PHA             V FLAG = START BIT SENT
0003 28                 PLP             Z FLAG = DATA BITS SENT
0004            *                       C FLAG = SERIAL DATA
0004 F013               BEQ     PSDATA  Sending data bits?
0006
0006 700A               BVS     FIRST   Send Start bit?
0008
0008 101B               BPL     EXIT    Transmit data empty?
000A
000A A5D7               LDA     PSDAT   load transmit register
000C 85D8               STA     SEROUT
000E A940               LDA     #%01000000  set start bit flag,
0010 8011               BRA     SAVFLG  data = start bit
0012
0012
0012 38         FIRST   SEC             ONE STOP BIT
0013 66D8               ROR     SEROUT  stop bit in, first data bit to C flag
0015 4942               EOR     #%01000010  clear start flag, set data flag
0017 8006               BRA     NOLAST
0019
0019
0019 46D8       PSDATA  LSR     SEROUT  get next data bit
001B D002               BNE     NOLAST  Is this the stop bit?
001D
001D 29FD               AND     #%11111101      clear data flag
001F
001F 29FE       NOLAST  AND     #%11111110      C flag (tx bit) to bit 0
0021 6900               ADC     #$00
0023
0023 85D6       SAVFLG  STA     PSFLG   update flag register
0025
0025 60         EXIT    RTS
0026
```

Listing A-9. Asynchronous Serial Data Receive Subroutine (CNVSP)

```
0000
0000            ********************************************************
0000            *                                                      *
0000            * CNVSP - Asynchronous serial bit receive.  This routine *
0000            *  is called after a bit has been received. The bit is   *
0000            *  in bit 0 of the flag register.  Start and framing     *
0000            *  errors are detected.                                  *
0000            *                                                      *
0000            ********************************************************
0000            *  SPFLG:
0000            *  N FLAG, BIT 7 : RECEIVE FULL
0000            *  V FLAG, BIT 6 : 0 = START BIT
0000            *  Z FLAG, BIT 1 : 1 = DATA
0000            *  C FLAG, BIT 0 : SERIAL DATA BIT
0000            *     V  Z
0000            *    ------
0000            *     0  0  Look for start
0000            *     0  1  During start
0000            *     1  1  Data
0000            *     1  0  Stop
0000
0000            CNVSP   START
0000
0000 A5DA               LDA     SPFLG   Put in Processor status
0002 48                 PHA
0003 28                 PLP
0004 5012               BVC     START   Is this a start bit?
0006
0006 F014               BEQ     DATA    Is this a data bit?
0008
0008 9006               BCC     ERROR   Framing error if stop bit is zero
000A
000A A5D9               LDA     SERIN           Save byte
000C 85DB               STA     SPDAT
000E A980               LDA     #%10000000      Set receive full, no data
0010
0010
0010 29BD       ERROR   AND     #%10111101      SET START, NO DATA
0012 64D9               STZ     SERIN           Initialize receive byte
0014 C6D9               DEC     SERIN              to $FF
0016 800A               BRA     EXIT
0018
0018
0018 B0F6       START   BCS     ERROR           FALSE START IF NOT ZERO
001A
001A 0942               ORA     #%01000010      SET TO LOOK FOR DATA
001C            *                               SHIFT START INTO BYTE
001C            DATA    DS      0
001C 66D9               ROR     SERIN           SHIFT DATA
001E B002               BCS     EXIT            DONE IF START IS SHIFTED OUT
0020
0020 29FD               AND     #%11111101      SET TO LOOK FOR STOP
0022
0022 85DA       EXIT    STA     SPFLG           UPDATE FLAGS
0024 60                 RTS
0025
```

Modem Routines

Listing A-10. Bell 103 Standard Constants for Modem Transmit and Receive (MDMCON)

```
0000                    COPY  MODEM,V10         Modem transmit, receive
0000              * FILE: MODEM
0000              ********************************************************
0000              *                                                      *
0000              * MDMCON - Modem constants, Bell 103 standard.         *
0000              *                                                      *
0000              ********************************************************
0000
0000              MDMCON DATA
0000
0000              * OSCILLATOR FREQ. = 8MHZ
0000              * MODEM WITH PRESCALER
0000
0000              * Register value = 8000000/(2*26*FREQ)
0000              * TRANSMIT   SPACE, MARK
0000 4B44         FREQ    DC    I1'75,68'         ANSWER    2025,2225
0002 8F78               DC    I1'143,120'       ORIGINATE 1070,1270
0004
0004              * RECEIVE    ANSWER, ORIGINATE
0004 0504         SCALE   DC    I1'5,4'           32,16  Scale receive count
0006 6B76         CENTP   DC    I1'107,118'       center frequency
0008 8040         SHBIT   DC    H'80 40'          shift register length
000A
000A 0100         NXTBUF  DC    I1'1,0'           buffer switch
000C              RXRTE   EQU   52                bit time
000C              RXRTE2  EQU   26                half bit time
000C
```

Listing A-11. Modem Initialization Subroutine (MDMINZ)

```
0000
0000              ********************************************************
0000              *                                                      *
0000              * MDMINZ - Initialize modem receive buffer pointer.    *
0000              *                                                      *
0000              ********************************************************
0000
0000              MDMINZ START
0000
0000 A901               LDA   #$01      ORIGINATE MODE
0002 85D1               STA   ANSORG
0004 A901               LDA   #$01      SELF TEST
0006 85D2               STA   SLFTST
0008 64CC               STZ   BUFPTR    INZ RECEIVER
000A A906               LDA   #$06        INTBIT value equals
000C 85CE               STA   INTBIT      seven minus the number
000E              *                       of ones in SR and SR+1
000E              *                       (originate mode)
000E A901               LDA   #$01      inz shift register
0010 85D3               STA   SR
0012 A900               LDA   #$00
0014 85D4               STA   SR+1
0016              *                       FALL THRU TO TXMODM
```

Listing A-12. Modem Bit Transmit Subroutine (TXMODM)

```
0000
0000              ********************************************************
0000              *                                                      *
0000              * TXMODM - Transmit a bit from modem.                  *
0000              *  Updates frequency at TXC/DTMF pin.                  *
0000              *                                                      *
0000              ********************************************************
0000
0000              TXMODM START
0000
0000                    USING MDMCON
0000
0000 A5D6               LDA   PSFLG
0002 2901               AND   #%00000001
0004 F004               BEQ   TX1       TXDATA AT PC0     *these
0006              *                                       *lines
0006 04F2               TSB   PC                          *may
0008 8006               BRA   TX2                         *be
000A              *                                       *omitted
000A A901         TX1   LDA   #%00000001                  *
000C 14F2               TRB   PC                          *
000E A900               LDA   #$00                        *
0010              *                                       *
0010              TX2   DS    0                         *
0010 4A                 LSR   A
0011 05D1               ORA   ANSORG
0013 45D2               EOR   SLFTST
0015 2A                 ROL   A
0016 AA                 TAX
0017 BD0080             LDA   FREQ,X
001A 85F6               STA   CTC
001C 60                 RTS
001D
```

Listing A-13. Row/Receive Interrupt Service Routine (RRCI)

```
0000
0000            ********************************************************
0000            *                                                      *
0000            * RRCI - Interrupt service routine                     *
0000            *  for Row/Receive counter.                            *
0000            *                                                      *
0000            * Demodulates modem receive carrier at RXC input pin.  *
0000            *                                                      *
0000            ********************************************************
0000
0000            RRCI    START
0000
0000                    USING MDMCON
0000
0000 48                 PHA             save registers
0001 DA                 PHX
0002 5A                 PHY
0003
0003 A5F4               LDA   RRC               SAVE TIMER REGISTERS
0005 85C4               STA   CRRC
0007 A5F5               LDA   RRC+1             CLEAR INTERRUPT SOURCE
0009 85C5               STA   CRRC+1
000B
000B            * SCALE RECEIVE COUNTER
000B A4D1               LDY   ANSORG
000D BE0080             LDX   SCALE,Y
0010
0010 4A         RR1     LSR   A
0011 66C4               ROR   CRRC
0013 CA                 DEX
0014 D0FA               BNE   RR1
0016
0016            * CALCULATE TIME SINCE LAST SAME RXC TRANSITION
0016 A4CC               LDY   BUFPTR            switch buffers
0018 BE0080             LDX   NXTBUF,Y
001B 86CC               STX   BUFPTR
001D B5CF               LDA   RXCB,X    AREG <-- RXCB - RRC
001F 38                 SEC
0020 E5C4               SBC   CRRC
0022 A8                 TAY
0023 A5C4               LDA   CRRC              RXCB <-- RRC
0025 95CF               STA   RXCB,X
0027 98                 TYA
0028
0028            * DEMODULATE
0028 A6D1               LDX   ANSORG
002A 38                 SEC             AREG <-- AREG - CENTER PERIOD
002B FD0080             SBC   CENTP,X RESULT SIGN IS DATA
002E                    EJECT
002E            * INTEGRATE OVER ONE BIT TIME
002E 2A                 ROL   A         SIGN TO CARRY FLAG
002F B00F               BCS   ONE       ONE OR ZERO?
0031
0031 26D3               ROL   SR        SHIFT IN ZERO
0033 26D4               ROL   SR+1
0035 B5D3               LDA   SR,X      GET BIT SHIFTED OUT
0037 3D0080             AND   SHBIT,X
003A F011               BEQ   TSTBIT
003C
003C E6CE               INC   INTBIT    ZERO IN, ONE OUT
003E 800D               BRA   TSTBIT
0040
0040 26D3       ONE     ROL   SR        DUPLICATE CODE FOR ONE SHIFT
0042 26D4               ROL   SR+1
0044 B5D3               LDA   SR,X      GET BIT SHIFTED OUT
0046 3D0080             AND   SHBIT,X
0049 D002               BNE   TSTBIT
004B
004B C6CE               DEC   INTBIT    ONE IN, ZERO OUT
004D
004D            TSTBIT  DS    0
004D A5CE               LDA   INTBIT  MODEM RECEIVE AT PC7       *these
004F 2980               AND   #%10000000                         *lines
0051 F004               BEQ   TSTA                               *may
0053            *                                                *be
0053 04F2               TSB   PC                                 *omitted
0055 8004               BRA   TSTB                               *
0057            *                                                *
0057 A980       TSTA    LDA   #%10000000                         *
0059 14F2               TRB   PC                                 *
005B            *                                                *
005B            TSTB    DS    0                                  *
005B A5DA               LDA   SPFLG
005D 4A                 LSR   A         SAVE PREVIOUS DATA IN C FLAG
005E A5DA               LDA   SPFLG
0060 24CE               BIT   INTBIT
0062 3004               BMI   TST1
0064
0064 29FE               AND   #%11111110
0066 8002               BRA   TST2
0068
0068 0901       TST1    ORA   #%00000001
006A
006A 85DA       TST2    STA   SPFLG
006C 8942               BIT   #%01000010        LOOKING FOR START BIT?
006E D012               BNE   SAMPLE
0070
0070            * LOOK FOR START TRANSITION
0070 24CE       STRBIT  BIT   INTBIT  DATA SPACE?
0072 302A               BMI   EXIT
0074
0074 9028       SBIT1   BCC   EXIT    PREVIOUS DATA MARK?
0076
0076 A5C5               LDA   CRRC+1  C FLAG = 1
0078 E900               SBC   #RXRTE2
007A 85CD               STA   NXTBIT
007C A902               LDA   #%00000010
007E 04DA               TSB   SPFLG
0080 801C               BRA   EXIT
0082
```

Listing A-13. (continued)

```
0082                    EJECT
0082                * SAMPLE DATA
0082 A5CD           SAMPLE LDA   NXTBIT              NXTBIT : RRC
0084 C5C5                  CMP   CRRC+1
0086 3016                  BMI   EXIT     TIME TO SAMPLE?
0088
0088                * SET NEXT SAMPLE TIME          NXTBIT <-- NXTBIT - RXRATE
0088 E900                  SBC   #RXRTE
008A 85CD                  STA   NXTBIT
008C A5DA                  LDA   SPFLG    RXDATA AT PC1       *these
008E 2901                  AND   #%00000001                   *lines
0090 0A                    ASL   A                            *may
0091 F004                  BEQ   DATA1                        *be
0093                *                                        *omitted
0093 04F2                  TSB   PC                           *
0095 8004                  BRA   DATA2                        *
0097                *                                        *
0097 A902           DATA1  LDA   #%00000010                   *
0099 14F2                  TRB   PC                           *
009B                *                                        *
009B                DATA2  DS    0                             *
009B 200080                JSR   CNVSP    save bit
009E
009E 7A             EXIT   PLY
009F FA                    PLX
00A0 68                    PLA
00A1 40                    RTI
00A2
```

DTMF and Pulse Dialing

Listing A-14. Initialization Routine (DLINZ)

```
0000                    COPY  DIAL,V10          DTMF and pulse dialing
0000                * FILE: DIAL
0000                ************************************************************
0000                *                                                          *
0000                * DLINZ - Pulse and DTMF dialing initialization.           *
0000                *  The CTU Row and Column registers are cleared            *
0000                *  and digit buffers are initialized.                      *
0000                *                                                          *
0000                ************************************************************
0000
0000                DLINZ  START
0000
0000 64F4                  STZ   RRC      clear Row and Column registers
0002 64F5                  STZ   RRC+1
0004 64F6                  STZ   CTC
0006 9C8D00                STZ   DLDIGIT initialize digit buffer
0009 9C8E00                STZ   DIALFLG initialize working storage
000C 60                    RTS
```

Listing A-15. Interrupt Service Routine for Pulse and DTMF Dialing (DIAL)

```
000D                    EJECT
000D                ************************************************************
000D                *                                                          *
000D                * DIAL - 50 mS timer interrupt service routine for         *
000D                *  pulse or DTMF dialing.                                  *
000D                *                                                          *
000D                ************************************************************
000D
000D                DIAL   ENTRY
000D
000D
000D
000D AD8E00                LDA   DIALFLG dialing in progress?
0010 300B                  BMI   SEND
0012
0012 AD8D00                LDA   DLDIGIT another digit?
0015 1055                  BPL   EXIT
0017
0017 8D8E00                STA   DIALFLG dial this digit
001A 9C8D00                STZ   DLDIGIT clear buffer for next digit
001D
001D 2C8E00         SEND   BIT   DIALFLG pulse or DTMF?
0020 8920                  BIT   #%00100000       inter digit pause?
0022 501D                  BVC   PULSE
0024
0024 D013           TONE   BNE   STOP
0026
0026 290F                  AND   #%00001111       get digit
0028 AA                    TAX
0029 BD6D00                LDA   FROW,X           send tones
002C 85F4                  STA   RRC
002E BD7D00                LDA   FCOL,X
0031 85F6                  STA   CTC
0033 A920                  LDA   #%00100000       set inter-digit pause
0035 0C8E00                TSB   DIALFLG
0038 60                    RTS
0039
0039
0039 64F6           STOP   STZ   CTC      tones off
003B 64F4                  STZ   RRC
003D
003D 9C8E00         CLEAR  STZ   DIALFLG clear flags
0040 60                    RTS
```

Listing A-15. (continued)

```
0041                    EJECT
0041 D01F       PULSE   BNE   IDP       inter-digit pause?
0043
0043 890F               BIT   #%00001111        zero?
0045 F016               BEQ   STIDP
0047
0047 A5C1               LDA   CPB       toggle ON HOOK
0049 4920               EOR   #%00100000
004B 85C1               STA   CPB
004D 85F1               STA   PB
004F 8920               BIT   #%00100000        on hook?
0051 F019               BEQ   EXIT
0053
0053 CE8E00             DEC   DIALFLG           decrement
0056 AD8E00             LDA   DIALFLG
0059 890F               BIT   #%00001111        zero?
005B D00F               BNE   EXIT
005D
005D A9AF       STIDP   LDA   #%10101111        start inter-digit pause
005F 8D8E00             STA   DIALFLG
0062
0062 CE8E00     IDP     DEC   DIALFLG           decrement
0065 AD8E00             LDA   DIALFLG
0068 890F               BIT   #%00001111        zero?
006A F0D1               BEQ   CLEAR
006C
006C 60         EXIT    RTS
006D                    EJECT
006D            * DTMF DIGIT MATRIX - SAME AS 8860, 8870
006D
006D            * |C1 |C2 |C3 |C4 |
006D            * +---+---+---+---+
006D            * | 1 | 2 | 3 | D | R1
006D            * | 4 | 5 | 6 | E | R2
006D            * | 7 | 8 | 9 | F | R3
006D            * | B | A | C | 0 | R4
006D
006D            * OSCILLATOR FREQUENCY = 8.0 MHz
006D            * Register value = 8000000/(2*26*FREQ)
006D
006D            * ROWS
006D            R1      EQU   220       697
006D            R2      EQU   199       770
006D            R3      EQU   180       852
006D            R4      EQU   162       941
006D
006D            * COLUMNS
006D            C1      EQU   126       1209
006D            C2      EQU   114       1336
006D            C3      EQU   103       1477
006D            C4      EQU   93        1633
006D
006D            * DTMF Matrix
006D
006D            * Row  tones
006D            FROW    DS    0
006D A2DCDC             DC    I1'R4,R1,R1,R1'   0123
0071 C7C7C7             DC    I1'R2,R2,R2,R3'   4567
0075 B4B4A2             DC    I1'R3,R3,R4,R4'   89AB
0079 A2DCC7             DC    I1'R4,R1,R2,R3'   CDEF
007D
007D            * Column tones
007D            FCOL    DS    0
007D 5D7E72             DC    I1'C4,C1,C2,C3'   0123
0081 7E7267             DC    I1'C1,C2,C3,C1'   4567
0085 726772             DC    I1'C2,C3,C2,C1'   89AB
0089 675D5D             DC    I1'C3,C4,C4,C4'   CDEF
008D
008D 00         DLDIGIT  DS   1         Main program stores digit to be
008E                                    dialed here.
008E            * Bits 3-0      Digit to be dialed.  Digit zero
008E                                    must be changed to ten.
008E            * Bit  6        Dialing mode flag:
008E                                    0 = pulse
008E                                    1 = DTMF
008E            * Bit 7         Digit flag:
008E                                    0 = buffer empty
008E                                    1 = buffer full
008E
008E 00         DIALFLG  DS   1         Working storage for interrupt routine
008F
008F
```

Listing A-16. Interrupt Vectors

```
0000                    COPY  VECTOR,V10        Interrupt vectors
0000                *
0000                VECTOR START
0000                      ORG   $FEF0
0000                RXBUF ENTRY
0000 000000               DS    16
0010                      ORG   $FFEC
0010 0080                 DC    A'NMI'
0012 0080                 DC    A'RESET'
0014                      ORG   $FFF8
0014 0080                 DC    A'RRCI'
0016 0080                 DC    A'IRQ'
0018 0080                 DC    A'TMRI'
001A 0080                 DC    A'BREAK'
```

Listing A-17. Program Global Symbol Table

```
Global Symbol Table:

ANSORG   00D1 3   BREAK    F889 0   BUFPTR   00CC 3   CCSR     00C7 3
CCTC     00C6 3   CENTP    F937 4   CLKCON   1A0B 0   CLKINZ   F8C9 0
CLKREG   00D5 3   CLOCK    F8D4 0   CNVPS    F8E6 0   CNVSP    F90C 0
CPA      00C0 3   CPB      00C1 3   CPC      00C2 3   CPD      00C3 3
CRRC     00C4 3   CSR      00F7 2   CTC      00F6 2   CTIMER   00C8 3
CTUDEF   F800 2   CTUINZ   F800 0   FREQ     F931 4   INTBIT   00CE 3
IRQ      F873 0   MAIN     F823 0   MDMCON   F931 4   MDMINZ   F93D 0
NMI      F88C 0   NXTBIT   00CD 3   NXTBUF   F93B 4   ORG      F800 1
PA       00F0 2   PAGEZERO F800 3   PB       00F1 2   PC       00F2 2
PD       00F3 2   PSDAT    00D7 3   PSFLG    00D6 3   RESET    F800 0
RRC      00F4 2   RRCI     F970 0   RXBUF    FEF0 0   RXCB     00CF 3
RXRTE    0034 4   RXRTE2   001A 4   SCALE    F935 4   SERIN    00D9 3
SEROUT   00D8 3   SHBIT    F939 4   SLFTST   00D2 3   SPDAT    00DB 3
SPFLG    00DA 3   SR       00D3 3   TIMER    00F8 2   TMRI     F876 0
TXMODM   F953 0   URTINZ   F8DF 0   VECTOR   FEF0 0

Program starts at $F800 and is $0800 bytes long.
```

Appendix B—The G65DS-150 Evaluation Board

When developing a CTU-based system, it is imperative that the design engineer have a convenient means for not only prototype development and debugging, but also for software development. The G65DS-150 Evaluation Board serves this purpose by providing G65SC150 CTU emulation during the various phases of system hardware and software development. Features include (See Figure B-1):

- Socket for G65SC150 CTU
- 2K × 8 EPROM or RAM
- Internal oscillator (3 to 16 MHz)
- Vector translation logic
- Configuration switches for function selection
- 40-pin socket for connection to an In-Circuit Emulator
- 68-pin grid array header for connection to the prototype system

The Evaluation Board's G65SC150 CTU replaces the prototype system's CTU during the development and emulation phase. During initial development, the Evaluation Board is normally used in conjunction with an In-Circuit Emulator. When using the In-Circuit Emulator, the CTU must be operated in the peripheral mode. In this way, the Emulator serves to replace the CTU's internal G65SC00 microprocessor, thus allowing full emulation of all G65SC150 CTU function. . . including its full instruction set.

In this mode, the CTU's internal microprocessor is disabled, allowing the Emulator's debugging and software development capabilities to be used within the designer's CTU-based system.

When using the Evaluation Board, the CTU's internal ROM can be disabled during software development and replaced by a 2K × 8 EPROM or RAM (designer's choice) on the Evaluation Board. This allows the designer's program to be easily debugged and modified prior to committing the code to the CTU's mask-programmed ROM. Normally, RAM storage is used during initial program development. Once the program is partially debugged, the RAM can be replaced with the less volatile EPROM for continued evaluation.

The Evaluation Board's Vector Translation Logic is used to translate address vectors as generated by the In-Circuit Emulator's G65SC00 microprocessor. This translation makes all vector addresses consistent with the G65SC150 CTU format.

Once the prototype system and software has been partially debugged, the In-Circuit Emulator is normally disconnected, the CTU internal microprocessor is enabled, and the CTU is switched from the peripheral mode to the CTU mode. At this point, the Evaluation Board appears as a full-functioning CTU to the designer's prototype system. The EPROM will continue to be used until development is complete and the CTU ROM is masked for final coding.

For further information on the GTE G65DS-150 Evaluation Board, feel free to call your nearest GTE Microcircuits representative.

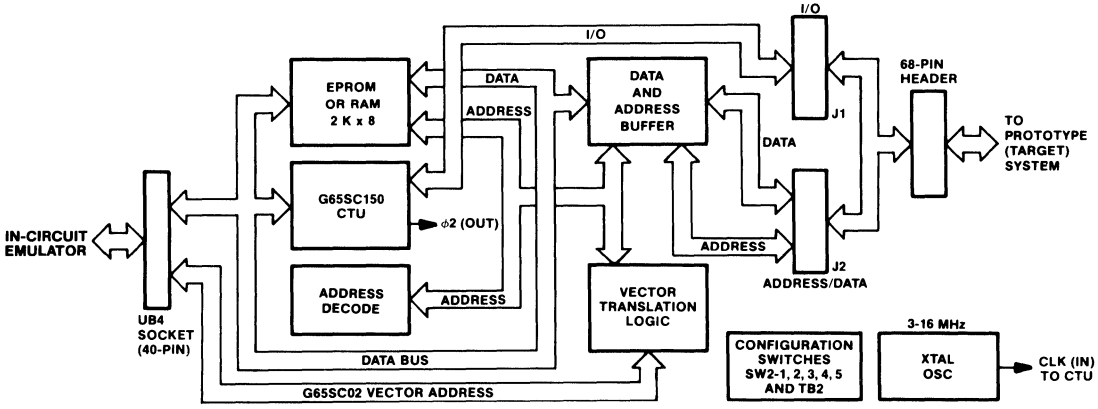


Figure B-1. G65DS-150 Evaluation Board Block Diagram

Material List

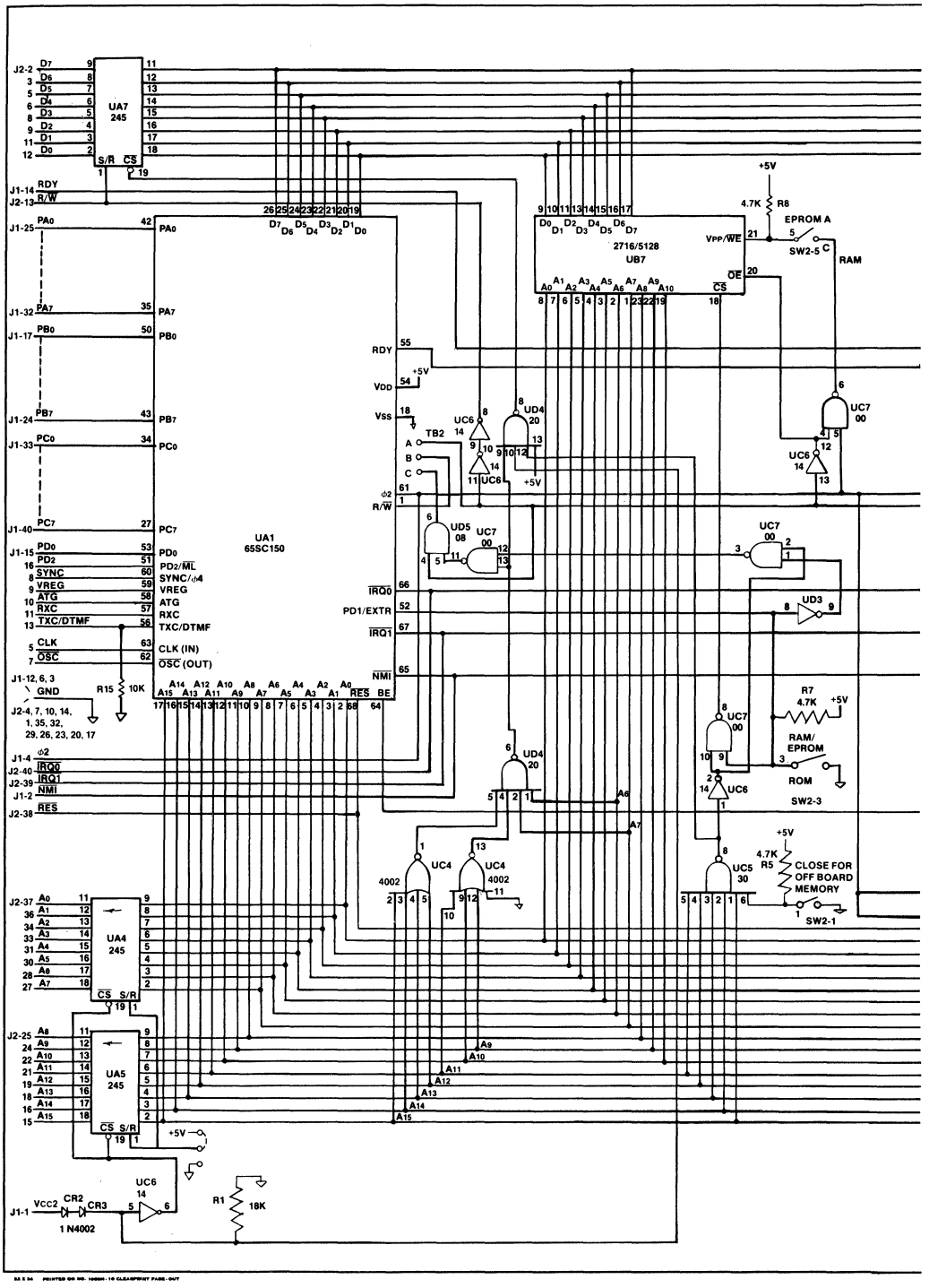
G65DS-150 Evaluation Board

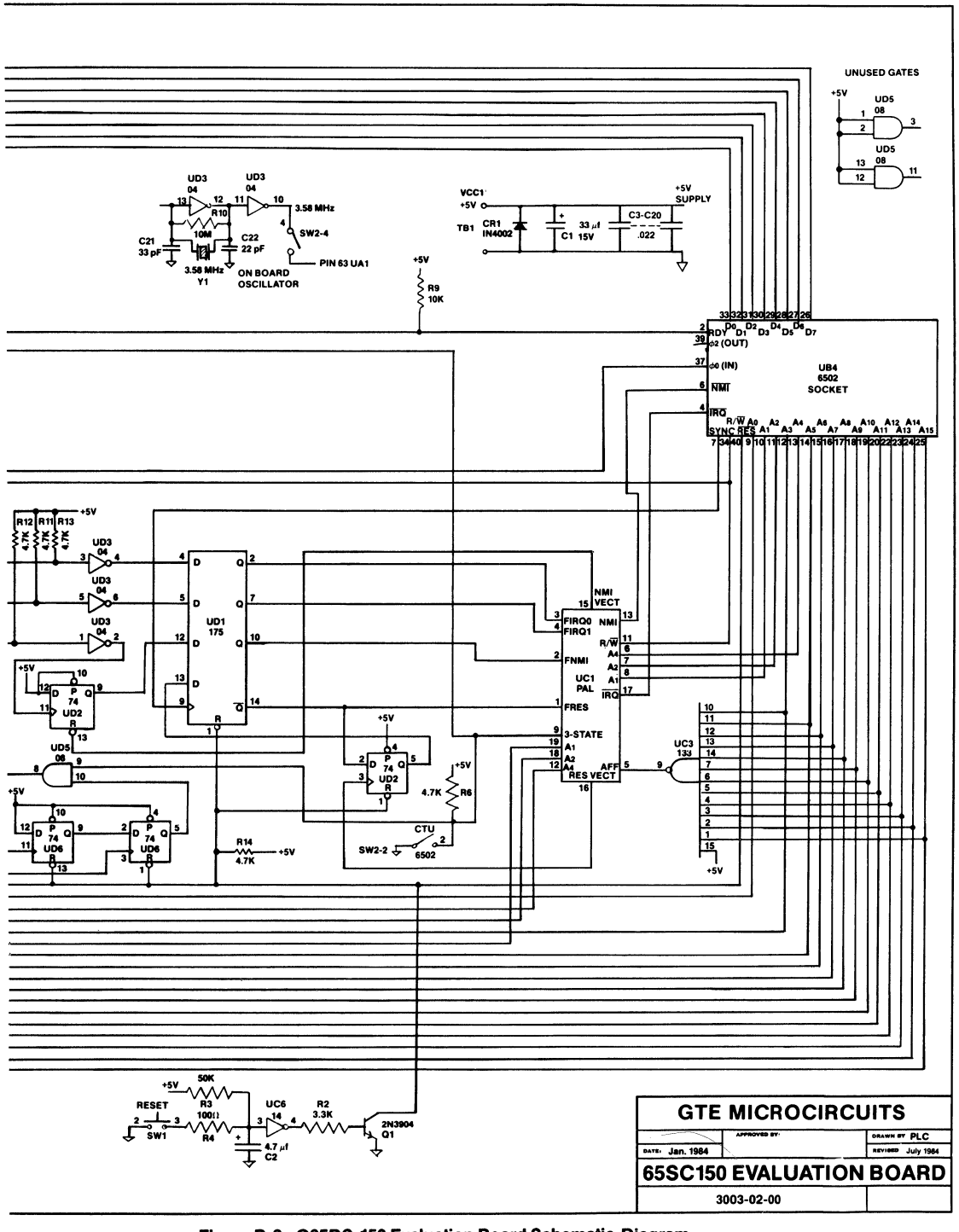
Item No.	Qty	P/N	Description	Ref. Desig.	Notes
1	1		PWB 3001 C		
2	1		65SC150 JEDEC C Package	UA1	GTE
3	1		65SC02 (Not Supplied)	UB4	
4	1		5128 2K × 8 CMOS RAM	UB7	OKI
5	1		74HC00 Quad 2-Input NAND	UC7	
6	1		74HC04 Hex Inverter	UD3	
7	1		74HC08 Quad 2-Input AND	UD5	
8	1		74HC14 Hex Schmitt Trigger	UC6	
9	1		74HC20 Dual 4-Input NAND	UD4	
10	1		74HC30 8-Input NAND	UC5	
11	2		74HC74 Dual D-Type Flip-Flops	UD2, UD6	
12	1		74HC133 13-Input NAND	UC3	
13	1		74HC175 Quad D-Type Flip-Flops	UD1	
14	3		74SC245 Octal Transceiver	UA4, 5, 7	
15	1		74HC4002 Dual 4-Input NOR	UC4	
16	1		PAL16L8A Programmable Array Logic	UC1	
			Resistors (1/4W 5%)		
17	1		3.3K	R2	
18	8		4.7K	R5-R8, R11-R14	
19	1		18K	R1	
20	1		100 ohm	R4	
21	1		51K	R3	
22	2		10K	R9, R15	
23	1		10M	R10	
			Capacitors		
24	17		0.022 μF Axial Ceramic	C3-C20	
25	1		3.3 μF 15V Tant	C1	
26	1		4.7 μF 15V Tant	C2	
27	1		22pfd SilverMica	C22	
28	1		33pfd SilverMica	C21	
29	1		Push. SW TP12-H8-V3-B-E	SW1	C&K
30	1		5 × 1 DIP SW 76SB0 5	SW2	Grayhill
31	2		40 Pin R/A Male Header 609-4007	J1, J2	Ansley
32	1		Terminal Block 2 Screw ED100/2DS	TB1	EURO-DIP
33	9		14 Pin DIP Socket	C4-C7, D2-D6	
34	2		16 Pin DIP Socket	C3, D1	
35	4		20 Pin DIP Socket	A4, A5, A7, C1	
36	1		24 Pin Socket	B7	
37	1		40 Pin Socket	B4	
38	1		68 Plastic Chip Carrier Socket	A1	
39	3		Option Selection Post for R/W Select	TB2-A, B, C	
40	1		Crystal 3.58 MHz HC-18/U	Y1	
41	5		Rubber Stick-on Feet		
42	3		1N4002 Diode	CR1, CR2, CR3	
43	1		Transistor 2N 3904	Q1	

G65DS-150 Cable

Item No.	Qty	P/N	Description	Ref. Desig.	Notes
1	2		40 Pin Ribbon Connectors		
2	2		8" Long 40 Conductor, Woven Wire, 24 Gage		
3	2		72 Pin, Pin Grid Arrays PPS-72-AG1 D		Augat

Figure B-2. G65DS-150 Evaluation Board Material List


UA7
245
S/R
CS
UA1
65SC150
UA4
245
UA5
245
2716/5128
UB7
EPROM A
RAM
SW2-5
SW2-3
SW2-1
R7
4.7K
RAM/
EPROM
ROM
CLOSE FOR
OFF BOARD
MEMORY
R8
R5
R15
10K
R1
18K
CR2
CR3
1 N4002
UC4
4002
UC5
30
UC6
14
UC7
00
UD3
UD4
20
UD5
08
TB2
+5V
GND
RDY
R/W
RES
NMI
IRQ0
IRQ1
SYNC
VREG
ATG
RXC
TXC/DTMF
CLK (IN)
OSC (OUT)
PD1/EXTR
PD2/ML
SYNC/φ4
VDD
VSS
VPP/WE
OE
CS



GTE MICROCIRCUITS		
	APPROVED BY:	DRAWN BY PLC
DATE: Jan. 1984		REVISED July 1984
65SC150 EVALUATION BOARD		
3003-02-00		

Figure B-3. G65DS-150 Evaluation Board Schematic Diagram

5 Quality Assurance

Quality Assurance

GTE Microcircuits' philosophy on Quality Assurance is to produce the highest quality and most reliable product possible...using the latest in technologies, instrumentation and procedures.

And at GTE Microcircuits we are continually striving to not only improve quality, but refine the empirical and statistical methods by which we measure quality and establish reliability. It is our goal to lead the way...setting standards for quality that are unsurpassed within the industry.

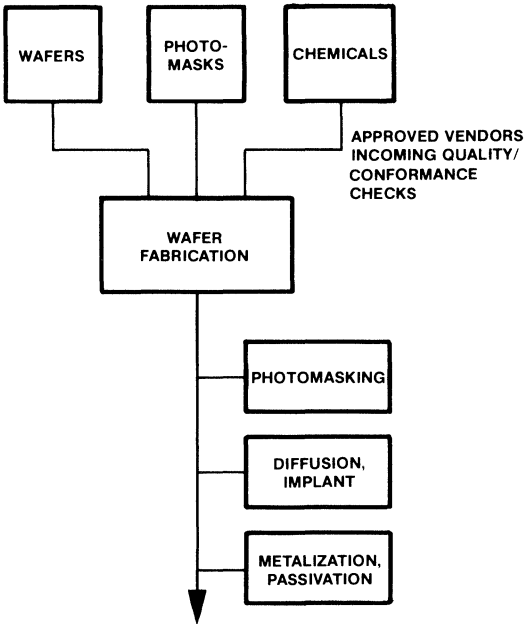


Figure 1. Process and Quality Checks

GTE Product Quality

Product quality is the ability of a product to perform as expected...to conform to its design specification without exception. It is a characteristic that must be consciously built into the product. And it starts with:

Quality Materials from Quality Vendors—Becoming a GTE supplier of raw materials is not easy. To become an approved vendor, one must first meet and maintain stringent standards and be willing to participate in periodic material specification reviews. During each review, materials such as wafers, masks and other piece parts are introduced into the manufacturing process through controlled experiments. The effect of these materials on overall quality and product reliability is evaluated by "split-lot" testing methods. At GTE, incoming inspection is a vital part of the quality program. Materials such as wafers and photomasks are inspected at a "receiving" gate.

Critical Checkpoints at the Photomask Stage—GTE processing maintains three critical inspection "gates" at the photomask stage. Each of these three gates involve visual inspections to not only guarantee correct mask alignment, but to check that critical dimensions fall within specified limits. See Figure 2.

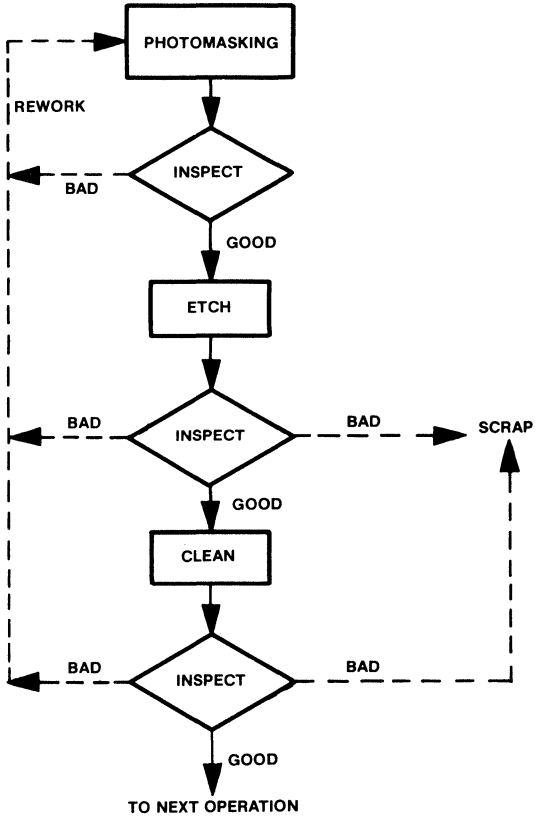


Figure 2. Process Quality Checkpoints

Quality Monitors During Diffusion and Implantation—Quality monitors are used during diffusion and implantation processes. These monitors provide for Capacitance/Voltage (CV) measurements. CV analysis is a useful tool... providing measurements of how much phosphorus or boron is being "doped" into each wafer. Furthermore, CV analysis is used during the diffusion process to monitor oxide quality and system cleanliness. Another means of controlling quality consists of sheet resistance and layer thickness measurements. These measurements are continuously monitored and compared against established criteria.

Quality Monitors During Test and Assembly—Once wafer processing has been completed, the wafers are sent to the test area for electrical probing. Wafer probing consists of a 100 percent functional and parametric test of each wafer in preparation for final assembly.

During the assembly process, Quality Assurance procedures require various audit points. See Figure 3. At least three audit points involve optical inspections at critical stages within the assembly process. These inspections ensure:

- Each wafer has been correctly and fully probed.
- Damage has not occurred as each wafer is sawed, cleaned and broken into individual dice.
- Quality is maintained during die attachment to the package and during wire bonding.

Once packaging has been completed, and the devices have been sealed, each ceramic and cerdip package is required to undergo a 100 percent gross leak test. And as a further check of package hermeticity, a sample fine leak test is conducted as a final check in the assembly process. At this point, each device is ready for final electrical (DIP) testing where worst case voltage and timing tests are performed.

Following DIP testing, all products are marked and, depending on the product, subjected to burn-in screening. Temperatures and burn-in times vary with product type and individual product specification. During the burn-in period, both voltage and temperature stresses are applied to weed out all possible "infant mortalities."

The Measure of Quality—At a given "window" in time, the number of parts which fail to meet specification can be expressed as a percentage or as PPM (Parts-Per-Million).

Example: 1.0% = 10,000 PPM
0.01% = 100 PPM

GTE Product Reliability

Product reliability is measured by the ability of a product to perform an intended function (conformance to specification) for a given period of time, and under specified environmental conditions.

To establish and maintain the highest standards of reliability, and to monitor the continued effectiveness of the production process and quality controls, GTE Microcircuits maintains an ongoing reliability assessment program as shown in Figure 4. A very important test within the reliability program is the "life test." This test is carefully designed to ensure specified component lifetime and to provide a prediction of failure rates.

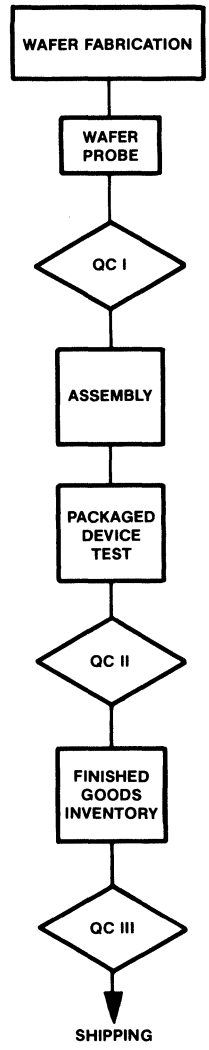


Figure 3. Quality Control Gates/Inspections

The Measure of Reliability—Reliability is measured as the number of units failing (or predicted to fail) in a given time period, and is typically expressed as a percent per 10^3 device-hours, or as "FITS" (Fails per 10^9 Hours). A more definitive description of "failure rate" is as follows:

Failure Rates—Failure Rate is an alternative expression to MTTF (Mean Time To Failure). It is expressed, through statistical techniques, as the probability that a given product or component will fail within a given period of time and within specified environmental conditions. Failure

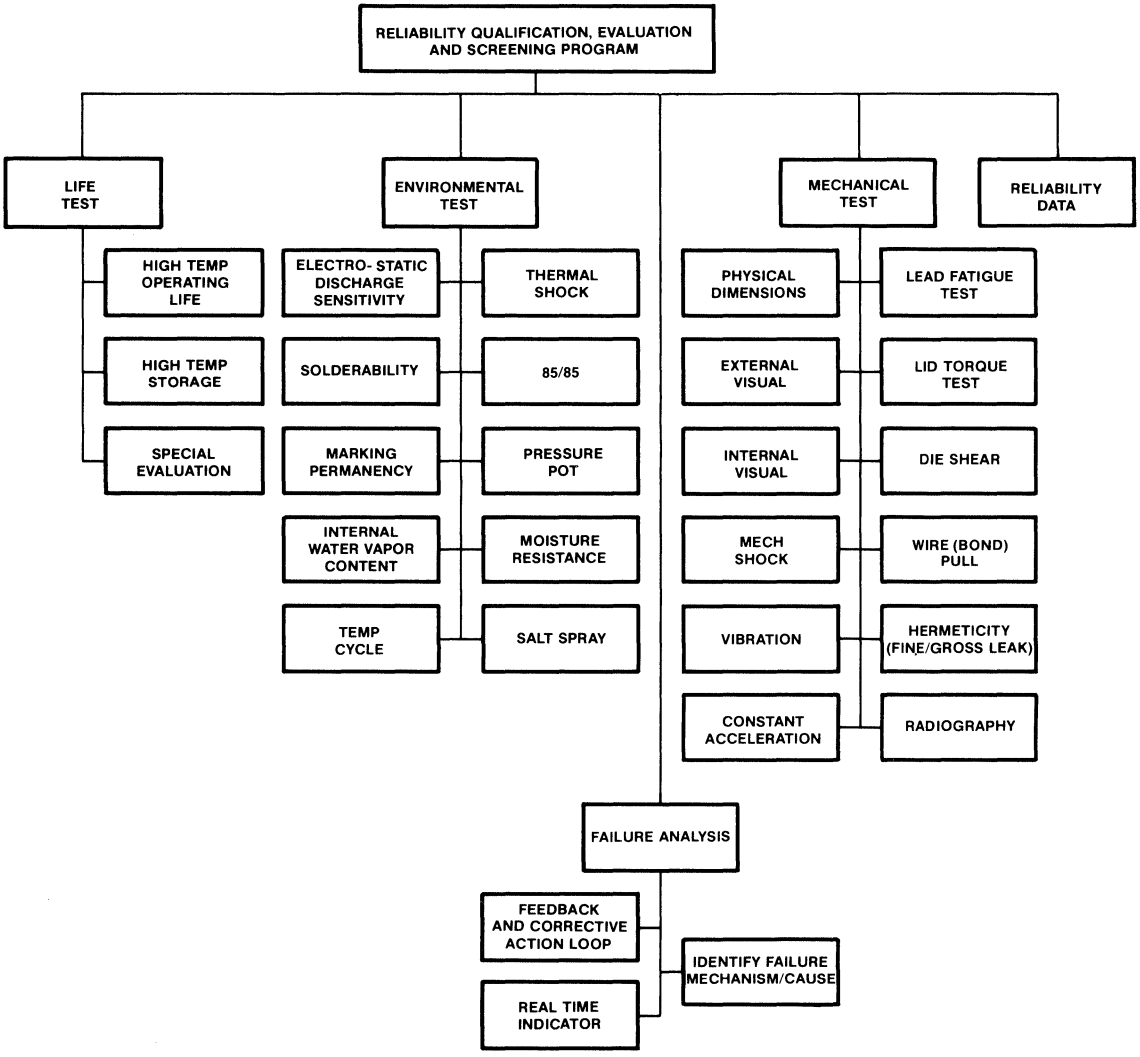


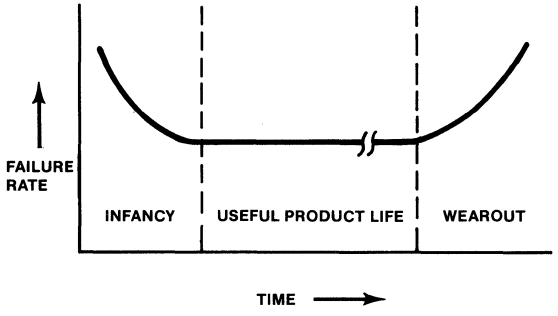
Figure 4. GTE Quality Assurance and Reliability Program

Rates may be presented in various ways, the more common being as follows:

TERM	SYMBOL	FAILS PER	EXPRESSED AS
Failure Rate	FR	10^5 Device Hours	% per 1000 Device Hours
Failure Units	FITS	10^9 Device Hours	FITS
Average Fail Rate	λ	10^6 Device Hours	—
Mean Time To Failure or Mean Time Between Failures	MTTF or MTBF	—	Time: Hours Years

The above failure-related terms may be interchanged according to the following relationship:

$$FR = \frac{FITS}{10^4} = \frac{1}{MTBF\ (10)} = \frac{\lambda}{10}$$



The familiar bathtub curve of product lifetime shows the regions of Infancy, Useful Product Life, and Wearout. These regions can be defined as follows:

Infancy—This region is the burn-in period. It is used to detect and eliminate early failures. Infant mortality is caused by early failure of weak components or is due to non-random events or causes. These conditions can cause early high failure rates which will fall off rapidly with time. Infant mortality is a quality-related issue.

Useful Product Life—Failures during product "middle age" are due to random causes which occur at random intervals, but with a fairly constant average rate of failure over a specified time period. Such failure rate is a reliability-related issue.

Wearout—Wearout normally occurs after a long period of useful life. During the Wearout period, failure rates will rise rapidly and failures will occur quite frequently. This marks the end of useful product life.

Customer Service is a QA Philosophy

GTE's Quality Assurance organization maintains a continuing awareness and concern about GTE product reliability. This concern extends far beyond our internal QA procedures and the examination of products that do not meet internal specifications. Although life tests are an effective check of product reliability, the crucial test begins after the parts have been installed into customer systems. Once in the customer environment, GTE's Quality Assurance program continues by monitoring and reacting to customer problems. Customer product experience is a vital link to our QA program.

Reliability Assessment Program

The purpose of this program is to provide a comprehensive and systematic procedure for the assessment of device reliability and product improvement.

This program includes the interdependent functions of Life Testing, Failure Analysis, and Special Evaluations as may be required. The program is an adjunct to our standard QA Qualification program, and serves as a follow-on effort for ongoing (generic) quality/reliability conformance verification. New product qualifications are conducted on die, process technologies, packages, process/design changes, new materials.

Product life testing is the primary means for determining reliability assessments. Devices are subjected to thermal stress to accelerate failure mechanisms. Data obtained from high temperature tests (typically +125°C) are "derated" to 50°C for the prediction of device failure rates. Life testing is performed as part of:

- New product qualifications
- Existing product verification (generic)
- The program to determine and monitor failure rates
- The program to determine infant mortality and failure rate predictions

New products are subjected to life testing as part of their acceptance qualification prior to being approved for standard production.

Each die process technology is routinely subjected to life tests. This is done by a rotating sampling of (generic) die types which represent each specific technology.

Failure Analysis

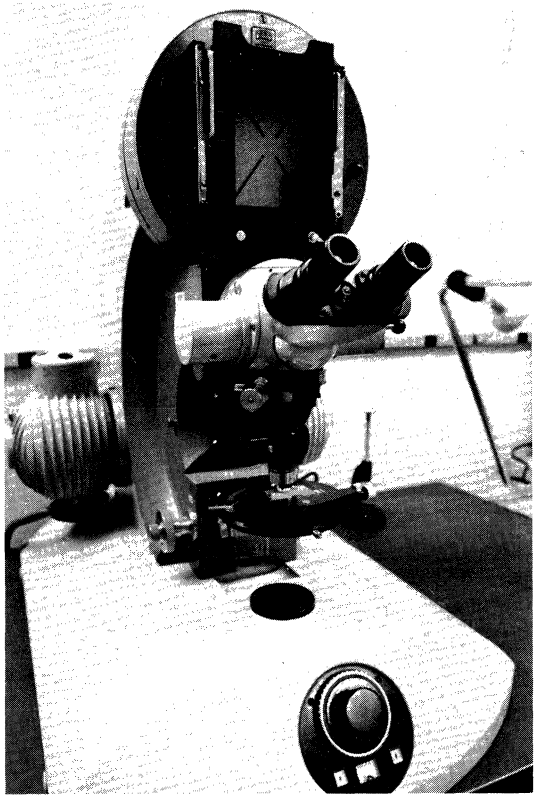
Devices which fail standard life tests or any other special testing are analyzed to determine the failure mechanism and cause. Each failure is classified and recorded. This information adds to our data base, aids in monitoring trends, and also provides the basic information for Pareto analysis, etc. These data are then summarized and published periodically...thus providing important information for ongoing product improvement programs. Furthermore, specific failure data are reported to appropriate groups (e.g., Design, Process Engineering, etc.) so that corrective action can be taken. It is this feedback

of failure analysis information which leads to improvements in testing, design and processing.

Intensive Failure Analysis... Let's Take a Look!

It can be said that analytical procedures are the reverse of the manufacturing process. Unacceptable devices are examined physically, optically and electrically on an individual basis. After identifying what caused the failure, Reliability Engineering analyzes the cause. The Microanalysis Laboratory at GTE Microcircuits is dedicated to failure analysis. This capability involves sensitive equipment which offers extensive analysis and problem solving capabilities. It is through precise optical and chemical analysis that miniscule metal lines and submicron geometries can be analyzed.

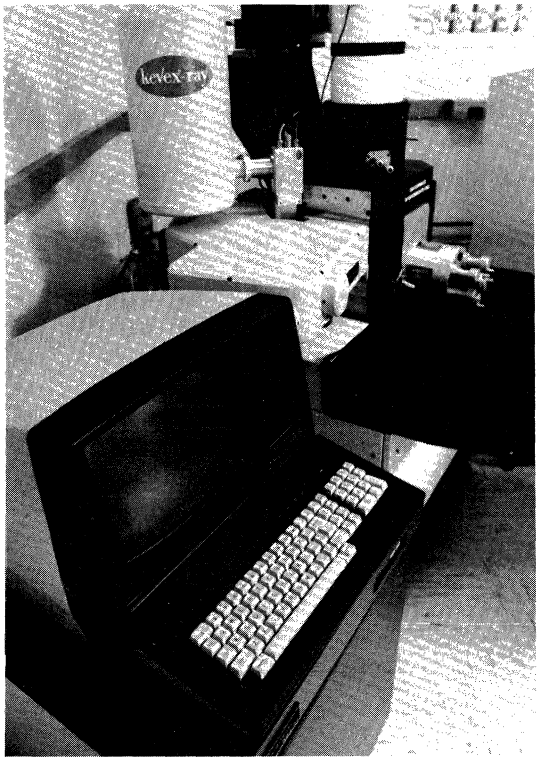
Optical Microscopes Provide Close-Up Color Photos—High power optical inspections are carried out with a Zeiss Ultaphot III® microscope. Cesium or halogen light sources, polarized light, interference contrast, and conventional bright field are among the techniques available. Extended magnification ranges of 10X to 1600X are used in combination with a 4" × 5" color photo format.



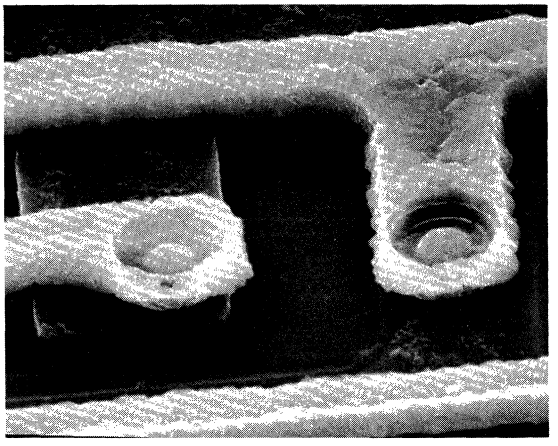
Cross Sectioning Provides a Detailed View of Internal Flaws—Cross sectioning is used extensively during failure analysis. Samples are cast in epoxy, cut or ground to the plane of interest, and then lapped and polished to a mirror-like surface. Cracks, voids and other internal flaws are easily observed in this way. Semiconductors can be stained to reveal junction depths or bulk defects. Samples can be observed by optical microscopy or with the SEM.

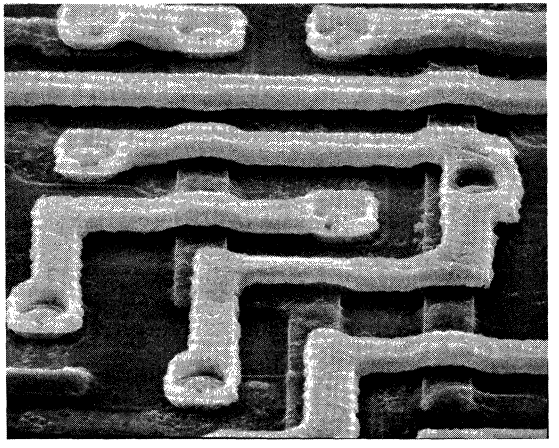
X-Ray Spectrometers Add Versatility to the SEM—Two x-ray spectrometers are attached to the SEM, thus allowing chemical analysis of the sample being observed. Chemical analysis is performed on a volume of material 1-2 micrometers in diameter where the electron beam strikes the sample. A large area can be analyzed by "rastering" the beam or a single spot analyzed by holding the beam stationary. X-ray maps can also be made which show the spatial distribution of an element within a sample. Energy Dispersive X-ray Spectrometry (EDS) is done with a Kevex Corporation system. Elements with atomic numbers of 11 (Sodium) and higher can be detected down to approximately 0.1% by weight. Extensive software exists for x-ray data analysis and processing.

Wavelength Dispersive X-ray Spectrometry (WDS) is performed with a Microspec WDX-2A®. Elements down to atomic number 5 (Boron) can be detected with a sensitivity of approximately 100 PPM. This system is primarily qualitative in nature and can also produce x-ray maps.



GTE's Scanning Electron Microscope—GTE's scanning electron microscope (SEM) is a vital instrument for visual failure analysis. The Cambridge Stereoscan 250® is capable of magnifications from 10X to 100,000X. Samples as large as an entire five-inch wafer can be accommodated intact with full 90° tilt and 360° rotation. In addition to the normal secondary electron image system, a high efficiency back scattered electron detector, cathodoluminescence detector, and specimen absorbed current system are fitted.



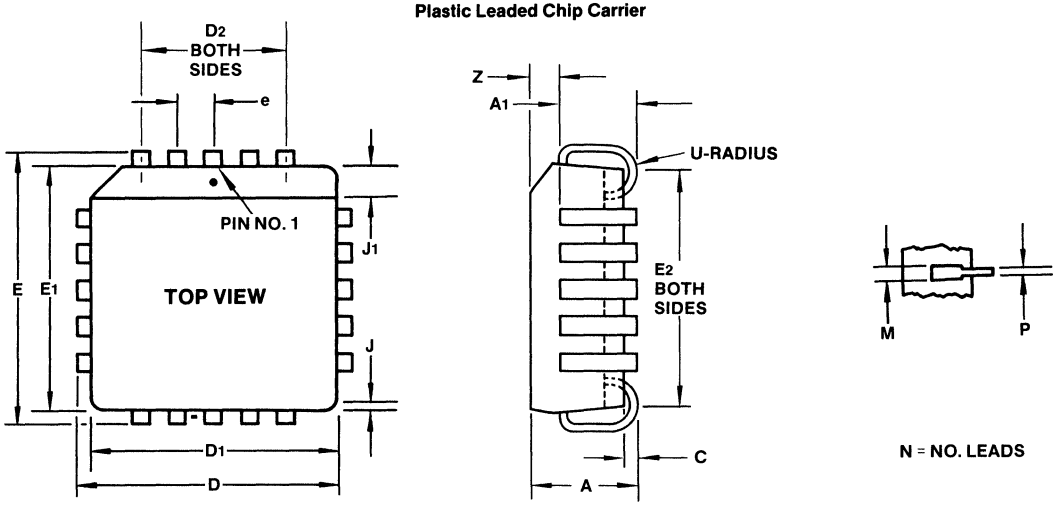


6 Packaging Information

GTE Microcircuits

Packaging Information

Plastic Leaded Chip Carrier



20-LEAD PLASTIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.20	4.57
A1	0.090	0.120	2.29	3.04
C	0.020	—	0.51	—
D	0.385	0.395	9.78	10.03
D1	0.350	0.356	8.890	9.042
D2	0.200 REF		5.08 BSC	
E	0.385	0.395	9.78	10.03
E1	0.350	0.356	8.890	9.042
E2	0.290	0.330	7.37	8.38
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	20		20	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

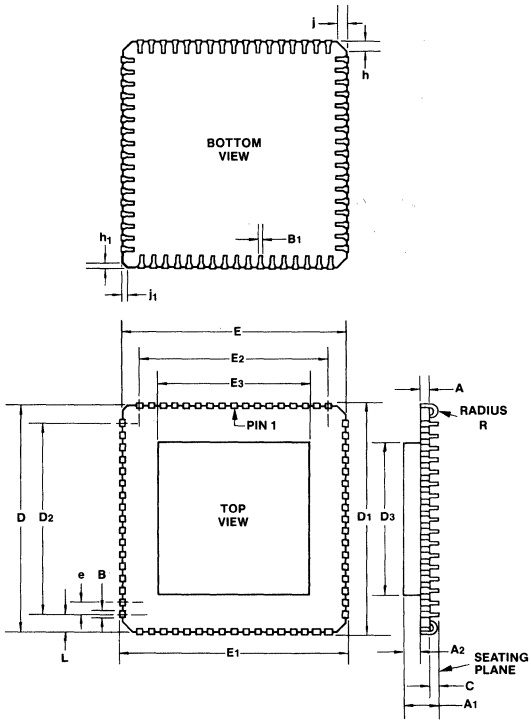
28-LEAD PLASTIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.20	4.57
A1	0.090	0.120	2.29	3.04
C	0.020	—	0.51	—
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.430	11.582
D2	0.300 REF		7.62 BSC	
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.430	11.582
E2	0.390	0.430	9.91	10.92
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	28		28	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

44-LEAD PLASTIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.20	4.57
A1	0.090	0.120	2.29	3.04
C	0.020	—	0.51	—
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.510	16.662
D2	0.500 REF		12.70 BSC	
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.510	16.662
E2	0.590	0.630	14.99	16.00
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	44		44	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

68-LEAD PLASTIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.20	5.08
A1	0.090	0.130	2.29	3.30
C	0.020	—	0.51	—
D	0.985	0.995	25.02	25.27
D1	0.950	0.958	24.130	24.330
D2	0.800 REF		20.32 BSC	
E	0.985	0.995	25.02	25.27
E1	0.950	0.958	24.130	24.333
E2	0.890	0.930	22.61	23.62
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	68		68	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

84-LEAD PLASTIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.20	5.08
A1	0.090	0.130	2.29	3.30
C	0.020	—	0.510	—
D	1.185	1.195	30.10	30.35
D1	1.150	1.158	29.210	29.413
D2	1.000 REF		25.40 BSC	
E	1.185	1.195	30.10	30.35
E1	1.150	1.158	29.210	29.413
E2	1.090	1.130	27.69	28.70
e	0.050 TYP		1.27 TYP	
J	—	0.020	—	0.51
J1	0.042	0.048	1.067	1.219
M	0.026	0.032	0.661	0.812
N	84		84	
P	0.013	0.021	0.331	0.533
Z	0.042	0.056	1.07	1.42

Leaded Ceramic Chip Carrier



28-LEAD CERAMIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.035	0.045	0.89	1.14
A1	—	0.180	—	4.51
A2	0.050	0.075	1.27	1.90
B	0.020	0.025	0.51	0.64
C	0.020	—	0.51	—
D	0.420	0.440	10.67	11.18
D1	0.480	0.500	12.19	12.70
D2	0.300		7.62	
D3	0.395	0.425	10.03	10.80
E	0.420	0.440	10.67	11.18
E1	0.480	0.500	12.19	12.70
E2	0.300		7.62	
E3	0.395	0.425	10.03	10.80
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.015	0.025	0.38	0.64
j	0.040 BSC		1.02 BSC	
j1	0.015	0.025	0.38	0.64
L	0.065 REF		1.66 REF	
N	28		28	
R	0.010	0.030	0.25	0.76

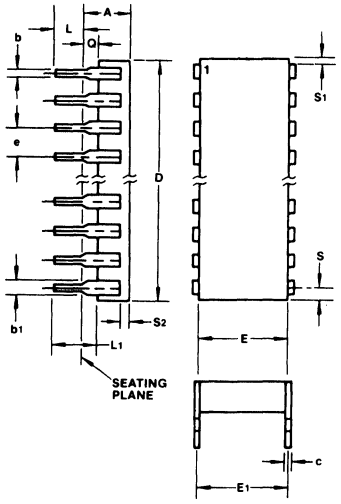
N = NO. LEADS

44-LEAD CERAMIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.035	0.045	0.89	1.14
A1	—	0.200	—	5.08
A2	0.070	0.095	1.78	2.41
B	0.020	0.025	0.51	0.64
C	0.020	—	0.51	—
D	0.620	0.640	15.75	16.26
D1	0.680	0.700	17.27	17.78
D2	0.500		12.70	
D3	0.485	0.530	12.32	13.46
E	0.620	0.640	15.75	16.26
E1	0.680	0.700	17.27	17.78
E2	0.500		12.70	
E3	0.485	0.530	12.32	13.46
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.015	0.025	0.38	0.64
j	0.040 BSC		1.02 BSC	
j1	0.015	0.025	0.38	0.64
L	0.065 REF		1.66 REF	
N	44		44	
R	0.010	0.030	0.25	0.76

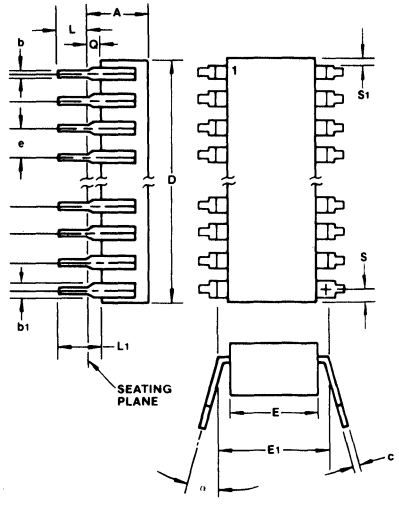
68-LEAD CERAMIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.035	0.045	0.89	1.14
A1	—	0.200	—	5.08
A2	0.070	0.095	1.78	2.41
B	0.020	0.025	0.51	0.64
C	0.020	—	0.51	—
D	0.920	0.940	23.37	23.88
D1	0.980	1.000	24.89	25.40
D2	0.800		20.32	
D3	0.600	0.630	15.24	16.00
E	0.920	0.940	23.37	23.88
E1	0.980	1.000	24.89	25.40
E2	0.800		20.32	
E3	0.600	0.630	15.24	16.00
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.015	0.025	0.38	0.64
j	0.040 BSC		1.02 BSC	
j1	0.015	0.025	0.38	0.64
L	0.065 REF		1.66 REF	
N	68		68	
R	0.010	0.030	0.25	0.76

84-LEAD CERAMIC CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.035	0.045	0.89	1.14
A1	—	0.200	—	5.08
A2	0.070	0.095	1.78	2.41
B	0.020	0.025	0.51	0.64
C	0.020	—	0.51	—
D	0.990	1.010	25.15	25.65
D1	1.180	1.200	29.5	30.48
D2	1.000		25.40	
D3	0.600	0.630	15.24	16.00
E	0.990	1.010	25.15	25.65
E1	1.180	1.200	29.97	30.48
E2	1.000		25.40	
E3	0.600	0.630	15.24	16.00
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.015	0.025	0.38	0.64
j	0.040 BSC		1.02 BSC	
j1	0.015	0.025	0.38	0.64
L	0.065 REF		1.66 REF	
N	84		84	
R	0.010	0.030	0.25	0.76

Ceramic Dual In-Line



Plastic & Cerdip Dual In-Line



14-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.785	—	19.94
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

16-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.840	—	21.34
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

18-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.960	—	24.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

20-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.060	—	26.92
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

22-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.260	—	32.00
E	0.350	0.390	8.89	9.91
E1	0.390	0.420	9.91	10.67
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.075	0.38	1.91
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

24-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.290	—	32.77
E	0.500	0.610	12.70	15.49
E1	0.520	0.620	13.21	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.200	3.05	5.08
L1	0.150	—	3.81	—
Q	0.015	0.075	0.38	1.91
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

continued on next page

continued from page 3

28-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.490	—	53.24
E	0.510	0.620	12.95	15.75
E1	0.520	0.630	13.21	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

40-PIN PACKAGE				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	2.096	—	53.24
E	0.510	0.620	12.95	15.75
E1	0.520	0.630	13.21	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

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