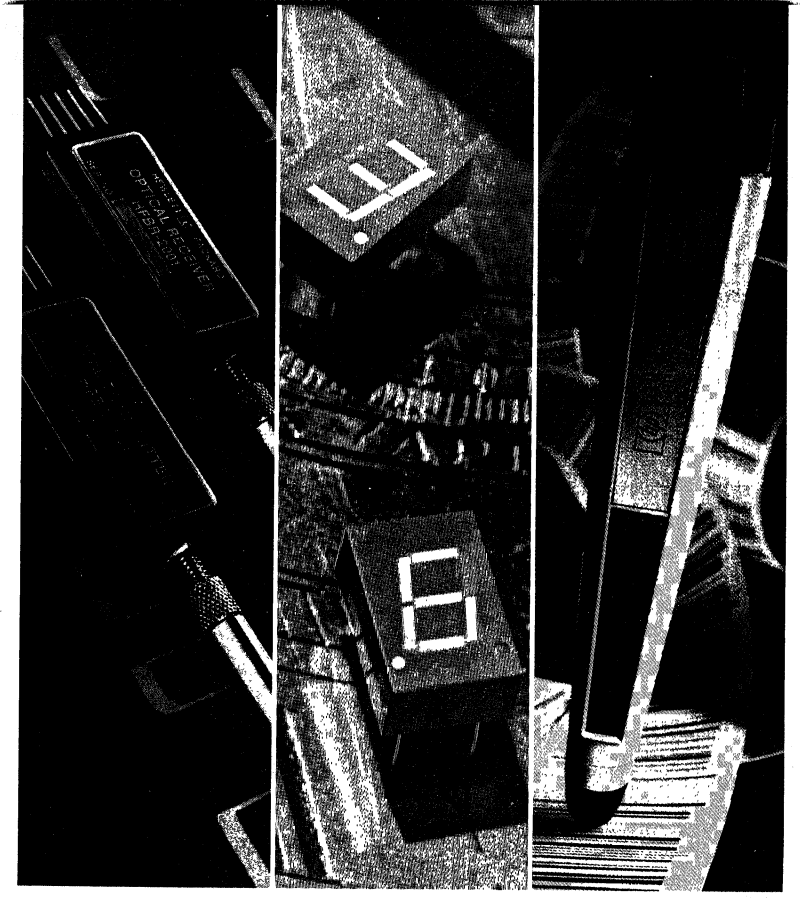
Optoelectronics Designer's Catalog

1980

HEWLETT PACKARD



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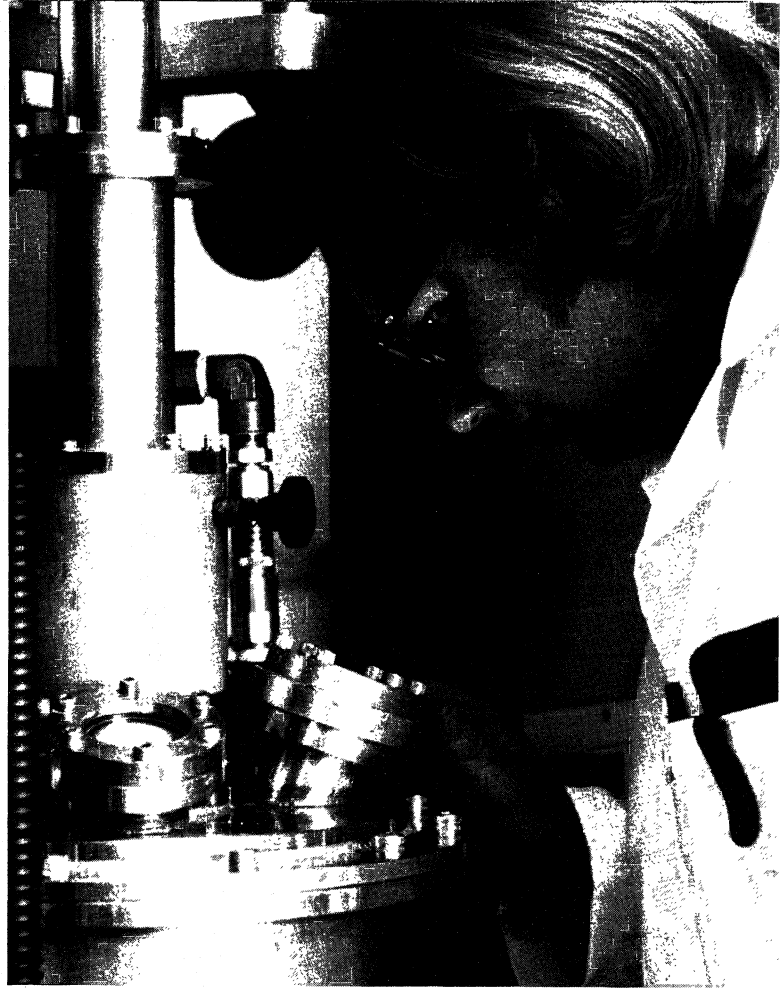
Intensive solid state research, the development of advanced manufacturing techniques and continued expansion has enabled Hewlett-Packard to become a high volume supplier of quality, competitively priced LED displays, LED lamps, optocouplers, fiber optics, and emitters/detectors.

In addition to our broad product line, Hewlett-Packard also offers the following services: immediate delivery from any of our authorized stocking distributors, applications support, special QA testing, and a one year guarantee on all of our optoelectronic products.

This package of products and services has enabled Hewlett-Packard to become a recognized leader in the optoelectronic industry.



A Brief Sketch

Hewlett-Packard is one of the world's leading designers and manufacturers of electronic, medical, analytical and computing instruments and systems, diodes, transistors, and optoelectronic products. Since its founding in Palo Alto, California, in 1939, HP has done its best to offer only products that represent significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue, and over 1,500 engineers and scientists are assigned the responsibilities of carrying out the company's various R and D projects.

HP produces more than 4,000 products at 32 domestic divisions in California, Colorado, Oregon, Idaho, Massachusetts, New Jersey and Pennsylvania and at overseas plants located in the German Federal Republic, Scotland, France, Japan, Singapore, Malaysia and Brazil.

However, for the customer, Hewlett-Packard is no further away than the nearest telephone. Hewlett-Packard currently has sales and service offices located around the world.

These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers. A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

Hewlett-Packard is guided by a set of written objectives. One of these is "to provide products and services of the greatest possible value to our customers". Through application of advanced technology, efficient manufacturing, and imaginative marketing, it is the customer that the more than 43,000 Hewlett-Packard people strive to serve. Every effort is made to anticipate the customer's needs, to provide the customer with products that will enable more efficient operation, to offer the kind of service and reliability that will merit the customer's highest confidence, and to provide all of this at a reasonable price.

To better serve its many customers' broad spectrum of technological needs, Hewlett-Packard publishes several catalogs. Among these are:

- Electronic Instruments and Systems for Measurement/Computation (General Catalog)
- DC Power Supply Catalog
- Medical Instrumentation Catalog
- Analytical Instruments for Chemistry Catalog
- Coax, and W/G Measurement Accessories Catalog
- Diode and Transistor Catalog

All catalogs are available at no charge from your local HP sales office.

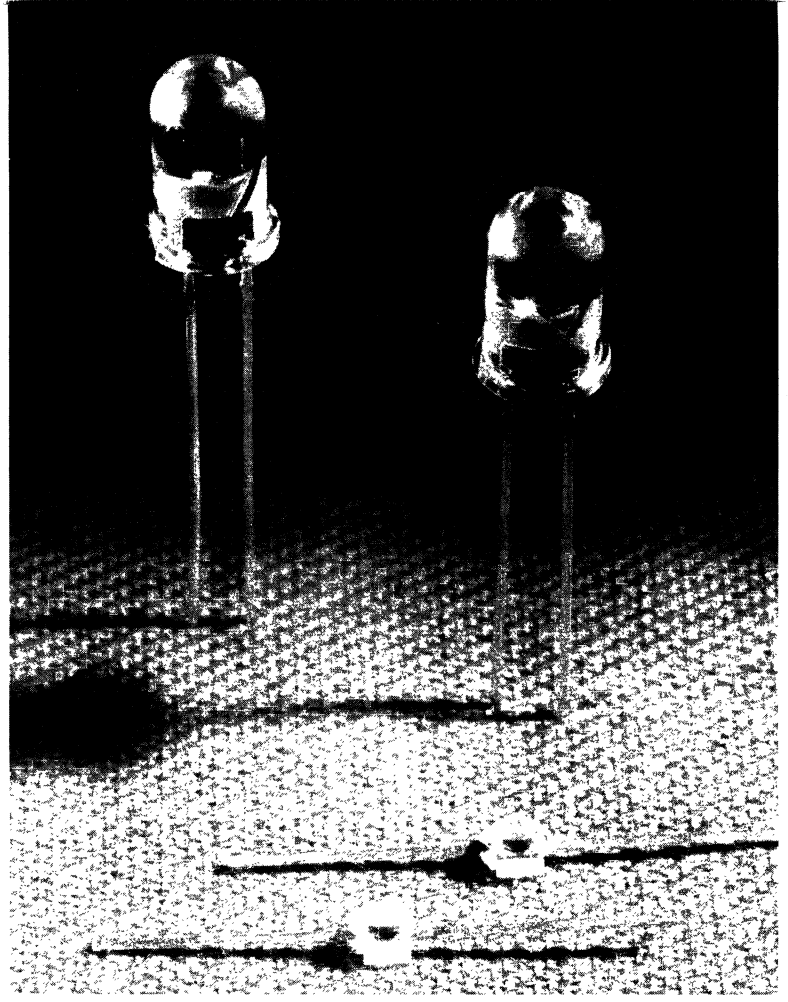
Where Reputation and Quality Count

When quality represents a competitive edge, or when the reputation and dependability of your products is on the line, you can count on Hewlett-Packard Optoelectronic components for excellent product consistency.

The optoelectronic products available include a complete line of GaAsP and GaP discrete light emitting diodes (LED's), numeric, hexadecimal, and alphanumeric displays, optocouplers, fiber optics, and emitters/detectors. For a general overview of the products available, the next seven pages will include highlights of the discrete product family groups. There is complete technical data included in this designer's catalog for each of the Hewlett-Packard Optoelectronic products.

Emitters/ Detectors

As the growing trend continues for microprocessor systems capable of high resolution-mechanical to electronic-interfaces, Hewlett-Packard addresses a genuine unfulfilled need with their new optical sensor. This small, self-contained optical reflective sensor combines a light source and detector with focused optics in a single package. This unique component can detect an object as fine as a human hair as well as the precise edge of large objects such as paper or printed lines and marks. It therefore becomes ideally suited in such applications as pattern recognition, optical limit switching, tachometry, defect detection, and bar code scanning.



This optical sensor also coupled with a clean circuit design is packaged attractively in a stylized digital bar code reading wand. The wand is designed to read black and white bar codes (it will also read most colors) on a fairly flat surface. It consists of an electro-optical emitter-detector module which produces an analog signal, followed by a current to voltage converter and then an A to D converter. The result is a computer-understandable digital electrical signal.

In addition to the complete emitter/detector system described in both the optical scanner and digital wand, Hewlett-Packard also offers the designer the choice of discrete emitter and detector components. High radiant intensity emitters near infrared in both floodlight and spotlight configurations are ideally suited for use in optical transducers and encoders, smoke detectors, and fiber optic drivers.

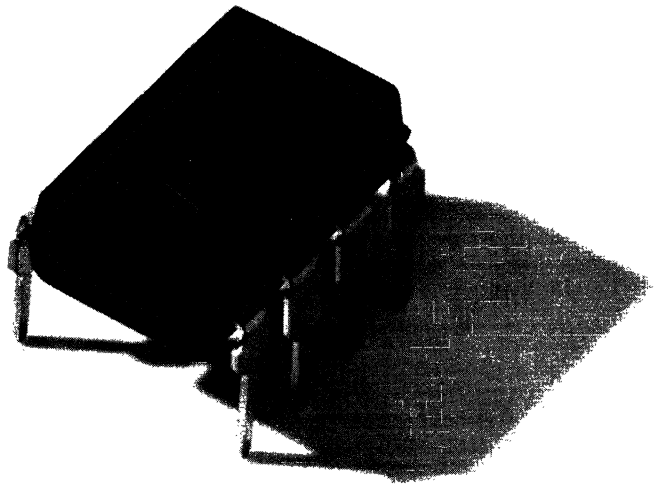
Hewlett-Packard PIN photodiodes are excellent light detectors with an exceptionally fast response of 1 ns, wide spectral response from near infrared to ultra-violet, and wide range linearity (constant efficiency over 6 decades of amplitude). With dark current as low as 250pA at 10V, these detectors are especially well-suited for operation at low light levels. The device construction allows high speed operation at reverse voltages of 5 volts. Some applications include fiber optic receivers, laser scanners, range finders, and medical diagnostic equipment. High reliability test programs are also available.

Fiber Optics

In 1978, Hewlett-Packard introduced its first complete fiber optic system. Fiber optics is one of the most exciting and fastest growing technologies in data transmission. With fiber optics, pulses of light travel down hair-thin fibers replacing electrical signals transmitted over copper wire. The light signals are impervious to electrical or magnetic interference and therefore generate no electrical or magnetic noise. This makes them ideal for linking computers or control devices and their peripherals in different environments such as those found in factories, aircraft, hospitals and large power plants.

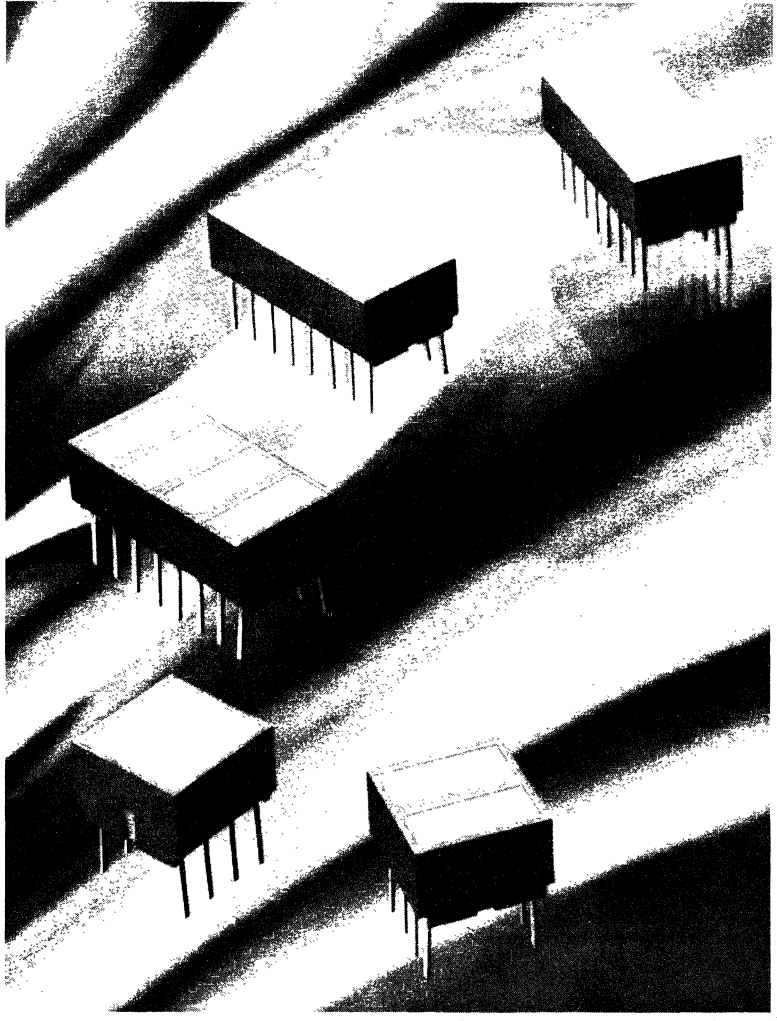
A fiber optic system consists of a transmitter, a receiver, and a length of cable encasing the hair-thin glass or plastic fiber that carries optical signals. Currently, Hewlett-Packard's fiber optic system is capable of receiving signals from distances up to 1000 metres.

The design of cost effective fiber optic systems requires the understanding and analysis of several complex technologies — optical fibers, precision connectors, LED/laser emitters, photodetectors, circuit design, packaging, and optics. Hewlett-Packard's approach to the design of fiber optic hardware is systems oriented, drawing on the broad base of technologies available within our computer, instrumentation, semiconductor components, and corporate research and development activities. State-of-the-art LED, photodetector, and integrated circuit capability are at the heart of HP's fiber optic systems. Beginning on page 26 of this catalog, you will find further details on Hewlett-Packard's fiber optic systems.



Optocouplers

Hewlett-Packard's family of optocouplers provide economical, high performance solutions to problems caused by ground loops and induced common mode noise for both analog and digital applications in commercial, industrial, and military products. Hewlett-Packard's original approach toward integrated output detectors provides performance not found in conventional phototransistor output optocouplers. With 3000 VDC isolation, the types of optocouplers available include high speed devices capable of 10M bits and high gain devices which are specified at 400% CTR at input currents as low as 0.5mA. In addition, highly linear optocouplers are useful in analog applications and a Hewlett-Packard integrated input optically coupled line receiver can be connected directly to twisted pair wires without additional circuitry. Most of these devices are available in dual versions, as well as in hermetic DIP packages. For military users, Hewlett-Packard's established hi-rel capability facilitates economical, hi-rel purchases.

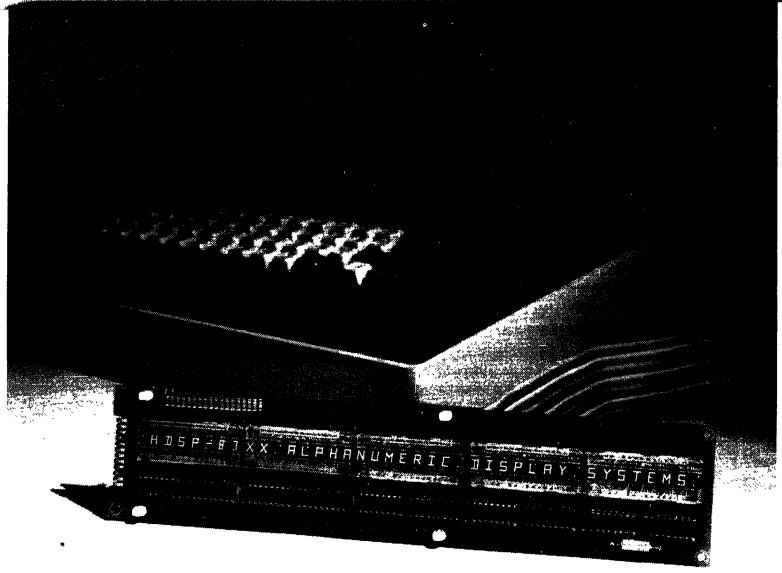


Lamps

Light Bar Modules are Hewlett-Packard's answer to the problem of how to effectively backlight legends. The Light Bar's large, uniformly illuminated surface provides a bright light source available in either high efficiency red, yellow, or green. The universal pinout arrangement allows connecting in parallel, series, or series/parallel configurations. Hewlett-Packard's LED Light Bar Modules are available in four sizes in a variety of arrangements including single, twin, and quad. They are X-Y stackable, and flush mounting is easy and convenient.

Besides the new Light Bar Modules, Hewlett-Packard LED lamps are available in a wide variety of plastic and hermetic packages to satisfy almost any application. Many styles can be mounted on a front panel using clips and all are suitable for P.C. board mounting. Hewlett-Packard military screened hermetic lamps are very popular in applications demanding high-reliability.

Products with wide or narrow viewing angles, and a range of brightnesses, are available in red, high efficiency red, yellow and green. Package styles include the traditional T-1-3/4, T-1, and TO-18 packages, as well as our own subminiature (stackable on 2.54mm (0.100 in.) centers), rectangular, and panel mountable hermetic packages.



Displays

Hewlett-Packard has expanded its selection of both alphanumeric and seven-segment numeric displays to satisfy an even broader base of applications.

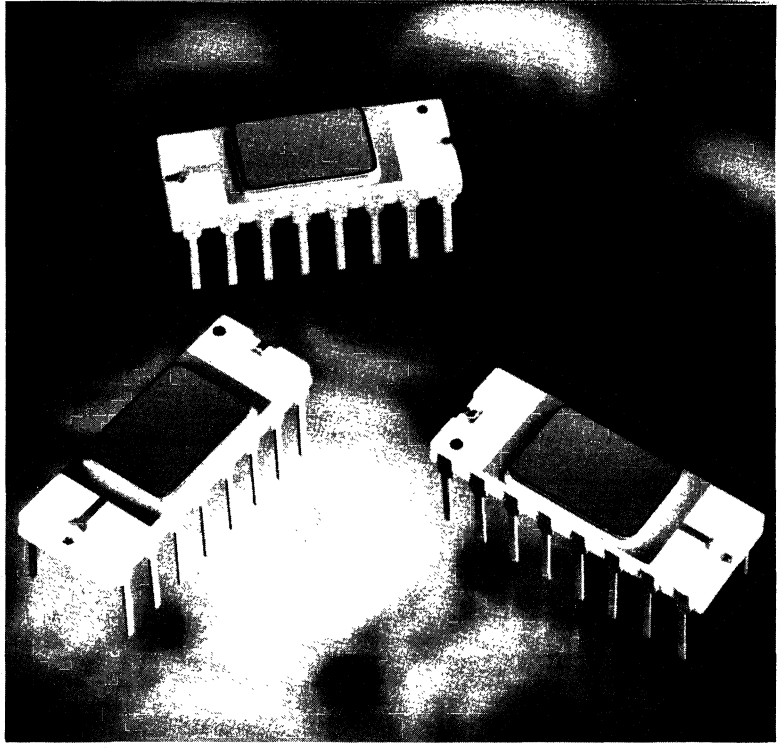
Hewlett-Packard's completely supported alphanumeric display systems allow freedom from costly display maintenance, require very low operating power, and minimize the interaction normally required for alphanumeric displays. The display systems are TTL compatible, require a single 5V supply, and easily interface to a keyboard or microprocessor. They are ideally suited for word processing equipment, instrumentation, desktop calculators, and automatic banking terminal applications.

Hewlett-Packard's yellow alphanumeric display is the answer to applications that require small size and prohibit the use of red displays. Both red and yellow alphanumeric displays feature four 5 x 7 dot matrix characters and on-board shift registers for data storage. They are contained in 16-pin DIPs which are end-stackable for unlimited possibilities in alphanumeric display formatting.

Available in four- and eight-character end-stackable modules are Hewlett-Packard's 18-segment solid state LED alphanumeric displays. Magnification of the LED by an integral lens results in a character size of 3.8mm (0.15 in.) making these displays ideal for use in computer peripheral products, automotive instrument panels, calculators, and electronic instruments and systems requiring low power consumption.

Low cost numeric displays, packaged single or clustered, are available in character heights from .11" to .8". Low power small character displays have been designed for portable instrumentation and calculator applications. Other seven-segment display units are available in red, yellow, and green colors for use in instrumentation, point of sale terminals, and TV indicator applications. High power, sun-light viewable, large character displays are readily adapted to outdoor terminals, gas pumps and agricultural instrumentation. For these displays, Hewlett-Packard has successfully integrated a gray package design with untinted segments. This results in excellent bright ambient contrast enhancement.

Integrated numeric and hexadecimal displays (with on-board IC's), available in plastic and hermetic packages, solve the designer's decoding/driving problem. These displays have been designed for low cost and ease of application in a wide range of environments.



High Reliability

Hewlett-Packard has supplied specially tested high reliability optoelectronic products since 1968 for use in state-of-the-art commercial, military, and aerospace applications. To meet the requirements of high reliability, products must be designed with rugged capabilities to withstand severe levels of environmental stress and exposure without failure. We have accomplished this objective by designing a unique family of hermetic products including lamps, displays and optocouplers which have proven their merits in numerous advanced space and defense programs to the international market place. These products receive reliability screening and qualification tests in accordance with appropriate reliability programs similar to those of MIL-S-19500 and MIL-M-38510 and are supplied as either standard JAN or JANTX devices or as HP standard light reliability units which meet our in-house TXV or TXVB programs. Reliability programs are also performed to individual customer control drawings and specifications when needed. Some of these special testing programs are very complex and may include Class S requirements for microcircuits.

HP's optoelectronic epoxy encapsulated products are designed for long life applications where non man rated or ground support requirements allow their use. As with hermetic products, the capabilities of epoxy parts can be enhanced by 100% screening and conditioning tests. Lot capabilities can be confirmed by acceptance qualification test programs.

All testing is done by experienced Hewlett-Packard employees using facilities which are either approved, or pending approval, by DESC for JAN products and by customer inspection for special programs. Environmental equipment capabilities and operating methods of the test laboratory meet MIL-STD-750 or MIL-STD-883 procedures.

About This Catalog

This Optoelectronics Designer's Catalog contains detailed, up-to-date specifications on our complete optoelectronic product line. It is divided into five major product sections: Emitters/Detectors, Fiber Optics, Optocouplers, LED Lamps, and LED Displays. A special section which includes all of the latest application notes in full-length version follows the Displays product section. Hewlett-Packard Sales and Service Offices are listed on pages 475-478 and the Hewlett-Packard Components Franchised Distributors and Representatives Directory can be found on pages 472-474.

How to Use This Catalog

Three methods are incorporated for locating components:

- a Table of Contents with tabs that allow you to locate components by their general description
- a Numeric Index that lists all components by part number and,
- a Selection Guide for each product group giving a brief overview of the product line.

How to Order

All Hewlett-Packard components may be ordered through any of the Sales and Service Offices listed on pages 475-478. In addition, for immediate delivery of Hewlett-Packard optoelectronic components, contact any of the world-wide stocking distributors and representatives listed on pages 472-474.

Warranty

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. HP will repair or, at its option, replace Components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

No other warranties are expressed or implied, including but not limited to, the implied warranties or merchantability and fitness for a particular purpose. HP is not liable for consequential damages.

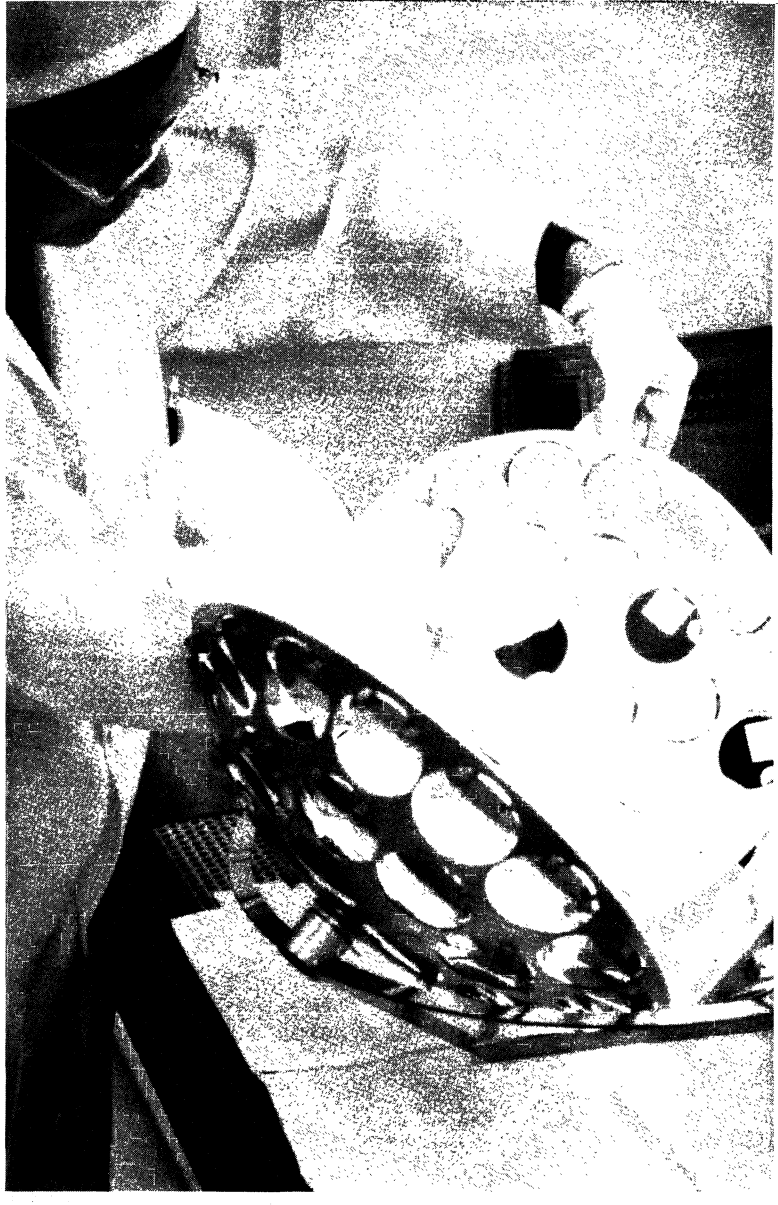
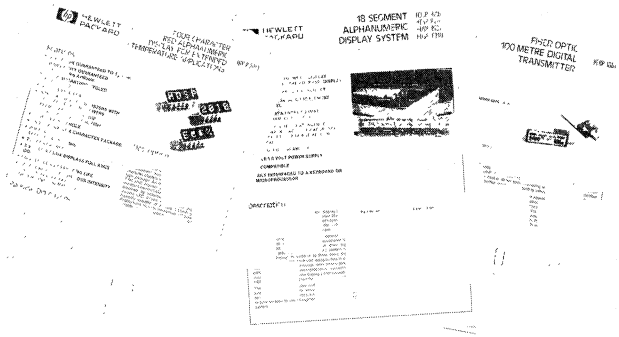


Table of Contents



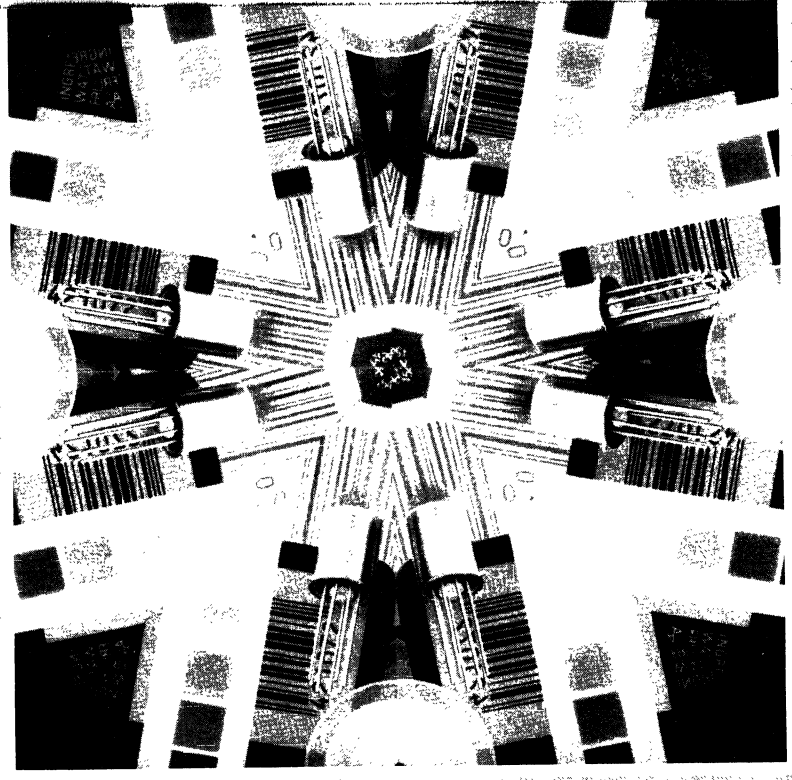
Alphanumeric Index

* New Product.

* New Product.

* New Product.

* New Product.



Emitters/Detectors

Emitter/Detector Systems

• Features	• Advantages	• Benefits
HEDS-1000 HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR		
Focused optics	Gives higher resolution	Less error No precision alignment of discrete components
Visible light source	Can detect most colors	Not limited to black & white patterns and objects
Photo IC detector	A. Faster response time	A. Can detect more transitions in less time
	B. Speed, linearity, and gain options available	B. Simplified interface electronics
Standard TO-5 package	Mounting hardware readily available	Easy to mount and use
Sealed package	Moisture resistant	Reliable operation in indoor/ outdoor environments
Detector IC operates from single ended 3.5V to 20V power supply	Compatible with all IC technologies	Easy to use
Fully integrated, assembled and tested	No precision alignment required	Easy to use Faster design-in
Performance fully specified and guaranteed	System design simplified	Assured performance
HEDS-3000 DIGITAL BAR CODE WAND		
Digital output	No analog signal conditioning circuitry needed	Microprocessor compatible
Low digitizing error	High percentage Good reads	Increased throughput
Push-to-read switch	Conserves power No strobing circuitry required	Longer battery life in portable systems
Guaranteed performance	System design simplified	Easy to use
Single supply operation	Compatible with standard digital systems	Easy to use
Lightweight stylized plastic case	Minimizes operator fatigue	Increased throughput
Custom options available	Styling to match customer's products	OEM product image enhanced

Emitters

• Features	• Advantages	• Benefits
Near IR emission	Visible	Facilitates alignment
Functions with most silicon phototransistors and photodiodes	Easy to use	Cost effective implementation
Plastic Package	Low cost	Cost effective implementation
HEMT 3300 uses isotropic LED chip	Provides floodlight type beam	Well suited for applications that require a large area to be irradiated
HEMT 6000 uses surface emitter LED chip	Provides bright spot of light	Facilitates focusing light on active area of photodetector
HEMT 6000 has offset wirebond	Active area of the chip is not masked or shadowed	Facilitates use with fiber optics

Detectors
(PIN Photodiodes)

• Features	• Advantages	• Benefits
Offset wirebond	Can be used with fiber optics	Fiber can be placed directly over active area
All HP PIN photodiodes have anti-reflective coating	Converts more incident radiation (light) into photocurrent	High Responsivity
Wide spectral response (ultraviolet through IR)	A single device can cover the light spectrum plus UV and IR	Works with a variety of sources
Low junction capacitance	Wide bandwidth	Can detect high speed pulses
ULTRA Linear	Permits operation over 10 decades	Eliminates the need for equalization

HEWLETT PACKARD

HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR

HEDS-1000

TECHNICAL DATA MARCH 1980

Features

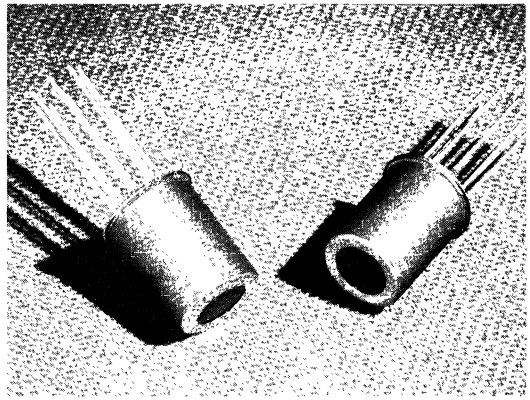
- **FOCUSED EMITTER AND DETECTOR IN A SINGLE PACKAGE**
- **HIGH RESOLUTION — .190mm SPOT SIZE**
- **700nm VISIBLE EMITTER**
- **LENS FILTERED TO REJECT AMBIENT LIGHT**
- **TO-5 MINIATURE SEALED PACKAGE**
- **PHOTODIODE AND TRANSISTOR OUTPUT**
- **SOLID STATE RELIABILITY**

Description

The HEDS-1000 is a fully integrated module designed for optical reflective sensing. The module contains a .178mm (.007 in.) diameter 700nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27mm (0.168 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

Applications include pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.

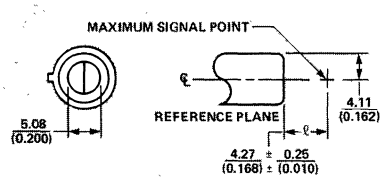


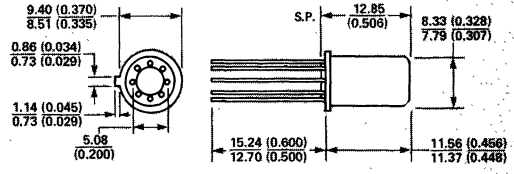
Mechanical Considerations

The HEDS-1000 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

Package Dimensions





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

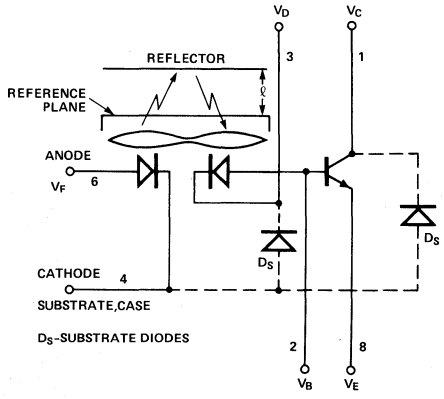
Electrical Operation

The detector section of the sensor can be connected as a single photodiode, or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 15 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

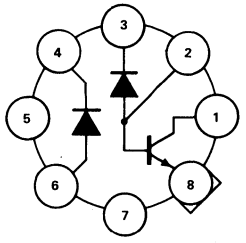
The cathode of the 700nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HEDS-1000 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

Absolute Maximum Ratings at T_A=25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D,V_C,V_E	-0.5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		5	V		

System Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent (I_{PR}+I_{PS})	I_P			375	nA	T_A=-20°C	2,3 15	4
		100	140	250		T_A=25°C, I_F=35mA, V_D=V_C=5V		
		50				T_A=70°C		
Reflected Photocurrent (I_{PR}) to Internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	6.5			I_F=35mA, V_C=V_D=5V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A=-20°C	4,5	
		100	200			T_A=25°C, V_{CE}=5V, I_C=10μA		
Slew Rate			.08		V/μs	R_L=100K I_{PK}=50mA R_F= 10M t_{ON}=100μs, Rate = 1kHz	6	
Image Diameter	d		.17		mm	I_F=35mA, ℓ=4.27mm (0.168in.)	8,10	8,9
Maximum Signal Point	ℓ	4.02	4.27	4.52	mm	Measured from Reference Plane	9	
50% Modulation Transfer Function	MTF		2.5		$I_{npr/mm}$	I_F=35mA, ℓ=4.27mm	10,11	5,7
Depth of Focus	$\frac{\Delta\ell}{FWHM}$		1.2		mm	50% of I_P at ℓ=4.27mm	9	5
Effective Numerical Aperature	N.A.		.3					
Image Location	D		.51		mm	Diameter Reference to Centerline ℓ=4.27mm		6
Thermal Resistance	Θ_{JC}		85		°C/W			

Detector Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Dark Current	I_{PD}		5	120	pA	T_A=25°C I_F=0, V_D=5V; Reflection=0%		
				10	nA	T_A=70°C		
Capacitance	C_D		45		pF	V_D=0V, I_P=0, f=1MHz		
Flux Responsivity	$R\phi$		.22		$\frac{A}{W}$	λ=700nm, V_D=5V	12	
Detector Area	A_D		.160		mm^2	Square, with Length=.4mm/Side		

Emitter Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F=35mA	13	
Reverse Breakdown Voltage	BV_R	5			V	I_R=100μA		
Radiant Flux	ϕ_E	5	9.0		μW	I_F=35mA, λ=700nm	14	
Peak Wavelength	λ_p	680	700	720	nm	I_F=35mA	14	
Thermal Resistance	Θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F=35mA		

Transistor Electrical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		pA	V_{CE}=5V		
Base-Emitter Voltage	V_{BE}		.6		V	I_C=10μA, I_B=70nA		
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$		.4		V	I_B=1μA, I_E=10μA		
Collector-Base Capacitance	C_{CB}		.3		pF	f=1MHz, V_{CB}=5V		
Base-Emitter Capacitance	C_{BE}		.4		pF	f=1MHz, V_{BE}=0V		
Thermal Resistance	Θ_{JC}		200		°C/W			

NOTES:
1. 300μs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6mA/°C.
3. Without heat sinking from T_A = 65°C, derate Maximum Average Power linearly by 12mW/°C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.27mm (0.168 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of maximum signal point image lies within a circle of diameter D relative to the center line of the package. A second emitter image (through the detector lens) is also visible. This image does not affect normal operation.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

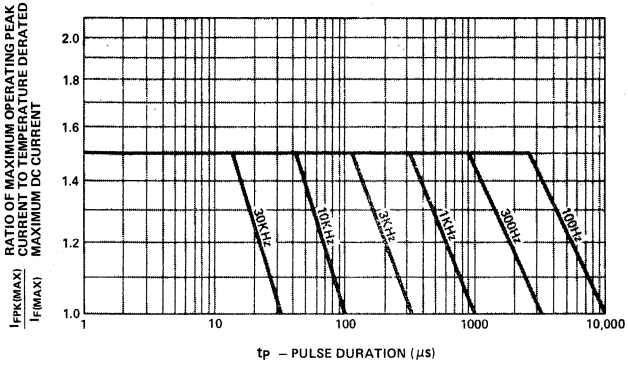


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

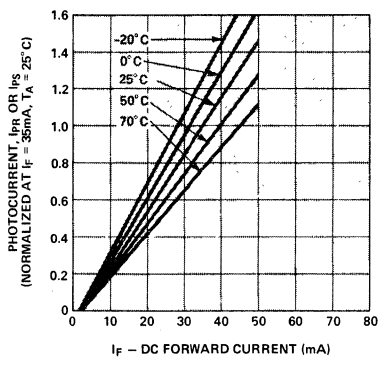


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current

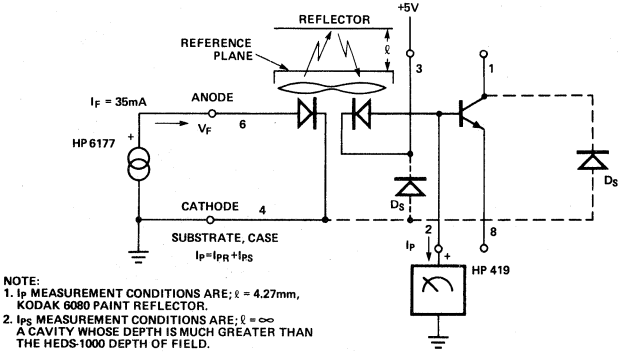


Figure 3. Ip Test Circuit

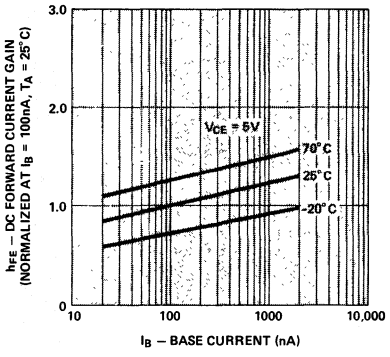


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature

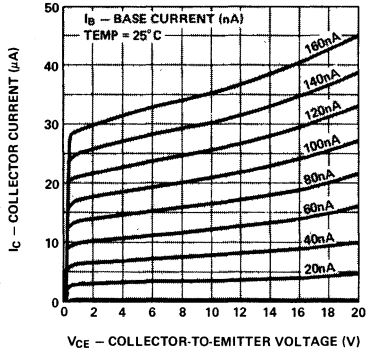


Figure 5. Common Emitter Collector Characteristics

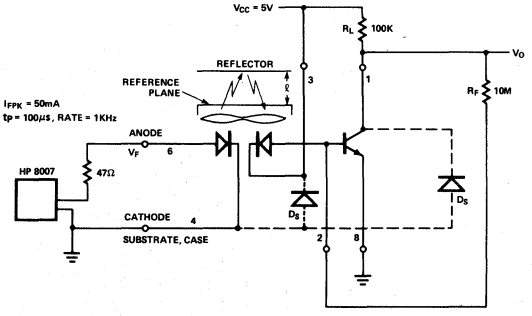


Figure 6. Slew Rate Measurement Circuit

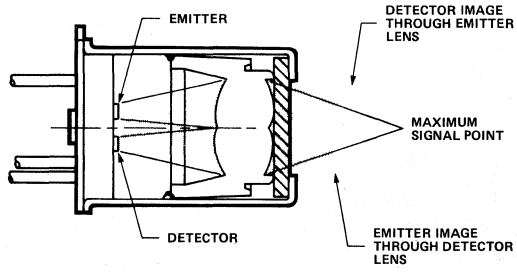


Figure 7. Image Location

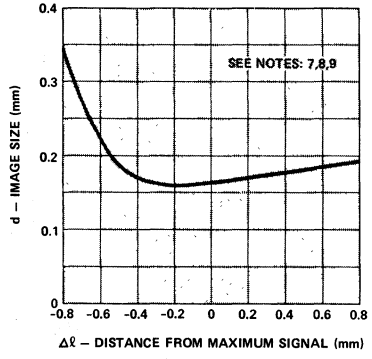


Figure 8. Image Size vs. Maximum Signal Point

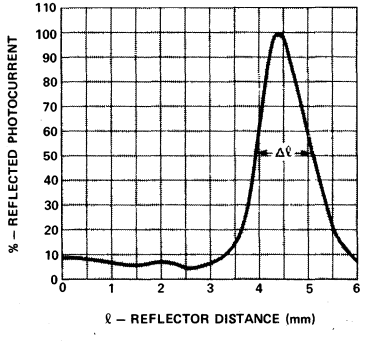


Figure 9. Reflector Distance vs. % Reflected Photocurrent

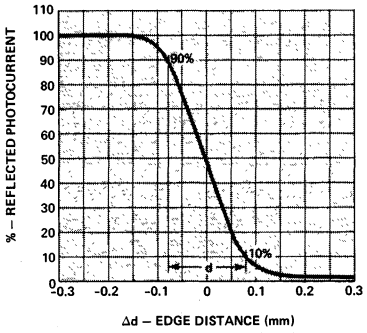


Figure 10. Step Edge Response

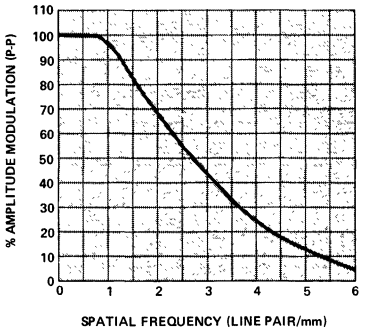


Figure 11. Modulation Transfer Function

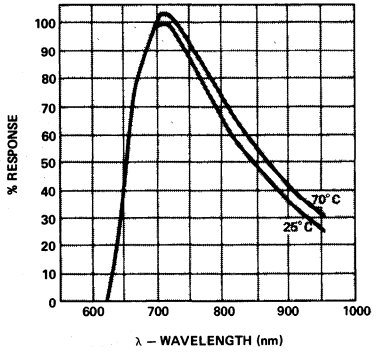


Figure 12. Detector Spectral Response

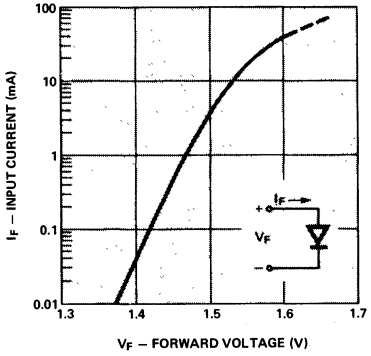


Figure 13. LED Forward Current vs. Forward Voltage Characteristics

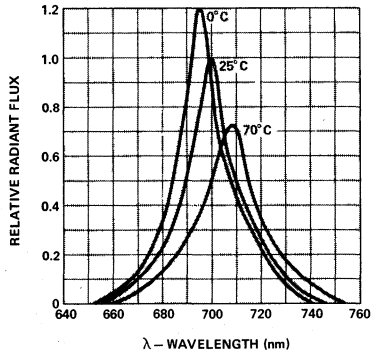


Figure 14. Relative Radiant Flux vs. Wavelength

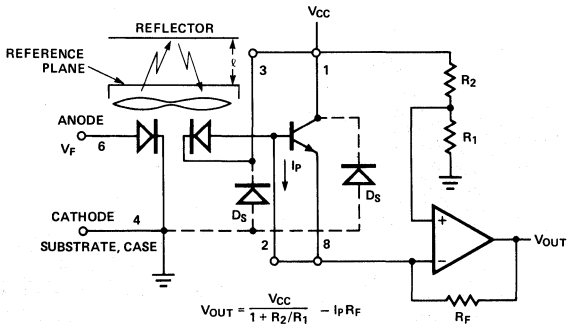


Figure 15. Photodiode Interconnection

HEWLETT PACKARD

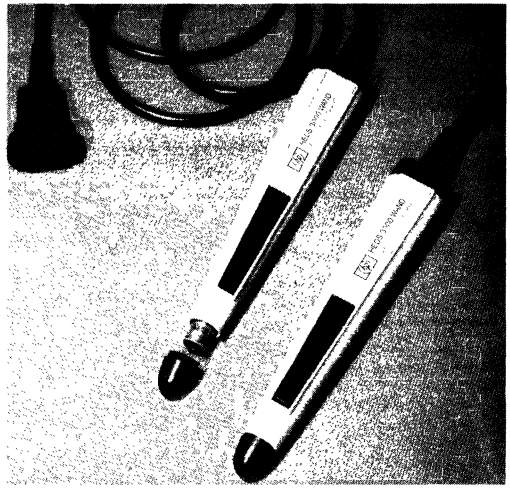
DIGITAL BAR CODE WAND

HEDS-3000

TECHNICAL DATA MARCH 1980

Features

- **0.3 mm RESOLUTION**
  Enhances the Readability of dot matrix printed bar codes
- **DIGITAL OUTPUT**
  Open Collector Output Compatible with TTL and CMOS
- **PUSH-TO-READ SWITCH**
  Wand Consumes Power Only When Switch is Depressed
- **SINGLE SUPPLY OPERATION**
- **STYLIZED CASE**
- **DURABLE LOW FRICTION TIP**
- **SOLID STATE RELIABILITY**
  Uses LED and IC Technology



Description

The HEDS-3000 Digital Bar Code Wand is a hand held scanner with integral push-to-read switch. It is designed to read all common bar code formats that have the narrowest bars printed with a nominal width of 0.3 mm (0.012 in.). The wand contains an optical sensor with a 700 nm visible light source, photo IC detector, and precision aspheric optics. Internal signal conditioning circuitry converts the optical information into a logic level pulse width representation of the bars and spaces.

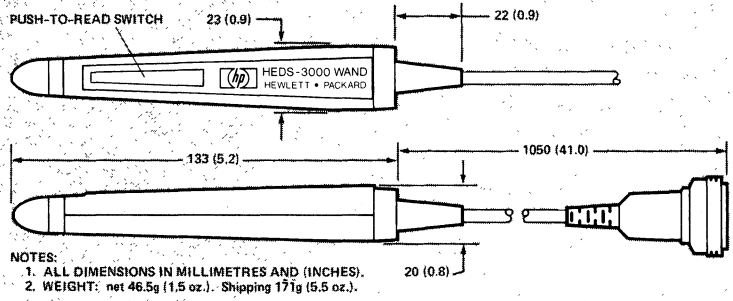
The HEDS-3000 comes equipped with a push-to-read switch which is used to activate the electronics, and strain relieved 104 cm (41 in.) cord with nine-pin subminiature D-style connector.

Applications

The Digital Bar Code Wand is an effective alternative to the keyboard when used to collect information in self-contained blocks. Bar code scanning is faster than key entry and also more accurate since most codes have check-sums built-in to prevent incorrect reads from being entered.

Applications include remote data collection, ticket identification systems, security checkpoint verification, file folder tracking, inventory control, identifying assemblies in service, repair, and manufacturing environments, and programming appliances, intelligent instruments and personal computers.

Wand Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. WEIGHT: net 46.5g (1.5 oz.). Shipping 171g (5.5 oz.).

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Bar Width	s, b	0.3		mm
Scan Velocity	V_{scan}	7.6	76	cm/s
Contrast	PCS	70		%
Supply Voltage	V_S	3.6	5.75	V
Temperature	T_A	0	55	°C
Orientation	See Figure 1			

Electrical Operation

The HEDS-3000 consists of a precision optical sensor, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single voltage supply range of 3.6V to 5.75V. A non-reflecting black bar results in a logic high (1) level, while a reflecting white space will cause a logic low (0) at the V_O connection (pin 2). The output of the HEDS-3000 is an open collector transistor.

A push-to-read switch is used to energize the 700 nm LED emitter and electronic circuitry. When the switch is initially depressed, its contact bounce may cause a series of random pulses to appear at the output, V_O. This pulse train will typically settle to a final value within 0.5 ms.

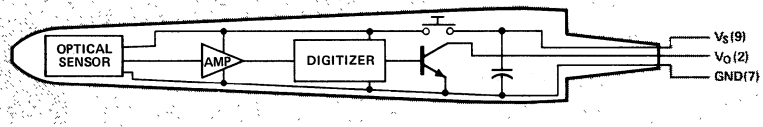
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-20	55	°C	1
Operating Temperature	T_A	0	55	°C	
Supply Voltage	V_S	-0.5	6.0	V	2
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O		20	V	

Electrical Characteristics (V_S = 3.6V to 5.75V at T_A = 25°C, R_L = 2.2kΩ, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Switch Bounce	t_{sb}		0.5	5	ms			3
High Level Output Current	I_{OH}			-400	μA	V_{OH} = 2.4V, Bar Condition (Black)	3	
Low Level Output Current	I_{OL}			16	mA	V_{OL} = 0.4V, Space Condition (White)	3	
Output Rise Time	t_r		2		μs	10%-90% Transition	3	
Output Fall Time	t_f		2		μs	90%-10% Transition	3	
Supply Current	I_S			50	mA	V_S = 5V, Bar Condition (Black)		2,4

Block Diagram



GUARANTEED WIDTH ERROR PERFORMANCE

(V_S = 5V, T_A = 0°C to 55°C, R_L = 2.2kΩ, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions		Fig.	Notes
Bar Width Error	1st	Δb_1		0.08 (3.2)	0.11 (4.5)	mm (in.x10^{-3})	T_A=25°C	Margin ≥ 5mm Height = 0.25mm Tilt = 0° v_{scan} = 50 cm/s Standard Test Tag Preferred Orientation b=s=0.3mm (0.012 in.) 2b=2s=0.6mm (0.024 in.)	1 2,6 11	5 7,8 9,10 11
				0.10 (3.8)	0.14 (5.5)		T_A = 0° to 55°C			
	Interior	Δb	-0.01 (-0.2)	0.05 (1.8)	0.09 (3.5)	mm (in.x10^{-3})	T_A=25°C		1,2 6,11	6,7 8,9 10,11
			-0.02 (-0.6)	0.05 (2.0)	0.10 (3.9)		T_A = 0° to 55°C			
Space Width Error	Interior	Δs	0.0 (0.0)	-0.05 (-1.8)	-0.09 (-3.5)	mm (in.x10^{-3})	T_A=25°C		1,2 6,11	6,7 8,10 11
			0.0 (0.0)	-0.05 (-2.0)	-0.10 (-3.9)		T_A = 0° to 55°C			
Tag Scan Velocity		v_{scan}	7.6		76	cm/s			9	7
Emitter Peak Wavelength		λ		700		nm	T_A=25°C			

TYPICAL WIDTH ERROR PERFORMANCE (V_S = 5V, T_A = 25°C, R_L = 2.2kΩ, unless otherwise noted)

Parameter	From	To	Symbol	Typical WE Tilt = 0° Height = 0.25mm	Typical WE Tilt = 30° Height = 0.0mm	Units	Conditions	Fig.	Notes
Bar Width Error	From Margin	To 1st	Δb_1	0.08 (3.2)	0.11 (4.2)	mm (in.x10^{-3})	Margin ≥ 5mm 1b=1s=0.3mm 2b=2s=0.6mm T_A=25°C V_S=5V v_{scan}=50cm/s Preferred Orientation Standard Test Tag	1,2	5,7,8
	1s	1b	Δb_{1-1}	0.03 (1.2)	0.04 (1.6)	mm (in.x10^{-3})		1,2	6,7,8
	2s	1b	Δb_{2-1}	0.06 (2.5)	0.07 (2.9)	mm (in.x10^{-3})		1,2	6,7,8
	1s	2b	Δb_{1-2}	0.02 (0.9)	0.02 (0.7)	mm (in.x10^{-3})		1,2	6,7,8
	2s	2b	Δb_{2-2}	0.05 (1.9)	0.05 (2.1)	mm (in.x10^{-3})		1,2	6,7,8
Space Width Error	1b	1s	Δs_{1-1}	-0.04 (-1.4)	-0.04 (-1.4)	mm (in.x10^{-3})		1,2	6,7,8
	2b	1s	Δs_{2-1}	-0.03 (-1.0)	-0.03 (-1.1)	mm (in.x10^{-3})		1,2	6,7,8
	1b	2s	Δs_{1-2}	-0.07 (-2.7)	-0.08 (-3.3)	mm (in.x10^{-3})		1,2	6,7,8
	2b	2s	Δs_{2-2}	-0.06 (-2.4)	-0.06 (-2.4)	mm (in.x10^{-3})		1,2	6,7,8

Notes:
1. Storage Temperature is dictated by Wand case.
2. Power supply ripple and noise should be less than 100 mV.
3. Switch bounce causes a series of sub-millisecond pulses to appear at the output, V_O.
4. Push-to-Read switch is depressed, and the Wand is placed on a non-reflecting (black) surface.
5. The margin refers to the reflecting (white) space that preceeds the first bar of the bar code.
6. The interior bars and spaces are those which follow the first bar of bar code tag.
7. The standard test tag consists of black bars, white spaces (0.3 mm, 0.012 in. min.) photographed on Kodagraph Transtar TC5® paper with a print contrast signal greater than 0.9.
8. The print contrast signal (PCS) is defined as: PCS = (R_W - R_b) /R_W, where R_W is the reflectance at 700 nm from the white spaces, and R_b is the reflectance at 700 nm for the bars.
9. 1.0 in. = 25.4 mm, 1 mm = 0.0394 in.
10. The Wand is in the preferred orientation when the surface of the switch button is parallel to the height dimension of the bar code.

OPERATION CONSIDERATIONS

The HEDS-3000 resolution is specified in terms of a bar and space Width Error, WE. The width error is defined as the difference between the calculated bar (space) width, B, (S), and the optically measured bar (space) widths, b (s). When a constant scan velocity is used, the width error can be calculated from the following:

$B = t_b \cdot v_{scan}$

$S = t_s \cdot v_{scan}$

$\Delta b = B - b$

$\Delta s = S - s$

Where

Δb, Δs= bar, space Width Error (mm)

b, s = optical bar, space width (mm)

B, S = calculated bar, space width (mm)

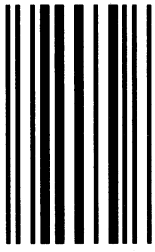
v_{scan} = scan velocity (mm/s)

t_b, t_s = wand pulse width output(s)

The magnitude of the width error is dependent upon the width of the bar (space) preceeding the space (bar) being measured. The Guaranteed Width Errors are specified as a maximum for the margin to first bar transition, as well as, maximums and minimums for the bar and space width errors resulting from transitions internal to the body of the bar code character. The Typical Width Error Performance specifies all possible transitions in a two level code (e.g. 2 of 5). For example, the $\Delta b_{2\to1}$ Width Error specifies the width error of a single bar module (0.3 mm) when preceeded by a double space module (0.6 mm).

The Bar Width Error Δb, typically has a positive polarity which causes the calculated bar, B, to appear wider than its printed counterpart. The typical negative polarity of the Space Width Error Δs, causes the measured spaces to appear narrower. The consistency of the polarity of the bar and space Width Errors suggest decoding schemes which average the measured bars and measured spaces within a character. These techniques will produce a higher percentage of good reads.

The Wand will respond to a bar code with a nominal module width of 0.3 mm when it is scanned at tilt angles between 0° and 30°. The optimum performance will be obtained when the Wand is held in the preferred orientation (Figure 1), tilted at an angle of 10° to 20°, and the Wand tip is in contact with the tag. The Wand height, when held normal to the tag, is measured from the tip's aperture, and when it is tilted it is measured from the tip's surface closest to the tag. The Width Error is specified for the preferred orientation, and using a Standard Test Tag consisting of black bars and white spaces. Figure 2 illustrates the random two level bar code tag. The Standard Test Tag is photographed on Kodagraph Transtar TC5® paper with a nominal module width of 0.3 mm (0.012 in.) and a Print Contrast Signal (PCS) of greater than 90%.



BAR WIDTH 0.3 mm (0.012 in.) BLACK & WHITE

$R_{WHITE} \geq 75\%$, PCS $\geq$ 0.9 KODAGRAPH TRANSTAR TC5® PAPER

Figure 2. Standard Test Tag Format.

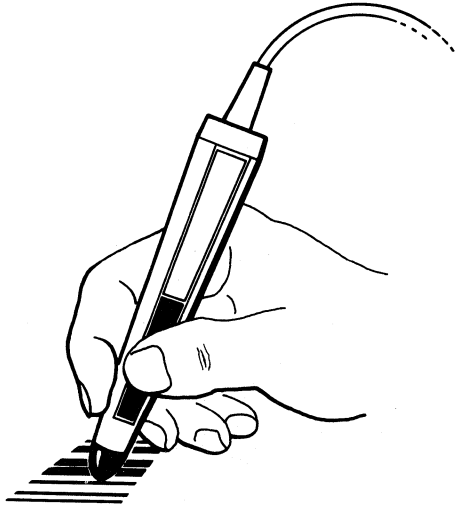


Figure 1. Preferred Wand Orientation.

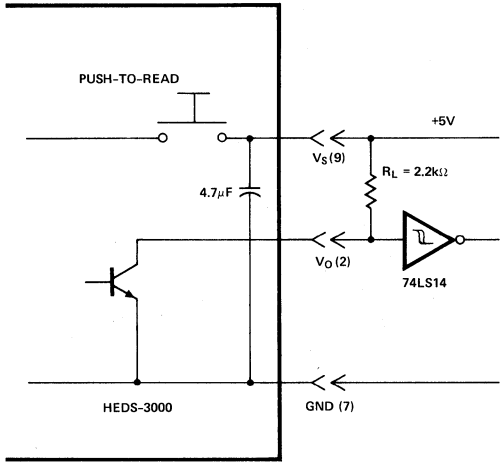


Figure 3. Recommended Logic Interface.

Typical Performance Curves (R_L = 2.2kΩ)

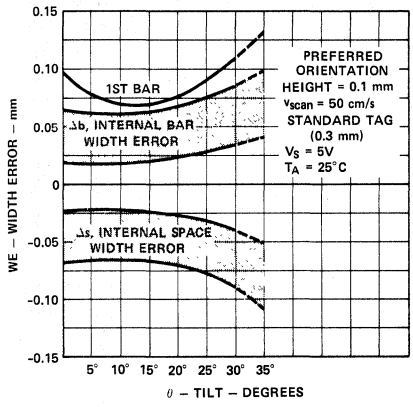


Figure 4. Width Error vs. Tilt (Preferred Orientation).

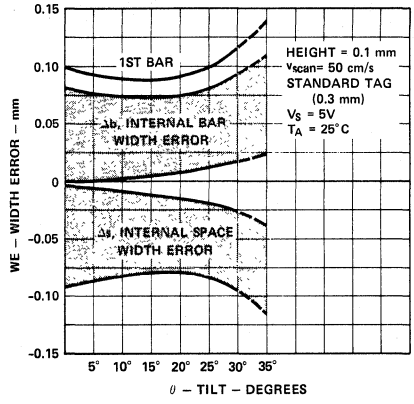


Figure 5. Width Error vs. Tilt (Any Orientation).

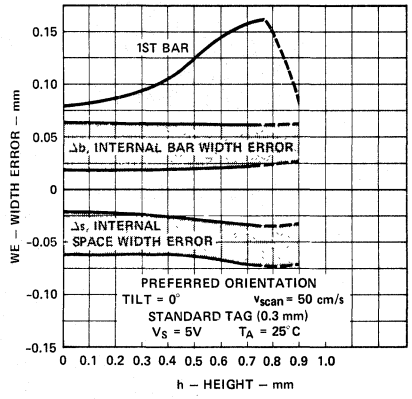


Figure 6. Width Error vs. Height (Preferred Orientation).

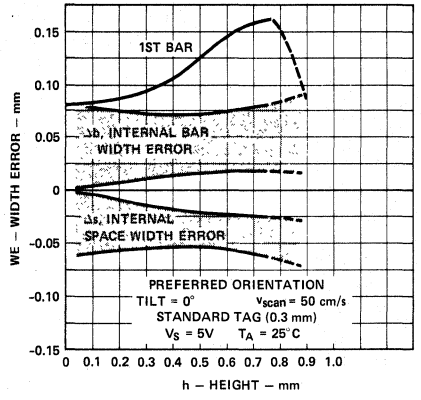


Figure 7. Width Error vs. Height (Any Orientation).

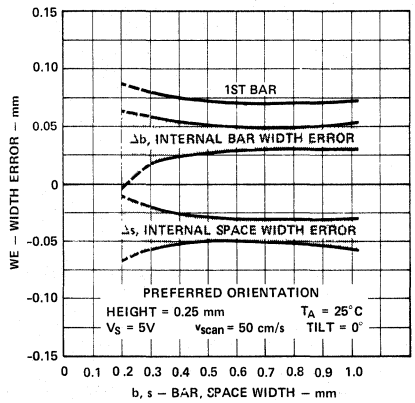


Figure 8. Width Error vs. Bar Width.

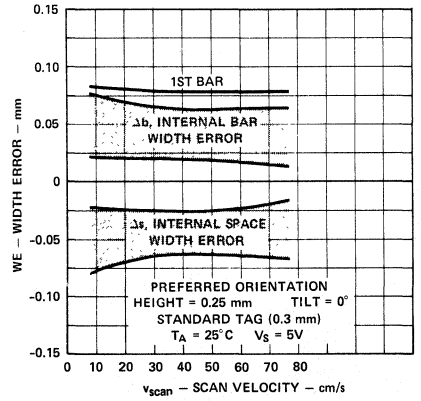


Figure 9. Width Error vs. Scan Velocity.

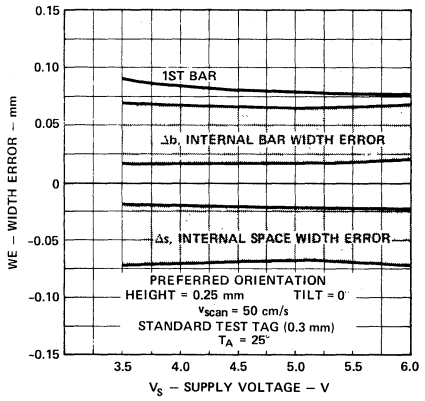


Figure 10. Width Error vs. Supply Voltage.

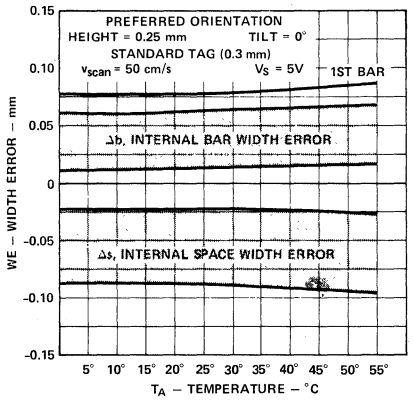


Figure 11. Width Error vs. Temperature.

MECHANICAL CONSIDERATIONS

The HEDS-3000 includes a standard nine pin D-style connector with integral squeeze-to-release retention mechanism. Two types of receptacles compatible with the retention mechanism are available from AMP Corp. (Printed circuit header: 745001-2 Panel mount: 745018, body; 66570-3, pins). Panel mount connectors that are compatible with the HEDS-3000 connector, but do not include the retention mechanism, are the Molex A7224, and AMP 2074-56-2.

MAINTENANCE CONSIDERATIONS

While there are no user serviceable parts inside the Wand, the tip should be checked periodically for wear and dirt, or obstructions in the aperture. The tip aperture is designed to reject particles and dirt but a gradual degradation in performance will occur as the tip wears down, or becomes obstructed by foreign materiais.

Before unscrewing the tip, disconnect the Wand from the system power source. The aperture can be cleaned with a cotton swab or similar device and a liquid detergent.

The glass window on the sensor should be inspected and cleaned if dust, dirt, or fingerprints are visible. To clean the sensor window dampen a lint free cloth with a liquid cleaner, then clean the window with the cloth taking care not to disturb the orientation of the sensor. DO NOT SPRAY CLEANER DIRECTLY ON THE SENSOR OR WAND.

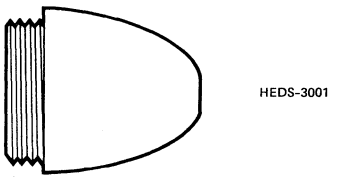


Figure 12. Wand Tip.

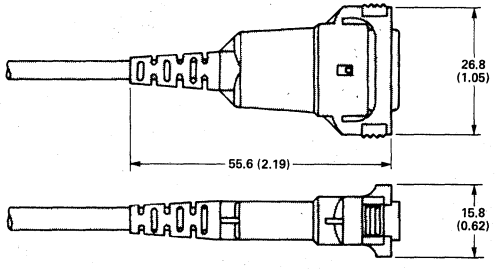
After cleaning the tip aperture and sensor window, the tip should be gently and securely screwed back into the Wand assembly. The tip should be replaced if there are visible indications of wear such as a disfigured, or distorted aperture. The part number for the Wand tip is HEDS-3001. It can be ordered from any Hewlett-Packard parts center or franchised Hewlett-Packard distributor.

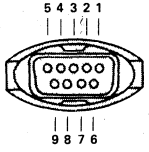
OPTIONAL FEATURES

The wand may also be ordered with the following special features:

- 193 color options
- Customer specified label
- No label
- Heavy duty retractable coiled cord
- No connector
- No switch button

For more information, call your local Hewlett-Packard sales office or franchised distributor.





PIN	FUNCTION
1	NC
2	V_O OUTPUT
3	NC
4	NC
5	NC
6	NC
7	GROUND
8	NC
9	V_S SUPPLY VOLTAGE

Figure 13. Connector Specifications.

HEWLETT PACKARD

670nm HIGH RADIANT INTENSITY EMITTER

HEMT-3300

TECHNICAL DATA MARCH 1980

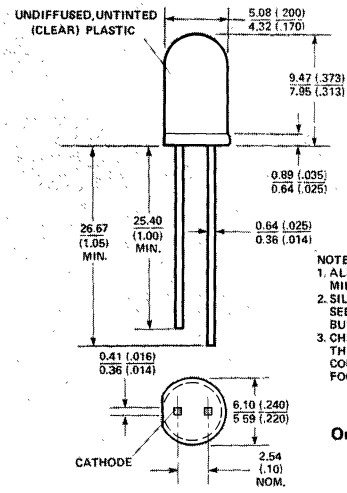
Features

- **HIGH EFFICIENCY**
- **NONSATURATING OUTPUT**
- **NARROW BEAM ANGLE**
- **VISIBLE FLUX AIDS ALIGNMENT**
- **BANDWIDTH: DC TO 3 MHz**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENT**

Description

The HEMT-3300 is a visible, near-IR, source using a GaAsP on GaP LED chip optimized for maximum quantum efficiency at 670 nm. The emitter's beam is sufficiently narrow to minimize stray flux problems, yet broad enough to simplify optical alignment. This product is suitable for use in consumer and industrial applications such as optical transducers and encoders, smoke detectors, assembly line monitors, small parts counters, paper tape readers and fiber optic drivers.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS SEE APPLICATION BULLETIN 3.
3. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Outline T - 1¾

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Figure
I_e	Axial Radiant Intensity	200	500		$\mu W/sr$	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.009		$°C^{-1}$	I_F = 10 mA, Note 1	
η_v	Luminous Efficacy		22		lm/W	Note 2	
$2\Theta_{½}$	Half Intensity Total Angle		22		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength		670		nm	Measured at Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		0.089		nm/°C	Measured at Peak, Note 4	
t_r	Output Rise Time (10% – 90%)		120		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90% – 10%)		50		ns	I_{PEAK} = 10 mA Pulse	
C_O	Capacitance		15		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5.0			V	I_R = 100 μA	
V_F	Forward Voltage		1.9	2.5	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.2		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		160		°C/W	Junction to cathode lead at seating plane.	

Notes: 1. I_e (T) = I_e (25°C)exp [K_e(T – 25°C)] 2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian and η_v in lumen/watt.
3. $\Theta_{½}$ is the off-axis angle at which the radiant intensity is half the axial intensity. The deviation between the mechanical and optical axis is typically within a conical half-angle of five degrees. 4. λ_{PEAK} (T) = λ_{PEAK} (25°C) + ($\Delta\lambda_{PEAK}/\Delta T$) (T – 25°C).

Maximum Ratings at T_A=25°C

Power Dissipation ..... 120 mW
(derate linearly from 50°C at 1.6 mW/°C)
Average Forward Current ..... 30 mA
(derate linearly from 50°C at 0.4 mA/°C)
Peak Forward Current ..... See Figure 5
Operating and Storage
Temperature Range ..... -55°C to +100°C
Lead Soldering Temperature ..... 260°C for 5 sec.
(1.6 mm [0.063 inch] from body)

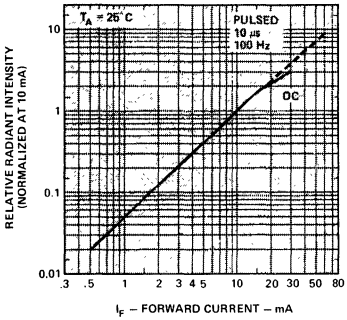


Figure 3. Relative Radiant Intensity versus Forward Current.

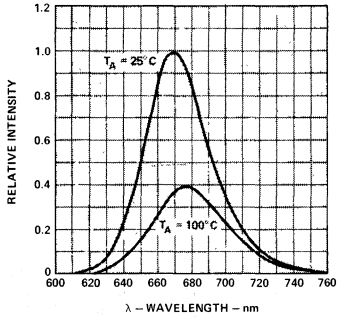


Figure 1. Relative Intensity versus Wavelength.

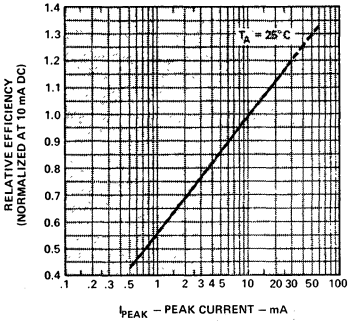


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

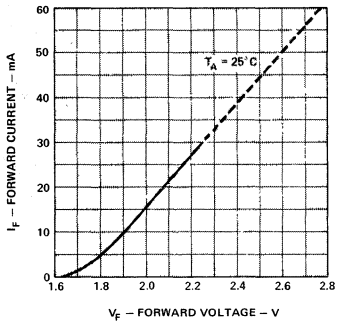


Figure 2. Forward Current versus Forward Voltage.

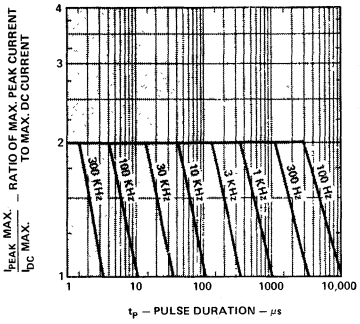


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

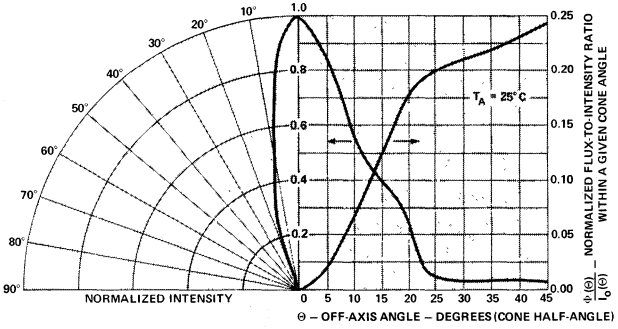


Figure 6. Far-Field Radiation Pattern.

HEWLETT PACKARD

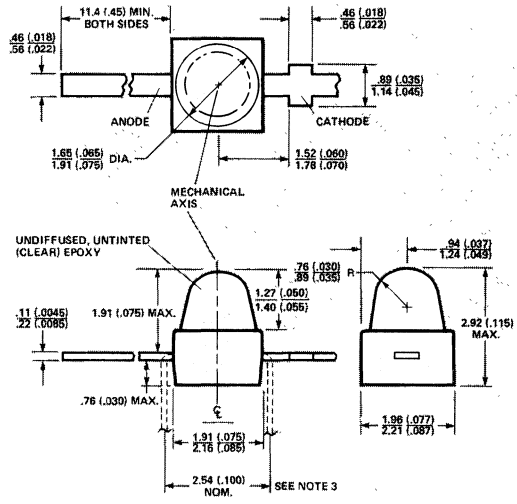
700nm HIGH INTENSITY SUBMINIATURE EMITTER

HEMT-6000

TECHNICAL DATA MARCH 1980

Features

- **HIGH RADIANT INTENSITY**
- **NARROW BEAM ANGLE**
- **NONSATURATING OUTPUT**
- **BANDWIDTH: DC TO 5 MHz**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENT**
- **VISIBLE FLUX AIDS ALIGNMENT**



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.
4. EPOXY ENCAPSULANT HAS A REFRACTIVE INDEX OF 1.53.
5. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Description

The HEMT-6000 uses a GaAsP chip designed for optimum tradeoff between speed and quantum efficiency. This optimization allows a flat modulation bandwidth of 5 MHz without peaking, yet provides a radiant flux level comparable to that of 900nm IREDs. The subminiature package allows operation of multiple closely-spaced channels, while the narrow beam angle minimizes crosstalk. The nominal 700nm wavelength can offer spectral performance advantages over 900nm IREDs, and is sufficiently visible to aid optical alignment. Applications include paper-tape readers, punch-card readers, bar code scanners, optical encoders or transducers, interrupt modules, safety interlocks, tape loop stabilizers and fiber optic drivers.

Maximum Ratings at $T_A = 25°C$

Power Dissipation ..... 50 mW
(derate linearly from 70°C @ 1.0mW/°C)

Average Forward Current ..... 20 mA
(derate linearly from 70°C @ 0.4mA/°C)

Peak Forward Current ..... See Figure 5

Operating and Storage Temperature Range ..... -55° to +100°C

Lead Soldering Temperature ..... 260°C for 5 sec.
[1.6 mm (0.063 in.) from body]

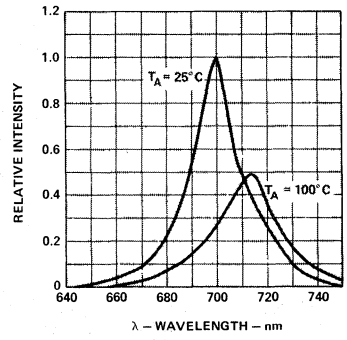


Figure 1. Relative Intensity versus Wavelength.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Fig.
I_e	Radiant Intensity along Mechanical Axis	100	250		μW/sr	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.005		°C^{-1}	Note 1	
η_v	Luminous Efficacy		2.5		lm/W	Note 2	
$2\Theta_{1/2}$	Optical Axis Half Intensity Total Angle		16		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength (Range)		690-715		nm	Measured @ Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		.193		nm/°C	Measured @ Peak, Note 4	
t_r	Output Rise Time (10%-90%)		70		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90%-10%)		40		ns	I_{PEAK} = 10 mA	
C_o	Capacitance		65		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5	12		V	I_R = 100 μA	
V_F	Forward Voltage		1.5	1.8	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.1		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		140		°C/W	Junction to cathode lead at 0.79 mm (.031 in) from body	

NOTES:
1. $I_e(T) = I_e\ (25°C)\ \exp\ [K_e\ (T - 25°C)]$.
2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian, and η_v in lumen/watt.
3. $\Theta_{1/2}$ is the off-axis angle at which the radiant intensity is half the intensity along the optical axis. The deviation between the mechanical and the optical axis is typically within a conical half-angle of three degrees.
4. $\lambda_{PEAK}\ (T) = \lambda_{PEAK}\ (25°C) + (\Delta\lambda_{PEAK}/\Delta T)\ (T - 25°C)$

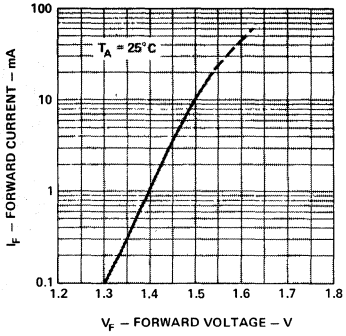


Figure 2. Forward Current versus Forward Voltage.

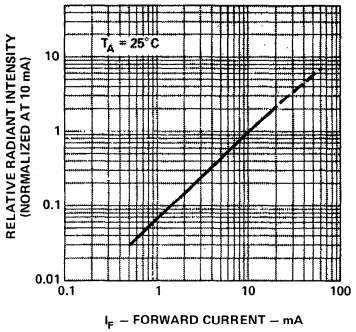


Figure 3. Relative Radiant Intensity versus Forward Current.

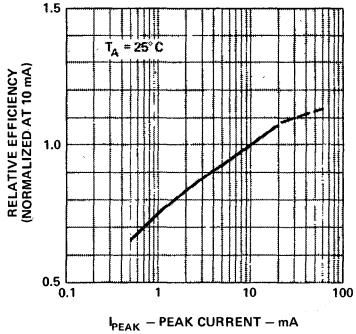


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

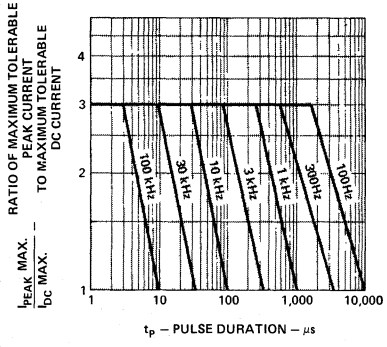


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

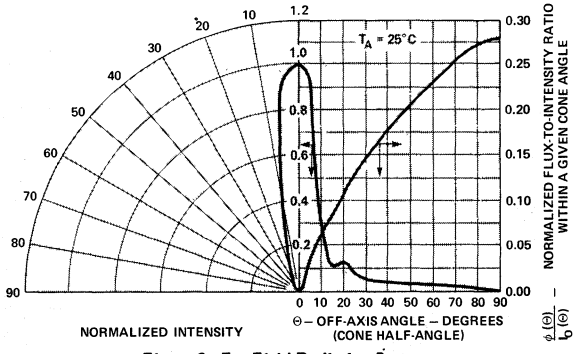


Figure 6. Far-Field Radiation Pattern.

HEWLETT PACKARD

PIN PHOTODIODES

5082-4200 SERIES

TECHNICAL DATA MARCH 1980

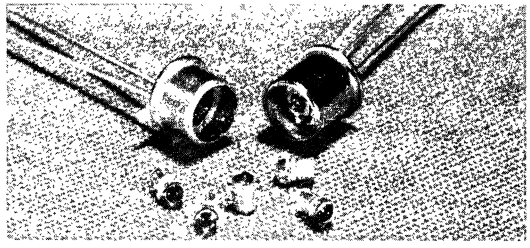
Features

- **HIGH SENSITIVITY (NEP<-108 dBm)**
- **WIDE DYNAMIC RANGE (1% LINEARITY OVER 100 dB)**
- **BROAD SPECTRAL RESPONSE**
- **HIGH SPEED (T_r, T_f<1ns)**
- **STABILITY SUITABLE FOR PHOTOMETRY/ RADIOMETRY**
- **HIGH RELIABILITY**
- **FLOATING, SHIELDED CONSTRUCTION**
- **LOW CAPACITANCE**
- **LOW NOISE**

Active area: 1mm Diam — 5082-4207, 5082-4203, 5082-4204 — **TALL SIZE (TO-18)**

0.5mm Diam — 5082-4204 — **Short (TO-46)**

0.25mm Magnified 2.5x — 5082-4205 — **Subminiature**



Description

The HP silicon planar PIN photodiodes are ultra-fast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

These devices are suitable for applications such as high speed tachometry, optical distance measurement, star tracking, densitometry, radiometry, and fiber-optic termination.

The speed of response of these detectors is less than one nanosecond. Laser pulses shorter than 0.1 nanosecond may be observed. The frequency response extends from dc to 1 GHz.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over ten decades of light intensity, providing a wide dynamic range.

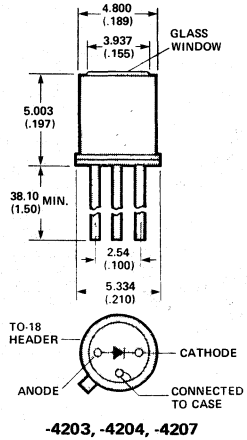
The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a flat glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitve area of the 5082-4203 and -4204 is 0.508mm (0.020 inch) in diameter and is located 1.905mm (0.075 inch) behind the window. The light sensitive area of the 5082-4207 is 1.016mm (0.040 inch) in diameter and is also located 1.905mm (0.075 inch) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical glass lens.

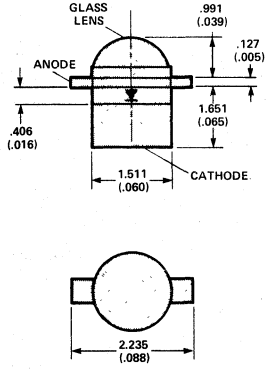
The 5082-4220 is packaged on a TO-46 header with the 0.508mm(0.020 inch) diameter sensitive area located 2.540mm (0.100 inch) behind a flat glass window.

Package Dimensions

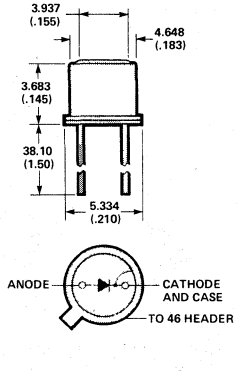
DIMENSIONS IN MILLIMETRES (INCHES)



-4203, -4204, -4207



-4205



-4220

Absolute Maximum Ratings Operating and Storage Temperature -55° to 125°C

Parameter	-4203	-4204	-4205	-4207	-4220	Units
P_{MAX} Power Dissipation 1	100	100	50	100	100	mW
Steady Reverse Voltage3	50	20	50	20	50	volts

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	-4203			-4204			-4205			-4207			-4220			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
R_E, 0= R_ϕ * A	Axial Incidance Response at 770nm[4]		1.0			1.0			1.5*			4.0			1.0		$\frac{\mu A}{mW/cm^2}$[2]
A	Active Area4		2 x 10^{-3}			2 x 10^{-3}			3 x 10^{-3}*			8 x 10^{-3}			2 x 10^{-3}		cm^2[2]
R_ϕ	Flux Responsivity 770 nm5 (Fig. 1, 3)		.5			.5			.5			.5			.5		$\frac{\mu A}{\mu W}$
I_D	Dark Current6 (Fig. 4)			2.0			0.6			.15			2.5			5.0	nA
NEP	Noise Equivalent Power 7 (Fig. 8)			5.1 x 10^{-14}			2.8 x 10^{-14}			1.4 x 10^{-14}			5.7 x 10^{-14}			8.1 x 10^{-14}	$\frac{W}{\sqrt{Hz}}$
D*	Detectivity8	8.7 x 10^{11}			1.6 x 10^{12}			4.0x* 10^{12}			1.5 x 10^{12}			5.6 x 10^{11}			$\frac{cm\sqrt{Hz}}{W}$
C_j	Junction Capacitance9 (Fig. 5)		1.5			2.0			0.7			5.5			2.0		pF
C_P	Package Capacitance 10		2			2						2					pF
t_r, t_f	Zero Bias Speed (Rise, Fall Time) 11		300			300			300			300			300		ns
t_r, t_f	Rev.-Bias Speed (Rise, Fall Time) 12			1			1			1			1			1	ns
R_S	Series Resistance			50			50			50			50			50	Ω

*see Note 4.

NOTES:

1. Peak Pulse Power

   When exposing the diode to high level incidance the following photocurrent limits must be observed:

   $$I_p \text{ (avg MAX.)} < \frac{P_{MAX} - P_\phi}{E_c}$$; and in addition:

   $$I_{p(PEAK)} < \frac{1000\ A}{t\ (\mu sec)}$$ or <500mA or $< \frac{I_p \text{ (avg MAX.)}}{f \times t}$

   whichever of the above three conditions is least.

   I_p - photocurrent (A) f - pulse repetion rate (MHz)
   E_c - supply voltage (V) P_ϕ - power input via photon flux
   t - pulse duration (μs) P_{MAX} - max dissipation (W)

   Power dissipation limits apply to the sum of both the optical power input to the device and the electrical power input from flow of photocurrent when reverse voltage is applied.
2. Exceeding the Peak Reverse Voltage will cause permanent damage to the diode. Forward current is harmless to the diode, within the power dissipation limit. For optimum performance, the diode should be reversed biased with E_c between 5 and 20 volts.
3. Exceeding the Steady Reverse Voltage may impair the low-noise properties of the photodiodes, an effect which is noticeable only if operation is diode-noise limited (see Figure 8).
4. The 5082-4205 has a lens with approximately 2.5x magnification; the actual junction area is 0.5 x 10^{-3} cm^2, corresponding to a diameter of 0.25mm (.010"). Specification includes lens effect.
5. At any particular wavelength and for the flux in a small spot falling entirely within the active area, responsivity is the ratio of incremental photodiode current to the incremental flux producing it. It is related to quantum efficiency, η_q in electrons per photon by:

   $$R_\phi = \eta_q \left(\frac{\lambda}{1240}\right)$$

   where λ is the wavelength in nanometers. Thus, at 770nm, a responsivity of 0.5 A/W corresponds to a quantum efficiency of 0.81 (or 81%) electrons per photon.
6. At -10V for the 5082-4204, -4205, and -4207; at -25V for the 5082-4203 and -4220.
7. For (λ, f, Δf) = (770nm, 100Hz, 6Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/noise ratio normalized for bandwidth. Thus:

   $$NEP = \frac{I_N/\sqrt{\Delta f}}{R_\phi}$$ where $I_N/\sqrt{\Delta f}$ is the bandwidth — normalized noise current computed from the shot noise formula:

   $I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15} \sqrt{I_D}$ ($A/\sqrt{Hz}$) where I_D is in nA.
8. Detectivity, D*is the active-area-normalized signal to noise ratio. It is computed: for (λ, f, Δf) = (770nm, 100Hz, 6Hz).

   $$D^* = \frac{\sqrt{A}}{NEP} \left(\frac{cm\sqrt{Hz}}{W}\right)$$ for A in cm^2,
9. At -10V for 5082-4204, -4205, -4207, -4220; at -25V for 5082-4203.
10. Between diode cathode lead and case — does not apply to 5082-4205, -4220.
11. With 50Ω load.
12. With 50Ω load and -20V bias.

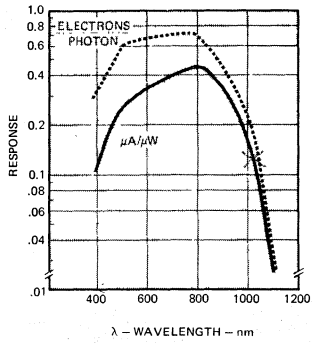


Figure 1. Spectral Response.

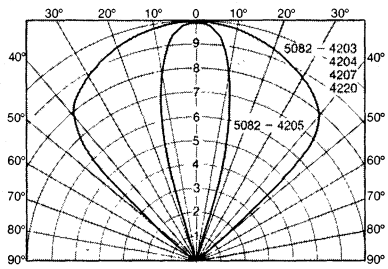


Figure 2. Relative Directional Sensitivity of the PIN Photodiodes.

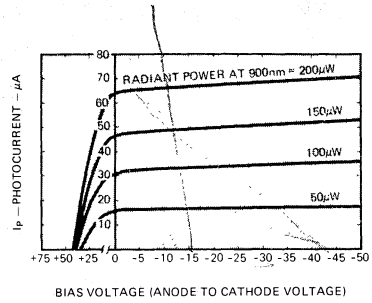


Figure 3. Typical Output Characteristics at λ = 900nm.

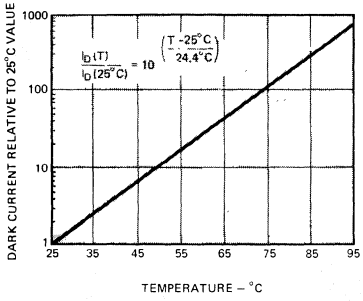


Figure 4. Dark Current at -10V Bias vs. Temperature.

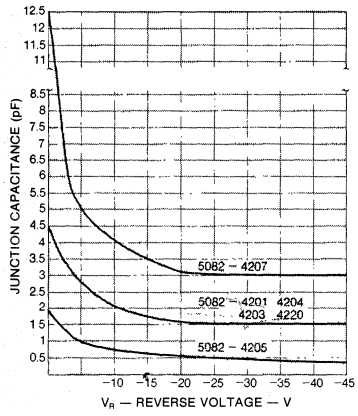


Figure 5. Typical Capacitance Variation With Applied Voltage.

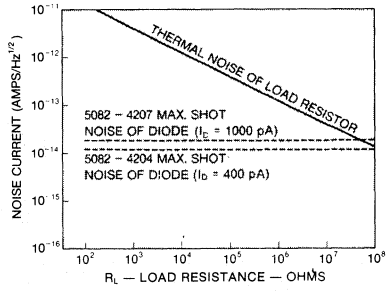


Figure 6. Noise vs. Load Resistance.

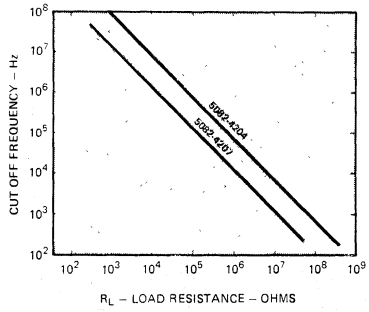


Figure 7. Photodiode Cut-Off Frequency vs. Load Resistance (C = 2pF).

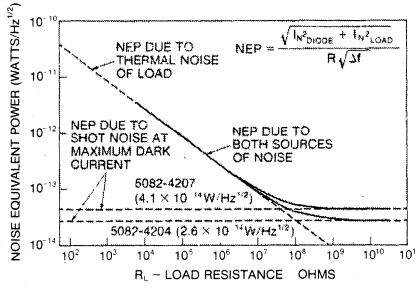


Figure 8. Noise Equivalent Power vs. Load Resistance.

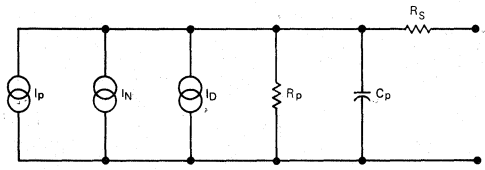


Figure 9. Photodiode Equivalent Circuit.

IP=Signal current ≈ 0.5μA/μW x flux input at 770 nm
IN= Shot noise current
<1.2 x 10-14 amps/Hz1/2(5082-4204)
<4 x 10-14 amps/Hz1/2(5082-4207)
ID= Dark current
<600 x 10-12 amps at -10 V dc (5082-4204)
<2500 x 10-12 amps at -10 V dc (5082-4207)
RP = 10^11Ω
RS = <50Ω

Application Information

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 600 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.4×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is 1.28×10^{-10} $(R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25°C, and far exceeds the diode shot noise for load resistance less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

HIGH SPEED PROPERTIES

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time less than one nanosecond. A significant advantage of this device is that the speed of response is exhibited at relatively low reverse bias (−10 to −20 volts).

OFF-AXIS INCIDANCE RESPONSE

Response of the photodiodes to a uniform field of radiant incidance E_e, parallel to the polar axis is given by $I = (RA) \times E_e$ for 770nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle of operation. For example, the multiplying factor for the 5082-4207 with incidance E_e at an angle of 40° from the polar axis is 0.8. If $E_e = 1mW/cm^2$, then $I_p = k \times (RA) \times E_e$; $I_p = 0.8 \times 4.0 \times 1 = 3.2$ μamps.

SPECTRAL RESPONSE

To obtain the response at a wavelength other than 770nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 770nm is given by:

$$\text{RATIO} = \frac{X}{0.5}$$

Multiplying this ratio by the incidance response at 770nm gives the incidance response at the desired wavelength.

ULTRAVIOLET RESPONSE

Under reverse bias, a region around the outside edge of the nominal active area becomes responsive. The width of this annular ring is approximately 25μm (0.001 inch) at −20V, and expands with higher reverse voltage. Responsivity in this edge region is higher than in the interior, particularly at shorter wavelengths; at 400nm the interior, responsivity is 0.1 A/W while edge responsivity is 0.35 A/W. At wavelengths shorter than 400nm, attenuation by the glass window affects response adversely. Speed of response for edge incidance is t_r, $t_f \approx 300ns$.

5082-4205 MOUNTING RECOMMENDATIONS

a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.51 to 1.52mm (0.02 to 0.06 inch).
b. Soldering temperature should be controlled so that at no time does the case temperature approach 280° C. The lowest solder melting point in the device is 280° C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280° C.
c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.
d. If printed circuit board mounting is not convenient, wire leads may be soldering or welded to the devices using the precautions noted above.

LINEAR OPERATION

Having an equivalent circuit as shown in Figure 9, operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 10.

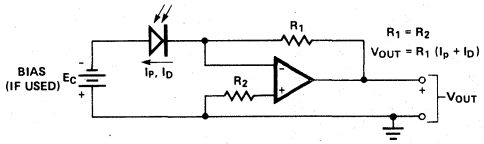


Figure 10. Linear Operation.

Lowest noise is obtained with $E_c = 0$, but higher speed and wider dynamic range are obtained if $5 < E_c < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

LOGARITHMIC OPERATION

If the photodiode is operated at zero bias with a very high impedance amplifier, the output voltage will be:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{kT}{q} \cdot \ln \left(1 + \frac{I_P}{I_S}\right)$$

where $I_S = I_F \left(e^{\frac{qV}{kT}} - 1\right)^{-1}$ at $0 < I_F < 0.1mA$

using a circuit as shown in Figure 11.

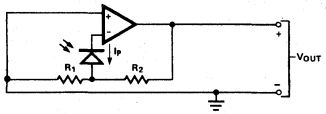
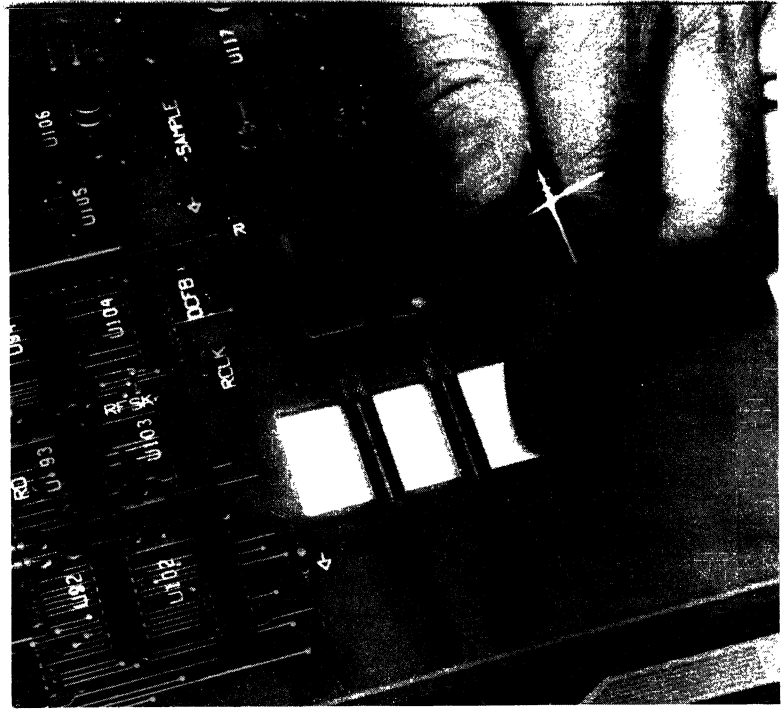


Figure 11. Logarithmic Operation.

Output voltage, V_{OUT}, is positive as the photocurrent, I_P, flows back through the photodiode making the anode positive.



Fiber Optics

Fiber Optics!

Fiber optics is emerging as a practical, cost-effective technology for data communications. Pulses of light traveling down hair-thin fibers are replacing electrical signals transmitted over copper wires. The transmission of information over optical cables offers many features, advantages, and benefits, some not available with any other technology:

• Features	• Advantages	• Benefits
Optical transmission path	Complete input-output electrical isolation	Freedom from ground loops. Lightning safe.
Light pulse "carrier" signals	No EMI susceptibility or radiation	Freedom from induced noise. Freedom from crosstalk. Secure communications.
	Very high distance/bandwidth products achievable	Greater data rates at longer distances than wire/coax.
Bandwidth independent of cable size	Light weight, small diameter cables possible	Lower cost installation and maintenance. More bandwidth (channels) per unit area or unit weight.

Versatile

HP's new fiber optic systems are point-to-point links intended for short to intermediate distance processor-to-processor or processor-to-peripheral interconnection in commercial, industrial, or military applications. Some of these are:

- **Large computer installations**
- **Distributed processing (minicomputer) systems**
- **Hospital computer systems**
- **Power plant communications/control**
- **Industrial/process control**
- **Industrial or military secure communications**
- **Aircraft/shipboard data links**
- **High voltage or electromagnetic field research**
- **Remote instrumentation systems**
- **Factory data collection**

In many of these applications induced noise, ground potential differences, high voltage, or extended distance, make twisted wire or coaxial data links difficult or impossible to use. Fiber optics can offer an alternative to expensive shielding, conduit, isolation transformers, or data error checking and retransmission circuitry.

System Specifications*

DATA RATE:	DC to 10Mb/s NRZ
DATA FORMAT:	No restrictions
LINK DISTANCE:	0 to 1000 metres
BIT ERROR RATE:	10^{-9} max. at 10Mb/s NRZ
DATA INPUT:	TTL compatible (1 LSTTL load)
DATA OUTPUT:	TTL compatible (up to 20 LSTTL loads)
CABLE CONSTRUCTION:	Reinforced, polyurethane jacketed, single fiber, glass core and cladding.
POWER SUPPLY REQUIREMENTS	
TRANSMITTER:	5V±5% at 125mA
RECEIVER:	5V±5% at 100mA
OPERATING TEMPERATURE RANGE:	0°C to 70°C

* Detailed electrical and mechanical specifications are contained in the following data sheets: HFBR-1001, HFBR-1002, HFBR-2001, HFBR-3000.

Easy-To-Use

The HP Fiber Optic Link is a versatile, easy-to-use system. It does not require optical design expertise, calibration or adjustment.

To make it easy to get started, HP offers the HFBR-0010, a complete 10 metre simplex link consisting of a transmitter, a receiver, a 10 metre cable/connector assembly, and technical literature. Also available are separate components: the HFBR-1001 100 metre digital transmitter the HFBR-1002, 1000 metre digital transmitter, the HFBR-2001 digital receiver, and the HFBR-3000 cable/connector assemblies.

HP systems feature:

- **Compatible plug-together transmitters, receivers, and cable assemblies**
- **Miniature PC board mountable packages**
- **TTL electrical interfaces**
- **Single 5 volt power supply requirement**
- **Accepts any data format from DC to 10 Mbits NRZ**
- **Accommodates cable lengths up to 1000 metres**
- **Integral fiber optic connectors**
- **Built-in "link monitor"**

Systems and Components

HP Part No.	Description	Page No.
HFBR-0010	Complete 10 Metre Simplex System (Contains one each HFBR-1001, -2001, -3001)	(Contact HP Sales Office)
HFBR-1001	100 Metre Digital Transmitter	28
HFBR-1002	1000 Metre Digital Transmitter	32
HFBR-2001	Digital Receiver	36
HFBR-3000	Cable/Connector Assemblies: In User Specified Cable Lengths	40

HEWLETT PACKARD

FIBER OPTIC 100 METRE DIGITAL TRANSMITTER

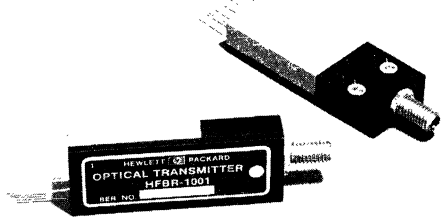
HFBR-1001

TECHNICAL DATA MARCH 1980

Features

- **HIGH SPEED: dc to 10Mb/s NRZ***
- **LONG DISTANCE: 100 metres***
- **LOW PROFILE: Fits 12.7mm (0.5") spaced card rack**
- **NO HEAT SINK REQUIRED**
- **ARBITRARY DATA FORMAT***
- **TTL INPUT LEVELS**
- **SCHMITT DATA INPUT**
- **OPTICAL PORT CONNECTOR**
- **SINGLE 5V SUPPLY**

*When used with HFBR-2001 Receiver Module and HFBR-3000 Cable/Connector Assemblies.

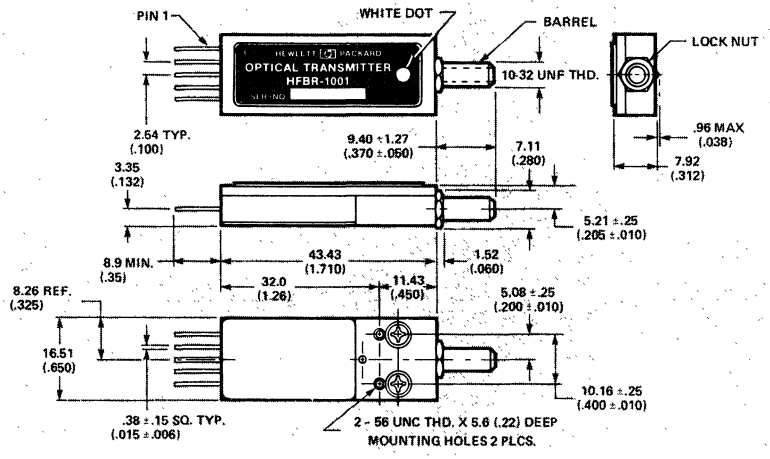


Description

The HFBR-1001 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single fiber channels. A bipolar integrated circuit and a GaAsP LED convert TTL level inputs to optical pulses at data rates from dc to 10Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of source/fiber alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-1001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances up to 100 metres. The HFBR-1001 generates optical signals in either of two externally selectable modes. The internally-coded mode produces a 3-level coded optical signal for reception and decoding by the HFBR-2001 receiver. This feature provides data format independence over the data rate range of dc to 10Mb/s NRZ while allowing for wide dynamic range and high sensitivity at the receiver. The externally-coded mode produces a 2-level optical signal which is a digital replica of the data input waveform. Used in this mode with the HFBR-2001 receiver, the user must provide proper data formatting (explained in the HFBR-2001 data sheet) to insure proper receiver operation. In either mode, the radiant output is radiologically safe (per ANSI Z136.1-1976).

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3000 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3000 DATA SHEET.

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:

1. DIMENSIONS IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015").

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[6]	Max	Units	Conditions		Fig.	Note
High Level Input Current	Mode Select	I_{IH}			100	µA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High, V_{CC} = 5.25V	1, 2	5
			40					Data Input Low, V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low, V_{CC} = 5.25V		
Optical Flux	High Level	ϕ_H		67		µW	Mode Select High	Data Input High	1, 2, 3	
	Low Level	ϕ_L		3				Data Input Low		
	Mid Level (average)	ϕ_M		35			Mode Select Low	Data Input		
	Excursion $\left(\frac{\text{peak-to-peak}}{2}\right)$	$\Delta\phi$	22	32			Mode Select High	Square Wave at 500 kHz		9
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	7
Exit Numerical Aperture		N.A.		0.5		—			3	
Optical Port (fiber optic core) Diam.		D_C		200		µm				
Coupling Loss	from area mismatch	α_A		6.0		dB	with HFBR-3000 Cable/Connector Assembly			
	from numerical aperture mismatch	$\alpha_{N.A.}$		4.0						
Peak Emission Wavelength		λ_P		700		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[6]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		31	45	ns	V_{CC} = 4.75 V	1	8
	Low-to-High Data Input Voltage Step	t_{PLH}		35	50	ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		60		ns	V_{CC} = 5.00 V, Mode Select Low	1	8
	Repetition Rate	f_R		300		kHz			

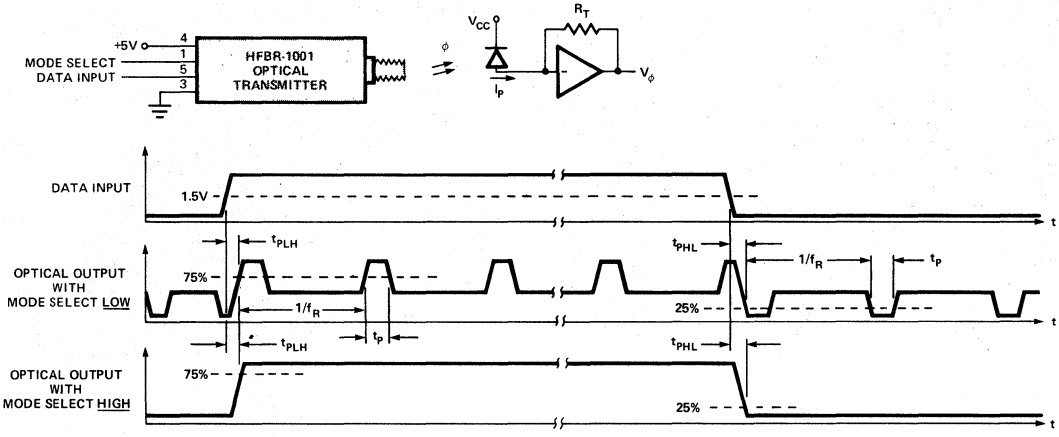


Figure 1. Flux Coding and Timing Diagram.

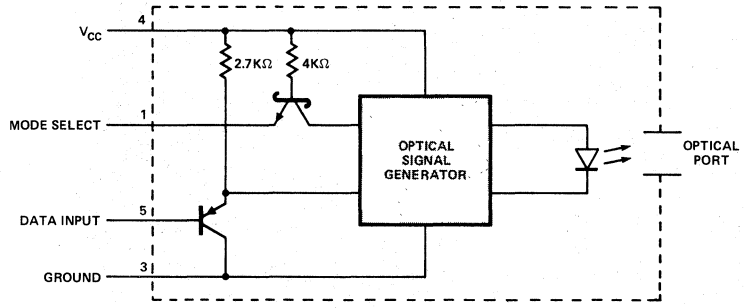


Figure 2. Schematic Diagram.

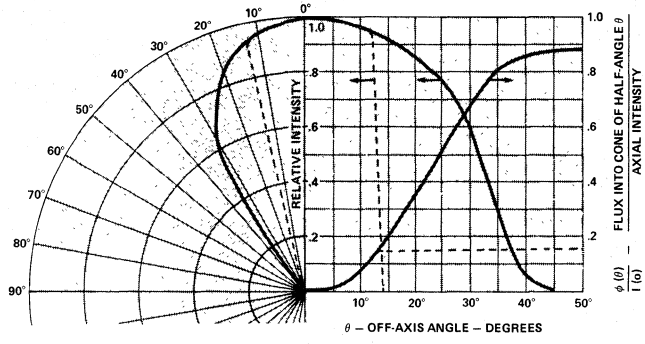


Figure 3. Radiation Pattern.*

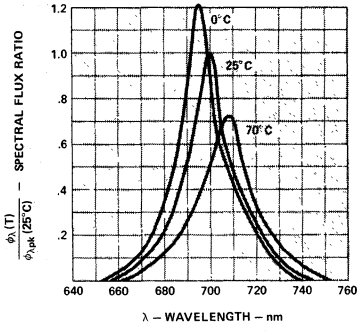


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. Average currents for steady-state conditions at Data Input.
6. For typical values, V_{CC} = 5.00V and T_A = 25°C.
7. Flux excursion ratio, k, is the ratio of flux excursion above mid level to flux excursion below mid level. $k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$.
8. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
9. Flux excursion
   $\Delta\phi = 0.5\ (\phi_H - \phi_L)$, or $\Delta\phi = 0.5\ (\phi_M - \phi_L) \bullet (1+k)$.

   Notice that under the conditions specified for $\Delta\phi$, the **average** flux is $(\Delta\phi + \phi_L)$.

Electrical Description

The HFBR-1001 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1001 produces a "mid-level" flux which has positive or negative excursions, depending on whether Data Input is "high" or "low." In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high;" when Data Input goes "low," a train of negative excursions is initiated. These excursions are pulses of approximately 60ns duration with a 300kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated—even at mid-pulse—as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average flux is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme is designed to operate the HFBR-2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, allowing low propagation delay for any change of state at Data Input. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, thus reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid level) when Data Input is "high," and nearly zero when Data Input is "low." This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either ϕ_H, or ϕ_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve; THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

The HFBR-1001 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

HEWLETT PACKARD

FIBER OPTIC 1000 METRE DIGITAL TRANSMITTER

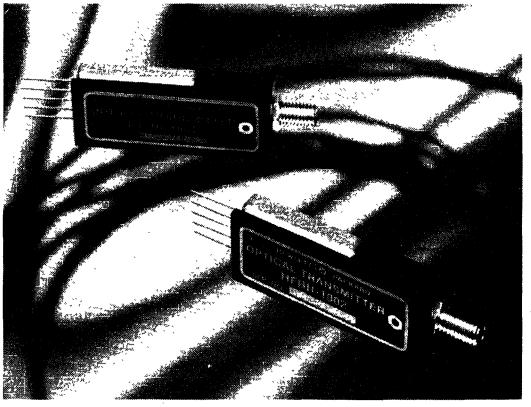
HFBR-1002

TECHNICAL DATA MARCH 1980

Features

- **LONG DISTANCE TRANSMISSION: 1000 METRES***
- **PIN COMPATIBLE WITH HFBR-1001 TRANSMITTER**
- **HIGH SPEED: DC TO 10 Mbaud***
- **NO DATA ENCODING REQUIRED***
- **FUNCTIONAL LINK MONITORING***
- **TTL INPUT LEVELS**
- **BUILT-IN OPTICAL CONNECTOR**
- **LOW PROFILE: PCB MOUNTABLE**
- **SINGLE +5V SUPPLY**

*When used with HFBR-2001 Receiver Module and any Hewlett-Packard HFBR-3000 Series Cable/Connector Assembly.



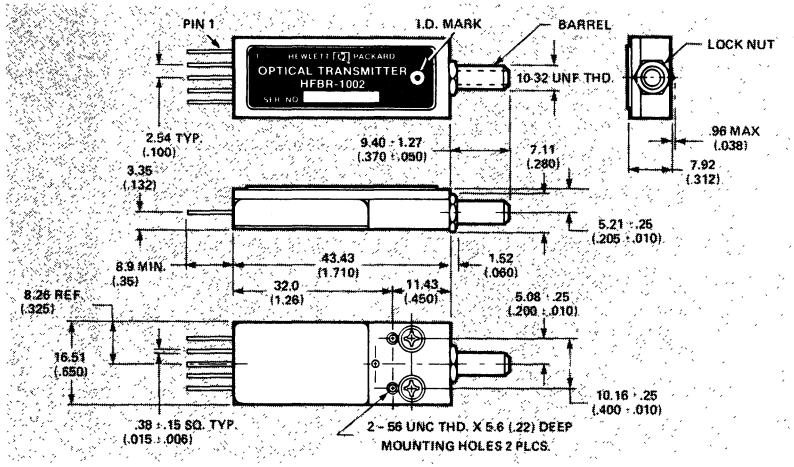
Description

The HFBR-1002 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single optical fiber channels. A bipolar integrated circuit and a high efficiency GaAlAs LED convert TTL level inputs to optical pulses at data rates from dc to 10 Mbaud (see note 5). An integral optical connector on the module allows easy interfacing without problems of fiber alignment. The low profile rugged industrial package is designed for direct circuit board mounting without additional heat sinking on printed circuit boards with 12.7 mm (0.5") card rack spacing.

The HFBR-1002 is intended for use with Hewlett-Packard fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances to 1000 metres. It is a direct replacement for extending links currently using the HFBR-1001 (100 metre) transmitter to give 1000 metre capability. The HFBR-1002 generates optical signals in either of two externally selectable modes. True dc response (data high or low for arbitrary time interval) is available when using the Internally-Coded mode.

WARNING: OBSERVING THE TRANSMITTER OUTPUT FLUX UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the near IR output flux is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1976.

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HEWLETT-PACKARD CABLE/ CONNECTOR DATA SHEET (FINGER TIGHT).

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	+70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	5
Transmission Distance	ℓ		1000	m	6

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[7]	Max	Units	Conditions		Fig.	Note
Optical Flux	Transmitter Output (peak-to-peak / 2)	ϕ_T	-13 50	-10 100		dBm μW	Mode Select High	Data Input Square Wave at 500 kHz	1, 2,	8
	High Level	ϕ_H		205		μW	Mode Select High	Data Input High	3, 5	
	Low Level	ϕ_L		5				Data Input Low		
	Mid Level	ϕ_M		105			Mode Select Low	Data Input Square Wave at 500 kHz		
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	–	Mode Select Low		1	9
Exit Numerical Aperture		N.A.		0.3		–			3	
Optical Port (fiber optic core) Diam.		D_C		100		μm				
Coupling Loss	Transmitter Optical Port to Cable/Connector Assy.	$\alpha_{T\text{-}C}$		3.0		dB	With Hewlett-Packard Cable/ Connector Assembly			
Peak Emission Wavelength		λ_{PK}		820		nm			4	
High Level Input Current	Mode Select	I_{IH}			100	μA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High V_{CC} = 5.25V	1, 2	10
			40					Data Input Low V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low, V_{CC} = 5.25V		

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[7]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		34	42	ns	V_{CC} = 4.75 V Data Input Square Wave at 500 kHz	1	11
	Low-to-High Data Input Voltage Step	t_{PLH}		32	38	ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		40		ns	V_{CC} = 5.00 V, Mode Select Low	1	11
	Repetition Rate	f_R		300		kHz			

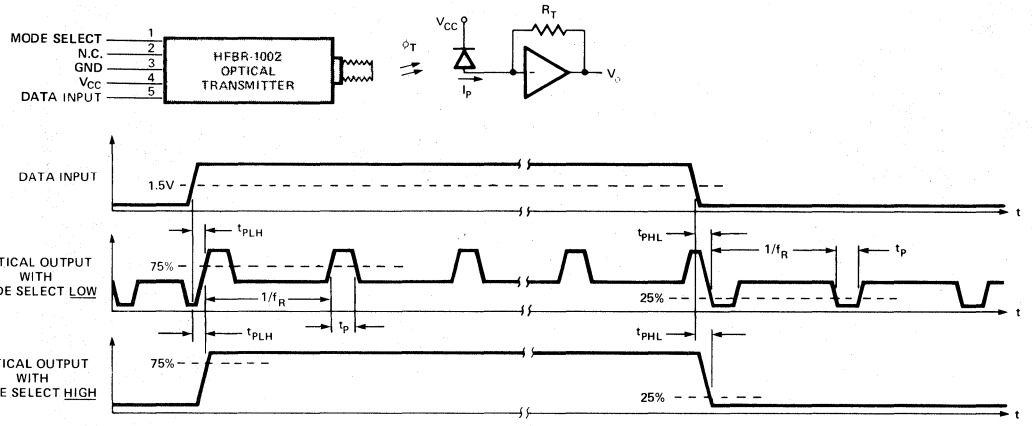


Figure 1. Flux Coding and Timing Diagram.

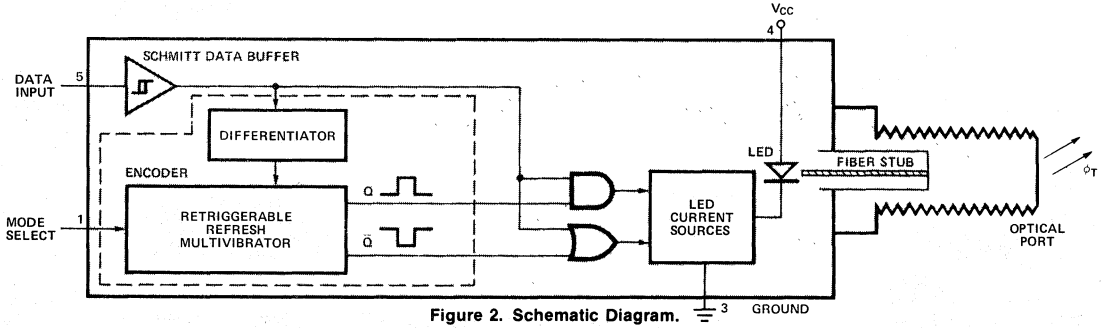


Figure 2. Schematic Diagram.

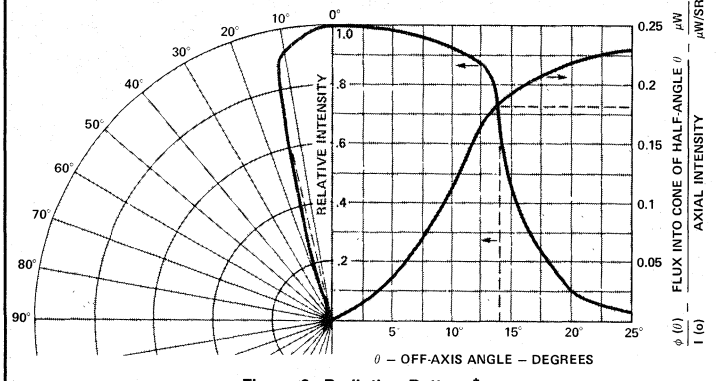


Figure 3. Radiation Pattern.*

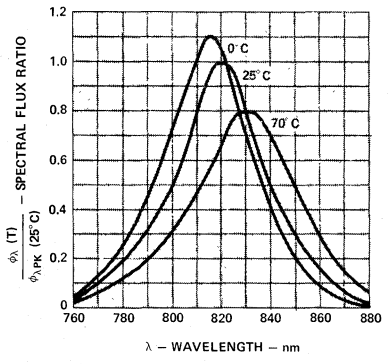


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. With NRZ data, 10 Mbaud corresponds to a data rate of 10 Mbits/second. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval. Self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5 Mbits/second at 10 Mbaud.
6. With Hewlett-Packard HFBR-2001 and HFBR-3000 Series Cable/Connector Assembly.
7. For typical values, V_{CC} = 5.00V and T_A = 25° C.
8. The transmitter output, ϕ_T, equals the flux excursion, $\Delta\phi = (\phi_H - \phi_L)/2$. Notice that under the conditions specified for $\Delta\phi$, the average flux is $(\phi_H + \phi_L)/2$.
9. Flux excursion ratio, k, is the ratio of flux excursion above mid level to flux excursion below mid level.

$$k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$$

10. Average currents for steady-state conditions at Data Input.
11. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.

Electrical Description

The HFBR-1002 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1002 produces a "mid-level" flux which has positive or negative excursions, depending on whether Data Input is "high" or "low". In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high;" when Data Input goes "low," a train of negative excursions is initiated. These excursions are pulses of approximately 40ns duration with a 300kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated — even at mid-pulse — as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average flux is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme, which is transparent to the user, is designed to operate the HFBR-2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, providing data format independence (no data encoding required) over the data rate range of dc to 10Mbaud. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, thus reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid-level) when Data Input is "high," and nearly zero when Data Input is "low." Used in this mode with the HFBR-2001 Receiver, the user must provide proper data formatting (e.g., Manchester or Bi-Phase coding, explained in HFBR-2001 data sheet) to ensure proper receiver operation. This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either ϕ_H, or ϕ_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the Hewlett-Packard Fiber Optic Cable/Connector Assembly. The threaded barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened finger-tight as specified in the Hewlett-Packard Fiber Optic Cable/Connector data sheet.

The HFBR-1002 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the transmitter ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

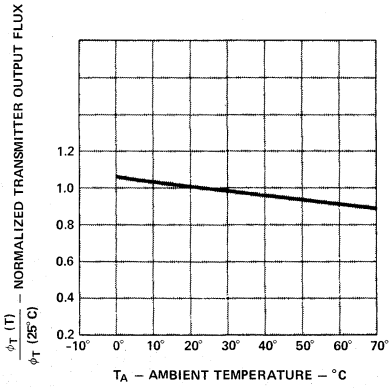


Figure 5. Normalized Transmitter Output Flux vs. Temperature.

HEWLETT PACKARD

FIBER OPTIC DIGITAL RECEIVER

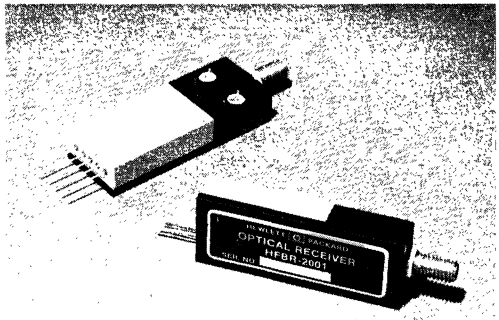
HFBR-2001

TECHNICAL DATA MARCH 1980

Features

- **HIGH SPEED: dc to 10Mb/s NRZ***
- **LOW NOISE: 10^{-9} BER with 0.8μW Input***
- **LOW PROFILE: Fits 12.7mm (0.5") spaced card rack**
- **SINGLE SUPPLY VOLTAGE**
- **WIDE OPTICAL DYNAMIC RANGE: 23dB**
- **OPTICAL PORT CONNECTOR**
- **ARBITRARY DATA FORMAT***
- **TTL OUTPUT LEVELS**
- **LINK MONITOR: Shows Satisfactory Input Signal***

*When used with HFBR-1001/1002 Transmitters and HFBR-3000 Cable/Connector Assemblies.



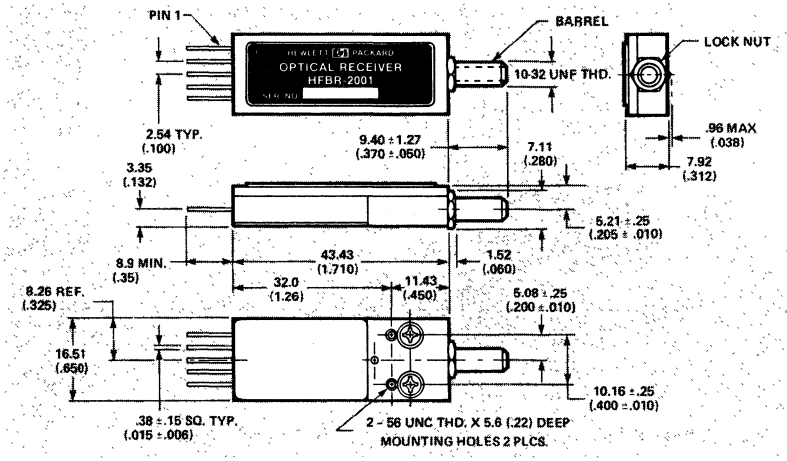
Description

HFBR-2001 fiber optic receiver is an integrated optical to electrical transducer designed for reception of digital data over single fiber channels. A silicon PIN photodetector and a bipolar integrated circuit convert optical pulses to TTL level outputs with an optical sensitivity of .8μW, a dynamic range of 23 dB, and data rates to 10 Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of fiber/detector alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-2001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies and the HFBR-1001/1002 fiber optic transmitters. In order to provide wide dynamic range, dc response, and high sensitivity, the receiver must periodically extract information from the optical waveform. When operating with a transmitter in the internally-coded mode, this information is automatically provided by the transmitter. When operating in the externally-coded mode, or with another transmission source, the user must provide proper data formatting to insure proper receiver operation.

An additional TTL output called Link Monitor (LM), provides a digital indication of link continuity independent of the presence of data. Link continuity is indicated by a logical high output state.

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3000 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3000 DATA SHEET.

PIN	FUNCTION
1	TEST POINT
2	LINK MONITOR
3	GROUND
4	V_{CC}
5	DATA OUTPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering	Temperature			260	°C	3
Cycle	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6.0	V	
Output Voltage (High State)		V_{OH}		6.0	V	

Recommended Operating Conditions

Parameter			Symbol	Min	Max	Units	Note
Ambient Temperature			T_A	0	70	°C	
Supply Voltage			V_{CC}	4.75	5.25	V	
Supply Ripple (Peak-to-Peak)			ΔV_{CC}		250	mV	4
High Level Output Current	Link Monitor		I_{OH}		-100	µA	
	Data Output				-400		
Low Level Output Current			I_{OL}		8	mA	
Average Input Flux			ϕ_M	0.8	100	µW	6
Peak-to-Peak Input Flux			ϕ_H-ϕ_L	1.6	200	µW	
Optical Input Pulse Duration and Timing	2-Level Code	High Level	t_H	100	5000	ns	
		Low Level	t_L				
	Flux Excursion Ratio		k	0.75	1.25		7
	3-Level Code	High Level	t_H	50		ns	
		Low Level	t_L				
		Mid Level	t_M	0.05	6.7	µs	8
	Refresh Repetition Rate		f_R	150		kHz	
	Refresh Duty Factor		$f_R t_H$, $f_R t_L$		0.04		

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions		Fig.	Note
Output Voltage	High State	Data Output	V_{OH}	2.4	2.85		V	$\phi = (\phi_M + 0.8\ \mu W)$, $I_O = -400\ \mu A$	V_{CC} = 4.75 V	1, 2	7, 9
		Link Monitor						$\Delta\phi = 0.8\ \mu W$, $I_O = -100\ \mu A$			
	Low State	Data Output	V_{OL}		0.35	0.5	V	$\phi = (\phi_M - 0.8\ \mu W)$	I_O = 8 mA, V_{CC} = 4.75 V		
		Link Monitor			0.2	0.4		$\Delta\phi = 0$			
Test Point Voltage			V_T		0		V	$\phi_M = 100\ \mu W$			10
					1.3			$\phi_M = 0$			
Supply Current			I_{CC}		77	100	mA	V_{CC} = 5.25 V			
				60	77			V_{CC} = 4.75 V			
Optical Port (fiber optic core) Diameter			D_c		200		µm				
Numerical Aperture			N.A.		0.5					3	
Peak Responsivity Wavelength			λ_p		770		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High to Low	3-Level Code	t_{PHL}		29	37	ns	V_{CC} = 4.75 V, k = 1, Link Monitor High	1	11
		2-Level Code			37	45				
	Low to High	3-Level Code	t_{PLH}		37	52	ns			12
		2-Level Code			45	60				
Link Monitor Response Time	Low-to-High		t_{MH}		20		ms	V_{CC} = 4.75 V, $\Delta\phi$ = 0.8 µW, I_{OL} = 8 mA, Peak-to-Peak		13
	High-to-Low		t_{ML}		1000					14
Bit Error Rate at 10 M baud			BER			10^{-9}		k = 1, $\Delta\phi \geq 0.8\ \mu W$		15

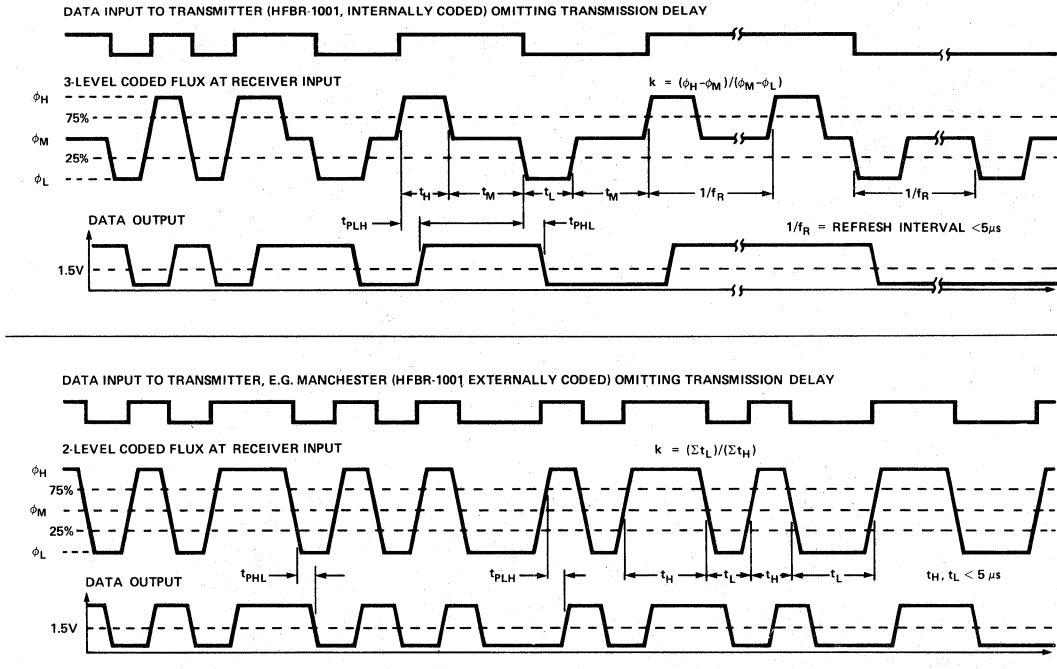


Figure 1. Optical Input Timing Requirements.

Notes (cont'd):

3. Measured at a point 2mm (.079") from where the lead enters the package.
4. If ripple exceeds the specified limit, the regulator shown in Figure 5 should be used. The LC filter shown in Figure 5 is recommended whether the regulator is used or not.
5. For typical values, V_{CC} = 5.00V and T_A = 25°C.
6. Flux is averaged over an interval of at least 50μs. Flux values specified are for the equivalent of a monochromatic source between 700nm and 820nm.
7. For either 2-level or 3-level code, k= $(\phi_H-\phi_M)/(\phi_M-\phi_L)$.
8. For the HFBR-2001, a *3-Level Code* is defined as having a mid-level, with equal-amplitude and pulse width excursions to high-level or to low-level.
9. Link Monitor provides a check of link continuity. A low Link Monitor output indicates that the optical signal path has been interrupted. For example, it might indicate a broken cable or a loose, dirty, or damaged connector. The link may still be operational with Link Monitor low, but it should be checked to determine the cause of the low indication. When the source of flux is an Internally-Coded HFBR-1001/1002 Fiber Optic Transmitter, Link Monitor high will be a valid indication of link continuity whether or not data is being transmitted. An optical input with excursions ($\Delta\phi$) greater than or equal to 0.8μW is sufficient to hold Link Monitor high.
10. When observing V_T, use a voltmeter with at least 10MΩ input resistance. With zero input flux, V_T is at its maximum value, $V_{T,MAX}$. Then when flux is being received, whether modulated or not:

$$(V_{T,MAX} - V_T) = (25k\Omega)(I_p) = (25k\Omega)(R_\phi\phi_M)$$

where I_p = average photodiode photocurrent
$R_\phi \approx 0.4A/W$ = photodiode responsivity
ϕ_M = average flux being received

11. Measured from the time at which optical input crosses the 25% level until DATA OUTPUT = 1.5V in HL transition.
12. Measured from the time at which optical input crosses the 75% level until DATA OUTPUT = 1.5V in LH transition.

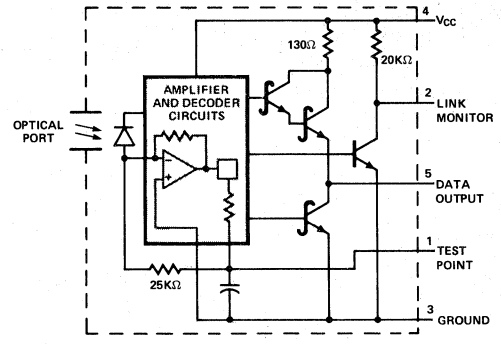


Figure 2. Schematic Diagram.

13. Measured from the time at which optical input fluctuation begins until LINK MONITOR rises to 1.5V.
14. Measured from the time at which optical input fluctuation ceases until LINK MONITOR falls to 1.5V.
15. With NRZ data, 10Mbaud corresponds to a data rate of 10Mb/s. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval—self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5Mb/s at 10Mbaud.

Electrical Description

Flux enters the HFBR-2001 via an optical fiber stub where a PIN photodiode converts it to a photocurrent. This photocurrent goes to an I-V (current-to-voltage) amplifier which utilizes both dc feedback and ALC (automatic level control).

The function of dc feedback is to keep the average value of the signal centered in the linear range of the amplifier. The dc feedback amplifier has a high impedance output to establish a long time constant on a capacitor at its output. (The voltage on the capacitor is observable at the test point). As seen in the schematic diagram, the voltage on this capacitor extracts the *average* component of photocurrent from the input of the I-V amplifier so its *average* output is at a *fixed level.* Optical flux excursions above and below the average cause voltage excursion above and below the fixed level at the output of the I-V amplifier.

The voltage excursions operate a flip-flop whose output drives the Data Output amplifier; an excursion above the average level sets the data output high, where it remains until an excursion below the average level resets the flip-flop.

To prevent overdrive, an ALC circuit, responding to excursions *either above or below* the average level, controls the gain of the I-V amplifier. Gain is then determined by *whichever polarity* of excursion is the *greater*. If these excursions are too far from being balanced, the gain limitation imposed by the larger excursion may cause the smaller (opposite polarity) excursion to be too small to operate the flip-flop.

The Link Monitor output is driven by an amplifier which responds to the ALC voltage. The Link Monitor is high when the flux excursions are greater than or equal to 0.8μW.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the Receiver can be mounted without consideration for additional heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Receiver with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve, THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

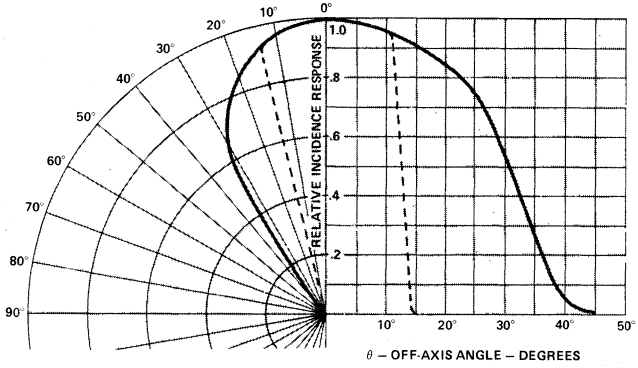


Figure 3. Reception Pattern.*

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents reception pattern at fiber stub without obscuration by connector barrel. Dashed line represents reception pattern as seen from outside of connector.

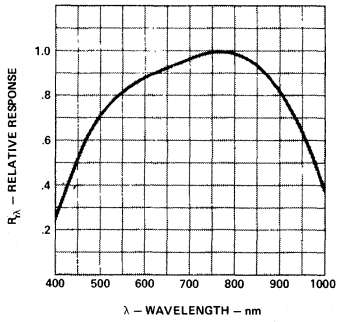


Figure 4. Spectral Response.

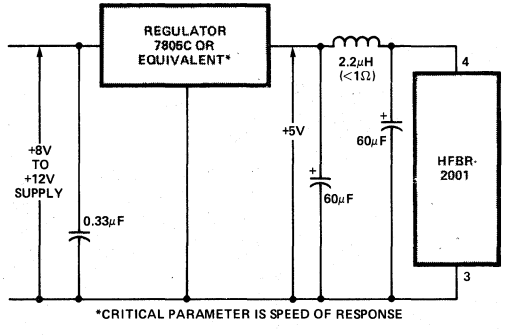


Figure 5. Power Supply Transient Filter Recommendation.

HEWLETT PACKARD

FIBER OPTIC SINGLE CHANNEL CABLE/CONNECTOR ASSEMBLIES

HFBR-3000

TECHNICAL DATA MARCH 1980

Features

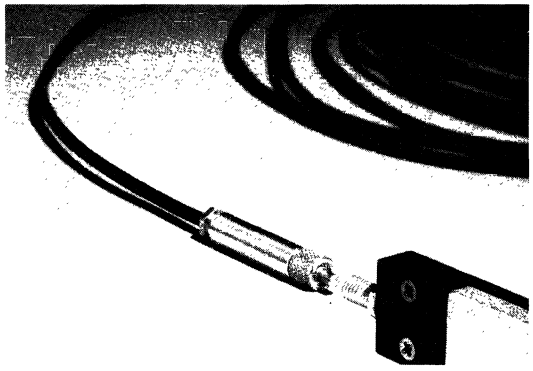
- **USER SPECIFIED CABLE LENGTHS**
- **CONNECTORS FACTORY INSTALLED AND TESTED**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE AND HUMIDITY**
- **HIGH STRENGTH**
- **LIGHT WEIGHT**
- **SMALL BEND RADIUS**

Description

The HFBR-3000 Simplex Fiber Optic Cable/Connector Assemblies are intended for use with the HFBR-1001/-1002 Transmitters and HFBR-2001 Receiver for digital data transmission. The Connectors mate directly with the optical ports on the Transmitters and Receiver. The cable uses a single fused silica, partially graded index, glass-clad fiber surrounded by silicone coating, buffer jacket, and tensile strength members. This combination is then covered by a scuff-resistant outer jacket. The cable resistance to mechanical abuse, safety in flammable environments, and inherent absence of electromagnetic interference effects may make the use of conduit unnecessary. However, the light weight and high strength of these assemblies allows them to be drawn through most electrical conduits. The HFBR-3099 Adapter, for interconnecting cables, consists of two parts: a sleeve to align the ferrules and barrel to join the connector couplings.

HFBR-3000 CABLE LENGTH TOLERANCE

Cable Length (Metres)	Tolerance	Units
1—10	$\frac{+10}{-0}$	%
11—100	$\frac{+1}{-0}$	Metre
> 100	$\frac{+1}{-0}$	%



Cable/Connector Ordering Guide

HFBR-3000 defines an optical cable of user specified length supplied with factory installed and tested connectors. Length must be specified in metres and can be any one metre increment from 1 to 1000 metres. Length information is shown as option 001 to the base product number with quantity equal to the number of cable assemblies ordered.

Examples:

For a single length of 245 metres specify:

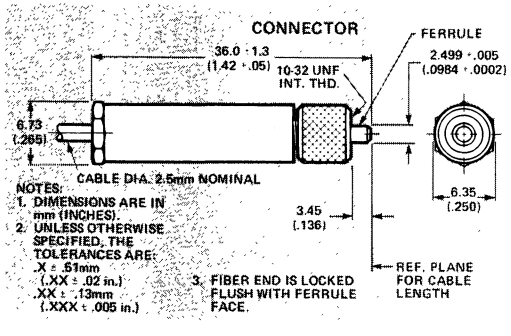
HFBR-3000	Optic Cable Assy	Quantity 1
Option 001	245 metres long	Quantity 1

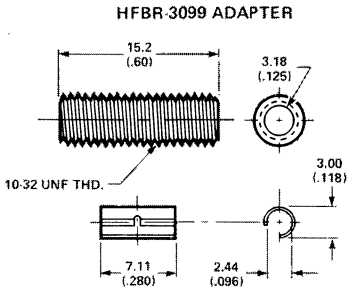
For seven lengths of 1000 metres specify:

HFBR-3000	Optic Cable Assy	Quantity 7
Option 001	1000 metres long	Quantity 7

Systems intended to operate at distances greater than 1000 metres may require special component selection, depending upon operating conditions. For cable lengths greater than 1000 metres contact your local Hewlett-Packard sales office.

Mechanical Dimensions





CAUTION:

A. COUPLING SHOULD NOT BE OVERTIGHTENED, SEE MECHANICAL/OPTICAL CHARACTERISTICS AND NOTE 14.

B. GOOD SYSTEM PERFORMANCE REQUIRES CLEAN FERRULE FACES TO AVOID OBSTRUCTING THE OPTICAL PATH. CLEAN COMPRESSED AIR OFTEN IS SUFFICIENT TO REMOVE PARTICLES. A COTTON SWAB SOAKED IN METHANOL OR FREON™ MAY ALSO BE USED.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Note
Relative Humidity at T_A = 70°C				95	%	12
Storage Temperature		T_S	-40	+85	°C	
Operating Temperature		T_A	0	+70		
Tensile Force	on Cable	F_T		300	N	10
	on Connector/Cable			100		

Parameter	Symbol	Min.	Max.	Units	Note
Bend Radius	r	7		mm	10
Flexing			50,000	cycles	4
Crush Load	F_C		200	N	5
Impact	m		1	kg	6
	h		0.3	m	

Mechanical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Exit Numerical Aperture		N.A.		0.3		—	λ = 820nm $\ell \geq$ 300m	1	7
Insertion Loss	Length Dependent	α_ℓ		16	20	dB/km	λ = 700nm ℓ = 100m	2	9,11
				7	10		λ = 820nm ℓ > 300m		
	Fixed	α_F		5.4	8.4	dB	λ = 820nm $\ell \leq$ 300m		13,14
Fiber Dispersion		$\Delta t/\ell$		17.5		ns/km	700 < λ < 820nm	3	
Fiber 3dB Bandwidth		$\Delta f \cdot \ell$		20		MHz•km			8
Optical Fiber Core Diameter		D_C		100		μm			
Cladding Outside Diameter		D_{CL}		140					
Optical Fiber Profile Index		α_1		10		—			
Elongation Under Tensile Force		$\Delta\ell/\ell$		0.5		%	F = 300N		9
Mass per Unit Length		m/ℓ		6		kg/km			
Cable Outside Diameter		D_{CA}		2.5		mm			

Notes (cont'd):

4. 180° bending at minimum bend radius, with 10N tensile load.
5. Force applied on 2.5 mm diameter mandrel laid across the cable on a flat surface, for 100 hours, followed by flexure test.
6. For mass m dropped from height h on 25 mm diameter mandrel laid across the cable on a flat surface.
7. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
8. Fiber 3dB Bandwidth • Length, (MHz • km) is defined as 350/fiber dispersion (ns/km).
9. Typical values are at T_A = 25°C.
10. This applies for short term testing, less than one hour.
11. Fiber loss exclusive of connector loss.
12. This applies to cable only.
13. When using HFBR-1002 transmitter with HFBR-3000 Cable/Connector Assembly, Total Insertion Loss, $\alpha_T \doteq \alpha_F + \alpha_O \left(\frac{\ell - 300}{1000}\right)$ for ℓ > 300 m; for lengths $\ell \leq$ 300 m, $\alpha_T = \alpha_F$.
14. Coupling Ring "Finger Tight", torque 0.05 < L < 0.1 N•m. Overtightening may cause excessive fiber misalignment or permanent damage.

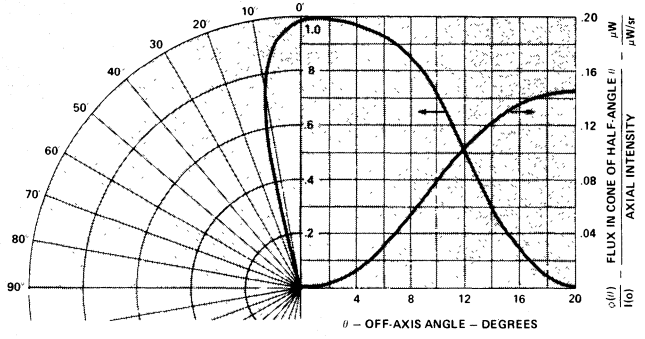


Figure 1. Optical Fiber Output Radiation Pattern.

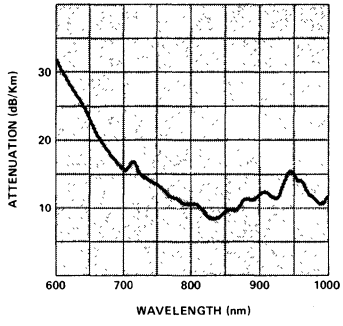


Figure 2. Spectral Transmission.

The actual fiber dispersion is determined from the RMS Pulse Spreading and can be approximated by:

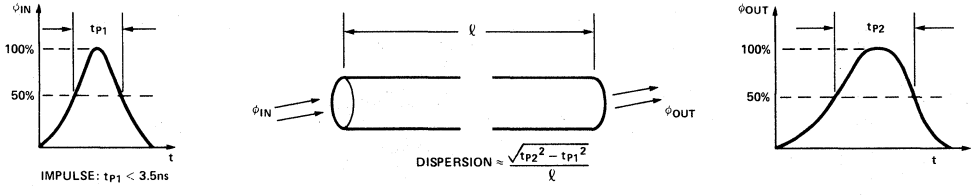
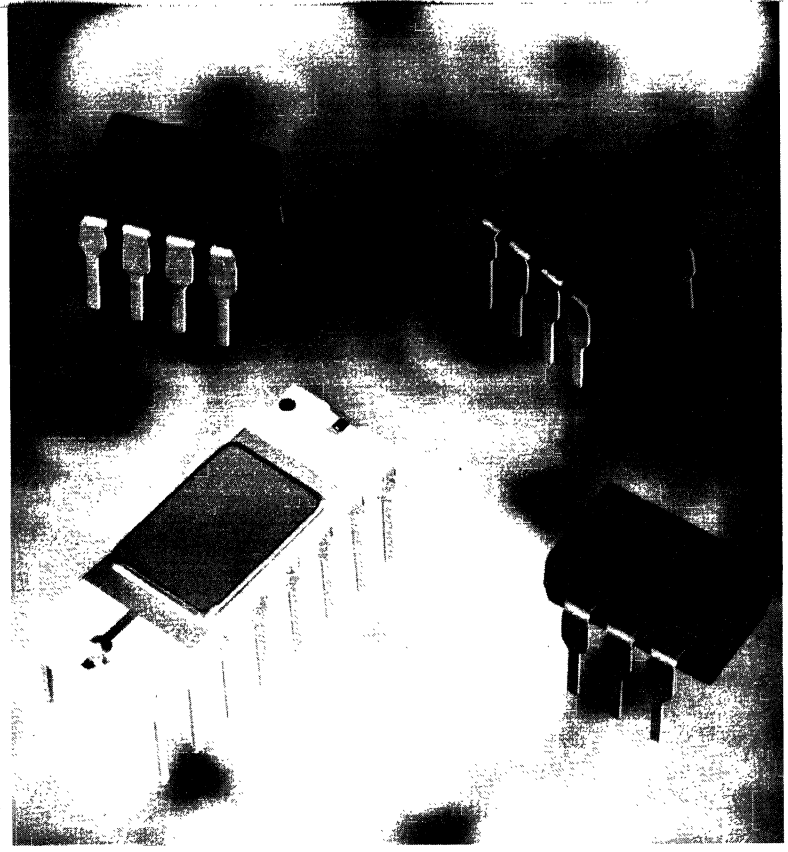
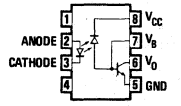
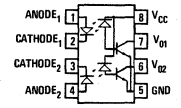
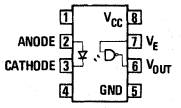
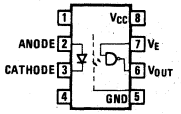
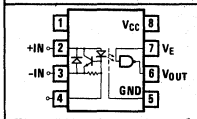
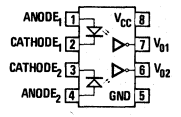


Figure 3. Fiber Dispersion

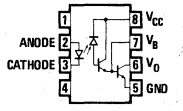
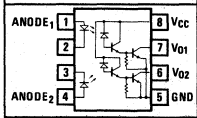
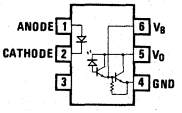


Optocouplers

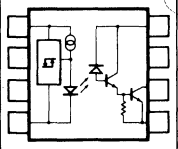
High Speed Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N135	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1M bit/s	7% Min.	16mA	3000Vdc[3]	46
	6N136				19% Min.			
	HCPL-2502				15-22%[2]			
	HCPL-2530	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1M bit/s	7% Min.	16mA	3000Vdc[3]	50
	HCPL-2531				19% Min.			
	6N137	Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation	10M Bit/s	700% Typ.	5.0mA	3000Vdc[3]	54
	HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation In High Ground or Induced Noise Environments	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	58
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers In High Ground or Induced Noise Environments	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	62
	HCPL-2630	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	68

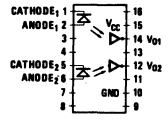
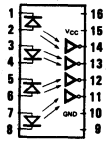
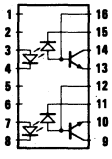
High Gain Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N138	Low Saturation Voltage, High Gain Output, V_{CC}=7VMax.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	300k bit/s	300% Min.	1.6mA	3000Vdc[3]	72
	6N139	Low Saturation Voltage, High Gain Output, V_{CC}=18V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL CMOS/TTL, CMOS/CMOS		400% Min.	0.5mA		
	HCPL-2730	Dual Channel, High Gain, V_{CC}=7V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	300k bit/s	300% Min.	1.6mA	3000Vdc[3]	76
	HCPL-2731	Dual Channel, High Gain, V_{CC}=18V Max.			400%Min.	0.5mA		
	4N45	Darlington Output V_{CC}=7V Max.	AC Isolation, Relay-Logic Isolation	3k bit/s	250% Min.	1.0mA	3000Vdc[3]	80
	4N46	Darlington Output V_{CC}=20V Max.			350% Min.	0.5mA		

AC/DC to Logic Interface Optocoupler

Device		Description	Application[1]	Typical Data Rates	Input Threshold Current	Output Current	Withstand Test Voltage	Page No.
	HCPL-3700	AC/DC to Logic Threshold Sensing Interface Optocoupler V_{CC} = 2.0V	Limit Switch Sensing, Low Voltage Detector, Relay Contact Monitor	4 KHz	2.5mA TH^+ 1.3mA TH^-	4.2mA	3000 Vdc[3]	84

Hermetic Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134 6N134 6N134TXVB	Dual Channel Hermetically Sealed Optically Coupled Logic Gate. TXV – Screened TXVB – Screened with Group B Data	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10mA	1500Vdc	90
	6N140 6N140TXV 6N140TXVB	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers TXV – Hi-Rel Screened TXVB – Hi-Rel Screened with Group B Data V_{CC}=18V	Line Receiver, Low Power Ground Isolation for High Reliability Systems	300k bit/s	300% Min.	0.5mA	1500Vdc	94
	4N55 4N55TXV 4N55TXVB	Dual Channel Hermetically Sealed Analog Optical Coupler TXV – Hi-Rel Screened TXVB – Hi-Rel Screened with Group B Data V_{CC}=20V	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	7% Min.	16mA	1500Vdc	98

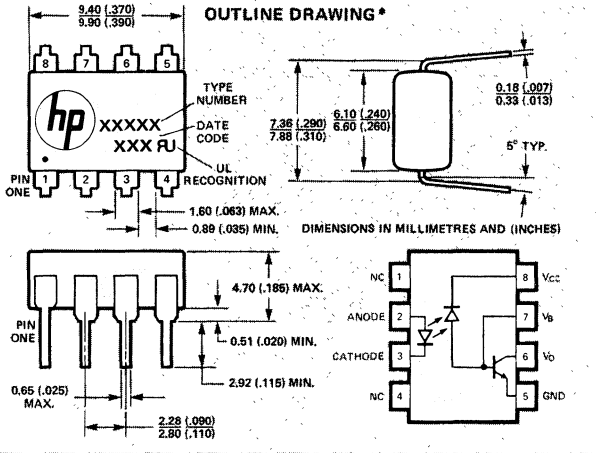
Notes: 1. AN 948, AN 951-1, and AN 951-2 are located in Application Notes Section, beginning on page 311. For further information ask for AN 939 and AN 947.
2. The HCPL-2502 Current Transfer Ratio Specification is guaranteed to be 15% minimum and 22% maximum.
3. Recognized under the Component Recognition Program of Underwriters Laboratories Inc. (File No. E55361), 220 VAC working voltage. This is guaranteed by a 3000 Vdc withstand voltage test for 5 seconds.

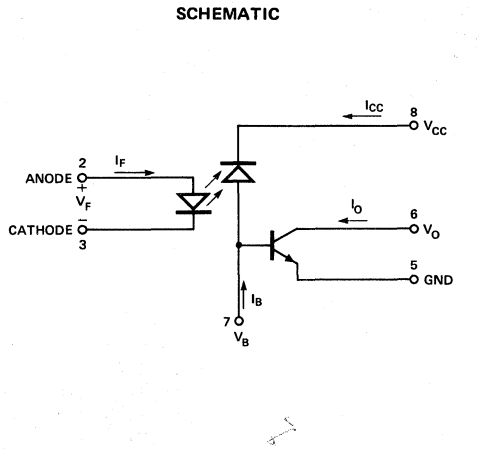
HEWLETT PACKARD

HIGH SPEED OPTOCOUPLERS

6N135
6N136
HCPL-2502

TECHNICAL DATA MARCH 1980





Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUT**

Description

These diode-transistor optocouplers use a light emitting diode and an integrated photon detector to provide 3000V dc electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired. CTR is 15 to 22% at I_F = 16 mA.

*JEDEC Registered Data. (The HCPL-2502 is not registered.)

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5V to 15V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Absolute Maximum Ratings*

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to 100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F . . . . . 25mA[1]
Peak Input Current – I_F . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F 1.0A
(≤1μs pulse width, 300pps)
Reverse Input Voltage – V_R (Pin 3-2) 5V
Input Power Dissipation . . . . . 45mW[3]
Average Output Current – I_O (Pin 6) 8mA
Peak Output Current 16mA
Emitter-Base Reverse Voltage (Pin 5-7). 5V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
. . . . . -0.5V to 15V
Base Current – I_B (Pin 7) 5mA
Output Power Dissipation . . . . . 100mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18		%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V, T_A = 25°C	1,2	5
		6N136	19	24		%			
		HCPL-2502	15		22	%			
	CTR	6N135	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		6N136	15	21		%			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		
		6N136 HCPL-2502		0.1	0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A = 25°C	6	
				0.1	100	µA	I_F = 0mA, V_O = V_{CC} = 15V, T_A = 25°C		
	I_{OH}				250	µA	I_F = 0mA, V_O = V_{CC} = 15V		
Logic Low Supply Current	I_{CCL}			40		µA	I_F = 16mA, V_O = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}*			0.02	1	µA	I_F = 0mA, V_O = Open, V_{CC} = 15V, T_A = 25°C		
	I_{CCH}				2	µA	I_F = 0mA, V_O = Open, V_{CC} = 15V		
Input Forward Voltage	V_F*			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, t = 5s, V_{I-O} = 3000Vdc, T_A = 25°C		6
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		6
Transistor DC Current Gain	h_{FE}			175		—	V_O = 5V, I_O = 3mA		

**All typicals at T_A = 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N135		0.5	1.5	µs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N135		0.4	1.5	µs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.3	0.8	µs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	6N135		1000		V/µs	I_F = 0mA, V_{CM} = 10Vp-p, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		1000		V/µs	I_F = 0mA, V_{CM} = 10Vp-p, R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	6N135		-1000		V/µs	V_{CM} = 10Vp-p, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		-1000		V/µs	V_{CM} = 10Vp-p, R_L = 1.9kΩ		
Bandwidth	BW			2		MHz	R_L = 100Ω	8	10

NOTES:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
9. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

*JEDEC Registered Data.

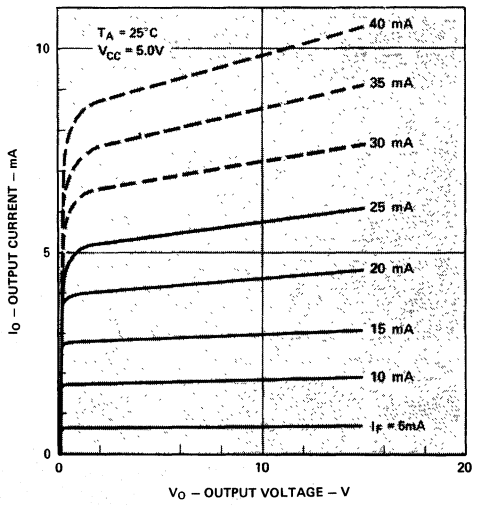


Figure 1. DC and Pulsed Transfer Characteristics.

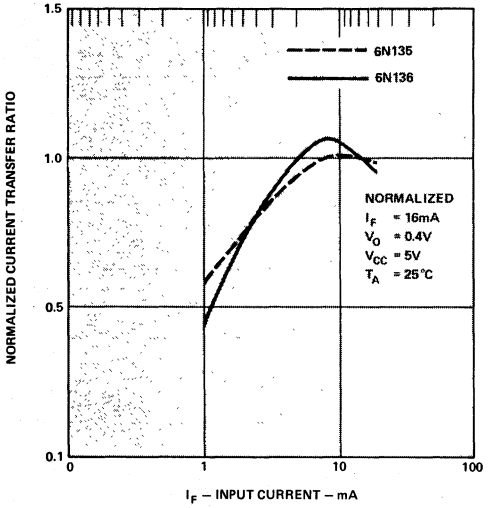


Figure 2. Current Transfer Ratio vs. Input Current.

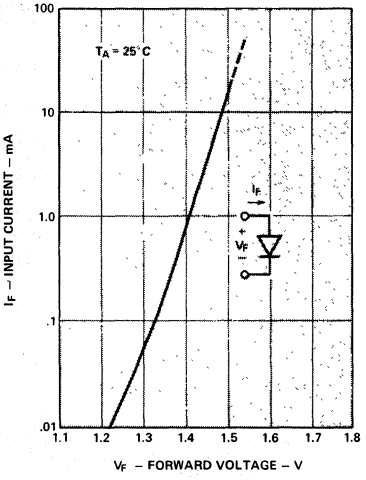


Figure 3. Input Current vs. Forward Voltage.

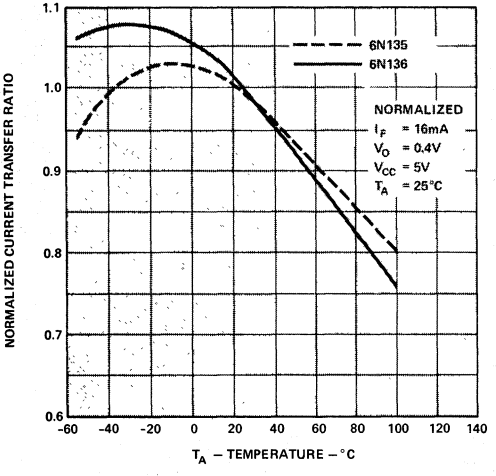


Figure 4. Current Transfer Ratio vs. Temperature.

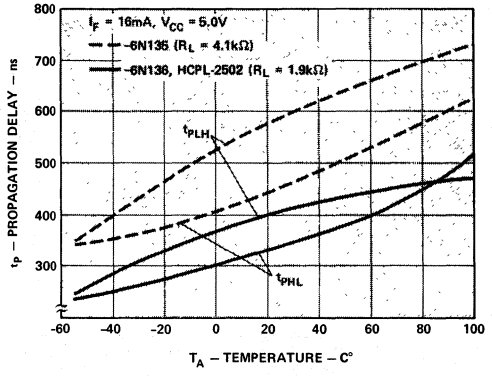


Figure 5. Propagation Delay vs. Temperature.

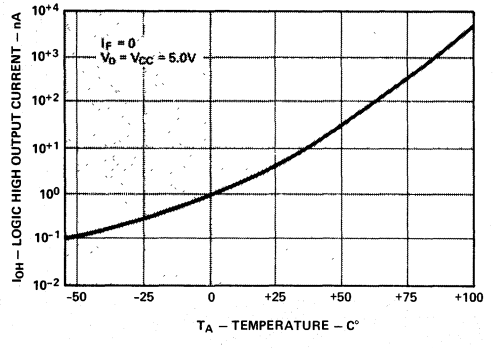


Figure 6. Logic High Output Current vs. Temperature.

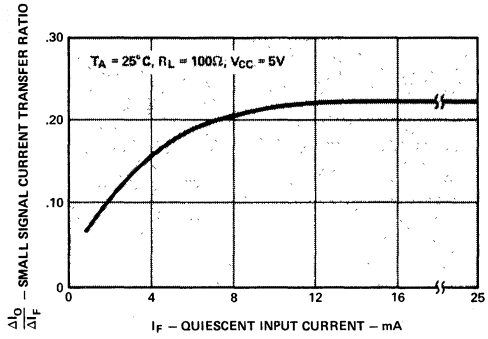
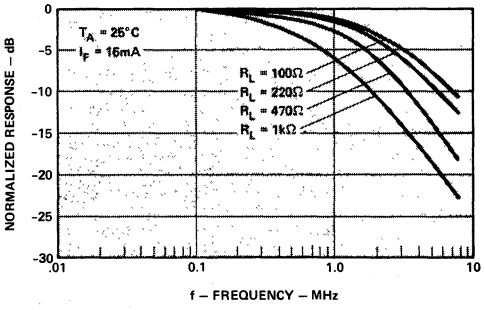


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



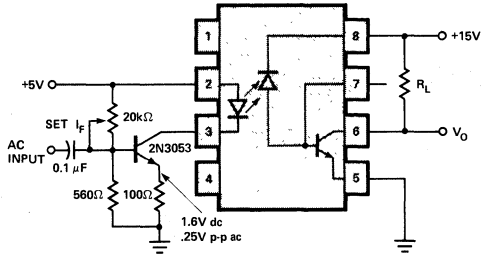


Figure 8. Frequency Response.

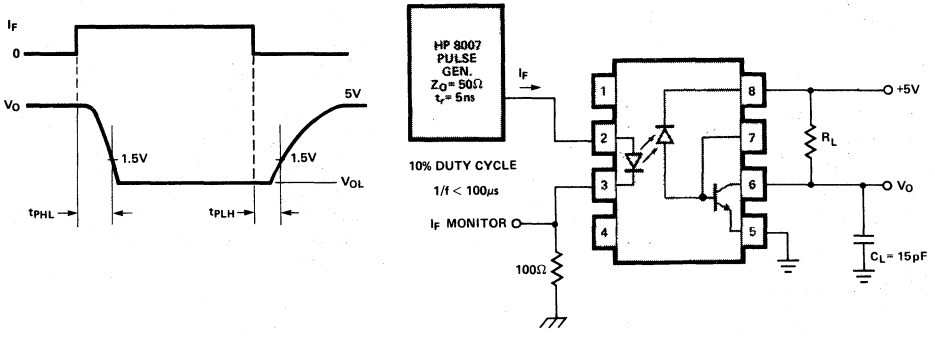
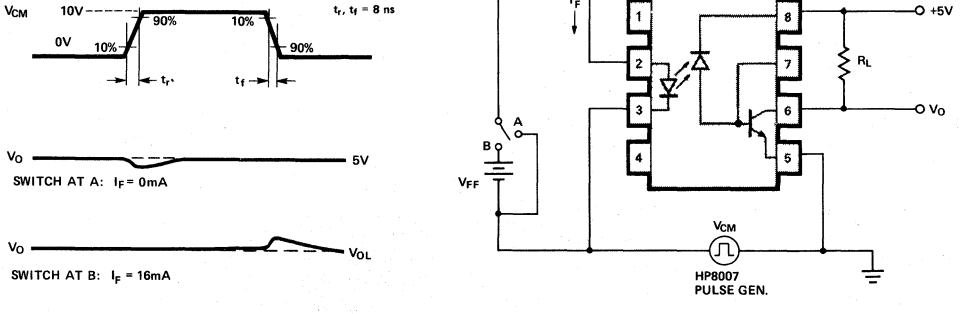


Figure 9. Switching Test Circuit.*



*JEDEC Registered Data

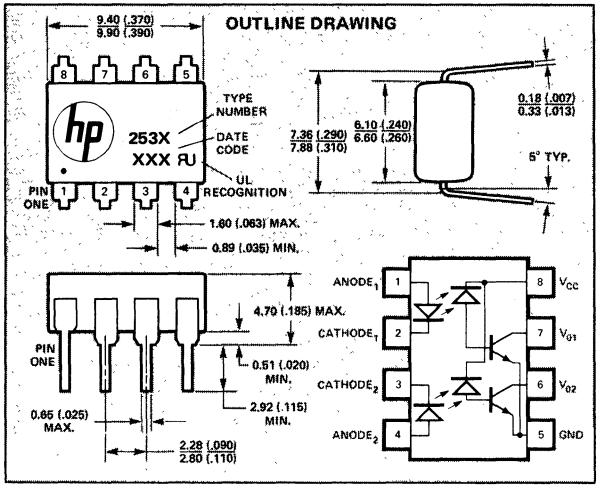
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

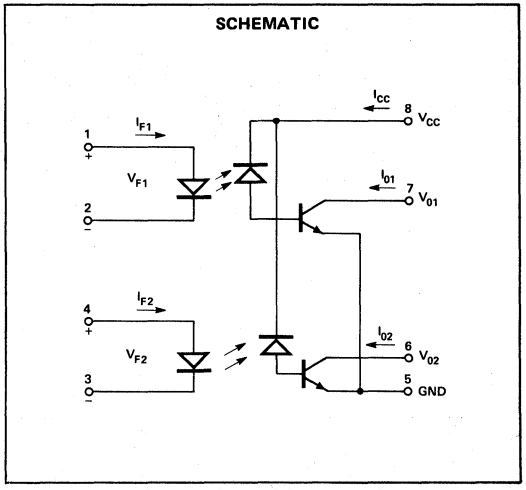
HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531

TECHNICAL DATA MARCH 1980





Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs**
- **HIGH DENSITY PACKAGING**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Description

The HCPL-2530/31 dual couplers contain a pair of light emitting diodes and integrated photon detectors with 3000V dc electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to +100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F (each channel) . . . . . 25mA[1]
Peak Input Current – I_F (each channel) . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage – V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . . 45mW[3]
Average Output Current – I_O (each channel) 8mA
Peak Output Current – I_O (each channel) 16mA
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 7,6-5)
. . . . . -0.5V to 15V
Output Power Dissipation (each channel) . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2530	7	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1,2	5,6
		2531	19	24		%			
		2530	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		2531	15	21		%			
Logic Low Output Voltage	V_{OL}	2530		0.1	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25°C		5
		2531		0.1	0.5	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25°C		
Logic High Output Current	I_{OH}			3	500	nA	T_A = 25°C, I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 5.5V	6	5
					250	µA	I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 5.5V		5
Logic Low Supply Current	I_{CCL}			80		µA	I_{F1} = I_{F2} = 16mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		5
Input Reverse Breakdown Voltage	V_R		5			V	I_F = 10µA, T_A = 25°C		5
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		5
Input - Output Insulation Leakage Current	I_{I-O}				1.0	µA	45% Relative Humidity, t = 5 s V_{I-O} = 3000Vdc, T_A = 25°C		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5 s V_{I-I} = 500Vdc		8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1MHz		8

**All typicals at 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2530		0.3	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	2530		0.4	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.3	0.8	µs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	2530		1000		V/µs	I_F =0mA, R_L=4.1kΩ, V_{CM}=10V_{p-p}	10	9,10,11
		2531		1000		V/µs	I_F=0mA, R_L=1.9kΩ, V_{CM}=10V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	2530		-1000		V/µs	V_{CM}=10V_{p-p}, R_L = 4.1kΩ	10	9,10,11
		2531		-1000		V/µs	V_{CM} = 10V_{p-p}, R_L = 1.9kΩ		
Bandwidth	BW			3		MHz	R_L = 100Ω	8	12

NOTES:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
11. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

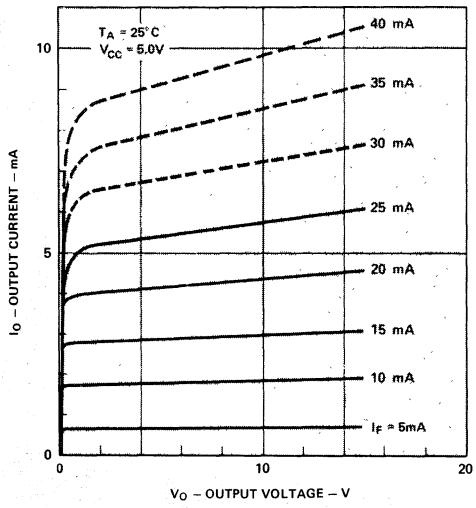


Figure 1. DC and Pulsed Transfer Characteristics.

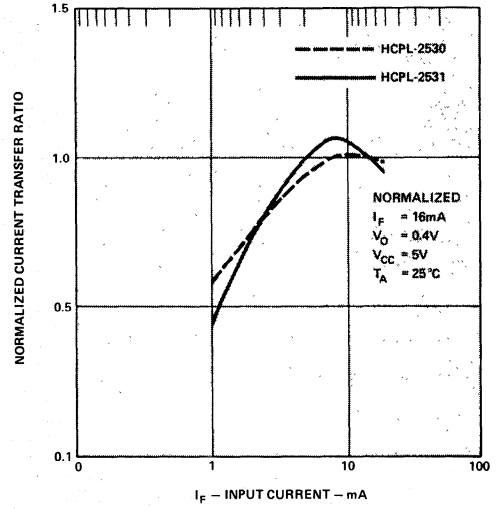


Figure 2. Current Transfer Ratio vs. Input Current.

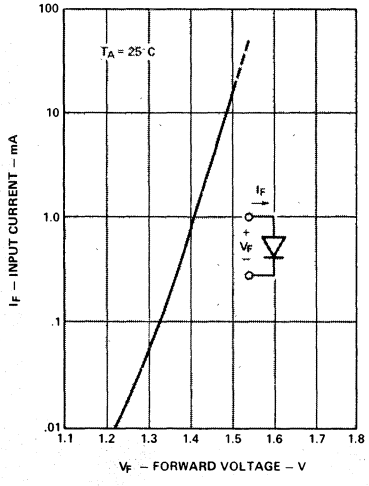


Figure 3. Input Current vs. Forward Voltage.

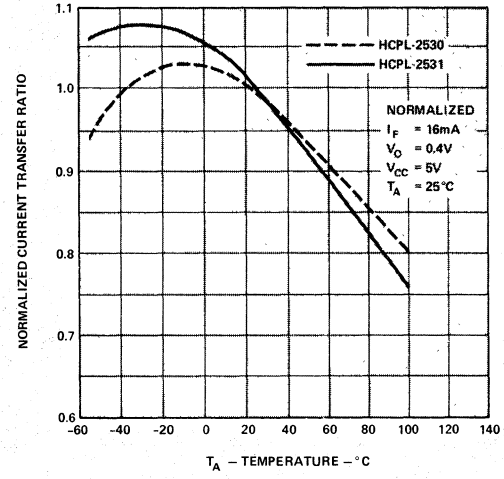


Figure 4. Current Transfer Ratio vs. Temperature.

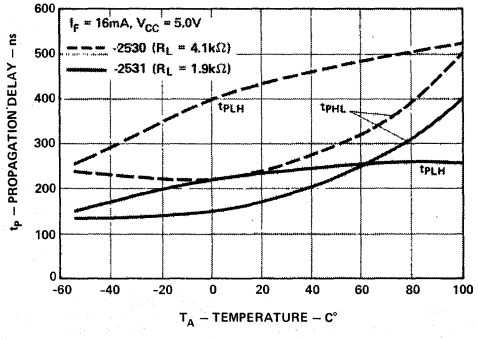


Figure 5. Propagation Delay vs. Temperature.

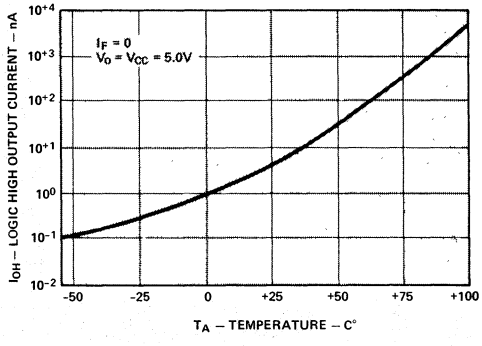


Figure 6. Logic High Output Current vs. Temperature.

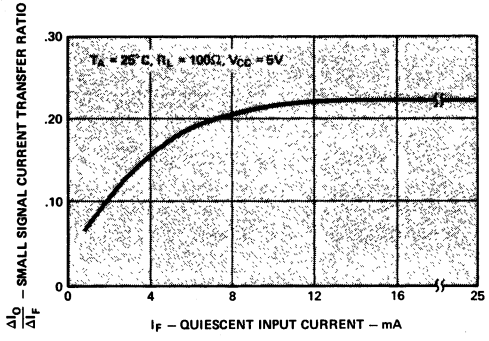


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

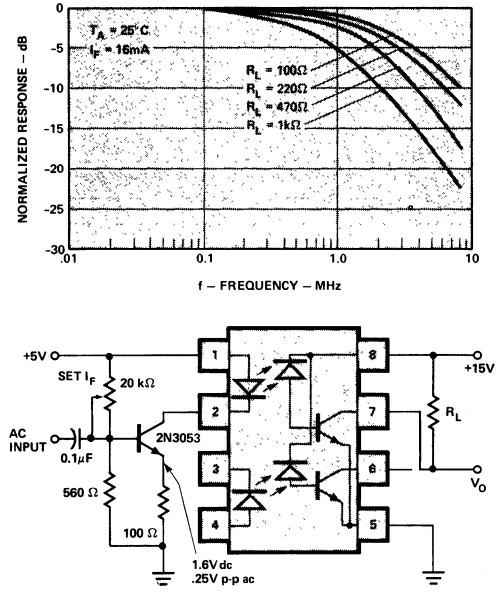


Figure 8. Frequency Response.

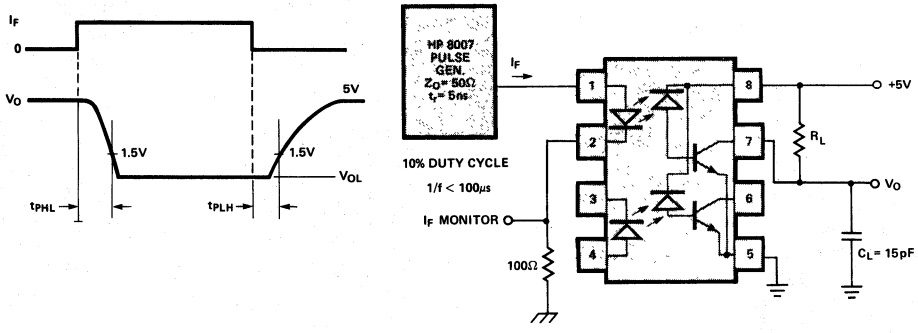


Figure 9. Switching Test Circuit.

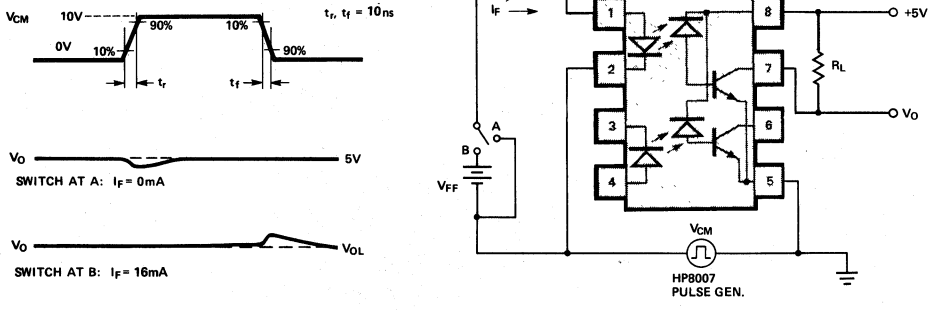


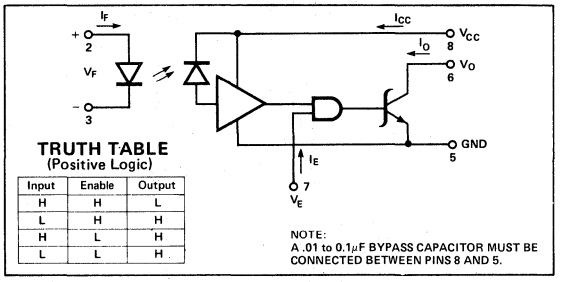
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LSTTL/TTL COMPATIBLE OPTOCOUPLER

6N137

TECHNICAL DATA MARCH 1980



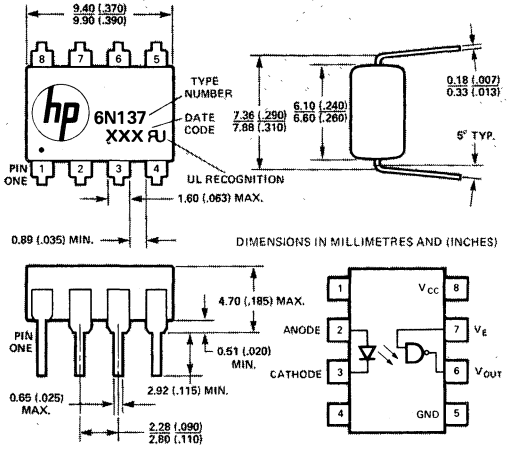
TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

NOTE:
A .01 to 0.1μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

Figure 1.

OUTLINE DRAWING*



Features

- **LSTTL/TTL COMPATIBLE: 5V SUPPLY**
- **ULTRA HIGH SPEED**
- **LOW INPUT CURRENT REQUIRED**
- **HIGH COMMON MODE REJECTION**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000 Vdc WITHSTAND TEST VOLTAGE**

Description Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3**	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current ..... 40mA (1≤ 1msec Duration)
Average Forward Input Current 20mA
Reverse Input Voltage 5V
Enable Input Voltage ..... 5.5V (Not to exceed V_{CC} by more than 500mV)
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O 50mA
Output Collector Power Dissipation 85mW
Output Voltage - V_O 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		50	250	μA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V	6	
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V I_{OL} (Sinking) =13mA	3,5	
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
Low Level Enable Current	I_{EL}*		-1.6	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Supply Current	I_{CCH}*		7	15	mA	V_{CC}=5.5V, I_F=0 V_E=0.5V		
Low Level Supply	I_{CCL}*		13	18	mA	V_{CC}=5.5V, I_F=10mA V_E=0.5V		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	Relative Humidity=45% T_A=25°C, t=5s V_{I-O}=3000Vdc		5
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V, T_A=25°C		5
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f=1MHz, T_A=25°C		5
Input Forward Voltage	V_F*		1.5	1.75	V	I_F=10mA, T_A=25°C	4	8
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		
Input Capacitance	C_{IN}		60		pF	V_F=0, f=1MHz		
Current Transfer Ratio	CTR		700		%	I_F=5.0mA, R_L=100Ω	2	7

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	1
Propagation Delay Time to Low Output Level	t_{PHL}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	2
Output Rise-Fall Time (10-90%)	t_r, t_f		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA		
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	3
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA V_{EH}=3.0V, V_{EL}=0.5V	8	4
Common Mode Transient Immunity at Logic High Output Level	CM_H		50		v/μs	V_{CM}=10V R_L=350Ω, V_O(min.)=2V, I_F=0mA	11	6
Common Mode Transient Immunity at Logic Low Output Level	CM_L		-150		v/μs	V_{CM}=10V R_L=350Ω, V_O(max.)=0.8V, I_F=5mA	11	6

*JEDEC Registered Data.

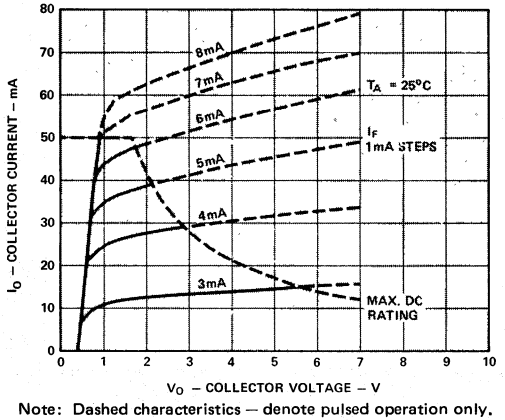
Operating Procedures and Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.



Note: Dashed characteristics — denote pulsed operation only.

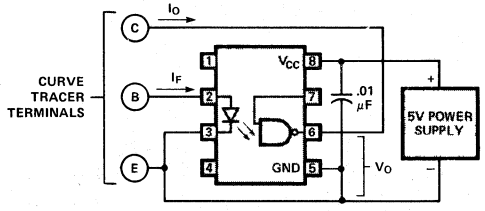
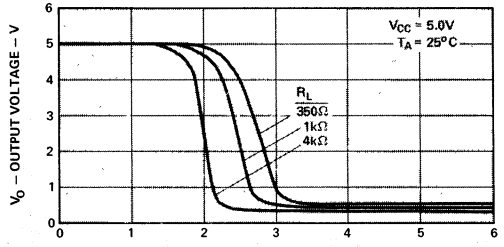


Figure 2. Optocoupler Collector Characteristics.



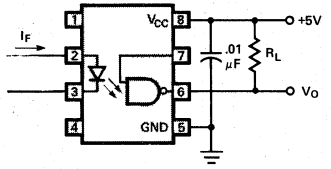


Figure 3. Input-Output Characteristics.

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.

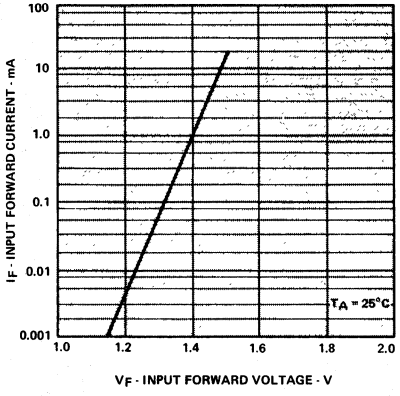


Figure 4. Input Diode Forward Characteristic.

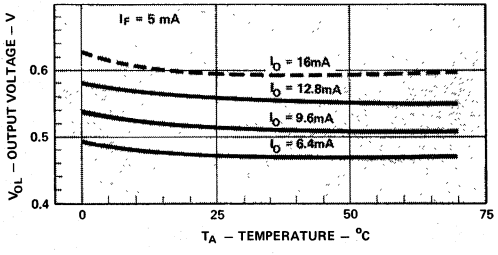


Figure 5. Output Voltage, V_{OL} vs. Temperature and Fan-Out.

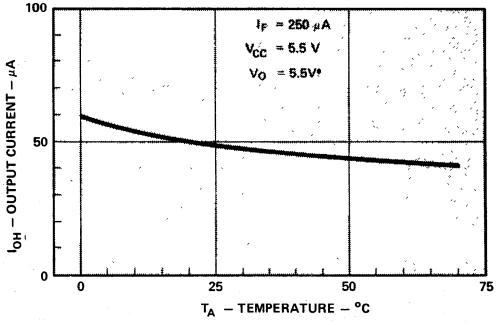


Figure 6. Output Current, I_{OH} vs. Temperature (I_F=250μA).

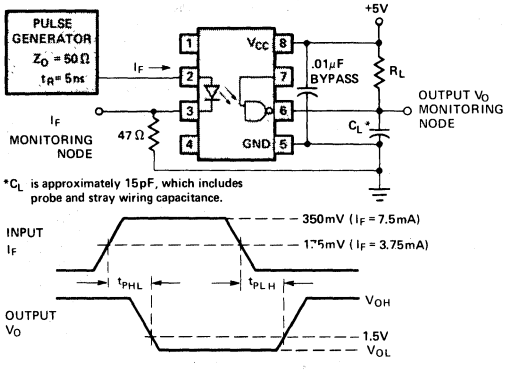


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.**

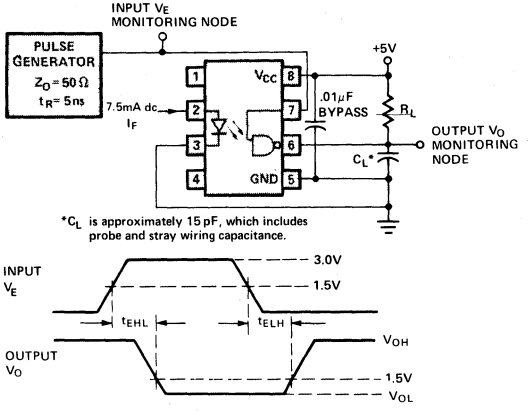


Figure 8. Test Circuit for t_{ELH} and t_{EHL}.

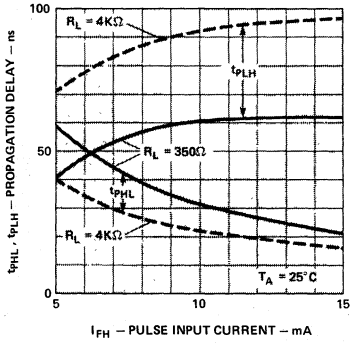


Figure 9. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

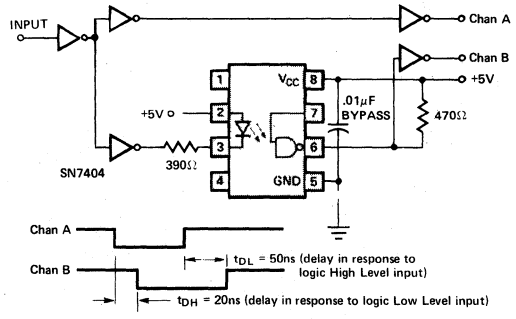
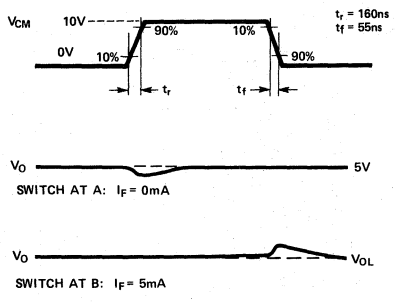


Figure 10. Response Delay Between TTL Gates.



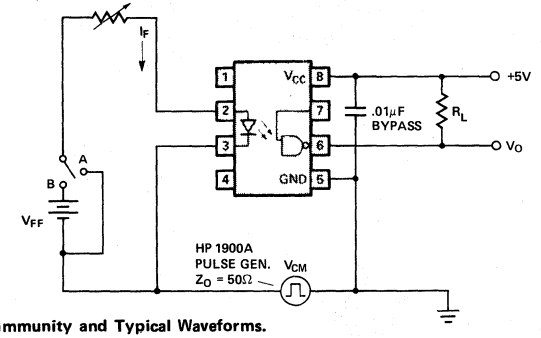


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

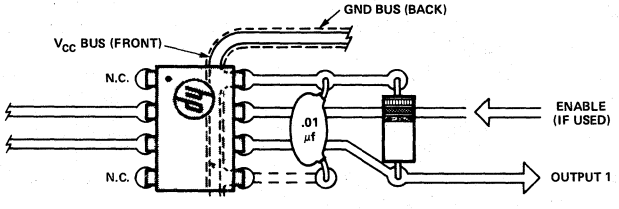


Figure 12. Recommended Printed Circuit Board Layout.

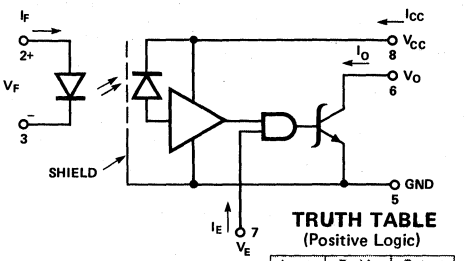
** JEDEC Registered Data.

HEWLETT PACKARD

HIGH CMR, HIGH SPEED OPTOCOUPLER

HCPL - 2601

TECHNICAL DATA MARCH 1980

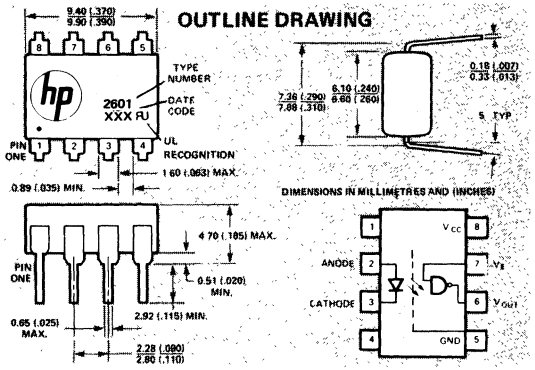


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Features

- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)**
- **HIGH SPEED**
- **GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **LSTTL/TTL COMPATIBLE**
- **LOW INPUT CURRENT REQUIRED: 5mA**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE: 0°C to 70°C**
- **STROBABLE OUTPUT**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000 Vdc WITHSTAND TEST VOLTAGE**

Description

The HCPL-2601 optically coupled gate combines a GaAsP light emitting diode and an integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 volts/μsec., equivalent to rejecting a 300 volt P-P sinusoid at 1 MHz.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL compatibility. The isolator D.C. operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance. This isolation is achieved with a typical propagation delay of 35 nsec.

The HCPL-2601's are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Switching Power Supply
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current − I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage − V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage − V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current − I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage − V_O ..... 7 V

*6.3 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0°C to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		7	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 μA, V_E = 2.0 V	2	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5V, I_F = 5 mA V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	3,5	
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5V, I_F = 0, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		15	18	mA	V_{CC} = 5.5V, I_F = 10 mA, V_E = 0.5 V		
Low Level Enable Current	I_{EL}		−1.6	−2.0	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Current	I_{EH}		−1.0		mA	V_{CC} = 5.5 V, V_E = 2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10 mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.6		mV/°C	I_F = 10 mA		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45% T_A = 25°C, t = 5 s, V_{I-O} = 3000 Vdc		3
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output level	t_{PLH}		35	75	ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		35	75	ns		6	5
Output Rise Time (10–90%)	t_r		25		ns			
Output Fall Time (90–10%)	t_f		15		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 350 Ω, I_F = 0 mA	12	8,10
Common Mode Transient Immunity at Low Output Level	CM_L	−1000	−10,000		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA	12	9,10

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} <0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.

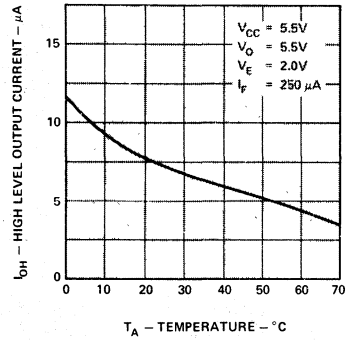


Figure 2. High Level Output Current vs. Temperature.

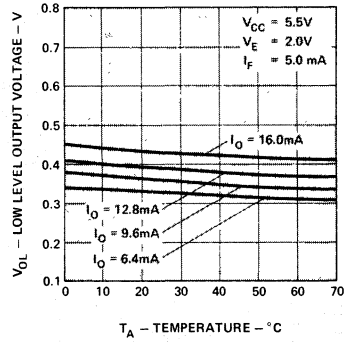


Figure 3. Low Level Output Voltage vs. Temperature.

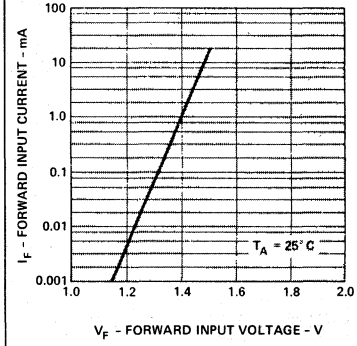


Figure 4. Input Diode Forward Characteristic.

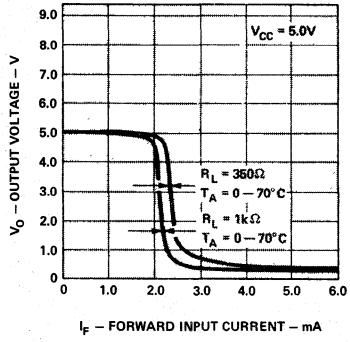


Figure 5. Output Voltage vs. Forward Input Current.

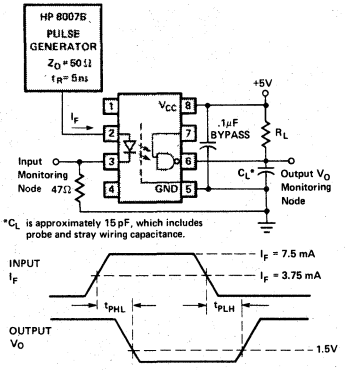


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

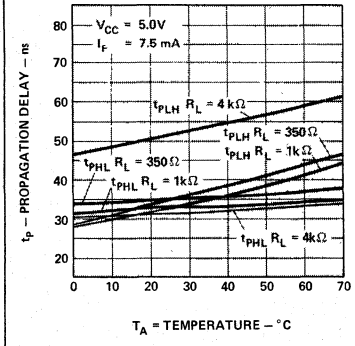


Figure 7. Propagation Delay vs. Temperature.

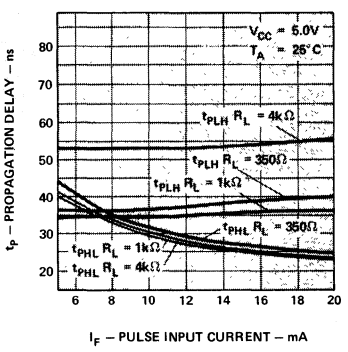


Figure 8. Propagation Delay vs. Pulse Input Current.

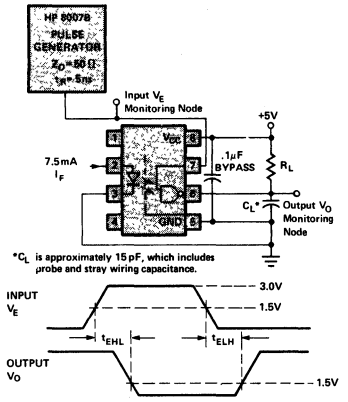


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

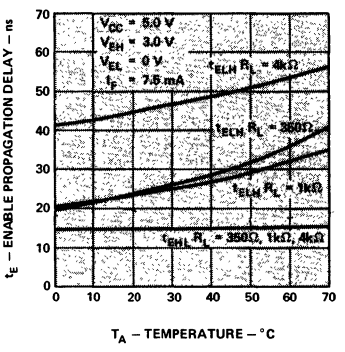


Figure 10. Enable Propagation Delay vs. Temperature.

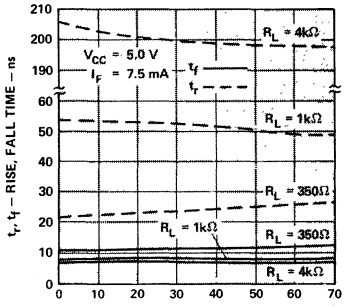


Figure 11. Rise, Fall Time vs. Temperature.

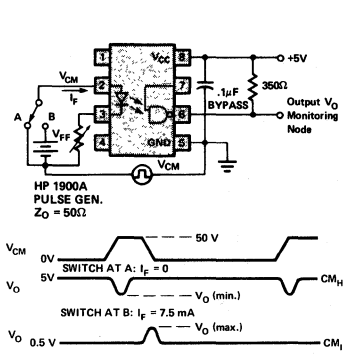


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

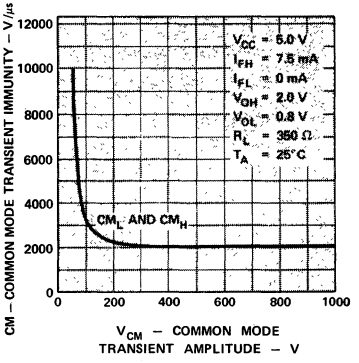


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

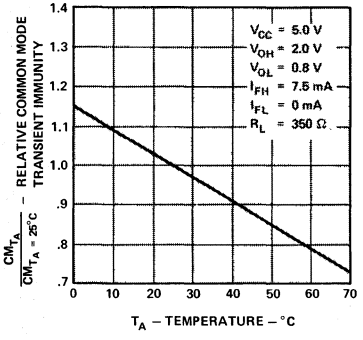


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

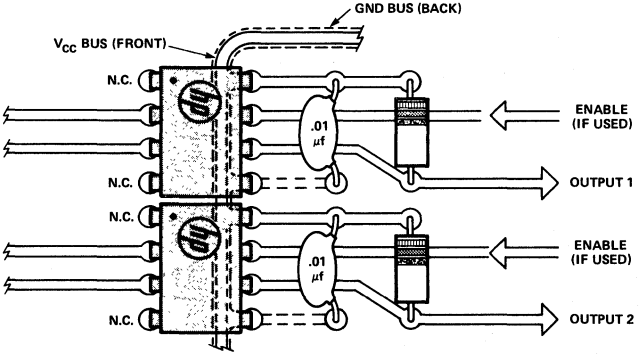


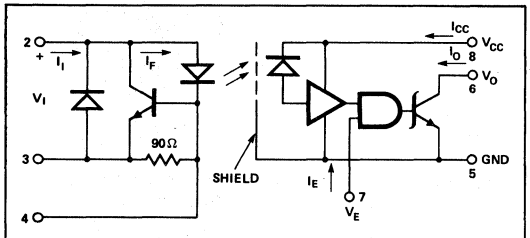
Figure 15. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

HIGH CMR LINE RECEIVER OPTOCOUPLER

HCPL-2602

TECHNICAL DATA MARCH 1980



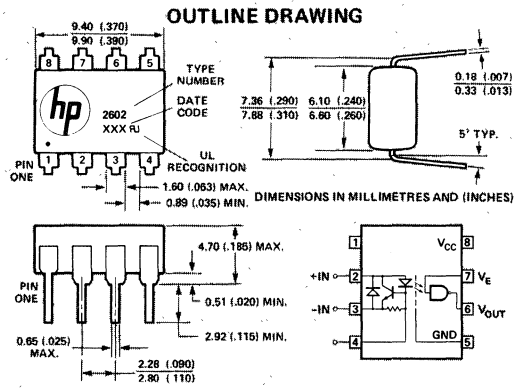
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

OUTLINE DRAWING



Features

- **LINE TERMINATION INCLUDED — NO EXTRA CIRCUITRY REQUIRED**
- **ACCEPTS A BROAD RANGE OF DRIVE CONDITIONS**
- **GUARDBANDED FOR LED DEGRADATION**
- **LED PROTECTION MINIMIZES LED EFFICIENCY DEGRADATION**
- **HIGH SPEED — 10Mbs (LIMITED BY TRANSMISSION LINE IN MANY APPLICATIONS)**
- **INTERNAL SHIELD PROVIDES EXCELLENT COMMON MODE REJECTION**
- **EXTERNAL BASE LEAD ALLOWS "LED PEAKING" AND LED CURRENT ADJUSTMENT**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Description

The HCPL-2602 optically coupled line receiver combines a GaAsP light emitting diode, an input current regulator and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000V/μsec, equivalent to rejecting a 300V P-P sinusoid at 1 MHz.

DC specifications are defined similar to TTL logic and are guaranteed from 0° C to 70° C allowing trouble free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

The HCPL-2602's are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0° C to +70° C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		7	250	μA	V_{CC} = 5.5V, V_O = 5.5V I_I=250 μA, V_E=2.0V	4	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC}=5.5V, I_I=5 mA V_E=2.0V, I_{OL} (Sinking)=13 mA	2,5	2
Input Voltage	V_I		2.0	2.4	V	I_I=5 mA	3	
			2.3	2.7		I_I=60 mA	3	
Input Reverse Voltage	V_R		0.75	0.95	V	I_R=5 mA		
Low Level Enable Current	I_{EL}		-1.6	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC}=5.5V, I_I=0, V_E=0.5V		
Low Level Supply Current	I_{CCL}		16	19	mA	V_{CC}=5.5V, I_I=60 mA V_E=0.5V		
Input Capacitance	C_{IN}		90		pF	V_I=0, f=1 MHz, (PIN 2-3)		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity=45% T_A=25° C, t=5 s, V_{I-O}=3000 Vdc		3
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25° C.

Switching Characteristics

(T_A = 25° C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		45	75	ns	R_L = 350 Ω C_L = 15 pF I_I = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		45	75	ns		6	5
Output Rise Time (10-90%)	t_r		25		ns			
Output Fall Time (90-10%)	t_f		15		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15 pF, I_I=7.5 mA, V_{EH}=3 V, V_{EL}=0 V	10	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns		10	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM}=50 V (peak), V_O (min.)=2 V, R_L=350Ω, I_I=0 mA	12	8
Common Mode Transient Immunity at Low Output Level	CM_L	-1000	-10,000		V/μs	V_{CM}=50 V (peak), V_O (max.)=0.8 V, R_L=350Ω, I_I=7.5 mA	12	9

Using the HCPL-2602 Line Receiver Optocoupler

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602, in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602's, or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leqslant 16t$
where C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

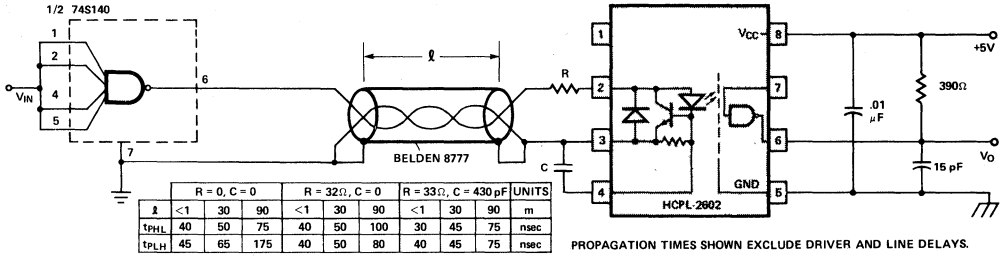
Use of additional logic at the output of two HCPL-2602's operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

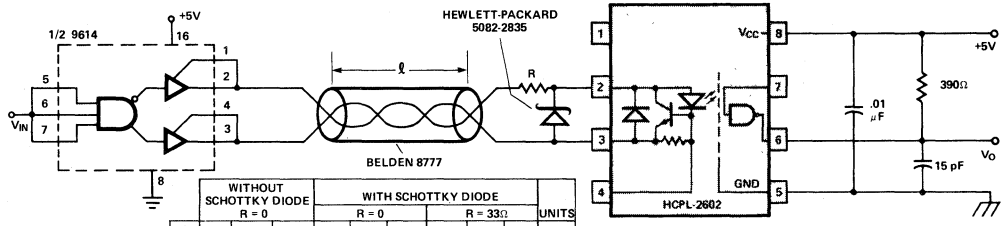
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602. Most drivers also have characteristics allowing the HCPL-2602 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

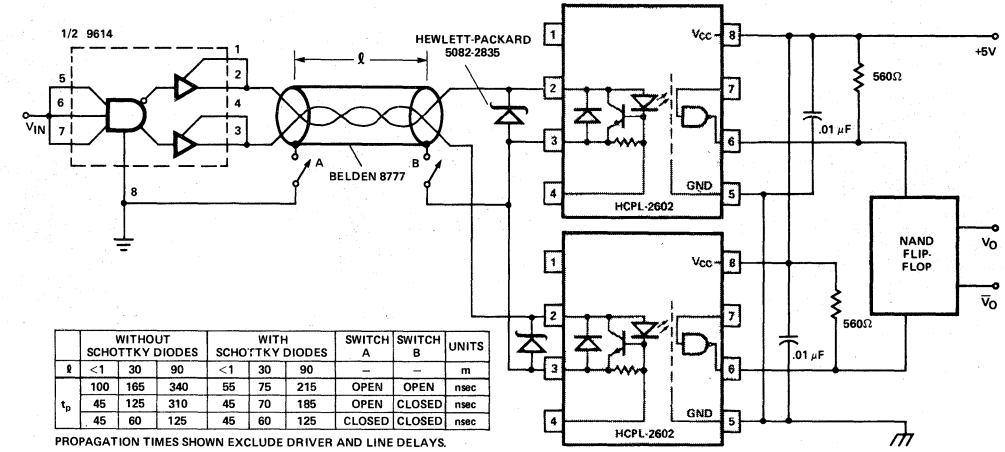
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

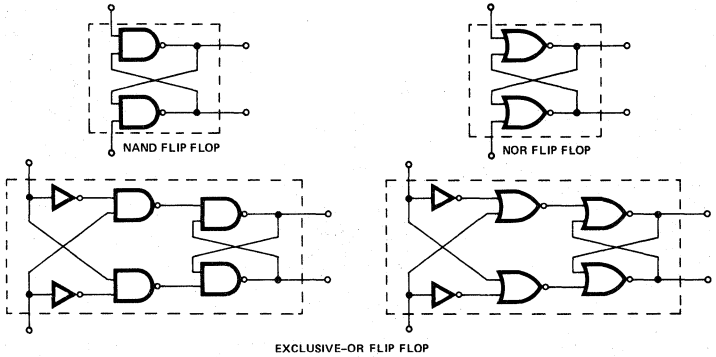
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	30	90	<1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip Flop Configurations.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level	I_{IH}	5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s (1.6mm below seating plane)
Forward Input Current — I_I ..... 60 mA
Reverse Input Current ..... 60 mA
Supply Voltage — V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage — V_E ..... 5.5 V (Not to exceed V_{CC} by more than 500 mV)
Output Collector Current — I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage — V_O ..... 7 V
Input Current, Pin 4 ..... ±10 mA

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. The HCPL-2602 is tested such that operation at I_I minimum of 5 mA will provide the user a minimum of 20% guardband for LED light output degradation.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} <0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.

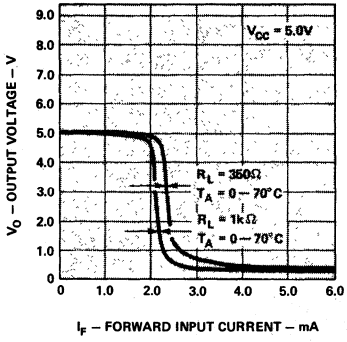


Figure 2. Output Voltage vs. Forward Input Current.

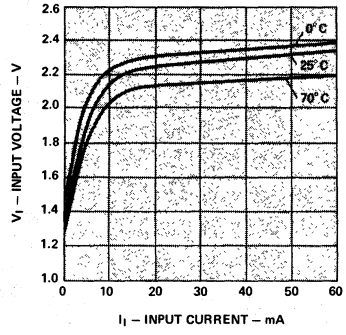


Figure 3. Input Characteristics.

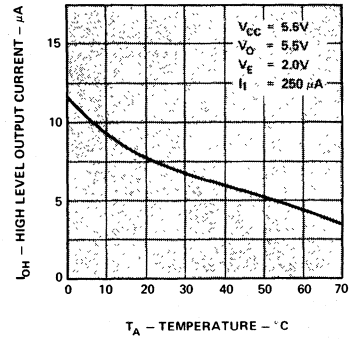


Figure 4. High Level Output Current vs. Temperature.

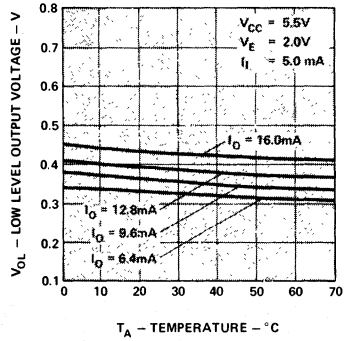


Figure 5. Low Level Output Voltage vs. Temperature.

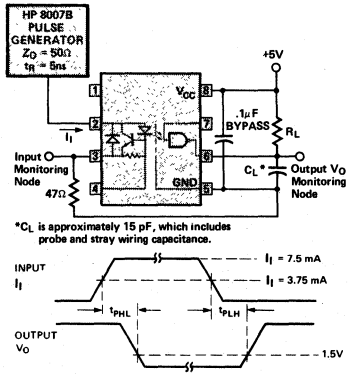


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

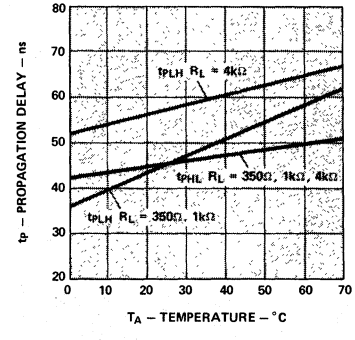


Figure 7. Propagation Delay vs. Temperature.

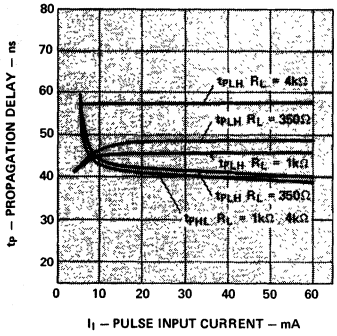


Figure 8. Propagation Delay vs. Pulse Input Current.

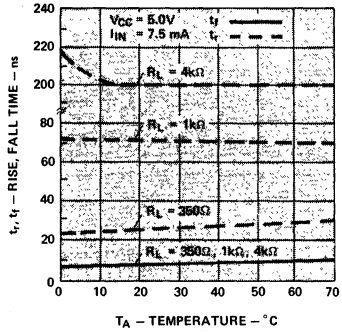


Figure 9. Rise, Fall Time vs. Temperature.

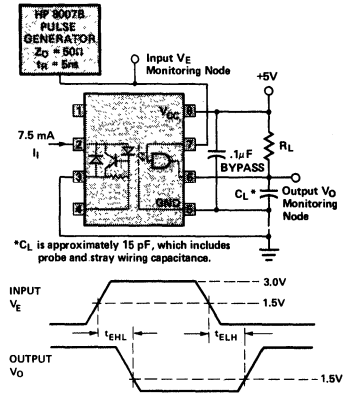


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

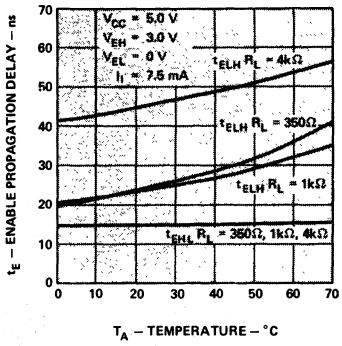


Figure 11. Enable Propagation Delay vs. Temperature.

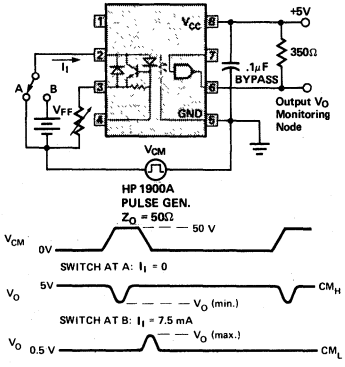


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

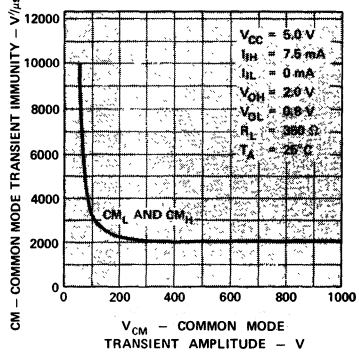


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

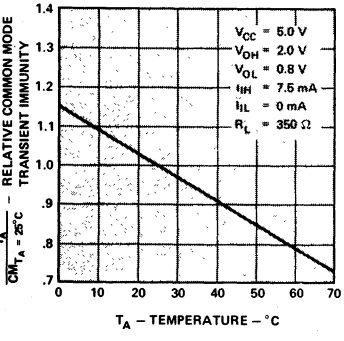


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

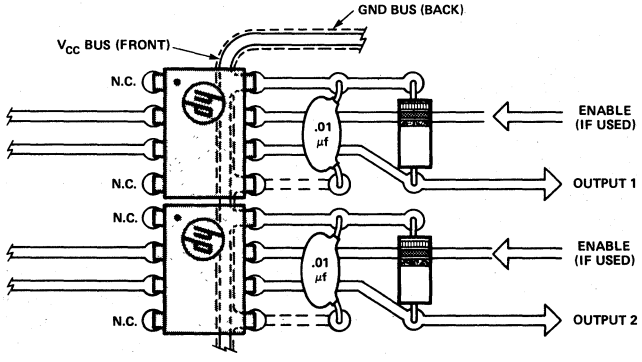


Figure 15. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

TECHNICAL DATA MARCH 1980

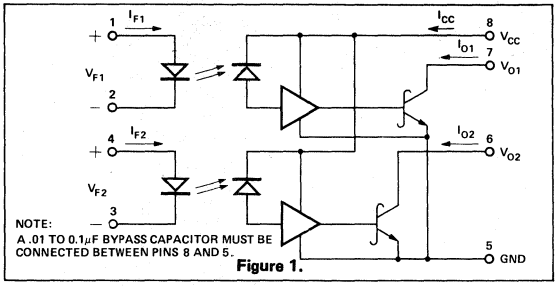


Figure 1.

Features

- HIGH DENSITY PACKAGING
- DTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- 3000Vdc WITHSTAND TEST VOLTAGE

Description/Applications

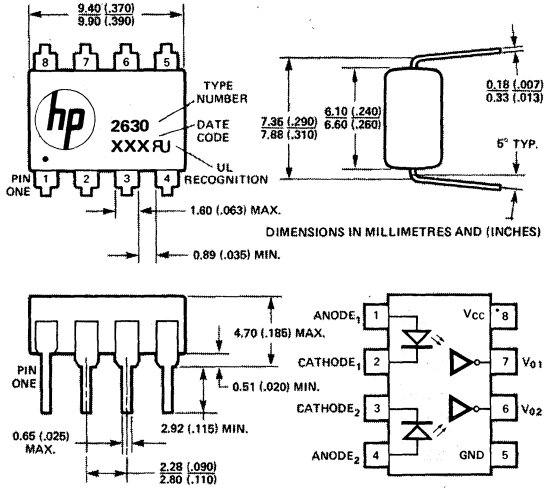
The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving DTL/TTL circuit compatibility. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 50 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.

OUTLINE DRAWING



Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Peak Forward Input
Current (each channel) ..... 30mA (≤ 1 msec Duration)
Average Forward Input Current (each channel) 15mA
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O (each channel) ..... 16 mA
Output Voltage - V_O (each channel) 7V
Output Collector Power Dissipation ..... 60 mW

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		50	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		3
Low Level Output Voltage	V_{OL}		0.5	0.6	V	V_{CC} = 5.5V, I_F = 5mA I_{OL} (Sinking) = 13mA	3	3
High Level Supply Current	I_{CCH}		14	30	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply	I_{CCL}		26	36	mA	V_{CC} = 5.5V, I_F = 10mA (Both Channels)		
Input – Output Insulation Leakage Current	I_{I-O}			1.0	μA	Relative Humidity = 45% T_A = 25°C, t = 5s, V_{I-O} = 3000Vdc		4
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V, T_A = 25°C		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1MHz, T_A = 25°C		4
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10mA, T_A = 25°C	4	7,3
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		3
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45%, t=5s, V_{I-I}=500V		8
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500V		8
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1MHz		8
Current Transfer Ratio	CTR		700		%	I_F = 5.0mA, R_L = 100Ω	2	6

*All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

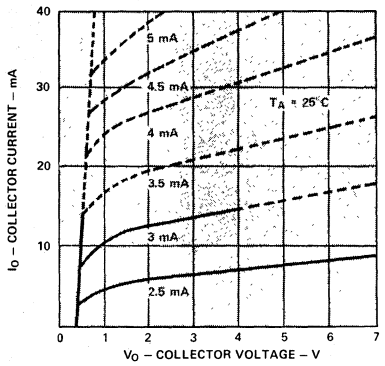
EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		55	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	1
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	2
Output Rise-Fall Time (10-90%)	t_r, t_f		25		ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA		
Common Mode Transient Immunity at High Output Level	CM_H		50		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (min.) = 2V, I_F = 0mA	9	5
Common Mode Transient Immunity at Low Output Level	CM_L		-150		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (max.) = 0.8V I_F = 7.5mA	9	5

NOTE: It is essential that a bypass capacitor (.01μF to 0.1μF, ceramic) be connected from pin 8 to pin 5. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm. Failure to provide the bypass may impair the switching properties (Figure 5).

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
7. At 10mA VF decreases with increasing temperature at the rate of 1.9mV/°C.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.



NOTE: Dashed characteristics indicate pulsed operation.

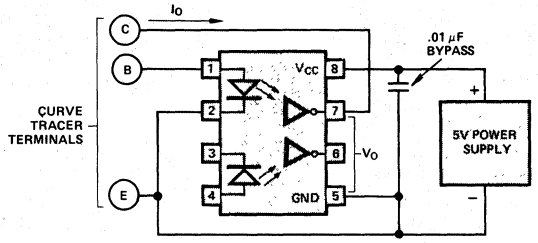
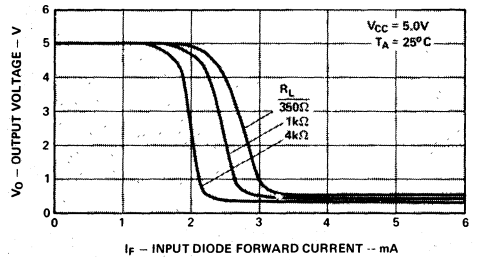


Figure 2. Optocoupler Transfer Characteristics.



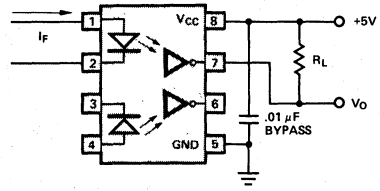


Figure 3. Input-Output Characteristics.

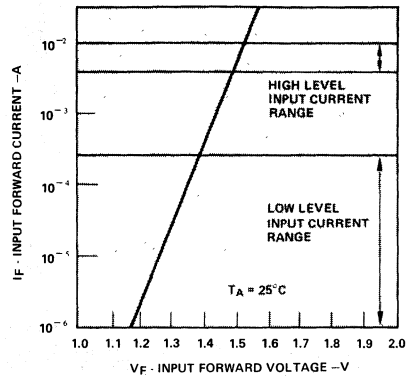


Figure 4. Input Diode Forward Characteristic

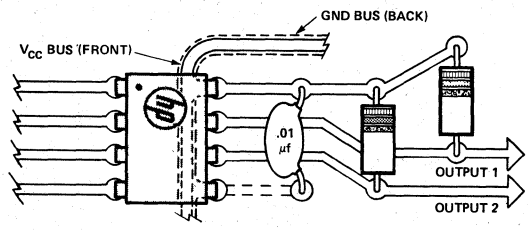


Figure 5. Recommended Printed Circuit Board Layout.

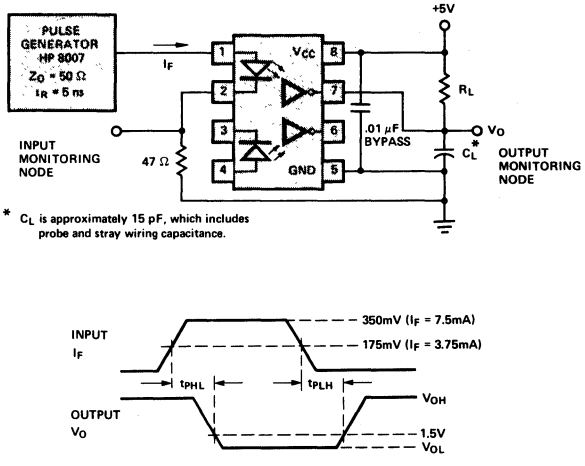


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

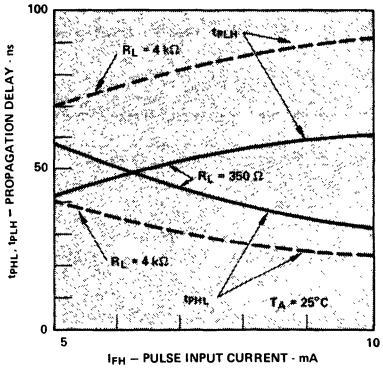


Figure 7. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

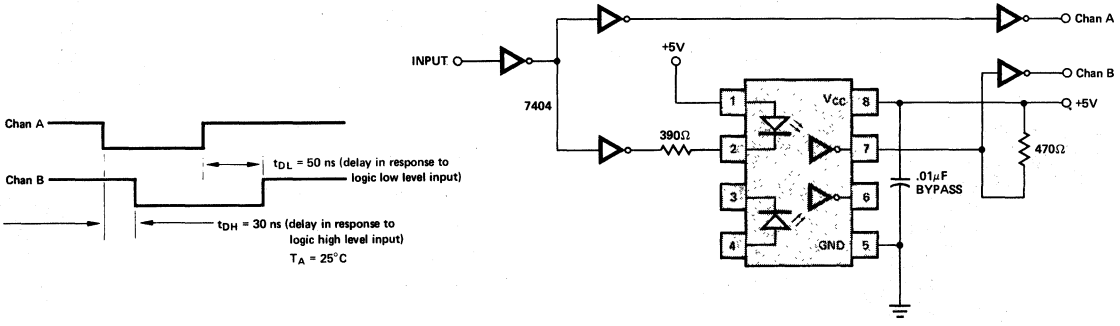


Figure 8. Response Delay Between TTL Gates.

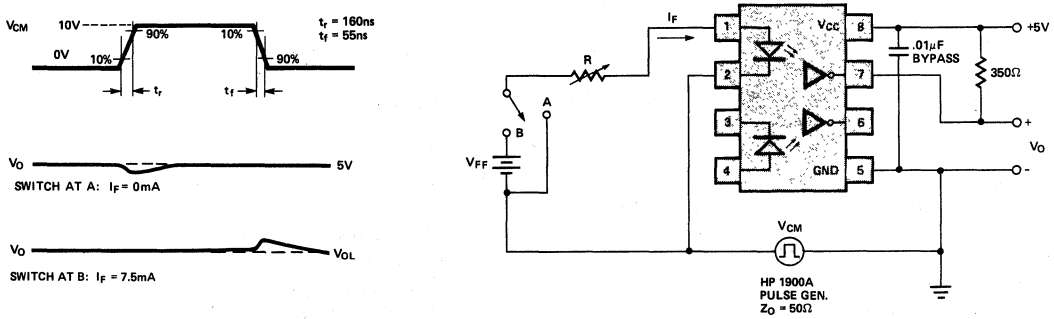


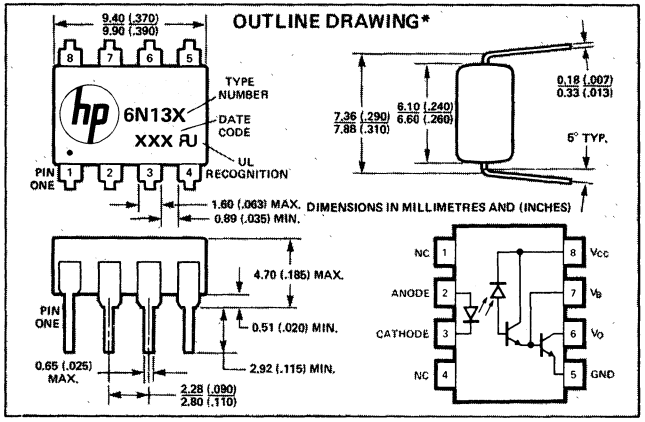
Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

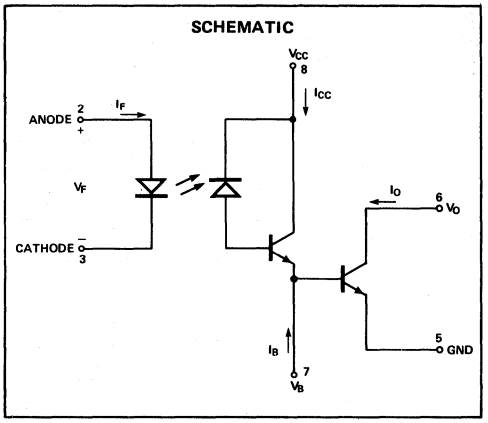
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA MARCH 1980





Features

- **HIGH CURRENT TRANSFER RATIO — 800% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5mA**
- **TTL COMPATIBLE OUTPUT — 0.1V V_{OL}**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **HIGH COMMON MODE REJECTION — 500V/μs**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0°C to 70°C**
- **BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT**
- **HIGH OUTPUT CURRENT — 60mA**
- **DC TO 1M bit/s OPERATION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LTTL/TTL, CMOS/LTTL
- Low Input Current Line Receiver – Long Line or Partyline
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide 3000V dc electrical insulation, 500V/μs common mode transient immunity and extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is suitable for use in CMOS, LTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5mA of LED current.

The 6N138 is suitable for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6mA [1 TTL unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. in, 1 U.L. out with a 2.2 kΩ pull-up resistor.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Storage Temperature ..... –55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F ..... 20mA [1]
Peak Input Current – I_F 40mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current – I_F 1.0A
(≤ 1μs pulse width, 300 pps)
Reverse Input Voltage – V_R 5V
Input Power Dissipation ..... 35mW [2]
Output Current – I_O (Pin 6) ..... 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) 0.5V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 .....–0.5 to 7V
6N139 .....–0.5 to 18V
Output Power Dissipation ..... 100mW [4]

See notes, following page.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N139	400 500	800 900		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	3	5,6
		6N138	300	600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1,2	6
		6N138		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*	6N139		0.05	100	μA	I_F = 0mA, V_O = V_{CC} = 18V		6
		6N138		0.1	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.2		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R*		5		V		I_R = 10μA, T_A=25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.8		mV/°C	I_F = 1.6mA		
Input Capacitance	C_{IN}			60		pF	f=1MHz, V_F = 0		
Input – Output Insulation Leakage Current	I_{I-O}*				1.0	μA	45% Relative Humidity, T_A = 25°C t = 5 s, V_{I-O} = 3000Vdc		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f=1MHz		7

**All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A= 25°C

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N139		5 0.2	25 1	μs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		1	10	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N139		5 1	60 7	μs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		4	35	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/μs	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10
Common Mode Transient Immunity at Logic Low Level Output	CM_L			−500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
10. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.

*JEDEC Registered Data.

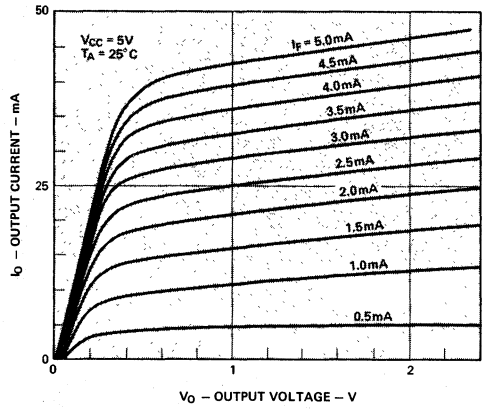


Figure 1. 6N139 DC Transfer Characteristics.

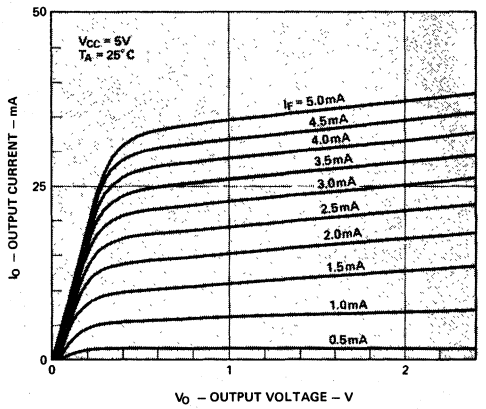


Figure 2. 6N138 DC Transfer Characteristics.

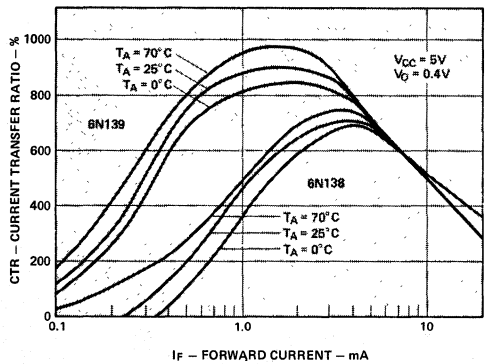


Figure 3. Current Transfer Ratio vs. Forward Current.

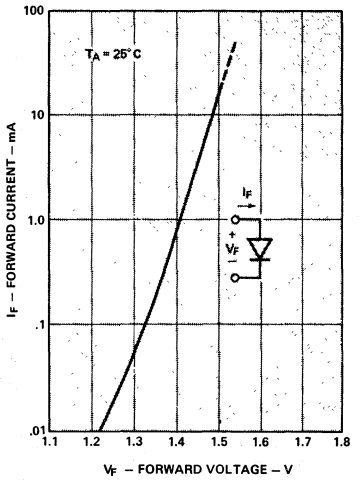


Figure 4. Input Diode Forward Current vs. Forward Voltage.

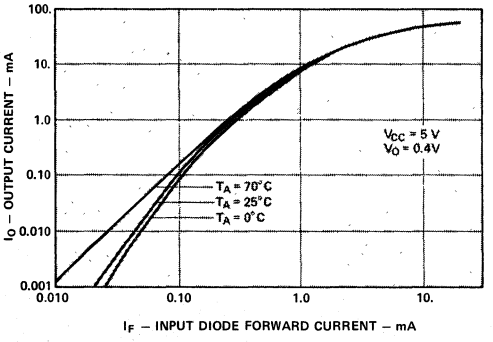


Figure 5. 6N139 Output Current vs. Input Diode Forward Current.

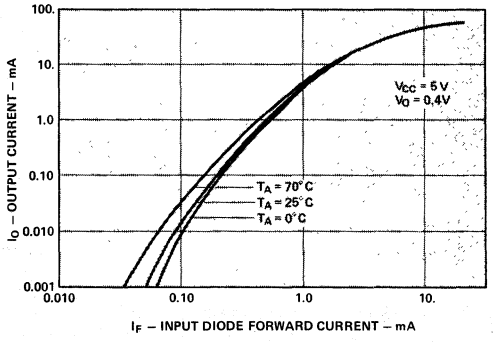


Figure 6. 6N138 Output Current vs. Input Diode Forward Current.

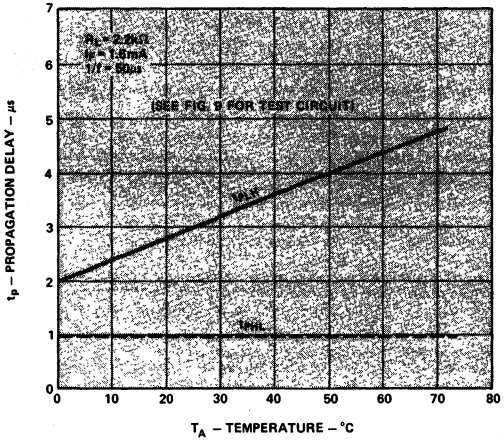


Figure 7. Propagation Delay vs. Temperature.

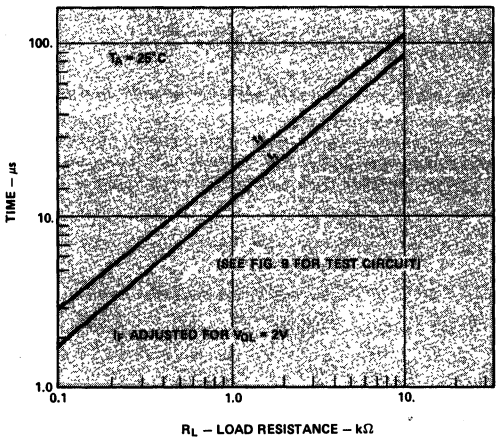


Figure 8. Non Saturated Rise and Fall Times vs. Load Resistance.

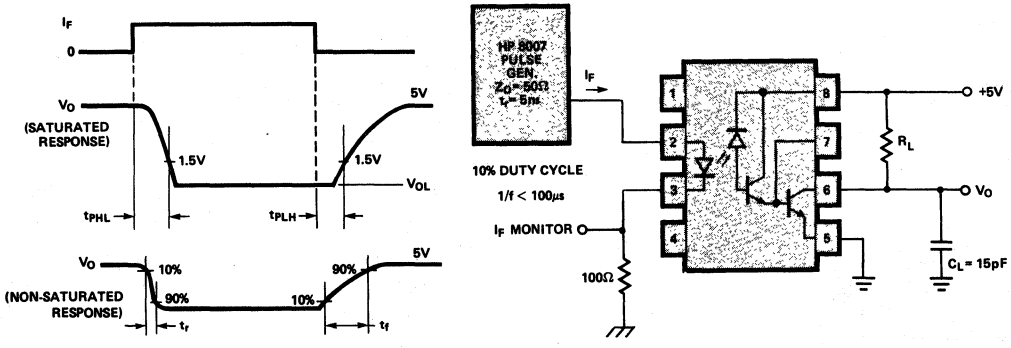


Figure 9. Switching Test Circuit.*

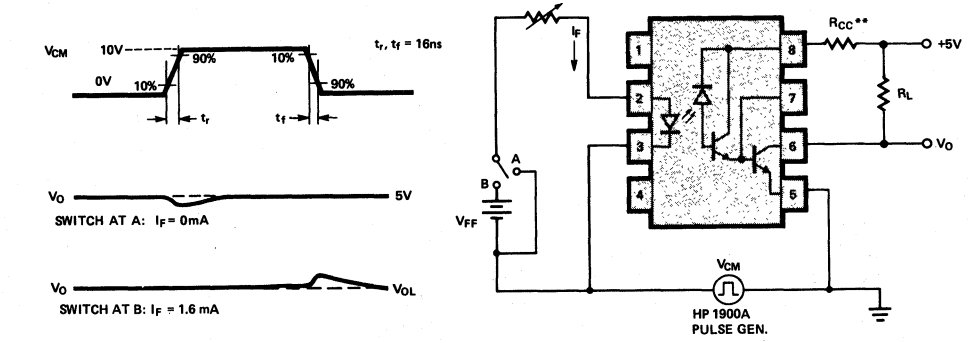


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.

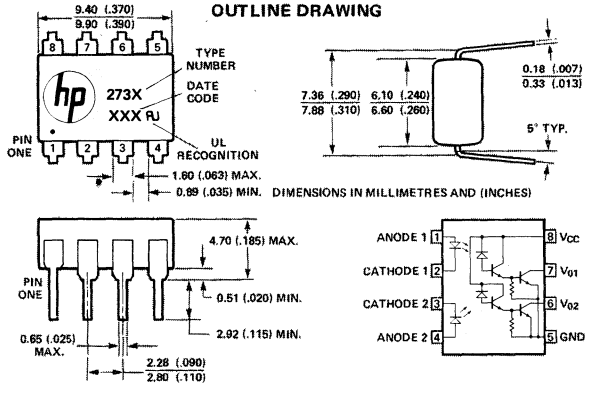
**See Note 10

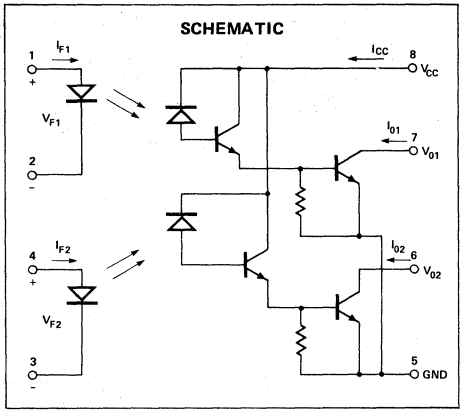
HEWLETT PACKARD

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730
HCPL-2731

TECHNICAL DATA MARCH 1980





Features

- **HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **LOW OUTPUT SATURATION VOLTAGE — 1.0V TYPICAL**
- **HIGH DENSITY PACKAGING**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE**
- **HIGH COMMON MODE REJECTION**
- **DATA RATES UP TO 200K BIT/s**
- **HIGH FANOUT**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361).**

Applications

- **Digital Logic Ground Isolation**
- **Telephone Ring Detector**
- **EIA RS-232C Line Receiver**
- **Low Input Current Line Receiver — Long Line or Partyline**
- **Microprocessor Bus Isolation**
- **Current Loop Receiver**
- **Polarity Sensing**
- **Level Shifting**
- **Line Voltage Status Indicator — Low input Power Dissipation**

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photon detectors. They provide extremely high current transfer ratio, 3000V dc electrical insulation and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type isolators. The separate V_{CC} pin can be strobed low as an output disable. In addition V_{CC} may be as low as 1.6V without adversely affecting the parametric performance.

Guaranteed operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 1.6 mA and has a 7V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing with an input current of only 1.6 mA.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation.

Electrical Specifications

(Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400 500	1000 1100		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	6,7
		2730	300	1000		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	
Logic Low Output Voltage	V_{OL}	2731		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 8mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1	6
		2730		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}	2731		0.005	100	μA	I_F = 0 mA, V_O = V_{CC} = 18V		6
		2730		0.01	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}	2731		1.2		mA	I_{F1} = I_{F2} = 1.6mA, V_{CC} = 18V		
		2730		0.9			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Logic High Supply Current	I_{CCH}	2731		5		nA	I_{F1} = I_{F2} = 0mA, V_{CC} = 18V		
		2730		4			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Input Forward Voltage	V_F			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	6
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 μA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation Leakage Current	I_{I-O}				1.0	μA	45% Relative Humidity, T_A = 25°C t = 5s, V_{I-O} = 3000 Vdc		8
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		8
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t=5s, V_{I-I} = 500Vdc		9
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		9
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C

Switching Specifications at T_A=25°C

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2731		25	100	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	
		2730/1		5 0.5	20 2	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}	2731		20	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	
		2730/1		10 1	35 10		I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/μs	I_F = 0mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = 10V_{p-p}	10	10,11
Common Mode Transient Immunity at Logic Low Level Output	CM_L			-500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = 10V_{p-p}	10	10,11

NOTES:
1. Derate linearly above 50°C free-air temperature at a rate of 0.5mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.9mW/°C.
3. Derate linearly above 35°C free-air temperature at a rate of 0.6mA/°C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35°C free-air temperature at a rate of 1.7mW/°C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.3\ I_F\ (mA)}$ kΩ.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 sec
(1.6mm below seating plane)
Average Input Current — I_F
(each channel) ..... 20 mA[1]
Peak Input Current — I_F
(each channel) ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R
(each channel) 5V
Input Power Dissipation
(each channel) ..... 35 mW[2]
Output Current — I_O
(each channel) ..... 60 mA[3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5)[4]
HCPL-2730 ..... -0.5 to 7V
HCPL-2731 ..... -0.5 to 18V
Output Power Dissipation
(each channel) ..... 100 mW[5]

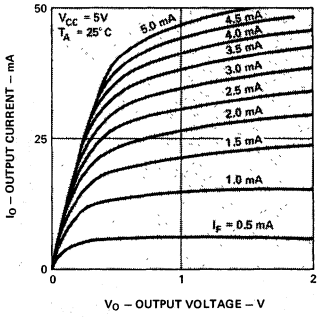


Figure 1. DC Transfer Characteristics.

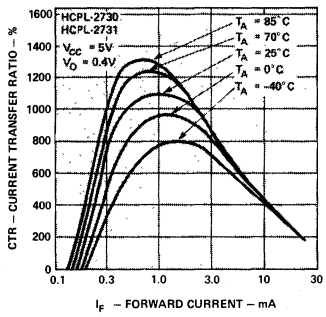


Figure 2. Current Transfer Ratio vs. Forward Current.

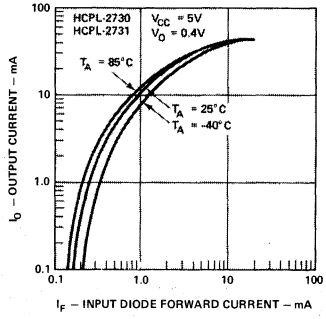


Figure 3. Output Current vs. Input Diode Forward Current.

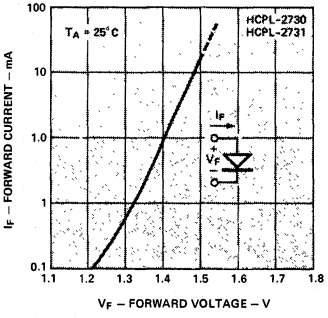


Figure 4. Input Diode Forward Current vs. Forward Voltage.

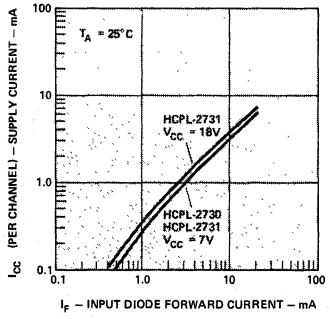


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

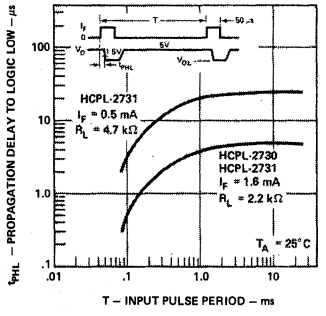


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

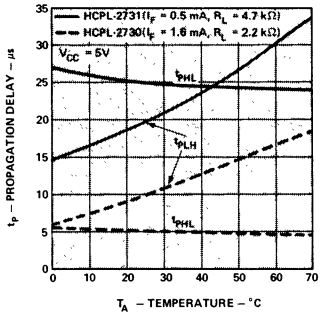


Figure 7. Propagation Delay vs. Temperature.

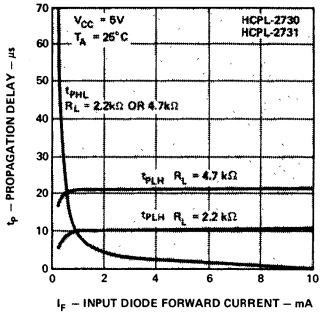
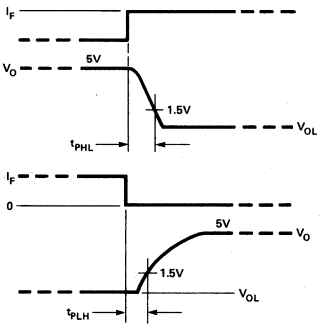


Figure 8. Propagation Delay vs. Input Diode Forward Current.



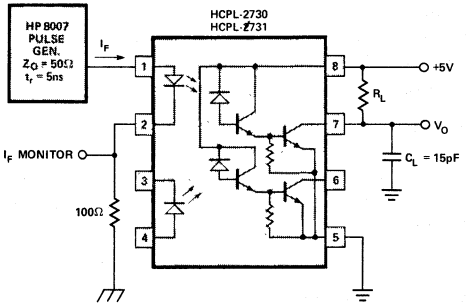
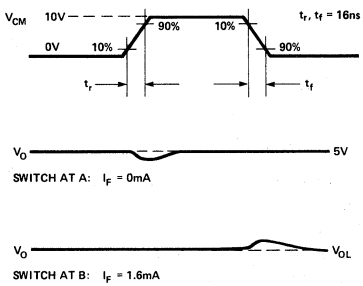
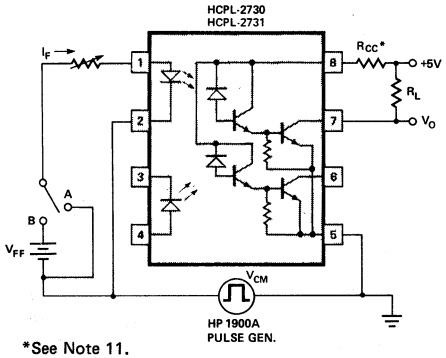


Figure 9. Switching Test Circuit.





*See Note 11.

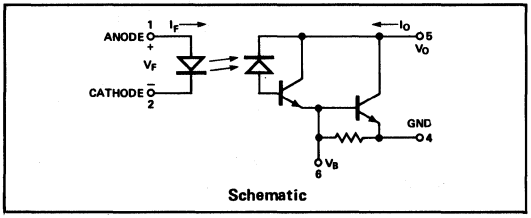
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46

TECHNICAL DATA MARCH 1980



Features

- **HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **3000 Vdc WITHSTAND TEST VOLTAGE**
- **PERFORMANCE GUARANTEED OVER 0° C TO 70° C TEMPERATURE RANGE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES INC. (FILE NO. E55361)**
- **INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE**
- **GAIN-BANDWIDTH ADJUSTMENT PIN**
- **HIGH COMMON MODE REJECTION**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

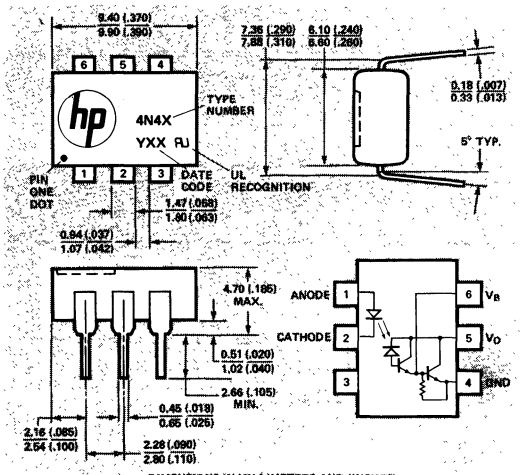
The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

*JEDEC Registered Data.



Applications

- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator — Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Absolute Maximum Ratings*

Storage Temperature ..... -55° C to +125° C
Operating Temperature ..... -40° C to +70° C
Lead Solder Temperature ..... 260° C for 10 s.
(1.6mm below seating plane)
Average Input Current — I_F ..... 20 mA[1]
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F 1.0A
(≤1 μs pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	4N46	350 500 200	1500 1500 600		%	I_F = 0.5mA, V_O = 1.0V I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V	4	5,6
		4N45	250 200	1200 500		%	I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V		
Logic Low Output Voltage	V_{OL}	4N46		.90 .92 .95	1.0 1.0 1.2	V	I_F = 0.5mA, I_{OL} = 1.75mA I_F = 1.0mA, I_{OL} = 5.0mA I_F = 10mA, I_{OL} = 20mA	2	6
		4N45		.90 .95	1.0 1.2	V	I_F = 1.0mA, I_{OL} = 2.5mA I_F = 10mA, I_{OL} = 20mA		
Logic High Output Current	I_{OH}*	4N46		.001	100	µA	I_F = 0mA, V_O = 18V		6
		4N45		.001	250	µA	I_F = 0mA, V_O = 5V		
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.0mA, T_A = 25°C	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, T_A=25°C t = 5 s, V_{I-O} = 3000VDC		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

Switching Specifications

AT T_A = 25°C

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}		80		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PHL}*		5	50	µs	I_F = 10mA, R_L = 220Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}		1500		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PLH}*		150	500	µs	I_F = 10mA, R_L = 220Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H		500		V/µs	I_F = 0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-500		V/µs	I_F = 1.0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

NOTES:

1. Derate linearly above 50° C free-air temperature at a rate of 0.4mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.7mW/° C.
3. Derate linearly above 25° C free-air temperature at a rate of 0.8mA/° C.
4. Derate linearly above 25° C free-air temperature at a rate of 1.5mW/° C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.5V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 2.5V$).

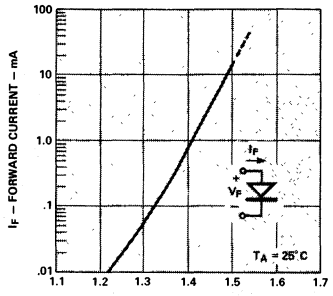


Figure 1. Input Diode Forward Current vs. Forward Voltage.

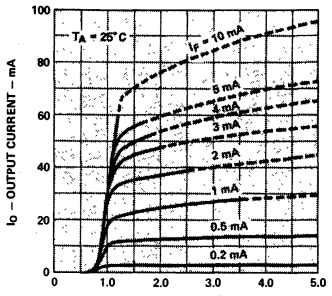


Figure 2. Typical DC Transfer Characteristics.

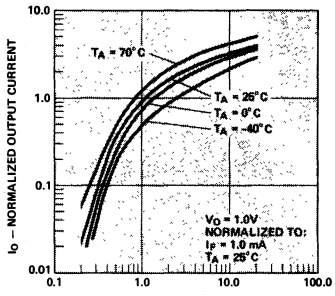


Figure 3. Output Current vs. Input Current.

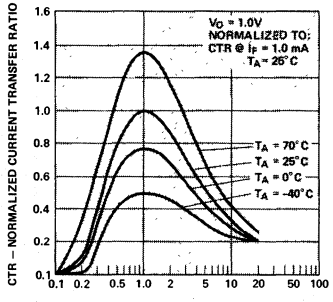


Figure 4. Current Transfer Ratio vs. Input Current.

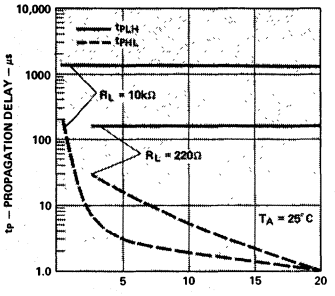


Figure 5. Propagation Delay vs. Forward Current.

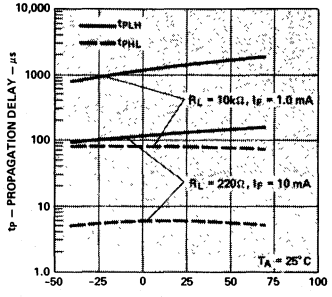


Figure 6. Propagation Delay vs. Temperature.

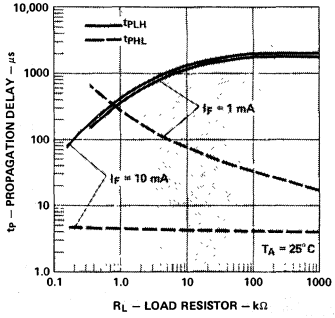
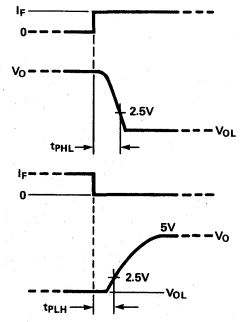


Figure 7. Propagation Delay vs Load Resistor.



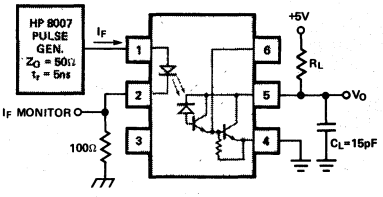
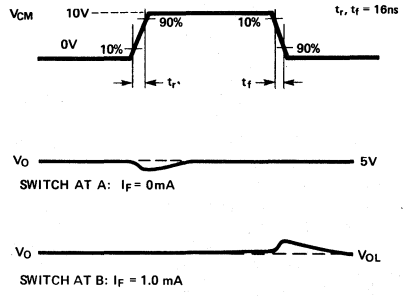


Figure 8. Switching Test Circuit



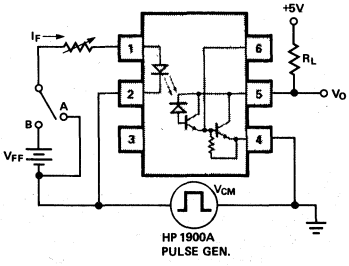


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

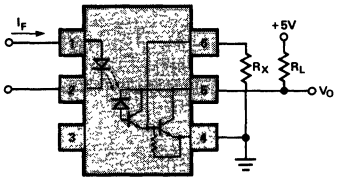


Figure 10. External Base Resistor, R_X

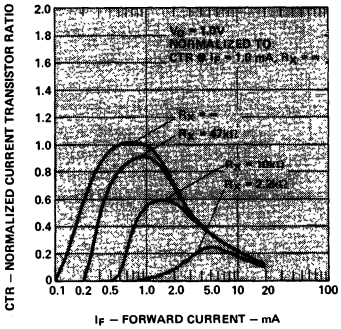


Figure 11. Effect of R_X On Current Transfer Ratio

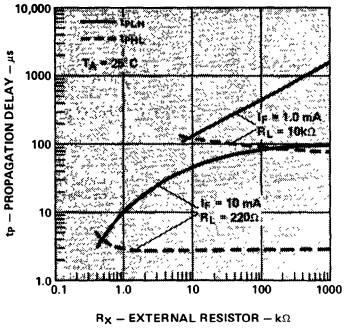
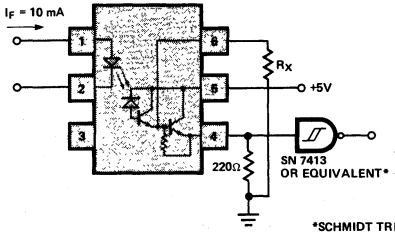


Figure 12. Effect of R_X On Propagation Delay

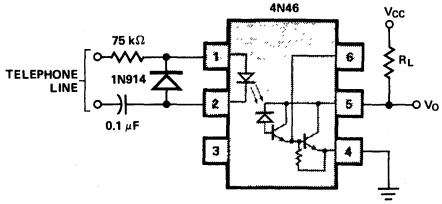
Applications



R_X (kΩ)	t_{PHL} (µs)	t_{PLH} (µs)
–	5	320
100	5	200
47	5	140
20	6	80
10	6	45

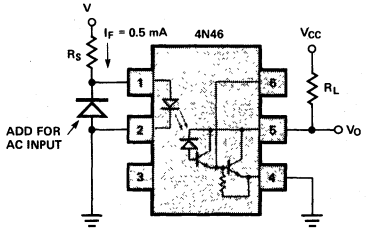
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



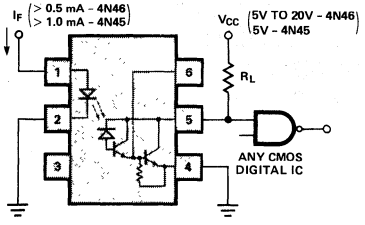
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

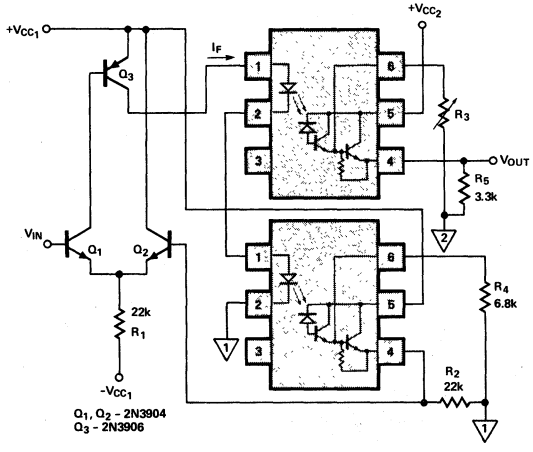


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Analog Signal Isolation

CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$

$V_{IN\,(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(<< \frac{V_{IN\,(MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\,(MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\,(MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\,(MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\,(MAX.)}}{2}$

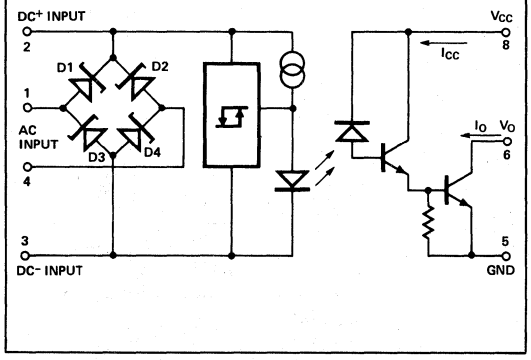
HEWLETT PACKARD

AC/DC TO LOGIC INTERFACE OPTOCOUPLER

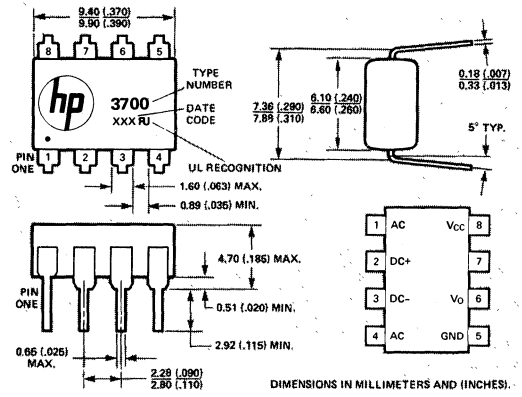
HCPL-3700

TECHNICAL DATA MARCH 1980

SCHEMATIC



OUTLINE DRAWING

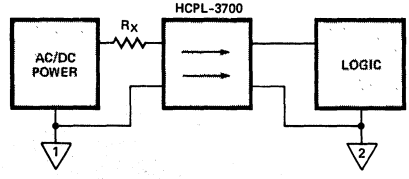


Features

- **AC OR DC INPUT**
- **PROGRAMMABLE SENSE VOLTAGE**
- **HYSTERESIS**
- **LOGIC COMPATIBLE OUTPUT**
- **SMALL SIZE: STANDARD 8 PIN DIP**
- **THRESHOLDS GUARANTEED OVER TEMPERATURE**
- **THRESHOLDS INDEPENDENT OF LED DEGRADATION**
- **3000V WITHSTAND TEST VOLTAGE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- **LIMIT SWITCH SENSING**
- **LOW VOLTAGE DETECTOR**
- **5V—240V AC/DC VOLTAGE SENSING**
- **RELAY CONTACT MONITOR**
- **RELAY COIL VOLTAGE MONITOR**
- **CURRENT SENSING**
- **MICROPROCESSOR INTERFACING**



Description

The HCPL-3700 is a voltage/current threshold detection optocoupler. This optocoupler uses an internal Light Emitting Diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.8 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The HCPL-3700, by combining several unique functions in a single package, provides the user with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

Absolute Maximum Ratings (No derating required up to 70° C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-25	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	sec	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2,3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	4.5	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	KHz	8

Switching Characteristics at T_A = 25° C, V_{CC} = 5.0V

Parameter	Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		4.0	15	μs	R_L = 4.7 kΩ, C_L = 30 pF	6,10	10
Propagation Delay Time to Logic High Output Level	t_{PLH}		10.0	40	μs	R_L = 4.7 kΩ, C_L = 30 pF		11
Common Mode Transient Immunity at Logic Low Output Level	CM_L		600		V/μs	I_{IN} = 3.11 mA, R_L = 4.7 kΩ, $V_{O\,max.}$ = 0.8V, V_{CM_L} = 140V	8,11	12,13
Common Mode Transient Immunity at Logic High Output Level	CM_H		4000		V/μs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O\,min}$ = 2.0V, V_{CM_H} = 1400V		
Output Rise Time (10-90%)	t_r		20		μs	R_L = 4.7 kΩ, C_L = 30 pF	7,10	
Output Fall Time (90-10%)	t_f		0.3		μs	R_L = 4.7 kΩ, C_L = 30 pF		

Electrical Characteristics

Over Recommended Temperature ($0°C \le T_A \le 70°C$) Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	1.96	2.5	3.11	mA	$V_{IN}=V_{TH+}$; V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA	2,3	14
		I_{TH-}	1.00	1.3	1.62	mA	$V_{IN} = V_{TH-}$; V_{CC} = 4.5V; V_O = 2.4V; $I_{OH} \le 100\ \mu A$		
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}	3.35	3.8	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA		
		V_{TH-}	2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \le 100\ \mu A$		
	AC (Pins 1, 4)	V_{TH+}	4.23	5.1	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA		14,15
		V_{TH-}	2.87	3.8	4.24	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \le 100\ \mu A$		
Hysteresis		I_{HYS}		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
		V_{HYS}		1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}	5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1	
		V_{IHC2}	6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}		12.0	13.4	V	$V_{IHC3} = V_2 - V_3$ = GND; I_{IN} = 15 mA; Pins1 & 4 Open		
		V_{ILC}		-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0V; Pins 1 & 4 Open	5	
Bridge Diode Forward Voltage		$V_{D1,2}$		0.59			I_{IN} = 3 mA (see schematic)		
		$V_{D3,4}$		0.74					
Logic Low Output Voltage		V_{OL}		0.1	0.4	V	V_{CC} = 4.5V; I_{OL} = 4.2 mA	5	14
Logic High Output Current		I_{OH}			100	μA	$V_{OH} = V_{CC}$ = 18V		
Logic Low Supply Current		I_{CCL}		1.0	4	mA	$V_2 - V_3$ = 5.0V; V_O = Open V_{CC} = 5.0V		
Logic High Supply Current		I_{CCH}		2		nA	V_{CC} = 18V; V_O = Open	4	14
Input-Output Insulation Leakage Current		I_{I-O}			1	μA	Relative Humidity = 45%, T_A = 25°C, V_{I-O} = 3000 Vdc; t = 5 sec.		16
Input-Output Resistance		R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		
Input-Output Capacitance		C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance		C_{IN}		50		pF	f=1 MHz; V_{IN}=0V, Pins 2 & 3, Pins 1 & 4 Open		

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70° C free-air temperature at a rate of 4.1 mW/° C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125° C at an ambient temperature of T_A = 70° C with a typical thermal resistance from junction to ambient of θ_{JA_i} = 240° C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70° C free-air temperature at a rate of 5.4 mW/° C.
6. Derate linearly above 70° C free-air temperature at a rate of 3.9 mW/° C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125° C at an ambient temperature of T_A = 70° C with a typical thermal resistance from junction to ambient of θ_{JA_o} = 265° C/W.
7. Derate linearly above 70° C free-air temperature at a rate of 0.6 mA/° C.
8. Maximum operating frequency is defined when output waveform (Pin 6) obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5V square wave input signal.

9. All typical values are at $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5V level of the leading edge of a 5.0V input pulse (1 μs rise time) to the 1.5V level on the leading edge of the output pulse (see Figure 9).
11. The t_{PLH} propagation delay is measured from the 2.5V level of the trailing edge of a 5.0V input pulse (1 μs fall time) to the 1.5V level on the trailing edge of the output pulse (see Figure 9).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$). See Figure 10.
13. In applications where dV_{CM}/dt may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.

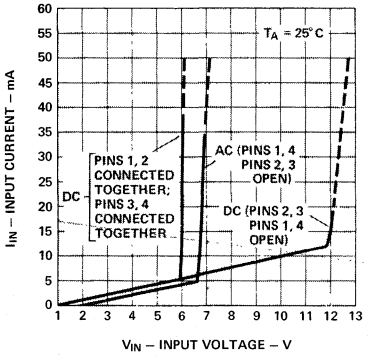


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN}.

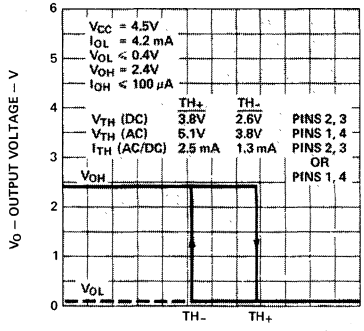


Figure 2. Typical Transfer Characteristics.

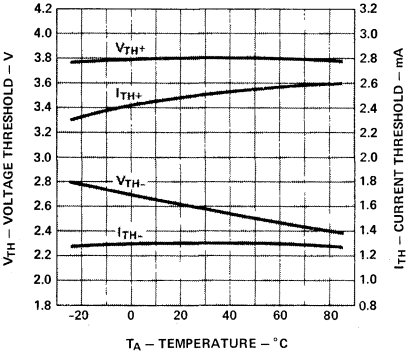


Figure 3. Typical DC Threshold Levels vs. Temperature.

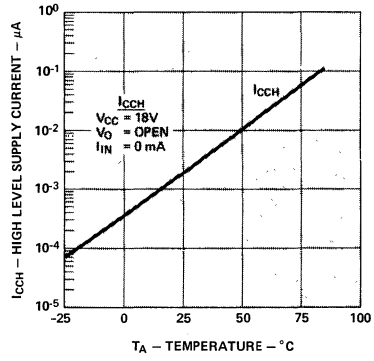


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

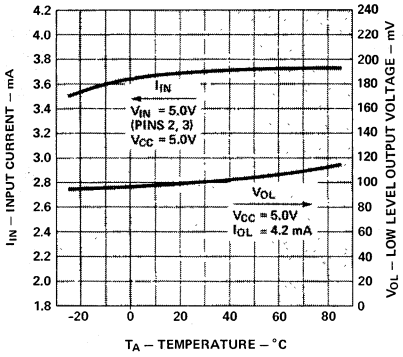


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

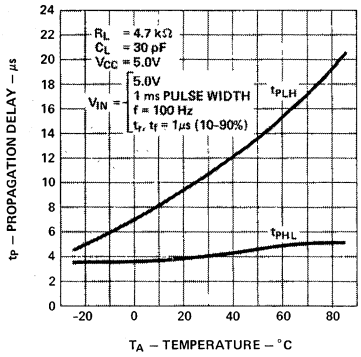


Figure 6. Typical Propagation Delay vs. Temperature.

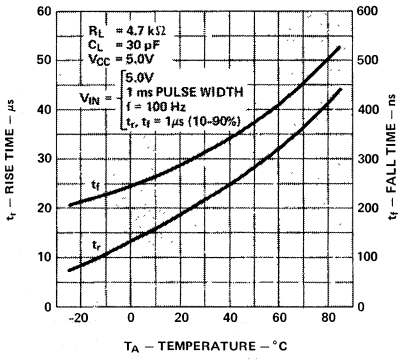


Figure 7. Typical Rise, Fall Times vs. Temperature.

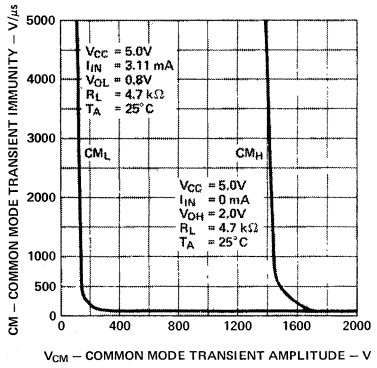
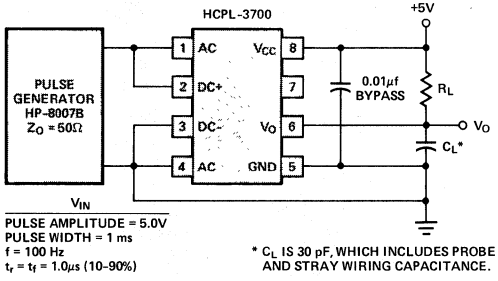


Figure 8. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.



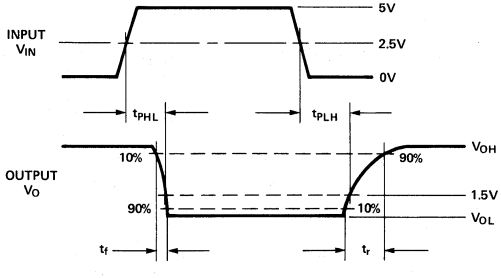
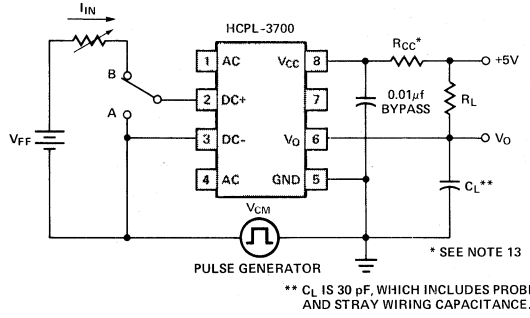


Figure 9. Switching Test Circuit.



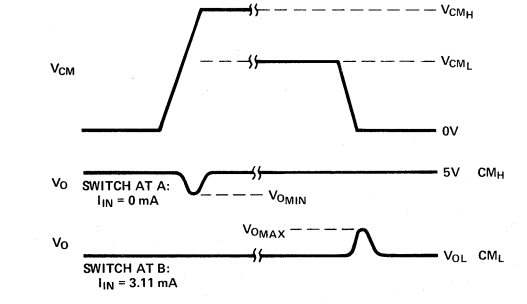


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Electrical Considerations

The HCPL-3700 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_x can be obtained from Figure 11. Specific calculation of R_x can be obtained from Equation (1) of Figure 12. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 12 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700 in combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where dV_{CM}/dt may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μf be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing AC signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 μf capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

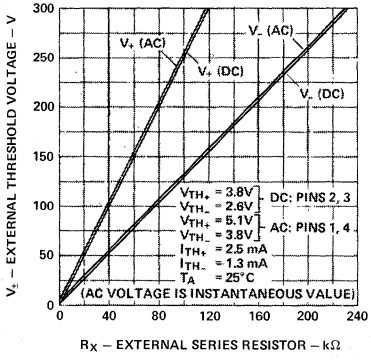


Figure 11. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_X.

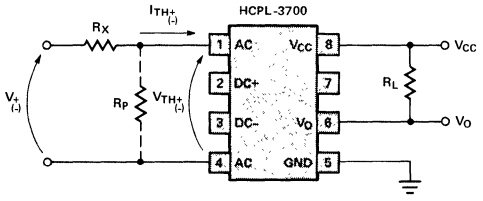


Figure 12. External Threshold Voltage Level Selection.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \qquad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \qquad (2)$$

$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \qquad (3)$$

$V_+ = \frac{3.00}{1.10} R = 2.5R$ $\quad V_- = \quad 1.3R$

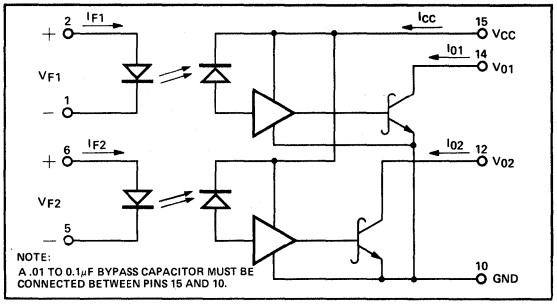
$R = 1.6, V_+ = 4.0V$ $\quad , 1.6, V_- =$

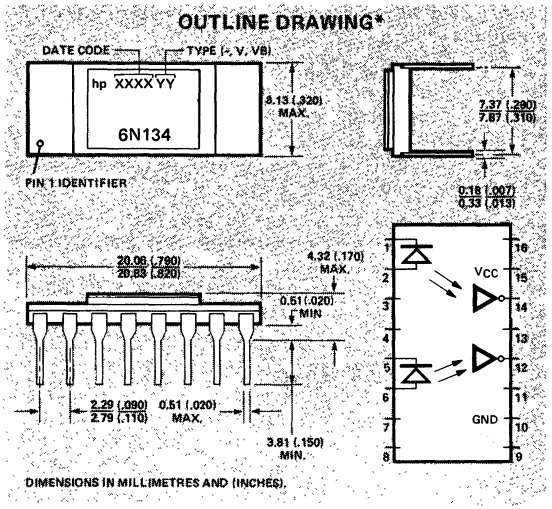
HEWLETT PACKARD

DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

6N134
6N134 TXV
6N134 TXVB

TECHNICAL DATA MARCH 1980





Features

- **HERMETICALLY SEALED**
- **HIGH SPEED**
- **PERFORMANCE GUARANTEED OVER -55°C TO +125°C AMBIENT TEMPERATURE RANGE**
- **STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE**
- **TTL COMPATIBLE INPUT AND OUTPUT**
- **HIGH COMMON MODE REJECTION**
- **DUAL-IN-LINE PACKAGE**
- **1500 VDC WITHSTAND TEST VOLTAGE**
- **EIA REGISTRATION**
- **HIGH RADIATION IMMUNITY**

Applications

- Logic Ground Isolation
- Line Receiver
- Computer - Peripheral Interface
- Vehicle Command/Control Isolation
- High Reliability Systems
- System Test Equipment Isolation

Description

The 6N134 consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compatibility. The isolator operational parameters are guaranteed from -55°C to +125°C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

Recommended Operating Conditions

TABLE I

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5**	20	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	
Operating Temperature	T_A	-55	125	°C

Absolute Maximum Ratings*

(No derating required up to 125°C)

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 40 mA (≤ 1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} ..... 7V (1 minute maximum)
Output Current - I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage - V_O (each channel) 7V
Total Power Dissipation (both channels) ..... 350 mW

**12.5mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10mA or less.

*JEDEC Registered Data.

TABLE II

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = –55°C TO +125°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		5	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		1
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC} = 5.5V, I_F = 10mA I_{OL} (Sinking) = 10mA	4	1, 9
High Level Supply Current	I_{CCH}*		18	28	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply Current	I_{CCL}*		26	36	mA	V_{CC} = 5.5V, I_F = 20mA (Both Channels)		
Input Forward Voltage	V_F*		1.5	1.75	V	I_F = 20mA, T_A = 25°C	1	1
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10μA, T_A = 25°C		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	V_{I-O} = 1500Vdc, Relative Humidity = 45% T_A = 25°C, t = 5s		2
Propagation Delay Time to High Output Level	t_{PLH}*		65	90	ns	R_L = 510Ω, C_L = 15pF, I_F = 13mA, T_A = 25°C	2,3	5
Propagation Delay Time to Low Output Level	t_{PHL}*		55	90	ns	R_L = 510Ω, C_L = 15pF I_F = 13mA, T_A = 25°C	2,3	6

**All typical values are at V_{CC} = 5V, T_A = 25°C

TABLE III

Typical Characteristics AT T_A = 25°C, V_{CC} = 5V EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.9		mV/°C	I_F = 20mA		1
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V		3
Capacitance (Input-Output)	C_{I-O}		1.7		pF	f = 1MHz		3
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	Relative Humidity = 45% V_{I-I} = 500V, t = 5s		4
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500V		4
Capacitance (Input-Input)	C_{I-I}		0.55		pF	f = 1MHz		4
Output Rise-Fall Time (10-90%)	t_r, t_f		35		ns	R_L = 510Ω, C_L = 15pF I_F = 13mA		
Common Mode Transient Immunity at High Output Level	CM_H		100		V/μs	V_{CM} = 10V (peak), V_O (min.) = 2V, R_L = 510Ω, I_F = 0mA	6	7
Common Mode Transient Immunity at Low Output Level	CM_L		-400		V/μs	V_{CM} = 10V (peak), V_O (max.) = 0.8V R_L = 510Ω, I_F = 10mA	6	8

NOTES:

1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 9 through 16 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0V).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8V).
9. It is essential that a bypass capacitor (.01 to 0.1μF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm (Fig. 7).

*JEDEC Registered Data.

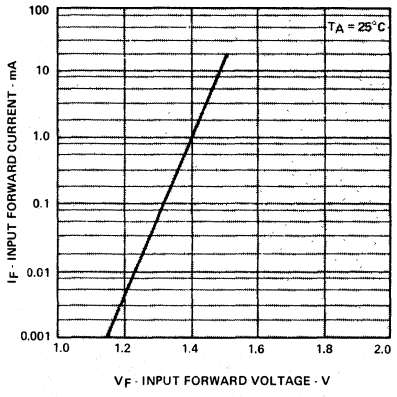


Figure 1. Input Diode Forward Characteristic

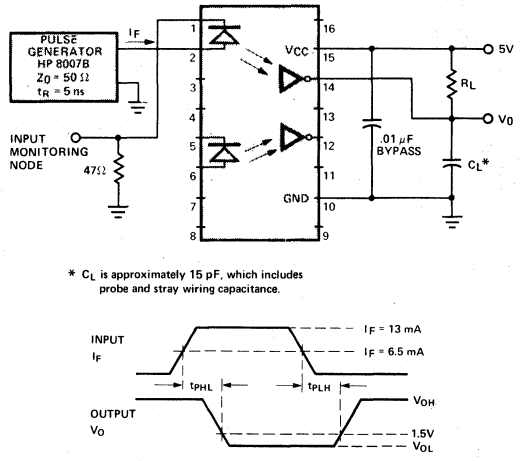


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

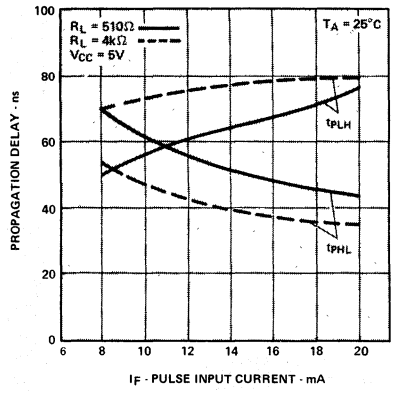


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

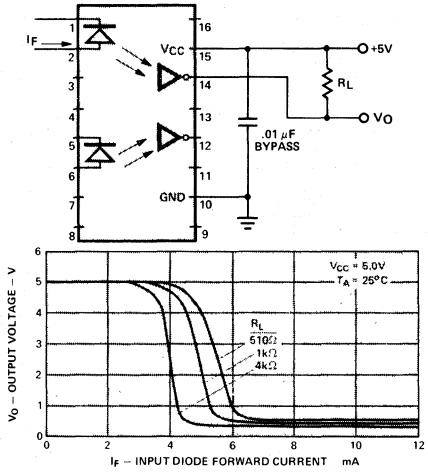


Figure 4. Input-Output Characteristics

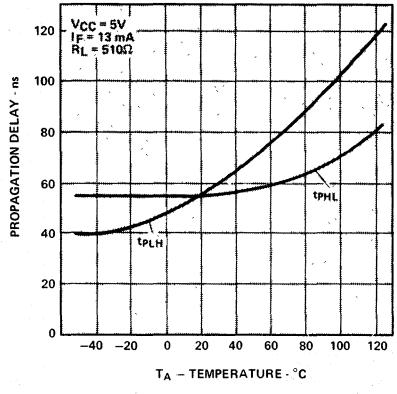


Figure 5. Propagation Delay vs. Temperature

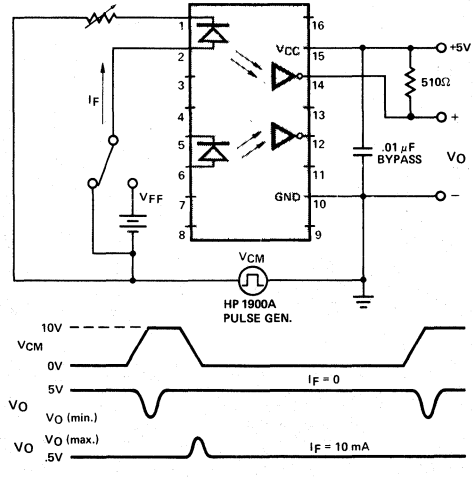


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

*JEDEC Registered Data.

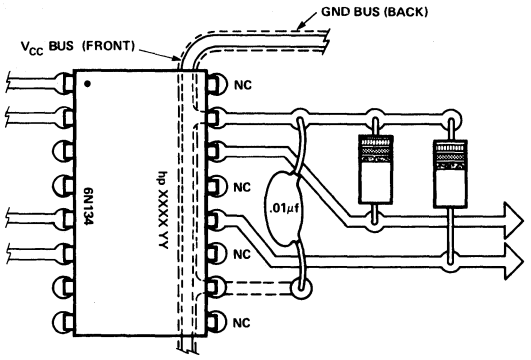


Figure 7. Recommended Circuit Board Layout.

High Reliability Test Program

Hewlett Packard provides standard high reliability test programs, patterned after MIL-M-38510.

- The TXV suffix identifies a part which has been preconditioned and screened per Table IV.
- The TXVB suffix identifies a part which has been preconditioned and screened per Table IV, and comes from a lot which has been subjected to the Group B tests detailed in Table V.

Part Number System

Commercial Product	With TX Screening	With TX Screening Plus Group B
6N134	6N134 TXV	6N134 TXVB

TABLE IV TXV Preconditioning and Screening –100%

Examination or Test	MIL-STD-883 Methods	Conditions
1. Pre-Cap Visual Inspection	2010	Condition B
2. Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}, V_F, BV_R, I_{I-O}		Per Table II, T_A = 25°C
3. High Temperature Storage	1008	168 hrs. @ 150°C
4. Temperature Cycling	1010	-65°C to +150°C
5. Acceleration	2001	5KG, Y_1
6. Helium Leak Test	1014	Test Cond. A
7. Gross Leak Test	1014	Test Cond. C
8. Electrical Test: V_{OL}		Per Table II, T_A = 25°C
9. Burn-In	1015	168 hrs., T_A = 125°C, V_{CC}=5.5V, I_F=13mA, I_O=25mA
10. Electrical Test: Same as Step 2		
11. Evaluate Drift		Max. ΔV_{OL} = ±20%
12. Sample Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}		Per Table II, LTPD = 7, T_A = -55°C
13. Sample Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}		Per Table II, LTPD = 7, T_A = +125°C
14. Sample Electrical Test: t_{PLH}, t_{PHL}		Per Table II, T_A = 25°C, LTPD = 7
15. External Visual	2009	

TABLE V, GROUP B

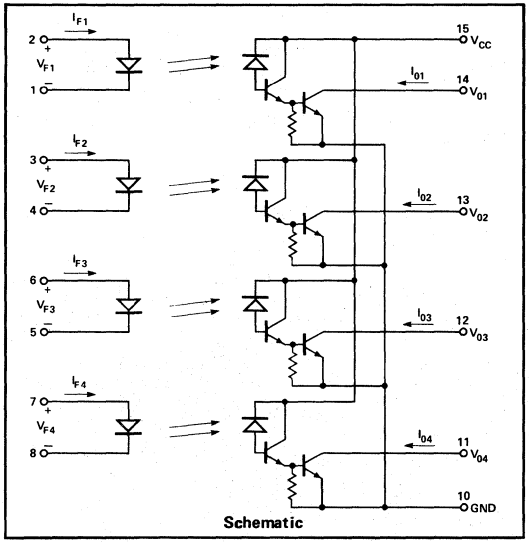
Examination or Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD
Subgroup 1			15
Physical Dimensions	2016	See Product Outline Drawing	
Subgroup 2			20
Solderability	2003	Immersion within 2.5mm of body, 16 terminations	
Subgroup 3			15
Temperature Cycling	1010	Test Condition C	
Thermal Shock	1011	Test Condition A, 5 cycles	
Hermetic Seal, Fine Leak	1014	Test Condition A	
Hermetic Seal, Gross Leak	1014	Test Condition C,	
End Points: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}, V_F, BV_R, I_{I-O}		Per Table II, T_A = 25°C	
Subgroup 4			15
Shock, non-operating	2002	1500 G, t = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	
Constant Acceleration	2001	5KG, Y_1	
End Points: Same as Subgroup 3			
Subgroup 5			15
Terminal Strength, tension	2004	Test Condition A, 4.5N (1 lb.), 15s	
Subgroup 6			
High Temperature Life	1008	T_A = 150°C	λ = 7
End Points: Same as Subgroup 3			
Subgroup 7			
Steady State Operating Life	1005	V_{CC} = 5.5V, I_F = 13mA, I_O = 25mA, T_A = 125°C	λ = 7
End Points: Same as Subgroup 3			

HEWLETT PACKARD

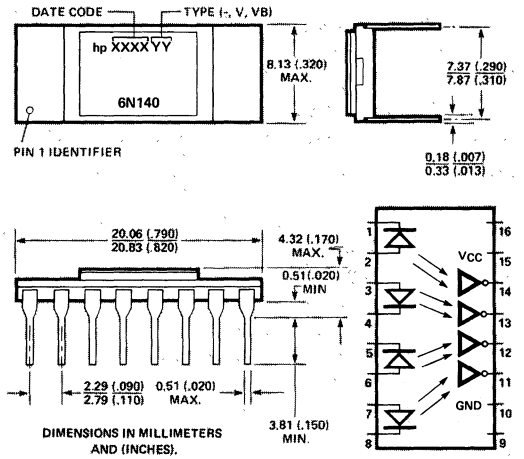
HERMETICALLY SEALED, FOUR CHANNEL, LOW INPUT CURRENT OPTOCOUPLER

6N140
6N140 TXV
6N140 TXVB

TECHNICAL DATA MARCH 1980



Schematic



Outline Drawing*

Features

- **HERMETICALLY SEALED**
- **HIGH DENSITY PACKAGING**
- **HIGH CURRENT TRANSFER RATIO: 500% TYPICAL**
- **CTR AND I_{OH} GUARANTEED OVER -55°C TO 100°C AMBIENT TEMPERATURE RANGE**
- **STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE**
- **1500 Vdc WITHSTAND TEST VOLTAGE**
- **LOW INPUT CURRENT REQUIREMENT: 0.5 mA**
- **LOW OUTPUT SATURATION VOLTAGE: 0.1V TYPICAL**
- **LOW POWER CONSUMPTION**
- **HIGH RADIATION IMMUNITY**

Applications

- **Isolated Input Line Receiver**
- **System Test Equipment Isolation**
- **Digital Logic Ground Isolation**
- **Vehicle Command/Control Isolation**
- **EIA RS-232C Line Receiver**
- **Microprocessor System Interface**
- **Current Loop Receiver**
- **Level Shifting**
- **Process Control Input/Output Isolation**

Description

The 6N140 contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. A common pin for the photodiodes and first stage of each detector IC (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photo-darlington type optocouplers. Also, the separate V_{CC} pin can be strobed low as an output disable or operated with supply voltages as low as 2.0V without adversely affecting the parametric performance.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 6N140 has a 300% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18V V_{CC} and by the guaranteed maximum output leakage (I_{OH}) at 18V.

Important specifications such as CTR, leakage current, supply current and output saturation voltage are guaranteed over the -55°C to 100°C temperature range to allow trouble free system operation.

*JEDEC Registered Data.

TABLE I

Recommended Operating Conditions

	Symbol	Min.	Max.	Units
Input Current, Low Level (Each Channel)	I_{FL}		2	μA
Input Current, High Level (Each Channel)	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings*

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +100°C
Lead Solder Temperature ..... 260°C for 10 s. (1.6mm below seating plane)
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage, V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ... 50 mW[2]
Peak Input Current (each channel, ≤1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) 5V

TABLE II.

Electrical Characteristics T_A = -55°C to 100°C, Unless Otherwise Specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	300 300 200	1000 750 400		% % %	I_F=0.5mA, V_O=0.4V, V_{CC}=4.5V I_F=1.6mA, V_O=0.4V, V_{CC}=4.5V I_F=5mA, V_O=0.4V, V_{CC}=4.5V	3	4,5
Logic Low Output Voltage	V_{OL}		.1 .2	.4 .4	V V	I_F=.5mA, I_{OL}=1.5mA, V_{CC}=4.5V I_F=5mA, I_{OL}=10mA, V_{CC}=4.5V	2	4
Logic High Output Current	I_{OH}*		.005	250	μA	I_F=2μA V_O=V_{CC}=18V		4,6
Logic Low Supply Current	I_{CCL}*		2	4	mA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=1.6mA V_{CC}=18V		
Logic High Supply Current	I_{CCH}*		.010	40	μA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=0 V_{CC}=18V		
Input Forward Voltage	V_F*		1.4	1.7	V	I_F=1.6mA, T_A=25°C	1	4
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		4
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	45% Relative Humidity, T_A=25°C, t=5s., V_{I-O}=1500 Vdc		7
Propagation Delay Time To Logic High At Output	t_{PLH}*		25	60	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	
			10	20	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	
Propagation Delay Time To Logic Low At Output	t_{PHL}*		35	100	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	
			2	5	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	
Common Mode Transient Immunity At Logic High Level Output	CM_H	500	1000		V/μs	I_F=0, R_L=1.5kΩ $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	10,12
Common Mode Transient Immunity At Logic Low Level Output	CM_L	-500	-1000		V/μs	I_F=1.6mA, R_L=1.5kΩ $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	11,12

TABLE III.

Typical Characteristics T_A = 25°C, V_{CC} = 5V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500 Vdc, T_A=25°C		4,8
Capacitance (Input-Output)	C_{I-O}		1.5		pF	f=1MHz, T_A=25°C		4,8
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, V_{I-I}=500 Vdc, T_A=25°C, t=5s.		9
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I}=500Vdc, T_A=25°C		9
Capacitance (Input-Input)	C_{I-I}		1		pF	f=1MHz, T_A=25°C		9
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F=1.6mA		4
Input Capacitance	C_{IN}		60		pF	f=1MHz, V_F=0, T_A=25°C		4

NOTES:
1. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus one fourth of total supply power. Derate at 1.25 mW/°C above 80°C.
3. Derate I_F at 0.25 mA/°C above 80°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_F=2μA for channel under test. For all other channels, I_F=10mA.
7. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
8. Measured between each input pair shorted together and all output pins.
9. Measured between adjacent input pairs shorted together, i.e. between pins 1 and 2 shorted together and pins 3 and 4 shorted together, etc.
10. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e. V_O > 2.0V).
11. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e. V_O < 0.8V).
12. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC's from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.6\ I_F\ (mA)}$ kΩ.

*JEDEC Registered Data.

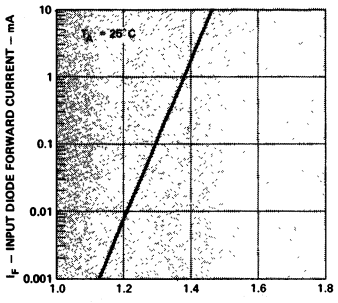


Figure 1. Input Diode Forward Current vs. Forward Voltage.

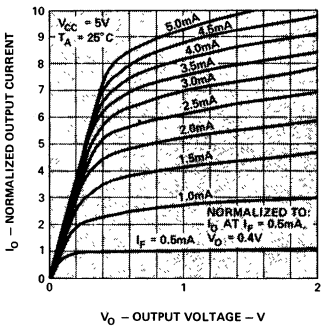


Figure 2. Normalized DC Transfer Characteristics.

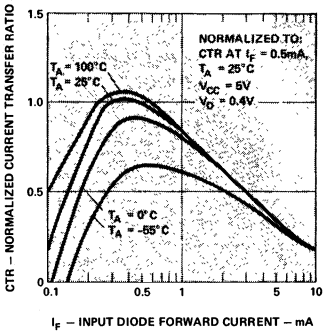


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

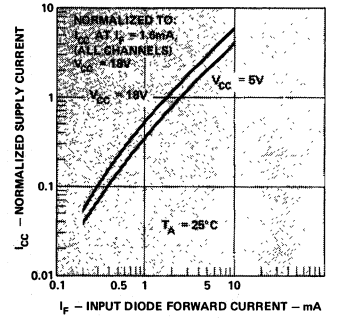


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

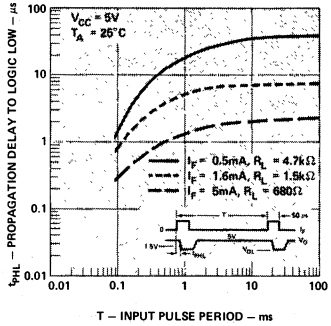


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

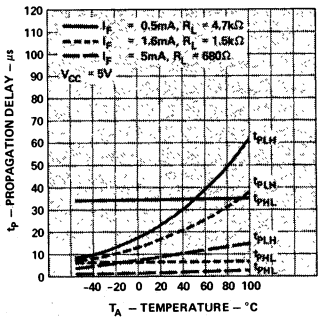


Figure 6. Propagation Delay vs. Temperature

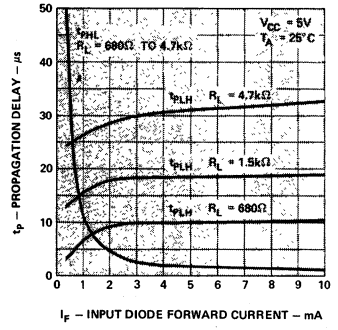
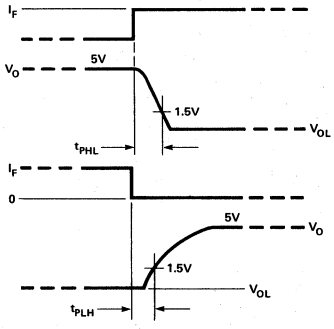


Figure 7. Propagation Delay vs. Input Diode Forward Current.



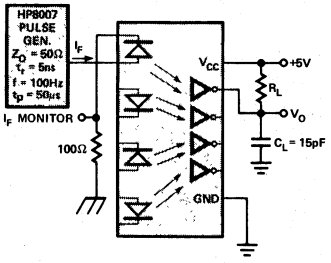
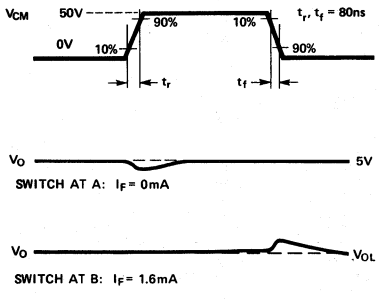


Figure 8. Switching Test Circuit.* (f, t_p not JEDEC registered)



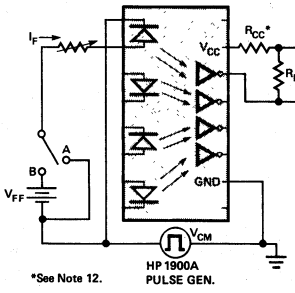


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

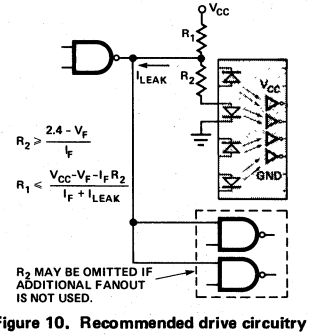


Figure 10. Recommended drive circuitry using TTL logic.

*JEDEC Registered Data.

High Reliability Test Program

Hewlett Packard provides standard high reliability test programs, patterned after MIL-M-38510 in order to facilitate the use of HP products in military programs.

HP offers two levels of high reliability testing:

- The TXV suffix identifies a part which has been preconditioned and screened per Table IV.
- The TXVB suffix identifies a part which has been preconditioned and screened per Table IV, and comes from a lot which has been subjected to the Group B tests detailed in Table V.

Part Number System

Commercial Product	With TXV Screening	With TXV Screening Plus Group B
6N140	6N140 TXV	6N140 TXVB

TABLE IV TXV Preconditioning and Screening – 100%

Examination or Test	MIL-STD-883 Methods	Conditions
1. Pre-Cap Visual Inspection	OED Procedure	72-4063, 72-4064
2. High Temperature Storage	1008	72 hrs. @ 150°C
3. Temperature Cycling	1010	-65°C to +150°C
4. Acceleration	2001	5KG, Y_1
5. Helium Leak Test	1014	Cond. A
6. Gross Leak Test	1014	Cond. C
7. Electrical Test CTR, I_{OH}, I_{CCL}, I_{CCH}, V_F, BV_R:		T_A = 25°C, per Table II
8. Burn-In	1015	V_{CC} = 18V, I_F = 5mA, I_O = 10mA t = 168 hrs. @ T_A = 100°C
9. Electrical Test: Same as step 7 and I_{I-O}		T_A = 25°C, per Table II
10. Evaluate Drift		Max. ΔCTR = ±25% @ I_F = 1.6mA
11. Sample Electrical Test: CTR, I_{OH}, I_{CCL}, I_{CCH}		Per Table II, LTPD = 7, T_A = -55°C
12. Sample Electrical Test: CTR, I_{OH}, I_{CCL}, I_{CCH}		Per Table II, LTPD = 7, T_A = +100°C
13. Sample Electrical Test: t_{PHL}, t_{PLH}, CM_H, CM_L		Per Table II, LTPD = 7, T_A = 25°C
14. External Visual	2009	

TABLE V, Group B

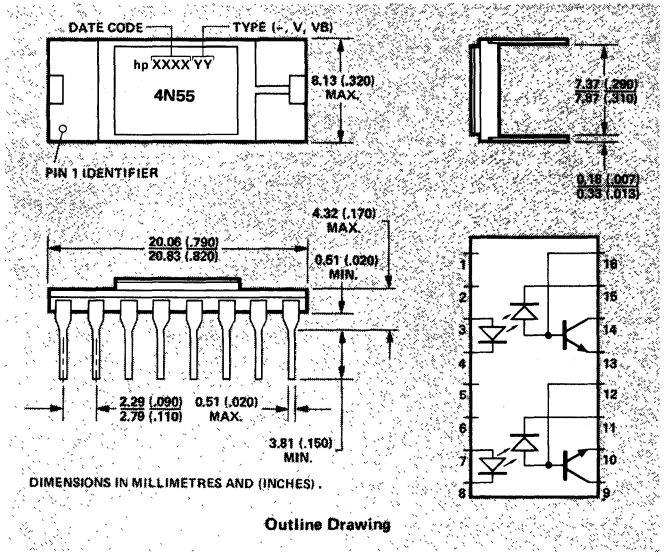
Examination or Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD
Subgroup 1			
Physical Dimensions	2016	See Product Outline Drawing	15
Subgroup 2			
Solderability	2003	Immersion within 2.5mm of body, 16 terminations	20
Subgroup 3			
Temperature Cycling	1010	Test Condition C	15
Thermal Shock	1011	Test Condition A, 5 cycles	
Hermetic Seal, Fine Leak	1014	Test Condition A	
Hermetic Seal, Gross Leak	1014	Test Condition C	
End Points:			
CTR, I_{OH}, I_{CCL}, I_{CCH}, V_F, BV_R		Per Table II, T_A = 25°C	
Subgroup 4			
Shock, non-operating	2002	1500 G, t = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	15
Constant Acceleration	2001	5KG, Y_1	
End Points:			
Same as Subgroup 3			
Subgroup 5			
Terminal Strength, tension	2004	Test Condition A, 4.5N (1 lb.), 15s.	15
Subgroup 6			
High Temperature Life	1008	T_A = 150°C, non-operating	λ = 10
End Points:			
Same as Subgroup 3			
Subgroup 7			
Steady State Operating Life	1005	V_{CC} = 18V, I_F = 5mA, I_O = 10mA, T_A = 100°C	λ = 10
End Points:			
Same as Subgroup 3			

HEWLETT PACKARD

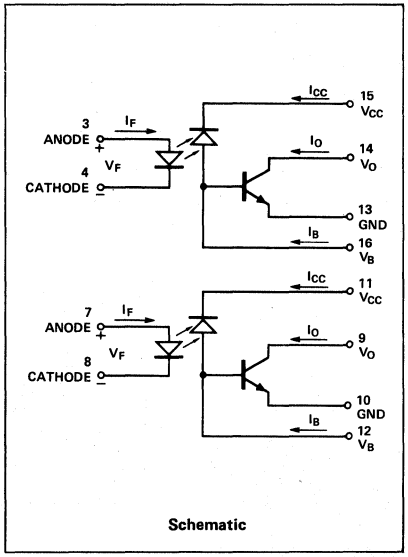
DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

4N55
4N55 TXV
4N55 TXVB

TECHNICAL DATA MARCH 1980



Outline Drawing



Schematic

Features

- **HERMETICALLY SEALED**
- **HIGH SPEED: TYPICALLY 400k bit/s**
- **PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE**
- **STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **18 VOLT V_{CC}**
- **DUAL-IN-LINE PACKAGE**
- **1500 Vdc WITHSTAND TEST VOLTAGE**
- **HIGH RADIATION IMMUNITY**

Applications

- **HIGH RELIABILITY SYSTEMS**
- **LINE RECEIVERS**
- **DIGITAL LOGIC GROUND ISOLATION**
- **ANALOG SIGNAL GROUND ISOLATION**
- **SWITCHING POWER SUPPLY FEEDBACK ELEMENT**
- **VEHICLE COMMAND/CONTROL**
- **SYSTEM TEST EQUIPMENT**
- **LEVEL SHIFTING**

Description

The 4N55 consists of two completely isolated optocouplers in a hermetically sealed ceramic package. Each channel has a light emitting diode and an integrated photon detector providing 1500 Vdc electrical isolation between input and output. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

The 4N55 is suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16mA over the full military operating temperature range, -55° C to +125° C. The 18V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

Absolute Maximum Ratings

Storage Temperature ..... -65° C to +150° C
Operating Temperature ..... -55° C to +125° C
Lead Solder Temperature ..... 260° C for 10 s (1.6mm below seating plane)
Average Input Current, I_F (each channel) 20mA
Peak Input Current, I_F (each channel, ≤ 1ms duration) 40mA
Reverse Input Voltage, V_R (each channel) 5V
Input Power Dissipation (each channel) 36mW
Average Output Current, I_O (each channel) 8mA
Peak Output Current, I_O (each channel) 16mA
Supply Voltage, V_{CC} (each channel) ..... -0.5V to 20V
Output Voltage, V_O (each channel) ..... -0.5V to 20V)
Emitter Base Reverse Voltage, V_{EBO} 3.0V
Base Current, I_B (each channel) 5mA
Output Power Dissipation (each channel) 50mW
Derate linearly above 100° C free air temperature at a rate of 1.4mW/° C.

TABLE I.

Recommended Operating Conditions (EACH CHANNEL)

	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Supply Voltage	V_{CC}	2	18	V

TABLE II.

Electrical Characteristics T_A = -55° C to +125° C, unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	9	20		%	I_F=16mA, V_O=0.4V, V_{CC}=4.5V	2,3	1,2
Logic High Output Current	I_{OH}		20	100	μA	I_F=0, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Output Leakage Current	I_{OH1}		70	250	μA	I_F=250μA, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Logic Low Supply Current	I_{CCL}		35	200	μA	I_{F1}=I_{F2}=20mA, V_{CC}=18V	5	1
Logic High Supply Current	I_{CCH}		0.2	10	μA	I_F=0mA, I_F (other channel)=20mA V_{CC}=18V		1
Input Forward Voltage	V_F		1.5	1.8	V	I_F=20mA	1	1
Input Reverse Breakdown Voltage	B_{VR}	3			V	I_R=10μA		1
Input-Output Insulation Leakage Current	I_{I-O}			1.0	μA	45% Relative Humidity, T_A=25° C, t=5s, V_{I-O}=1500Vdc		3
Propagation Delay Time to Logic High at Output	t_{PLH}		2.0	6.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.4	2.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1

*All typicals at T_A=25° C.

Notes:
1. Each channel.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. Refer to Application Note 1002 for more detail. In short it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.

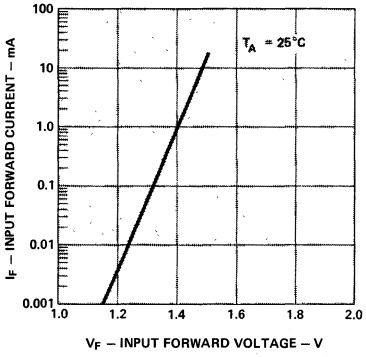


Figure 1. Input Diode Forward Characteristic.

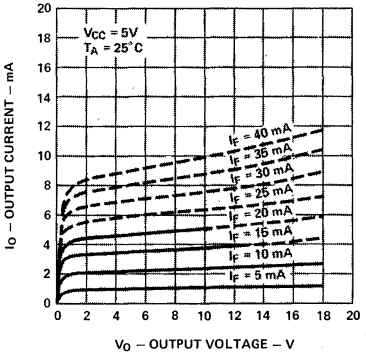


Figure 2. DC and Pulsed Transfer Characteristic

TABLE III.

Typical Characteristics at T_A=25°C

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.9	mV/°C	I_F=18mA		1
Input Capacitance	C_{in}	120	pF	f=1 MHz, V_F=0		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O}=500 Vdc		1
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f=1 MHz		1,4
Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, V_{I-I}=500Vdc, t=5s		5
Capacitance (Input-Input)	C_{I-I}	.55	pF	f=1 MHz		5
Transistor DC Current Gain	h_{FE}	250	—	V_O=5V, I_O=3mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC}=5V, V_O=2V	7	1
Common Mode Transient Immunity at Logic High Level Output	CM_H	1000	V/μs	I_F=0, R_L=8.2kΩ V_{CM}=10V_{p-p}	10	1,6
Common Mode Transient Immunity at Logic Low Level Output	CM_L	-1000	V/μs	I_F=16mA, R_L=8.2kΩ V_{CM}=10V_{p-p}	10	1,7
Bandwidth	BW	2	MHz	R_L=100Ω	8	8

Notes (cont.):

4. Measured between each input pair shorted together and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM}, for which the output will remain in the logic high state.
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM}, for which the output will remain in the logic low state.
8. Bandwidth is the frequency at which the ac output voltage is 3dB below the low frequency asymptote.

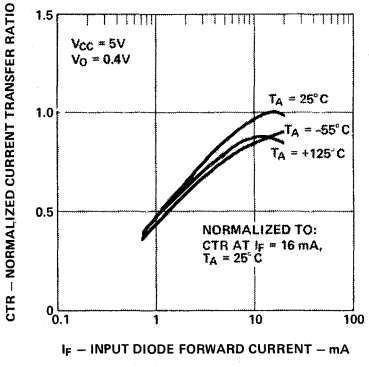


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

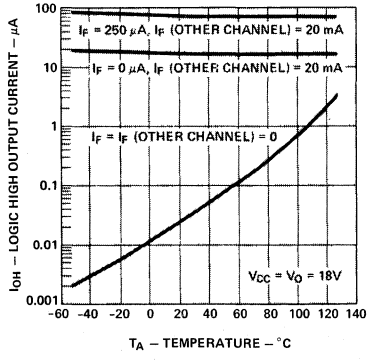


Figure 4. Logic High Output Current vs. Temperature.

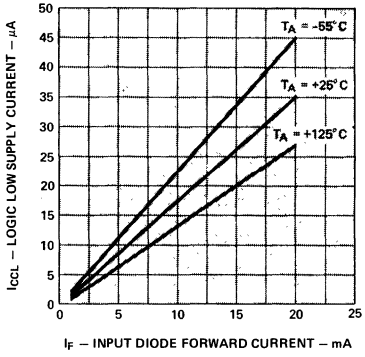
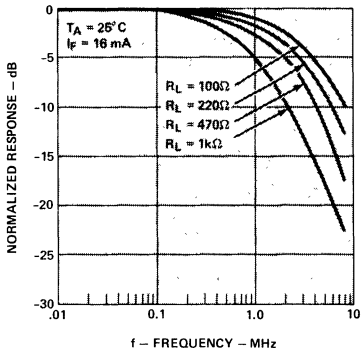


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.



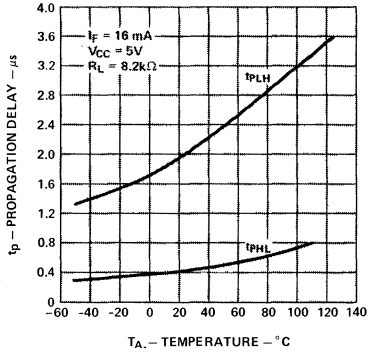


Figure 6. Propagation Delay vs. Temperature.

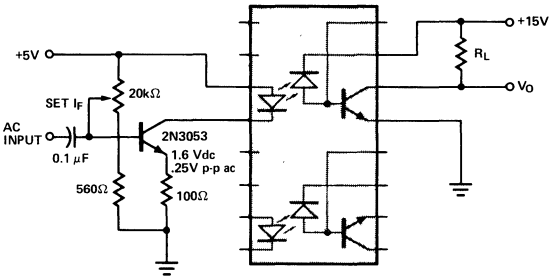


Figure 8. Frequency Response.

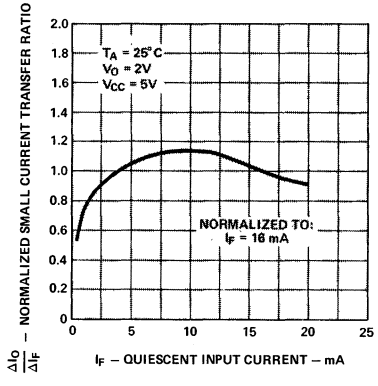
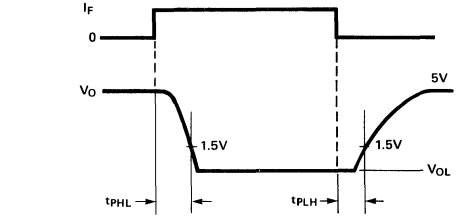


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.



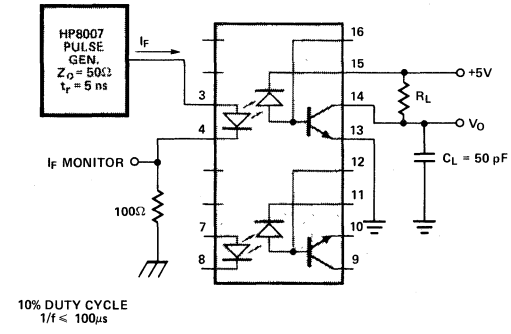


Figure 9. Switching Test Circuit.

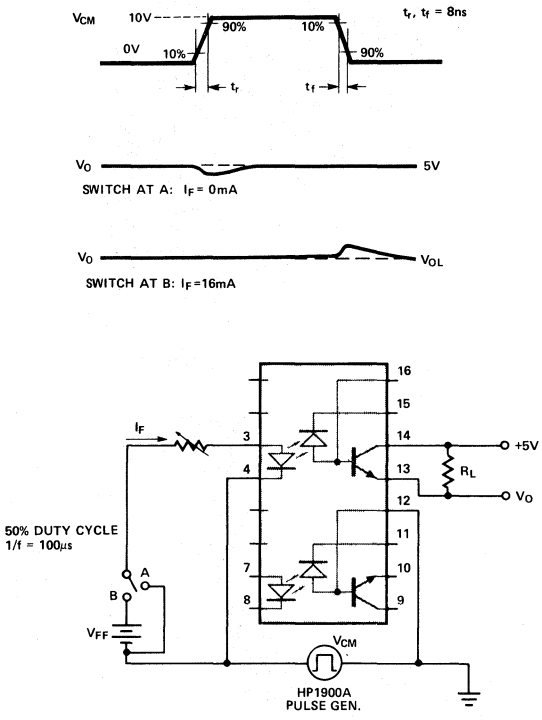
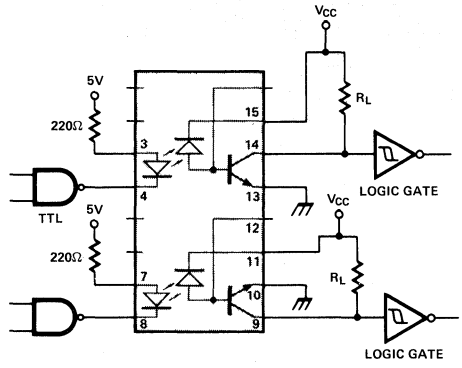


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
V_{CC}	5V	5V	15V
R_L 5% TOLERANCE	*18kΩ	8.2kΩ	22kΩ

*THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2kΩ.

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

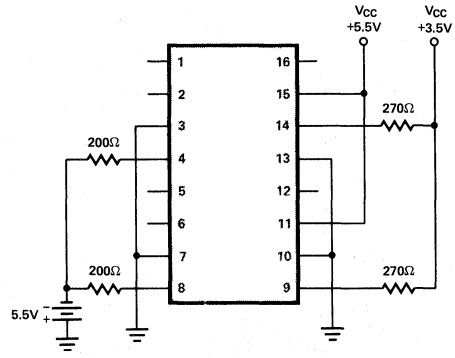
High Reliability Test Program

Hewlett-Packard provides standard high reliability test programs, patterned after MIL-M-38510.

- The TXV suffix identifies a part which has been preconditioned and screened per Table IV.
- The TVXB suffix identifies a part which has been preconditioned and screened per Table IV, and comes from a lot which has been subjected to the Group B tests detailed in Table V.

Part Number System

Commercial Product	With TXV Screening	With TXV Screening Plus Group B
4N55	4N55TXV	4N55TXVB



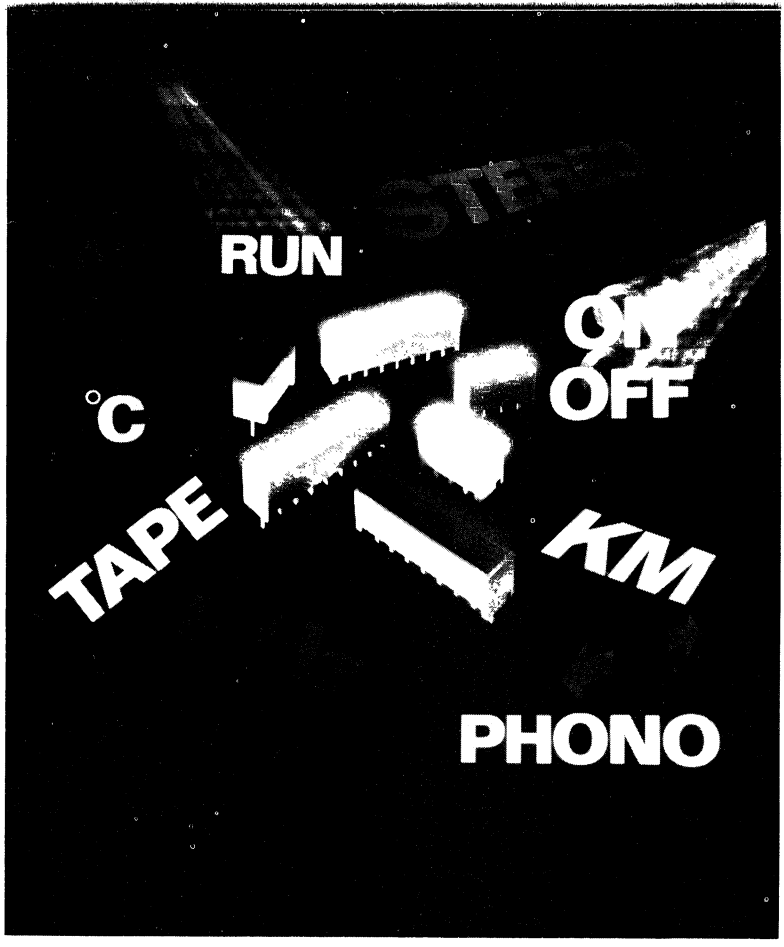
Burn-in-Circuit

TABLE IV. TXV PRECONDITIONING AND SCREENING – 100%

Examination or Test	MIL-STD-883 Methods	Conditions
1. Pre-Cap Visual Inspection	2010	Condition B
2. High Temperature	1008	24 Hrs. @ 150°C
3. Temperature Cycling	1010	65°C to +150°C
4. Acceleration	2001	5kG, Y_1
5. Helium Leak Test	1014	Test Condition A
6. Gross Leak Test	1014	Test Condition C
7. Electrical Test: CTR		Per Table II, $T_A = 25°C$
8. Burn-In	1015	168 Hrs., $T_A = 125°C$ $V_{CC} = 5.5V$, $I_F = 20mA$, $V_{OC} = 3.5V$ $R_L = 270\Omega$
9. Electrical Test: CTR, I_{OH}, I_{CCL}, I_{CCH}, V_F, BV_R, I_{I-O}		Per Table II, $T_A = 25°C$
10. Evaluate Drift		Max. $\Delta CTR = \pm 20\%$
11. Sample Electrical Test: I_{OH}, I_{CCH}, I_{CCL}, CTR, V_F, BV_R		Per Table II, LTPD = 5, $T_A = -55°C$
12. Sample Electrical Test: I_{OH}, I_{CCH}, I_{CCL}, CTR, V_F, BV_R		Per Table II, LTPD = 5, $T_A = +125°C$
13. Sample Electrical Test: t_{PHL}, t_{PLH}		Per Table II, $T_A = 25°C$, LTPD = 5
14. External Visual	2009	

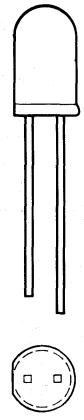
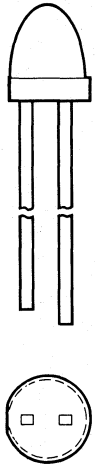
TABLE V. GROUP B

Examination or Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD
Subgroup 1			15
Physical Dimensions	2016	See Product Outline Drawing	
Subgroup 2			20
Solderability	2003	Immersion within 2.5mm of body, 16 terminations	
Subgroup 3			15
Temperature Cycling	1010	Test Condition C	
Thermal Shock	1011	Test Condition A	
Hermetic Seal, Fine Leak	1014	Test Condition A	
Hermetic Seal, Gross Leak	1014	Test Condition C	
End Points: I_{OH}, CTR, I_{CCH}, I_{CCL}, V_F, BV_R, I_{I-O}		Per Table II, $T_A = 25°C$	
Subgroup 4			15
Shock, non-operating	2002	1500 G, t = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	
Constant Acceleration	2001	5KG, Y_1	
End Points: Same as Subgroup 3			
Subgroup 5			15
Terminal Strength, tension	2004	Test Condition A, 4.5N (1 lb.), 15s	
Subgroup 6			
High Temperature Life	1008	$T_A = 150°C$	$\lambda = 7$
End Points: Same as Subgroup 3			
Subgroup 7			
Steady State Operating Life	1005	$V_{CC} = 5V$, $I_F = 20mA$, $T_A = 125°C$	$\lambda = 7$
End Points: Same as Subgroup 3		$V_{CC} = 3.5V$, $R_L = 270\Omega$	



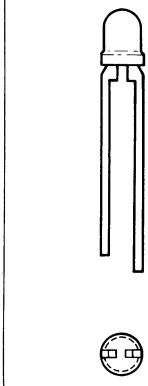
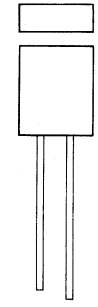
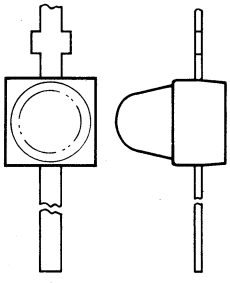
Solid State Lamps

High Efficiency Red, Yellow, Green LED Lamps

Device		Description			Typical Luminous Intensity	$2\Theta_{1/2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
	5082-4550	Yellow (538 nm)	T-1¾ [3]	Yellow Diffused	1.8 mcd @ 10mA	90°	2.2 Volts @ 10mA	113
	5082-4555				3.0 mcd @ 10mA			
	5082-4557			Yellow Non-Diffused	9.0 mcd @ 10mA	35°		
	5082-4558				16.0 mcd @ 10mA			
	5082-4650	High Efficiency Red (635 nm)		Red Diffused	2.0 mcd @ 10mA	90°		
	5082-4655				4.0 mcd @ 10mA			
	5082-4657			Red Non-Diffused	12.0 mcd @ 10mA	35°		
	5082-4658				24.0 mcd @ 10mA			
	5082-4950	Green (565 nm)		Green Diffused	1.8 mcd @ 20mA	90°	2.4 Volts @ 20mA	
	5082-4955				3.0 mcd @ 20mA			
	5082-4957			Green Non-Diffused	9.0 mcd @ 20mA	30°		
	5082-4958				16.0 mcd @ 20mA			
	5082-4590	Yellow (538 nm)	T-1¾ Low Profile	Yellow Diffused	3.5 mcd @ 10mA	50°	2.2 Volts @ 10mA	117
	5082-4592				6.0 mcd @ 10mA			
	5082-4595			Yellow Non-Diffused	6.5 mcd @ 10mA	45°		
	5082-4597				11.0 mcd @ 10mA			
	5082-4690	High Efficiency Red (635 nm)		Red Diffused	3.5 mcd @ 10mA	50°		
	5082-4693				7.0 mcd @ 10mA			
	5082-4694			Red Non-Diffused	8.0 mcd @ 10mA	45°		
	5082-4695				11.0 mcd @ 10mA			
	5082-4990	Green (565 nm)		Green Diffused	4.5 mcd @ 20mA	50°	2.4 Volts @ 20mA	
	5082-4992				7.5 mcd @ 20mA			
	5082-4995			Green Non-Diffused	6.5 mcd @ 20mA	40°		
	5082-4997				11.0 mcd @ 20mA			

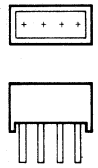
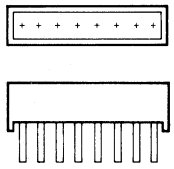
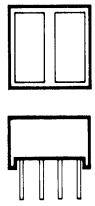
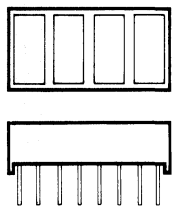
See Page 111 for Notes.

High Efficiency Red, Yellow, Green LED Lamps (continued)

Device		Description			Typical Luminous Intensity	$2\Theta\frac{1}{2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
	HLMP-1300	High Efficiency Red (635 nm)	T-1 [4]	Red Diffused	1.5 mcd @ 10mA	70°	2.2 Volts @ 10mA	123
	HLMP-1301				2.0 mcd @ 10mA			
	HLMP-1302				2.5 mcd @ 10mA			
	HLMP-1400	Yellow (583 nm)		Yellow Diffused	1.5 mcd @ 10mA	60°		
	HLMP-1401				2.5 mcd @ 10mA			
	HLMP-1402				4.0 mcd @ 10mA			
	HLMP-1500	Green (565 nm)		Green Diffused	1.2 mcd @ 10mA		2.4 Volts @ 20mA	
	HLMP-1501				2.0 mcd @ 10mA			
	HLMP-1502				3.0 mcd @ 10mA			
	HLMP-0300	High Efficiency Red (635 nm)	Rectangular	Red Diffused	1.0 mcd @ 25mA	100°	2.5 Volts @ 25mA	127
	HLMP-0301				2.5 mcd @ 25mA			
	HLMP-0400	Yellow (583 nm)		Yellow Diffused	1.2 mcd @ 25mA			
	HLMP-0401				2.5 mcd @ 25mA			
	HLMP-0500	Green (565 nm)		Green Diffused	1.2 mcd @ 25mA			
	HLMP-0501				2.5 mcd @ 25mA			
	5082-4150	Yellow (583 nm)	Subminiature with Radial Leads	Yellow Diffused	2.0 mcd @ 10mA	90°	2.2 Volts @ 10mA	131
	5082-4160	High Efficiency Red (635 nm)		Red Diffused	3.0 mcd @ 10mA	80°		
	5082-4190	Green (565 nm)		Green Diffused	1.5 mcd @ 20mA	70°	2.4 Volts @ 20mA	

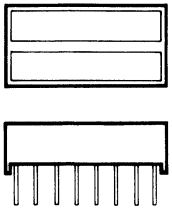
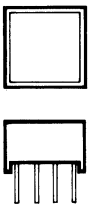
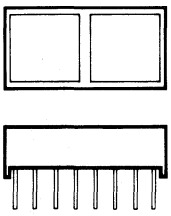
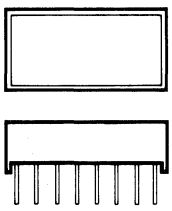
See Page 111 for Notes.

High Efficiency Red, Yellow, Green Light Bar Modules

Device		Description			Typical Luminous Intensity	$2\Theta\frac{1}{2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
	HLMP-2300	High Efficiency Red (635 nm)	4 Pin In-Line; .100" Centers; .400"L x .195"W x .240"H	Red Diffused	7 mcd @ 20mA	(Not Applicable)	1.9 Volts @ 20mA	135
	HLMP-2400	Yellow (538 nm)		Yellow Diffused	5 mcd @ 20mA		2.0 Volts @ 20mA	
	HLMP-2500	Green (565 nm)		Green Diffused	3.5 mcd @ 20mA		2.1 Volts @ 20mA	
	HLMP-2350	High Efficiency Red (635 nm)	8 Pin In-Line; .100" Centers; .800"L x .195"W x .240"H	Red Diffused	15 mcd @ 20mA		1.9 Volts @ 20mA	
	HLMP-2450	Yellow (538 nm)		Yellow Diffused	11 mcd @ 20mA		2.0 Volts @ 20mA	
	HLMP-2550	Green (565 nm)		Green Diffused	7.5 mcd @ 20mA		2.1 Volts @ 20mA	
	HLMP-2600	High Efficiency Red (635 nm)	8 Pin DIP; .100" Centers; .400L x .400"W x .240"H; Dual Arrangement	Red Diffused	7 mcd @ 20mA			139
	HLMP-2700	Yellow (538 nm)		Yellow Diffused	5 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2800	Green (565 nm)		Green Diffused	3.5 mcd @ 20mA			
	HLMP-2620	High Efficiency Red (635 nm)	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Quad Arrangement	Red Diffused	7 mcd @ 20mA		2.1 Volts @ 20mA	
	HLMP-2720	Yellow (538 nm)		Yellow Diffused	5 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2820	Green (565 nm)		Green Diffused	3.5 mcd @ 20mA			

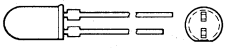
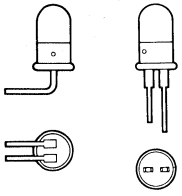
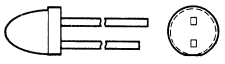
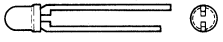
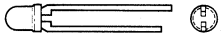
See Page 111 for Notes.

High Efficiency Red, Yellow, Green Light Bar Modules (continued)

Device		Description			Typical Luminous Intensity	$2\Theta_{1/2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
	HLMP-2635	High Efficiency Red (635 nm)	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Dual Bar Arrangement	Red Diffused	14 mcd @ 20mA	(Not Applicable)	2.1 Volts @ 20mA	139
	HLMP-2735	Yellow (538 nm)		Yellow Diffused	10 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2835	Green (565 nm)		Green Diffused	7 mcd @ 20mA			
	HLMP-2655	High Efficiency Red (635 nm)	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H; Square Arrangement	Red Diffused	14 mcd @ 20mA		2.1 Volts @ 20mA	
	HLMP-2755	Yellow (538 nm)		Yellow Diffused	10 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2855	Green (565 nm)		Green Diffused	7 mcd @ 20mA			
	HLMP-2670	High Efficiency Red (635 nm)	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Dual Square Arrangement	Red Diffused	14 mcd @ 20mA		2.1 Volts @ 20mA	
	HLMP-2770	Yellow (538 nm)		Yellow Diffused	10 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2870	Green (565 nm)		Green Diffused	7 mcd @ 20mA			
	HLMP-2685	High Efficiency Red (635 nm)	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Single Bar Arrangement	Red Diffused	28 mcd @20mA		2.1 Volts @ 20mA	
	HLMP-2785	Yellow (538 nm)		Yellow Diffused	20 mcd @ 20mA		2.2 Volts @ 20mA	
	HLMP-2885	Green (565 nm)		Green Diffused	14 mcd @ 20mA			

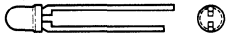
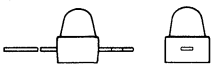
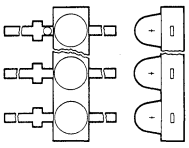
See Page 111 for Notes.

Red LED Lamps

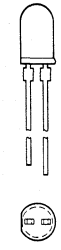
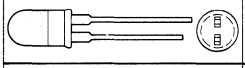
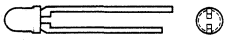
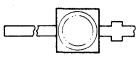
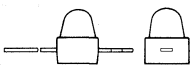
Device		Description			Typical Luminous Intensity	2Θ½[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	5082-4850	Red (655 nm)	T-1¾[3]	Red Diffused	0.8 mcd @ 20mA	95°	1.6 Volts @ 20mA	145
	5082-4855				1.4 mcd @ 20mA			
	5082-4403				1.2 mcd @ 20mA	75°		147
	5082-4440				0.7 mcd @ 20mA			
	5082-4415		[4]		1.2 mcd @ 20mA			
	5082-4444		[4]		0.7 mcd @ 20mA			
	5082-4880				0.8 mcd @ 20mA	58°		
	5082-4883			Clear Non-Diffused		50°		
	5082-4886			Clear Diffused		65°		
	5082-4881			Red Diffused	1.3 mcd @ 20mA	58°		
	5082-4884			Clear Non-Diffused		50°		
	5082-4887			Clear Diffused		65°		
	5082-4882			Red Diffused	1.8 mcd @ 20mA	58°		
	5082-4885			Clear Non-Diffused		50°		
	5082-4888			Clear Diffused		65°		
	5082-4790		T-1¾ Low Profile	Red Diffused	1.2 mcd @ 20mA	60°		117
	5082-4791				2.5 mcd @ 20mA			
	5082-4484		T-1[4]	Red Diffused	1.4 mcd @ 20mA	120°		145
	5082-4494							
	5082-4480				0.8 mcd @ 20mA			149
	5082-4483			Clear Diffused				
	5082-4486			Clear Non-Diffused		80°		

See Page 111 for Notes.

Red LED Lamps (continued)

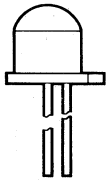
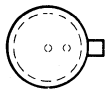
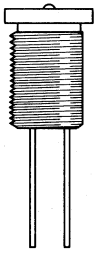
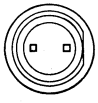
Device		Description			Typical Luminous Intensity	2Θ½[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	5082-4487	Red (655 nm)	T-1 Low Profile[4]	Clear Non-Diffused	0.8 mcd @ 20mA	120°	1.6 Volts @ 20mA	149
	5082-4488				Guaranteed Min. 0.3 mcd @ 20mA			
	5082-4100		Subminiature Radial Leads	Red Diffused	0.5 mcd @ 10mA	45°	1.6 Volts @ 10mA	131
	5082-4101				10 mcd @ 10mA			
	HLMP-6203		Subminiature Array Radial Leads					153
	HLMP-6204							
	HLMP-6205							

Integrated LED Lamps

Device		Description			Typical Luminous Intensity	2Θ½[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3600	High Eff. Red (635 nm)	T - 1¾[3]	Red Diffused	2.4 mcd @ 5V	90°	15mA @ 5V	155
	HLMP-3650	Yellow (538nm)		Yellow Diffused				
	HLMP-3680	Green (565 nm)		Green Diffused	1.8 mcd @ 5V			
	HLMP-3105	Red (655 nm)		Red Diffused	1.5 mcd @ 5V		20mA @5V	157
	HLMP-3112						14mA @12V	
	5082-4860				0.8 mcd @ 5V	58°	16mA @ 5V	159
	5082-4468		T - 1[4]	Clear Diffused		70°		
	5082-4732			Red Diffused	0.7 mcd @ 2.75V	95°	13mA @2.75V	161
	HLMP-6600		Subminiature; Radial Leads		2.4 mcd @5V	90°	9.6mA @5V	163
	HLMP-6620				0.6 mcd @5V		3.5mA @5V	

NOTES: 1. Θ½ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Peak Wavelength
3. Panel Mountable. For Panel Mounting Kit, see page 171.
4. PC Board Mountable
5. Military Approved and qualified for High Reliability Applications.

Hermetically Sealed and High Reliability LED Lamps

Device		Description			Minimum Luminous Intensity	$2\Theta_{1/2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
	1N5765 JAN 1N5765 [5] JANTX 1N5765 [5]	Red (655 nm)	Hermetic/TO-46 [4]	Red Diffused	0.5 mcd @ 20mA	70°	1.6 Volts @ 20mA	165
	1N6092 JAN 1N6092 [5] JANTX 1N6092 [5]	High Efficiency Red (635 nm)			1.0 mcd @ 20mA		2.0 Volts @ 20mA	
	1N6093 JAN 1N6093 [5] JANTX 1N6093 [5]	Yellow (583 nm)		Yellow Diffused				
	1N6094 JAN 1N6094 [5] JANTX 1N6094 [5]	Green (565 nm)		Green Diffused	0.8 mcd @ 25mA		2.1 Volts @ 20mA	
	5082-4787 HLMP-0930 [5] HLMP-0931 [5]	Red (655 nm)	Panel Mount Version	Red Diffused	0.5 mcd @ 20mA		1.6 Volts @ 20mA	
	5082-4687 M 19500/519-01 [5] M 19500/519-02 [5]	High Efficiency Red (635 nm)			1.0 mcd @ 20mA		2.0 Volts @ 20mA	
	5082-4587 M 19500/520-01 [5] M 19500/520-02 [5]	Yellow (583 nm)		Yellow Diffused				
	5082-4987 M 19500/521-01 [5] M 19500/521-02 [5]	Green (565 nm)		Green Diffused	0.8 mcd @ 25mA		2.1 Volts @ 20mA	

See Page 111 for Notes.

HEWLETT PACKARD

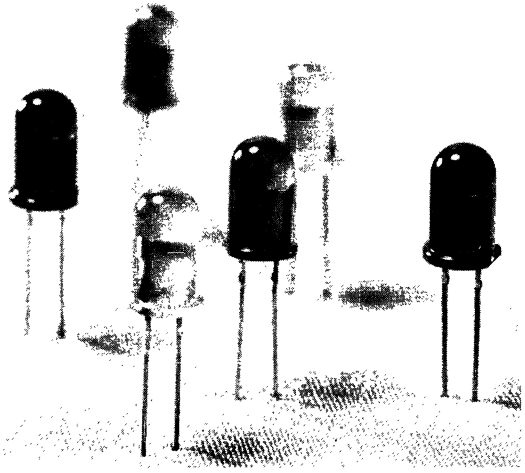
SOLID STATE LAMPS

HIGH EFFICIENCY RED • 5082-4650 Series
YELLOW • 5082-4550 Series
GREEN • 5082-4950 Series

TECHNICAL DATA MARCH 1980

Features

- **HIGH INTENSITY**
- **CHOICE OF 3 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **POPULAR T-1¾ DIAMETER PACKAGE**
- **LIGHT OUTPUT CATEGORIES**
- **WIDE VIEWING ANGLE AND NARROW VIEWING ANGLE TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**

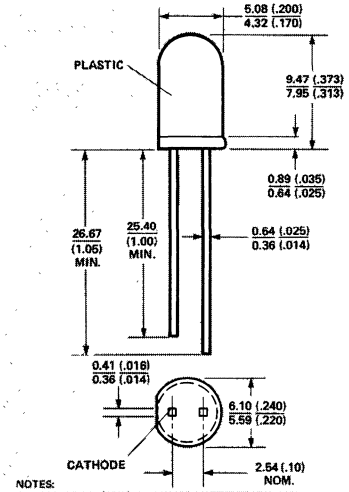


Description

The 5082-4650 and the 5082-4550 Series lamps are Gallium Arsenide Phosphide on Gallium Phosphide diodes emitting red and yellow light respectively. The 5082-4950 Series lamps are green light emitting Gallium Phosphide diodes.

General purpose and selected brightness versions of both the diffused and non-diffused lens type are available in each family.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Part Number 5082-	Application	Lens	Color
4650	Indicator — General Purpose	Diffused	High Efficiency Red
4655	Indicator — High Ambient	Wide Angle	
4657	Illuminator/Point Source	Non Diffused	
4658	Illuminator/High Brightness	Narrow Angle	
4550	Indicator General Purpose	Diffused	Yellow
4555	Indicator — High Ambient	Wide Angle	
4557	Illuminator/Point Source	Non-Diffused	
4558	Illuminator/High Brightness	Narrow Angle	
4950	Indicator — General Purpose	Diffused	Green
4955	Indicator — High Ambient	Wide Angle	
4957	Illuminator/Point Source	Non-Diffused	
4958	Illuminator/High Brightness	Narrow Angle	

Electrical Characteristics at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditons
I_V	Luminous Intensity	4650 4655 4657 4658	1.0 3.0 9.0 15.0	2.0 4.0 12.0 24.0		mcd.	I_F = 10mA (Fig. 3)
		4550 4555 4557 4558	1.0 2.2 6.0 12.0	1.8 3.0 9.0 16.0		mcd.	I_F = 10mA (Fig. 8)
		4950 4955 4957 4958	1.0 2.2 6.0 12.0	1.8 3.0 9.0 16.0		mcd.	I_F = 20mA (Fig. 13)
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4650 4655 4657 4658		90 90 35 35		Deg.	I_F = 10mA See Note 1 (Fig. 6)
		4550 4555 4557 4558		90 90 35 35		Deg.	I_F = 10mA See Note 1 (Fig. 11)
		4950 4955 4957 4958		90 90 30 30		Deg.	I_F = 20mA See Note 1 (Fig. 16)
λ_{PEAK}	Peak Wavelength	4650s 4550s 4950s		635 583 565		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength	4650s 4550s 4950s		626 585 572		nm	See Note 2 (Fig.1)
τ_S	Speed of Response	4650s 4550s 4950s		90 90 200		ns	
C	Capacitance	4650s 4550s 4950s		16 18 18		pF	V_F = 0, f = 1 MHz
Θ_{JC}	Thermal Resistance	4650s 4550s 4950s		135 135 145		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	4650s 4550s 4950s		2.2 2.2 2.4	3.0 3.0 3.0	V	I_F = 10mA (Fig. 2, I_F = 10mA Fig. 7, I_F = 20mA Fig. 12)
BV_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100μA
η_V	Luminous Efficacy	4650s 4550s 4950s		147 570 665		lumens/watt	See Note 3

NOTES:

1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at T_A=25°C

Parameter	High Efficiency Red 4650 Series	Yellow 4550 Series	Green 4950 Series	Units
Power Dissipation	120	120	120	mW
DC Forward Current	20[1]	20[1]	30[2]	mA
Peak Operating Forward Current	60 (Fig. 5)	60 (Fig. 10)	60 (Fig. 15)	mA
Operating and Storage Temperature Range	-55°C to +100°C			
Lead Solder Temperature (1.6mm[0.063 inch] below package base)	260°C for 5 seconds			

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.4mA/°C

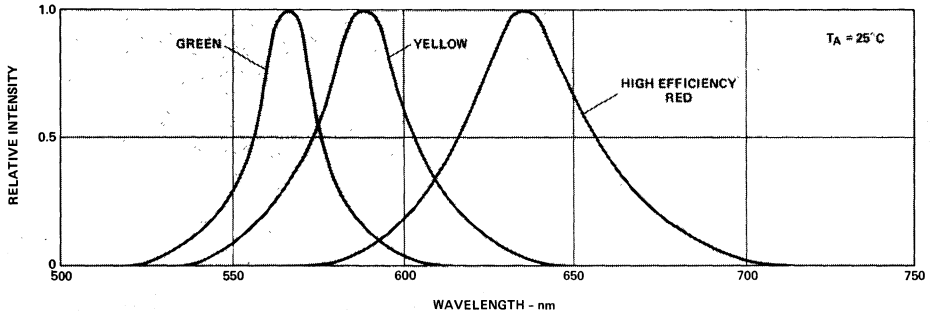


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red 5082-4650 Series

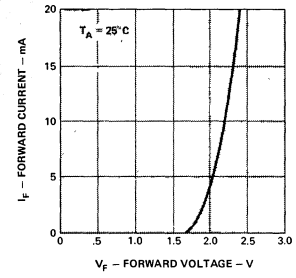


Figure 2. Forward Current vs. Forward Voltage

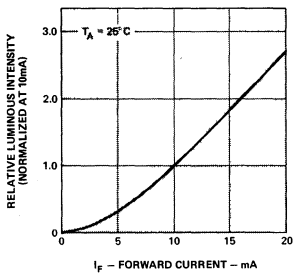


Figure 3. Relative Luminous Intensity vs. Forward Current.

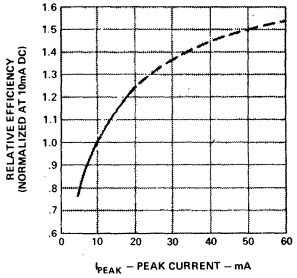


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

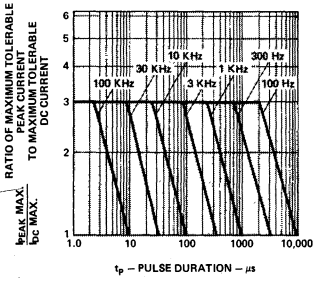


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

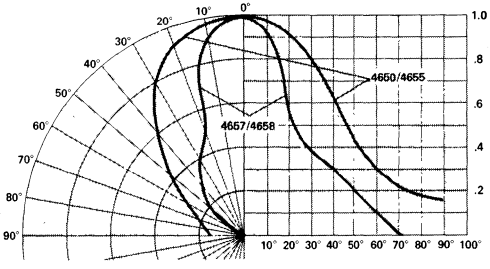


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow 5082-4550 Series

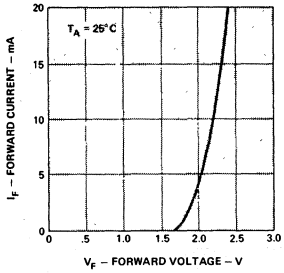


Figure 7. Forward Current vs. Forward Voltage.

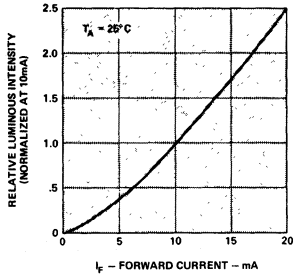


Figure 8. Relative Luminous Intensity vs. Forward Current.

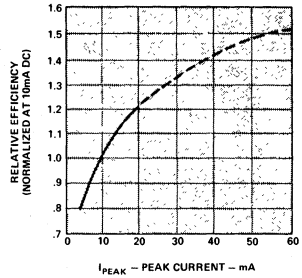


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

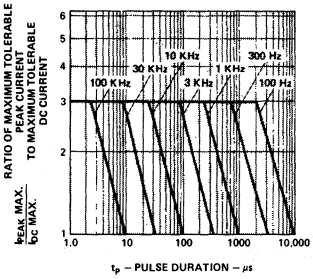


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

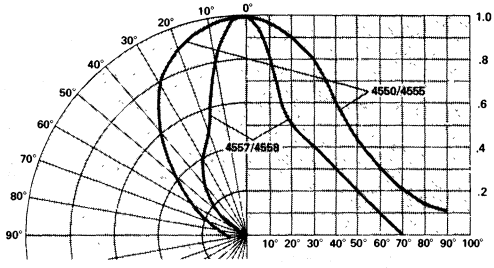


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Green 5082-4950 Series

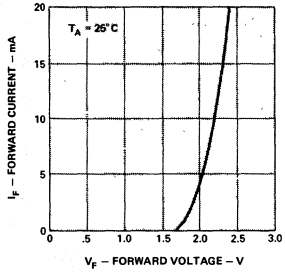


Figure 12. Forward Current vs. Forward Voltage.

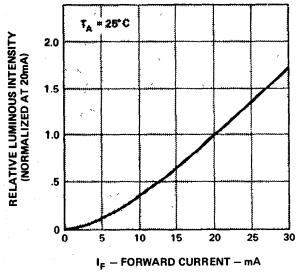


Figure 13. Relative Luminous Intensity vs. Forward Current.

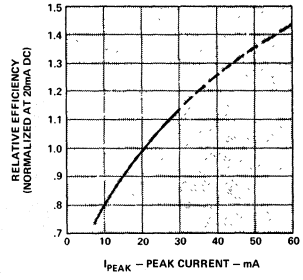


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

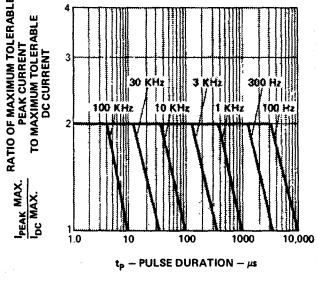


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

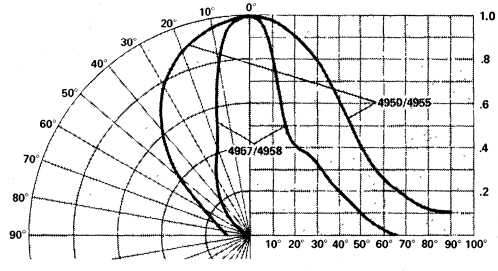


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

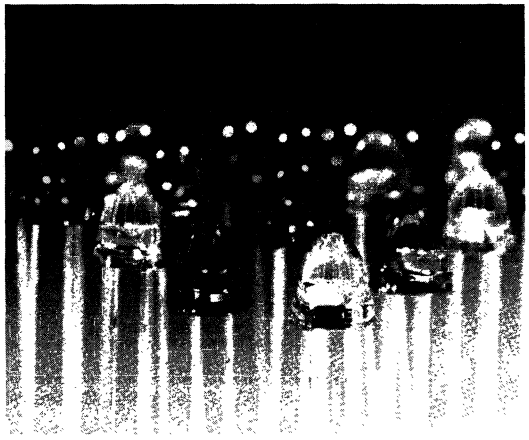
LOW PROFILE SOLID STATE LAMPS

RED • 5082-4790 SERIES
HIGH EFFICIENCY RED • 5082-4690 SERIES
YELLOW • 5082-4590 SERIES
GREEN • 5082-4990 SERIES

TECHNICAL DATA MARCH 1980

Features

- **HIGH INTENSITY**
- **LOW PROFILE: 5.8mm (0.23 In) NOMINAL**
- **T-1¾ DIAMETER PACKAGE**
- **LIGHT OUTPUT CATEGORIES**
- **DIFFUSED AND NON-DIFFUSED TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**
- **CHOICE OF 4 BRIGHT COLORS**
  Red High Efficiency Red
  Yellow Green



Description

The 5082-4790/4791 are Gallium Arsenide Phosphide Red Light Emitting Diodes packaged in a Low Profile T-1¾ outline with a red diffused lens.

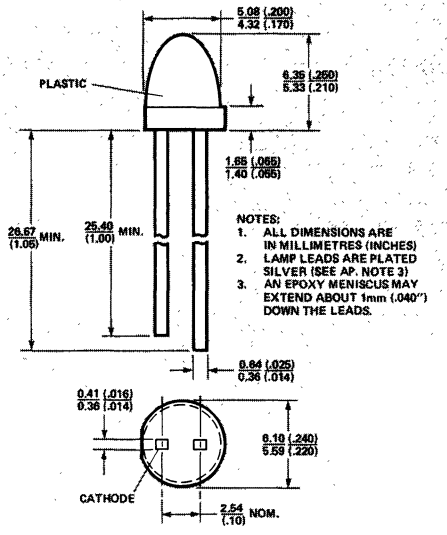
The 5082-4690 Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The 5082-4590 Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The 5082-4990 Series are Gallium Phosphide Green Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.

Package Dimensions



Part Number 5082-	Application	Lens	Color
4690	Indicator — General Purpose	Diffused Wide Angle	High Efficiency Red
4693	Indicator — High Brightness		
4694	General Purpose Point Source	Non-diffused Narrow Angle	
4695	High Brightness Annunciator		
4590	Indicator — General Purpose	Diffused Wide Angle	Yellow
4592	Indicator — High Brightness		
4595	General Purpose Point Source	Non-diffused Narrow Angle	
4597	High Brightness Annunciator		
4990	Indicator — General Purpose	Diffused Wide Angle	Green
4992	Indicator — High Brightness		
4995	General Purpose Point Source	Non-diffused Narrow Angle	
4997	High Brightness Annunciator		
4790	Indicator — General Purpose	Diffused Wide Angle	Red
4791	Indicator — High Brightness		

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 4790 Series	Hi-Eff. Red 4690 Series	Yellow 4590 Series	Green 4990 Series	Units
Power Dissipation	100	120	120	120	mW
DC Forward Current	50[1]	20[1]	20[1]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-55°C to + 100°C				
Lead Solder Temperature (1.6mm [0.63 inch] from body)	260°C For 5 Seconds				

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.4mA/°C

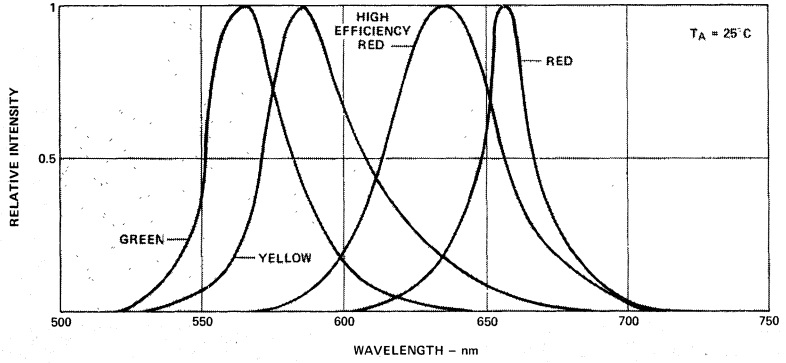


Figure 1. Relative Intensity versus Wavelength.

RED 5082-4790 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4790	0.8	1.2		mcd	I_F = 20mA (Fig. 3)
		4791	1.6	2.5			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points			60		deg.	Note 1 (Fig. 6)
λ_{PEAK}	Peak Wavelength			655		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			648		nm	Note 2
τ_s	Speed of Response			15		ns	
C	Capacitance			100		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			125		°C/W	Junction to Cathode Lead 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage			1.6	2.0	V	I_F = 20mA (Fig. 2)
BV_R	Reverse Breakdown Voltage		3	10		V	I_R = 100μA
η_V	Luminous Efficacy			55		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

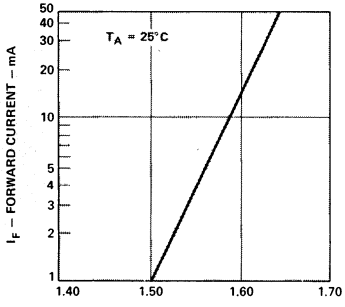


Figure 2. Forward Current versus Forward Voltage.

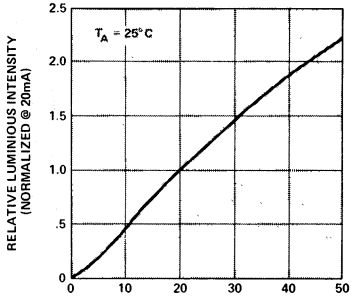


Figure 3. Relative Luminous Intensity versus Forward Current.

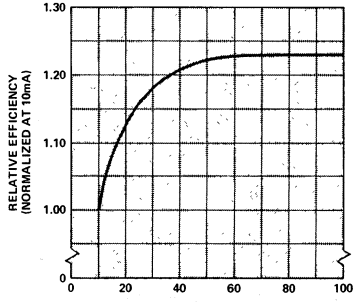


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

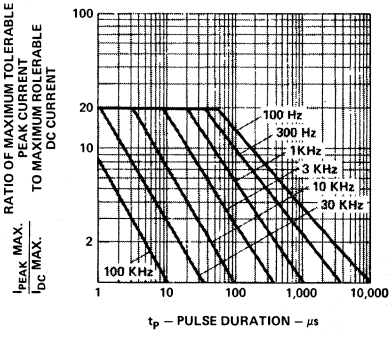


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

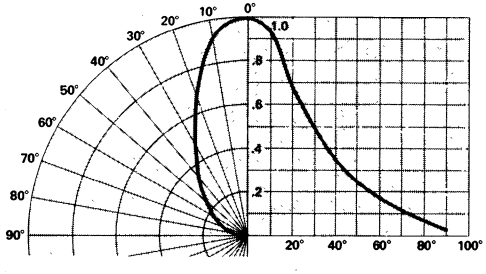


Figure 6. Relative Luminous Intensity versus Angular Displacement.

HIGH EFFICIENCY RED 5082-4690 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4690 4693 4694 4695	1.5 5.0 4.0 8.0	3.5 7.0 8.0 11.0		mcd	I_F = 10mA (Fig.8)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4690 4693 4694 4695		50 50 45 45		deg.	Note 1 (Fig. 11)
λ_{PEAK}	Peak Wavelength			635		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			626		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			16		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			130		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.2	3.0	V	I_F = 10mA (Fig. 7)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			147		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

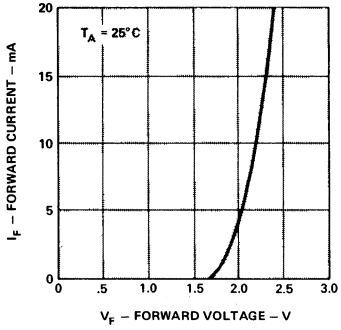


Figure 7. Forward Current versus Forward Voltage.

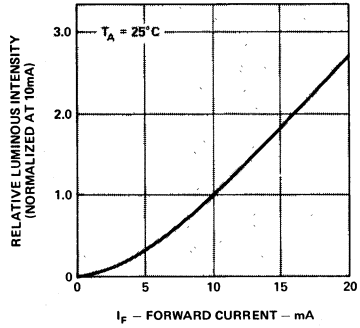


Figure 8. Relative Luminous Intensity versus Forward Current.

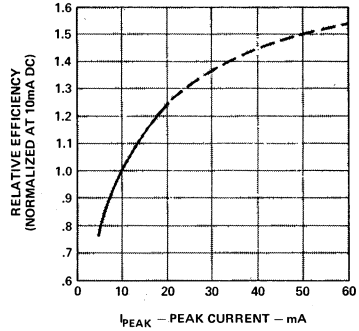


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

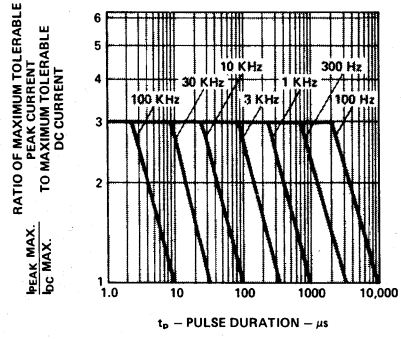


Figure 10. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

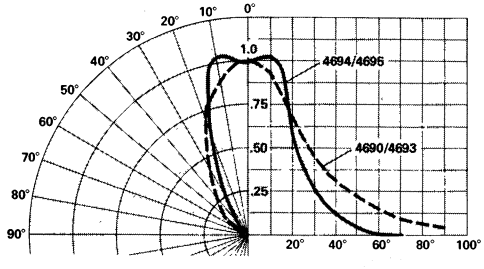


Figure 11. Relative Luminous Intensity versus Angular Displacement.

YELLOW 5082-4590 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4590 4592 4595 4597	1.5 4.5 4.0 8.0	3.5 6.0 6.5 11.0		mcd	I_F = 10mA (Fig. 13)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4590 4592 4595 4597		50 50 45 45		deg.	Note 1 (Fig. 16)
λ_{PEAK}	Peak Wavelength			583		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			585		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			100		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.2	3.0	V	I_F = 10mA (Fig. 12)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			570		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

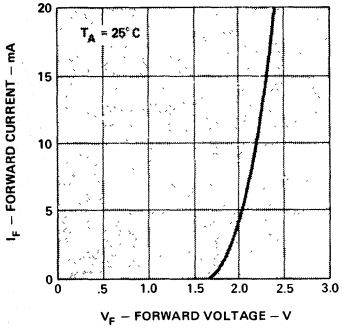


Figure 12. Forward Current versus Forward Voltage.

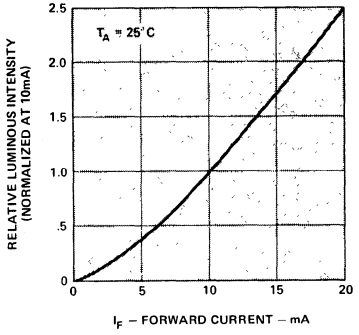


Figure 13. Relative Luminous Intensity versus Forward Current.

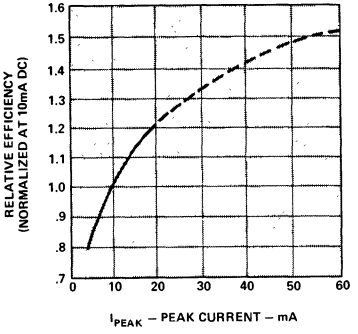


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

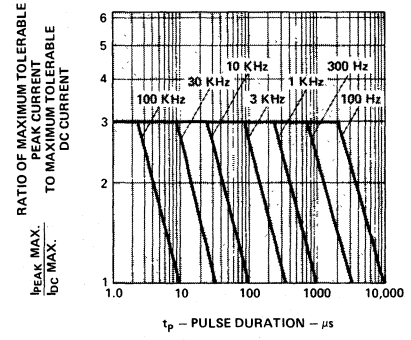


Figure 15. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings).

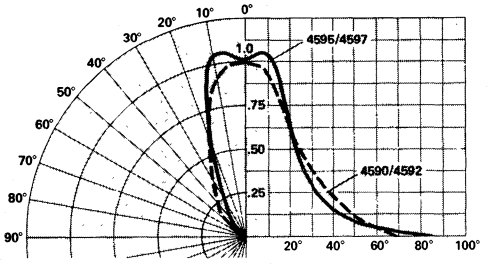


Figure 16. Relative Luminous Intensity versus Angular Displacement

SOLID STATE LAMPS

GREEN 5082-4990 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4990 4992 4995 4997	2.0 6.0 3.5 8.0	4.5 7.5 6.5 11.0		mcd	I_F = 20mA (Fig.18)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4990 4992 4995 4997		50 50 40 40		deg.	Note 1 (Fig.21)
λ_{PEAK}	Peak Wavelength			565		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			570		nm	Note 2
τ_s	Speed of Response			200		ns	
C	Capacitance			12		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			90		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.4	3.0	V	I_F = 20mA (Fig. 17)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			665		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

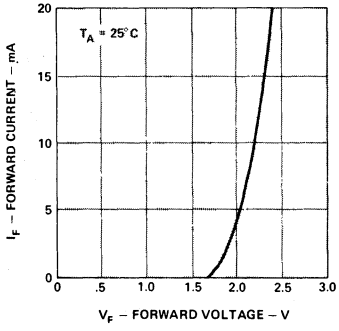


Figure 17. Forward Current versus Forward Voltage.

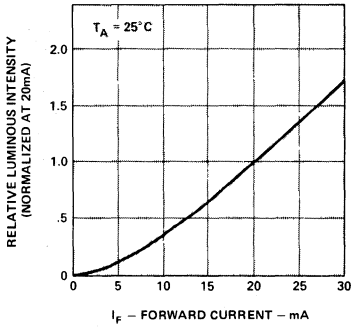


Figure 18. Relative Luminous Intensity versus Forward Current.

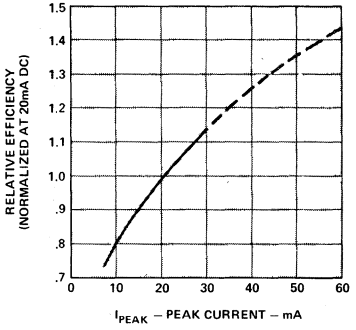


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

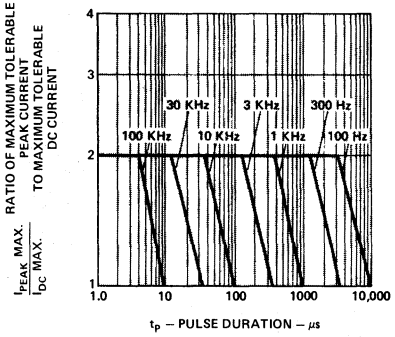


Figure 20. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX ratings).

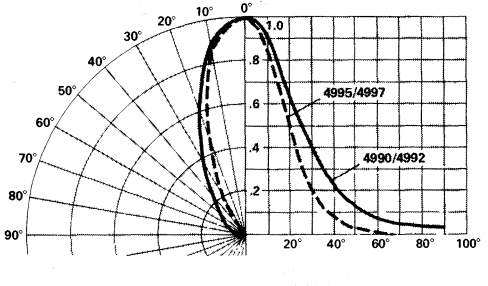


Figure 21. Relative Luminous Intensity versus Angular Displacement.

HEWLETT PACKARD

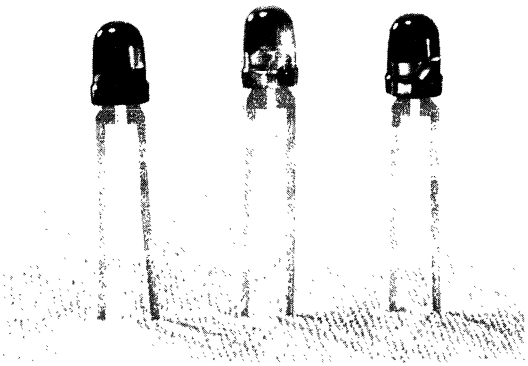
SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-1300,-1301,-1302
YELLOW • HLMP-1400,-1401,-1402
GREEN • HLMP-1500,-1501,-1502

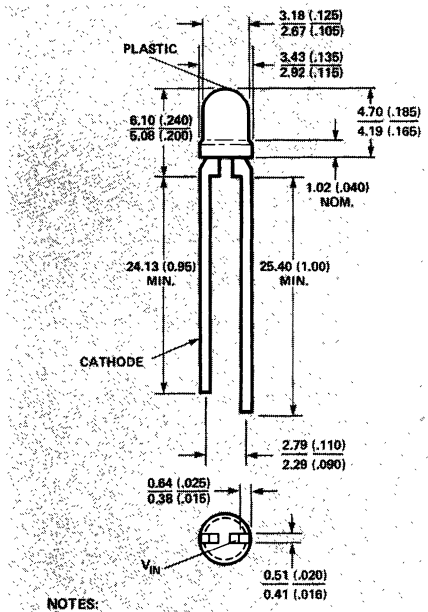
TECHNICAL DATA MARCH 1980

Features

- **HIGH INTENSITY**
- **WIDE VIEWING ANGLE**
- **SMALL SIZE T-1 DIAMETER 3.18mm (0.125 inch)**
- **IC COMPATIBLE**
- **RELIABLE AND RUGGED**
- **CHOICE OF 3 BRIGHT COLORS**
  - **HIGH EFFICIENCY RED**
  - **YELLOW**
  - **GREEN**



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

The HLMP-1300, -1301, and -1302 have a Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diode packaged in a T-1 outline with a red diffused lens, which provides excellent on-off contrast ratio, high axial luminous intensity and a wide viewing angle.

The HLMP-1400, -1401, and -1402 have a Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diode packaged in a T-1 outline with a yellow diffused lens, which provides good on-off contrast ratio, high axial luminous intensity and a wide viewing angle.

The HLMP-1500, -1501, and -1502 have a Gallium Phosphide Green Light Emitting Diode packaged in a T-1 outline with a green diffused lens, which provides good on-off contrast ratio, high axial luminous intensity, and a wide viewing angle.

I_V — Axial Luminous Intensity at 25°C (Figures 3,8,15)

	I_V (mcd)		
	Min.	**Typ.**	**Test Conditions**
High Efficiency Red			
HLMP-1300	0.5	1.5	
HLMP-1301 (-4684)	1.0	2.0	I_F=10 mA
HLMP-1302	2.0	2.5	
Yellow			
HLMP-1400	0.5	1.5	
HLMP-1401 (-4584)	1.0	2.5	I_F=10 mA
HLMP-1402	2.5	4.0	
Green			
HLMP-1500	0.5	1.2	
HLMP-1501 (-4984)	0.8	2.0	I_F=20 mA
HLMP-1502	2.0	3.0	

SOLID STATE LAMPS

Absolute Maximum Ratings at T_A=25°C

Parameter	High Efficiency Red HLMP-1300,1301,1302	Yellow HLMP-1400,1401,1402	Green HLMP-1500,1501,1502	Units
Power Dissipation	120	120	120	mW
DC Forward Current	20[1]	20[1]	30[2]	mA
Peak Forward Current	60 See Figure 5	60 See Figure 10	60 See Figure 15	mA
Operating and Storage Temperature Range	-55°C to 100°C			
Lead Soldering Temperature [1.6mm (0.063 in.) from Body]	230°C for 7 Seconds			

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.4mA/°C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-1300, -1301, -1302			HLMP-1400, -1401, -1402			HLMP-1500, -1501, -1502			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		70			60			60		Deg.	Note 1 (Figs. 6, 11, 16)
λ_{peak}	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		628			585			572		nm	Note 2
τ_s	Speed of Response		90			90			200		ns	
C	Capacitance		20			15			8		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance		95			95			95		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
V_F	Forward Voltage		2.2	3.0		2.2	3.0		2.4 at I_F = 20mA	3.0	V	I_F=10mA (Figs. 2,7,12)
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R=100μA
η_v	Luminous Efficacy		147			570			665		lm/W	Note 3

1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

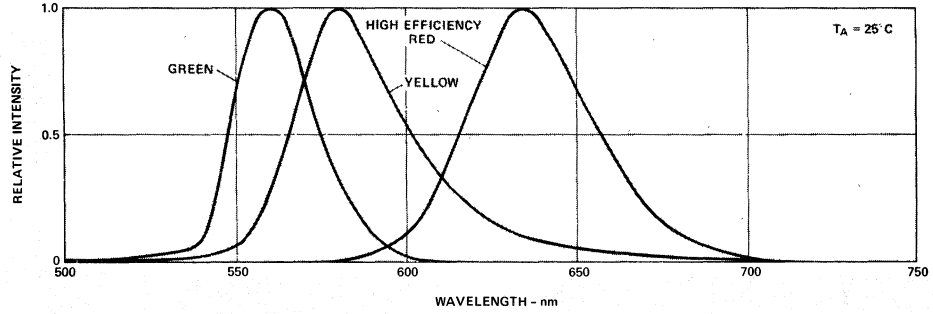


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red HLMP-1300,-1301,-1302

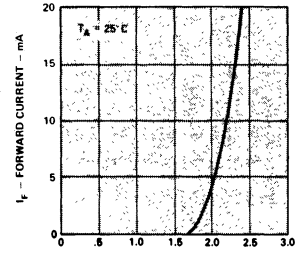


Figure 2. Forward Current vs. Forward Voltage.

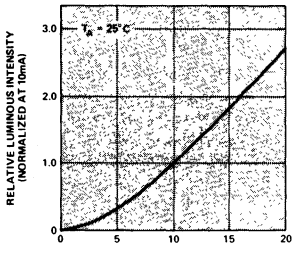


Figure 3. Relative Luminous Intensity vs. Forward Current.

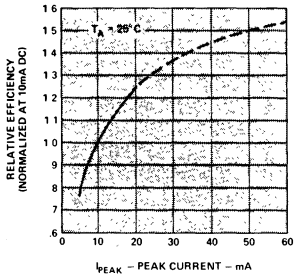


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

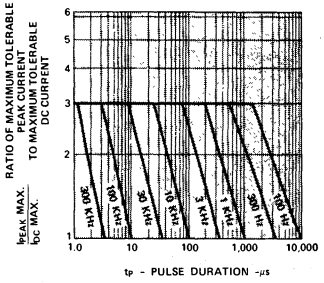


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings).

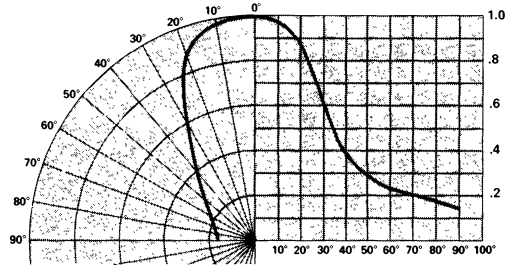


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-1400,-1401,-1402

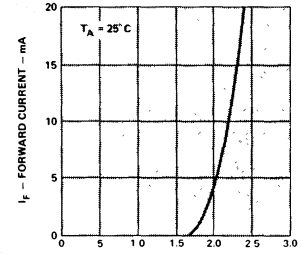


Figure 7. Forward Current vs. Forward Voltage.

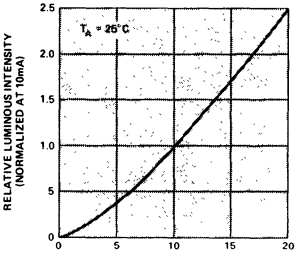


Figure 8. Relative Luminous Intensity vs. Forward Current.

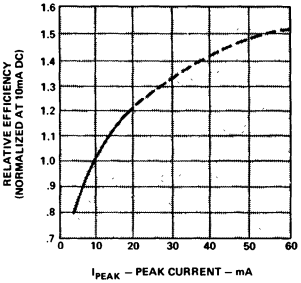


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

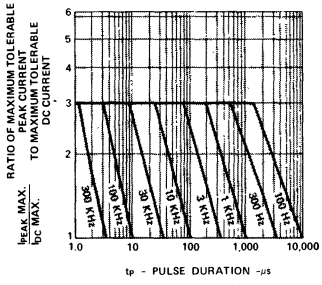


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

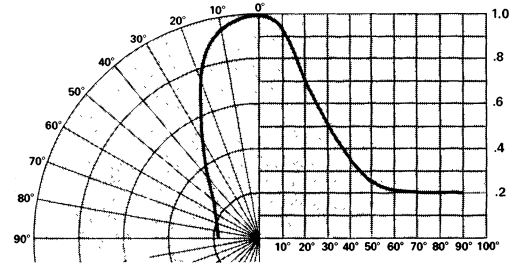


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-1500,-1501,-1502

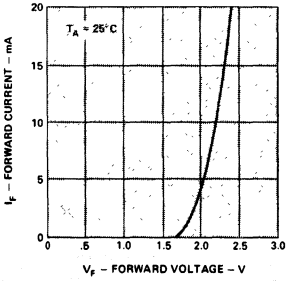


Figure 12. Forward Current vs. Forward Voltage.

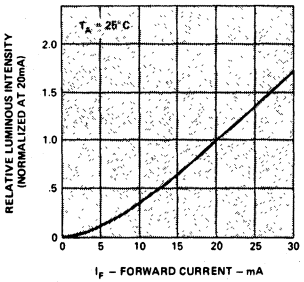


Figure 13. Relative Luminous Intensity vs. Forward Current.

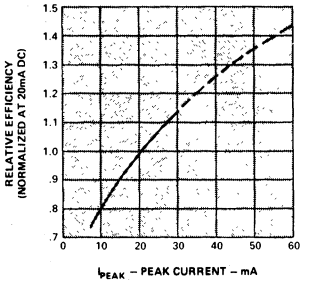


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

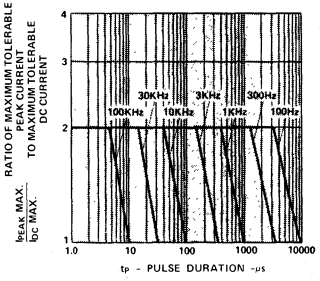


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

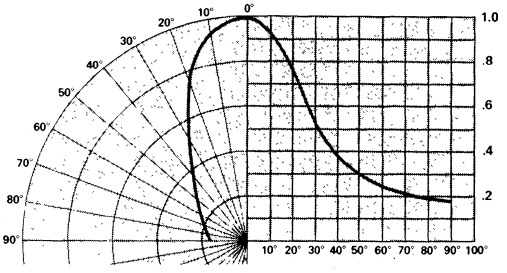


Figure 16. Relative Luminious Intensity vs. Angular Displacement.

HEWLETT PACKARD

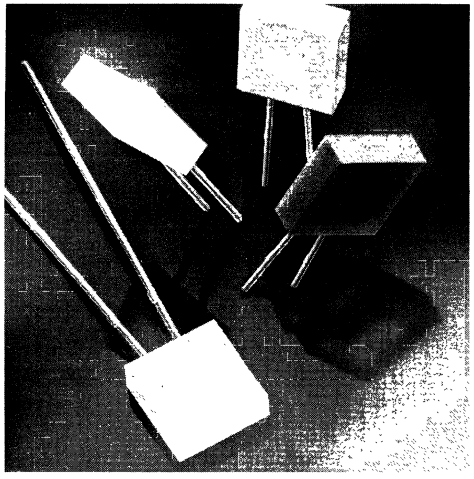
RECTANGULAR SOLID STATE LAMPS

HIGH EFFICIENCY RED HLMP-0300/0301
YELLOW HLMP-0400/0401
GREEN HLMP-0500/0501

TECHNICAL DATA MARCH 1980

Features

- **RECTANGULAR LIGHT EMITTING SURFACE**
- **FLAT HIGH STERANCE EMITTING SURFACE**
- **STACKABLE ON 2.54 MM (0.100 INCH) CENTERS**
- **IDEAL AS FLUSH MOUNTED PANEL INDICATORS**
- **IDEAL FOR BACKLIGHTING LEGENDS**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **CHOICE OF 3 BRIGHT COLORS**
  - **HIGH EFFICIENCY RED**
  - **YELLOW**
  - **GREEN**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**



SOLID STATE LAMPS

Description

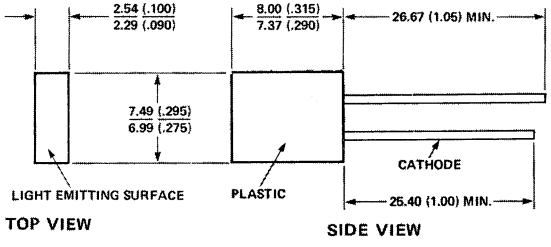
The HLMP-03XX, -04XX, -05XX are solid state lamps encapsulated in an axial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

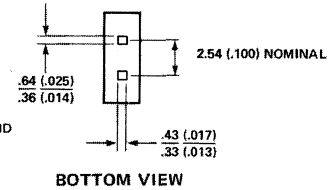
The HLMP-0300 and -0301 have a high-efficiency red GaAsP on GaP LED chip in a light red epoxy package. This lamp's efficiency is comparable to that of the Gap red, but extends to higher current levels.

The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.

The HLMP-0500 and -0501 provide a green GaP LED chip in a green epoxy package.

Package Dimensions





NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

AXIAL LUMINOUS INTENSITY

		MIN.	TYP.	TEST CONDITIONS
HER	HLMP-0300	.8	1.0 mcd	I_F = 25mA
	HLMP-0301	1.5	2.5 mcd	I_F = 25mA
		.8	1.5 mcd	I_F = 15mA
YELLOW	HLMP-0400	1.0	1.2 mcd	I_F = 25mA
	HLMP-0401	2.0	2.5 mcd	I_F = 25mA
		1.0	1.5 mcd	I_F = 15mA
GREEN	HLMP-0500	1.0	1.2 mcd	I_F = 25mA
	HLMP-0501	1.5	2.5 mcd	I_F = 25mA
		1.0	1.5 mcd	I_F = 20mA

NOTE: Luminous sterance, L_V, in foot lamberts, may be found from the equation $L_V = 16.7\ I_V$, where I_V is the luminous intensity in millicandelas.

Absolute Maximum Ratings at T_A=25°C

Parameter	High-Efficiency Red HLMP-0300/0301	Yellow HLMP-0400/0401	Green HLMP-0500/0501	Units
Power Dissipation	120	120	120	mW
DC Forward Current	30 [1]	30 [1]	30 [1]	mA
Peak Forward Current	60 See Figure 5	60 See Figure 10	60 See Figure 15	mA
Operating and Storage Temperature Range	-55°C to 100°C			
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 5 seconds			

1. Derate from 50°C at 0.4mA/°C.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-0300/0301			HLMP-0400/0401			HLMP-0500/0501			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points, Both Axes		100			100			100		deg.	Note 1. Figures 6,11,16
λ_{PEAK}	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		626			585			571		nm	Note 2
τ_S	Speed of Response		90			90			200		ns	
C	Capacitance		17			17			17		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance		130			130			130		°C/W	Junction to Cathode Lead at 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage		2.5	3.0		2.5	3.0		2.5	3.0	V	I_F= 25mA Figures 2,7,12
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100 μA
η_V	Luminous Efficacy		147			570			665		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

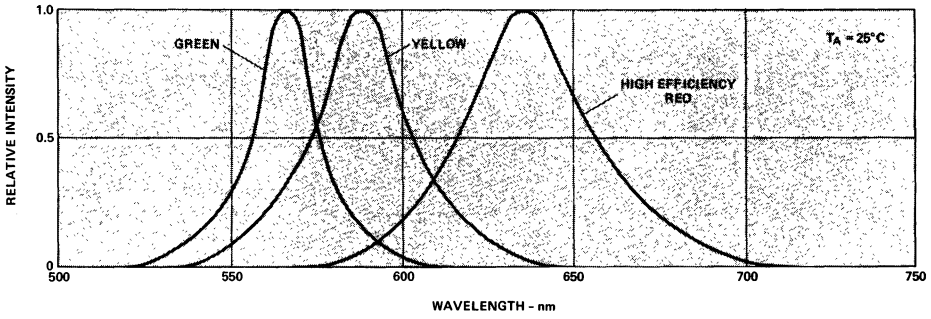


Figure 1. Relative Intensity vs. Wavelength.

HIGH EFFICIENCY RED HLMP-0300/0301

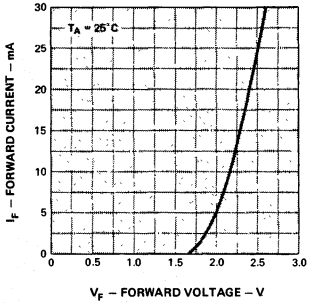


Figure 2. Forward Current vs. Forward Voltage.

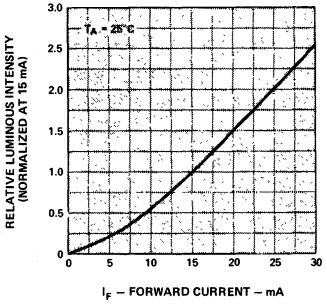


Figure 3. Relative Luminous Intensity vs. Forward Current.

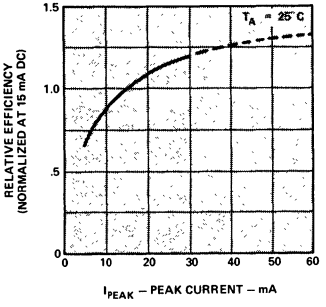


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

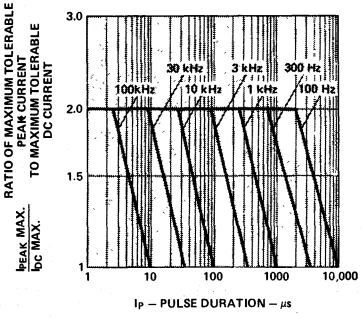


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

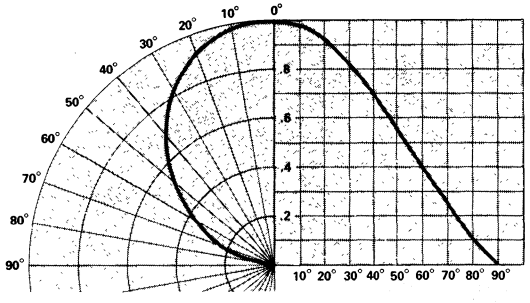


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

YELLOW HLMP-0400/0401

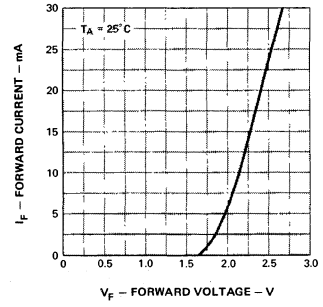


Figure 7. Forward Current vs. Forward Voltage.

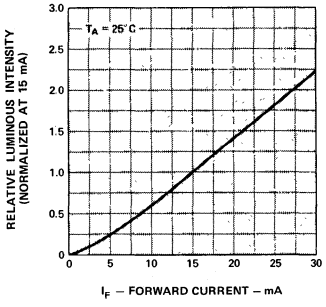


Figure 8. Relative Luminous Intensity vs. Forward Current.

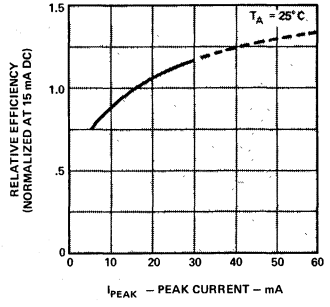


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

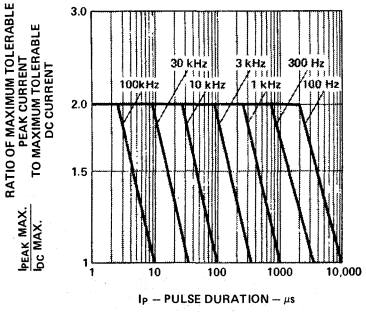


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

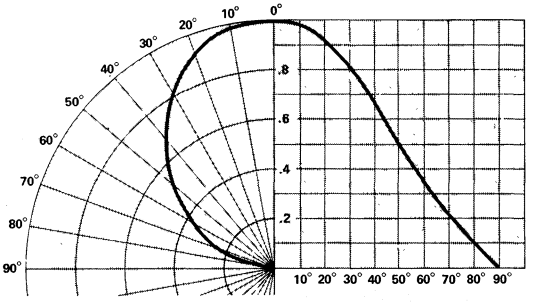


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

GREEN HLMP-0500/0501

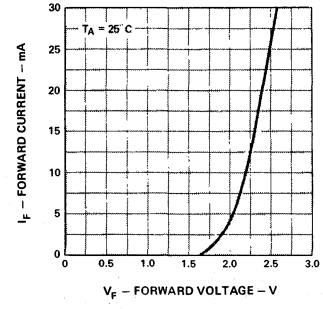


Figure 12. Forward Current vs. Forward Voltage.

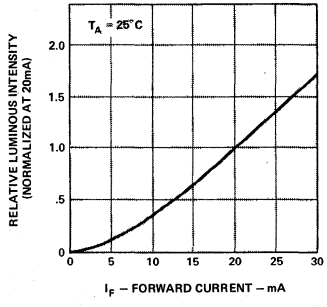


Figure 13. Relative Luminous Intensity vs. Forward Current.

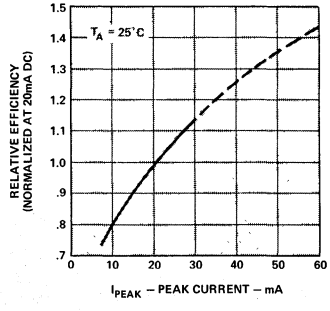


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

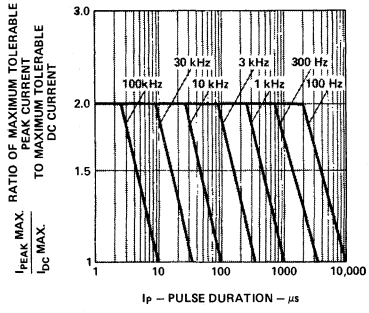


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

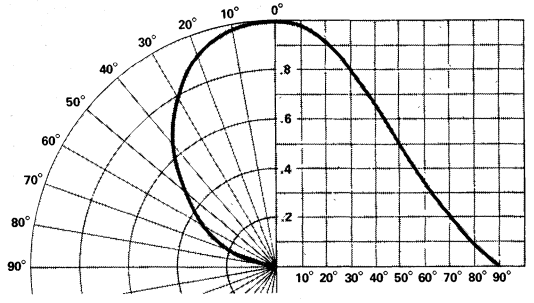


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

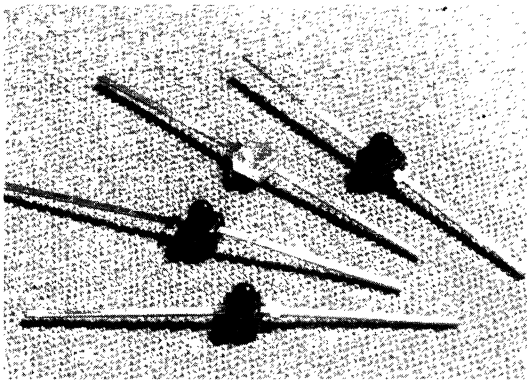
SUBMINIATURE SOLID STATE LAMPS

RED • 5082-4100/4101
HIGH EFFICIENCY RED • 5082-4160
YELLOW • 5082-4150
GREEN • 5082-4190

TECHNICAL DATA MARCH 1980

Features

- **SUBMINIATURE PACKAGE STYLE**
- **END STACKABLE ON 2.21mm (0.087 in.) CENTERS**
- **LOW PACKAGE PROFILE**
- **RADIAL LEADS**
- **WIDE VIEWING ANGLE**
- **LONG LIFE — SOLID STATE RELIABILITY**
- **CHOICE OF 4 BRIGHT COLORS**
  - **Red**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**



SOLID STATE LAMPS

Description

The 5082-4100/4101, 4150, 4160 and 4190 are solid state lamps encapsulated in a radial lead subminiature package of molded epoxy. They utilize a tinted, diffused lens providing high on-off contrast and wide-angle viewing.

The -4100/4101 utilizes a GaAsP LED chip in a deep red molded package.

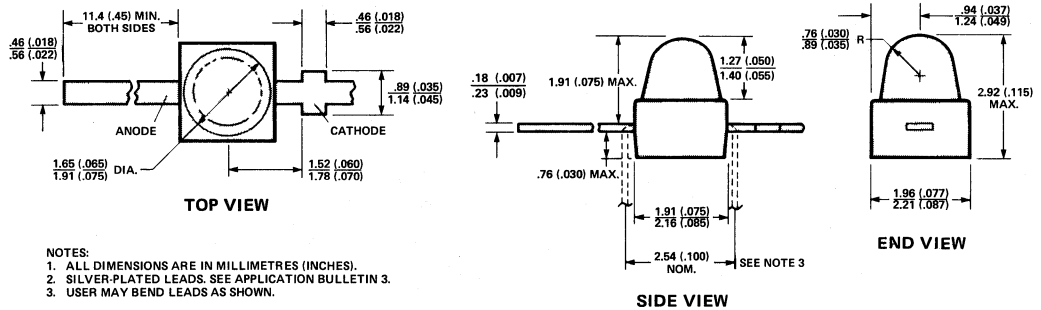
The -4160 has a high-efficiency red GaAsP on GaP LED chip in a light red molded package. This lamp's efficiency is comparable to that of the GaP red but does not saturate at low current levels.

The -4150 provides a yellow GaAsP on GaP LED chip in a yellow molded package.

The -4190 provides a green GaP LED chip in a green molded package.

Tape-and-reel mounting is available on request.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 4100/4101	High Eff. Red 4160	Yellow 4150	Green 4190	Units
Power Dissipation	100	120	120	120	mW
DC Forward Current	50[1]	20[1]	20[1]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-55°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	245°C for 3 seconds				

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.4mA/°C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	5082-4100/4101			5082-4160			5082-4150			5082-4190			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	-/0.5	.7/1.0		1.0	3.0		1.0	2.0		0.8	1.5		mcd	I_F=10mA, Figs. 3,8,13,18
											At I_F = 20mA				
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		45			80			90			70		deg.	Note 1, Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			628			585			572		nm	Note 2
τ_S	Speed of Response		15			90			90			200		ns	
C	Capacitance		100			11			15			13		pF	V_F=0; f=1 MHz
θ_{JC}	Thermal Resistance		125			120			100			100		°C/W	Junction to Cathode Lead at 0.79mm (.031 in) from Body
V_F	Forward Voltage		1.6	2.0		2.2	3.0		2.2	3.0		2.4	3.0	V	I_F=10mA, Figures 2, 7, 12, 17
											At I_F = 20mA				
BV_R	Reverse Breakdown Voltage	3.0	10		5.0			5.0			5.0			V	I_R = 100μA
η_V	Luminous Efficacy		55			147			570			665		lm/W	Note 3

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

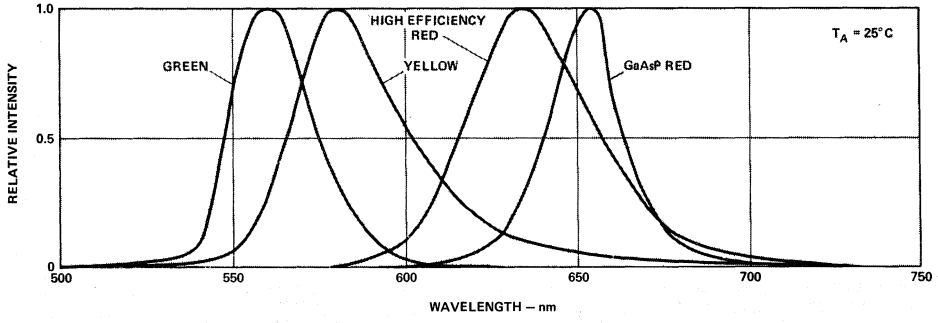


Figure 1. Relative Intensity vs. Wavelength.

Red 5082-4100/4101

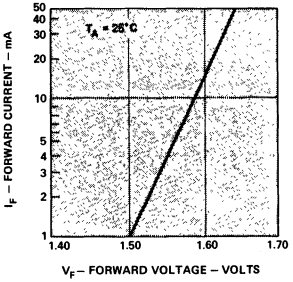


Figure 2. Forward Current vs. Forward Voltage.

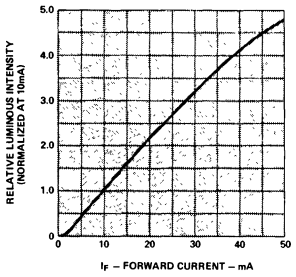


Figure 3. Relative Luminous Intensity vs. Forward Current.

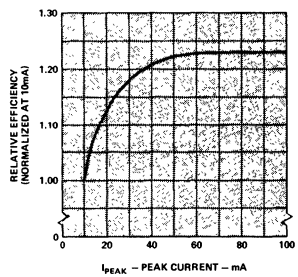


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

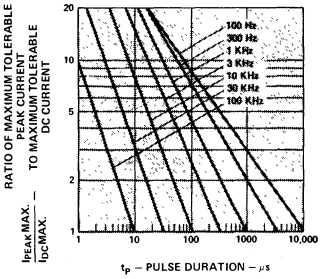


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

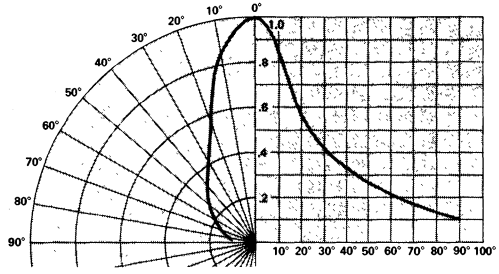


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red 5082-4160

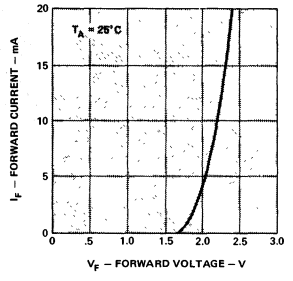


Figure 7. Forward Current vs. Forward Voltage.

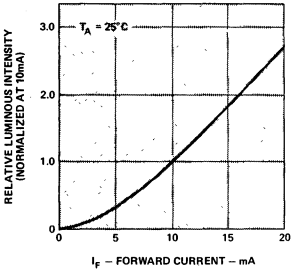


Figure 8. Relative Luminous Intensity vs. Forward Current.

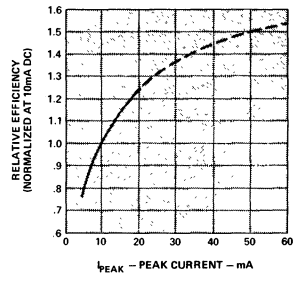


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

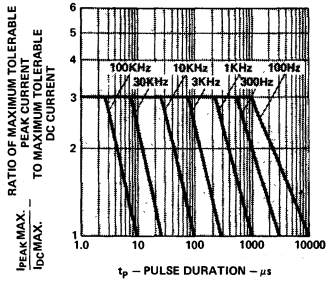


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

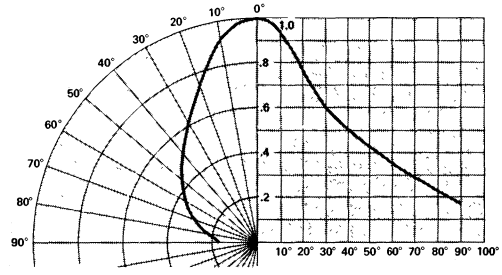


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Yellow 5082-4150

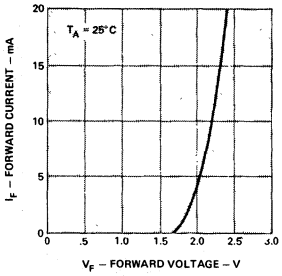


Figure 12. Forward Current vs. Forward Voltage.

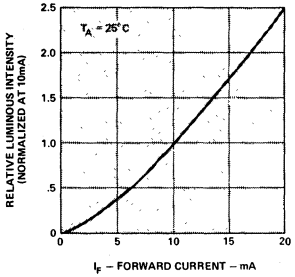


Figure 13. Relative Luminous Intensity vs. Forward Current.

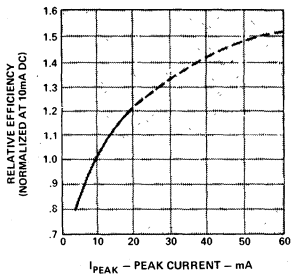


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

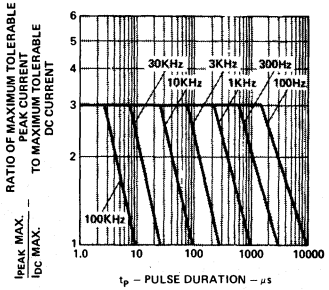


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

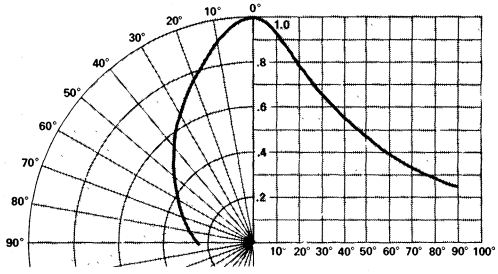


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green 5082-4190

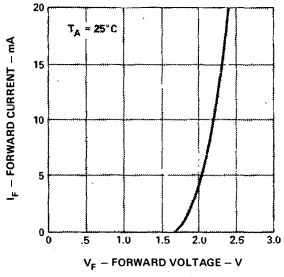


Figure 17. Forward Current vs. Forward Voltage.

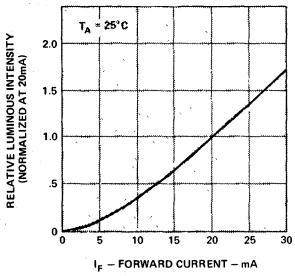


Figure 18. Relative Luminous Intensity vs. Forward Current.

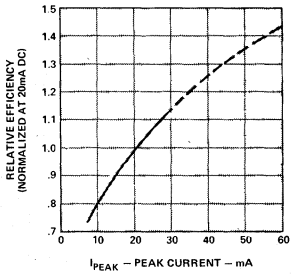


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

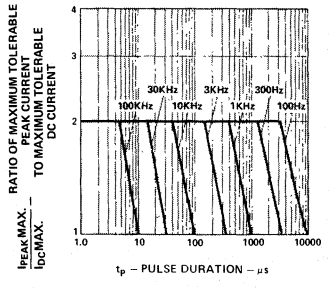


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

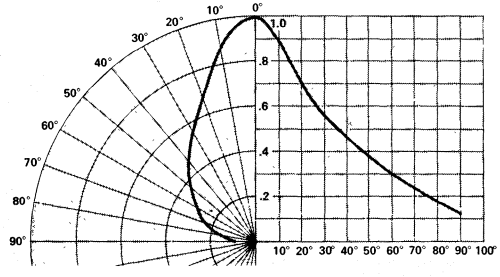


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

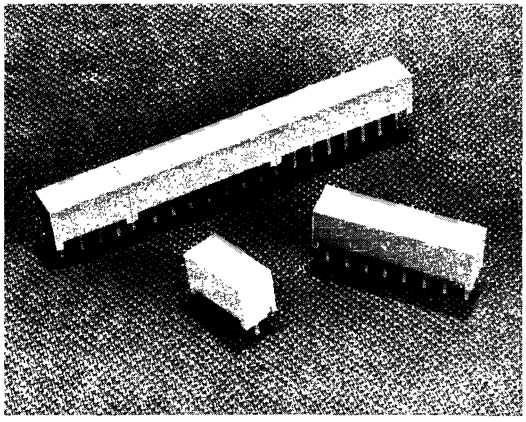
9 mm (0.35 INCH) AND 19 mm (0.75 INCH) LIGHT BAR MODULES

HIGH EFFICIENCY RED HLMP-2300 SERIES
YELLOW HLMP-2400 SERIES
GREEN HLMP-2500 SERIES

TECHNICAL DATA MARCH 1980

Features

- **LARGE, BRIGHT, UNIFORM LIGHT EMITTING SURFACE**
  Typical Luminous Stearance 260 cd/m² at 100mA Peak, 20mA Average
  Approximately Lambertian Radiation Pattern
- **SUITABLE FOR MULTIPLEX OPERATION**
  LED's in Either Parallel, Series or Parallel/ Series Connection
- **CHOICE OF THREE COLORS**
  High Efficiency Red
  Yellow
  Green
- **CATEGORIZED FOR LIGHT OUTPUT**
  Use of Like Chip Categories Yields a Uniform Display
- **EASILY MOUNTED ON P.C. BOARDS OR SOCKETS**
  Single In-Line Package, Leads on Industry Standard 2.54mm (0.1 in.) Centers
  I.C. Compatible
  Mechanically Rugged
- **X-Y STACKABLE**
- **FLUSH MOUNTABLE**
- **EASY ALIGNMENT**
- **EXCELLENT ON-OFF CONTRAST**



Applications

- **ILLUMINATED LEGENDS**
- **INDICATORS**
- **BAR GRAPHS**
- **LIGHTED SWITCHES**

Description

The HLMP-2300/-2400/-2500 series light bar modules are 9mm (.35 inch) and 19mm (.75 inch) rectangular light sources designed for a variety of applications where a large, bright source of light is required. The -2300 and -2400 series devices utilize LED chips which are made from GaAsP on a transparent GaP substrate. The-2500 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

Part No. HLMP-	Color	Size of Emitting Area	Package Drawing
2300	High Efficiency Red	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2350		19.05mm x 3.81mm (.750 in. x .150 in.)	B
2400	Yellow	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2450		19.05mm x 3.81mm (.750 in. x .150 in.)	B
2500	Green	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2550		19.05mm x 3.81mm (.750 in. x .150 in.)	B

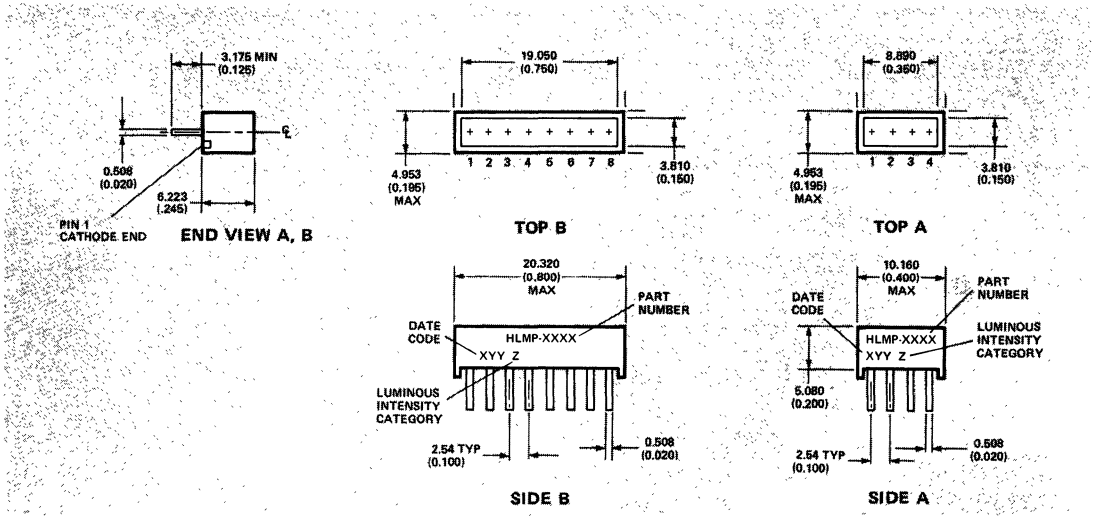
Absolute Maximum Ratings

Average Power Dissipation Per LED Chip (T_A=50°C) 90mW
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −40°C to +85°C
Peak Forward Current Per LED Chip (T_A=50°C)[2,3] 120mA
(Maximum Pulse Width = 1.25ms)
DC Forward Current Per LED Chip (T_A=50°C)[1,3] 30mA
Reverse Voltage Per LED Chip 6.0V
Lead Soldering Temperature [1.6mm (1/16 inch) below seating plane] ..... 260°C for 3 Seconds

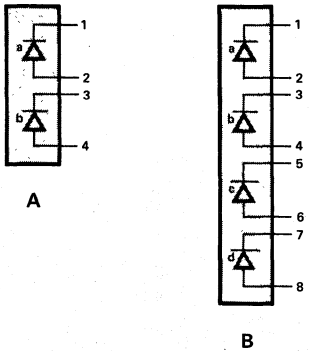
NOTES: 1. Derate maximum DC current above T_A=50°C at 0.51 mA/°C per LED chip, see Figure 2.
2. See Figure 1 to establish pulsed operating conditions.
3. For operation above T_A=50° C, see the allowed deratings for higher temperatures shown in Figure 2.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

Package Dimensions



Internal Circuit Diagram



PIN	FUNCTION A -2300/-2400 -2500	FUNCTION B -2350/-2450 -2550
1	Cathode — a	Cathode — a
2	Anode — a	Anode — a
3	Cathode — b	Cathode — b
4	Anode — b	Anode — b
5		Cathode — c
6		Anode — c
7		Cathode — d
8		Anode — d

NOTES: 1. Dimensions in millimetres and (inches).
2. Tolerances ±.25 mm unless otherwise indicated.

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED HLMP-2300/-2350

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2300	I_V	100mA Pk: 1 of 5 Duty Factor		10		mcd
			20mA DC	3	7		mcd
	-2350	I_V	100mA Pk: 1 of 5 Duty Factor		21		mcd
			20mA DC	7	15		mcd
Peak Wavelength		λpeak			635		nm
Dominant Wavelength[5]		λ_d			626		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.5	3.5	V
			I_F= 20mA		1.9	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		$\Delta V_F/°C$	I_F=100mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$			150		°C/W/ LED

YELLOW HLMP-2400/-2450

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2400	I_V	100mA Pk: 1 of 5 Duty Factor		8		mcd
			20mA DC	2	5		mcd
	-2450	I_V	100mA Pk: 1 of 5 Duty Factor		18		mcd
			20mA DC	5	11		mcd
Peak Wavelength		λpeak			583		nm
Dominant Wavelength[5]		λ_d			585		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.6	3.5	V
			I_F= 20mA		2.0	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		$\Delta V_F/°C$	I_F=100mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$			150		°C/W/ LED

GREEN HLMP-2500/-2550

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2500	I_V	100mA Pk: 1 of 5 Duty Factor		6		mcd
			20mA DC	1.5	3.5		mcd
	-2550	I_V	100mA Pk: 1 of 5 Duty Factor		13		mcd
			20mA DC	3.5	7.5		mcd
Peak Wavelength		λpeak			565		nm
Dominant Wavelength[5]		λ_d			572		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.7	3.6	V
			I_F= 20mA		2.1	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		$\Delta V_F/°C$	I_F=100mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$			150		°C/W/ LED

NOTES: 4. Each device is categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
5. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.

Electrical

The HLMP-2300/-2400/-2500 series of light bar devices are composed of two or four light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface. The LED's have a large area P-N junction diffused into the epitaxial layer on a GaP transparent substrate.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows for the wiring of the LED's within a device in any of three possible configurations: parallel, series, or series/parallel.

These light bar devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$V_F = 2.2V + I_{PEAK}\ (13\Omega)$ For $I_{PEAK} \geq 30mA$

$V_F = 1.9V + I_{DC}\ (23.3\Omega)$ For $10mA \leq I_{DC} < 30mA$

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V(cd/m^2) = \frac{I_V(cd)}{A(m^2)}$$

$$L_V(footlamberts) = \frac{\pi I_V(cd)}{A(ft^2)}$$

SIZE OF EMITTING SURFACE	AREA	
	SQ. METRES	SQ. FEET
8.89mm x 3.81mm	33.87×10^{-6}	364.58×10^{-6}
19.05mm x 3.81mm	72.58×10^{-6}	781.25×10^{-6}

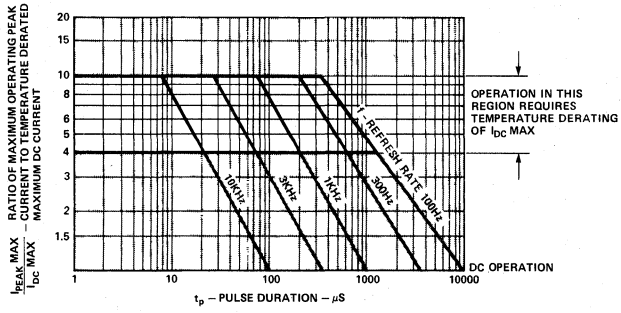


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration

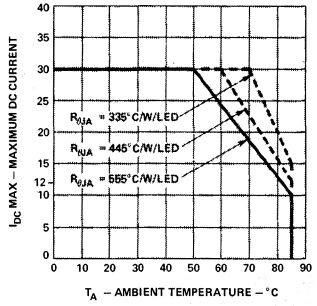


Figure 2. Maximum Allowable DC Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED Basis. T_JMAX=100°C.

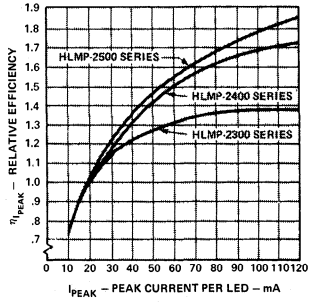


Figure 3. Relative Efficiency Luminous Intensity per Unit Current) vs. Peak LED Current.

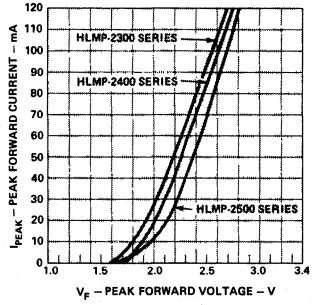


Figure 4. Peak Forward Current per LED vs. Peak Forward Voltage.

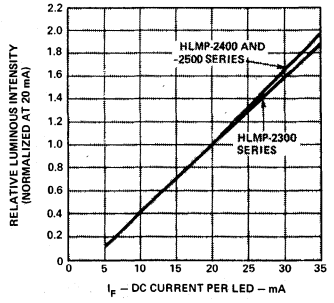


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

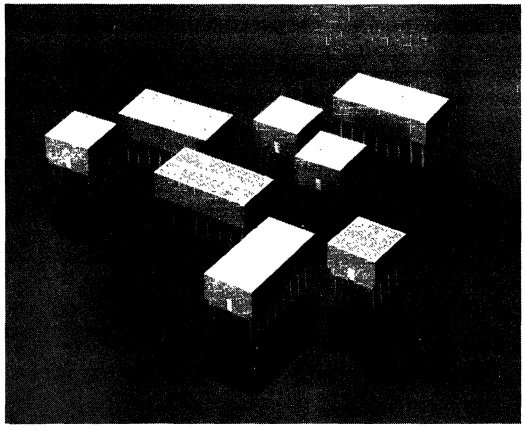
HEWLETT PACKARD

LED LIGHT BAR MODULES
SINGLE, TWIN, & QUAD ARRANGEMENTS
HIGH EFFICIENCY RED -HLMP-2600 SERIES
YELLOW -HLMP-2700 SERIES
GREEN -HLMP-2800 SERIES

TECHNICAL DATA MARCH 1980

Features

- **LARGE, BRIGHT, UNIFORM LIGHT EMITTING SURFACE**
  - **Typical Luminous Sterance 160 cd/m² at 60 mA Peak, 20 mA Average**
  - **Approximately Lambertian Radiation Pattern**
- **SUITABLE FOR MULTIPLEX OPERATION**
  - **LED's in Either Parallel, Series or Parallel/Series Connection**
- **CHOICE OF THREE COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **CATEGORIZED FOR LIGHT OUTPUT**
  - **Use of Like Chip Categories Yields a Uniform Display**
- **EASILY MOUNTED ON P.C. BOARDS OR SOCKETS**
  - **Industry Standard 7.62 mm (0.3 in.) DIP Leads on 2.54 mm (0.100 in.) Centers**
  - **I.C. Compatible**
  - **Mechanically Rugged**
- **X — Y Stackable**
- **FLUSH MOUNTABLE**
- **EASY ALIGNMENT**
- **EXCELLENT ON-OFF CONTRAST**



Applications

- **ANNUNCIATORS WITH ILLUMINATED LEGENDS**
- **BACKLIGHTED FRONT PANELS**
- **FRONT PANEL INDICATORS**
- **BAR GRAPHS**
- **LIGHTED SWITCHES**
- **EDGE LIGHT PANELS**

SOLID STATE LAMPS

Description

The HLMP-2600/-2700/-2800 series light bar modules are rectangular light sources designed for a variety of applications where a large, bright source of light is required. These modules are configured in packages that contain either a single, twin or quad light emitting surface arrangement. The -2600 and -2700 series devices utilize LED chips which are made from GaAsP on a transparent GaP substrate. The -2800 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

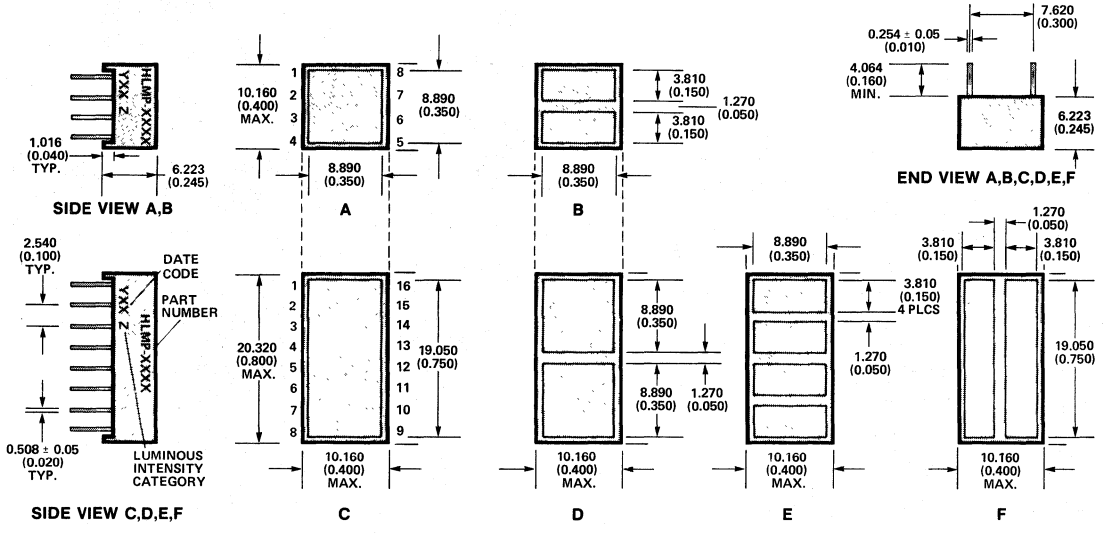
Part Number HLMP-			Size of Light Emitting Areas	Number of Light Emitting Areas	Package Outline	
High Efficiency Red	Yellow	Green				
2655	2755	2855	8.89 mm x 8.89 mm (.350 in. x .350 in.)	1	A	
2600	2700	2800	8.89 mm x 3.81 mm (.350 in. x .150 in.)	2	B	
2685	2785	2885	8.89 mm x 19.05 mm (.350 in. x .750 in.)	1	C	
2670	2770	2870	8.89 mm x 8.89 mm (.350 in. x .350 in.)	2	D	
2620	2720	2820	8.89 mm x 3.81 mm (.350 in. x .150 in.)	4	E	
2635	2735	2835	3.81 mm x 19.05 mm (.150 in. x .750 in.)	2	F	

Absolute Maximum Ratings

Average Power Dissipation Per LED Chip (T_A = 50°C) 93mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per LED Chip (T_A = 50°C)[3,5] ..... 60 mA
(Maximum Pulse Width = 2.0 ms)
Time Average Forward Current Per LED Chip
Pulsed Conditions[4] ..... 20 mA
DC Forward Current Per LED Chip (HLMP-2700 Series)
(T_A = 50°C)[2] ..... 25 mA
DC Forward Current Per LED Chip (HLMP-2600/-2800
Series) (T_A = 50°C)[1] ..... 30 mA
Reverse Voltage Per LED Chip 6.0V
Lead Soldering Temperature [1.6 mm (1/16 inch) below
seating plane] ..... 260°C for 3 seconds

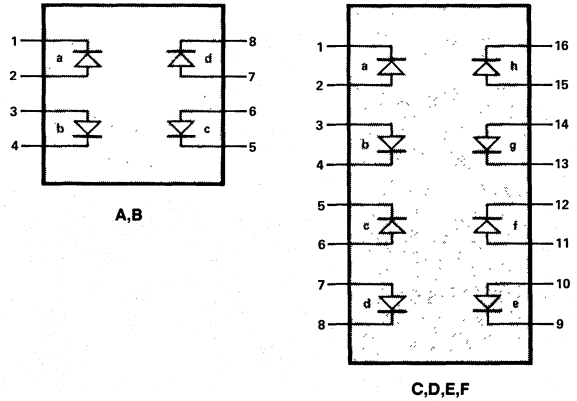
NOTES:
1. Derate maximum DC current above T_A = 50°C at 0.57 mA/°C per LED chip, see Figure 2.
2. Derate maximum DC current above 58°C at 0.56 mA/°C per LED chip, see Figure 2.
3. See Figure 1 to establish pulsed operating conditions.
4. Derate maximum I_{AVG} current above T_A = 50°C at 0.40 mA average/°C per LED chip, see Figure 2.
5. For operation above T_A = 50°C, see the allowed deratings for higher temperatures shown in Figures 2 and 3.

Package Dimensions



NOTES: OUTSIDE WALL THICKNESS 0.508 (0.020) TYPICAL ALL PACKAGES.
DIMENSIONS IN INCHES AND (MILLIMETRES).

Internal Circuit Diagrams



Pin Function

PIN	FUNCTION	
	A, B	C, D, E, F
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	ANODE b	ANODE b
4	CATHODE b	CATHODE b
5	CATHODE c	CATHODE c
6	ANODE c	ANODE c
7	ANODE d	ANODE d
8	CATHODE d	CATHODE d
9		CATHODE e
10		ANODE e
11		ANODE f
12		CATHODE f
13		CATHODE g
14		ANODE g
15		ANODE h
16		CATHODE h

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED HLMP-2600 SERIES

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[6] Per Light Emitting Surface Area	-2655	I_V		16		mcd	60 mA Pk: 1 of 3 Duty Factor
			6	14		mcd	20 mA DC
	-2600	I_V		8		mcd	60 mA Pk: 1 of 3 Duty Factor
			3	7		mcd	20 mA DC
	-2685	I_V		32		mcd	60 mA Pk: 1 of 3 Duty Factor
			12	28		mcd	20 mA DC
	-2670	I_V		16		mcd	60 mA Pk: 1 of 3 Duty Factor
			6	14		mcd	20 mA DC
	-2620	I_V		8		mcd	60 mA Pk: 1 of 3 Duty Factor
			3	7		mcd	20 mA DC
	-2635	I_V		16		mcd	60 mA Pk: 1 of 3 Duty Factor
			6	14		mcd	20 mA DC
Peak Wavelength		λ_{peak}		635		nm	
Dominant Wavelength[7]		λ_d		626		nm	
Forward Voltage Per LED		V_F		2.1	2.6	V	I_F = 20 mA
Reverse Current Per LED		I_R		10		μA	V_R = 6V
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

YELLOW HLMP-2700 SERIES

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[6] Per Light Emitting Surface Area	-2755	I_V		12		mcd	60 mA Pk: 1 of 3 Duty Factor
			5.4	10		mcd	20 mA DC
	-2700	I_V		6		mcd	60 mA Pk: 1 of 3 Duty Factor
			2.7	5		mcd	20 mA DC
	-2785	I_V		24		mcd	60 mA Pk: 1 of 3 Duty Factor
			10.8	20		mcd	20 mA DC
	-2770	I_V		12		mcd	60 mA Pk: 1 of 3 Duty Factor
			5.4	10		mcd	20 mA DC
	-2720	I_V		6		mcd	60 mA Pk: 1 of 3 Duty Factor
			2.7	5		mcd	20 mA DC
	-2735	I_V		12		mcd	60 mA Pk: 1 of 3 Duty Factor
			5.4	10		mcd	20 mA DC
Peak Wavelength		λ_{peak}		583		nm	
Dominant Wavelength[7]		λ_d		585		nm	
Forward Voltage Per LED		V_F		2.2	2.6	V	I_F = 20 mA
Reverse Current Per LED		I_R		10		μA	V_R = 6V
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

Electrical/Optical Characteristics at T_A=25°C

GREEN HLMP-2800 SERIES

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[6] Per Light Emitting Surface Area	-2855	I_V		10		mcd	60 mA Pk: 1 of 3 Duty Factor
			5	7		mcd	20 mA DC
	-2800	I_V		5		mcd	60 mA Pk: 1 of 3 Duty Factor
			2.5	3.5		mcd	20 mA DC
	-2885	I_V		20		mcd	60 mA Pk: 1 of 3 Duty Factor
			10	14		mcd	20 mA DC
	-2870	I_V		10		mcd	60 mA Pk: 1 of 3 Duty Factor
			5	7		mcd	20 mA DC
	-2820	I_V		5		mcd	60 mA Pk: 1 of 3 Duty Factor
			2.5	3.5		mcd	20 mA DC
	-2835	I_V		10		mcd	60 mA Pk: 1 of 3 Duty Factor
			5	7		mcd	20 mA DC
Peak Wavelength		λ_{peak}		565		nm	
Dominant Wavelength[7]		λ_d		572		nm	
Forward Voltage Per LED		V_F		2.2	2.6	V	I_F = 20 mA
Reverse Current Per LED		I_R		10		μA	V_R = 6V
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

Notes:
6. These devices are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
7. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.

Electrical

The HLMP-2600/-2700/-2800 series of light bar devices are composed of four or eight light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface. The LED's have a P-N junction diffused into the epitaxial layer on a GaP transparent substrate.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows for the wiring of the LED's within a device in any of three possible configurations: parallel, series, or series/parallel.

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}\ (40\Omega)$$
For $I_{PEAK} \geq 20mA$
$$V_F = 1.6V + I_{DC}\ (50\Omega)$$
For $5mA \leq I_{DC} \leq 20mA$

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\ (cd/m^2) = \frac{I_V\ (cd)}{A\ (m^2)}$$

$$L_V\ (footlamberts) = \frac{\pi I_V\ (cd)}{A\ (ft^2)}$$

Size of Light Emitting Surface Area	Area	
	Sq. Metres	Sq. Feet
8.89 mm x 8.89 mm	67.74×10^{-6}	729.16×10^{-6}
8.89 mm x 3.81 mm	33.87×10^{-6}	364.58×10^{-6}
8.89 mm x 19.05 mm	135.48×10^{-6}	1458.32×10^{-6}
3.81 mm x 19.05 mm	72.58×10^{-6}	781.25×10^{-6}

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, $\eta_{I_{PEAK}}$, and adjusted for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right] (\eta_{I_{PEAK}}) (I_V \text{ Data Sheet})$$

Example: For HLMP-2735 series

$$\eta_{I_{PEAK}} = 1.18 \text{ at } I_{PEAK} = 48 \text{ mA}$$

$$I_{V\ TIME\ AVG} = \left[\frac{12mA}{20mA}\right] (1.18)\ (10 \text{ mcd}) = 7 \text{ mcd}$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V\ (T_A) = I_V\ (25°C)\ e^{[K\ (T_A - 25°C)]}$$

Device	K
-2600 Series	-0.0131/°C
-2700 Series	-0.0112/°C
-2800 Series	-0.0104/°C

Example: $I_V\ (80°C) = (7 \text{ mcd})\ e^{[-0.0112\ (80-25)]} = 3.8\text{mcd}$

Mechanical

These devices are constructed utilizing a lead frame in a DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, $T_{J\ MAX}$, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 250°C/W/LED. This will then establish a maximum thermal resistance LED junction-to-ambient of 400°C/W/LED.

These light bar devices may be operated in ambient temperatures above +60°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 250°C/W/LED. See Figure 6 to determine the maximum allowed thermal resistance for the PC board, $R\theta_{PC-A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

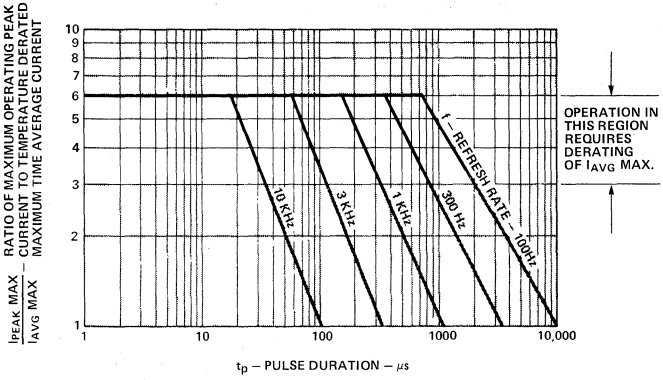


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

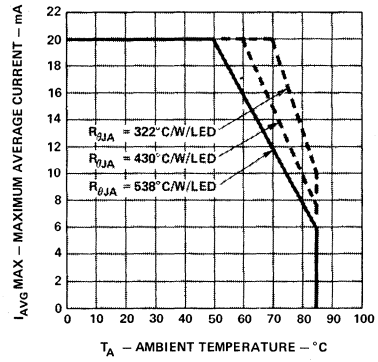


Figure 2. Maximum Allowable Average Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a Per LED Basis. T_J MAX = 100°C.

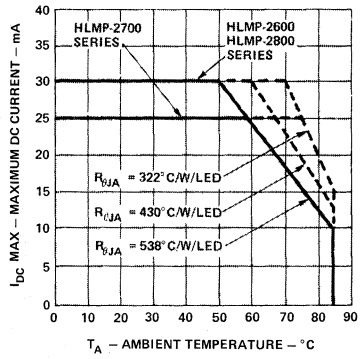


Figure 3. Maximum Allowable DC Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a Per LED Basis. T_J MAX = 100°C.

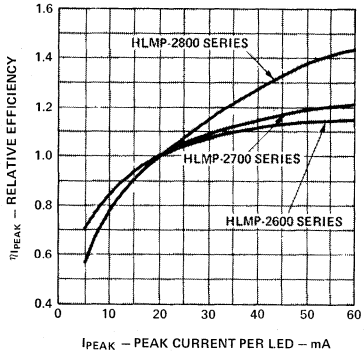


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

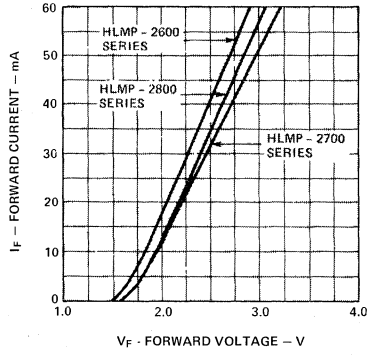


Figure 5. Forward Current vs. Forward Voltage Characteristics.

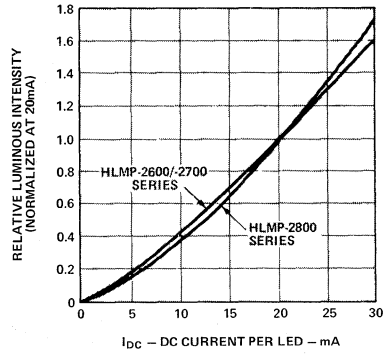


Figure 6. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

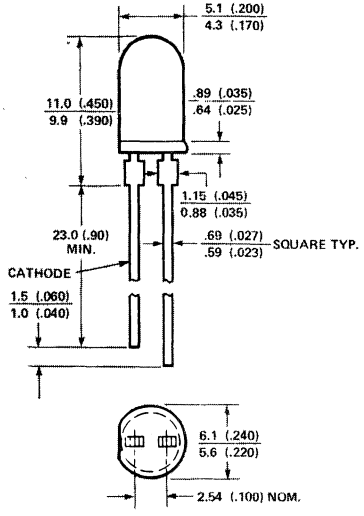
HEWLETT PACKARD

COMMERCIAL LIGHT EMITTING DIODES

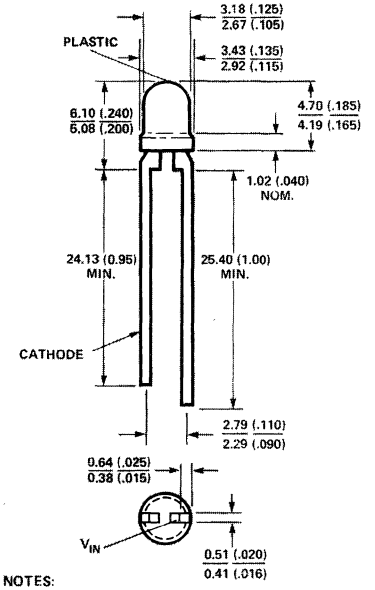
5082-4850
5082-4855
5082-4484
5082-4494

TECHNICAL DATA MARCH 1980

5082-4850/4855



5082-4484/4494



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Features

- **LOW COST: BROAD APPLICATION**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **LOW POWER REQUIREMENTS: 20mA @ 1.6V**
- **HIGH LIGHT OUTPUT**
  0.8 mcd TYPICAL FOR 5082-4850/4484
  1.4 mcd TYPICAL FOR 5082-4855/4494
- **WIDE VIEWING ANGLE**
- **RED DIFFUSED LENS**

Description

The 5082-4850/4855 and 5082-4484/4494 are Gallium Arsenide Phosphide Light Emitting Diodes intended for **High Volume/Low Cost** applications such as indicators for appliances, automobile instrument panels and many other commercial uses.

The 5082-4850/4855 are T-1¾ lamp size, have red diffused lenses and can be panel mounted using mounting clip 5082-4707.

The 5082-4484/4494 are T-1 lamp size, have red diffused lenses and are ideal where space is at a premium, such as high density arrays.

Absolute Maximum Ratings at T_A=25°C

Power Dissipation 100mW

DC Forward Current (Derate linearly from 50°C at 0.2mA/°C) 50mA

Peak Forward Current 1Amp
(1μsec pulse width, 300pps)

Operating and Storage Temperature Range ..... -55°C to +100°C

Lead Soldering Temperature ..... 230°C for 7 sec.

SOLID STATE LAMPS

Electrical Characteristics at T_A=25°C

Symbol	Parameters	5082-4850			5082-4855			5082-4484			5082-4494			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity		0.8		0.8	1.4			0.8		0.8	1.4		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655			655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10			10			10		ns	
C	Capacitance		100			100			100			100		pF	V_F = 0, f = 1MHz
V_F	Forward Voltage		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		3	10		3	10		V	I_R = 100μA
θ_{JC}	Thermal Resistance		100			100			100			100		°C/W	Junction to Cathode Lead

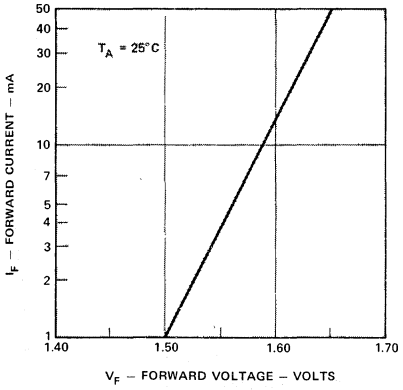


Figure 1. Forward Current Versus Forward Voltage Characteristic For 5082-4850/4855/4484/4494.

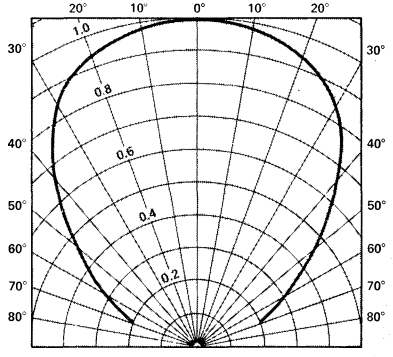


Figure 2. Relative Luminous Intensity Versus Angular Displacement For 5082-4850/4855.

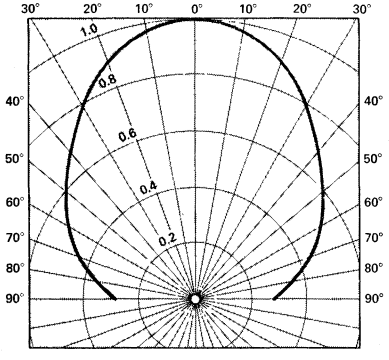


Figure 3. Relative Luminous Intensity Versus Angular Displacement For 5082-4484/4494.

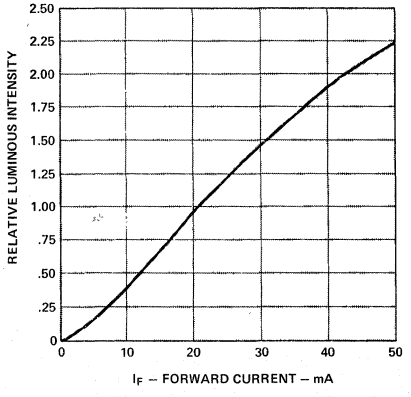


Figure 4. Relative Luminous Intensity Versus Forward Current For 5082-4850/4855/4484/4494.

HEWLETT PACKARD

SOLID STATE LAMPS

5082-4403
5082-4415
5082-4440
5082-4444
5082-4880 SERIES

TECHNICAL DATA MARCH 1980

Features

- **EASILY PANEL MOUNTABLE**
- **HIGH BRIGHTNESS OVER A WIDE VIEWING ANGLE**
- **RUGGED CONSTRUCTION FOR EASE OF HANDLING**
- **STURDY LEADS ON 2.54mm (0.10 in.) CENTERS**
- **IC COMPATIBLE/LOW POWER CONSUMPTION**
- **LONG LIFE**

Description

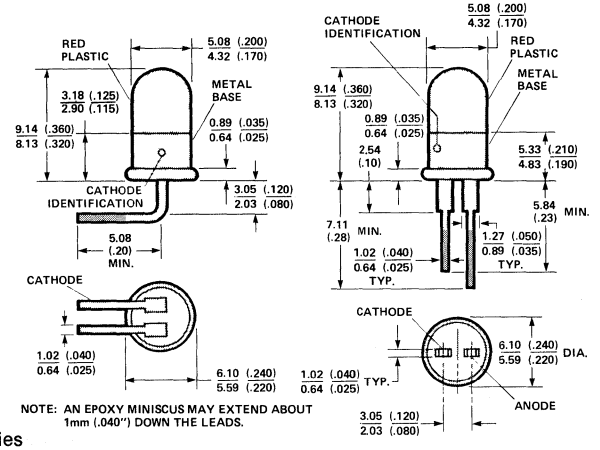
The 5082-4403, -4415, -4440, -4444 and the -4880 series are plastic encapsulated Gallium Arsenide Phosphide Light Emitting Diodes. They radiate light in the 655 nanometer (red light) region.

The 5082-4403 and -4440 are LEDs with a red diffused plastic lens, providing high visibility for circuit board or panel mounting with a clip.

The 5082-4415 and -4444 have the added feature of a 90° lead bend for edge mounting on circuit boards.

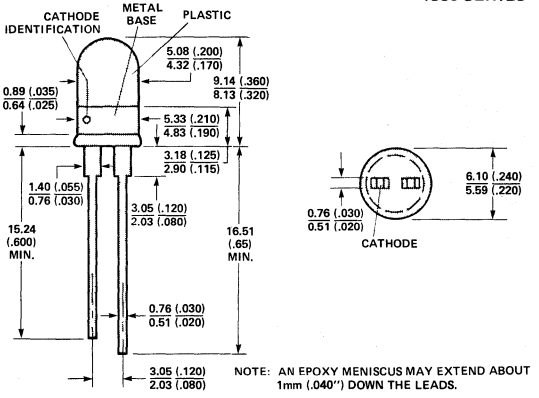
The 5082-4880 series is available in three different lens configurations. These are Red Diffused, Clear Diffused, and Clear Non-Diffused.

The Red Diffused lens provides an excellent off/on contrast ratio. The Clear Non-Diffused lens is designed for applications where a point source is desired. It is particularly useful where the light must be focused or diffused with external optics. The Clear Diffused lens is useful in masking the red color in the off condition.



DIMENSIONS IN MILLIMETRES AND (INCHES).

-4880 SERIES



LED SELECTION GUIDE

MINIMUM LIGHT OUTPUT (mcd)	LONG LEAD (UNBENT)		
	Red Diffused Lens	Clear Non-Diffused Lens	Clear Diffused Lens
0.5	5082-4880	5082-4883	5082-4886
1.0	5082-4881	5082-4884	5082-4887
1.6	5082-4882	5082-4885	5082-4888
	SHORT LEAD		
0.3	5082-4440	UNBENT	
0.8	5082-4403		
0.3	5082-4444	BENT	
0.8	5082-4415		

Maximum Ratings at T_A=25°C

DC Power Dissipation ..... 100 mW
DC Forward Current ..... 50 mA
(Derate linearly from 50°C at 0.2mA/°C)
Peak Transient Forward Current ..... 1 Amp
(1μsec pulse width, 300 pps)
Isolation Voltage (between lead and base) ..... 300 V
Operating and Storage
Temperature Range .....-55°C to +100°C
Lead Soldering Temperature ..... 230°C for 7 sec

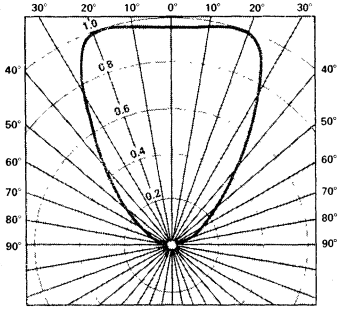
SOLID STATE LAMPS

Electrical Characteristics at $T_A = 25°C$

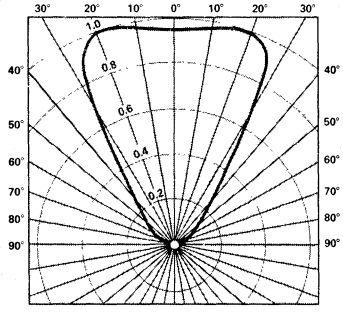
Symbol	Parameter	5082-4403 5082-4415			5082-4440 5082-4444			5082-4880 5082-4883 5082-4886			5082-4881 5082-4884 5082-4887			5082-4882 5082-4885 5082-4888			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity	0.8	1.2		0.3	0.7		0.5	0.8		1.0	1.3		1.6	1.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655			655			655			655		nm	Measurement at Peak
τ_S	Speed of Response		15			15			15			15			15		ns	
C	Capacitance		100			100			100			100			100		pF	
θ_{JC}	Thermal Resistance		87			87			100			100			100		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		3	10		3	10		3	10		V	I_R = 100μA

TYPICAL RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT

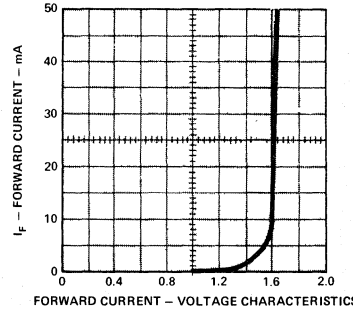
44XX



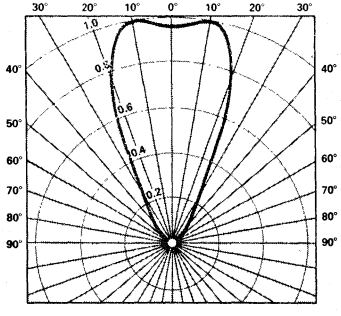
4880, 4881, 4882



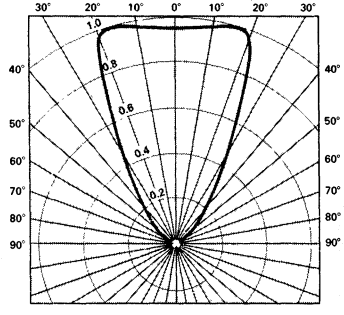
FORWARD CURRENT VS. VOLTAGE CHARACTERISTICS



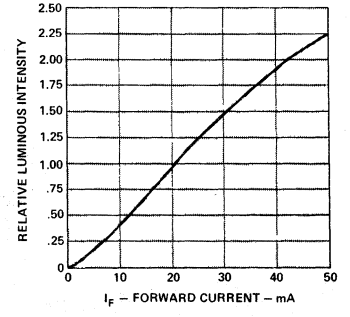
4883, 4884, 4885



4886, 4887, 4888



LUMINOUS INTENSITY VS. FORWARD CURRENT (I_F)



HEWLETT PACKARD

SOLID STATE LAMPS

5082-4480 SERIES

TECHNICAL DATA MARCH 1980

Features

- **HIGH INTENSITY: 0.8mcd TYPICAL**
- **WIDE VIEWING ANGLE**
- **SMALL SIZE T-1 DIAMETER 3.18mm (0.125")**
- **IC COMPATIBLE**
- **RELIABLE AND RUGGED**

Description

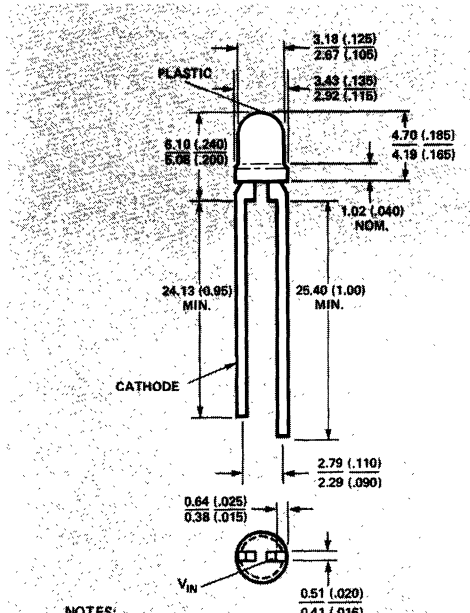
The 5082-4480 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The 5082-4480 series is available in three lens configurations.

5082-4480 — Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

5082-4483 — Same as 5082-4480, but Clear Diffused to mask red color in the "off" condition.

5082-4486 — Clear Non-Diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

PART NO.	LENS CONFIGURATION
5082-4480	Red Diffused
5082-4483	Untinted Diffused
5082-4486	Clear Plastic

Maximum Ratings at T_A=25°C

DC Power Dissipation 100mW

DC Forward Current 50mA
(Derate linearly from 50°C at 0.2mA/°C)

Peak Forward Current . . . . . 1 Amp
(1 μsec pulse width, 300 pps)

Operating and Storage Temperature Range . . . . . −55°C to +100°C

Lead Soldering Temperature . . . . . 230°C for 7 sec.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	5082-4480 5082-4483 5082-4486			Units	Test Conditions
		Min.	Typ.	Max.		
I_V	Luminous Intensity	0.3	0.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
C	Capacitance		100		pF	V_F = 0, f = 1MHz
θ_{JC}	Thermal Resistance		270		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		V	I_R = 10μA

SOLID STATE LAMPS

5082-4480 AND 5082-4483

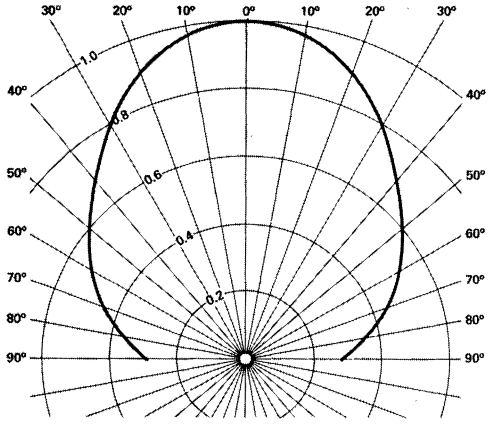


Figure 1. Relative Luminous Intensity vs. Angular Displacement.

5082-4486

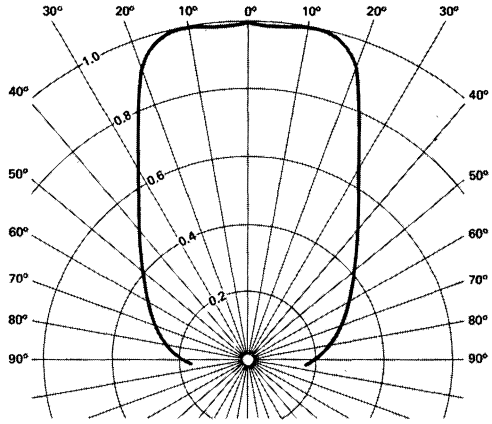


Figure 2. Relative Luminous Intensity vs. Angular Displacement.

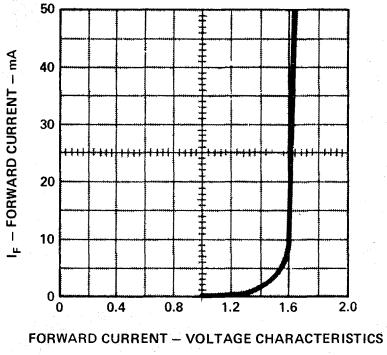


Figure 3. Forward Current vs. Voltage Characteristic.

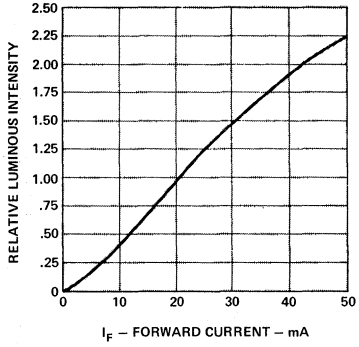


Figure 4. Luminous Intensity vs. Forward Current (I_F).

HEWLETT PACKARD

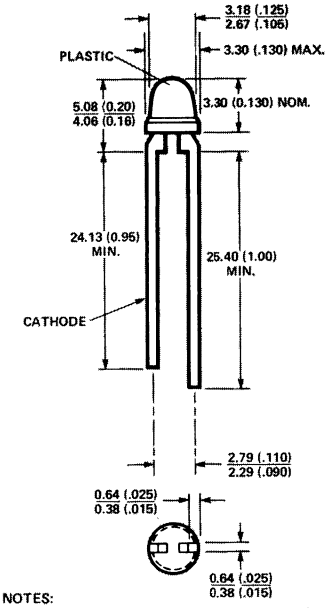
LOW PROFILE SOLID STATE LAMPS

5082-4487
5082-4488

TECHNICAL DATA MARCH 1980

Features

- **LOW COST: BROAD APPLICATION**
- **LOW PROFILE: 4.57mm (0.18") LENS HEIGHT TYPICAL**
- **HIGH DENSITY PACKAGING**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **LOW POWER REQUIREMENTS: 20mA @ 1.6V**
- **HIGH LIGHT OUTPUT: 0.8mcd TYPICAL**



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

The 5082-4487 and 5082-4488 are Gallium Arsenide Phosphide Light Emitting Diodes for High Volume/Low Cost Applications such as indicators for calculators, cameras, appliances, automobile instrument panels, and many other commercial uses.

The 5082-4487 is an untinted non-diffused, low profile T-1 LED lamp, and has a typical light output of 0.8 mcd at 20 mA.

The 5082-4488 is an untinted non-diffused, low profile T-1 LED lamp, and has a guaranteed minimum light output of 0.3 mcd at 20 mA.

Absolute Maximum Ratings at T_A=25°C

DC Power Dissipation	100mW
DC Forward Current [Derate linearly from 50°C at 0.2mA/°C]	50mW
Peak Forward Current [1μsec pulse width, 300pps]	1 Amp
Operating and Storage Temperature Range	−55°C to +100°C
Lead Soldering Temperature	230°C for 7 sec.

SOLID STATE LAMPS

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameters	5082-4487			5082-4488			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity		0.8		0.3	0.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10		ns	
C	Capacitance		100			100		pF	V_F = 0, f = 1MHz
V_F	Forward Voltage		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		V	I_R = 100μA

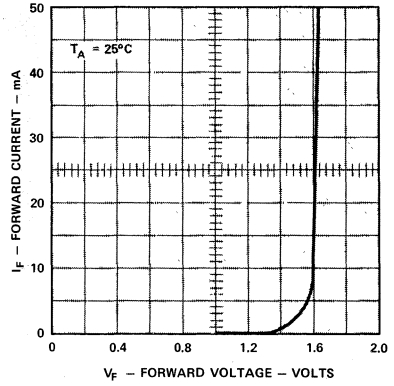


Figure 1. Typical Forward Current Versus Voltage Characteristic.

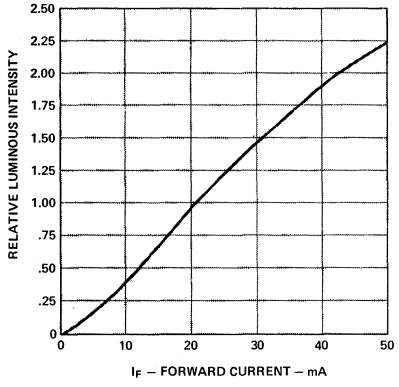


Figure 2. Typical Luminous Intensity Versus Forward Current.

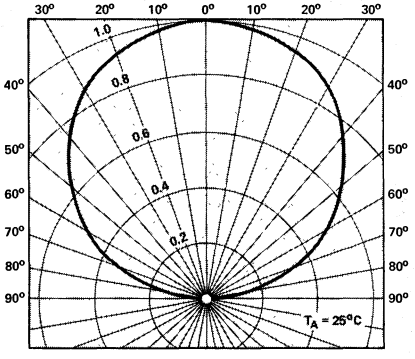


Figure 3. Typical Relative Luminous Intensity Versus Angular Displacement.

HEWLETT PACKARD

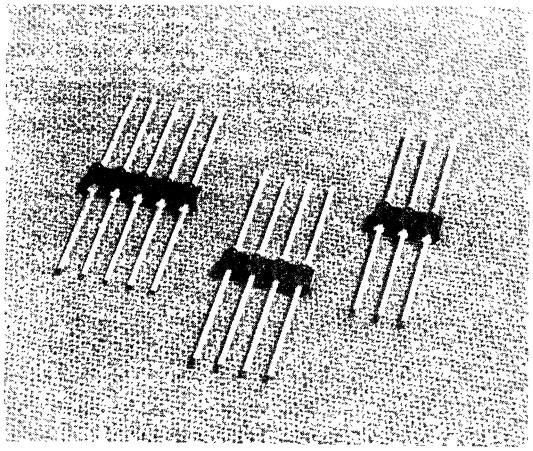
MATCHED ARRAYS OF SUBMINIATURE RED SOLID STATE LAMPS

3 - ELEMENT • HLMP - 6203
4 - ELEMENT • HLMP - 6204
5 - ELEMENT • HLMP - 6205

TECHNICAL DATA MARCH 1980

Features

- **EXCELLENT UNIFORMITY BETWEEN ELEMENTS AND BETWEEN ARRAYS**
- **EASY INSERTION AND ALIGNMENT**
- **VERSATILE LENGTHS — 3,4,5 ELEMENTS**
- **END STACKABLE FOR LONGER ARRAYS**
- **COMPACT SUBMINIATURE PACKAGE STYLE**
- **NO CROSSTALK BETWEEN ELEMENTS**



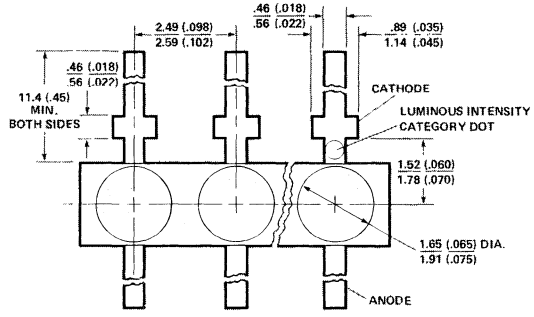
Description

The HLMP-62XX Series arrays are comprised of several Gallium Arsenide Phosphide Red Solid State Lamps molded as a single bar. Arrays are tested to assure uniformity between elements and matching between arrays. Each element has separately accessible leads and a red diffused lens which provides a wide viewing angle and a high on/off contrast ratio. Center-to-center spacing is 2.54mm (.100 in.) between elements and arrays are end stackable on 2.54mm (.100 in.) centers.

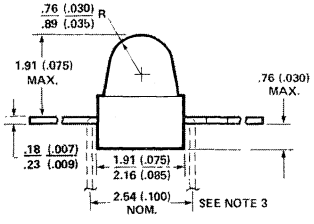
Absolute Maximum Ratings/Element at $T_A = 25°C$

Power Dissipation ..... 100 mW
Average Forward Current (Derate linearly from 50°C at 0.2mA/°/C) ..... 50 mA
Peak Forward Current (see Figure 4) ..... 1000 mA
Operating and Storage Temperature Range ..... -55°C to +100°C
Lead Soldering Temperature [1.6 mm (0.063 in.) from body] ..... 245°C for 3 sec.

Package Dimensions



Notes:
1. All dimensions are in millimetres (inches).
2. Silver-plated leads. See Application Bulletin 3.
3. User may bend leads as shown.
4. Overall length is the number of elements times 2.54mm (.100 in.).



SOLID STATE LAMPS

Electrical Specifications/Element at T_A=25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Figure
I_V	Axial Luminous Intensity	.5	1.0		mcd	I_F = 10 mA; Note 1	2
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		45		Deg.	Note 2	5
λ_{PEAK}	Peak Wavelength		655		nm	Measurement @ Peak	
λ_d	Dominant Wavelength		640		nm	Note 3	
τ_s	Speed of Response		15		ns		
C	Capacitance		100		pF	V_F = 0; f = 1 MHz	
θ_{JC}	Thermal Resistance		125		°C/W	Junction to Cathode Lead at .79mm(.031in)from the body	
V_F	Forward Voltage		1.6	2.0	V	I_F = 10 mA	1
BV_R	Reverse Breakdown Voltage	3	10		V	I_R = 100 μA	
η_V	Luminous Efficacy		55		lm/W	Note 4	

Notes:
1. Arrays categorized for luminous intensity.
2. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
3. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

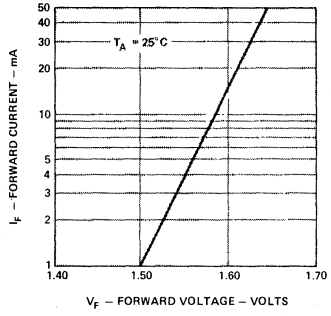


Figure 1. Forward Current vs. Forward Voltage.

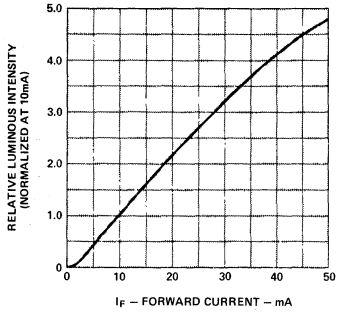


Figure 2. Relative Luminous Intensity vs. DC Forward Current.

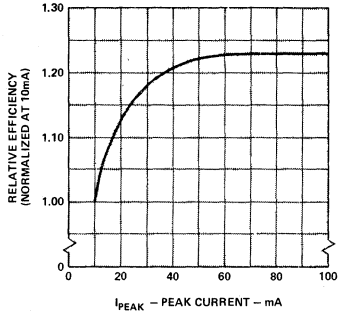


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

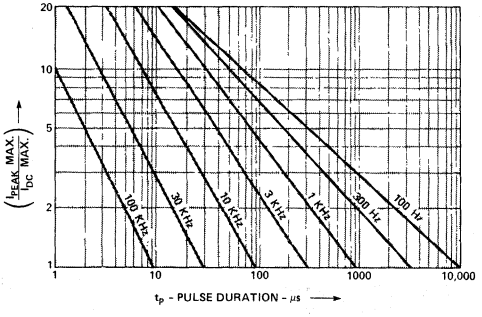


Figure 4. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

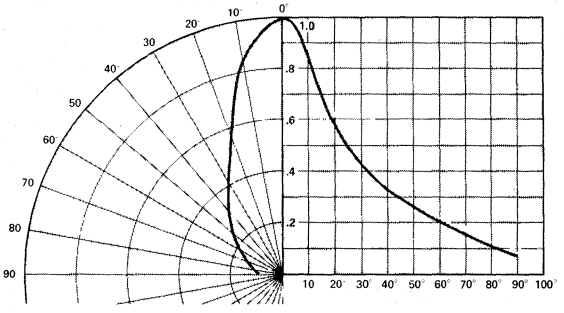


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

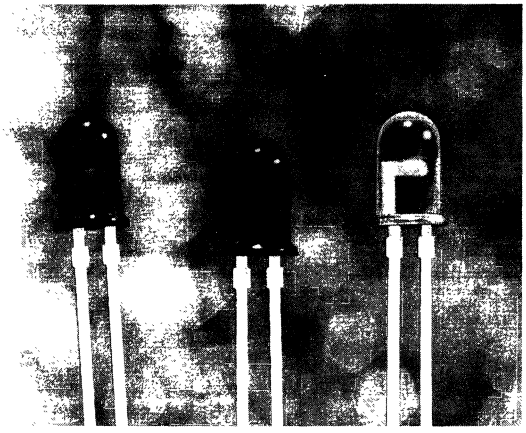
5 VOLT LED RESISTOR LAMPS

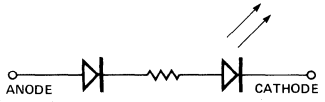
HIGH EFFICIENCY RED • HLMP-3600
YELLOW • HLMP-3650
GREEN • HLMP-3680

TECHNICAL DATA MARCH 1980

Features

- **INTEGRAL CURRENT LIMITING RESISTOR**
- **INTEGRAL REVERSE PROTECTION DIODE**
- **TTL COMPATIBLE: REQUIRES NO EXTERNAL CURRENT LIMITER WITH 5 VOLT SUPPLY**
- **COST EFFECTIVE: SPACE SAVING**
- **PANEL MOUNTABLE T-1¾ PACKAGE**
- **WIRE WRAPPABLE LEADS**
- **WIDE VIEWING ANGLE**





Description

The HLMP-3600 series lamps contain an integral current limiting resistor and reverse current protection diode in series with the LED. This allows the lamp to be driven from a 5 volt source without the need for an external current limiter. The -3600 and -3650 lamps utilize LED chips which are made from GaAsP on a transparent GaP substrate. The -3680 lamp utilizes an LED chip made from GaP on a transparent GaP substrate. These T-1¾ lamps are diffused to provide wide off-axis viewing and may be front panel mounted using the 5082-4707 clip and ring. The leads are wire wrappable.

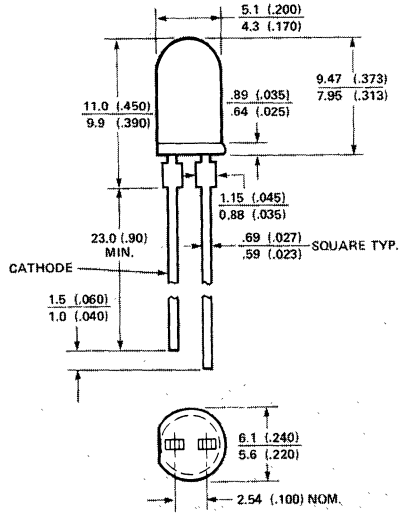
Absolute Maximum Ratings

(T_A = 25°C unless otherwise specified)

DC Forward Voltage (T_A = 25°C)[1]	7.5V
Reverse Voltage	20V
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-40°C to 85°C
Lead Soldering Temperature [1.6 mm (0.063 inch) from body]	260°C for 5 sec.

Notes:
1. Derate from T_A = 50°C at 0.071V/°C. See Figure 3.

Package Dimensions



DIMENSIONS IN MILLIMETRES (INCHES).

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity[4]	3600 3650 3680	1.0 1.0 0.8	2.4 2.4 1.8		mcd	V_F = 5 Volts
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	All		90			Note 1 (See Figure 4)
λ_{Peak}	Peak Wavelength	3600 3650 3680		635 585 565		nm	Measurement at Peak
λ_d	Dominant Wavelength	3600 3650 3680		626 585 572		nm	Note 2
$R\theta_{J-PIN}$	Thermal Resistance	All		90		°C/W	Junction to Lead at 3 mm from Body
I_F	Forward Current	3600 3650 3680		10 10 12	15 15 15	mA	V_F = 5 Volts
I_R	Reverse Current	All			10	μA	V_R = 12 Volts
η_V	Luminous Efficacy	3600 3650 3680		147 570 665		m/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.
4. The luminous intensity may be adjusted for operating ambient temperature by the following exponential equation: $I_V(T_A) = I_V(25°C)\, e^{[k(T_A - 25°C)]}$

Device	k
-3600	-0.0131/°C
-3650	-0.0112/°C
-3680	-0.0104/°C

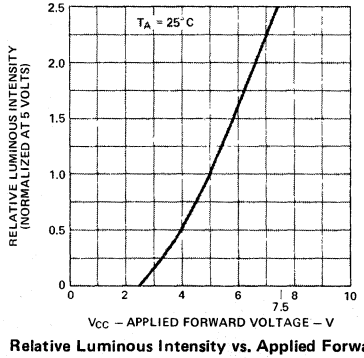


Figure 1. Relative Luminous Intensity vs. Applied Forward Voltage

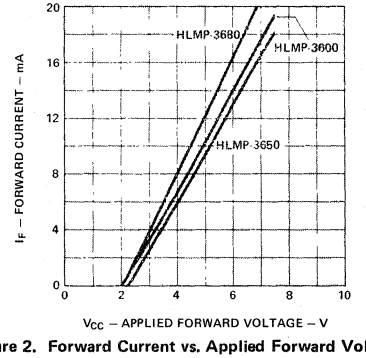


Figure 2. Forward Current vs. Applied Forward Voltage

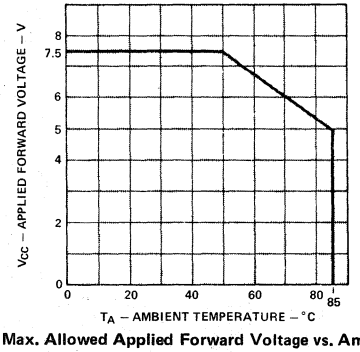


Figure 3. Max. Allowed Applied Forward Voltage vs. Ambient Temp.

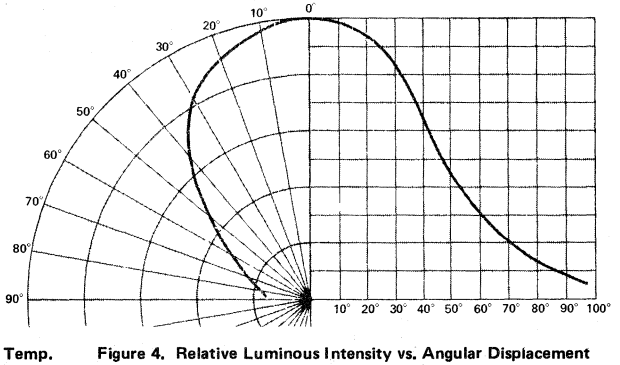


Figure 4. Relative Luminous Intensity vs. Angular Displacement

HEWLETT PACKARD

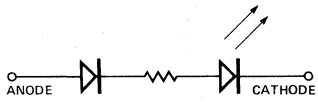
RED 5 AND 12 VOLT LED RESISTOR LAMPS

HLMP-3105
HLMP-3112

TECHNICAL DATA MARCH 1980

Features

- **INTEGRAL CURRENT LIMITING RESISTOR**
- **INTEGRAL REVERSE DIODE PROTECTION**
- **TTL COMPATIBLE: REQUIRES NO EXTERNAL CURRENT LIMITER WITH 5 VOLT/12 VOLT SUPPLY**
- **COST EFFECTIVE: SPACE SAVING**
- **PANEL MOUNTABLE T-1¾ PACKAGE**
- **WIRE WRAPPABLE LEADS**
- **WIDE VIEWING ANGLE**



Description

The HLMP-3105 and -3112 lamps contain an integral current limiting resistor and reverse current protection diode in series with the LED. This allows the lamp to be driven from a 5 volt/12 volt source without the need for an external current limiter. Both lamps utilize LED chips which are made from GaAsP on a GaAsP substrate. The color is standard red. These T-1¾ lamps are diffused to provide wide off-axis viewing and may be front panel mounted using the 5082-4707 clip and ring. The leads are wire wrappable.

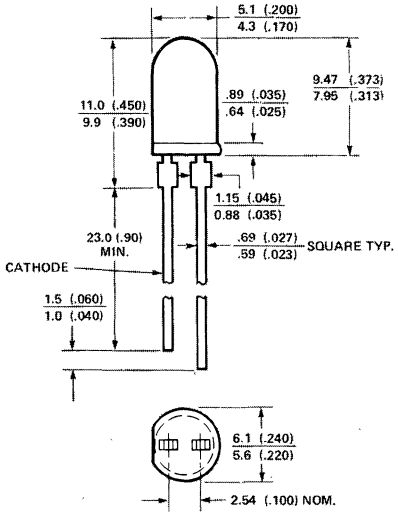
Absolute Maximum Ratings

(T_A = 25°C unless otherwise specified)

	HLMP-3105	HLMP-3112
DC Forward Voltage (T_A=25°C)	7.5 Volts[1]	15 Volts[2]
Reverse Voltage	20 Volts	20 Volts
Operating Temperature Range	-40°C to 85°C	-40°C to 85°C
Storage Temperature Range	-40°C to 85°C	-40°C to 85°C
Lead Soldering Temperature [1.6 mm (0.063 inch) from body]	260°C for 5 seconds	

Notes:
1. Derate from T_A = 50°C at 0.071V/°C. See Figure 3.
2. Derate from T_A = 50°C at 0.086V/°C. See Figure 3.

Package Dimensions



DIMENSIONS IN MILLIMETRES (INCHES).

SOLID STATE LAMPS

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	HLMP-3105			HLMP-3112			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity[4]	0.8	1.5					mcd	V_F = 5 Volts
					0.8	1.5		mcd	V_F = 12 Volts
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		90			90			Note 1 (See Figure 2)
λ_{Peak}	Peak Wavelength		655			655		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			640		nm	Note 2
$R\theta_{J-PIN}$	Thermal Resistance		90			90		°C/W	Junction to Lead at 3mm from Body
I_F	Forward Current		13	20				mA	V_F = 5 Volts
						14	20	mA	V_F = 12 Volts
I_R	Reverse Current			10			10	μA	V_R = 12 Volts
η_V	Luminous Efficacy		55			55		lm/W	Note 3

Notes:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.
4. The luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:
$I_V(T_A) = I_V(25°C)\, e^{[-0.188(T_A - 25°C)]}$

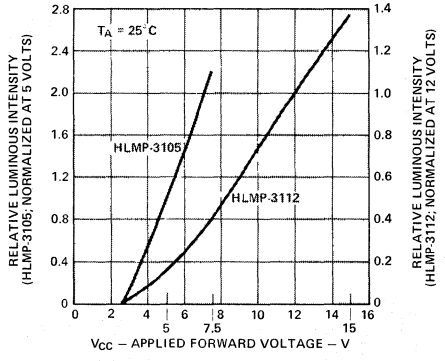


Figure 1. Relative Luminous Intensity vs. Applied Forward Voltage

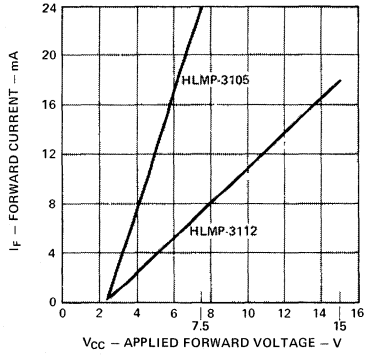


Figure 2. Forward Current vs. Applied Forward Voltage

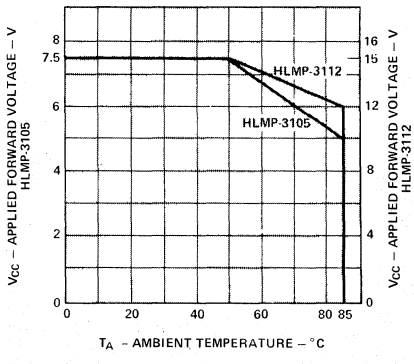


Figure 3. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R_{\theta JA}$ = 175°C/W

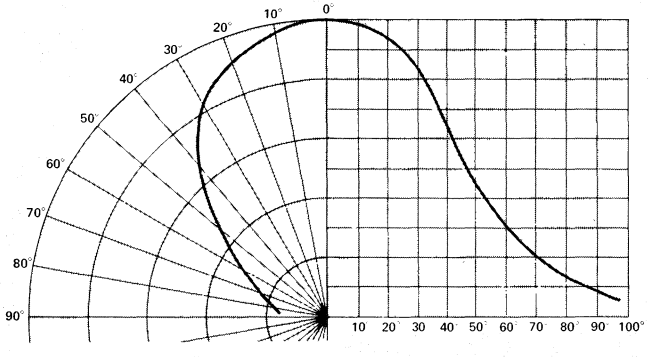


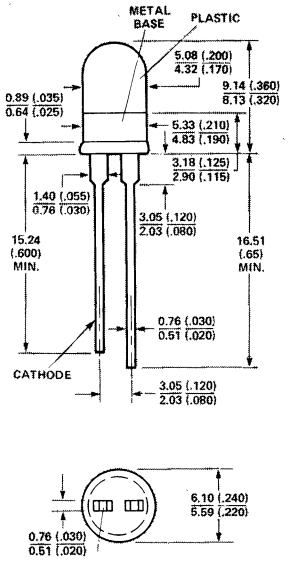
Figure 4. Relative Luminous Intensity vs. Angular Displacement

HEWLETT PACKARD

RESISTOR LEDs

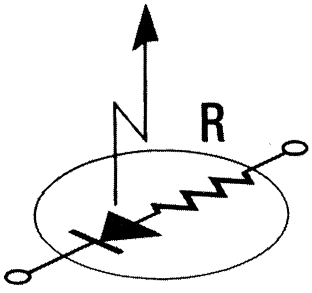
5082-4860
5082-4468

TECHNICAL DATA MARCH 1980

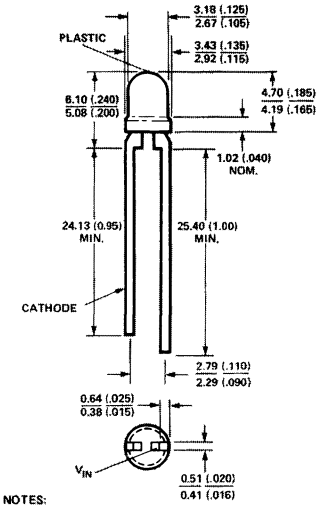


5082-4860

NOTE: AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (0.040") DOWN THE LEADS.



DIMENSIONS IN MILLIMETRES AND (INCHES)



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

5082-4468

Features

- **TTL COMPATIBLE: 16mA @ 5 VOLTS TYPICAL**
- **INTEGRAL CURRENT LIMITING RESISTOR**
- **T-1 DIAMETER PACKAGE, 3.18mm (.125 in.)**
  T-1¾ DIAMETER PACKAGE, 5.08mm (.200 in.)
- **RUGGED AND RELIABLE**

Description

The HP Resistor-LED series provides an integral current limiting resistor in series with the LED. Applications include panel mounted indicators, cartridge indicators, and lighted switches.

The 5082-4860 is a standard red diffused 5.08mm (.200") diameter (T-1¾ size) LED, with long wire wrappable leads.

The 5082-4468 is a clear diffused 3.18mm (.125") diameter (T-1 size) LED.

Absolute Maximum Ratings at T_A=25°C

DC Forward Voltage [Derate linearly to 5V @ 100°C]	7.5V
Reverse Voltage	7V
Isolation Voltage [between lead and base of the 5082-4860]	300V
Operating and Storage Temperature Range	–55°C to +100°C
Lead Soldering Temperature	230°C for 7 sec.

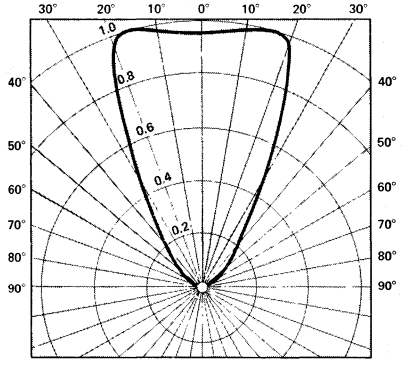
SOLID STATE LAMPS

Electrical Characteristics at $T_A = 25°C$

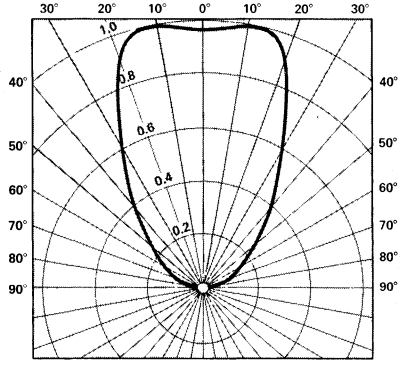
Symbol	Parameters	5082-4860/-4468			Units	Test Conditions
		Min.	Typ.	Max.		
I_V	Luminous Intensity	0.3	0.8		mcd	$V_F = 5.0V$
λ_{PEAK}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
I_F	Forward Current		16	20	mA	$V_F = 5.0V$
BV_R	Reverse Breakdown Voltage	3			V	$I_R = 100\mu A$

TYPICAL RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT

4860



4468



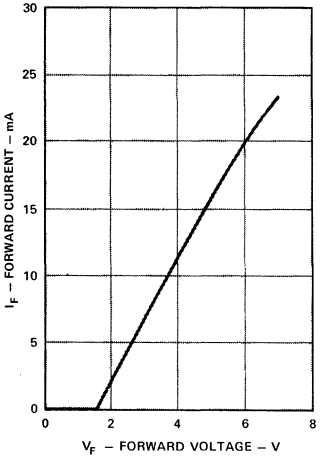


Figure 1. Typical DC Forward Current – Voltage Characteristic

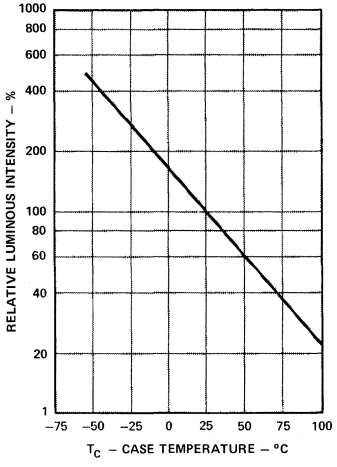


Figure 2. Relative Luminosity vs. Case Temperature

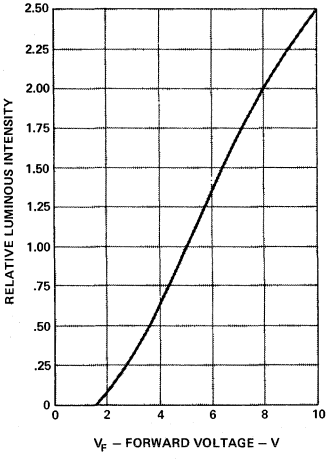


Figure 3. Relative Luminous Intensity vs. Voltage

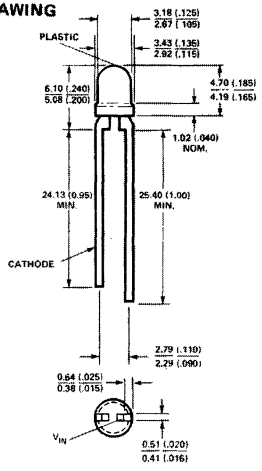
HEWLETT PACKARD

VOLTAGE SENSING LED

5082-4732

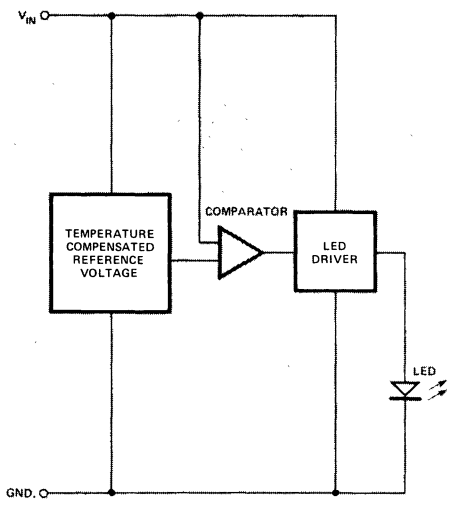
TECHNICAL DATA MARCH 1980

OUTLINE DRAWING



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

BLOCK DIAGRAM



Features

- **HIGH SENSITIVITY: 10mV ON TO OFF**
- **BUILT IN LED CURRENT LIMITING**
- **TEMPERATURE COMPENSATED THRESHOLD VOLTAGE**
- **COMPACT: PACKAGE INCLUDES INTEGRATED CIRCUIT AND LED**
- **GUARANTEED MINIMUM LUMINOUS INTENSITY**
- **THRESHOLD VOLTAGE CAN BE INCREASED WITH EXTERNAL COMPONENT**

Applications

- Push-to-test battery voltage tester (pagers, cameras, appliances, radios, test equipment. . .)
- Logic level indicator
- Power supply voltage monitor
- V-U meter
- Analog level sense
- Voltage indicating arrays — use several with different thresholds
- Current monitor

Description

The HP voltage sensing LEDs use an integrated circuit and a red GaAsP LED to provide a complete voltage sensing function in a standard red diffused T-1 LED package. When the input voltage (V_{IN}) exceeds the threshold voltage (V_{TH}) the LED turns "on". The high gain of the comparator provides unambiguous indication by the LED of the input voltage with respect to the threshold voltage. The V-I characteristics are resistive above and below the threshold voltage. This allows battery testing under simulated load conditions. Use of a resistor, diode or zener in series allows the threshold voltage to be increased to any desired voltage. A resistor in parallel allows the sensing LED to be used as a current threshold indicator.

The 5082-4732 has a nominal threshold voltage of 2.7V.

Absolute Maximum Ratings

Storage Temperature	-55°C to +100°C
Operating Temperature	-55°C to +85°C
Lead Solder Temperature	230°C for 7 Sec
Input Voltage — V_{IN} [1]	+5V dc
Reverse Input Voltage — V_R	-0.5V

NOTES:
1. Derate linearly above 50° C free-air temperature at a rate of 37mV/°C.

SOLID STATE LAMPS

Electro-Optical Characteristics at $T_A = 25°C$

Parameter	Sym.	5082-4732 Min.	Typ.	Max.	Units	Test Conditions	Fig.
Threshold Voltage	V_{TH}	2.5	2.7	2.9	V		1,2
Temperature Coefficient of Threshold	$\frac{\Delta V_{TH}}{\Delta T_A}$		−1		mV/°C		
Input Current	I_{IN}		13		mA	$V_{IN} = 2.75V$	2
			33	50	mA	$V_{IN} = 5.0V$	2
Luminous Intensity	I_V	0.3	0.7		mcd	$V_{IN} = 2.75V$	1
Wavelength	λ_{PEAK}		655		nm	Measurement at peak	
Dominant Wavelength	λ_d		639		nm	Note 1	

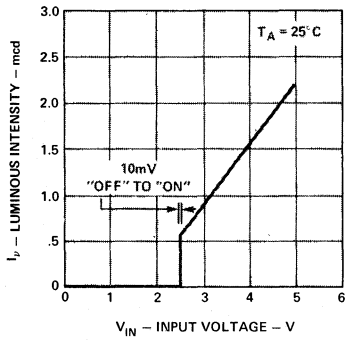


Figure 1. Luminous Intensity vs. Input Voltage.

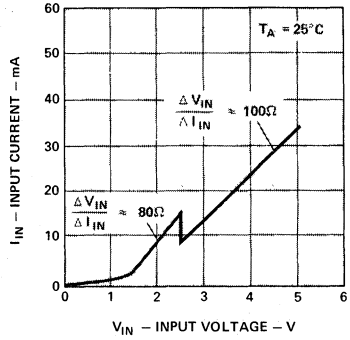


Figure 2. Input Current vs. Input Voltage.

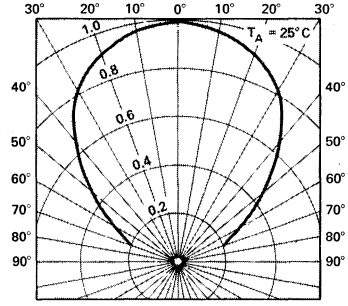
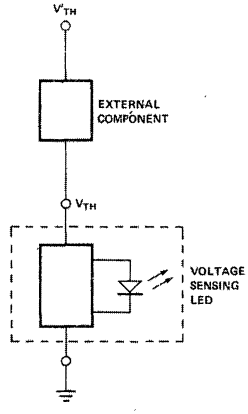


Figure 3. Relative Luminous Intensity vs. Angular Displacement.

Techniques For Increasing The Threshold Voltage



External Component	V'_{TH}	$TC = \frac{\Delta V'_{TH}}{\Delta T_A}$ (mV/°C)
Schottky Diode (HP 5082-2835)	$V_{TH} + 0.45V$	-2
P-N Diode (1N914)	$V_{TH} + 0.75V$	-2.5
LED (HP 5082-4484)	$V_{TH} + 1.6V$	-2.9
Zener Diode	$V_{TH} + V_Z$	−1 + Zener TC

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. I_{TH} is the maximum current just below the threshold, V_{TH}. Since both I_{TH} and V_{TH} are variable, a precise value of V'_{TH} is obtainable only by selecting R to fit the measured characteristics of the individual devices (e.g., with curve tracer).
3. The temperature coefficient (TC) will be a function of the resistor TC and the value of the resistor.

HEWLETT PACKARD

SUBMINIATURE RESISTOR LAMPS

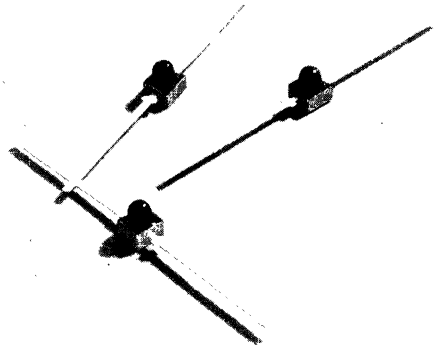
HIGH EFFICIENCY RED

5 VOLT, 4mA • HLMP-6620
5 VOLT, 10mA • HLMP-6600

TECHNICAL DATA JANUARY 1980

Features

- **IDEAL FOR TTL AND LSTTL GATE STATUS INDICATION**
- **REQUIRES NO EXTERNAL RESISTORS WITH 5 VOLT SUPPLY**
- **SPACE SAVING SUBMINIATURE PACKAGE**
- **TWO CHOICES OF CURRENT LEVEL**
- **RUGGED INTEGRAL RESISTOR AND REVERSE PROTECTION DIODE**
- **EXCELLENT VIEWING ANGLE**



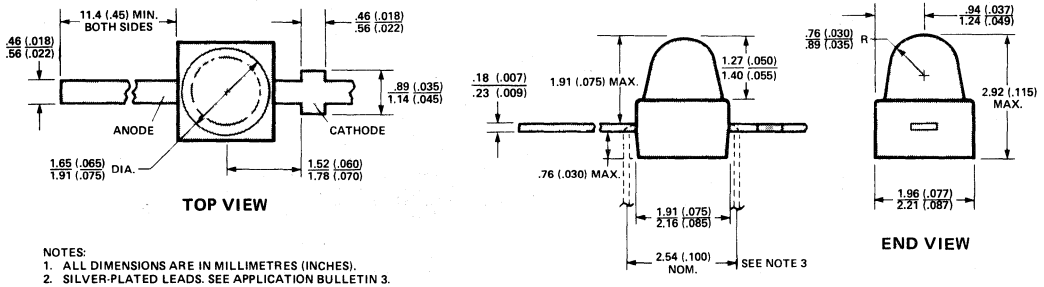
Description

The HLMP-6600 and HLMP-6620 provide a Red Gallium Arsenide Phosphide on Gallium Phosphide Light Emitting Diode together with an integral biasing resistor and reverse protection diode. The package has a red diffused lens and radial leads. Tape-and-reel mounting is available on request.

Absolute Maximum Ratings

	HLMP-6600	HLMP-6620
DC Forward Voltage	6 Volts	6 Volts
Reverse Voltage	15 Volts	15 Volts
Operating Temperature Range	-55°C to 70°C	
Storage Temperature Range	-55°C to 100°C	
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	245°C for 5 sec.	

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	HLMP-6600			HLMP-6620			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	1.0	2.4	—	0.2	0.6	—	mcd	V_F = 5 Volts (See Figure 1)
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		90°			90°			Note 1 (See Figure 2)
λ_{PEAK}	Peak Wavelength		635			635		nm	Measurement at Peak
λ_d	Dominant Wavelength		628			628		nm	Note 2
Θ_j	Thermal Resistance		120			120		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
I_F	Forward Current		9.6	13		3.5	5	mA	V_F=5 Volts (See Figure 3)
I_R	Reverse Current			10			10	μA	V_R=15 Volts
η_V	Luminous Efficacy		147			147		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

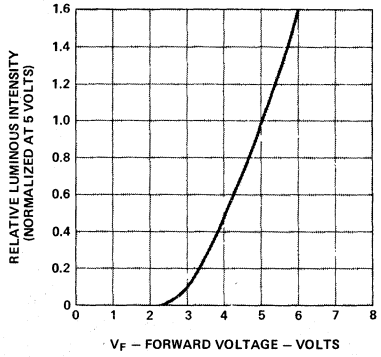


Figure 1. Relative Luminous Intensity vs. Forward Voltage.

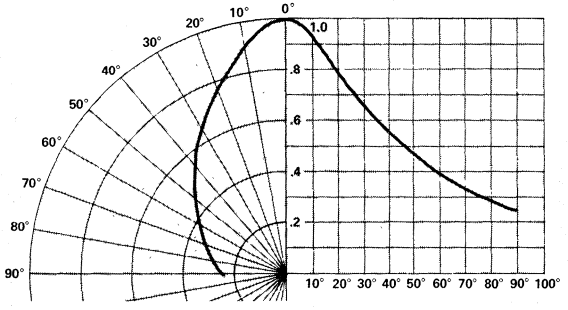


Figure 2. Relative Luminous Intensity vs. Angular Displacement.

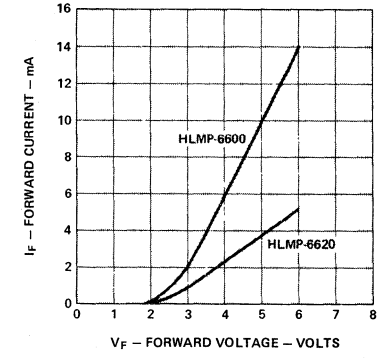


Figure 3. Forward Current vs. Forward Voltage.

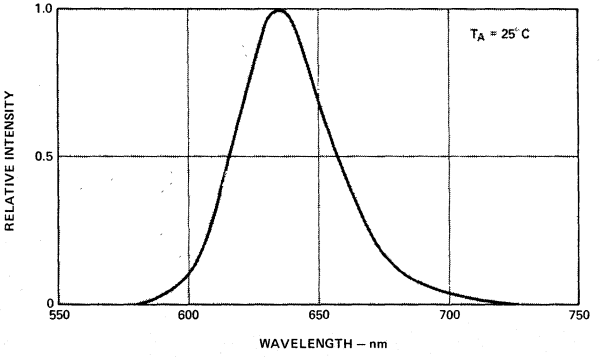


Figure 4. Relative Intensity vs. Wavelength.

HEWLETT PACKARD

HERMETIC SOLID STATE LAMPS*

1N6092 1N6094
1N6093 1N5765

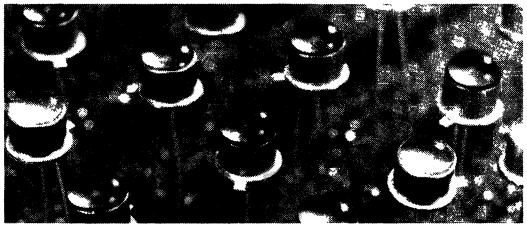
JAN 1N5765/ 1N6092/1N6093/1N6094

JAN TX 1N5765/ 1N6092/1N6093/1N6094

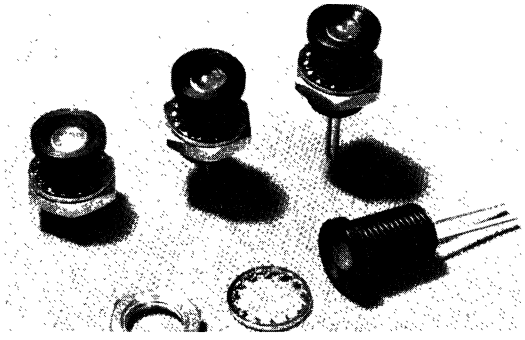
TECHNICAL DATA MARCH 1980

Features

- **CHOICE OF 4 COLORS**
  - **Red**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **DESIGNED FOR HIGH-RELIABILITY APPLICATIONS**
- **HERMETICALLY SEALED**
- **WIDE VIEWING ANGLE**
- **LOW POWER OPERATION**
- **IC COMPATIBLE**
- **LONG LIFE**
- **PANEL MOUNT OPTION HAS WIRE WRAPPABLE LEADS AND AN ELECTRICALLY ISOLATED CASE**



TO-46



HERMETIC PANEL MOUNT

Description

The 1N5765, 1N6092, 1N6093, and 1N6094 are hermetically sealed solid state lamps encapsulated in a TO-46 package with a tinted diffused plastic lens over a glass window. These hermetic lamps provide good on-off contrast, high axial luminous intensity and a wide viewing angle.

All of these devices are available in a panel mountable fixture. The semiconductor chips are packaged in a hermetically sealed TO-46 package with a tinted diffused plastic lens over glass window. This TO-46 package is then encapsulated in a panel mountable fixture designed for high reliability applications. The encapsulated LED lamp assembly provides a high on-off contrast, a high axial luminous intensity and a wide viewing angle.

The 1N5765 utilizes a GaAsP LED chip with a red diffused plastic lens over glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused plastic lens over glass window. This lamp's efficiency is comparable to that of a GaP red but extends to higher current levels.

The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow diffused plastic lens over glass window.

The 1N6094 provides a green GaP LED chip with a green diffused plastic lens over glass window.

Color — Part Number — Panel Mount Matrix				
Description	**Red**	**High Efficiency Red**	**Yellow**	**Green**
Base Hermetic Part	1N5765	1N6092	1N6093	1N6094
Base Hermetic Part in Panel-Mount	5082-4787	5082-4687	5082-4587	5082-4987
JAN Part	JAN1N5765	JAN1N6092	JAN1N6093	JAN1N6094
JAN Part in Panel-Mount	HLMP-0930	M19500/519-01	M19500/520-01	M19500/521-01
JANTX Part	JANTX1N5765	JANTX1N6092	JANTX1N6093	JANTX1N6094
JANTX Part in Panel-Mount	HLMP-0931	M19500/519-02	M19500/520-02	M19500/521-02

*Panel-Mount versions of all of the above are available per the selection matrix on this page.

JAN 1N5765: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/467. A summary of the data gathered in Groups A, B, and C lot acceptance testing is supplied with each shipment.

JAN TX 1N5765: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/467. The JAN TX lot is then subjected to Group A, Group B and Group C tests as for the JAN 1N5765 above. A summary of the data gathered in Groups A, B and C acceptance testing can be provided upon request. Serialized data can be gathered, but lead times will be increased accordingly.

Group B Sample Acceptance Tests	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Thermal Shock	1056A
Temperature Cycling	1051A
Fine Leak Test	1071H
Gross Leak Test	1071C
Moisture Resistance	1021
Mechanical Shock	2016
Vibration	2056
Constant Acceleration	2006
Terminal Strength	2036E
Salt Atmosphere	1041
Temp. Storage (100°C, 340 hours)	1032
Operating Life (50mAdc, 340 hours)	1027

Group C Sample Acceptance Tests	Method MIL-STD-750
Low Temp. Operation (–55°C)	
Breakdown Voltage	4021
Temperature Cycling	1051A
Resistance to Solvents	*
Temp. Storage (100°C, 1K hours)	1031
Operating Life (50mAdc, 1K hours)	1026
Peak Forward Pulse Current	
TX Screening (100%)	
Temp. Storage (100°C, 72 hours)	
Temperature Cycling	1051A
Constant Acceleration	2006
Fine Leak Test	1071H
Gross Leak Test	1071C
Burn-in (50mAdc, 168 hours)	
Evaluation of Drift (I_{V1}, V_F, I_R)	

*MIL-STD-202 Method 215

Electrical / Optical Characteristics at T_A=25°C

(Per Table I, Group A Testing of MIL-S 19500/467)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Luminous Intensity (Axial)	I_{v1}	0.5	3.0	mcd	I_F = 20mAdc, θ = 0°
Luminous Intensity (off Axis)	I_{v2}	0.3		mcd	I_F = 20mAdc, θ = 30° [see Note 1]
Wavelength	λ_v	630	700	nM	Design Parameter
Capacitance	C		300	pF	V_R = 0, f = 1MHz
Forward Voltage	V_F		2.0	Vdc	I_F = 20mAdc
Reverse Current	I_R		1	μAdc	V_R = 3Vdc [see Note 1]

NOTES:

1. These specifications apply only to JAN/JAN TX levels.

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 1N5765/4787	High Eff. Red 1N6092/4687	Yellow 1N6093/4587	Green 1N6094/4987	Units
Power Dissipation (derate linearly from 50°C at 1.6mW/°C)	100	120	120	120	mW
DC Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in:) from body]	260°C for 7 seconds.				

1. Derate from 50° C at 0.2mA/° C
2. Derate from 50° C at 0.5mA/° C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	1N5765/5082-4787			1N6092/5082-4687			1N6093/5082-4587			1N6094/5082-4987			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	0.5	1.0		1.0	2.5		1.0	2.5		0.8	1.6		mcd	I_F = 20mA Figs. 3,8,13,18
											At I_F = 25mA				
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		60			70			70			70		deg.	Note 1. Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			626			585			570		nm	Note 2
τ_S	Speed of Response		10			200			200			200		ns	
C	Capacitance		200			35			35			35		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance*		425			425			425			425		°C/W	Note 3
Θ_{JC}	Thermal Resistance**		550			550			550			550		°C/W	Note 3
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20mA Figures 2, 7, 12, 17
												At I_F = 25mA			
BV_R	Reverse Breakdown Voltage	4	5		5.0			5.0			5.0			V	I_R = 100μA
η_V	Luminous Efficacy		56			140			455			600		lm/W	Note 4

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-46

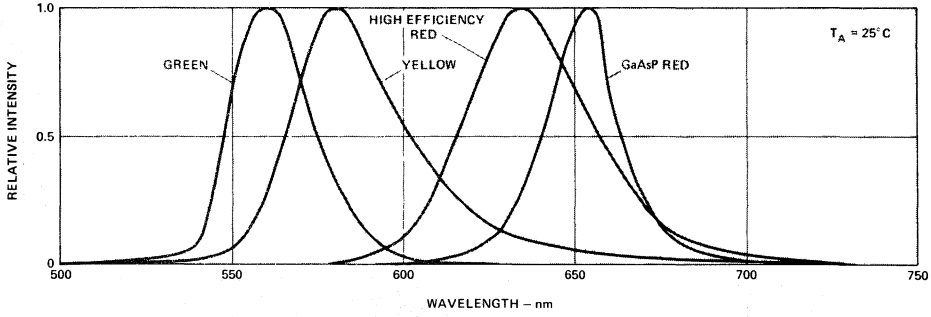
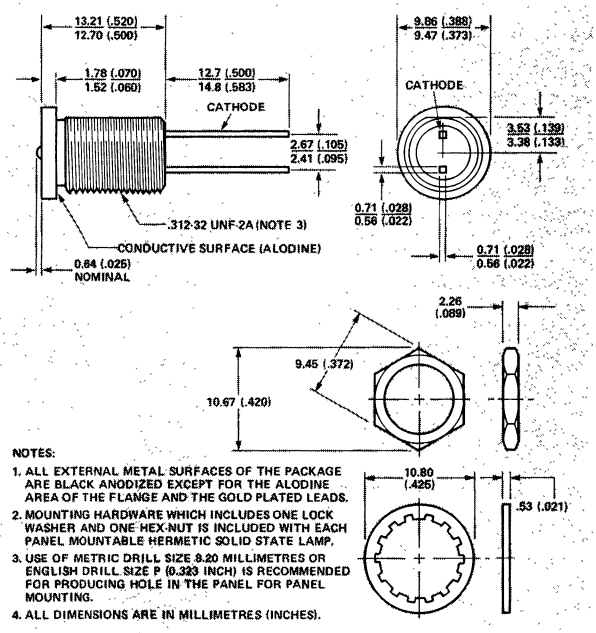


Figure 1. Relative Intensity vs. Wavelength.

Package Dimensions

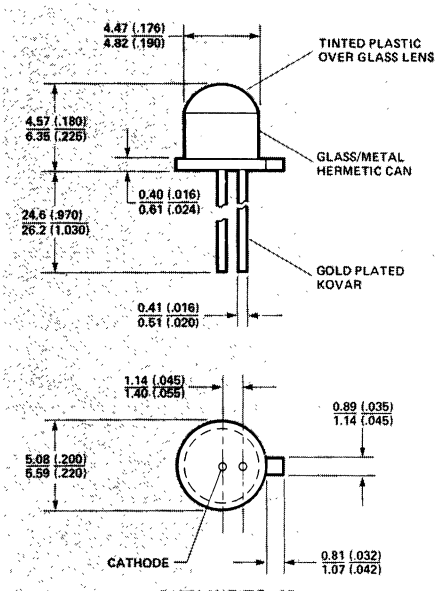
5082-4787, 4687, 4587, 4987



NOTES:

1. ALL EXTERNAL METAL SURFACES OF THE PACKAGE ARE BLACK ANODIZED EXCEPT FOR THE ALODINE AREA OF THE FLANGE AND THE GOLD PLATED LEADS.
2. MOUNTING HARDWARE WHICH INCLUDES ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNTABLE HERMETIC SOLID STATE LAMP.
3. USE OF METRIC DRILL SIZE 9.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
4. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED LEADS.

RED 1N5765/5082-4787

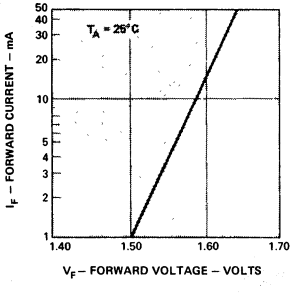


Figure 2. Forward Current vs. Forward Voltage.

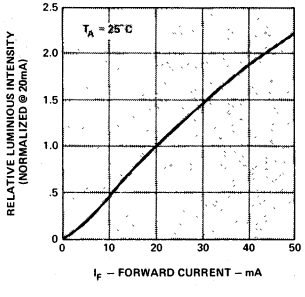


Figure 3. Relative Luminous Intensity vs. Forward Current.

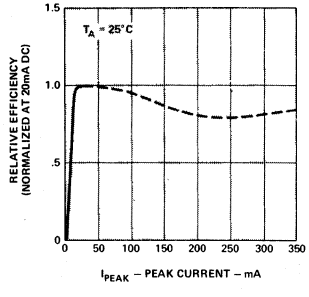


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

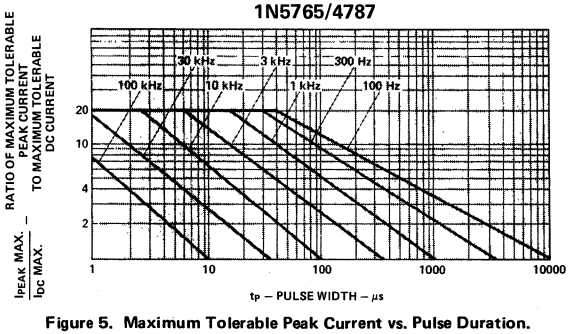


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

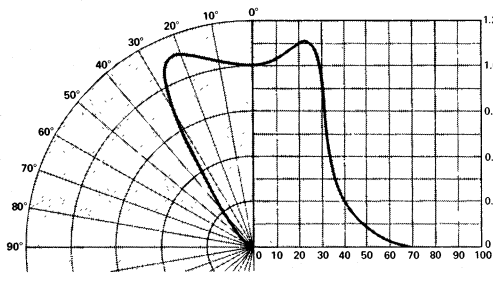


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HIGH EFFICIENCY RED 1N6092/5082-4687

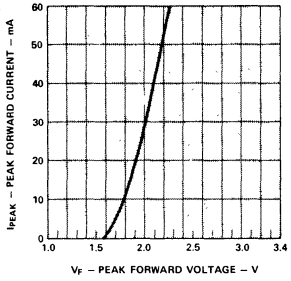


Figure 7. Forward Current vs. Forward Voltage.

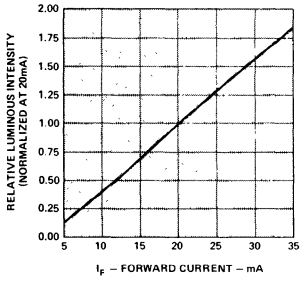


Figure 8. Relative Luminous Intensity vs. Forward Current.

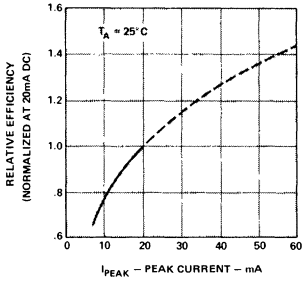


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

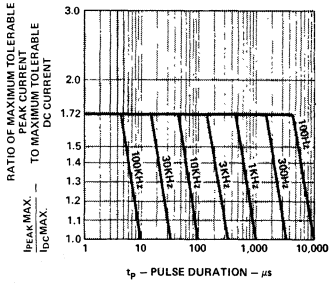


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

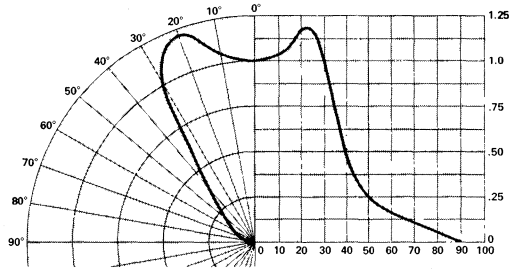


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

YELLOW 1N6093/5082-4587

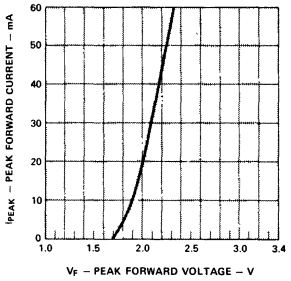


Figure 12. Forward Current vs. Forward Voltage.

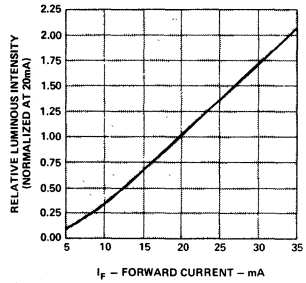


Figure 13. Relative Luminous Intensity vs. Forward Current.

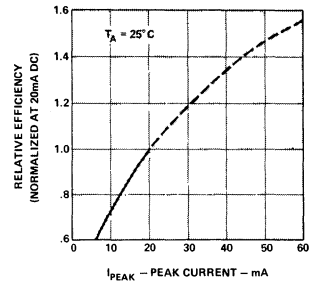


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

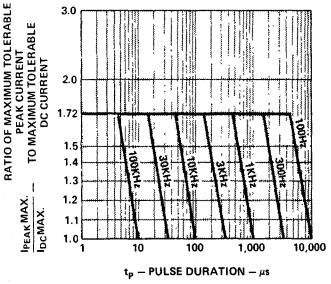


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

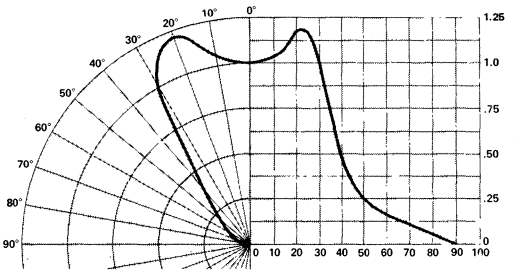


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

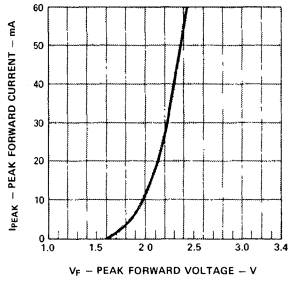


Figure 17. Forward Current vs. Forward Voltage.

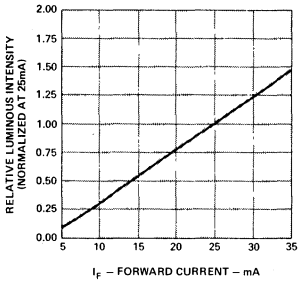


Figure 18. Relative Luminous Intensity vs. Forward Current.

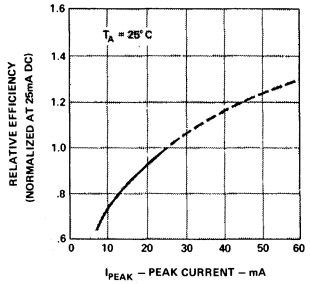


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

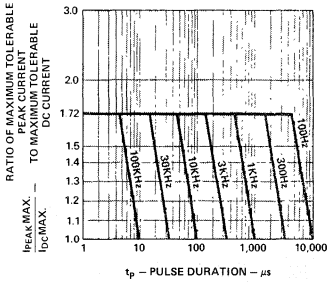


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

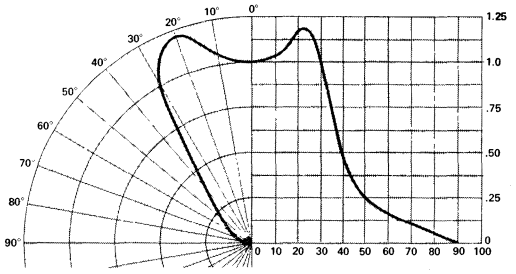


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

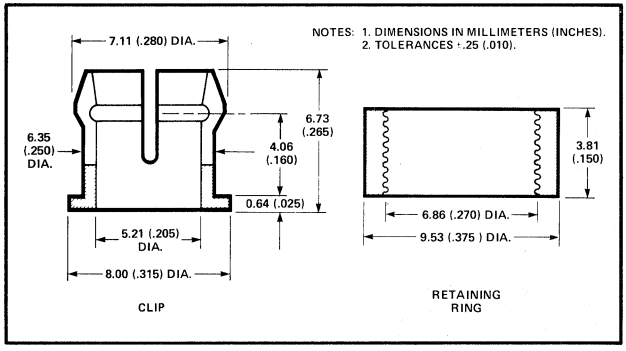
CLIP AND RETAINING RING FOR PANEL MOUNTED LEDs

5082-4707

TECHNICAL DATA MARCH 1980

Description

The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State high profile T - 1¾ size lamps. This clip and ring combination is intended for installation in instrument panels up to 3.18mm (.125") thick. For panels greater than 3.18mm (.125"), counterboring is required to the 3.18mm (.125") thickness.



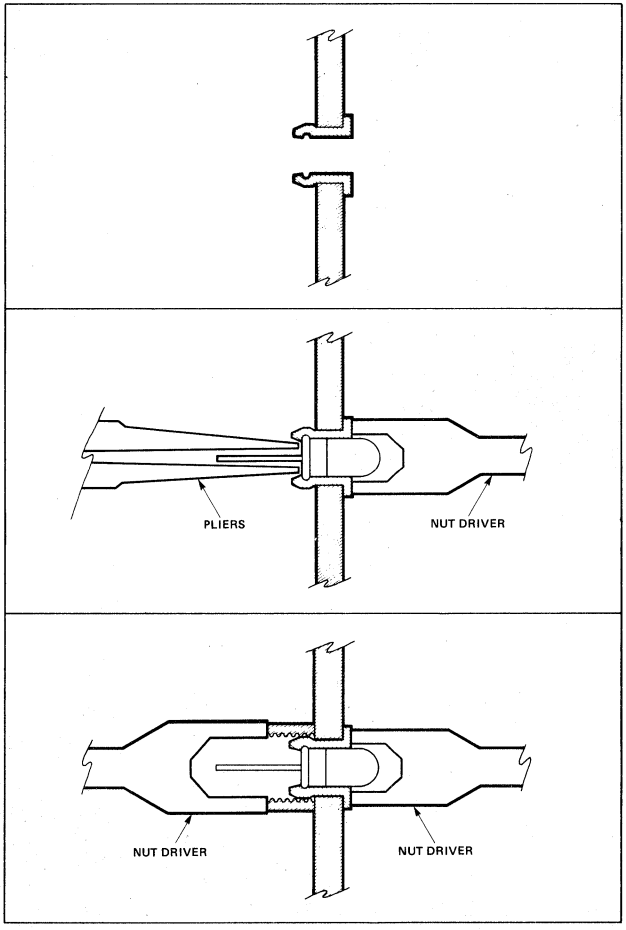
Mounting Instructions

1. Drill an ASA C size 6.15mm (.242") dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

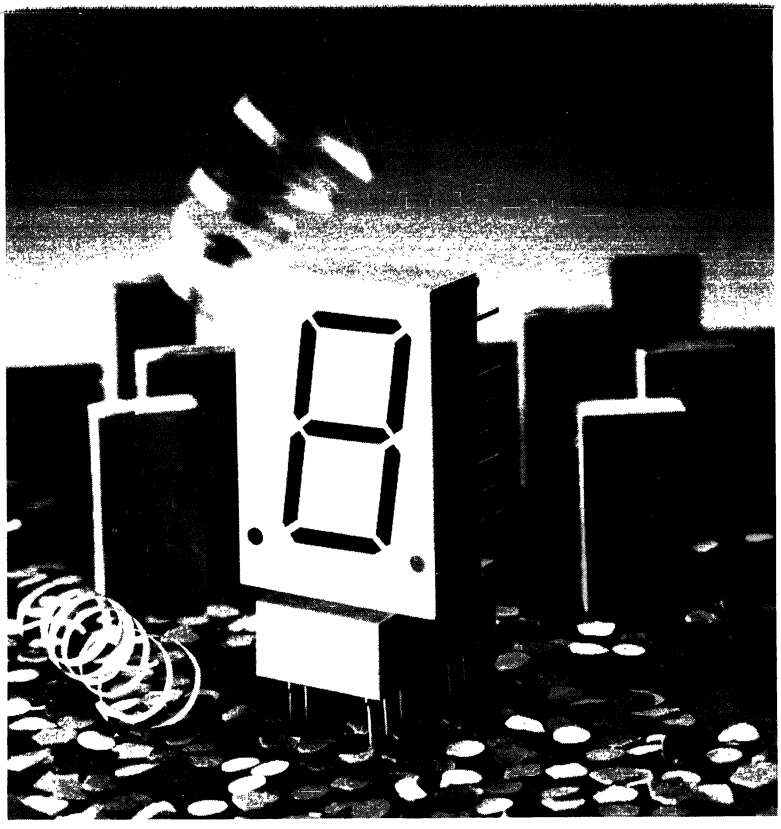
2. Press the panel clip into the hole from the front of the panel.

3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.

4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.

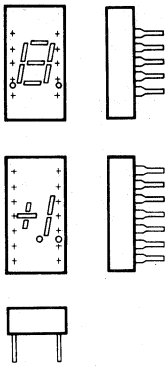
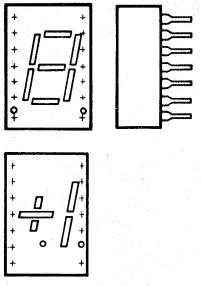
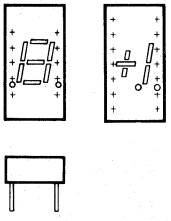


SOLID STATE LAMPS

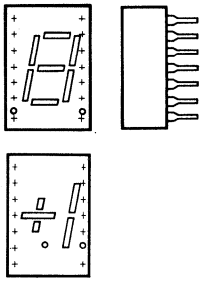
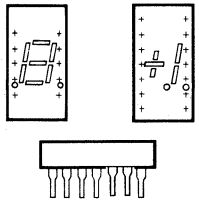
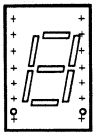
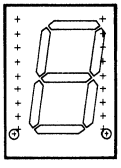


Solid State Displays

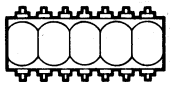
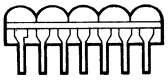
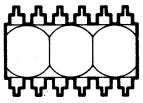
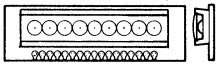
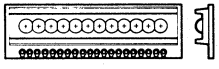
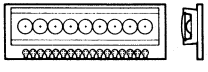
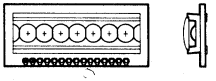
Red, High Efficiency Red, Yellow and Green Seven Segment LED Displays

Package	Device	Description	Application	Page No.
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	5082-7610	High Efficiency Red, Common Anode, LHDP (14 Pin Epoxy)	General Purpose Market • Test Equipment • Digital Clocks • Clock Radios • TV Channel Indicators • Business Machines • Digital Instruments • Automobiles For further information see Application Notes 941 and 964 beginning on page 332.	180
	5082-7611	High Efficiency Red, Common Anode, RHDP (14 Pin Epoxy)		
	5082-7613	High Efficiency Red, Common Cathode, RHDP (10 Pin Epoxy)		
	5082-7616	7.11mm (.29") High Efficiency Red, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		
	5082-7620	Yellow, Common Anode LHDP (14 Pin Epoxy)		
	5082-7621	Yellow, Common Anode RHDP (14 Pin Epoxy)		
	5082-7623	Yellow, Common Cathode, RHDP (10 Pin Epoxy)		
	5082-7626	7.11mm (.29") Yellow, Universal Polarity and Overflow Indicator RHDP (14 Pin Epoxy)		
	5082-7630	Green, Common Anode LHDP (14 Pin Epoxy)		
	5082-7631	Green, Common Anode RHDP (14 Pin Epoxy)		
	5082-7633	Green, Common Cathode RHDP (10 Pin Epoxy)		
	5082-7636	7.11mm (.29") Green, Universal Polarity and Overflow Indicator RHDP (14 Pin Epoxy)		
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	5082-7650	High Efficiency Red, Common Anode, LHDP		185
	5082-7651	High Efficiency Red, Common Anode, RHDP		
	5082-7653	High Efficiency Red, Common Cathode RHDP		
	5082-7656	10.36 (.4") High Efficiency Red Universal Polarity and Overflow Indicator RHDP		
	5082-7660	Yellow Common Anode LHDP		
	5082-7661	Yellow Common Anode RHDP		
	5082-7663	Yellow Common Cathode RHDP		
	5082-7666	10.36 (.4") Yellow Universal Polarity and Overflow Indicator RHDP		
	5082-7670	Green Common Anode LHDP		
	5082-7671	Green Common Anode RHDP		
	5082-7673	Green Common Cathode RHDP		
	5082-7676	10.36 (.4") Green Universal Polarity and Overflow Indicator RHDP		
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	HDSP-3530	High Efficiency Red, Common Anode, LHDP (14 Pin Epoxy)		190
	HDSP-3531	High Efficiency Red, Common Anode, RHDP (14 Pin Epoxy)		
	HDSP-3533	High Efficiency Red, Common Cathode RHDP (10 Pin Epoxy)		
	HDSP-3536	7.11mm (.29") High Efficiency Red, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		
	HDSP-4030	Yellow , Common Anode, LHDP (14 Pin Epoxy)		
	HDSP-4031	Yellow, Common Anode, RHDP		
	HDSP-4033	Yellow, Common Cathode, RHDP (10 Pin Epoxy)		
	HDSP-4036	7.11mm (.29") Yellow, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		

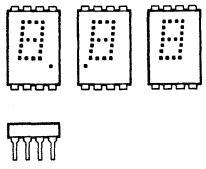
Red, High Efficiency Red, Yellow and Green Seven Segment LED Displays (Cont.)

Package	Device	Description	Application	Page No.
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	HDSP-3730	High Efficiency Red, Common Anode, LHDP	General Purpose Market • Test Equipment • Digital Clocks • Clock Radios • TV Channel Indicators • Business Machines • Digital Instruments • Automobiles For further information see Application Notes 941 and 964 beginning on page 332.	190
	HDSP-3731	High Efficiency Red, Common Anode, RHDP		
	HDSP-3733	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3736	10.36mm (.4") High Efficiency Red, Universal Polarity Overflow Indicator RHDP		
	HDSP-4130	Yellow, Common Anode LHDP		
	HDSP-4131	Yellow, Common Anode RHDP		
	HDSP-4133	Yellow, Common Cathode RHDP		
	HDSP-4136	10.36mm (.4") Yellow, Universal Polarity Overflow Indicator RHDP		
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	5082-7730	Red, Common Anode, LHDP (14 Pin Epoxy)		196
	5082-7731	Red, Common Anode, RHDP (14 Pin Epoxy)		
	5082-7736	7.11mm (.29") Red, Common Anode, Polarity and Overflow Indicator (14 Pin Epoxy)		
	5082-7740	Red, Common Cathode, RHDP (10 Pin Epoxy)		
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	5082-7750	Red, Common Anode, LHDP		200
	5082-7751	Red, Common Anode, RHDP		
	5082-7756	10.36mm (.4") Red, Universal Polarity and Overflow Indicator, RHDP		
	5082-7760	Red, Common Cathode, RHDP		
 20.32mm (.8") Dual-In-Line 1.09"H x .78"W x .33"D (18 Pin Epoxy)	HDSP-3400	Red, Common Anode LHDP		204
	HDSP-3401	Red, Common Anode RHDP		
	HDSP-3403	Red, Common Cathode RHDP		
	HDSP-3405	Red, Common Cathode LHDP		
	HDSP-3406	18.87mm (.74") Red, Universal Polarity Overflow Indicator RHDP		

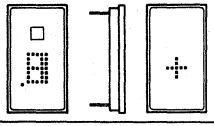
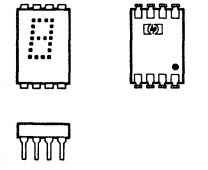
Red Seven Segment LED Displays

Device		Description	Package	Application	Page No.
  	5082-7402	2.79mm(.11") Red, 3 Digits Right,[1] Centered D.P.	12 Pin Epoxy, 7.62mm (.3") DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatches • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	208
	5082-7403	2.79mm(.11") Red, 3 Digits Left,[1] Centered D.P.			
	5082-7404	2.79mm(.11") Red, 4 Digits Centered D.P.			
	5082-7405	2.79mm(.11") Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7412	2.79mm (.11") Red, 3 Digits Right,[1] RHDP	12 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7413	2.79mm (.11") Red, 3 Digits Left,[1] RHDP			
	5082-7414	2.79mm(.11") Red, 4 Digit, RHDP			
	5082-7415	2.79mm(.11") Red, 5 Digit, RHDP	14 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7432	2.79mm(.11") Red, 2 Digits Right,[2] RHDP	12 Pin Epoxy, 7.62mm (.3") DIP		212
	5082-7433	2.79mm(.11") Red, 3 Digits, RHDP			
	5082-7440	2.67mm(.105") Red, 8 Digits, Mounted on P.C. Board	50.8mm(2") P.C. Bd., 17 Term. Edge Con.		216
	5082-7448	2.67mm(.105") Red, 8 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 17 Term. Edge Con.		
	5082-7441	2.67mm(.105") Red, 9 Digits, Mounted on P.C. Board	50.8mm(2") PC Bd., 17 Term. Edge Con.		
	5082-7449	2.67mm(.105") Red, 9 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 17 Term. Edge Con.		
	5082-7442	2.54mm(.100") Red, 12 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 20 Term. Edge Con.		220
	5082-7445	2.54mm(.100") Red, 12 Digits, Mounted on P.C. Board	59.6mm(2.345")PC Bd., 20 Term. Edge Con.		
	5082-7444	2.54mm(.100") Red, 14 Digits, Mounted on P.C. Board	60.3mm(2.375") PC Bd., 22 Term. Edge Con.		
	5082-7446	2.92mm(.115") Red, 16 Digits, Mounted on P.C. Board	69.85mm(2.750")PC Bd., 24 Term. Edge Con.		
	5082-7447	2.85mm(.112") Red, 14 Digits, Mounted on P.C. Board	60.3mm(2.375") PC Bd., 22 Term. Edge Con.		
	5082-7240	2.59mm(.102") Red, 8 Digits, Mounted on P.C. Board	50.8mm (2") PC Bd., 17 Term. Edge Con.		224
	5082-7241	2.59mm(.102") Red, 9 Digits, Mounted on P.C. Board.			
	5082-7265	4.45mm(.175") Red, 5 Digits, Mounted on P.C. Board. Centered D.P.	50.8mm(2") PC Bd., 15 Term. Edge Con.		228
	5082-7285	4.45mm(.175") Red, 5 Digits Mounted on P.C. Board. RHDP			
	5082-7275	4.45mm(.175") Red, 15 Digits, Mounted on P.C. Board. Centered D.P.	91.2mm(3.59") PC Bd., 23 Term. Edge Con.		
	5082-7295	4.45mm(.175") Red, 15 Digits, Mounted on P.C. Board. RHDP			

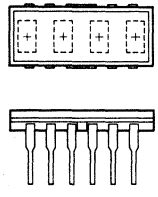
Integrated LED Displays

Device		Description	Package	Application	Page No.
	5082-7300	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decover/Driver/Memory	8 Pin Epoxy, 15.2mm (.6") DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics For further information ask for Application Note 934 on LED Display Installation Techniques	232
	5082-7302	7.4mm (.29") 4x7 Single Digit Numeric, LHDP, Built-In Decover/Driver/Memory			
	5082-7340	7.4mm (.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7304	7.4mm (.29") Overrange Character Plus/Minus Sign			
	5082-7356	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2mm (.6") DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package IC's are required.	236
	5082-7357	7.4mm(.29") 4x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
	5082-7359	7.4mm (.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7358	7.4mm(.29") Overrange Character Plus/Minus Sign			

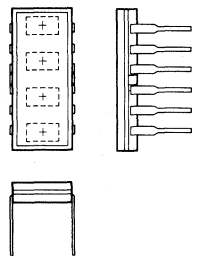
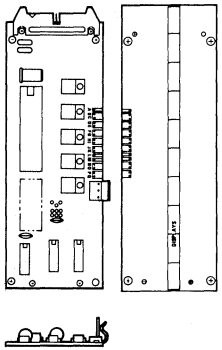
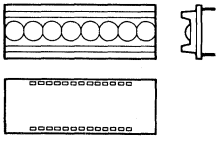
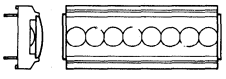
Hermetically Sealed Integrated LED Displays

Device		Description	Package	Application	Page No.
	5082-7010	6.8mm (.27") 5x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver	8 Pin Hermetic 2.54mm (.100") Pin Centers	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems	241
	5082-7011	6.8mm (.27") Plus/Minus Sign			
	5082-7391	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Hermetic 15.2mm (.6") DIP with Gold Plated Leads	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Applications	247
	5082-7392	7.4mm(.29") 4x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
	5082-7395	7.4mm(.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7393	7.4mm(.29") Overrange Character Plus/Minus Sign			

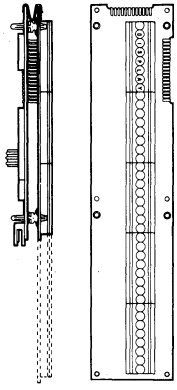
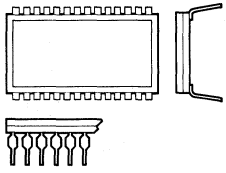
Alphanumeric LED Displays

Device		Description	Package	Application	Page No.
	HDSP-2000	3.7mm (.15") 5x7 Four Character Alphanumeric Built-In Shift Register, Drivers	12 Pin Ceramic 7.62mm (.3") DIP. Redglass Contrast Filter	• Programmable Calculators • Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Notes 966 and 1001, starting on page 368.	253

Alphanumeric LED Displays (Cont.)

Device		Description	Package	Application	Page No.
	HDSP-2001	3.7mm (.15") 5x7 Four Character Alphanumeric Built-In Shift Register, Drivers	12 Pin Ceramic 7.62mm (.3") DIP Integral Untinted Glass Lens	• Programmable Calculators • Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communication For further information see Application Notes 966 and 1001, starting on page 368.	257
	HDSP-2010		12 Pin Ceramic 7.62mm (.3") DIP Integral Red Glass Contrast Filter.	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics	261
	HDSP-2416	Single-Line 16 Character Display Panel Utilizing the HDSP-2000 Display	162.56mm (6.4") L x 58.42mm (2.3") H x 7.11mm (.28") D	• Data Entry Terminals • Instrumentation • Electronic Typewriters For further information see Application Note 1001 beginning on page 398.	265
	HDSP-2424	Single-Line 24 Character Display Panel Utilizing the HDSP-2000 Display.			
	HDSP-2432	Single-Line 32 Character Display Panel Utilizing the HDSP-2000 Display			
	HDSP-2440	Single-Line 40 Character Display Panel Utilizing the HDSP-2000 Display	177.80mm (7.0") L x 58.42mm (2.3") H x 7.11mm (.28") D		
	HDSP-2470	HDSP-2000 Display Interface Incorporating a 64 Character ASCII Decoder	171.22mm (6.74") L x 58.42mm (2.3") H x 16.51mm (.65") D		
	HDSP-2471	HDSP-2000 Display Interface Incorporating a 128 Character ASCII Decoder			
	HDSP-2472	HDSP-2000 Display Interface without ASCII Decoder. Instead, a 24 Pin Socket is Provided to Accept a Custom 128 Character Set from a User Programmed 1K x 8 PROM			
	HDSP-6300	3.56mm (.14") Eighteen Segment Eight Character Alphanumeric	26 Pin 15.2mm (.6") DIP	• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-held Instruments For further information ask for Application Note 931.	277
	HDSP-6504	3.8mm (.15") Sixteen Segment Four Character Alphanumeric	22 Pin 15.2mm (.6") DIP		282
	HDSP-6508	3.8mm (.15") Sixteen Segment Eight Character Alphanumeric	26 Pin 15.2mm (.6") DIP		

Alphanumeric LED Displays (Cont.)

Device		Description	Package	Application	Page No.
	HDSP-8716	Single-line 16 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	167.64mm (6.6")L x 58.42mm (2.3")H x 33mm (1.3")D	• Data Entry Terminals • Instrumentation • Electronic Typewriters	288
	HDSP-8724	Single-line 24 Character Alphanumeric Display System Utilizing the HDSP-6508 Display			
	HDSP-8732	Single-line 32 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	218.44mm (8.6")L x 58.42mm (2.3")H x 33mm (1.3")D		
	HDSP-8740	Single-line 40 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	269.24mm (10.6")L x 58.42mm (2.3") H x 33mm (1.3")D		
	5082-7100	7.4mm (.29") 5x7 Three Digit Alphanumeric	22 Pin Hermetic 15.2mm (.6") DIP	General Purpose Market • Business Machines • Calculators • Solid State CRT • High Reliability Applications For further information ask for Application Note 931 on Alphanumeric Displays.	300
	5082-7101	7.4mm (.29") 5x7 Four Digit Alphanumeric	28 Pin Hermetic 15.2mm (.6") DIP		
	5082-7102	7.4mm (.29") 5x7 Five Digit Alphanumeric	36 Pin Hermetic 15.2mm (.6") DIP		

SOLID STATE DISPLAYS

HEWLETT PACKARD

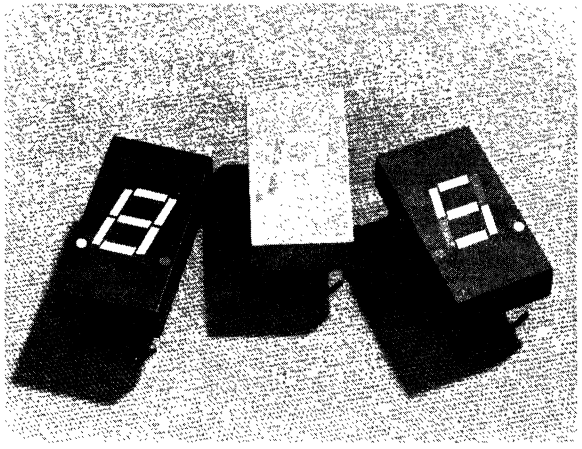
.3 INCH SEVEN SEGMENT DISPLAYS

HIGH EFFICIENCY RED · 5082-7610 SERIES
YELLOW · 5082-7620 SERIES
GREEN · 5082-7630 SERIES

TECHNICAL DATA MARCH 1980

Features

- **COMPACT SIZE**
- **CHOICE OF 3 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **LOW CURRENT OPERATION**
  - **As Low as 3mA per Segment**
  - **Designed for Multiplex Operation**
- **EXCELLENT CHARACTER APPEARANCE**
  - **Evenly Lighted Segments**
  - **Wide Viewing Angle**
  - **Body Color Improves "Off" Segment Contrast**
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  - **Industry Standard 7.62mm (.3 in.) DIP Leads on 2.54mm (.1 in.) Centers**
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  - **Use of Like Categories Yields a Uniform Display**
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The 5082-7610, -7620, and -7630 series are 7.62mm (.3 in.) High Efficiency Red, Yellow, and Green seven segment displays. These displays are designed for use in instruments, point of sale terminals, clocks, and appliances.

The -7610, and -7620 series devices utilize high efficiency LED chips which are made from GaAsP on a transparent GaP substrate.

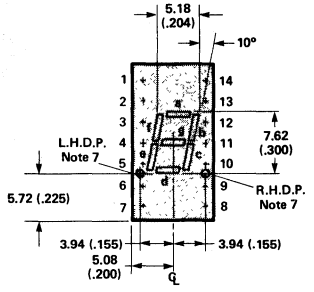
The -7630 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

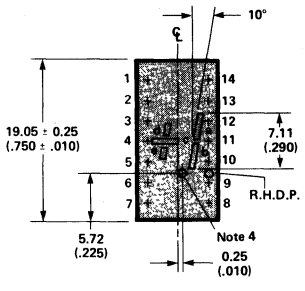
Part No. 5082-	Color	Description	Package Drawing
-7610	High Efficiency Red	Common Anode Left Hand Decimal	A
-7611	High Efficiency Red	Common Anode Right Hand Decimal	B
-7613	High Efficiency Red	Common Cathode Right Hand Decimal	C
-7616	High Efficiency Red	Universal Overflow ±1 Right Hand Decimal	D
-7620	Yellow	Common Anode Left Hand Decimal	A
-7621	Yellow	Common Anode Right Hand Decimal	B
-7623	Yellow	Common Cathode Right Hand Decimal	C
-7626	Yellow	Universal Overflow ±1 Right Hand Decimal	D
-7630	Green	Common Anode Left Hand Decimal	A
-7631	Green	Common Anode Right Hand Decimal	B
-7633	Green	Common Cathode Right Hand Decimal	C
-7636	Green	Universal Overflow ±1 Right Hand Decimal	D

NOTE: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram D.

Package Dimensions

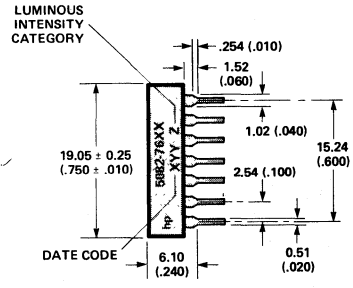


A,B,C

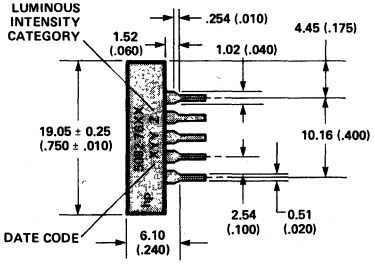


D

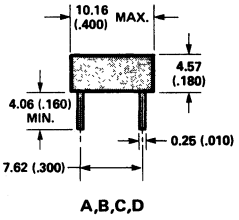
PIN	FUNCTION A 7610/-7620/-7630	B 7611/-7621/-7631	C 7613/-7623/-7633	D 7616/-7626/-7636
1	CATHODE-g	CATHODE-g	CATHODE-f	ANODE-g
2	CATHODE-f	CATHODE-f	ANODE-f	NO PIN
3	ANODE-(3)	ANODE-(3)	ANODE-a	CATHODE-g
4	NO PIN	NO PIN	ANODE-c	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-d
6	CATHODE-dp	NO CONNECTION	CATHODE-(3)	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-dp	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONNECTION	CATHODE-dp	ANODE-b	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-g	CATHODE-dp
11	CATHODE-b	CATHODE-b		CATHODE-b
12	NO PIN	NO PIN		CATHODE-a
13	CATHODE-a	CATHODE-a		ANODE-f
14	ANODE-(3)	ANODE-(3)		ANODE-b



A,B,D
SIDE



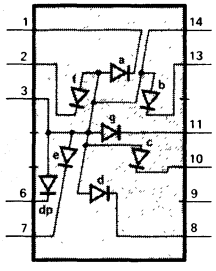
C
SIDE



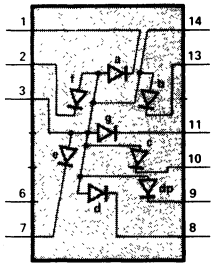
A,B,C,D
END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

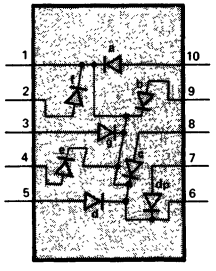
Internal Circuit Diagram



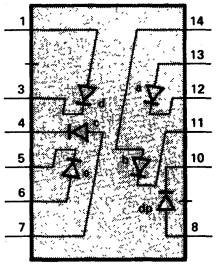
A



B



C



D

Absolute Maximum Ratings

Average Power Dissipation Per Segment or D.P.[1] (T_A=50°C) 81mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P.[3] (T_A=50°C) 60mA
Average Forward Current Per Segment or D.P.[1,2] (T_A = 50°C) 20mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig. 2). 2. Derate DC current from 50°C at 0.4mA/°C per segment. 3. See Fig. 1 to establish pulsed operating conditions. 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED 5082-7610/-7611/-7613/-7616

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	5mA D.C.	70	250		µcd
		20mA D.C.		1430		µcd
		60mA Pk: 1 of 6 Duty Factor		810		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength [6]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.7		V
		I_F = 20mA		2.0	2.5	
		I_F = 60mA		2.8		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		µA
Response Time [8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

YELLOW 5082-7620/-7621/-7623/-7626

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	5mA D.C.	90	200		µcd
		20mA D.C.		1200		µcd
		60mA Pk: 1 of 6 Duty Factor		740		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength [6,7]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.8		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		3.1		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		µA
Response Time [8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	V_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

GREEN 5082-7630/-7631/-7633/-7636

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	10mA D.C.	150	300		µcd
		20mA D.C.		765		µcd
		60mA Pk: 1 of 6 Duty Factor		540		µcd
Peak Wavelength	λ_{PEAK}			565		nm
Dominant Wavelength [6,7]	λ_d			572		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.9		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		2.9		
Reverse Current/Segment or D.P.	I_F	V_R = 6V		10		µA
Response Time [8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

NOTES: 5. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
6. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
7. The 5082-7620/-7630 series yellow/green displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
8. Time for a 10% — 90% change of light intensity for step change in current.

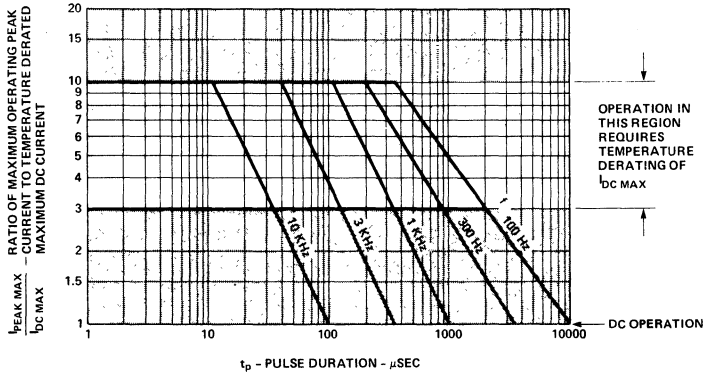


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

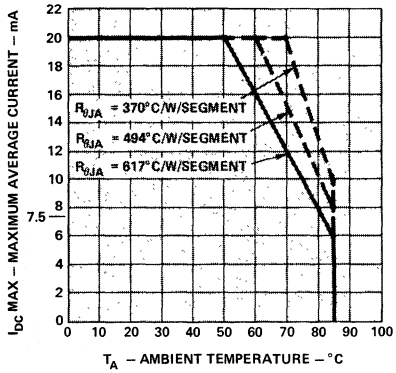


Figure 2. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature.

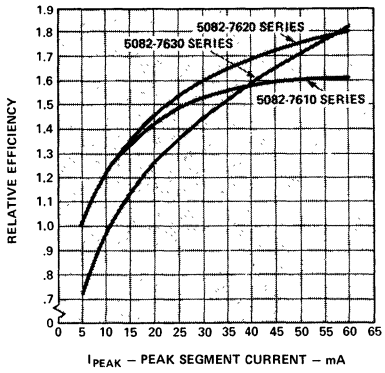


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

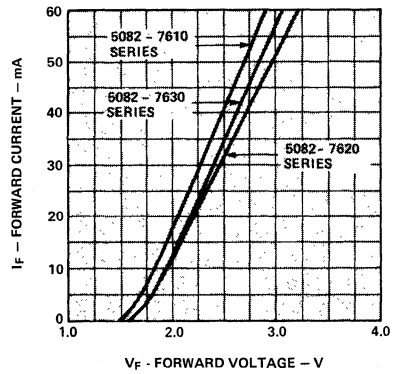


Figure 4. Forward Current vs. Forward Voltage Characteristic.

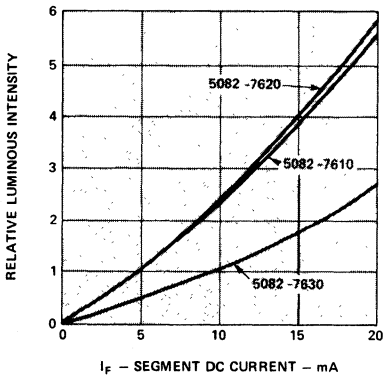


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

ELECTRICAL

The 5082-7600 series of display products are arrays of eight light emitting diodes which are optically magnified to form seven individual segments plus a decimal point.

The diodes in these displays utilize a Gallium Arsenide Phosphide junction on a Gallium Phosphide substrate to produce high efficiency red and yellow emission spectra and a Gallium Phosphide junction for the green.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models.

$V_F = 1.75V + I_{PEAK}\ (38\Omega)$
For $I_{PEAK} \geq 20mA$

$V_F = 1.60V + I_{DC}\ (45\Omega)$
For $5mA \leq I_{DC} \leq 20mA$

All of the colored display products should be used in conjunction with contrast enhancing filters. Some suggested contrast filters: for red displays, Panelgraphic Scarlet Red 65 or Homalite 1670; for yellow displays, Panelgraphic Yellow 27 or Homalite (100-1720, 100-1726); for green, Panelgraphic Green 48 or Homalite (100-1440, 100-1425). Another excellent contrast enhancement material for all colors is the 3M light control film.

HEWLETT PACKARD

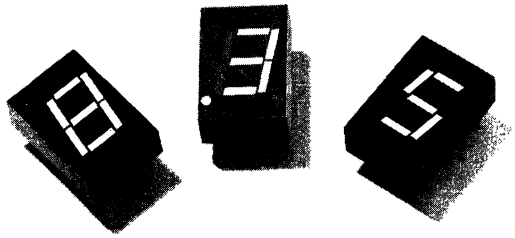
.43 INCH SEVEN SEGMENT DISPLAYS

HIGH EFFICIENCY RED • 5082-7650 SERIES
YELLOW • 5082-7660 SERIES
GREEN • 5082-7670 SERIES

TECHNICAL DATA MARCH 1980

Features

- **LARGE DIGIT**
  Viewing up to 6 meters (19.7 feet)
- **CHOICE OF 3 BRIGHT COLORS**
  High Efficiency Red
  Yellow
  Green
- **LOW CURRENT OPERATION**
  As Low as 3mA per Segment
  Designed for Multiplex Operation
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Body Color Improves "Off" Segment Contrast
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 7.62mm (.3") DIP Leads on 2.54mm (.1") Centers
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The 5082-7650, -7660, and -7670 series are large 10.92mm (.43 in.) Red, Yellow, and Green seven segment displays. These displays are designed for use in instruments, point of sale terminals, clocks, and appliances.

The -7650 and -7660 series devices utilize high efficiency LED chips which are made from GaAsP on a transparent GaP substrate.

The -7670 series devices utilize chips made from GaP on a transparent GaP substrate.

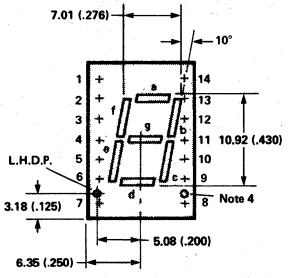
SOLID STATE DISPLAYS

Devices

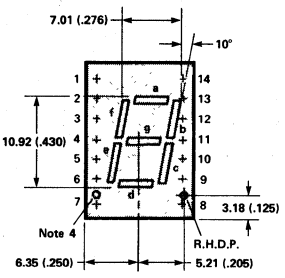
Part No. 5082-	Color	Description	Package Drawing
-7650	High Efficiency Red	Common Anode Left Hand Decimal	A
-7651	High Efficiency Red	Common Anode Right Hand Decimal	B
-7653	High Efficiency Red	Common Cathode Right Hand Decimal	C
-7656	High Efficiency Red	Universal Overflow ±1 Right Hand Decimal	D
-7660	Yellow	Common Anode Left Hand Decimal	A
-7661	Yellow	Comon Anode Right Hand Decimal	B
-7663	Yellow	Common Cathode Right Hand Decimal	C
-7666	Yellow	Universal Overflow ±1 Right Hand Decimal	D
-7670	Green	Common Anode Left Hand Decimal	A
-7671	Green	Common Anode Right Hand Decimal	B
-7673	Green	Common Cathode Right Hand Decimal	C
-7676	Green	Universal Overflow ±1 Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins, see internal diagram D.

Package Dimensions

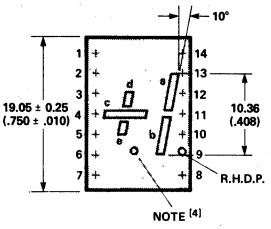


A

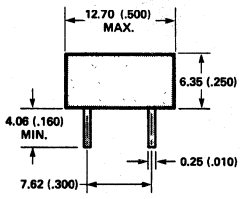


B,C

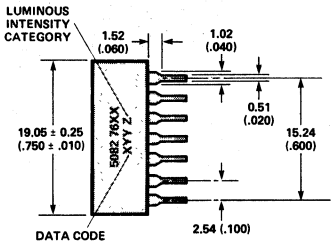
FRONT VIEW



D



END VIEW



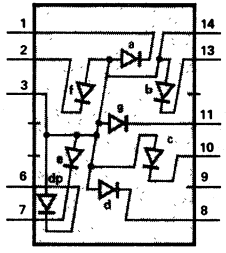
SIDE VIEW

PIN	FUNCTION			
	A -7650/-7660/ -7670	B -7651/-7661/ -7671	C -7653/-7663/ -7673	D -7656/-7666/ -7676
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

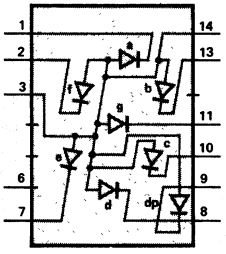
NOTES:

1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.

Internal Circuit Diagram



A



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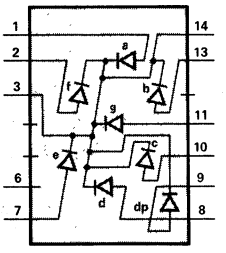

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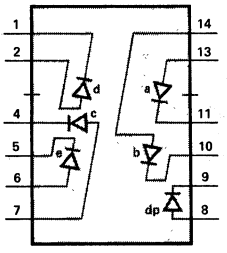


D

Absolute Maximum Ratings

Average Power Dissipation Per Segment or D.P.[1] (T_A=50°C) 81mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P[3] (T_A=50°C) 60mA
DC Forward Current Per Segment or D.P.[1,2] (T_A=50°C) 20mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate average current from 50° C at 0.4mA/° C per segment. 3. See Maximum Tolerable Segment Peak Current vs. Pulse Duration curve, (Fig. 1). 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED 5082-7650/-7651/-7653/-7656

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5] (Digit Average)	I_v	5mA D.C.	135	300		µcd
		20mA D.C.		1720		µcd
		60mA Pk: 1 of 6 Duty Factor		970		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[6]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.7		V
		I_F = 20mA		2.0	2.5	
		I_F = 60mA		2.8		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		µA
Response Time[8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

YELLOW 5082-7660/-7661/-7663/-7666

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5] (Digit Average)	I_v	5mA D.C.	100	250		µcd
		20mA D.C.		1500		µcd
		60mA Pk: 1 of 6 Duty Factor		925		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[6,7]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.8		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		3.1		
Reverse Current/Segment or D.P.	I_R	V_R = 6V				µA
Response Time[8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	V_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

GREEN 5082-7670/-7671/-7673/-7676

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5] (Digit Average)	I_v	10mA D.C.	125	250		µcd
		20mA D.C.		640		µcd
		60mA Pk: 1 of 6 Duty Factor		450		µcd
Peak Wavelength	λ_{PEAK}			565		nm
Dominant Wavelength[6,7]	λ_d			572		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 10mA		1.9		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		2.9		
Reverse Current/Segment or D.P.	I_F	V_R = 6V		10		µA
Response Time[8]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

NOTES:
5. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
6. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is the single wavelength which defines the color of the device.
7. The 5082-7660/-7670 series yellow/green displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
8. Time for a 10%-90% change of light intensity for step change in current.

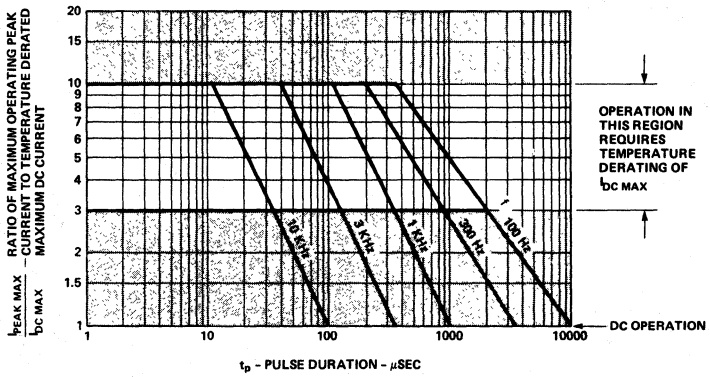


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

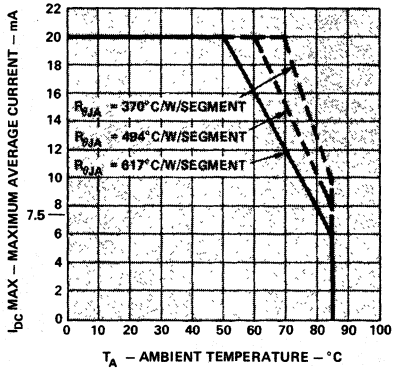


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. T_J MAX=100°C

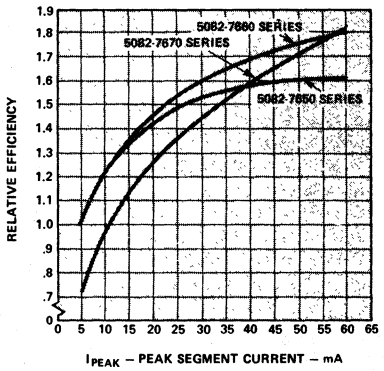


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

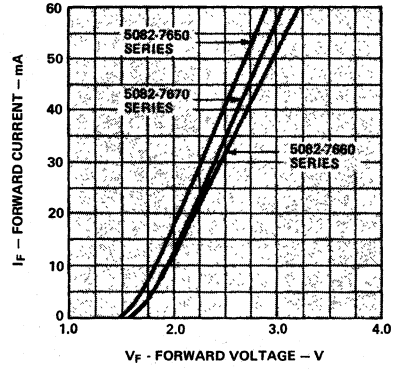


Figure 4. Forward Current vs. Forward Voltage Characteristic.

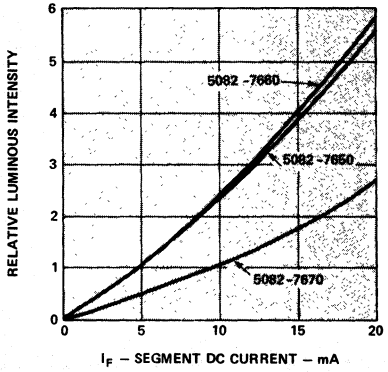


Figure 5. Relative Luminous Intensity vs. DC Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

ELECTRICAL

The 5082-7600 series of display products are arrays of eight light emitting diodes which are optically magnified to form seven individual segments plus a decimal point.

The diodes in these displays utilize a Gallium Arsenide Phosphide junction on a Gallium Phosphide substrate to produce high efficiency red and yellow emission spectra and a Gallium Phosphide junction for the green.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$V_F = 1.75V + I_{PEAK}\ (38\Omega)$
For $I_{PEAK} \geq 20mA$

$V_F = 1.60V + I_{DC}\ (45\Omega)$
For $5mA \leq I_{DC} \leq 20mA$

All of the colored display products should be used in conjunction with contrast enhancing filters. Some suggested contrast filters: for red displays, Panelgraphic Scarlet Red 65 or Homalite 1670; for yellow displays, Panelgraphic Amber 23 or Homalite (100-1720, 100-1726); for green, Panelgraphic Green 48 or Homalite (100-1440, 100-1425). Another excellent contrast enhancement material for all colors is the 3M light control film.

HEWLETT PACKARD

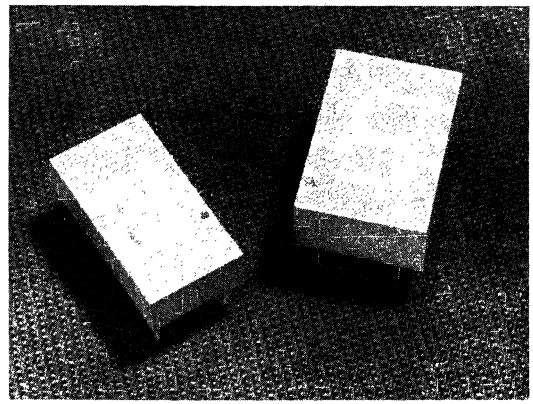
7.6/10.9 mm (0.3/0.43 INCH) SEVEN SEGMENT DISPLAYS FOR HIGH LIGHT AMBIENT CONDITIONS

HIGH EFFICIENCY RED · HDSP-3530/3730 SERIES
YELLOW · HDSP-4030/4130 SERIES

TECHNICAL DATA MARCH 1980

Features

- **HIGH LIGHT OUTPUT**
  Typically 2300 μcd/Segment at 100mA Peak, 20mA Average
  Designed for Multiplex Operation
- **CHOICE OF TWO COLORS**
  High Efficiency Red
  Yellow
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Gray Body Color for Optimum Contrast
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 7.62mm (0.3 in.) DIP Leads on 2.54mm (0.1 in.) Centers
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The HDSP-3530/4030 and -3730/4130 series are 7.62/10.92mm (0.3/0.43 in.) high efficiency red and yellow displays designed for use in high light ambient conditions. These displays are designed for use in instruments, airplane cockpits, weighing scales, and point of sale terminals.

The HDSP-3530/4030 and -3730/4130 series devices utilize high efficiency LED chips, which are made from GaAsP on a transparent GaP substrate. The active junction area is larger than that used in the 5082-7610/7620/7650/7660 series to permit higher peak currents.

Devices

Part No. HDSP-	Color	Description	Package Drawing
3530	High Efficiency Red	7.6mm Common Anode Left Hand Decimal	A
3531	High Efficiency Red	7.6mm Common Anode Right Hand Decimal	B
3533	High Efficiency Red	7.6mm Common Cathode Right Hand Decimal	C
3536	High Efficiency Red	7.6mm Universal Overflow ±1 Right Hand Decimal	D
4030	Yellow	7.6mm Common Anode Left Hand Decimal	A
4031	Yellow	7.6mm Common Anode Right Hand Decimal	B
4033	Yellow	7.6mm Common Cathode Right Hand Decimal	C
4036	Yellow	7.6mm Universal Overflow ±1 Right Hand Decimal	D
3730	High Efficiency Red	10.9mm Common Anode Left Hand Decimal	E
3731	High Efficiency Red	10.9mm Common Anode Right Hand Decimal	F
3733	High Efficiency Red	10.9mm Common Cathode Right Hand Decimal	G
3736	High Efficiency Red	10.9mm Universal Overflow ±1 Right Hand Decimal	H
4130	Yellow	10.9mm Common Anode Left Hand Decimal	E
4131	Yellow	10.9mm Common Anode Right Hand Decimal	F
4133	Yellow	10.9mm Common Cathode Right Hand Decimal	G
4136	Yellow	10.9mm Universal Overflow ±1 Right Hand Decimal	H

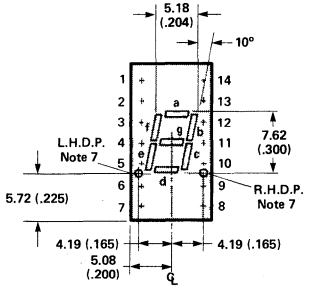
Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams D and H.

Absolute Maximum Ratings (All Products)

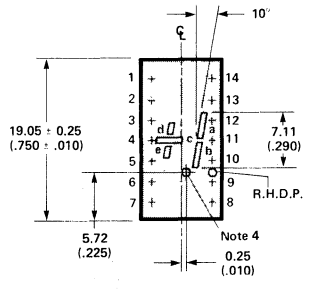
Average Power Dissipation Per Segment or DP (T_A=50° C) 85mW
Operating Temperature Range ..... -40° C to +85° C
Storage Temperature Range ..... -40° C to +85° C
Peak Forward Current Per Segment or DP (T_A = 50° C)[2] 120mA
(Pulse Width = 1.25ms)
DC Forward Current Per Segment or DP (T_A=50° C)[1] 30mA
Reverse Voltage Per Segment or DP 6.0V
Lead Soldering Temperature (1.6mm [1/16 inch] below seating plane) ..... 260° C for 3 Seconds

Notes: 1. Derate maximum DC current above T_A=50° C at 0.51 mA/° C per segment, see Figure 2. 2. See Figure 1 to establish pulsed operating conditions.

Package Dimensions (HDSP-3530/4030 Series)

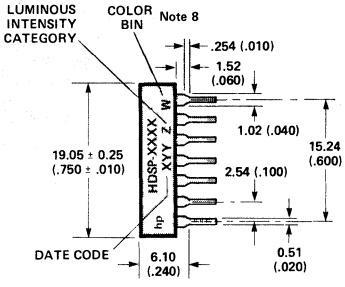


A,B,C

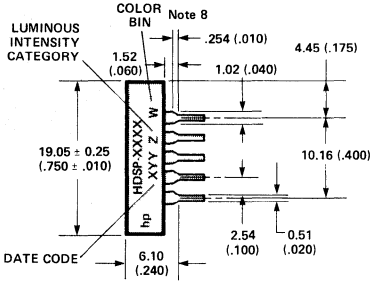


D

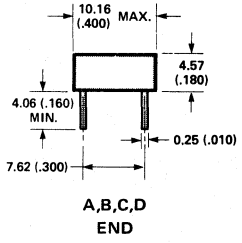
PIN	FUNCTION A -3530/-4030	B -3531/-4031	C -3533/-4033	D -3536/-4036
1	CATHODE-a	CATHODE-a	CATHODE[6]	ANODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-g	CATHODE-d
4	NO PIN	NO PIN	ANODE-e	CATHODE-c
5	NO PIN	NO PIN	ANODE-d	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	CATHODE[6]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-dp	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-c	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-b	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-a	CATHODE-dp
11	CATHODE-g	CATHODE-g		CATHODE-b
12	NO PIN	NO PIN		CATHODE-a
13	CATHODE-b	CATHODE-b		ANODE-a
14	ANODE[3]	ANODE[3]		ANODE-b



A,B,D SIDE



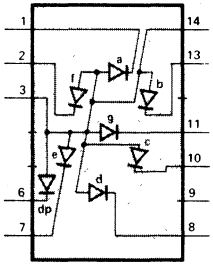
C SIDE



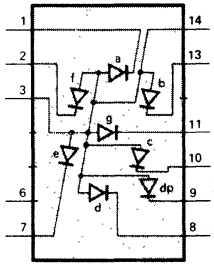
A,B,C,D END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.
8. For HDSP-4030 series product only.

Internal Circuit Diagram (HDSP-3530/4030 Series)



A



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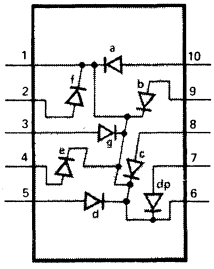

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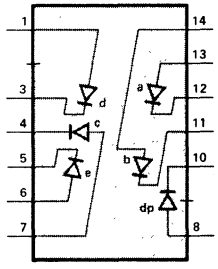
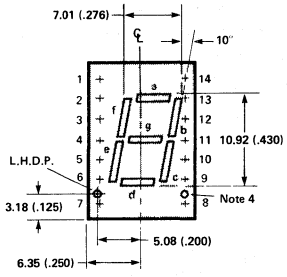
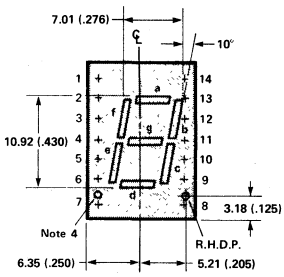


D

Package Dimensions (HDSP-3730/4130 Series)

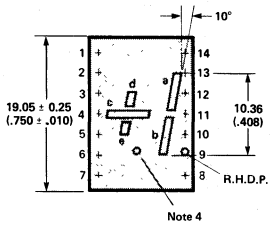


E

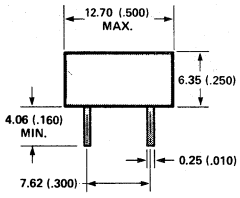


F,G

FRONT VIEW

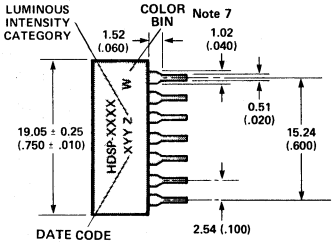


H



E, F, G, H

END VIEW



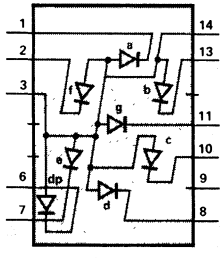
E, F, G, H

SIDE VIEW

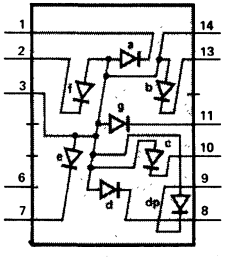
PIN	FUNCTION			
	E -3730/-4130	F -3731/-4131	G -3733/-4133	H -3736/-4136
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram
6. Redundant cathode.
7. For HDSP-4130 series product only.

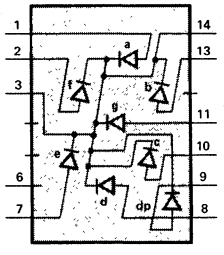
Internal Circuit Diagram (HDSP-3730/4130 Series)



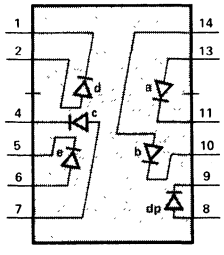
E



F



G



H

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED HDSP-3530/-3531/-3533/-3536/-3730/-3731/-3733/-3736

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3]	I_V	100mA Pk: 1 of 5 Duty Factor	1000	2300		μcd
(Digit Average)		20mA DC		1800		μcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[4]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 100mA		2.55	3.3	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time, Rise and Fall[6]	t_r, t_f			300		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C	I_F = 100mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

YELLOW HDSP-4030/-4031/-4033/-4036/-4130/-4131/-4133/-4136

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3]	I_V	100mA Pk: 1 of 5 Duty Factor	1000	2700		μcd
(Digit Average)		20mA DC		2100		μcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[4,5]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 100mA		2.6	3.3	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time, Rise and Fall[6]	t_r, t_f			200		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C	I_F = 100mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

NOTES:
3. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
5. The HDSP-4030/-4130 series yellow displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
6. The rise and fall times are for a 10%-90% change of light intensity to a step change in current.

ELECTRICAL

The HDSP-3530/3730/4030/4130 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have a large area P-N junction diffused into a GaAsP epitaxial layer on a GaP transparent substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$V_F = 2.15V + I_{PEAK}\ (11.5\Omega)$

For $I_{PEAK} \geq 30mA$

$V_F = 1.9V + I_{DC}\ (19.8\Omega)$

For $10mA \leq I_{DC} \leq 30mA$

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. To most effectively use Figures 1 and 2, perform the following steps:

1. Determine desired duty factor, DF.
   Example: Five digits, DF = 1/5
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_p. Note: DF = f·t_p.
   Example: f = 1 kHz, t_p = 200 μs
3. Enter Figure 1 at the calculated t_p. Move vertically to the refresh rate line and record the corresponding value of I_{PEAK} MAX/I_{DC} MAX.
   Example: At t_p = 200μs and f = 1 kHz, I_{PEAK} MAX/I_{DC} MAX = 4.0
4. From Figure 2, determine I_{DC} MAX. Note: I_{DC} MAX is derated above T_A = 50°C.
   Example: At T_A = 60°C, I_{DC} MAX = 25mA
5. Calculate I_{PEAK} MAX from I_{PEAK} MAX/I_{DC} MAX ratio and calculate I_{AVG} from I_{PEAK} MAX and DF.
   Example: I_{PEAK} MAX = (4.0) (25mA) = 100mA peak. I_{AVG} = (1/5) (100mA) = 20mA average.

The above calculations determine the maximum allowed strobing conditions. Operation at a reduced peak current and/or pulse width may be desirable to adjust display light output to match ambient light level or to reduce power dissipation to insure even more reliable operation.

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, η_{IPEAK}, and adjusted for operating ambient temperature. The time average luminous intensity at T_A=25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right]\left[\eta_{IPEAK}\right]\left[I_{V\ DATA\ SHEET}\right]$$

Example: For HDSP-4030 series

η_{IPEAK} = 1.00 at I_{PEAK} = 100mA

$$I_{V\ TIME\ AVG} = \left[\frac{20mA}{20mA}\right]\left[1.00\right]\left[2.7mcd\right] = 2.7mcd/segment$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V(T_A) = I_V(25°C)\, e^{[K\,(T_A - 25°C)]}$$

Device	K
-3530/3730 Series	-0.0131/°C
-4030/4130 Series	-0.0112/°C

Example: I_V (70°C) = (2.7mcd) $e^{[-0.0112\,(70-25)]}$ = 1.63mcd/segment

MECHANICAL

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 320° C/W per segment. This will then establish a maximum thermal resistance LED junction-to-ambient of 602°C/W per segment.

These display devices may be operated in ambient temperatures above +50°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 602°C/W/Segment. See Figure 6 to determine the maximum allowed thermal resistance for the PC board, $R_{\theta PC-A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

CONTRAST ENHANCEMENT

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and have the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and untinted encapsulating epoxy in the segments.

Contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10. Additional contrast enhancement may be achieved by using the neutral density 3M Light Control Film (louvered filter).

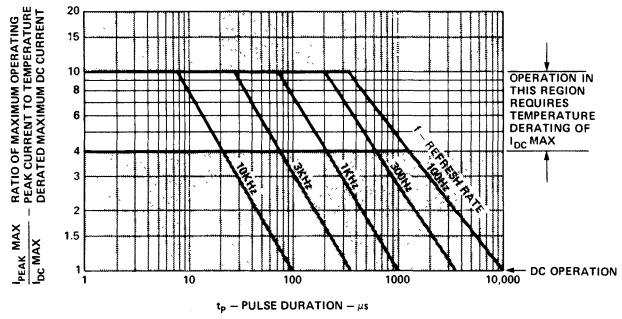


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration.

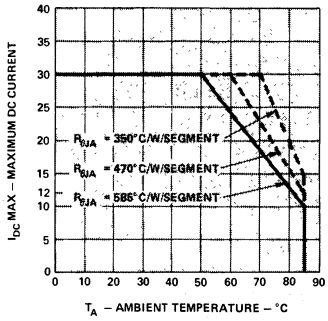


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. T_JMAX-100°C.

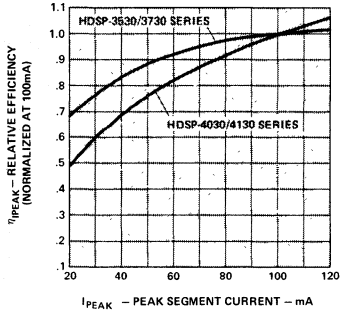


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

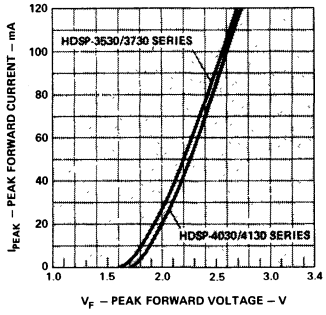


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

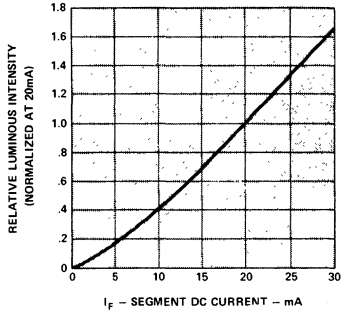


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

HEWLETT PACKARD

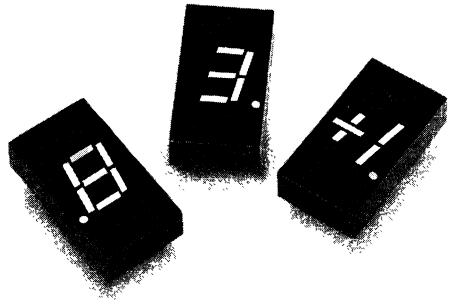
0.3 INCH RED SEVEN SEGMENT DISPLAY

5082-7730 SERIES 5082-7740

TECHNICAL DATA MARCH 1980

Features

- **5082-7730**
  Common Anode
  Left Hand D.P.
- **5082-7731**
  Common Anode
  Right Hand D.P.
- **5082-7736**
  Polarity and Overflow Indicator
  Universal Pinout
  Right Hand D.P.
- **5082-7740**
  Common Cathode
  Right Hand D.P.
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Uniform Segments
  Wide Viewing Angle
  High Contrast
- **IC COMPATIBLE**
  1.6V dc per Segment
- **STANDARD 0.3" DIP LEAD CONFIGURATION**
  PC Board or Standard Socket Mountable
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7730/7740 series devices are common anode LED displays. The series includes a left hand and a right hand decimal point numeric display as well as a polarity and overflow indicator. The large 7.62 mm (0.3 in.) high character size generates a bright, continuously uniform seven segment display. Designed for viewing distances of up to 3 meters (9.9 feet), these single digit displays provide a high contrast ratio and a wide viewing angle.

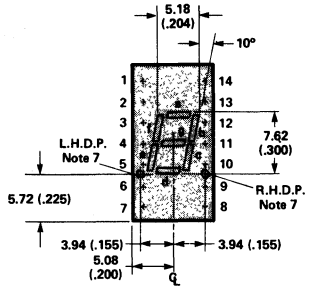
The 5082-7730 series devices utilize a standard 7.62 mm (0.3 in.) dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point of sale terminals, TVs, radios, and digital clocks.

Devices

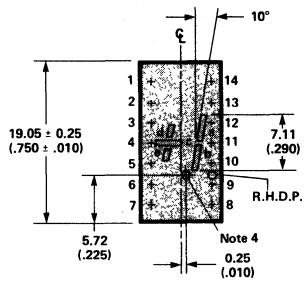
Part No. 5082-	Description	Package Drawing
7730	Common Anode Left Hand Decimal	A
7731	Common Anode Right Hand Decimal	B
7736	Universal Overflow ±1 Right Hand Decimal	C
7740	Common Cathode Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram C.

Package Dimensions

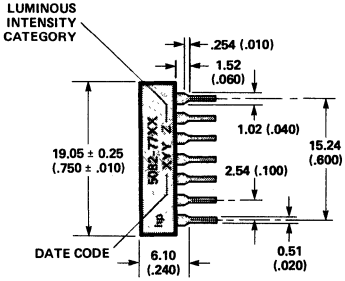


A,B,D

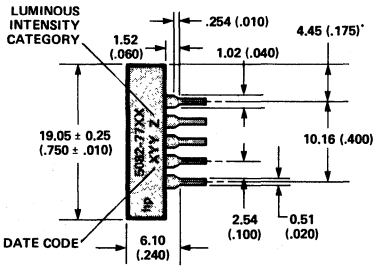


C

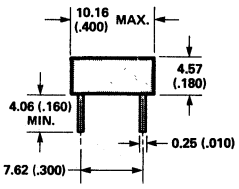
PIN	FUNCTION A 7730	B 7731	C 7739	D 7740
1	CATHODE-e	CATHODE-a	ANODE-d	CATHODE[6]
2	CATHODE-f	CATHODE-f	NO PIN	ANODE-f
3	ANODE[3]	ANODE[3]	CATHODE-d	ANODE-g
4	NO PIN	NO PIN	CATHODE-c	ANODE-e
5	NO PIN	NO PIN	CATHODE-e	ANODE-d
6	CATHODE-dp	NO CONN.[5]	ANODE-a	CATHODE[6]
7	CATHODE-a	CATHODE-e	ANODE-c	ANODE-dp
8	CATHODE-d	CATHODE-d	ANODE-dp	ANODE-c
9	NO CONN.[5]	CATHODE-dp	NO PIN	ANODE-b
10	CATHODE-c	CATHODE-c	CATHODE-dp	ANODE-a
11	CATHODE-g	CATHODE-g	CATHODE-b	
12	NO PIN	NO PIN	CATHODE-a	
13	CATHODE-b	CATHODE-b	ANODE-a	
14	ANODE[3]	ANODE[3]	ANODE-b	



A,B,C SIDE



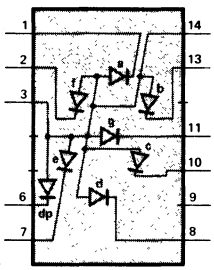
D SIDE



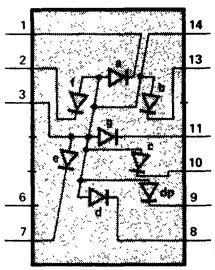
A,B,C,D END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

Internal Circuit Diagram



A



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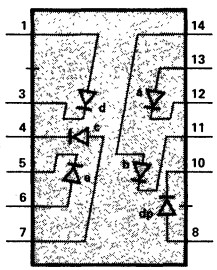
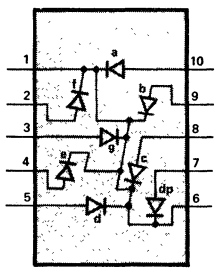


C



D

Absolute Maximum Ratings

Average Power Dissipation Per Segment or D.P.[1] (T_A=50°C)	65mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Peak Forward Current Per Segment or D.P.[3] (T_A=50°C)	150mA
Average Forward Current Per Segment or D.P.[1,2] (T_A=50°C)	25mA
Reverse Voltage Per Segment or D.P.	6.0V
Lead Soldering Temperature [1.59mm (1/16 inch) below seating plane[4]]	260°C for 3 Sec

Notes: 1. See power derating curve (Fig.2). 2. Derate DC current from 50°C at 0.43mA/°C per segment. 3. See Fig. 1 to establish pulsed operating conditions. 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [2] (Digit Average)	I_V	I_{PEAK} = 100mA 10% Duty Cycle		200		µcd
		I_F = 20mA	100	350		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [2]	λ_d			640		nm
Forward Voltage, any Segment or D.P.	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or D.P.	I_R	V_R = 6V		10		µA
Rise and Fall Time [3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.

ELECTRICAL

The HDSP-7730/7740 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have the P-N junction diffused into a GaAsP epitaxial layer on a GaAs substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.55V + I_{PEAK}\ (7\Omega)$
For $5mA \leq I_{PEAK} \leq 150mA$

CONTRAST ENHANCEMENT

The 5082-7730/7740 series display may be effectively filtered using one of the following filter products: Homalite H100-1605: H 100-1804 (purple); Panelgraphic Ruby Red 60: Dark Red 63: Purple 90; Plexiglas 2423; 3M Brand Light Control Film for daylight viewing.

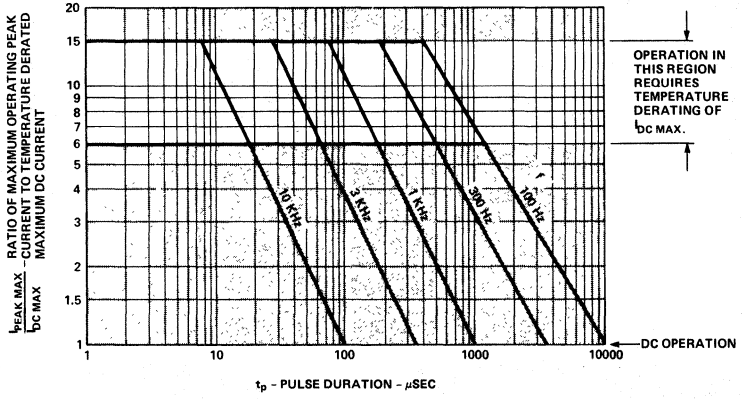


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

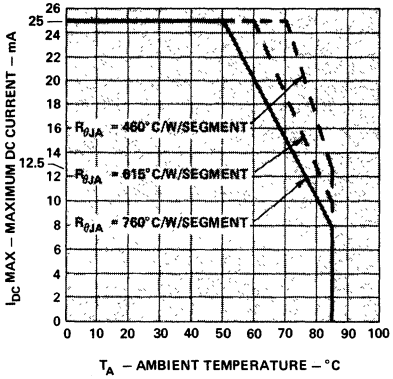


Figure 2. Maximum Allowable DC Current Dissipation per Segment as a Function of Ambient Temperature.

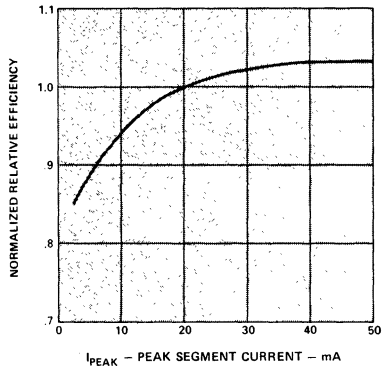


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

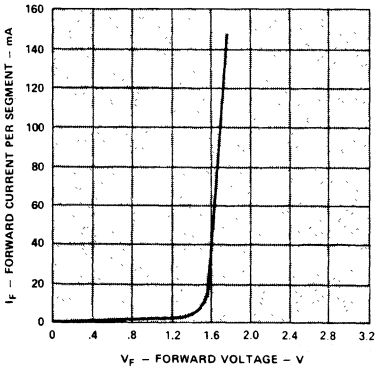


Figure 4. Forward Current vs. Forward Voltage.

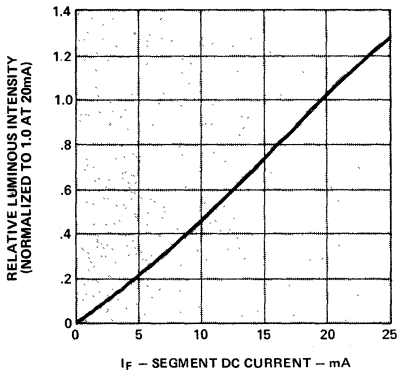


Figure 5. Relative Luminous Intensity vs. DC Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

HEWLETT PACKARD

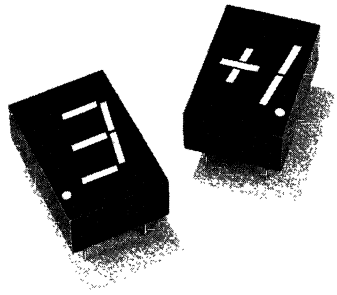
.43 INCH RED SEVEN SEGMENT DISPLAY

5082-7750 SERIES 5082-7760

TECHNICAL DATA MARCH 1980

Features

- **5082-7750**
  Common Anode
  Left Hand D.P.
- **5082-7751**
  Common Anode
  Right Hand D.P.
- **5082-7756**
  Polarity and Overflow Indicator
  Universal Pinout
  Right Hand D.P.
- **5082-7760**
  Common Cathode
  Right Hand D.P.
- **LARGE DIGIT**
  Viewing Up to 6 Meters (19.7 Feet)
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Uniform Segments
  Wide Viewing Angle
  High Contrast
- **IC COMPATIBLE**
- **STANDARD 7.62mm (.3 in.) DIP LEAD CONFIGURATION**
  PC Board or Standard Socket Mountable
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The 5082-7750/7760 series are large 10.92mm (.43 in.) GaAsP LED seven segment displays. Designed for viewing distances up to 6 meters (19.7 feet), these single digit displays provide a high contrast ratio and a wide viewing angle.

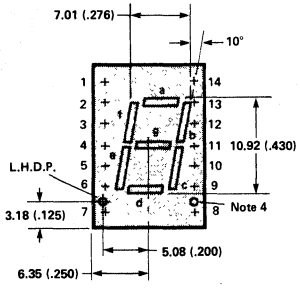
These devices utilize a standard 7.62mm (.3 in.) dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point of sale terminals, TVs, radios, and digital clocks.

Devices

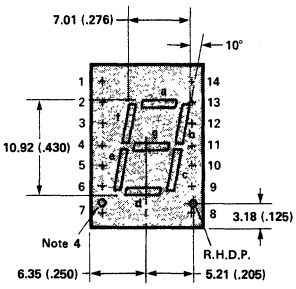
Part No. 5082-	Description	Package Drawing
–7750	Common Anode Left Hand Decimal	A
–7751	Common Anode Right Hand Decimal	B
–7756	Universal Overflow ±1 Right Hand Decimal	C
–7760	Common Cathode Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram C.

Package Dimensions

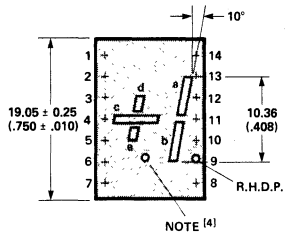


A

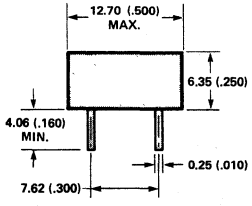


B,D

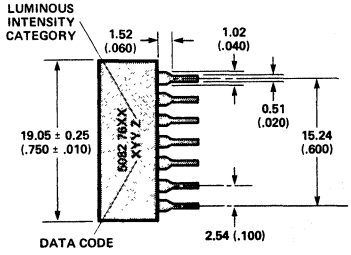
FRONT VIEW



C



END VIEW

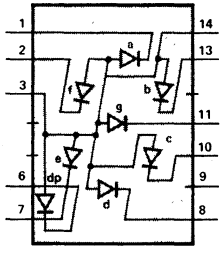


SIDE VIEW

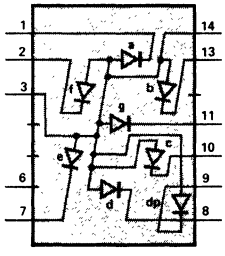
PIN	FUNCTION A -7750	B -7751	C -7756	D -7760
1	CATHODE-a	CATHODE-a	CATHODE-d	ANODE-a
2	CATHODE-f	CATHODE-f	ANODE-d	ANODE-f
3	ANODE[3]	ANODE[3]	NO PIN	CATHODE[6]
4	NO PIN	NO PIN	CATHODE-c	NO PIN
5	NO PIN	NO PIN	CATHODE-e	NO PIN
6	CATHODE-dp	NO CONN.[5]	ANODE-e	NO CONN.[5]
7	CATHODE-e	CATHODE-e	ANODE-c	ANODE-e
8	CATHODE-d	CATHODE-d	ANODE-dp	ANODE-d
9	NO CONN.[5]	CATHODE-dp	CATHODE-dp	ANODE-dp
10	CATHODE-c	CATHODE-c	CATHODE-b	ANODE-c
11	CATHODE-g	CATHODE-g	CATHODE-a	ANODE-g
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-b
14	ANODE[3]	ANODE[3]	ANODE-b	CATHODE[6]

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathodes.

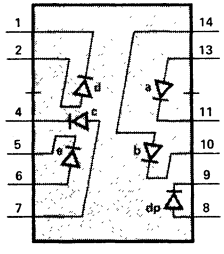
Internal Circuit Diagram



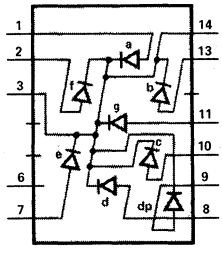
A



B



C



D

Absolute Maximum Ratings

Average Power Dissipation Per Segment or D.P.[1] (T_A=50°C)	65mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Peak Forward Current Per Segment or D.P[3] (T_A=50°C)	150mA
DC Forward Current Per Segment or D.P.[1,2] (T_A=50°C)	25mA
Reverse Voltage Per Segment or D.P.	6.0V
Lead Soldering Temperature	260°C for 3 Sec
	[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate average current from 50°C at 0.43mA/°C per segment. 3. See Maximum Tolerable Segment Peak Current vs. Pulse Duration curve, (Fig. 1). 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [2] (Digit Average)	I_V	I_{PEAK} = 100mA 12.5% Duty Cycle		350		μcd
		I_F = 20mA	150	400		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [2]	λ_d			645		nm
Forward Voltage, any Segment or D.P.	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or D.P.	I_R	V_R = 6V		10		μA
Rise and Fall Time [3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

Notes:

1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.

ELECTRICAL

The HDSP-7750/-7760 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have the P-N junction diffused into a GaAsP epitaxial layer on a GaAs substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.55V + I_{PEAK}\ (7\Omega)$
For $5mA \leq I_{PEAK} \leq 150mA$

CONTRAST ENHANCEMENT

The 5082-7750/7760 series display may be effectively filtered using one of the following filter products: Homalite H 100-1605 or H 100-1804 Purple; Panelgraphic Ruby Red 60, Dark Red 63 or Purple 90; Plexiglas 2423; 3M Brand Light Control Film for daylight viewing.

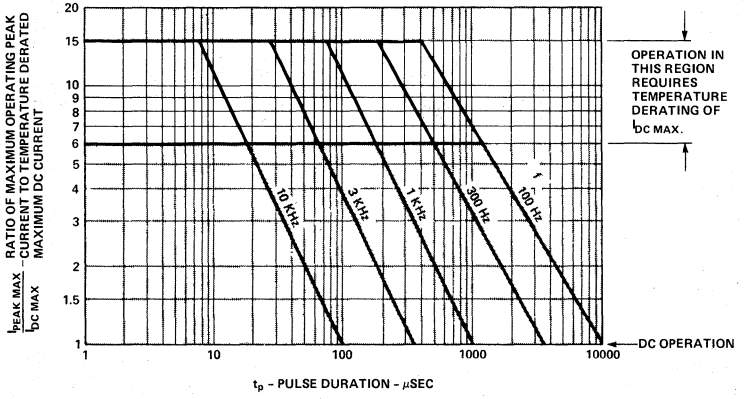


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

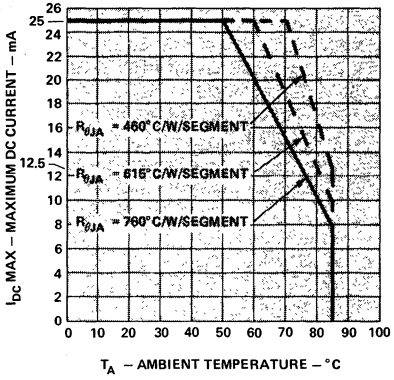


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. T_JMAX=100°C

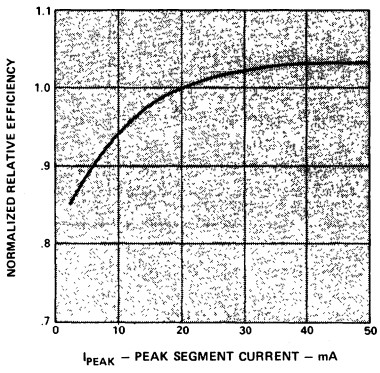


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

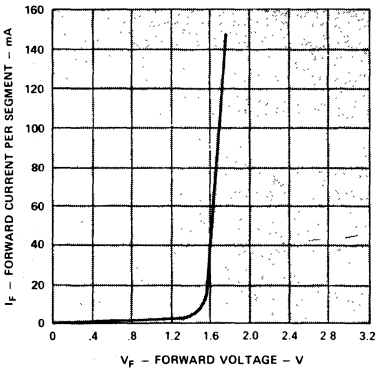


Figure 4. Forward Current versus Forward Voltage.

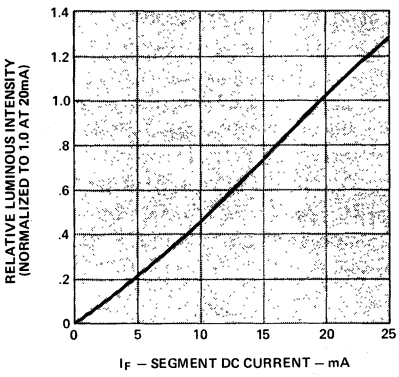


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

HEWLETT PACKARD

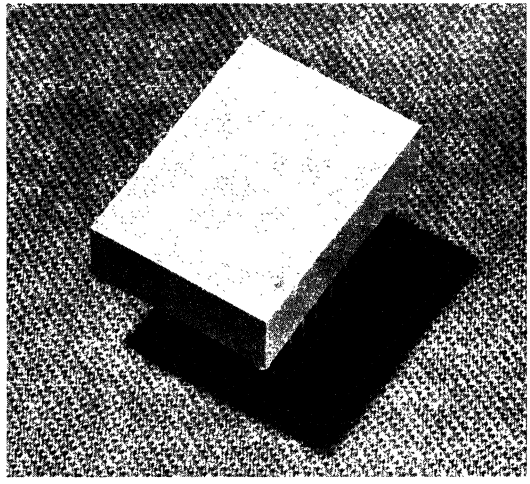
20mm (0.8") RED SEVEN SEGMENT DISPLAY

HDSP-3400 SERIES

TECHNICAL DATA MARCH 1980

Features

- **20mm (0.8") DIGIT HEIGHT**
  Viewing Up to 10 Metres (33 Feet)
- **EXCELLENT CHARACTER APPEARANCE**
  Excellent Readability in Bright Ambients Through Superior Contrast Enhancement
  — Gray Body Color
  — Untinted Segments
  Wide Viewing Angle
  Evenly Lighted Segments
  Mitered Corners on Segments
- **LOW POWER REQUIREMENTS**
  Single GaAsP Chip per Segment
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 15.24mm (0.6") DIP with Lead Spacing on 2.54mm (0.1") Centers
  Industry Standard Package Dimensions and Pinouts
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit Within a Single Category
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The HDSP-3400 Series are very large 20.32mm (0.8 in.) GaAsP LED seven segment displays. Designed for viewing distances up to 10 metres (33 feet), these single digit displays provide excellent readability in bright ambients.

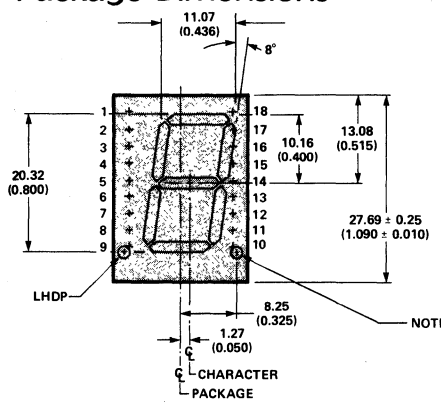
These devices utilize a standard 15.24mm (0.6 in.) dual in line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point-of-sale terminals, TVs, weighing scales, and digital clocks.

Devices

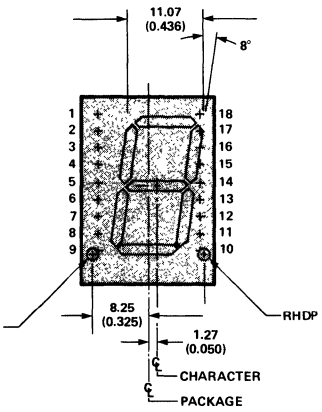
Part No. HDSP	Description	Package Drawing
-3400	Common Anode Left Hand Decimal	A
-3401	Common Anode Right Hand Decimal	B
-3403	Common Cathode Right Hand Decimal	C
-3405	Common Cathode Left Hand Decimal	D
-3406	Universal Overflow ±1 Right Hand Decimal	E

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram E.

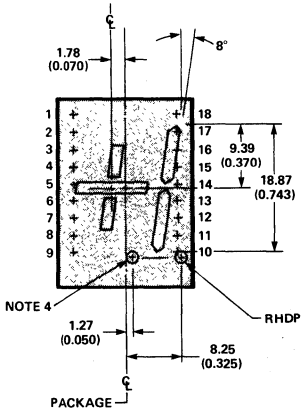
Package Dimensions



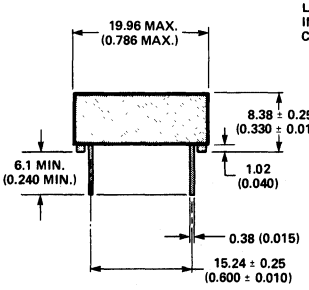
FRONT VIEW A,D



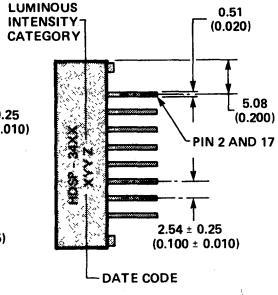
FRONT VIEW B,C



FRONT VIEW E



END VIEW

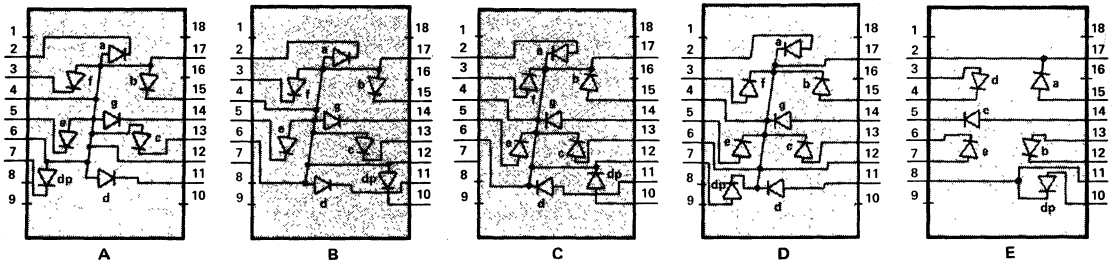


SIDE VIEW

Pin	Function A -3400	B -3401	C -3403	D -3405	E -3406
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE a	CATHODE a	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO CONNEC	NO CONNEC	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. Dimensions in millimetres and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathodes.

Internal Circuit Diagram



Absolute Maximum Ratings

Average Power Dissipation per Segment or DP ($T_A = 50°C$)[1] 100mW
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -20°C to +85°C
Peak Forward Current per Segment or DP ($T_A = 50°C$, Pulse Width = 1.2ms)[2] 200mA
DC Forward Current per Segment or DP ($T_A = 50°C$)[1] 50mA
Reverse Voltage per Segment or DP 6.0V
Lead Soldering Temperature (1.6mm [1/16 inch] Below Seating Plane) ..... 260°C for 3 sec.

Notes:
1. Derate maximum DC current above $T_A = 50°C$ at 1mA/°C per segment, see Figure 2.
2. See Figure 1 to establish pulsed operating conditions.

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[1]	I_V	I_F = 20mA	500	900		µcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[2]	λ_d			640		nm
Forward Voltage, any Segment or DP	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or DP	I_R	V_R = 5V		10		µA
Rise and Fall Time[3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	I_F = 20mA		-1.5		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.

Electrical

The HDSP-3400 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have the P-N junction diffused into a GaAsP epitaxial layer on a GaAs substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.78V + I_{PEAK}(3.7\Omega)$
For: $30mA \leq I_{PEAK} \leq 200mA$

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to have the OFF-segments blend into the display background and to have the ON-segments stand out vividly against this same background. To achieve this goal the HDSP-3400 displays use a gray package and untinted segments to maximize readability in bright ambients.

Contrast enhancement is achieved by using one of the following filter products: SGL Homalite H100-1605 RED or H100-1804 PURPLE: Panelgraphic RUBY RED 60, DARK RED 63 or PURPLE 90; Plexiglass 2423; 3M Light Control Film (louvered filters) in 80% Neutral Density, RED 655, VIOLET or PURPLE colors.

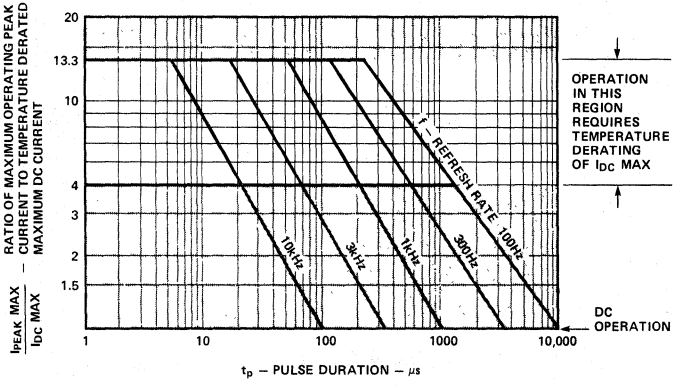


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration.

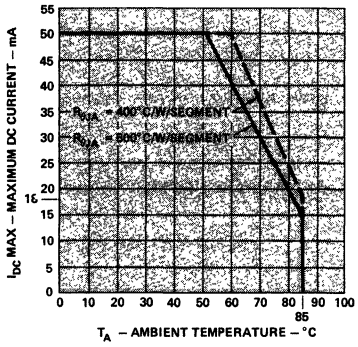


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. T_JMAX=100° C.

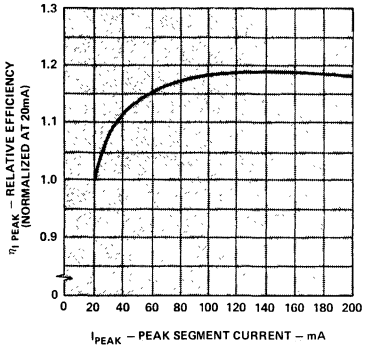


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

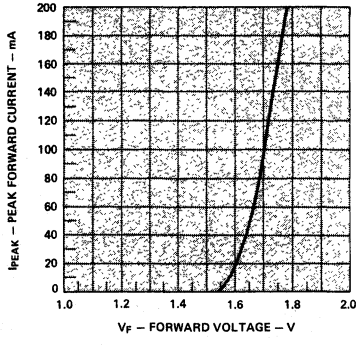


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

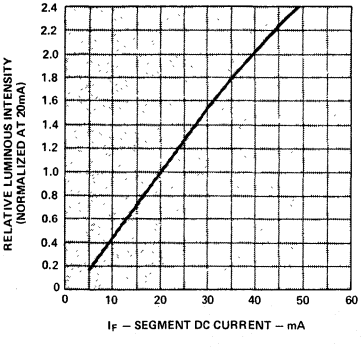


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

HEWLETT PACKARD

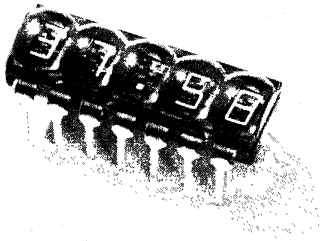
SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

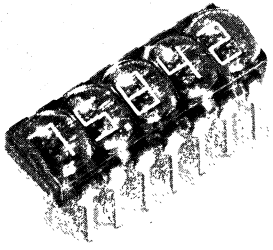
5082-7400 SERIES

TECHNICAL DATA MARCH 1980

Features

- **ULTRA LOW POWER**
  Excellent Readability at Only 500 µA Average per Segment
- **CONSTRUCTED FOR STROBED OPERATION**
  Minimizes Lead Connections
- **STANDARD DIP PACKAGE**
  End Stackable
  Integral Red Contrast Filter
  Rugged Construction
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category
- **IC COMPATIBLE**





Description

The HP 5082-7400 series are 2.79mm (.11"), seven segment GaAsP numeric indicators packaged in 3, 4, and 5 digit end-stackable clusters. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. Options include either the standard lower right hand decimal point or a centered decimal point for increased legibility in multi-cluster applications.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.

Device Selection Guide

Digits per Cluster	Configuration Device	Part Number Center Decimal Point	Part Number Right Decimal Point
3 (right)		5082-7402	5082-7412
3 (left)		5082-7403	5082-7413
4		5082-7404	5082-7414
5		5082-7405	5082-7415

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment (Duration < 1msec)	I_{PEAK}		110	mA
Average Current per Segment	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	–40	75	°C
Storage Temperature	T_S	–40	100	°C
Reverse Voltage	V_R		5	V

NOTES: 1. At 25°C; derate 1mW/°C above 25°C ambient. 2. See Mechanical Section for recommended flux removal solvents.

Electrical /Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3,4] (Time Averaged)	I_V	I_{AVG} = 1mA (I_{PK} = 10mA duty cycle = 10%)	5	20		µcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 10mA		1.6	2.0	V
Reverse Current/Segment or dp	I_R	V_R = 5V			100	µA
Rise and Fall Time [5]	t_r, t_f			10		ns

NOTES: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package. 4. Operation at Peak Currents less than 5mA is not recommended. 5. Time for a 10%-90% change of light intensity for step change in current.

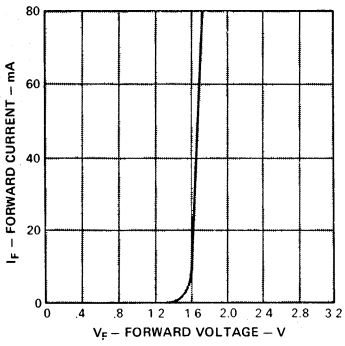


Figure 1. Forward Current vs. Forward Voltage.

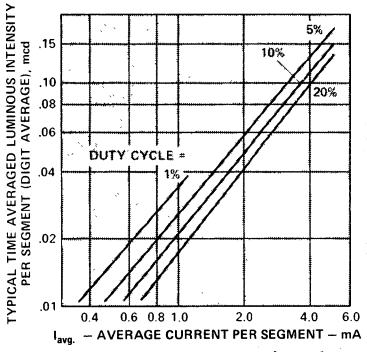


Figure 2. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

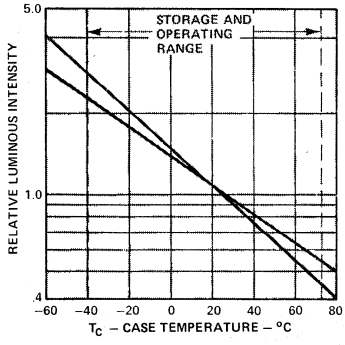


Figure 3. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

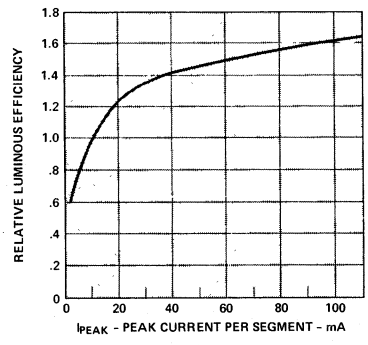


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Package Description

NOTES: 1. Dimensions in millimeters and (inches).
2. Tolerances on all dimensions are ±0.038mm (±.015 in.) unless otherwise noted.

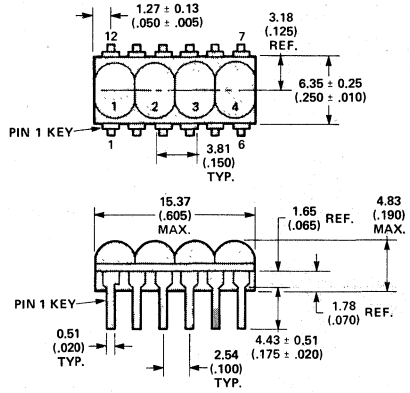


Figure 5. 5082-7402/-7403/-7404/ -7412/-7413/-7414

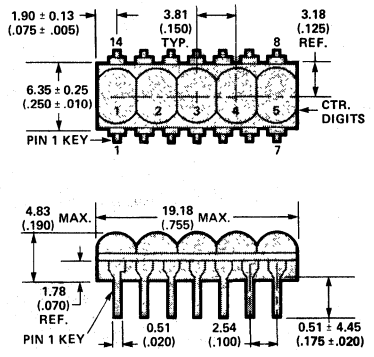
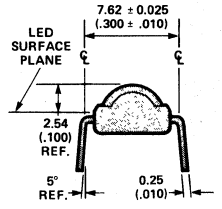


Figure 6. 5082-7405/7415



All Devices

Magnified Character Font Description

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES
5082-7402
5082-7403
5082-7404
5082-7405

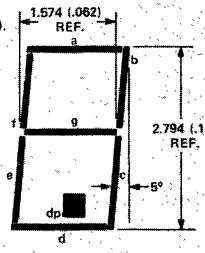


Figure 7. Center Decimal Point Configuration.

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES
5082-7412
5082-7413
5082-7414
5082-7415

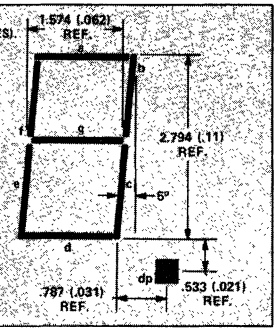


Figure 8. Right Decimal Point Configuration

Device Pin Description

PIN NO.	5082-7402/7412 FUNCTION	5082-7403/7413 FUNCTION	5082-7404/7414 FUNCTION	5082-7405/7415 FUNCTION
1	SEE NOTE 1.	CATHODE 1	CATHODE 1	CATHODE 1
2	ANODE e	ANODE e	ANODE e	ANODE e
3	ANODE c	ANODE c	ANODE c	ANODE c
4	CATHODE 3	CATHODE 3	CATHODE 3	CATHODE 3
5	ANODE dp	ANODE dp	ANODE dp	ANODE dp
6	CATHODE 4	SEE NOTE 1.	CATHODE 4	ANODE d
7	ANODE g	ANODE g	ANODE g	CATHODE 5
8	ANODE d	ANODE d	ANODE d	ANODE g
9	ANODE f	ANODE f	ANODE f	CATHODE 4
10	CATHODE 2	CATHODE 2	CATHODE 2	ANODE f
11	ANODE b	ANODE b	ANODE b	(See Note 1)
12	ANODE a.	ANODE a	ANODE a	ANODE b
13	—	—	—	CATHODE 2
14	—	—	—	ANODE a

NOTE 1. Leave Pin unconnected

Electrical/Optical

The 5082-7400/-7410 series devices utilize a monolithic GaAsP chip of 8 common cathode segments for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 2.79mm (0.11) inches. Satisfactory viewing will be realized within an angle of approximately ±30° from the center-line of the digit.

The decimal point in the 7412, 7413, 7414, and 7415 displays is located at the lower right of the digit for conventional driving schemes.

The 7402, 7403, 7404 and 7405 displays contain a centrally located decimal point which is activated in place of a digit. In long registers, this technique of setting off the decimal point significantly improves the display's readability. With respect to timing, the decimal point is treated as a separate character with its own unique time frame.

Mechanical

The 5082-7400 series package is a standard 12 or 14 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package. The shoulders of the lead frame pins are intentionally raised above the bottom of the package to allow tilt mounting of up to 20° from the PC board.

To improve display contrast, the plastic incorporates a red dye that absorbs strongly at all visible wavelengths except the 655 nm emitted by the LED. In addition, the lead frames are selectively darkened to reduce reflectance. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and SGL Homalite 100-1605, will further lower the ambient reflectance and improve display contrast.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

HEWLETT PACKARD

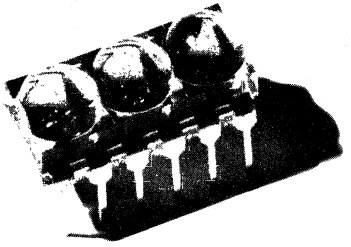
SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

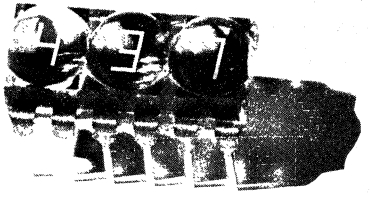
5082-7430 SERIES

TECHNICAL DATA MARCH 1980

Features

- **MOS COMPATIBLE**
  Can be Driven Directly from many MOS Circuits
- **LOW POWER**
  Excellent Readability at Only 250 μA Average per Segment
- **CONSTRUCTED FOR STROBED OPERATION**
  Minimizes Lead Connections
- **STANDARD DIP PACKAGE**
  End Stackable
  Integral Red Contrast Filter
  Rugged Construction
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



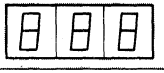


Description

The HP 5082-7430 series displays are 2.79mm (.11 inch, seven segment GaAsP numeric indicators packaged in 2 or 3 digit end-stackable clusters on 200 mil centers. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. These clusters have the standard lower right hand decimal points.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.

Device Selection Guide

Digits per Cluster	Configuration		Part Number
	Device	Package	
2(right)		(Figure 5)	5082-7432
3		(Figure 5)	5082-7433

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	–40	75	°C
Storage Temperature	T_S	–40	100	°C
Reverse Voltage	V_R		5	V
Solder Temperature 1/16" below seating plane (t ≤ 3 sec.) [2]			230	°C

NOTES: 1. Derate linearly @ 1 mW/°C above 25°C ambient. 2. See Mechanical section for recommended flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	10	40		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55	2.0	V
Reverse Current/Segment or dp	I_R	V_R = 5V			100	μA
Rise and Fall Time [5]	t_r, t_f			10		ns

NOTES: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package. 4. Operation at Peak Currents less than 3.5mA is not recommended. 5. Time for a 10%-90% change of light intensity for step change in current.

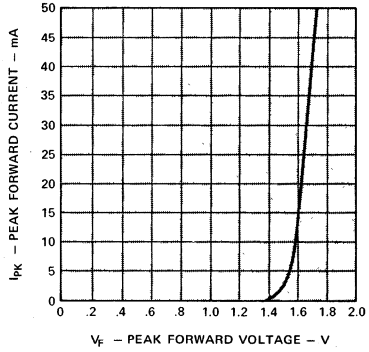


Figure 1. Peak Forward Current vs. Peak Forward Voltage

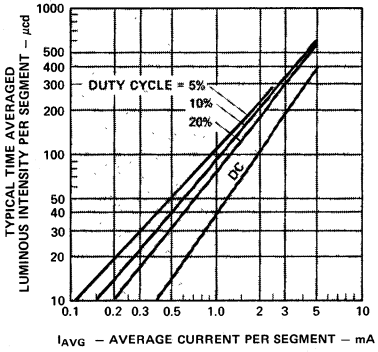


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

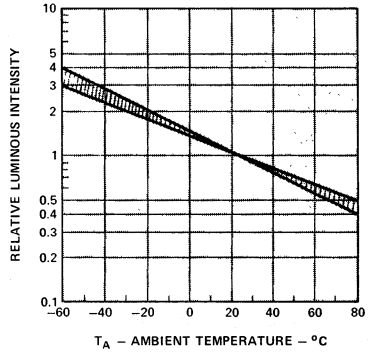


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

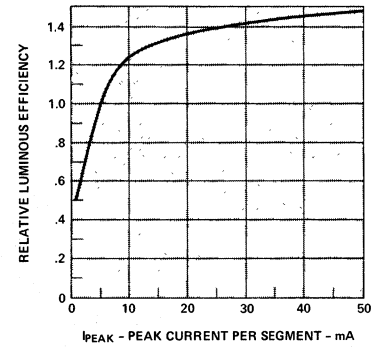


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

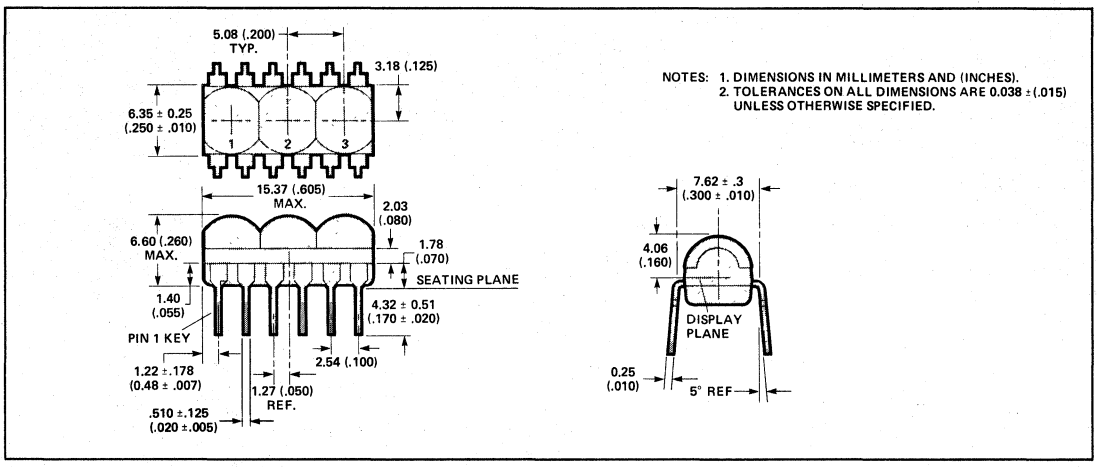


Figure 5.

Magnified Character Font Description

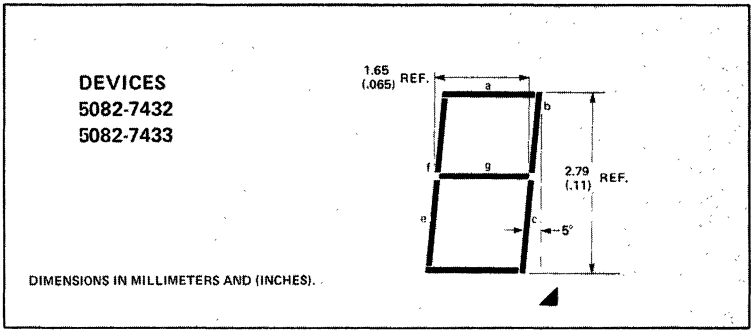


Figure 6.

Device Pin Description

PIN NUMBER	5082-7432 FUNCTION	5082-7433 FUNCTION
1	SEE NOTE 1.	CATHODE 1
2	ANODE e	ANODE e
3	ANODE d	ANODE d
4	CATHODE 2	CATHODE 2
5	ANODE c	ANODE c
6	ANODE dp	ANODE dp
7	CATHODE 3	CATHODE 3
8	ANODE b	ANODE b
9	ANODE g	ANODE g
10	ANODE a	ANODE a
11	ANODE f	ANODE f
12	SEE NOTE 1.	SEE NOTE 1.

NOTE 1. Leave Pin unconnected.

Electrical/Optical

The 5082-7430 series devices utilize a monolithic GaAsP chip of 8 common cathode segments for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 2.79mm (0.11) inches. Satisfactory viewing will be realized within an angle of approximately ±20° from the center-line of the digit.

To improve display contrast, the plastic encapsulant contains a red dye to reduce the reflected ambient light. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and SGL Homalite 100-1605, will further lower the ambient reflectance and improve display contrast.

Character encoding on the 5082-7430 series devices is performed by standard 7 segment decoder/driver circuits. Through the use of strobing techniques only one decoder/driver is required for very long multidigit displays.

Mechanical

The 5082-7430 series package is a standard 12 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

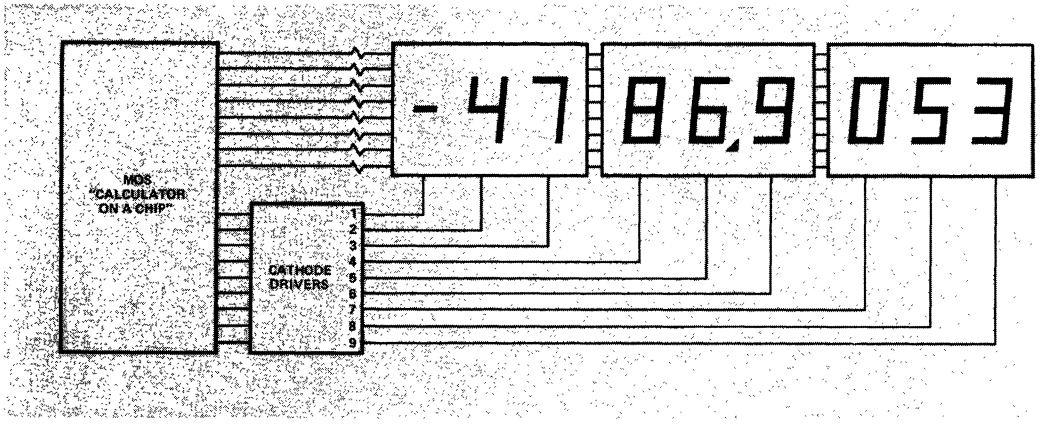


Figure 7. Block Diagram for Calculator Display

HEWLETT PACKARD

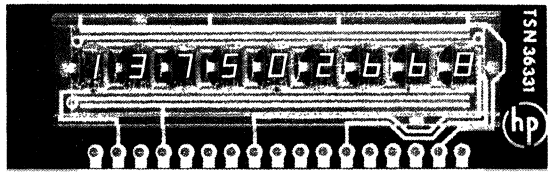
SPECIAL PARTS FOR CALCULATORS

5082-7440 SERIES

TECHNICAL DATA MARCH 1980

Features

- **MOS COMPATIBLE**
  Can be driven directly from MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC Board.
- **AVAILABLE IN 50.8mm (2.0 inch) AND 60.325mm (2.375 inch) BOARD LENGTHS**



Description

The HP 5082-7440 series displays are 2.67mm (.105") high, seven segment GaAsP Numeric Indicators mounted in an eight or nine digit configuration on a P.C. Board. These special parts, designed specifically for calculators, have right hand decimal points and are mounted on 5.08mm (200 mil) centers. The plastic lens magnifies the digits and includes an integral protective bezel.

Applications are primarily portable, hand-held calculators and other products requiring low power, low cost and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Configuration		Part No.
	Device	Package	
8	8.8.8.8.8.8.8.8.	(Figure 5)	5082-7440 5082-7448
9	8.8.8.8.8.8.8.8.8.	(Figure 5)	5082-7441 5082-7449

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t≤3 sec.)[2]			230	°C

NOTES: 1. Derate linearly @ 0.1mA/°C above 60°C ambient.
2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	9	40		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55		V

NOTES: 3. See Figure 7 for test circuit.
4. Operation at Peak Currents of less than 3.5mA is not recommended.

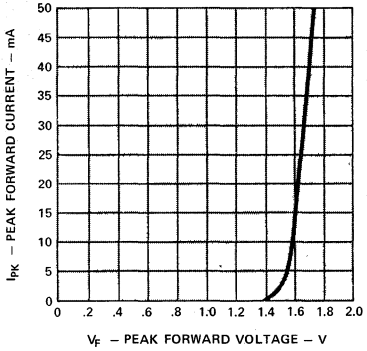


Figure 1. Peak Forward Current vs. Peak Forward Voltage

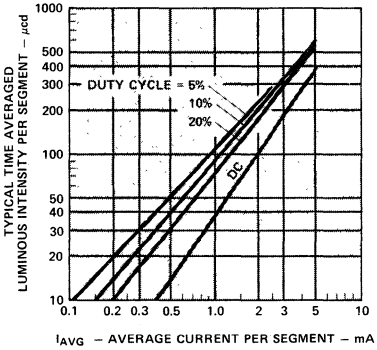


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

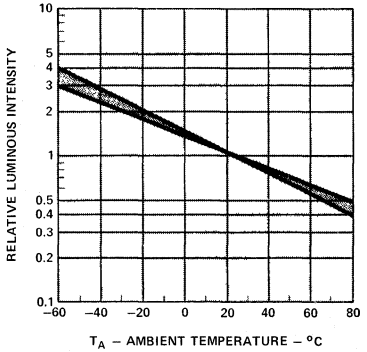


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

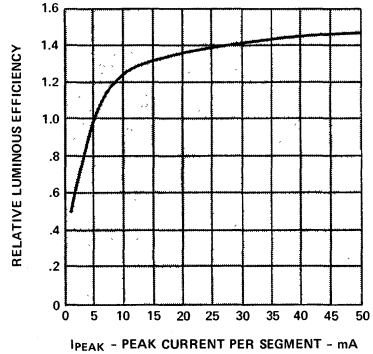


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

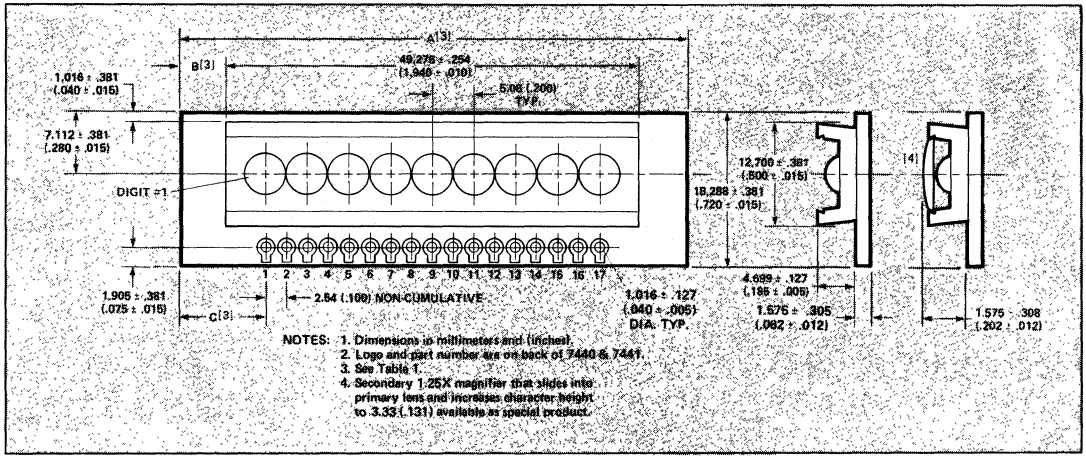


Figure 5.

Magnified Character Font Description

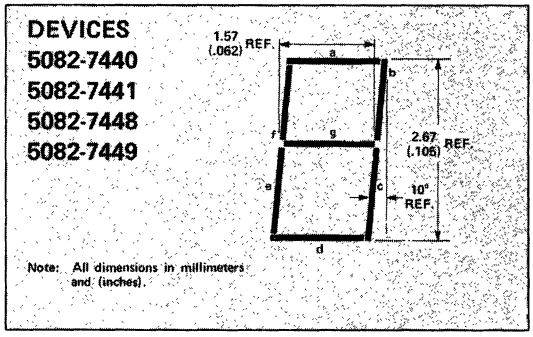


Figure 6.

Part No.	Dim. A	Dim. B	Dim. C
5082-7440	50.800(2.000)	0.760(.030)	5.08(.200)
5082-7441	50.800(2.000)	0.760(.030)	5.08(.200)
5082-7448	60.325(2.375)	5.512(.217)	9.830(.387)
5082-7449	60.325(2.375)	5.512(.217)	9.830(.387)

Tolerances: ±.381(.015)

Table 1.

Device Pin Description

Pin No.	5082-7440 5082-7448 Function	5082-7441 5082-7449 Function	Pin No.	5082-7440 5082-7448 Function	5082-7441 5082-7449 Function
1	N/C	Dig. 1 Cathode	10	Seg. d Anode	Seg. d Anode
2	Seg. c Anode	Seg. c Anode	11	Dig. 6 Cathode	Dig. 6 Cathode
3	Dig. 2 Cathode	Dig. 2 Cathode	12	Seg. g Anode	Seg. g Anode
4	d.p. Anode	d.p. Anode	13	Dig. 7 Cathode	Dig. 7 Cathode
5	Dig. 3 Cathode	Dig. 3 Cathode	14	Seg. b Anode	Seg. b Anode
6	Seg. a Anode	Seg. a Anode	15	Dig. 8 Cathode	Dig. 8 Cathode
7	Dig. 4 Cathode	Dig. 4 Cathode	16	Seg. f Anode	Seg. f Anode
8	Seg. e Anode	Seg. e Anode	17	Dig. 9 Cathode	Dig. 9 Cathode
9	Dig. 5 Cathode	Dig. 5 Cathode			

Electrical/Optical

The HP 5082-7440 series devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 0.105" (2,67mm). Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. The secondary lens magnifier that will increase character height from 2.67mm (0.105") to 3.33mm (0.131") and reduce viewing angle in the vertical plane only from ±20° to approximately ±18° is available as a special product. A filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower ambient reflectance and improve display contrast. Character encoding of the -7440 series devices is performed by standard 7 segment decoder driver circuits.

The 5082-7440 series devices are tested for digit to digit luminous intensity matching using the circuit depicted in Figure 7. Component values are chosen to give an I_F of 5mA per segment at a segment V_F of 1.55 volts. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby insuring excellent digit to digit matching. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical

The 5082-7440 series devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens containing 9 individual magnifying elements is attached to the PC board over the digits. The device may be mounted either by use of pins which may be soldered into the plate through holes at the connector edge of the board or by insertion into a standard PC board connector.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations.

Special Cleaning Instructions

For bulk cleaning after a hand solder operation, the following process is recommended: Wash display in clean liquid Freon TP-35 or Freon TE-35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30°C (86°F). Methanol, isopropanol, or ethanol may be used for hand cleaning at room temperature. Water may be used for hand cleaning if it is not permitted to collect under display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

These devices are constructed on a silver plated printed circuit board. To prevent the formation of a tarnish (Ag_2S) which could impair solderability, the boards should be stored in the unopened shipping packages until they are used. Further information on the storage, handling and cleaning of silver-plated components is contained in Hewlett-Packard Application Bulletin No. 3.

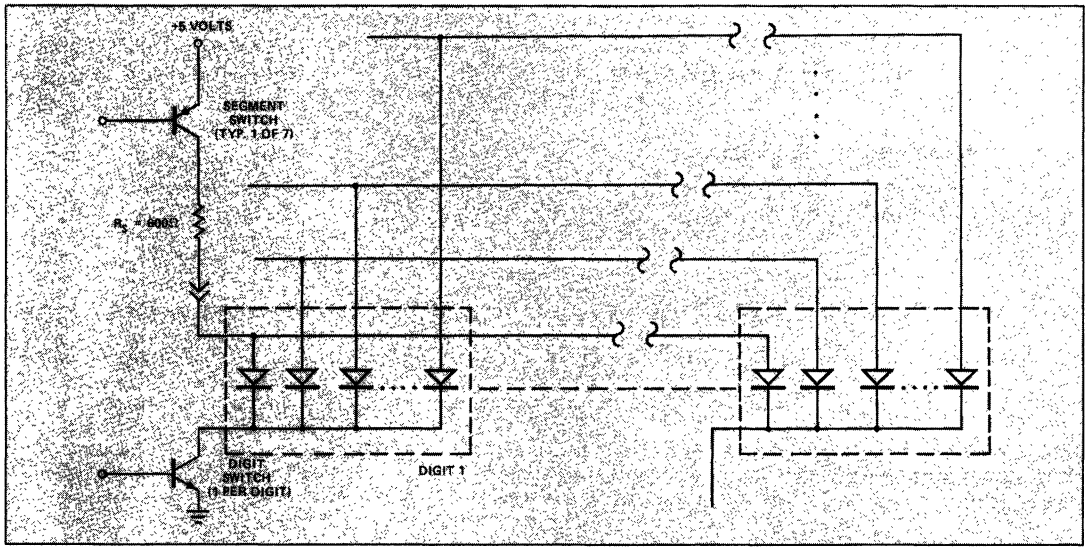


Figure 7. Circuit Diagram used for Testing the Luminous Intensity of the HP 5082-7440

HEWLETT PACKARD

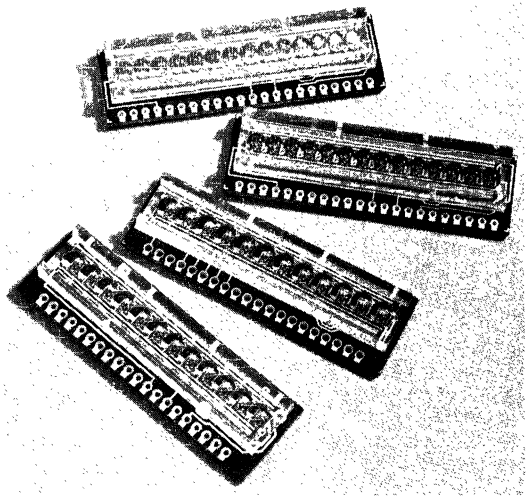
SPECIAL PARTS FOR SCIENTIFIC AND BUSINESS CALCULATORS

5082-7442
5082-7444
5082-7445
5082-7446
5082-7447

TECHNICAL DATA MARCH 1980

Features

- **12, 14, AND 16 DIGIT CONFIGURATIONS**
- **MOS COMPATIBLE**
  Can be driven directly from most MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent Alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC board.



Description

The HP 5082-7442, 7444, 7446, and 7447 are seven segment GaAsP Numeric indicators mounted in 12, 14, or 16 digit configurations on a P.C. board. These special parts, designed specifically for scientific and business calculators, have right hand decimal points and are mounted on 175 mil (4.45mm) centers in the 12 digit configurations and 150 mil (3.81mm) centers in the 14 and 16 digit configurations. The plastic lens magnifies the digits and includes an integral protective bezel.

Applications are primarily portable, hand held calculators, digital telephone peripherals, data entry terminals and other products requiring low power, low cost, and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Digit Height mm (inches)	Configuration DEVICE	Package	Part No. 5082-
12	2.54 (.100)	8.8.8.8.8.8.8.8.8.8.8.8.	Figure 4	7442 and 7445
14	2.54 (.100)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 5	7444
14	2.84 (.112)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 5	7447 *
16	2.92 (.115)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 6	7446

*5082-7447 is a 5082-7444 with a slide-in cylindrical lens to provide added magnification.

Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration <500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t ≤3 sec.)[2]			230	°C

NOTES: 1. Derate linearly at 0.1mA/°C above 60°C ambient.
2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Part No.	Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
7442/7445	Luminous Intensity/ Segment or dp[3] (Digit Average)	I_V	5mA Peak 1/12 Duty Cycle	7	35		μcd
7444/7447			5mA Peak 1/14 Duty Cycle	7	35		μcd
7446			5mA Peak 1/16 Duty Cycle				
7442/7445 7444/7447 7446	Peak Wavelength	λ_{PEAK}			655		nm
	Forward Voltage/ Segment or dp	V_F	I_F = 5mA		1.55		V

NOTE: 3. Operation at Peak Currents of less than 3.5mA is not recommended.

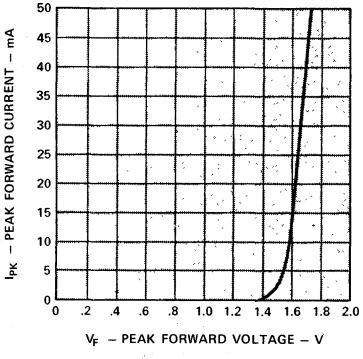


Figure 1. Peak Forward Current vs. Peak Forward Voltage

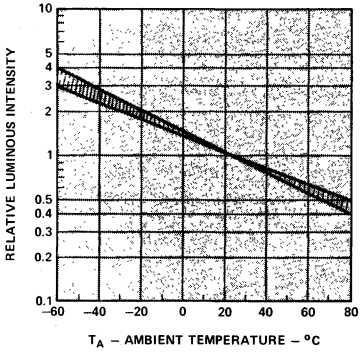


Figure 2. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

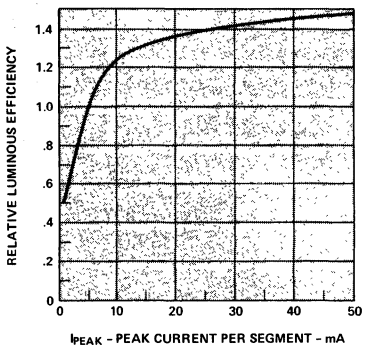


Figure 3. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical/Optical

The HP 5082-7442, 7444, 7445, 7446 and 7447 devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of digits in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character. Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A filter, such as plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower the ambient reflectance and improve display contrast. Digit encoding of these devices is performed by standard 7 segment decoder driver circuits.

These devices are tested for digit-to-digit luminous intensity matching. This test is performed with a power supply of 5V and component values selected to supply 5mA I_{PEAK} at V_F = 1.55V. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical Specifications

The 5082-7442, 7444, 7445, 7446, and 7447 devices are constructed on a silver plated printed circuit board substrate. A molded plastic lens array is attached to the PC board over the digits to provide magnification.

These devices may be mounted using any one of several different techniques. The most straightforward is the use of standard PC board edge connectors. A less expensive approach can be implemented through the use of stamped or etched metal mounting clips such as those available from Burndy (Series LED-B) or JAV Manufacturing (Series 022-002). Some of these devices will also serve as an integral display support. A third approach would be the use of a row of wire stakes which would first be soldered to the PC mother-board and the display board then inserted over the wire stakes and soldered in place.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the lens. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations. A solder containing approximately 2% silver (Sn 62) will enhance solderability by preventing leaching of the plated silver off the PC board into the solder solution.

Special Cleaning Instructions

For bulk cleaning after a hand solder operation, the following process is recommended. Wash display in clean liquid Freon TP-35 or Freon TE-35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30°C (86°F). Methanol, isopropanol, or ethanol may be used for cleaning at room temperature. Soap and water solutions may be utilized for removing water-soluble fluxes from the contact area but must not be allowed to collect under the display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

These devices are constructed on a silver plated printed circuit board. To prevent the formation of a tarnish (Ag_2S) which could impair solderability, the boards should be stored in the unopened shipping packages until they are used. Further information on the storage, handling and cleaning of silver-plated components is contained in Hewlett-Packard Application Bulletin No. 3.

Device Pin Description

Pin No.	5082-7442 5082-7444 5082-7447 Function	5082-7445 Function	5082-7446 Function
1	Cathode-Digit 1	Anode-Segment a	Cathode-Digit 1
2	Cathode-Digit 2	Anode-Segment f	Cathode-Digit 2
3	Cathode-Digit 3	Anode-Segment b	Cathode-Digit 3
4	Anode-Segment c	Anode-Segment c	Cathode-Digit 4
5	Cathode-Digit 4	Anode-Segment d	Cathode-Digit 5
6	Anode-DP	Anode-Segment DP	Anode-Segment e
7	Cathode-Digit 5	Anode-Segment e	Cathode-Digit 6
8	Anode-Segment a	Anode-Segment g	Anode-Segment d
9	Cathode-Digit 6	Cathode-Digit 3	Cathode-Digit 7
10	Anode-Segment e	Cathode-Digit 2	Anode-Segment a
11	Cathode-Digit 7	Cathode-Digit 4	Cathode-Digit 8
12	Anode-Segment d	Cathode-Digit 1	Anode-Segment DP
13	Cathode-Digit 8	Cathode-Digit 5	Cathode-Digit 9
14	Anode-Segment g	Cathode-Digit 12	Anode-Segment c
15	Cathode-Digit 9	Cathode-Digit 6	Cathode-Digit 10
16	Anode-Segment b	Cathode-Digit 11	Anode-Segment g
17	Cathode-Digit 10	Cathode-Digit 7	Cathode-Digit 11
18	Anode-Segment f	Cathode-Digit 10	Anode-Segment b
19	Cathode-Digit 11	Cathode-Digit 9	Cathode-Digit 12
20	Cathode-Digit 12	Cathode-Digit 8	Anode-Segment f
21	Cathode-Digit 13		Cathode-Digit 13
22	Cathode-Digit 14		Cathode-Digit 14
23			Cathode-Digit 15
24			Cathode-Digit 16

Package Dimensions

DEVICE	X	Y	Z
5082-7442	60.3 (2.375)	6.03 (.2375)	1.02 (.040)
5082-7445	59.6 (2.345)	5.70 (.2225)	1.42 (.056)

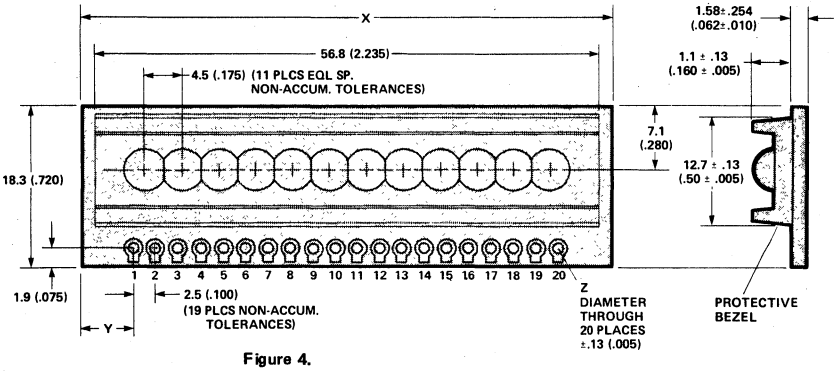


Figure 4.

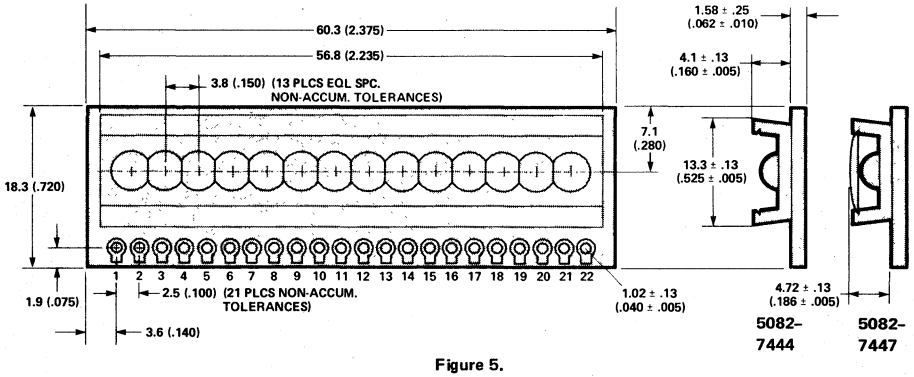


Figure 5.

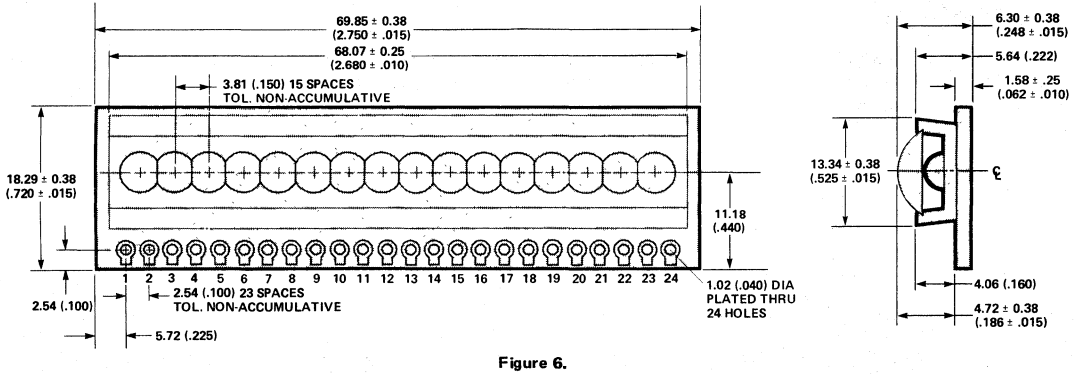
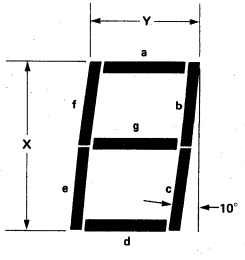


Figure 6.



DEVICE	X	Y
5082-7442	2.54 (.100)	1.42 (.056)
5082-7444	2.54 (.100)	1.40 (.055)
5082-7445	2.54 (.100)	1.42 (.056)
5082-7446	2.92 (.115)	1.40 (.055)
5082-7447	2.84 (.112)	1.40 (.055)

NOTES: 1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. TOLERANCES ON ALL DIMENSIONS ARE ±0.38 (.015) UNLESS OTHERWISE SPECIFIED.

HEWLETT PACKARD

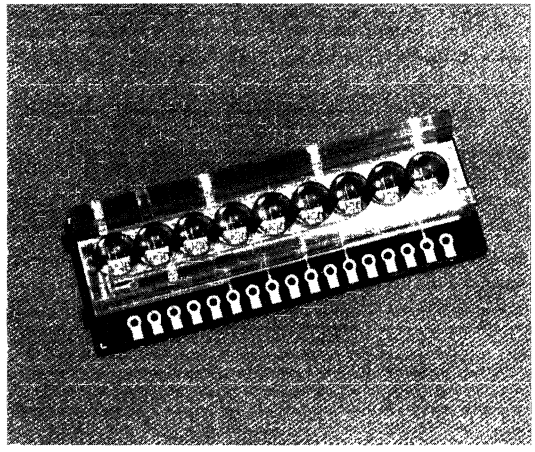
SPECIAL PARTS FOR CALCULATORS

5082-7240 SERIES

TECHNICAL DATA MARCH 1980

Features

- **MOS COMPATIBLE**
  Can be driven directly from MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC Board.
- **STATE OF THE ART LENS DESIGN**
  Assures the best possible character height, viewing angle, off-axis distortion tradeoff.



Description

The HP 5082-7240 series displays are 2.59mm (.102") high, seven segment GaAsP Numeric Indicators mounted in an eight or nine digit configuration on a P. C. Board. These special parts, designed specifically for calculators, have right hand decimal points and are mounted on 5.08mm (200 mil) centers. The plastic lens over the digits has a magnifier and a protective bezel built-in. A secondary magnifying lens, available on special request, can be added to the primary lens for additional character enlargement.

Applications are primarily portable, hand-held calculators and other products requiring low power, low cost and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Configuration		Part No.
	Device	Package	
8	8.8.8.8.8.8.8.8.	(Figure 5)	5082-7240
9	8.8.8.8.8.8.8.8.8.	(Figure 5)	5082-7241

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t≤3 sec.)[2]			230	°C

NOTES: 1. Derate linearly @ 0.1mA/°C above 60°C ambient. 2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	12.5	50		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.6		V

NOTES: 3. See Figure 7 for test circuit.
4. Operation at Peak Currents of less than 3.0mA is not recommended.

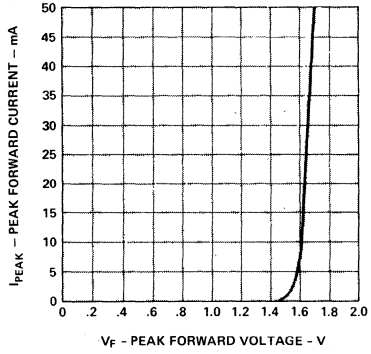


Figure 1. Peak Forward Current vs. Peak Forward Voltage

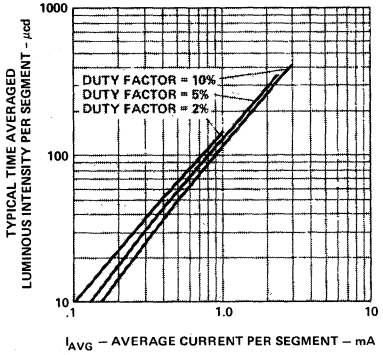


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

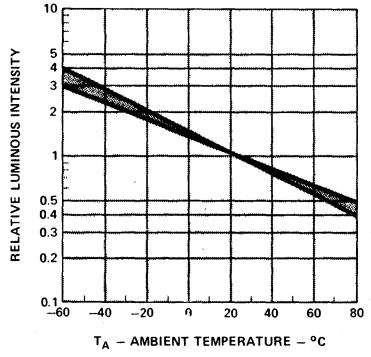


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

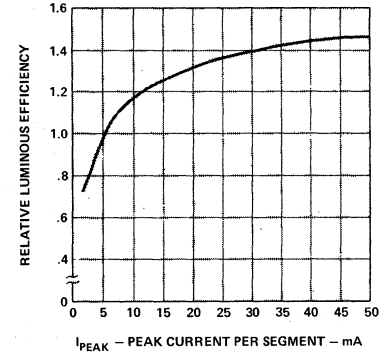


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

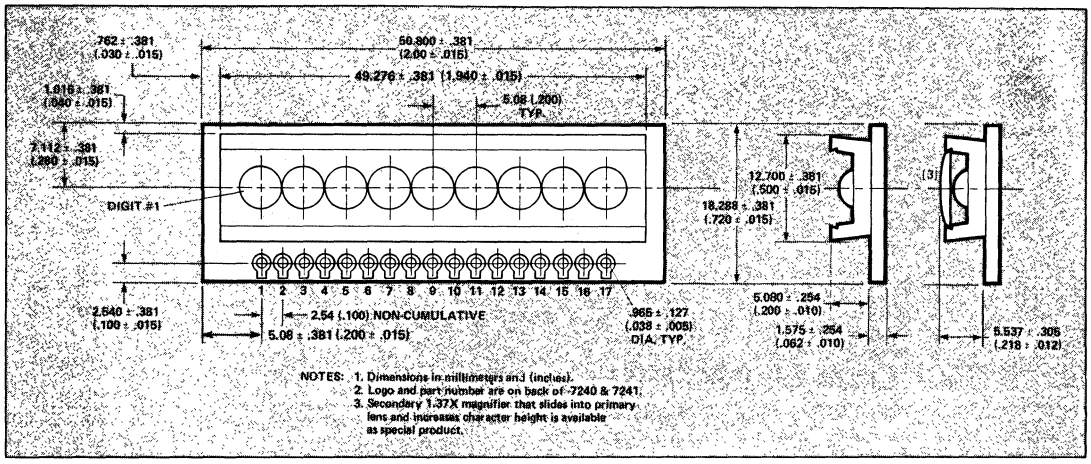


Figure 5.

Magnified Character Font Description

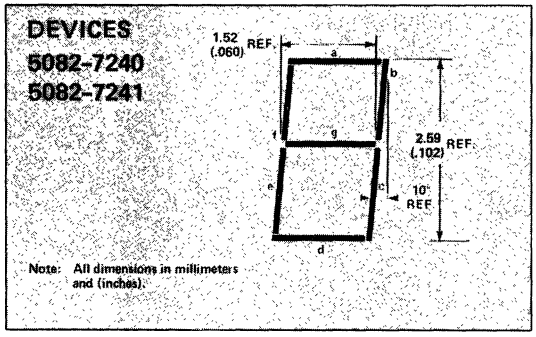


Figure 6.

Device Pin Description

Pin No.	5082-7240 Function	5082-7241 Function	Pin No.	5082-7240 Function	5082-7241 Function
1	NOTE 4	Dig. 1 Cathode	10	Seg. d Anode	Seg. d Anode
2	Seg. c Anode	Seg. c Anode	11	Dig. 6 Cathode	Dig. 6 Cathode
3	Dig. 2 Cathode	Dig. 2 Cathode	12	Seg. g Anode	Seg. g Anode
4	d.p. Anode	d.p. Anode	13	Dig. 7 Cathode	Dig. 7 Cathode
5	Dig. 3 Cathode	Dig. 3 Cathode	14	Seg. b Anode	Seg. b Anode
6	Seg. a Anode	Seg. a Anode	15	Dig. 8 Cathode	Dig. 8 Cathode
7	Dig. 4 Cathode	Dig. 4 Cathode	16	Seg. f Anode	Seg. f Anode
8	Seg. e Anode	Seg. e Anode	17	Dig. 9 Cathode	Dig. 9 Cathode
9	Dig. 5 Cathode	Dig. 5 Cathode			

NOTE 4: Leave pin 1 unconnected on the 5082-7240.

Electrical/Optical

The HP 5082-7240 series devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 2.59mm (0.102"). Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A secondary lens magnifier that will increase character height from 2.59mm (.102") to 3.56mm (.140") is available as a special product. Character encoding of the 7240 series devices is performed by standard 7 segment decoder driver circuits.

The 5082-7240 series devices are tested for digit to digit luminous intensity matching using the circuit depicted in Figure 7. Component values are chosen to give an I_F of 5mA per segment at a segment V_F of 1.6 volts. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby insuring excellent digit to digit matching. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical

The 5082-7240 series devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens bar containing 9 individual magnifying elements is attached to the PC board over the digits. The device may be mounted either by use of pins which may be soldered into the plate through holes at the connector edge of the board or by insertion into a standard PC board connector.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations.

Special Cleaning Instructions

For bulk cleaning after a hand solder operation, the following process is recommended: Wash display in clean liquid Freon TP-35 or Freon TE-35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30°C (86°F). Methanol, isopropanol, or ethanol may be used for hand cleaning at room temperature. Water may be used for hand cleaning if it is not permitted to collect under display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

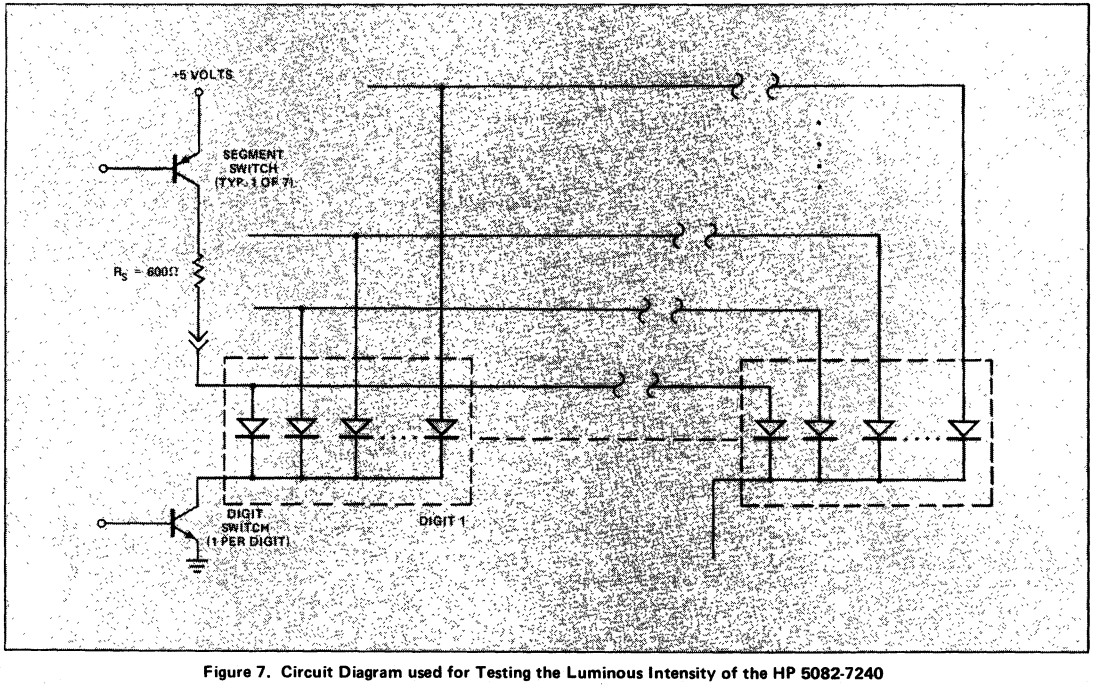


Figure 7. Circuit Diagram used for Testing the Luminous Intensity of the HP 5082-7240

HEWLETT PACKARD

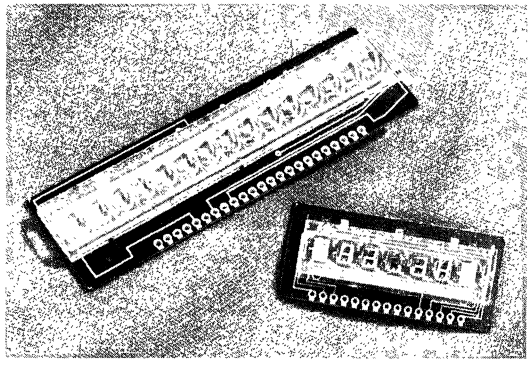
LARGE MONOLITHIC NUMERIC INDICATORS

5082-7265
5082-7275
5082-7285
5082-7295

TECHNICAL DATA MARCH 1980

Features

- **LARGE 4.45mm (.175") CHARACTER HEIGHT**
- **LOW POWER**
  Satisfactory Readability can be Achieved with Drive Currents as Low as 1.0-1.5mA Average per Segment Depending on Peak Current Levels
- **MOS COMPATIBLE**
  Can be Driven Directly from MOS Circuits
- **COMPACT INFORMATION DISPLAY**
  5.84mm (.23") Digit Spacing Yields Over 4 Characters per Inch.
- **HIGH AMBIENT READABILITY**
  High Sterance Emitting Areas Mean Excellent Readability in High Ambient Light Conditions
- **HIGH LEGIBILITY AND NUMBER RECOGNITION**
  High On/Off Contrast and Fine Line Segments Improve Viewer Recognition of the Displayed Number
- **UNIFORM ALIGNMENT**
  Excellent Alignment is Assured by Design
- **MATCHED BRIGHTNESS**
  Provides Uniform Light Output from Digit to Digit on a Single PC Board
- **EASY MOUNTING**
  Flexible Mounting in Desired Position with Edge Connectors or Soldered Wires



Description

The HP 5082-7265, 7275, 7285, and 7295 displays are 4.45 mm (.175") seven segment GaAsP numeric indicators mounted in 5 or 15 digit configurations on a PC Board. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. Options include both a right hand decimal point and centered decimal version for improved legibility. The digits are mounted on 5.84 mm (230 mil) centers.

These displays are attractive for applications such as digital instruments, desk top calculators, avionics and automobile displays, P.O.S. terminals, in-plant control equipment, and other products requiring low power, display compactness, readability in high ambients, or highly legible, long lifetime numerical displays.

Device Selection Guide

Digits Per PC Board	Configuration			Part No. 5082-
	Device	Package	Character	
5		(Figure 5)	Center Decimal Point (Figure 7)	7265
15		(Figure 6)	Center Decimal Point (Figure 7)	7275
5		(Figure 5)	Right Decimal Point (Figure 7)	7285
15		(Figure 6)	Right Decimal Point (Figure 7)	7295

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or DP (Duration <35μs)	I_{PEAK}		200	mA
Average Current per Segment or DP [1]	I_{AVG}		7	mA
Power Dissipation per Digit [2]	P_D		125	mW
Operating Temperature, Ambient	T_A	-20	+70	°C
Storage Temperature	T_S	-20	+80	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t≤3 sec.) [3]			230	°C

NOTES: 1. Derate linearly at 0.12 mA/°C above 25°C ambient.
2. Derate linearly at 2.3 mW/°C above 25°C ambient.
3. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp (Time Averaged) 15 digit display 5082-7275, 5082-7295 [4,6]	I_v	$I_{avg.}$ = 2 mA (30 mA Peak 1/15 duty cycle)	30	90		μcd
Luminous Intensity/Segment or dp (Time Averaged) 5 digit display 5082-7265, 5082-7285 [4,6]	I_v	$I_{avg.}$ = 2 mA (10 mA Peak 1/5 duty cycle)	30	70		μcd
Forward Voltage per Segment or dp 5082-7275, 5082-7295 15 digit display	V_F	I_F = 30 mA		1.60	2.3	V
Forward Voltage per Segment or dp 5082-7265, 5082-7285 5 digit display	V_F	I_F = 10 mA		1.55	2.0	V
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [5]	λ_d			640		nm
Reverse Current per Segment or dp	I_R	V_R = 5V			100	μA
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C

NOTES: 4. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship:
$I_V(T_A) = I_{V(25°C)}(.985)^{(T_A - 25°C)}$
5. The dominant wavelength λ_d, is derived from the C.I.E. Chromaticity Diagram and represents the single wavelength which defines the color of the device.
6. Operation at peak currents of less than 6.0 mA is not recommended.

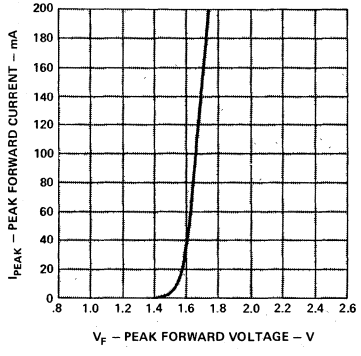


Figure 1. Peak Forward Current vs. Peak Forward Voltage.

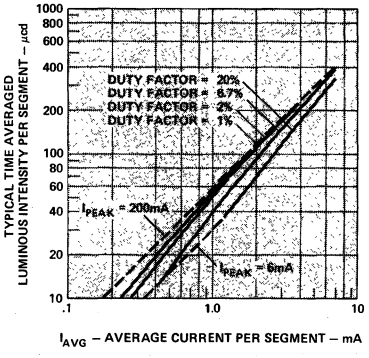


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

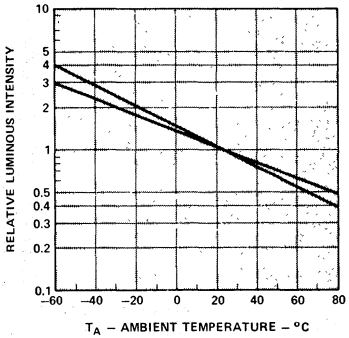


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

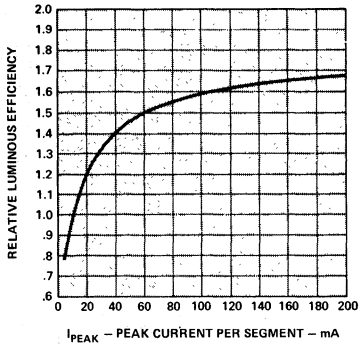


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical

The HP 5082-7265, 7275, 7285, and 7295 devices utilize a seven segment monolithic GaAsP chip. The 5082-7285 and 7295 devices use a separate decimal point chip located to the right of each digit. The 5082-7265 and 7275 devices use a centered decimal point on the monolithic seven segment chip. The centered decimal point version improves the displays readability by dedicating an entire digit position to distinguishing the decimal point. In the driving scheme for the centered decimal point version the decimal point is treated as a separate character with its own time frame.

The segments and decimal points of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Character encoding is performed by standard 7 segment decoder driver circuits. A detailed discussion of display circuits and drive techniques appears in Applications Note 937.

These devices are tested for digit to digit luminous intensity using the circuit depicted in Figure 8. Component values are chosen to give a Peak I_F of 10 mA per segment for the 5 digit displays and 30 mA per segment for the 15 digit displays. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby ensuring excellent digit to digit matching. If the device is to be driven at peak currents of less than 6.0 mA, it is recommended that the HP field salesman or factory be contacted.

For special product applications, the number of digits per display can be altered. It is also possible to provide a colon instead of the centered decimal point. Contact the HP field salesman or factory to discuss such special modifications.

Optical

Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 4.45mm (.175"). To increase vertical viewing angle the secondary cylindrical magnifier can be removed reducing character height to 3.86mm (.152"). A filter, such as Panelgraphic 60 or 63, or Homalite 100-1600, will lower ambient reflectance and improve display contrast.

Mechanical

These devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens is attached to the PC board over the digits. The lens is an acrylic styrene material that gives good optical lens performance, but is subject to scratching so care should be exercised in handling.

The device may be mounted either by use of pins which may be hand soldered into the plated through holes at the connector edge of the PC board or by insertion into a standard PC board connector. The devices may be hand soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations.

The PC board is silver plated. To prevent the formation of a tarnish (Ag_2S) which could impair solderability the displays should be stored in the unopened shipping packages until they are used. Further information on the storage, handling, and cleaning of silver plated components is contained in Hewlett-Packard Application Bulletin No. 3.

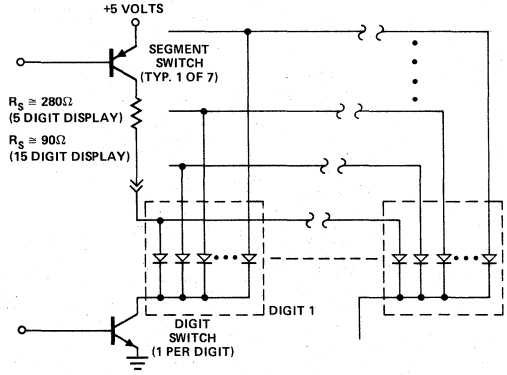


Figure 5. Circuit Diagram used for Testing the Luminous Intensity.

Package Dimensions

ALL DIMENSIONS IN MILLIMETERS AND (INCHES). TOLERANCES ARE ±0.203 (±.008) UNLESS OTHERWISE NOTED

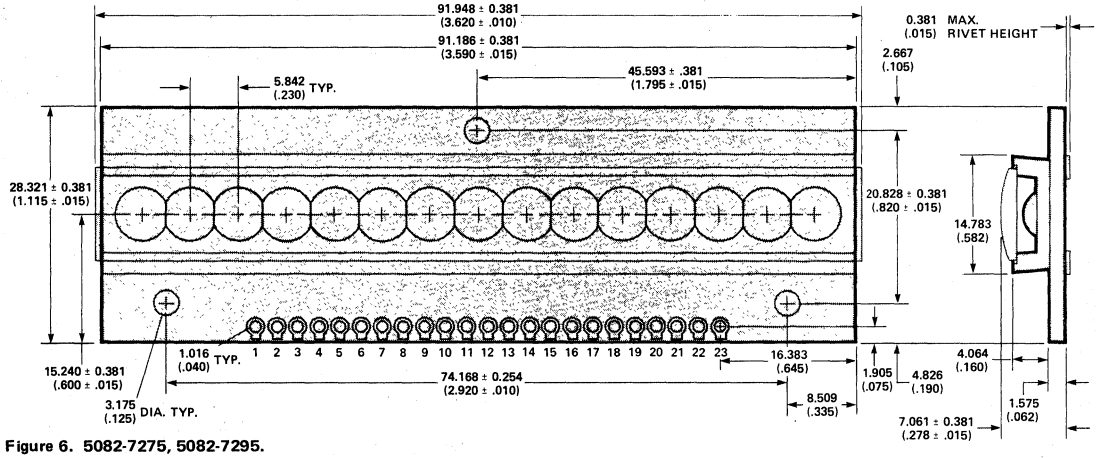


Figure 6. 5082-7275, 5082-7295.

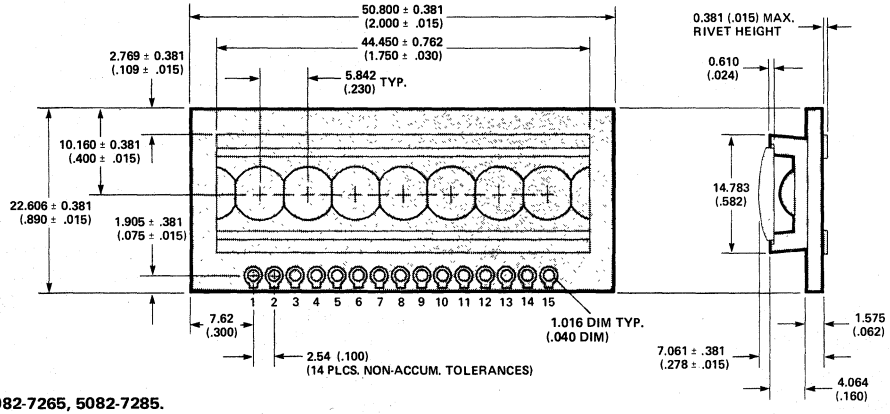
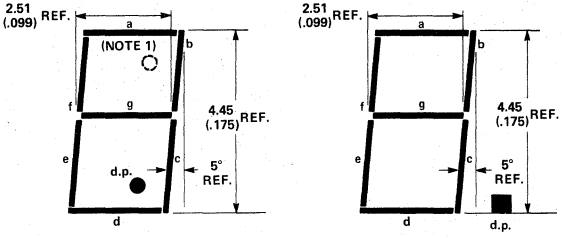


Figure 7. 5082-7265, 5082-7285.

Magnified Character Font Description

DEVICES
5082-7265
5082-7275

DEVICES
5082-7285
5082-7295



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE 1. Bonding Option for Colon Instead of Decimal Point. See Electrical Section.

Figure 8.

Device Pin Description

Pin No.	5082-7265 5082-7285 Function	5082-7275 5082-7295 Function
1	Anode Segment b	Cathode Digit 1
2	Anode Segment g	Cathode Digit 2
3	Anode Segment e	Cathode Digit 3
4	Cathode Digit 1	Cathode Digit 4
5	Cathode Digit 2	Anode Segment dp
6	Cathode Digit 3	Cathode Digit 5
7	Cathode Digit 4	Anode Segment c
8	Cathode Digit 5	Cathode Digit 6
9	Cathode Digit 6	Anode Segment e
10	Cathode Digit 7	Cathode Digit 7
11	Anode Segment dp	Anode Segment a
12	Anode Segment d	Cathode Digit 8
13	Anode Segment c	Anode Segment g
14	Anode Segment a	Cathode Digit 9
15	Anode Segment f	Anode Segment d
16		Cathode Digit 10
17		Anode Segment f
18		Cathode Digit 11
19		Anode Segment b
20		Cathode Digit 12
21		Cathode Digit 13
22		Cathode Digit 14
23		Cathode Digit 15

HEWLETT PACKARD

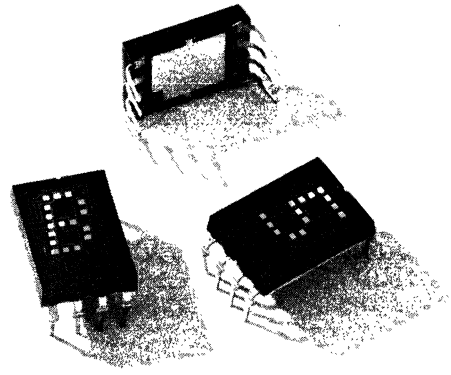
NUMERIC and HEXADECIMAL INDICATORS

5082-7300
5082-7302
5082-7304
5082-7340

TECHNICAL DATA MARCH 1980

Features

- **NUMERIC 5082-7300/-7302**
  - **0-9, Test State, Minus Sign, Blank States Decimal Point**
  - **7300 Right Hand D.P.**
  - **7302 Left Hand D.P.**
- **HEXADECIMAL 5082-7340**
  - **0-9, A-F, Base 16 Operation**
  - **Blanking Control, Conserves Power**
  - **No Decimal Point**
- **DTL/TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY**
  8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readibility
- **STANDARD .600 INCH x .400 INCH DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide a reliable, low-cost method for displaying digital information.

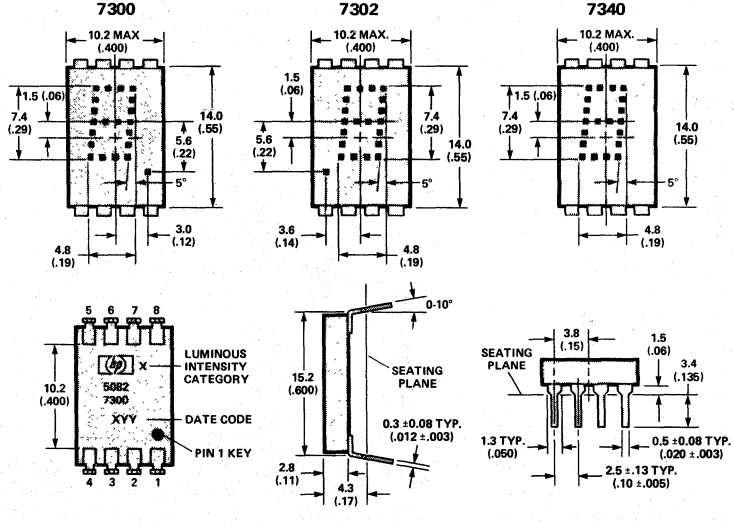
The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "-" sign, a test pattern, and four blanks in the invalid BCD states, The unit employs a right-hand decimal point. Typical applications include point-of-sale terminals, instrumentation, and computer systems.

The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a (±1.) overrange character, including decimal point, used in instrumentation applications.

Package Dimensions



PIN	FUNCTION	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−40	+100	°C
Operating temperature, case [1,2]	T_C	−20	+85	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_C=25° C	32	70		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C=25° C		655		nm
Dominant Wavelength [8]	λ_d	T_C=25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C = +85° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_C=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_V(T_C)$ may be calculated from this relationship: $I_V(T_C)=I_V$ (25° C) $e^{[-.0188/°C\,(T_C-25°C)]}$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

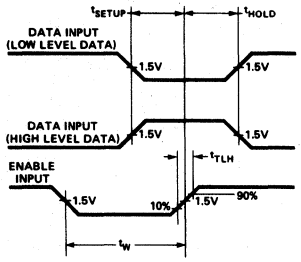


Figure 1. Timing Diagram of 5082-7300 Series Logic.

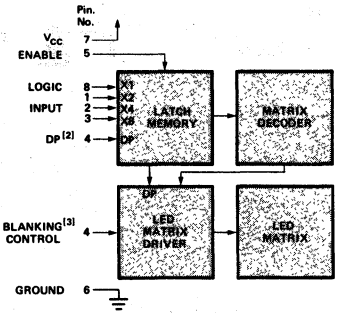


Figure 2. Block Diagram of 5082-7300 Series Logic.

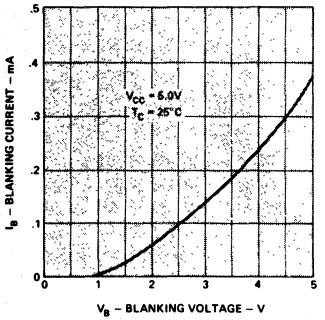


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

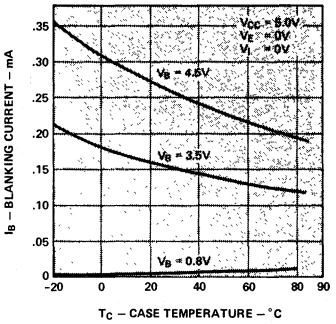


Figure 4. Typical Blanking Control Input Current vs. Temperature 5082-7340.

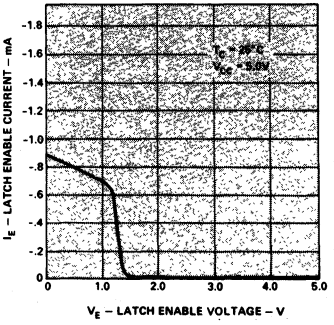


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

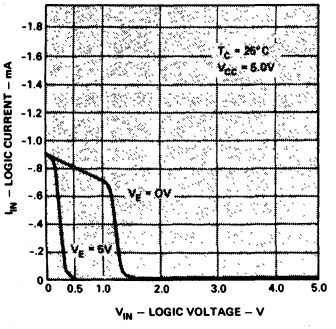


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE

BCD DATA[1]					
X_8	X_4	X_2	X_1	5082-7300/7302	5082-7340
L	L	L	L		
L	L	L	H		
L	L	H	L		
L	L	H	H		
L	H	L	L		
L	H	L	H		
L	H	H	L		
L	H	H	H		
H	L	L	L		
H	L	L	H		
H	L	H	L		
H	L	H	H	(BLANK)	
H	H	L	L	(BLANK)	
H	H	L	H		
H	H	H	L	(BLANK)	
H	H	H	H	(BLANK)	

DECIMAL PT.[2]	ON	V_{DP} = L
	OFF	V_{DP} = H
ENABLE[1]	LOAD DATA	V_E = L
	LATCH DATA	V_E = H
BLANKING[3]	DISPLAY ON	V_B = L
	DISPLAY OFF	V_B = H

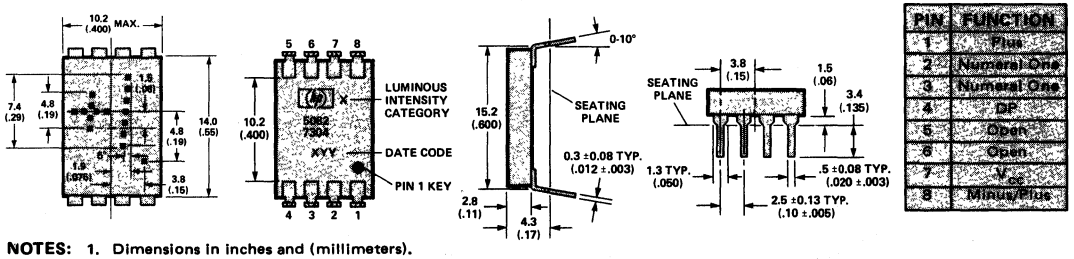
Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range character is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

NOTES: 1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches. (± .38 mm)

5082–7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN 1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Fig. 7 cutoff.
H: Line switching transistor in Fig. 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_s	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to figure 7 for recommended resistor values.

TYPICAL DRIVING CIRCUIT FOR 5082-7304.

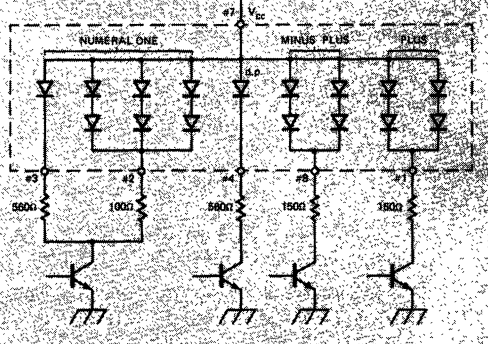


Figure 7.

Electrical/Optical Characteristics (T_C = -20°C TO +85°C, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				0.8		gm

HEWLETT PACKARD

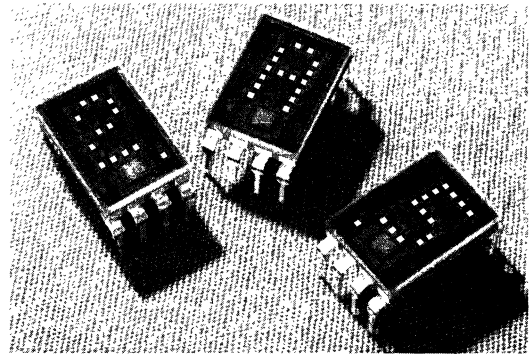
NUMERIC AND HEXADECIMAL DISPLAYS FOR INDUSTRIAL APPLICATIONS

5082-7356
5082-7357
5082-7358
5082-7359

TECHNICAL DATA MARCH 1980

Features

- **CERAMIC/GLASS PACKAGE**
- **ADDED RELIABILITY**
- **NUMERIC 5082-7356/-7357**
  - **0-9, Test State, Minus Sign, Blank States Decimal Point**
    - **7356 Right Hand D.P.**
    - **7357 Left Hand D.P.**
- **HEXADECIMAL 5082-7359**
  - **0-9, A-F, Base 16 Operation Blanking Control, Conserves Power No Decimal Point**
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY**
  - **8421 Positive Logic Input and Decimal Point**
- **4 x 7 DOT MATRIX ARRAY**
  - **Shaped Character, Excellent Readability**
- **STANDARD DUAL-IN-LINE PACKAGE**
  - **15.2mm x 10.2mm (.6 inch x .4 inch)**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  - **Assures Uniformity of Light Output from Unit to Unit within a Single Category**



Description

The HP 5082-7350 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4mm (0.29 inch) displays for use in adverse industrial environments.

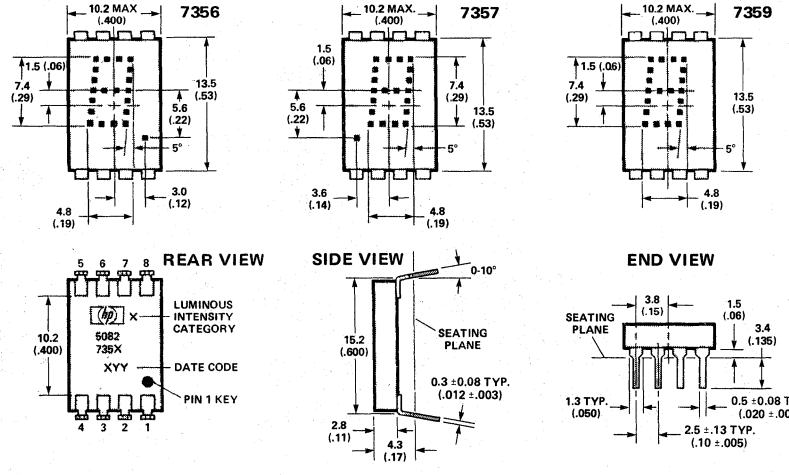
The 5082-7356 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " – " sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point. Typical applications include control systems, instrumentation, communication systems and transportation equipment.

The 5082-7357 is the same as the 5082-7356 except that the decimal point is located on the left-hand side of the digit.

The 5082-7359 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a "±1." overrange display, including a right hand decimal point.

Package Dimensions



PIN	FUNCTION	
	5082-7356 AND 7357 NUMERIC	5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015").
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	0		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = 0°C to +70°C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_V	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}				0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}	V_{CC}=4.5V			0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W; 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

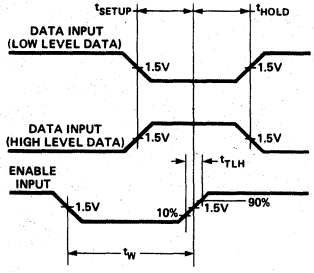


Figure 1. Timing Diagram of 5082-7350 Series Logic.

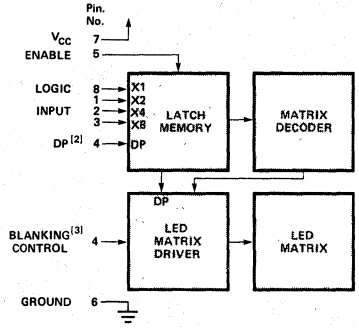


Figure 2. Block Diagram of 5082-7350 Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	A	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

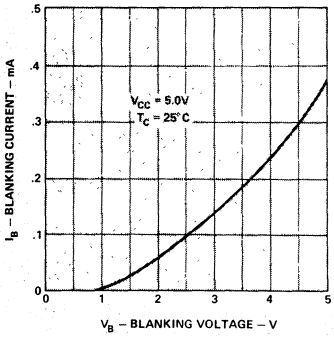


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

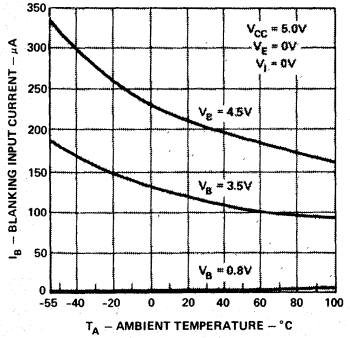


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

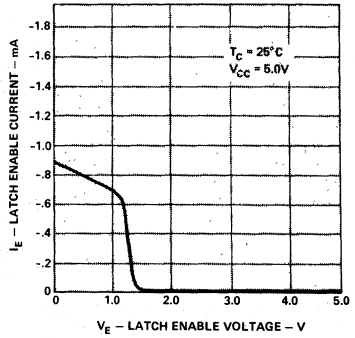


Figure 5. Typical Latch Enable Input Current vs. Voltage.

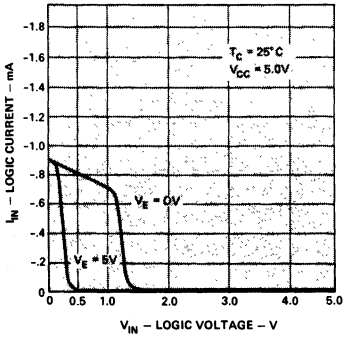


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

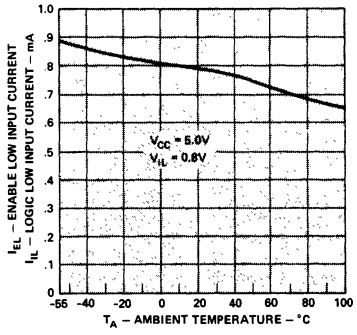


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

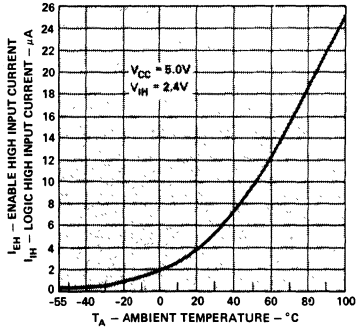


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-7350 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

These hermetic displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling). or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

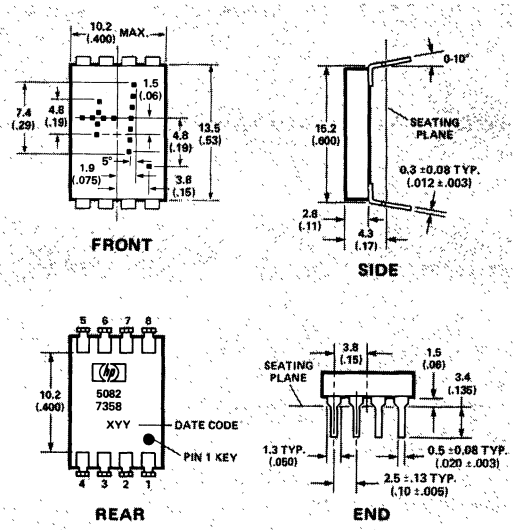
CONTRAST ENHANCEMENT

The 5082-7350 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range character is available. This display module comes in the same package as the 5082-7350 series numeric indicator and is completely compatible with it.

Package Dimensions



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

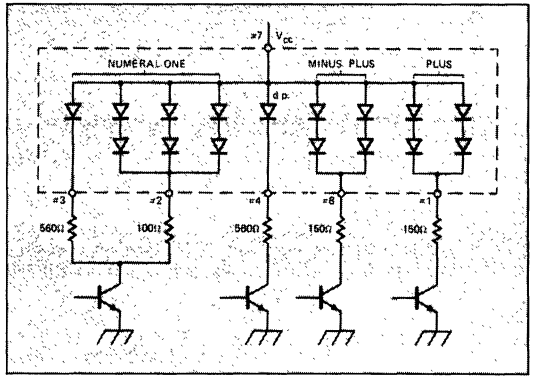


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = 0°C to 70°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

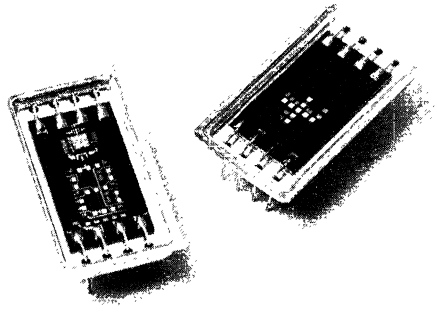
SOLID STATE NUMERIC INDICATOR

5082-7010
5082-7011

TECHNICAL DATA MARCH 1980

Features

- **RUGGED, SHOCK RESISTANT, HERMETIC**
- **DESIGNED TO MEET MIL STANDARDS**
- **INCLUDES DECODER/DRIVER**
  BCD Inputs
- **TTL/DTL COMPATIBLE**
- **CONTROLLABLE LIGHT OUTPUT**
- **5 x 7 LED MATRIX CHARACTER**



Description

The HP 5082-7010 solid state numeric indicator with built-in decoder/driver provides a hermetically tested 6.8mm (0.27 in.) display for use in military or adverse industrial environments. Typical applications include ground, airborne and shipboard equipment, fire control systems, medical instruments, and space flight systems.

The 5082-7010 is a modified 5x7 matrix display that indicates the numerals 0-9 when presented with a BCD code. The BCD code is negative logic with blanks displayed for invalid codes. A left-hand decimal point is included which must be externally current limited.

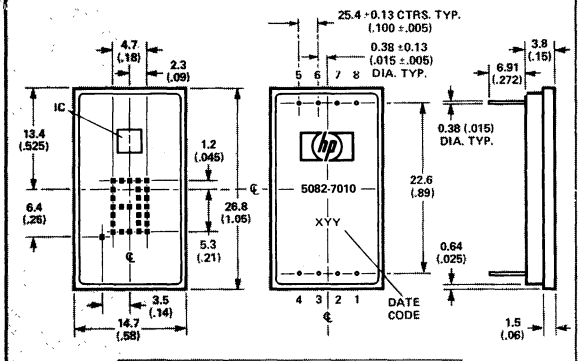
The 5082-7011 is a companion plus/minus sign in the same hermetically tested package. Plus/minus indications require only that voltage be applied to two input pins.

Both displays allow luminous intensity to be varied by changing the DC drive voltage or by pulse duration modulation of the LED voltage.

SOLID STATE DISPLAYS

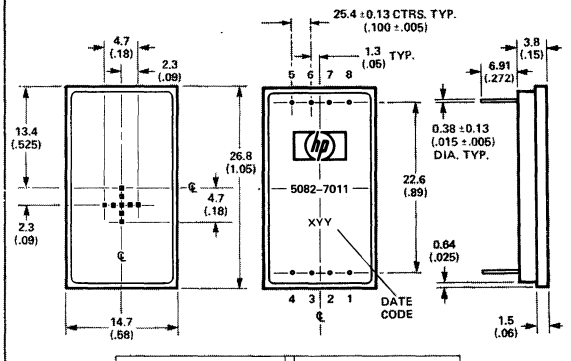
Package Dimensions

5082-7010



PIN	FUNCTION	PIN	FUNCTION
1	Input 1	5	Input 4
2	V_{DP}	6	Ground
3	V_{LED}	7	V_{CC}
4	Input 8	8	Input 2

5082-7011



PIN	FUNCTION	PIN	FUNCTION
1	NC	5	NC
2	NC	6	Ground
3	Plus	7	Minus/Plus
4	NC	8	NC

Notes:
1. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm. (±0.015 inches).
2. All dimensions in millimetres and (inches).
3. The package and mounting pins are tin plated Kovar.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	−65	+100	°C
Operating Temperature, Case	T_C	−55	+95	°C
Logic Supply Voltage to Ground	V_{CC}	−0.5	+7.0	V
Logic Input Voltage	V_I	−0.5	+5.5	V
LED Supply Voltage to Ground	V_{LED} [1]	−0.5	+5.5	V
Decimal Point Current	I_{DP}		−10	mA

Note: 1. Above T_C = 65°C derate V_{LED} per derating curve in Figure 10.

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Logic Supply Voltage	V_{CC}	4.5	5.0	5.5	V
LED Supply Voltage, Display Off	V_{LED}	−0.5	0	+1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V
Decimal Point Current	I_{DP}[2]	0	−5.0	−10.0	mA
Logic Input Voltage, "H" State	V_{IH}	2.0		5.5	V
Logic Input Voltage, "L" State	V_{IL}	0		0.8	V

Note: 2. Decimal point current must be externally current limited. See application information.

Electrical/Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions		Min.	Typ.[4]	Max.	Unit
Logic Supply Current	I_{CC}	V_{CC} = 5.5V			45	75	mA
LED Supply Current	I_{LED} [3] [5]	V_{CC}	V_{LED}				mA
		5.5V	5.5V		255	350	
		5.5V	4.2V		170	235	
		5.5V	3.5V		125		
Logic Input Current, "H" State (ea. input)	I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V				100	µA
Logic Input Current, "L" State (ea. input)	I_{IL}	V_{CC} = 5.5V V_{IL} = 0.4V				−1.6	mA
Decimal Point Voltage Drop	V_{LED} − V_{DP}	I_{DP} = −10mA			1.6	2.0	V
Power Dissipation	P_T [3] [5]	V_{CC}	V_{LED}				W
		5.5V	5.5V		1.7	2.3	
		5.5V	4.2V		1.0	1.4	
		5.5V	3.5V		0.7		
Luminous Intensity per LED (digit avg.)	I_V	V_{LED}	T_C				µcd
		5.5V	25°C	60	115		
		4.2V	25°C	40	80		
		3.5V	25°C		50		
Peak Wavelength	λ_{peak}				655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$				30		nm
Weight					4.9		gram

Notes:
3. With numeral 8 displayed.
4. All typical values at T_C = 25°C.
5. T_C = 0°C to 65°C for V_{LED} = 5.5V.

Truth Table

Character	Logic X8	X4	X2	X1	
0	H	H	H	H	0
1	H	H	H	L	1
2	H	H	L	H	2
3	H	H	L	L	3
4	H	L	H	H	4
5	H	L	H	L	5
6	H	L	L	H	6
7	H	L	L	L	7
8	L	H	H	H	8
9	L	H	H	L	9
Blank	L	H	L	H	
Blank	L	H	L	L	
Blank	L	L	H	H	
Blank	L	L	H	L	
Blank	L	L	L	H	
Blank	L	L	L	L	

V_{IL} = 0.0 to 0.8V
V_{IH} = 2.0 to 5.5V

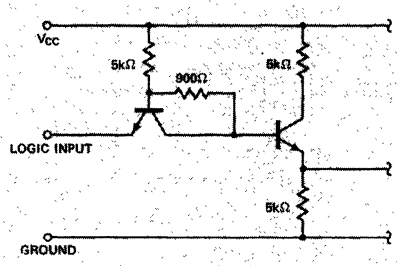


Figure 1. Equivalent input circuit of the 5082-7010 decoder. Note: Display metal case is isolated from ground pin #6.

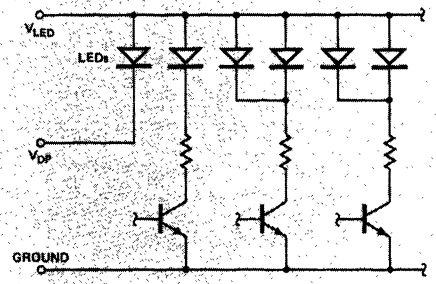


Figure 2. Equivalent circuit of the 5082-7010 as seen from LED and decimal point drive lines.

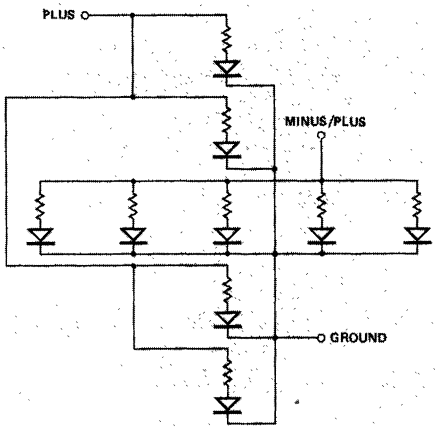


Figure 3. Equivalent circuit of 5082-7011 plus/minus sign. All resistors 345Ω typical. Note: Display metal case is isolated from ground pin #6.

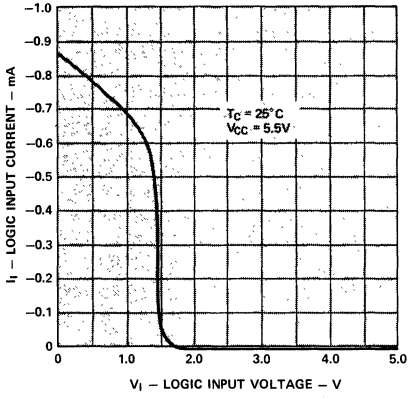


Figure 4. Input current as a function of input voltage, each input.

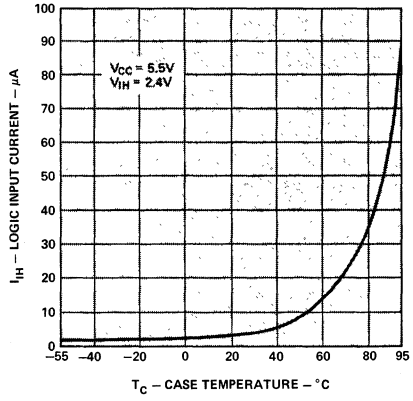


Figure 5. Logic "H" input current as a function of case temperature, each input.

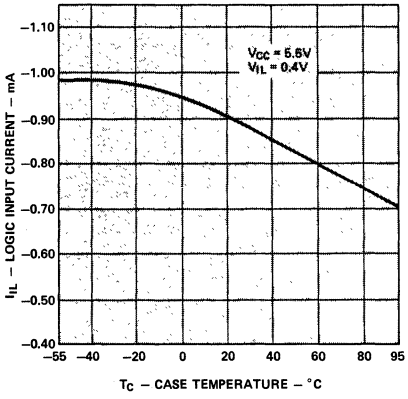


Figure 6. Logic "L" input current as a function of case temperature, each input.

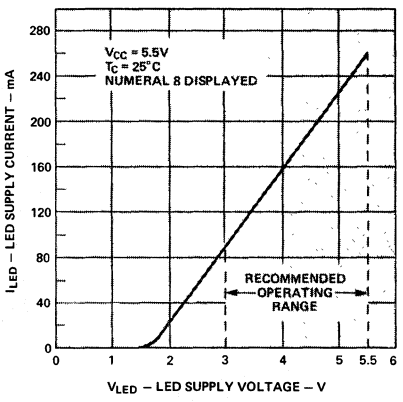


Figure 7. LED supply current as a function of LED supply voltage.

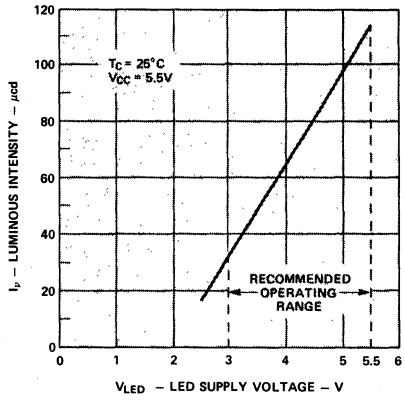


Figure 8. Luminous intensity per LED (digit average) as a function of LED supply voltage.

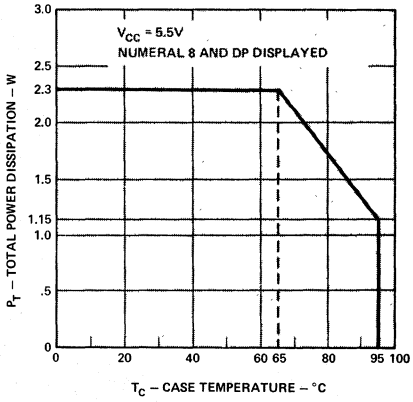


Figure 9. Maximum power derating as a function of case temperature.

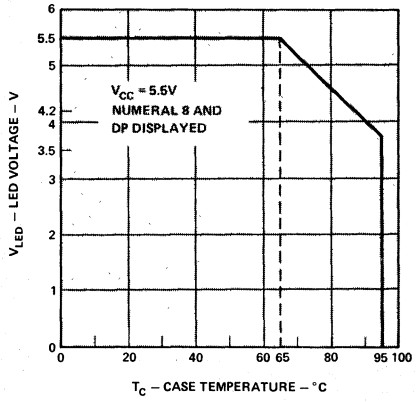


Figure 10. LED voltage derating as a function of case temperature.

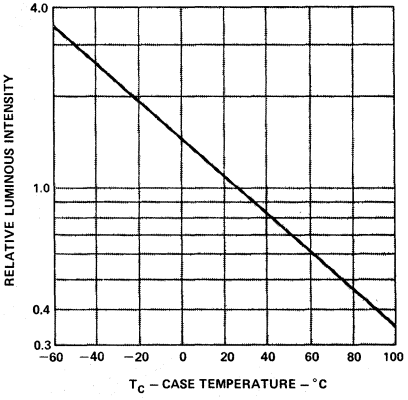


Figure 11. Relative luminous intensity as a function of case temperature at fixed current level.

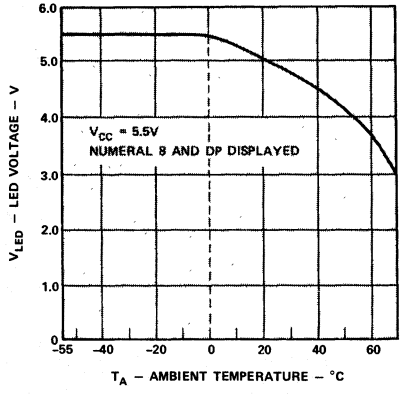


Figure 12. LED voltage derating as a function of ambient temperature, display soldered into P.C. board without heat sink.

Solid State Plus/Minus Sign

For display applications requiring ± designation, the 5082-7011 solid state plus/minus sign is available. This display module comes in the same package as the 5082-7010 numeric indicator and is completely compatible with it. Plus or minus information can be indicated by supplying voltage to one (minus sign) or two (plus sign) input leads. A third lead is provided for the ground connection. Luminous intensity is controlled by changing the LED drive voltage. Each LED has its own built-in 345Ω (nominal) current limiting resistor. Therefore, no external current limiting is required for voltages at 5.5V or lower. Like the numeric indicator, the -7011 plus/minus sign is TTL/DTL compatible.

Truth Table

CHARACTER	PIN	
	3	7
+	H	H
–	L	H
Blank	L	L

V_L = –0.5 to 1.0V

V_H = 3.0 to 5.5V

Electrical/Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
LED Supply Current	I_{LED}	V_{LED} = 5.5V		105	150	mA
		V_{LED} = 4.2V		70	100	
Power Dissipation	P_T	V_{LED} = 5.5V		0.6	0.9	W
		V_{LED} = 4.2V		0.3	0.6	
Luminous Intensity per LED (Digit Avg.)	I_v[2]	V_{LED} = 5.5V	60	115		µcd
		V_{LED} = 4.2V	40	80		
		V_{LED} = 3.5V		50		
Peak Wavelength	λ_{peak}			655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$			30		nm
Weight				4.9		gram

Notes: 1. All typical values at T_C = 25°C
2. At T_C = 25°C

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	–65	+100	°C
Operating Temperature, Case	T_C	–55	+95	°C
Plus, Plus/Minus Input Potential to Ground	V_{LED}	–0.5	5.5	V

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
LED Supply Voltage, Display Off	V_{LED}	–0.5	0	1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V

Applications

Decimal Point Limiting Resistor

The decimal point of the 5082-7010 display requires an external current limiting resistor, between pin 2 and ground. Recommended resistor value is 220Ω, 1/4 watt.

Mounting

The 5082-7010 and 5082-7011 displays are packaged with two rows of 4 contact pins each in a DIP configuration with a row center line spacing of 0.890 inches.

Normal mounting is directly onto a printed circuit board. If desired, these displays may be socket mounted using contact strip connectors such as Augat's 325-AGI or AMP 583773-1 or 583774-1.

Heat Sink Operation

Optimum display case operating temperature for the 5082-7010 and 7011 displays is T_C=0°C to 70°C as measured on back surface. Maintaining the display case operating temperature within this range may be achieved by mounting the display on an appropriate heat sink or metal core printed circuit board. Thermal conducting compound such as Wakefield 120 or Dow Corning 340 can be used between display and heat sink. See figure 10 for V_{LED} derating vs. display case temperature.

Operation Without Heat Sink

These displays may also be operated without the use of a heat sink. The thermal resistance from case to ambient for these displays when soldered into a printed circuit board is nominally θ_{CA}=30°C/W. See figure 12 for V_{LED} derating vs. ambient temperature.

Cleaning

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

HEWLETT PACKARD

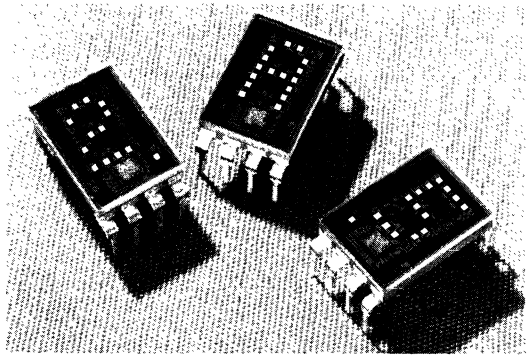
HERMETIC NUMERIC AND HEXADECIMAL DISPLAYS FOR HIGH RELIABILITY APPLICATIONS

5082-7391 (4N51)
5082-7392 (4N52)
5082-7393 (4N53)
5082-7395 (4N54)

TECHNICAL DATA MARCH 1980

Features

- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HERMETICITY GUARANTEED**
- **TXV SCREENING AVAILABLE**
- **GOLD PLATED LEADS**
- **HIGH TEMPERATURE STABILIZED**
- **NUMERIC**
  5082-7391 Right Hand D.P.
  5082-7392 Left Hand D.P.
- **HEXADECIMAL**
  5082-7395
- **TTL COMPATIBLE**
- **DECODER/DRIVER WITH 5 BIT MEMORY**
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7390 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory are hermetically tested 7.4mm (0.29 inch) displays for use in military and aerospace applications.

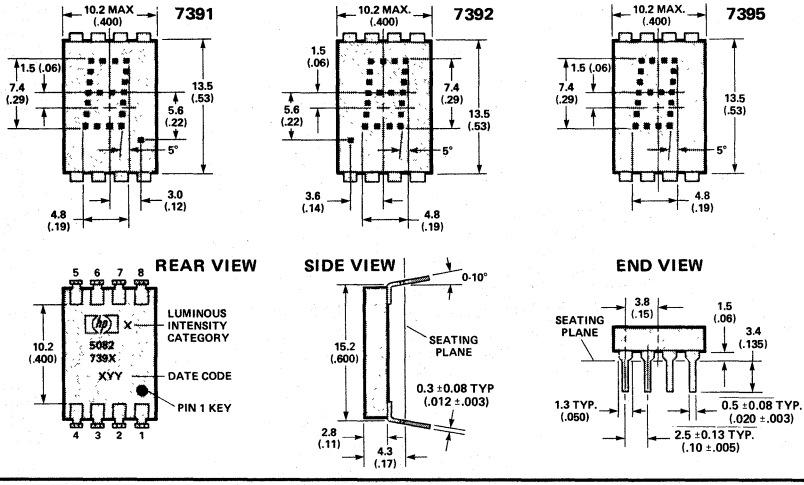
The 5082-7391 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " −" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point. Typical applications include control systems, instrumentation, communication systems and transportation equipment.

The 5082-7392 is the same as the 5082-7391 except that the decimal point is located on the left-hand side of the digit.

The 5082-7395 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7393 is a "±1." overrange display, including a right hand decimal point.

Package Dimensions*



PIN	FUNCTION	
	5082-7391 AND 7392 NUMERIC	5082-7395 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.

*JEDEC Registered Data.

SOLID STATE DISPLAYS

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics* (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight**				1.0		gm
Leak Rate					$5x10^{-7}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7395. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

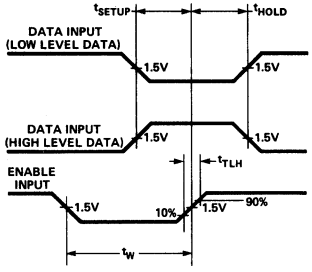


Figure 1. Timing Diagram of 5082-7390 Series Logic.

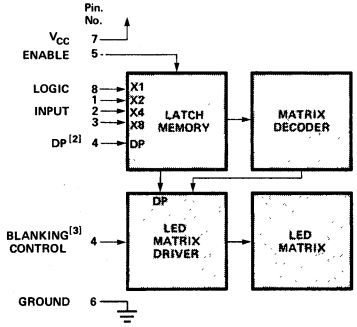


Figure 2. Block Diagram of 5082-7390 Series Logic.

TRUTH TABLE

BCD DATA[1]				5082-7391/7392	5082-7395
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	-	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F

DECIMAL PT.[2]	ON	V_{DP} = L
	OFF	V_{DP} = H
ENABLE[1]	LOAD DATA	V_E = L
	LATCH DATA	V_E = H
BLANKING[3]	DISPLAY-ON	V_B = L
	DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7391 and 5082-7392 displays.
3. The blanking control input, B, pertains only to the 5082-7395 hexadecimal display. Blanking input has no effect upon display memory.

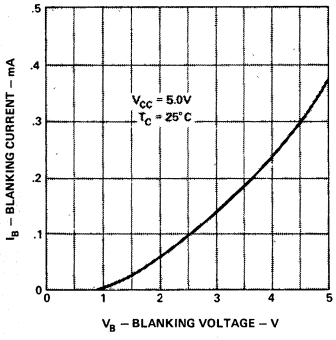


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7395.

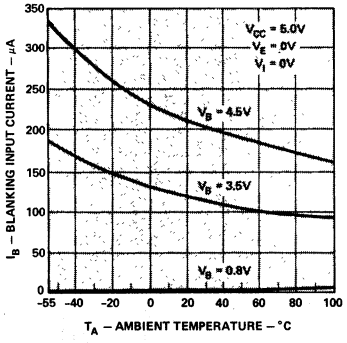


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7395.

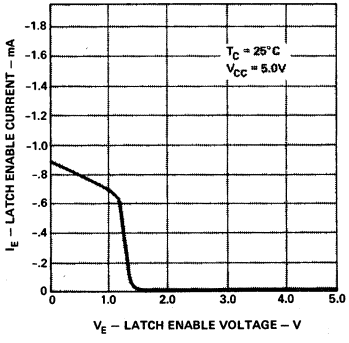


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

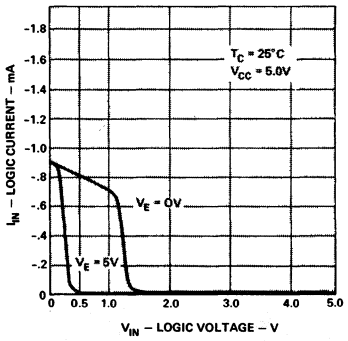


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

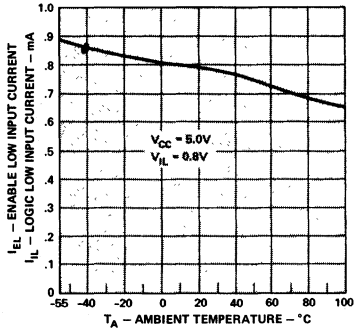


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

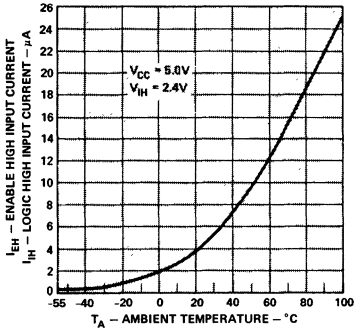


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-7390 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

5082-7390 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5×10^{-7} cc/sec and a standard dye penetrant gross leak test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

5082-7390 series displays are 100% preconditioned by 24 hour storage at 125°C.

CONTRAST ENHANCEMENT

The 5082-7390 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

*JEDEC Registered Data.

High Reliability Test Program

Hewlett-Packard provides standard high reliability test programs, patterned after MIL-M-38510 in order to facilitate the use of HP products in military programs.

HP offers two levels of high reliability testing:

The TXV prefix indentifies a part which has been preconditioned and screened per Table 1.

The TXVB prefix identifies a part which has been preconditioned and screened per Table 1, and comes from a lot which has been subjected to the Group B tests described in Table 2.

Standard Product	With TXV Screening	Plus Group B
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	4N51TXVB
4N52	4N52TXV	4N52TXVB
4N54	4N54TXV	4N54TXVB
4N53	4N53TXV	4N53TXVB
ALTERNATE PART NUMBER SYSTEM		
5082-7391	TXV-7391	TXVB-7391
5082-7392	TXV-7392	TXVB-7392
5082-7395	TXV-7395	TXVB-7395
5082-7393	TXV-7393	TXVB-7393

Table 1. TXV Preconditioning and Screening — 100%.

Examination or Test	MIL-STD-883 Methods	Conditions
1. Internal Visual Inspection	HP Procedure A-5956-7572-52	
2. Electrical Test: I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}.		Per Electrical/Optical Characterstics.
3. High Temperature Storage	1008	125°C, 168 hours.
4. Temperature Cycling	1010	−65°C to +125°C, 10 cycles.
5. Acceleration	2001	2,000 G, Y_1 orientation.
6. Helium Leak Test	1014	Condition A
7. Gross Leak Test	1014	Condition D
8. Electrical Test: Same as Step 2		
9. Burn-in	1015	T_A=100°C, t=168 hours, at V_{CC}=5.0V and cycling through logic at 1 character per sec.
10. Electrical Test as in Step 2		
11. Sample Electrical Test Over Temperature: I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}		Per Electrical Characteristics, T_A = -55°C, LTPD = 7
12. Sample Electrical Test Over Temperature I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}		Per Electrical Characteristics, T_A = +100°C, LTPD = 7
13. External Visual	2009	

Table 2. Group B.

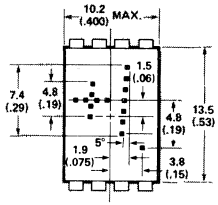
Examination or Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD
Subgroup 1 Physical Dimensions	2008	Package Dimensions per Product Outline Drawing.	20
Subgroup 2 Solderability Temperature Cycling Thermal Shock Hermetic Seal Moisture Resistance End Points: Electrical Test	 2003 1010 1011 1014 1004 	 Immersion within 0.062" of seating plane 260°C, t=5 sec., omit aging. 10 cycles −65°C to +125°C Test Condition A Condition A and Condition D Omit initial conditioning. Same as Step 2, Table 1.	15
Subgroup 3 Shock — Non-operating Vibration Variable Frequency Constant Acceleration End Points: Electrical Test	 2002 2007 2001 	 1500 G, t=0.5ms, 5 blows in each orientation X_1, Y_1, Y_2. Non-operating. 2,000 G, Y_1 orientation. Same as Step 2, Table 1.	15
Subgroup 4 Terminal Strength End Points: Hermetic Seal	 2004 1014	 Test Condition B2. Condition A and Condition D	15
Subgroup 5 Salt Atmosphere	 1009	 Test Condition A	15
Subgroup 6 High Temperature Life End Points: Electrical Test	 1008 	 T_A= 125°C, non-operating, t=1000 hours. Same as Step 2, Table 1.	λ=7
Subgroup 7 Steady State Operating Life End Points: Electrical Test	 1005 	 T_A=100°C, t=1000 hours, at V_{CC}=5.0V and cycling through logic at 1 character per second. Same as Step 2, Table 1.	λ=5

*JEDEC Registered Data.

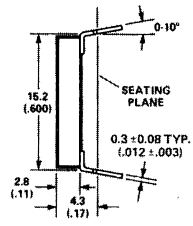
Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7393 over range character is available.This display module comes in the same package as the 5082-7390 series numeric indicator and is completely compatible with it.

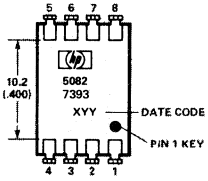
Package Dimensions*



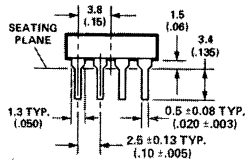
FRONT



SIDE



REAR



END

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

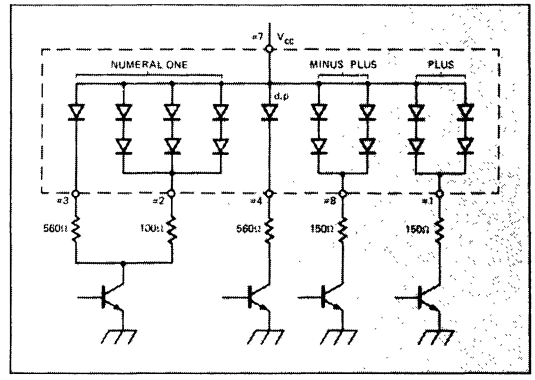


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

5082-7393 (T_A = -55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight**				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

*JEDEC Registered Data. **Non Registered Data.

HEWLETT PACKARD

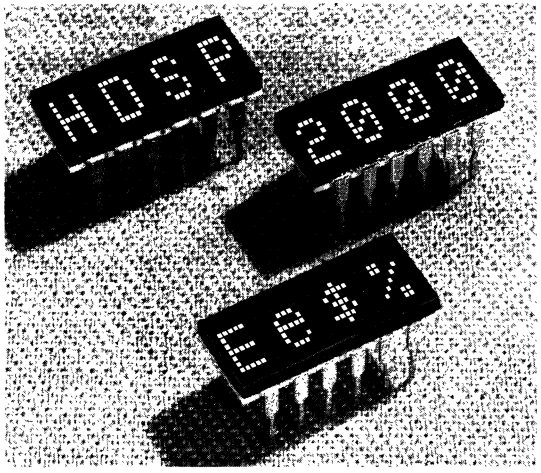
RED FOUR CHARACTER SOLID STATE ALPHANUMERIC DISPLAY

HDSP-2000

TECHNICAL DATA MARCH 1980

Features

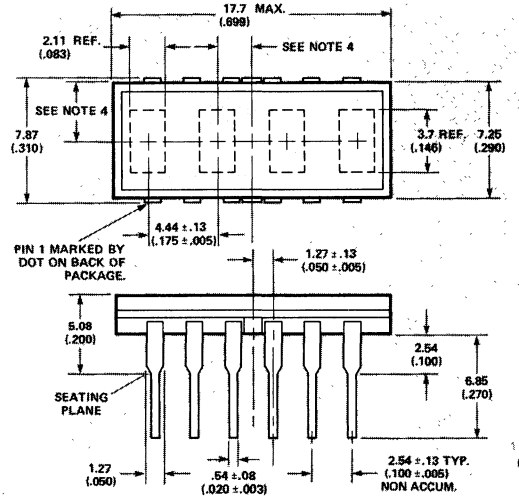
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **CERAMIC 7.62 mm (.3 in.) DIP**
  Integral Red Glass Contrast Filter
- **WIDE VIEWING ANGLE**
- **END STACKABLE 4 CHARACTER PACKAGE**
- **PIN ECONOMY**
  12 Pins for 4 Characters
- **TTL COMPATIBLE**
- **5x7 LED MATRIX DISPLAYS FULL ASCII CODE**
- **RUGGED, LONG OPERATING LIFE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Ease of Package to Package Brightness Matching



Description

The HP HDSP-2000 display is a 3.8mm (0.15 inch) 5x7 LED array for display of alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7 bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, point of sale equipment, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

SOLID STATE DISPLAYS

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature Range, T_A[2] ..... −20°C to +70°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation at T_A=25°C[1,2,6] ..... 1.70 Watts
Maximum Solder Temperature 1.59mm (.063") Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.6		V_{CC}	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	−20		70	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified.)

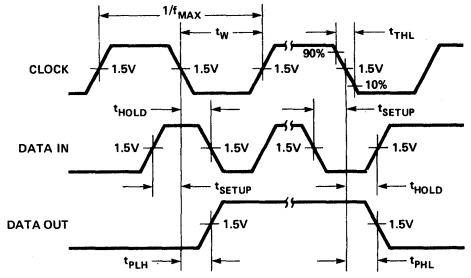
Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA
				V_B = 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25V, V_{COL} = 3.5V	V_B=0.4V			1.5	mA
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B=2.4V		335	410	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{vPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[4] V_B=2.4V		105	200		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B,Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = −0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LEDs on per character, V_B = 2.4V			0.66		W
Peak Wavelength		λ_{PEAK}				655		nm
Dominant Wavelength[5]		λ_d				639		nm

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with 4 characters illuminated.

NOTES:
1. Maximum absolute dissipation is with the device in a socket having a thermal resistance from pins to ambient of 35°C/watt.
2. The device should be derated linearly above 25°C at 16mW/°C (see Electrical Description on page 3).
3. The characters are categorized for Luminous Intensity with the intensity category designated by a letter code on the bottom of the package.
4. T_j refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from V_{CC} = V_B = V_{COL} = 5.25 Volts, 20 LEDs on per character.
7. The luminous stearance of the LED may be calculated using the following relationships:

L_V (Lux) = I_V (Candela)/A (Metre)^2
L_V (Footlamberts) = πI_V (Candela)/A (Foot)^2
A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -20°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2000 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The -2000 can be operated over a wide range of temperature and supply voltages. Full power operation at T_A = 25°C (V_{CC} = V_B = V_{COL} = 5.25V) is possible by providing a total thermal resistance from the seating plane of the pins to ambient of 35°C/W/cluster maximum. For operation above T_A = 25°C, the maximum device dissipation should be derated above 25°C at 16mW/°C (see Figure 2). Power derating can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The -2000 display has an integral contrast enhancement filter in the glass lens. Additional front panel contrast filters may by desirable in most actual display applications. Some suggested filters are Panelgraphic Ruby Red 60, SGL Homalite H100-1605 and Plexiglass 2423. Hewlett-Packard Application Note 964 treats this subject in greater detail.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2000 four character alphanumeric display has been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection such that display strings of up to 80 digits may be driven from a single character generator. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the HDSP-2000. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The reference current for the current mirror is generated from the output voltage of the V_B input buffer applied across the resistor R. The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation is depicted in the block diagram of Figure 6. In this circuit, binary input data for digit 4, column 1 is decoded by the 7 line output ROM and then loaded into the 7 on board shift register locations 1 through 7 through a parallel-in-serial-out shift register. Column 1 data for digits 3, 2 and 1 is similarly decoded and shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

The time frame, t + T, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary

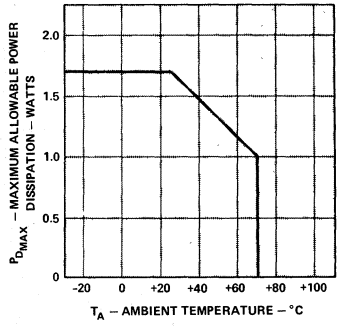


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

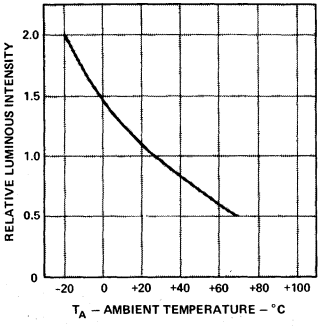


Figure 3. Relative Luminous Intensity vs. Temperature.

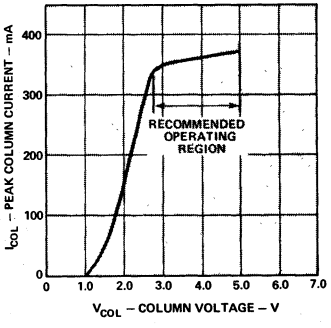


Figure 4. Peak Column Current vs. Column Voltage.

to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With 5 columns to be addressed, this refresh rate then gives a value for the time t + T of:

$1/[5 \times (100)] = 2$ msec.

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%. For longer display strings operation at column duty factors of less than 10% will still provide adequate display intensity in most applications. For further applications information, refer to HP Application Note 966 and Application Note 1001.

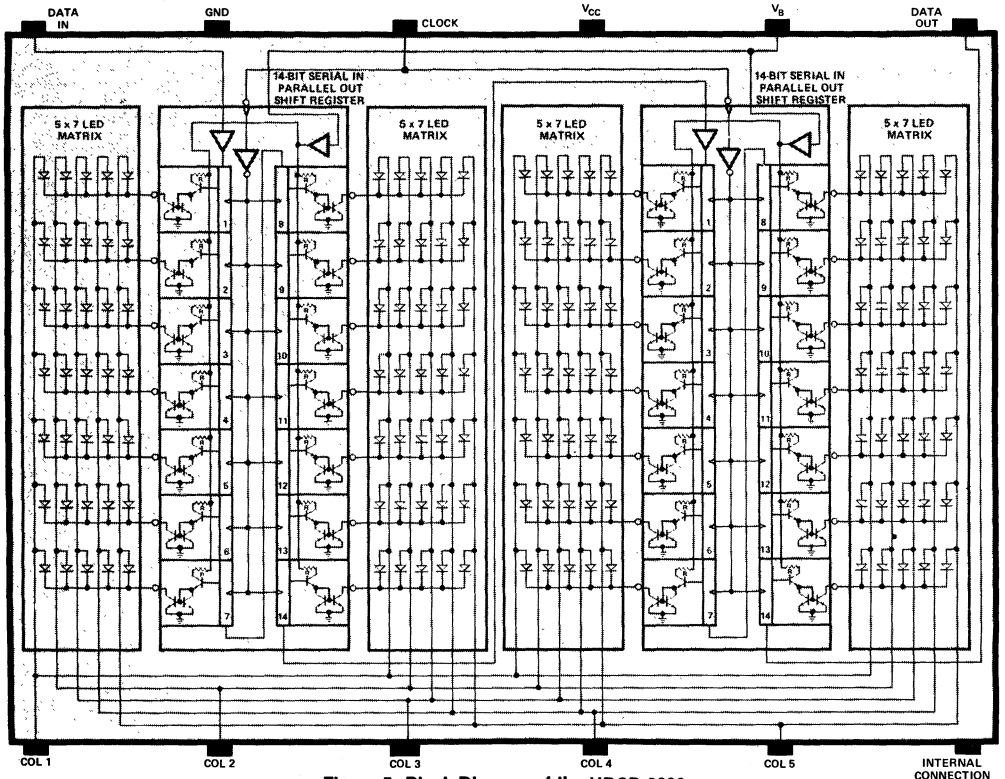


Figure 5. Block Diagram of the HDSP-2000.

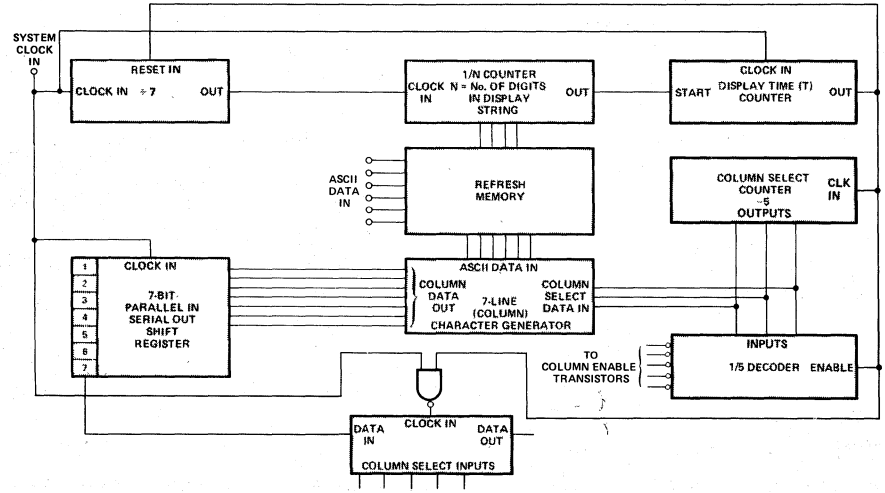


Figure 6. Block Diagram of a Basic Display System.

HEWLETT PACKARD

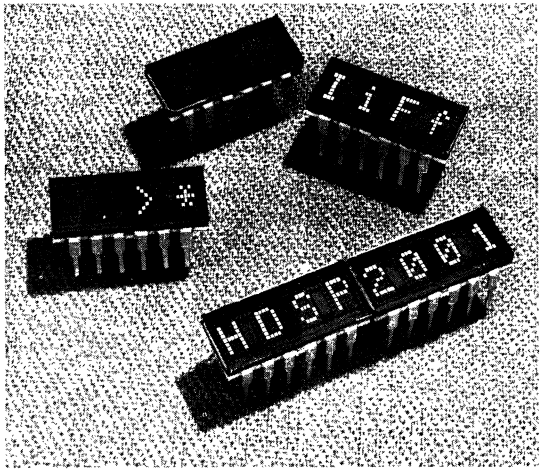
YELLOW FOUR CHARACTER SOLID STATE ALPHANUMERIC DISPLAY

HDSP-2001

TECHNICAL DATA MARCH 1980

Features

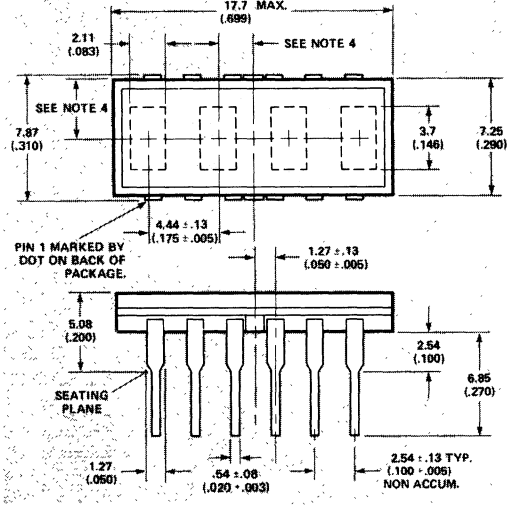
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **CERAMIC 7.62 mm (.3 in.) DIP**
- **WIDE VIEWING ANGLE**
- **END STACKABLE 4 CHARACTER PACKAGE**
- **PIN ECONOMY**
  12 Pins for 4 Characters
- **TTL COMPATIBLE**
- **5x7 LED MATRIX DISPLAYS FULL ASCII CODE**
- **RUGGED, LONG OPERATING LIFE**
- **CATEGORIZED FOR LUMINOUS INTENSITY AND COLOR**
  Assures Ease of Package to Package Brightness and Color Matching

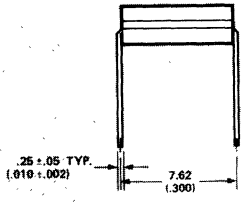


Description

The HP HDSP-2001 display is a 3.8mm (0.15 inch) 5x7 yellow LED array for display of alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, avionics, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

SOLID STATE DISPLAYS

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature Range, T_A[2] ..... −20°C to +70°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation at $T_A = 25°C$[1,2,6] ..... 1.70 Watts
Maximum Solder Temperature 1.59mm (.063") Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.75		V_{CC}	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	−20		70	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified.)

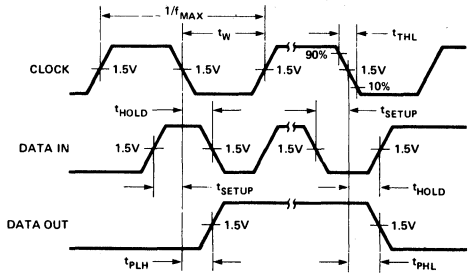
Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, $V_{CLOCK} = V_{DATA}$ = 2.4V, All SR Stages = Logical 1	V_B 0.4V		45	60	mA
				V_B 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25V, V_{COL} = 3.5V	V_B=0.4V			1.5	mA
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B=2.4V		335	410	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{VPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[4], V_B=2.4V		500	750		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	$V_{CC} = V_{COL}$ = 4.75V		2.0			V
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B,Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = −0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.75V, 15 LEDs on per character, V_B = 2.4V			0.68		W
Peak Wavelength		λ_{PEAK}				583		nm
Dominant Wavelength[5]		λ_d				585		nm

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with 4 characters illuminated.

NOTES:
1. Maximum absolute dissipation is with the device in a socket having a thermal resistance from pins to ambient of 35°C/watt/device.
2. The device should be derated linearly above 25°C at 16mW/°C (see Electrical Description on page 3).
3. The characters are categorized for Luminous Intensity and color with the category designated by a letter code on the bottom of the package.
4. T_j refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from $V_{CC} = V_B = V_{COL}$ = 5.25 Volts, 20 LEDs on per character.
7. The luminous stearance of the LED may be calculated using the following relationships:

L_V (Lux) = I_V (Candela)/A (Metre)^2
L_V (Footlamberts) = πI_V (Candela)/A (Foot)^2
A = 8.02 x 10^{-8} M^2 = 8.64 x 10^{-7} $(Foot)^2$



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -20°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2001 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The HDSP-2001 can be operated over a wide range of temperature and supply voltages. Full power operation at T_A = 25°C (V_{CC} = V_B = V_{COL} = 5.25V) is possible by providing a total thermal resistance from the seating plane of the pins to ambient of 35°C/W/device maximum. For operation above T_A = 25°C, the maximum device dissipation should be derated above 25°C at 16mW/°C (see Figure 2). Power derating can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The HDSP-2001 display has an integral untinted glass lens. A front panel contrast filter is desirable in most actual display applications. Some suggested filters are Panelgraphic Gray 10, SGL Homalite H100-1266 Gray and 3M Light Control Film (louvered filters).

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2001 four character alphanumeric display has been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection such that display strings of up to 80 digits may be driven from a single character generator. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the HDSP-2001. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The reference current for the current mirror is generated from the output voltage of the V_B input buffer applied across the resistor R. The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation is depicted in the block diagram of Figure 6. In this circuit, binary input data for digit 4, column 1 is decoded by the 7 line output ROM and then loaded into the 7 on board shift register locations 1 through 7 through a parallel-in-serial-out shift register. Column 1 data for digits 3, 2 and 1 is similarly decoded and shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

The time frame, t + T, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary

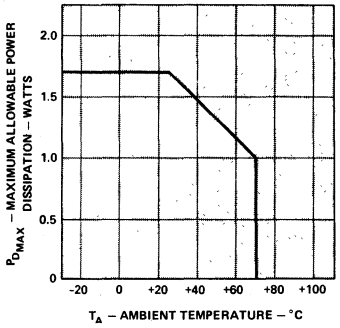


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

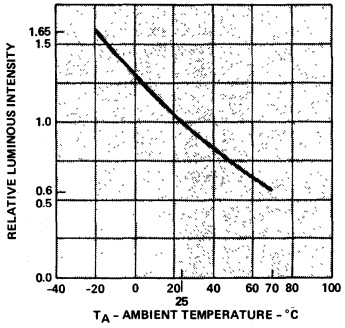


Figure 3. Relative Luminous Intensity vs. Temperature.

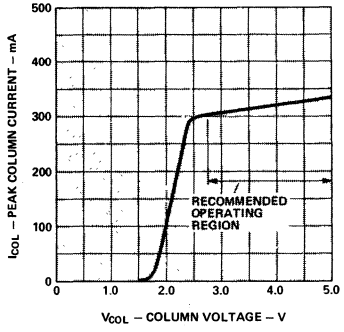


Figure 4. Peak Column Current vs. Column Voltage.

to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With 5 columns to be addressed, this refresh rate then gives a value for the time t + T of:

$1/[5 \times (100)] = 2$ msec.

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%. For longer display strings operation at column duty factors of less than 10% will still provide adequate display intensity in most applications. For further applications information, refer to HP Application Note 1001.

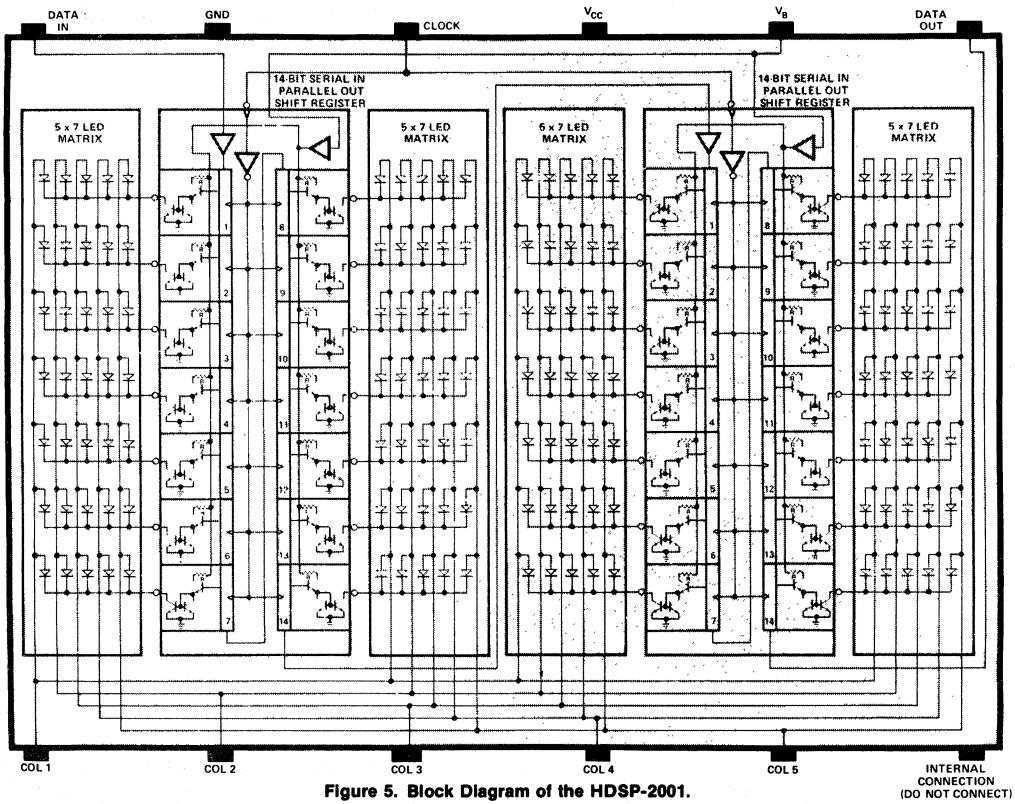


Figure 5. Block Diagram of the HDSP-2001.

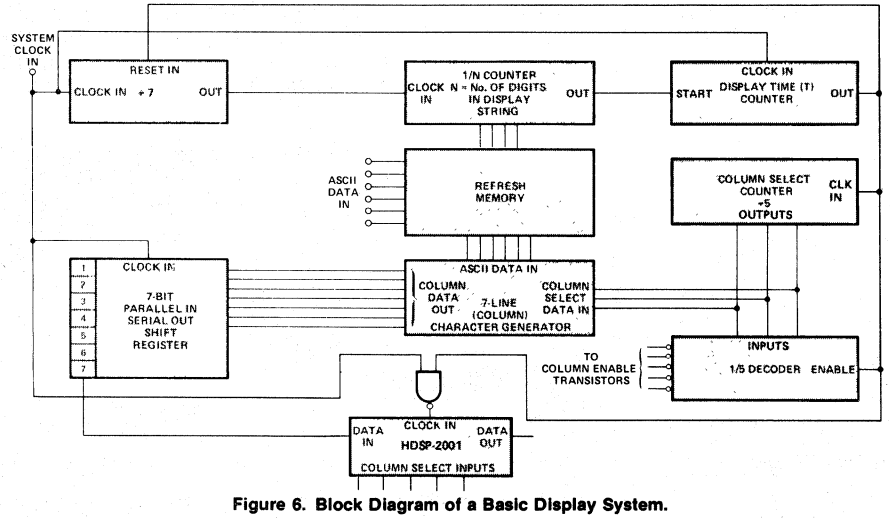


Figure 6. Block Diagram of a Basic Display System.

HEWLETT PACKARD

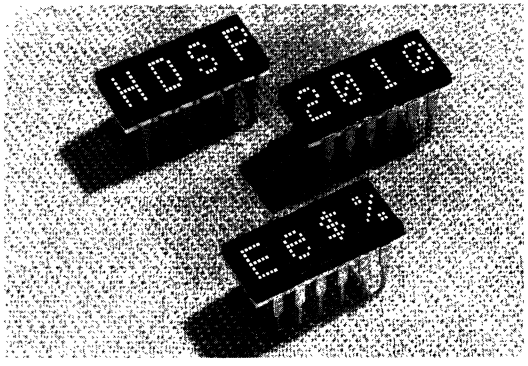
FOUR CHARACTER RED ALPHANUMERIC DISPLAY FOR EXTENDED TEMPERATURE APPLICATIONS

HDSP-2010

TECHNICAL DATA MARCH 1980

Features

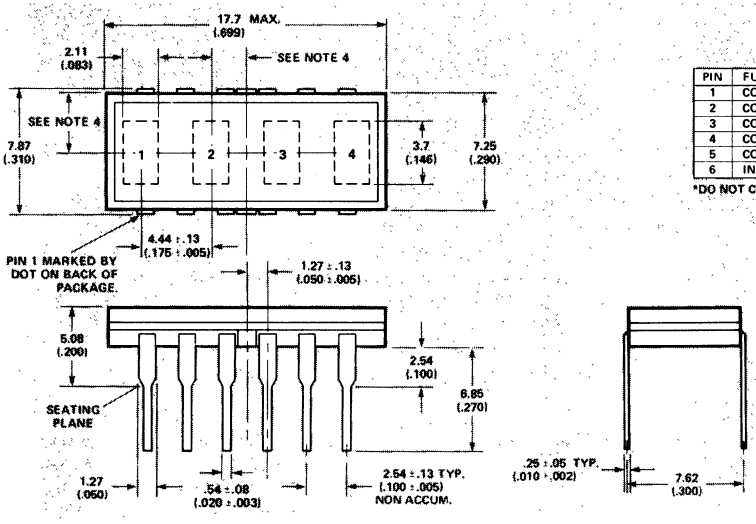
- **OPERATION GUARANTEED TO T_A = -40°C**
- **HERMETICITY GUARANTEED TXV Screening Available**
- **100% TEMPERATURE CYCLED -55°C to +100°C**
- **GOLD PLATED LEADS**
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **CERAMIC 7.62mm (.3 in.) DIP Integral Red Glass Contrast Filter**
- **WIDE VIEWING ANGLE**
- **END STACKABLE 4 CHARACTER PACKAGE**
- **PIN ECONOMY 12 Pins for 4 Characters**
- **TTL COMPATIBLE**
- **5 x 7 LED MATRIX DISPLAYS FULL ASCII CODE**
- **RUGGED, LONG OPERATING LIFE**
- **CATEGORIZED FOR LUMINOUS INTENSITY Assures Ease of Package to Package Brightness Matching**



Description

The HP HDSP-2010 display is designed for use in applications requiring high reliability. The character font is a 3.8mm (0.15 inch) 5 x 7 red LED array for displaying alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, avionics, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

SOLID STATE DISPLAYS

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature Range, T_A[2] ..... −40°C to +70°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation at $T_A = 25°C$[1,2,6] ..... 1.70 Watts
Maximum Solder Temperature 1.59mm (.063") Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.6		V_{CC}	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{TRL}			200	ns
Free Air Operating Temperature Range	T_A	-40		70	°C

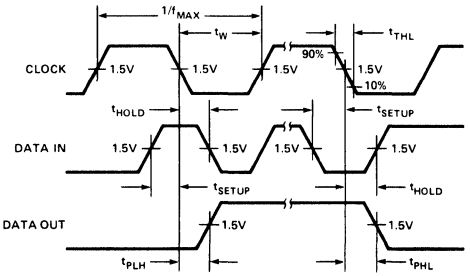
Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified.)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA
				V_B = 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25V, V_{COL} = 3.5V, All SR Stages = Logical 1	V_B = 0.4V			1.5	mA
Column Current at any Column Input		I_{COL}		V_B = 2.4V		350	435	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{VPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[4] V_B = 2.4V		105	200		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	$V_{CC} = V_{COL}$ = 4.75V		2.0			V
V_B, Data Input Threshold Low		V_{IL}					0.8	V
Clock Threshold Low		V_{IL}					0.6	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LEDs on per character, V_B = 2.4V			0.66		W
Peak Wavelength		λ_{PEAK}				655		nm
Dominant Wavelength[5]		λ_d				640		nm
Leak Rate							5×10^{-7}	cc/s

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.
**Power dissipation per package with 4 characters illuminated.

NOTES:
1. Maximum absolute dissipation is with the device in a socket having a thermal resistance from pins to ambient of 35°C/watt/device.
2. The device should be derated linearly above 25°C at 16mW/°C (see Electrical Description on page 3).
3. The characters are categorized for Luminous Intensity and color with the category designated by a letter code on the bottom of the package.
4. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from $V_{CC} = V_B = V_{COL}$ = 5.25 Volts, 20 LEDs on per character.
7. The luminous stearance of the LED may be calculated using the following relationships:
   L_v (Lux) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   A = 5.3×10^{-8} M^2 = 5.8×10^{-7} (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -40°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2010 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The HDSP-2010 can be operated over a wide range of temperature and supply voltages. Full power operation at T_A = 25°C (V_{CC} = V_B = V_{COL} = 5.25V) is possible by providing a total thermal resistance from the seating plane of the pins to ambient of 35°C/W/device maximum. For operation above T_A = 25°C, the maximum device dissipation should be derated above 25°C at 16mW/°C (see Figure 2). Power derating can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The HDSP-2010 display has an integral red glass lens. A front panel contrast filter is desirable in most actual display applications. Some suggested filters are Panel graphic Ruby Red 60, SGL Homalite H100-1605 Red and 3M Light Control Film (louvered filters). OCLI Sungard optically coated glass filters offer superior contrast enhancement.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2010 display provides on-board storage of decoded column data and constant current sinking row drivers for each of 28 rows in the 4 character display. The device consists of four LED matrices and two integrated circuits that form a 28-bit serial input-parallel output (SIPO) shift register, see Figure 5. Each character is a 5 x 7 diode array arranged with the cathodes of each row connected to one constant current sinking output of the SIPO shift register. The anodes of each column are connected together, with the same column of each of the 4 characters connected together (i.e. column 1 of all four characters are connected to pin 1). Any LED within any character may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

Associated with each shift register location is a constant current sinking LED driver, capable of sinking a nominal 13.5 mA. A logical 1 loaded into a shift register location enables the current source at that location. A voltage applied to the appropriate column input turns on the desired LED.

The display is column strobed on a 1 of 5 basis by loading 7 bits of row data per character for a selected column. The data is shifted through the SIPO shift register, one bit location for each high-to-low transition of the clock. When the HDSP-2010 display is operated with pin 1 in the lower left hand corner, the first bit that is loaded into the SIPO shift register will be the information for row 7 of the right most character. The 28th bit loaded into the SIPO shift register will be the information for row 1 of the left most character. When the 28 bits of row data for column 1 have been loaded into the SIPO shift register, the first column is energized for a time period, T, illuminating column 1 in all four characters. Column 1 is turned off and the process is repeated for columns 2 through 5.

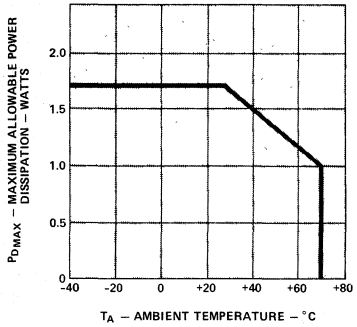


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

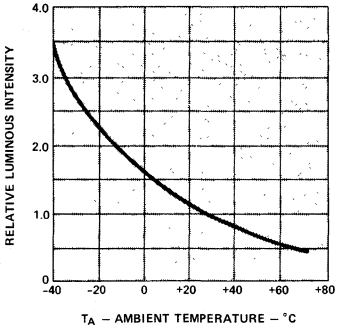


Figure 3. Relative Luminous Intensity vs. Temperature.

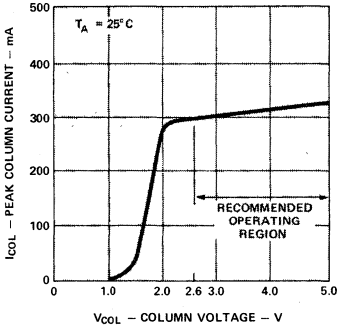


Figure 4. Peak Column Current vs. Column Voltage.

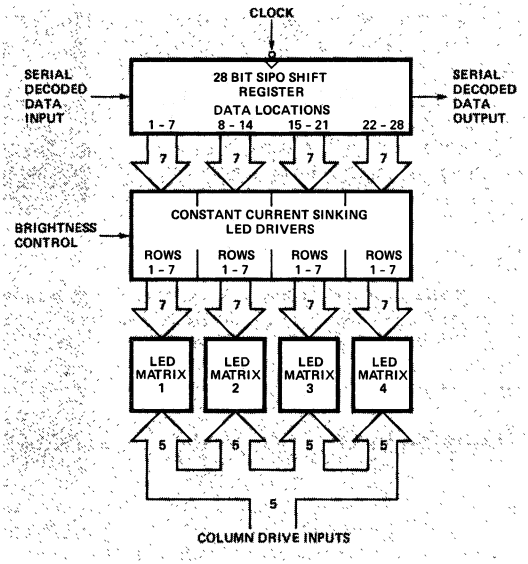


Figure 5. Block Diagram of the HDSP-2010 Display

Knowing the time period, t, to load the data into the display, the LED on time duty factor, DF, may be determined

$$DF = \frac{T}{5(t+T)}$$

The time frame allotted per column is $(t + T)$ and the minimum recommended refresh rate for a flicker free display is 100 Hz, so that $(t + T) \leq 2$ ms. If the display is operated at the 3 MHz maximum clock rate, it is possible to maintain $t << T$. For display strings of 24 characters or less, the LED on time DF will be approximately 19.4%. For longer display strings, operation of the display with DF approximately 10% will provide adequate light output for indoor applications.

The 28th stage of the SIPO shift register is connected to the Data Output, which is designed to interface directly to the Data Input of the next HDSP-2010 in the display string.

The V_B input may be used to control the apparent brightness of the display. A logic high applied to the V_B input enables the display to be turned ON, and a logic low blanks the display by disabling the constant current LED drivers. Therefore, the time average luminous intensity of the display can be varied by pulse width modulation of V_B. For application and drive circuit information refer to HP Application Notes 966 and 1001.

High Reliability Test Program

Hewlett-Packard provides standard high reliability test programs in order to facilitate the use of HP products in military programs. The TXV prefix identifies a part which has been preconditioned and screened per Table 1.

PART NUMBER SYSTEM

Standard Product	With TXV Screening
HDSP-2010	TXV-2010

TABLE 1. TXV Preconditioning and Screening — 100%

Examination or Test	MIL-STD-883 Methods	Conditions
1. Internal Visual Inspection	OED Procedure	
2. High Temperature Storage	1008	100°C, 24 Hrs.
3. Temperature Cycling	1010	-55°C to +100°C, 10 Cycles
4. Constant Acceleration	2001	2,000 G's, Y_1 Orientation
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C, Inspect at 100°C
7. Electrical Test: (I_V, I_{CC}, I_{COL}, I_{IL}, I_{IH}, V_{OH}, V_{OL})		
8. Burn-In	1015	T_A = 70°C, t = 168 hrs. P_D = .9W Max
9. Electrical Test: (I_V, I_{CC}, I_{COL}, I_{IL}, I_{IH}, V_{OH}, V_{OL})		
10. External Visual	2009	

HEWLETT PACKARD

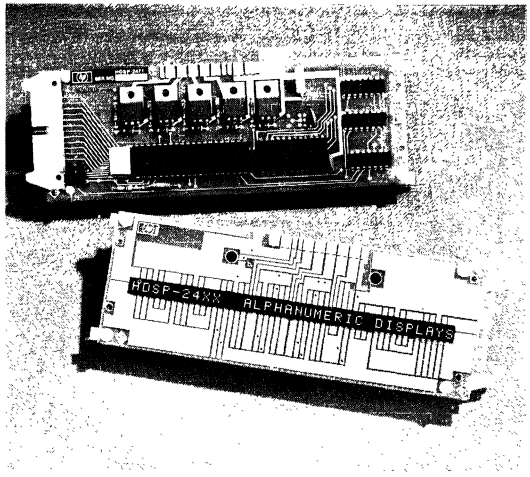
5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP-2416
HDSP-2424
HDSP-2432
HDSP-2440
HDSP-2470
HDSP-2471
HDSP-2472

TECHNICAL DATA MARCH 1980

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY**
- **CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET**
- **CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P.C. board designed to have low thermal resistance.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation, electronic typewriters, and other products which require an easy to use 5 x 7 dot matrix alphanumeric display system.

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

SOLID STATE DISPLAYS

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V

Operating Temperature Range, Ambient (T_A) ..... 0°C to 70°C

Storage Temperature Range (T_S) .... -55°C to 100°C

Voltage Applied to any Input or Output ..-0.5V to 6.0V

I_{SOURCE} Continuous for any Column Driver ..... 5.0 Amps (60 sec. max. duration)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out	I_{OL}		0.4	mA
	I_{OH}		-20	μA
Ready, Data Valid, Column On, Display Data	I_{OL}		1.6	mA
	I_{OH}		-40	μA
Clock	I_{OL}		10.0	mA
	I_{OH}		-1.0	mA
$Column_{1-5}$	I_{SOURCE}		-5.0	A

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current[1]	I_{CC}			400	mA	V_{CC} = 5.25V Column On and All Outputs Open
Input Threshold High (except Reset)	V_{IH}	2.0			V	V_{CC} = 5.0V ± .25V
Input Threshold High — Reset[2]	V_{IH}	3.0			V	V_{CC} = 5.0V ± .25V
Input Threshold Low — All Inputs	V_{IL}			0.8	V	V_{CC} = 5.0V ± .25V
Data Out Voltage	V_{OH}Data	2.4			V	I_{OH} = -20μA V_{CC} = 4.75V
	V_{OL}Data			0.5	V	I_{OL} = 0.4mA V_{CC} = 4.75V
Clock Output Voltage	V_{OH}Clk	2.4			V	I_{OH} = -1000μA V_{CC} = 4.75V
	V_{OL}Clk			0.5	V	I_{OL} = 10.0mA V_{CC} = 4.75V
Ready, Display Data, Data Valid, Column on Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA V_{CC} = 4.75V
	V_{OL}			0.5	V	I_{OL} = 1.6mA V_{CC} = 4.75V
Input Current,[3] All Inputs Except Reset, Chip Select, D_7	I_{IH}			-0.3	mA	V_{IH} = 2.4V V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V V_{CC} = 5.25V
$\overline{\text{Reset}}$ Input Current	I_{IH}			-0.3	mA	V_{IH} = 3.0V V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V V_{CC} = 5.25V
Chip Select, D_7 Input Current	I_I	-10		+10	μA	0 < V_I < V_{CC}
Column Output Voltage	V_{OL}COL	2.6	3.2		V	I_{OUT} = -5.0A V_{CC} = 5.00V

NOTES:

1. See Figure 11 for total system supply current.
2. External reset may be initiated by grounding Reset with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/s.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-2470/1/2.

HDSP-2416/-2424/-2432/-2440

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... -0.5V to 6.0V
Inputs, Data Out and V_B ..... -0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... -0.5V to +6.0V
Free Air Operating Temperature Range, T_A[1] ..... 0°C to +55°C
Storage Temperature Range, T_S .... -55°C to +100°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Norm.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Column Input Voltage, Column On	V_{COL}	2.6			V
Setup Time	t_{SETUP}	70	45		ns
Hold Time	t_{HOLD}	30	0		ns
Width of Clock	$t_{W(CLOCK)}$	75			ns
Clock Frequency	f_{CLOCK}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating[1] Temperature Range	T_A	0		55	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.*	Max.	Units	Conditions
Supply Current		I_{CC}		45n	60n[2]	mA	V_{CC} = 5.25V, V_{CLOCK}=V_{DATA}=2.4V, All SR Stages = Logical 1, V_B = 0.4V
				73n	95n	mA	V_B = 2.4V
Column Current at any Column Input		I_{COL}			1.5n	mA	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1, V_B = 0.4V
		I_{COL}		335n	410n	mA	V_B = 2.4V
Peak Luminous Intensity per LED (Character Average)		$I_{V\ PEAK}$	105	200		µcd	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[3], V_B = 2.4V
V_B, Clock or Data Input Threshold High		V_{IH}	2.0			V	V_{CC} = V_{COL} = 4.75V
V_B, Clock or Data Input Threshold Low		V_{IL}			0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}			80	µA	V_{CC} = 5.25V, V_{IH} = 2.4V
	Data In	I_{IH}			40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}		-500	-800	µA	V_{CC} = 5.25V, V_{IL} = 0.4V
	Data In	I_{IL}		-250	-400	µA	
Power Dissipation Per Board[4]		P_D		0.66n		W	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LED's on per Character, V_B = 2.4V

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

NOTES:

1. Operation above 55°C (70°C MAX) may be achieved by the use of forced air (150 fpm normal to component side of HDSP-247X controller board at sea level). Operation down to -20°C is possible in applications that do not require the use of HDSP-2470/-2471/-2472 controller boards.
2. n = number of HDSP-2000 packages
   HDSP-2416 n = 4
   HDSP-2424 n = 6
   HDSP-2432 n = 8
   HDSP-2440 n = 10
3. Tj refers to initial case temperature immediately prior to the light measurement.
4. Power dissipation with all characters illuminated.

System Overview

The HDSP-2470/-2471/-2472 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-2000 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system refreshes HDSP-2000 displays from 4 to 48 characters with the decoded data.

The user interfaces to any of the systems through eight DATA IN inputs, five ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, seven DATA OUT outputs, a READY output, DATA VALID output, and a COLUMN ON output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. The controller outputs a status word, cursor address and 32 ASCII data characters through the DATA OUT outputs and DATA VALID output during the time the system is waiting to refresh the next column of the display. The COLUMN ON output can be used to synchronize the DATA OUT function. A block diagram for the HDSP-2470/-2471/-2472 systems is shown in Figure 1.

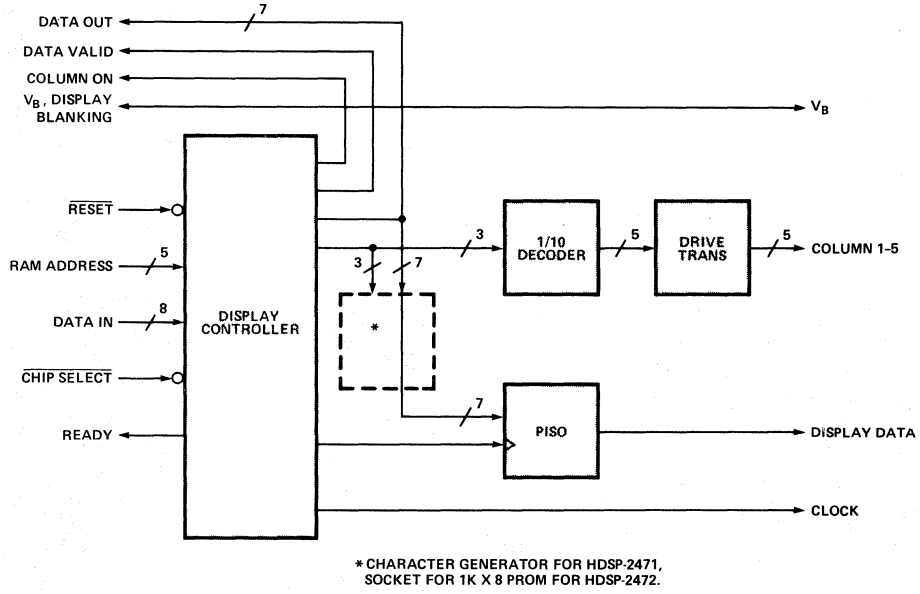


Figure 1. Block Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

The system interfaces to the HDSP-2000 display through five COLUMN outputs, a CLOCK output, DISPLAY DATA output, and the COLUMN ON output. The user should connect DISPLAY DATA to DATA IN of the leftmost HDSP-2000 cluster and cascade DATA OUT to DATA IN of all HDSP-2000 clusters. COLUMN outputs from the system are connected to the COLUMN inputs of all HDSP-2000 clusters. The HDSP-24XX Series display boards are designed to interconnect directly with the HDSP-247X Series display controllers. The COLUMN outputs can source enough current to drive up to 48 characters of the HDSP-2000 display. Pulse width modulation of display luminous intensity can be provided by connecting COLUMN ON to the input of a monostable multivibrator and the output of the monostable multivibrator to the V_B inputs of the HDSP-2000 displays. The system is designed to refresh the display at a fixed refresh rate of 100 Hz. COLUMN ON time is optimized for each display length in order to maximize light output as shown in Figure 2.

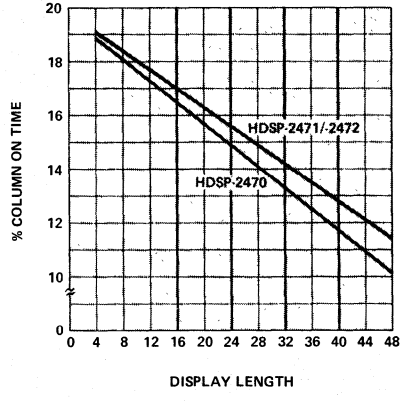


Figure 2. Column on Time vs. Display Length for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Control Mode/Data Entry

User interface to the HDSP-247X Series controller is via an 8 bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8 bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and the number of alphanumeric characters to be displayed.

The 8 bit control data word format is outlined in Figure 3. For the control word (D_7 high), bits D_6 and D_5 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_4 is ignored.

Control word inputs are first checked to verify that the control word is valid. The system ignores display lengths greater than 1011 for left block or right, or 0111 for RAM. If the word is valid, the present state—next state table shown in Figure 4 is utilized to determine whether or not to clear the display. For display lengths of up to 32 characters, RAM entry can be used as a powerful editing tool, or can be used to preload the cursor. With other transitions, the internal data memory is cleared.

CONTROL WORD: $D_7D_6D_5D_4D_3D_2D_1D_0$

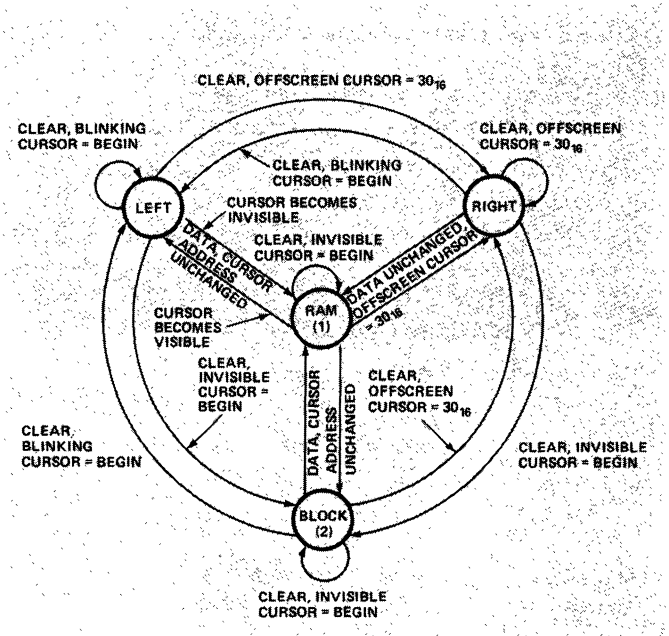
1	X	X	–	Y	Y	Y	Y

Y Y Y Y	DISPLAY LENGTH:
0 0 0 0	4 DIGITS
0 0 0 1	8 "
0 0 1 0	12 "
0 0 1 1	16 "
0 1 0 0	20 "
0 1 0 1	24 "
0 1 1 0	28 "
0 1 1 1	32* "
1 0 0 0	36 "
1 0 0 1	40 "
1 0 1 0	44 "
1 0 1 1	48 "

*maximum for RAM data entry mode

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Figure 3. Control Word Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



(1) RAM ENTRY MODE IS VALID FOR DISPLAYS OF 32 CHARACTERS OR LESS IN LENGTH.
(2) FOLLOWING A TRANSITION FROM RAM TO BLOCK, WHEN THE CURSOR ADDRESS IS 48 (30_{16}) DURING THE TRANSITION, THE FIRST VALID ASCII CHARACTER WILL BE IGNORED AND THE SECOND VALID ASCII CHARACTER WILL BE LOADED IN THE LEFT-MOST DISPLAY LOCATION.

WHERE BEGIN IS DEFINED AS FOLLOWS:

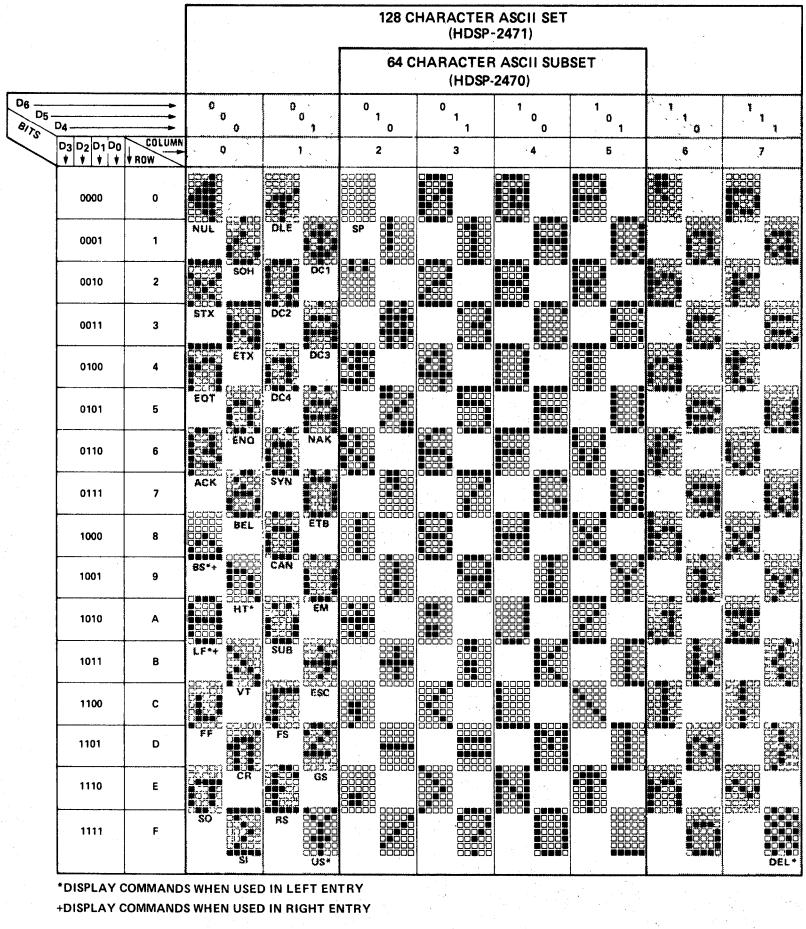
DISPLAY LENGTH	CURSOR ADDRESS OF BEGIN
4	$2C_{16}$, 44_{10}
8	28_{16}, 40_{10}
12	24_{16}, 36_{10}
16	20_{16}, 32_{10}
20	$1C_{16}$, 28_{10}
24	18_{16}, 24_{10}
28	14_{16}, 20_{10}
32	10_{16}, 16_{10}
36	$0C_{16}$, 12_{10}
40	08_{16}, 8_{10}
44	04_{16}, 4_{10}
48	00_{16}

Figure 4. Present State-Next State Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded and displayed. The system accepts seven bit ASCII for all three versions. However, the HDSP-2470 system displays only the 64 character subset [20_{16} (space) to $5F_{16}$ (_)] and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 5. Displayed character sets for the HDSP-2470/-2471 systems are shown in Figure 6.

DATA WORD:	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
ASCII ASSIGNMENT	0	A	A	A	A	A	A	A	DISPLAY COMMAND	
LF	0	0	0	0	1	0	1	0	CLEAR	Valid in Right Entry Mode; Valid in Left Entry Mode
BS	0	0	0	0	1	0	0	0	BACKSPACE CURSOR	Valid in Right Entry Mode; Valid in Left Entry Mode
HT	0	0	0	0	1	0	0	1	FORWARDSPACE CURSOR	Valid in Left Entry Mode
US	0	0	0	1	1	1	1	1	INSERT CHARACTER	Valid in Left Entry Mode
DEL	1	1	1	1	1	1	1	1	DELETE CHARACTER	Valid in Left Entry Mode

Figure 5. Display Commands for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

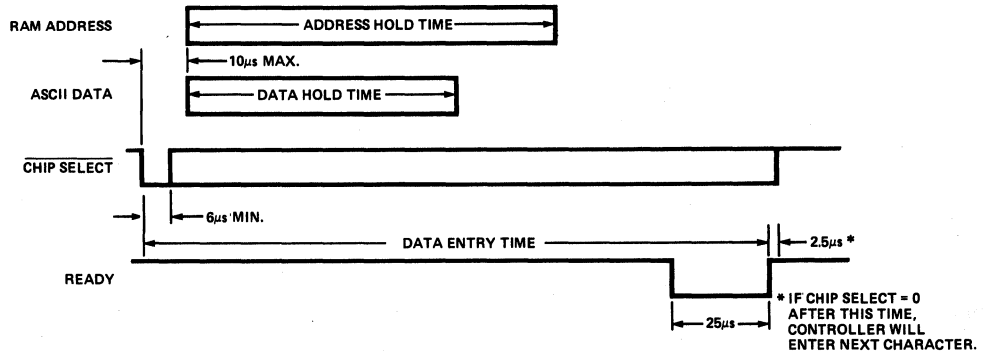


*DISPLAY COMMANDS WHEN USED IN LEFT ENTRY
+DISPLAY COMMANDS WHEN USED IN RIGHT ENTRY

Figure 6. Display Font for the HDSP-2470 (64 Character ASCII Subset), and HDSP-2471 (128 Character ASCII Set) Alphanumeric Display Controller.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 25μs and upon a positive transition, a new CHIP SELECT may be accepted by the controller. Data Entry Timing is shown in Figure 7.

DATA ENTRY TIMING



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE			FUNCTION					
HDSP-	DATA HOLD TIME*		DATA ENTRY	BACK SPACE	CLEAR	FORWARD SPACE	DELETE	INSERT
LEFT (2471/2)	135μs		235μs	195μs	505μs	205μs	725μs	725μs
LEFT (2470)	150μs		245μs	215μs	530μs	225μs	745μs	735μs
RIGHT (2471/2)	85μs		480μs	470μs	465μs			
RIGHT (2470)	105μs		490μs	490μs	485μs			
RAM (2471/2)	55μs	120μs**	190μs					
RAM (2470)	55μs	130μs**	200μs					
BLOCK (2471/2)	55μs		120μs	(155μs FOR RIGHTMOST CHARACTER)				
BLOCK (2470)	55μs		130μs	(165μs FOR RIGHTMOST CHARACTER)				
LOAD CONTROL (2471/2)	50μs		505μs					
LOAD CONTROL (2470)	50μs		505μs					

*Minimum time that data inputs must remain valid after Chip Select goes low.
**Minimum time that RAM address inputs must remain valid after Chip Select goes low.

Figure 7. Data Entry Timing and Data Entry Times for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forward space the cursor. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. FORWARDSPACE, INSERT, and DELETE have character assignments in this mode since they are not treated as editing characters. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a nonvisible cursor, the cursor is always loaded with the address of the next character to be entered. In this entry mode, the system can display the complete 128 character ASCII set. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the five bit RAM address. Due to the limitation of only five address lines, RAM data entry is allowed only for displays less than or equal to 32 characters. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. In RAM entry, the system can display the complete 128 character ASCII set because it does not interpret any of the characters as control functions. The display can be cleared by loading in a new RAM control word.

Data Out

For display lengths of 32 characters or less, the data stored in the internal RAM is available to the user during the time between display refresh cycles. The system outputs a STATUS WORD, CURSOR ADDRESS, and 32 ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD output differs slightly from the CONTROL WORD input. This difference is depicted in Figure 8. Regardless of display length, the CURSOR ADDRESS of the rightmost character location is address 47 ($2F_{16}$) and the offscreen address of the cursor is address 48 (30_{16}). The CURSOR ADDRESS of the leftmost location is defined as address 48 minus the display length. A general formula for CURSOR ADDRESS is:

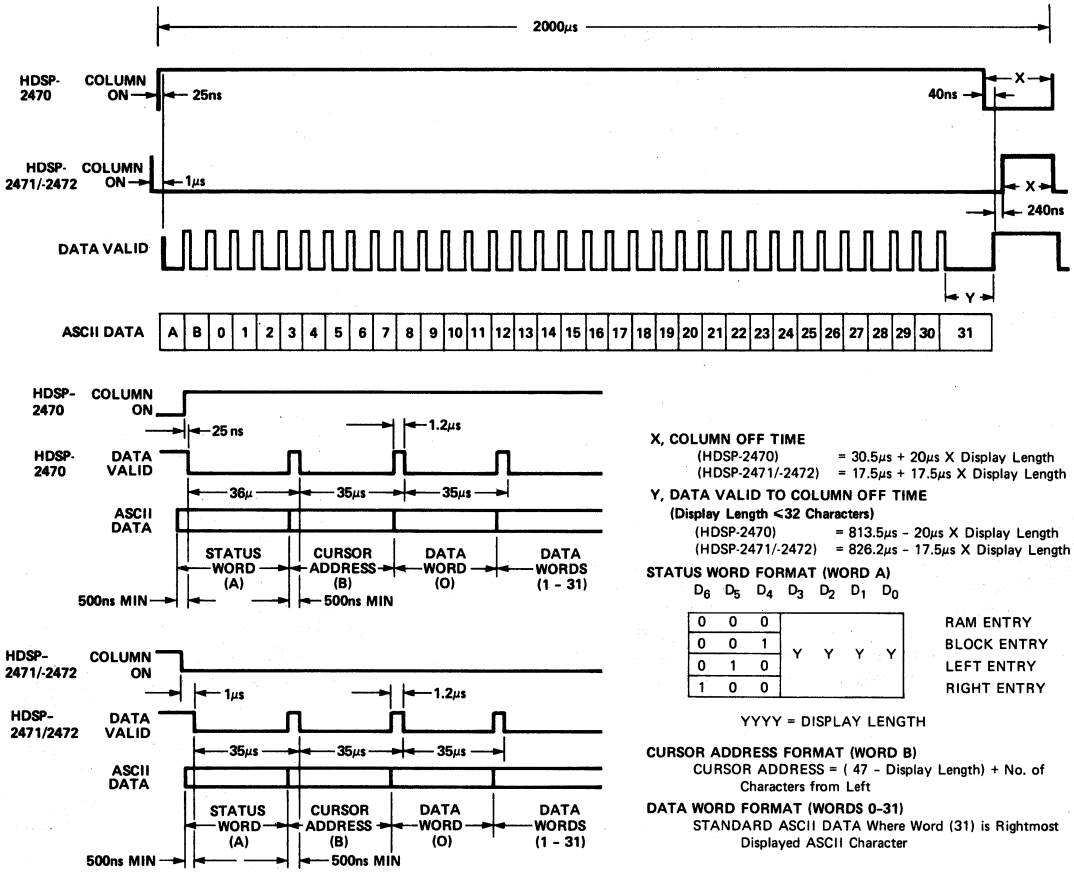
CURSOR ADDRESS =

(47 - Display Length) + Number of Characters from Left.

For example, suppose the alphanumeric display is 16 characters long and the cursor was blinking at the third digit from the left. Then the CURSOR ADDRESS would be 47 - 16 + 3 or 34 (22_{16}) and the 18th ASCII data word would correspond to the ASCII character at the location of the display cursor. In Left and Block entry, the CURSOR ADDRESS specifies the location where the next ASCII data character is to be entered. In RAM entry, the CURSOR ADDRESS specifies the location to the right of the last character entered. In Right entry, the CURSOR ADDRESS is always 48 (30_{16}). The negative edge of the DATA VALID output can be used to load the 34 DATA OUT words into the user's system. The DATA OUT timing for the HDSP-247X systems are summarized in Figure 8. For displays longer than 32 characters, the system only outputs the STATUS WORD between refresh cycles.

Master/Power On Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the systems loads the control word on the DATA INPUTS into the system. If $D_7 \leq .8V$ or the system sees an invalid control word, the system initializes as Left entry for a 32 character display with a flashing cursor in the leftmost location. For POWER ON RESET to function properly, the power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the RESET input low for a minimum of 50 milliseconds. POWER ON/MASTER RESET timing is shown in Figure 9.



X, COLUMN OFF TIME

(HDSP-2470) = 30.5μs + 20μs X Display Length
(HDSP-2471/-2472) = 17.5μs + 17.5μs X Display Length

Y, DATA VALID TO COLUMN OFF TIME

(Display Length <32 Characters)

(HDSP-2470) = 813.5μs - 20μs X Display Length
(HDSP-2471/-2472) = 826.2μs - 17.5μs X Display Length

STATUS WORD FORMAT (WORD A)

D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	Y	Y	Y	Y	RAM ENTRY
0	0	1					BLOCK ENTRY
0	1	0					LEFT ENTRY
1	0	0					RIGHT ENTRY

YYYY = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (WORD B)

CURSOR ADDRESS = (47 - Display Length) + No. of Characters from Left

DATA WORD FORMAT (WORDS 0-31)

STANDARD ASCII DATA Where Word (31) is Rightmost Displayed ASCII Character

Figure 8. Data Out Timing and Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

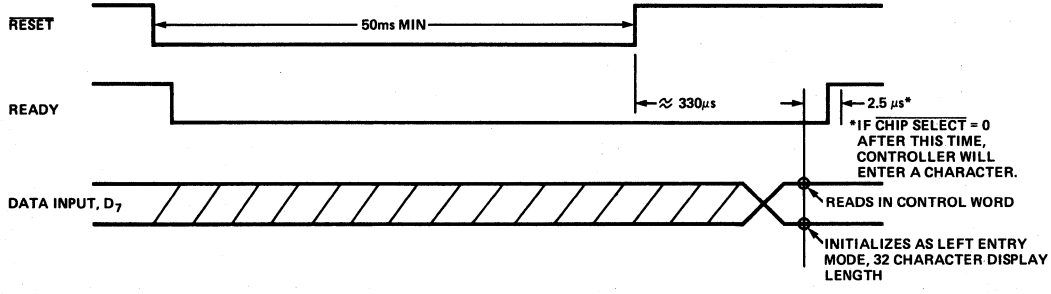


Figure 9. Power-On/Master Reset Timing for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Custom Character Sets

The HDSP-2472 system has been specifically designed to permit the user to insert a custom 128 ASCII character set. This system features a 24 pin socket that is designed to accept a custom programmed 1K X 8 PROM, EPROM, or ROM. The read only memory should have an access time $\leq$ 500ns, $I_{IL} \leq |-.4mA|$ and $I_{IH} \leq 40\mu A$. A list of pin compatible read only memories is shown in Figure 10. Jumper locations are provided on the HDSP-2472 P.C. board which allow the use of ROM's requiring chip enables tied either to 0 or 5V. For further information on ROM programming, please contact the factory.

Power Supply Requirements

The HDSP-247X Alphanumeric Display System is designed to operate from a single 5 volt supply. Total I_{CC} requirements for the HDSP-247X Alphanumeric Display Controller and HDSP-24XX Display Panel are shown in Figure 11. Peak I_{CC} is the instantaneous current required for the system. Maximum Peak I_{CC} occurs for $V_{CC} = 5.25V$ with 7 dots ON in the same Column in all display characters. This current must be supplied by a combination of the power supply and supply filter capacitor. Maximum Average I_{CC} occurs for $V_{CC} = 5.25V$ with 21 dots ON per character in all display characters. The inclusion of a 375 X microfarad capacitor (where X is the number of characters in the display) adjacent to the HDSP-247X Alphanumeric Display System will permit the use of a power supply capable of supplying the maximum average I_{CC}.

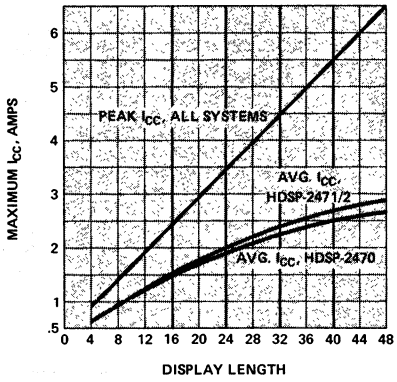


Figure 11. Maximum Peak and Average I_{CC} for the HDSP-2470/71/72 Alphanumeric Display Controller and HDSP-2000 Display.

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	26 Pin Ribbon Cable	3M P/N 3399-X000 Series
POWER(1)	3 Pin With Locking Ramp	Molex P/N 09-50-3031 with 08-50-0106 Terminals
DISPLAY DRIVE(2,3)	17 Lead Board to Board	Amp P/N 1-530500-7, also available in board to cable and other configurations

NOTES:
(1) Power leads should be 18-20 gauge stranded wire.
(2) The maximum lead length from the controller board to the display should not exceed 1 metre.
(3) The suggested Amp connector is supplied with the controller.

PART NUMBER	MANUFACTURER	TYPE	CONSTRUCTION	EXTERNAL CONNECTION* X	Y	Z
2758	Intel	EPROM	NMOS	GND	GND	+5
7608	Harris	PROM	BIPOLAR-NiCr	NC	NC	NC
3628-4	Intel	PROM	BIPOLAR-Si	+5	+5	GND
82S2708	Signetics	PROM	BIPOLAR-NiCr	NC	NC	NC
6381	Monolithic Mem.	PROM	BIPOLAR-NiCr	+5	+5	GND
6385	Monolithic Mem.	PROM	BIPOLAR-NiCr	NC	NC	NC
87S228	National	PROM	BIPOLAR-TiW	+5	+5	GND
93451	Fairchild	PROM	BIPOLAR-NiCr	+5	+5	GND
68308	Motorola	ROM	NMOS	**	NC	NC
2607	Signetics	ROM	NMOS	**	NC	NC
30000	Mostek	ROM	NMOS	**	+5	NC

*Board jumpers correspond to pins 18, 19 & 21 of ROM.

**As defined by customer

Figure 10. Pin Compatible 1K x 8 Read Only Memories for the HDSP-2472 Alphanumeric Display Controller.

Display Boards/Hardware

The mechanical layout of the HDSP-247X Series allows direct mating of the controller P.C. board to a compatible series of display boards available from Hewlett-Packard. These display boards consist of matched and tested HDSP-2000 clusters soldered to a P.C. board.

Included with the controller board are: 1 each Amp P/N 1-530500-7 board to board connector, and 4 each locking circuit board support nylon standoffs (Richco LCBS-4). This hardware allows the controller board to interconnect with any of the standard display boards. Figure 12 depicts correct assembly technique.

Assembly Steps

1. Insert the standoffs into .151 diameter holes (noted as "S" on Figure 12. The long end of the standoffs should protrude through the controller board side.
2. Position the controller board and display board with the components and displays facing out. The HP logo should be in the upper left corner when viewed facing the boards. Insert the standoffs through the mating holes on the display board and press the boards together so that the standoffs lock in place.
3. After the standoffs are secured, the Amp connector should be placed on the edge connect pads (marked "A" through "Q" Figure 12) at the top of the boards. Visual alignment of this connector may be done on the controller board by determining that the first connector contact finger is centered on the pad labeled "A".

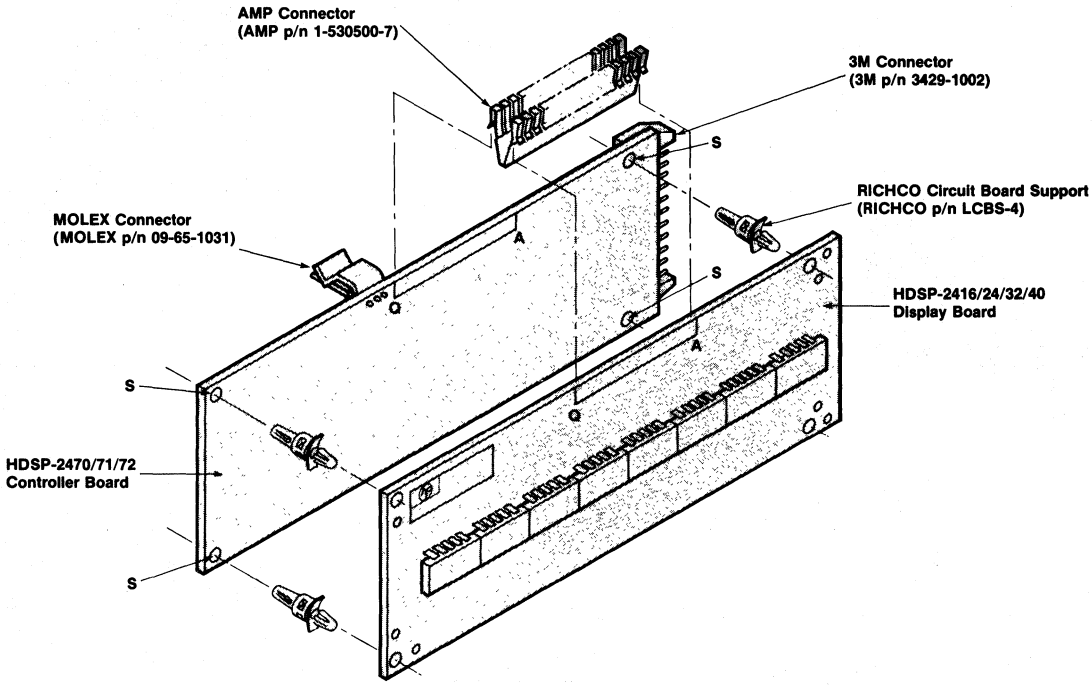


Figure 12. Assembly Drawing.

Package Dimensions

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN mm AND (INCHES)

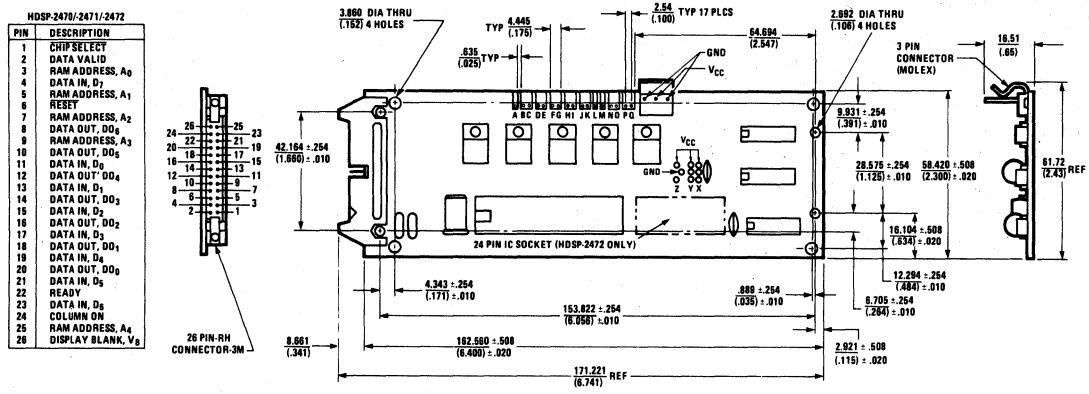


Figure 13. HDSP-2470/-2471/-2472

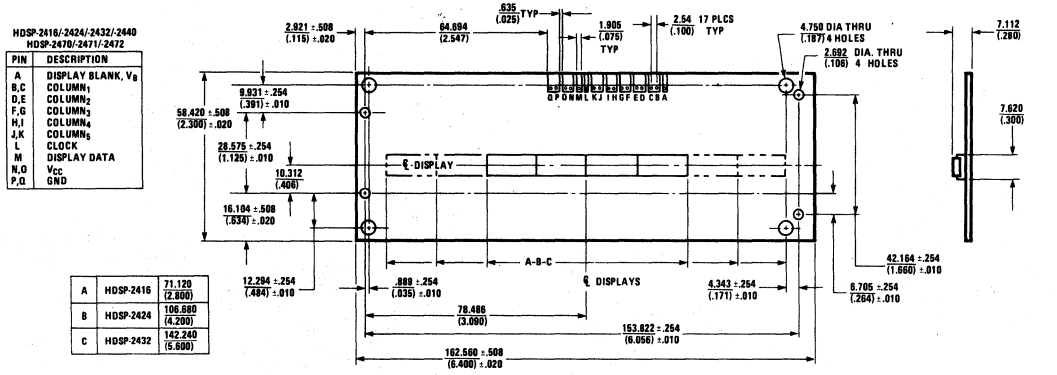


Figure 14. HDSP-2416/-2424/-2432

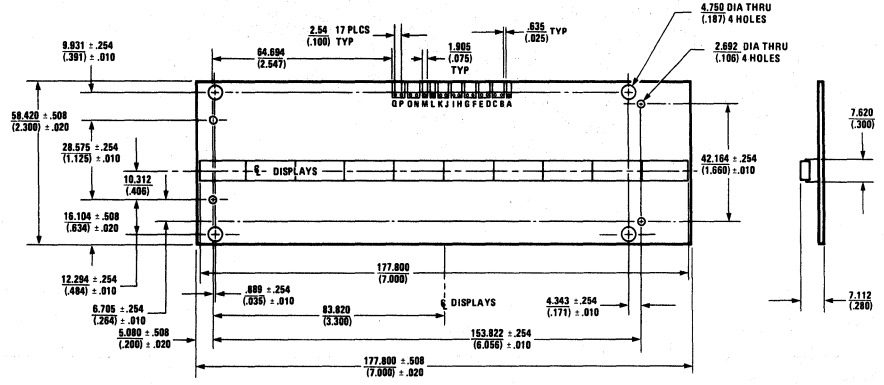


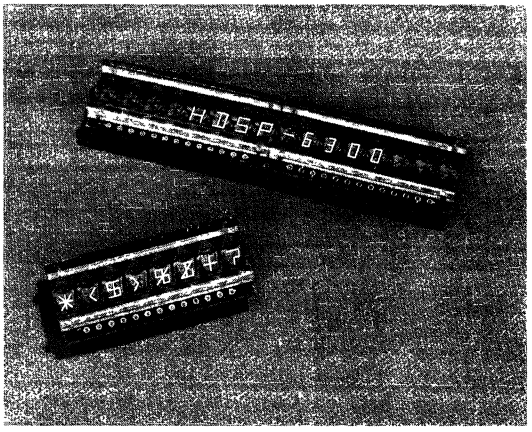
Figure 15. HDSP-2440

HEWLETT PACKARD

18 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6300

TECHNICAL DATA MARCH 1980



Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **18 SEGMENT FONT INCLUDING CENTERED D.P. AND COLON**
- **3.56mm (0.140") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  8 Character Dual-In-Line Package
  End Stackable
  Sturdy Leads on 2.54mm (0.100") Centers
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  5.08mm (0.200") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 1.5 Metres
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output From Unit to Unit Within a Single Category

Description

The HDSP-6300 is an eighteen segment GaAsP red alphanumeric display mounted in an 8 character dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The eighteen segments consist of sixteen segments for alphanumeric and special characters plus centered decimal point and colon for good visual aesthetics. Character spacing yields 5 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and mobile terminals, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 417μs)		150	mA
I_{AVG}	Average Current Per Segment or DP[1]		6.25	mA
P_D	Average Power Dissipation Per Character[1,2]		133	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 5 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.47 mW/°C. P_D Max. (T_A = 85°C) = 47 mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 24mA 1/16 Duty Factor	400	1200		μcd
V_F	Forward Voltage Per Segment or DP	I_F = 24mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin per Character			250		°C/W/ Char.

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Operation at peak currents of less than 7mA is not recommended.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

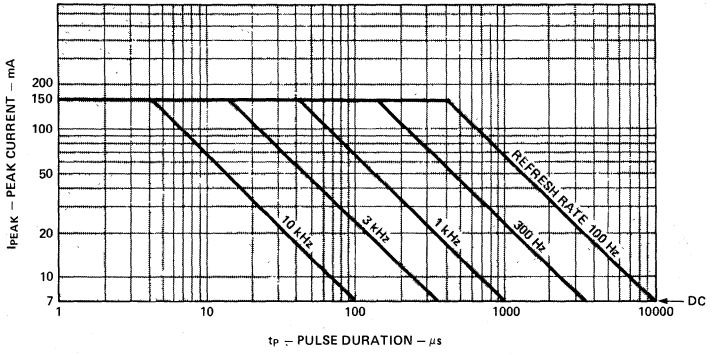


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

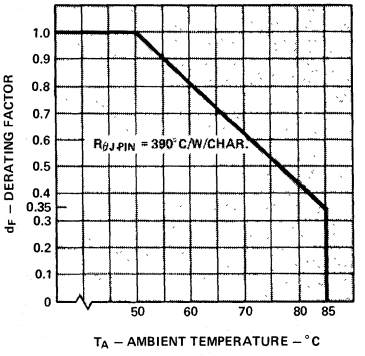


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. T_JMAX = 110°C

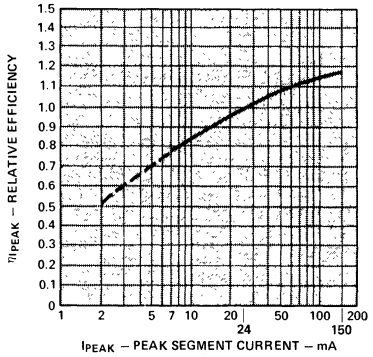


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

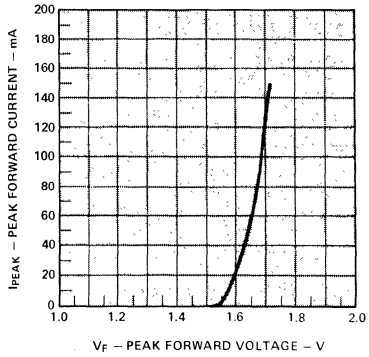


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

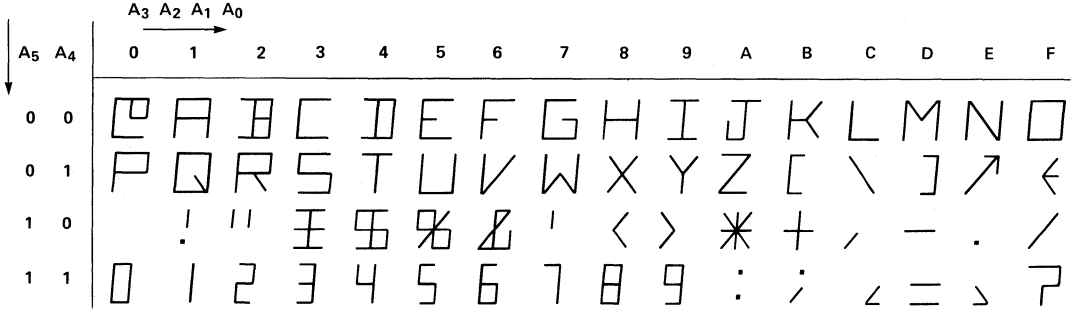
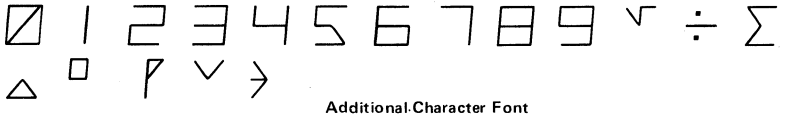
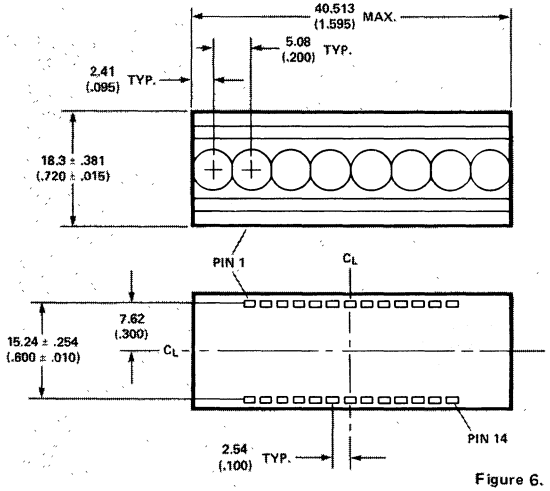
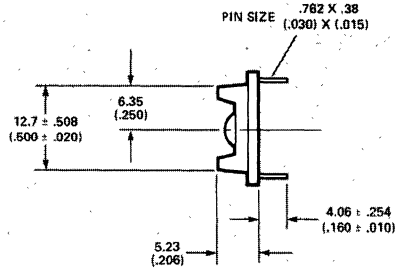


Figure 5. Typical 64 Character ASCII Set.



Additional Character Font





NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY DOT ADJACENT TO LEAD.

Figure 6.

Magnified Character Font Description

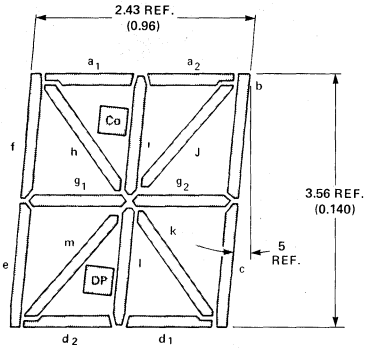


Figure 7.

Device Pin Description

Pin No.	Function	
1	Anode	Segment K
2	Anode	Segment D_1
3	Anode	Segment C
4	Cathode	Digit 1
5	Cathode	Digit 2
6	Cathode	Digit 3
7	Cathode	Digit 4
8	Anode	Segment L
9	Anode	Segment G_2
10	Anode	Segment E
11	Anode	Segment M
12	Anode	Segment D_2
13	Anode	Segment DP
14	Anode	Segment A_2
15	Anode	Segment I
16	Anode	Segment J
17	Cathode	Digit 8
18	Cathode	Digit 7
19	Cathode	Digit 6
20	Cathode	Digit 5
21	Anode	Segment C_o
22	Anode	Segment G_1
23	Anode	Segment B
24	Anode	Segment F
25	Anode	Segment H
26	Anode	Segment A_1

Operational Considerations

ELECTRICAL

The HDSP-6300 device utilizes large monolithic 18 segment GaAsP LED chips including centered decimal point and colon. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame. A detailed discussion of character font capabilities, ASCII code to 18 segment decoding, and display drive techniques will appear in a forthcoming application note.

This display is designed specifically for strobed (multiplexed) operation, with a minimum recommended peak forward current per segment of 7.0 mA. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}\ (1.8\Omega)$
For $30mA \leq I_{PEAK} \leq 150mA$
$V_F = 1.58V + I_{PEAK}\ (10.7\Omega)$
For $10mA \leq I_{PEAK} \leq 30mA$

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens producing a magnified character height of 3.56mm (0.140 inch). The aspheric lens provides wide included viewing angles of 60 degrees horizontal and 55 degrees vertical with low off axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 1.5 metres. Effective contrast enhancement can be obtained by employing an optical filter product such as Panelgraphic Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite H100-1605 Red or H100-1804 Purple; or Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Red 655 or Neutral Density Light Control Film is recommended.

MECHANICAL

This device is constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board.

The HDSP-6300 can be end stacked to form a character string which is a multiple of a basic eight character grouping. These devices may be soldered onto a printed circuit board or inserted into 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

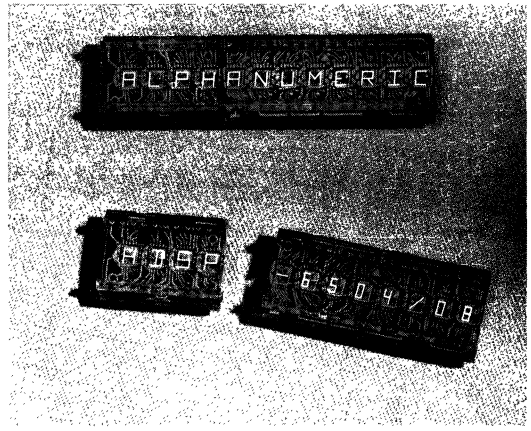
Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. For more information, consult the local HP Sales Office or Hewlett-Packard Components, Palo Alto, California.

HEWLETT PACKARD

18 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6504
HDSP-6508

TECHNICAL DATA MARCH 1980



Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.81mm (0.150") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  4 and 8 Character Dual-In-Line Packages
  End Stackable-On Both Ends for 8 Character and On One End for 4 Character
  Sturdy Gold-Plated Leads on 2.54mm (0.100") Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  6.35mm (0.250") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 2 Metres
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output From Unit to Unit Within a Single Category

Description

The HDSP-6504 and HDSP-6508 are 3.81mm (0.150") eighteen segment GaAsP red alphanumeric displays mounted in 4 character and 8 character dual-in-line package configurations that permit mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The rugged package construction, enhanced by the back fill design, offers extended environmental capabilities compared to the standard PC board/lens type of display package. Its temperature cycling capability is the result of the air gap which exists between the semiconductor chip/wire bond assembly and the lens. In addition to the sixteen segments, a centered D.P. and colon are included. Character spacing yields 4 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and terminals, computer base emergency mobile units, automotive instrument panels, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Device Selection Guide

Characters Per Display	Configuration Device	Package	Part No. HDSP-
4		(Figure 6)	6504
8		(Figure 7)	6508

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 312μs)		200	mA
I_{AVG}	Average Current Per Segment or DP[1]		7	mA
P_D	Average Power Dissipation Per Character[1,2]		138	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 3 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.17mW/°C. P_D Max. (T_A = 85°C) = 62mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 30mA 1/16 Duty Factor	0.40	1.65		mcd
V_F	Forward Voltage Per Segment or DP	I_F = 30mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$\Delta V_F/\Delta°C$	Temperature Coefficient of Forward Voltage			-2		mV/°C
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin			232		°C/W/ Seg

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Operation at peak currents of less than 7mA is not recommended.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

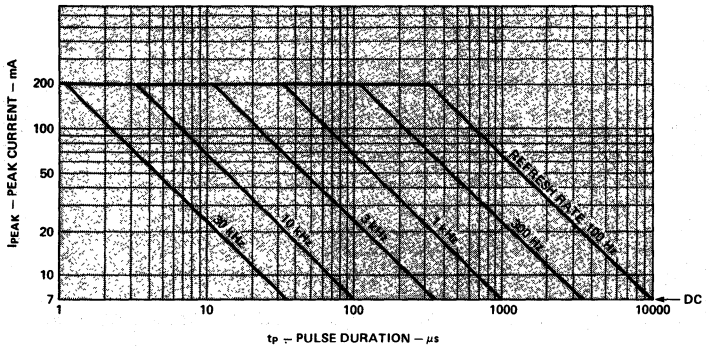


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

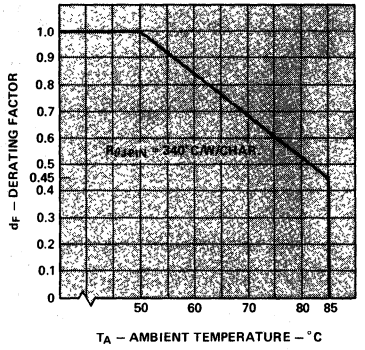


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. T_JMAX = 110°C

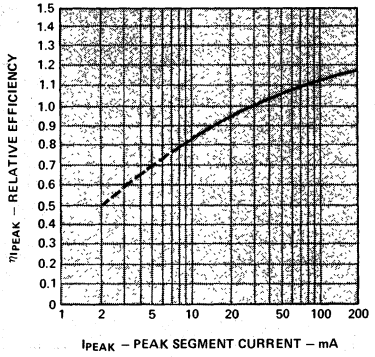


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

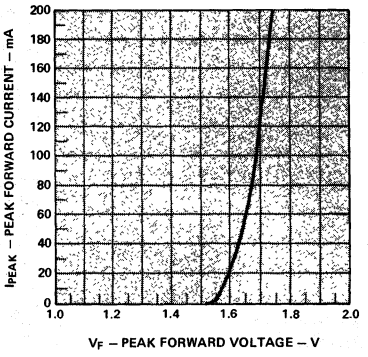


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005, Page 464.

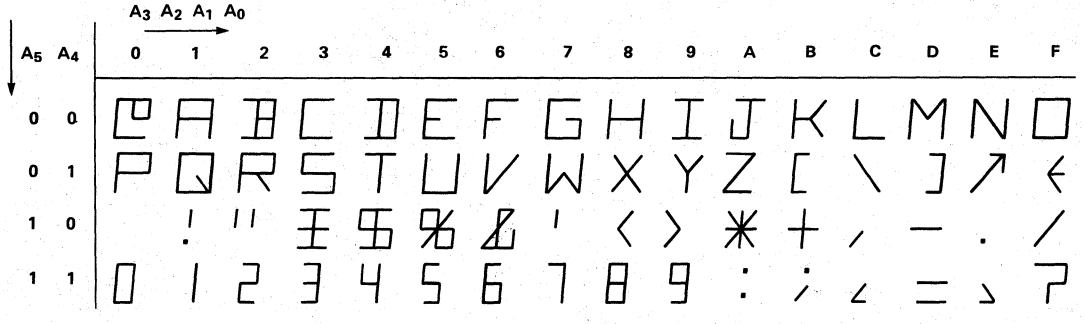
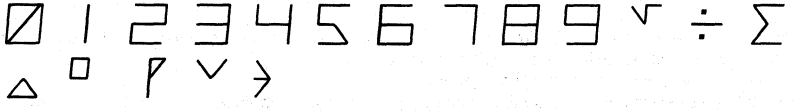


Figure 5. Typical 64 Character ASCII Set.



Additional Character Font

Package Dimensions

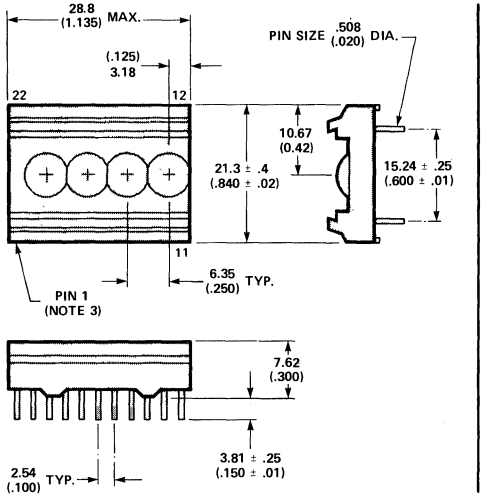


Figure 6. HDSP-6504

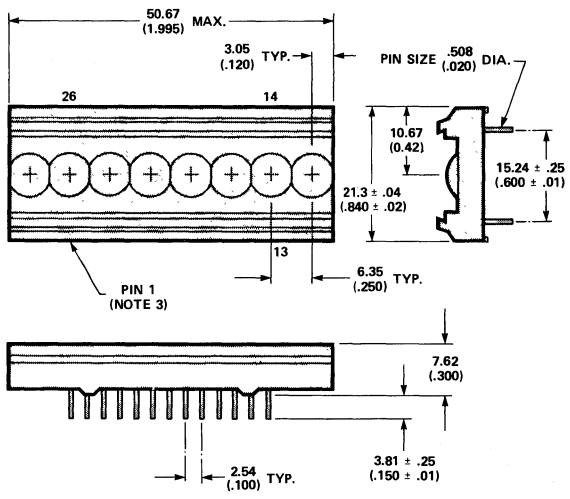


Figure 7. HDSP-6508

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD.

Magnified Character Font Description

DEVICES
HDSP-6504
HDSP-6508

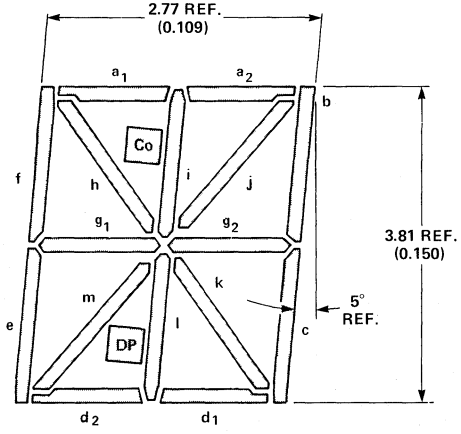


Figure 8.

Device Pin Description

Pin No.	Function	
	HDSP-6504	HDSP-6508
1	Anode Segment g_1	Anode Segment g_1
2	Anode Segment DP	Anode Segment DP
3	Cathode Digit 1	Cathode Digit 1
4	Anode Segment d_2	Anode Segment d_2
5	Anode Segment l	Anode Segment l
6	Cathode Digit 3	Cathode Digit 3
7	Anode Segment e	Anode Segment e
8	Anode Segment m	Anode Segment m
9	Anode Segment k	Anode Segment k
10	Cathode Digit 4	Cathode Digit 4
11	Anode Segment d_1	Anode Segment d_1
12	Anode Segment j	Cathode Digit 6
13	Anode Segment C_O	Cathode Digit 8
14	Anode Segment g_2	Cathode Digit 7
15	Anode Segment a_2	Cathode Digit 5
16	Anode Segment i	Anode Segment j
17	Cathode Digit 2	Anode Segment C_O
18	Anode Segment b	Anode Segment g_2
19	Anode Segment a_1	Anode Segment a_2
20	Anode Segment c	Anode Segment i
21	Anode Segment h	Cathode Digit 2
22	Anode Segment f	Anode Segment b
23		Anode Segment a_1
24		Anode Segment c
25		Anode Segment h
26		Anode Segment f

Operational Considerations

ELECTRICAL

The HDSP-6504 and -6508 devices utilize large monolithic 16 segment GaAsP LED chips with centered decimal point and colon. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame. A detailed discussion of character font capabilities, ASCII code to 18 segment decoding and display drive techniques appear in Application Note 1003.

These displays are designed specifically for strobed (multiplexed) operation, with a minimum recommended time peak forward current per segment of 7mA. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}(1.8\Omega)$
For: $30mA \leq I_{PEAK} \leq 200mA$
$V_F = 1.58V + I_{PEAK}(10.7\Omega)$
For: $10mA \leq I_{PEAK} \leq 30mA$

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens, producing a magnified character height of 3.810mm (.150 inch). The aspheric lens provides wide included viewing angles of typically 75 degrees horizontal and 75 degrees vertical with low off axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 2 metres. Effective contrast enhancement can be obtained by employing any of the following optical filter products: Panelgraphic: Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite: H100-1605 Red or H100-1804 Purple, Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Light Control Film is recommended: Red 655, Violet, Purple or Neutral Density.

For those applications requiring only 4 or 8 characters, a secondary barrel magnifier, HP part number HDSP-6505 (four character) and -6509 (eight character), may be inserted into support grooves on the primary magnifier. This secondary magnifier increases the character height to 4.45mm (.175 inch) without loss of horizontal viewing angle (see below).

MECHANICAL

These devices are constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board and the resulting assembly is backfilled with a sealing epoxy to form an environmentally sealed unit.

The four character and eight character devices can be end stacked to form a character string which is a multiple of a basic four character grouping. As an example, one -6504 and two -6508 devices will form a 20 character string. These devices may be soldered onto a printed circuit board or inserted into 24 and 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. For more information, consult the local HP Sales Office or Hewlett-Package Components, Palo Alto, California.

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

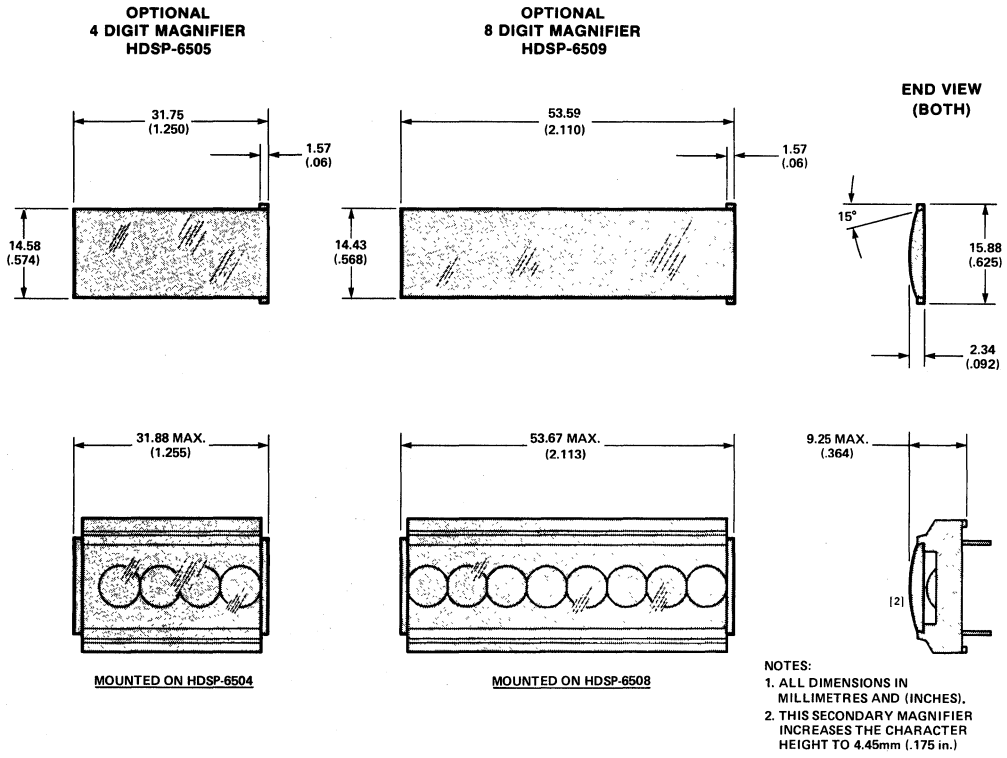


Figure 9. Design Data for Optional Barrel Magnifier in Single Display Applications.

HEWLETT PACKARD

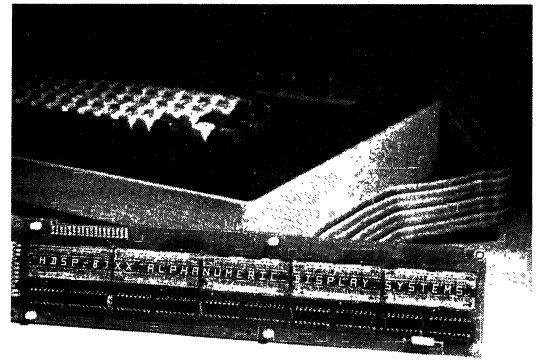
18 SEGMENT ALPHANUMERIC DISPLAY SYSTEM

HDSP-8716
HDSP-8724
HDSP-8732
HDSP-8740

TECHNICAL DATA MARCH 1980

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-6508 DISPLAY**
- **DISPLAYS 64 CHARACTER ASCII SET**
- **CHOICE OF 16, 24, 32, OR 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, CARRIAGE RETURN, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-87XX series of alphanumeric display systems provides the user with a completely supported 18 segment display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays.

Each alphanumeric display system consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-6508 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines. This microprocessor controller is mounted behind a single line display panel consisting of HDSP-6508 displays matched for luminous intensity.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation,, electronic typewriters, and other products which require an easy to use 18 segment alphanumeric display system.

Part Number	Description
HDSP-8716	Single-line 16 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8724	Single-line 24 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8732	Single-line 32 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8740	Single-line 40 Character Alphanumeric Display System utilizing the HDSP-6508 Display

HDSP-8716/-8724/-8732/-8740

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V
Operating Temperature Range,
Ambient (T_A) ..... 0°C to 70°C
Storage Temperature Range (T_S) ..... -40°C to 85°C
Voltage Applied to any
Input or Output ..... -0.5V to 6.0V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out, Data Valid, Ready, Refresh	I_{OL}		3.2	mA
	I_{OH}		-80	μA
Active, Clock	I_{OL}		1.6	mA
	I_{OH}		-40	μA

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions
Supply Current HDSP-8716/-8724	I_{CC}		560	1150	mA	V_{CC}=5.25V, "$" Displayed in All
Supply Current HDSP-8732/-8740	I_{CC}		700	1320	mA	Character Locations, All Outputs Open
Time Average Luminous Intensity Per Digit, 10 Segments on[1]	I_V	24	70		mcd	V_{CC}=5.0V, Digit Average '$' Displayed In All Character Locations, T_A=25°C
Input Threshold High (except $\overline{Reset}$)	V_{IH}	2.0			V	V_{CC}=5.0V ± .25V
Input Threshold High — $\overline{Reset}$[2]	V_{IH}	3.0			V	
Input Threshold Low — All Inputs	V_{IL}			0.8	V	
Data Out, Data Valid, Ready,	V_{OH}	2.4			V	I_{OH}=-80μA, V_{CC} = 4.75V
$\overline{Refresh}$, Output Voltage	V_{OL}			0.5	V	I_{OL}=3.2 mA, V_{CC}=4.75V
$\overline{Active}$, Clock Output Voltage	V_{OH}	2.4			V	I_{OH}=-40μA, V_{CC}=4.75V
	V_{OL}			0.5	V	I_{OL}=1.6mA, V_{CC}=4.75V
Address,[3] Expand, Input Current	I_{IH}			-0.3	mA	V_{IH}=2.4V, V_{CC}=5.25V
	I_{IL}			-0.6	mA	V_{IL}=0.5V, V_{CC}=5.25V
$\overline{Blank}$ Input Current	I_{IH}			-0.5	mA	V_{IH}=2.4V, V_{CC}=5.25V
	I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
$\overline{Reset}$ Input Current	I_{IH}			-0.5	mA	V_{IH}=3.0V, V_{CC}=5.25V
	I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
Data In, Chip Select, Input Current	I_I	-10		+10	μA	0<V_I<V_{CC}
Peak Wavelength	λ_{PEAK}		655		nm	
Dominant Wavelength[4]	λ_d		640		nm	

NOTES:
1. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus, each segment will appear with equal brightness to the eye.
2. External reset may be initiated by grounding $\overline{Reset}$ with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/S.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-8716/-8724/-8732/-8740.
4. The dominant wavelength, λ_d, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.
5. All typical values at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

System Overview

The HDSP-8716/-8724/-8732/-8740 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-6508 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM, or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system may also be expanded to form multiple line panels with system to system control signals.

The user interfaces to any of the system through eight DATA IN inputs, six ADDRESS inputs (RAM mode), a $\overline{\text{CHIP SELECT}}$ input, $\overline{\text{RESET}}$ input, $\overline{\text{BLANK}}$ input, $\overline{\text{EXPAND}}$ input, six DATA OUT outputs, a READY output, DATA VALID output, $\overline{\text{REFRESH}}$ output, and CLOCK output. A low level on the $\overline{\text{RESET}}$ input clears the display and initializes the system. A low level on the $\overline{\text{CHIP SELECT}}$ input causes the system to load data from the DATA IN and ADDRESS inputs into the system. A special control word causes the controller to output a STATUS WORD, CURSOR ADDRESS, and a string of ASCII characters through the DATA OUT outputs and DATA VALID output. A low level on the $\overline{\text{EXPAND}}$ input allows two or more systems to be configured for multiple line display panels. Pulse width modulation of display luminous intensity can be provided by connecting $\overline{\text{REFRESH}}$ to the input of a monostable multivibrator and the output of the monostable multivibrator to the $\overline{\text{BLANK}}$ input. A 400kHz clock is provided on the CLOCK output. A system block diagram for the HDSP-8716/-8724/-8732/-8740 systems is shown in Figure 1. The system is designed to refresh the display at a fixed refresh rate of 100Hz. The display duty factor is optimized for each display length in order to maximize light output.

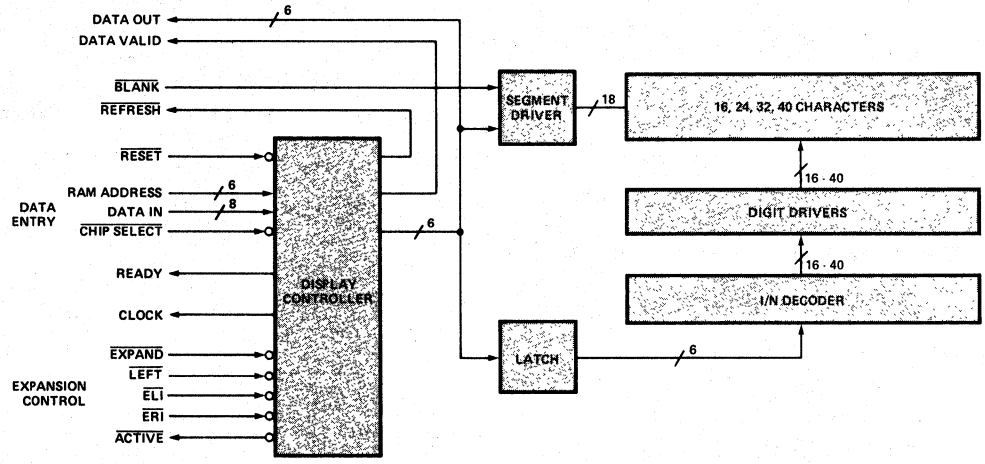


Figure 1. Block Diagram of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Control Mode/Data Entry

User interface to the HDSP-87XX series controller is via an 8-bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8-bit word, two additional control lines, $\overline{\text{CHIP SELECT}}$ and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the $\overline{\text{CHIP SELECT}}$ input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and appropriate display length.

The 8 bit control data word format is outlined in Figure 2. For the control word (D_7 high), bits D_5 and D_4 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_6 is ignored.

Control word inputs are first checked to verify that the control word is valid. If the word is valid, the present state — next state table shown in Figure 3 is utilized to determine whether or not to clear the display. RAM entry can be used as a powerful editing tool or can be used to preload the cursor. With other transitions, the internal memory is cleared. The CONTROL WORD $1XXX11XX_2$ is used by the controller to initiate the DATA OUT function.

DATA ENTRY CONTROL WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

1	–	X	X	Y	Y	Y	Y

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Y Y Y Y	DISPLAY LENGTH	
0 0 1 1	16 DIGITS	HDSP-8716
0 1 0 1	24 DIGITS	HDSP-8724
0 1 1 1	32 DIGITS	HDSP-8732
1 0 0 1	40 DIGITS	HDSP-8740

DATA OUT CONTROL WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

1	–	–	–	1	1	–	–

DATA OUT

Figure 2. Control Word Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

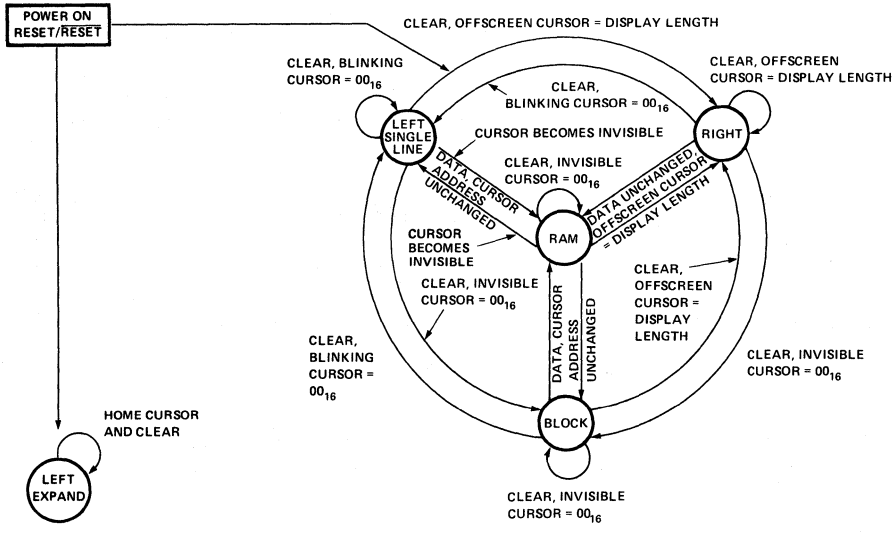


Figure 3. Present State-Next State Diagram for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

DATA WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

ASCII ASSIGNMENT

0	X	X	X	X	X	X	X

BS	0	0	0	1	0	0	0	BACKSPACE	RIGHT	LEFT, EXPAND*
LF	0	0	0	1	0	1	0	CLEAR (NEW LINE*)	RIGHT	LEFT, EXPAND*
HT	0	0	0	1	0	0	1	FORWARDSPACE	RIGHT	LEFT, EXPAND*
CR	0	0	0	1	1	0	1	CARRIAGE RETURN	RIGHT	LEFT, EXPAND*
US	0	0	1	1	1	1	1	INSERT CHARACTER	LEFT, SINGLE	LEFT, EXPAND*
DEL	1	1	1	1	1	1	1	DELETE CHARACTER	LEFT, SINGLE	LEFT, EXPAND*
VT	0	0	0	1	0	1	1	CURSOR DOWN	LEFT, SINGLE	LEFT, EXPAND*
FF	0	0	0	1	1	0	0	HOME & CLEAR	LEFT, SINGLE	LEFT, EXPAND*
RS	0	0	1	1	1	1	0	CURSOR UP	LEFT, SINGLE	LEFT, EXPAND*

OTHERWISE, THE 7 BIT ASCII CODE

Figure 4. Display Commands for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

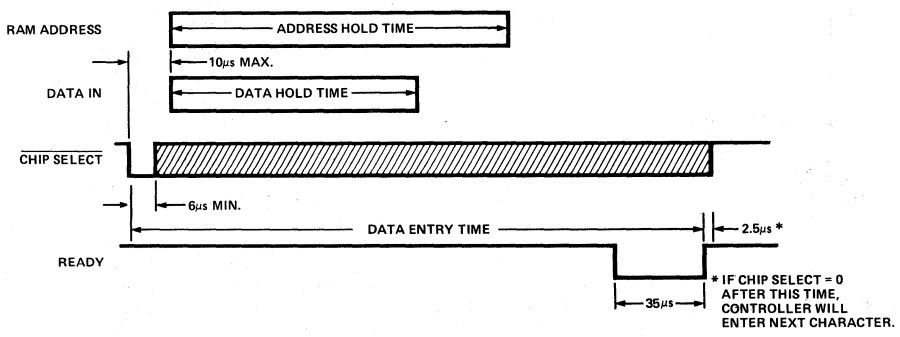
If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded, and displayed. The system accepts the standard 7-bit ASCII code. However, the HDSP-87XX system displays only the 64 character subset $|20_{16}$ (space) to $5F_{16}$ (↑)| and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 4. The displayed character set for the HDSP-87XX system is shown in Figure 5.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 35μs and upon a positive transition, a new $\overline{\text{CHIP SELECT}}$ may be accepted by the controller. Data Entry Timing is shown in Figure 6.

BITS D_3 D_2 D_1 D_0		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←

Figure 5. Display Font for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

DATA ENTRY TIMING



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE		FUNCTION										
	DATA HOLD TIME*	DATA ENTRY	BS	HT	LF	CR	US	INSERT	DEL	VT	FF	RS
LEFT, SINGLE	25μs	250μs	215μs	235μs	505μs	220μs	200μs	665μs	645μs			
LEFT, EXPANDED	25μs	345μs	265μs	265μs	285μs	245μs	245μs	705μs	690μs	250μs	630μs	245μs
RIGHT	25μs	480μs	480μs		485μs							
RAM	25μs	145μs**	220μs									
BLOCK	25μs	130μs (165μs FOLLOWING RIGHTMOST CHARACTER)										
CONTROL	25μs	545μs										
DATA OUT	25μs	280μs + 36nμs, WHERE n = CONFIGURED DISPLAY LENGTH										

*MINIMUM TIME THAT DATA INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.
**MINIMUM TIME THAT RAM ADDRESS INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.

Figure 6. Data Entry Timing and Data Entry Times for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forwardspace the cursor. CARRIAGE RETURN resets the cursor to the leftmost display location leaving the display unchanged. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR, CARRIAGE RETURN, or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE, CARRIAGE RETURN, and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Expanded Left entry is selected by grounding the $\overline{\text{EXPAND}}$ input prior to $\overline{\text{RESET}}$. Expanded Left entry mode allows several HDSP-87XX systems to be connected into a multiple line panel. Expanded Left entry uses the $\overline{\text{ERI}}$ input, $\overline{\text{ELI}}$ input, $\overline{\text{LEFT}}$ input, and $\overline{\text{ACTIVE}}$ output to provide a handshake between each system as shown in Figure 7. With the proper connections, the cursor can be moved in a circular fashion from the end of the last line to the beginning of the first line, or such that it shifts offscreen and is lost until the next CLEAR/HOME display command. Expanded Left entry adds three display commands: CURSOR UP moves the cursor to the same location in the preceeding line; CURSOR DOWN moves the cursor to the same location in the following line; CLEAR/HOME loads all displays with spaces and resets the cursor to the leftmost display location in the first line. The CLEAR command in Left entry mode is replaced by the LINE FEED function. LINE FEED moves the cursor to the leftmost display location in the following line leaving the current line unchanged.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

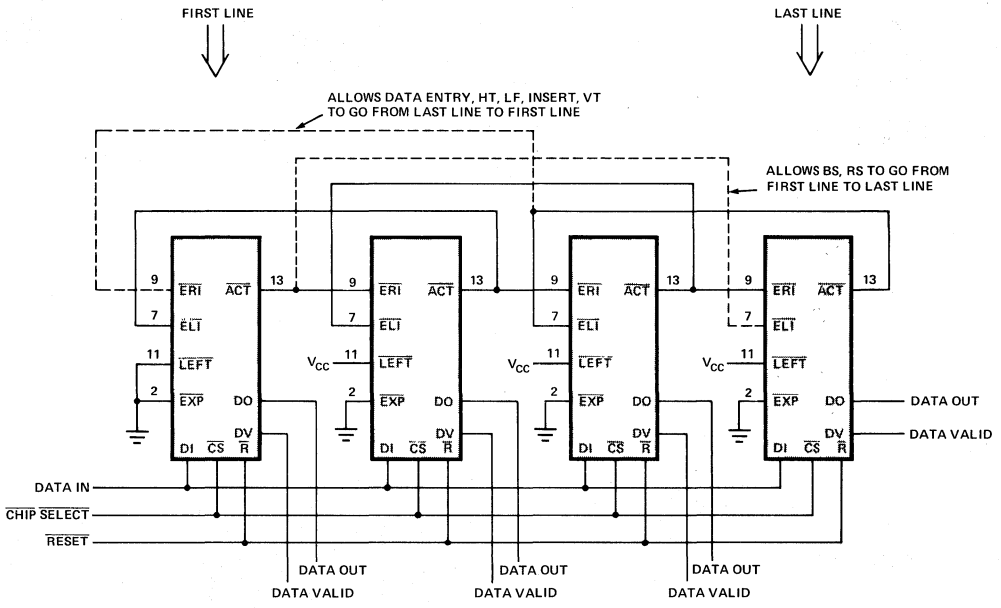


Figure 7. External Connections for Expanded Left Entry Mode for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a non-visible cursor, the cursor is always loaded with the address of the next character to be entered. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the six bit RAM address. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. The display can be cleared by loading in a new RAM control word.

Power-On Reset/$\overline{\text{Reset}}$

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the system loads the control word on the DATA INPUTS into the system. If $D_7 \leq 0.8V$ or the system sees an invalid control word, the system initializes as Left entry for a 40 character display with a flashing cursor in the leftmost location. During $\overline{\text{RESET}}$, the system also tests the state of the $\overline{\text{EXPAND}}$ input. If $\overline{\text{EXPAND}}$ is low, the system initializes in expanded left entry mode. A flow chart that describes the $\overline{\text{RESET}}$ function is shown in Figure 8. For POWER-ON RESET to function properly, the

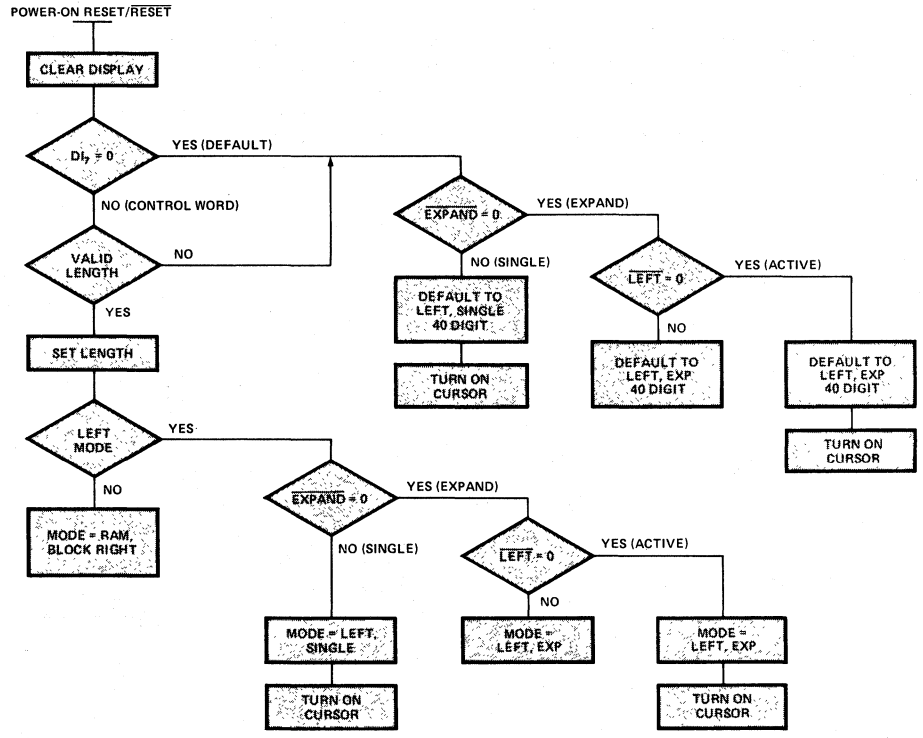


Figure 8. Reset Sequence for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the $\overline{\text{RESET}}$ input low for a minimum of 50 milliseconds. POWER-ON RESET/$\overline{\text{RESET}}$ timing is shown in Figure 9.

If some entry mode or display length is desired other than 40 character Left entry, it is necessary to either load the appropriate control word or provide a control word during POWER-ON RESET/$\overline{\text{RESET}}$. The circuit shown in Figure 10 can be used to load any desired preprogrammed control word into the HDSP-87XX Series Display Controller during POWER-ON RESET/$\overline{\text{RESET}}$.

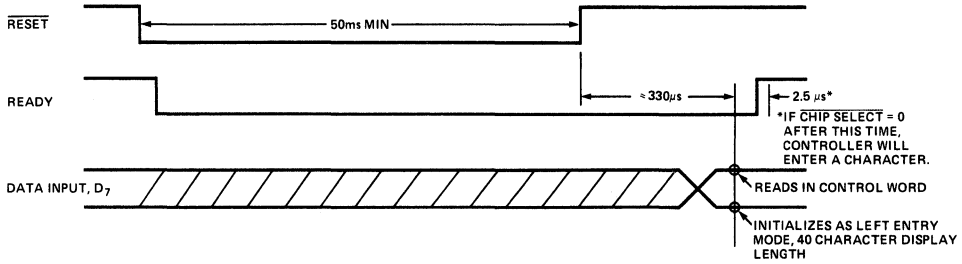
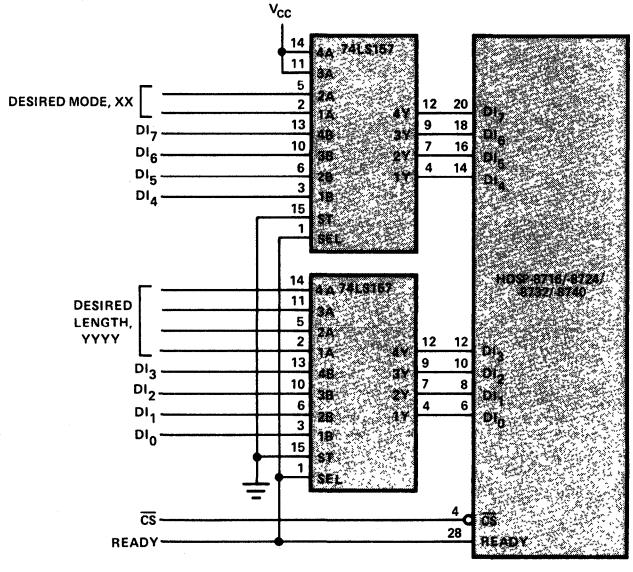


Figure 9. POWER-ON RESET/$\overline{\text{RESET}}$ Timing for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.



XX		YYYY	
00	RAM	0011	16 DIGITS
01	LEFT	0101	24 DIGITS
10	RIGHT	0111	32 DIGITS
11	BLOCK	1001	40 DIGITS

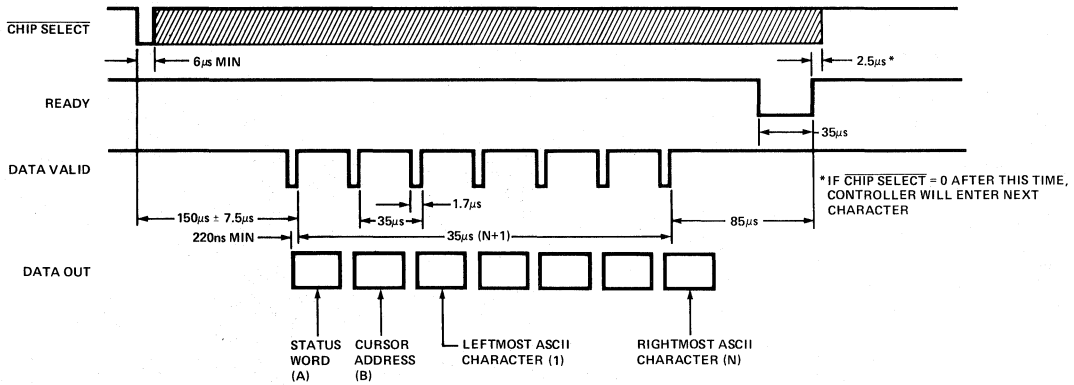
Figure 10. External Circuitry to Load a Control Word into the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System Upon POWER-ON RESET/$\overline{\text{RESET}}$.

Data Out

Data stored in the HDSP-87XX system is available to the user upon command. Data Out is initiated by the control word $1XXX11XX_2$. Following this control word, the system outputs a STATUS WORD, CURSOR ADDRESS, and a string of ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD is the same format as a valid control word with D_7 and D_6 deleted. The CURSOR ADDRESS specifies the location of the cursor within the display. The CURSOR ADDRESS of the leftmost display location is address 00. In Expanded Left entry mode, a CURSOR ADDRESS of 63 ($3F_{16}$) is used to indicate a non-active line. The system outputs the same number of ASCII data characters as the display length specified by the control word. The first ASCII data character is always the leftmost display character. The positive edge of the DATA VALID output can be used to load the DATA OUTPUT words into the user's system. The DATA OUT timing for the HDSP-87XX systems is summarized in Figure 11.

Luminous Intensity Modulation

Pulse width modulation of display luminous intensity can be provided by connecting the $\overline{\text{REFRESH}}$ output of the system to the input of a monostable multivibrator. The output of the monostable multivibrator should then be connected to the $\overline{\text{BLANK}}$ input of the system. Modulation of display luminous intensity is then achieved by varying the delay of the monostable multivibrator with a potentiometer or photoresistor. $\overline{\text{REFRESH}}$ is repeated at a rate of 10ms divided by the configured display length. For example, an HDSP-8732 system, when configured for a 32 character display length, would pulse the $\overline{\text{REFRESH}}$ output every 312.5μs. The circuit shown in Figure 12 may be utilized to provide manual control of display luminous intensity. Automatic control may be achieved by substituting an appropriate value photoconductor for potentiometer R_1. If luminous intensity modulation is not desired, $\overline{\text{BLANK}}$ should be left open.



STATUS WORD FORMAT (A)

$D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

0 0	Y Y Y Y	RAM ENTRY
0 1		LEFT ENTRY
1 0		RIGHT ENTRY
1 1		BLOCK ENTRY

Y Y Y Y = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (B)

CURSOR ADDRESS = NO. OF CHARACTERS FROM THE LEFT

HDSP	N
-8716	16
-8724	24
-8732	32
-8740	40

DATA WORD FORMAT (1 – N)

LOWEST 6 BITS OF ASCII CODE
WORD (1) = LEFTMOST DISPLAY CHARACTER
WORD (N) = RIGHTMOST DISPLAY CHARACTER

Figure 11. Data Out Timing and Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Microprocessor Interface

Interfacing the HDSP-87XX Series Display System to microprocessor systems depends on the needs of the particular application. Figure 13 shows a latched interface between the host microprocessor and the HDSP-87XX system. The latch provides temporary storage to avoid making the host microprocessor wait for the system to accept data. Data from the host microprocessor system is loaded into the 74LS273 octal register on the positive transition of the clock input (pin 11). At the same time, the $\overline{\text{CHIP SELECT}}$ input is forced low. The $\overline{\text{CHIP SELECT}}$ input stays low until READY goes low. The host microprocessor should avoid loading new data into the 74LS273 as long as BUSY is high. The latched interface can be implemented with an octal register and $\overline{\text{SR}}$ flip-flop if the HDSP-87XX system is operated in Left, Right, or Block entry. RAM entry requires an additional register for the RAM address inputs. Additional flexibility can be achieved by using a peripheral interface adapter (PIA) to interface the HDSP-87XX system to the host microprocessor system. The PIA provides a data entry handshake between the host microprocessor system and the HDSP-87XX system and allows the host microprocessor system to read the Data Output port of the HDSP-87XX system.

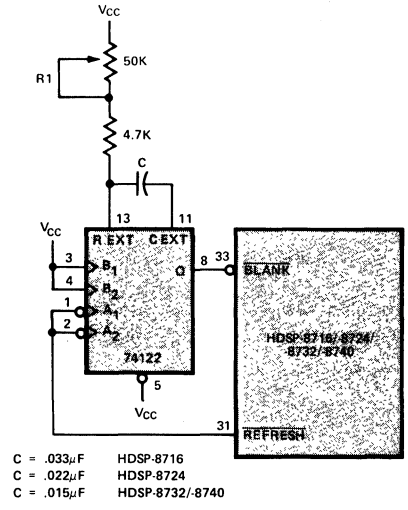
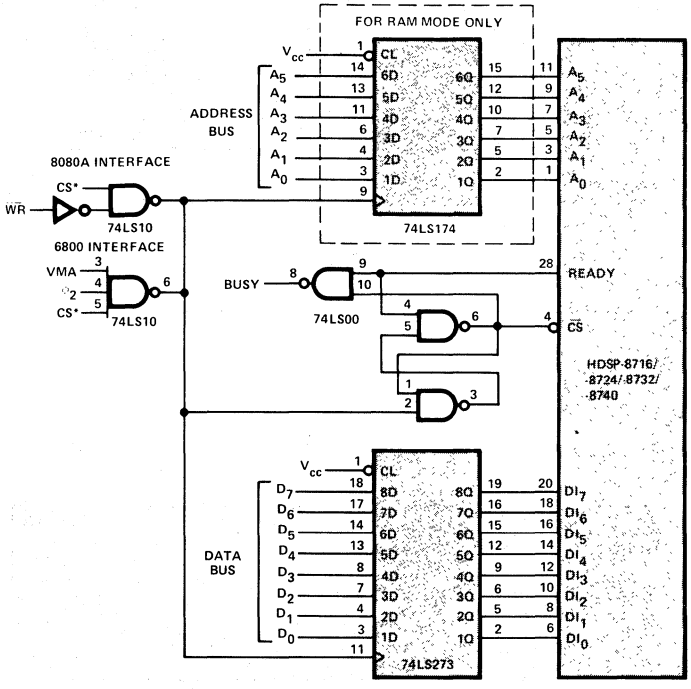


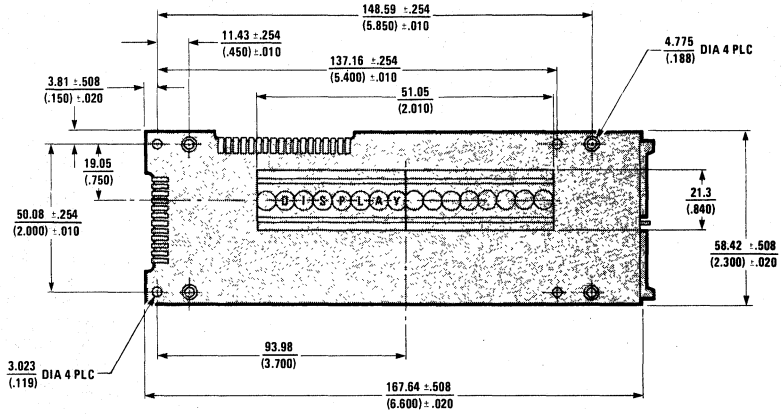
Figure 12. External Circuitry to Vary the Luminous Intensity of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.



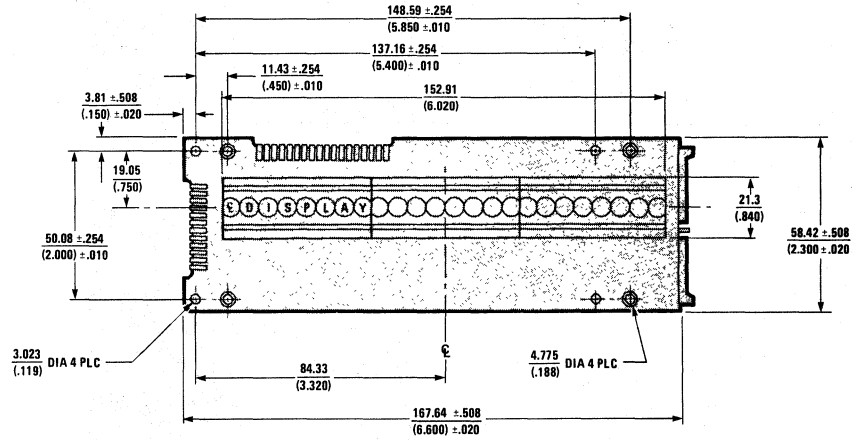
*CS IS A LOGICAL COMBINATION OF HIGH ORDER ADDRESS BITS THAT DISTINGUISH THE ADDRESS OF THE HDSP-8716/-8724/-8732/-8740 FROM THE REST OF THE MICROPROCESSOR SYSTEM.

Figure 13. Latched Interface to the HDSP-87XX Series Alphanumeric Display System.

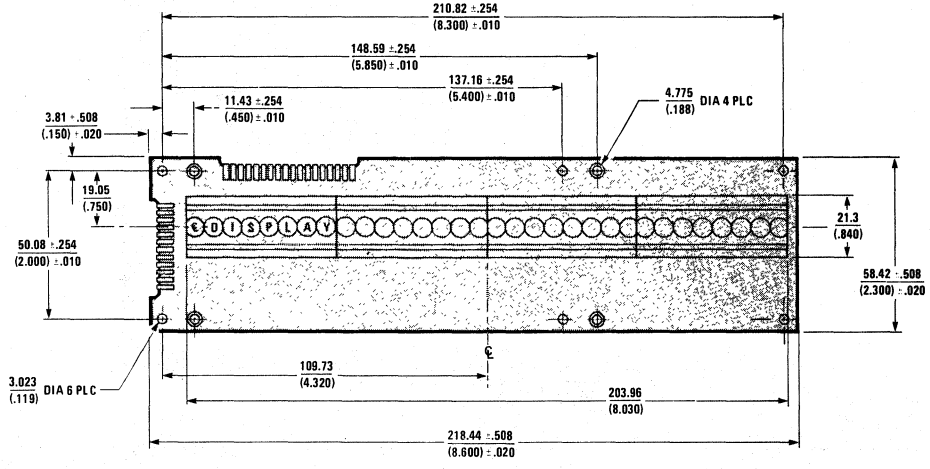
Package Dimensions



HDSP-8716

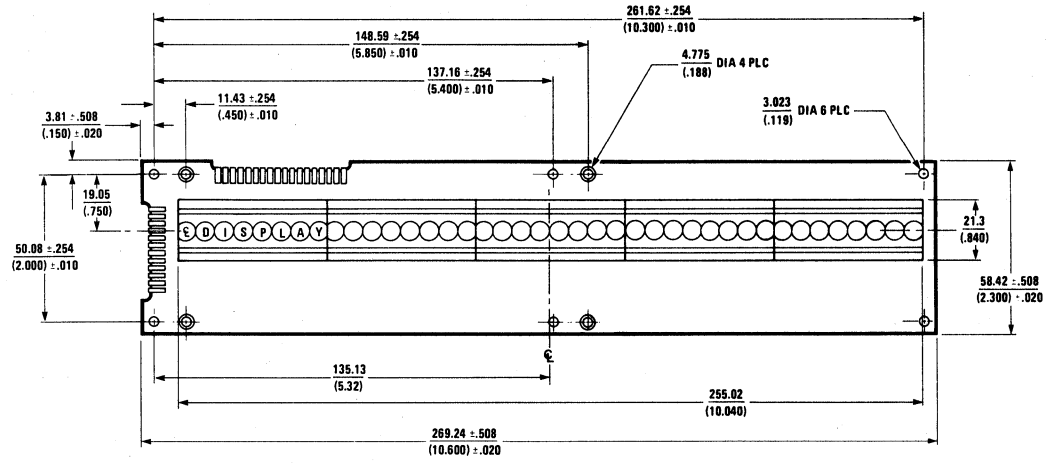


HDSP-8724

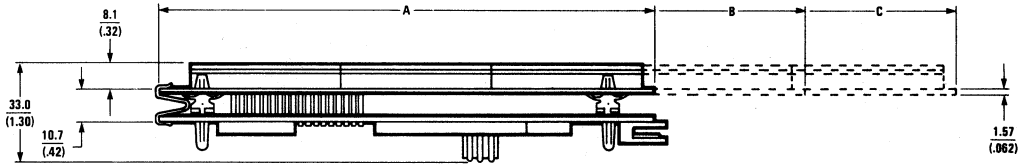


HDSP-8732

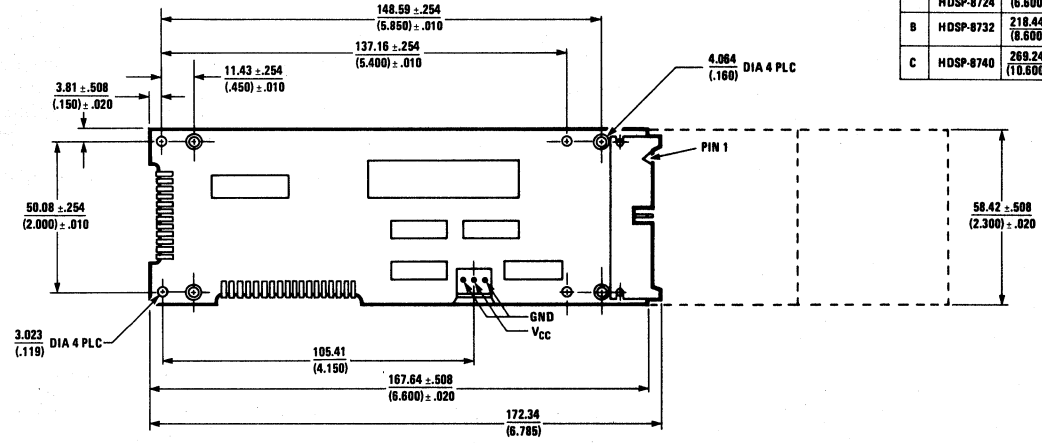
Package Dimensions



HDSP-8740



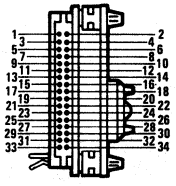
A	HDSP-8716 HDSP-8724	167.64 (6.600)
B	HDSP-8732	218.44 (8.600)
C	HDSP-8740	269.24 (10.600)



CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	34 PIN RIBBON CABLE	3M P/N 3414-X000 SERIES
POWER(1)	3 PIN WITH LOCKING RAMP	MOLEX P/N 09-50-3031 WITH 08-50-0106 TERMINALS

NOTES: (1) POWER LEADS SHOULD BE 18-20 GAUGE STRANDED WIRE.



PIN	DESCRIPTION
1	RAM ADDRESS, A_0
2	$\overline{\text{EXPAND}}$
3	RAM ADDRESS, A_1
4	$\overline{\text{CHIP SELECT}}$
5	RAM ADDRESS, A_2
6	DATA IN, D_0
7	RAM ADDRESS, A_3 (ELI)
8	DATA IN, D_1
9	RAM ADDRESS, A_4 (ERI)
10	DATA IN, D_2
11	RAM ADDRESS, A_5 (LEFT)
12	DATA IN, D_3
13	$\overline{\text{ACTIVE}}$
14	DATA IN, D_4
15	$\overline{\text{RESET}}$
16	DATA IN, D_5
17	NO CONNECTION

PIN	DESCRIPTION
18	DATA IN, D_6
19	NO CONNECTION
20	DATA IN, D_7
21	NO CONNECTION
22	DATA OUT, DO_0
23	DATA OUT, DO_1
24	DATA OUT, DO_2
25	DATA OUT, DO_3
26	DATA OUT, DO_4
27	DATA OUT, DO_5
28	READY
29	DATA VALID
30	400 kHz CLOCK OUT
31	$\overline{\text{REFRESH}}$
32	NO CONNECTION
33	$\overline{\text{DISPLAY BLANK}}$
34	NO CONNECTION

HDSP-8716/-8724/-8732/-8740

HEWLETT PACKARD

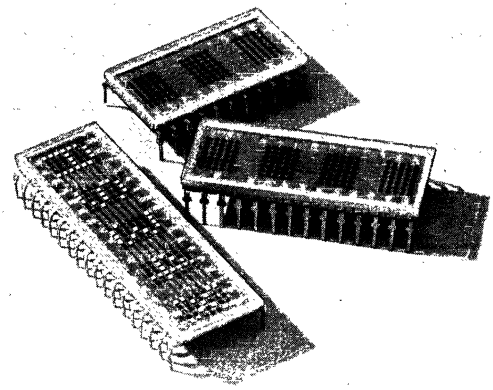
LED SOLID STATE ALPHANUMERIC INDICATOR

5082-7100
5082-7101
5082-7102

TECHNICAL DATA MARCH 1980

Features

- **5 x 7 LED MATRIX CHARACTER**
  Human Factors Engineered
- **BRIGHTNESS CONTROLLABLE**
- **IC COMPATIBLE**
- **SMALL SIZE**
  Standard 15.24mm (.600 inch) Dual In-Line Package; 6.9mm (.27 inch) Character Height
- **WIDE VIEWING ANGLE**
- **RUGGED, SHOCK RESISTANT**
  Hermetically Sealed
  Designed to Meet MIL Standards
- **LONG OPERATING LIFE**



Description

The Hewlett-Packard 5082-7100 Series is an X-Y addressable, 5 x 7 LED Matrix capable of displaying the full alphanumeric character set. This alphanumeric indicator series is available in 3, 4, or 5 character end-stackable clusters. The clusters permit compact presentation of information, ease of character alignment, minimum number of interconnections, and compatibility with multiplexing driving schemes.

Alphanumeric applications include computer terminals, calculators, military equipment and space flight readouts.

The **5082-7100** is a three character cluster.
The **5082-7101** is a four character cluster.
The **5082-7102** is a five character cluster.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current Per LED (Duration < 1 ms)	I_{PEAK}		100	mA
Average Current Per LED	I_{AVG}		10	mA
Power Dissipation Per Character (All diodes lit) [1]	P_D		700	mW
Operating Temperature, Case	T_C	–55	95	°C
Storage Temperature	T_S	–55	100	°C
Reverse Voltage Per LED	V_R		4	V

Note 1: At 25°C Case Temperature; derate 8.5 mW/°C above 25°C.

Electrical / Optical Characteristics at T_C=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Luminous Intensity Per LED (Character Average) @ Pulse Current of 100mA/LED	I_V (PEAK)	1.0	2.2		mcd
Reverse Current Per LED @ V_R = 4V	I_R		10		μA
Peak Forward Voltage @ Pulse Current of 50mA/LED	V_F		1.7	2.0	V
Peak Wavelength	λ_{PEAK}		655		nm
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		30		nm
Rise and Fall Times [1]	t_r, t_f		10		ns

Note 1. Time for a 10% - 90% change of light intensity for step change in current.

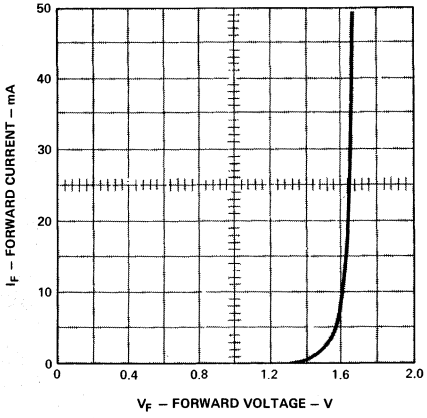


Figure 1. Forward Current-Voltage Characteristic.

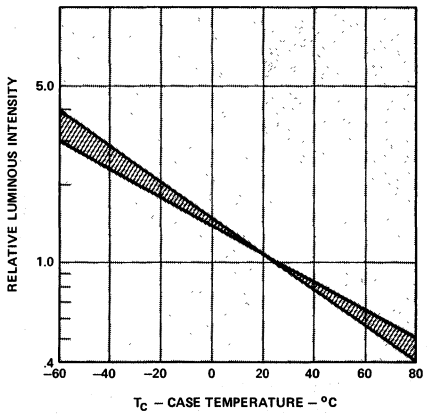


Figure 2. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

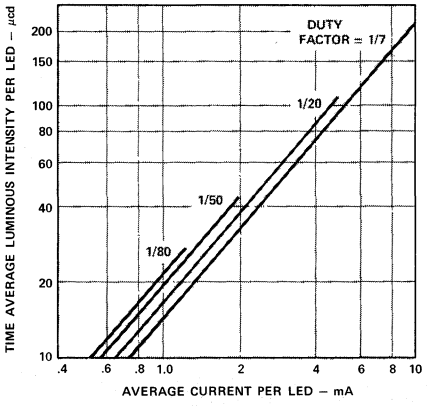


Figure 3. Typical Time Average Luminous Intensity per LED vs. Average Current per LED.

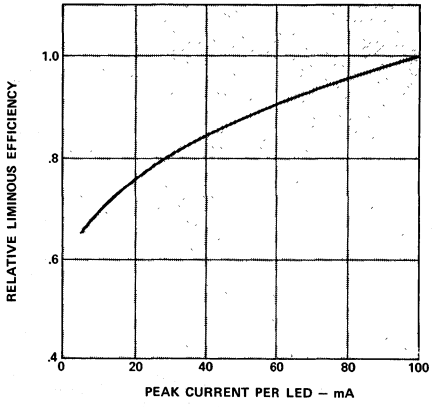
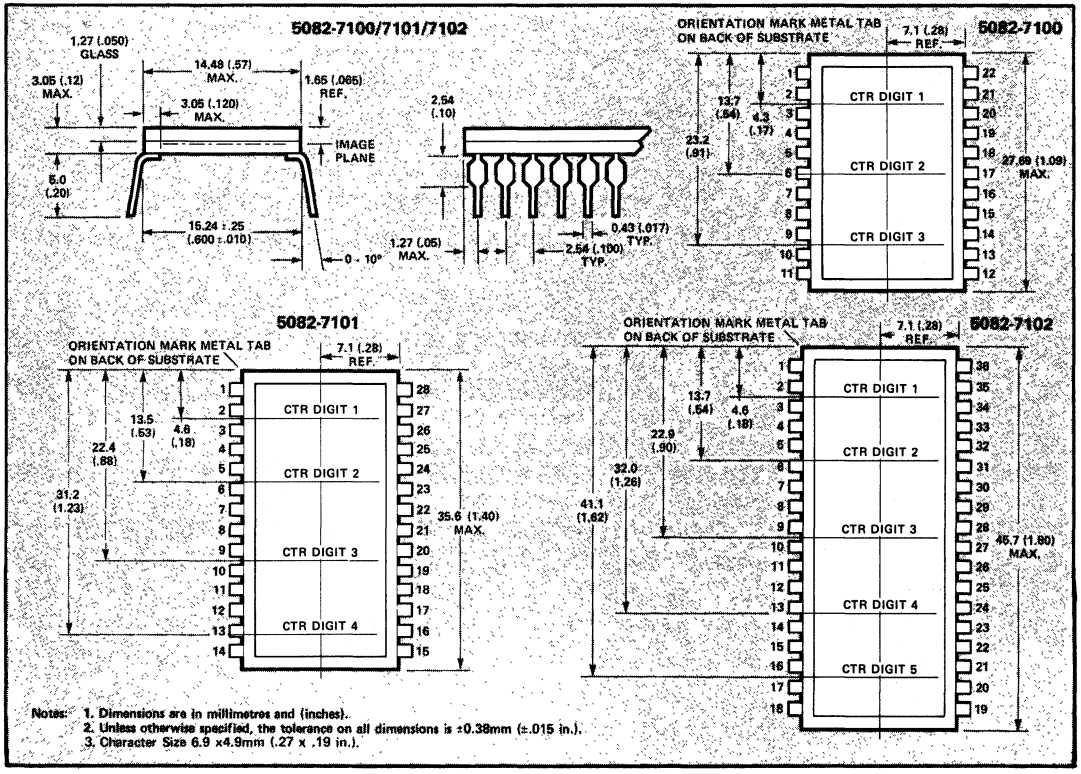


Figure 4. Typical Relative Luminous Efficiency vs. Peak Current per LED.

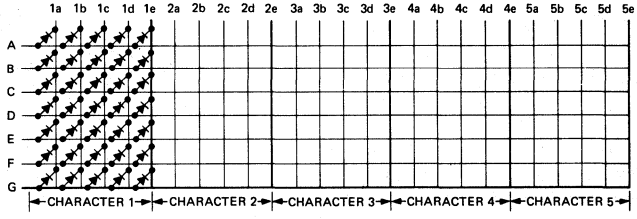
Package Dimensions and Pin Configurations



Notes: 1. Dimensions are in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38mm (±.015 in.).
3. Character Size 6.9 ×4.9mm (.27 x .19 in.).

Device Pin Description

5082-7100				5082-7101				5082-7102			
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Anode G	12	Anode B	1	N/C	15	Anode C	1	N/C	19	5e
2	1c	13	3d	2	1c	16	4c	2	1c	20	5c
3	1d	14	3b	3	1e	17	4a	3	1e	21	5a
4	Anode F	15	Anode A	4	Anode G	18	Anode B	4	Anode F	22	Anode D
5	Anode E	16	2e	5	2b	19	3e	5	2b	23	4e
6	2b	17	2c	6	2d	20	3b	6	2d	24	4c
7	2d	18	2a	7	Anode D	21	3a	7	2e	25	N/C
8	Anode C	19	Anode D	8	Anode E	22	2e	8	Anode E	26	Anode C
9	3a	20	1e	9	3c	23	2c	9	3c	27	3d
10	3c	21	1b	10	3d	24	2a	10	3e	28	3b
11	3e	22	1a	11	Anode F	25	Anode A	11	Anode G	29	3a
				12	4b	26	1d	12	4a	30	Anode B
				13	4d	27	1b	13	4b	31	2c
				14	4e	28	1a	14	4d	32	2a
								15	N/C	33	Anode A
								16	5b	34	1d
								17	5d	35	1b
								18	N/C	36	1a



5082-7100/7101/7102
Schematic Wiring Diagram

Operating Considerations

ELECTRICAL

The 5 x 7 matrix of LED's, which make up each character, are X-Y addressable. This allows for a simple addressing, decoding and driving scheme between the display module and customer furnished logic.

There are three main advantages to the use of this type of X-Y addressable array:

1. It is an elementary addressing scheme and provides the least number of interconnection pins for the number of diodes addressed. Thus, it offers maximum flexibility toward integrating the display into particular applications.
2. This method of addressing offers the advantage of sharing the Read-Only-Memory character generator among several display elements. One character generating ROM can be shared over 25 or more 5 x 7 dot matrix characters with substantial cost savings.
3. In many cases equipments will already have a portion of the required decoder/driver (timing and clock circuitry plus buffer storage) logic circuitry available for the display.

To form alphanumeric characters a method called "scanning" or "strobing" is used. Information is addressed to the display by selecting one row of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been excited one at a time, the process is repeated. By scanning through all rows at least 100 times a second, a flicker free character can be produced. When information moves sequentially from row to row of the display (top to bottom) this is row scanning, as illustrated in Figure 5. Information can also be moved from column to column (left to right across the display) in a column scanning mode. For most applications (5 or more characters to share the same ROM) it is more economical to use row scanning.

A much more detailed description of general scanning techniques along with specific circuit recommendations is contained in HP Application Note 931.

MECHANICAL/THERMAL MOUNTING

The solid state display typically operates with 200 mW power dissipation per character. However, if the operating conditions are such that the power dissipation exceeds the derated maximum allowable value, the device should be heat sunk. The usual mounting technique combines mechanical support and thermal heat sinking in a common structure. A metal strap or bar can be mounted behind the display using silicone grease to insure good thermal control. A well-designed heat sink can limit the case temperature to within 10°C of ambient.

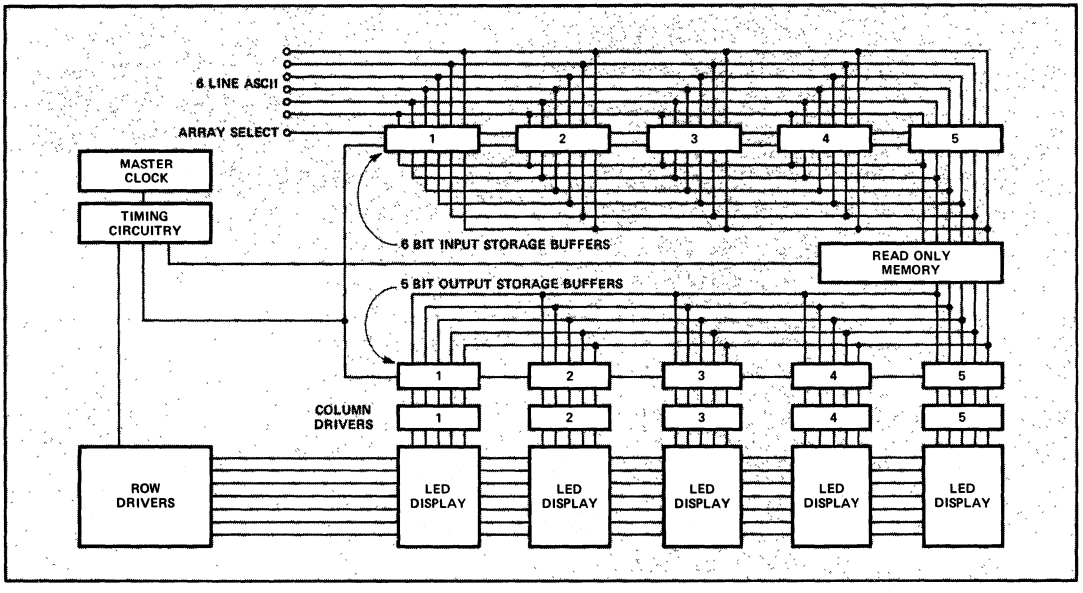
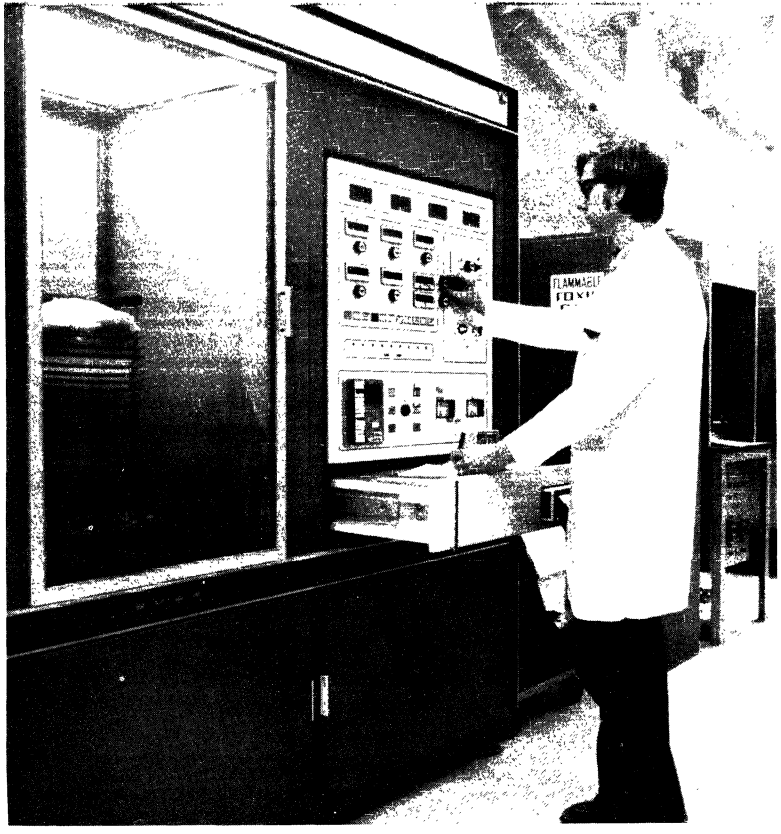


Figure 5. Row Scanning Block Diagram.



High Reliability

High Reliability, Military Parts

Hewlett-Packard product designs and manufacturing methods assure our ability to supply high reliability products patterned after MIL-S-19500 and MIL-M-38510 programs. Testing programs may include 100% screening tests with precap visual, lot qualification or both. Programs performed to customer drawings and specifications are available and strictly follow their control documents and procedures.

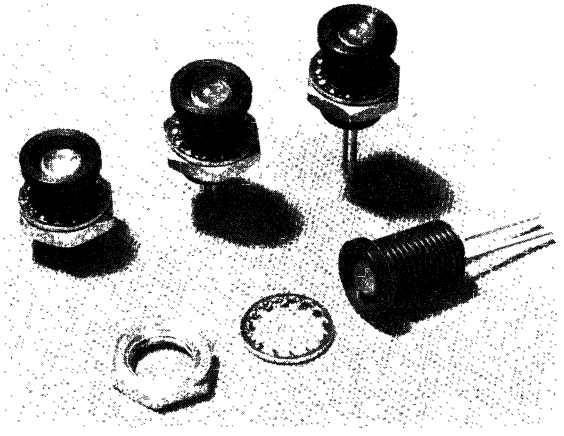
PROGRAM CAPABILITIES

	Available Programs*		
HERMETIC PRODUCTS	**Lot Qual.**	**100% Screen**	**100% Screen and Lot Qual.**
Lamps Meet MIL-S-19500	JAN	—	JANTX
Displays Using Hybrid Die Configuration Patterned to Class B of MIL-M-38510	—	TXV	TXVB
Optocouplers Using Hybrid Die Configuration Designed Against Class B of MIL-M-38510	—	TXV	TXVB
Optocouplers with Controls of MIL-M-38510 Class S	X	X	X
Special Optocoupler Assemblies with Testing Patterned to Class B or S or MIL-M-38510	X	X	X
NON HERMETIC PRODUCTS			
All Products to Customer Test Programs Designed Against MIL-S-19500 or MIL-M-38510 Class B	X	X	X

*Testing program details vary between products based on device design objectives, product history and capabilities.

— Not Available

X Available



Hewlett-Packard Components have three types of package sealing methods to meet different customer needs in the market. The recommended high reliability part is packaged in a conventional glass to glass, glass to metal seal or equivalent sealing technique using ceramic. These products are impervious to moisture and meet hermeticity testing to prescribed levels.

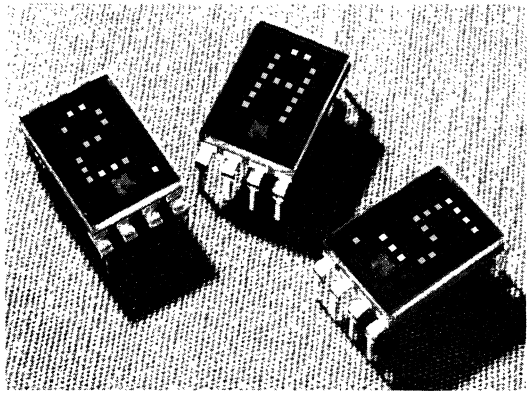
In addition to our hermetic products, Hewlett-Packard makes units which use an epoxy seal. These units are also capable of passing hermeticity testing and can be utilized in those high reliability applications with limited moisture exposure over long periods.

A third package type is also non-hermetic using complete epoxy encapsulation material to form both the package structure and outline. These products are often used in non man rated ground support programs and successfully pass customer lot acceptance qualification testing and 100% screening programs designed for plastic components.

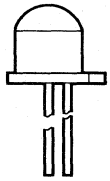
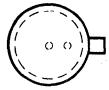
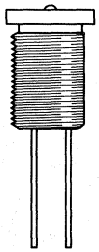
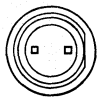
The optional tests in the following recommended screening sequence for non-hermetic devices are based on package configuration, point of assembly and customer preference. The conditions for all selected tests are product design dependent and are based on absolute maximum ratings.

Test Sequence	MIL-STD-883 Method	MIL-STD-750 Method	Non-Hermetic Program
1. Pre Cap Visual	HP Procedure	HP Procedure	Optional
2. High Temperature Storage	1008	1031	100 Percent
3. Temperature Cycling	1010	1051	Optional
4. Constant Acceleration	2001	NA	Optional
5. Fine Leak	1014	1071	Optional
6. Gross Leak	1014	1071	Optional
7. Interim Electrical/Optical Tests	—	—	Optional
8. Burn In	1015	1038	100 Percent
9. Final Electrical/Optical Tests	—	—	100 Percent
10. Delta Drift Measurements	—	—	Optional
11. External Visual	2009	2071	100 Percent

Hewlett-Packard's emphasis on reliability extends across commercial and high reliability markets. As part of our new product introduction and periodically during the life of a part, samples from typical manufacturing lots are subjected to qualification testing. The data obtained from these tests indicates reliability levels maintained by the product family and is assembled periodically into Reliability Summary data sheets. Copies may be obtained from your local Hewlett-Packard field sales office.

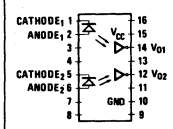
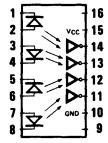
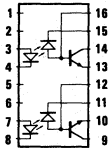


Hermetically Sealed and High Reliability LED Lamps

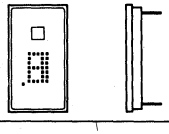
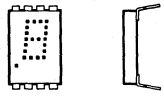
Device		Description			Minimum Luminous Intensity	$2\Theta_{1/2}$ [1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color [2]	Package	Lens				
 	1N5765 JAN 1N5765 [5] JANTX 1N5765 [5]	Red (655 nm)	Hermetic/TO-46 [4]	Red Diffused	0.5 mcd @ 20mA	70°	1.6 Volts @ 20mA	165
	1N6092 JAN 1N6092 [5] JANTX 1N6092 [5]	High Efficiency Red (635 nm)			1.0 mcd @ 20mA		2.0 Volts @ 20mA	
	1N6093 JAN 1N6093 [5] JANTX 1N6093 [5]	Yellow (583 nm)		Yellow Diffused				
	1N6094 JAN 1N6094 [5] JANTX 1N6094 [5]	Green (565 nm)		Green Diffused	0.8 mcd @ 25mA		2.1 Volts @ 20mA	
 	5082-4787 HLMP-0930 [5] HLMP-0931 [5]	Red (655 nm)	Panel Mount Version [3]	Red Diffused	0.5 mcd @ 20mA		1.6 Volts @ 20mA	
	5082-4687 M 19500/519-01 [5] M 19500/519-02 [5]	High Efficiency Red (635 nm)			1.0 mcd @ 20mA		2.0 Volts @ 20mA	
	5082-4587 M 19500/520-01 [5] M 19500/520-02 [5]	Yellow (583 nm)		Yellow Diffused				
	5082-4987 M 19500/521-01 [5] M 19500/521-02 [5]	Green (565 nm)		Green Diffused	0.8 mcd @ 25mA		2.1 Volts @ 20mA	

See page 309 for notes.

Hermetic Optocouplers

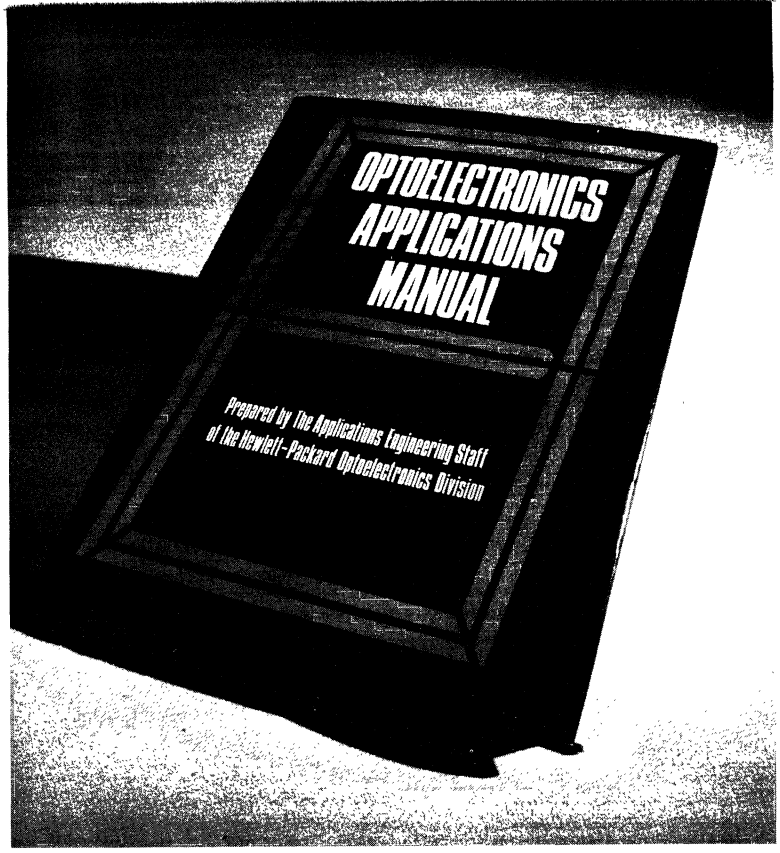
Device		Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134 6N134TXV 6N134TXVB	Dual Channel Hermetically Sealed Optically Coupled Logic Gate. TXV – Screened TXVB – Screened with Group B Data	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10mA	1500Vdc	90
	6N140 6N140TXV 6N140TXVB	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers TXV – Hi-Rel Screened TXVB – Hi-Rel Screened with Group B Data	Line Receiver, Low Power Ground Isolation for High Reliability Systems	300k bit/s	300% Min.	0.5mA	1500Vdc	94
	4N55 4N55TXV 4N55TXVB	Dual Channel Hermetically Sealed Analog Optical Coupler TXV – Hi-Rel Screened TXVB – Hi-Rel Screened with Group B Data	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	7% Min.	16mA	1500Vdc	98

Hermetically Sealed Integrated LED Displays

Device		Description	Package	Application	Page No.
	5082-7010	6.8mm (.27") 5x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver	8 Pin Hermetic 2.54mm (.100") Pin Centers	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems	241
	5082-7011	6.8mm (.27") Plus/Minus Sign			
	5082-7391	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Hermetic 15.2mm (.6") DIP with Gold Plated Leads	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Applications	247
	5082-7392	7.4mm(.29") 4x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
	5082-7395	7.4mm(.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7393	7.4mm(.29") Overrange Character Plus/Minus Sign			

NOTES: 1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Peak Wavelength.
3. For Panel Mounting Kit, see page 171.
4. PC Board Mountable.
5. Military Approved and qualified for High Reliability Applications.

For Applications Information, see page 311.



Applications Information

Below is a complete listing of all of the Optoelectronic Applications Information available. For those items which were not included in this catalog, a brief abstract is shown. These are available in their entirety from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

APPLICATION BULLETINS

Model/Pub. No. (Date)	Description	Ref.
AB-1/5952-8378 (1/75)	Construction and Performance of High Efficiency Red, Yellow and Green LED Materials	Abst.
AB-3/5952-8380 (3/75)	Soldering Hewlett-Packard Silver Plated Lead Framed LED Devices	P. 315
AB-4/5952-8381 (4/75)	Detection and Indication of Segment Failures in 7-Segment LED Displays	Abst.
AB-52/5953-0330 (3/77)	Large Monolithic LED Displays	Abst.
AB-54/5953-0363 (7/77)	Mechanical Handling of Sub-miniature LED Lamps and Arrays	Abst.
AB-56/5953-0415 (11/79)	Interface Timing and Display Length Expansion Information for the HDSP-2000 Coded Data Controller	P. 319
AB-57/5953-0418 (1/80)	Flux Budget Considerations for Fiber Optic Link Design	P. 323

APPLICATIONS MANUAL

Model/Pub. No. (Date)	Description	Ref.
HPBK-1000 McGraw-Hill (No. 0-07-028605-1) (1977)	Optoelectronics Applications Manual	Abst.

APPLICATION NOTES

Model/Pub. No. (Date)	Description	Ref.
AN-915/5953-0431 (4/80)	Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes	P. 326
AN-931/5952-0235 (11/70)	Solid State Alphanumeric Display, Decoder/Driver Circuitry	Abst.
AN-934/5952-0337 (11/72)	5082-7300 Series Solid State Display Installation Techniques	Abst.
AN-937/5952-0396 (5/73)	Monolithic 7-Segment LED Display Installation Techniques	Abst.
AN-939/5952-0331 (11/72)	High Speed Optically Coupled Isolators	Abst.
AN-941/5952-0418 (9/73)	5082-7700 Series 7-Segment Display Applications	P. 332
AN-945/5952-0420 (10/73)	Photometry of Red LEDs	Abst.
AN-946/5952-0429 (11/73)	5082-7430 Series Monolithic 7-Segment Displays	Abst.
AN-947/5952-8497 (7/76)	Digital Data Transmission Using Optically Coupled Isolators	Abst.
AN-948/5952-0458 (3/74)	Performance of the 5082-4350/51/60 Series of Isolators in Short to Moderate Length Digital Data Transmission Systems	P. 343
AN-951-1/5953-0413 (11/79)	Applications for Low Input Current, High Gain Optically Coupled Isolators	P. 352
AN-951-2/5952-8451 (5/76)	Linear Applications of Optically Coupled Isolators	P. 356
AN-964/5952-8345 (3/75)	Contrast Enhancement Techniques	P. 360
AN-966/5953-0427 (2/80)	Applications of the HDSP-2000 Alphanumeric Display	P. 368
AN-1000/5953-0391 (11/78)	Digital Data Transmission with the HP Fiber Optic System	P. 380
AN-1001/5953-0384 (10/78)	Interfacing the HDSP-2000 to Microprocessor Systems	P. 398
AN-1002/5953-0385 (6/79)	Consideration of CTR Variations in Optically Coupled Isolator Circuit Designs	P. 414
AN-1003/5953-0405 (9/79)	Interfacing 18-Segment Displays to Microprocessors	P. 430
AN-1004/5953-0406 (11/79)	Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler	P. 450
AN-1005/5953-0419 (3/80)	Operational Considerations for LED Lamps and Display Devices	P. 464

Abstracts

APPLICATION BULLETIN 1
Construction and Performance of High Efficiency Red, Yellow and Green LED Materials

The high luminous efficiency of Hewlett-Packard's High Efficiency Red, Yellow and Green lamps and displays is made possible by a new kind of light emitting material utilizing a GaP transparent substrate. This application bulletin discusses the construction and performance of this material as compared to standard red GaAsP and red GaP materials.

APPLICATION BULLETIN 4
Detection and Indication of Segment Failures in Seven Segment LED Displays

The occurrence of a segment failure in certain applications of seven segment displays can have serious consequences if a resultant erroneous message is read by the viewer. This application bulletin discusses three techniques for detecting open segment lines and presenting this information to the viewer.

APPLICATION BULLETIN 52
Large Monolithic LED Displays

The trend to incorporate more complex functions into smaller package configurations that are portable and battery powered is reaching a point where the limiting items are the space and power constraints imposed upon the display at the operator-to-machine interface. The large monolithic LED display has been designed to meet many of these constraints. This application bulletin describes the beneficial features of a large monolithic LED display and presents circuits which interface the display to CMOS logic and to a microprocessor.

APPLICATION BULLETIN 54
Mechanical Handling of Subminiature LED Lamps and Arrays

The Need for Careful Mechanical Handling

Hewlett-Packard manufactures a series of individual LED lamps and lamp arrays that are very small epoxy encapsulated devices. These devices are classified as having a SUBMINIATURE package configuration. When carefully installed on a printed circuit board, these devices will reliably function with a long predictable operating life.

To obtain long operating life, these subminiature devices must be carefully installed on the printed circuit board in such a manner as to insure the integrity of the encapsulating epoxy. This will in turn maintain the integrity of the device by not permitting mechanical and thermal stresses to induce strains on the LED die attach and wire bonds which may cause failure.

This application bulletin describes the subminiature package assembly, the package's mechanical limitations and offers specific suggestions for proper installation.

APPLICATION NOTE 931
Solid State Alphanumeric Display...Decoder/ Driver Circuitry

Hewlett-Packard offers a series of solid state displays capable of producing multiple alphanumeric characters utilizing 5 x 7 dot arrays of GaAsP light emitting diodes (LED's). These 5 x 7 dot arrays exhibit clear, easily read characters. In addition, each array is X-Y addressable to allow for a simple addressing, decoding, and driving scheme between the display module and external logic.

Methods of addressing, decoding and driving information to such an X-Y addressable matrix are covered in detail in this application note. The note starts with a general definition of the scanning or strobing technique used for this simplified addressing and then proceeds to describe horizontal and vertical strobing. Finally, a detailed circuit description is given for a practical vertical strobing application.

APPLICATION NOTE 934
5082-7300 Series Solid State Display Installation Techniques

The 5082-7300 series Numeric/Hexadecimal indicators are an excellent solution to most standard display problems in commercial, industrial and military applications. The unit integrates the display character and associated drive electronics in a single package. This advantage allows for space, pin and labor cost reductions, at the same time improving overall reliability.

The information presented in this note describes general methods of incorporating the -7300 into varied applications.

Abstracts

APPLICATION NOTE 937
Monolithic Seven Segment LED Display Installation Techniques

The Hewlett-Packard series of small end-stackable monolithic GaAsP displays are designed for strobing, a drive method that allows time sharing of the character generator among the digits in a display.

This Application Note begins with an explanation of the strobing technique, followed by a discussion of the uses and advantages of the right hand and center decimal point products.

Several circuits are given for typical applications. Finally, a discussion of interfacing to various data forms is presented along with comments on mounting the displays.

APPLICATION NOTE 939
High Speed Optically Coupled Isolators

Often designers are faced with the problem of providing circuit isolation in order to prevent ground loops and common mode signals. Typical devices for doing this have been relays, transformers and line receivers. However, both relays and transformers are low speed devices, incompatible with modern logic circuits. Line receiver circuits are fast enough, but are limited to a common mode voltage of 3 volts.

In addition, they do not protect very well against ground loop signals. Now Optically Coupled Isolators are available which solve most isolation problems.

This Application Note contains a description of Hewlett-Packard's high speed isolators, and discusses their applications in digital and analog systems.

APPLICATION NOTE 945
Photometry of Red LEDs

Nearly all LEDs are used either as discrete indicator lamps or as elements of a segmented or dot-matrix display. As such, they are viewed directly by human viewers, so the primary criteria for determining their performance is the judgment of a viewer. Equipment for measuring LED light output should, therefore, simulate human vision.

This Application Note will provide answers to these questions:

1. What to measure (definitions of terms)
2. How to measure it (apparatus arrangement)
3. Whose equipment to use (criteria for selection)

APPLICATION NOTE 947
Digital Data Transmission Using Optically Coupled Isolators

Optically coupled isolators make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common mode interference between two isolated data transmission systems. This application note describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common mode rejection. Both resistive and active terminations are described in detail. Specific techniques are described for multiplexing applications, and for common mode rejection and data rate enhancement.

OPTOELECTRONICS APPLICATIONS MANUAL (HPBK-1000)

The commercial availability of the Light Emitting Diode has provided electronic system designers with a revolutionary component for application in the areas of information display and photocouplers.

Many electronic engineers have encountered the need for a resource of information about the application of and designing with LED products. This book is intended to serve as an engineering guide to the use of a wide range of solid state optoelectronic products.

The book is divided into chapters covering each of the generalized LED product types. Additional chapters treat such peripheral information as contrast enhancement techniques, photometry and radiometry, LED reliability, mechanical considerations of LED devices, photodiodes and LED theory.

This book can be purchased from a Hewlett-Packard franchised distributor or from the McGraw-Hill Publishing Company. A complete listing of all HP Components franchised distributors can be found on pages 472-474.

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COMPONENTS

APPLICATION BULLETIN 3

Soldering Hewlett-Packard Silver Plated Lead Frame LED Devices

INTRODUCTION

Since the price of gold has increased several times over past years, the cost of a gold plated lead frame has increased substantially above the cost of a silver plated lead frame. The impact of this increase in cost has been industry wide.

By using silver plating, no additional manufacturing process steps are required. Silver has excellent electrical conductivity. LED die attach and wire bonding to a silver lead frame is accomplished with the same reliability as with a gold lead frame. Also, soldering to a silver lead frame provides a reliable electrical and mechanical solder joint. Soldering silver plated lead frame LED devices into a printed circuit board is not more complicated than soldering LED devices with gold plated lead frames. This application bulletin offers some suggestions on how to solder HP silver plated lead frame LED devices.

THE SILVER PLATING

The silver plating process is performed as follows: The lead frame base metal is activated (cleaned) and then plated with a copper strike, nominally 50 microinches (0.00127mm) thick. Then a minimum 150 microinch (0.00381mm) thick plating of silver is added. A "brightener" is usually added to the silver plating bath to insure an optimum surface texture to the silver plating. The term "brightener" comes from the medium bright surface reflectance of the silver plate.

Since silver is porous with respect to oxygen, the copper strike acts as an oxygen barrier for the lead frame base metal. Thus, oxide compounds of the base metal are prevented from forming underneath the silver plating. Copper readily diffuses into silver forming a solution that has a low temperature eutectic point. The interdiffusion between the copper strike and the silver overplate improves the solderability of the overall plating system. If basic soldering time and temperature limits are not exceeded, a lead frame base metal-copper-silver-solder metallurgical bonding system will be obtained.

THE EFFECT OF TARNISH

Silver reacts chemically with sulfur to form the tarnish, silver sulfide (Ag_2S). The build-up of tarnish is the primary reason for poor solderability. However, the density of the tarnish and the kind of solder flux used actually determine the solderability. As the density of the tarnish increases, the more active the flux must be to penetrate and remove the tarnish layer. Some recommended fluxes and cleaner/surface conditions are discussed in the "Solder, Flux and Cleaners" section.

STORAGE AND HANDLING

The best technique for insuring good solderability of a silver plated lead frame device is to prevent the formation of tarnish. This is easily accomplished by preventing the leads from being exposed to sulfur and sulfur compounds. The two primary sources of sulfur are free air and most paper products such as paper sacks and cardboard containers. The best defense against the formation of tarnish is to keep silver lead frame devices in protective packaging until just prior to the soldering operation. One way to accomplish this is to store the LED devices unwrapped in their original packaging as received from HP. For example, Hewlett-Packard ships its seven segment display products in plastic tubes which are sealed air tight in polyethylene. It is best to leave the polyethylene intact during storage and open just prior to soldering.

Listed below are a few suggestions for storing silver lead frame devices.

1. Store the devices in the original wrapping unopened until just prior to soldering.
2. If only a portion of the devices from a single tube are to be used, tightly re-wrap the plastic tube containing the unused devices in the original or a new polyethylene sheet to keep out free air.
3. Loose devices may be stored in zip-lock or tightly sealed polyethylene bags.
4. For long term storage of parts, place one or two petroleum napthalene mothballs inside the plastic package containing the devices. The evaporating napthalene creates a vapor pressure inside the plastic package which keeps out free air.
5. Any silver lead frame device may be wrapped in "Silver Saver" paper for positive protection against the formation of tarnish. "Silver Saver" is manufactured by:

   The Orchard Corporation
   1154 Reco Avenue
   St. Louis, Missouri 63126 (312) 822-3888

6. To reduce shelf storage time, it will be worthwhile to use inventory control to insure that the devices first received will be the first devices to be used.

   One caution: The adhesives used on pressure sensitive tapes such as cellophane, electrical and masking tape can soak through silver protecting papers and may leave an adhesive film on the leads. This film reduces solderability and should be removed with freon T-P35, freon T-E35 or equivalent prior to soldering.

SOLDER, FLUX AND CLEANERS

The solder most widely used for soldering electronic components into printed circuit boards is Sn60 (60% tin and 40% lead) per federal standard QQ-S-571. Two alternates are the eutectic composition Sn63 and the 2% silver solder Sn62.

As the device leads pass through the solder wave of a flow solder process, the tin in the solder scavenges silver from the silver plating and forms one of two silver-tin intermetallics (Ag_6Sn or Ag_3Sn). This silver in the molten solder should not be considered a contaminant. As the silver content increases, the rate of scavenging decreases and the probability of obtaining the desired base metal-copper-silver-solder metallurgical system is improved. The result is that the silver content in solder, which reaches a maximum of 2-1/2% in Sn60 at 230°C, aids in producing reliable solder joints on silver plated lead frames.

Solder flux classifications per federal standard QQ-S-571, listed in order of increasing strength, are as follows:

Type R: Non-Activated Rosin Flux
Type RMA: Mildly Activated Rosin Flux
Type RA: Activated Rosin Flux
Type AC: Organic Acid Flux, Water Soluble

Suggested applications of these flux types with respect to various tarnish levels are as follows:

Silver plated lead frames that are clean, contaminant and tarnish free may be soldered using a Type R flux such as Alpha 100.

Minor Tarnish

Since some minor tarnish or other contaminant may be present on the leads, a type RMA flux such as Alpha 611 or 611 Foam, Kester 197 or equivalent is recommended. Minor tarnish may be identified by reduced reflectance of the ordinarily medium bright surface of the silver plating. Type RMA fluxes which meet MIL-F-14256 are used in the construction of telephone communication, military and aero space equipment.

Mild Tarnish

For a mild tarnish, a type RA flux such as Alpha 711-35, Alpha 809 foam, Kester 1544, Kester 1585 or equivalent should be used. A mild tarnish may be identified by a light yellow tint to the surface of the silver plating.

Moderate Tarnish

A type AC water soluable flux such as Alpha 830, Alpha 842, Kester 1429 or 1429 foam, Lonco 3355 or equivalent will give acceptable results on surface conditions up to a moderate tarnish. A moderate tarnish may be identified by a light yellow-tan color on the surface of the silver plating.

If a more severe tarnish is present, such as a heavy tarnish identified by a dark tan to black color, a cleaner/surface conditioner must be used. Some possible cleaner/surface conditioners are Alpha 140, Alpha 174, Kester 5560, and Lonco TL-1. The immersion time for each cleaner/surface conditioner will be just a few seconds and each is used at room temperature. For example, Alpha 140 will remove severe tarnish almost upon contact; therefore, the immersion time need not exceed 2 seconds. These cleaner/surface conditioners are acidic formulations. Therefore, thoroughly wash all devices which have been cleaned with a cleaner/surface conditioner in cold water. A hot water wash will cause undue etching of the surface of the silver plating. A post rinse in deionized water is advisable.

CAUTION: These cleaner/surface conditioners may etch exposed glass and may have a detrimental effect upon the glass filled encapsulating epoxies used in optoelectronic devices. Complete immersion of an optoelectronic device into a surface conditioner solution is NOT recommended. For best results, immerse only the tarnished leads and do not expose the encapsulating epoxy to the solutions.

The cleaning of printed circuit boards after soldering is important to remove ionic contaminants and increase circuit reliability. When a Type RMA or Type RA flux is used, vapor clean with an azeotrope of fluorocarbon F113 and approximately 15% alcohol by weight. Some equivalent products are Allied Chemical Genesolve DI-15/DE-15, Blaco-Tron DE-15/DI-15 and Arklone K. A Type RMA or Type RA flux is a mixture of basic Type R rosin flux and an organic acid. The fluorocarbon F113 removes the residual rosin and the alcohol removes the residual active ions. Room temperature cleaning may be accomplished by using Freon T-E35, T-P35 or equivalent. When a Type AC flux is used, wash thoroughly with water. Specific cleaning processes are suggested in the soldering process section.

SOLDERING PROCESS

Before the actual soldering begins, the printed circuit boards and components to be soldered should be free of dirt, oil, grease, finger prints and other contaminants. Fluorinated cleaners such as Freon T-P35 may be used to preclean both the printed circuit boards and LED devices. Operators may wear cotton gloves to prevent finger prints when loading components into the printed circuit boards.

If the silver lead frames have acquired an unacceptable layer of tarnish, remove this tarnish layer with a cleaner/surface conditioner just prior to soldering. Since a cleaner/surface conditioner does slightly etch the surface of the silver plating, the silver leads are now more susceptible to tarnish formation. Therefore, use a cleaner/surface conditioner only on those silver lead frame devices which will be soldered within a four hour time period. The effect of various tarnish levels on the choice of flux is discussed in the previous section.

Many of Hewlett-Packard's LED Lamps and Display products have a soldering specification of 230°C (446°F) for a maximum time period of 5 seconds. Therefore, in a flow solder operation adjust the solder temperature and belt speed to conform to this specification, or as is specified on the device data sheet. The flow solder operation may now proceed in a normal fashion. For best results, any one single lead should be immersed in molten solder for as short a time period as possible. At a solder

temperature of 230°C (446°F), Sn60 solder will dissolve silver at the rate of 60 microinches per second. Therefore, with an initial silver plating thickness of 150 microinches, an immersion time of 2 seconds will provide the desired lead base metal-copper-silver-solder metallurgical system. At a solder temperature of 260°C (500°F), Sn60 solder will dissolve silver at the rate of 80 microinches per second. These dissolving rates decrease as the silver content increases in the molten solder bath.

Post cleaning of soldered assemblies when a type RMA or Type RA flux has been used may be accomplished via a vapor cleaning process in a degreasing tank, using an azeotrope of fluorocarbon F113 and alcohol as the cleaning agent. A recommended method is a 15 second suspension in vapors, a 15 to 30 second spray wash in liquid cleaner, and finally a one minute suspension in the vapors. When a water soluable Type AC flux such as Alpha 830 or Kester 1429/1429F is used, the following post cleaning process is suggested: thoroughly wash with water, neutralize using Alpha 2441 or Kester 5760 or Kester 5761 foaming, then thoroughly wash with water and air dry.

CAUTION: The use of tetrachloro-di-fluoroethane (F112), acetone, trichloroethylene, MEK, carbon tetrachloride and similar solvents as cleaning agents is NOT recommended, as these cleaners will attack or dissolve the epoxies used in optoelectronic devices.

A WORD ABOUT PRINTED CIRCUIT BOARDS

Printed circuit boards, either single sided, double sided or multilayer, may be manufactured with plated through holes with a metal trace pad surrounding the hole on both sides of the printed circuit board. The plated through hole is desirable to provide a sufficient surface for the solder to wet, and thereby be pulled up by capillary attraction along the lead through the hole to the top of the printed circuit board. This provides the best possible solder connection between the printed circuit board and the leads of the LED device.

SOLDERED LEADS

Figure 1 illustrates an ideally soldered lead. The amount of solder which has flowed to the top of the printed circuit board is not critical. A sound electrical and mechanical joint is formed.

Figure 2 illustrates a soldered lead which is undesirable.

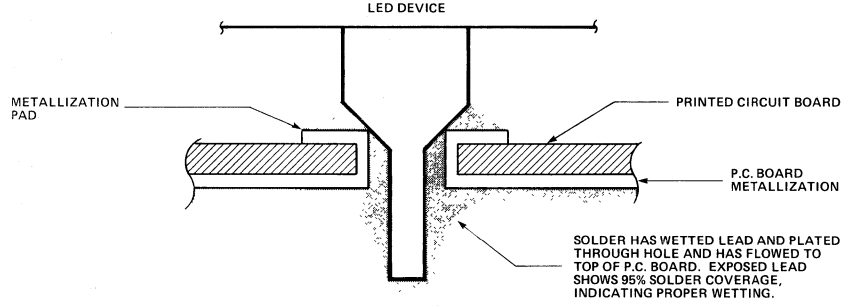


Figure 1. Ideally Soldered Lead

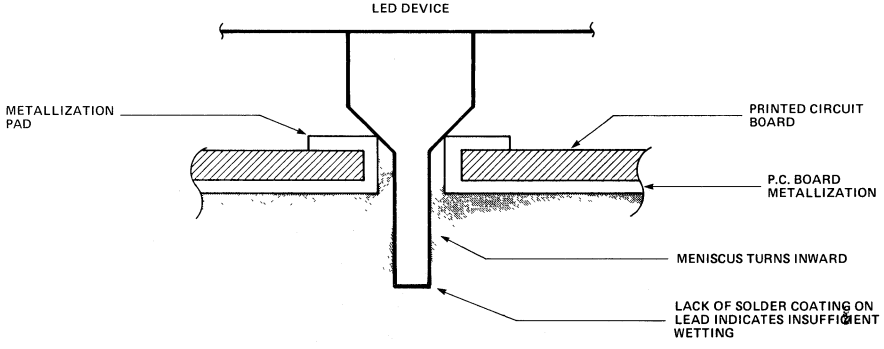


Figure 2. Undesirable Soldered Lead

LIST OF MANUFACTURERS

Alpha Metals, Inc.
56 G Water Street
Jersey City, New Jersey 07304
(302) 434-6778

London Chemical Co. (Lonco®)
240 G Foster
Bensenville, Illinois 60106
(312) 287-9477

E.I. DuPonte De Nemours & Co.
Freon Products Division
Wilminton, Delaware 19898
(302) 774-8341

Frank Curran Co. (Petroleum Napthalene Mothballs)
8101 South Lemont Road
Downers Grove, Illinois 60515
(312) 969-2200

Kester Solder Co.
4201 G Wrightwood Avenue
Chicago, Illinois 60639
(312) 235-1600

Allied Chemical Corporation
Speciality Chemicals Division
P.O. Box 1087R
Morristown, New Jersey 07960
(201) 455-5083

Baron-Blakeslee (Blaco-Tron)®
1620 S. Laramie Avenue
Chicago, Illinois 60650
(312) 656-7300

Imperial Chemical Industries, Ltd. (Arklone)®
Imperial Chemical House, Millbank
London SW1P3JF, England

REFERENCES

Manko, Howard H. *Solders and Soldering.* New York: McGraw-Hill, 1964.

Coombs, Clyde F. *Printed Circuits Handbook. New York: McGraw-Hill, 1964.*

Flaskerud, Paul and Rick Mann. "Silver Plated Lead Frames for Large Molded Packages," IEEE Catalog No. 74CH0839-1PHY (1974), pp. 211-222.

HEWLETT PACKARD

Application Bulletin 56

INTERFACE TIMING AND DISPLAY LENGTH EXPANSION INFORMATION FOR THE HDSP-2000 CODED DATA CONTROLLER

The HDSP-2000 CODED DATA CONTROLLER shown in Application Note 1001 is a versatile circuit and is easily modified to multiplex any display length. This Application Bulletin contains the key timing information and a detailed explanation of how the circuit operates. With this information, it should be a straightforward exercise to expand the display to any desired length. Included in this Application Bulletin are designs for 32, 64, and 128 character displays. The ASCII to 5x7 decoder table within the Motorola MCM6674 ROM has also been shown. This decoder table can be stored within a Bipolar PROM if faster speeds are required.

The circuit shown in Figure 2 shows a CODED DATA CONTROLLER designed for a 32 character HDSP-2000 alphanumeric display. The key waveforms shown in Figure 1, labeled ① ② , and ③ , are shown to simplify the analysis of this circuit. Label ① is the 1 MHz clock. Label ② is the output of 7404 pin 2 which is the inverted Q_D output of the 74197. Label ③ is the output of the 7404 pin 6 which is the ANDed output of $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393. The Motorola 6810 RAM stores 32 bytes of ASCII data which is continuously read, decoded, and displayed. The ASCII data from the RAM is decoded by the Motorola 6674 128 character ASCII decoder. The 6674 decoder has five column outputs which are gated to the Data Input of the display via a 74151 multiplexer. Strobing of the display is accomplished via the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 6674. As shown by waveform ② , the 74197 also enables seven clock cycles to be gated to the clock input of the display. The 74393 is a divide by 256 counter connected so that the five lowest order outputs select each of the 32 ASCII characters within the RAM. The three highest order outputs determine the relationship between load time and column on time. When $2Q_B = 2Q_C = 2Q_D = 1$ of the 74393, waveform ③ goes to a logical 1. The circuit then scans 32 characters from the RAM and serializes the column data by counting through each of the seven rows of the 6674 and gating the appropriate column of the display. During the seven counts when $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393 are not equal to a logical 1, the column data is displayed, as shown in waveform ④ . Since only one column can be on at a single moment, the highest possible column on time is 1/5 or 20%. Thus, the column on time of the display in Figure 2 is (20%) (7/8) or 17.5%.

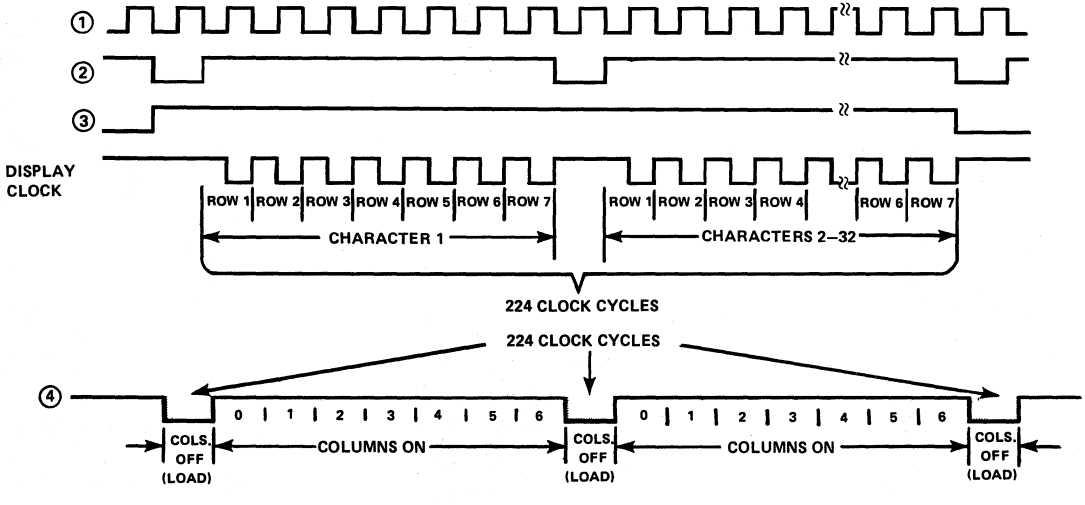


Figure 1. Timing Information for the 32 Character HDSP-2000 CODED DATA CONTROLLER

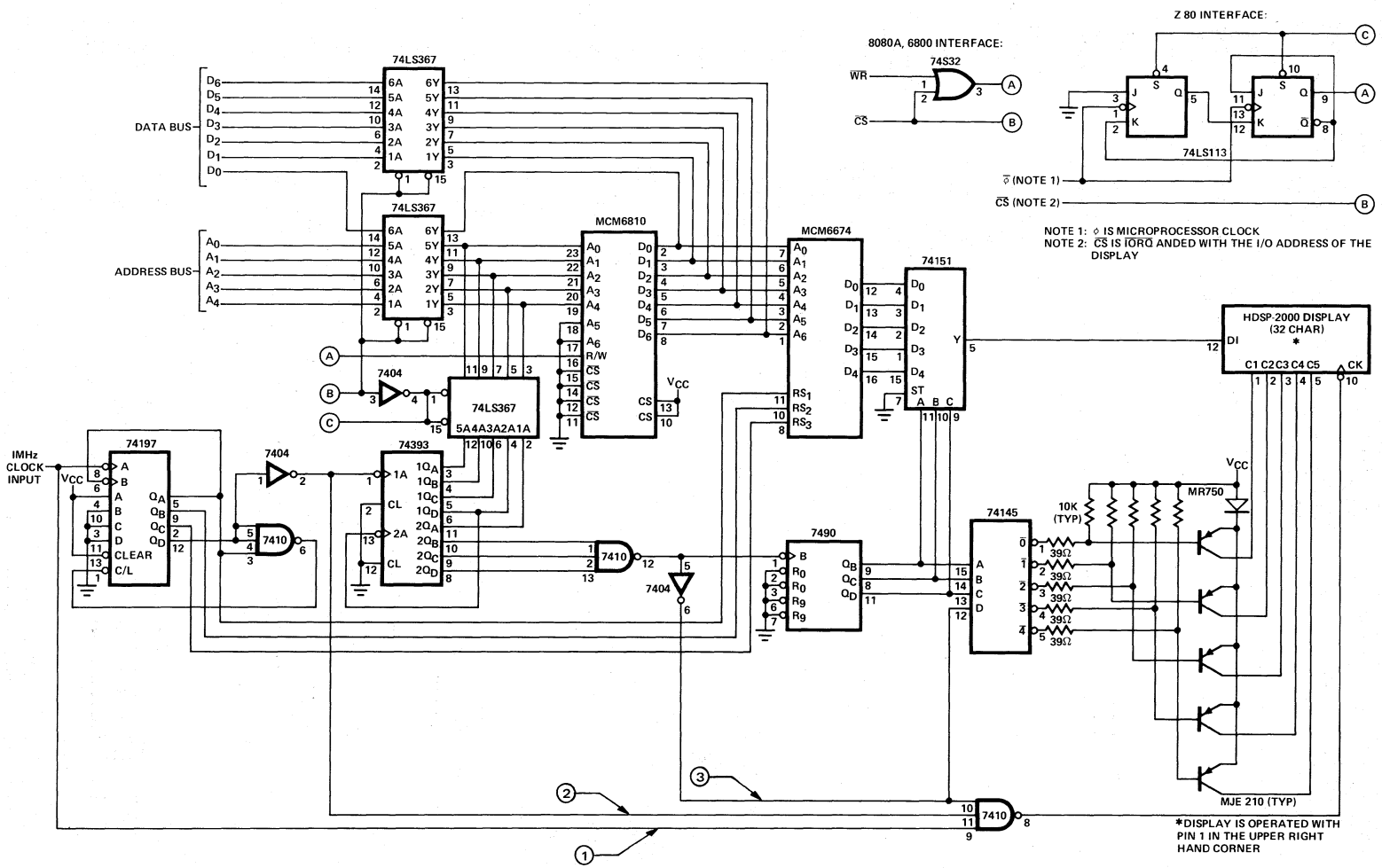


Figure 2. 6800, 8080A, and Z-80 Interface to the 32Character HDSP-2000 CODED DATA CONTROLLER

Changing the display length to 64 characters is a simple modification. This configuration can be easily realized by disconnecting $2Q_B$ of the 74393 from the 7410 and connecting it through the remaining tri-state buffer on the 74LS367 and using the 6810 RAM to store 64 ASCII characters. By leaving only $2Q_C$ and $2Q_D$ attached to the 7410, the column on time of the display is reduced from 17.5% to 15%. This reduction is caused because the relationship between actual column on time and theoretical column on time is 3/4 as opposed to 7/8 for the 32 characters. Since the display length has been doubled, the drive transistors must be upgraded to handle the higher column currents.

To implement a 128 character display, several modifications are needed. These changes are incorporated into the circuit in Figure 5. First, the input clock frequency has been increased to 2 MHz. This has been done to maintain a refresh rate of approximately 100 Hz for each digit, thus providing a flicker-free display. This higher speed of operation causes propagation delay problems within the MCM6674 (NMOS) whose maximum access time is 350ns. For this reason, the MCM6674 must be replaced by a faster Bipolar PROM. Refer to Figure 3 for a list of 1Kx8 PROMs that will function correctly in the circuit. From this list, the 82S2708 (maximum access time of 70ns) has been implemented. If this PROM is programmed with the code listed in Figure 4, it will decode a character font identical to the MCM6674. This same propagation delay problem is present with the MCM6810 RAM. Following worst case design procedures, the MCM68A10 1.5 MHz RAM should be used. To accommodate the additional address line made necessary by the display length expansion, the two 74LS367 tri-state buffers have been replaced with the 74LS244 octal version. Strobing of the display is accomplished using the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 82S2708. The 74393 is a divide by 256 counter connected so that the seven lowest outputs select each of the 128 ASCII characters within the RAM. The previously unused input A/output Q_A of the 7490 has been used as an additional divide by 2 counter. Thus, when the highest output of the 74393, $2Q_D$, and the Q_A output of the 7490 are NANDed through 7437, the basic relationship between load time and column on time is established. However, the external gating that has been added does affect the column on time slightly. Although these additional gates increase the total package count by one, they perform the necessary function of ensuring that the column drivers are turned off before the clock is gated to the display. This prevents noise from being generated on the clock of the display and eliminates erroneous display data. The resultant column on time is (23/32) (1/5) or 14.4%. The final modification made concerns the necessary column current needed to drive the display. Since the HDSP-2000 is rated at $I_{col(max)} = 410$ mA and there are 32 modules of four digits each, the transistors must source up to (32) (410 mA) or approximately 13A. Darlington PNP power transistors (2N6285) with the proper resistors have been used to accomplish this task.

Part Number	Manufacturer	Construction
7608	Harris	Bipolar — NiCr
3628-4	Intel	Bipolar — Si
82S2708	Signetics	Bipolar — NiCr
6381	Monolithic Memory	Bipolar — NiCr
6385	Monolithic Memory	Bipolar — NiCr
825228	National	Bipolar — TiW
93451	Fairchild	Bipolar — NiCr

Figure 3. 1Kx8 PROMs for Use in the HDSP-2000 CODED DATA CONTROLLER

PROM ADDRESS	HEXIDECIMAL DATA																
080	FF	FF	E4	E1	E8	FF	E0	EE	E4	E0	FF	E0	E4	E0	EE	EE	ROW 1
090	FF	EE	EE	EE	EE	E0	EE	E1	FF	E4	EE	EE	FF	FF	FF	FF	
0A0	E0	E4	EA	EA	E4	F8	E8	EC	E2	E8	E4	E0	E0	E0	E0	E0	
0B0	EE	E4	EE	EE	E2	FF	E6	FF	EE	EE	E0	EC	E2	E0	E8	EE	
0C0	EE	E4	FE	EE	FE	FF	FF	EF	F1	EE	E1	F1	F0	F1	F1	EE	
0D0	FE	EE	FE	EE	FF	F1	F1	F1	F1	FF	EE	E0	EE	E4	E0		
0E0	E6	E0	F0	E0	E1	E0	E2	ED	F0	E4	E1	F0	EC	E0	E0	E0	
0F0	F6	ED	E0	E0	E4	E0	E0	E0	E0	F1	E0	E2	E4	E8	E8	EA	
100	F1	F0	E4	E1	E4	F1	E1	F1	E8	E4	E0	E4	F5	E4	F1	F1	ROW 2
110	F1	F5	F1	F1	F5	E5	EA	E1	F1	E4	F1	F1	F5	F1	F1	F5	
120	E0	E4	EA	EA	EF	F9	F4	EC	E4	E4	F5	E4	E0	E0	E0	E1	
130	F1	EC	F1	F1	E6	F0	E8	E1	F1	F1	EC	EC	E4	E0	E4	F1	
140	F1	EA	E9	F1	E9	F0	F0	F0	F1	E4	E1	F2	F0	FB	F9	F1	
150	F1	F1	F1	F1	E4	F1	F1	F1	F1	F1	E1	E8	F0	E2	EA	E0	
160	E6	E0	F0	E0	E1	E0	E5	F3	F0	E0	E0	F0	E4	E0	E0	E0	
170	F9	F3	E0	E0	E4	E0	E0	E0	E0	F1	E0	E4	E4	E4	F5	F5	
180	F1	F0	E4	E1	E2	FB	E2	F1	FE	E2	E0	E4	EE	E8	FB	F1	ROW 3
190	F1	F5	F1	F1	F5	E2	EA	E1	EA	EE	F0	F1	F5	F1	F1	F5	
1A0	E0	E4	EA	FF	F4	E2	F4	E8	E8	E2	EE	E4	E0	E0	E0	E2	
1B0	F3	E4	E1	E1	EA	FE	F0	E2	F1	F1	EC	E0	E8	FF	E2	E1	
1C0	E1	F1	E9	F0	E9	F0	F0	F0	F1	E4	E1	F4	F0	F5	F5	F1	
1D0	F1	F1	F1	F0	E4	F1	F1	F1	EA	EA	E2	E8	E8	E2	F1	E0	
1E0	E4	EE	F6	EE	ED	EE	E4	F3	F6	EC	E1	F2	E4	FA	F6	EE	
1F0	F1	F1	F6	EF	FF	F1	F1	F1	F1	F1	FF	E4	E4	E4	E2	EA	
200	F1	F0	E4	E1	EF	F5	F4	FF	E9	FF	FF	F5	E4	FF	F5	F5	ROW 4
210	FF	F7	F7	FD	FD	F5	EA	FF	E4	EE	E8	FF	FD	FD	F7	F7	
220	E0	E4	E0	EA	EE	E4	E8	F0	E8	E2	FF	FF	EC	FF	E0	E4	
230	F5	E4	EE	E6	F2	E1	FE	E4	EE	EF	E0	EC	F0	E0	E1	E2	
240	ED	F1	EE	F0	E9	FC	FC	F3	FF	E4	E1	F8	F0	F5	F3	F1	
250	FE	F1	FE	EE	E4	F1	EA	F1	E4	E4	E4	E8	E4	E2	E0	E0	
260	E2	E1	F9	F1	F3	F1	EE	ED	F9	E4	E1	F4	E4	F5	F9	F1	
270	F9	F3	F9	F0	E4	F1	F1	F1	EA	EF	E2	E8	E0	E2	E0	F5	
280	F1	F0	E4	E1	E4	FB	F8	EA	E5	E2	E0	EE	F5	E8	FB	F1	ROW 5
290	F1	F1	F5	F5	F1	F8	EA	E1	EA	E4	E4	F1	F1	F5	F5	F1	
2A0	E0	E4	E0	FF	E5	E8	F5	E0	E8	E2	EE	E4	EC	E0	E0	E8	
2B0	F9	E4	F0	E1	FF	E1	F1	E8	F1	E1	EC	EC	E8	FF	E2	E4	
2C0	F5	FF	E9	F0	E9	F0	F0	F1	F1	E4	E1	F4	F0	F1	F1	F1	
2D0	F0	F5	F4	E1	E4	F1	EA	F5	EA	E4	E8	E8	E2	E2	E0	E0	
2E0	E0	EF	F1	F0	F1	FF	E4	E1	F1	E4	E1	F8	E4	F5	F1	F1	
2F0	F6	ED	F0	EE	E4	F1	F1	F5	E4	E1	E4	E4	E4	E4	E0	EA	
300	F1	F0	E4	E1	E2	F1	F0	EA	E1	E4	E0	E4	EE	E4	F1	F1	ROW 6
310	F1	F1	F5	F5	F1	F0	EA	E1	F1	E4	E0	F1	F1	F5	F5	F1	
320	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	
330	F1	E4	F0	F1	E2	F1	F1	F0	F1	E2	EC	E8	E4	E0	E4	E0	
340	F5	F1	E9	F1	E9	F0	F0	F1	F1	E4	F1	F2	F0	F1	F1	F1	
350	F0	F2	F2	F1	E4	F1	E4	FB	F1	E4	F0	E8	E1	E2	E0	E0	
360	E0	F1	F9	F1	F3	F0	E4	F1	F1	E4	F1	F4	E4	F5	F1	F1	
370	F0	E1	F0	E1	E5	F3	EA	F5	EA	F1	E8	E4	E4	E4	E0	F5	
380	FF	F0	FF	FF	E1	FF	E0	FB	E1	E0	FF	E0	E4	E0	EE	EE	ROW 7
390	FF	EE	EE	EE	EE	E0	FB	E1	FF	E4	E4	EE	FF	FF	FF	FF	
3A0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	F0	E0	EC	E0	
3B0	EE	EE	FF	EE	E2	EE	EE	F0	EE	EC	E0	F0	E2	E0	E8	E4	
3C0	EE	F1	FE	EE	FE	FF	F0	EF	F1	EE	EE	F1	FF	F1	F1	EE	
3D0	F0	ED	F1	EE	E4	EE	E4	F1	F1	E4	FF	EE	E0	EE	E0	FF	
3E0	E0	EF	F6	EE	ED	EE	E4	EE	F1	EE	EE	F2	EE	F5	F1	EE	
3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	

Figure 4. 82S2708 PROM Listing

APPLICATION NOTES

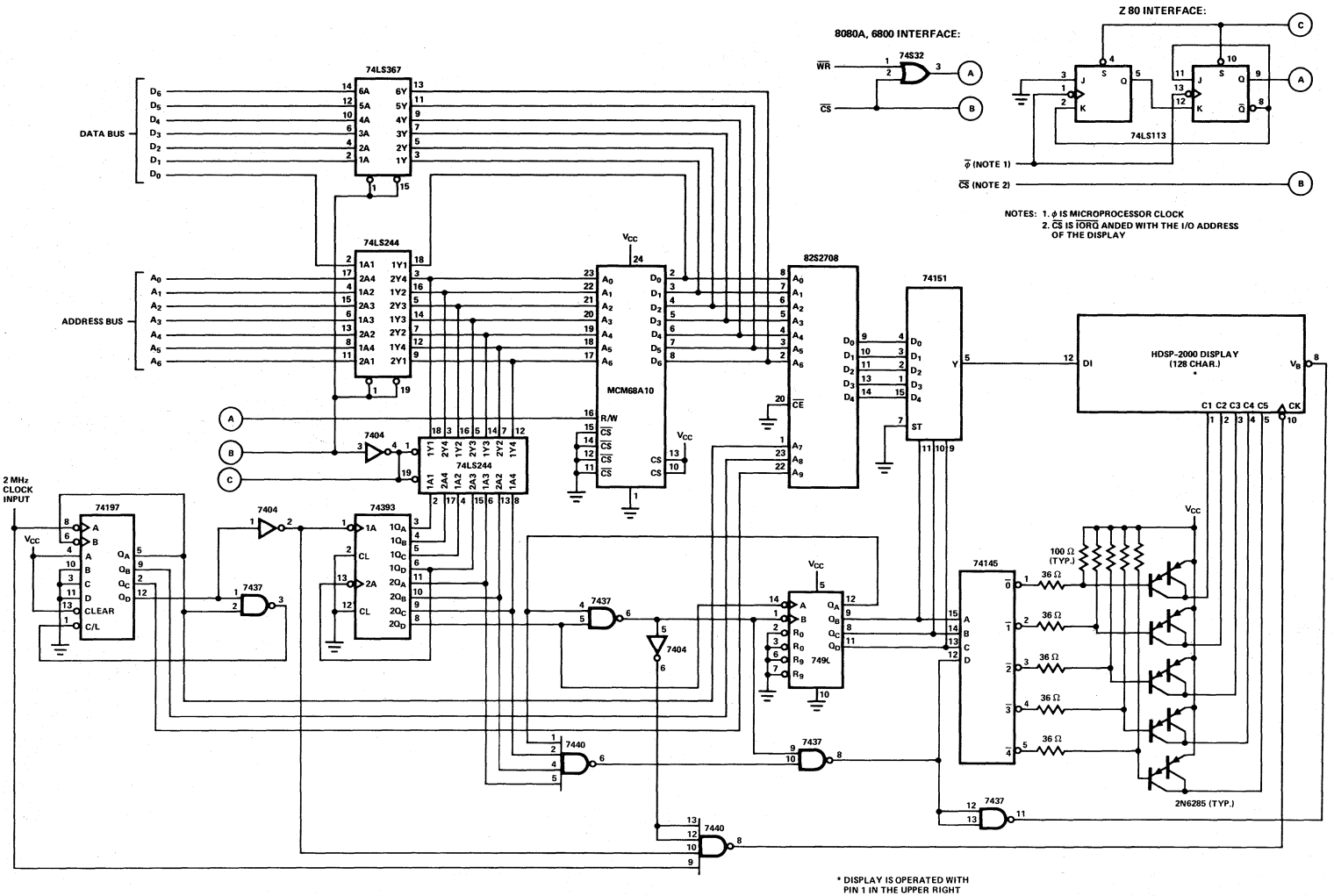


Figure 5. 6800, 8080A, and Z-80 Interface to the 128 Character HDSP-2000 CODED DATA CONTROLLER

HEWLETT PACKARD

APPLICATION BULLETIN 57

Flux Budget Considerations for Fiber Optic Link Design

This application bulletin is intended to supplement Application Note 1000. Basic information on flux budgeting with specific examples using the Hewlett-Packard HFBR-1002 Fiber Optic Transmitter, HFBR-2001 Fiber Optic Receiver, and HFBR-3000 Series Fiber Optic Cable/Connector Assemblies is presented.

To determine the performance of a fiber optic system, three main areas must be considered:

Transmitter Output Optical Flux
Receiver Input Sensitivity
System Insertion Losses

When designing a fiber optic system, an analysis that includes temperature, humidity, and voltage variations will require using the minimum transmitter output flux and corresponding minimum receiver input sensitivity to ensure the performance of the fiber optic system for the environmental conditions of the system.

Transmitter Output Optical Flux

The transmitter output optical flux, (ϕ_T), is usually expressed in microwatts (μW). For convenience in system calculations, the output flux can be expressed in dBm, allowing all system calculations to be algebraic summations.

When changing microwatts to dBm, the output optical flux is referenced to one milliwatt (1000μW).

$$\text{Transmitter Output Flux, } \phi_T(\text{dBm}) = 10 \log \frac{\phi_T(\mu W)}{\phi_O}$$

$$(\phi_O = 1000\mu W)$$

Receiver Input Sensitivity

The receiver input sensitivity is the minimum input flux that will produce a particular Bit Error Rate (BER) at a specified baud rate. The receiver sensitivity is a function of its internal noise and bandwidth. The receiver sensitivity, ϕ_R , may be expressed in microwatts or in dBm for convenience in system calculations.

$$\text{Receiver Input Sensitivity, } \phi_R(\text{dBm}) = 10 \log \frac{\phi_R(\mu W)}{\phi_O}$$

$$(\phi_O = 1000\mu W)$$

System Insertion Loss

The system insertion loss is defined as the total of all losses of optical flux in the transmission path. The losses at the connector interfaces are caused by reflections, differences in fiber diameter, N.A., and fiber alignment. The system insertion loss also includes losses in the fiber due to scattering and absorption. Each loss is subscripted to correspond to its location in the system and the loss is expressed in decibels. For a worst case design, values should be used taking temperature, humidity, etc. into account for the maximum loss.

A typical system insertion loss includes:

Transmitter to Cable/ Connector Assembly	— α_{TC} (dB)
Steady State Fiber Losses	— $\alpha_0 \cdot \ell$ (dB/km · length)
Cable/Connector Assembly to Receiver	— α_{CR} (dB)
Connector to Connector	— α_{CC} (dB)
Splice	— α_S (dB)
Directional Coupler	— α_{DC} (dB)
Star Coupler	— α_{SC} (dB)

Flux Budget

The flux budget calculation is a method of comparing the ratio of transmitter optical flux and receiver sensitivity to the total loss of the system.

The System Flux Ratio is the ratio of transmitter output flux to the receiver input sensitivity and is expressed in decibels.

$$\text{System Flux Ratio, } \alpha_{FR}(\text{dB}) = 10 \log \frac{\phi_T(\mu W)}{\phi_R(\mu W)}$$

If the transmitter output flux and receiver sensitivity are already expressed in dBm, the System Flux Ratio is merely the difference between ϕ_T and ϕ_R.

$$\text{System Flux Ratio, } \alpha_{FR}(\text{dB}) = \phi_T(\text{dBm}) - \phi_R(\text{dBm})$$

The System Insertion Loss, α_{SL}(dB), is then computed by summing the individual element losses in the transmission path.

$$\alpha_{SL}(\text{dB}) = \Sigma\alpha_i(\text{dB})$$

APPLICATION NOTES

For a system to work satisfactorily, the losses must not exceed the System Flux Ratio. The Flux Margin, α_M, is the difference between the System Flux Ratio, α_{FR}, and the System Insertion Loss, α_{SL}. For a system to operate, the flux margin must be greater than zero.

$$\alpha_M(dB) = \alpha_{FR}(dB) - \alpha_{SL}(dB)$$
$$\alpha_M(dB) > 0$$

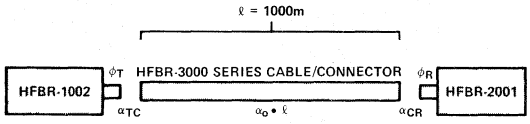
Some designs may require a specific flux margin to account for losses that may increase with time, or to "design-in" a safety margin.

Sample Flux Budget Calculation

DATA SHEET PARAMETERS			MIN	TYP	MAX	UNITS	NOTES
HFBR-1002 Transmitter	Output Optical Flux		50	100		μW	*
			−13	−10		dBm	
HFBR-2001 Receiver	Input Optical Sensitivity		0.8	0.5		μW	*
			−31	−33		dBm	
HFBR-3000 Series Cable/Connector	Insertion Loss	Length Dependent		7	10	dB/km	*λ = 820nm $\ell > 300$m
		Fixed		5.4	8.4	dB	*λ = 820nm $\ell \leq 300$m

*NOTE: Guaranteed specifications 0°C-70°C, ±5% Voltage, 10^{-9} BER @ 10 Mbaud.

A sample "flux budget" calculation is presented for a Hewlett-Packard 1000 metre point-to-point fiber optic system. The system uses a Hewlett-Packard HFBR-1002 Transmitter, HFBR-2001 Receiver, and an HFBR-3000 series 1000 metre Cable/Connector Assembly with no intermediate connector or splice.



1. System Flux Ratio

   The System Flux Ratio is the ratio of the transmitter output flux to the receiver input sensitivity.

   System Flux Ratio, α_{FR} =

   $$10 \log \frac{\phi_T(\mu W)}{\phi_R(\mu W)} = 10 \log \frac{50\mu W}{0.8\mu W} = 18dB$$

   OR $\alpha_{FR} = \phi_T(dBm) - \phi_R(dBm) = -13dBm - (-31dBm)$
   $= 18dB$

2. System Insertion Loss

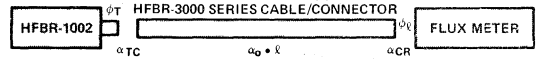
   $$\alpha_{SL} = \Sigma\alpha_i = \alpha_{TC} + \alpha_0 \cdot \ell + \alpha_{CR}$$

   The loss from the Transmitter to Cable, α_{TC}, is not directly measurable and is shown as a "typical" value on the HFBR-1002 data sheet.

   More easily measurable and convenient to state is a maximum insertion loss from the Transmitter to the end of a connectored cable of length, ℓ, called $\alpha_T\ell$, for use in system flux budgeting calculations. The insertion loss then includes α_{TC}, the loss of the cable, and α_{CR}. This approach is convenient for systems where the propagation characteristics of the cable have not reached a steady state, and values of both α_{TC} and α_0 are a function of the cable length.

The insertion loss $\alpha_T\ell$ may be easily expressed as the difference between two measurable quantities:

ϕ_T — Transmitter Output Flux
$\phi\ell$ — Flux Measured at the end of a cable of length, ℓ



$$\alpha_T\ell\ (dB) = \phi_T(dBm) - \phi\ell(dBm)$$

Using this measurement method, under worst-case conditions, the maximum insertion loss is 15.4dB for a Hewlett-Packard 1000 metre fiber optic system.

The System Insertion Loss can then be expressed as:

$$\alpha_{SL} = \alpha_T\ell = 15.4dB$$

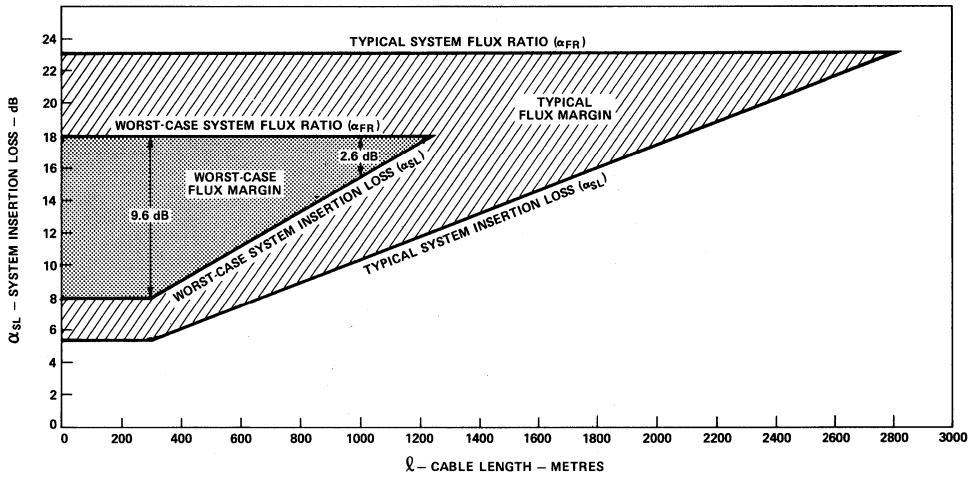
3. System Flux Margin

   Flux Margin, α_M, is the difference between the System Flux Ratio and the System Insertion Loss.

   Flux Margin = System Flux Ratio—System Insertion Loss

   $$\alpha_M = \alpha_{FR} - \alpha_{SL}$$
   $$\alpha_M = 18.0dB - 15.4dB$$
   $$\alpha_M = +2.6dB$$

   In this example, the Flux Margin, α_M, represents the worst case margin: 0–70°C, 10^{-9} BER @ 10Mbaud for a 1000 metre system.



Graphical Representation

The insertion loss for a Hewlett-Packard point-to-point system (using the HFBR-1002, HFBR-2001, and HFBR-3000 Series Cable/Connector) can be represented graphically. The graph is a convenience for readily determining the flux margin for systems less than 1000 metres and also is a guide for determining the flux margin available when splices, connectors, and couplers are a proposed part of a fiber optic system.

For the HFBR-1002 Transmitter and the HFBR-3000 series Cable/Connector Assembly steady state propagation occurs at distances greater than 300 metres from the transmitter. Therefore the system insertion loss for a Cable/Connector Assembly less than or equal to 300 metres is defined as a single insertion loss, α_F(dB). For lengths greater than 300 metres the system insertion loss is composed of two parts: 1) the fixed loss, α_F(dB), $\ell \leq 300$ metres; and 2) a length dependent loss, α_0(dB/Km), the linear cable attenuation, valid where optical flux is in equilibrium ($\ell > 300$m).

Two cases will be graphed, one using typical data sheet values, the second using worst case insertion losses.

1. Typical System Insertion Loss

$$\alpha_{SL} = \alpha_F \text{ (typ)} \quad , (\ell \leq 300\text{m})$$
$$\alpha_{SL} = 5.4\text{dB}$$

$$\alpha_{SL} = \alpha_F \text{ (typ)} + \alpha_o \text{ (typ)} \cdot (\ell - 300) \quad , (\ell > 300\text{m})$$
$$\alpha_{SL} = 5.4\text{dB} + 0.007 \text{ (dB/m)} \cdot [\ell \text{ (m)} - 300]$$

2. Typical Flux Ratio

$$\alpha_{FR} = 10 \log \frac{100\mu W}{0.5\mu W} = 23\text{dB}$$

3. Worst Case Insertion Loss

$$\alpha_{SL} = \alpha_F \text{ (max)}, (\ell \leq 300\text{m})$$
$$\alpha_{SL} = 8.4\text{dB}$$

$$\alpha_{SL} = \alpha_F \text{ (max)} + \alpha_o \text{ (max)} \cdot (\ell - 300) \quad , (\ell > 300\text{m})$$
$$\alpha_{SL} = 8.4\text{dB} + 0.010 \text{ (dB/m)} [\ell \text{ (m)} - 300]$$

4. Worst Case Flux Ratio

$$\alpha_{FR} = 10 \log \frac{50\mu W}{0.8\mu W} = 18\text{dB}$$

As shown on the graph, the Flux Margin is the number of dB between the System Flux Ratio line and the System Insertion Loss. Hewlett-Packard system performance (worst case*) guarantees a minimum Flux Margin at 1000 metres of 2.6dB, while typical performance is greater than 12dB. For a 300 metre system worst case Flux Margin is 9.6dB and typical performance is greater than 17dB.

As demonstrated by the graph, the H-P system can be expected to function at distances considerably beyond 1000 metres under *typical* operating conditions.

*0-70° C, 10^{-9} BER @ 10Mbaud

APPLICATION NOTES

HEWLETT PACKARD

APPLICATION NOTE 915

Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes

Traditionally, the detection and demodulation of extremely low level optical signals has been performed with multiplier phototubes. Because of this tradition, solid-state photodetectors are often overlooked even though they have a number of clear functional advantages and in some applications provide superior performance as well. Some of these advantages are summarized below and become even more apparent in the following discussion.

ADVANTAGES OF PIN PHOTODIODES VERSUS MULTIPLIER PHOTOTUBES

1. Size and weight:
   PIN photodiodes are approximately three orders of magnitude smaller and lighter. This greatly simplifies and reduces the cost of mounting.
2. Power Supply:
   Multiplier phototubes require more than 1000 volts, which must be precisely regulated and divided among the dynodes. By comparison, PIN photodiodes and associated amplifiers operate stably on less than 20 volts, which does not require precise regulation.
3. Cost:
   The cost, including that of the necessary amplifier, is lower for the PIN photodiode because of lower power supply requirements.
4. Spectral Response:
   Broad skirts of the PIN photodiode make it useful from the ultra-violet, through the visible, and well into the infrared region. This exceeds the range of any other device of comparable sensitivity.
5. Sensitivity:
   Noise equivalent power of the PIN photodiode is lower than that of any other type of photodetector. The signal levels are extremely low, however, and to achieve low level performance they require a high gain, high input resistance amplifier. Multiplier phototubes have built-in gain and do not require additional low-noise amplification. Moreover, the high input resistance needed for sensitive performance precludes fast response, whereas the response time of multiplier phototubes may be in the nanosecond region even in the sensitive mode.
6. Stability:
   The characteristics of noise, responsivity, and spectral response of the PIN photodiode are not dependent on time, temperature, or other environmental considerations. The same conditions may be hazardous to multiplier phototubes.
7. Overloading:
   In the presence of excessive signal, multiplier phototubes of comparable sensitivity are capable of destroying themselves as a result of excessive output current. The PIN photodiode is unaffected by exposure to room light or even direct sunlight.
8. Ruggedness:
   PIN photodiodes can tolerate exposure to extreme levels of shock and vibration. Typical shock capability is 1500 G's for 0.5 millisecond.
9. Magnetic Fields:
   Multiplier phototube gain is affected by fields as small as one gauss. If the interfering field is fluctuating, the output will be modulated by it. The PIN photodiode is insensitive to magnetic fields.
10. Precision:
    The responsivity of the PIN photodiode is inherently precise and repeatable. Within a given type, the characteristics agree (from unit to unit) within plus or minus 0.1 decade. Responsivity of multiplier phototubes may vary over more than a decade from one unit to another.
11. Sensitive Area:
    The small sensitive area of the PIN photodiode makes it unnecessary to establish an aperture which may be required for some applications. However, in some applications good optical alignment is imposed by the small area.

PIN PHOTODIODE DETECTORS

At the present time a variety of different types of solid-state photodetectors are available. Of these, the Silicon PIN Photodiode has the broadest applicability and is the subject of this note. The PIN photodiode's main advantages are: broad spectral response, a wide dynamic range, high speed, and extremely low noise. With appropriate terminal circuits it is well suited for many applications that require converting an optical signal to an electrical signal. The

present discussion, however, will be limited to the description of the PIN photodiode's threshold detection sensitivity and the design of suitable terminal circuits that will realize this capability.

PHOTODIODE DESCRIPTION

Construction

A brief description of the PIN photodiode will be helpful in understanding its performance and the principles for designing appropriate circuits to be used with it. Figure 1 shows a typical construction of the PIN photodiode. This figure is for the purpose of explanation only and is not to scale. The relative proportions have been deliberately distorted for the sake of clarity.

The PIN structure is produced by diffusion through an oxide (S_i0_2) mask which also serves to protect the surface. Since most metals are very opaque to optical radiation, especially at infrared wavelengths, the gold contact is deposited only around the perimeter of the P-layer, and the gold contact pattern provides for lead attachment a short distance away from the junction region, so the lead is not in the light path.

Mode of Operation

When a photon is absorbed by the silicon it produces a hole and an electron. If the absorption of the photon occurs in the I-layer, as shown in Figure 1, the hole and the electron are separated by the electric field in the I-layer. For the highest quantum conversion efficiency (electrons per photon) it is desirable to have the P-layer as thin as possible and the I-layer as thick as possible. The thickness of the P-layer also determines the value of the parasitic series resistance (R_S in Figure 2). The thinner the P-layer the higher the R_S. Since R_S affects high frequency performance there is therefore a design trade-off between quantum efficiency and bandwidth. Once the trade-off is settled, the desired thickness is then controlled during the diffusion process. The effective thickness of the I-layer is controlled partly by the manufacturing diffusion process and partly by the magnitude of the electric field applied to the diode—the higher the field, the thicker will be the effective I-layer. It is therefore desirable to operate the diode with an external reverse bias, as shown in Figure 2. As the reverse bias voltage is increased from zero, there are three beneficial effects: hole and electron transit time decreases; conversion efficiency increases slightly; and most importantly, the capacitance decreases sharply with bias up to about ten volts and continues to decrease slightly up to about twenty volts reverse bias.

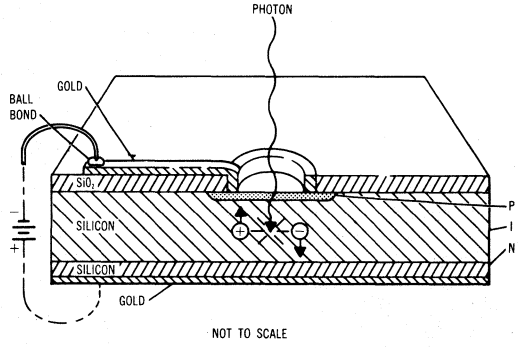


Figure 1. PIN Photodiode Cutaway View

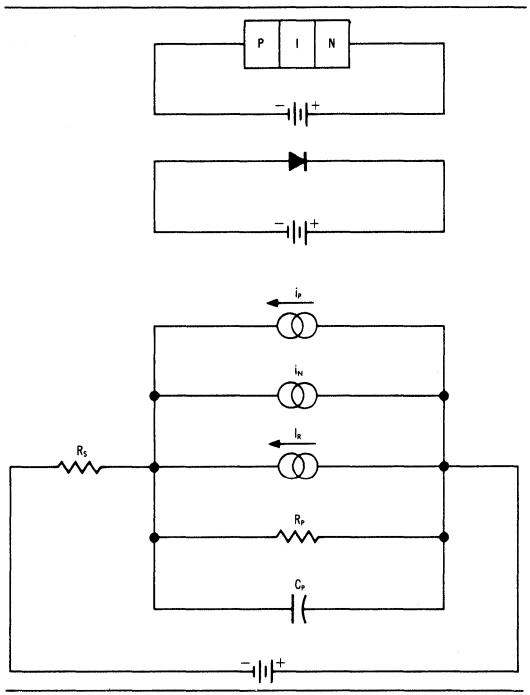


Figure 2. PIN Photodiode Schematic Symbol, and Equivalent Circuit

In the presence of optical signals there is a slight modulation of the shunt conductance as the presence of photon-produced holes and electrons in the I-layer modulate its conductivity. This effect can be quite significant at very high levels of illumination since the I-layer may become saturated, resulting in a decrease in quantum efficiency and an increase in rise time. Saturation can be prevented by applying a very high reverse bias voltage (up to 200 volts). However, such a high voltage, applied over a long period of time, may cause a degradation of the diode's leakage properties. Since our present concern is with threshold performance, reverse bias voltages greater than twenty volts need not be considered.

Equivalent Circuit

When properly biased, the PIN photodiode can be accurately represented by the equivalent circuit shown in Figure 2. Here i_p is the external current resulting when the diode is illuminated. It has a time constant of 10 picoseconds and a value of approximately 0.5 amp per watt of input at a wavelength of 8000 angstroms (800 nanometers). This corresponds to a quantum efficiency of 75%, that is, 0.75 electrons per photon. The quantum efficiency is constant from 500 nanometers to 800 nanometers (5,000 Å to 8,000 Å).

i_N is the noise current of the PIN photodiode. Since the diode is reverse biased, the shot noise formula is applicable, so that the noise current can be computed from:

$$\frac{i_N^2}{B} = 2qI_{dc} \qquad (1)$$

where B = system output bandwidth, Hz
q = electron charge, 1.6×10^{-19} coulombs
I_{dc} = dc current, Amp.

In the case of the photodiode, I_{dc} is simply the dark current, I_R, which has a value determined by the construction and dimensions of the particular diode type. Maximum values are: 100 picoamps for **5082-4204**, 150 picoamps for **5082-4205** and 2 nanoamps for **5082-4203**.

Shunt resistance, R_p, is very large, being usually greater than 10 gigaohms (10,000 megohms), and its noise current may therefore be neglected. Shunt capacitance, C_p, has a value from two to five picofarads, depending upon the diode type and reverse bias. For high frequency operation it is important to minimize C_p because the cutoff frequency is determined by:

$$f_c = \frac{1}{2\pi R_s C_p} \quad (2)$$

Although our present concern is with low frequency threshold operation, there is another reason for minimizing C_p. This will be discussed later, when circuit design principles are presented.

Performance

Threshold performance can and has been specified in a number of different ways. The most commonly understood and usable expression takes the form of a noise equivalent input signal. This is the input signal which produces an output signal level that is equal in value to the noise level that is present when no input signal is applied. The noise equivalent input in watts is called Noise Equivalent Power (NEP) and is defined by:

$$\text{NEP} = \frac{\text{NOISE CURRENT (amps per root hertz)}}{\text{CURRENT RESPONSIVITY (amps per watt)}} \quad (3)$$

which has the units of watts per root hertz. Devices for photo-detection could then be compared on the basis of NEP. The lower the NEP the more sensitive is the device.

Another method of defining threshold sensitivity is on the basis of signal-to-noise ratio for given input signal power levels. Taking a power level of one picowatt, for example, the signal-to-noise ratio at the output can be obtained from:

$$\text{SNR} = \frac{\text{RESPONSIVITY } \left(\frac{\text{amps}}{\text{watts}}\right) \times \text{INPUT (watts)}}{\text{NOISE CURRENT (amps)}} \quad (4)$$

This is a ratio of currents. To express it in dB we would take twenty times its log to base ten, even though the expression converts linearly to a power ratio. This is because the devices respond *linearly* to input *power*.

Figure 3 shows spectral sensitivity characteristics of several PIN photodiodes and multiplier phototubes. Sensitivity is given in terms of SNR and NEP. The latter is in terms of dBm. Several interesting features are evident in Figure 3. Although the quantum efficiency for PIN photodiodes is constant from 500 to 800 nanometers, the sensitivity curve is not. This is due to the fact that the energy per quantum (photon) of radiant energy varies with wavelength.

The curves for the three different PIN photodiodes also show the dependence of sensitivity on leakage current. Here the highest sensitivity is obtained with the **5082-4204** which has a maximum leakage current of 100 picoamps. Next is the **5082-4205** with 150 picoamps and finally the **5082-4203** with maximum leakage of 2 nanoamps. The three curves are in effect displaced by the magnitude of the noise current difference because quantum efficiency is equal for all. These curves also show the inherent broad response of PIN photodiodes with respect to multiplier phototubes. Therefore, the power responsivity of the PIN photodiode

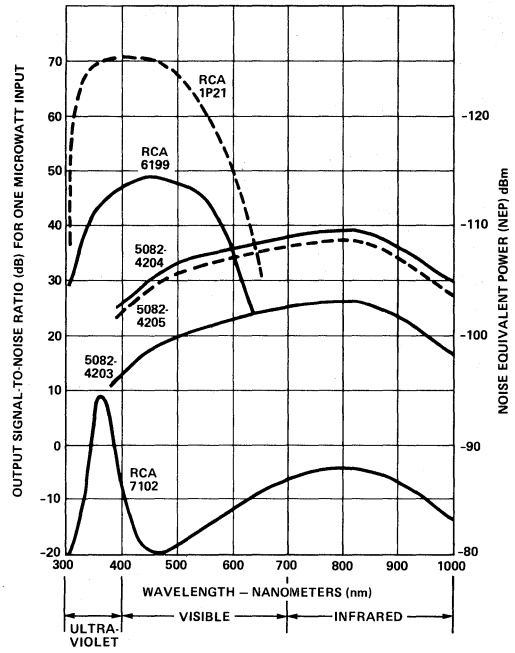


Figure 3. Spectral Sensitivity Comparisons of Photodetectors

has a corresponding slope. Notice how the inherently broad response of silicon, enhanced by the thick I-layer construction, extends the range of useful performance over the response ranges of two types of photocathodes.

Although the threshold sensitivity of multiplier phototubes is superior in the visible region, nevertheless for many applications the advantage is not significant enough to outweigh the disadvantages of generally unstable and temperature-sensitive gain, large size and weight, and the need of very high and stable power supply voltages. On the other hand, the superior red and infrared threshold performance of the PIN photodiode does not necessarily mean it is better in any application, because one must take into account its small sensitive area and low signal levels. Realization of the performance capability described in Figure 3 also requires fairly careful attention to the design of the terminal circuits into which the PIN photodiode operates.

TERMINAL CIRCUIT DESIGN PRINCIPLES

The design of the terminal amplifier must consider the usual design objectives of low noise, broad band, wide dynamic range, etc. In addition, there are two fundamental considerations which are dictated by the PIN photodiode:

1. High Reverse Voltage:
   The diode must be operated at ten to twenty volts of reverse bias to reduce shunt capacitance.
2. High Input Resistance:
   This is a fundamental consideration in the sensitivity/rise time trade-off.

The effects of reverse voltage on capacitance have been discussed earlier. However, the effect is sufficiently important to deserve a re-emphasis here.

A high input resistance is necessary in order to maintain a high signal-to-noise ratio. Since the output signal from the photodiode is a current, and its own internal noise is repre-

sented by a current, it is appropriate to represent the noise of the terminal amplifier as an equivalent noise current at the input. The smallest value of resistor which may be connected to the input is then limited by its noise current according to the formula for thermal noise:

$$\frac{i_N^2\ (\text{thermal})}{B} = \frac{4kT}{R} \qquad (5)$$

By comparing eq(1), relating diode noise current to leakage current, with eq(5), relating resistor noise current to its resistance value, it is clear that there is some value of resistance below which the NEP of the system, i.e., threshold sensitivity, would be degraded at the rate of 5 dB per decade of decreasing resistance. For example, in the case of the 5082-4203, assuming a maximum leakage current of 2 nanoamps, the value of resistance should be greater than 25 megohms, to avoid degrading the threshold sensitivity.

TRANSISTOR AMPLIFIER

In addition to keeping the input noise current low by using large values of input resistance, it is also important to keep other sources of noise in the amplifier at a minimum. Using ordinary transistors (PNP or NPN) it is not possible to approach the ultimate sensitivity of which the PIN photodiode alone is capable, even when low-noise transistors, such as the 2N2484, are used. However, in those applications where it is possible to sacrifice sensitivity for simplicity, transistors may be used. A typical transistor circuit is shown in Figure 4. With this circuit, a sensitivity corresponding to an NEP of — 95 dBm was obtained. In this case, Q1 was operated at the lowest possible collector current which would still give adequate gain. A high loop gain was desired in order to compensate, with negative feedback, for the long open-loop rise time produced by the high input resistance. A resistance higher than 10 megohms was not necessary here, since the transistor itself sets the fundamental noise limitation. A PNP transistor was selected for Q2 in order to balance out most of the base-to-emitter voltage of Q1, so that the output would tend to be near zero without any zero adjustment. A slight zero adjustment, provided by R2 and R3, gives the necessary range without appreciably attenuating the feedback current. As the photocurrent, I_2, increases, the amplifier causes the voltage at the emitter of Q3 to decrease, which causes a current in R1 to flow out of the node (base of Q1) into which I_2 flows.

Basic Amplifier Arrangements

For linear operation, the photodiode should be operated with as small a load resistance as possible. Figure 5 shows the recommended amplifier arrangement. The negative-going input is at virtual ground; the dynamic resistance seen there by the photodiode is R_1 divided by loop gain. If the op-amp has extremely high input resistance, loop gain is very nearly the forward gain of the op-amp. R_2 can be omitted if the photocurrent is reasonably high — its purpose is only to balance off the effect of offset current. As shown, the output voltage will rise in response to the optical signal. If it is preferable to have the output drop in response to optical input, then *both* the photodiode *and* E_C should be reversed. E_C may, of course, be zero. Speed of response is usually limited by the time constant of R_1 with its own capacitance, so it is improved by using a string of two or more resistors in place of a single R_1.

Logarithmic operation requires the highest possible load resistance — at least 10GΩ. With an FET-input op-amp, this is

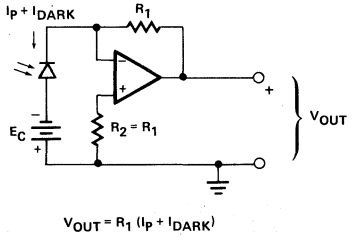
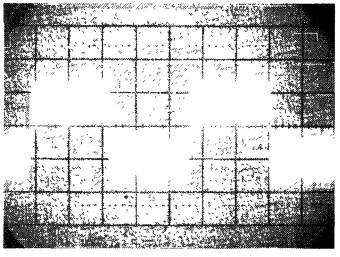
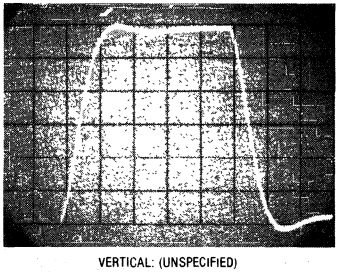


Figure 5. Linear Response; Photodiode and Amplifier Circuit Arrangement



400 uV/cm x 1 msec/cm



VERTICAL: (UNSPECIFIED)
HORIZONTAL: 20 usec/cm

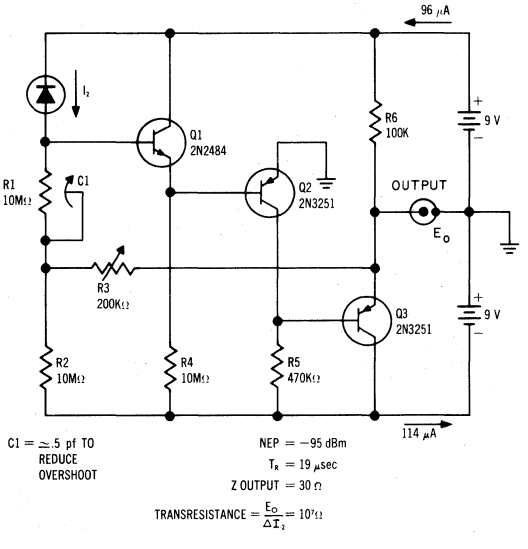
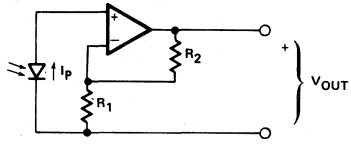


Figure 4. Transistor Photodiode Amplifier Schematic

easily achieved as in Figure 6. If the offset current of the amplifier poses a problem, a resistor can be added between the positive- and negative-going inputs. Its value should not be less than 10GΩ divided by loop gain. If the amplifier has a very high input resistance, loop gain is equal to the forward gain of the amplifier divided by $(1 + R_2/R_1)$ so making $R_2 = 0$ allows the smallest possible resistance between the inputs. The speed of response of this amplifier will be very low, with a time constant $\tau \approx 0.1$s. If high speed logarithmic operation is required, it is best to use the linear amplifier of Figure 5 followed by a logarithmic converter.



$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \frac{kT}{q} \log_\epsilon \left(1 + \frac{I_P}{I_S}\right)$$

$$\frac{kT}{q} \approx 25\ mV$$

$$I_S = \frac{I_F}{\epsilon^{\frac{qV}{kT}} - 1} \quad AT \quad 0 < I_F < 0.1\ mA$$

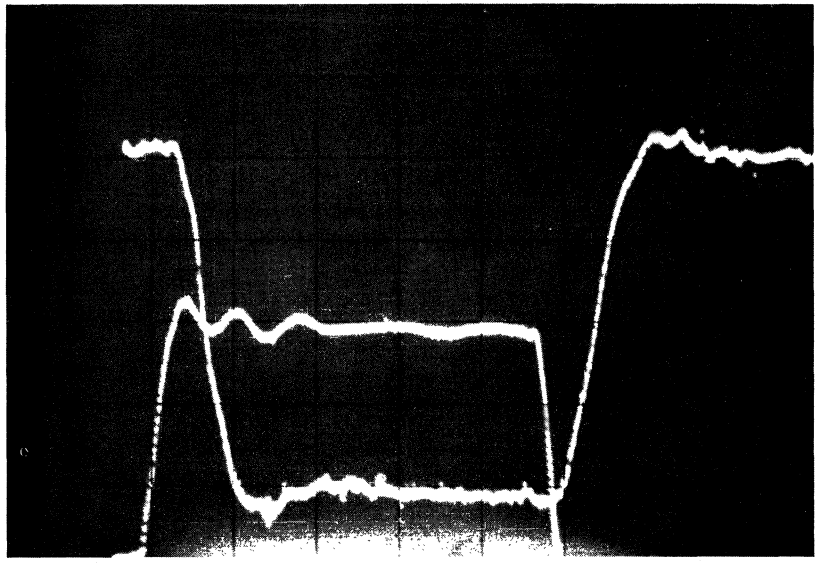
Figure 6. Logarithmic Response; Photodiode and Amplifier Circuit Arrangement

High Speed Photodiode Amplifier

Applications that call for high speed data signaling, such as CRT light pens, require amplifiers that have a wider bandwidth than the circuit shown in Figure 5.

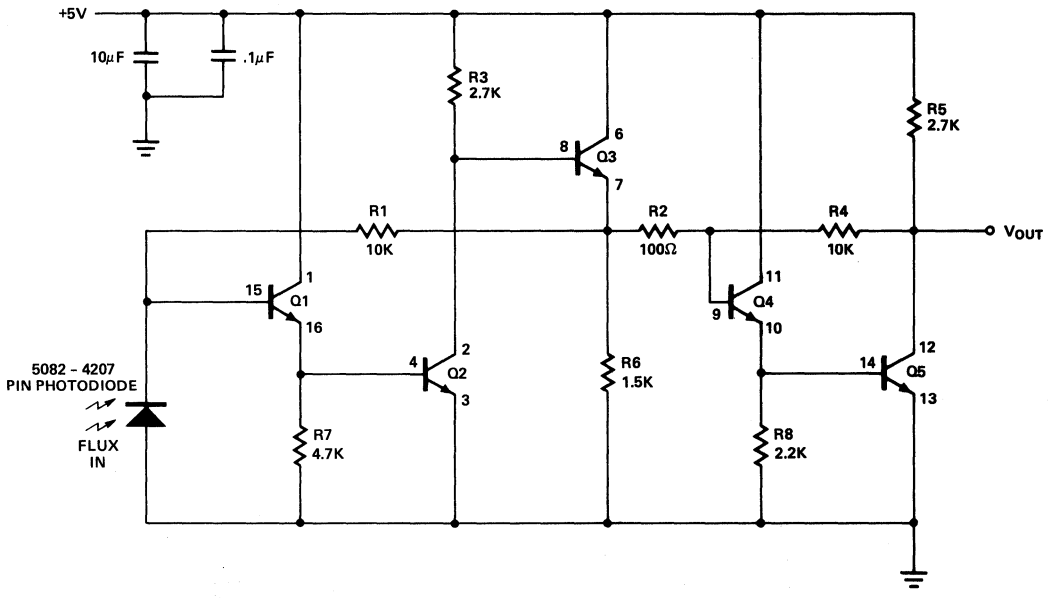
Using a five transistor array (RCA CA3127E) it is possible to construct a high speed, high gain photodiode amplifier. This circuit is shown in Figure 8. It is configured as a two stage amplifier. The first stage is composed of transistors Q1-Q3, where Q1 is an input emitter follower with feedback obtained from the emitter of Q3. Q2 functions as an inverting amplifier interconnecting Q1 to Q3. The second stage consists of Q4 and Q5 which provide additional gain and output buffering, of the first stage. These two stages provide an equivalent transresistance of 420K ohms. This means that the output voltage Vo is equal to the photocurrent, Ip, times 420K ohms.

When high speed circuit layout techniques are used it is possible to obtain the rise and fall time performance shown in Figure 7. This speed is equivalent to a bandwidth of 9.5MHz with an input flux of 1.9μW. This flux level can be obtained from a HEMT-6000 700nm High Intensity Subminiature Emitter when it is operated at 10mA, at a distance of 1cm from the 5082-4207 PIN photodiode.



VOLTAGE ACROSS HEMT-6000 EMITTER
t_r = 37ns t_f = 24ns $V_{O(DC)}$ = 1.7V

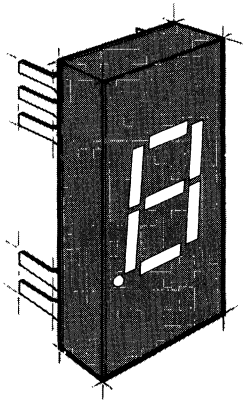
Figure 7. Pulse Response of Photodiode Amplifier

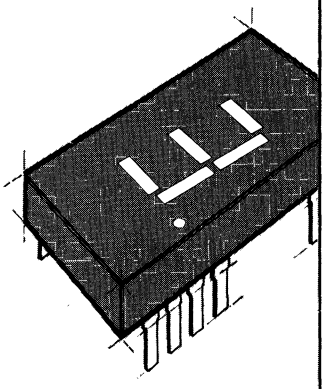


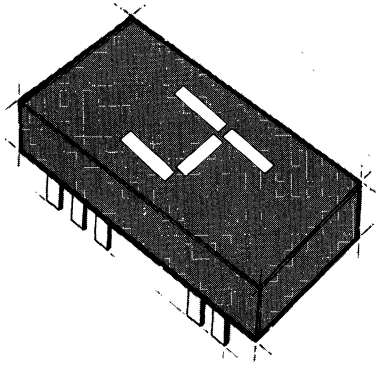
NOTES: TRANSISTORS ARE SINGLE PACKAGE, CA3127E. PINS LABELED FOR EACH. PIN 5 IS SUBSTRATE.

Figure 8. High Speed, High Gain Photodiode Amplifier

Application Note 941







5082-7700 Series Seven Segment LED Display Applications

5082-7700 Series
Seven Segment LED Display Applications

INTRODUCTION

The HP 5082-7700 series of LED displays are available in both common anode and common cathode configurations.. The large 0.3" high character size generates a bright, continuously uniform seven segment display of both numeric and selected alphabetic information.

Designed for viewing distances of up to 10 feet, these single digit displays have been engineered to provide a high contrast ratio and a wide viewing angle.

The 7700 series utilizes a standard 0.3" dual-in-line package configuration that allows for easy mounting on PC boards or in standard IC sockets. Requiring a forward voltage of only 1.7 volts, the displays are inherently IC compatible, allowing for easy integration into electronic systems.

The 5082-7730 and the 5082-7731 are common anode displays employing a left hand or a right hand decimal point respectively. Typical applications would be found in electronic instrumentation, computer systems, and business machines. The 5082-7740 is the common cathode version featuring a right hand decimal point for applications that include electronic calculators and business terminals such as credit card verifiers.

This Application Note begins with DC drive techniques and circuits. Next is an explanation of the strobe drive technique and the resultant increase in device efficiency. This is followed by general strobing circuits and some typical applications such as clocks, calculators and counters.

Finally, information is presented on general operating conditions, including intensity uniformity, light output control as a function of ambient, contrast enhancement and device mounting.

DC DRIVE

In DC or non-strobed drive the display is operated with each character continuously illuminated, usually with one decoder per character. This technique is commonly used for short character strings where the cost of the decoders for DC drive is less than that for the timing and drive circuits for strobed operation. The LEDs are more efficient when strobed; however, in DC operation the drivers need not handle high current levels. The DC drive circuit for the common anode display is shown in Figure 1a. The current level, set here at 20mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_{LED} - V_{CE}}{I_{SEGMENT}}$$

where V_{CC} = voltage supply potential,
V_{LED} = forward voltage of LED at $I_{SEGMENT}$
V_{CE} = "ON" voltage of segment switch.

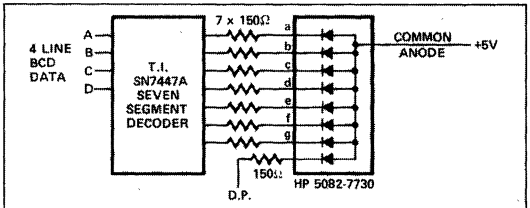


Figure 1a. Direct Drive Circuit for the 5082-7730/7731 Common Anode Display.

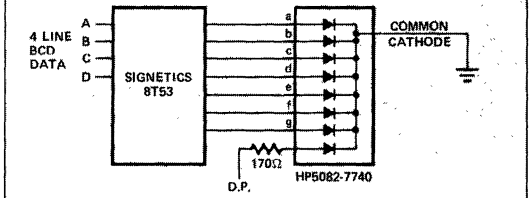


Figure 1b. Direct Drive Circuit for the 5082-7740 Common Cathode Display.

An analogous circuit is shown in Figure 1b for a common cathode DC drive system utilizing a current sourcing decoder/driver instead of a standard decoder/driver and external resistors.

See Table I for a list and comparative ratings of some of the commercially available seven segment decoder/driver circuits.

STROBING DRIVE CIRCUITS

In strobing, the decoder is timeshared among the digits in the display, which are illuminated one at a time. The digits are electrically connected with like segments wired in parallel. This forms an 8 (7 segments and decimal point) x N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. At the same time a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position.

Since the eye is a relatively slow sensor, a viewer will perceive as continuous a repetitive visual phenomena which occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read. In displays subject to vibration, a minimum strobe rate of 5 times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than DC drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 2a). Thus, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output (see Figure 2b). For example, from

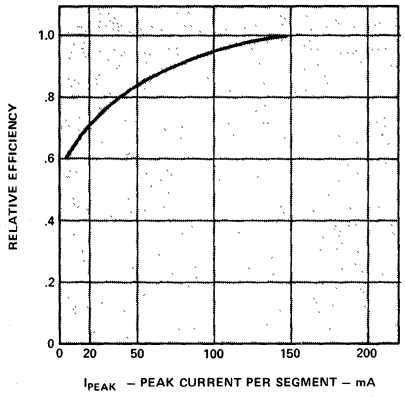


Figure 2a. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

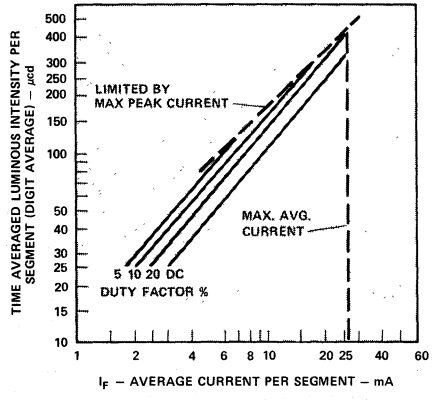


Figure 2b. Typical Time Averaged Luminous Intensity per Segment versus Average Current.

Figure 2b, a typical device operated at 10mA DC would produce a luminous intensity of approximately 120 microcandelas. The same device operated at 50mA peak, 20% duty cycle (as if in a 5 digit strobed display) will produce approximately 145 mcd time averaged luminous intensity.

For common decoder/driver circuits, a series resistor is placed in each segment enable line to limit the light emitting diode current. They are placed in the segment enable lines to prevent uneven current distribution among segments, commonly referred to as "current hogging". The resistive current limiting approach for LEDs outlined above is compact and easy to implement. However, the resistor consumes power.

Various techniques for driving LED displays from energy storage devices (such as inductors or capacitors) are quite practical though generally somewhat higher in cost and bulkier. However, power savings of as much as 50% over the resistive drive techniques are attainable. SCR switches may be attractive in circuits utilizing energy storage devices.

Figures 3 and 4 illustrate two possible memory buffer and display drive techniques used in strobed applications. Both memory techniques assume a bit-parallel/character-serial data entry format. If the system memory is available to supply data to the decoder, the buffer portion of these circuits may be deleted.

Figure 3 depicts a 5-digit strobed display employing a recirculating shift register memory. One shift register is used for each bit of the 4-bit BCD code. Four lines of data from the shift registers drive an SN7447A seven-segment decoder. The value of the current limiting resistors is calculated to provide 40mA per segment peak drive current. The resistor value may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{LED} - V_{CE1} - V_{CE2}}{N\, I_{AVE}}$$

where V_{CC} = voltage supply potential, V_{LED} = forward voltage of LED at peak $I_{SEGMENT}$ ($N\, I_{AVE}$), V_{CE1} = "ON" voltage of segment switch at peak $I_{SEGMENT}$, V_{CE2} = "ON" voltage of digit switch at 8 times peak $I_{SEGMENT}$, I_{AVE} = desired average operating current per segment, and N = number of digits in the display.

Data for each digit of the display is sequentially shifted to the QE output of the shift register by the display scan clock. The scan clock also drives an SN7496 shift register set up as a ripple scanner. The scan shift register outputs are buffered to source the 320mA peak digit current. Data entry to the storage registers is controlled by the system clock of the data source. During data entry, the display is blanked and the scan shift register is reset to the

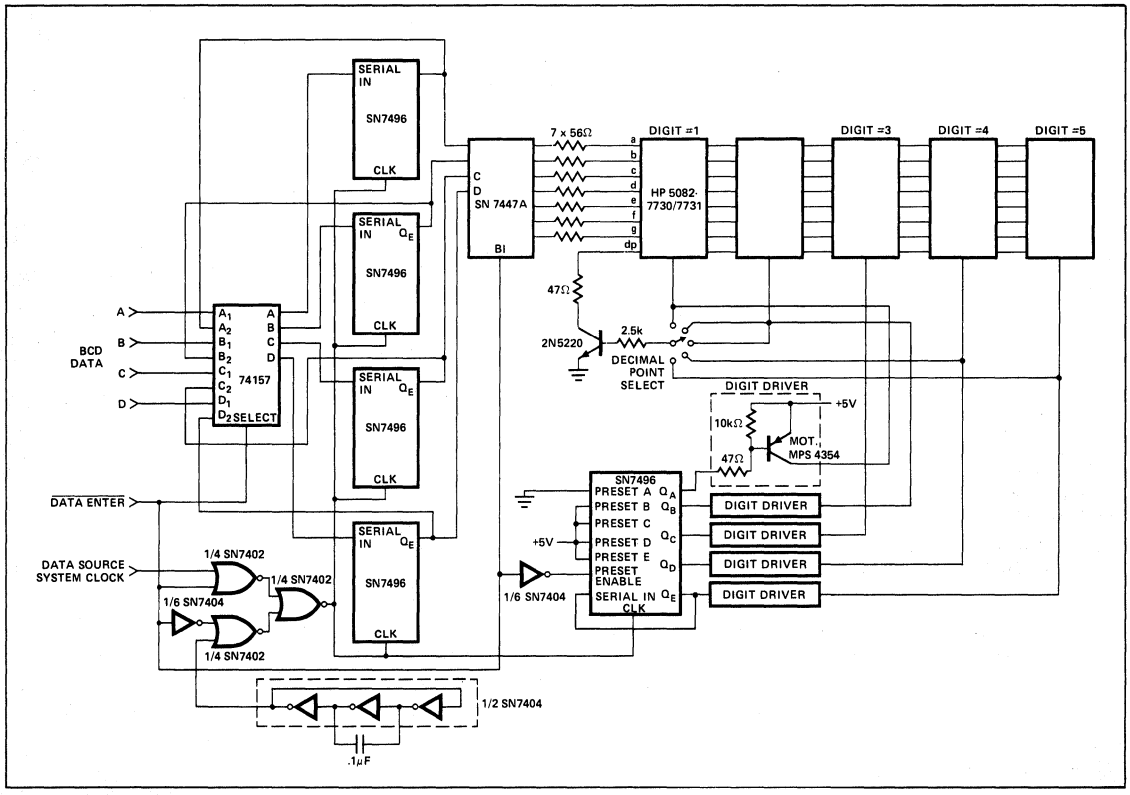


Figure 3. Five Digit Strobed Display with Recirculating Shift Register Memory.

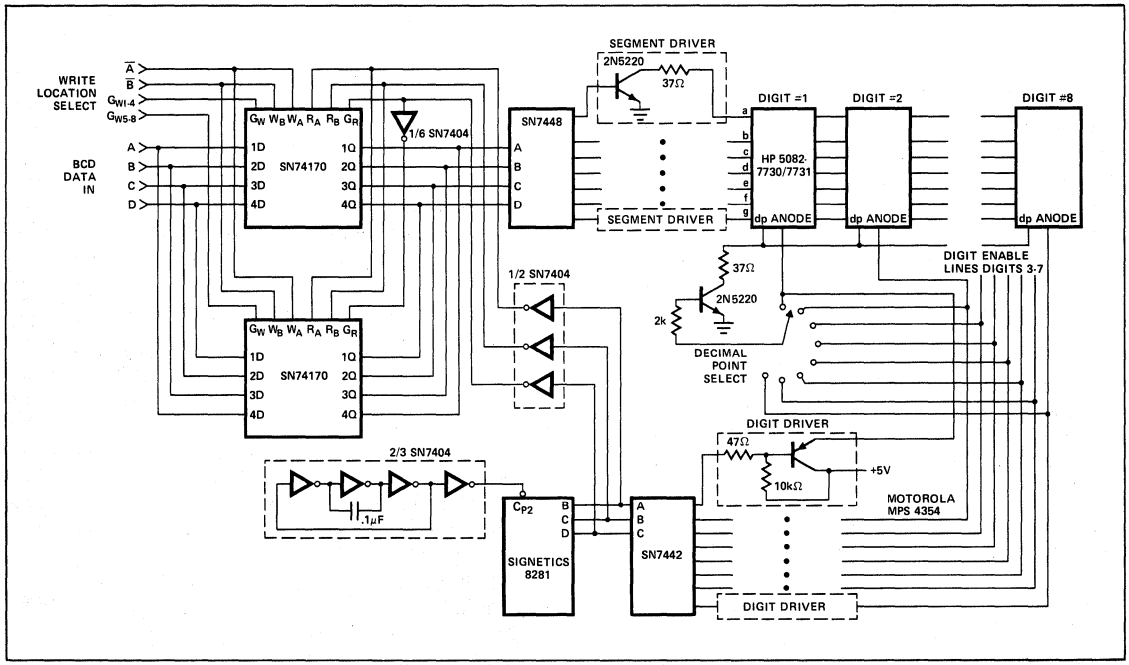


Figure 4. Strobed Eight Digit Common Anode Display with Static Memory Buffer.

first digit position by a logic "0" at $\overline{\text{DATA ENTER}}$. The DATA SOURCE SYSTEM CLOCK and the external BCD lines are also enabled by $\overline{\text{DATA ENTER}}$. The 5 digits of new data will be entered into the shift registers on each positive transition of the system clock. After data entry, $\overline{\text{DATA ENTER}}$ is returned to a high state, and scanning begins at position "A" under control of the SCAN CLOCK.

Figure 4 depicts an eight digit strobed display employing a static 4 x 8 bit memory. Data from the memory buffer is selected by the read lines under the control of the scan counter. This data is decoded by an SN7448 to drive the display segment lines. In this case the 80mA per segment peak current is beyond the current sinking capability of any common decoder/driver so an output buffer transistor must be used. Current limiting resistor values are calculated as before. The digit scan counter uses a Signetics 8281 binary counter in the divide by 8 mode. Data entry to the memory buffer can occur simultaneously with data read and any one of the eight digits may be selected or written independently.

The display length illustrated in either of the above schemes may be changed by simply providing the additional memory requirements and extending the capacity of the digit scanner. Displays of up to 16 digits are practical.

Numerous manufacturers are now supplying transistor arrays and buffer drivers which offer the advantages of lower costs and improved packing densities over discrete segment and digit drivers. See Table II for a list of some of the presently available products. See Table III for other useful display circuits.

CALCULATORS

The display circuit for a 10-digit calculator is given in Figure 5. A MOSTEK MK5010P single chip calculator circuit provides the calculating, decoding, and timing for a four function (+, −, x, ÷), 10-digit calculator. The displays are strobed at 100mA peak on a 1 of 10 duty cycle. The Darlington segment drivers source 100mA while the digit drivers sink 800mA peak. The MOS output transistor connecting the output to V_{SS} is "OFF" when the segment (or digit) is to be activated. In this state, the pull-down resistor connected to V_{GG} sinks the current necessary to turn on the PNP drive stage. When the MOS transistor is "ON", the 1mA output current through the pull-down resistor biases the PNP drive stage "OFF".

There are a variety of calculator chips for 8, 10, and 12-digit applications with varying voltage supply requirements and features. These include circuits from companies such as AMI, Cal-Tex, MOSTEK, NORTEC, Rockwell Int'l., and TI. Output stages vary although the P-channel, open-drain approach used in the MK5010P example is the most common.

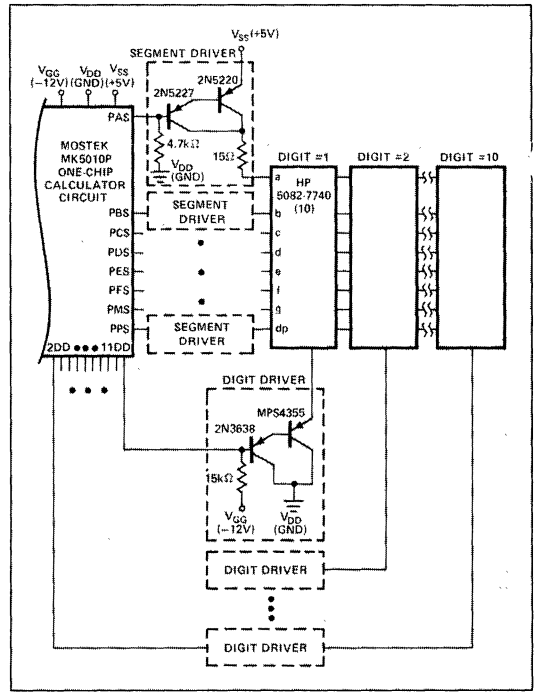


Figure 5. Typical Single Chip Calculator Circuit.

CLOCKS

Figures 6 and 7 depict the complete circuitry for 6-character digital clocks using monolithic clock chips from two different manufacturers. Both clocks use the 60Hz AC line as a time base and derive power from unregulated bridge rectifier power supplies.

Figure 6 illustrates a 6-digit clock circuit using the National Semiconductor NM5314 clock chip. This chip uses a strobed technique with all scanning logic and memory buffers on board. Scan frequency is established by an external RC network and should be maintained between 60Hz and 10kHz. The values shown should generate approximately a 1kHz scan rate. Each of the P-channel MOS outputs is buffered to provide adequate drive current to the individual segment and digit enable lines.

Figure 7 illustrates a 6 digit clock radio circuit using the MOSTEK MK5010PAN clock chip and HP 5082-7740 common cathode displays. Since the MK5010P series chips provide a 12.85% duty cycle digit enable, the component values shown will supply approximately 10mA average or 77mA peak current to each segment of the strobed display. The base inputs of the MPSA-13 segment drivers and the MPSU 45 digit drivers each have series current limiting resistors and pull-down resistors to limit maximum drain current and assure cut-off in the "OFF" state. In this circuit, the digit drive lines are multiplexed to accept input data for alarm set, time set, and other functions.

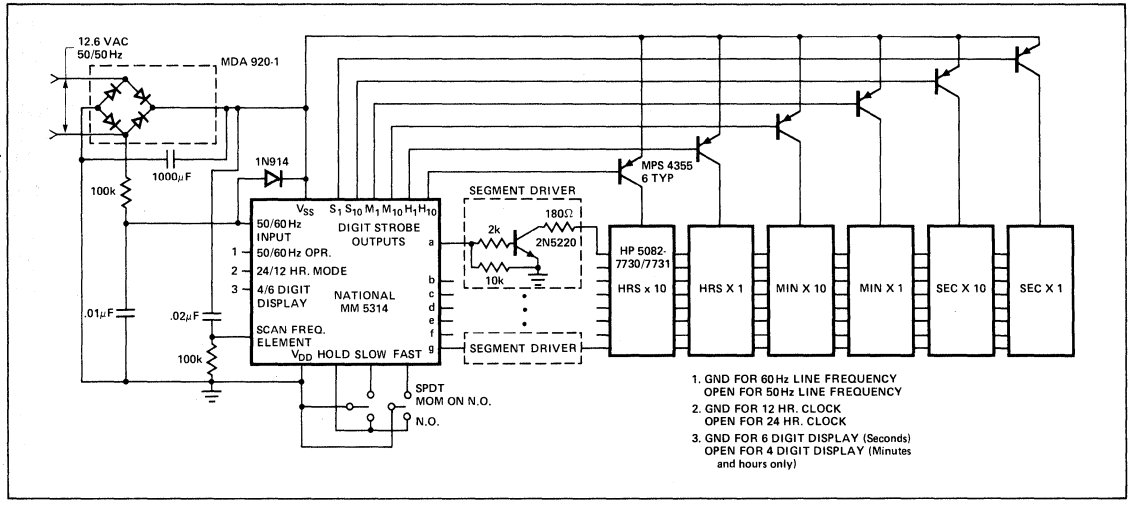


Figure 6. Strobed Drive for a Six Digit Clock.

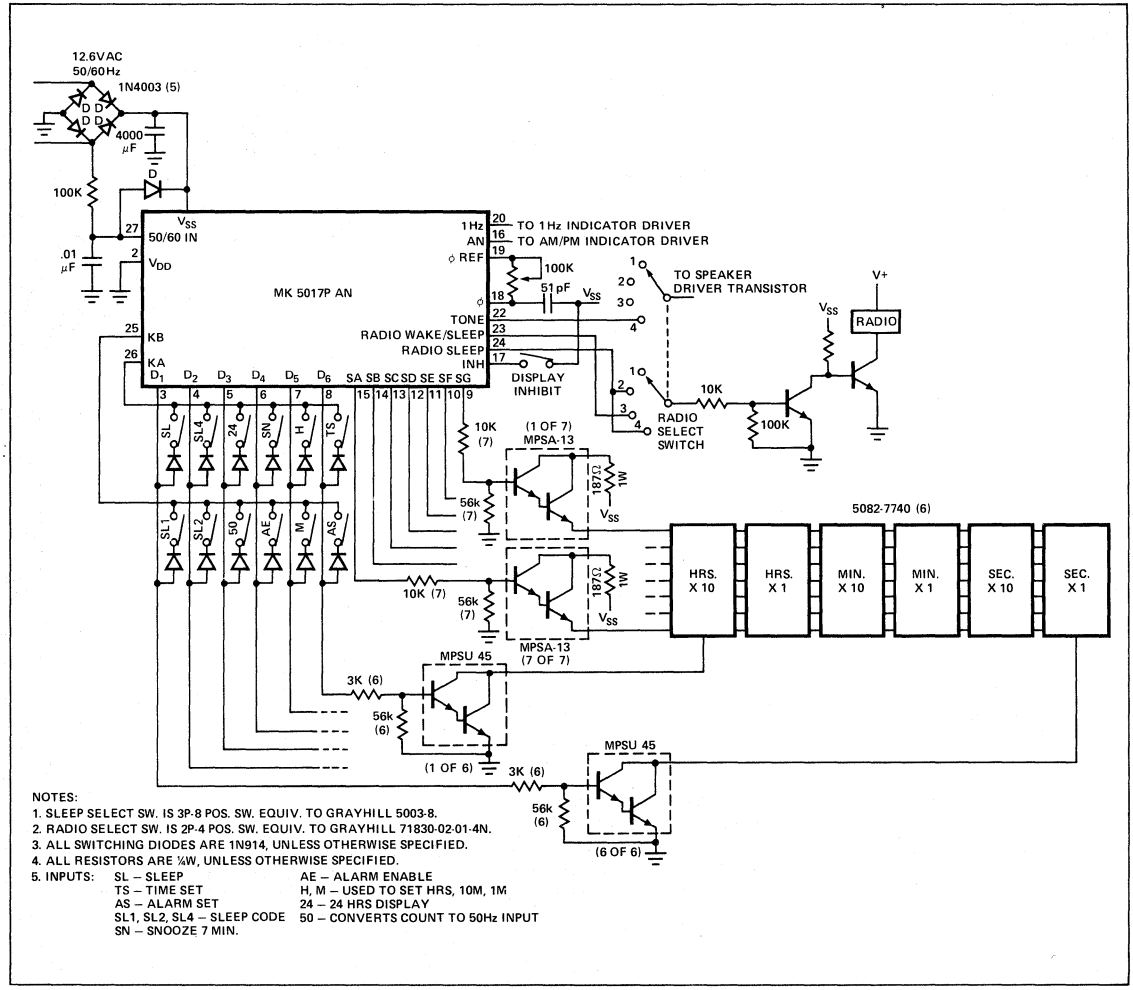


Figure 7. Six Digit Clock Radio.

COUNTERS

The strobe display circuit for a 4½ digit counter is shown in Figure 8 utilizing the 7730 common anode display (left hand decimal point) and the MOSTEK MK5007P four decade counter. Available in a 16-pin package, this circuit is a less expensive version of the familiar MK5002P, and includes latches, decoding and multiplexing functions. In addition to counting, this circuit can be used with its internal clock for DVM, timer and other measuring applications. In this example, the MK5007P's BCD outputs are converted to a seven segment format by the SN7447A decoder/driver which can sink 40mA per segment. A flip-flop is used to implement an overflow digit "1", providing a 4½ digit display. The average light level of the display is controlled by two factors. First, R controls the peak current per segment, set here for 40mA. The second factor is the duty cycle of the counter's SCAN INPUT signal. The internal multiplexing circuit for scanning the digits is triggered on the falling edge of the scan clock. While this signal is low, the segment and digit outputs are blanked.

Therefore, a duty cycle greater than 80% of the SCAN INPUT signal is desirable for efficient operation. In this circuit, use has been made of the MK5007P's internal scan clock; a timing capacitor at the SCAN INPUT sets the frequency. The MOSTEK units can be cascaded for greater than 4 decades of readout. Similar circuits in function are General Instrument's AY-5-4007 series, which have the additional feature of a 25mA sourcing capability at each segment output line.

A DC drive circuit for a 5 digit counter is outlined in Figure 9. This combines the -7730 common anode display (left hand decimal point) with the TI SN74143, a 4-bit counter/latch/decoder having 15mA constant current outputs. For applications requiring counting up to 12MHz, the use of this circuit greatly reduces the component count (even the current limiting resistors are eliminated). The LATCH STROBE INPUT allows the display to operate in a data sampling mode while the counter continues to function. The BLANKING INPUT allows total suppression or intensity modulation of the display. The stored BCD data is available for driving other logic via the LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D). For higher current drives, the SN74144 with its open-collector outputs can sink 25mA per segment.

INTENSITY UNIFORMITY

The 5082-7700 series devices are categorized for light output intensity to minimize the variation between digits or segments within a digit. Luminous intensity categories are designated by a letter located on the right hand side of the package. Display appearance will be optimized when a group of display digits uses devices from a single category.

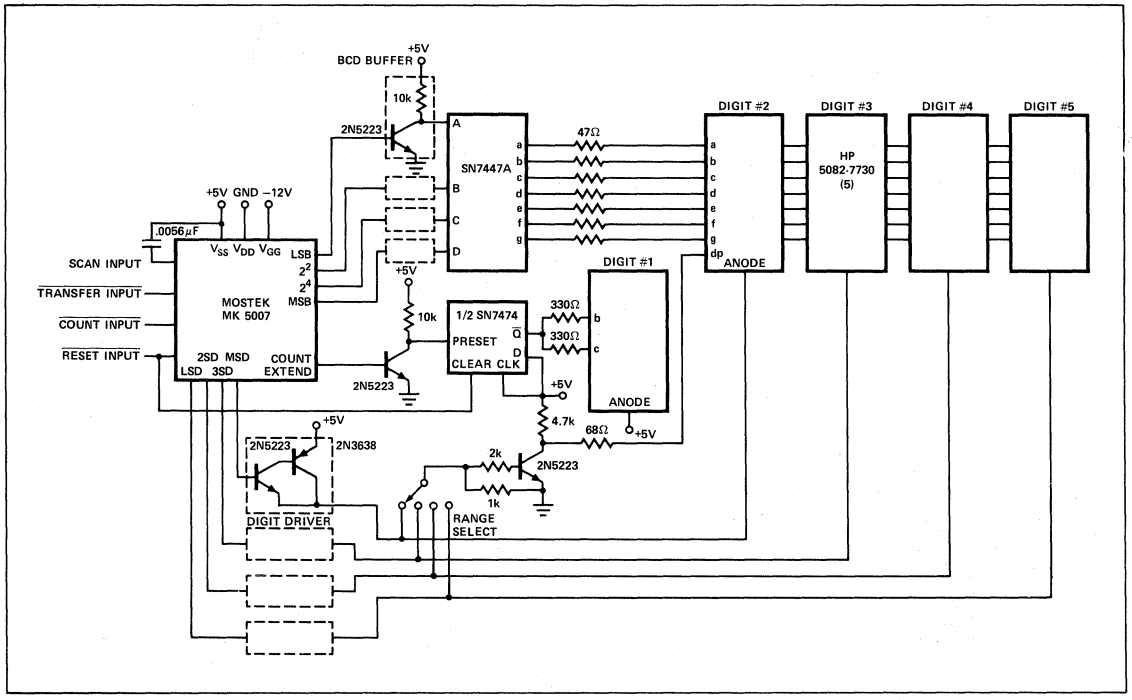
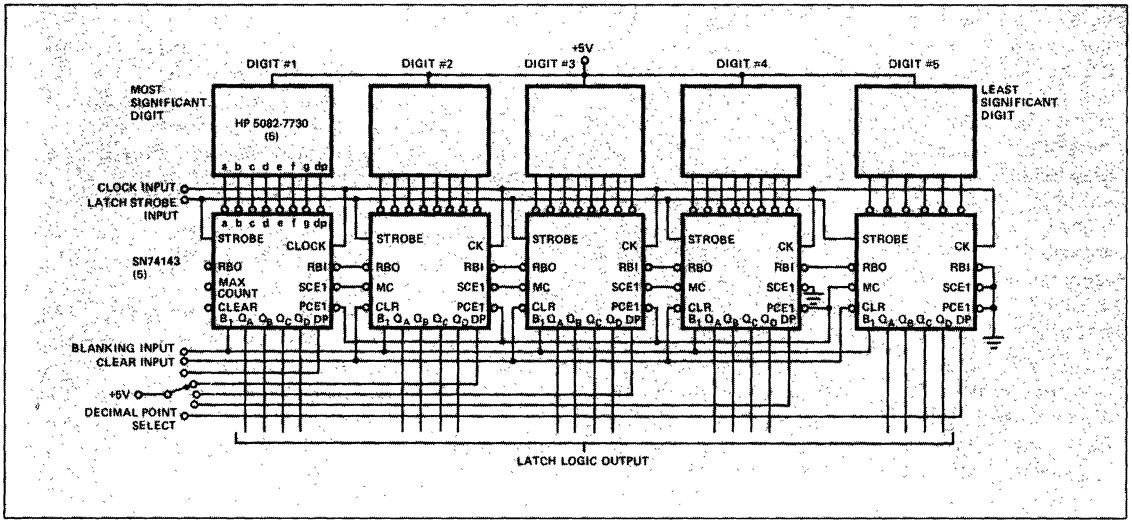


Figure 8. Four and One-half Digit Strobed Counter



INTENSITY MODULATION

It is often desirable to vary the intensity of a display to provide improved readability under varying ambient lighting conditions. Intensity control can be achieved using either amplitude or pulse width modulation techniques. The latter is recommended for broad dynamic range of intensity control. Pulse width modulation offers the advantage of good tracking between segments as the intensity is decreased, and also allows the LEDs to operate with a high peak current where they are more efficient. Figures 10 and 11 illustrate two possible techniques of control.

In Figure 10 a monostable multivibrator is triggered by the scan clock. Photo-resistor R_1 tracks with ambient light intensity and causes the monostable multivibrator to produce an output pulse width proportional to ambient lighting. This method will provide duty cycles ranging from approximately 20% to 100%.

Figure 11 depicts another intensity modulation technique. The scan clock input square wave is integrated by R_1 and C_1 to form a triangular wave. Ambient light is monitored by a phototransistor and an amplified output voltage proportional to ambient lighting is produced by A_1. These two signals are presented to the comparator A_2. The output of A_2 will be true only as long as the triangle wave voltage is greater than the ambient light signal. The LM311 amplifier used in this circuit can be replaced with any medium to high gain amplifier which will give adequate swing with a single 5 volt supply. This technique offers a 0 to 100% dynamic range of modulation.

In both of the above examples, the pulse width modulated signal is connected to the blanking input

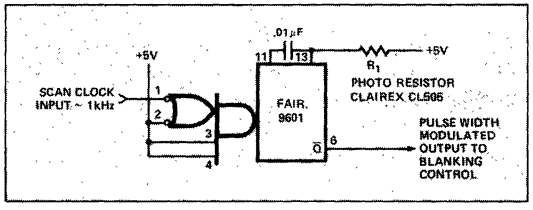


Figure 10. Multivibrator Modulation Circuit.

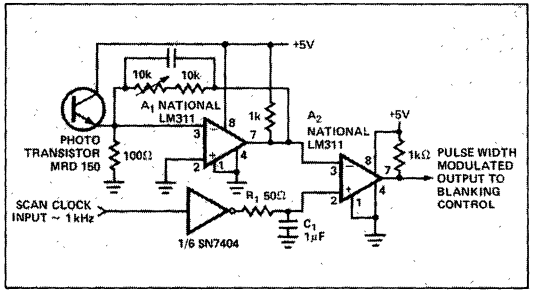


Figure 11. Wide Dynamic Range Intensity Control Circuit.

of the display driver. The display duty cycle is then controlled by the modulated signal which is proportional to the ambient intensity. If the scan frequency is substantially greater or less than 1 kHz in either of the above circuits, timing and integrating component values will have to be changed to produce satisfactory results.

CONTRAST ENHANCEMENT

The quality of the perceived display is a function not only of light intensity but also of contrast to the background. To improve display contrast, the

entire front surface of the display, except for the light emitting areas, is finished in a uniform flat black. The plastic encapsulant in the light emitting areas contains a red dye to further reduce the reflected ambient light. The display's background and the type of contrast enhancing filter used affect the display quality. Typically, PC board mounting and an inexpensive red filter (e.g., Plexiglass 2423 or materials having similar transmission characteristics) are used. Under strobe drive conditions of 10 mA/segment average, the display is easily readable to distances of ten feet and will retain good contrast under relatively high ambient lighting conditions.

There are several additional contrast enhancing measures that can be implemented to allow lower display intensity and power levels. With respect to PC board design, keep as many metallized lines as possible out of the normal viewing area. These surfaces reduce contrast by reflecting ambient light. Whenever possible, the lines running to the displays should be placed out of sight on the board's back side. You can also hide metal traces by placing them beneath the display package. To minimize the light reflected from the PC board, the area surrounding the display can be darkened either through use of a screened black epoxy ink (e.g., WORNOW W-O-N black ink) or a black piece of material cut as a collar to fit around the display. Circular polarizing filters (such as Polaroid HRCP-red) or 3M Display Film are particularly effective in enhancing contrast in high ambient light although they may be more expensive. Antiglare coatings are available from firms such as Panelgraphic Corp. to reduce front filter reflections. An antiglare surface finish may also be incorporated into the molds used to manufacture the filters.

MOUNTING CONSIDERATIONS

The 5082-7700 series devices are constructed utilizing a lead frame in a standard DIP package. In addition to easy PC board mounting, the standard pin spacing of 0.100" between pins and 0.300" between pin rows allows use of the familiar 14-pin IC sockets. See Table IV for a list of some of the available display sockets. The displays may be end-stacked as close as 0.400" center-to-center. The lead frame has an integral seating plane which holds the package approximately 0.035" above the PC board during standard soldering and flux removal operations. The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). To optimize device performance, materials are used that are limited to certain solvents for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

Note: See following pages for Tables I, II, III and IV.

Table I. Decoder/Driver Circuits for Seven Segment Displays

Manufacturer's Product No.	Manufacturer	Common Anode or Common Cathode	Rated Maximum Output Current [mA]	Other Features	Other Manufacturers
7447	Texas Instr.	CA	40		National Semi, Fairchild, Motorola, Signetics
7448	Texas Instr.	CC	4*		National Semi, Fairchild, Motorola, Signetics
9307	Fairchild	CC	5.6*		
9317 B/C	Fairchild	CA	40/20		
9357	Fairchild	CA	40		
9368	Fairchild	CC	19***	Quad Latch	
9369	Fairchild	CC	50		
9370	Fairchild	CA	25	Quad Latch	
9660	Fairchild	CC	5-50**	Pgmbl Current and Decimal Pt. Drive	
MC 14511	Motorola	CC	25	CMOS	
MC 4039	Motorola	CA	20		
N8T51 B N8T59 B	Signetics	CA, CC		MOS Compatible Inputs	
N8T74 B N8T75 B	Signetics	CA, CC		Quad latch MOS Compatible Inputs	
8140	Harris	CA	40	Quad latch	
1001/1002	SCS Microsystems		120*	Quad latch, some versions available w/resistors on board	

*with external pull-up resistance **constant current supply ***current limit resistors on board

Table II. Driver Arrays for LED Displays

Manufacturer and Product No.	Maximum Output Current	Drivers Per Package	Typical Application
ITT Semiconductor			
502	200mA Sink	6	Digit Drive
503	34mA Source	4	Segment Drive
National Semiconductor			
DM8861	50mA Source or Sink	5	Segment Drive
DM8863	500mA Sink	8	Digit Drive
Sprague Electronics			
ULN 2031A	80mA Sink	7	Segment Drive
ULN 2032A	80mA Source	7	Segment Drive
Series 400	250mA Sink	4	Digit Drive
Texas Instruments			
SN75491*	50mA Source or Sink	4	Segment Drive
SN75492*	250mA Sink	6	Digit Drive

Table III. Circuits for Seven Segment Displays

Manufacturer and Product No.	Description	Comments
Texas Instruments		
SN74143	BCD Counter/4 Bit Latch/BCD-7 Segment Decoder/15mA Constant Current Driver	Ideal for Counting Applications (Time or frequency measurements, A-D Converters).
SN74145	BCD to Decimal Decoder (1 of 10 Decoder)/ Driver	Capable of sinking 80mA per line making it ideal for a digit scanner.
SN74144	Same as SN74143 except output driver can sink up to 25mA per line	Need current limiting resistor for each segment.
SN74142	BCD Counter/4 Bit Latch/BCD to Decimal Decoder (1 of 10 Decoder) Driver	Useful for digit scanner. Need only a clock signal since counter is in circuit.
National 8551 TI SN74173 Signetics 8T10	Tri-State Quad Latches (Also known as "Bus Buffers")	Allows bussing of data lines eliminating numerous gates.
Mostek		
MK5002, 5007, 5005	4 Decade Counter/BCD-7 Segment Decoder/ 4 Digit Scanner in 1 package, 3 options	Provides all counting and timing signals for a 4 Decade Strobed Counter Display (can be end stacked for 8 decades, ...)
GI		
AY-5-4007 Series	4 Decade Counter/BCD-7 Segment Decoder/ 4 Digit Scanner/LED Driver	Similar in function to Mostek 5002 series but adds 25mA LED drivers for strobed display.

Table IV. 14 Pin DIP Sockets for 7700 Series Displays

Manufacturer and Product No.	Termination	Description
Amphenol-Barnes		
821-20011-144	Solder	Nylon, Low Profile
821-20013-144	Wire Wrap	Nylon, Low Profile
821-25011-144	Solder	Full Sized Body
821-25012-144	Wire Wrap	Full Sized Body
Augut		
314-AG50-2R	Solder	Full Sized, Phenolic
Cinch		
14-W-DIP	Wire Wrap	Low Profile, Nylon
14-DIP	Socket	Phenolic
Cambion		
3777-01-0312	Solder	Nylon
3897-01-0316	Wire Wrap	DAP Plastic

HEWLETT hp PACKARD
COMPONENTS

APPLICATION NOTE 948

Performance of the 6N135, 6N136 and 6N137 Optocouplers in Short To Moderate Length Digital Data Transmission Systems

This application note assists system designers by describing the performance to be expected from the use of HP 6N135-6N137 optocouplers as a line receiver in a TTL-TTL compatible NRZ[1] data transmission link. It describes several useful total systems including line driver, cable, terminations and TTL compatible connections. The systems described utilize inexpensive cable and operate satisfactorily over the range of transmission distances from 1 ft. to 300 ft. Over this range of distances, the data rate varies from 0.6 megabits per second to 19 megabits per second largely limited by coupler performance at short distances, and cable losses at longer distances.

[1] Non-return to zero

INTRODUCTION

Optocouplers can function as excellent alternatives to integrated circuit line receivers in digital data transmission applications. Their major advantages consist of superior common-mode noise rejection and true ground isolation between the two subsystems. For example, a conventional line receiver is limited to a ±20V common-mode noise rejection at best from DC over its operating frequency range, while an optocoupler can achieve rejections of ±2.5kV at 60Hz.

A conventional optocoupler that utilizes a photo-transistor is limited in its minimum total switching time. At the higher data rates, above 200-500 kbits/s, these delay times can become very significant. The HP 6N135 and 6N136 utilize an integrated photo-diode and transistor to produce lower total switching time. The HP 6N137 adds an integrated amplifier within its package to decrease these delay times still further. All three units can produce data rates well in excess of 500 kbits/s, while the 6N137 can couple an isolated 9.5MHz (19M bits/s) clock from its input to its output. These data rates are achieved with common-mode noise voltage rejection in excess of that provided by most types of line receivers at all frequencies.

The information contained in this application note covers the performance of optocoupler line receiver circuits; however, it does not describe design details. These details are covered in Application Note 947 "Digital Data Transmission Using Optically Coupled Isolators".

This application note describes the basic design elements of a data transmission link and presents several examples of total systems that will be useful to systems designers at distances that range from 1 ft. to 300 ft. and have a moderate overall cost. First, a few measures of performance are defined to allow systems to be compared with one another. Second, the elements of an optocoupler data transmission system are discussed. Third, circuit examples and demonstrated performance of a selected set of systems are presented for the various transmission distances. This presentation includes schematics, representative waveforms at intermediate circuit points, and a summary performance table. It compares the results of passive (resistive) terminations with active terminations that improve overall performance at the longer transmission distances. Fourth, the trade-offs that were made to arrive at the selected system components are described. Along with the trade-offs, there is a discussion of approaches to increase performance by selection of other circuit components or by "peaking" a given length system.

DEFINITIONS OF PERFORMANCE

In data transmission systems that utilize optocouplers, there are no standardized definitions that allow performance capability to be specified. The major performance parameters that are of interest are data rate capability, usually specified in bits per second; and immunity to common mode noise at the coupler input, usually specified as AC or DC common mode voltage rejection in volts, or transient voltage noise rejection in volts/microsecond.

To arrive at a definition of maximum data rate capability requires that the total system be specified including all components, and in addition, data modulation and demodulation techniques. In order to compare the various systems presented in the application note, it is necessary to define some useful terms.

One commonly used modulation technique for digital data data transmission is NRZ, or non-return-to-zero transmission. In the most common form of this technique, a twisted pair transmission line is driven by a balanced driver with an alternating plus or minus voltage signal. A number of integrated circuits are available to provide the drive signals and create a straightforward design.

One potential measure of system performance for NRZ, and potentially other modulation techniques as well, is the measurement of the maximum 50% duty cycle clock frequency that the system will pass. Since a clock represents a total 1/0 and 0/1 transition each full cycle, this square wave provides two bits of data for each cycle. As the upper clock frequency limit of a system using couplers is reached, the duty cycle will change from 50%. The MAXIMUM CLOCK DATA RATE is found by observing the system output as a function of a square wave input until the output distorts to a 10% duty cycle and multiplying this frequency by two (two bits/cycle). At this input frequency, the system data rate is very close to its absolute maximum and any potential recovery of a signal at a higher data rate is impractical. A more detailed definition of this term appears in the glossary.

Another parameter indicative of the performance of a system is to measure the system transient response in its worst case condition. The step response of a transmission system using isolators is a function of the duty cycle and repetition rate. For NRZ, if this term is properly defined, it can indicate a worst case maximum data rate that the system will faithfully transmit, regardless of the combination of ones and zeroes in the data bit stream. This step response term will be referred to as the STEP TRANSIENT DATA RATE MAXIMUM. It assumes that the pulse propagation delay down the transmission line is essentially constant, and defines a data rate maximum at which a single bit of data in a stream of all zeroes and a one, or all ones and a zero may be successfully sent through the system. This is simulated by placing a very low frequency square wave input into the line. Then the circuit delay time from a pulse received at the *end* of the line until the system output makes a transition is measured. This delay time is a function of the cable output risetime and the delays experienced in the coupler and its associated circuitry. The specific delay times are called t_{PHL} and t_{PLH}, indicating delay times for a 1/0 and 0/1 transition respectively. The STEP TRANSIENT DATA RATE MAXIMUM is defined as the inverse of t_{PLH} or t_{PHL}, whichever is longer. In general, this data rate will be lower than the MAXIMUM CLOCK DATA RATE. A more exact definition of t_{PHL}, t_{PLH} and STEP TRANSIENT DATA RATE appears in the glossary.

The parameters used to define worst-case common mode noise immunity are measured for the coupler and associated circuitry without the transmission cable. The common mode voltage rejection is a function of frequency and indicates the maximum AC steady state signal voltage common to both inputs and output ground that will not create an error in the output. This rejection reaches a minimum at some frequency. The transient voltage noise immunity is a measure of the maximum rate of rise (or fall) that can be placed across the common input terminals and output ground without producing an error voltage in the output. This term is a function of the input pulse magnitude and rate of rise for an optocoupler and is stated as a dv/dt minimum in volts per microsecond. Further definitions of these terms appear in the glossary. It should be noted that common mode characteristics of such systems are largely determined by the point at which the noise enters the transmission system. Common mode rejection for a total system would be expected to improve with increasing distance between the common mode insertion point and the input to optocoupler.

ELEMENTS OF AN OPTOCOUPLER DATA TRANSMISSION SYSTEM

The basic elements of an optocoupler transmission system are:

- ☐ Line Driver
- ☐ Transmission Cable
- ☐ Line Termination Circuit
- ☐ Optocoupler
- ☐ TTL Interface Circuit

In order that the performance of systems using the 6N135-6N137 optocouplers might be demonstrated, component elements had to be defined for several systems. These elements are chosen to be TTL compatible at the input and the output. They are also chosen to produce high performance, be moderate in cost, and work over a range of distances of one foot to 300 feet. This can then maximize the utility to systems designers of the circuits demonstrated, thus allowing them to be used without change in a variety of specific applications to produce a known level of performance.

CIRCUIT EXAMPLES AND DEMONSTRATED PERFORMANCE

To reduce the number of complete systems upon which performance is demonstrated to a practical number, a basic representative set of elements must be selected or designed. This includes a single line driver and cable type with performance measurements taken at three transmission distances — 1 ft., 100 ft., and 300 ft. It also includes two termination types, active and passive, and three types of couplers with companion TTL interface circuits. This produces six total data transmission systems upon which data rate performance can be observed at the three transmission distances. Figure 1 illustrates the line driver and cable combination selected. Figure 2 illustrates the pulse response of this driver/cable combination. Figures 3 through 8 indicate the line termination, coupler, and TTL interface circuitry for the various terminations. Included are representative waveforms measured on the three passive termination systems at the 300 ft. transmission distance. Table 1 outlines the critical parameters of the cable used and Tables 2, 3, and 4 summarize the performance demonstrated on all of the transmission systems.

The performance tabulated for the 1 ft. transmission length is indicative of that which might be achieved by a system with negligible performance degradation in the cable. The performance at 100 ft. and 300 ft. indicates the decrease in data rate due to cable losses as the transmission distance increases. This decrease is the most critical data rate limitation and is indicative of the change in performance of systems using low cost cable. Clearly evident in the tables is the increase in performance of the active termination at the 300 ft. transmission distance. Note also that the data rate of the system utilizing the 6N137 at short transmission distances is less with the active than with the passive termination. This decrease is due to the additional delay added by the active termination.

These performance tables can be used to select a design suitable for an application required by a system designer. For example, assume it is desired to design a data transmission system of variable lengths up to 100 ft. and data rates of up to 1.6 Mbits/s. The circuit shown in Figure 4 and the line driver and cable shown in Figure 1 could be selected to assure this level of performance.

SELECTION OF DEMONSTRATION CIRCUIT ELEMENTS

The foregoing systems exemplify achievable performance and incorporate a number of design decisions which are discussed in this section.

LINE DRIVER

Line Drivers generate the signal that is sent down the transmission line. They have limits as to voltage swing, output impedance, and switching time. A good compromise is provided by National Semiconductor's DM 8830. Any similar device with a low output impedance such as the Fairchild 9614 would operate satisfactorily. These devices are TTL input compatible, require no external components, are relatively inexpensive and readily available. They provide adequate performance and produce directly a dual rail (inverting and non-inverting) output.

For systems requiring higher data rates, more sophisticated and expensive drivers can be selected or designed. Figure 9 illustrates a circuit that has a higher current output and produces a higher data rate than an integrated driver. It uses several components, but does not require a supply voltage above the standard TTL 5 volts. To obtain still higher data rates, the driver line voltage output must be increased. This in turn requires a supply voltage above 5 volts. The National Semiconductor LH 0002C is an example of an integrated circuit that can be used to produce directly a higher line voltage. Numerous other discrete circuits could be designed.

TRANSMISSION CABLE

Transmission cables are very critical in the overall system. They can decrease the effect of extraneous noise voltages on system performance by providing shielding. They also greatly affect the signal losses as the transmission length increases. By controlling these losses, cables can permit a single set of system elements to function adequately for both long and short transmission distances. The critical performance parameters of a transmission cable include cost, transmission length, line series resistance (DC losses), high frequency losses, type and amount of shielding and characteristic impedance.

The Belden type 8777 is representative of a relatively well-shielded, inexpensive cable with typical transmission loss. The important characteristics of this cable are summarized in Table 1.

If it is desired to attain higher performance, the line cost becomes considerably more expensive and tends to dominate system costs. These higher performance cables utilize a large conductor size to lower DC losses, and provide considerably lower losses at high frequencies. Examples of such a cable would be Belden 9269 (IBM 32392), Belden 9250 or their equivalents.

The pulse response of the DM 8830 and the Belden 8777 illustrates the waveform degradation of signals sent down this driver/transmission line pair, regardless of the line receiver employed. Figure 1 illustrates this circuit combination, and Figure 2 illustrates the pulse waveform degradation at 1 ft., 100 ft., and 300 ft. into a 68Ω equivalent load.

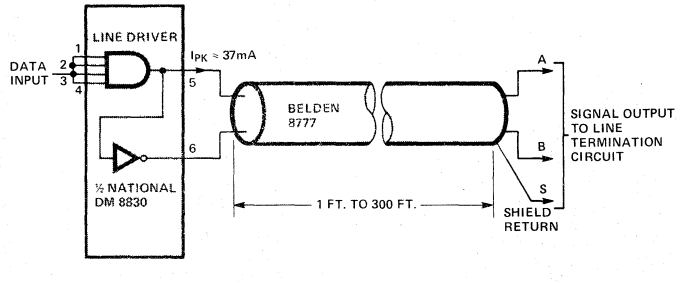


Figure 1. Line Driver and Cable Combination Selected for Use on All Six Systems to Indicate Their Performance.

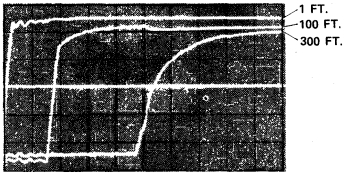


Figure 2. Pulse Characteristics of the Selected Line Driver and Cable. Measurement Observed with a 68Ω Equivalent Termination at One, 100, and 300' Distances. All Waveforms are Line to Line Voltage, Time Referenced to zero feet. Note Time Delay and Waveform Degradation.

LINE TERMINATION CIRCUIT

The line termination circuit converts the voltage arriving at the end of the line to a current impulse to drive the coupler emitter diode. In these system examples, performance of both passive and active circuits was measured.

A passive circuit consists of a set of resistors to match the line to its characteristic impedance and to convert the line voltage to a current. The circuits illustrated here were designed to provide good performance at 300 ft., while not exceeding the coupler input drive current maximum at the 1 ft. line length condition. With this design criterion, these circuits are useful over this *range* of transmission cable lengths. These design characteristics required that two resistive line termination circuits be designed for the three isolators. They are illustrated in Figures 3, 4, and 5.

An improvement in the performance of a resistive termination can be obtained by peaking the line to operate at a specific length as shown in Figure 10. This technique allows the coupler to operate from the peak to peak voltage at the end of the line. To avoid overdriving the coupler, the peaking capacitor value must be minimized. It is chosen by observing the circuit delay time t_{PLH} and selecting the smallest value of capacitor that significantly decreases this delay. With this technique, performance can be expected to improve by as much as 20-30% or more, but the values of peaking capacitor tend to vary with many of the characteristics of components in all of the elements of the system. These include driver output voltage, line length, line losses, coupler delay, etc. This in turn requires each individual system to have a selected value of peaking capacitor.

An active termination utilizes a transistor to act as a line voltage to coupler input current regulator. This technique ignores any attempt to match the line, but instead converts any incoming voltage to a suitable current, once the circuit threshold voltage is exceeded. This tends to decrease circuit sensitivity to line length and other line voltage variations. The delay of an active circuit can limit the maximum system data rate, especially for short transmission distances. But, in general, their use can improve the maximum data rate at the longer distances. In the system examples, two active termination circuits were designed and are illustrated in Figures 6, 7 and 8.

Improving the performance of the active circuit consists of finding transistors and circuit designs to perform the voltage to input current regulation function without limiting overall system performance.

OUTPUT TO TTL INTERFACE

The 6N136 and 6N137 have sufficiently high input to output coupling efficiency (CTR) that the only component required to interface the optocoupler to a TTL input gate is a pull-up resistor. The 6N135 has a somewhat lower CTR and requires an external transistor and resistor to interface with a TTL gate input. The actual circuit configuration and values required for these interface circuits are illustrated in Figures 3 through 8. The circuits illustrate, in general, the optimum interface for a TTL-TTL compatible circuit. Performance could be improved through the use of lower pull-up resistor values in the coupler output collectors and high speed TTL compatible comparators.

Table 1

IMPORTANT LINE CHARACTERISTICS OF BELDEN 8777

- Three sets of two conductor, twisted and individually foil shielded, 22 gauge wire
- Z_0 (Measured Characteristic Impedance)—68Ω line to line
- Line-to-line capacitance — 30pF/ft.
- Line Resistance — 3.2Ω/100 ft. (per conductor pair)
- Attenuation at 10MHz ≃ 4 dB/100 ft.
- Delay ≃ 1.5 nsec/ft.
- Cost ≈ 5¢/ft./Transmission Pair

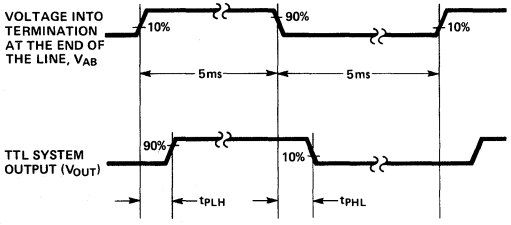
GLOSSARY

1. DATA RATE – This term is typically stated in bits per second and has no standardized definition when used in reference to optocouplers. It is related to the minimum pulse transition time that will be passed by the system and detected. This in turn is related to the distortion or change in duration the pulse experiences upon passing through the system.

2. STEP TRANSIENT DATA RATE MAXIMUM – This term, stated in bits per second, is a function of the maximum delay experienced by a 0/1 or a 1/0 transition in passing through the optocoupler. The step transient data rate maximum is defined as:

$$\text{STEP TRANSIENT DATA RATE (MAX)} = \frac{1}{t_{PHL}} \text{ or } \frac{1}{t_{PLH}}$$

whichever is smaller. Where t_{PLH} and t_{PHL} are measured at the coupler termination input (end of the line) and the TTL output and are defined as follows:

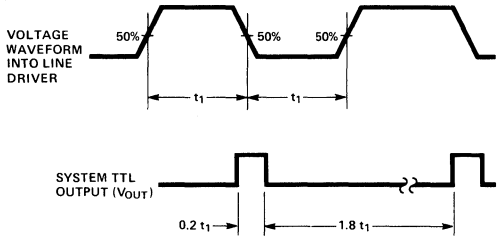


The t_{PHL} and t_{PLH} measured under these conditions approach the maximum delay that will be experienced by data sent through the isolator.

3. MAXIMUM CLOCK DATA RATE – This term defines the maximum data rate at which a 50% duty cycle square wave (clock) will be distorted to a 90%/10% pulse. It is very close to the maximum alternating 1/0 and 0/1 transition that can be passed by the system. It is defined mathematically as:

$$\text{MAXIMUM CLOCK DATA RATE} = \frac{1}{t_1}$$

where t_1 is defined as:



4. COMMON MODE REJECTION VOLTAGE – This term is defined as the maximum sinusoidal voltage at a given frequency that can be applied *simultaneously* to both inputs with respect to output ground and not produce an error signal in the system output. In optocouplers, the value of this voltage is very high at low frequencies and decreases with increasing frequency until it reaches a minimum. The effect is caused by the effective intercircuit capacitance of the emitter and detector chips, and the detector gain and bandwidth. (See Figure 11.)

5. COMMON MODE dv/dt REJECTION MINIMUM – This term is defined as the maximum rate of change of voltage that can be applied to both inputs *simultaneously* with respect to output ground and not produce an error in the system output. Note that this parameter is a function of the duration of the change, or equivalently the pulse amplitude. The stated values in this application note are for a 10V step pulse amplitude generated by a source having a controlled risetime and falltime (e.g., HP 8007B). (See Figure 11.)

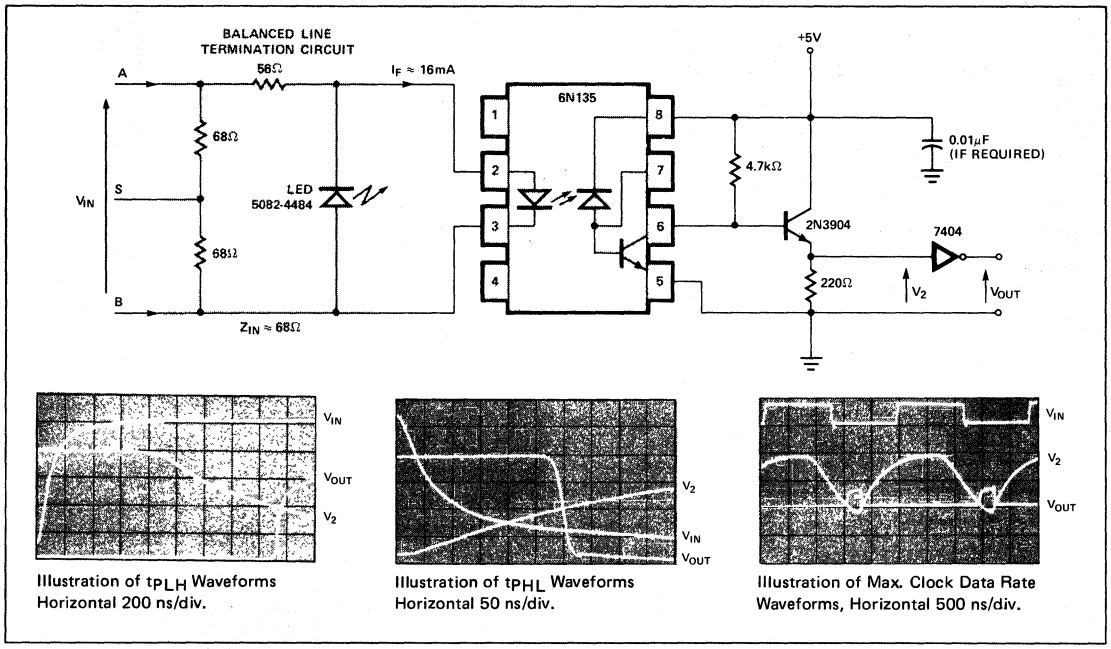


Illustration of t_{PLH} Waveforms
Horizontal 200 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 50 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 500 ns/div.

Figure 3. TTL Compatible Passive (Resistive) Termination for the 6N135 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

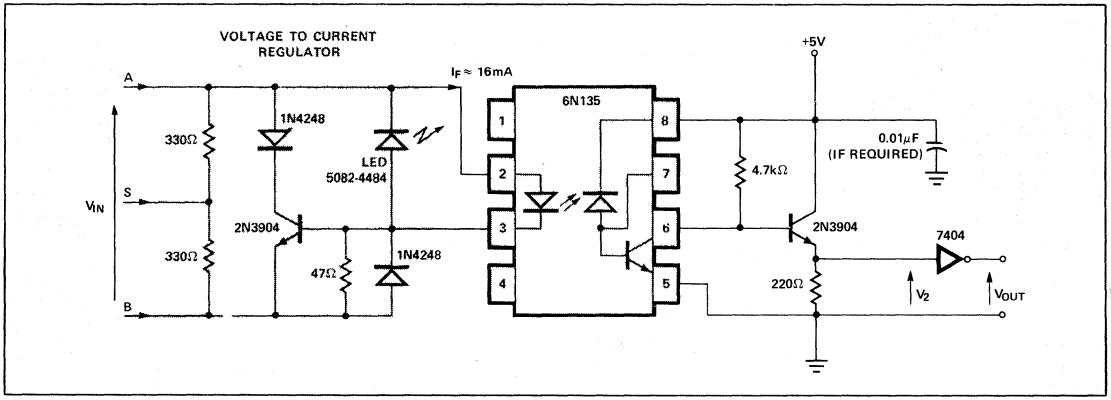


Figure 6. TTL Compatible Active Termination for the 6N135.

Table 2. Summary of Performance of 6N135 Data Transmission Systems at 1, 100, and 300 ft.

Termination	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	475	500	2.0	11.2	≤10kHz: 5.0kV pk-pk	250V/μs min.
	100	900	425	1.1	3.0		
Fig. 3	300	1700	300	0.6	0.8	1MHz: 84V pk-pk min.	
ACTIVE	1	500	330	2.0	5.3		
Fig. 6	100	580	270	1.7	4.0		
	300	875	330	1.1	1.6		

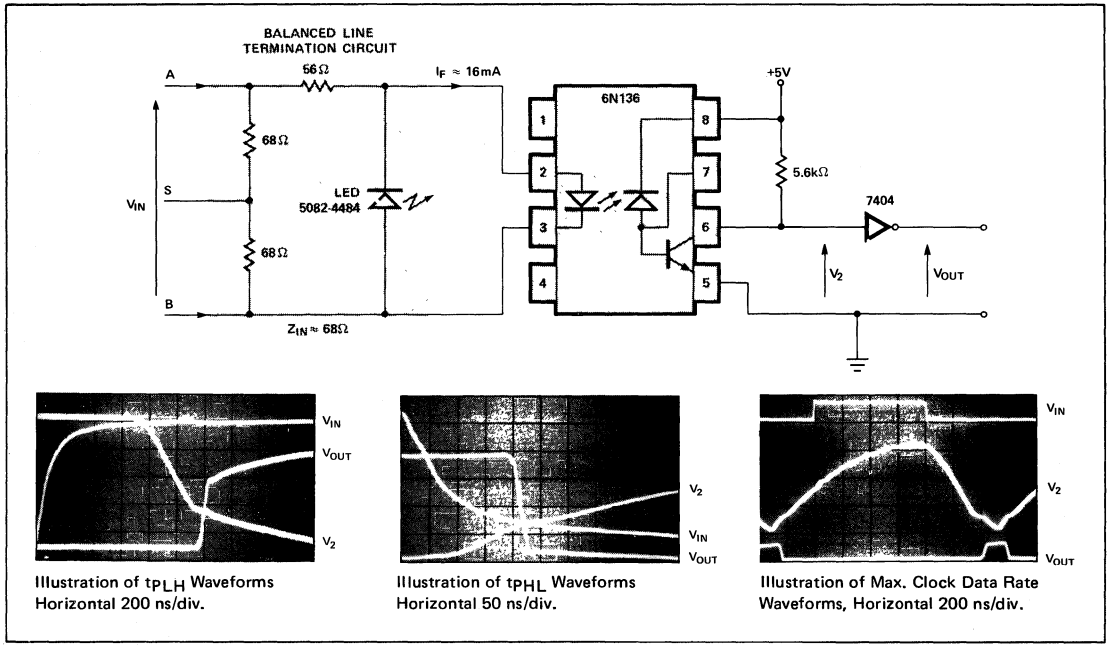


Illustration of t_{PLH} Waveforms
Horizontal 200 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 50 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 200 ns/div.

Figure 4. TTL Compatible Passive (Resistive) Termination for the 6N136 and Photographs Indicating Measured Performance at the End of the 300 Ft Cable.

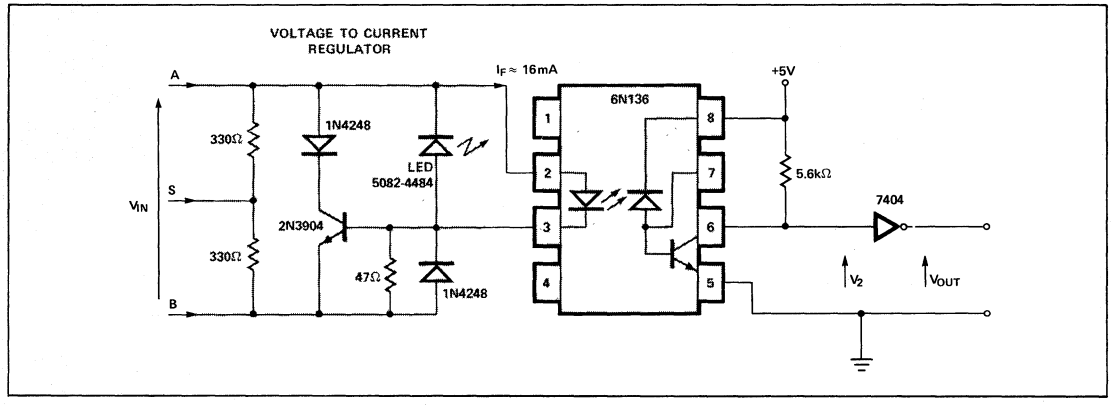


Figure 7. TTL Compatible Active Termination for the 6N136.

Table 3. Summary of Performance of 6N136 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	320	270	2.7	10.0	≤10kHz: 5.0kV pk-pk 1MHz: 84V pk-pk min.	250V/μs min.
	100	640	265	1.6	4.0		
Fig. 4	300	1200	220	0.8	1.2		
ACTIVE	1	375	250	2.7	6.6		
Fig. 7	100	440	250	2.3	5.0		
	300	700	250	1.4	2.4		

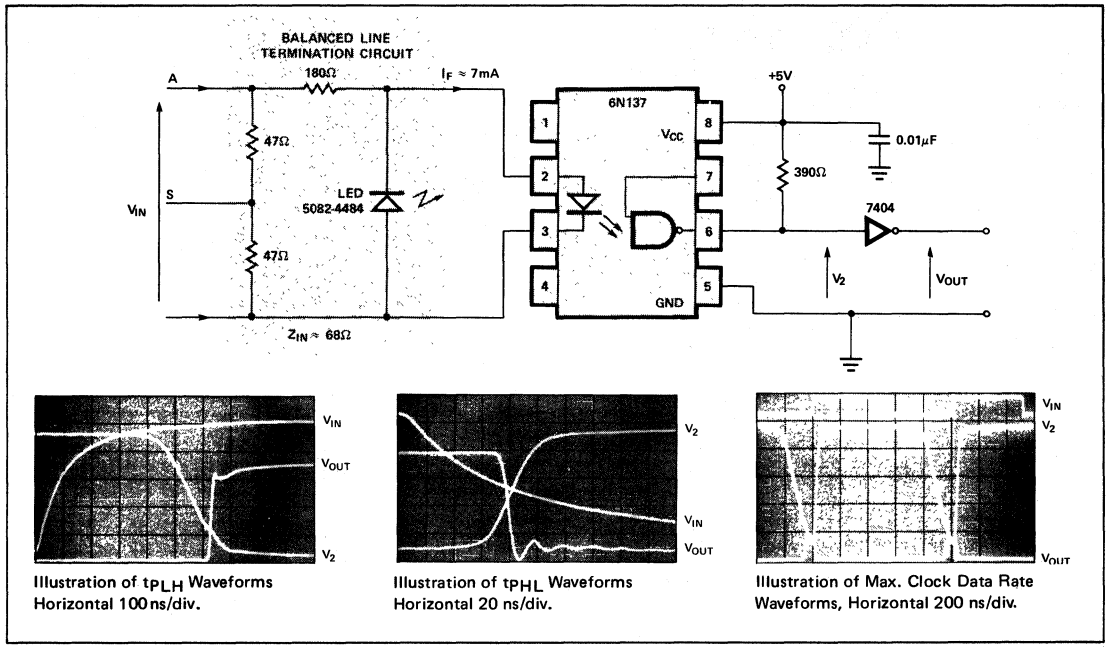


Illustration of t_{PLH} Waveforms
Horizontal 100 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 20 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 200 ns/div.

Figure 5. TTL Compatible Passive (Resistive) Termination for the 6N137 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

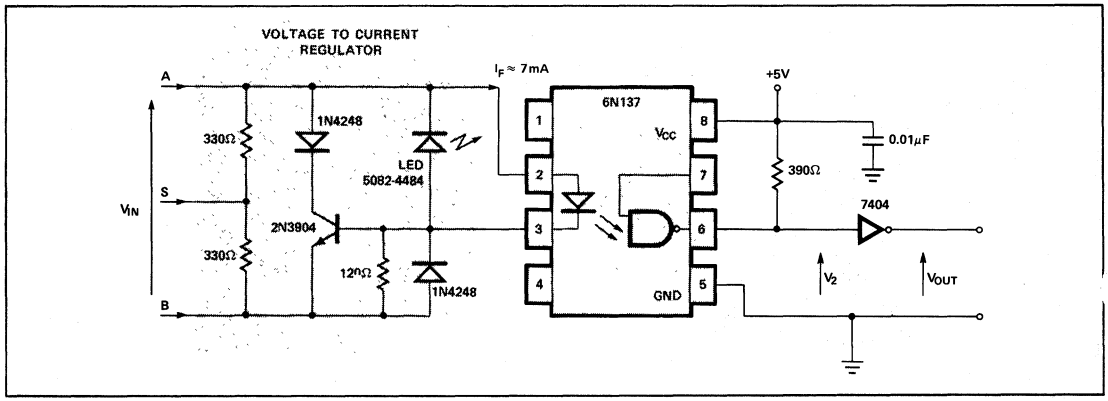


Figure 8. TTL Compatible Active Termination for the 6N137.

Table 4. Summary of Performance of 6N137 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	105	70	9.5	19.0	≤10kHz: 5.0kV pk-pk 8MHz: 22V pk-pk min.	40V/μs min.
	100	170	70	5.8	8.0		
	300	625	70	1.6	2.0		
ACTIVE	1	190	65	5.3	11.0		
	100	190	70	5.3	13.2		
	300	275	80	3.9	8.2		

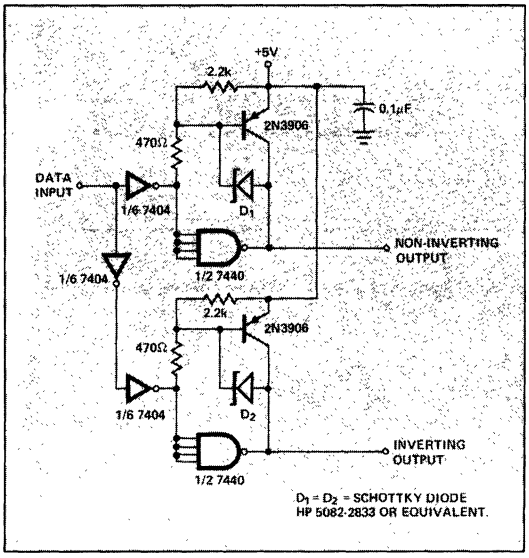


Figure 9. High Output Voltage Swing, High Current, Wide Bandwidth Line Driver that Operates From a 5 Volt Supply and Produces a >8.5V Pk to Pk Pulse into 300 Ft. of Belden 8777 at 10 MHz.

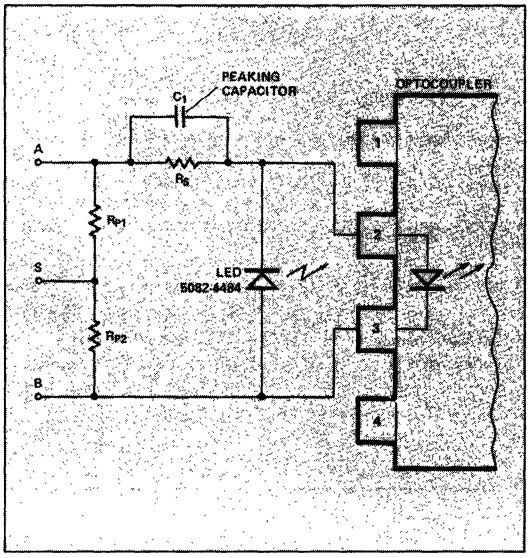


Figure 10. An Example of Circuit Peaking to Improve the Performance of the Passive Termination. C_1 is Chosen for the Minimum Value that Significantly Reduces Input to Output Delay Time. In General, C_1 Must be Selected Individually For Each System.

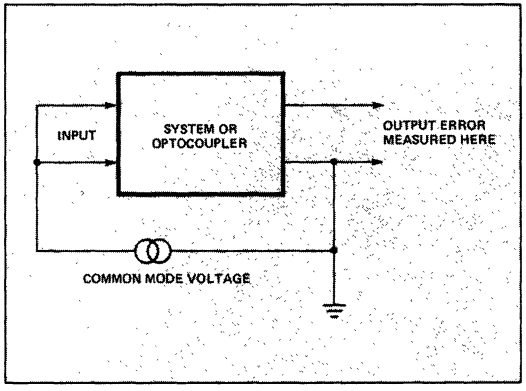


Figure 11. Common Mode Measurement Circuit.

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APPLICATION NOTE 951-1

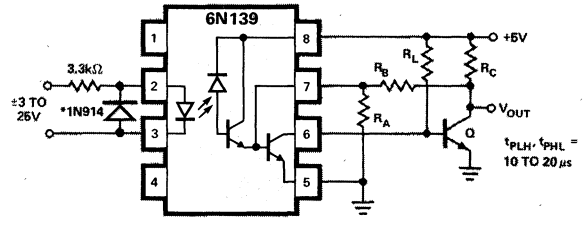
Applications for Low Input Current, High Gain Optocouplers

Optically coupled isolators are useful in applications where large common mode signals are encountered. Examples are: line receivers, logic isolation, power lines, medical equipment and telephone lines. This application note has at least one example in each of these areas for the 6N138/9 series high CTR couplers.

HP's 6N138/9 series couplers contain a high gain, high speed photodetector that provides a minimum current transfer ratio (CTR) of 300% at input currents of 1.6 mA for the 6N138 and 400% at 0.5 mA for the 6N139. The excellent low input current CTR enables these devices to be used in applications where low power consumption is required and those applications that do not provide sufficient input current for other couplers. Separate pin connections for the photodiode and output transistor permit high speed operation and TTL compatible output. A base access terminal allows a gain bandwidth adjustment to be made.

RS-232C COMPATIBLE LINE RECEIVER

- 2500V 60Hz Common Mode Rejection
- Allows use of Low Cost Line
- Full 40kbs Data Rate for Line Lengths up to 5000'
- Hysteresis for Increased Noise Immunity



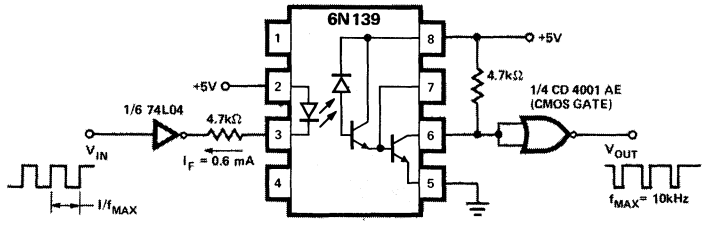
*ANTIPARALLEL DIODE IS NEEDED ONLY IF REVERSE LINE VOLTAGE EXCEEDS 15V (TO PREVENT HIGH REVERSE VOLTAGE FROM CAUSING POWER DISSIPATION IN EXCESS OF INPUT DIODE MAXIMUM RATING).

REMOVE R_A AND R_B FOR NO HYSTERESIS

R_A	R_B	R_C	R_L	Q
680kΩ	1.5MΩ	1.8kΩ	15kΩ	2N3904

LOW POWER INTERFACE

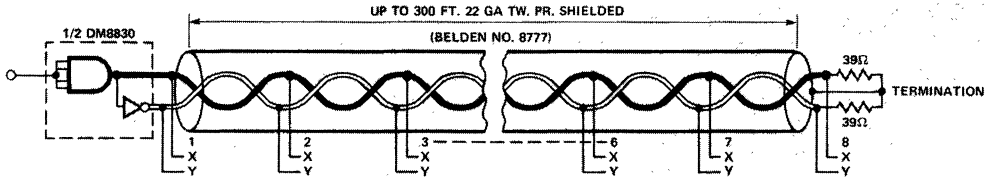
- Operation at $I_F \geq 0.5$mA
- 10kHz f_{MAX}
- Low Power Consumption



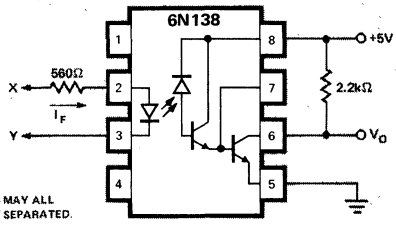
f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

LINE RECEIVER FOR PARTY LINE

- 1-8 Receivers can be used with circuit shown
- Uses conventional IC Line Driver
- Total Line Length 1-300'
- Typical Data Rate ~180kbs (t_{PHL}, t_{PLH} = 3 μsec)
- Allows use of Low Cost Line



ISOLATOR LOADS MAY BE DISTRIBUTED RANDOMLY ALONG THE LENGTH OF THE LINE, OR ALL MAY BE LUMPED AT THE END. I_F FOR 1 AND 8 ISOLATOR LOADS WOULD BE 2.7 AND 1.8mA RESPECTIVELY.

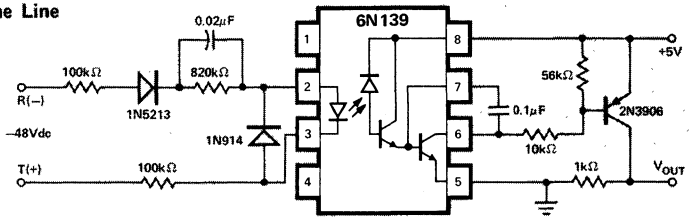


PROPAGATION DELAY: t_{PHL}, t_{PLH} = 0.5 to 5μs

OUTPUT GROUNDS MAY ALL BE ELECTRICALLY SEPARATED.

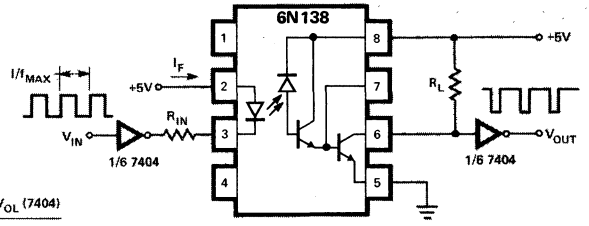
TELEPHONE RING DETECTOR

- Discriminates between Ring and Dial Signals
- Minimal Line Loading (1MΩ dc, 450kΩ at 20Hz)
- 2500V Insulation from Telephone Line
- Small Size
- Integrator Included



TTL TO TTL INTERFACE

- Direct Input and Output Compatibility
- Adjustable Data Rate
- High Fan-Out



$$I_F = \frac{5V - V_F - V_{OL}(7404)}{R_{IN}}$$

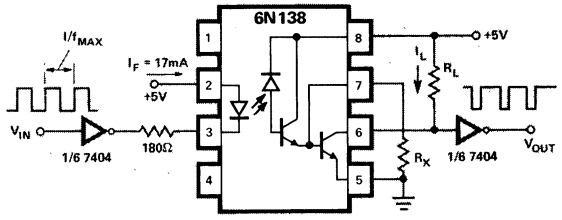
FOR HIGHER FANOUT WITH COMPARABLE DATA RATES USE SMALLER VALUES OF R_{IN}.

f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

R_L (Ω)	R_{IN} (Ω)	I_F (mA)	f_{MAX} (kHz)
2200	1800	1.7	40
270	390	8	125
100	180	17	250

GAIN/SPEED TRADE OFF

- **Obtain Maximum Speed at Required Gain**
- **Single Resistor Required**
- **Use same device for Multiple Applications**

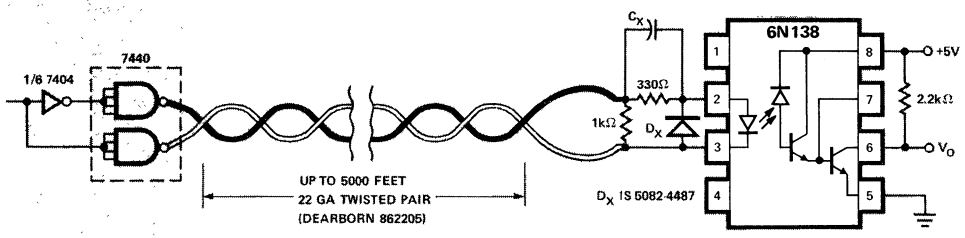


f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% or 90% DUTY FACTOR AT THE OUTPUT.

R_X (Ω)	R_L (Ω)	I_L (mA)	f_{MAX} (kHz)
NONE	100	46	250
820	1000	4.6	650

1-5000 FT. LINE RECEIVER

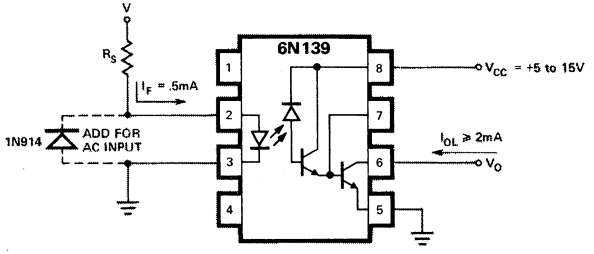
- **Drive with Standard TTL Buffer Gate**
- **2500V 60Hz Common Mode Rejection**
- **Allows use of Low Cost Line**
- **40kbs Data Rate**
- **TTL Compatible Output**



PROPAGATION DELAY: WITHOUT C_X,D_X, t_{PLH} = 2 to 5μs; t_{PHL} = 25μs
WITH D_X, $C_X \geq 0.002\mu F$, t_{PLH} = 2μs; t_{PHL} = 7μs

HIGH VOLTAGE STATUS INDICATOR

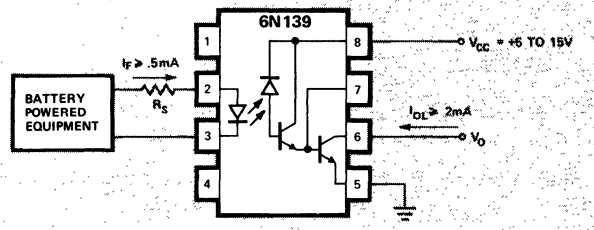
- **Low Power Consumption**
- **TTL Compatible Output**
- **High Speed**
- **Use for Power Turn On Anticipation Circuit, 117V Line Monitor or Other High Voltage Sensing**



V(Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
117	220kΩ	62
230	470kΩ	113

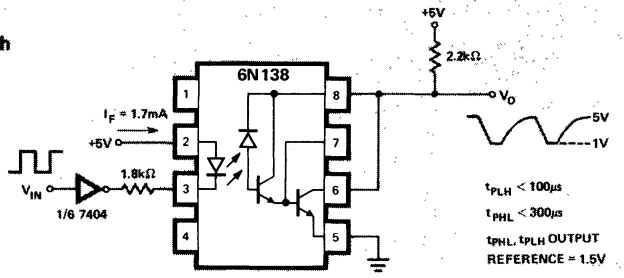
MEDICAL EQUIPMENT ISOLATION

- Low Power Consumption
- 2500V 60Hz Isolation
- Digital or Analog Operation



CONVENTIONAL DARLINGTON

- No Bias Supply Required
- Base Lead available for Gain/Bandwidth Adjust
- Data Rates of 2kbs



APPLICATION NOTES

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COMPONENTS

APPLICATION NOTE 951-2

Linear Applications of Optocouplers

Optocouplers are useful in applications where analog or DC signals need to be transferred from one module to another in the presence of a large potential difference or induced noise between the ground or common points of these modules.

Potential applications are those in which large transformers, expensive instrumentation amplifiers or complicated A/D conversion schemes are used. Examples are: sensing circuits (thermocouples, transducers ...), patient monitoring equipment, power supply feedback, high voltage current monitoring, adaptive control systems, audio amplifiers and video amplifiers.

HP's optocouplers have integrated photodetector/amplifiers with speed and linearity advantages over conventional phototransistors. In a photo transistor, the photodetector is the collector-base junction so the capacitance impairs the collector rise time. Also, amplified photocurrent flows in the collector-base junction and modulates the photo-response, thereby causing non-linearity. The photodetector in an HP optocoupler is a separately integrated diode so its photoresponse is not affected by amplified photocurrent and its capacitance does not impair speed. Some linear isolation schemes employ digital conversion techniques (A/D-D/A, PWM, PCM, etc.) in which the higher speed of the integrated photodetector permits better linearity and bandwidth.

The 6N135/6N136 is recommended for single channel AC analog designs. The HCPL-2530/31 is recommended for dual channel DC linear designs. The 6N135/6 series or the 6N137 series are recommended for digital conversion schemes.

If the output transistor is biased in the active region, the current transfer relationship for the 6N135 series optocoupler can be represented as:

$$I_C = K\left(\frac{I_F}{I_F'}\right)^n$$

where I_C is the collector current; I_F is the input LED current; I_F' is the current at which K is measured; K is the collector current when $I_F = I_F'$; and n is the slope of I_C vs. I_F on logarithmic coordinates.

The exponent n varies with I_F, but over some limited range of ΔI_F, n can be regarded as a constant. The current transfer relationship for an opto isolator will be linear only if n equals one.

For the 6N135 series optocoupler, n varies from approximately 2 at input currents less than 5mA to approximately 1 at input currents greater than 16mA. For AC coupled applications, reasonable linearity can be obtained with a single optocoupler. The optocoupler is biased at higher levels of input LED current where the ratio of incremental photodiode current to incremental LED current ($\partial I_D/\partial I_F$) is more nearly constant.

For better linearity and stability, servo or differential linearization techniques can be used.

The servo linearizer forces the input current of one optocoupler to track the input current of the second optocoupler by servo action. Thus, if $n_1 \approx n_2$ over the excursion range, the non linearities will cancel and the overall transfer function will be linear. In the differential linearizer, an input signal causes the input current of one optocoupler to increase by the same amount that input current of the second optocoupler is decreased. If $n_2 \approx n_2 \approx 2$, then a gain increment in the first optocoupler will be balanced by a gain decrement in the second optocoupler and the overall transfer function will be linear. With these techniques, matching of K will not effect the overall linearity of the circuit but will simplify circuit realization by reducing the required dynamic range of the zero and offset potentiometers.

Gain and offset stability over temperature is dependent on the stability of current sources, resistors, and the optocoupler. For the servo technique, changes of K over temperature will have only a small effect on overall gain and offset as long as the ratio of K_1 to K_2 remains constant. With the differential technique, changes of K over temperature will cause a change in gain of the circuit. Offset will remain stable as long as the ratio of K_1 to K_2 remains constant. In the AC circuit, since ($\partial I_D/\partial I_F$) varies with temperature, the gain will also vary with temperature. A thermister can be used in the output amplifiers of the Differential and AC circuits to compensate for this change in gain over temperature.

There are also several digital techniques to transmit an optocoupler analog signal. Optocouplers can be used to transmit a frequency or pulse width modulated signal. In these applications, overall circuit bandwidth is determined by the required linearity as well as the propagation delay of the optocoupler. The 6N137 series optocoupler features propagation delays typically less than 50ns and

the 6N135 series optocoupler features propagation typically less than 300ns.

In several places the circuits shown call for a current source. They can be realized in several ways. If V_{CC} is stable, the current source can be a mirror type circuit as shown in Figure 1.

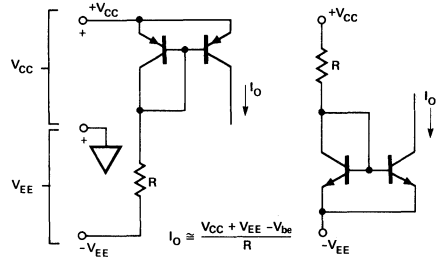

Figure 1.

If V_{CC} is not stable, a simple current source such as the ones shown in Figure 2 can be realized with an LED as a voltage reference. The LED will approximately compensate the transistor over temperature since $\Delta V_{be}/\Delta T \cong \Delta V_F/\Delta T = -2mV/°C$:

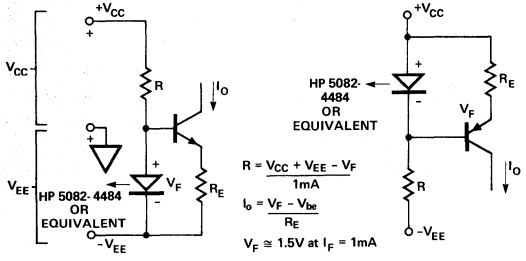

Figure 2.

SERVO ISOLATION AMPLIFIER

The servo amplifier shown in Figure 3 operates on the principle that two optocouplers will track each other if their gain changes by the same amount over some operating region. U_2 compares the outputs of each optocoupler and forces I_{F2} through D_2 to be equal to I_{F1} through D_1. The constant current sources bias each I_F at 3mA quiescent current. R_1 has been selected so that I_{F1} varies over the range of 2mA to 4mA as V_{IN} varies from −5V to +5V. R_1 can be adjusted to accommodate any desired range. With V_{IN}=0, R_2, is adjusted so that V_{OUT}=0. Then with V_{IN} at some value, R_4 can be adjusted for a gain of 1. Values for R_2 and R_4 have been picked for a worst case spread of optocoupler or current transfer ratios. The transfer function of the servo amplifier is:

$$V_{OUT} = R_4\left[\left(\frac{I_F}{2}\right)\left(\frac{K_1 R_2 (I_{CC_1})^{n_1}}{K_2 R_3 (I_F{}'_1)^{n_1}}\right)^{1/n_2}\left(1+\frac{V_{IN}}{R_1 I_{CC_1}}\right)^{n_1/n_2} - I_{CC_2}\right]$$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_4 I_{CC_2}\left[(1+x)^n - 1\right], \text{ where } x = \frac{V_{IN}}{R_1 I_{CC_1}}, \; n = \frac{n_1}{n_2}$$

The non linearities in the transfer function where $n_1 \neq n_2$ can be written as shown below. For example, if $|x| \leq .35$, $n = 1.05$, then the linearity error is 1% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^n - n\,x - 1}{n\,x}$$

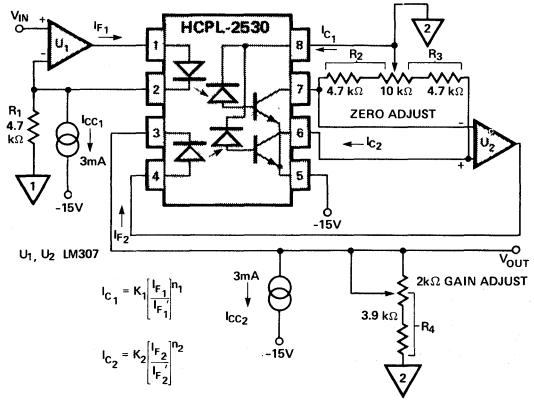

Figure 3. Servo Type DC Isolation Amplifier.

Typical Performance for the Servo Linearized DC Amplifier:

1% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2)
Gain drift: −.03%/°C
Offset drift: ±1 mV/°C
Common mode rejection: 46dB at 1 kHz
500V DC insulation (3000V if 2 single couplers are used)

DIFFERENTIAL ISOLATION AMPLIFIER

The differential amplifier shown in Figure 4 operates on the principle that an operating region exists where a gain increment in one optocoupler can be approximately balanced by a gain decrement in the second optocoupler. As I_{F1} increases due to changes in V_{IN}, I_{F2} decreases by an equal amount. If $n_1 = n_2 = 2$, then the gain increment caused by increases in I_{F1} will be balanced by the gain decrement caused by decreases in I_{F2}. The constant current source biases each I_F at 3mA quiescent current. R_1 and R_2 are designed so that I_F varies over the range of 2mA to 4mA as V_{IN} varies from −5V to +5V. R_1 and R_2 can be adjusted to accommodate any desired dynamic range. U_3 and U_4 are used as a differential current amplifier:

$$V_{OUT} = R_5\left[(R_3/R_4) I_{C1} - I_{C2}\right]$$

R_3, R_4, R_5 have been picked for an amplifier with a gain of 1 for a worst case spread of coupler current transfer ratios. The transfer function of the differential amplifier is:

$$V_{OUT} = R_5\left[\left(\frac{K_1 R_3}{R_4}\right)\left(\frac{I_{CC}}{2 I_F{}'_1}\right)^{n_1}\left(1+\frac{V_{IN}}{R\, I_{CC}}\right)^{n_1} - K_2\left(\frac{I_{CC}}{2 I_F{}'_2}\right)^{n_2}\left(1-\frac{V_{IN}}{R\, I_{CC}}\right)^{n_2}\right]$$

if $R \equiv R_1 \equiv R_2$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_5 K' \left[\left(1 + \frac{V_{IN}}{R\ I_{CC}}\right)^{n_1} - \left(1 - \frac{V_{IN}}{R\ I_{CC}}\right)^{n_2} \right],$$

$$\text{where } K' = \frac{K_1 R_3}{R_4} \left(\frac{I_{CC}}{2\ I_{F'1}}\right)^{n_1} = K_2 \left(\frac{I_{CC}}{2\ I_{F'2}}\right)^{n_2}$$

The non linearities in the transfer function when $n_1 \neq n_2 \neq 2$ can be written as shown below. For example, if $|x| \leq .35$, $n_1 = 1.9$, $n_2 = 1.8$, then the linearity error is 1.5% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^{n_1} - (1-x)^{n_2} - (n_1 + n_2)\,x}{(n_1 + n_2)\,x}, \text{ where } x = \frac{V_{IN}}{R\ I_{CC}}$$

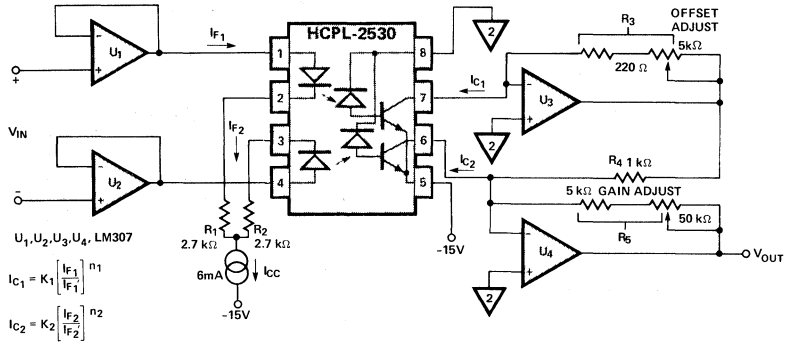

Figure 4. Differential Type DC Isolation Amplifier.

Typical Performance of the Differential Linearized DC Amplifier:

3% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2, U_3, U_4)
Gain drift: −.4%/°C
Offset drift: ±4mV/°C
Common mode rejection: 70dB at 1 kHz
3000V DC insulation

AC COUPLED AMPLIFIER

In an AC circuit, since there is no requirement for a DC reference, a single optocoupler can be utilized by biasing the optocoupler in a region of constant incremental CTR ($\partial I_D/\partial I_F$). An example of this type of circuit is shown in Figure 5. Q_1 is biased by R_1, R_2 and R_3 for a collector quiescent current of 20mA. R_3 is selected so that I_F varies from 15mA to 25mA for V_{IN} of 1V p-p. Under these operating conditions, the 6N136 operates in a region of almost constant incremental CTR. Linearity can be improved at the expense of signal-to-noise ratio by reducing I_F excursions. This can be accomplished by increasing R_3, then adding a resistor from the collector of Q_1 to ground to obtain the desired quiescent I_F of 20mA. Q_2 and Q_3 form a cascade amplifier with feedback applied through R_4 and R_6. R_6 is selected as V_{be}/I_3 with I_3 selected for maximum gain bandwidth product of Q_3. R_7 is selected to allow maximum excursions of V_{OUT} without clipping. R_5 provides DC bias to Q_3. Closed loop gain ($\Delta V_{OUT}/\Delta V_{IN}$) can be adjusted with R_4. The transfer function of the amplifier is:

$$\frac{V_{OUT}}{V_{IN}} \cong \left(\frac{\partial I_D}{\partial I_F}\right)\left(\frac{1}{R_3}\right)\left(\frac{R_4\ R_7}{R_6}\right)$$

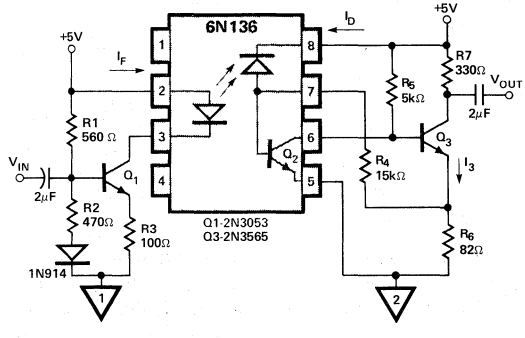

Figure 5. Wide Bandwidth AC Isolation Amplifier.

Typical Performance of the Wide Bandwidth AC Amplifier:

2% linearity over 1V p-p dynamic range
Unity voltage gain
10 MHz bandwidth
Gain drift: −.6%/°C
Common mode rejection: 22dB at 1 MHz
3000V DC insulation

DIGITAL ISOLATION TECHNIQUES

Digital conversion techniques can be used to transfer an analog signal between two isolated systems. With these techniques, the analog signal is converted into some digital form and transmitted through the optocoupler. This digital information is then converted back to the analog signal at the output. Since the optocoupler is used only as a switch, the overall circuit linearity is primarily dependent on the accuracy by which the analog signal can be converted into digital form and then back to the analog signal. However, the overall circuit bandwidth is limited by the propagation delays of the optocoupler.

Figure 6 shows a pulse width modulated scheme to isolate an analog signal. The oscillator operates at a fixed frequency, f, and the monostable multivibrator varies the duty factor of the oscillator proportional to the input signal, V_{IN}. The maximum frequency at which the oscillator can be operated is determined by the required linearity of the circuit and the propagation delay of the opto isolators:

$$(t_{max} - t_{min}) \text{ (required linearity)} \geq |t_{PLH} - t_{PHL}|$$

At the output, the pulse width modulated signal is then converted back to the original analog signal. This can be accomplished with an integrator circuit followed by a low pass filter or through some type of demodulator circuit that gives an output voltage proportional to the duty factor of the oscillator.

Figure 7 shows a voltage to frequency conversion scheme to isolate an analog signal. The voltage to frequency converter gives an output frequency proportional to V_{IN}. The maximum frequency that can be transmitted through the optocoupler is approximately:

$$f_{max} \approx \frac{1}{t}, \text{ where } t = t_{PLH} \text{ or } t_{PHL}, \text{ whichever is larger.}$$

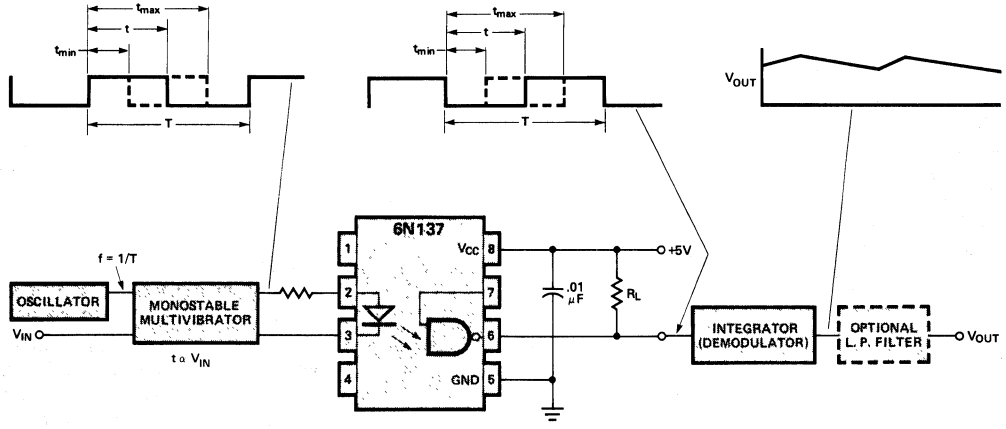

Figure 6. Pulse Width Modulation.

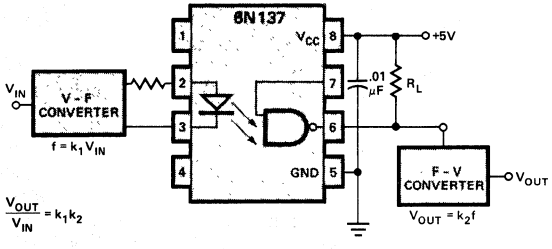

Figure 7. Voltage to Frequency Conversion.

At the output, the frequency is converted back into a voltage. The overall circuit linearity is dependent only on the linearity of the V-F and F-V converters.

Another scheme similar to voltage to frequency conversion is frequency modulation. A carrier frequency, f_o, is modulated by Δf such that $f_o \pm \Delta f$ is proportional to V_{IN}. Then at the output, V_{OUT} is reconstructed with a phase locked loop or similar circuit.

One further scheme to isolate an analog signal is to use A-D and D-A converters and transfer the binary or BCD information through optocoupler. The information can be transmitted through the optocoupler in parallel or serial format depending on the outputs available from the A-D converter. If serial outputs are not available, the A-D outputs can be converted into serial form with a PISO shift register and transmitted through one high speed optocoupler. This scheme becomes economical especially where high resolution is required allowing several optocouplers to be replaced with one high speed optocoupler. Refer to HP Application Note 947 for further discussion of digital data transmission techniques.

HEWLETT PACKARD

APPLICATION NOTE 964

Contrast Enhancement Techniques

Why Contrast Enhancement?

The most important attribute of any equipment utilizing a digital readout is the ability to clearly display information to an observer. A person viewing the display must be able to quickly and accurately recognize the information being displayed by the instrument. The display, usually front panel mounted, must be visible without difficulty in the ambient light conditions where the instrument will be used.

Since most ambient light levels are sufficiently bright to impair the visibility of an LED display it is necessary to employ certain techniques to develop a high viewing contrast between the display and its background. Since the quality of visibility is primarily subjective, it is not easily measured or treated by analytical means. Thus, human engineering plays a very important role in display applications. The best judge of the viewing esthetics of a display is the human eye. In short, is the final display design pleasing to the eye when viewed in the end use ambient?

This application note presents various criteria and techniques that a display designer should consider to obtain optimum contrast enhancement for red, yellow and green LED displays. A representative list of filter manufacturers and available filters is given at the end of this discussion.

Basic Concepts

The objective of contrast enhancement is to maximize the contrast between display "On" and display "Off" conditions. This is accomplished by (1) reducing to a minimum the reflected ambient light from the face of the display and (2) allowing a maximum of the display's emitted light to reach the eye of a viewer. The goal is to achieve a maximum contrast between "On" segments and "Off" segments as well as a maximum contrast between "Off" segments and display package and background.

Let us begin by defining the following basic terms:
Contrast Ratio, CR, may be defined as follows:

$$CR = \frac{\text{Source Luminance} + \text{Background Luminance}}{\text{Background Luminance}}$$

Contrast Improvement Ratio, CIR, may be defined as follows:

$$CIR = \frac{CR\ (\text{With Filter})}{CR\ (\text{Without Filter})}$$

It is desirable to have as high a CR as possible. One is able to measure the improvement in contrast enhancement by the CIR.

Contrast Ratio is usually applied to the face of a display as a whole. However, with stretched segment displays, such as Hewlett-Packard's 5082-7750 and 5082-7760 displays, it is difficult to achieve a high value of segment on/off contrast while effectively concealing the display package from view. For example, a display with a black package is easily concealed from view, however, the "Off" segments will be visible. This is due to the difference in reflectivity between the "Off" segments and the black package.

A reduction in the reflectivity difference between the "Off" segments and the package of a stretched segment display may be obtained by adding a small amount of dye to color tint the segments, and the display package may be colored to match the off segment color. With the addition of an appropriate optical filter placed in front of the display, the "Off" segments tend to be indistinguishable from the background. The trade-off is that a colored package is more visible than a black package. Because of this trade-off a designer has to decide which is more important, concealing "Off" segments or concealing the display package. Since the usual choice is to conceal "Off" segments, Hewlett-Packard is using this colored package technique on its 5082-7600 series High-Efficiency Red, Yellow and Green Stretched Segment Displays.

Contrast enhancement under artificial lighting conditions may be accomplished by use of selected wavelength optical filters. Under bright sunlight conditions contrast enhancement becomes more difficult and requires additional techniques such as the use of louvered filters combined with shading of the display. The effect of a wavelength optical filter is illustrated in Figure 1. The filtered portion of the display can be easily read while the "Off" segments are not apparent. By comparison, reading the unfiltered portion of the display is difficult.

Figure 1. Effect of wavelength optical filter on LED display.

Eye Response, Peak Wavelength and Dominant Wavelength

The 1931 CIE (Commission Internationale De L'Eclairage) standard observer curve, also known as the photopic curve, is shown in Figure 2. This curve represents the eye response of a standard observer to various wavelengths of light. The vivid color ranges are also identified in Figure 2. The photopic curve peaks at 555 nanometers (nm) in the yellowish-green region. This peak corresponds to 680 lumens of luminous flux (lm) per watt of radiated power (W).

Two wavelengths of the LED emission are important to a user of LED displays; Peak Wavelength and Dominant Wavelength. **Peak Wavelength** (λ_p) is the wavelength of the peak of the radiated spectrum. The peak wavelength may be used to estimate the approximate amount of display emitted light that is passed by an optical filter. For example, if an optical filter has a relative transmission of 40% at a given λ_p, then approximately 40% of the display emitted light at the peak wavelength will pass through the filter to the viewer while 60% will be absorbed. This gives a designer an initial estimate of the amount of loss of display emitted light he should expect.

Dominant Wavelength (λ_d) is used to define the color of an LED display. Since an LED approximates a monochromatic light source, the dominant wavelength of an LED may be defined as the single wavelength which is perceived by the eye to match the complete radiated spectrum of the device. As an example, the dominant wavelength of Hewlett-Packard's "Yellow" Display, which has a peak wavelength of 583 nm, is 585 nm. As shown in Figure 2, the actual color corresponding to λ_d = 585 nm is yellowish-orange. Therefore, an optimum wavelength filter will be one that is yellowish-orange (or amber) in color.

Both peak wavelength and dominant wavelength are listed in the electrical-optical characteristics on the data sheets for Helwett-Packard's LED display and lamp products.

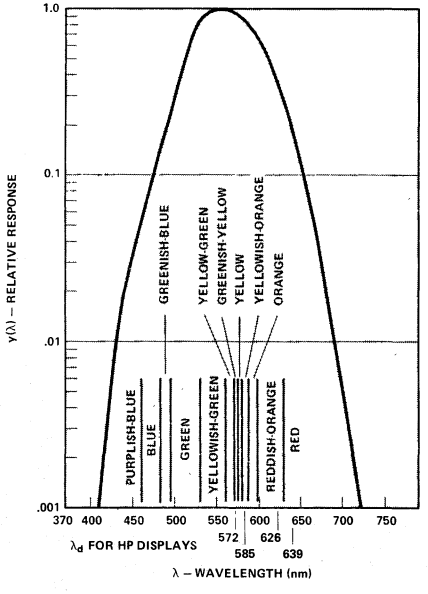

Figure 2. CIE Standard observer eye response curve (photopic curve), including CIE vivid color ranges.

Filter Transmittance

The relative transmittance of an optical filter with respect to wavelength is:

$$T(\lambda) = \frac{\text{Luminous Flux with Filter at Wavelength } \lambda}{\text{Luminous Flux without Filter at Wavelength } \lambda}$$

Most manufacturers of wavelength filters for use with LED displays provide relative transmittance curves for their products. Sample transmittance curves are presented in Figures 3, 4, 5 and 6. These curves represent approximate filter characteristics which may be used in various ambient light levels. The total transmittance curve shape and wavelength cut-off points have been chosen in direct relationship to the LED radiated spectrum. Each filter curve has been empirically determined and is similar to commercially available products. The higher the ambient light[1], the more optically dense the filter must be to absorb reflected light from the face of the display. Because the display emitted light is also strongly absorbed, the display must be driven at a high average current to be readily visible. For dim ambient light, the filter may have a high value of transmittance as the ambient light will be at levels much less than display emitted light. The display can now be driven at a low average current.

Listed on each filter transmittance curve (Figures 3, 4, 5 and 6) are empirically selected ranges of relative transmittance values at the peak wavelength which may give satisfactory filtering. For example, a filter to be used with a yellow display in moderate ambient lighting could have a transmittance value at the peak wavelength [$T(\lambda_p)$] between 0.15 and 0.30. The filter wavelength cut-off should occur between 530 and 550 nm for best results.

When selecting a filter, the transmittance curve shape, attenuation at the peak wavelength and wavelength cut-off should be carefully considered in relationship to the LED radiated spectrum and ambient light level so as to obtain optimum contrast enhancement.

[1] Dim ambients are in the range of 3 to 20 footcandles (32 to 215 lux), moderate ambients are in the range of 20 to 100 footcandles (215 to 1076 lux), and bright ambients are in the range of 100 to 500 footcandles (1076 to 5382 lux). Footcandle = (lm/ft^2) and lux = (lm/m^2).

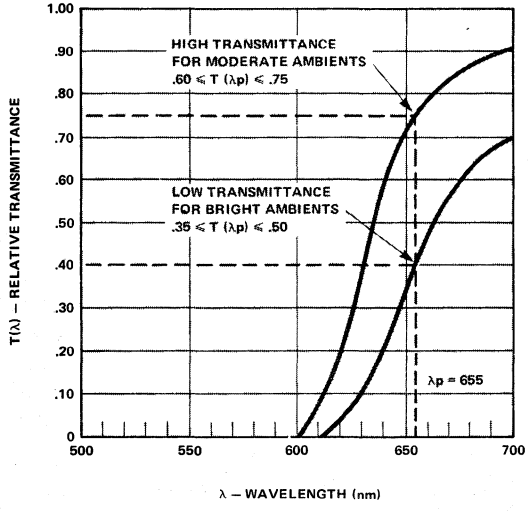

Figure 3. Typical transmittance curve for filters to be used with HP standard GaAsP red displays.

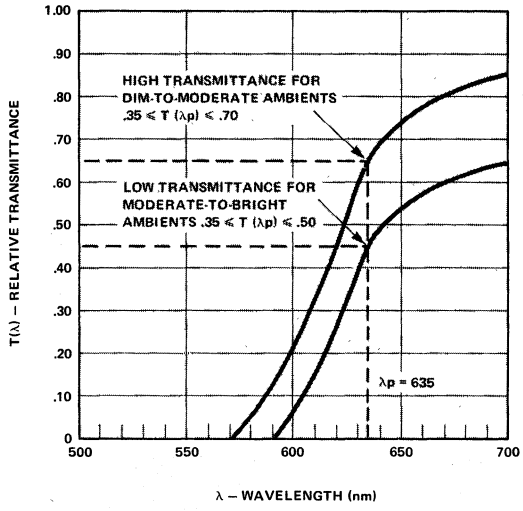

Figure 4. Typical transmittance curves for filters to be used with HP high-efficiency red displays.

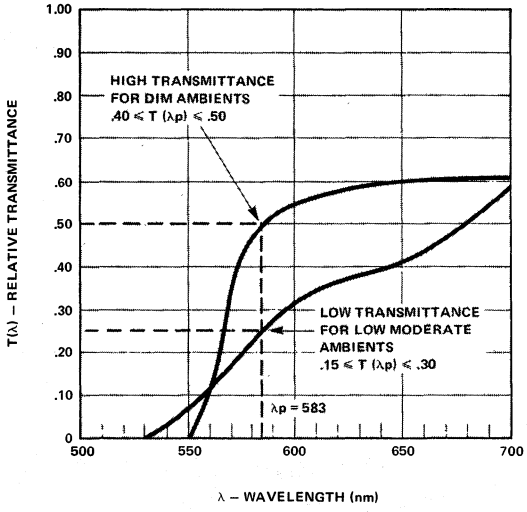

Figure 5. Typical transmittance curves for filters to be used with HP yellow displays.

Wavelength Filtering

The application of wavelength filters as described in the previous section is the most widely used method of contrast enhancement under artificial lighting conditions. Wavelength filters are very effective in artificial lighting. However, they are not very effective in daylight due to the high level ambient light. Filtering in daylight conditions is best achieved by using louvered filters (discussed in a later section).

Figures 7, 8, 9 and 10 show the relationship between artificial lighting and the spectra of LED displays, both unfiltered and filtered. Figures 7a through 10a show the relationship between the various LED spectra and the spectra of daylight flourescent and incandescent light. The photometric spectrum (shaded curve) is obtained by multiplying the LED radiated spectrum [f(λ)] by the photopic curve

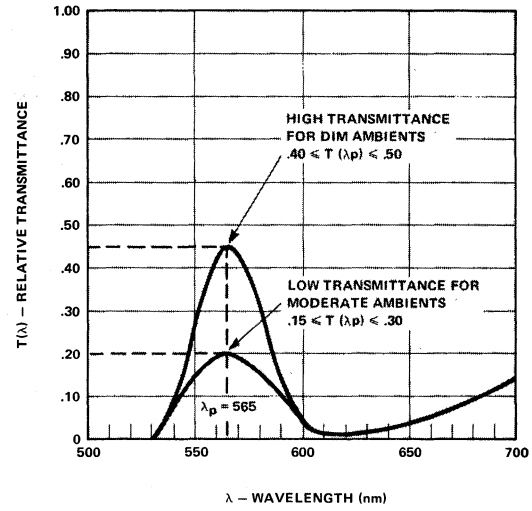

Figure 6. Typical transmittance curves for filters to be used with HP green displays.

[y(λ)]. Thus, photometric spectrum = f(λ)•y(λ). Figures 7b through 10b demonstrate the effect of a wavelength filter. The filtered photometric spectrum is what the eye perceives when viewing a display through a filter (shaded curve). Thus, filtered photometric spectrum = f(λ)•y(λ)•T(λ). The ratio of the area under the filtered photometric spectrum to the area under the unfiltered photometric spectrum is the fraction of the visible light emitted by the display which is transmitted by the filter:

$$\text{Fraction of Available Light from Filtered Display} = \frac{\int f(\lambda)\cdot y(\lambda)\cdot T(\lambda)\cdot d\lambda}{\int f(\lambda)\cdot y(\lambda)\cdot d\lambda}$$

In addition to attenuating a portion of the light emitted by the display, a filter also shifts the dominant wavelength, thus causing a shift in the perceived color. For a given display spectrum, the color shift depends on the cut-off wavelength and shape of the filter transmittance characteristic. A choice among available filters must be made on the basis of which filter and LED combination is most pleasing to the eye. A designer must experiment with each filter as he cannot tell by transmittance curves alone. The filter spectra presented in Figures 3, 4, 5 and 6 are suggested starting points. Filters with similar characteristics are commercially available.

Filtering Red Displays (λp = 655 nm) Filtering out reflected ambient light from red displays is easily accomplished with a long wavelength pass filter having a sharp cut-off in the 600 nm to 625 nm range (see Figures 3 and 7b). Under bright flourescent light, a red filter is very effective due to the low concentration of red in the flourescent spectrum. The spectrum of incandescent light contains a large amount of red, and therefore, it is difficult to filter red displays effectively in bright incandescent light.

Filtering High-Efficiency Red Displays (λp = 635 nm) The use of a long wavelength pass filter with a cut-off in the 570 nm to 590 nm range gives essentially the same results as is obtained when filtering red displays (see Figures 4 and 8b). The resulting color is a rich reddish-orange.

Filtering Yellow Displays (λp = 583 nm) The peak wavelength of a yellow LED display is in the region of the

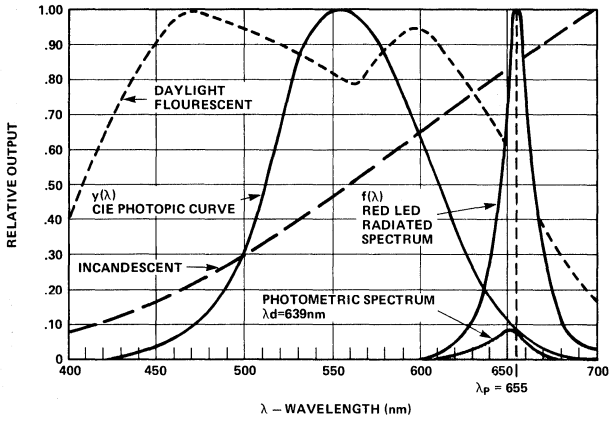

Figure 7A. Relative relationship between standard GaAsP red LED display spectrum, photopic curve and artificial lighting.

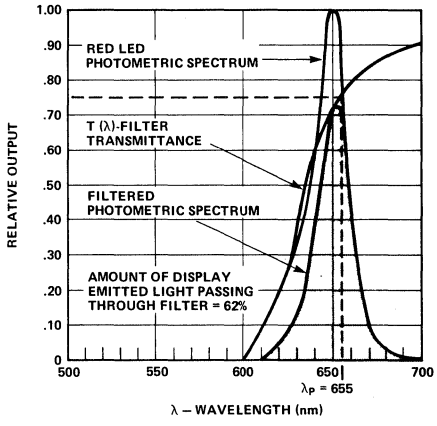

Figure 7B. Effect of a long pass wavelength filter on red LED displays.

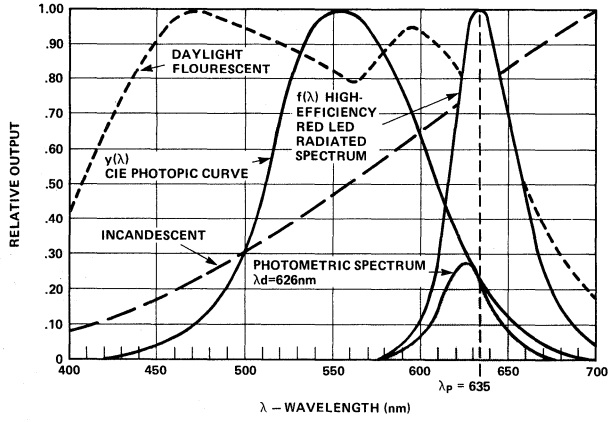

Figure 8A. Relative relationship between high-efficiency red LED display, photopic curve and artificial lighting.

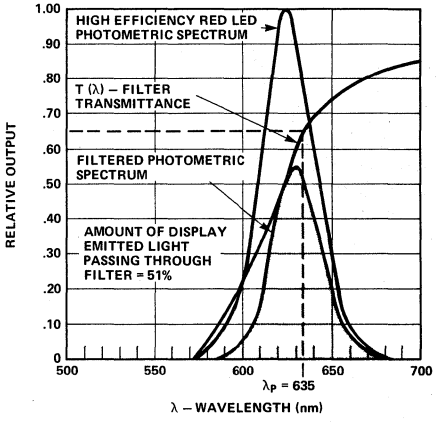

Figure 8B. Effect of a long pass wavelength filter on high-efficiency red LED displays.

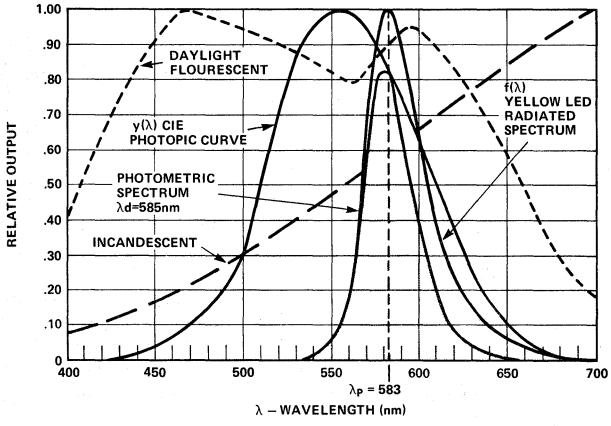

Figure 9A. Relative relationship between yellow LED displays, photopic curve and artificial lighting.

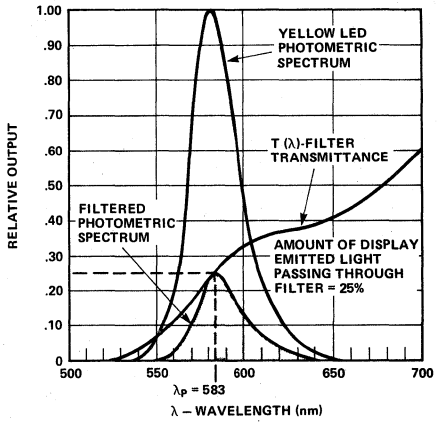

Figure 9B. Effect of a long pass wavelength filter on yellow LED displays.

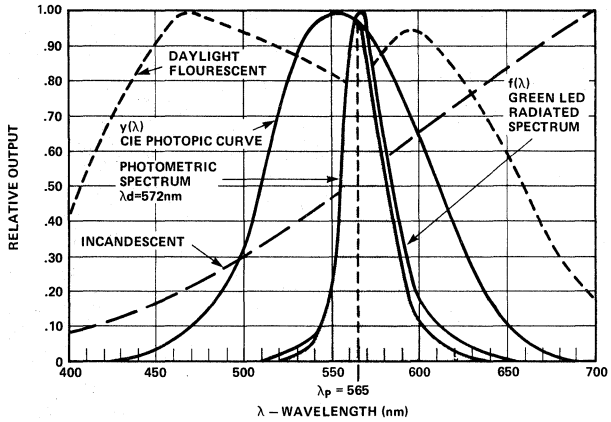

Figure 10A. Relative relationship between green LED displays, photopic curve and artificial lighting.

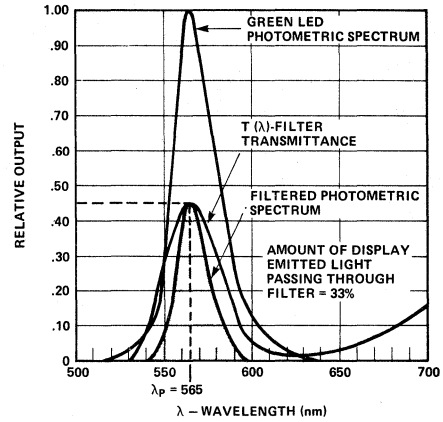

Figure 10B. Effect of a bandpass wavelength filter on green LED displays.

photopic curve where the eye is most sensitive (see Figure 9a). Also, there is a high concentration of yellow in the spectrum of flourescent light and a lesser amount of yellow in incandescent light. Therefore, filters that are more optically dense than red filters at the peak wavelength are required to filter yellow displays. The most effective filters are the dark yellowish-orange (or dark amber) filters as shown in Figure 5. The use of a low transmittance yellowish-orange filter, as shown in Figure 9b, results in a similar color to that of a gas discharge display. Pure yellow filters provide very little contrast enhancement.

Filtering Green Displays (λp = 565 nm) The peak wavelength of a green LED display is only 10 nm from the peak of the eye response curve (see Figure 10a). Therefore, it is very difficult to effectively filter green displays. A long wavelength pass filter, such as is used for red and yellow displays, is no longer effective. An effective filter is obtained by combining the dye of a short wavelength pass filter with the dye of a long wavelength pass filter, thus forming a bandpass yellow-green filter which peaks at 565 nm as shown in Figure 6. Pure green filters peak at 520 nm and drop off rapidly in the 550 nm to 570 nm range and are not recommended. The best possible filters for green LED displays are those which are yellow-green bandpass, peaking at 565 nm and dropping off rapidly between 575 nm and 590 nm. As shown in Figure 10b, this filter passes wavelengths 550 to 570 while sharply reducing the longer wavelengths in the yellow region. To effectively filter green LED displays in flourescent light would require the use of a filter with a low transmittance value at the peak wavelength. This is due to the high concentration of green in the flourescent spectrum. It is easier to filter green displays in bright incandescent light due to the low concentration of green in the incandescent spectrum, see Figure 10a.

Three manufacturers of wavelength filters are **Panelgraphic Corporation** (Chromafilter®), **SGL Homalite** and **Rohm & Haas Company** (Plexiglas). The LED filters produced by these manufacturers are useable with all of Hewlett-Packard's display and lamp products. Table 2 lists some of the filter manufacturers and where to go for further information. Table 3 lists some specific wavelength filter products with recommended applications.

Louvered Filters

Louvered filters are very effective in reducing the amount of bright artificial light or daylight reflected from the face of a display, without a substantial reduction in display emitted light. The construction of a louvered filter is diagrammed in Figure 11. Inside a plastic sheet are thin parallel louvers which may be oriented at a specific angle with respect to the surface normal. The zero degree louvered filter has the louvers perpendicular to the filter surface.

The operation of a louvered filter is similar to a venetian blind as shown in Figure 12. Light from the LED display passes between the parallel louvers to the viewer. Off-axis ambient light is blocked by the louvers and therefore is not able to reach the face of the display to be reflected back to the viewer. This results in a very high contrast ratio with minimal loss of display emitted light at the On-axis viewing angle. The trade-off is a restricted viewing angle. For example, the zero degree louvered filter shown in Figure 11 has a horizontal viewing angle of 180°; however, the vertical viewing included angle is 60°. The louver aspect ratio (louver depth/distance between louvers) determines viewing angle. A list of louver option possibilities is given in Table 1.

Some applications require a louver orientation other than zero degrees. For example, an 18 degree louvered filter may be used on the sloping top surface of a point of sale terminal. A second, is the use of a 45 degree louvered filter on overhead instrumentation to block out ambient light from ceiling mounted lighting fixtures.

Louvered filters are effective filters for enhancing the viewing of LED displays installed in equipment operating under daylight ambient conditions. In bright sunlight, the most effective filter is the crosshatch louvered filter. This is essentially two zero degree neutral density louvered filters oriented at 90 degrees to each other. Red, yellow and green digits may be mounted side by side in the same display. Using only the crosshatch filter, all digits will be clearly visible and easily read in bright sunlight as long as the sunlight is not parallel to the viewing axis. The trade-off is restricted vertical and horizontal viewing. The effective viewing cone is an included angle of 40° degrees (for a filter aspect ratio of 2.75:1).

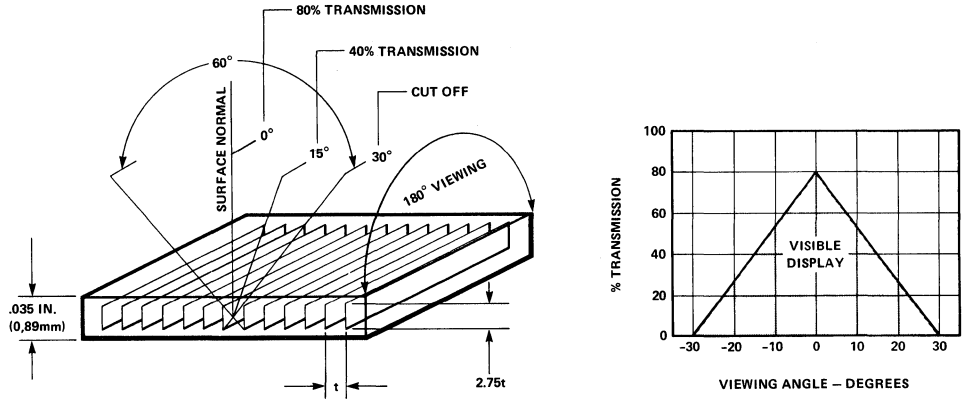

Figure 11. Construction characteristics of 0° neutral density louvered filter.

Table 1. Available Options for Louvered Filters – Any Combination is Possible

Aspect Ratio and Viewing Angle	Louver Angle	Louver Color
2.75:1 = 60°	0°	Opaque Black
2.0:1 = 90°	18°	Translucent Gray
3.5:1 = 48°	30°	Transparent Black
	45°	

Example: 2.75:1 – 18° – Transparent Black

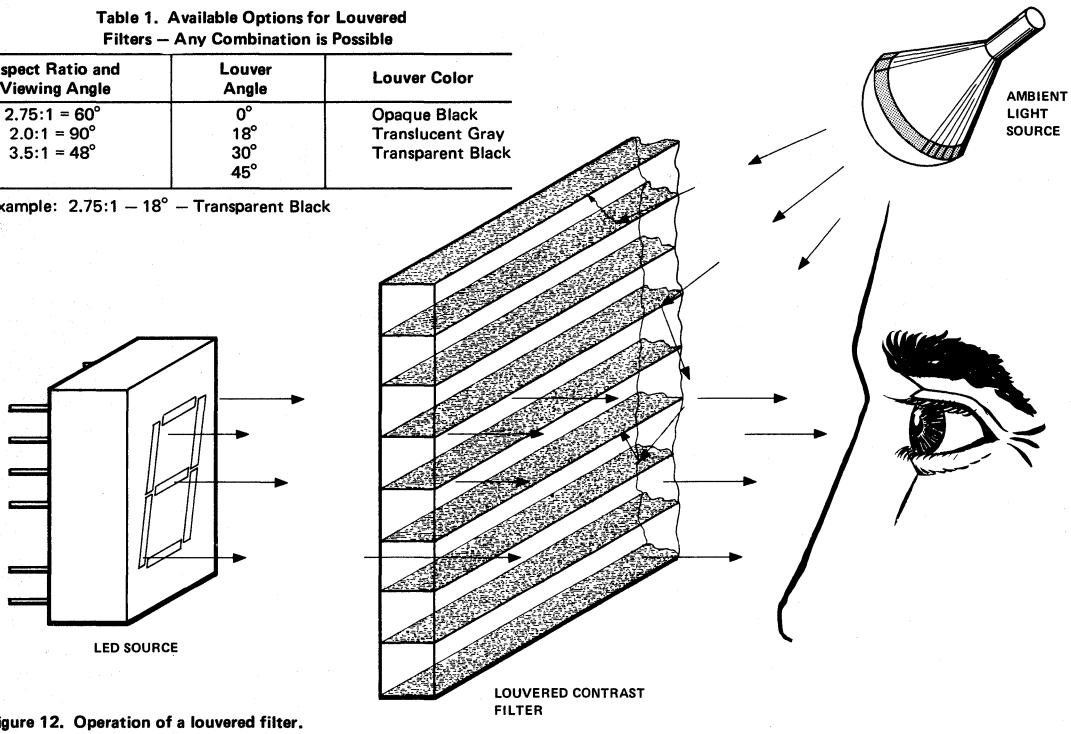

Figure 12. Operation of a louvered filter.

Neutral density louvered filters are effective by themselves in most bright ambient lighting conditions without the aid of a secondary wavelength filter. However, colored louvered filters may be used for additional wavelength filtering at the expense of display emitted light.

3M Company, Light Control Divison, manufactures louvered filters for LED displays. Their product trade name is "Light Control Film", which is useable with all of Hewlett-Packard's LED display and lamp products.

Circular Polarizing Filters

Circular Polarizing Filters are effective when used with LED displays that have specular reflecting front surfaces. Specular reflecting surfaces reflect light without scattering. Displays that have polished glass or plastic facial surfaces belong to this category. Circular Polarizing Filters are effective when used with Hewlett-Packard's 5082-7010, -7100 and -7300 series displays.

The operation of a circular polarizer may be described as follows. As shown in Figure 13, the filter consists of a laminate of a linear polarizer and a quarter wave plate. A quarter wave plate has its optical axis parallel to the flat surface of the polarizer and is oriented at 45° to the linear polarization axis. Non-polarized light is first linearly polarized by the linear polarizer. The linearly polarized light has x and y components with respect to the quarter wave plate.

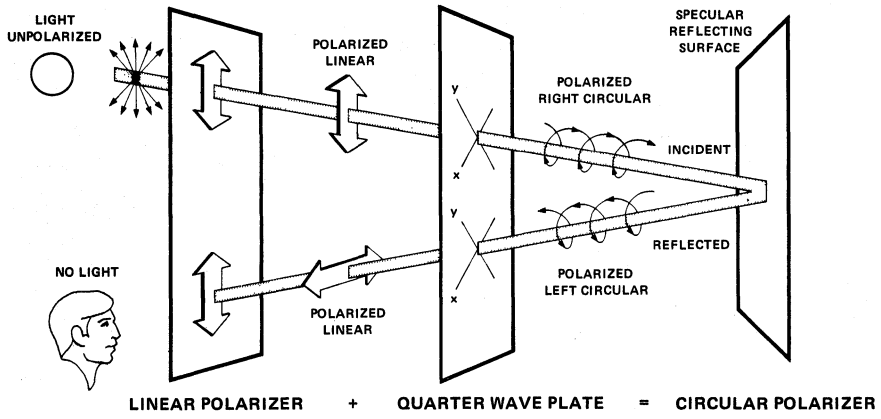

Figure 13. The operation of a circular polarizer.

As the light passes through the quarter wave plate, the x and y components emerge 90° out of phase with each other. The polarized light now has x and y forming a helical pattern with respect to the optical path, and is termed circular polarized light. As this circular polarized light is reflected by the specular reflecting surface, the circular polarization is reversed. When the light passes back through the quarter wave plate it becomes linearly polarized at 90° to the linear polarizer. Thus reflected ambient light is blocked.

The advantage of a circular polarizer is that reflected ambient light is reduced more than 95%. However, the trade-off is that display emitted light passing through the circular polarizer is reduced by approximately 65% at the peak wavelength. This then necessitates an increased drive current for the display, more than that required for a wavelength filter.

Circular polarizers are normally colored to obtain additional selected wavelength filtering. **One Caution:** outdoor applications will require the use of an ultraviolet, uv, filter in front of the circular polarizer. Prolonged exposure to ultraviolet light will destroy the filter's polarizing properties.

Polaroid Corporation manufactures circular polarizing filters in the United States. In Europe, E. Käseman of West Germany produces high quality circular polarizers.

Anti-Reflection Filters, Mounting Bezels and Other Suggestions

Anti-reflection filters: A filtered display still may not be readable by an observer if glare is present on the filter surface. Glare can be reduced by the addition of an anti-reflection surface as part of the filter. Both sections of the display shown in Figure 14 are filtered. The left hand filter has an anti-reflection surface while the right hand filter does not.

An anti-reflection surface is a mat, or textured, finish or coating which diffuses incident light. The trade-off is that both incident ambient and display emitted light are diffused. It is therefore desirable to mount the filter as close to the display as possible to prevent the display image from appearing fuzzy.

Panelgraphic Chromafilters® come standard with an anti-reflection coating. SGL Homalite offers two grades of a molded anti-reflection surface. 3M Company and Polaroid also offer anti-reflection surface options. Optical coating companies will apply anti-reflection coating for specialized applications, though this is usually an expensive process. Three companies of many which do commercial filter coating are: Optical Coating Labs, Inc., Santa Rosa, California; Optics Technology, Inc., Redwood City, California; Valpey Corporation, Holliston, Massachusetts.

Mounting bezels: It is wise to take into account the added appearance of a front panel that has the display set-off by a bezel. A bezel of black plastic, satin chrome or brushed aluminum, as examples, will accent the display and attract the eye of the viewer. The best effect can be achieved by a custom bezel. Commercial black plastic bezels for digits up to .3 inch (7.62 mm) tall are available, see Table 2.

Other suggestions: When designing the mounting configuration of a display, consider recessing the display and filter 0.25 inch (6.35 mm) to 0.5 inch (12.7 mm) to add some shading effect. If a double sided printed circuit board is used, keep traces away from the normal viewing area or cover the top surface traces with a dark coating so they can not be seen. Mount the display panel in such a manner as to be easily removed if service should become necessary. If possible, mount current limiting resistors on a separate board to reduce the ambient temperature in the vicinity of the displays.

Figure 14. Effect of anti-reflection surface on an optical filter.

Table 2. List of Filter and Bezel Product Manufacturers

Manufacturer	Product
Panelgraphic Corporation 10 Henderson Drive West Caldwell, New Jersey 07006 Phone: (201) 227-1500	Chromafilter® — Wavelength filters with anti-reflective coating; Red, Yellow, Green
SGL Homalite 11 Brookside Drive Wilmington, Delaware 19804 Phone: (302) 652-3686	Wavelength filters; two optional anti-reflective surfaces; three plastic grades; Red, Yellow, Green
3M - Company Visual Products Division 3M Center, Bldg. 235-2E Saint Paul, Minnesota 55101 Phone: (612) 733-5747	3M - Brand Light control film; louvered filters
Glarecheq, Ltd. 1-4 Christina St. London EC2A 4PA England Phone: (44) 1-739-6964	Spectrafilter
Rohm and Haas Independence Mall West Philadelphia, Pennsylvania 19105 Phone: (215) 592-3000	Plexiglass; sheet and molding powder; wavelength filters, sold as Oroglas in Europe
Polaroid Corporation Polarizer Division 549 Technology Square Cambridge, Massachusetts 02139 Phone: (617) 864-6000	Circular polarizing filters
E. Käsemann GmbH D 8203 Oberaudorf West Germany Phone: (08033) 342	Circular polarizing filters
Norbex Division Griffith Plastics Corporation 1027 California Drive Burlingame, California 94010 Phone: (415) 344-7691	DIGIBEZEL®; Plastic bezels for LED displays
Industrial Electronic Engineers, Inc. 7720-40 Lemona Avenue Van Nuys, California 91405 Phone: (213) 787-0311	Plastic bezels for .30 inch (7,62mm) tall LED displays
Rochester Digital Displays, Inc. 120 North Main Street Fairport, New York 14450 Phone: (716) 223-6855	Complete mounting kits for H.P. 5082-7300, -7700 and -7600 displays.

Table 3. Specific Wavelength Filter Products

Filter Product	Type of LED Display	Ambient Lighting
Panelgraphic Chromafilter® With Anti-Reflection		
Ruby Red 60 Dark Red 63	Standard Red	Moderate Bright
Scarlet Red 65	High-Efficiency Red	Moderate
Yellow 27	Yellow	Moderate
Green 48	Green	Moderate
Gray 10	All Colors	Sunlight
SGL Homalite, Grade 100		
H100-1605	Standard Red	Moderate
H100-1670	High-Efficiency Red	Moderate
H100-1726 H100-1720	Yellow	Dim Moderate
H100-1440 H100-1425	Green	Dim Moderate
H100-1266 Gray	All Colors	Sunlight
Anti-Reflection LR-72: 0.5 inch (12.70mm) Mounting Distance From Display LR-92: Up to 3.0 inch (76.20mm) Mounting Distance From Display		
Rohm & Haas		
Plexiglas 2423 Oroglas 2444	Standard Red	Moderate
3M Company — Visual Products Division Louvered Filters		
R6510	Standard Red	Indirect Sunlight
R6310	High-Efficiency Red	Indirect Sunlight
A5910	Yellow	Indirect Sunlight
G5610	Green	Indirect Sunlight
N0220 25% N.D. Gray	All Colors	Sunlight
Anti-Reflective Matte or Very Light Matte Front Surface Finish		
Glarecheq Spectrafilter		
110	High-Efficiency Red	Moderate
118 112	Standard Red	Moderate Bright
106	Yellow	Moderate
107	Green	Moderate
105	All Colors	Sunlight

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Fred W. Billmeyer, Jr., and Max Saltzman; Principles of Color Technology; Interscience Publishers, Division of John Wiley & Sons; New York; 1966.

J. Pucilowski, R. Schuman, and J. Velasquez; Contrast Enhancement of Light Emitting Diode Displays; Applied Optics, Volume 13, Number 10, October 1974; pp 2248-2252.

J.M. Ralston; Filter Considerations for Light Emitting Diode Displays; Proceeding of the SID; 3rd Quarter 1973; Volume 1413; pp 81-86.

M.R. Allyn, R.W. Dixon, and R.Z. Bachrach; Visibility of Red and Green Electroluminescent Diodes for Color-Anomalous Observers; Applied Optics, Volume 11, Number 11, November 1972; pp 2450-2454.

Application Note 945; Photometry of Red LED's; Hewlett-Packard; October 1973.

HEWLETT PACKARD

APPLICATION NOTE 966

Applications of the HP HDSP-2000 Alphanumeric Display

This note is intented to serve as a design and application guide for users of the HP HDSP-2000 alphanumeric display device. The information presented will cover: the theory of the device design and operation; considerations for specific circuit designs; thermal management, power derating, and heat sinking; and intensity modulation techniques.

The HP HDSP-2000 device has been designed to provide a high resolution information display subsystem. Each character of the 4 character package consists of a 5x7 array of LEDs which can display a full range of alphabetic and numeric characters plus punctuation, mathematical and other special symbols.

Each character is 3.8mm high by 2.2mm wide with 4.5mm center to center spacing. The overall package size is designed to allow end stacking of multiple clusters to form character strings of any desired length.

ELECTRICAL DESCRIPTION

The on-board electronics of the HP HDSP-2000 display will eliminate some of the classical difficulties associated with the use of alphanumeric displays. Traditionally, single digit LED dot matrix displays have been organized in an x-y addressable array requiring 12 interconnect pins per digit plus extensive row and column drive support electronics. The HP HDSP-2000 provides on-board storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4 character display. This approach allows the user to address each display package through just 11 active interconnections vs. the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Figure 1 is a block diagram of the internal circuitry of the HP HDSP-2000 display. The device consists of four LED matrices and two 14-bit serial-in-parallel-out shift registers. The LED matrix for each character is a 5x7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. The 7 row cathode commons of each character are tied to the constant current sinking outputs of 7 successive stages of the shift register. The like columns of the 4 characters are tied together and brought to a single address pin (i.e., column 1 of all 4 characters is tied to pin 1, etc.). In this way, any diode in the four 5x7 matrices may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

The serial-in-parallel-out (SIPO) shift register has a constant current sinking output associated with each shift register stage. The output stage is a current mirror design with a nominal current gain of 10. The current to the reference diode is established from the output voltage of the brightness input buffer applied across the current reference resistors, R. The reference current flow is controlled by a switching transistor tied to the output of the associated shift register stage. A logical 1 loaded into the shift register will turn the current source "ON" thereby sinking current from the row line. A voltage applied to the appropriate column input will then turn "ON" the desired diode.

Data is loaded serially into the shift register on the high to low transition of the clock line. The data output terminal is a TTL buffer interface to the 28th bit of the shift register (i.e., the 7th row of character 4 in each package). The Data Output is arranged to directly interconnect to the Data Input on a succeeding 4 digit HP HDSP-2000 display package. The Data, Clock and V_B inputs are all buffered to allow direct interface to any TTL or DTL logic family.

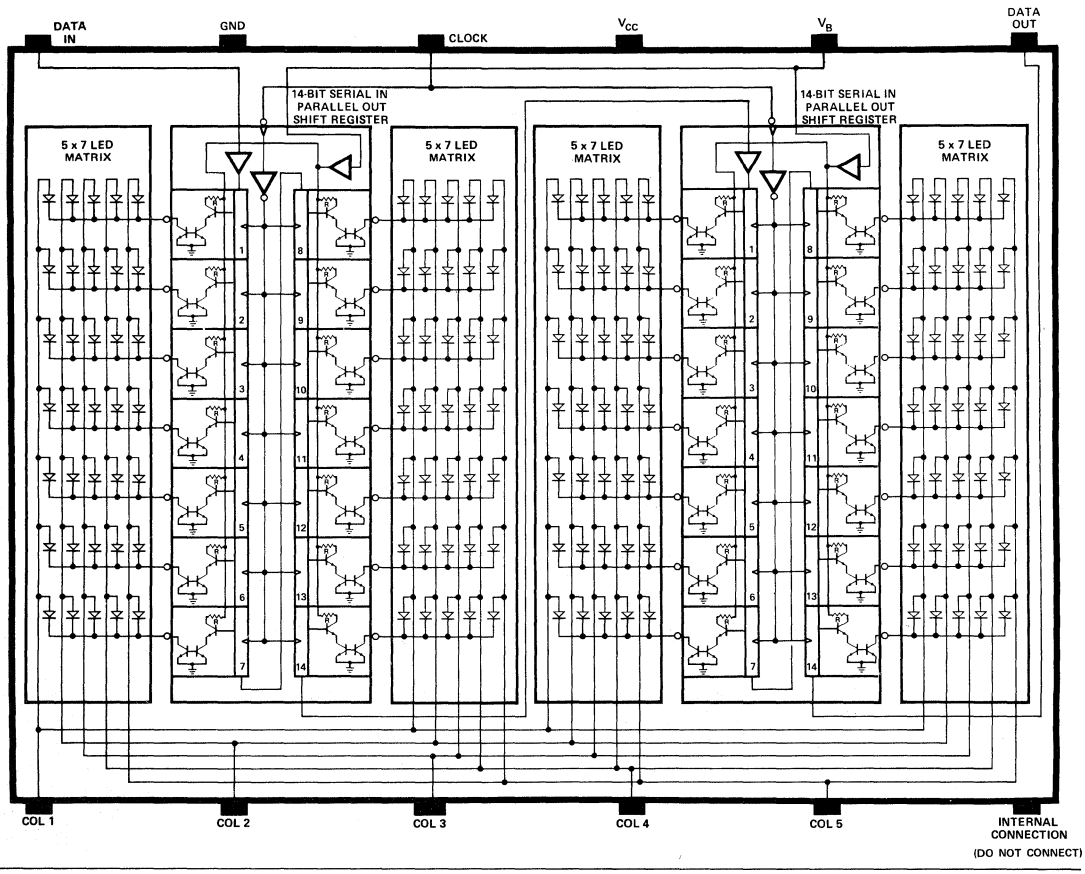


Figure 1. Block Diagram of the HDSP-2000.

THEORY OF OPERATION

Dot matrix aplhanumeric display systems generally have a logical organization which prescribes that any character be generated as a combination of several subsets of data. In a 5x7 matrix, this could be either 5 subsets of 7 bits each or 7 subsets of 5 bits each. This technique is utilized to reduce from 35 to 5 or 7 the number of outputs required from the character generator. In order to display a complete character, these subsets of data are then presented sequentially to the appropriate locations of the display matrix. If this process is repeated at a rate which insures that each of the appropriate matrix locations is re-energized, a minimum of 100 times per second, the eye will perceive a continuous image of the entire character. The apparent intensity of each of the display elements will be equal to the intensity of that element during the "ON" period multiplied by the ratio of "ON" time to refresh period. This ratio is referred to as the display duty factor, and the technique is referred to as "strobing". In the case of the HP HDSP-2000, each character is made up of 5 subsets of 7 bits. For a four character display, 28 bits representing the first subset of each of the four characters are loaded serially into the on-board SIPO shift register and the first column is then energized for a period of time, T. This process is then repeated for columns 2 through 5.

If the time required to load the 28 bits into the SIPO shift register is t, then the duty factor is:

$$D.F. = \frac{T}{5(t+T)} \; ; \qquad (1)$$

the term 5(t+T) is then the refresh period. For a satisfactory display, the refresh period should be:

$$1/[5(t+T)] \geqslant 100 \text{ Hz} \qquad (2)$$

or conversely

$$5(t+T) \leqslant 10 \text{ msec}, \qquad (3)$$

which gives

$$(t+T) \leqslant 2 \text{ msec}. \qquad (4)$$

Two milliseconds then is the maximum time period which should be allowed for loading and display of each column location. For $t \ll T$, the duty factor will approach 20%. The number of digits which can be addressed in a single string is then dependent upon the minimum acceptable duty factor and the choice of clock rate. For instance, at 1 MHz clock rate, a 100 character string of 25 packages could be operated at a duty factor of

$$D.F. = \frac{(T+t) - (\text{No. of bits to be loaded}) \times (1/1\ \text{MHz})}{5(T+t)}$$

$$= \frac{(2\ \text{msec}) - (700)\ (1\mu\text{sec})}{5 \times 2\ \text{msec}} = 13\%$$

For most applications, a duty factor of 10% or greater will provide more than satisfactory display intensity. In brightly illuminated ambient environments, a higher duty factor may be desirable whereas, in dim ambient situations, the duty factor may have to be reduced in order to provide a display with satisfactory contrast.

DRIVE CIRCUIT CONCEPTS

A practical display system utilizing the HP HDSP-2000 display requires interfacing with a character generator and refresh memory. A block diagram of such a display system is depicted in Figure 2. In explanation, assume that this system is for a four character display. Therefore, the 1/N counter becomes a 1/4 counter where N is equal to the number of characters in the string. The refresh memory is utilized to store the information to be displayed. Information can be coded in any one of several different standard data codes, such as ASCII or EBDIC, or the code and the display font can be customized through the use of a custom coded ROM. The only requirement is the output data be generated as 5 subsets of 7 bits each. The character generator receives data from the refresh memory and outputs 7 display data bits corresponding to the character and the column select data input. This data is converted to serial format in the parallel to serial shift register for clocking into the HP HDSP-2000 display shift register. In the typical system, the right most character to be displayed is selected first and the data corresponding to the ON and OFF display elements in the fist column is clocked into the first 7 shift register locations of the HP HDSP-2000. In a similar manner, column 1 data for characters 3, 2, and 1 is selected by the 1/N counter, decoded and shifted into the display shift register. After 28 clock counts, data for each character is located in the HP HDSP-2000 shift register locations which are associated with the 7 rows of the appropriate LED matrix. The 1/N counter overflows, triggering the display time counter, enabling the output of the 1/5 column select decoder and disabling the clock input to the HP HDSP-2000. The information now present in the shift registers will be displayed for a period, T, at the column 1 location. At the end of the display period, T, the divide by 5 counter which provides column select data for both the HP HDSP-2000 and the character generator is incremented one count and column 2 data is then loaded and displayed in the same manner as column 1. This process is repeated for each of the 5 columns which comprise the 5 subsets of data necessary to display the desired characters. After the fifth count, the 1/5 decoder automatically resets to one and the sequence is repeated. The only changes required to extend this interface to character strings of more than 4 digits are to increase the size of the refresh memory and to change the divide by four counter to a modulus equal to the number of digits in the desired string.

Since data is loaded for all of the like columns in the display string and these columns are then enabled simultaneously, only five column switch transistors are required regardless of the number of characters in the string. The column switch transistors should be selected to handle approxmately 110mA per character in the display string. The collector emitter saturation voltage characteristics and column voltage supply should be chosen to provide a $2.6V \leqslant V_{COL} \leqslant V_{CC}$. To save on power

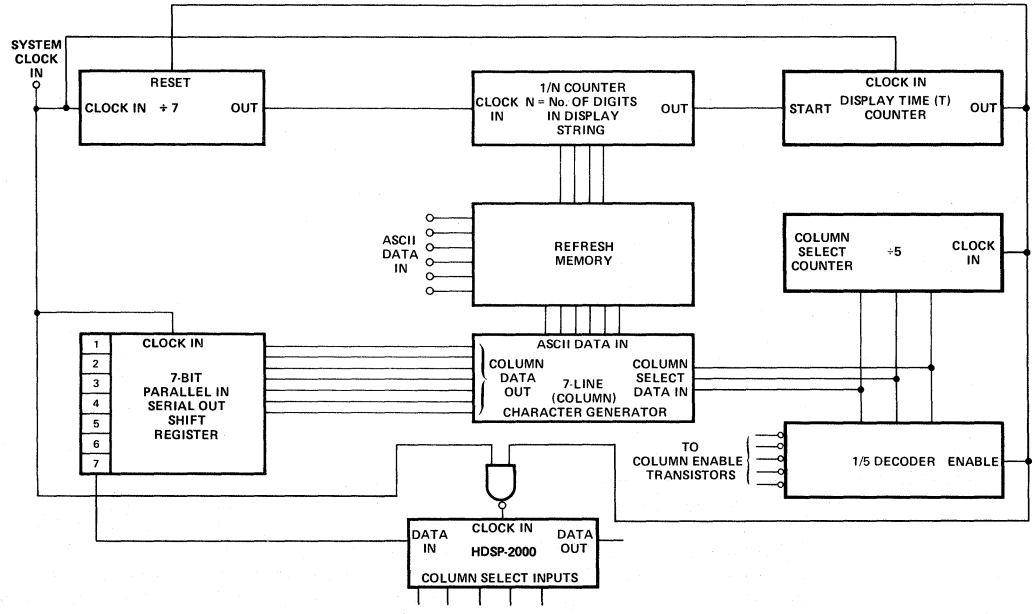


Figure 2. Block Diagram of a Basic Display System.

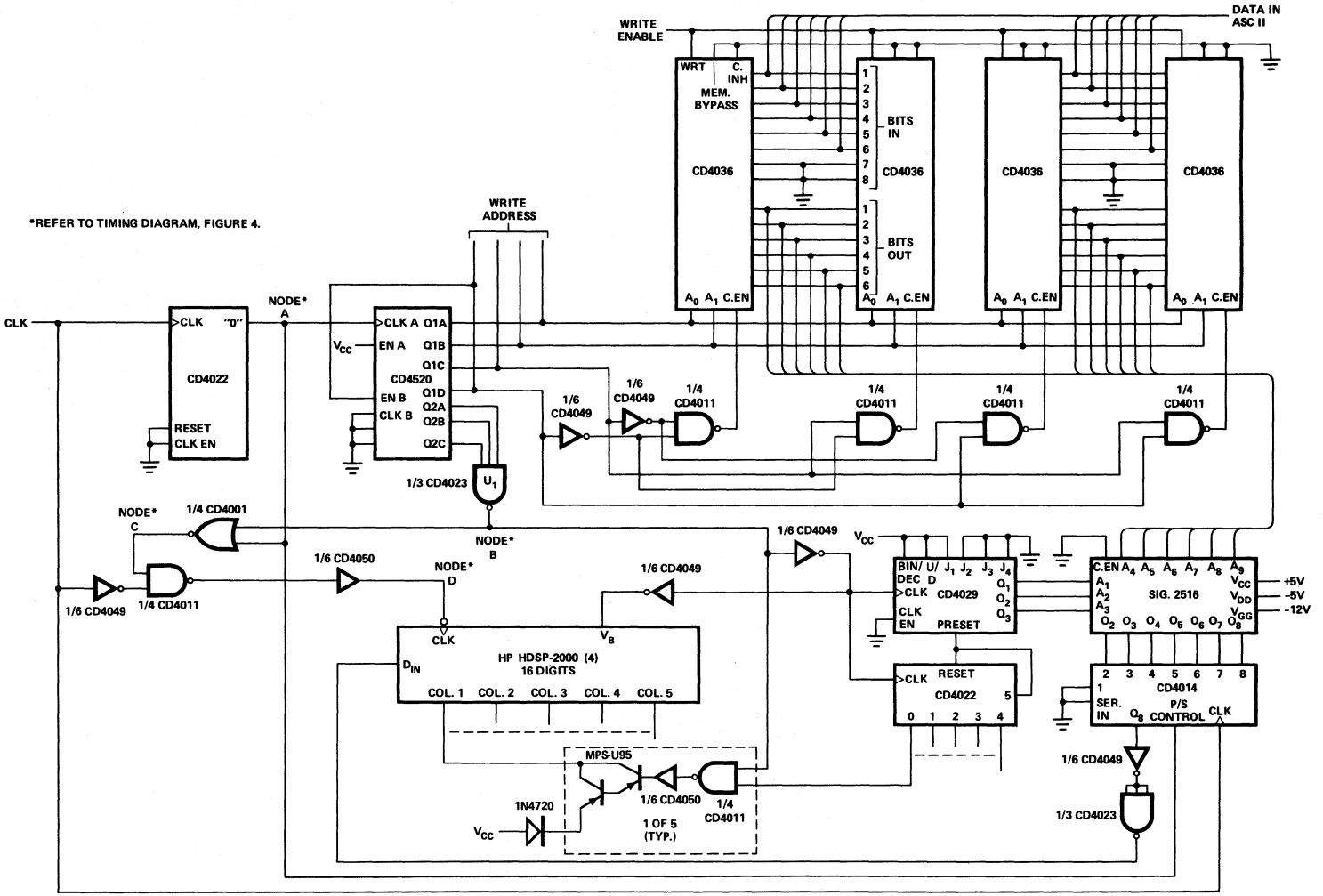


Figure 3. 16 Character CMOS Logic Interface to the HP HDSP-2000.

supply costs and improve efficiency, this supply may be a fullwave rectified unregulated DC voltage as long as the PEAK value does not exceed the value of V_{CC} and the minimum value does not drop below 2.6 volts.

Since large current transients can occur if a column line is enabled during data shifting operations, the most satisfactory operation will be achieved if the column current is switched off before clocking begins. I_{CC} will be reduced by about 10-15% if the clock is held in the logical 1 state during the display period, T.

INTERFACE CIRCUITS FOR THE HP HDSP-2000

There are many possible practical techniques for interfacing to the HP HDSP-2000 alphanumeric display. Three basic approaches will be treated here.

Instrumentation Interface Circuit

The circuit shown in Figure 3 is for a 16 character display and is designed to function primarily as a readout for general instrumentation systems. CMOS logic circuitry is utilized in this design, however, it should be a simple exercise to substitute TTL functions if CMOS is not desired. In this circuit, a CD4022 and CD4520 are combined to perform the functions of the divide by 7, divide by 16 (1/N) and display time counters as depicted in Figure 2. The timing diagram, Figure 4, demonstrates the relationship of the various critical outputs and inputs. The CD4022 actually acts here as a divide by 8 counter with the first count used to latch data into the parallel-in-serial-out (PISO) shift register and the other 7 counts shifting data out of the PISO and into the HP HDSP-2000. The CD4520 is a dual 4 bit counter wired as an 8 bit binary ripple counter. The NAND gate, U_1, establishes the ratio of loading time to display time. In this case, loading will occur once in every 8×2^7 clock counts for a period of 8×2^4 clock counts. Duty factor is then from (1)

$$\text{D.F.} = \frac{(8 \times 2^7) - (8 \times 2^4)}{5\,(8 \times 2^7)} = 17.5\% \quad (1)$$

and the refresh period is

$$5\,(8 \times 2^7)\,\tau,$$

where τ = clock period.

The four least significant bits of the CD4520 counter are used to continually address the CD4036 refresh memory. Data can be written into the desired memory address by strobing the WRITE ENABLE line when the appropriate memory address appears on the WRITE ADDRESS lines. This function can occur simultaneously with a read from memory.

Two counters, a CD4029 and a CD4022, are used for the column data generator and the column select decoder, respectively. Note that the Signetics 2516 character generator requires column select inputs of binary codes 1 to 5 instead of binary 0 to 4. For this reason, the CD4029 is preset to a binary 1 by the same pulse which is used to reset the CD4022 column select decoder. To minimize I_{CC}, the V_B terminal is held low during data load operations, turning "OFF" the current mirror reference current. The column current switch is a PNP Darlington transistor driven from a buffered NAND gate. The 1N4720 serves to reduce the column voltage by approximately 1 volt, thereby reducing on board power dissipation in the HP HDSP-2000 devices. Due to maximum clock rate limitations of the CMOS logic, clock input should not exceed 1 MHz.

32 Character Keyboard Interface Circuit

The circuit shown in Figure 5 will directly interface the HP HDSP-2000 display to most standard keyboards. Interfac-

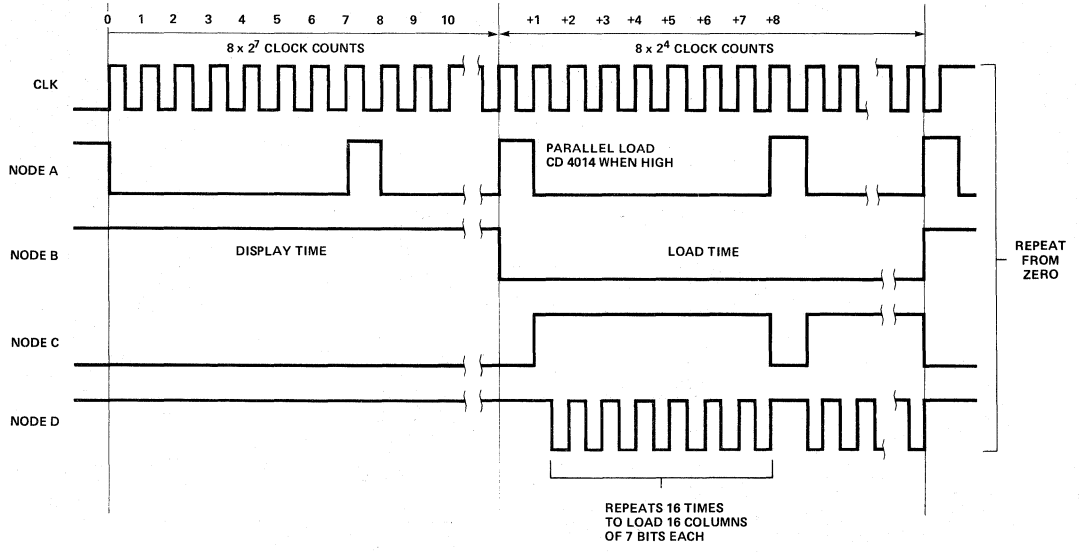


Figure 4. Timing Diagram for Display Interface.

ing to a keyboard without a "smart" system to generate some of the special functions required can result in some unique problems which must be considered. This system provides the following special features:

- Provides a cursor to indicate the position in the line of the next character to be entered.
- Blanks all data to the right of the cursor in the display.
- Provides for external display blanking and intensity control.
- Implements "Return" and "Backspace" functions.

The timing and data scan portions of this circuit are similar to those of the circuit shown in Figure 3 and will not be reviewed in detail. These portions of the circuit are enclosed in the dashed line. The major addition to the circuit which allows simple implementation of the special functions is a position counter and comparator. The position counter is an up-down counter which is preset to n-1 (n = number of characters in the display string) by "RETURN". The counter is decremented for each keystroke representing a valid display character and incremented for a "BACKSPACE" input code. A Fairchild 9324 five bit comparator compares the position counter output to the memory scan address. The memory scan begins at zero and represents the data for the right most (32nd) character in the display. The position count is indicative of the number of character keystrokes which have decremented the position counter from 31. The comparator senses two conditions of the relative values of the two counters. For memory scan equal to position count, the A=B output of the comparator will be a logical "1". For all other conditions of the two counters, A=B is a logical "0". This signal is inverted and is used to gate data from the PISO via U_1 into the HP HDSP-2000. For the condition A=B, the gating input is a logical "0" and the output of NAND gate U_2 is therefore held at a logical "1". This will cause all of the diodes associated with the character position A=B to be illuminated, thus forming the "cursor". The second condition which is sensed by the comparator is for a memory scan count less than position count, (A>B). This condition represents all character data to the right of the cursor and results in a logical "1" at the "A>B" output of the comparator. It is normally desirable for these characters to blank, hence a logical "0" should be loaded into the corresponding HP HDSP-2000 shift register locations. This is implemented by inverting the "A>B" output and applying the resulting signal to one input of NAND gate, U_1. For "A>B" at a logical "1", the output of U_1 will be a logical "1". This signal will then be inverted by U_2, causing logical "0" data to be loaded into the HP HDSP-2000 shift register for all characters to the right of the cursor. For "A=B" and "A<B", U_1 will pass inverted data from the PISO to U_2. These comparator signals are also used to control the loading of data into the proper refresh memory location. Keyboard data is initially stored in the 7475 D latches using the keyboard "STROBE" signal to trigger a one shot clock pulse from U_3. This pulse triggers a second one shot, U_4, which gates a "SET" signal to the load control flip flops, U_5 and U_6, for any valid character code. This arms the load control so that a write enable pulse will be sent to the 7489 RAM as soon as "A=B". The "$\overline{A=B}$" signal is used to prevent a second data entry from occurring during the middle of a write pulse. The write pulse also clears the load control flip-flops on the next clock cycle so that a new arriving signal can be recognized. The $\overline{Q}$ output of U_5 is also used to decrement the position counter.

The other special functions which are added to the circuit of Figure 3 are an intensity control and a blanking input. Intensity control is realized through the 74122 retriggerable monostable multivibrator, U_7. This circuit controls the time that the column select decoder is enabled during the display time, T. The display is externally blanked by holding the "RESET" input of the column select counter at a logical "0".

The circuit shown in Figure 5 is also convenient for use in instrumentation and computer readouts. In this situation, a "Busy" signal composed of $\overline{Q}$-U_2, $\overline{Q}$-U_3 and $\overline{Q}$-U_4 will allow the display interface to indicate to the driving system when data can be accepted.

Remote Display-Interface

In many systems, it is desirable to display data at multiple remote locations without having to provide the relatively complex and expensive decoding and timing scheme depicted in the previous two examples. This type of application may most often be utilized in paging system readouts, remote message displays and other systems where multiple displays would be addressed from a single central processor. The circuit shown in Figure 6 is designed to store and display a string of decoded data. The circuit requires data input from a system which can generate and serially output display and column select data — for instance, a minicomputer or microprocessor. The total number of bits of storage required (including the HP HDSP-2000 and the 5 bit column select shift register) is:

$$\text{Storage} = 35\,N + 25. \qquad (5)$$

where N = the number of characters in the display string.

The data input format should be divided into 5 equal subsets of information. Each subset should contain all of the data required to completely load the HP HDSP-2000 display string shift register (7N bits) for a given column, preceeded by a 5-bit column select code which will be shifted into the 5-bit SIPO at the HP HDSP-2000 output. The circuit has been designed to operate from two different clocks. This is important in systems where the display may be radio link addressed with the DATA ENTRY CLOCK being reconstituted from the data stream. For loading, $\overline{\text{LOAD DATA}}$ is taken low and loading can commence after $\overline{\text{READY}}$ goes low. Data is entered into the shift register through a gated input. The data string must contain the proper number of bits as defined by (5) and should be loaded in the shift register with one of the 5-bit column select codes loaded fully in the column select SIPO shift register. After loading is complete, $\overline{\text{LOAD DATA}}$ is returned high and clocking will be controlled by the DISPLAY CLOCK. The display clocking is designed to shift the stored data by 7N + 5 bits and then stop and display the shift-register contents for a period of time, T, as defined by the period of the one shot, U_1. U_1 is triggered when the clock line goes low after the synchronous counter has counted to 7N + 5. The output of U_1 resets the counter and disables the counting until the end of the period, T. The D flip-flop, U_2, insures that clock pulses to

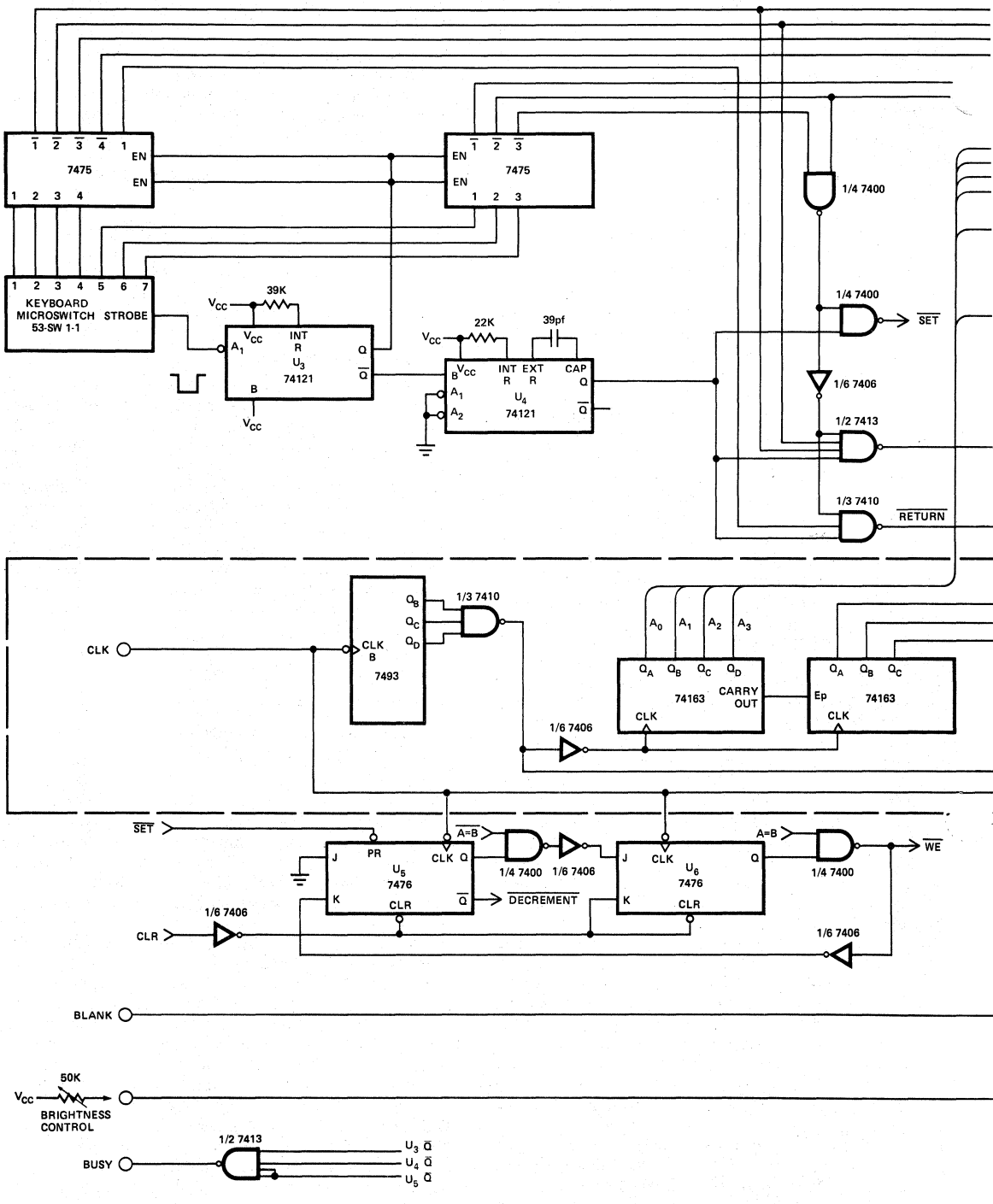
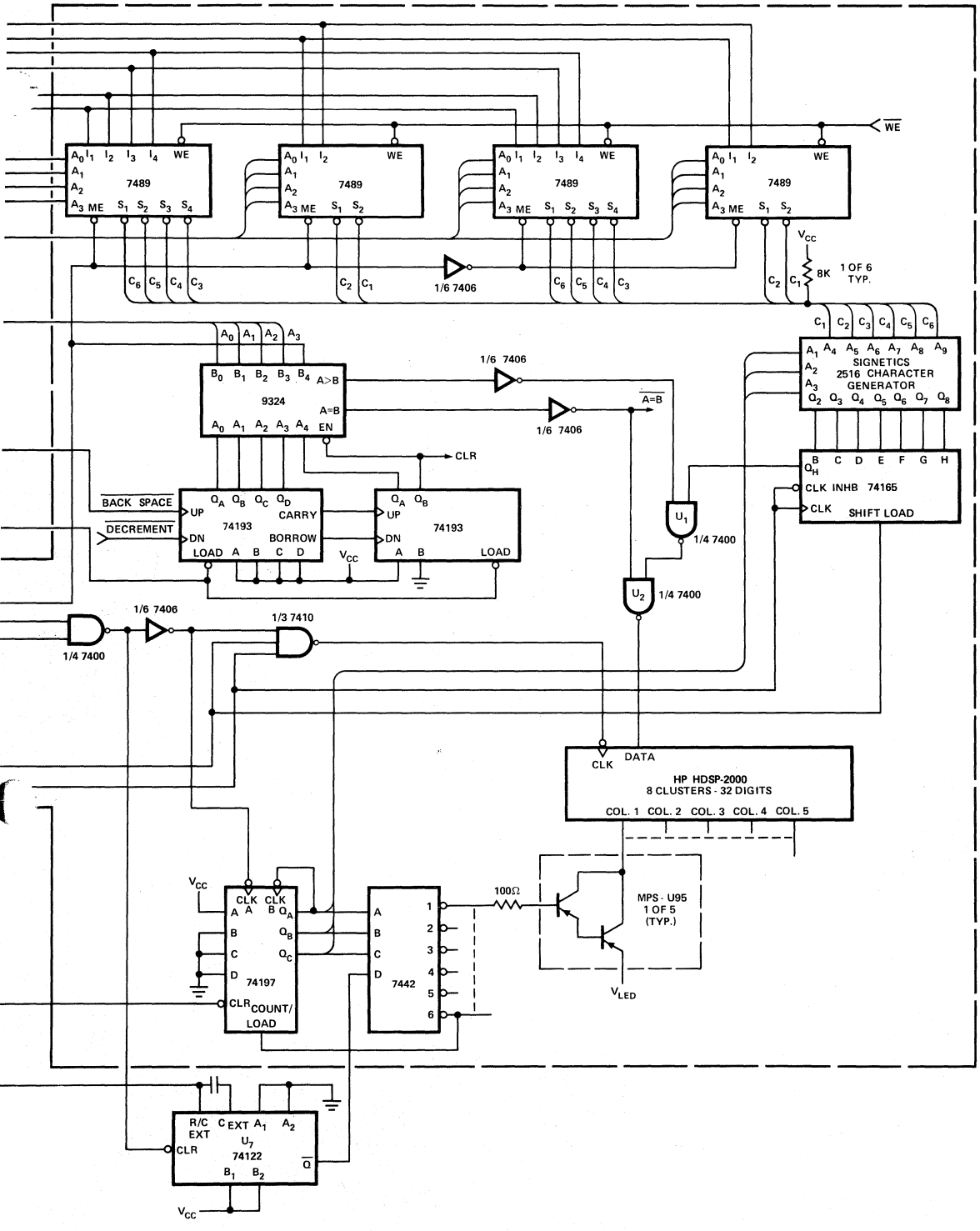


Figure 5. 32 Character Keyboard Interface Circuit.


7489
WE
1/6 7406
8K 1 OF 6 TYP.
9324
A=B
CLR
BACK SPACE
DECREMENT
74193
UP
DN
CARRY
BORROW
LOAD
1/4 7400
1/6 7406
1/3 7410
SIGNETICS
2516 CHARACTER
GENERATOR
CLK INHB 74165
SHIFT LOAD
DATA
CLK
HP HDSP-2000
8 CLUSTERS - 32 DIGITS
COL. 1 COL. 2 COL. 3 COL. 4 COL. 5
74197
COUNT/
LOAD
7442
100Ω
MPS - U95
1 OF 5
(TYP.)
74122
R/C EXT
EXT
CLR

the shift registers always start synchronous with the beginning of a full clock cycle so that erroneous clocking will not occur. U_3 is utilized to give intensity control for the HP HDSP-2000, if desired. It can be overridden by connecting the $U_{4(1-5)}$ input to the Q output of U_1 instead of U_3.

The shift register memory utilized in this circuit is only one of several forms of memory which could be chosen. Another possibility would be the use of a 512 x 1 bit or 1024 x 1 bit RAM. The counter outputs would then be used to select the RAM address.

POWER DISSIPATION/JUNCTION TEMPERATURE CALCULATIONS

The HP HDSP-2000 combines a significant amount of logic and display capability in a very small package. As such, on board power dissipation is relatively high and thermal design of the display mounting becomes an important consideration. The HP HDSP-2000 is designed to permit operation over a wide range of temperature and supply voltages. Full power operation at $T_A = 25°C$ (with $V_{CC} = V_B = V_{COL} = 5.25V$) is acceptable if the thermal resistance from pins to ambient, θ_{CA}, is no greater than 35°C/watt/cluster. This value assumes that the mounting surface of the display becomes an isothermal plane. If only one display is operated on this isothermal plane at 1.7 watts maximum, then the temperature raise above ambient is:

$$T_{RISE} = [35°C/watt] \times 1.7 \text{ watts} = 42.5°C. \quad (6)$$

If a second display is placed on this same thermal plane, with no increase in thermal dissipation capability the temperature would be doubled (i.e., 85°C) — reaching catastrophic levels very quickly. However, in most applications maximum achievable power dissipation is considerably less than the maximum allowable package dissipation of 1.7W. Calculation of power dissipation in the HP HDSP-2000 can be made using the following formula:

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) \quad (7)$$

where

$$P(I_{CC}) = I_{CC} (V_B = 0.4V) \times V_{CC} \quad (8)$$

$$P(I_{REF}) = [I_{CC} (V_B = 2.4V) - I_{CC} (V_B = 0.4V)] \times V_{CC} \times (n/35) \times 5 \times D.F. \quad (9)$$

$$P(I_{COL}) = I_{COL} \times V_{COL} \times (n/35) \times 5 \times D.F. \quad (10)$$

where

I_{CC} is measured with all S.R. stages equal to logical 1.
n = average number of diodes illuminated per character.
D.F. = Column On Time from equation (1) or the Column On Time due to pulse width modulation of V_B, whichever is lower.

As can be seen from formulas (8), (9) and (10), there are several techniques by which total power dissipation can be derated:

- Lower V_{CC} to minimum
- Lower V_{COL} to minimum
- Lower D.F.

Maximum and typical power dissipation can be calculated from the maximum and typical values of I_{CC} and I_{COL} published in the HP HDSP-2000 data sheet. While it is possible to operate the columns of the HDSP-2000 display using fullwave rectified unregulated DC, lower power dissipation can be achieved by using the regulated V_{CC} supply. Then, V_{COL} is equal to V_{CC} minus the collector to emitter saturation voltage across the column switching

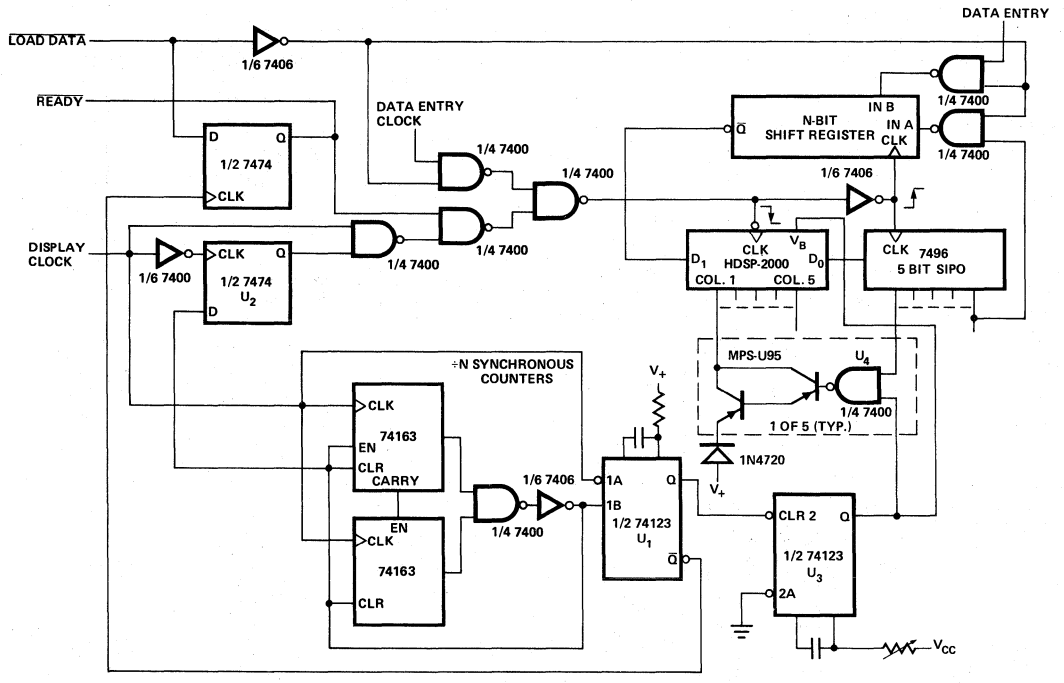


Figure 6. Display Interface Designed to Accept Decoded Data.

transistors. Since the minimum recommended V_{COL} is 2.6V, PNP Darlington transistors with a silicon diode in series with the emitter can be used to lower the power dissipation within the display. In most implementations of the ASCII character set the maximum number of diodes illuminated within a display character, n, is 21 while a typical character has 15 dots illuminated. While the maximum D.F. is 20%, in most applications D.F. $\leq$ 17.5% due to the required time to load the display. A D.F. of 17.5% represents a (7/8) ratio of display time to total time such as illustrated in the circuit shown in Figure 3. Many applications achieve a D.F. much lower than 17.5%. For example, the HDSP-2470 alphanumeric display system when configured for 40 characters has a D.F. of 11.6%.

As an example, the maximum power dissipation can be calculated for the circuit shown in Figure 3. In this circuit $V_{COL}(MAX)$ = 5.25V – 1.3V (MPS-U95 @ 1.6A) – .85V (1N4720 @ 1.6A) = 3.10V. Thus maximum achievable power dissipation can be calculated as shown below:

$$P(I_{CC}) = 60mA \times 5.25V = 315\ mW \quad (11)$$

$$P(I_{REF}) = (95mA - 60mA) \times 5.25V \times (21/35) \times 5 \times 0.175 = 96.5\ mW \quad (12)$$

$$P(I_{COL}) = 410mA \times 3.1V \times (21/35) \times 5 \times 0.175 = 667\ mW \quad (13)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 1079\ mW \quad (14)$$

Similarly, typical power dissipation can be calculated as:

$$P(I_{CC}) = 45mA \times 5.00V = 225\ mW \quad (15)$$

$$P(I_{REF}) = (73mA - 45mA) \times 5.00V \times (15/35) \times 5 \times 0.175 = 52.5\ mW \quad (16)$$

$$P(I_{COL}) = 335mA \times (5.00V - 1.3V - .85V) \times (15/35) \times 5 \times 0.175 = 358\ mW \quad (17)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 636\ mW \quad (18)$$

For operation at the maximum temperature of 70°C, it is important that the following criteria be met:

a. $T_{CASE} \leq 100°C$, where T_{CASE} = hottest pin temperature

b. $T_{IC\ JUNCTION} \leq 125°C$

Thermal resistance from junction to case, θ_{JC}, is typically 25°C/watt. Using these factors, it is possible to determine the required heat sink power dissipation capability and associated power derating through the following assumptions:

$$T_{IC\ JUNCTION} = (\theta_{CA} \times P_D) + \theta_{JC}\left(\frac{P_D - .015n}{2}\right) \quad (19)$$

$$T_{CASE} = (\theta_{CA})\ P_D \quad (20)$$

where $\left(\frac{P_D - .015n}{2}\right)$ is the power dissipated in each IC.

HEAT SINKING CONSIDERATIONS

In practice, heat sink design for the HP HDSP-2000 involves optimization of techniques to dissipate heat through the device leads. Figures 7 and 8 schematically depict two possible heat sink designs. In many applications, a maximum metalized printed circuit board such as shown in Figure 7 can provide adequate heat sinking for the HDSP-2000 display. For example, the HDSP-2416/-2424/-2432/-2440 display boards consist of

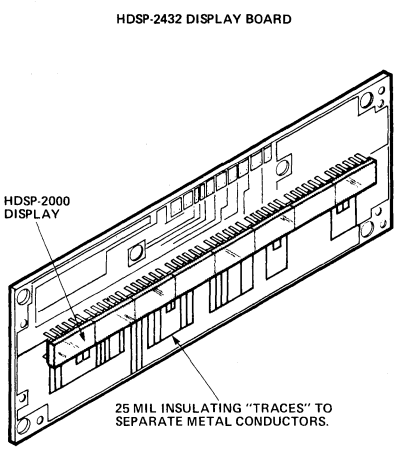


Figure 7. Maximum Metalized Printed Circuit for the HP HDSP-2000.

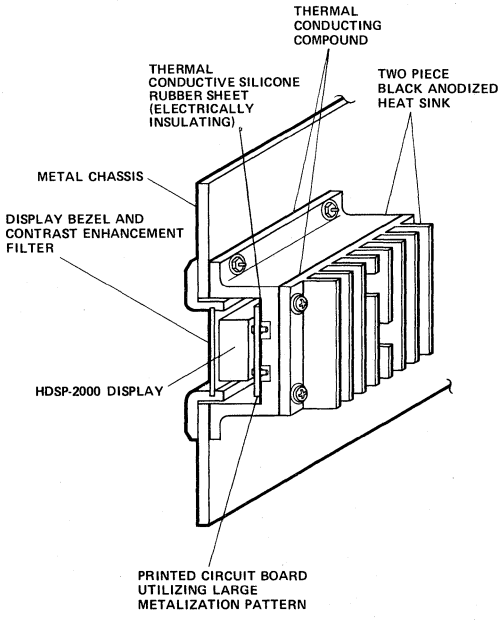


Figure 8. Two-Part Heat Sink for the HP HDSP-2000.

a 16, 24, 32 or 40 character HDSP-2000 display mounted on a maximum metalized printed circuit board. These display boards are designed for free air operation to 55°C and operation to 70°C with forced air cooling of 150 fpm normal to the component side of the board. A free air operating temperature of 70°C can be achieved by heat sinking the display. Figure 8 depicts a two part heat sink which can be assembled using two different extruded

parts. In this design, the vertical fins promote heat transfer due to naturally induced convection. Care should be taken to insure a good thermal path between the two portions of the heat sink. To optimize power handling capability, the metal heat transfer contact area between the PCB metalization and the heat sink should be maximized. A surface area of approximately 8 square inches per cluster will permit operation at 1.1 watts/cluster at the maximum operating temperature of 70°C ambient. The value of 1.1 watts/cluster is easily achieved by reduction of V_{COL} to 3 volts. Next to increasing total heat sink area, a provision for at least some forced air flow is probably the most effective means of improving heat transfer. Thermal design for the HP HDSP-2000 must be carefully considered as operation at excess temperatures can lead to premature failure.

The HP HDSP-2000 displays may also be mounted in standard DIP sockets which are cut down to accept the 6 pin devices in end-to-end strings. Another alternative for socket mounting is the stripline socket such as the Augat 325-AG1D or AMP 583773. These sockets will allow enough space bewteen the PCB and the HP HDSP-2000 to permit a heat sink bar to be inserted to conduct heat to an external sink. Most sockets add a thermal resistance of about 2°C/watt bewteen the device leads and the PCB.

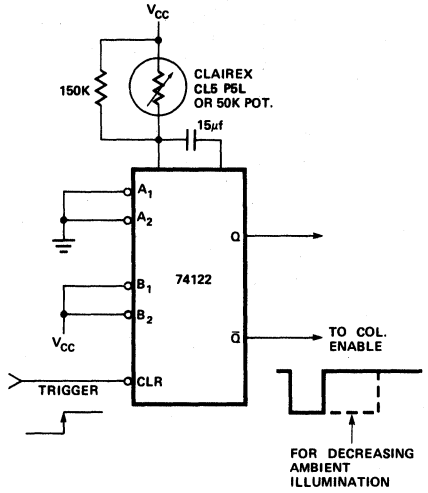


Figure 9. Intensity Modulation Control Using a One Shot Multivibrator.

DISPLAY INTENSITY MATCHING AND CONTROL

The luminous intensity of LED displays in general has a fairly wide dynamic range. If there is too great a difference between the luminous intensity of adjacent characters in the display string, the display will appear objectionable to the viewer. To solve the problem, the HP HDSP-2000 displays are categorized for luminous intensity. The category of each display package is indicated by a letter preceding the date code on the package. When assembling display strings, all packages in the string should have the same intensity category. This will insure satisfactory intensity matching of the characters. The HP HDSP-2000 displays are categorized in 8 overlapping intensity categories. All characters of all packages designated to be within a given letter category will fall within an intensity ratio of less than 2:1. For dot matrix displays, a character-to-character intensity ratio of 2:1 is not generally discernable to the human eye.

A more important consideration regarding display intensity is the control of the intensity with respect to the ambient lighting level. In dim ambients, a very bright display will produce very rapid viewer fatigue. Conversely, in bright ambient situations, a dim display will be difficult, if not impossible, to read and will also produce viewer fatigue and high error rates. For this reason, control of display intensity with respect to the environment ambient intensity is an important consideration. Figure 9 depicts a scheme which will automatically control display intensity as a function of ambient intensity. This circuit utilizes a resettable one shot multivibrator which is triggered by the column enable pulse. The duration of the multivibrator output is controlled by a photoconductor. At the end of a column enable pulse, the multivibrator is reset to insure that column current is off prior to the initiation of a new display shift register loading sequence. The output of this circuit is used to modulate either the V_B inputs of the HP HDSP-2000 displays or the column enable input circuitry. For maximum reduction in display power, both inputs should be modulated.

In the circuit shown in Figure 9, the photocell may be replaced by a 50K potentiometer to allow manual control of display intensity.

Contrast Enhancement

Another important consideration for optimum display appearance and readablity is the contrast between the display "ON" elements and the background. High contrast can be achieved by merely driving the highest possible power into the display. This, of course, is feasible in some situations as long as ambient lighting is not too intense and power dissipation is not a consideration. A much more practical technique is the use of an effective contrast enhancement filter material. The following materials, Panelgraphic Ruby Red 60 and Dark Red 63 or SGL Homalite H100-1605 and H100-1670 will all provide improved contrast for the HP HDSP-2000 display. Other good practices to enhance display contrast are to avoid PCB traces in the visible areas around the display and, if possible, the utilization of a black silk screen over the relatively light PCB areas around the display. The subject of contrast enhancement is treated in greater detail in HP Application Note 964. Microprocessor interfaces to the HDSP-2000 display are shown in HP Application Note 1001.

KEY POINTS REGARDING THE HP HDSP-2000:

- A logical "1" in the display shift register turns a corresponding LED "ON".
- Clocking occurs on the high to low transition of the clock input.
- A character generator which produces 7 bit "COLUMN" data should be utilized.
- The internal shift register is 28 bits in length.
- Each column should be refreshed at a minimum rate of 100 Hz.

The following is a list of commercially available character generators which can be used in conjunction with the HP HDSP-2000. These devices are all programmed to convert from ASCII input code to 5 sets of 7 bits each for a 5 x 7 display format. Any desired input-output coding can be utilized in custom programmed ROMs.

Manufacturer	Part Number	Typical Access Time	Required Power Supplies	Typical Power Dissipation
Texas Instruments	TMS 4100	500 nsec	±12V	450 mW
National	5241 ABL	700 nsec	±12V	
Signetics	2513	450 nsec	±5V −12V	290 mW
	2516	500 nsec	±5V −12V	280 mW
AMI	S8773B	450 nsec	+5V −12V	625 mW (max)
Mostek	2002 2302		±14V +5V −12V	320 mW 200 mW
Electronic Arrays	40105	750 nsec	±12V	430 mW
Fairchild	3257	500 nsec	+5V −12V	360 mW

Figure 10. Column Output Character Generators Suitable for Use with the HP HDSP-2000.

The refresh memory for the HP HDSP-2000 display can take any one of several different forms. The following table lists a few of the devices which the display system designer may find convenient.

Type	Organization
Bipolar RAM	Words x Bits
*7489	16 x 4
*7481A	16 x 1
*7484A	16 x 1
Fairchild 93403	16 x 4
Intel 3101	16 x 4
Intel 3104	4 x 4
MOS RAM	
TI TMS 4000 JC/NC	16 x 8
CMOS RAM	
RCA CD 4036	4 x 8
RCA CD 4039	4 x 8
National 74C89	16 x 4
Motorola MCM 4064	16 x 4
Shift Register	
TI TMS 3112	32 x 6
Signetics 2518	32 x 6
Signetics 2519	40 x 6
Fairchild 3348	32 x 6
Fairchild 3349	32 x 6

*Standard 7400 Series TTL logic parts available from most Integrated Circuits manufacturers.

Figure 11. Memory Elements Which can be Utilized in HDSP-2000 Display Systems.

HEWLETT PACKARD

APPLICATION NOTE 1000

Digital Data Transmission With the HP Fiber Optic System

Fiber optics can provide solutions to many data transmission system design problems. The purpose of this application note is to aid designers in obtaining optimal benefits from this relatively new technology. Following a brief review of the merits, as well as the limitations, of fiber optics relative to other media, there is a description of the optical, mechanical, and electrical fundamentals of fiber optic data transmission system design. How these fundamentals apply is seen in the detailed description of the Hewlett-Packard system. The remainder of the note deals with techniques recommended for operation and maintenance of the Hewlett-Packard system, with particular attention given to deriving maximum benefit from the unique features it provides.

ELECTRICAL WIRE VS. FIBER OPTICS

In fiber optic cables, the signals are transmitted in the form of energy packets (photons) which have no electrical charge. Consequently, it is physically impossible for high electric fields (lightning, high-voltage, etc.) or large magnetic fields (heavy electrical machinery, transformers, cyclotrons, etc.) to affect the transmission. Although there can be a slight leakage of flux from an optical fiber, shielding is easily done with an opaque jacket, so signal-bearing fibers cannot interfere with each other or with the most sensitive electric circuits, and the optically-transmitted information is, therefore, secure from external detection. In some applications, optical fibers carry signals large enough to be energetically useful (e.g., for photocoagulation) and potentially harmful, but in most data communication applications, economy dictates the use of flux levels of 100μW or less. Such levels are radiologically safe and in the event of a broken or damaged cable, the escaping flux is harmless in explosive environments where a spark from a broken wire could be disastrous. Jacketed fiber optic cables can tolerate more mechanical abuse (crush, impact, flexure) than electrical cables of comparable size; moreover, fiber optic cables have an enormous weight and size advantage — for equivalent information capacity. Properly cabled optical fibers can tolerate any kind of weather and can, without ill-effect, be immersed in most fluids, including polluted air and water.

Bandwidth considerations clearly give the advantage to fiber optics. In either parallel- or coaxial-wire cable, the bandwidth varies inversely as the square of the length, while in fiber optic cable it varies inversely as only the FIRST power of the length. Here are some typical values for length, ℓ , in metres:

(1) $f_{3dB} = \frac{12{,}000}{\ell}$ MHz for HFBR-3001 to 3005 cables

(2) $f_{3dB} = \frac{225{,}000}{\ell^2}$ MHz for typical 50Ω coax (RG-59)

For example, if ℓ = 100m, the 3dB frequency is only 22.5MHz for the coax cable, but for the fiber optic cable it is 120MHz.

The limitations of fiber optics arise mainly from the means for producing the optical flux and from flux losses. While the power into a wire cable can easily and inexpensively be made several watts, the flux into a fiber optic cable is typically much less than a milliwatt. Wire cable may have several signal "taps"; multiple taps on fiber optic cables are economically impractical at present.

The losses in a point-to-point fiber optic system are insertion loss at the input and output, connector loss, and transmission loss proportional to cable length. Variations in these losses require a receiver with a dynamic range capable of accommodating these variations and yet able to provide adequate BW (bandwidth) and SNR (signal-to noise) ratio at the lowest flux level. Fortunately, no noise is picked up by a fiber optic cable so the receiver SNR at any BW is limited only by the noise produced within the receiver.

Fiber optics is not the best solution to every data transmission problem; but where safety, security, durability, electrical isolation, noise immunity, size, weight, and bandwidth are paramount, it has a clear advantage over wire.

FIBER OPTIC FUNDAMENTALS

Flux coupled into an optical fiber is largely prevented from escaping through the wall by being re-directed toward the center of the fiber. The basis for such re-direction is the index of refraction, n_1, of the core relative to the index of refraction, n_2, of the cladding.

Index of refraction is defined as the ratio of the velocity of light in a given medium to the velocity of light in a vacuum.

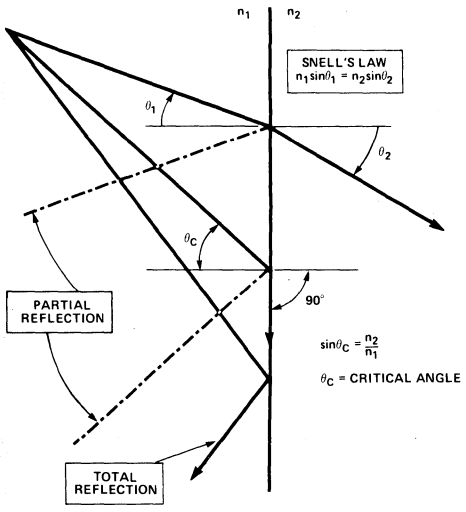


Figure 1. Snell's Law.

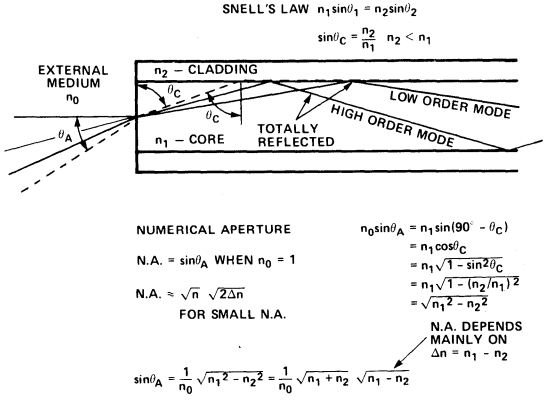


Figure 2. Total Internal Reflection.

As a ray of light passes from one medium into another of a different index of refraction, the direction changes according to Snell's Law:

(3) $n_1 \sin\theta_1 = n_2 \sin\theta_2$ **SNELL'S LAW**

This is illustrated in Figure 1. Notice that the relationship between the angles is the same, whether the ray is incident from the high-index side (n_1) or low-index side (n_2). For rays incident from the high-index side, there is a particular incidence angle for which the exit angle is ninety degrees. This is called the critical angle. At incidence angles less than the critical angle, there is only a partial reflection, but for angles greater than the critical angle, the ray is totally reflected. This phenomenon is called TOTAL INTERNAL REFLECTION (TIR).

Numerical Aperture.

Rays within the core of an optical fiber may be incident at various angles, but TIR applies only to those rays which are incident at angles greater than the critical angle. TIR prevents these rays from leaving the core until they reach the far end of the fiber. Figure 2 shows how the reflection angle at the core/cladding interface is related to the angle at which a ray enters the face of the fiber. The acceptance angle, θ_A, is the maximum angle, with respect to the fiber axis, at which an entering ray will experience TIR. With respect to the index of refraction, n_0, of the external medium, the acceptance angle is related to the indices of refraction of the core and cladding. When the external medium is air ($n_0 \approx 1$), the sine of the acceptance angle is called the NUMERICAL APERTURE (N.A.) of the fiber:

(4) NUMERICAL APERTURE, N.A. = $\sin\theta_A$

The derivation in Figure 2 applies only to meridional rays, i.e., rays passing through the axis of the fiber; skew rays (non-meridional) can also be transmitted, and these account for the observation that the reception and radiation patterns of optical fibers are not perfect step functions at the acceptance angle. For this reason, the practical definition of N.A. is somewhat arbitrary.

Modes of Propagation

Within the limits imposed by the N.A., rays may propagate at various angles. Those propagating at small angles with respect to the fiber axis are called LOW-ORDER MODES, and those propagating at larger angles are called HIGH-ORDER MODES. These modes do not exist as a continuum. At any given wavelength, there are a number of discrete angles where propagation occurs. SINGLE-MODE fibers result when the core area and the N.A. are so small that only one mode can propagate.

In addition to high- and low-order modes, there are others, called LEAKY MODES, which are trapped as skew rays — partly in the core, but mostly in the cladding where they are called CLADDING MODES. As implied by the term, leaky modes do not propagate as well as the more nearly meridional modes; their persistence, depending mainly on the structure of the optical fiber, ranges from less than a metre to more than fifty metres. The presence of leaky modes will, of course, affect the results obtained in measurement of N.A. and transmission loss, making them both artificially high. For this reason, N.A. is usually specified in terms of the EXIT N.A. for a fiber of length adequate to assure that leaky modes have effectively disappeared.

Since most leaky mode propagation is in the cladding, it can be "stripped." Such cladding mode stripping is done by surrounding the unjacketed fiber with a material having a refractive index higher than that of the cladding. EXIT N.A. is defined as the sine of the angle at which the radiation pattern (relative intensity vs. off-axis angle) has a particular value. This value is usually taken at 10% of the axial (maximum) value.

Transmission Loss

Regular core (non-leaky) modes also exhibit transmission losses. These are due to (1) scattering by foreign matter, (2) molecular (material) absorption, (3) irregularities at the core/cladding interface, and (4) microbending of the optical fiber by the cable structure. The first two loss mechanisms depend on the length of path taken by a ray; the third depends on the number of reflections of the ray before it emerges. It is clear from Figure 2 that the higher order modes have longer paths and more reflections with consequently higher loss. Larger N.A. fibers permit higher-order-mode propagation and, therefore, exhibit generally a higher transmission loss. Transmission loss is exponential and is, therefore, usually expressed in "dB per km." Coupling loss consideration usually favors larger N.A.

The three main loss mechanisms for coupling between fibers or between fibers and the optical ports of other devices are: (1) relative N.A.'s, (2) relative area of the optical ports, and (3) Fresnel (reflection) loss. In addition to these, there may be coupling loss due to misalignment and/or separation of optical ports. Relative N.A. loss can be ignored (≈ zero dB) whenever the N.A. of the receiving port (fiber or detector) is larger than the N.A. of the source port (flux generator or fiber), otherwise:

$$(5)\ \text{N.A. LOSS (dB)} = 20 \log \frac{\text{N.A. of Source Port}}{\text{N.A. of Receiver Port}}$$

Relative area loss can be ignored whenever the area of the receiver port is larger than the area of the source port, otherwise:

$$(6)\ \text{AREA LOSS (dB)} = 20 \log \frac{\text{Diameter of Source}}{\text{Diameter of Receiver}}$$

In applying equation (6) to coupling between single fibers, the diameter to be used is the CORE DIAMETER. If the receiver port is a FIBER OPTIC BUNDLE, the "packing fraction" loss must be added to the area loss, even when the area of the bundle is larger than the area of the source port.

$$(7)\ \text{PACKING FRACTION LOSS (dB)} = 10 \log \frac{\text{Active Area}}{\text{Total Area}}$$

"Active area" is the sum of areas of the cores of individual fibers, and "total" area is that of the bundle.

Fresnel loss occurs when a ray passes from one medium to another having a different index of refraction. Part of the flux is reflected; the fraction transmitted is described by the transmittance, τ, so the loss is:

$$(8)\ \text{FRESNEL LOSS (dB)} = 10 \log \frac{1}{\tau} = 10 \log \frac{2 + \frac{n_x}{n_y} + \frac{n_y}{n_x}}{4}$$

n_x = index of refraction of medium x
n_y = index of refraction of medium y

It is clear from equation (8) that the loss is the same in either direction. If two fibers are joined with an air gap between their faces, taking $n_x = 1$ for air and $n_y = 1.49$ for the cores of the fibers, the fiber-to-air Fresnel loss is 0.17dB. The air-to-fiber loss is the same, so the total airgap loss is 0.34dB. If several such connections are made, the loss could be high enough to make it worthwhile to use a coupling medium, such as silicone, to remove the air gap. Often, however, connector loss comes mainly from a gap deliberately inserted to prevent scratch damage to the fiber face and to reduce the variability of misalignment loss; i.e., it is sometimes more important to make the connector loss be consistent rather than low.

The use of a coupling medium is more significant when a fiber is coupled to an LED or IRED source. These sources are usually of gallium arsenide, or related substances, with a refractive index of 3.6. With such a high index of refraction, the use of an epoxy cement can reduce coupling loss by approximately 1dB. Figure 3 shows how the flux coupling is derived. If the size of the LED is much less than that of the fiber, a more effective technique is the use of a tiny lens over the LED. If the size of the fiber is smaller, the lens should be on the fiber, rather than the LED.

Rise Time Dispersion

Bandwidth limitation in fiber optics is the result of a phenomenon called DISPERSION, which is a composite of MATERIAL dispersion and MODAL dispersion. Both of these relate to the velocity of flux transmission in the core. Velocity varies inversely as the index of refraction, and if the index of refraction varies over the wavelength spectrum of the source, the flux having a wavelength at which the refractive index is lower will travel faster than the flux having a wavelength at which the index is higher. Thus, all portions of the spectrum of flux launched simultaneously will not arrive simultaneously, but will suffer time dispersion due to differences in travel time. This is MATERIAL DISPERSION. It is reduced by using sources of narrow spectrum (e.g., lasers) or fibers with a core index of refraction which is constant over the source spectrum.

In Figure 2, notice that rays moving parallel to the axis travel a path length which is shorter than that of rays which are not paraxial. Those rays propagating in the higher-order modes will, therefore, have a longer travel time than those in lower-order modes, and simultaneously launched rays will suffer dispersion of their arrival times. This is MODAL DISPERSION. It can be reduced only by reducing the N.A. (smaller acceptance angle) to allow only lower-order modes to propagate.

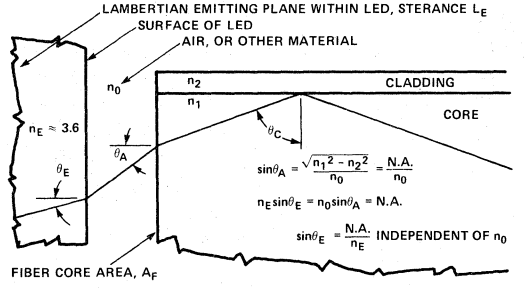


Figure 3. Acceptance Angle and Fresnel Loss Effects.

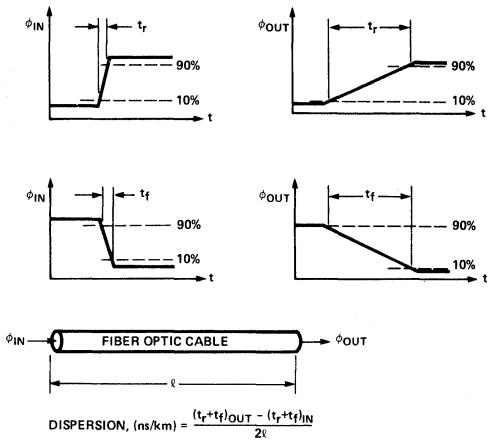


Figure 4. Rise Time Dispersion.

Whether the dispersion is material or modal (or both), it is measured, as shown in Figure 4, by applying positive and negative steps of flux and measuring the rise and fall times at the input and output of a fiber long enough to exhibit significant dispersion. Time dispersion is then defined as

(9) RISE TIME DISPERSION

$$\frac{\Delta t}{\ell}\ (\text{ns/km}) = \frac{1}{2\ell}\left[(t_r + t_f)_{OUT} - (t_r + t_f)_{IN}\right]$$

where ℓ is the length (in kilometres) of the fiber and t_r, t_f are the 10% to 90% rise and fall times.

Flux steps, rather than pulses, are used to avoid incorrect results that source or detector rise and fall times might introduce. Both polarities of step are recommended in order to compensate for non-linearity in either the source or the detector used.

Modulation frequency response of a fiber has a 6dB per octave roll-off, so the effect of rise time dispersion can also be described in terms of a length-bandwidth product:

(10) 3dB BANDWIDTH CONSTANT = $\Delta f \cdot \ell = 0.35\frac{\ell}{\Delta t}$

Construction of Fiber Optics

Fibers having a sharp boundary between core and cladding, as in Figure 2, are called STEP INDEX fibers. The reflection at the boundary is not a "zero-distance" phenomenon — the ray, in being reflected, is actually entering a minute distance into the cladding and there is some loss. This loss can be seen as a faint glow along the length of unjacketed lossy fibers carrying visible flux. To reduce such reflection loss, it is possible to make the rays turn less sharply by reducing the index of refraction gradually, rather than sharply, from core to cladding. A fiber of such a form is called a GRADED INDEX fiber and the rays propagate as shown in Figure 5. Graded index fiber has not only a very low transmission loss, but modal dispersion is also very low. Higher-order modes do travel longer paths, but in the off-axis, lower-index regions they travel faster so the travel time differential between high-order and low-order modes is not as large as it is in step index fibers.

Graded index fiber has higher coupling loss and may be more costly than step index fiber. It is, therefore, used mainly in applications requiring transmission over many kilometres at modulation bandwidths over 50MHz. For shorter distances and/or lower bandwidths, a variety of step index fibers are available at a variety of costs.

Figure 6 shows the construction of a Hewlett-Packard fiber optic cable. Over the fused-silica, step-index, glass-clad fiber there is a silicone coating to protect the thin

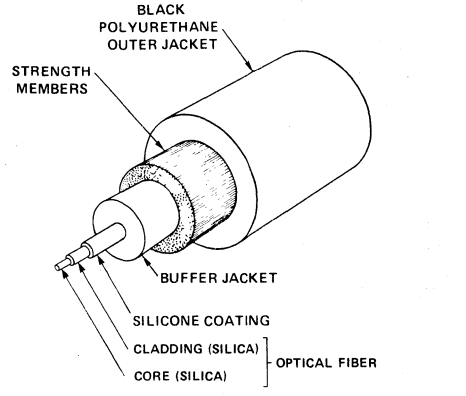


Figure 6. Step Index Fiber Optic Cable Construction.

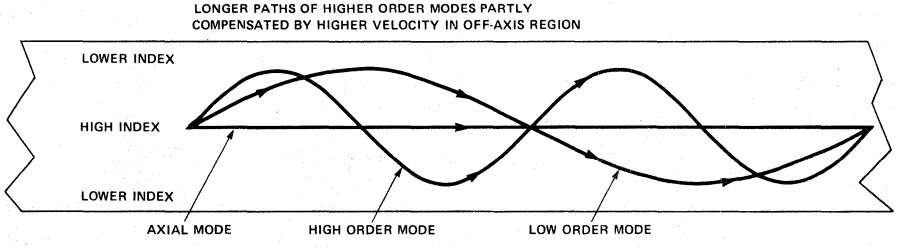


Figure 5. Graded Index Fiber Modes.

(20μm) cladding from scuffing. Over the buffer jacket are the tensile strength members, which allow the cable to be pulled through long conduits, and an outer jacket to protect the cable against crush and impact damage. This cable tolerates far more abuse than most wire cable. A sample was laid across the main entrance to the Hewlett-Packard headquarters and factory at 1501 Page Mill Road, Palo Alto. After several weeks of being driven over, night and day, there was no impairment of performance.

Other materials used in step index fibers are glass-clad glass, plastic-clad glass or fused silica, and plastic-clad plastic. These have N.A.'s ranging from less than 0.2 to more than 0.5, and transmission losses from less than 10dB/km to more than 1000dB/km. Some manufacturers offer bundled fibers in which the individual glass fibers are small enough to allow the cable to be very flexible. In earlier days of fiber optic development, bundled fibers were considered necessary for reliability because breakage of one or more fibers could be tolerated without total loss of signal transmission. Also, the large diameter of the fiber bundle allowed more tolerance in connector alignment. The popularity of fiber bundles has dwindled because the single-fiber cable durability is better than had been anticipated, and connectors are now available which are capable of providing the precise alignment required for low coupling loss with small-diameter single fibers.

Flux Budgeting

Flux requirements for fiber optic systems are established by the characteristics of the receiver noise and bandwidth, coupling losses at connectors, and transmission loss in the cable.

The flux level at the receiver must be high enough that the signal-to-noise ratio (SNR) allows an adequately low probability of error, P_e. In the Hewlett-Packard fiber optic system, the receiver bandwidth and noise properties allow a $P_e < 10^{-9}$ with a receiver input flux of 0.8μW under worst-case conditions. At higher flux levels, the P_e is reduced.

From the receiver flux requirement (for given P_e), the flux which the transmitter must produce is determined from the expression for a point-to-point system:

$$(11)\quad 10 \log \left(\frac{\phi_T}{\phi_R} \right) = \alpha_0 \ell + \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_M$$

where ϕ_T is the flux (in μW) available from the transmitter
ϕ_R is the flux (in μW) required by the Receiver at P_e
α_0 is the fiber attenuation constant (dB/km)
ℓ is the fiber length (km)
α_{TC} is the Transmitter-to-Fiber coupling loss (dB)
α_{CC} is the Fiber-to-Fiber loss (dB) for in-line connectors
n is the number of in-line connectors; n does not include connectors at the transmitter and receiver optical ports
α_{CR} is the Fiber-to-Receiver coupling loss (dB)
α_M is the Margin (dB), chosen by the designer, by which the Transmitter flux exceeds the system requirement

Equation (11) is called the FLUX BUDGET and it is represented graphically in Figure 7. The same basic units (watts) are used for flux and for power, so it is correct and convenient to express flux in "dBm".

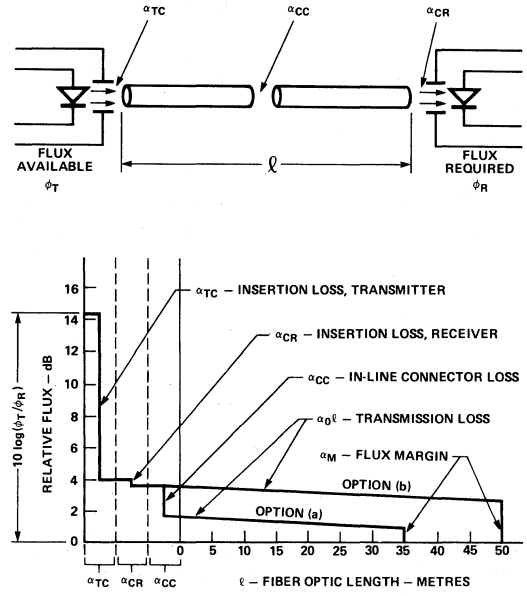


Figure 7. Flux Budget — Graphical Representation.

$$(12)\quad \phi(\text{dBm}) = 10 \log \left(\frac{\phi(\text{mW})}{1\ \text{mW}} \right) = 10 \log \left(\frac{\phi\ (\mu\text{W})}{1000\ \mu\text{W}} \right)$$

Here is an example of how the flux budget works:

1. Transmitter $\phi_T = 44\mu W$
2. Receiver $\phi_R = 1.6\mu W$

$$\Big\rangle\ 10 \log \left(\frac{\phi_T}{\phi_R} \right) = 14.39\text{dB}$$

Transmitter optical port: diameter = 200μm, N.A. = 0.5

Optical fiber (in connector): core diam. = 100μm, N.A. = 0.3

3. $$\alpha_{TC} = \alpha_A + \alpha_{NA} = 20 \log \left(\frac{200}{100} \right) + 20 \log \left(\frac{0.5}{0.3} \right)$$

$$= 6.02\text{dB} + 4.44\text{dB} = 10.46\text{dB}$$

Receiver optical port: diameter = 200μm, N.A. = 0.5

4. Because the diameter and N.A. of the receiver are both larger than those of the fiber, there is only a small amount of Fresnel loss, making $\alpha_{CR} \approx 0.34$dB

5. Apply equation (11) to see what the flux budget allows:

$$14.39\text{dB} = \alpha_0 \ell + 10.46\text{dB} + n\alpha_{CC} + 0.34\text{dB} + \alpha_M$$

$$\alpha_0 \ell + n\alpha_{CC} + \alpha_M = (14.39 - 10.46 - 0.34)\text{dB} = 3.59\text{dB}$$

6. Assume a transmission distance of 35 metres at 20dB/km

If cable length selections are 10-, 25-, and 50-metre lengths and connector loss is $\alpha_{CC} = 2dB$, then either of two options may be chosen:

7. a) Use a 10m and 25m length with one connector:
$\alpha_0 \ell + \alpha_{CC} = (35m \times 0.02dB/m) + 2dB = 2.7dB$
This leaves $\alpha_M = (3.59 - 2.7)dB = 0.89dB$

7. b) Use a 50m length and no connector:
$\alpha_0 \ell = (50m \times 0.02dB/m) = 1.0dB$ leaving $\alpha_M = 2.59dB$

Unless there is some good reason (cost, convenience, etc.) for choosing the 10m/25m option, it would be better to select the 50-metre option because it allows a larger α_M. In flux budgeting, α_M should always be large enough to allow for degradation of the efficiency of the flux generator in the transmitter (LED, IRED, laser, etc.). On the other hand, in dealing with more powerful transmitters, α_M must not be so large that it exceeds the dynamic range of the receiver.

Dynamic Range

The dynamic range of the receiver must be large enough to accommodate all the variables a system may present. For example, if the system flexibility requirement is for transmission distances ranging from 10 metres to 1000 metres with 12.5dB/km cable, and up to two in-line connectors, the dynamic range requirement is:

$$\begin{aligned} \alpha_0 \ell &= 1km \times 12.5dB/km = 12.5dB \\ n\alpha_{CC} &= 2 \times 2dB = 4.0dB \\ \alpha_M &= 3.0dB \\ \text{thermal variations} &= \underline{1.0dB} \text{ (estimated)} \\ & 20.5dB \end{aligned}$$

Accommodating a 20dB optical power dynamic range plus high sensitivity requires the receiver to have two important features: automatic level control, and a-c coupling or its equivalent. The a-c coupling keeps the output of the amplifier at a fixed quiescent level, relative to the logic thresholds, so that signal excursions as small as the specified minimum can cause the amplifier output to exceed the logic threshold. This function can also be called d-c restoration.

ALC (automatic level control) adjusts the gain of the amplifier. Low-amplitude excursions are amplified at full gain; high-amplitude excursions are amplified at a gain which is automatically reduced enough to prevent saturation of the output amplifier. Saturation affects propagation delay adversely so ALC is needed to allow high speed performance at high, as well as low, signal levels.

HEWLETT-PACKARD'S FIBER OPTIC SYSTEM

A number of objectives were established as targets for this development. Convenience and simplicity of installation and operation were the primary objectives, along with a probability of error $P_e < 10^{-9}$ at 10Mb/s NRZ, over moderate distances. In addition, there were the traditional Hewlett-Packard objectives of rugged construction and reliable performance. Manufacturing costs had to be low enough to make the system attractively priced relative to its performance.

Electrical convenience is provided by several system features. The Receiver and the Transmitter require only a single +5-volt supply. All inputs and outputs function at TTL logic levels. No receiver adjustments are ever necessary because the dynamic range of the Receiver is 21dB or more, accommodating fiber length variations as well as age and thermal affects. When the system is operated in its internally coded mode, it has NRZ (arbitrarily timed data) capability and is no more complicated to operate than a non-inverting logic element. Built-in performance indicators are available in the Receiver; the Link Monitor indicates satisfactory signal conditions and the Test Point allows simple periodic maintenance checks on the system's flux margin.

There are also several optical and mechanical convenience features. The optical ports of the Transmitter and Receiver are well defined by optical fiber stubs built into receptacles that mate with self-aligning connectors. Low-profile packaging and low power dissipation permit the modules to be mounted without heat-sink provision on P.C. boards spaced as close as 12.5mm (0.5 in.).

The internally-coded mode of operation is the simplest way to use the Hewlett-Packard system. This mode places no restriction on the data format as long as either positive or negative pulse duration is not less than the minimum specified. The simplicity is achieved by use of a 3-level coding scheme called a PULSE BI-POLAR (PBP) code. This mode is selected simply by applying a logic low (or grounding) to the Mode Select terminal on the Transmitter — no conditioning signal or adjustment is necessary in the Hewlett-Packard Receiver because it automatically responds to the PBP code.

Transmitter Description

Figure 8 shows symbolically the logical arrangement of the Transmitter, waveforms for the signal currents I_A and I_B, and the resulting waveforms for the output flux. The arrangement shown is logically correct but circuit details are not actually realized as shown. For example, the current sources actually have partial compensation for the negative temperature coefficient of the LED (or IRED). In Figure 8, there are five important things to notice.

First, notice that the bias current, I_C, is never turned off — not even when the Transmitter is operated in the externally coded mode (Mode Select "high"). This is done to enhance the switching speed of the LED (or IRED) in either internally- or externally-coded mode. The bias current also stabilizes the flux excursion ratio (k in Equation 14) symmetry in the internally-coded mode.

Second, notice that

ϕ_L, the low-level flux, is produced by I_C
ϕ_M, the mid-level flux, requires $I_B + I_C$
ϕ_H, the high-level flux, requires $I_A + I_B + I_C$

As far as the Receiver is concerned, the excursion flux, $\Delta\phi$, produced by switching I_A and I_B, is the important parameter of the Transmitter. Average flux is, of course, related to excursion flux but is not as important in establishing the SNR of the system.

Third, notice that with Mode Select "low" and a 500kHz signal at Data Input, there will be only one refresh pulse generated in each logic state. The excursions (ϕ_H-ϕ_M) and (ϕ_M-ϕ_L) are nearly balanced so an average-reading flux meter will indicate the mid-level flux, ϕ_M, within +0.6% or -0.6% depending on whether the flux excursion ratio, k, is at its maximum or at its minimum limit.

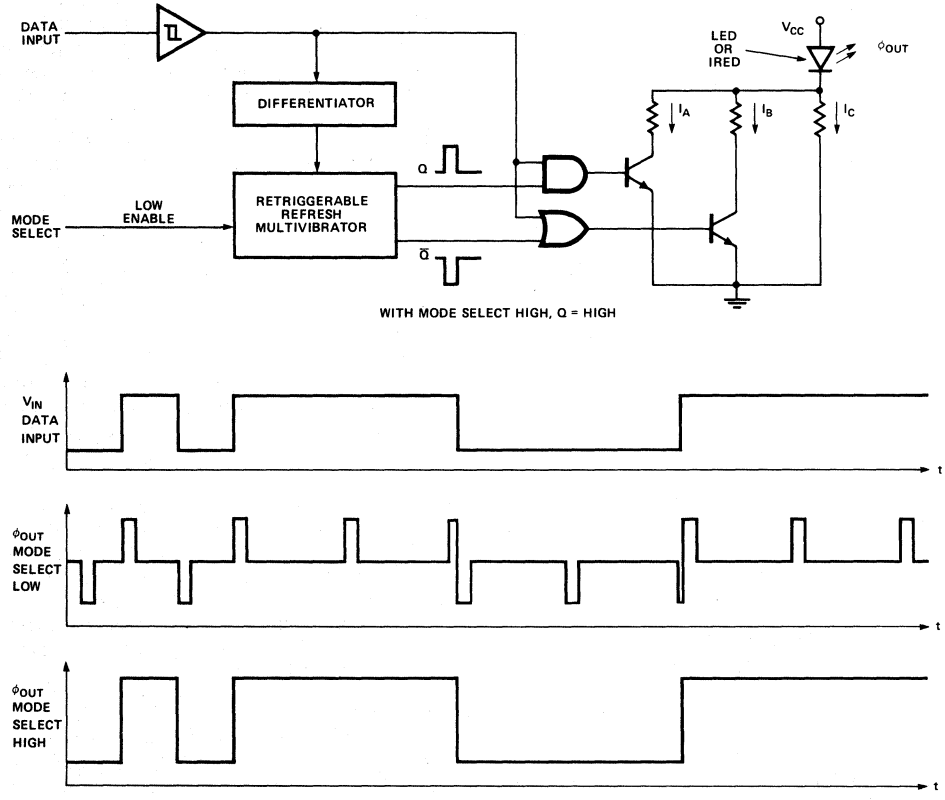


Figure 8. Transmitter Block Diagram and Waveforms.

Fourth, notice that, with Mode Select "low", any Data Input transition (either H-L or L-H) retriggers the Refresh Multivibrator to start a new train of pulses. All refresh pulses for either logic state have the same duration. This keeps the average flux very near the mid-level even when the duration in either logic state of arbitrarily timed input data is very short. Notice also that any refresh pulse is overridden (abbreviated) by the occurrence of a Data Input transition so there is no additional jitter when the duration of the Data Input in either state is at or near the same length of time as the refresh interval. The refresh interval is very long, relative to the refresh pulse duration, making a duty factor of approximately 2%; this also is done to keep the average flux near mid-level regardless of how long Data Input remains in either logic state. The only condition under which the average flux can deviate significantly from the mid-level occurs when Data Input remains in one state for a period of time LESS than the duration of the refresh pulse. If this is likely to occur, the format should be configured so the numbers of 1's and 0's are balanced as they would be in Manchester code. Observing this data format allows the use of the internally-coded mode of the Hewlett-Packard system at data rates ranging from arbitrarily low to higher than 10M Baud, with the absolute limit being that at which the signal intervals become as short as t_{PHL} and/or t_{PLH}.

Fifth, notice that with Mode Select "high," the Q output of the Refresh Multivibrator is "high" (and $\overline{Q}$ is "low"). Under this condition, I_A and I_B are both ON when Data Input is "high" and both OFF when it is "low". This makes the output flux excursion a logical replica of the Data Input.

Flux Measurement

A high-speed photodetector and oscilloscope could be used for measuring the excursion flux, but an average-reading flux meter can be used to measure $\Delta\phi$ as follows:

With Mode Select "high":

1. Apply steady-state "low" to Data Input and observe ϕ_L with flux meter.
2. Apply a 500kHz square wave (50% duty factor) to Data Input and observe $(\Delta\phi + \phi_L)$ with the flux meter and subtract ϕ_L (Step 1) to obtain $\Delta\phi$.

This procedure also yields the proper value of the high-level flux, ϕ_H, to be used in computing the flux excursion ratio, k. Since $\phi_H = (\phi_L + 2\Delta\phi)$, the value of ϕ_H is:

(13) HIGH-LEVEL FLUX, $\phi_H = 2(\Delta\phi + \phi_L) - (\phi$
Step 2 Step 1

It appears, from the waveforms in Figure 8, that the 500kHz signal prescribed in Step 2 is not necessary; that is, with Data Input at a steady-state high, the flux meter would read ϕ_H directly, from which $\Delta\phi$ could be calculated by

subtracting ϕ_L (observed in Step 1) and dividing by two. However, this method would cause slightly more heating of the LED and lead to a slightly different (and incorrect) measurement of ϕ_H and $\Delta\phi$. With the values of ϕ_H and ϕ_L from Step 1 and 2, the flux excursion ratio can now be computed:

$$(14)\ \text{FLUX EXCURSION RATIO, } k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$$

In a 2-Level Code, there is, of course, no mid-level; however, the definition of flux excursion ratio is the same as for Pulse Bi-Polar code, i.e., Equation (14). It is only necessary to substitute average flux for mid-level flux, ϕ_M, in Equation (14). For 2-Level Code, the average flux is:

$$(15)\ \text{AVERAGE FLUX (2-Level Code)} = \frac{\phi_H \Sigma t_H + \phi_L \Sigma t_L}{\Sigma t_H + \Sigma t_L}$$

where Σt_H is the total time the flux is at level ϕ_H
Σt_L is the total time the flux is at level ϕ_L

Substitution of this expression for ϕ_M in Equation (14) leads to:

$$(16)\ \text{FLUX EXCURSION RATIO} = k = \frac{\Sigma t_L}{\Sigma t_H}$$

Equation (16) shows why it is that when a 2-Level Code is used (e.g., with Mode-Select "high" in the Hewlett-Packard Transmitter) the data input signal must, on average, have a 50% duty factor to make k = 1. That is, in the averaging interval, the total number of "mark" intervals should be equal to the total number of "space" intervals, such as in Manchester code.

Use of 2-Level Code also requires that the input flux remain for less than 5μs at either high or low level. This is necessary to avoid "pulling" the receiver dc restorer voltage too far away from the value corresponding to the average flux, and possibly losing occasional bits.

Receiver Description

The Hewlett-Packard Receiver block diagram is shown in Figure 9. There are four functional blocks:

1. The amplifier, including a gain-control stage and split-phase outputs with a voltage divider for each.
2. The dc-restorer with a long time constant.
3. Logic comparators with an R-S latch.
4. Positive and negative peak comparator with single-ended output for the ALC and link monitor circuits.

Optical flux at the input is converted by the PIN photodiode to a photocurrent, I_P, which is converted to a voltage by the PREAMPLIFIER. This voltage is amplified to a positive-going output, V_{P1}, and a negative-going output, V_{N1}. A rising input flux will cause V_{P1} to rise and V_{N1} to fall. These voltages are applied to the differential inputs of the DC RESTORER AMPLIFIER whose output, V_T, falls until it is low enough to draw the average photocurrent away from the preamplifier via the 25k resistor. This makes $V_{P1} \approx V_{N1}$ when the input flux is at the average level. The output impedance of the dc restorer amplifier is very high, making a long time constant with the filter capacitor, C_T. The long time constant is required for loop stability when input flux levels are so low that there is little or no ALC gain reduction, with consequently high loop gain. With no input flux, $V_T = V_{TMAX}$; as input flux rises, V_T falls proportionately, so the voltage at the TEST POINT can be used as an indicator of the average input

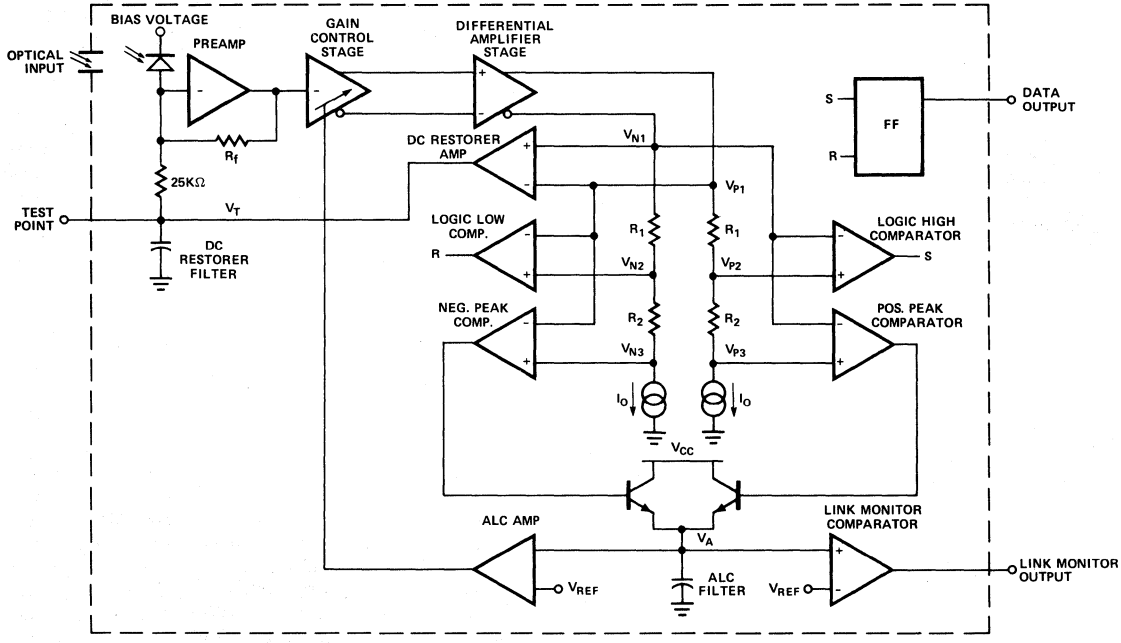


Figure 9. Receiver Block Diagram.

flux. With respect to the Receiver optical port, the responsivity of the PIN photodiode is approximately 0.4A/W, leading to the expression:

$$(17)\ \text{AVERAGE INPUT FLUX}, \phi_{AV}(\mu W) \approx \frac{[V_{TMAX} - V_T]\ (mV)}{10}$$

where V_{TMAX} = Test Point Voltage with no optical input signal.

The instrument for observing V_T must not load the Test Point significantly, so an input resistance of 10MΩ is recommended.

As described above, when the input flux is at the average level, the positive-going and negative-going output voltages V_{P1} and V_{N1} are approximately equal. Notice that this makes the outputs of both logic comparators low. A positive flux excursion, rising faster than the dc restorer (with its long time constant) can follow, will cause V_{P1} to rise and V_{N1} to fall. If the positive flux excursion is high enough, the LOGIC HIGH COMPARATOR input voltage ($V_{P2} - V_{N1}$) becomes positive, and a SET pulse is produced for the R-S flip-flop. [Similarly, a negative flux excursion of such amplitude would make ($V_{N2} - V_{P1}$) become positive and a RESET pulse would be produced.] A larger amplitude of positive flux excursion would make the POSITIVE PEAK DETECTOR input voltage ($V_{P3} - V_{N1}$) change from negative to positive and cause current to flow into the ALC FILTER capacitor. When the voltage V_A starts to rise above V_{REF}, the ALC AMPLIFIER output will operate on the GAIN CONTROL AMPLIFIER to limit the Receiver's forward gain. Notice that the ALC action is the same for a negative flux excursion, so that the Receiver's gain limitation is determined EITHER by positive flux excursion OR by negative flux excursion — whichever is the larger. For this reason, the positive and negative excursions must be nearly balanced with respect to the average flux. The allowable imbalance is determined by the values of the resistors in the negative and positive voltage dividers. The ALC action limits the maximum excursion to a voltage I_O ($R_1 + R_2$), whereas the logic threshold is only $I_O R_1$. Actual limits are established by the tolerances on the resistors and current sources. Notice that the ALC voltage, V_A, activates both the ALC COMPARATOR and the LINK MONITOR COMPARATOR. Therefore, a "high" LINK MONITOR signifies two conditions:

1. The input flux excursions are high enough to cause ALC action (gain limitation).
2. The excursions are more than adequate for operation of the logic comparator.

Notice that the LINK MONITOR could be "high," but k could be outside the specified limits such that P_e exceeds 10^{-9}. Conversely, because of safety margin in the Receiver design, it is also possible to have $P_e < 10^{-9}$ when the flux excursions are too small to make the LINK MONITOR "high".

OPERATION OF THE HEWLETT-PACKARD SYSTEM

With Hewlett-Packard Components Exclusively

The main concern in a fiber optic link is the flux budget. Other areas of concern are: data rate, data format, and the interface with other elements of a data transmission system.

Flux budgeting, using the Hewlett-Packard Transmitter, Receiver, Connector, and Cable components is very straightforward for most applications. It is necessary only to use the data sheet information correctly in making the coupling loss and transmission loss allowances.

When used with other Hewlett-Packard components, the characteristics of the Receivers are not critical. Their optical ports have a diameter and N.A. which are both greater than the size and N.A. of the Hewlett-Packard Cable. The Receivers also have a high responsivity and the spectral response is nearly constant over the spectrums radiated by Hewlett-Packard Transmitters.

With Components From Other Manufacturers

When using the Hewlett-Packard Receivers with other cables, it may be necessary to account for N.A. loss and/or area mismatch loss. When other sources are used, it may be necessary to compute an effective flux ratio:

$$(18)\ \text{EFFECTIVE FLUX RATIO, EFR}_S\ (\text{Source Spectrum}) = \frac{\int \phi_\lambda R_{r\lambda} d\lambda}{\int \phi_\lambda d\lambda}$$

where $R_{r\lambda}$ is the relative response of the Receiver (from data sheet)

ϕ_λ is the spectral flux function of the source

If the transmission loss of the cable varies sharply over the wavelength range of the source spectrum, then the spectral transmittance of the cable should be included in the computation of EFR. The spectral transmittance varies with cable length, so the integration must be performed using the cable length required in a particular installation:

$$(19)\ \text{EFFECTIVE FLUX RATIO, EFR}_{CS}\ (\text{Cable and Source}) = \frac{\int \tau_\lambda \phi_\lambda R_{r\lambda} d\lambda}{\int \tau_\lambda \phi_\lambda d\lambda}$$

where τ_λ is the spectral transmittance of a particular length of fiber optic cable, computed as:

$$(20)\ \tau_\lambda = 10^{-\left(\frac{\ell}{10}\right)\alpha_{0\lambda}}$$

where $\alpha_{0\lambda}$ is the spectral function in (dB/km) of the fiber optic cable and ℓ is the particular cable length (km)

Notice that as the length is reduced, τ_λ becomes more nearly a constant and may be factored out of both numerator and denominator of Equation (19). When EFR is significantly less than unity, it enters the flux budget expression, Equation (11).

$$(21)\ 10 \log\left(\frac{\phi_T}{\phi_R}\right) = \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_0 \ell + \alpha_M \underset{-10 \log (EFR)}{}$$

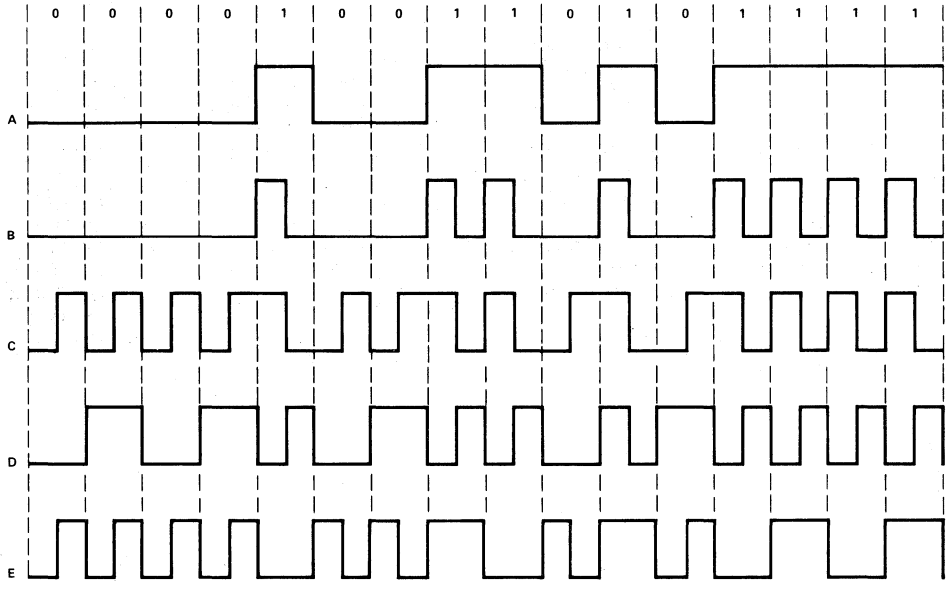
See Equations 11, 18, and 19 for definition of terms.

The optical ports of Hewlett-Packard Transmitters are designed for mating with Hewlett-Packard Cable/Connector assemblies, but their characteristics require a little more attention than do the Receiver optical ports. The Transmitter and Cable/Connector data sheets should be consulted for the correct values of size and N.A., or for the directly-given value of transmitter-to-fiber coupling loss, α_{TC}, to use in flux budgeting. In applications having very short transmission distances, but requiring a number of in-line (cable-to-cable) connections, it is likely to be advantageous to use fiber optics of larger core diameter

and N.A., such as some of the plastic types. The larger core diameter reduces the likelihood of losses in connectors due to misalignment. Depending on the size and N.A. of the Transmitter optical port, a larger core diameter and N.A. in the fiber optic cable may also reduce α_{TC}, but if the cable core diameter is too large, the cable-to-receiver loss, α_{CR}, may be excessive.

Data Rate and Format

The other areas of concern (data rate, data format, and interface) are interactive, depending on system requirements. In any single transmitter-to-receiver link, the flux budget along with probability of error P_e, establish the signaling rate, in baud units, while the data rate, in bits per second, depends also on the data format, or transmission code. NRZ (Non-Return-to-Zero) is the term for a transmission code in which the signal does not periodically return to zero. If a stream of NRZ data contains a series of consecutive "1's", the signal remains at the "1" level; similarly, the signal remains at the "0" level for consecutive "0's". With RZ (Return-to-Zero) codes, the level periodically changes from high level to low level or back, never remaining at either level for a period of time longer than one bit interval. Some examples of codes are given in Figure 10. Notice that NRZ code uses the channel capacity most efficiently since it requires only one code interval per bit interval. The RZ codes illustrated use two code intervals per bit interval while other codes may require an even higher channel capacity for a given data rate. NRZ code requires a clock signal at the receiving end to define, for each interval, the point in time at which the data is valid. The time at which the data is clocked must be sufficiently clear of the interval edges to avoid phase-shift errors due to jitter, rise time, or propagation delay. Since the clock signal is separately transmitted, phase shift in the clock channel can contribute to the phase-shift error unless it is equal, in direction and magnitude, to the phase shift in the data channel. For this reason, fiber optic



	CODE	DESCRIPTION	CHANNEL REQUIRED	REQUIRES DC?	REQUIRES CLOCK?
A	NON-RETURN TO ZERO (NRZ)	High during entire "mark", low during entire "space" interval	1 Mbaud per Mb/s	YES	YES
B	RETURN TO ZERO (RZ)	Low during entire "space", momentarily high during "mark" interval	2 Mbaud per Mb/s	NO	YES
C	MANCHESTER (SELF-CLOCKING RZ)	Positive transition for "space", negative transition for "mark"	2 Mbaud per Mb/s	NO	NO
D	BIPHASE MARK (MANCHESTER II)	Each bit period begins with a transition. "Space" has NO transition during bit period — "mark" has one transition during bit period	2 Mbaud per Mb/s	NO	NO
E	BIPHASE SPACE	Same as Biphase Mark except "mark" and "space" reversed	2 Mbaud per Mb/s	NO	NO

NOTE THAT C, D, E HAVE 50% DUTY FACTOR (k = 1.00)

Figure 10. Examples of NRZ and RZ Code Patterns.

channels carrying clock signals should use the same type of cable and the same length, unless the transmission distance is very short. Note that the transmission time delay in an optical fiber depends on the core index of refraction:

(22) TRANSMISSION DELAY, $t_\ell = \left(\frac{1}{c}\right) \ell n$

where c is the velocity of light in a vacuum, $c = 3 \times 10^8$ m/s
ℓ is the fiber optic cable length (m)
n is the core index of refraction

and differential delay between a data channel and a clock channel is:

(23) DIFFERENTIAL DELAY, $t = \left(\frac{1}{c}\right) [\ell_2 n_2 - \ell_1 n_1]$

Some RZ codes are self-clocking — i.e., a separate channel to transmit the clock signal is not required, so there is no problem with differential delay. For this reason, RZ codes may be preferred even though the data rate is less than that of NRZ. Note that in its internally coded mode, the Hewlett-Packard fiber optic system transmits either NRZ or RZ codes of arbitrary format and duty factor. In the externally coded mode, the system requires the code to be RZ; moreover, the duty factor of the code must be 50% and the signal must remain LESS than 5μs in either high state or low state.

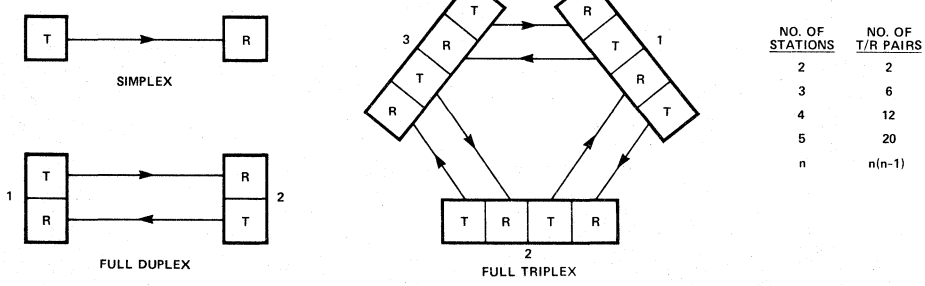
The Hewlett-Packard system is capable of a 10 Mbaud signaling rate. If a higher data rate is required, the data stream can be divided among additional channels. If each channel is RZ coded, such as with Manchester code, the capacity of each channel is 5Mb/s and if the total data rate requirement is 20Mb/s, four channels are required. Using NRZ, the 20Mb/s data can be transmitted on two channels, with a third channel for the clock signal. Thus, if the data rate requirement exceeds 15Mb/s, the NRZ format requires fewer fiber optic channels.

System Configuration

The simplex arrangement in Figure 11 allows data in one direction only, and the format should, therefore, include error checks, such as parity bits. The full duplex arrangement requires two Transmitter/Receiver (T/R) pairs and two cables but allows data to go in both directions simultaneously. If, at a given time, Station 1 is transmitting, the return transmission from Station 2 can be unrelated to the information from Station 1, but could also be a relay or re-transmission of the data received by Station 2, so a logic delay and comparator circuit in Station 1 can check for errors and allow corrections. The same is true for the full triplex arrangement. Extension to larger numbers of stations is possible and the benefits are the same, but the number of T/R pairs increase rapidly, as shown by the series in Figure 11, requiring n (n-1) T/R pairs for n stations.

Half-duplex (not illustrated) is a means for allowing two stations to alternately use the same transmission medium. With a wire cable, half-duplex operation is commonly and easily done; it can also be done with fiber optic cable but the fiber-furcating couplers for accomplishing it are very lossy, are not commonly available, and will not be discussed.

Data interchange among a large number of stations can be accomplished with fewer T/R pairs by using the Master Station Multiplex (MSM) arrangement in Figure 12. The MSM arrangement requires only 2(n-1) T/R pairs for n stations (master + (n-1) slaves). Its operation differs from the full n-plex arrangement of Figure 11 in that only the master station transmits directly to all other stations. Data from any slave station is transmitted to master and re-transmitted to all slave stations according to the "re-transmit enable" ($E_1 ... E_X$) selection made in the master station. Thus, a complete error check is possible. Regardless of how many slave stations are added, the transmission delay from any slave to any other slave is just the delay of two fiber optic links plus the propagation



NO. OF STATIONS	NO. OF T/R PAIRS
2	2
3	6
4	12
5	20
n	n(n-1)

Figure 11. Simplex, Full-Duplex, Full Triplex, Full-n-plex Fiber Optic Links.

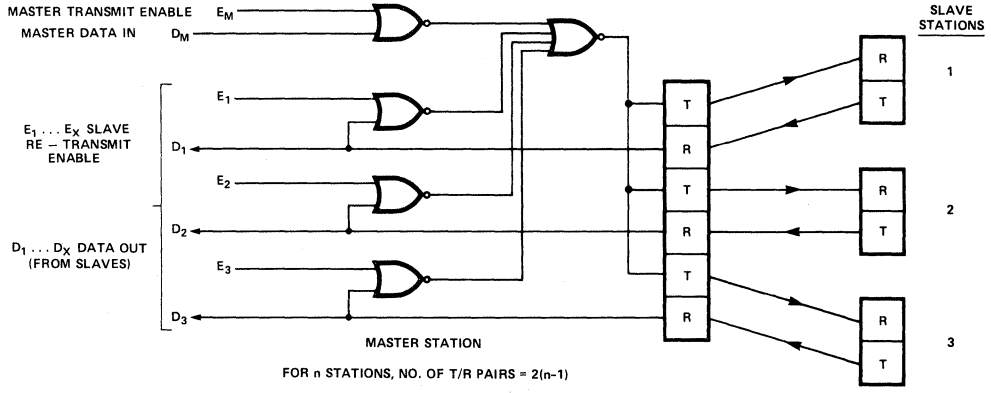


Figure 12. Master Station Multiplex Arrangement for Fiber Optic Links.

delay in the master station's relay circuit. The time delay between re-transmission from the master and the error-check return transmissions from the slaves is the same if each link length is the same, i.e., two links plus relay time. Notice that a complete error check requires an error check in the master, plus an error check in the station where the data originated. Another feature of the MSM system is that any slave station can be disconnected or turned off without affecting the other stations. With slightly more complicated relay control logic in the master stations, the MSM system can provide even more flexibility in the control of data movement — the schematic in Figure 12 is intended only to illustrate the potential flexibility of MSM.

At the expense of less flexibility and longer transmission delay, multiplex operation can be done with an even smaller number of T/R pairs by means of Looped-Station Multiplexing (LSM) as in Figure 13. In addition to requiring only n T/R pairs for n stations, LSM offers the advantage that an error check is required only at the station from which the data originates. There are some disadvantages. A relatively minor disadvantage is the data delay around the loop to where the data originated. A less minor disadvantage is the fact that, even if one of the stations in the loop is designated for loop control, it does not have control as absolute as that of the master station in MSM. A major disadvantage is that removal of one or more stations from the loop may require a re-run of the fiber optic cable unless the flux budget allows insertion of a connector to replace the station(s) removed. There is some error accumulation around the loop, but this is not a disadvantage if error correction is applied.

Error Accumulation

Where error correction is inconvenient or impossible, the accumulation of error through data relay units may be significant. With Hewlett-Packard components operated within the limits prescribed by the data sheet parameters and the flux budget, any point-to-point link has a

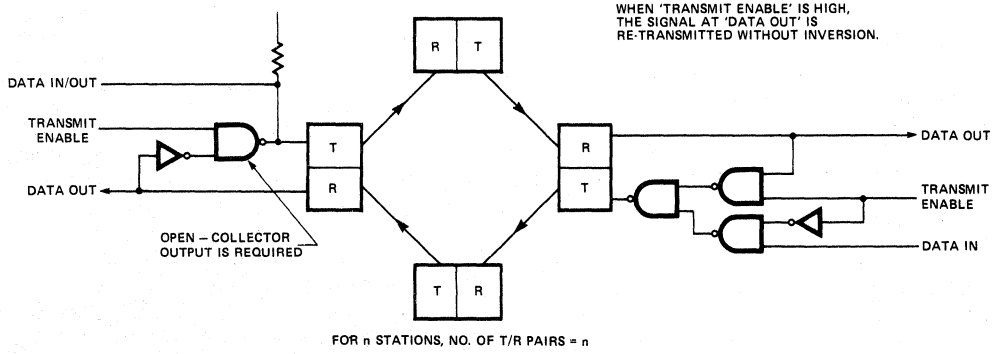


Figure 13. Looped-Stations Multiplex Arrangement for Fiber Optic Links.

probability of error $P_e < 10^{-9}$. This means that $P_e < 10^{-9}$ as long as the loss margin, α_M(dB) is above zero. With a number, n, of repeater links, the worst case estimate of cumulative probability of error is the RMS value:

(24) CUMULATIVE PROBABILITY OF ERROR,
$$P_{e,n} = 1 - \prod_{i=1}^{n} (1 - P_{e,i}) \approx \sum_{i=1}^{n} P_{e,i}$$

where $P_{e,i}$ is the probability of error in link "i"

If each link has the same probability of error, P_e, then the cumulative value of P_e is estimated at:

(25) CUMULATIVE PROBABILITY OF ERROR FOR EQUAL P_e's
$$P_{e,n} \approx nP_e$$

However, as in any chain, the probability of error is usually just that of the "weakest link," that is, the link having the highest probability of error.

Measuring the probability of error can be very time-consuming if P_e has a very low value. For instance, if $P_e = 10^{-9}$ at 10 Mbaud (BER = 10^{-9}), this suggests that if the system is operated for 100 seconds at 10 Mbaud (accumulate 10^9 bits) with one error, the $P_e = 10^{-9}$ is verified. This is not necessarily true. The significance of $P_e = 10^{-9}$ is that over several such periods the average error is one per 100 seconds. A less time-consuming procedure is to lower the signal (flux) level until the error rate, $P_{e,N}$ is measurably high in a comfortable period of time, and note this flux level as ϕ_N, the Noise measurement flux level. The operating flux level is designated ϕ_0, and is found from the ratio:

26. $$\frac{X_0}{X_N} = \frac{\phi_0}{\phi_N} \text{ and } X_0 = X_N \frac{\phi_0}{\phi_N}$$

and from the complementary error function:

$P_e = \text{erfc}\,(X_0) = 1 - \text{erf}(X_0)$ calculated for ϕ_0
$P_{e,N} = \text{erfc}(X_N) = 1 - \text{erf}(X_N)$ measured at ϕ_N
$$\text{erfc}(X) \approx \frac{.54}{X}(\epsilon^{-X^2}) \text{ for } P_e < 10^{-4}$$

This measurement and relationship can be useful in evaluating the relative merits in the tradeoff between running a single link over a long distance versus operating with one or more repeaters. The use of repeaters usually yields the lower P_e, but may be "overkill" in some cases.

INSTALLATION, MEASUREMENT, AND MAINTENANCE

The shielded metal packages of Hewlett-Packard Fiber Optic Modules are very sturdy and can be mounted in any position. Both Transmitter and Receiver dissipate very low power, so heat sinking is not required. A cool location is preferred, especially for the Transmitter. The main concern in selecting the locations of both modules is accessibility of the optical ports.

Mounting

The preferred mounting is with two #2-56 screws on a printed circuit board. Clearance must be provided for the Lock Nut, which protrudes 0.5mm to 1.0mm (depending on angular position) beyond the plane of the module's bottom surface. The usual way to deal with this is to allow the Lock Nut to overhang the edge of the P.C. board as in Figure 14. Lock Nut clearance could also be provided by an opening in the board, or by using washers of 1mm thickness on the #2-56 mounting screws to space the Module bottom 1mm from the board. Screws entering the #2-56 tapped holes MUST NOT TOUCH BOTTOM AS THIS MAY DAMAGE THE MODULE. The #2-56 tapped hole is 5.6mm (0.22 in.) deep, which provides an ample purchase on the thread.

P.C. Board Thickness		Recommended Screw Length — mm (in.)	
mm	in.	W/O Spacer	W/1-mm Spacer
0.79	1/32	4.78 (.188)	6.35 (.250)
1.59	1/16	6.35 (.250)	6.35 (.250)
2.38	3/32	6.35 (.250)	6.35 (.250)

The #2-56 holes near the front of the package are the only screw holes that may be used for mounting the module. UNDER NO CIRCUMSTANCES MAY THE SCREWS ALREADY INSTALLED OR THE SET SCREW BE DISTURBED. Disturbing these may cause interior damage.

For additional support, the electrical leads may be bent down and soldered into the P.C. board. In bending the leads, care must be taken to avoid strain at the point where the leads enter the glass seal. This can be done by applying mechanical support between the module and the bending point which should be at least 1.0mm (0.04 in.) from the end of the module. A needle-nose pliers can also be used to bend the leads individually, providing no bending moment is transferred to the seal. See Figure 14 for details fo these techniques.

Panel mounting can also be used. This is an especially attractive mounting when R.F. shield integrity must be maintained. As seen in Figure 15, the panel thickness must be less than 4mm (5/32 in.) and have a counter-bore to receive the Lock Nut. This will make the mounting secure and leave enough of the Barrel outside the panel to permit installation of an external mounting nut as well as the Cable Connector.

Fiber Optic Cable Connections

The data sheet cautions against disturbing the Lock Nut and Barrel. This is to prevent damage by someone who has not read the following material:

As seen in Figure 16, there is a clearance between the interior end of the Barrel and a shoulder on the Fiber Alignment Sleeve. If this clearance is not maintained, there is a risk that a force applied to the Barrel may be transmitted by the Fiber Alignment Sleeve to the optical fiber stub, forcing the stub against the face of the source or detector. The source (or detector) is an extremely fragile semiconductor device and even a very small force can cause severe damage. Should it be necessary to remove the Lock Nut and Barrel, they should be reinstalled with this procedure:

1. Lightly and carefully thread the Barrel into the Module body until it comes against the shoulder of the Fiber Alignment Sleeve.
2. Back the Barrel OUT ONE FULL TURN, then HOLD THE BARREL FROM TURNING while seating the Lock Nut securely against the body. During final tightening of the Lock Nut, the Barrel may be allowed to enter no more than HALF A TURN.

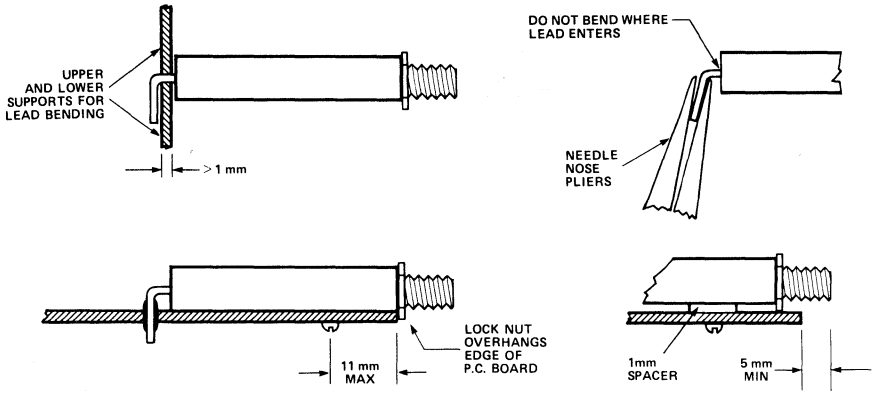


Figure 14. Lead Bending and P.C. Board Mounting.

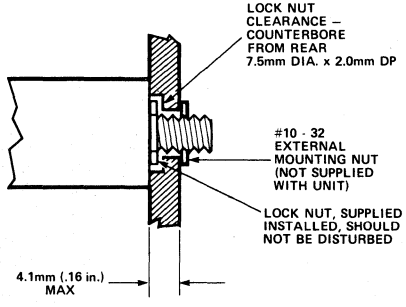


Figure 15. Panel Mounting.

When Hewlett-Packard Cable Connectors are joined, either to each other or to the optical port of a Transmitter or Receiver, there is a cylindrical spring Sleeve that aligns the Ferrules. This is shown in Figures 16 and 17. It may be difficult to see, but the Sleeve does have a slightly flattened "leaf" on either side of a notch. The notch makes the leaves spring separately, allowing the Ferrules at opposite ends of the sleeve to have slightly different diameters and yet be firmly aligned by the curved interior wall. A chamfer on the edge of the Ferrule aids insertion. In making temporary Cable-to-Cable connection, it is permissible, and often convenient, to omit the Barrel, since it does not perform an alignment function. When the Barrel is used for a more sturdy joint, the connection procedure is:

1. Install the Sleeve and Barrel on one Connector, using only FINGER TIGHTNESS of the Coupling on the Barrel.
2. Start the Ferrule of the second Connector into the Sleeve.
3. Engage the Coupling on the Barrel threads and tighten FINGER TIGHT.

Alignment of the Ferrules (and hence the fiber optics) is performed by the Sleeve; the Barrel and Couplings are intended only for tensile support, but if they are OVER tightened, they may cause misalignment. Loss of coupling due to misalignment can be observed at the V_T (Test Point) on the Receiver when the System is active: $\Delta V_T/\Delta\phi \approx 10mV/\mu W$.

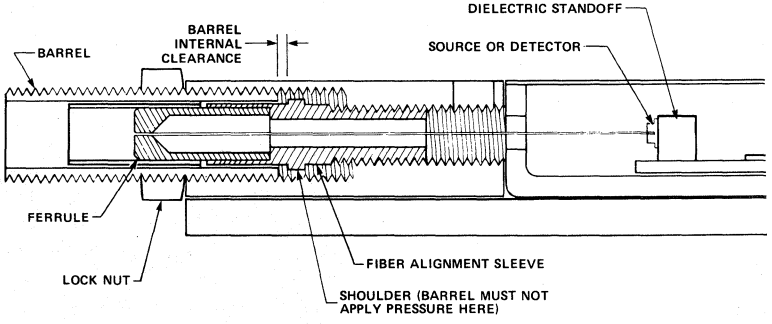


Figure 16. Opto-Mechanical Structure of T/R Modules.

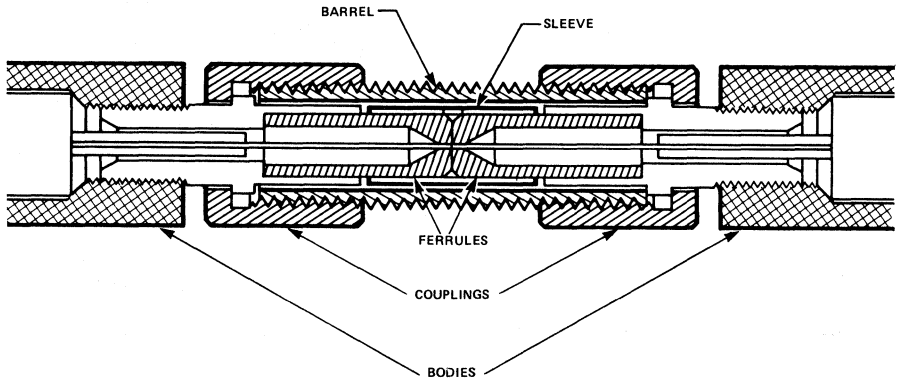


Figure 17. In-Line Connector Arrangement.

The procedure above applies also to making Cable connection at the Receiver and Transmitter, except that the Sleeve and Barrel are already installed. In manufacture, the Sleeve in the Module is pre-stressed for a tighter fit on the Ferrule in the Module than on the Ferrule in the Connector. The Sleeve is not likely to be pulled out when the Module is disconnected, but if that does happen, it can be reinstalled without removing the Barrel by using the Connector Ferrule to guide and support it.

In connecting fiber optics other than those from Hewlett-Packard to a Hewlett-Packard module, it is necessary to center the fiber in a cylinder with the same outside diameter as the Hewlett-Packard Ferrule over a length (to first shoulder) equal to half the length of the Sleeve, i.e., 3.5mm. This is adequate for a temporary connection. For a more permanent connection, add a coupling to fit the #10-32 thread on the Barrel.

Power Supply Requirements

Power supply lines for the Transmitter and the Receiver should each have a pi filter of two 60μF shunt capacitors and a 2.2μH (<1Ω) inductor. The Transmitter needs this filter to prevent transients from reaching other equipment when the LED (or IRED) currents are switched. The Receiver needs the filter to keep line transients from interfering with its extremely sensitive amplifier. In addition, the Receiver may need its own regulator, as shown in the data sheet, to prevent low-frequency transients or ripple from interfering with the data stream. If a regulator is used, the pi filter should be between the regulator output and the Receiver supply terminal. The Transmitter needs no regulator if the supply voltage is in the specified range.

System Performance Evaluation

System performance checks may be done by using error-detection equipment, such as the Hewlett-Packard Mod. 3760A Word Generator and 3761 Error Detector as indicated in Figure 18. The Mod. 3780A Pattern Generator/Error Detector which contains both word generator and error detector is also usable, although it has less flexibility in word generation and a lower data rate capability. These instruments have low-impedance (50Ω and 75Ω) inputs and outputs. The outputs have adequate voltage swing to drive the Fiber Optic Transmitter Data Input, but ringing may occur unless the signal line is properly terminated. The low-impedance inputs require a buffer amplifier between the Receiver output and the Error Detector input. Here also the voltage swing is ample, so a simple emitter follower will do as a buffer.

With Mode Select "low" (on the Fiber Optic Transmitter), the Word Generator may be set for either NRZ or RZ code, and there is no restriction of any kind on word length or composition (pseudo random or selected). With Mode Select "high", the code selection can be either NRZ or RZ but in either code the word composition must be such that:

1. No interval > 5μs of consecutive marks or consecutive spaces
2. Duty factor: .44 < DF < .57 or .75 < k < 1.25

The first condition can be examined with an oscilloscope, but if word length is such that:

$$\frac{\text{word length (bits)}}{\text{data rate (bits/second)}} < 5 \text{ microseconds}$$

then there is no way that any consecutive marks or spaces can extend over 5μs.

The easiest way to check duty factor is by observing k directly on an ac coupled oscilloscope: first establish the baseline position (e.g., center of scope face) with zero signal input, then with the data signal applied:

$$k = \frac{\text{excursion above baseline position}}{\text{excursion below baseline position}}$$

where the oscilloscope deflects upward for positive input. For this observation, the oscilloscope need not be synchronized — it could be free-running. The word composition should be adjusted to bring k within the specified limits. The word composition can be adjusted by adding zeroes, changing word length, or by handselecting the bit sequence.

Either error detector has two modes of operation: BER (Bit Error Rate) mode and "count" mode. The count mode is simplest to use and gives an earlier indication of the result of any system adjustment.

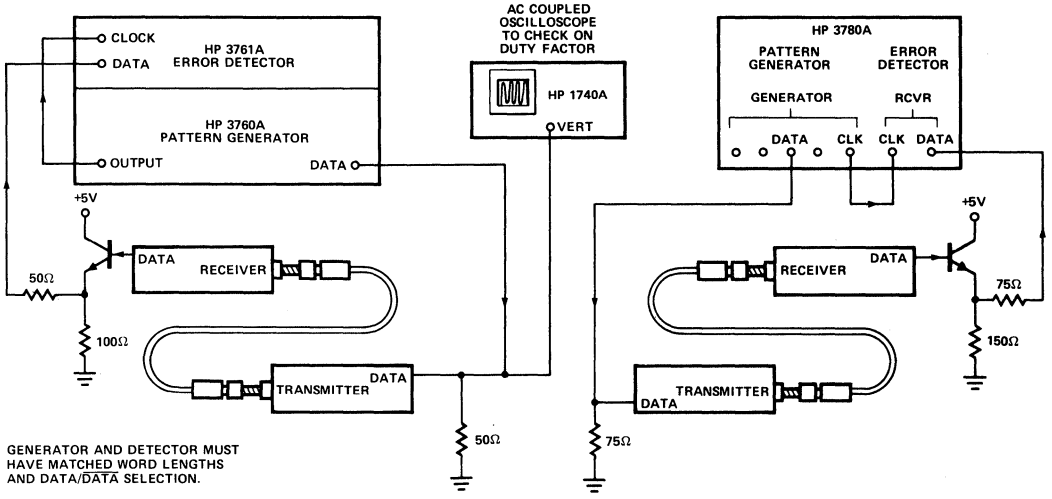


Figure 18. Bit Error Rate Measurement Arrangement.

With the System at normal operating flux level, the error rate is so low that it would take several hours or even days to make an accurate BER measurement. If the flux level is reduced, SNR falls and BER rises until it becomes measurable. Then the error function [see Equation (26)] can be applied to determine the BER at the normal flux level in terms of the ratio ϕ_O/ϕ_N where ϕ_O is the operating flux level and ϕ_N is the flux at the reduced level where the BER was measured. The problem now is that ϕ_N may be too low to measure with equipment at hand. The solution is in the Receiver Test Point voltage, V_T, which varies linearly as Receiver input flux — see Equation (17). But even this method has limits; when the flux becomes a small fraction of a microwatt, the voltage difference ($V_{TMAX} - V_T$) cannot be accurately observed. The solution to this problem is in the Transmitter-to-Cable connection. Just back off the Coupling, noting the number of turns while observing V_T, then plot a curve like that of Figure 19. The curve is quite repeatable if care is taken to avoid backlash and rotation of the Connector Body (rotate Coupling only) but the curve is not the same for each System.

Operating Margin Measurement

The flux budget margin, α_M, for a given P_e can be found using the Connector on the Transmitter as an adjustable attenuator as described above, proceeding as follows:

1. Prepare a curve similar to Figure 19.
2. Count the turns, N, needed to get measurable error, $P_{e,N}$.
3. Find α_N(dB) from N and the curve from Step 1.
4. Find X_N from erfc (X_N) = $P_{e,N}$ (measured).
5. Find X_0 from erfc (X_0) = P_e (given).

$$(27)\ \alpha_M(dB) = \alpha_N - 10 \log \frac{X_0}{X_N} \text{ FOR GIVEN } P_e$$

Absolute flux levels at "N" turns can be found by measuring the flux level when N = 0 and applying a ratio. A rough measurement can be made using the Test Point voltage, V_T, and Equation (15). A more precise measurement requires a calibrated radiometer, such as the EG&G Mod. 550, used as shown in Figure 20a. With its "flat" filter installed, the EG&G Mod. 550 reads the radiant

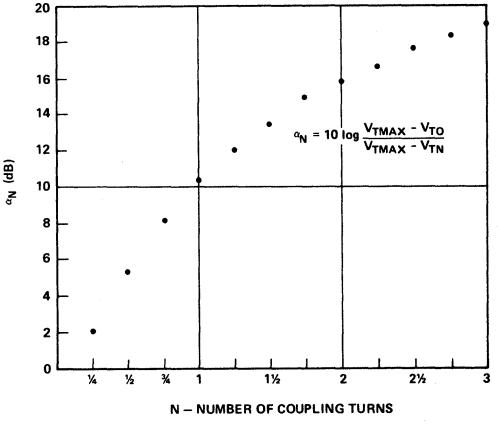
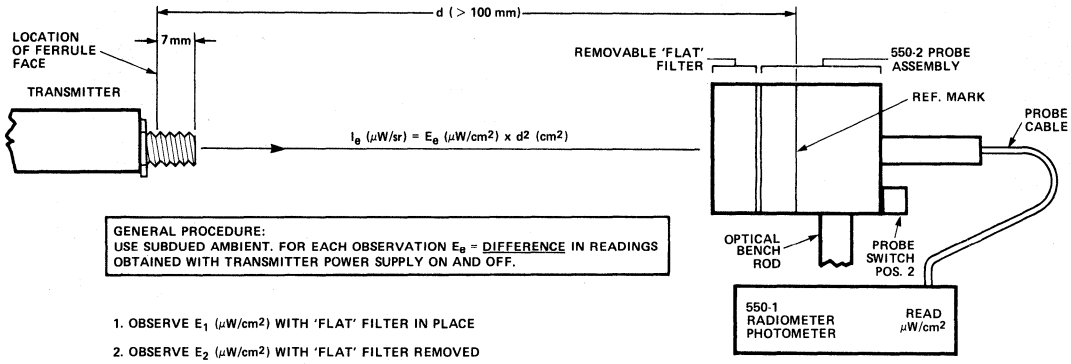


Figure 19. Flux Decoupling by Rotation of Connector Coupling.



GENERAL PROCEDURE:
USE SUBDUED AMBIENT. FOR EACH OBSERVATION E_e = DIFFERENCE IN READINGS OBTAINED WITH TRANSMITTER POWER SUPPLY ON AND OFF.

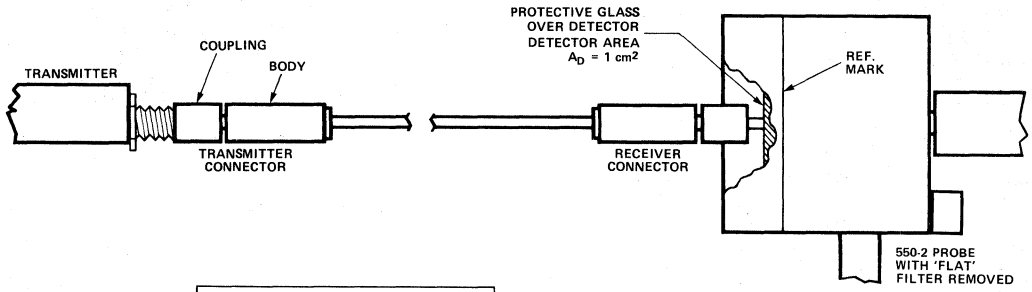
1. OBSERVE E_1 (μW/cm²) WITH 'FLAT' FILTER IN PLACE
2. OBSERVE E_2 (μW/cm²) WITH 'FLAT' FILTER REMOVED

FILTER TRANSMITTANCE: $\tau_F = E_1 / E_2$

AVERAGE FLUX FROM TRANSMITTER: $\phi\ (\mu W) = \left[E_1 \left(\frac{\mu W}{cm^2}\right)\right] \left[d^2 (cm^2)\right] \left[\left(\frac{\phi}{I}\right)_{MAX}\right]$

$\left(\frac{\phi}{I}\right)_{MAX}$ IS THE MAXIMUM VALUE OF THE RADIATION PATTERN INTEGRAL: $\frac{\phi(\theta)}{I(0)}$ (SEE DATA SHEET)

(a) MEASUREMENT OF TRANSMITTER AVERAGE FLUX



GENERAL PROCEDURE SAME AS ABOVE

3. WITH TRANSMITTER CONNECTOR SEATED, CENTER RECEIVER CONNECTOR OVER DETECTOR, THEN POSITION AGAINST GLASS. (DO NOT SLIDE – SLIDING MAY CAUSE SCRATCH DAMAGE.) OBSERVE E_O (μW/cm²).
4. WITHOUT ROTATING THE BODY, ROTATE THE COUPLING BY SMALL INCREMENTS OF TURNS, NOTING THE NUMBER OF TURNS, N, AND FOR EACH VALUE OF N: OBSERVE E_N (μW/cm²).

RECEIVER INPUT FLUX, AT OPERATING LEVEL $\phi_O\ (\mu W) = \frac{[E_O\ (\mu W/cm^2)]\ [A_D\ (cm^2)]}{\tau_F \text{ (SEE ABOVE)}}$

FLUX DECOUPLING (SEE FIG. 19) $\alpha_N = 10 \log_{10}(E_O / E_N)$

(b) MEASUREMENT OF AVERAGE RECEIVER INPUT FLUX AND FLUX DECOUPLING AT TRANSMITTER CONNECTOR.

Figure 20. Flux Measurement with EG&G Mod 550 Radiometer.

incidance, E, in W/cm² on an aperture area, A_D = 1 cm² and N.A. = 1. With the filter removed, a fiber optic cable can be placed so close to the aperture that there is no flux loss, and since the radiometer N.A. exceeds the fiber N.A., the radiometer will have a reading in W/cm² which is numerically equal to the flux in watts. However, a correction must be made for the removal of the filter.

The insertion loss of the filter must be evaluated at the measurement wavelength because it varies with wavelength to compensate for spectral variation in the response of the silicon detector. The arrangement shown in Figure 20 for measurement of radiant intensity is a good one for measuring insertion loss of the filter. Two observations are made — one with and one without the filter. Error due to ambient radiation is avoided by working in subdued ambient and for each observation taking two radiometer readings (source off and source on); the difference in readings is the observation of the radiant incidance, E_e, produced by the radiant intensity, I_e, of the source. The ratio of the two observations gives:

$$(28)\ \text{FILTER INSERTION LOSS, } \alpha_F = 10 \log \frac{E_{e(\text{filter out})}}{E_{e(\text{filter in})}}$$

This same arrangement can be used to measure the average flux of the Transmitter as shown in Figure 20b. From the observation of E_e with the filter IN:

$$(29)\ \text{AVERAGE INTENSITY, } I_e\left(\frac{\mu W}{sr}\right) = E_e\left(\frac{\mu W}{cm^2}\right) \times d^2\ (cm^2)$$

$$(30)\ \text{AVERAGE FLUX, } \phi_e(\mu W) = I_e \left(\frac{\mu W}{sr}\right)\left[\frac{\phi(\theta)}{I(0)}\ (MAX)\right]$$

(from Equation (29); value from radiation pattern integral in Transmitter Data Sheet)

SYSTEM MAINTENANCE

Preventive Maintenance

Long-term degradation occurs in any LED and LED degradation affects the Hewlett-Packard Fiber Optic System in two ways: reduced average flux, affecting either externally- or internally-coded mode, and altered flux excursion ratio, affecting only the internally-coded mode. Significant degradation of either the flux or the flux excursion ratio can be detected by regular observation of the flux margin, α_M, and of k.

α_M is evaluated as explained under Operating Margin Measurement from Equation (27). A plot of α_M against the logarithm of the cumulative hours of operation will allow an estimate to be made of the operating time remaining until α_M = 0 FOR THE P_e DESIRED.

k must be evaluated by measuring ϕ_H, ϕ_M, and ϕ_L as explained in the Transmitter description. The Test Point voltage can be used in making this measurement — see Equation (15). The upper and lower margins on k for a particular Receiver can be found by operating the Transmitter with Mode Select "high" and a rectangular signal (f ≈ 500kHz) at Data Input. As the duty factor of the signal is varied, the limits on k are found as those at which the Receiver fails to follow the Data Input signal.

$$(31)\ k = \left(\frac{1}{ft_P}\right) - 1 = \frac{1}{\frac{1}{ft_N} - 1}$$

where ft_P is the positive-pulse duty factor
ft_N is the negative-pulse duty factor

Changes in k do not affect externally-coded mode performance, and if this mode is used, then flux margin, α_M, is the only concern.

Corrective Maintenance

Trouble in the System may range from complete breakdown to excessive BER. The flux used in the Hewlett-Packard System is visible so the cause of complete breakdown can sometimes be localized by simply looking at the output of the Cable and the Transmitter. If there is visible output from the cable, then, when the Cable is connected to the Receiver, there should be an 8mV change in Test Point voltage, V_T, as the Transmitter (Mode Select "low") is turned on and off by switching V_{CC}. If ΔV_T is more than 8mV but the system is not working, then either the Receiver logic is not functioning properly or the flux excursion ratio, k, is either too high or too low. Excursion ratio can be checked as described above, using V_T. If k is satisfactory, the logic malfunction could be due to incorrect supply voltage or output loading.

If the System is functioning but has excessive BER, either the flux and flux excursion ratio are marginal (can be checked as described above) or there is too much interference from noise or other effects. If the Data Input voltage levels are correct, either random noise is high or errors are occurring due to incorrect supply voltage or output loading, or due to noise on the supply line. Random noise effects can be checked by lowering the flux level to a point where P_e is measurably high. If P_e varies with flux level according to P_e = erfc(X), as in Equation (26), then the problem is excessive random noise. Random noise can also be checked by changing the data rate while the flux level is low enough to make P_e measurable. If P_e is the same at any data rate, the problem is excessive random noise. Excessive random noise is more likely to occur in the Receiver than in the Transmitter; the best way to check is by replacement of the Receiver. Noise on the supply line is difficult to trace. If there is any doubt, the Receiver should be operated from its own supply (e.g., a 5V regulator). Receiver noise should be low enough to make $P_e < 10^{-9}$ at 10 Mbaud with normal flux level ($\Delta V_T > 8$ mV by the method described above indicates normal flux level).

HEWLETT PACKARD

APPLICATION NOTE 1001

Interfacing the HDSP-2000 to Microprocessor Systems

INTRODUCTION

Over the past two years, the need for alphanumeric displays has grown very rapidly due to the extensive use of microprocessors in new systems design. The presence of the microprocessor in such systems substantially simplifies the traditionally difficult task of designing an alphanumeric display into a system. This task is further simplified by using a display element such as the HDSP-2000 which has in one package a four character display, as well as most of the basic electronics necessary to drive the display. Depending upon overall systems configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, one may choose several different partitioning schemes to drive such a display.

This note will deal with four different techniques (see Figure 1) for interfacing the HDSP-2000 display to microprocessor systems:

1. The REFRESH CONTROLLER interrupts the microprocessor at a 500 Hz rate to request refresh data for the display.
2. The DECODED DATA CONTROLLER accepts 5 x 7 matrix data from the microprocessor and then automatically refreshes the display with the same information until new data is supplied by the microprocessor.
3. The RAM CONTROLLER accepts ASCII data and interfaces like a RAM to the microprocessor.
4. The DISPLAY PROCESSOR CONTROLLER (HDSP-247X series) employs a dedicated single chip microprocessor as a data display/control/keyboard interface which has many of the features of a complete terminal.

The interface techniques depicted are specifically for the 8080A or 6800 microprocessor families. Extension of these techniques to other processors should be a relatively simple software chore with little or no hardware changes required.

COMPARISON OF INTERFACE TECHNIQUES

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. The REFRESH CONTROLLER provides the lowest cost interface because it uses the microprocessor to provide ASCII decoding and display strobing. Because the ASCII decoder is located within the microprocessor system, the designer has total control over the display font within the program. This feature is particularly important when the system will be used to display different languages and special graphic symbols. However, the REFRESH CONTROLLER requires a significant amount of microprocessor time. Furthermore, while the interrupt allows the refresh program to operate asynchronously from the main program, this technique limits some of the software techniques that can be used in the main program.

The DECODED DATA CONTROLLER requires microprocessor interaction only when the display message is changed. Like the REFRESH CONTROLLER, the ASCII decoder is located within the microprocessor program. However, the time required to decode the ASCII string and store the resulting 5 x 7 display data into the interface requires several milliseconds of microprocessor time.

The RAM CONTROLLER also requires interaction from the microprocessor system only when the display message is changed. Because the ASCII decoder is located within the display interface, the microprocessor requires much less time to load a new message into the display.

The DISPLAY PROCESSOR CONTROLLER, the HDSP-247X series, is the most powerful interface. The software within the DISPLAY PROCESSOR CONTROLLER further reduces the microprocessor interaction by providing more powerful left and right data entry modes compared to the RAM entry mode of the DECODED DATA and RAM CONTROLLERS. The DISPLAY PROCESSOR CONTROLLER can also provide features such as a Blinking Cursor, Editing Commands, and a Data Out function. One version of the DISPLAY PROCESSOR CONTROLLER allows the user to provide a custom ASCII decoder for applications needing a special character font.

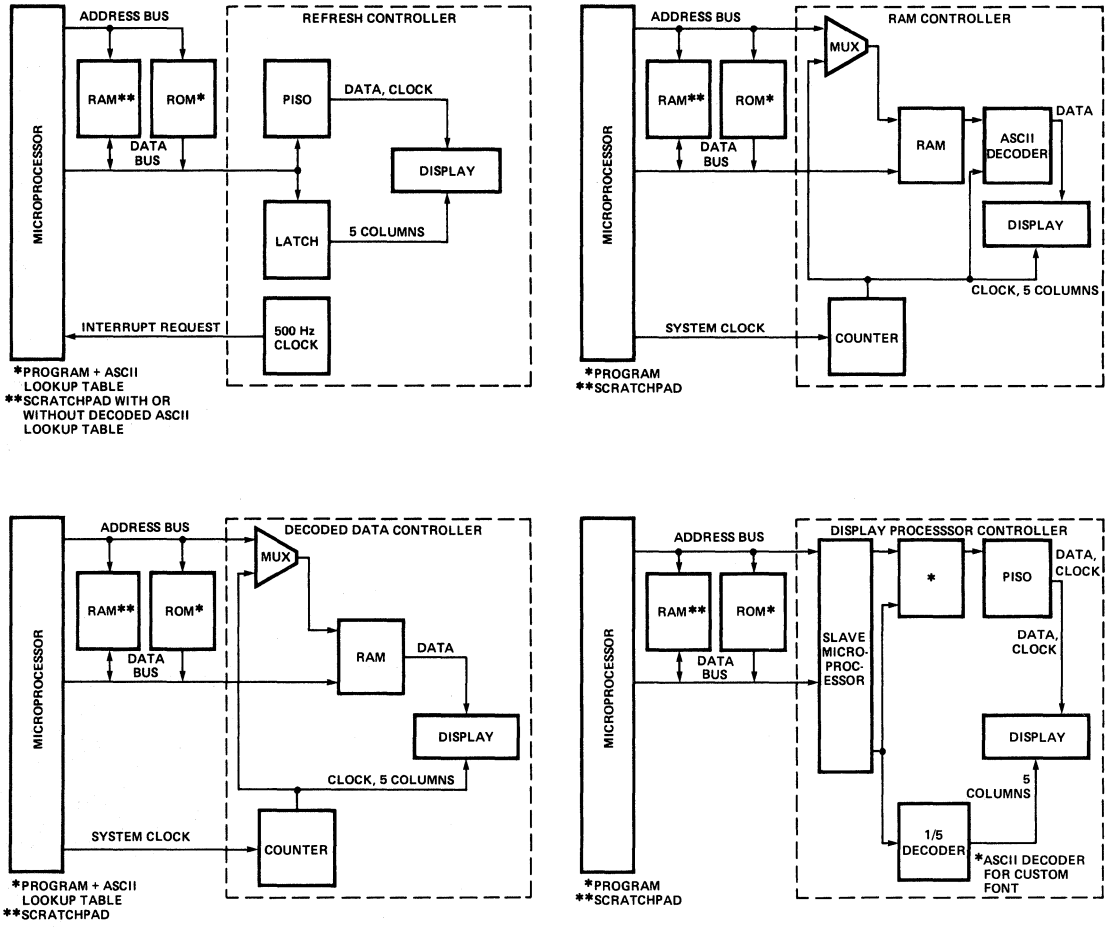


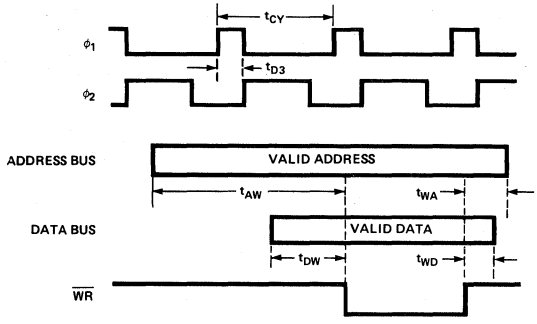
Figure 1. Four Different Techniques to Interface the HDSP-2000 Alphanumeric Display to a Microprocessor System

MICROPROCESSOR OVERVIEW

In order to effectively utilize the interface techniques listed above, an understanding of microprocessor fundamentals is required. A microprocessor system usually consists of a microprocessor, ROM memory, RAM memory, and some specific I/O interface. The microprocessor performs the desired system function by executing a program stored within the ROM. The RAM memory is used to provide a stack for the microprocessor, as well as a temporary scratchpad memory. The I/O interface consists of circuitry that is used as an input to the system as well as an output from the system. The alphanumeric display subsystem would be considered part of this interface. The microprocessor interfaces to this system through an Address Bus, a Data Bus, and a Control Bus. The Address Bus consists of several outputs from the microprocessor (A_0, A_1...A_n) which collectively specify a binary number. This number or "address" uniquely specifies each word in the ROM memory, RAM memory, and I/O interface. The Data Bus consists of several lines from the microprocessor which are used both as inputs and outputs. The Data Bus serves as an input during a memory or I/O read operation and as an output for a memory or I/O write operation. The Control Bus provides the required signals and timing to the rest of the microprocessor system to distinguish a memory read from a memory write, and in some systems an I/O read from an I/O write. These control lines and the timing between the Address, Data, and Control Buses vary for different microprocessors.

For the 8080A microprocessor, the Address Bus consists of 16 lines, the Data Bus consists of 8 lines, and the Control Bus consists of several lines including DBIN (Data Bus In), $\overline{WR}$ (Write), and clock signals ϕ_1 and ϕ_2. DBIN and $\overline{WR}$ are used to specify a memory read or write. The 8080A microprocessor provides several other control lines which are usually decoded with DBIN and $\overline{WR}$ to generate composite control signals $\overline{MEM\ R}$ (Memory Read), $\overline{MEM\ W}$ (Memory Write), $\overline{I/O\ R}$ (I/O Read), and $\overline{I/O\ W}$ (I/O Write). Since the alphanumeric display subsystem is an

output of the microprocessor system, the timing between the Address Bus, Data Bus, and $\overline{WR}$ is of particular significance. This timing is generalized in Figure 2.



8080 MICROPROCESSOR WITH 8228 CLOCK	MINIMUM TIMES (ns)			
	t_{AW}	t_{WA}	t_{DW}	t_{WD}
8080A, t_{CY} = 480	740	90	230	90
8080A-2, t_{CY} = 380	560	80	140	80
8080A-1, t_{CY} = 320	470	70	110	70

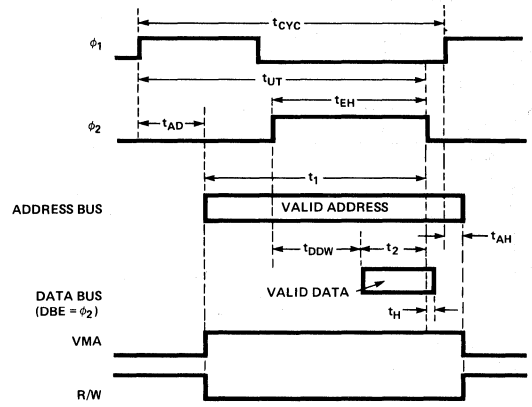
$t_{AW} = 2t_{CY} - t_{D3} - [140(A), 130(A\text{-}2), 110(A\text{-}1)]$

$t_{WA} = t_{WD} = t_{D3} + 10$

$t_{DW} = t_{CY} - t_{D3} - [170(A), 170(A\text{-}2), 150(A\text{-}1)]$

From INTEL Component Data Catalog, 1978

Figure 2. Memory Write Timing for the Intel 8080A Microprocessor Family



6800 MICROPROCESSOR	MINIMUM TIMES (ns)			
	t_1	t_{AH}	t_2	t_H
6800, t_{CYC} = 1000	630	30	225	10
68A00, t_{CYC} = 666	420	30	80	10
68B00, t_{CYC} = 500	290	30	60	10

$t_1(MIN) = t_{UT}(MIN) - t_{AD}(MAX)$

$t_2(MIN) = t_{EH}(MIN) - t_{DDW}(MAX)$

From MOTOROLA Semiconductor MC6800 Data Sheet (DS9471), 1978

Figure 3. Memory Write Timing for the Motorola 6800 Microprocessor Family

The 6800 microprocessor has a 16 line Address Bus, 8 line Data Bus, and a Control Bus that includes the signals VMA (Valid Memory Address), R/W (Read/Write), DBE (Data Bus Enable), and clock signals ϕ_1 and ϕ_2. R/W specifies either a memory read or write while VMA is used in conjunction with R/W to specify a Valid Memory Address. DBE gates the internal data bus of 6800 into the Data Bus. In many applications, DBE is connected to ϕ_2. The timing between the Address Bus, Data Bus, VMA, and R/W (when DBE = ϕ_2) is shown in Figure 3. Additional data hold time, t_H, can be achieved by delaying ϕ_2 to the microprocessor or by extending DBE beyond the falling edge of ϕ_2.

The ASCII to 5 x 7 dot matrix decoder used by the REFRESH CONTROLLER and DECODED DATA CONTROLLER is located within the microprocessor program. This decoder requires 640 bytes of storage to decode the 128 character ASCII set. The decoder used by these controllers is formatted so that the first 128 bytes contain column 1 information; the next 128 bytes contain column 2 information, etc. Each byte of this decoder is formatted such that D_6 through D_0 contain Row 7 through Row 1 display data respectively. The data is coded so that a HIGH bit would turn the corresponding 5 x 7 display dot ON. This decoder table is shown in Figure 20. The resulting 5 x 7 dot matrix display font is shown in the HDSP-2471 data sheet.

REFRESH CONTROLLER

The REFRESH CONTROLLER circuit depicted in Figure 4 is designed for interface to either 6800 or 8080A microprocessors. This circuit operates by interrupting the microprocessor every two milliseconds to request a new block of display data and column select data. Display data is loaded from the data bus into the serial input of the HDSP-2000 via a 74165 parallel in, serial out shift register. The 74LS293 counter and associated gates insure that only seven clock pulses are delivered to the shift register and the HDSP-2000 for each word loaded. Column Select data is loaded into a 74174 latch which, in turn, drives the column switch transistors. The circuit timing relative to the microprocessor clock and I/O is depicted in Figure 5.

The 6800 software necessary to support this interface is divided into two separate subroutines, "RFRSH" and "LOAD" (Figure 6). This approach is desirable to minimize microprocessor involvement during display refresh. The subroutine "RFRSH" loads a new set of decoded display data from the microprocessor scratchpad memory into the interface at each interrupt request. The subroutine "LOAD" is utilized to decode a string of 32 ASCII characters into 5 x 7 formatted display data and store this data in the scratchpad memory used by "RFRSH".

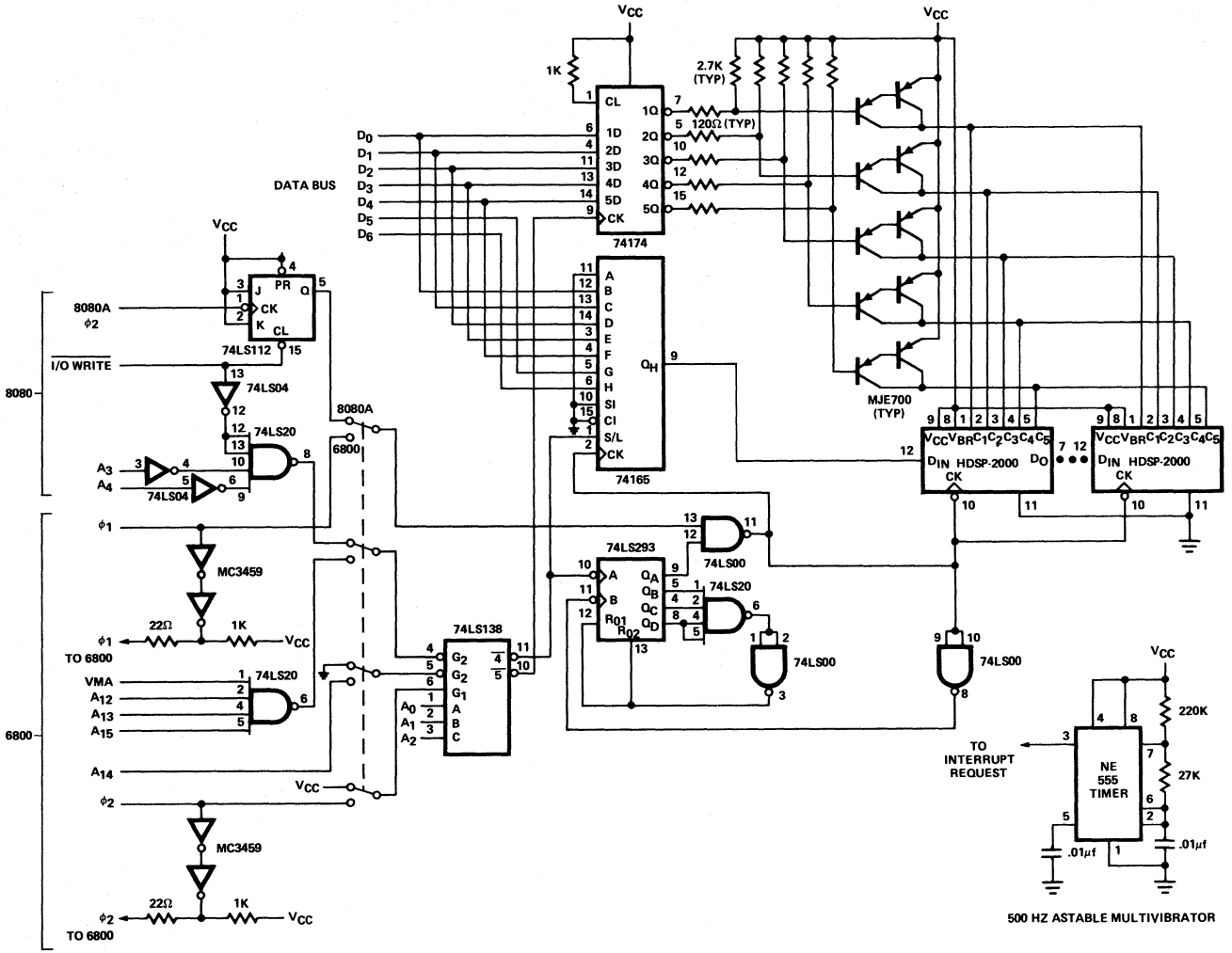


Figure 4. 6800 or 8080A Microprocessor Interface to the HDSP-2000 REFRESH CONTROLLER

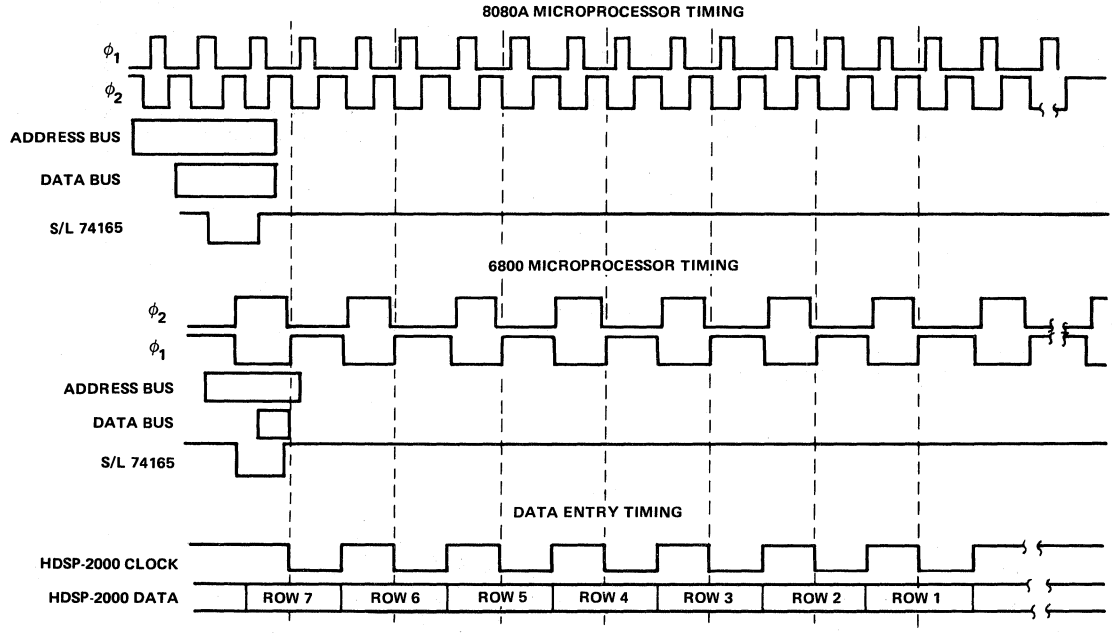


Figure 5. REFRESH CONTROLLER Timing

Figures 7a and 7b depict two different software routines for interfacing the REFRESH CONTROLLER to an 8080A microprocessor. The two subroutines shown in Figure 7a are functional replacements for the 6800 program shown in Figure 6. The programs shown in Figures 6 and 7a require a 5n byte scratchpad memory where n is the display length. The routine in Figure 7b eliminates this scratchpad memory by decoding and loading data each time a new interrupt request is received.

Because the microprocessor system is interrupted every 2ms, proper software design is especially important for the REFRESH CONTROLLER. The use of the scratchpad memory significantly reduces the time required to refresh the display. The fastest program, shown in Figure 6, uses in-line code to access data from the buffer and output it to the display. This program requires 3.7% + .50n% of the available microprocessor time for a 1MHz clock. The program shown in Figure 7a is similar to the one shown in Figure 6, except that it uses a program loop instead of the in-line code. This program uses 5.4% + .93n% of the microprocessor time for a 2MHz clock. These programs utilize a subroutine "LOAD" which is called whenever the display message is changed. This subroutine executes in 10.2ms and 7.5ms respectively for Figure 6 and Figure 7a. The program in Figure 7b uses 7.6% + 1.35n% of the microprocessor time for a 2MHz clock. A 50% reduction in the previously described microprocessor times can be achieved by using faster versions of the 6800 and 8080A microprocessors.

```
LOC   OBJECT CODE     SOURCE STATEMENTS
                      *
                      *
      BF 05           CDVR    EQU     $BF05
      BF 04           RDVR    EQU     $BF04
      06 00           DECDR   EQU     $0600
0000                  POINT   RMB     2
0002                  COLMN   RMB     1
0003                  COUNT   RMB     2

0005  00 AD           ASCII   FDB     DATA
0007                  DISPNT  RMB     2
0009                  DCRPNT  RMB     2
000B                  COLCNT  RMB     1
000C                  DIGCNT  RMB     1

000D                  BUFFR   RMB     160
00AD                  DATA    RMB     32

0400                  ORG     $0400
0400  86 FF           RFRSH   LDA A   I, $FF
0402  B7 BF 05                STA A   E, CDVR
0405  DE 00                   LDX     D, POINT
0407  A6 00           LOOPHH  LDA A   X, 0
0409  B7 BF 04                STA A   E, RDVR
040C  A6 01                   LDA A   X, 1
040E  B7 BF 04                STA A   E, RDVR
                              •
                              •
                              •
04A2  A6 1F                   LDA A   X, 31
04A4  B7 BF 04                STA A   E, RDVR
04A7  96 02                   LDA A   D, COLMN
04A9  B7 BF 05                STA A   E, CDVR
04AC  81 EF                   CMP A   I, $EF
04AE  27 10                   BEQ     LOOPB
04B0  D6 00                   LDA B   D, POINT +1
04B2  CB 20                   ADD B   I, 32
04B4  D7 00                   STA B   D, POINT +1
04B6  24 03                   BCC     LOOPA
04B8  7C 00 00                INC     E, POINT
04BB  0D              LOOPA   SEC
04BC  79 00 02                ROL     E, COLMN
04BF  3B                      RTI
04C0  CE 00 0D        LOOPB   LDX     I, BUFFR
04C3  DF 00                   STX     D, POINT
04C5  DE 03                   LDX     D, COUNT
04C7  09                      DEX
04C8  DF 03                   STX     D, COUNT
04CA  86 FE                   LDA A   I, $FE
04CC  97 02                   STA A   D, COLMN
04CE  3B                      RTI

04CF  5F              LOAD    CLR B
04D0  CE 00 0D                LDX     I, BUFFR
04D3  DF 07                   STX     D, DISPNT
04D5  86 06                   LDA A   I, <DECDR
04D7  97 09                   STA A   D, DCRPNT
04D9  86 05                   LDA A   I, 5
04DB  97 0B                   STA A   D, COLCNT
04DD  86 20           LOOP1   LDA A   I, 32
04DF  97 0C                   STA A   D, DIGCNT
04E1  9B 06                   ADD A   D, ASCII+1
04E3  24 03                   BCC     LOOP2
04E5  7C 00 05                INC     E, ASCII
04E8  97 06           LOOP2   STA A   D, ASCII+1
04EA  DE 05           LOOP3   LDX     D, ASCII
04EC  09                      DEX
04ED  A6 00                   LDA A   X, 0
04EF  DF 05                   STX     D, ASCII
04F1  1B                      ABA
04F2  97 0A                   STA A   D, DCRPNT+1
04F4  DE 09                   LDX     D, DCRPNT
04F6  A6 00                   LDA A   X, 0
04F8  DE 07                   LDX     D, DISPNT
04FA  A7 00                   STA A   X, 0
04FC  08                      INX
04FD  DF 07                   STX     D, DISPNT
04FF  7A 00 0C                DEC     E, DIGCNT
0502  26 E6                   BNE     LOOP3
0504  CB 80                   ADD B   I, $80
0506  24 03                   BCC     LOOP4
0508  7C 00 09                INC     E, DCRPNT
050B  7A 00 0B        LOOP4   DEC     E, COLCNT
050E  26 CD                   BNE     LOOP1
0510  39                      RTS
```

Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS
0004                  RDVR    EQU     0004H
0005                  CDVR    EQU     0005H
E500                  DECDR   EQU     0E500H

                      ORG     0E000H
E000  05 E0           POINT   DW      BUFFR
E002  FE              COLMN   DB      0FEH
E003  FF FF           COUNT   DW      0FFFFH
E005  00              BUFFR   DS      160

                      ORG     0E0A5H
E0A5  A7 E0           ASCII   DW      DATA
E0A7  00              DATA    DS      32

                      ORG     0E400H
E400  F5              RFRSH   PUSH    PSW
E401  C5                      PUSH    B
E402  E5                      PUSH    H
E403  2A 00 E0                LHLD    POINT
E406  06 20                   MVI     B, 32
E408  3E FF                   MVI     A, 0FFH
E40A  D3 05                   OUT     CDVR
F40C  7E              LOOP    MOV     A, M
E40D  D3 04                   OUT     RDVR
E40F  23                      INX     H
E410  05                      DCR     B
E411  C2 0C E4                JNZ     LOOP
E414  3A 02 E0                LDA     COLMN
E417  D3 05                   OUT     CDVR
E419  FE EF                   CPI     0EFH
E41B  CA 28 E4                JZ      FIRST
E41E  22 00 E0                SHLD    POINT
E421  07                      RLC
E422  32 02 E0                STA     COLMN
E425  C3 3A E4                JMP     END
E428  21 05 E0        FIRST   LXI     H, BUFFR
E42B  22 00 E0                SHLD    POINT
E42E  3E FE                   MVI     A, 0FEH
E430  32 02 E0                STA     COLMN
E433  2A 03 E0                LHLD    COUNT
E436  2B                      DCX     H
E437  22 03 E0                SHLD    COUNT
E43A  E1              END     POP     H
E43B  C1                      POP     B
E43C  F1                      POP     PSW
E43D  C9                      RET

E43E  11 24 E0        LOAD    LXI     D, BUFFR+31
E441  0E 20                   MVI     C, 32
E443  2A A5 E0        LOOP1   LHLD    ASCII
E446  7E                      MOV     A, M
E447  23                      INX     H
E448  22 A5 E0                SHLD    ASCII
E44B  26 E5                   MVI     H, DECDR/256
E44D  6F                      MOV     L, A
E44E  06 05                   MVI     B, 5
E450  7E              LOOP2   MOV     A, M
E451  12                      STAX    D
E452  7D                      MOV     A, L
E453  C6 80                   ADI     80H
E455  6F                      MOV     L, A
E456  D2 5A E4                JNC     LOOP3
E459  24                      INR     H
E45A  7B              LOOP3   MOV     A, E
E45B  C6 20                   ADI     32
E45D  5F                      MOV     E, A
E45E  05                      DCR     B
E45F  C2 50 E4                JNZ     LOOP2
E462  7B                      MOV     A, E
E463  C6 5F                   ADI     5FH
E465  5F                      MOV     E, A
E466  0D                      DCR     C
E467  C2 43 E4                JNZ     LOOP1
E46A  C9                      RET
```

Figure 7a. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS

0004                  RDVR    EQU     0004H
0005                  CDVR    EQU     0005H
E500                  DECDR   EQU     0E500H

                              ORG     0E000H
E000  07 E0           ASCII   DW      DATA
E002  FE              COLMN   DB      0FEH
E003  FF FF           COUNT   DW      0FFFFH
E005  00 E5           BASE    DW      DECDR
E007  00              DATA    DS      32

                              ORG             0E400H
E400  F5              RFRSH   PUSH    PSW
E401  C5                      PUSH    B
E402  D5                      PUSH    D
E403  E5                      PUSH    H
E404  2A 05 E0                LHLD    BASE
E407  EB                      XCHG
E408  2A 00 E0                LHLD    ASCII
E40B  01 1F 00                LXI     B, 31
E40E  09                      DAD     B
E40F  43                      MOV     B, E
E410  0E 20                   MVI     C, 32
E412  3E FF                   MVI     A, 0FFH
E414  D3 05                   OUT     CDVR
E416  78              LOOP    MOV     A, B
E417  86                      ADD     M
E418  5F                      MOV     E, A
E419  1A                      LDAX    D
E41A  D3 04                   OUT     RDVR
E41C  2B                      DCX     H
E41D  0D                      DCR     C
E41E  C2 16 E4                JNZ     LOOP
E421  EB                      XCHG
E422  3A 02 E0                LDA     COLMN
E425  D3 05                   OUT     CDVR
E427  FE EF                   CPI     0EFH
E429  CA 3B E4                JZ      FIRST
E42C  07                      RLC
E42D  32 02 E0                STA     COLMN
E430  68                      MOV     L, B
E431  01 80 00                LXI     B, 0080H
E434  09                      DAD     B
E435  22 05 E0                SHLD    BASE
E438  C3 4D E4                JMP     END
E43B  3E FE           FIRST   MVI     A, 0FEH
E43D  32 02 E0                STA     COLMN
E440  21 00 E5                LXI     H, DECDR
E443  22 05 E0                SHLD    BASE
E446  2A 03 E0                LHLD    COUNT
E449  2B                      DCX     H
E44A  22 03 E0                SHLD    COUNT
E44D  E1              END     POP     H
E44E  D1                      POP     D
E44F  C1                      POP     B
E450  F1                      POP     PSW
E451  C9                      RET
```

Figure 7b. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the REFRESH CONTROLLER

DECODED DATA CONTROLLER

The DECODED DATA CONTROLLER circuit schematic for a 32 character display is depicted in Figure 8. The circuit is specifically designed for interface to an 8080A microprocessor. This circuit is designed to accept and store in local memory all of the display data for a 32 character HDSP-2000 display (1120 bits). The microprocessor loads 160 bytes of display data into the two 1K x 1 RAM's via the 74165 parallel in, serial out shift register. Each byte of data represents one column of display data. The counter string automatically generates the proper address location for each serial bit of data after initialization by $\overline{\text{MEM W}}$, the character address, and the desired column. Once the loading is complete, the counter sequentially loads and displays each column (224 bits) of data at a 90Hz rate (2MHz input clock rate). The timing for this circuit is shown in Figure 9. The software required to decode a 32 character ASCII string is shown in Figure 10. This program decodes the 32 ASCII characters into 160 bytes of display data which are then stored in the controller. The program requires about 6.6ms, for a 2MHz clock, to decode and load the message into the DECODED DATA CONTROLLER.

RAM CONTROLLER

The RAM CONTROLLER (Figure 11a) is designed to accept ASCII coded data for storage in a local 128 x 8 RAM. After the microprocessor has loaded the RAM, local scanning circuitry controls the decoding of the ASCII, the display data loading, and the column select function. With minor modification, the circuit can be utilized for up to 128 display characters. The RAM used in this circuit is an MCM6810P with the Address and Data inputs isolated via 74LS367 tristate buffers. This allows the RAM to be accessed either by the microprocessor or by the local electronics. The protocol is arranged such that the microprocessor always takes precedence over the local scanning electronics. The "Write" cycle timing for the RAM CONTROLLER is depicted in Figure 11b. This circuit, as with the DECODED DATA CONTROLLER, requires no microprocessor time once the local RAM has been loaded with the desired data.

DISPLAY PROCESSOR CONTROLLER

The previously mentioned interface techniques provide only for the display of ASCII coded data. Such important features as a blinking cursor, editing routines, and character addressing must be provided by other subroutines in the microprocessor software. The DISPLAY PROCESSOR CONTROLLER is a system which utilizes a dedicated 8048 single chip microprocessor to provide these important features. This controller, as depicted in Figure 12, is a series of printed circuit board subsystems available from Hewlett-Packard under the following part numbers:

HDSP-2470 — Controller with 64 character ASCII to 5 x 7 decoder
HDSP-2471 — Controller with 128 character universal ASCII to 5 x 7 decoder
HDSP-2472 — Controller with socket for user supplied custom coded ROM/PROM/EPROM.

All of the controllers have the following features:

- Choice of character string length:
  4-48 characters in increments of four characters
- Four modes of data entry
  Left Entry
  Right Entry
  RAM Entry (≤ 32 characters only)
  Block Entry
- Flashing Cursor — Left Entry Only
- Data Out (≤ 32 characters only)
- Edit Functions
  Clear Display, Backspace Cursor — RIGHT ENTRY
  Forwardspace Cursor, Insert, Delete — LEFT ENTRY

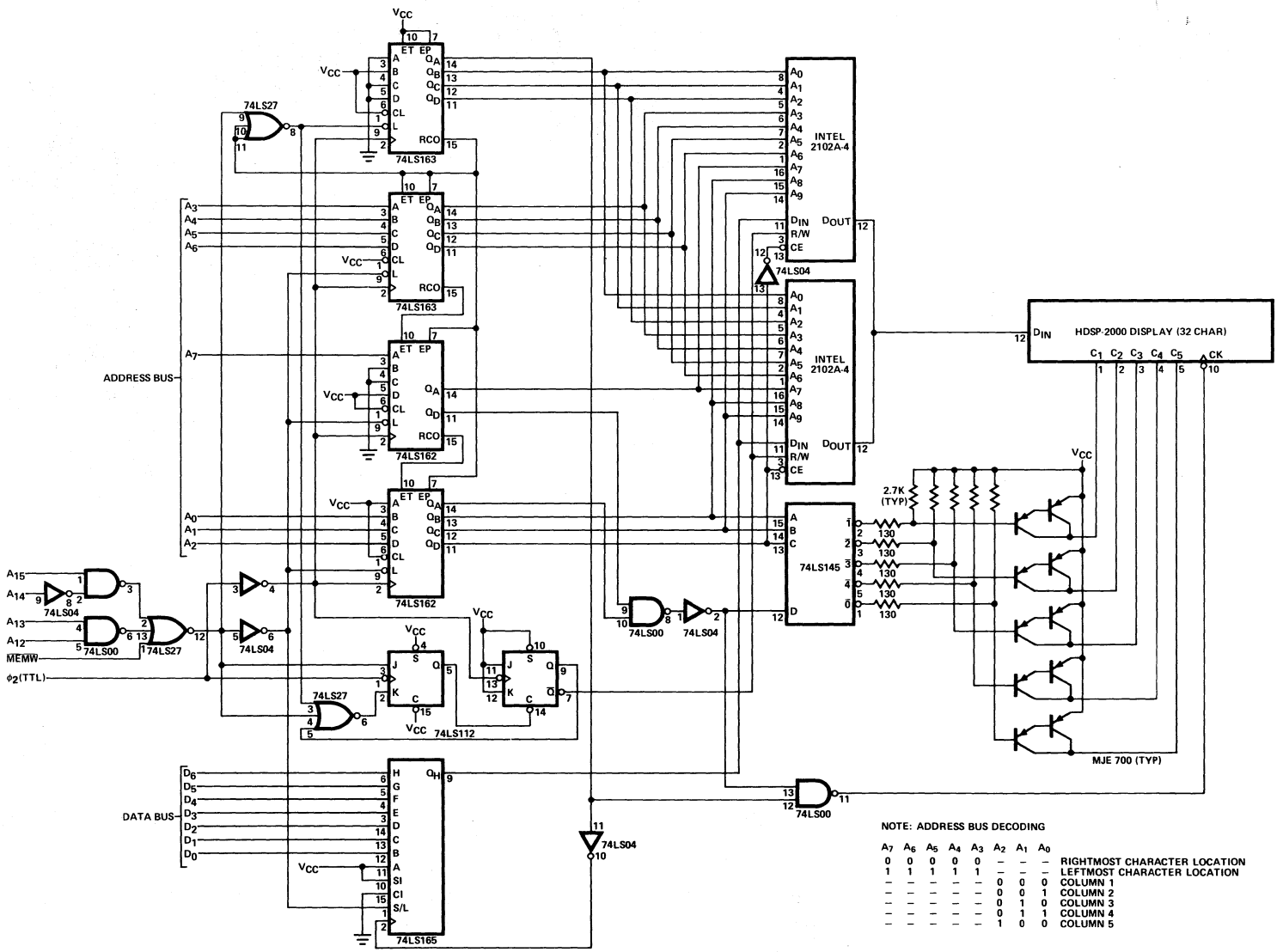


Figure 8. 8080A Microprocessor Interface to the HDSP-2000 DECODED DATA CONTROLLER

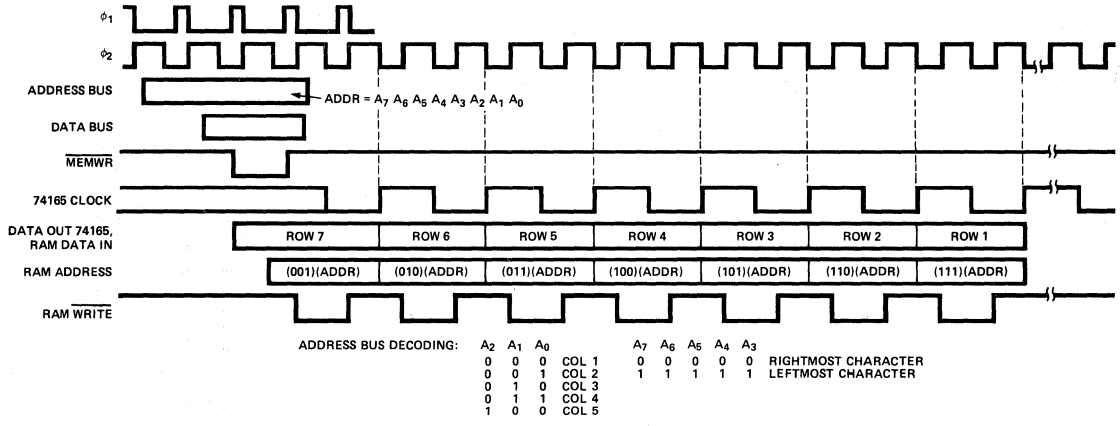


Figure 9. Data Entry Timing for DECODED DATA CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS

B000                  DISPL   EQU   0B000H
E500                  DECDR   EQU   0E500H

                      ORG     0E000H
E000  02  E0          ASCII   DW    DATA
E002  00              DATA    DS    32

                      ORG     0E400H
E400  11  F8  B0      LOAD    LXI   D, DISPL+00F8H
E403  0E  20                  MVI   C, 32
E405  2A  00  E0      LOOP1   LHLD  ASCII
E408  7E                      MOV   A, M
E409  23                      INX   H
E40A  22  00  E0              SHLD  ASCII
E40D  26  E5                  MVI   H, DECDR/256
E40F  6F                      MOV   L, A
E410  06  05                  MVI   B, 5
E412  7E              LOOP2   MOV   A, M
E413  12                      STAX  D
E414  13                      INX   D
E415  7D                      MOV   A, L
E416  C6  80                  ADI   80H
E418  6F                      MOV   L, A
E419  D2  1D  E4              JNC   LOOP3
E41C  24                      INR   H
E41D  05              LOOP3   DCR   B
E41E  C2  12  E4              JNZ   LOOP2
E421  7B                      MOV   A, E
E422  D6  0D                  SUI   13
E424  5F                      MOV   E, A
E425  0D                      DCR   C
E426  C2  05  E4              JNZ   LOOP1
E429  C9                      RET
```

Figure 10. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the DECODED DATA CONTROLLER

These controllers have been designed to eliminate the burden of data handling between keyboard, display, and microprocessor. The product data sheet describes the technical function of the controllers in detail.

Interfacing the controller to microprocessor systems depends on the needs of the particular application. Figures 13a and 13b depict latched interfaces from a master microprocessor to the HDSP-247X series of controllers. These interfaces are utilized to avoid having the master processor wait for the controller to accept data.

In sophisticated systems, it may be desirable to have the HDSP-247X controller handle all of the keyboard/display interface while the microprocessor reads edited messages from the controller DATA OUT port. This function can be achieved through the use of peripheral interface adapters (PIA) available from the microprocessor manufacturers. Figure 14 depicts a 6800 based system in which data may enter the display from either a keyboard or a microprocessor. This interface uses a 6821 PIA configured so that PB_7 controls whether the microprocessor or keyboard enters data into the controller. The 6800 program is shown in Figure 15. Subroutine "LOAD" uses CA_1 and CA_2 to provide a data entry handshake that allows the 6800 to load data into the controller as fast as the controller can accept it. After the prompting message has been loaded, the microprocessor turns the control of data entry over to the keyboard. A signal from the keyboard ("ER" in the example) sets a flag within the 6821. Depending on how the 6821 is configured, the microprocessor can either test the flag or allow the flag to automatically interrupt the microprocessor. Subroutine "READ" would then be used to read the DATA OUT

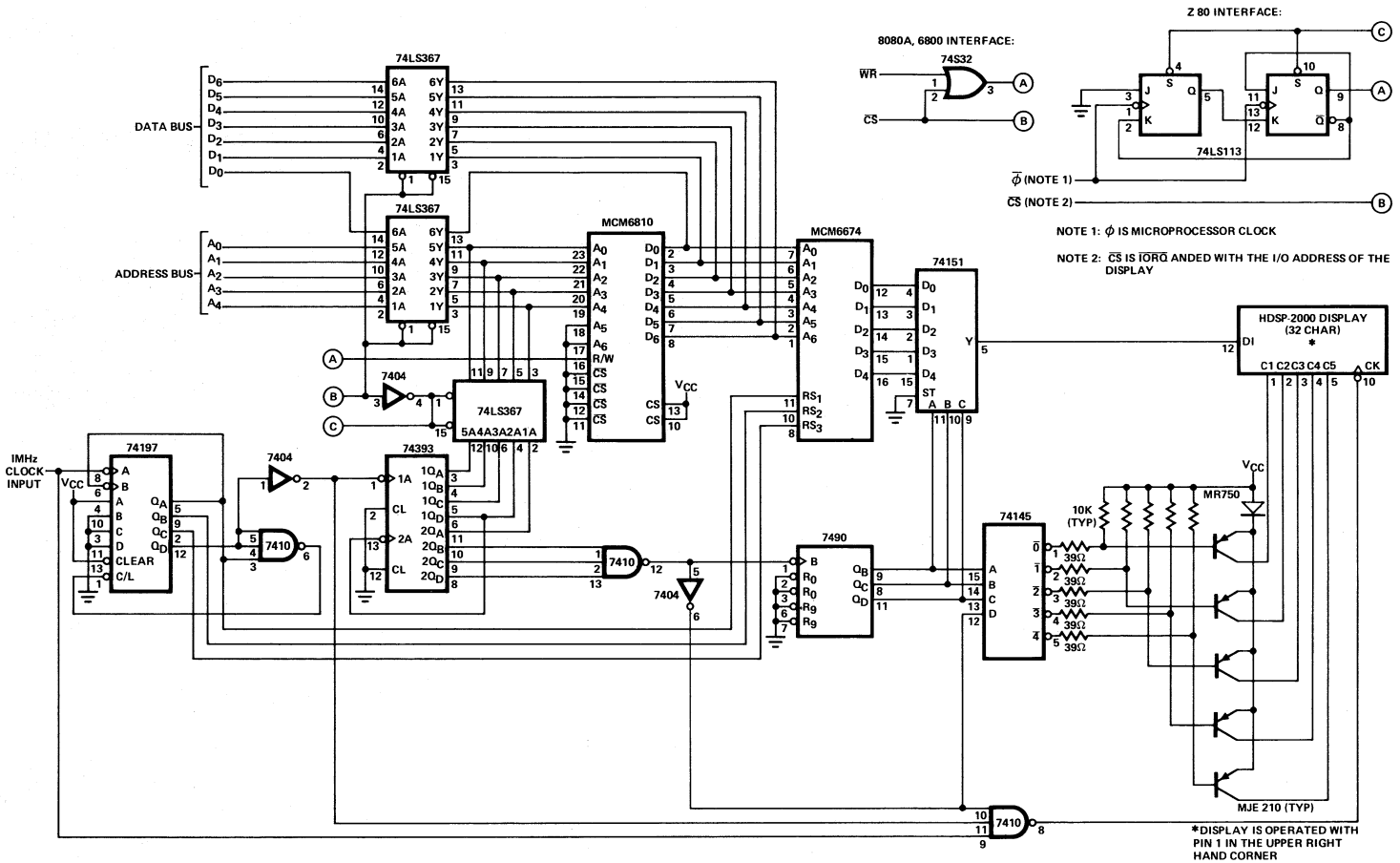


Figure 11a. 8080A Microprocessor Interface to the HDSP-2000 RAM CONTROLLER

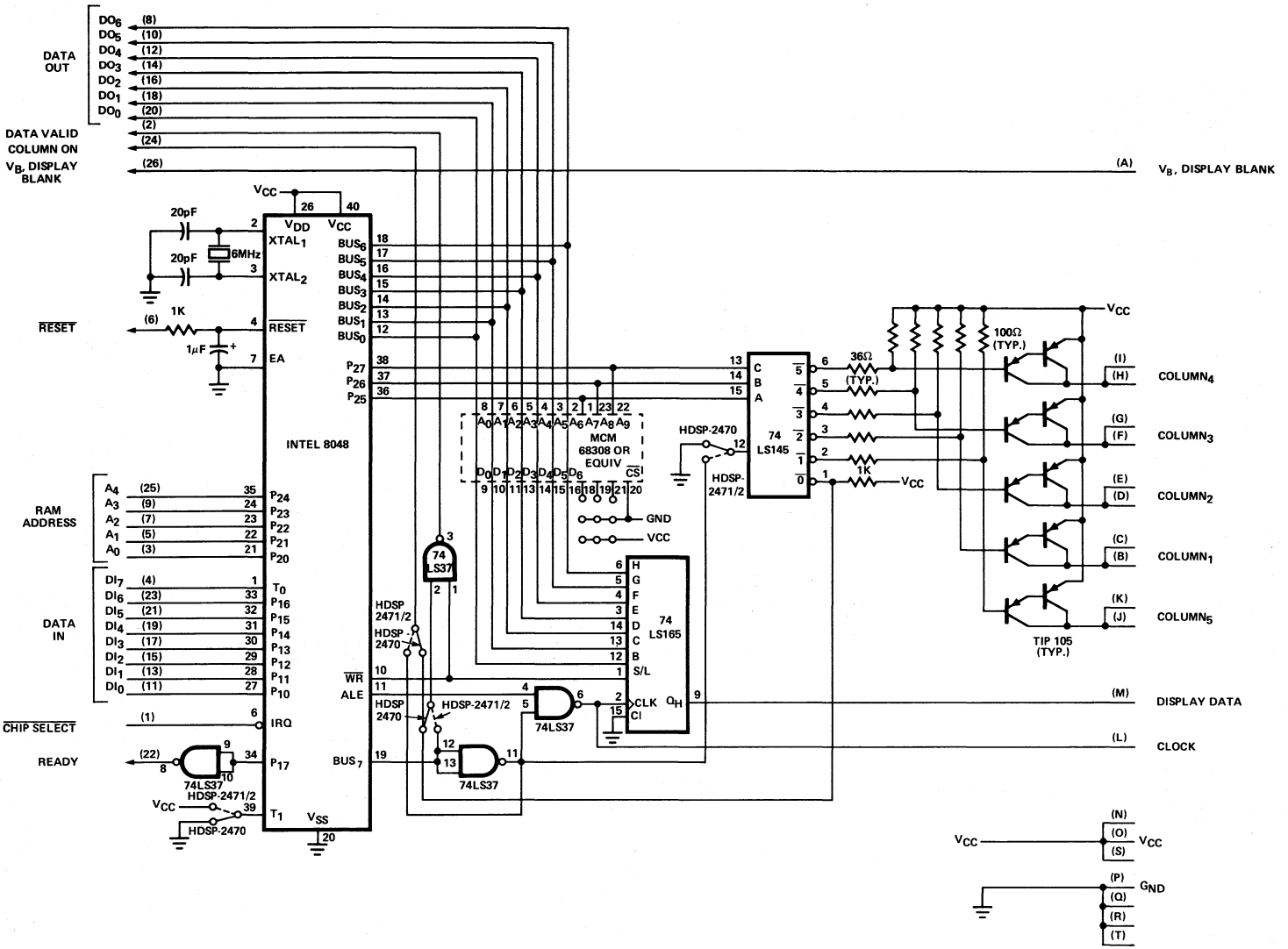
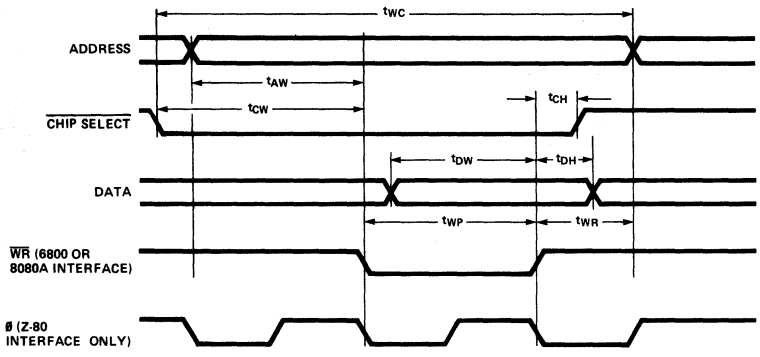


Figure 12. HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	390ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	220ns
DATA HOLD	t_{DH}	20ns
WRITE PULSE	t_{WP}	310ns
WRITE RECOVERY	t_{WR}	10ns
CHIP ENABLE HOLD	t_{CH}	20ns

Figure 11b. Memory Write Timing for the HDSP-2000 RAM CONTROLLER

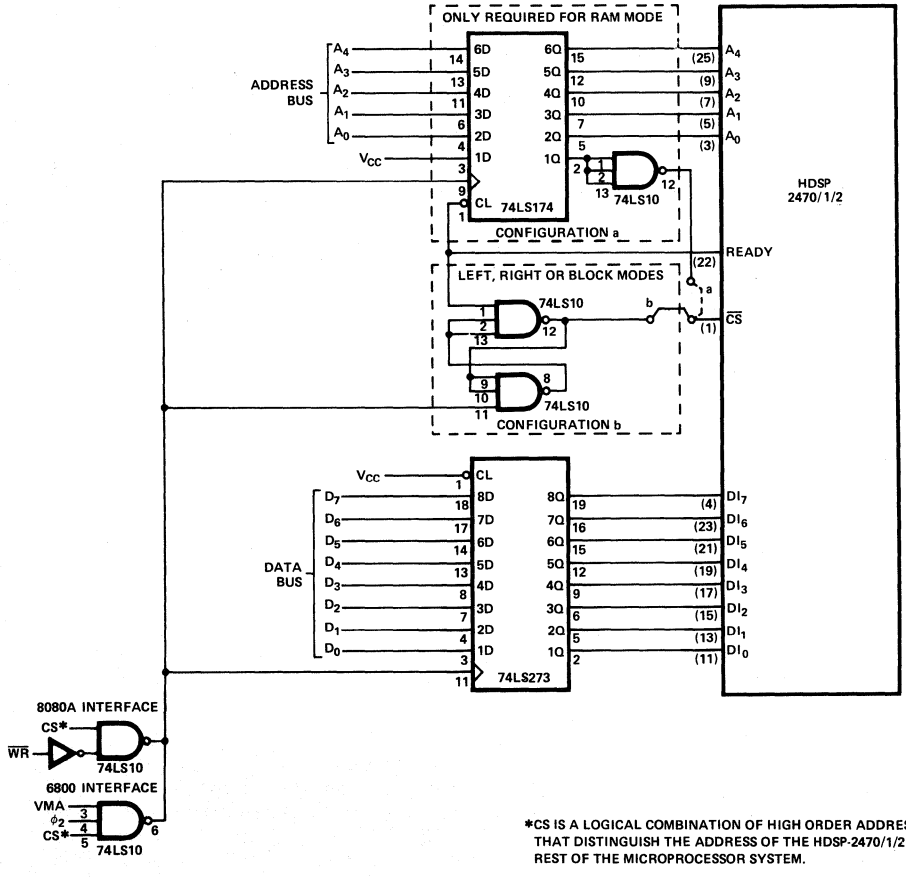


Figure 13. Latched Interface to the HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

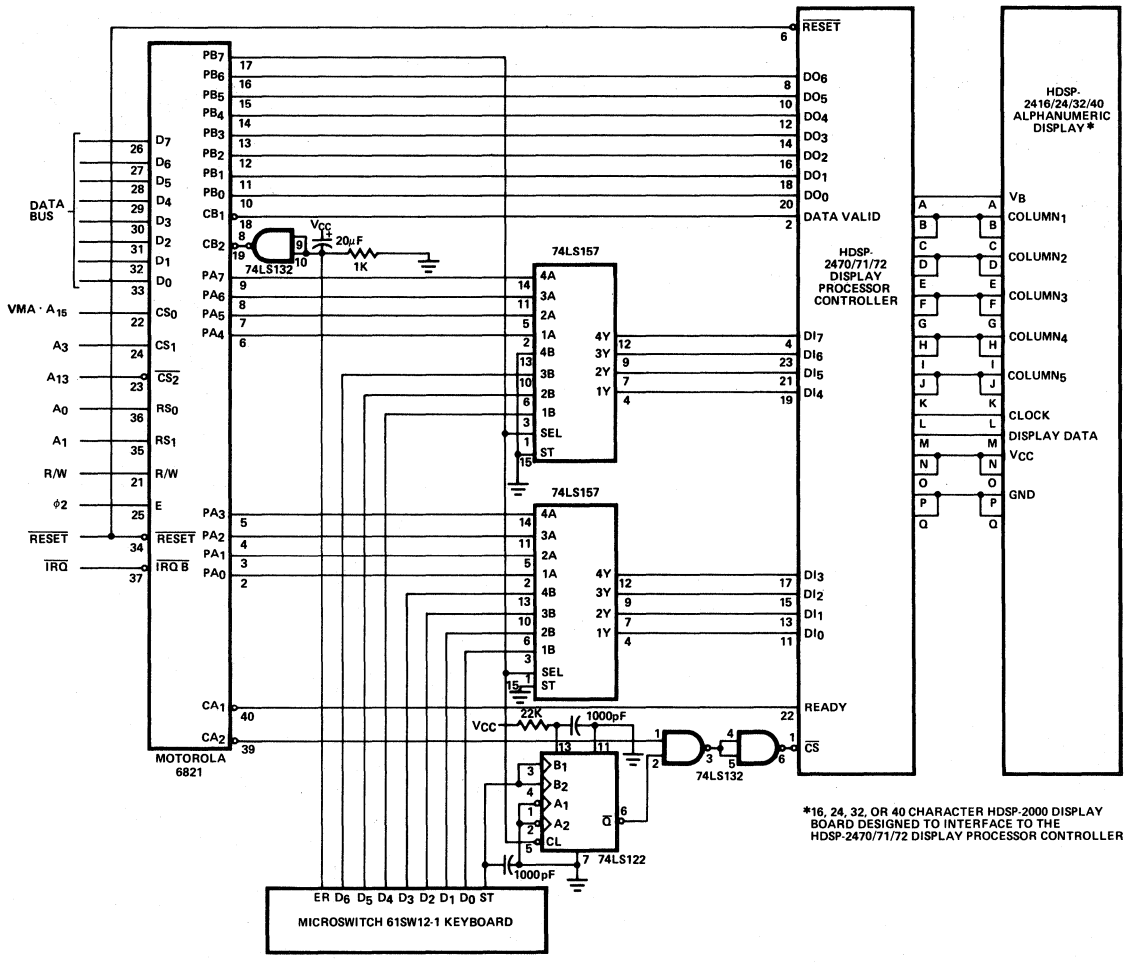


Figure 14. 6800 Microprocessor Interface Utilizing a 6820 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

outputs from the controller into the microprocessor system. The microprocessor uses the CB_1 input of the 6821 PIA to determine when to read each of the 34 data output words into the system.

A similar PIA interface for the 8080A microprocessor is depicted in Figures 16 and 17.

The HDSP-247X series of controllers are programmed to default to "Left Entry" mode for a 32 character string of displays. If some other entry mode or string length is desired, it is necessary to either load the appropriate control word from the microprocessor or to provide a control word during POWER ON RESET. The controller will read the DATA IN lines during RESET and interpret the contents as the control word. The circuit depicted in Figure 18 can be utilized to load any desired preprogrammed word into the HDSP-247X controller, during power on.

Under certain operating conditions, it may be desirable to vary the brightness of displays controlled by the HDSP-247X controllers. The circuit depicted in Figure 19 may be utilized to provide manual brightness control of the display through pulse width modulation. Automatic control may be achieved by substituting an appropriate value photoconductor for potentiometer R_1.

```
* PORT CONFIGURATION:
* 1.  PORT A:
*           PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
*           CA1  (INPUT) MODE 00 SET FLAG NEG EDGE OF READY
*           CA2  (OUTPUT) MODE 100 CLEARED MPU READ PRA, SET
*           NEG  EDGE OF READY
* 1.  PORT B:
*           PB0-PB6 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP-247X
*           CB1  (INPUT) MODE 00 SETS FLAG NEG EDGE OF DATA VALID
*           CB2  (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
*           CB2  (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
            CAUSING IRQ
*           PB7  (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
*                         HIGH ENABLES  KEYBOARD TO MUX
*

LOC   OBJECT     CODE     SOURCE STATEMENT

      8008       PRA      EQU    $8008
      8008       DRA      EQU    $8008
      8009       CRA      EQU    $8009
      800A       PRB      EQU    $800A
      800A       DRB      EQU    $800A
      800B       CRB      EQU    $800B

                          ORG    $0000
0000              MESSAGE  RMB    2

                          ORG    $0100
0100              STATUS   RMB    1
0101              CURSOR   RMB    1
0102              DATA     RMB    32

                          ORG    $0400
0400  CE 0100     READ     LDX    I, STATUS
0403  B6 800A     LOOP1    LDA A  E, PRB          CLEAR CB1 AND CB2
0406  5F                   CLR B
0407  5C          LOOP2    INC B
0408  B6 800B              LDA A  E, CRB
040B  2A FA                BPL    LOOP2           WAIT FOR DATA VALID
040D  C1 0A                CMP B  I, 10
040F  23 F2                BLS    LOOP1
0411  C6 21                LDA B  I, 33
0413  B6 800A     LOOP3    LDA A  E, PRB          READ AND CLEAR CB1
0416  84 7F                AND A  I, $7F
0418  A7 00                STA A  X, 0            STORE IN RAM
041A  B6 800B     LOOP4    LDA A  E, CRB
041D  2A FB                BPL    LOOP4           WAIT FOR DATA VALID
041F  08                   INX
0420  5A                   DEC B
0421  26 F0                BNE    LOOP3           READ DATA
0423  B6 800A              LDA A  E, PRB
0426  84 7F                AND A  I, $7F
0428  A7 00                STA A  X, 0
042A  39                   RTS

042B  DE 00     LOAD       LDX    D, MESSGE
042D  A6 00     LOOP10     LDA A  X, 0
042F  08                   INX
0430  81 FF                CMP A  I, $FF          LAST WORD IN STRING
0432  27 0D                BEQ    ENDL            JUMP WHEN DONE
0434  B7 8008              STA A  E, PRA
0437  7D 8008              TST    E, PRA          CLEAR CA1 AND CA2
043A  B6 8009     LOOP11   LDA A  E, CRA
043D  2A FB                BPL    LOOP11          WAIT
043F  20 EC                BRA    LOOP10
0441  DF 00     ENDL       STX    D, MESSGE
0443  39                   RTS

                          ORG    $0500
0500  7F 8009     START    CLR    E, CRA
0503  7F 800B              CLR    E, CRB
0506  86 FF                LDA A  I, $FF
0508  B7 8008              STA A  E, DRA
050B  86 24                LDA A  I, $24
050D  B7 8009              STA A  E, CRA
0510  86 80                LDA A  I, $80
0512  B7 800A              STA A  E, DRB
0515  86 04                LDA A  I, $04
0517  B7 800B              STA A  E, CRB

                  * PROCEDURE TO LOAD HDSP-247X SYSTEM
051A  0E                   CLI
051B  7F 800A              CLR    E, PRB          DISABLE KEYBD FROM MUX
051E  BD 042B              JSR    E, LOAD

                  * PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
0521  7D 800A              TST    E, PRB          CLEAR CB1, CB2
0524  86 80                LDA A  I, $80
0526  B7 800A              STA A  E, PRB          ENABLE KEYBD TO MUX
0529  86 0C                LDA A  I, $0C
042B  B7 800B              STA A  E, CRB          ENABLE IRQ,
052E  0F                   SEI                    IRQ CAUSE JSR TO READ
```

Figure 15. 6800 Microprocessor Program that Interfaces to the Circuit shown in Figure 14.

```
* PORT CONFIGURATION:
* 1.  PORT A (MODE 1 OUTPUT):
*           PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
*           PC7  (OBF) OUTPUT; TO CHIP SELECT
*           PC6 (ACK) INPUT; TO READY
*           FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
*
* 2.  PORT B (MODE 1 INPUT):
*           PB0-PB6 INPUTS DATA FROM DATA OUT OF HDSP-247X
*           PC2 (STB) INPUT; LOADS DATA ON NEG EDGE OF DATA VALID
*           FLAG PC0 (INTR) CLEARED BY INPUT; SET BY DATA VALID
*
* 3.  PORT C:
*           PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-247X
*                       HIGH ENABLES KEYBOARD TO HDSP-247X

LOC   OBJECT     CODE     SOURCE STATEMENTS

000C              PA       EQU    0CH
000D              PB       EQU    0DH
000E              PC       EQU    0EH
000F              CNTRL    EQU    0FH

                           ORG    0E000H
E000  02 E0       ASCII    DW     TEXT
E002  00          TEXT     DS     32

                           ORG    0E100H
E100  00          STAT     DB     0
E101  00          ADDR     DB     0
E102  00          DATA     DS     32

                           ORG    0E400H
E400  F3          READ     DI
E401  F5                   PUSH   PSW
E402  E5                   PUSH   H
E403  C5                   PUSH   B
E404  0E 20                MVI    C, 32
E406  21 00 E1             LXI    H, STAT         FIRST WORD
E409  DB 0D                IN     PB              CLEAR INTR
E40B  06 00       LOOP1    MVI    B, 0
E40D  DB 0E       LOOP2    IN     PC
E40F  04                   INR    B
E410  1F                   RAR
E411  D2 0D E4             JNC    LOOP2           WAIT UNTIL INTR IS SET
E414  3E 0A                MVI    A, 10
E416  B8                   CMP    B
E417  DB 0D                IN     PB
E419  D2 0B E4             JNC    LOOP1           WAIT UNTIL STATUS WORD
E41C  77          LOOP3    MOV    M, A            STORE IN RAM
E41D  23                   INX    H
E41E  DB 0E       LOOP4    IN     PC
E420  1F                   RAR
E421  D2 1E E4             JNC    LOOP4           WAIT UNTIL INTR IS SET
E424  DB 0D                IN     PB
E426  0D                   DCR    C
E427  C2 1C E4             JNZ    LOOP3
E42A  77                   MOV    M, A            STORE LAST WORD
E42B  C1                   POP    B
E42C  E1                   POP    H
E42D  F1                   POP    PSW
E42E  FB                   EI
E42F  C9                   RET

E430  2A 00 E0    LOAD     LHLD   ASCII          FIRST WORD OF MESSAGE
E433  7E          LOOP5    MOV    A, M
F434  FE FF                CPI    0FFH            CHECK TO SEE IF DONE
E436  CA 45 E4             JZ     ENDL
E439  D3 0C                OUT    PA              OUTPUT TO DISPLAY
E43B  23                   INX    H
E43C  DB 0E       LOOP6    IN     PC
E43E  17                   RAL
E43F  D2 3C E4             JNC    LOOP6           WAIT
E442  C3 33 E4             JMP    LOOP5           NEXT WORD
E445  23          ENDL     INX    H
E446  22 00 E0             SHLD   ASCII
E449  C9                   RET

E44A  3E A7       START    MVI    A, 0A7H         PA OUTPUT, PB INPUT
E44C  D3 0F                OUT    CNTRL
E44E  3E 0C                MVI    A, 0CH          CLEAR INTE A
E450  D3 0F                OUT    CNTRL
E452  3E 05                MVI    A, 05H
E454  D3 0F                OUT    CNTRL           SET INTE B

                  * PROCEDURE TO LOAD HDSP-247X SYSTEM
E456  3E 08                MVI    A, 08H
E458  D3 0F                OUT    CNTRL           ENABLE A SIDE OF MUX
E45A  CD 30 E4             CALL   LOAD

                  * PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
E45D  3E 09                MVI    A, 09H
E45F  D3 0F                OUT    CNTRL           ENABLE B SIDE OF MUX
E461  FB                   EI                     INT MUST CALL READ
```

Figure 16. 8080A Microprocessor Program that Interfaces to the Circuit shown in Figure 17.

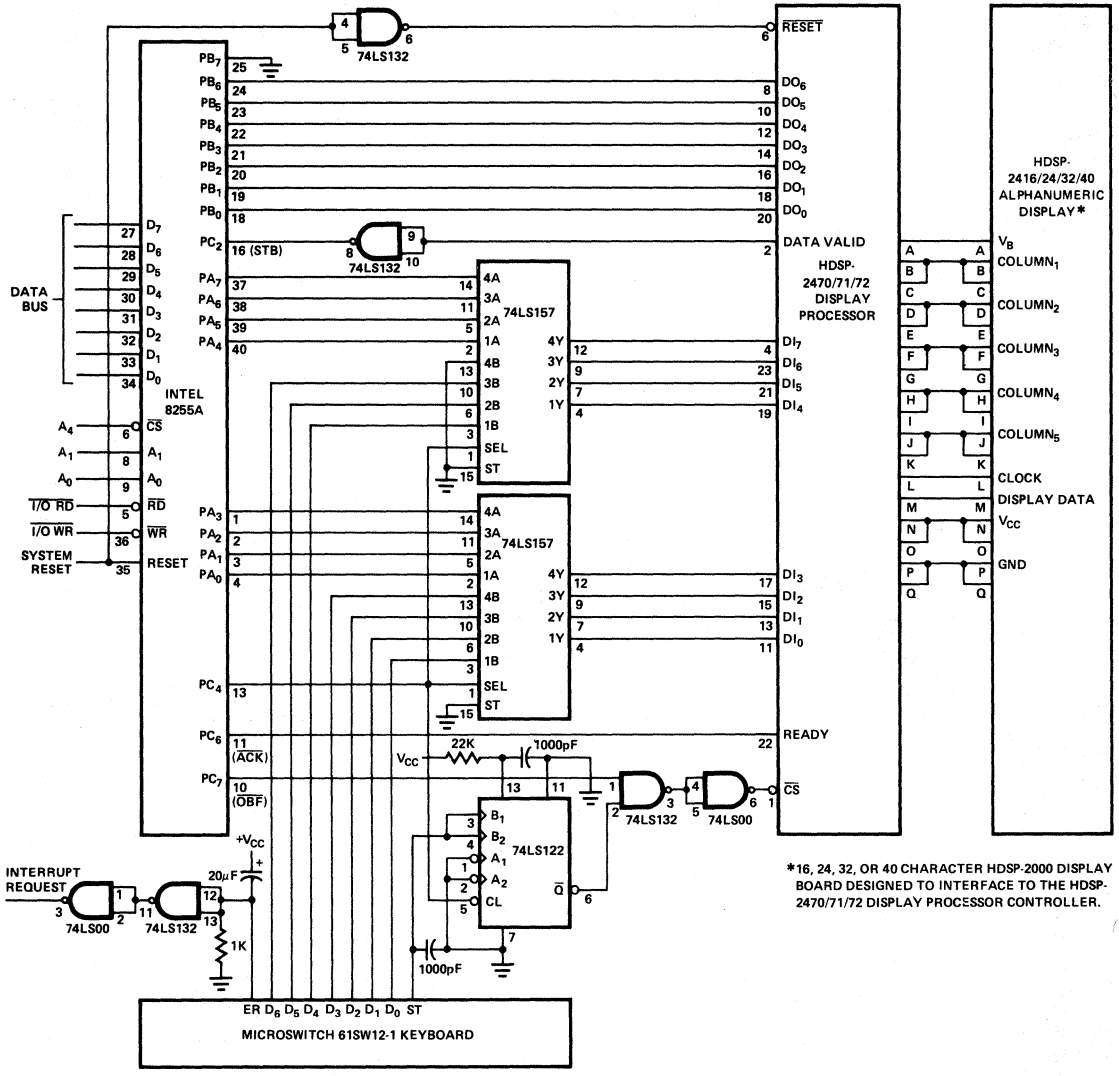


Figure 17. 8080A Microprocessor Interface Utilizing an 8255 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

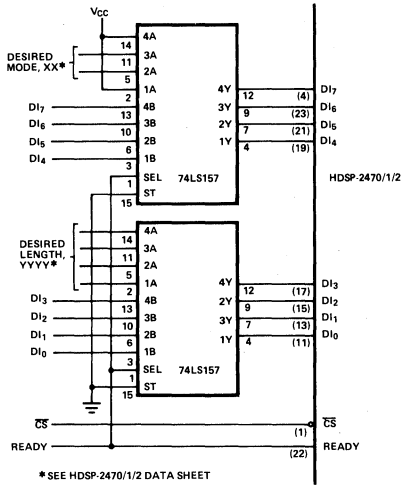


Figure 18. External Circuitry to Load a Control Word into the HDSP-2470/-2471/-2472 Alphanumeric System upon Reset

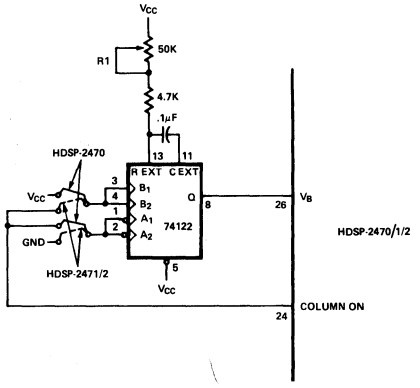


Figure 19. External Circuitry to Vary Luminous Intensity of the HDSP-2470/-2471/-2472 Alphanumeric Display System

DECODER ADDRESS FOR FIG. 7a, 7b, 10	DECODER ADDRESS FOR FIG. 6	HDSP-2471 ROM ADDRESS	HEXIDECIMAL DATA															
E500	0600	080	08	30	45	7D	7D	38	7E	30	60	1E	3E	62	40	08	38	41	$COLUMN_1$
		090	10	18	5E	78	38	78	38	3C	38	3C	38	08	20	12	48	01	
		0A0	00	00	00	14	24	23	36	00	00	00	08	08	00	08	00	20	
		0B0	3E	00	62	22	18	27	3C	01	36	06	00	00	00	14	41	06	
		0C0	3E	7E	7F	3E	7F	7F	7F	3E	7F	00	20	7F	7F	7F	7F	3E	
		0D0	7F	3E	7F	26	01	3F	07	7F	63	03	61	00	02	41	04	40	
		0E0	00	38	7F	38	38	38	08	08	7F	00	20	00	00	78	7C	38	
		0F0	7C	18	00	48	04	3C	1C	3C	44	04	44	00	00	00	08	2A	
E580	0680	100	1C	48	29	09	09	44	01	4A	50	04	49	14	3C	7C	44	63	$COLUMN_2$
		110	08	24	61	14	44	15	45	43	45	41	42	08	7E	19	7E	12	
		120	00	5F	03	7F	2A	13	49	0B	00	41	2A	08	58	08	30	10	
		130	51	42	51	41	14	45	4A	71	49	49	36	5B	08	14	22	01	
		140	41	09	49	41	41	49	09	41	08	41	40	08	40	02	04	41	
		150	09	41	09	49	01	40	18	20	14	04	51	00	04	41	02	40	
		160	07	44	48	44	44	54	7E	14	08	44	40	7F	41	04	08	44	
		170	14	24	7C	54	3E	40	20	40	28	48	64	08	00	41	04	55	
E600	0700	180	3E	45	11	11	05	44	29	4D	48	04	49	08	20	04	44	55	$COLUMN_3$
		190	78	7E	01	15	45	14	44	42	44	40	40	2A	02	15	49	7C	
		1A0	00	00	00	14	7F	08	56	07	3E	3E	1C	3E	38	08	30	08	
		1B0	49	7F	49	49	12	45	49	09	49	49	36	3B	14	14	14	51	
		1C0	5D	09	49	41	41	49	09	41	08	7F	40	14	40	0C	08	41	
		1D0	09	51	19	49	7F	40	60	18	08	78	49	7F	08	7F	7F	40	
		1E0	0B	44	44	44	44	54	09	54	04	7D	44	10	7F	18	04	44	
		1F0	24	14	08	54	44	40	40	30	10	30	54	36	77	36	08	2A	
E680	0780	200	7F	40	29	21	05	38	2E	49	50	38	49	10	20	7C	3C	49	$COLUMN_4$
		210	08	24	61	14	3C	15	3D	43	45	41	42	1C	02	12	41	12	
		220	00	00	03	7F	2A	64	20	00	41	00	2A	08	00	08	00	04	
		230	45	40	49	49	7F	45	49	05	49	29	00	00	22	14	08	09	
		240	55	09	49	41	41	49	09	51	08	41	40	22	40	02	10	41	
		250	09	21	29	49	01	40	18	20	14	04	45	41	10	00	02	40	
		260	00	3C	44	44	48	54	02	54	04	40	3D	28	40	04	04	44	
		270	24	7C	04	54	20	20	20	40	28	08	4C	41	00	08	10	55	
E700	0800	280	00	30	45	7D	79	44	10	30	60	40	3E	60	1C	02	04	41	$COLUMN_5$
		290	04	18	5E	78	40	78	40	3C	38	3C	38	08	02	00	42	01	
		2A0	00	00	00	14	12	62	50	00	00	00	08	08	00	08	00	02	
		2B0	3E	00	46	36	10	39	30	03	36	1E	00	00	41	14	00	06	
		2C0	1E	7E	36	22	3E	41	01	72	7F	00	3F	41	40	7F	7F	3E	
		2D0	06	5E	46	32	01	3F	07	7F	63	03	43	41	20	00	04	40	
		2E0	00	40	38	20	7F	08	00	3C	78	00	00	44	00	78	78	38	
		2F0	18	40	04	20	00	7C	1C	3C	44	04	44	00	00	00	08	2A	

Figure 20. 128 Character ASCII Decoder Table Used by the 6800 Refresh Program in Figure 6, 8080A Refresh Programs in Figures 7a, 7b, and 10, and the HDSP-2471 DISPLAY PROCESSOR CONTROLLER. Decoded 5x7 Display Font is shown in the HDSP-247X Data Sheet

APPLICATION NOTES

HEWLETT hp PACKARD
COMPONENTS

APPLICATION NOTE 1002

Consideration of CTR Variations in Optically Coupled Isolator Circuit Designs

INTRODUCTION – Optocouplers Aging Problem

A persistent, and sometimes crucial, concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The CTR is defined as the ratio of the output current, I_o, of the optocoupler divided by the input current, I_F, to the light emitting diode expressed as a percentage value at a specified input current. The resulting optocoupler's gain change, ΔCTR^+, with time is referred to as CTR degradation. This change, or degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed.

A number of different sources for this degradation will be explained in the next section, but numerous studies have demonstrated that the predominant factor for degradation is reduction of the total photon flux being emitted from the LED, which, in turn, reduces the device's CTR. This degradation occurs to some extent in all optocouplers.

$$^+\Delta CTR = CTR_{final} - CTR_{initial} \quad (1)$$

Causes

The main cause for CTR degradation is the reduction in efficiency of the light emitting diode within the optocoupler. Its quantum efficiency, η, defined as the total photons per electron of input current, decreases with time at a constant current. The LED current is comprised primarily of two components, a diffusion current component, and a space-charge recombination current:

$$I_F(V_F) = \underbrace{A\, e^{qV_F/kT}}_{\text{Diffusion}} + \underbrace{B\, e^{qV_F/2kT}}_{\text{Space-Charge Recombination}} \quad (2)$$

where A and B are independent of V_F, q is electron charge, k is Boltzmann's constant, T is temperature in degrees Kelvin, and V_F is the forward voltage across the light emitting diode.

The diffusion current component is the important radiative current and the non-radiative current is the space-charge recombination current. Over time, at fixed V_F, the total current increases through an increase in the value of B. From another point of view, with fixed total current, if the space-charge recombination current increases, due to an increase in the value of B, then the diffusion current, the radiative component, will decrease. The specific reasons for this increase in the space-charge recombination current component with time are not fully understood.

The reduction in light output through an increase in the proportion of recombination current at a specific I_F is due to both the junction current density, J, and junction temperature, T_J. In any particular optocoupler, the emitter current density will be a function of not only the required current necessary to produce the desired output, but also of the junction geometry and of the resistivity of both the P and N regions of the diode. For this reason, it is important not to operate a coupler at a current in excess of the manufacturer's maximum ratings. The junction temperature is a function of the coupler packaging, power dissipation and ambient temperature. As with current density, high T_J will promote a more rapid increase in the proportion of recombination current.

The junction and IC detector temperature of Hewlett-Packard optocouplers can be calculated from the following expressions:

$$T_J = T_A + \theta_{JA}(V_F I_F) + \theta_{D\text{-}E}(V_o I_o + V_{cc} I_{cc})$$

$$T_D = T_A + \theta_{E\text{-}D}(V_F I_F) + \theta_{DA}(V_o I_o + V_{cc} I_{cc}) \quad (3)$$

where the T_J is the junction temperature of the LED emitter, T_D is the junction temperature of the detector IC, T_A is ambient temperature, and the thermal resistances are the emitter junction to ambient, $\theta_{JA} = 370°C/W = \theta_{DA}$ detector to ambient, and the detector to emitter thermal resistance is $\theta_{D\text{-}E} = 170°C/W = \theta_{E\text{-}D}$. V_F, I_F are the forward LED voltage and current; V_o, I_o are the output stage voltage, and current and V_{cc}, I_{cc} are the power supply voltage and current to the device. In general, it is desirable to maintain $T_J \leqslant 125°C$.

A useful model can be constructed to describe the basic optocoupler's parameters which are capable of influencing the current transfer ratio. The 6N135 optocoupler, Figure 1 is the simplest device and one which is easily accessible for needed parameter measurements. However, any optocoupler can be modeled in this fashion within its linear region. Figure 1 shows the system block diagram which yields the relationship of input current, I_F, to output current, I_o. The resulting expression for CTR is:

$$CTR = \frac{I_o}{I_F}(100\%) = K\,R\,\eta(I_F,t)\,\beta(I_P,t) \qquad (4)$$

where K represents the total transmission factor of the optical path, generally considered a constant as is R, the responsivity of the photodetector, defined in terms of electrons of photocurrent per photon. η is the quantum efficiency of the emitter defined as the photons emitted per electron of input current and depends upon the level of input current, I_F, and upon time. Finally, β is the gain of the output amplifier and is dependent upon I_P, the photocurrent, and time. Temperature variations would, of course, cause changes in η, β as well.

From Equation (4), a normalized change in CTR, at constant I_F, can be expressed as:

(5)

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right)_{I_F} + \left(\frac{\Delta\eta}{\eta}\right)_{I_F}\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right)_t + \left(\frac{\Delta\beta}{\beta}\right)_{I_P}$$

The first term, $\Delta\eta/\eta$, represents the major contribution to ΔCTR due to the relative emitter efficiency change; generally, over time, $\Delta\eta$ is negative. This change is strongly related to the input current level, I_F, as discussed earlier and more elaboration will be given later. The second term, $(\Delta\eta/\eta)_{I_F}$ $(\partial \ln\beta/\partial \ln I_P)_t$, represents a second order effect of a shift, positive or negative, in the operating point of the output amplifier as the emitter efficiency changes. The third term, $(\Delta\beta/\beta)_{I_P}$, is a generally negligible effect which represents a positive or negative change in the output transistor gain over time. The parameters K and R are considered constants in this model.

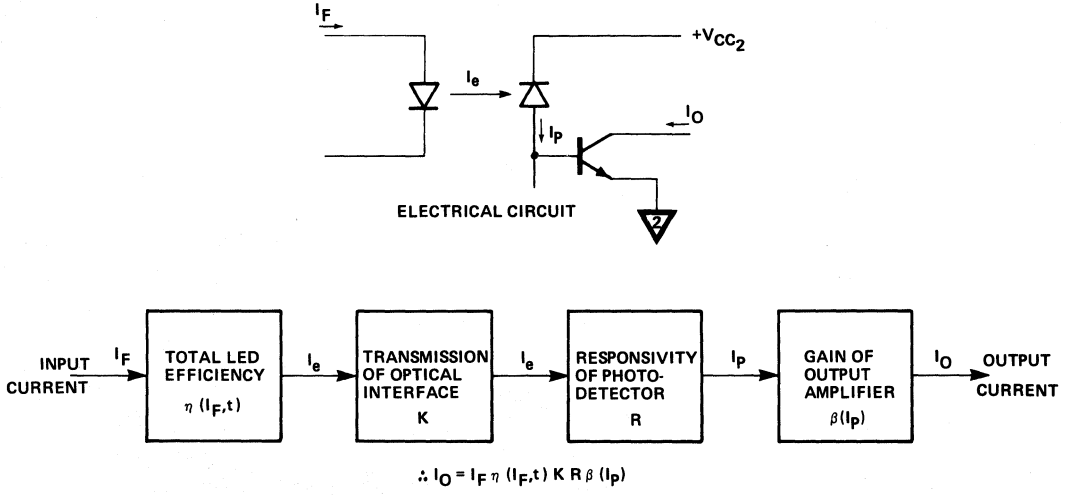


Figure 1. System Model for an Optocoupler

Degradation Model

In this section, an extensive test program conducted at Hewlett-Packard to characterize the CTR degradation of optocouplers is discussed. The development which will follow is mainly of interest to those concerned with reliability and quality assurance. From the basic data, the CTR degradation equations will be developed in order to predict the percentage change in CTR with time. Complete data and analysis of CTR degradation will be found in an internal Hewlett-Packard report.

This study is based on a total of 640 optocouplers of the 6N135 type (Figure 1) with 700 nm $GaAs_{.7}P_{.3}$ LEDs from twenty different epitaxial growth lots representing a range of n-type doping and radiance. The 6N135 allows access to measurement of the emitter degradation via the relative percentage change in photodiode current, $\Delta I_P/I_P$, as well as output amplifier β change. Stress currents of I_{FS} = .6, 7.5, 25 and 40 mA were applied to different groups of optocouplers, and at each measurement time of t=0, 24, 168, 1000, 2000, 4000 and 10,000 hours, measurement currents of I_{FM} = .5, 1.6, 7.5, 25 and 40 mA were used to determine the CTR.

The important results to be noted are the following. First, a factor of major significance in the study of CTR degradation is the ΔCTR varies as a function of the ratio of $I_{FS}/I_{FM} \equiv R$. Large values of R will result in greater CTR degradation than at lower R values with the same magnitude of I_{FS}. However, knowledge of the ratio of I_{FS}/I_{FM} alone does not give a complete picture of degradation because ΔCTR is also dependent upon the absolute magnitude of the stress current, $|I_{FS}|$. The following data will allow the derivation of the necessary equations with which to predict ΔCTR as a function of I_{FS}, I_{FM} and time.

Figure 2 displays the mean and mean plus 2σ values of emitter degradation versus R for 1K, 4K, and 10K hours at 25°C. Accelerated degradation can be seen at larger R values.

The data of Figure 2 can be replotted to illustrate the percentage degradation versus time as a function of R. Figure 3 illustrates the mean and mean plus 2σ distribution with R = 1 and 50.

From this curve, a useful expression which relates the average degradation in emitter efficiency to time is obtained for the mean or mean plus 2σ distributions. [The symbol "D" will refer to CTR degradation due solely to emitter degradation, $\Delta\eta/\eta$, whereas ΔCTR/CTR will refer to total CTR degradation as expressed in Equation (5)].

$$D_{\bar{x}} \text{ or } D_{\bar{x}+2\sigma} \equiv \frac{-\Delta I_P}{I_P} = A_0 R^{\alpha} t^{n(R)} \quad \text{for } I_{FS} = \bar{I}_{FS} \text{ in \%} \tag{6}$$

where t is in 10^3 hours and A_0 and α differ for mean or mean plus 2σ. Equation (6) represents an average degradation corresponding to a specific R, t, and an average stress current I_{FS}. A knowledge of I_{FS} and the actual device operating stress I_{FS} can be utilized to correct D to reflect the absolute magnitude of I_{FS}. This will be shown in the development of Equations (11) and (13). The data shows that I_{FS} increases with R and can be represented as follows:

$$\bar{I}_{FS}(R) = 14.13 + 9.06 \log_{10} R \quad , T_A = 25°C \tag{7}$$

$$\bar{I}_{FS}(R) = 10.5 + 5.76 \log_{10} R \quad , T_A = 85°C \tag{8}$$

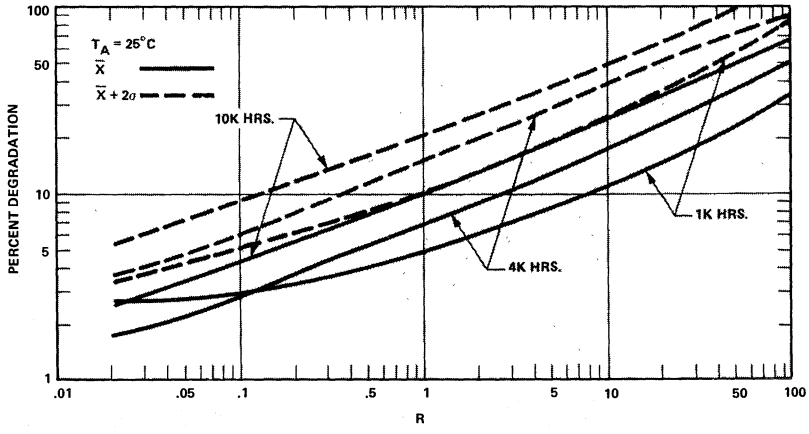


Figure 2. Emitter Degradation vs. R (Ratio of Stress Current to Measurement Current) for 1k, 4k, and 10k Hours, Mean, Mean +2σ Distribution, T_A = 25°C.

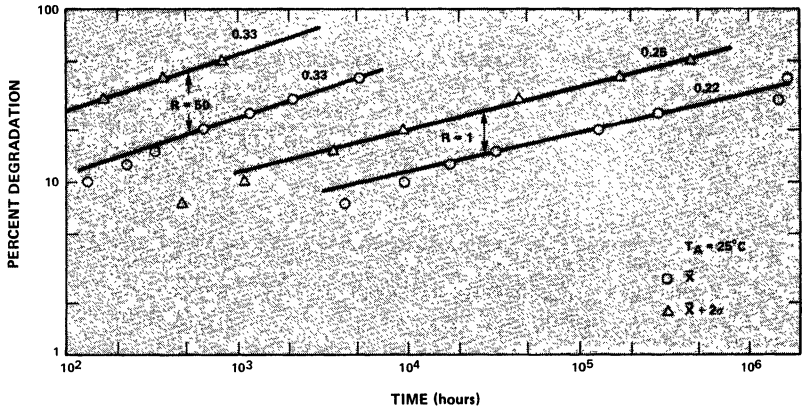


Figure 3. Degradation vs. Time at R = 1 and R = 50 for Mean, Mean + 2σ Distributions, T_A = 25°C.

These equations are obtained from averaged degradation data versus I_{FS} at different measurement times.

The expression for n(R) was found to obey the relationship

$$n(R) = .0475 \log_{10} R + .25 \qquad (9)$$

A_o and α were determined from degradation data versus R and are found in Figure 7, "Matrix of Coefficients."

Equation (6) gives a direct relationship between the average degradation, $\bar{D}$, and time. As mentioned earlier, the magnitude of the stress current also determines the amount of degradation. In order to allow for the effect of $|I_{FS}|$, empirical observations were made on D at different I_{FS} and at different times for several values of R. The dependence of degradation on stress current is linear up to I_{FS} = 40 mA, for all values of R. From these observations, the average rate of change, or slope, S(R,t), of degradation D with I_{FS} over time was found to behave in the following fashion for any R:

$$S \equiv \frac{\partial D}{\partial I_{FS}} = \alpha(R) \log_{10} t + \beta(R) \quad \%/mA \qquad (10)$$

where t is in 10^3 hours, the coefficients $\alpha(R)$ and $\beta(R)$ can be found on Figure 7.

Along with Equation (10), the mean distribution degradation, $D_{\bar{X}}$, can be estimated for any specific stress current, I_{FS}, ratio R, and time t via the subsequent expression:

$$D_{\bar{X}} = \bar{D}_{\bar{X}} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (11)$$

or substituting Equation (6),

$$D_{\bar{X}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (12)$$

where, again, D_X is the average degradation at time t, in units of 10^3 hours, corresponding to a stress current, $\bar{I}_{FS}$, given by Equations (7) and (8); I_{FS} is the actual stress current and $R = I_{FS}/I_{FM}$; S is the expression (10) for the change of slope of D versus I_{FS} with time; n(R) is a power of t, given by Equation (9), and A_o, α are found in Figure 7.

Equation (12) gives the mean distribution degradation by using a degradation value, $\bar{D}$ (first term), corresponding to the ratio of I_{FS}/I_{FM}, or a stress current, $\bar{I}_{FS}$, and then applying a correction quantity (second term) to $\bar{D}$ due to the magnitude of the actual stress current, I_{FS}, yielding the actual degradation D.

The expression for the mean + 2σ distribution degradation, $D_{\bar{X}+2\sigma}$, (worst case) is almost of the same form as Equation (12). The dissimilarity arises from the fact that the standard deviation, σ, is dependent upon the stress current, I_{FS}, the ratio R, and upon time. This complex dependency was analytically deduced from the data to be the following expression:

$$D_{\bar{X}+2\sigma} = \bar{D}_{\bar{X}+2\sigma} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (13)$$

or substituting Equation (6)

$$D_{\bar{X}+2\sigma} = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \qquad (14)$$

where $D_{\bar{X}+2\sigma}$ is the degradation for $\bar{X} + 2\sigma$ distribution corresponding to the stress current $\bar{I}_{FS}$, Equations (7)

and (8). A_o and α are found in Figure 7 under the $\bar{x}+2\sigma$ category. S [Equation (10)] represents the slope to correct for actual I_{FS} versus $\bar{I}_{FS}$ current levels, and P [Equation (15)] is the new term which is a slope to correct for the α variation with I_{FS}, R and t. The coefficients $\gamma(R)$, $\delta(R)$ in P are found in Figure 7.

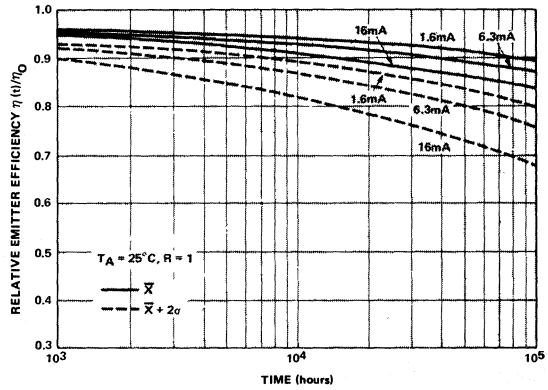
$$P = \gamma(R) \log_{10} t + \delta(R) \quad \%/mA \qquad (15)$$

where t is in 10^3 hours.

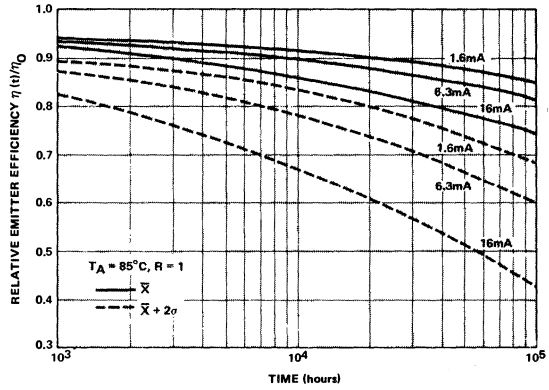
The degradation Equations (11) and (13) are considered accurate for the ranges of $I_{FS} \leq 40$ mA and $R \leq 20$; outside this range, the model does not predict degradation as well. Hence, check to see if I_{FS} and R satisfy the above conditions. If I_{FS} or R exceed these limits, predition of D will be, in general, greater than the actual degradation due to large values for S and P which do not reflect actual S and P. If $\bar{I}_{FS}$ is approximately equal to the actual I_{FS}, then the second term in the degradation equations need not be determined. Otherwise, the second term needs to be determined to obtain true emitter degradation, D. If $\bar{I}_{FS} < I_{FS}$, then the degradation, D, will be less than the degradation, $\bar{D}$, corresponding to $\bar{I}_{FS}$, and vice versa when $\bar{I}_{FS} > \bar{I}_{FS}$. A quick and coarse estimate for degradation $\bar{D}$ can be obtained by using $\bar{D} = A_o R^{\alpha} t^{n(R)}$ for a specific R with approximate values for $\alpha \approx 0.4$ and $n \approx 0.3$. Figure 4 represents plots of Equations (11) and (13) for R = 1 and I_{FS} = 1.6, 6.3, and 16mA at both T_A = 25°C and T_A = 85°C. These plots are very useful in making a quick approximation of D for the specific conditions for which the plots have been made. These conditions represent the recommended operating conditions for the three HP optocoupler families.

This discussion of reliability data and its interpretation with model equations is qualified to specific optocouplers, 6N135 and 6N138, where continuous LED operation was maintained, and extrapolation of data for times beyond 10,000 hours is assumed to be valid. Different types of LEDs or preparation processes may produce different results than those presented in this section. These expressions only incorporate the first order effect, emitter degradation $\Delta\eta/\eta$, whereas comments about higher order effects upon total CTR degradation will be given in the following section. With these expressions for degradation, accelerated testing may be accomplished by employing large values of R. Such testing can provide a means by which to determine acceptable emitter lots for optocoupler fabrication, acceptable degradation performed for lot selection, or predict functional lifetime expectance for optocouplers under specific operational conditions.

An important point to note is that the total operational life of an optocoupler is greater than the worst case mean plus 2σ distribution implies. Specifically, the worst case degradation given in Figures 4a (25°C) and 4b (85°C) are for the continuous operation of the 6N135 optocoupler. The actual lifetime for an optocoupler is greater than Figures 4a and 4b would indicate since the majority of units will be centered around the mean distribution lifetime. Secondly, the optocoupler which is operated at some signal duty factor less than 100%, for example 50%, would increase the optocoupler's life by a factor of two. Third, the fact that an optocoupler is used within equipment which may have a typical 2000 hours per year (8 hours/day – 5 days/week – 50 weeks/year) instrument or system operating time, could expect to increase the optocoupler's life by another factor of 4.4 in terms of years of useful life.



a



b

Figure 4. Calculated Curves of Relative Emitter Efficiency vs. Time for P = 1: $I_{FS} = I_{FM}$ = 1.6, 6.3, and 16mA which are Recommended I_F for 6N138, 6N137, and 6N135 Optocouplers Respectively. Mean, Mean + 2σ Distributions. a) T_A = 25°C, b) T_A = 85°C.

The appropriate operating time considerations will vary depending upon the designer's knowledge of the system in which the optocoupler will be used. The operating lifetime of an optocoupler can be expressed, for a maximum allowable degradation at a particular I_{FS}, by using Figures 4a and 4b for $t_{continuous}$ lifetime and the following expression:

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Data Factor}\right] \quad (16)$$

Another equally important point to observe is that of the worst case conditions under which the optocoupler is used. As will be illustrated in the design examples, the worst possible combination of variations in V_{cc1}, V_{cc2}, R_{in}, CTR, R_L, I_{IL}, and temperature still result in the optocoupler functioning over an extended length of time (10^5 hours) for a particular maximum allowable degradation. However, the likelihood of seven parameters all deviating in their worst directions at the same time is extremely remote. A thorough statistical error accumulation analysis would illustrate that this worst-worst case is not a representative situation from which to design.

Higher Order Effects

The first order effect of emitter degradation, $\Delta\eta/\eta$, has a pronounced influence upon the ΔCTR as explained in the previous sections; however, consideration of higher order effects is important as well.

Consider the second term in Equation (5) $(\Delta\eta/\eta)I_F$ $(\partial \ln\beta/\partial \ln I_P)t$, the emitter degradation part has been explained; however, $(\partial \ln\beta/\partial \ln I_P)_t$ represents a shift in the operating point of the output amplifier of an optocoupler. The term $(\partial \ln\beta/\partial \ln I_P)$ can be rewritten as $(1/2.3\beta)(\partial\beta/\partial \log_{10} I_P)$ which is more convenient to use with the accompanying typical curves of β versus $\log_{10} I_P$ for the two optocouplers 6N135 and 6N138, given in Figure 5a.

If the operating photocurrent, I_P, is to the right of the maximum β point of either curve, then with reduced emitter efficiency over time, I_P will decrease, but the increasing β will tend to compensate for this degradation. However, if the operating I_P is to the left of the maximum β and then I_P decreases, the β change will accentuate the emitter's degradation, yielding a larger CTR loss. The magnitude of the contributions of $\partial \ln\beta/\partial \ln I_P$ to overall CTR degradation can be illustrated by the following examples.

Consider a 6N138 optocoupler of Figure 5c operating at its recommended I_F = 1.6 mA which corresponds to an $I_P \approx 1.6\mu A$. (An I_F to I_P relationship for Hewlett-Packard optocouplers is 1 mA input current yields approximately 1μA of photodiode current.) At $I_P = 1.6\mu A$, the slope of the V_{CE} = 5V curve is equal to -15,000 and the gain is β = 26,000; hence, $\partial \ln\beta/\partial \ln I_P \approx$ -0.25. If, for instance, the emitter degradation $\Delta\eta/\eta$ is -10%, then the second order term would improve the overall CTR degradation, i.e.,

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right) + \left(\frac{\Delta\eta}{\eta}\right)\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right) + \ldots = -10\% + 2.5\% = -7.5\% \quad (17)$$

This improvement is what was expected while operating on the right side of the β maximum. In fact, with an I_F = 4 mA or $I_P \approx 4\mu A$, the term $\partial \ln\beta/\partial \ln I_P$ = -0.8, and again, if $\Delta\eta/\eta$ = -10%, the resulting ΔCTR/CTR = -2%, nearly cancelling the emitter's degradation.

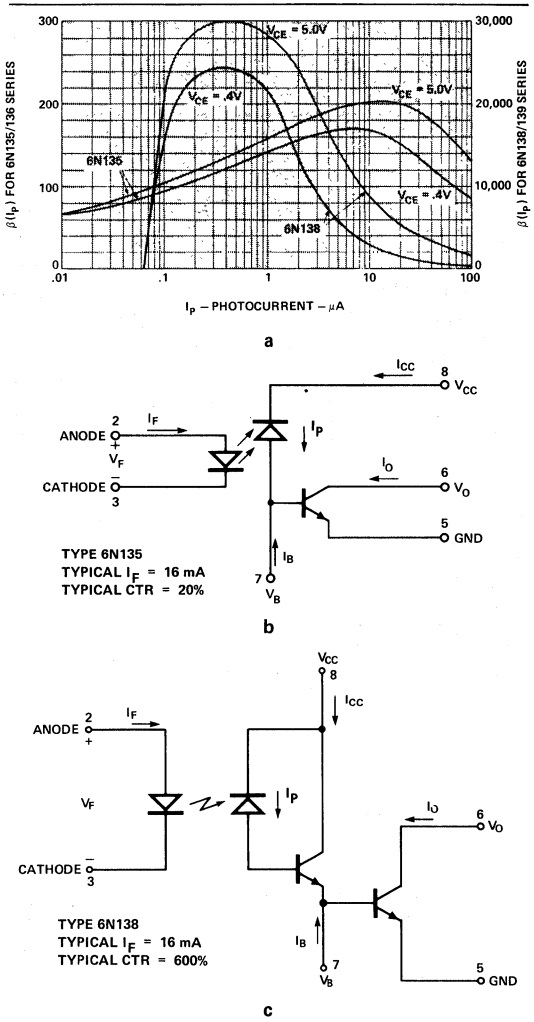


Figure 5. a) DC Current Gain, β, vs. Photocurrent, I_P, for 6N135 and 6N138 Optocouplers. Current Diagrams and Typical Values of I_F and CTR for Hewlett-Packard Optocouplers, b) 6N135, c) 6N138.

With the 6N135 optocoupler, Figure 5b operating at I_F = 10 mA, or $I_P \approx 10\mu A$, which corresponds to the maximum β point on the V_{CE} = .4V curve, the slope is zero and the total CTR degradation is basically the emitter's degradation.

Another subtle effect is seen from the third term in Equation (5), $(\Delta\beta/\beta)I_P$, over time. At constant I_P, β can increase or decrease by a few percent over 10,000 hours. This change is so small that the third term is generally neglected.

For the optocouplers containing an output amplifier, such as the 6N137, which switches abruptly about a particular threshold input current, the actual emitter degradation can be determined from Equations (11) and (13). An appropriate $I_{F_{initial}}$ can be determined to provide for adequate guard band current which will allow the optocoupler emitter to degrade while maintaining sufficient I_P to switch the amplifier. An actual design procedure to determine the needed $I_{F_{initial}}$ for proper operation of Hewlett-Packard optocouplers is given in the design examples section.

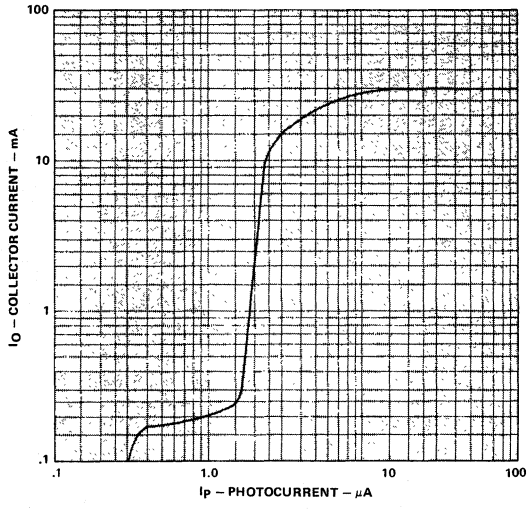


Figure 6. a) Output Current, I_O, vs. Photocurrent, I_P, for 6N137 Optocoupler.
b) Circuit Diagram and Typical Values of I_F and CTR for 6N137 Optocoupler.

MATRIX OF COEFFICIENTS

	25°C		85°C			
	$\bar{X}$	$\bar{X}+2\sigma$	$\bar{X}$		$\bar{X}+2\sigma$	
			R<6	6≤R	R<8	8≤R
A_o	4.95	9.7	6.8	5.0	15.0	11.0
α	.388	.428	.302	.467	.284	.430
	25°C		85°C			
	R≤1	R≥1	R≤1		R≥1	
$\alpha(R)$	$.19\,R^{.052}$	$.19\,R^{.32}$	$.32\,R^{.08}$		$.32\,R^{.30}$	
$\beta(R)$	.055	$.055\,R^{.68}$	$.11\,R^{.25}$		$.11\,R^{.65}$	
	25°C		85°C			
$\gamma(R)$	$.063\,R^{.30}$		$.154\,R^{.26}$			
$\delta(R)$	$.081\,R^{.38}$		$.196\,R^{.39}$			

Figure 7. Matrix of Coefficients.

Procedure for Calculation of CTR Degradation

1. Specify I_{FS}, I_{FM}

2. Determine $R = I_{FS}/I_{FM} \leq 20$, $I_{FS} \leq 40$ mA — Degradation Model Equations (11) and (13) Valid

3. First Approximation of Degradation

$$\bar{D}_{\bar{x}} \text{ or } \bar{x} + 2\sigma = A_o R^{\alpha} t^{n} \quad (\%)$$

with $\alpha \approx .4$, A_o (Figure 7), $n \approx .3$, t in 10^3 hours (D corresponds to I_{FS})

4. Calculate $\bar{I}_{FS}$ =

$$\begin{cases} 14.13 + 9.06 \log_{10} R \text{ @ } 25^{\circ}C & \text{Equation (7)} \\ 10.5 + 5.76 \log_{10} R \text{ @ } 85^{\circ}C & \text{Equation (8)} \end{cases}$$

If $I_{FS} \approx \bar{I}_{FS}$, Step 6 and the second terms in Equations (11) and (13) do not need to be calculated.

5. Calculate $n(R) = .0475 \log_{10} R + .25$

6. Calculate $S = \alpha(R) \log_{10} t + \beta(R)$; $\alpha(R), \beta(R)$

$P = \gamma(R) \log_{10} t + \delta(R)$; $\gamma(R), \delta(R)$ — Figure 7, t in 10^3 hours

7. Calculate Mean, Mean + 2σ Degradation

$$D_{\bar{x}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \quad \text{Equation (11)}$$

$$D_{\bar{x}} + 2\sigma = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \quad \% \quad \text{Equation (13)}$$

(A_o, α via Figure 7, t in 10^3 hours)

8 For Second Order Effect, Determine Slope

$$\frac{\partial \ln \beta}{\partial \ln I_P} = \frac{1}{2.3\beta} \frac{\partial \beta}{\partial \log_{10} I_P}$$

Figure 5a — typical curves with an approximation for HP optocouplers of I_F = 1 mA yields $I_P \approx 1\mu A$

9a. Total CTR Degradation for Mean Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}} + D_{\bar{x}} \frac{\partial \ln \beta}{\partial \ln I_P}$$

9b. Total CTR Degradation for Mean + 2σ Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}} + 2\sigma + D_{\bar{x}} + 2\sigma \frac{\partial \ln \beta}{\partial \ln I_P}$$

Practical Application

A very common application of an optocoupler is to function as the interfacing element between digital logic. In this section, the designer will be shown an approach which will insure the initial and long term performance of such an interface, and take into account the practical aspects of the system that surrounds it. These system elements include the data rate, the logic families being interfaced, the variations of the power supply, the tolerances of the components used, the operational temperature range, and lastly the expected lifetime of the system.

The system data speed can be considered as the primary selection criteria for selecting a specific optocoupler family. Figure 9 lists the ranges of data rates for four Hewlett-Packard optocoupler families when driven at specified LED input current, I_F. With this table, and the knowledge of the system data rate requirements, it is possible to select an optimum coupler.

An example of an optocoupler interconnecting two logic gates is shown in Figure 8. A logic low level is insured when the saturated output sinking current, I_O, is greater than the combined sourcing currents of the pull-up resistor, and the logic low input current, I_{IL}, of the interconnecting gate. Using the coupler specifications selected from Figure 9 and the corresponding CTR (MIN) from Figure 10,

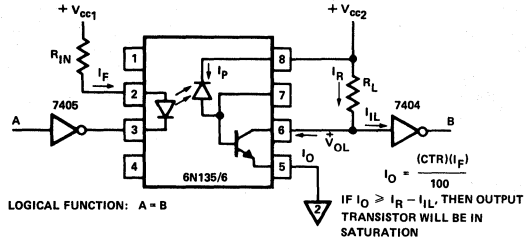


Figure 8. Typical Digital Interface Using an Optocoupler.

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}} \quad (18)$$

$$I_{F\,(MAX)} = \frac{V_{cc1\,(MAX)} - V_{F\,(MIN)} - V_{OL}}{R_{in\,(MIN)}} \quad (19)$$

$$I_F = \frac{I_o \times 100}{CTR(MIN)} \quad (20)$$

$$R_{in} = \frac{V_{cc1} - V_F - V_{OL}}{I_F} \quad (21)$$

FAMILY	NRZ DATA RATE BITS/S	INPUT CURRENT – I_F						
		.5mA	1.0mA	1.6mA	7.5mA	10mA	12mA	16mA
6N135/6 SINGLE TRANSISTOR	MIN							333k
	TYP							2M
6N138/9 SPLIT DARLINGTON	MIN	12k		22k			125k	
	TYP	100k		200k			840k	
4N45/6 DARLINGTON	MIN					1.8k		
	TYP		640			6.5k		
6N137 OPTICALLY COUPLED GATE	MIN				6.7M			
	TYP				10M			

Figure 9. Figure 13.5-2. Optocoupler Data Rates Specifications.

FAMILY		% CTR @ I_F = (mA)						TEMP °C	V_{OL}
		.5	1.0	1.6	5	10	16		
SINGLE TRANSISTOR	6N135						7	25	0.4
	6N136						19		
SPLIT DARLINGTON	6N138		300					0–70	0.4
	6N139	400	500					0–70	0.4
DARLINGTON	4N45		250			200		0–70	1.0
	4N46	350	500			200		0–70	1.0
OPTICALLY COUPLED GATE	6N137				400			0–70	0.6

Figure 10. Optocoupler CTR (MIN).

it is possible to determine from Equation (20) the minimum initial value of I_F for the coupler. The design criteria is that $I_O \geq I_{IL} + I_R$ for the V_{IL} specified in Figure 11.

Using Equation (21), the typical value of R_{in} can be calculated for the selected I_F and the logic low output voltage, V_{OL}, of the driving gate. The V_{OL} of the logic family is given in Figure 11. The next step is to determine the worst case value of the LED input current, I_F, resulting from the tolerance variations of the LED current limiting resistor, R_{in}, and the power supply voltage, V_{cc1}. The conditions of $I_{F(MIN)}$ and the initial CTR (MIN) are then used to determine the initial worst case value of $I_{O(MIN)}$. Conversely, the worst case CTR degradation will occur when the LED is stressed at $I_{F(MAX)}$ conditions; thus, $I_{F(MAX)}$ will be used to determine the worst case degradation of the optocoupler performance. Using the maximum V_{cc1} and the minimum R_{in} will accomplish this worst case calculation, as shown in Equation (19).

TTL FAMILY	I_{IL}	V_{IL}	I_{IH}	V_{IH}	I_{OL}	V_{OL}	I_{OH}	V_{OH}
74S	−2 mA	.8V	50 μA	2V	20 mA	.5V	−1000 μA	2.7V
74H	−2 mA	.8V	50 μA	2V	20 mA	.4V	− 500 μA	2.4V
74	−1.6 mA	.8V	40 μA	2V	16 mA	.4V	− 400 μA	2.4V
74LS	−.36 mA	.8V	20 μA	2V	8 mA	.5V	− 400 μA	2.7V
74L	−.18 mA	.7V	10 μA	2V	3.6 mA	.4V	− 200 μA	2.4V

Figure 11. Logic Interface Parameters.

The change in CTR from the initial value at time t = 0 to a final value at some later time can be compensated by choosing a value of R_L which is consistent with $I_{O(MIN)} - mI_{IL}$ at the end of system life. Equation (22) describes this worst case calculation.

(22)

$$R_{L\,(MIN)} \geq \left[\frac{V_{cc2\,(MAX)} - V_{OL}}{I_{F(MIN)} \cdot CTR(MIN) \cdot 1 - \left(\frac{D_{\bar{x}} + 2\sigma}{100}\right)} - mI_{IL} \right]$$

$D_{x} + 2\sigma$ = worst case CTR degradation

The selection of the maximum value of R_L is also of important in that its value insures that the collector is pulled up to the logic one voltage conditions, V_{IH}, under the conditions of maximum I_{OH} of the coupler, and the I_{IH} of the interconnecting gate.

(23)

$$R_{L\,(MAX)} \leq \frac{V_{cc2\,(MIN)} - V_{IH}}{I_{OH\,(MAX)} + m\,I_{IH}}$$

The selection of the value of R_L between the boundaries of $R_{L\,(MIN)}$, and $R_{L\,(MAX)}$ has certain trade offs. As in any open collector logic system, T_{PLH} increases with increasing R_L. Conversely, as R_L is increased above R_{LMIN}, a larger guardband between I_{OMIN} and $I_{IL} + I_R$ is achieved. Engineering judgement should be employed here to achieve the optimum trade off for desired performance.

Using the coefficient Figure 7 and Equations (11) and (13), the following examples are developed to demonstrate the methods of optocoupler system design in the presence of the mean and mean plus two sigma CTR degradation.

Example 1.

System Specifications

Data Rate	20 k bit NRZ
Logic Family	Standard TTL
Power Supply 1 & 2	5V ± 5
Component Tolerances	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	350 k hr (40 yr) at 50% system use time and 50% Data Duty Factor

Interface Specifications

Coupler 6N139

$CTR\ (MIN) = 500\% @ I_F = 1.6\ mA$
$V_{OL}\ (MAX) = .4V @ I_F = 1.6\ mA$
$I_{OH}\ (MAX) = 250\mu A @ V_{cc2} = 7V$
$V_F\ (MAX) = 1.7V @ I_F = 1.6\ mA$
$V_F\ (MIN) = 1.4V @ I_F = 1.6\ mA$
$V_F\ (TYP) = 1.6V @ I_F = 1.6\ mA$

Logic Standard TTL

$I_{IL} = 1.6\ mA$ $I_{IH} = 40\mu A$
$V_{IL} = .8V$ $V_{IH} = 2V$
$I_{OL} = 16\ mA$ $I_{OH} = 400\mu A$
$V_{OL} = .4V$ $V_{OH} = 2.4V$

Step 1. $R_{in\ (TYP)}$

$$R_{in} = \frac{V_{cc1} - V_{F\ (TYP)} - V_{OL}}{I_{F\ (TYP)}} \quad (24)$$

$$R_{in} = \frac{5.0 - 1.6 - .4}{1.6 \times 10^{-3}} = 1.87k\Omega, \text{ select } 1.8k\Omega \pm 5\%$$
$R_{(MIN)} = 1710\Omega$
$R_{(MAX)} = 1890\Omega$

Step 2. $I_{F\ (MAX)}$

$$I_{F\ (MIN)} = \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{R_{in\ (MAX)}} \quad (25)$$

$$I_{F\ (MIN)} = \frac{4.75 - 1.7 - .4}{1890\Omega} = 1.4\ mA$$

Step 3. $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}} \quad (26)$$

$$I_{F\ (MAX)} = \frac{5.25 - 1.4 - .4}{1710\Omega} = 2.02\ mA$$

Step 4. Determine continuous operation time for LED emitter.

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Duty Factor}\right]$$
$$= (40\ yr \times 8.76\ k\ hr/yr)(50\%)(50\%)$$
$$t_{\text{continuous lifetime}} = 87.60K\ hr$$

Step 5. Obtain the mean and mean + 2σ CTR degradation at $I_{F\ (MAX)}$ and $t_{\text{continuous lifetime}}$ either as an approximation from Figure 4 or by calculations as shown below.

Step 5a. Determine $D_{\bar{x}}$

$$D_{\bar{x}} = A_o t^{.25} + S\,[I_{FS} - \bar{I}_{FS}] \quad (27)$$

$$D_{\bar{x}} = 4.95 t_{(k\ hr)}^{.25} + [.186 \log t_{(k\ hr)} + .055]$$

$$[I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\bar{x}} = 4.95\ (87.6)^{.25} + (.186 \log 87.6 + .055)$$

$$(2.02\ mA - 14.13\ mA)$$

$D_{\bar{x}} = 10.10\%$ for 40 yr system operation

Step 5b. Determine $\bar{D}_x + 2\sigma$

$$D_{\bar{x}} + 2\sigma = A_o t^{.25} + [S + 2P]\,[I_{FS} + \bar{I}_{FS}] \quad (28)$$

$$D_{\bar{x}} + 2\sigma = 9.7 t_{(k\ hr)}^{.25} + [2\ (.063 \log t_{(k\ hr)} + .081)$$

$$+ (.186 \log t_{(k\ hr)} + .055)]$$

$$\times [I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 9.7\ (87.6)^{.25} + [2\ (.063 \log 87.6 + .081)$$

$$+ (.186 \log 87.6 + .055)]$$

$$\times [2.02\ mA - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 19.71\%$$

Step 6. Guardband the worst case value of CTR degradation.

It is often desirable to add some additional operating margin over and above conditions dictated by simple worst case analysis. The use of engineering judgement to increase the worst possible CTR degradation by an additional 5% margin would insure that the entire distribution would fall within the analysis. Thus,

$$D_{\bar{x}+2\sigma} + 5\% = 24.71\%$$

Step 7. Selecting $R_{L\ (MIN)}$ for guardbanded worst case

$$D_{\bar{x}+2\sigma} + 5\% \quad , \ m = 1$$

(22)

$$R_{L(MIN)} \geq \frac{V_{cc2\ (MAX)} - V_{OL}}{\frac{I_{F(MIN)} \cdot CTR_{(MIN)} \cdot 1 - \left(\frac{D_{\bar{x}+2\sigma} + 5\%}{100}\right)}{100} - m|I_{IL}|}$$

$$R_{L(MIN)} \geq \frac{5.25 - .4}{\frac{1.4 \times 10^{-3} \cdot 500\% \cdot 1 - \left(\frac{24.71\%}{100}\right)}{100} - 1\ 1.6\ mA}$$

$$R_{L\ (MIN)} = 1.32k\Omega$$

Step 8. Select $R_{L\ (MAX)}$

$$R_{L\ (MAX)} \leq \frac{V_{cc2\ (MAX)} - V_{OL}}{I_{OH\ (MAX)} + m|I_{IH}|} \qquad (29)$$

$$R_{L\ (MAX)} \leq \frac{4.75 - 2.4}{250\mu A + 40\mu A} = 8.1k$$

The range of R_L is from 1.32kΩ to 8.1kΩ. It is desirable to select a pull-up resistor which optimizes both speed performance and additional I_O guardband. This criteria leads to a tradeoff between a value close to $R_{L\ (MIN)}$ for speed performance and one bordering near $R_{L(MAX)}$ for I_O guardbanding. In this design example, the system's lifetime has a higher priority than does the moderate speed performance demanded from the optocoupler. An R_L of 3.3kΩ ± 5% is selected under this condition.

An additional guardband of 5% was added to the worst case $D_{\bar{x}+2\sigma}$ CTR degradation guardband to insure that even a greater percentage of the distribution would be accounted for. The actual percentage difference between $I_{OL\ (MAX)}$ and $I_{O\ (MIN)}$ at the end of system life is shown below:

(30)

$$I_{O\ (MIN)} = \frac{CTR_{(MIN)} \cdot I_{F\ (MIN)} \cdot 1 - \left(\frac{D_{\bar{x}+2\sigma}}{100}\right)}{100}$$

(31)

$$I_{OL\ (MAX)} = \frac{V_{cc2\ (MAX)} - V_{OL}}{R_{L\ (TYP - 5\%)}} + m|I_{IL}|$$

$$\%\ Guardband = \left[1 - \frac{I_{OL\ (MAX)}}{I_{O\ (MIN)}}\right] X\ 100 \qquad (32)$$

For the example shown, the additional end of system life I_O guardband results from the selection of an R_L greater than the $R_{L\ (MIN)}$ as shown in Steps 9, 10, and 11.

Step 9. $I_{O\ (MIN)}$ at end of system life

$$I_{O\ (MIN)} = \frac{500\% \cdot 1.4\ mA \cdot \left(1 - \frac{19.17\%}{100}\right)}{100} = 5.65\ mA$$

Step 10. $I_{OL\ (MAX)}$ for worst case of $I_{R\ (MAX)} + I_{IL}$

(33)

$$I_{OL\ (MAX)} = \frac{5.25 - .4}{3.13k\Omega} + 1.6\ mA = 3.14\ mA$$

Step 11. % Guardband

$$\% = 1 - \frac{3.14\ mA}{5.65\ mA}\ 100 = 44.4\% \qquad (34)$$

Thus, this circuit interface design offers an additional 44.4% I_O guardband beyond the 19.71% required to compensate for the CTR change caused by 86.7k hr of continuous operation at an $I_{F\ (MAX)}$ of 2 mA. This extra guardband results from having chosen an $R_L = 3.3k$ rather than the lowest allowable value of R_L plus the engineering guardband chosen in Step 6.

Example 2.

System Specifications

Data Rate	250K bit NRZ
Logic Family	TTL to LSTTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	25°C
Expected System Lifetime	175 k hr (20 yr) at 50% System Use Time and 50% Data Duty Factor

Interface Conditions

Coupler 6N136

$CTR_{(MIN)} = 19\%\ @\ I_F = 16\ mA$
$V_{OL} = .4V$
$I_{OH} = 500\ nA\ @\ V_{cc2} = 5.0V$
$V_{F(TYP)} = 1.6V\ @\ I_F = 16\ mA$
$V_{F(MIN)} = 1.5V\ @\ I_F = 16\ mA$
$V_{F(MAX)} = 1.7V\ @\ I_F = 16\ mA$

Logic LSTTL

$I_{IL} = .36\ mA$ $\quad I_{OL} = 8\ mA$
$V_{IL} = .8V$ $\quad V_{OL} = .5V$
$I_{IH} = 40\mu A$ $\quad I_{OH} = 400\mu A$
$V_{IH} = 2V$ $\quad V_{OH} = 2.7V$

Again using Figure 7, the data rate dictates the use of a 6N136 at an $I_{F\ (TYP)}$ of 16 mA. Using the same 12 step worst case analysis, it is possible to determine the values of R_{in}, R_L and the degree of guardbanding of I_O at end of system lifetime.

Step 1. $R_{in} = 187\Omega$, select $180\Omega \pm 5\%$
$R_{L\ (MIN)} = 179\Omega$
$R_{L\ (MAX)} = 189\Omega$

Step 2. $I_{F\ (MIN)} = 14.02\ mA$

Step 3. $I_{F\ (MAX)} = 19\ mA$

Step 4. **System Lifetime**

$t = 43.8k\ hr$

Step 5. $D_{\bar{x}}$ and $D_{\bar{x}} + 2\sigma$ for $I_{F\ (MAX)}$ of 19 mA by calculation or from Figure 4

$D_{\bar{x}} = 14.5\%$
$D_{\bar{x}} + 2\sigma = 28.5\%$
} 43.8k hr continuous lifetime

Step 6. Engineering Guardband of 5%,

$D_{\bar{x} + 2\sigma} + 5\% = 33.5\%$

Step 7. R_L selection with guardbanding of $D_{x + 2\sigma} + 5\%$

$R_{L\ (MIN)} = 3.44k\Omega$

Step 8. $R_{L\ (MAX)} = 50k\Omega$

Step 9. $R_{L\ (TYP)} = 5.1k\Omega \pm 5\%$, $R_{L\ (TYP - 5\%)}$
$= 4.84k\Omega$, $R_{L\ (MAX + 5\%)}$
$= 5.35k\Omega$

Step 10. End of System Life $I_{O\ (MIN)}$

$I_{O\ (MIN)} = 1.5\ mA$

Step 11. $I_{OL\ (MAX)} = 1.36\ mA$

Step 12. Engineering % Guardband of $I_{O\ (MIN)} = 9.3\%$

Example 3.

If a particular design requirements specifies a maximum tolerable degradation over a system lifetime, the optimum value of $I_{F(TYP)}$ can be obtained from Figure 12. For example, if a maximum acceptable degradation, $D_{\bar{x}} + 2\sigma$, is 40%, and a continuous operation of 400k hr is desired, this curve specifies that $I_{F\ (TYP)}$ should be less than or equal to 10 mA. A 400k hr continuous operation with 100% system duty factor as might be encountered in telephone switching equipment is equivalent to 45 years of system lifetime.

If a 6N139 split Darlington were used to interface an LSTTL logic gate with the system specifications stated, a collector pull-up resistor of as low as 160Ω could be used. If an R_L of 1k were selected, this optocoupler would offer an additional end of life guardband of 81.8%. This worst case analysis points out that with the knowledge of selecting proper values of R_L, the CTR performance of the

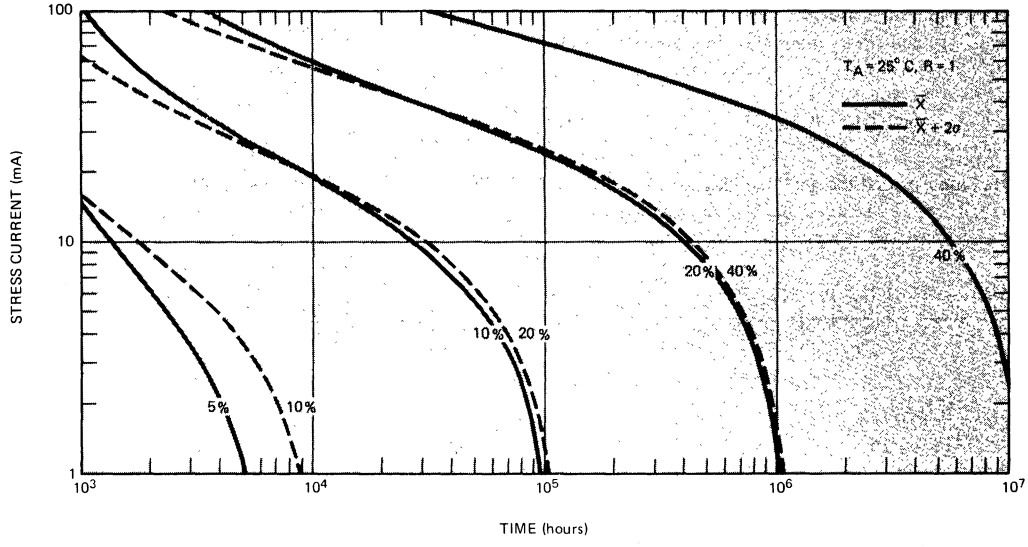


Figure 12. Stress Current (I_{FS}) vs. Time vs. % Degradation.

coupler far exceeds the normal MTBF requirements for most commercial electronic systems.

Consideration of the Optically Coupled Gate

System data speed requirements in the multi-megabit range can also be communicated through an optocoupler. The first three coupler families listed in Figure 9 are not applicable in these very high speed data interface applications; however, the optically coupled gate, 6N137, will function to speeds of up to 10 MHz. This type of coupler differs in operation from the single transistor and Darlington style units in that it exhibits a non-linear transfer relationship of I_F to I_O. This is shown in Figure 13. The relationship is described as a minimum threshold of LED input current, I_{Fth} which is required to cause the output transistor to sink the current supplied by the pull-up resistor and interconnected gate. As the LED degrades, the effect is that a larger value of $I_{F\,th}$ is required to create the same detector photodiode current necessary to switch the output gate.

In the previous interface examples, the worst case analysis and guardbanding is based on the output collector current, I_O. With the optically coupled gate, worst case guardbanding is concerned with the selection of the initial value of the I_F, which at end of system lifetime will generate the necessary threshold photocurrent demanded by the gate's amplifier to change state.

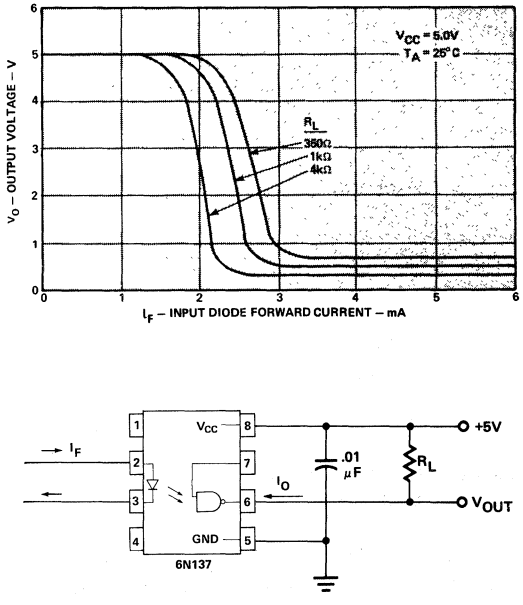


Figure 13. 6N137 Input – Output Characteristics.

The calculation of the required I_F to allow for worst case LED degradation is approached by guardbanding the guaranteed minimum isolator input current, I_{FH}, for a specified I_{OL} and V_{OL} interface. Equation (35) shows the relationship of the I_P to I_F for this coupler.

$$I_P \propto (I_F)^n \quad \text{, where } 1.1 \leqslant n \leqslant 1.3 \tag{35}$$

Using the concept that the guardbanding of the initial value of I_F will result in a similarly guardbanded I_P, the relationship presented in Equation (36) results:

$$\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right] = \left[\frac{I_{PH}}{I_P}\right] = \left[\frac{I_{FH}}{I_F}\right]^n \tag{36}$$

$$I_F = \frac{I_{FH}}{\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right]^n} \tag{37}$$

The previous interface example showed that the first term of the $D_X + 2\sigma$ equation dominated the magnitude of the worst case degradation. This term, $A_0 R^{\alpha_t n(R)}$, i.e., $(9.7\ t_{(k\ hr)}^{.25})$, does not contain an I_F current dependent term; thus, an approximation of the worst case LED degradation can be made that relates to the system's lifetime. This initial value of $D_X + 2\sigma$ can be used in Equation (37) to calculate the initial value of the I_F. With this initial I_F, a more accurate degradation value can be calculated using Equation (28). This procedure results in an iterative process to zero in on a value of I_F that will insure reliable operation.

The following example will illustrate this approach.

Example 4.

System Specifications

Data Rate	6 MHz NRZ
Logic Family	LSTTL to TTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	203k hr (23 yr) at 50% System Use Time and 50% Data Duty Factor

Step 1. Determine the continuous operation time for LED emitter

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Factor}\right]$$

$$= \left[23\text{ yr } 8.76\text{k hr/yr}\right]\left[50\%\right]\left[50\%\right]$$

$$= 50.3\text{k hr}$$

Step 2. Calculate the worst case LED degradation

$$D_x + 2\sigma \approx 9.7\ t_{(k\ hr)}^{.25}$$

$$D_x + 2\sigma \approx 9.7\ (50.3)^{.25}$$

$$D_x + 2\sigma \approx 26\%$$

Step 3. Calculate the first approximation of guardbanded I_F, n = 1.2

$$I_F = \frac{I_{FH}}{\left[1 - \frac{(\approx D_{\bar{x}} + 2\sigma)}{100}\right]^{1/n}} = \frac{5\text{ mA}}{.78} = 6.41\text{ mA}$$

Step 4. Calculate input resistor R_{in}

$$R_{in} \leqslant \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{I_F}$$

$$R_{in} \leqslant \frac{4.75 - 1.7 - .4}{.00641}$$

$$R_{in} \leqslant 413\Omega \text{ select } R_{in} = 390\Omega \pm 5\%$$

Rin (MAX)

$$R_{in\ (MAX)} = 409\Omega$$

$$R_{in\ (MIN)} = 370\Omega$$

Step 5. Calculate the $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}}$$

$$I_F = \frac{5.25 - 1.4 - .4}{370}$$

$$I_F = 9.32\text{ mA}$$

Step 6. Calculate the worst case $D_{\bar{x}} + 2\sigma$ for $I_{F\ (MAX)}$

$$D_{\bar{x}} + 2\sigma = 25.8\% + .747\ (9.32\text{ mA} - 14.13\text{ mA})$$

$$D_{\bar{x}} + 2\sigma = 22.2\%$$

Step 7. Calculate the new minimum required I_F at end of life based on degradation found in Step 6.

$$I_{F(EOL)} = \frac{I_{FH}}{\left[1 - \frac{22.2}{100}\right]^{1/1.2}} = \frac{5}{.81} = 6.16\,mA$$

Step 8. Calculate $I_{F\,(MIN)}$

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}}$$

$$I_{F\,(MIN)} = \frac{4.75 - 1.7 - .4}{409}$$

$$I_{F\,(MIN)} = 6.47\,mA$$

Step 9. $R_{L\,(MIN)}$, m = 1

$$R_{L\,(MIN)} = \frac{V_{cc2\,(MAX)} - V_{OL}}{I_{OL\,(MIN)} - mI_{IL}}$$

$$= \frac{5.25 - .6}{.016 - .0016}$$

$$R_{L\,(MIN)} = 332\Omega$$

Step 10. $R_{L\,(MAX)}$, m = 1

$$R_{L\,(MAX)} = \frac{V_{cc2\,(MAX)} - V_{OH}}{I_{OH\,(MAX)} + mI_{IH}}$$

$$R_{L\,(MAX)} = \frac{4.75 - 2.4}{250\mu A + 40\mu A}$$

$$R_{L\,(MAX)} = 8.1k\Omega$$

Step 11. Minimum % Emitter Degradation Guardband

$$\%_{(MIN)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MIN)}}\ 100\right] \qquad (38)$$

$$4.8\% = \left[1 - \frac{6.16\,mA}{6.47\,mA}\ 100\right]$$

where $I_{F\,(EOL)}$ represents the switching threshold at the end of life.

Step 12. Maximum % Emitter Degradation Guardband

$$\%_{(MAX)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MAX)}}\right] 100 \qquad (39)$$

$$34\% = \left[1 - \frac{6.16\,mA}{9.32\,mA}\ 100\right]$$

The conclusions that are to be drawn from this analysis are that as long as the $I_{F\,(MAX)}$ is less than $I_{\overline{FS}} = 14.13$ mA, the worst-worst case CTR degradation may be calculated using only the first term, $A_o R^{\alpha_t n(R)}$, of the $D_{\overline{x}+2\sigma}$ case. In the example presented, 26% degradation was determined from the first term, and when the more accurate calculation using Equation (28) was used, a 22% degradation resulted. The end of life I_F guardband may be calculated using Equations (38) and (39). Using Equation (38), the minimum guardband is 5.7%, and with Equation (39), the maximum guardband is 35%.

HEWLETT PACKARD

APPLICATION NOTE 1003

Interfacing 18 Segment Displays to Microprocessors

INTRODUCTION

Over the past four years, the need for alphanumeric displays has grown very rapidly due to the extensive use of microprocessors in new system designs. The HDSP-6508 and HDSP-6300 alphanumeric displays were developed to provide a low cost, easy-to-use alternative to 5x7 dot matrix displays. These displays use an 18 segment display font that includes a centered decimal point and colon for increased readability. This font is capable of displaying the 64 character ASCII subset (numbers, punctuation symbols, and upper case alphabet) as well as many special purpose symbols. The HDSP-6504 and HDSP-6508 are 3.81 mm (0.150") red 4 or 8 character displays in a dual-in-line package. The HDSP-6300 is a 3.56 mm (0.140") red 8 character display in a dual-in-line package. The HDSP-6508 has character-to-character spacing on 6.35 mm (0.250") centers while the HDSP-6300 has character-to-character spacing on 5.08 mm (0.200") centers. Paralleling the development of these alphanumeric displays have been the introduction of several new display interface circuits that simplify the use of the 18 segment display. These circuits include an ASCII to 18 segment decoder/driver and improved NPN Darlington digit drivers that are designed to interface directly to 5 volt digital logic. This Application Note deals with several techniques to interface the 18 segment display to microprocessor systems. Depending upon the overall system configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, the system designer would choose the best interface technique to drive an 18 segment display.

DISPLAY INTERFACE TECHNIQUES

This application note will deal with four different techniques, as shown in Figure 1a-d, for interfacing the HDSP-6508 and HDSP-6300 displays to microprocessor systems.

1a. The REFRESH CONTROLLER interfaces the microprocessor system to a multiplexed LED display. The controller periodically interrupts the microprocessor and after each interrupt, the microprocessor supplies new display data for the next refresh cycle of the display.

1b. The DECODED DATA CONTROLLER refreshes a multiplexed LED display independently from the microprocessor system. A local RAM stores decoded display data. This data is continuously read from the RAM and then used to refresh the display. Whenever the display message is changed, the microprocessor decodes each character in software and writes the decoded data into the local RAM.

1c. The CODED DATA CONTROLLER also refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores ASCII data which is continuously read from the RAM, decoded, and used to refresh the display. The display message is changed by writing new ASCII characters within the local RAM.

1d. The DISPLAY PROCESSOR CONTROLLER uses a separate microprocessor to drive the LED display. This microprocessor provides ASCII storage, ASCII decode, and display refresh independently from the main microprocessor system. Software within the dedicated microprocessor provides many powerful features not available in the other controllers. The main microprocessor updates the LED display by sending new ASCII characters to the slave microprocessor.

COMPARISON OF INTERFACE TECHNIQUES

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. Each interface requires one or more memory or I/O addresses. These addresses are generated by decoding the microprocessor address bus. The display decoder can be located within the microprocessor program or as circuitry within the display interface. Location of the display decoder within the microprocessor program gives the designer total control of the display font within the program. This feature can be particularly important if the display will be used to display different languages and special graphics symbols. The interface technique chosen may limit or interfere with some programming techniques used in the rest of the microprocessor program. For example, the use of an

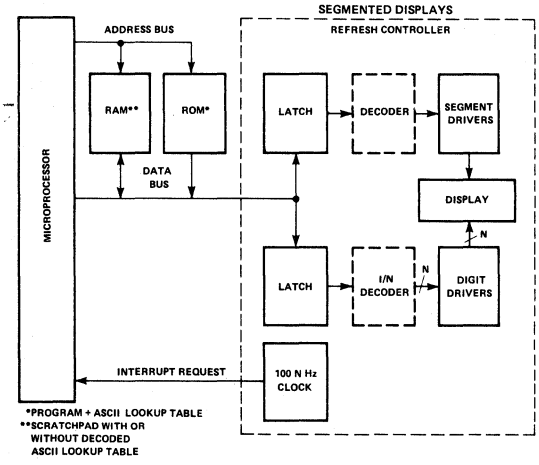


Figure 1a. REFRESH CONTROLLER Display Interface

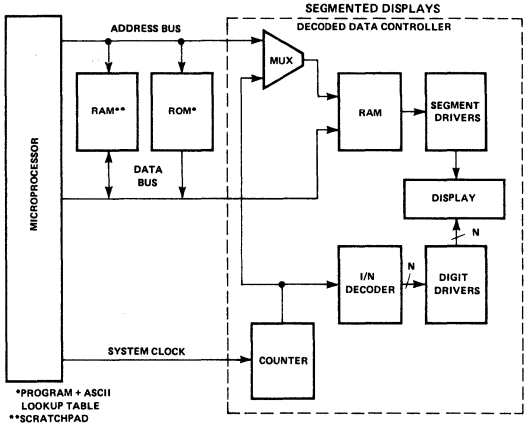


Figure 1b. DECODED DATA CONTROLLER Display Interface

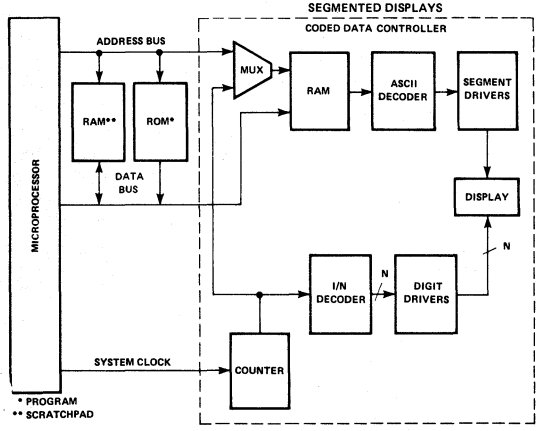


Figure 1c. CODED DATA CONTROLLER Display Interface

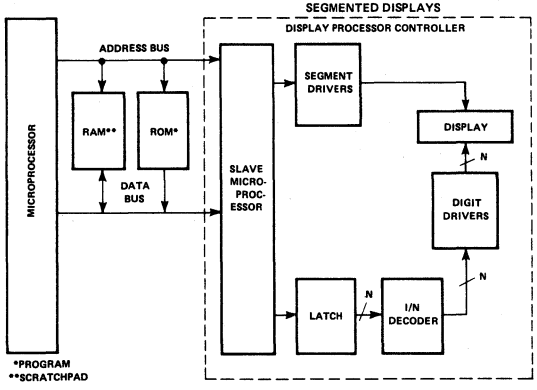


Figure 1d. DISPLAY PROCESSOR CONTROLLER Display Interface

interrupt may restrict the use of some programming techniques used in the interruptable portions of the microprocessor program.

The REFRESH CONTROLLER requires continuous interaction from the microprocessor system. Since the microprocessor actively strobes the LED display, the display interface circuitry is reduced. Generally, this technique provides the lowest hardware cost for any given display length. The display decoder can be located either within the microprocessor program or as circuitry within the interface. Display strobing is accomplished through use of the microprocessor interrupt circuitry. Demands upon microprocessor time are directly proportional to display length.

The DECODED DATA CONTROLLER and CODED DATA CONTROLLER require microprocessor interaction only when the display message is changed. Both techniques employ a local RAM memory that is continuously scanned by the display interface electronics. For the DECODED DATA CONTROLLER, the display decoder is located within the microprocessor software and the local RAM stores decoded display data. The CODED DATA CONTROLLER includes the display decoder within the display interface circuitry and the local RAM stores ASCII data. Since ASCII data is more compact than decoded display data, the CODED DATA CONTROLLER uses a smaller RAM than the DECODED DATA CONTROLLER. Both techniques allow the microprocessor to individually

change each display character by a memory or I/O write to a specific display address. These interface techniques can accept new data at a very high rate.

The DISPLAY PROCESSOR CONTROLLER, like the previously defined CODED and DECODED DATA CONTROLLERS, requires microprocessor interaction only when the display message is changed. By using a dedicated microprocessor, the DISPLAY PROCESSOR CONTROLLER provides many additional display features. These features include multiple entry modes, a blinking cursor, editing commands, and a data output function. The software with the DISPLAY PROCESSOR CONTROLLER further reduces microprocessor interaction by providing more sophisticated data entry modes compared to the RAM entry mode provided by the DECODED DATA and CODED DATA CONTROLLERS. The display decoder can either be designed into the dedicated display microprocessor or can be located within a separate PROM. The use of a PROM allows the user to provide a special character font with additional circuitry. The DISPLAY PROCESSOR CONTROLLER does not allow as high a data entry rate as either the DECODED DATA or CODED DATA CONTROLLERS.

MICROPROCESSOR OPERATION

In order to effectively utilize the interface techniques outlined in the following sections, an understanding of microprocessor fundamentals is required. A brief description of microprocessor fundamentals is included in the following section. A microprocessor system usually consists of a microprocessor, ROM memory, RAM memory, and a specific I/O interface as outline in Figure 2. The microprocessor performs the desired system function by executing a program stored within the ROM. The RAM memory provides temporary storage for the microprocessor system. The I/O interface consists of circuitry that is used as an input to the system or as an output from the system. The microprocessor interfaces to this system through an address bus, data bus, and control bus. The address bus consists of several outputs (A_0, A_1,...A_n) from the microprocessor which collectively specify a binary number. This number or "address" uniquely specifies each word in the ROM memory, RAM memory, and I/O interface. The data bus serves as an input to the microprocessor during a memory or input read and as an output from the microprocessor during a memory or output write. The control bus provides the required timing and signals to the microprocessor system to distinguish a memory read from a memory write, and in some systems an I/O read from an I/O write. These control lines and the timing between the address bus, data bus, and control bus vary for different microprocessors.

The address, data, and control buses provide the flow of instructions and data into the microprocesor. Program execution consists of a series of memory reads (instruction fetches) which are sometimes followed by a memory read or write (instruction execution). The microprocessor performs a memory read by outputting the memory address of the word to be read on the address bus. This address uniquely specifies a word within the memory system. The microprocessor also outputs a signal on the control bus, which instructs the memory system to perform a memory read. The address selects one memory element, either RAM or ROM, within the memory system. Then, the desired word within the selected memory element is gated on the data bus by the read signal. Meanwhile, the unselected memory elements tristate their output lines so that only the selected memory element is active on the data bus. After sufficient delay, the microprocessor reads the word that appears on the data bus. Similarly, for a memory write, the microprocessor outputs the memory address of the word to be written on the address bus. After sufficient delay, the microprocessor outputs a signal on the control bus, which instructs the memory system to perform a memory write.

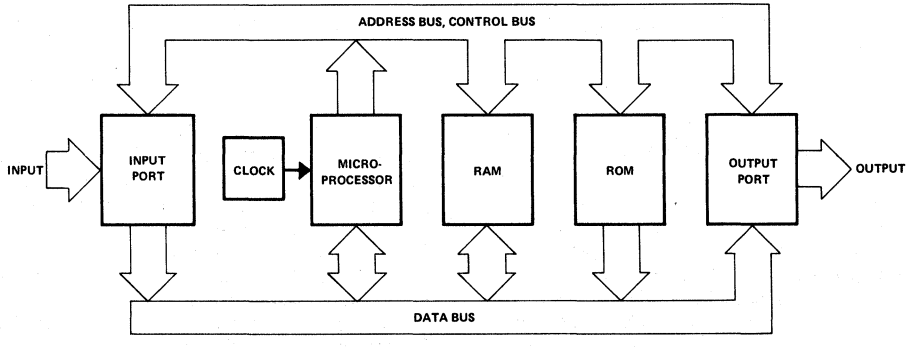


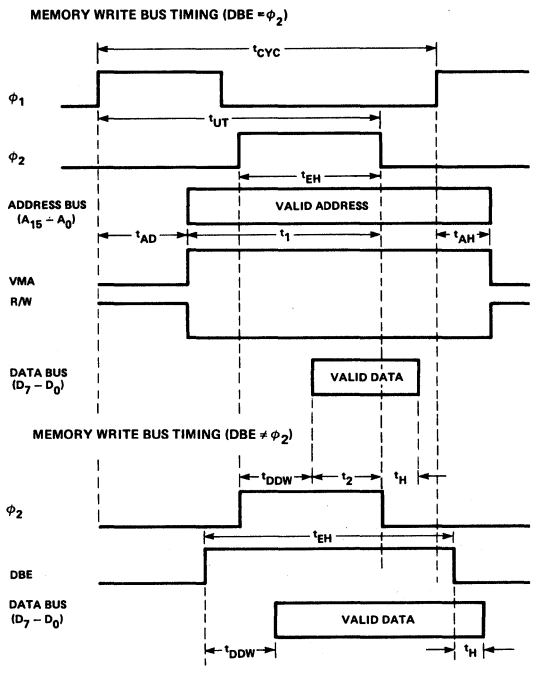
Figure 2. Block Diagram of a Typical Microprocessor System

The microprocessor also outputs the desired memory word on the data bus. The address selects one RAM memory element within the memory system. The write signal causes the memory element to read the word on the data bus and store it at the desired location. After the write cycle has been completed, the new word will have replaced the previous word within the RAM memory. During the memory write, outputs from the unselected memory elements remain tristated so that only the microprocessor is active on the data bus. These control lines and the timing for the address bus, data bus, and control bus vary for different microprocessors.

Some microprocessors, such as the Motorola 6800 microprocessor family, handle memory and I/O in exactly the same way. Memory and I/O occupy a common address space and are accessed by the same instructions. With this type of microprocessor, the hardware decoding of the address bus determines whether the read or write is to a memory or I/O element. Other microprocessors, such as the Intel 8080A, Intel 8085A, and the Zilog Z-80 have separate address spaces for memory and I/O. These microprocessors use different instructions for a memory access or an I/O access and provide signals on the control bus to distinguish between memory and I/O. One advantage of this approach is that the I/O address space can be made smaller to simplify device decoding. However, the I/O instructions that are available are usually not as powerful as the memory reference instructions. Of course, the user can always locate specific I/O devices within the memory address space through proper decoding of the address and control buses. This would allow these I/O devices to be accessed with memory reference instructions.

The 6800 microprocessor family has a 16 line address bus, 8 line data bus, and a control bus that includes the signals VMA (Valid Memory Address), R/$\overline{W}$ (Read/Write), $\overline{DBE}$ (Data Bus Enable), and clock signals ϕ_1 and ϕ_2. R/$\overline{W}$ specifies either a memory read or write while VMA is used in conjunction with R/$\overline{W}$ to specify a valid memory address. DBE gates the internal data bus of the 6800 to the external data bus. In many applications, DBE is connected to ϕ_2. Additional data hold time, t_H, can be achieved by delaying ϕ_2 to the microprocessor or by extending DBE beyond the falling edge of ϕ_2. The timing between the address bus, data bus, VMA, and R/$\overline{W}$ for a memory write is shown in Figure 3.

For the 8080A microprocessor, the address bus consists of 16 lines, the data bus consists of 8 lines, and the control bus consists of several lines including DBIN (Data Bus In), $\overline{WR}$ (Write), SYNC (Synchronizing Signal), READY, and clock signals ϕ_1 and ϕ_2. DBIN and $\overline{WR}$ are used to specify a read or write operation. The 8080A microprocessor distinguishes memory from I/O through the use of a status word that precedes every machine cycle. When SYNC is high, the status word should be loaded into an octal latch on the positive edge of ϕ_1. The outputs from the latch can then be decoded to specify whether the machine cycle is a memory write, memory read, I/O write, or I/O read. The Intel 8228 or 8238 System Controller provides this status latch and additionally encodes the outputs of the status latch with DBIN and $\overline{WR}$ to generate four timing signals $\overline{MEM\ R}$ (Memory Read), $\overline{MEM\ W}$ (Memory Write), $\overline{I/O\ R}$ (I/O Read), and $\overline{I/O\ W}$ (I/O Write). However, the 8228 and 8238 do not provide the outputs of the status latch. The timing between the address bus, data bus, $\overline{WR}$, and SYNC



6800 MICROPROCESSOR	MINIMUM TIMES (nS)				
	t_{DDW} (MAX)	t_1	t_{AH}	t_2	t_H
6800, t_{CYC} = 1000	225	630	30	225	10
68A00, t_{CYC} = 666	200	420	30	80	10
68B00, t_{CYC} = 500	160	290	30	60	10

$t_1(MIN) = t_{UT}(MIN) - t_{AD}(MAX)$

$t_2(MIN) = t_{EH}(MIN) - t_{DDW}(MAX)$

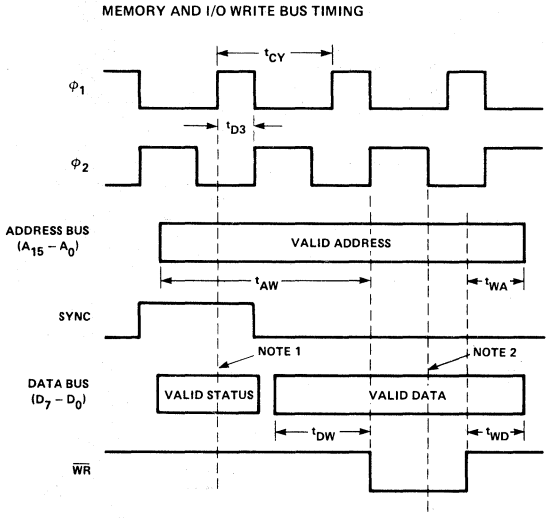
From MOTOROLA SEMICONDUCTOR MC6800 Data Sheet (DS9471), 1978

Figure 3. Memory Write Timing for the Motorola 6800 Microprocessor Family.

for both a memory write and an I/O write is shown in Figure 4. The 8080A also provides an input, READY, which allows the memory system to extend the time the address and data bus is valid by integral clock cycles.

REFRESH CONTROLLERS

Figure 5 shows a REFRESH CONTROLLER for a 16 character 18 segment alphanumeric display. The circuit operates by interrupting the microprocessor at a 1600 Hz rate. Following each interrupt, the microprocessor responds by outputting a new ASCII character to the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver and a new digit word to the 74LS174. The character font for the AC5947 is shown in Figure 6. The outputs of the 74LS174 are decoded such that digit word 00_{16} turns the leftmost display character on, digit word $0F_{16}$ turns the rightmost display character on, and digit word $1F_{16}$ turns all digits off. The interface can be expanded to 24 characters with an additional Signetics NE590 driver. This change would also require modifications in I_F peak, and the interrupt rate.



8080 MICROPROCESSOR WITH 8228 CLOCK	MINIMUM TIMES (nS)			
	t_{AW}	t_{WA}	t_{DW}	t_{WD}
8080A, t_{CY} = 480	740	90	230	90
8080A–2, t_{CY} = 380	560	80	140	80
8080A–1, t_{CY} = 320	470	70	110	70

$t_{AW} = 2t_{CY} - t_{D3} - [140(A), 130(A-2), 110(A-1)]$

$t_{WA} = t_{WD} = t_{D3} + 10$

$t_{DW} = t_{CY} - t_{D3} - [170(A), 170(A-2), 150(A-1)]$

From INTEL Component Data Catalog, 1978

NOTE 1: Status Word should be loaded into an octal latch when SYNC = 1 on positive edge of ϕ_1.

NOTE 2: Additional wait cycles can be inserted here. A wait cycle is added by forcing READY low prior to the falling edge of ϕ_2 during the clock cycle preceeding the falling edge of $\overline{WR}$.

Figure 4. Memory and I/O Write Timing for the Intel 8080A Microprocessor Family

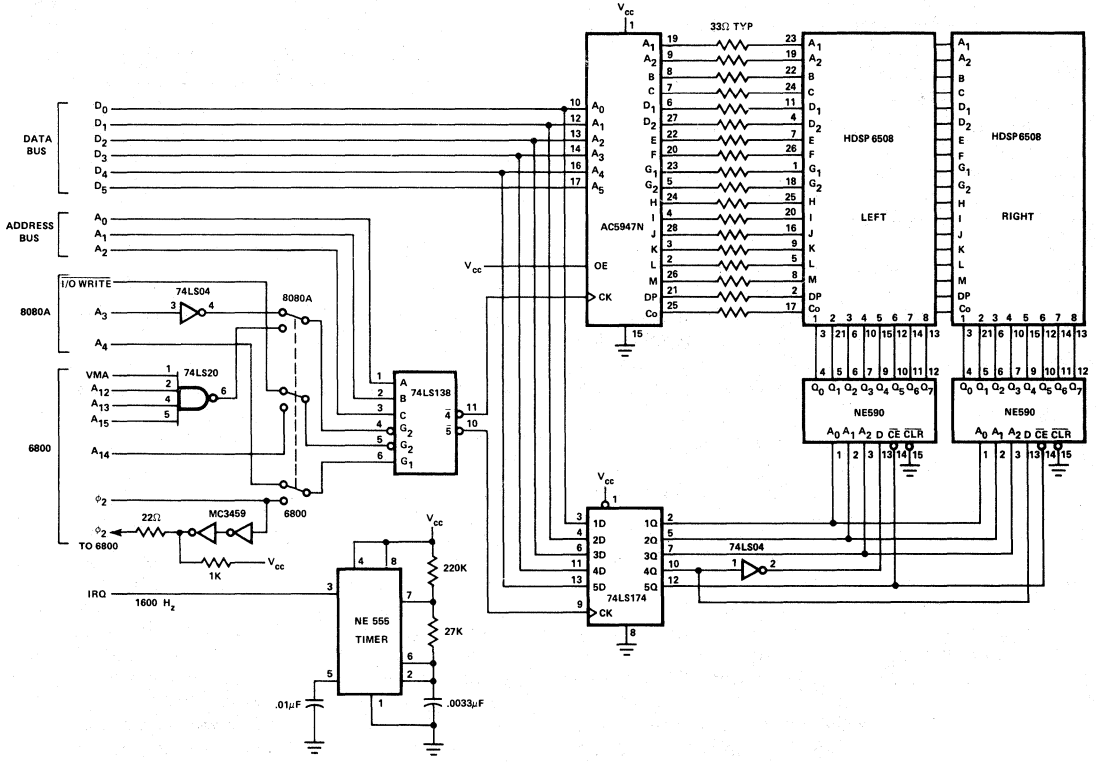


Figure 5. 6800 or 8080A Microprocessor Interface to the HDSP-6508 REFRESH CONTROLLER Utilizing the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver

BITS	D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←

Figure 6. 18 Segment Display Font for the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver

A 6800 microprocessor program that interfaces to this REFRESH controller is shown in Figure 7. Following each interrupt, the program "RFRSH" is executed. The program uses a scratch pad register "POINT" that points to the location within a 16 byte ASCII message of the next ASCII character to be stored in the display interface. The scratch pad register "DIGIT" contains the next digit word to be loaded into the display interface. The program interfaces to the circuit through two memory or I/O addresses. A memory write to address "SEG" writes a six bit word into the AC5947, and a memory write to address "DIG" writes a five bit word into the 74LS174. To prevent undesirable ghosting, the digit drivers are turned off prior to loading the next ASCII character into the AC5947. After sufficient delay, the next digit is turned on. Registers "POINT" and "DIGIT" are then updated by the program. Following execution of the "RTI" instruction, execution of the main program is resumed. A similar program written for an 8080A microprocessor is shown in Figure 8. The 6800 microprocessor program shown in Figure 7 operated with a 1 MHz clock requires 0.11% + 0.72n% of the available microprocessor time to refresh the display at a 100 Hz refresh rate, where n is the display length. The 8080A microprocessor program shown in Figure 8 when operated with a 2 MHz clock requires 0.31% + 0.96n% of the available microprocessor time to refresh the display at a 100 Hz refresh rate, where n is the display length. For example, the 16 character display shown in Figure 5

```
LOC   OBJECT CODE        SOURCE STATEMENTS
      BF04       SEG     EQU   $BF04
      BF05       DIG     EQU   $BF05

0000  0003       POINT   FDB   DATA
0002  00         DIGIT   FCB   0
0003             DATA    RMB   16

0400             RFRSH   ORG   $0400
0400  DE  00              LDX   D,POINT
0402  E6  00              LDA B X,0
0404  86  1F              LDA A I,$1F
0406  B7  BF05            STA A E,DIG
0409  F7  BF04            STA B E,SEG
040C  96  02              LDA A D,DIGIT
040E  81  0F              CMP A I,15
0410  27  0A              BEQ   LOOP1
0412  7C  0002            INC   E,DIGIT
0415  08                  INX
0416  B7  BF05            STA A E,DIG
0419  DF  00              STX   D,POINT
041B  3B                  RTI
041C  7F  0002  LOOP1     CLR   E,DIGIT
041F  F6  0001            LDA B E,POINT+1
0422  B7  BF05            STA A E,DIG
0425  C0  0F              SUB B I,15
0427  D7  01              STA B D,POINT+1
0429  24  03              BCC   LOOP2
042B  7A  0000            DEC   E,POINT
042E  3B        LOOP2     RTI
```

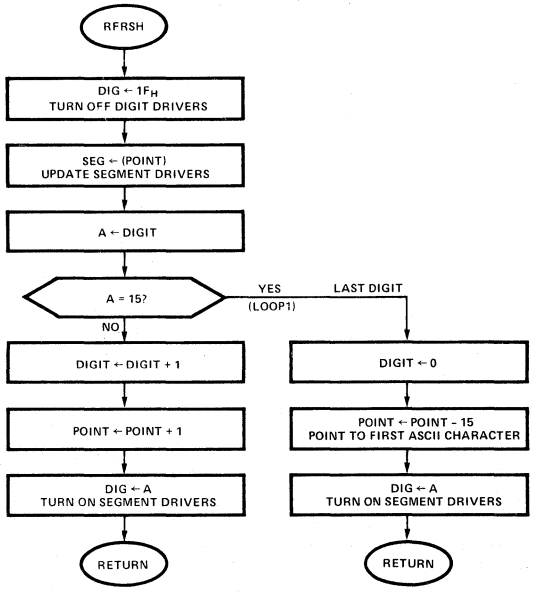


Figure 7. 6800 Microprocessor Program and Flowchart that Interfaces to the REFRESH CONTROLLER Shown in Figure 5

```
LOC   OBJECT CODE        SOURCE STATEMENTS

001C                SEG   EQU   001CH
001D                DIG   EQU   001DH

                          ORG   0E000H
E000  03  E0        POINT DW    DATA
E002  00            DIGIT DB    00H
E003  00            DATA  DS    16

                          ORG   0E400H
E400  F5            RFRSH PUSH  PSW
E401  E5                  PUSH  H
E402  2A  00E0            LHLD  POINT
E405  3E  1F              MVI   A,1FH
E407  D3  1D              OUT   DIG
E409  7E                  MOV   A,M
E40A  D3  1C              OUT   SEG
E40C  3A  02E0            LDA   DIGIT
E40F  D3  1D              OUT   DIG
E411  FE  0F              CPI   15
E413  CA  21E4            JZ    LOOP1
E416  3C                  INR   A
E417  32  02E0            STA   DIGIT
E41A  23                  INX   H
E41B  22  00E0      LOOP2 SHLD  POINT
E41E  E1                  POP   H
E41F  F1                  POP   PSW
E420  C9                  RET
E421  3E  00        LOOP1 MVI   A,0
E423  32  02E0            STA   DIGIT
E426  7D                  MOV   A,L
E427  D6  0F              SUI   15
E429  6F                  MOV   L,A
E42A  D2  1BE4            JNC   LOOP2
E42D  25                  DCR   H
E42E  C3  1BE4            JMP   LOOP2
```

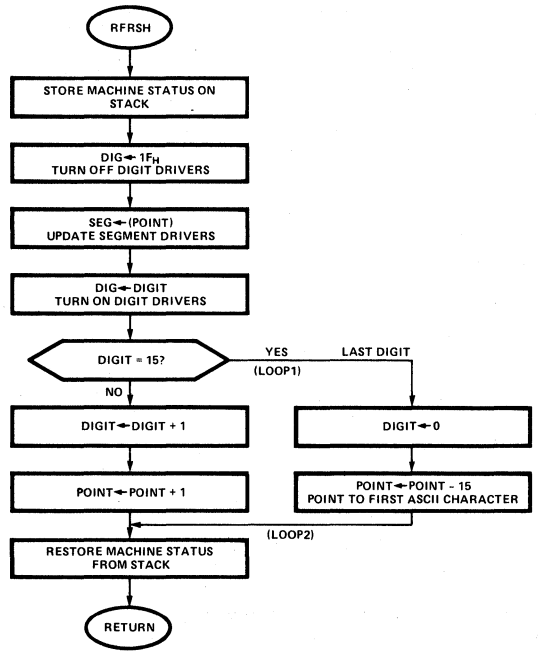


Figure 8. 8080A Microprocessor Program and Flowchart that Interfaces to the REFRESH CONTROLLER Shown in Figure 5

requires 11.6% of the 6800 microprocessor time or 15.7% of the 8080A microprocessor time to refresh the display at a 100 Hz refresh rate. Faster versions of the 6800 and 8080A microprocessors can reduce this microprocessor time by 50%.

DECODED CONTROLLERS

Figure 9 shows a DECODED DATA CONTROLLER designed for a 32 character 18 segment alphanumeric display. To simplify the circuitry, the display is configured as a 14 segment display with decimal point and colon. This allows each display character to be specified by two 8 bit words. One possible display font is shown in Figure 10. The Motorola 6810 RAM stores 64 bytes of display data that are continually read and displayed. The display data is organized within the RAM such that addresses A_5, A_4, A_3, A_2, and A_1 specify the desired character and address A_0 differentiates between the two words of display data for each character. The display data is formatted such that word 0 (D_7—D_0) is decoded as G_2, G_1, F, E, D, C, B, and A; and word 1 (D_7—D_0) is decoded as COLON, DP, M, L, K, J, I, and H. The display data is coded low true such that a low output turns the appropriate segment on. Strobing of the display is accomplished with the 74LS14 oscillator and 74LS393 counter. The counter continuously reads display data from the RAM and enables the appropriate digit driver. The time allotted to each digit is broken into four segments. During the first segment of time, the display is turned off and work 0 is read from the RAM and stored in the 74LS273 octal register. During the next three segments of time, word 1 is read from the RAM and the display is turned on. Thus, the display duty factor is (1/32) (3/4) or 1/42.6. For values of R and C specified, the display is strobed at a 130 Hz refresh rate.

Data is entered into the RAM from the address and data bus of the microprocessor via two control lines, Chip Select and Write. When Chip Select goes low, the address generated by the counter is disabled and the microprocessor address and data bus is gated to the RAM. Then, after sufficient delay, the Write input is pulsed, which stores the data within the RAM. The data entry timing for the 18 segment DECODED DATA CONTROLLER is shown in Figure 11. Because of the requirement that the address inputs of the 6810 RAM must be stable prior to the falling edge of Write, Chip Select should go low for time t_{CW} prior to the falling edge of Write. To guarantee that the address and data inputs of the RAM remain stable until after Write goes high, Chip Select should remain low for time t_{CH} following the rising edge of Write. This requirement for two separate timing signals is also required for the CODED DATA CONTROLLER shown in Figure 15. Because this interface timing is somewhat more difficult than the previously described circuits, the following methods are presented for interfacing to commonly used microprocessors.

Interface to the 6800 microprocessor family is accomplished by NANDing together VMA and some specified combination of high order address lines to generate Chip Select and using ϕ_2 to generate Write.

For the 8080A and 8085A microprocessor families, the limited flexibility of the output instruction requires that the 18 segment DECODED DATA CONTROLLER must be addressed as memory instead of I/O. The 8080A micro-

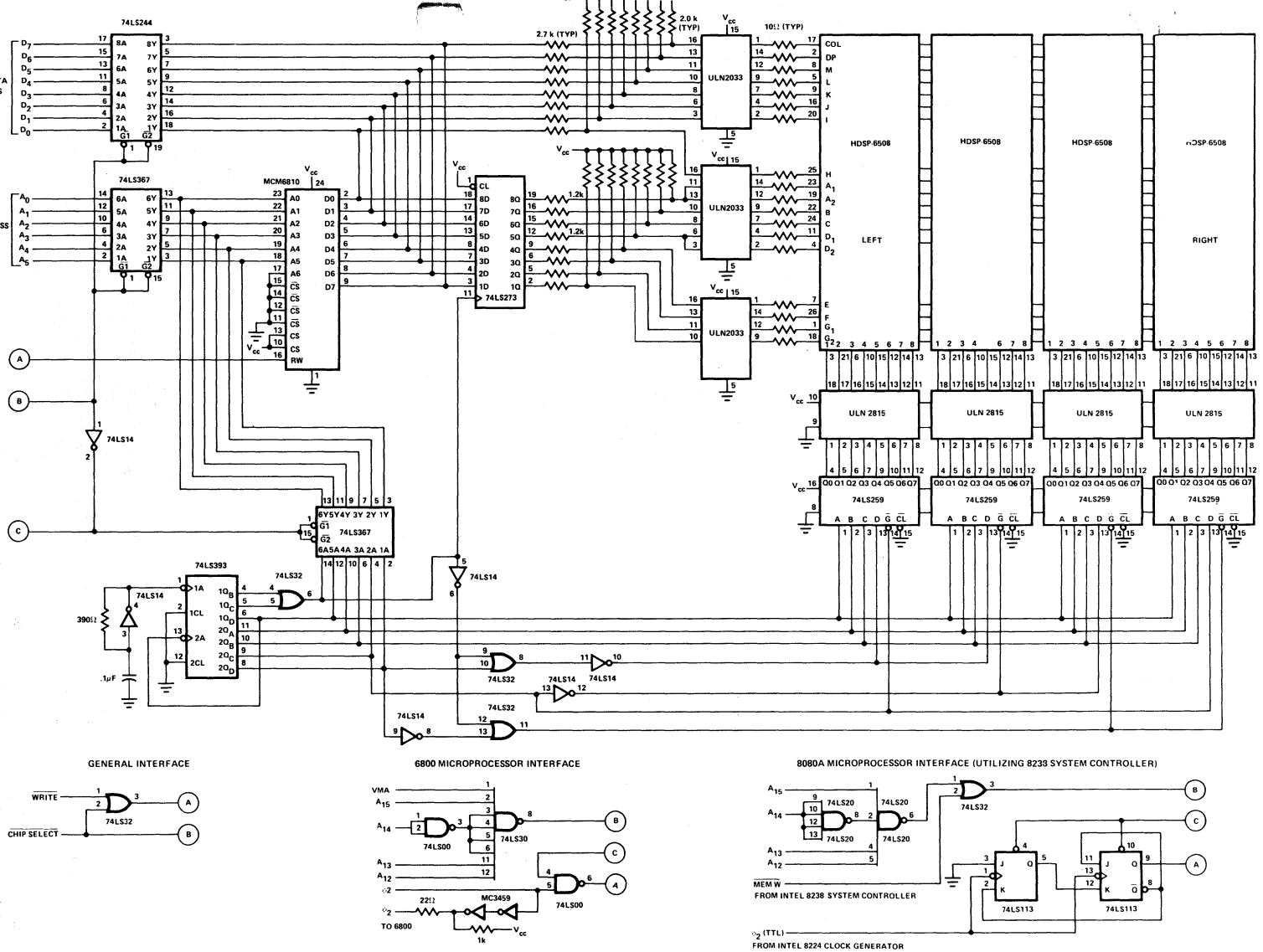


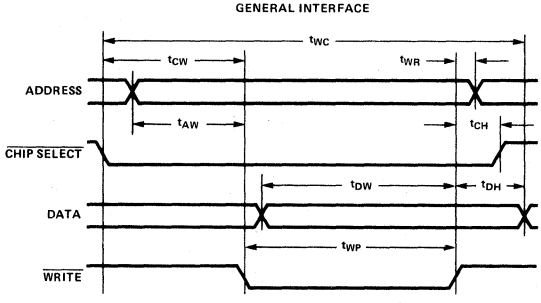
Figure 9. 6800, 8080A, and General Interface to the HDSP-6508 DECODED DATA CONTROLLER

BITS	D_3 D_2 D_1 D_0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
D_6 D_5 D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0	2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

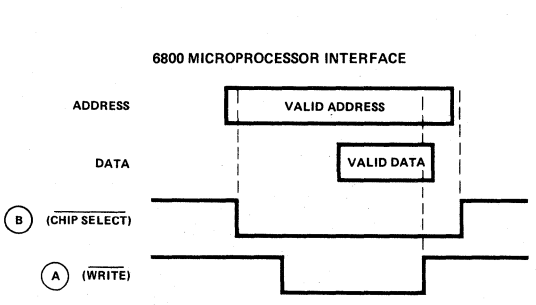
Figure 10. One Possible 16 Segment Display Font (14 Segments Plus Decimal Point and Colon) for the DECODED DATA CONTROLLER Shown in Figure 9.

processor requires an external status latch to hold status information provided during program execution. This status latch function can be implemented with an octal register such as the Intel 8212 or 74LS273. A Memory $\overline{\text{Write}}$ signal can be generated by NORing together all outputs of this status latch. This signal can then be NANDed with some specified combination of high order address lines to generate $\overline{\text{Chip Select}}$. The 8080A $\overline{\text{WR}}$ output can then be connected to $\overline{\text{Write}}$. The Intel 8238 System Controller, which is commonly used with the 8080A microprocessor, prevents direct access to the outputs of the status latch. An example of an interfacing to a system utilizing the 8238 is illustrated in Figure 9. $\overline{\text{MEM W}}$ from the 8238 is inverted and then NANDed with some specified combination of high order address lines to generate $\overline{\text{Chip Select}}$. The 74LS113 generates $\overline{\text{Write}}$ from the microprocessor clock, $\phi 2$ (TTL).

Interface to the 8085A microprocessor family can be accomplished by inverting the I/O/$\overline{\text{M}}$ output and NANDing the resulting signal with the S_0 output and some specified combination of high order address lines to generate $\overline{\text{Chip Select}}$. The $\overline{\text{WR}}$ output from the microprocessor is connected directly to $\overline{\text{Write}}$.



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	425ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	210ns
DATA HOLD	t_{DH}	35ns
WRITE PULSE	t_{WP}	325ns
WRITE RECOVERY	t_{WR}	25ns
CHIP ENABLE HOLD	t_{CH}	35ns



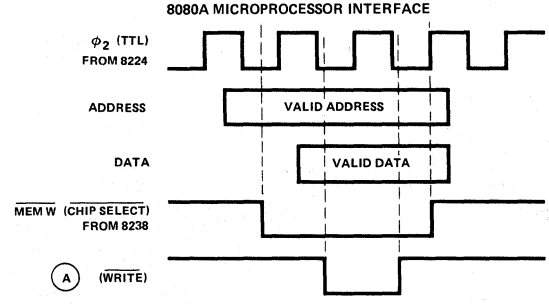


Figure 11. Data Entry Timing for the DECODED DATA CONTROLLER Shown in Figure 9

```
LOC   OBJECT CODE          SOURCE STATEMENTS

      BF00          DSPLY  EQU   $BF00
      0600          DECDR  EQU   $0600

0000  0006          ASCII  FDB   MESSGE
0002  BF00          PAD1   FDB   DSPLY
0004  0600          PAD2   FDB   DECDR
0006                MESSGE RMB   32

0400                       ORG   $0400
0400  CE  BF00       LOAD   LDX   I,DSPLY
0403  DF  02                STX   D,PAD1
0405  CE  0600              LDX   I,DECDR
0408  DF  04                STX   D,PAD2
040A  DE  00       LOOP1   LDX   D,ASCII
040C  A6  00               LDA A X,0
040E  08                   INX
040F  DF  00               STX   D,ASCII
0411  48                   ASL A
0412  97  05               STA A D,PAD2+1
0414  DE  04               LDX   D,PAD2
0416  A6  00               LDA A X,0
0418  E6  01               LDA B X,1
041A  DE  02               LDX   D,PAD1
041C  A7  00               STA A X,0
041E  08                   INX
041F  E7  00               STA B X,0
0421  08                   INX
0422  DF  02               STX   D,PAD1
0424  8C  BF40             CPX   I,DSPLY+64
0427  26  E1               BNE   LOOP1
0429  39                   RTS
```

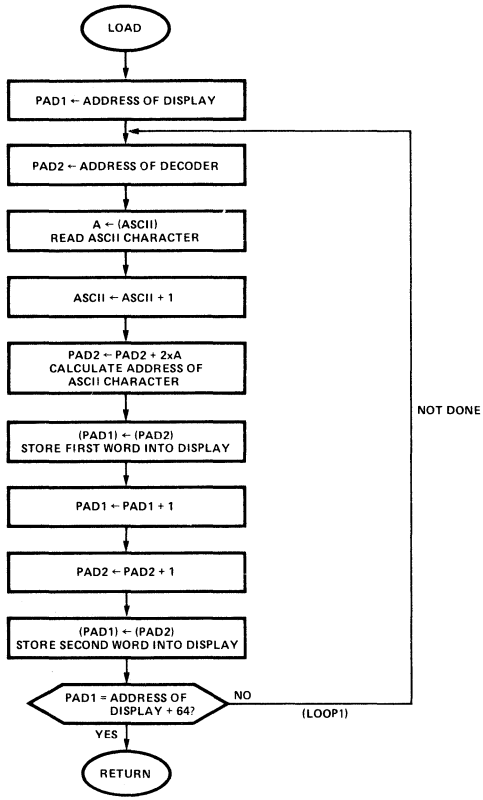


Figure 12. 6800 Microprocessor Program and Flowchart that Interfaces to the DECODED DATA CONTROLLER Shown in Figure 9

The simplest interface to the Z-80 microprocessor family is accomplished by addressing the 18 segment DECODED DATA CONTROLLER as I/O instead of memory. An example of this interface is shown in Figure 15. The $\overline{IORQ}$ output is inverted and NANDed with some specified combination of address lines to generate $\overline{Chip\ Select}$. The 74LS113 circuit generates $\overline{Write}$ from the inverted microprocessor clock $\overline{\phi}$.

A 6800 microprocessor program that interfaces to the 18 segment DECODED DATA CONTROLLER is shown in Figure 12. This program decodes 32 ASCII characters and stores the resulting decoded display data within the display. The scratch pad register "ASCII" points to the location of the next ASCII character to be decoded. The program reads the first ASCII character, increments the point, "ASCII," and then looks up two words of display data within the 64 character ASCII look-up table "DECDR." These words of display data are then stored at the two addresses for the leftmost display location. Subsequent ASCII characters are decoded, and stored at the appropriate address within the display until all 32 characters have been decoded. After the program is finished, the pointer "ASCII" will have been incremented by 32. This program requires 2.4 ms for a 1 MHz clock to decode and load 32 ASCII characters into the 18 segment DECODED DATA CONTROLLER. The corresponding 8080A microprocessor program is shown in Figure 13. This program requires 1.4 ms for a 2 MHz clock to decode and load 32 ASCII characters into the 18 segment DECODED DATA CONTROLLER.

The 64 character ASCII font shown in Figure 10 can be generated using the table shown in Figure 14. This ASCII decoder uses two 8 bit words to represent each ASCII character. The format of the decoder is consistent with either the 6800 microprocessor program shown in Figure 12 or the 8080A microprocessor program shown in Figure 13.

CODED DATA CONTROLLERS

Figure 15 shows a CODED DATA CONTROLLER designed for a 32 character 18 segment alphanumeric display. Operation of this circuit is similar to the DECODED DATA CONTROLLER shown in Figure 9 except that the Motorola 6810 RAM stores 32 six bit ASCII words and the Texas Instruments AC5947 decodes this ASCII data into 18 segment display data. The resulting display font is shown in Figure 6. Strobing of the display is accomplished by the 74LS14 oscillator and 74LS393 counter. Because the long propagation delay through the AC5947 tends to cause display ghosting, the display is

```
LOC   OBJECT CODE          SOURCE STATEMENTS

BF00                DSPLY  EQU   0BF00H

                           ORG   0E000H
E000  02   E0       ASCII  DW    DATA
E002  00            DATA   DS    32

                           ORG   0E400H
E400  01   00BF     LOAD   LXI   B,DSPLY
E403  11   00E5            LXI   D,DECDR
E406  2A   00E0            LHLD  ASCII
E409  7E            LOOP1  MOV   A,M
E40A  23                   INX   H
E408  07                   RLC
E40C  5F                   MOV   E,A
E40D  1A                   LDAX  D
E40E  02                   STAX  B
E40F  13                   INX   D
E410  03                   INX   B
E411  1A                   LDAX  D
E412  02                   STAX  B
E413  03                   INX   B
E414  79                   MOV   A,C
E415  FE   40              CPI   64
E417  C2   09E4            JNZ   LOOP1
E41A  22   00E0            SHLD  ASCII
E41D  C9                   RET
```

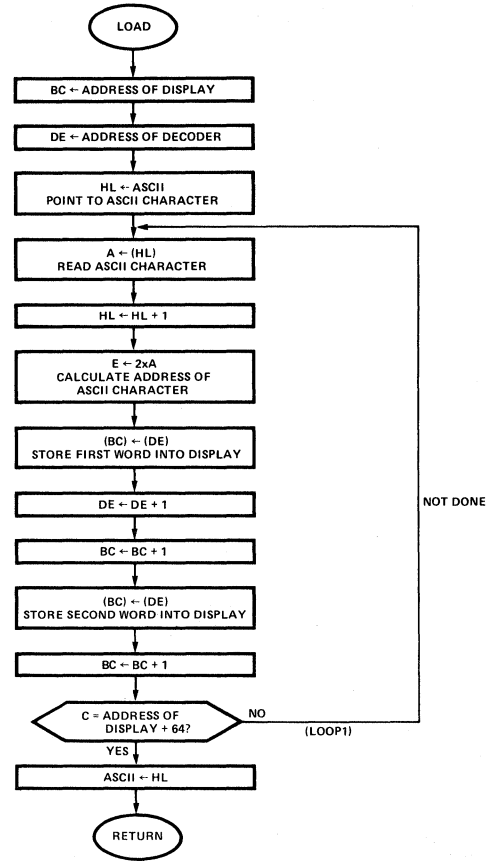


Figure 13. 8080A Microprocessor Program and Flowchart that Interfaces to the DECODED DATA CONTROLLER Shown in Figure 9

ASCII	SYMBOL	WORD 0	WORD 1
20	(SPACE)	FF	FF
21	!	FF	BD
22	"	DF	FD
23	#	36	ED
24	$	12	ED
25	%	1B	D2
26	&	F2	CA
27	'	FF	FD
28	(	FF	F3
29	)	FF	DE
2A	*	3F	C0
2B	+	3F	ED
2C	,	FF	DF
2D	-	3F	FF
2E	.	FF	BF
2F	/	FF	DB
30	0	C0	DB
31	1	FF	ED
32	2	24	FF
33	3	30	FF
34	4	19	FF
35	5	96	F7
36	6	02	FF
37	7	F8	FF
38	8	00	FF
39	9	18	FF
3A	:	FF	3F
3B	;	FF	5F
3C	<	7F	FB
3D	=	37	FF
3E	>	BF	FE
3F	?	7C	EF

ASCII	SYMBOL	WORD 0	WORD 1
40	@	44	FD
41	A	08	FF
42	B	70	ED
43	C	C6	FF
44	D	F0	ED
45	E	86	FF
46	F	8E	FF
47	G	42	FF
48	H	09	FF
49	I	F6	ED
4A	J	E1	FF
4B	K	8F	F3
4C	L	C7	FF
4D	M	C9	FA
4E	N	C9	F6
4F	O	C0	FF
50	P	0C	FF
51	Q	C0	F7
52	R	0C	F7
53	S	12	FF
54	T	FE	ED
55	U	C1	FF
56	V	CF	DB
57	W	C9	D7
58	X	FF	D2
59	Y	FF	EA
5A	Z	F6	DB
5B	[	7F	F3
5C	\	FF	F6
5D	]	BF	DE
5E	^	FF	D7
5F	_	F7	FF

Figure 14. 64 Character ASCII Decoder Table for the Microprocessor Programs Shown in Figures 12 and 13. 18 Segment Display Font is Shown in Figure 10.

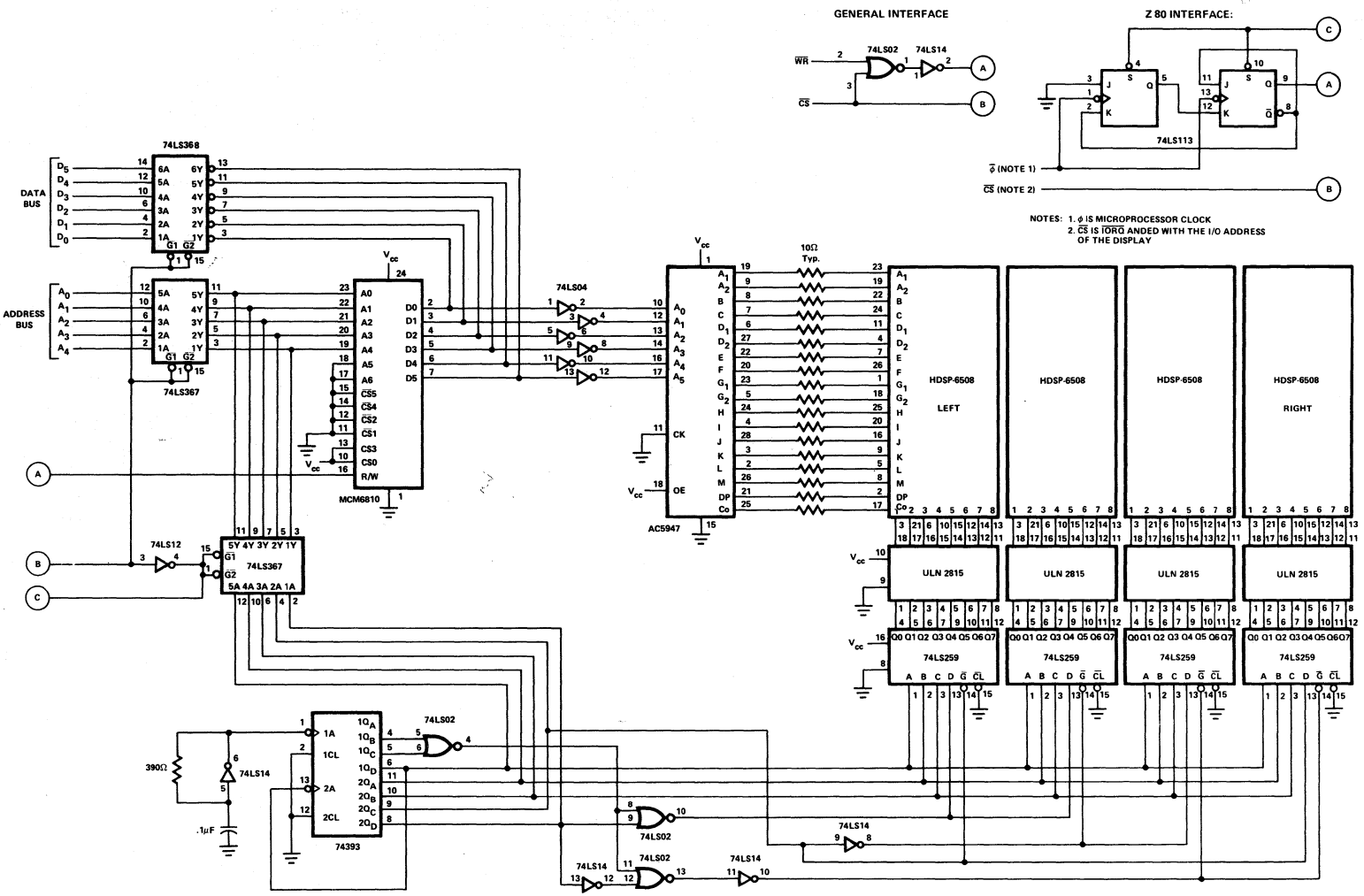
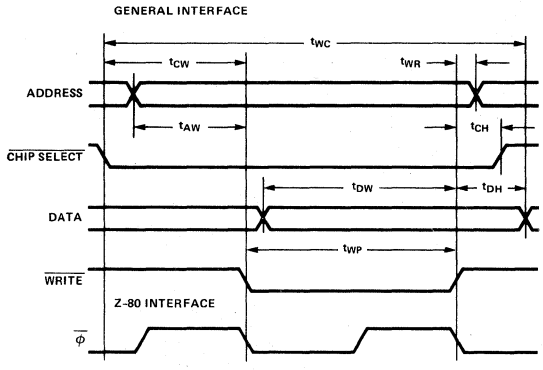


Figure 15. General Interfaces to the HDSP-6508 CODED DATA CONTROLLER



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	455ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	215ns
DATA HOLD	t_{DH}	50ns
WRITE PULSE	t_{WP}	340ns
WRITE RECOVERY	t_{WR}	40ns
CHIP ENABLE HOLD	t_{CH}	50ns

Figure 16. Data Entry Timing for the CODED DATA CONTROLLER Shown in Figure 15

blanked momentarily after each new character is read from the RAM. This is accomplished by breaking the total time allotted for each digit into four segments. During the first segment, the display is turned off to allow data to ripple through the AC5947 and during the next three segments, the display is turned on. The resulting display duty factor is (1/32) (3/4) or 1/42.6. The display is strobed at a 130 Hz refresh rate.

Data is entered into the RAM from the address and data bus of the microprocessor via two control lines Chip Select and Write. When Chip Select goes low, the address from the counter is tristated and the microprocessor address bus and data bus is gated to the RAM. Then after sufficient delay, the Write input is pulsed, which stores the data within the RAM. Data entry timing for the 18 segment CODED DATA CONTROLLER is shown in Figure 16. Since this timing is very similar to the DECODED DATA CONTROLLER shown in Figure 9, interface to the various microprocessor families is the same as described in the section on DECODED DATA CONTROLLERS.

DISPLAY PROCESSOR CONTROLLERS

The DISPLAY PROCESSOR CONTROLLER provides a powerful, smart interface which performs many of the functions normally found in a small terminal. The DISPLAY PROCESSOR CONTROLLER is designed around a slave microprocessor or custom LSI integrated circuit that provides display storage and multiplexing with a very minimum of circuit complexity. The simplest DISPLAY PROCESSOR CONTROLLER designed for a 16 digit 18 segment alphanumeric display is shown in Figure 17. This circuit is designed around the Intel 8279 Programmable Keyboard/Display Interface. This LSI chip contains the circuitry necessary to interface directly to a microprocessor bus and provides a 16 x 8 RAM, programmable scan counter, and keyboard debounce and control logic. While the 8279 is specifically designed for 7 segment displays, inclusion of the Texas Instruments AC5947 ASCII to 18 segment decoder/driver allows the use of an 18 segment alphanumeric display. The 8279 Keyboard/Display Controller interfaces to a microprocessor via an eight line bidirectional Data Bus, control lines RD (Read), WR (Write), CS (Chip Select), A_0 (Command/Data), RESET, IRQ (Interrupt Request), and a clock input, CLK. The display is scanned by outputs A_{0-3} and B_{0-3} which are connected to the inputs of the AC5947, and outputs SL_{0-3} which are connected to the digit scanning circuitry. The 74LS122 is used to provide interdigit blanking to prevent display ghosting. In addition to display scanning, the 8279 also has the ability to scan many different types of encoded or decoded keyboards, X-Y matrix keyboards, or provide a strobed data input to the microprocessor. The 8279 provides for either block data entry, where data enters from left to right across the display overflowing to the leftmost display location; right data entry, where data enters at the righthand side of the display and previous data shifts toward the left; and RAM data entry, where a four bit field in the control word specifies the address at which the next data word will be written. The 8279 allows data written into the display to be read by the microprocessor, and provides commands to either blank or clear the display.

The HDSP-8716/-8724/-8732/-8740 DISPLAY PROCESSOR CONTROLLER shown in Figure 18 is designed to provide a flexible 18 segment display interface for displays up to 40 characters in length. This circuit utilizes a dedicated Intel 8048 single chip microprocessor to provide features such as a blinking cursor, display editing routines, multiple data entry modes, variable display string length, and data out. This controller is available as a series of printed circuit board subsystems of 16, 24, 32, and 40 characters in length. The user interfaces to the 8048 microprocessor through eight Data In inputs, six Address inputs, a Chip Select input, Reset input, Blank input, six Data Out outputs, Data Valid output, Refresh output, and Clock output. The software within the 8048 microprocessor provides four data entry modes — Left Entry with a blinking cursor, Right Entry, Block Entry, and RAM Entry. The Data Out port allows the user to read the ASCII data stored within the display, determine the configured data entry mode and display length, and locate the position of the cursor within the display. Since the Data Out port is separate from the Data In port, the 18 segment DISPLAY PROCESSOR CONTROLLER can be used for text editing independent of the main microprocessor system. In Left Entry mode, the controller provides the Clear, Carriage Return, Backspace, Forwardspace, Insert, and Delete editing functions; while in Right Entry mode, the controller provides Clear and Backspace editing functions. The controller can also be expanded into multiple line panels.

The 8048 microprocessor interfaces to the display via the Port 2 output. The output is configured to enable the microprocessor to send a six bit word to one of three destinations as selected by P_{26} and P_{27}. The PROG output

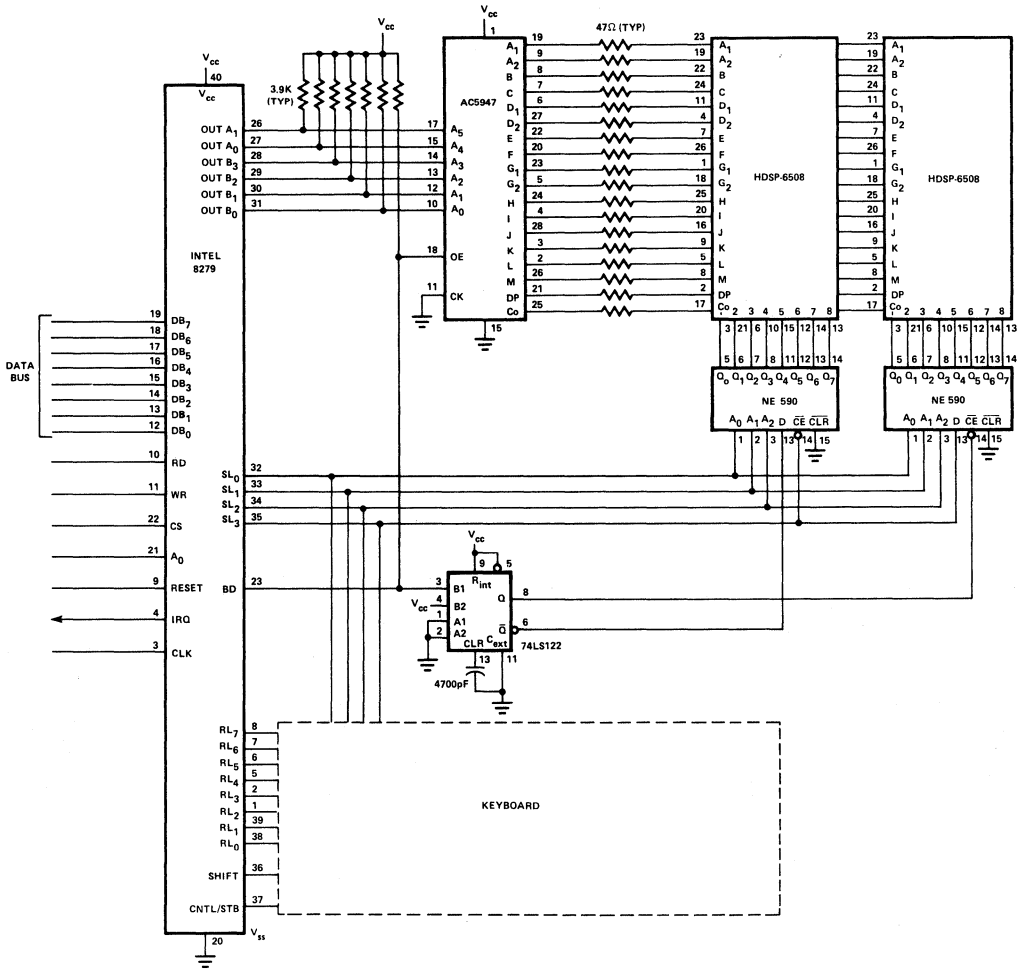


Figure 17. HDSP-6508 DISPLAY PROCESSOR CONTROLLER Utilizing the Intel 8279 Programmable Keyboard Display Interface

is then used to store this word at the specified destination. Destination$_0$ is the 74LS174 hex register. The outputs of this register are decoded by the 74LS259 addressable latches and Sprague ULN 2815 digit drivers. Output $3F_{16}$ is decoded to turn on the rightmost display digit while the address of the leftmost display digit varies from 18_{16} for a 40 character display to 30_{16} for a 16 character display. Destination$_1$ is the AC5947 18 segment decoder/driver. The positive edge of $\overline{\text{PROG}}$ stores a six bit ASCII code within the AC5947. Because destination$_1$ is pulsed once every time a digit is refreshed, this output is also used as the $\overline{\text{Refresh}}$ output. Destination$_2$ is the Data Valid output of the Data Out port. Thus, Data Out actually consists of a series of six bit words that are sent to Destination$_2$. Display refresh is accomplished by first turning off the digit drivers by outputting a 0_{16} to the 74LS174. Then a new ASCII character is stored within the AC5947. Finally, a new digit word is stored within the 74LS174. The actual time that each digit is on varies according to the configured display length so as to provide a fixed 100 Hz refresh rate.

Interfacing the DISPLAY PROCESSOR CONTROLLER shown in Figure 18 to microprocessor systems depends on the needs of the particular application. Since the information on the Data In and Address inputs is loaded into the controller through a program within the 8048 microprocessor, the time required to read these inputs varies from about 100 to 700 microseconds. A latch as shown in the HDSP-8716/-8724/-8732/-8740 Data Sheet can be used as a buffer between these inputs and the data bus and address bus of the main microprocessor system. The latch provides temporary storage to avoid making the main microprocessor wait for the DISPLAY PROCESSOR CONTROLLER to accept data.

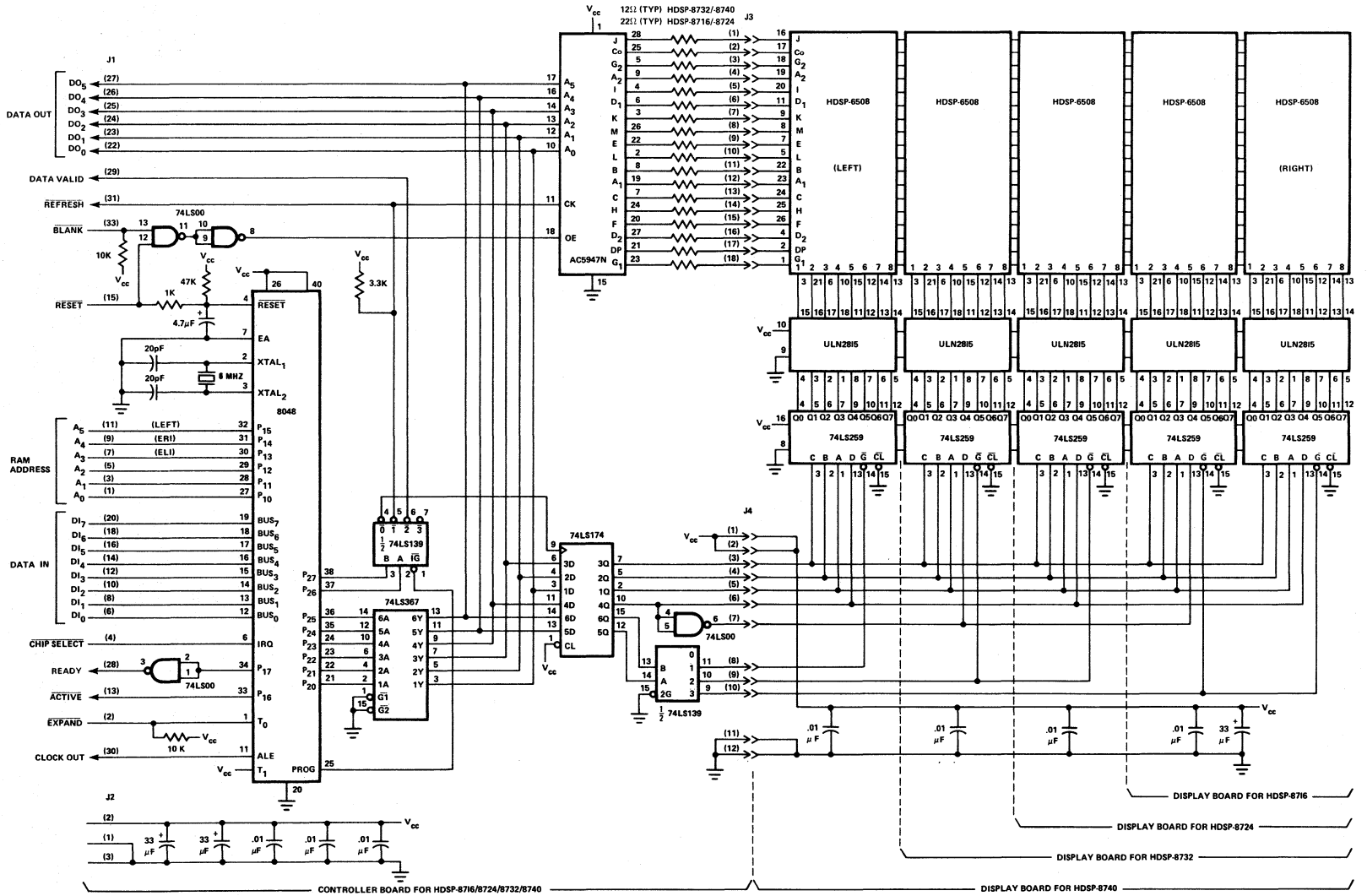


Figure 18. HDSP-8716/-8724/-8732/-8740 DISPLAY PROCESSOR CONTROLLER

The 18 segment DISPLAY PROCESSOR CONTROLLER shown in Figure 18 can also be interfaced to the main microprocessor system through a Peripheral Interface Adapter (PIA). The Data In inputs of the controller would be connected to an output port of the PIA. In RAM Entry mode, the Address inputs of the controller would be connected to another output port of the PIA. The PIA provides a handshake back to the main microprocessor system that tells when the DISPLAY PROCESSOR CONTROLLER is ready to accept another data input word from the main microprocessor. This allows the microprocessor to load data into the controller at the highest possible rate. A PIA can also be used to allow the 18 segment DISPLAY PROCESSOR CONTROLLER to act as a buffer between a keyboard and the main microprocessor. In this configuration, the main processor could output a prompting message to the user via the DISPLAY PROCESSOR CONTROLLER. The user could then enter data from the keyboard into the display utilizing the controller's editing capability. After the message has been entered and edited, the user would instruct the main microprocessor to read the final edited message from the Data Out port. One port from the PIA can be used to control the Data In inputs of the DISPLAY PROCESSOR CONTROLLER and another port of the PIA can be used to read the Data Out port. Figure 19 shows a 6800 microprocessor system using a Motorola 6821 PIA to control the DISPLAY PROCESSOR CONTROLLER shown in Figure 18. The PB_7 output of the PIA determines whether data is entered into the controller

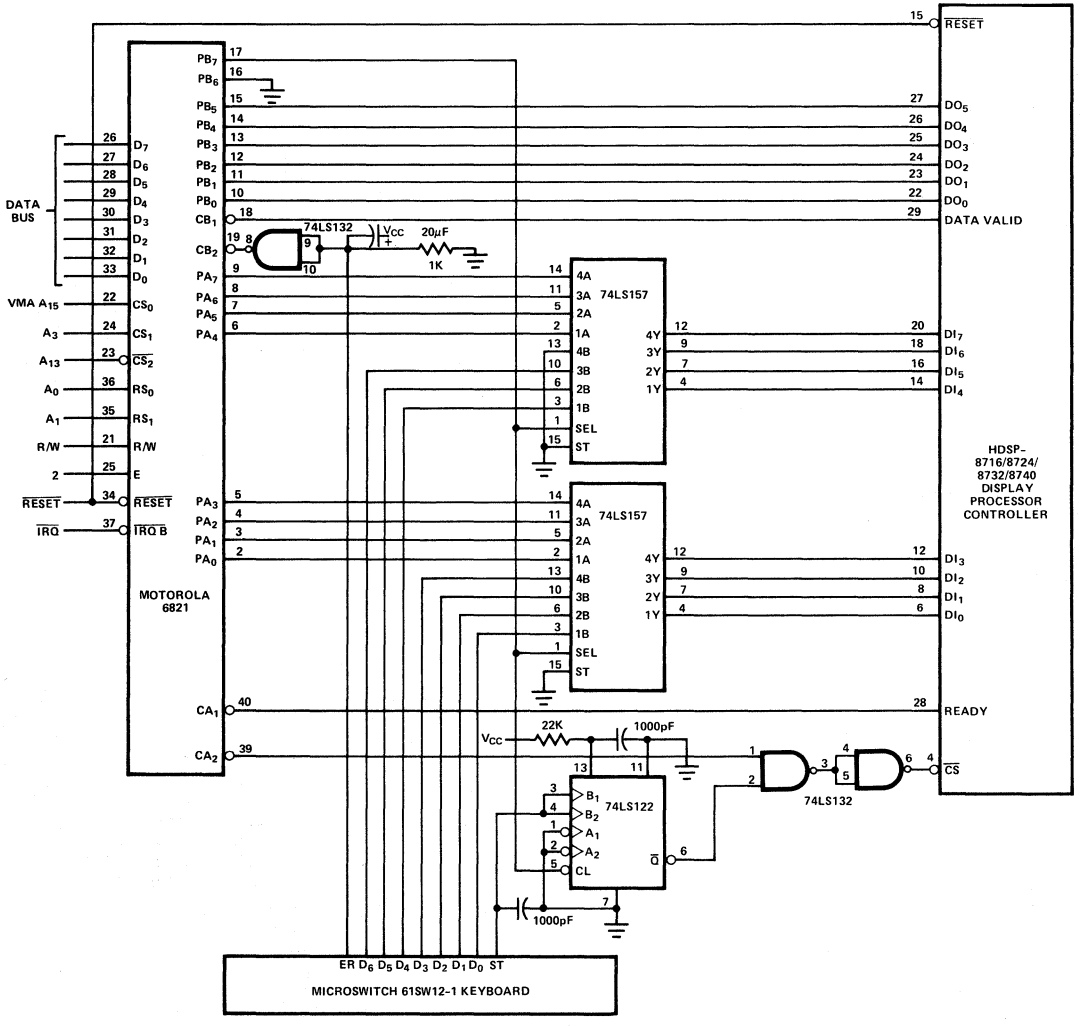


Figure 19. 6800 Microprocessor Interface to the DISPLAY PROCESSOR CONTROLLER Shown in Figure 18 Utilizing a Motorola 6821 PIA

```
* PORT CONFIGURATION:
* 1. PORT A:
*        PA0-PA7 OUTPUTS TO DATA IN OF HDSP-87XX
*        CA1 (INPUT) MODE 00 SETS FLAG NEG EDGE OF READY
*        CA2 (OUTPUT) MODE 100 CLEARED MPU READ PRA, SET
*        NEGATIVE EDGE OF READY
* 2. PORT B:
*        PB0-PB5 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP
*        CB1 (INPUT) MODE 10 SETS FLAG POS EDGE OF DATA VA
*        CB2 (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
*        CB2 (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
*        CAUSING IRQ
*        PB7 (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
*                     HIGH ENABLES KEYBOARD TO MUX AND KEY

          8008      PRA     EQU     $8008
          8008      DRA     EQU     $8008
          8009      CRA     EQU     $8009
          800A      PRB     EQU     $800A
          800A      DRB     EQU     $800A
          800B      CRB     EQU     $800B
          0028      LENGTH  EQU     40          MUST BE SAME AS LENGTH

0000                        ORG     $0000
0000 0002           MESSGE  FDB     TEXT

0100                        ORG     $0100
0100                STATUS  RMB     1
0101                CURSOR  RMB     1
0102                DATA    RMB     40


0400                        ORG     $0400
0400 CE 0100        READ    LDX     I,STATUS
0403 7F 800A                CLR     E,PRB       ENABLE PORT A TO MUX
0406 86 FF                  LDA A   I,$FF
0408 B7 8008                STA A   E,PRA       BEGIN DATA OUT SEQUENCE
040B 7D 8008                TST     E,PRA       CLEAR CA1 AND CA2
040E 7D 800A                TST     E,PRB       CLEAR CB1 AND CB2
0411 C6 2A                  LDA B   I,LENGTH+2
0413 B6 800B        LOOP1   LDA A   E,CRB
0416 2A FB                  BPL     LOOP1       WAIT FOR DATA VALID
0418 B6 800A                LDA A   E,PRB
041B 84 3F                  AND A   I,$3F
041D A7 00                  STA A   X,0         STORE IN RAM
041F 08                     INX
0420 5A                     DEC B
0421 26 F0                  BNE     LOOP1       NEXT DATA OUT WORD
0423 7D 8008                TST     E,PRA       CLEAR CA1 AND CA2
0426 B6 8009        LOOP2   LDA A   E,CRA
0429 2A FB                  BPL     LOOP2       WAIT UNTIL READY
042B 39                     RTS

042C DE 00          LOAD    LDX     D,MESSGE
042E A6 00          LOOP10  LDA A   X,0
0430 08                     INX
0431 81 FF                  CMP A   I,$FF
0433 27 0D                  BEQ     ENDL        JUMP WHEN DONE
0435 B7 8008                STA A   E,PRA
0438 7D 8008                TST     E,PRA       CLEAR CA1 AND CA2
043B B6 8009        LOOP11  LDA A   E,CRA
043E 2A FB                  BPL     LOOP11      WAIT
0440 20 EC                  BRA     LOOP10
0442 DF 00          ENDL    STX     D,MESSGE
0444 39                     RTS

0500                        ORG     $0500
0500 7F 8009        START   CLR     E,CRA
0503 7F 800B                CLR     E,CRB
0506 86 FF                  LDA A   I,$FF
0508 B7 8008                STA A   E,DRA
050B 86 24                  LDA A   I,$24
050D B7 8009                STA A   E,CRA
0510 86 80                  LDA A   I,$80
0512 B7 800A                STA A   E,DRB
0515 86 06                  LDA A   I,$06
0517 B7 800B                STA A   E,CRB
051A 0E             MAIN    CLI
051B 7F 800A                CLR     E,PRB       DISABLE KEYBOARD FROM MUX
051E BD 042C                JSR     E,LOAD
0521 7D 800A                TST     E,PRB       CLEAR CB1, CB2
0524 86 80                  LDA A   I,$80
0526 B7 800A                STA A   E,PRB       ENABLE KEYBOARD TO MUX
0529 86 0E                  LDA A   I,$0E
052B B7 800B                STA A   E,CRB       ENABLE IRG
052E 0F                     SEI                 IRQ CAUSES JSR TO READ
```

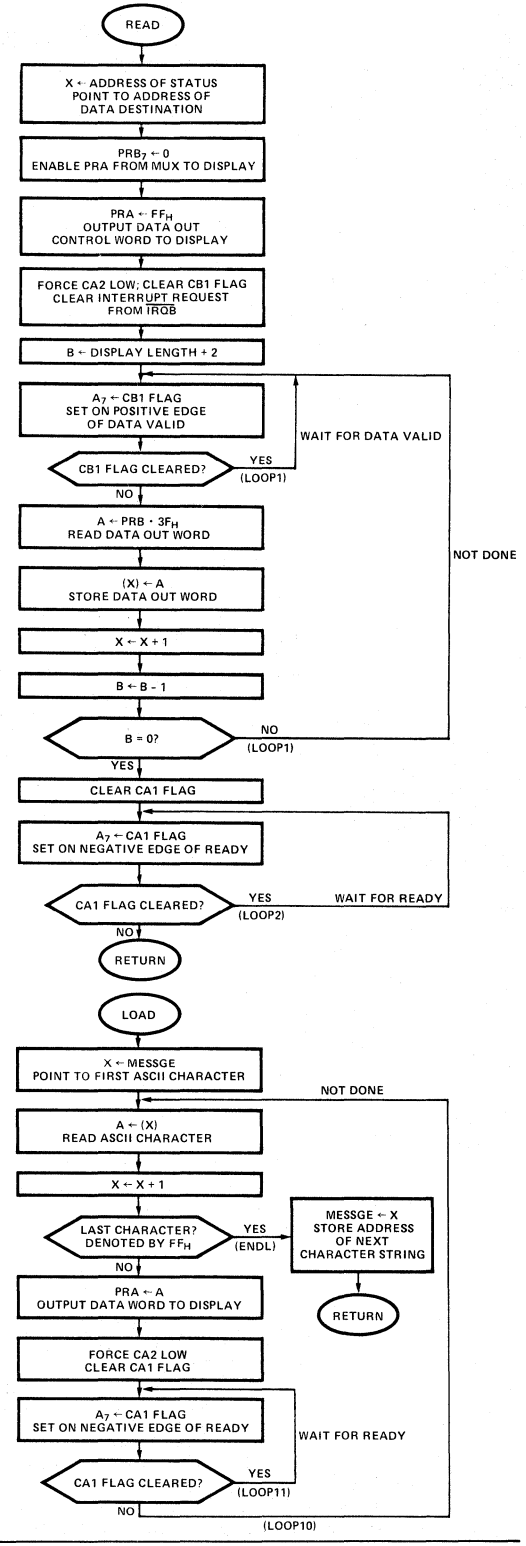


Figure 20. 6800 Microprocessor Program and Flowchart that Interfaces to the Circuit Shown in Figure 19

from the microprocessor system or from the keyboard. Control lines CA_1 and CA_2 are used to provide a data entry handshake to allow data to be loaded into the controller at the highest possible rate. Data is read into the main microprocessor system through Port B of the PIA using the CB_1 input as a data strobe.

The 6800 microprocessor program shown in Figure 20 is used to operate the PIA interface described in Figure 19. The microprocessor program following "START" is used to initialize the 6821 PIA. Once initialized, the PIA can be used either to load data into the controller via the main microprocessor, allow data to be loaded into the controller via the keyboard, or to read data from the Data Out port into the main microprocessor. The instruction CLR E, PRB at location $051B_{16}$ forces PB_7 low to connect the outputs of Port A to the Data In inputs of the controller.

Subroutine "LOAD" then loads a series of eight bit words into the controller. "LOAD" continues to output words until it reads an FF_{16} to denote the end of the prompting message. The instruction sequence LDA A I, $80 and STA A E, PRB at location 0526_{16} forces PB_7 high to connect the output of the keyboard to the Data In inputs of the controller. In this mode, the user can enter or edit data into the DISPLAY PROCESSOR CONTROLLER. The 4B input of the 74LS157 has been grounded to prevent the keyboard from loading a control word into the DISPLAY PROCESSOR CONTROLLER. The instructions LDA A I, $0E and STA A E, CRB at location $052B_{16}$ enables the "ER" key on the keyboard to interrupt the microprocessor when the edited message is complete. Subroutine "READ" would then be used to read data into the 6800 system. First, subroutine "READ" outputs a special control word,

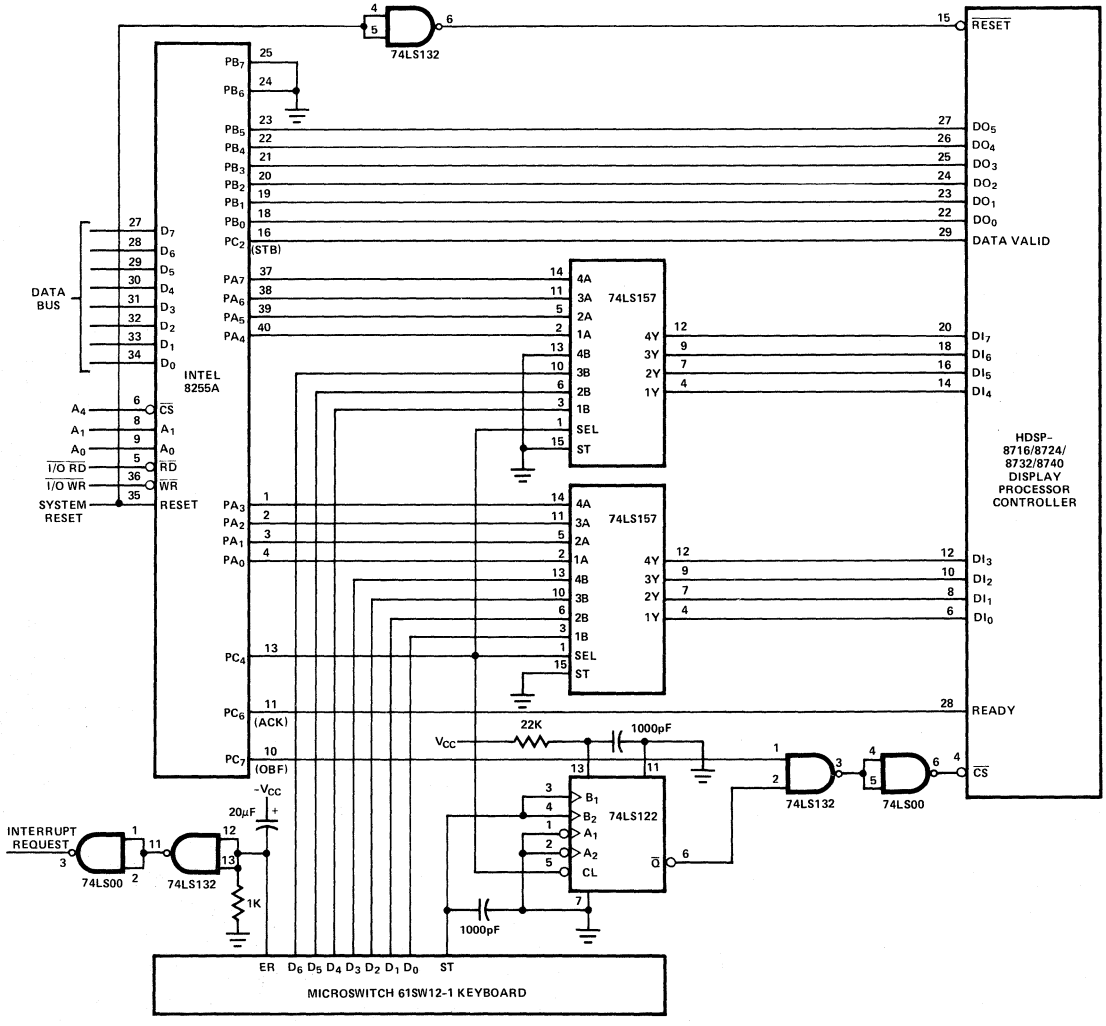


Figure 21. 8080A Microprocessor Interface to the DISPLAY PROCESSOR CONTROLLER Shown in Figure 18 Utilizing an Intel 8255 PIA

```
;THIS PROGRAM IS WRITTEN IN 8080 ASSEMBLY LANGUAGE.
;THIS PROGRAM USES AN 8255 PIA TO ACCESS THE HDSP-87XX
;ALPHANUMERIC DISPLAY SYSTEM.
;
;PORT CONFIGURATION:
;1. PORT A (MODE 1 OUTPUT):
;       PA0-PA7 OUTPUTS TO DATA IN OF HDSP-87XX
;       PC7 (OBF) OUTPUT; TO CHIP SELECT
;       PC6 (ACK) INPUT; TO READY
;       FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
;
;2. PORT B (MODE 1 INPUT):
;       PB0-PB6 INPUTS DATA FROM DATA OUT OF HDSP-87XX
;       PC2 (STB) INPUT; LOADS DATA ON POS EDGE OF DATA VALID
;       FLAG PC0 (INTR) CLEARED BY INPUT; SET BY DATA VALID
;
;3. PORT C:
;       PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-87XX
;                   HIGH ENABLES KEYBOARD TO HDSP-87XX

000C            PA      EQU     0CH
000D            PB      EQU     0DH
000E            PC      EQU     0EH
000F            CNTRL   EQU     0FH
0028            LENTH   EQU     40          MUST BE DISPLAY LENGTH
                        ORG     0E000H
E000 02 E0      ASCII   DW      TEXT
E002 00         TEXT    DS      40
                ;
                        ORG     0E100H
E100 00         STAT    DB      0
E101 00         ADDR    DB      0
E102 00         DATA    DB      0
                ;
                        ORG     0E400H
E400 F3         READ    DI
E401 F5                 PUSH    PSW
E402 E5                 PUSH    H
E403 C5                 PUSH    B
E404 3E 08              MVI     A,08H
E406 D3 0F              OUT     CNTRL       ENABLE A SIDE OF MUX
E408 3E FF              MVI     A,0FFH
E40A D3 0C              OUT     PA          BEGIN DATA OUT SEQUENCE
E40C 0E 2A              MVI     C,LENTH+2
E40E 21 00E1            LXI     H,STAT      FIRST WORD
E411 DB 0D              IN      PB          CLEAR INTR
E413 DB 0E      LOOP1   IN      PC
E415 1F                 RAR
E416 D2 13E4            JNC     LOOP1       WAIT UNTIL INTR IS SET
E419 DB 0D              IN      PB
E41B 77                 MOV     M,A         STORE IN RAM
E41C 23                 INX     H
E41D 0D                 DCR     C
E41E C2 13E4            JNZ     LOOP1       READ LENGTH+2 WORDS
E421 DB 0E      LOOP2   IN      PC
E423 17                 RAL
E424 D2 21E4            JNC     LOOP2       WAIT UNTIL READY
E427 C1                 POP     B
E428 E1                 POP     H
E429 F1                 POP     PSW
E42A FB                 EI
E42B C9                 RET
                ;
E42C 2A 00E0    LOAD    LHLD    ASCII       FIRST WORD OF MESSAGE
E42F 7E         LOOP5   MOV     A,M
E430 FE FF              CPI     0FFH        CHECK TO SEE IF DONE
E432 CA 44E4            JZ      ENDL
E435 D3 0C              OUT     PA          OUTPUT TO DISPLAY
E437 23                 INX     H
E438 DB 0E      LOOP6   IN      PC
E43A 17                 RAL
E43B D2 38E4            JNC     LOOP6       WAIT
E43E 00                 NOP
E43F 00                 NOP
E440 00                 NOP
E441 C3 2FE4            JMP     LOOP5       NEXT WORD
E444 23         ENDL    INX     H
E445 22 00E0            SHLD    ASCII
E448 C9                 RET
                ;
E449 3E A7      START   MVI     A,0A7H      PA AS M1 OUTPUT, PB AS M1 INPUT
E44B D3 0F              OUT     CNTRL
E44D 3E 0C              MVI     A,0CH       CLEAR INTE A
E44F D3 0F              OUT     CNTRL
E451 3E 05              MVI     A,05H
E453 D3 0F              OUT     CNTRL       SET INTE B
                ;
                ;PROCEDURE TO LOAD HDSP-87XX SYSTEM
                ;
E455 3E 08              MVI     A,08H
E457 D3 0F              OUT     CNTRL       ENABLE A SIDE OF MUX
E459 CD 2CE4            CALL    LOAD
                ;
                ;PROCEDURE TO READ DATA OUT OF HDSP-87XX SYSTEM
                ;
E45C 3E 09              MVI     A,09H
E45E D3 0F              OUT     CNTRL       ENABLE B SIDE OF MUX
E460 FB                 EI
                ;                           INTERRUPT MUST CALL READ
```

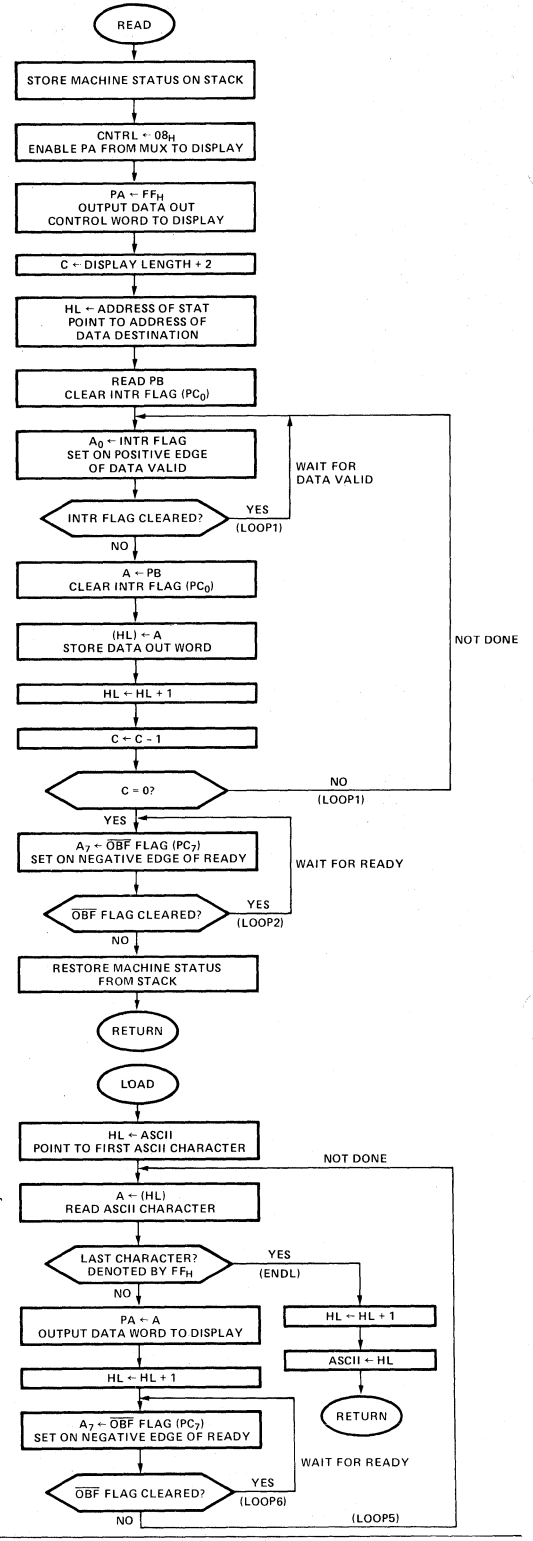


Figure 22. 8080A Microprocessor Program and Flowchart that Interfaces to the Circuit Shown in Figure 21

FF_{16}, to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. This control word causes the controller to begin its data output sequence. The controller outputs a series of data output words that define the configured entry mode and display length, location of the cursor, and the ASCII text stored within the DISPLAY PROCESSOR CONTROLLER. "LOOP 1" within the program continuously reads the Data Valid output and waits until the controller outputs the STATUS word. This STATUS word, the subsequent CURSOR ADDRESS word, and the string of ASCII characters are then stored in consecutive words of scratch pad memory starting at address "STATUS."

A similar PIA interface designed for an 8080A microprocessor system that uses an Intel 8255A PIA is shown in Figure 21. This interface operates in much the same way as the 6821 PIA interface that was previously described. The PC_4 output of the PIA determines whether the Data In inputs of the 18 segment DISPLAY PROCESSOR CONTROLLER shown in Figure 18 are connected to the PIA or to the keyboard. Control lines PC_6 and PC_7 are used to provide a data entry handshake between the 8080A microprocessor and the DISPLAY PROCESSOR CONTROLLER. Data is read into the 8080A microprocessor system through Port B of the PIA using PC_2 as the data strobe.

The 8080A microprocessor program shown in Figure 22 is used to operate the PIA interface described in Figure 21. The microprocessor program following "START" is used to initialize the 8255A PIA. The instructions MVI A, 08H and OUT CNTRL at location $E457_{16}$ force PC_4 low to connect Port A of the PIA to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. Subroutine "LOAD" would then be used to load a prompting message into the controller. The instructions MVI A, 09H and OUT CNTRL at location $E45E_{16}$ connect the keyboard to the Data In inputs of the controller. In this mode, the user can enter data into the DISPLAY PROCESSOR CONTROLLER, or to edit an existing line. Subroutine "READ" would then be used to read the data from the Data Out port into the 8080A microprocessor system.

Subroutine "READ" begins the data output sequence by outputting the special control word FF_H to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. Then, the subroutine reads the series of data output words that are outputted by the controller and stores them in consecutive words of scratch pad memory starting at address STAT.

HEWLETT PACKARD

APPLICATION NOTE 1004

Threshold Sensing For Industrial Control Systems With the HCPL-3700 Interface Optocoupler

INTRODUCTION

The use of electronic logic circuitry in most applications outside of a controlled environment very quickly brings the design engineer into contact with the problems and hazards involved in interfacing between the logic function and the controlled function. These problems have always been particularly evident in the field of industrial control where the electrically "noisy" environment produced by motors, power lines, lightning and other sources of interference may mask the desired signal, and in some cases even result in the destruction of the logic control system itself. In these situations, the designer must resort to solutions which will provide isolation between the logic system and the input or output function Traditional methods of isolation involve the use of such devices as capacitors, relays, tranformers, and optocouplers. Of these methods, the optocoupler provides an ideal combination of speed, dc response, high common mode rejection, and low input to output coupling capacitance.

In the implementation of an interface from an electrically noisy environment into logic systems, it is often desirable, if not mandatory, to establish some current or voltage switching point or threshold at which the input signal is considered true. Since the input, or feedback, signal in industrial control systems may be ac or dc and may range from low, 5 volt, levels to 110 or 240 volts ac, the design of such a threshold switching system can become more than a trivial problem. This is especially true when using the optocoupler, considering the relatively large range of current transfer ratio (CTR) found in most devices.

The problem of establishing an input switching threshold is resolved in the design of the Hewlett-Packard HCPL-3700 optocoupler. This device combines an ac or dc voltage and/or current detection function with a high insulation voltage optocoupler in a single eight pin plastic dual in-line package.

As shown in the block diagram of Figure 1, this device consists of a full-wave bridge rectifier and threshold detection integrated circuit, an LED, and an optically coupled detector integrated circuit. The detector circuit is a combination of a photodiode and a high current gain, split Darlington, amplifier.

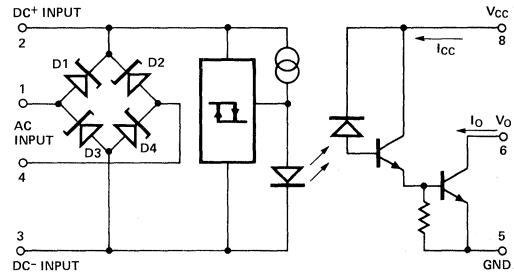


Figure 1. Block Diagram of the HCPL-3700

The input circuit will operate from an ac or dc source and provide a guaranteed, temperature compensated threshold level with hysteresis. The device may be programmed for higher switching thresholds through the use of a single external resistor.

With threshold level detection provided prior to the optical isolation path and subsequent gain stage, variations in the current transfer ratio of the device with time or from unit to unit are no longer important.

In addition to allowing ac or dc input signals, the Zener diodes of the bridge circuit also provide input voltage clamping to protect the threshold circuitry and LED from over voltage/current stress conditions. The LED current is provided by a switched current source.

The HCPL-3700 optocoupler output is an open collector, high gain, split Darlington configuration. The output is compatible with TTL and CMOS logic levels. High common mode rejection, or transient immunity of 600V/μs, allows excellent isolation. Insulation capability is 3000 volts dc. The recommended operating temperature range is 0°C to 70°C.

The HCPL-3700 meets the requirements of the industrial control environment for interfacing signals from ac or dc power equipment to logic control electronics. Isolated monitoring of relay contact closure or relay coil voltages, monitoring of limit or proximity switch operation or sensor signals for temperature or pressure, etc., can be accomplished by the HCPL-3700. The HCPL-3700 may also be used for sensing low power line voltage (Brown Out) or loss of line power (Black Out).

Device Characteristics

The function of the HCPL-3700 can best be understood through a review of the input V/I function and the input to output transfer function. Figure 2 shows the input characteristics, I_{IN} (mA) versus V_{IN} (volts), for both the ac and dc cases.

The dc input of the HCPL-3700 appears as a 1000Ω resistor in series with a one volt offset. If the ac pins (1, 4) are left unconnected, the dc input voltage can increase to 12V (two Zener diode voltages) before the onset of input voltage clamping occurs. If the ac pins (1, 4) are connected to ground or to dc pins (2, 3) respectively, the dc input voltage will clamp at 6.0V (one Zener diode voltage). Under clamping conditions, it is important that the maximum input current limits not be exceeded. Also, to prevent excessive current flow in a substrate diode, the dc input can not be backbiased more than −0.5V. The choice of the input voltage clamp level is determined by the requirements of the system design. The advantages of clamping the input at a low voltage level is in limiting the magnitude of forward current to the LED as well as limiting the input power

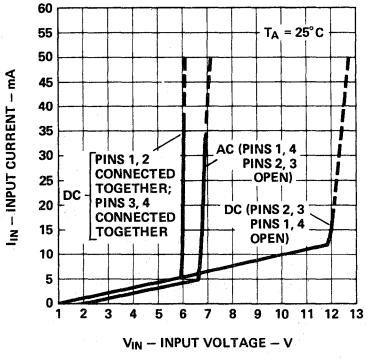


Figure 2. Typical Input Characteristics, I_{IN} vs. V_{IN}

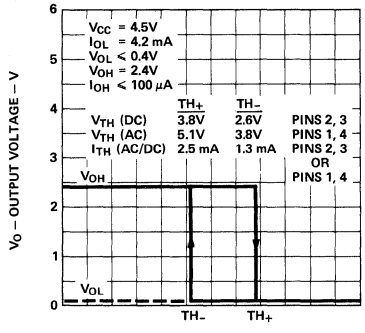


Figure 3. Typical Transfer Characteristics of the HCPL-3700

to the device during large voltage or current transients in the industrial control environment. The internal limiting will in some cases eliminate the need for additional protection components.

The ac input appears similar to the dc input except that the circuit has two additional diode forward voltages. The ac input voltage will clamp at 6.7V (one Zener diode voltage plus one forward biased diode voltage), and is symmetric for plus or minus polarity. The ac voltage clamp level can not be changed with different possible dc pin connections.

The transfer characteristic displayed in Figure 3 shows how the output voltage varies with input voltage, or current, levels. Hysteresis is provided to enhance noise immunity, as well as to maintain a fast transition response (t_r, t_f) for slowly changing input signals.

The hysteresis of the device is given in voltage terms as $V_{HYS} = V_{TH+} - V_{TH-}$, or in terms of current as $I_{HYS} = I_{TH+} - I_{TH-}$. The optocoupler output is in the high state until the input voltage (current) exceeds $V_{TH+}(I_{TH+})$. The output state will return high when the input voltage (current) becomes less than $V_{TH-}(I_{TH-})$.

As is shown in Figure 3, the HCPL-3700 has preprogrammed ac and dc switching threshold levels. Higher input switching thresholds may be programmed through the use of a single series input resistance as defined in Equation (1). In some cases, it may be desirable to split this resistance in half to achieve transient protection on each input lead and reduce the power dissipation requirement of each of the resistors.

Figure 4 illustrates three typical interface situations which a designer may encounter in utilizing a microprocessor as a controller in industrial environments.

Example 1. A dc voltage applied to the motor is monitored as an indication of proper speed and/or load condition.

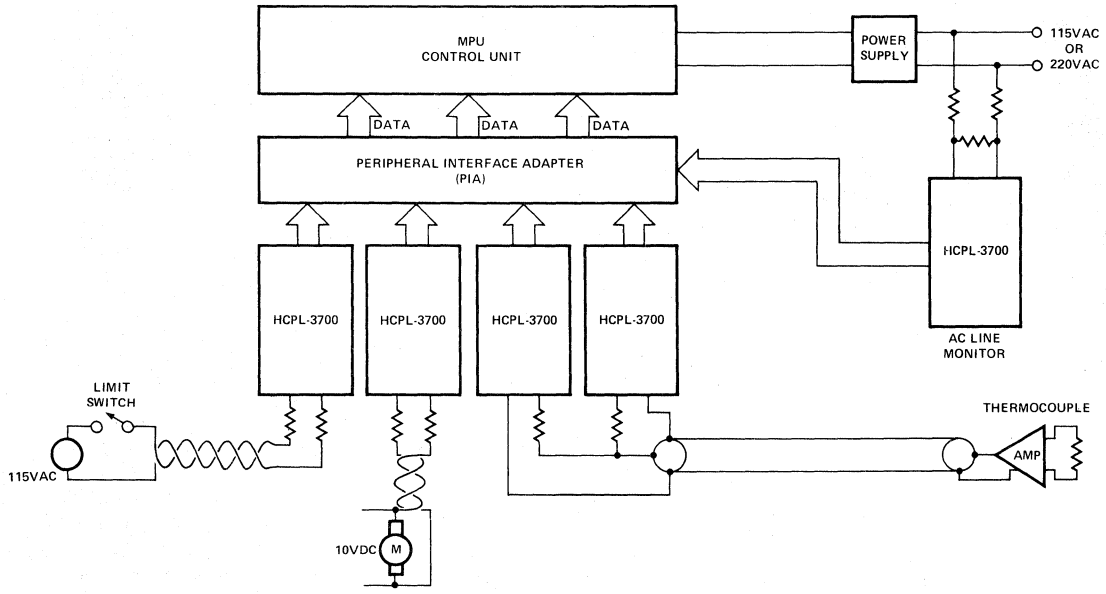


Figure 4. Applications of the HCPL-3700 for Interfacing AC and DC Voltages to a Microprocessor

Example 2. A limit switch uses a 115V ac or 220V ac control loop to improve noise immunity and because it is a convenient high voltage for that purpose.

Example 3. An HCPL-3700 is used to monitor a computer power line to sense a loss of line power condition. Use of a resistive shunt for improvement of threshold accuracy is analyzed in this example.

Also illustrated is an application in which two HCPL-3700's are used to monitor a window of safe operating temperatures for some process parameters. This example also requires a rather precise control of the optocoupler switching threshold. An additional dedicated leased line system example is also shown (Example 4).

Example 1. DC Voltage Sensing

The dc motor monitor function is established to provide an indication that the motor is operating at a minimum desired speed prior to the initiation of another process phase. If the applied voltage, V_M, is greater than 5V, it is assumed that the desired speed is obtained. The maximum applied voltage in the system is 10V. The HCPL-3700 circuit configuration for this dc application is shown in Figure 5.

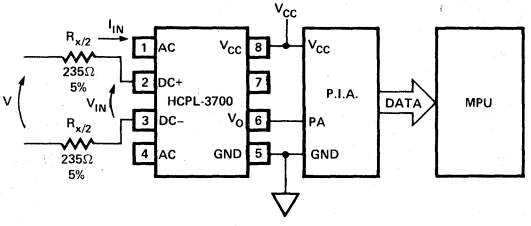


Figure 5. Interfacing a DC Voltage to an MPU using the HCPL-3700

NOTE: See Appendix for a definition of terms and symbols for this and all other examples.

The following conditions are given for the external voltage threshold level and input requirements of the HCPL-3700:

External Voltage Levels – V_M

V_+ = 5V dc (50%)

V_{peak} = 10V dc

HCPL-3700 Input Levels

$V_{TH+} = 3.8V$

$V_{TH-} = 2.6V$

$V_{ICH3} = 12V$

$I_{TH+} = 2.5mA$

$I_{TH-} = 1.3mA$

For the 5V threshold, R_x is calculated via the expression:

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (1)$$

$$= \frac{5V - 3.8V}{2.5mA}$$

$R_x = 480\Omega \quad (470\Omega \pm 5\%)$

The resultant lower threshold level is formed by using the following expression:

$$V_- = I_{TH-} R_x + V_{TH-} \quad (2)$$

$$= (1.3mA)\ 470\Omega + 2.60V$$

$V_- = 3.21V$

With the possible unit to unit variations in the input threshold levels as well as ±5% tolerance variations with R_x, the variation of V_+ is +12.4%, −15% and V_- varies +14%, −23.5%. (NOTE: With a low, external, voltage threshold level, V_+, which is comparable in magnitude to the V_{TH+} voltage threshold level of the optocoupler ($V_+ \leq 10V_{TH+}$) the tolerance variations are not significantly improved by the use of a 1% precision resistor for R_x. However, at a large external voltage threshold level compared to V_{TH+} ($V_+ > 10V_{TH+}$), the use of a precision 1% resistor for R_x does reduce the variation of V_+.)

For simultaneous selection of external upper, V_+, and lower, V_-, voltage threshold points a combination of a series and parallel input resistors can be used. Refer to the example on "ac operation with improved threshold control and accuracy" for detailed information.

Calculation of the maximum power dissipation in R_x is determined by knowing which of the following inequalities is true:

$$\frac{V_+}{V_{peak}} > \frac{V_{TH+}}{V_{IHC}} \quad (V_{IN} \text{ will not clamp}) \quad (3)$$

$$\frac{V_+}{V_{peak}} < \frac{V_{TH+}}{V_{IHC}} \quad (V_{IN} \text{ will clamp}) \quad (4)$$

where V_{IHC} is the particular input clamp voltage listed on the data sheet.

For this dc application with ac pins (1, 4) open, input voltage clamping will not occur, i.e.,

$$\frac{V_+}{V_{peak}} > \frac{V_{TH+}}{V_{IHC3}}$$

$$\frac{5V}{10V} > \frac{3.8V}{12.0V}$$

Consequently, a conservative value for the maximum power dissipation in R_x for the unclamped input voltage condition ignoring the input offset voltage is given by:

$$P_{R_x} = \frac{\left[V_{peak}\left(\frac{R_x}{R_x + 1\,k\Omega}\right)\right]^2}{R_x} \quad \text{(Unclamped Input)} \quad (5)$$

$$= \frac{\left[10V\left(\frac{470\Omega}{1470\Omega}\right)\right]^2}{470\Omega}$$

$P_{R_x} = 21.8mW$

If $V_+/V_{peak} < V_{TH+}/V_{IHC}$ was true (clamped input voltage condition), then the formula for the maximum power dissipation in R_x becomes:

$$P_{R_x} = \frac{(V_{peak} - V_{IHC})^2}{R_x} \quad \text{(Clamped Input)} \quad (6)$$

The maximum input current or power must be determined to ensure that it is within the maximum input rating of the HCPL-3700. For the clamped input voltage condition,

$$I_{IN} = \frac{V_{peak} - V_{IHC}}{R_x} < I_{IN\,(max)} \quad (7)$$

or

$$P_{IN} = V_{IHC}(I_{IN}) < P_{IN\,(max)} \quad (8)$$

Clamped Condition

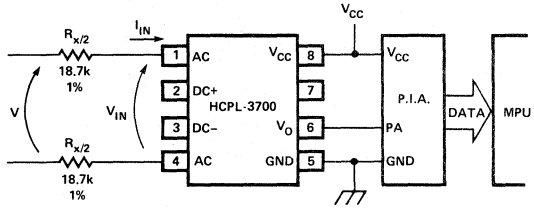


Figure 6. Interfacing an AC Voltage to an MPU using the HCPL-3700

For the unclamped input voltage condition, the maximum input current, or power will not be exceeded, because maximum input current and power will occur only under clamp conditions.

An output load resistance is not needed in this application because the peripheral interface adapter, such as MC6821, has an internal pullup resistor connected to its input.

Example 2. AC Operation

As shown in Figure 6, an ac application is that of a monitored 115V ac limit switch. Ac sensing is commonly used and the HCPL-3700 conveniently provides an internal rectification circuit. With the HCPL-3700 interfacing to the P.I.A., a choice can be made not to filter the ac signal or to filter the ac signal at the input or output of the device. All three conditions will be explored. Simplicity is obtained with no filtering at all, but software detection techniques must be used. Output filtering is a standard method, but may present problems with slow RC rise time of the output waveform when TTL logic is used. Input filtering avoids the RC rise time problem of output filtering, but introduces an extra time delay at the input.

AC Operation With No Filtering

In this example, a V_+ value of 98V is selected based on a criteria of 60% of V_{peak}. Monitoring a limit switch for a 60% level of the signal will give sufficient noise immunity from an open 115V ac line while allowing the HCPL-3700 to turn on under low line voltage conditions of −15% from nominal values when the limit switch is closed.

The value of R_X for the upper threshold detection level without the filter capacitor, C, across the dc input, can be obtained from the following expression.

$$R_X = \frac{V_+ - V_{TH+}}{I_{TH+}} \qquad (9)$$

V_{TH+} = 5.1V (ac instantaneous)

I_{TH+} = 2.5mA

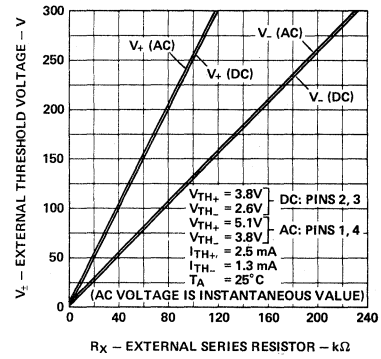


Figure 7. Typical External Threshold Characteristic, $V_\pm$ – vs. R_X

$$R_X = \frac{98V - 5.1V}{2.5mA}$$

R_X = 37.2kΩ (use $R_X/2$ = 18.7kΩ, 1% resistor for each input lead)

The resulting lower threshold point is

$$V_- = I_{TH-}R_X + V_{TH-} \qquad (10)$$

$$= (1.3mA)(37.4k\Omega) + 3.8V$$

V_- = 52.4V (32% of peak input voltage)

Figure 7 provides a convenient, graphical choice for the external series resistor, R_X, and a particular external threshold voltage $V_\pm$.

The corresponding R_X value and output waveform of the HCPL-3700 for a V_+ = 98V (60% of peak) is shown in Figure 8.

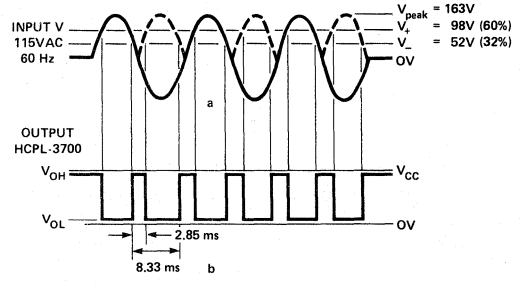


Figure 8. Output Waveforms of the HCPL-3700 Design in Figure 7 with no Filtering Applied

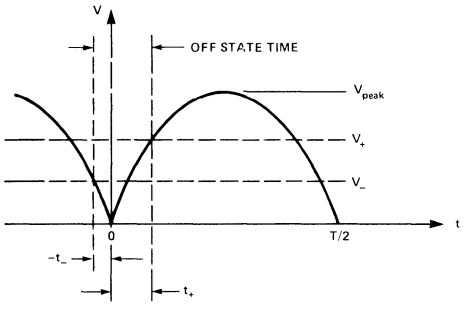


Figure 9. Determination of Off/On State Time

To determine the time in the high state, refer to Figure 9 and Equation (11).

Due to symmetry of sinusoidal waveform, the high state time is $t_- + t_+$ where $t_\pm$ is given by:

$$t_\pm = \frac{T}{360^\circ} \sin^{-1}\left(\frac{V_\pm}{V_{peak}}\right) \qquad (11)$$

where arc sine is in degrees and T = period of sinusoidal waveform.

In the unfiltered condition, the output waveform of Figure 8 must be used as sensed information. Software can be created in which the microprocessor will examine the waveform from the optocoupler at specific intervals to determine if ac is present or absent at the input to the HCPL-3700. This technique eliminates the problem of filtering, and accompanying delays, but requires more sohpisticated software implementation in the microprocessor.

Input Filtering for AC Operation

A convenient method by which to achieve a continuous output low state in the presence of the applied ac signal is to filter the input dc terminals (pins 2–3) with a capacitance C while the ac signal is applied to the ac input (pins 1–4) of the full wave rectifier bridge. Input filtering allows flexibility in using the HCPL-3700 output for direct interfacing with TTL or CMOS devices without the slow rise time which would be encountered with output filtering. In addition, the input filter capacitor provides extra transient and contact bounce filtering. Because filtering is done after R_x, the capacitor working voltage is limited by the V_{IHC2} clamp voltage rating which is 6.7V peak for ac operation. The disadvantage of input filtering is that this technique introduces time delays at turn on and turn off of the optocoupler due to initial charge/discharge of the input filter capacitor.

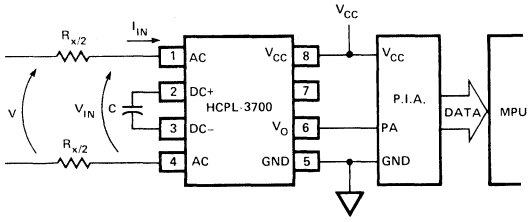


Figure 10. Input Filtering with the HCPL-3700

The application of ac input filtering is illustrated in Figure 10 and is described in the following example. The ac input conditions are the same as in the previous example of the 115V ac limit switch.

The minimum value of capacitance C to ensure proper ac filtering is determined by the parameters of the optocoupler. At low ac input voltage, the capacitor must charge to at least V_{TH+} in order to turn on, but must not discharge to V_{TH-} during the discharge cycle. A conservative estimate for the minimum value of C is given by the following equations.

$$V_{TH+} - V_{TH-} = V_{TH+}e^{-t/\tau}, \ \tau = R_{IN}C_{min} \qquad (12)$$

where R_{IN} is the equivalent input resistance of the HCPL-3700.

$$C_{min} = \frac{t}{R_{IN} \ln\left(\frac{V_{TH+}}{V_{TH+} - V_{TH-}}\right)} \qquad (13)$$

with R_{IN} = 1kΩ, V_{TH+} = 3.8V, V_{TH-} = 2.6V and t = 8.33ms for 60 Hz or t = 10ms for 50 Hz.

C_{min} = **7.23μF for 60 Hz**

C_{min} = **8.68μF for 50 Hz**

To ensure proper filtering, the recommended value of C should be large enough such that with the tolerance variation, C will always be greater than C_{min} (C should otherwise be kept as small as possible to minimize the inherent delay times which are encountered with this technique). Since the filter capacitor affects the input impedance, a slightly different value of R_x is required for the input filtered condition. Figure 11 shows the R_x versus $V_\pm$ threshold voltage for C = 10μF, 22μF, and 47μF. For an application of monitoring a 115V RMS line for 65% of nominal voltage condition (75V RMS), an R_x = 26.7kΩ ± 1% with C = 10μF will yield the desired threshold. The power dissipation for R_x is determined from the clamped

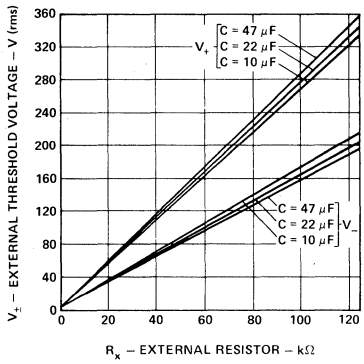


Figure 11. External Threshold Voltage versus R_X for Applications Using an Input Filter Capacitor C (Figure 10)

condition ($V_+/V_{peak} < V_{TH+}/V_{ICH2}$) and is 455mW (see Figure 6) which suggests $R_X/2$ of 1/2 watt resistors for each input lead.

Example 3. AC Operation with Improved Threshold Control and Accuracy

Some applications may occur which require threshold level detection at specific upper and lower threshold points. The ability to independently set the upper and lower threshold levels will provide the designer with more flexibility to meet special design criteria. As illustrated in Figure 12, a computer power line is monitored for a power failure condition in order to prevent loss of memory information during power line failure.

In this design, the HCPL-3700 optocoupler monitors the computer power line and the output of the optocoupler is interfaced to a TTL Schmitt trigger gate (7414).

In the earlier ac application of the HCPL-3700 (limit switch example), a single external series resistor, R_X, was used to determine one of the threshold levels. The other threshold level was determined by the hysteresis of the device, and not the designer. A potential problem of single threshold

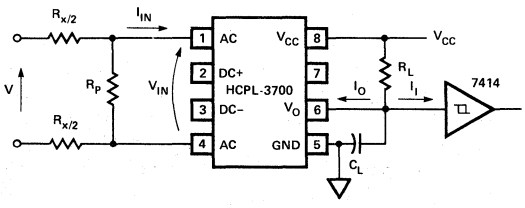


Figure 12. An AC Power Line Monitor with Simultaneous Selection of Upper and Lower Threshold Levels and Output Filtering

selection with 115V line application would be to determine R_X for a lower threshold level of 50% of nominal peak input voltage, only to find that the upper threshold level is 90% of peak input voltage. With the possible ac line voltage variations (+10%, −15%), it would be possible that the optocoupler could never reach the upper threshold point with an ac line that is at −15% of nominal value. To give the designer more control over both threshold points, a combination of series resistance, R_X, and parallel resistance, R_P, may be used, as shown in Figure 12.

Two equations can be written for the two external threshold level conditions. At the upper threshold point,

$$V_+ = R_X\left(I_{TH+} + \frac{V_{TH+}}{R_P}\right) + V_{TH+} \qquad (14)$$

and at the lower threshold point,

$$V_- = R_X\left(I_{TH-} + \frac{V_{TH-}}{R_P}\right) + V_{TH-} \qquad (15)$$

Solving these equations for R_X and R_P yield the following expressions:

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \qquad (16)$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \qquad (17)$$

Equations (16) and (17) are valid only if the conditions of Equations (18) or (19) are met. The desired external voltage threshold levels, V_+ and V_-, are established and the values for $V_{TH\pm}$ and $I_{TH\pm}$ are found from the data sheet. With the $V_{TH\pm}$, $I_{TH\pm}$ values, the denominator of R_X, Equation (16) is checked to see of it is positive or negative. If it is positive, then the following ratios must be met:

$$\frac{V_+}{V_-} \geqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}} \qquad (18)$$

Conversely, if the denominator of R_X Equation (16) is negative, then the following ratios must hold:

$$\frac{V_+}{V_-} \leqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}} \qquad (19)$$

Consider that the computer power line is monitored for a 50% line drop condition and a 75% line presence condition. The 115V 60 Hz ac line (163V peak) can vary from 85% (139V) to 110% (179V) of nominal value.

Require:

V_- = 81.5V (50%) – Turn off threshold

V_+ = 122.5V (75%) – Turn on threshold

Given:

V_{TH+} = 5.1V I_{TH+} = 2.5mA V_{IHC2} = 6.7V

V_{TH-} = 3.8V I_{TH-} = 1.3mA

Using the Equations (16, 17) for R_X, R_P with the conditions of Equations (18, 19) being met yields

R_X = 17.4 kΩ use 18 kΩ 5%

R_P = 1.2 kΩ use 1.2 kΩ 5%

To complete the input calculations for maximum input current, I_{IN}, to the device and maximum power dissipation in R_X and R_P, a check must be made to determine if the input voltage will clamp at peak applied voltage. Using Equations (3) and (4) to determine if a clamp or no clamp exists, it is found that the ratios

$$0.75 = \frac{V_+}{V_{peak}} \approx \frac{V_{TH+}}{V_{IHC2}} = 0.76$$

indicate that V_{IN} slightly entered clamp condition. In this application, the operating input current, I_{IN}, is given approximately by

$$I_{IN} = \frac{V - \frac{V_{IHC2}}{\sqrt{2}}}{R_X} - \frac{\frac{V_{IHC2}}{\sqrt{2}}}{R_P} < I_{IN\,(max)} \qquad (20)$$

$$= \frac{115V - \frac{6.7V}{\sqrt{2}}}{18\,k\Omega} - \frac{\frac{6.7V}{\sqrt{2}}}{1.2\,k\Omega}$$

I_{IN} = 2.18mA RMS < 34.3mA

Power dissipation in R_X is determined from the following equation,

$$P_{R_X} = \frac{\left(V - \frac{V_{IHC2}}{\sqrt{2}}\right)^2}{R_X} \qquad (21)$$

which yields 0.675W. With the clamp condition existing, the maximum power dissipation for R_P is 18.7mW which is determined from

$$P_{R_P} = \frac{\left(\frac{V_{IHC2}}{\sqrt{2}}\right)^2}{R_P} \qquad (22)$$

Output Filtering

The advantages of filtering at the output of the HCPL-3700 are that it is a simple method to implement. The output waveform introduces only one additional delay time at turn off condition as opposed to the input filtering method which introduces additional delay times at both the turn on and turn off conditions due to initial charge or discharge of the input filter capacitor. The disadvantage of output filtering is that the long transition time, t_r, which is introduced by the output RC filter requires a Schmitt trigger logic gate to buffer the output filter circuit from the subsequent logic circuits to prevent logic chatter problems. The determination of load resistance and capacitance is illustrated in the following text.

The following given values specify the interface conditions.

HCPL-3700

V_{OL} = 0.4V

I_{OL} = 4.2mA

I_{OH} = 100μA max

V_{CC} = 5.0V ± 5%

7414

$V_{T+\,(min)}$ = 1.5V } Schmitt trigger upper

$V_{T+\,(max)}$ = 2.0V } threshold level

I_{IH} = 40μA max

I_{IL} = –1.2mA max

With the current convention shown in Figure 12, the minimum value of R_L which ensures that the output transistor remains in saturation is:

$$R_{L\,(min)} \geq \frac{V_{CC\,(max)} - V_{OL}}{I_{OL} + I_{IL}} \qquad (23)$$

$$= \frac{5.25V - 0.4V}{4.2mA - 1.2mA} = 1.62\,k\Omega$$

The maximum value for R_L is calculated allowing for a guardband of 0.4V in $V_{T+\,(max)}$ parameter, or $V_{IH} = V_{T+\,(max)} + 0.4V$.

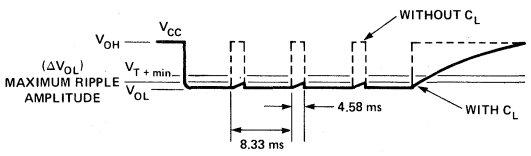


Figure 13. Output Waveforms of the HCPL-3700

$$R_{L\,(max)} \leq \frac{V_{CC\,(min)} - V_{IH}}{I_{OH} - I_{IH}} \qquad (24)$$

$$= \frac{4.75V - 2.4V}{0.1mA + 0.04mA} = 16.8\ k\Omega$$

R_L is chosen to be 1650Ω.

C_L can be determined in the following fashion. As illustrated in Figure 8, the output of the optocoupler will be in the high state for a specific amount of time dependent upon the selected V_+ levels. In this example, $V_+ = 122.5V$ (75%) and $V_- = 81.5V$ (50%) and allowing for a minimum peak line voltage of 138V (−15%), the high state time (without C_L) is from Equation (11), 4.58ms. With the appropriate C_L value, the output waveform (solid line) shown in Figure 13 is filtered.

The maximum ripple amplitude above V_{OL} is chosen to be 0.6V; that is, $V_{OL} + \Delta V_{OL} = 1.0V$. This gives a 0.5V noise margin before $V_{T+\,(min)} = 1.5V$ is reached. The exponential ripple waveform is caused by the C_L being charged through R_L and input resistance, $R_{IN_{TTL}}$, of TTL gate. An expression for the allowable change in V_{OL} can be written:

$$\Delta V_{OL} = (V_{OH} - V_{OL})\,(1 - e^{-t/\tau}) \qquad (25)$$

where $\tau = R'_L C_L$ with R'_L equal to parallel combination of R_L and $R_{IN_{TTL}}$.

Below $V_{T+} = 1.5V$ (min), $R_{IN_{TTL}}$ is constant and nominally 6 kΩ. Hence:

$$R'_L = \frac{R_L\,R_{IN_{TTL}}}{R_L + R_{IN}} \qquad (26)$$

$$= \frac{(1.65\ k\Omega)\,(6\ k\Omega)}{1.65\ k\Omega + 6\ k\Omega}$$

$$R'_L = 1.29\ k\Omega$$

Solving Equation (25) for τ yields

$$\tau = \frac{t}{\ln\left(\frac{V_{OH} - V_{OL}}{V_{OH} - V_{OL} - \Delta V_{OL}}\right)} \qquad (27)$$

and substituting previous parameter values and using $V_{OH} = V_{CC} - (I_{OH} + I_{IH})\,R_L$ results in

$$= \frac{4.58ms}{\ln\left(\frac{4.8V - 0.4V}{4.8V - 0.4V - 0.6V}\right)}$$

$$\tau = 31.24ms$$

C_L can be calculated directly,

$$C_L = \frac{\tau}{R'_L} \qquad (28)$$

$$= \frac{31.24ms}{1.29\ k\Omega}$$

$C_L = 24.2\mu F$ use $27\mu F \pm 10\%$

or $33\mu F \pm 20\%$

With this value of C_L, the time the $R'_L C_L$ filter network takes to reach V_{T+} of the TTL gate is found as follows.

$$V_{OL} + (V_{OH} - V_{OL})\,(1 - e^{-t/\tau}) = V_{T+} \qquad (29)$$

Solving for t,

$$t = \tau \ln\left(\frac{V_{OH} - V_{OL}}{V_{OH} - V_{T+\,(min)}}\right) \qquad (30)$$

and substituting $V_{OH} = 4.8V$, $V_{OL} = 0.4V$, $V_{T+\,(min)} = 1.5V$, and $\tau = 31.24ms$ yields

$$t = 9.0ms$$

This is the delay time that the system takes to respond to the ac line voltage going below the 50% (V_-) threshold level. In essence, the response time is slightly more than a half cycle (8.33ms) of 60 Hz ac line with worst case line variation taken into account. This delay time is acceptable for system power line protection. In this example, a complete worst case analysis was not performed. A worst case analysis should be done to ensure proper function of the circuit over variations in line voltage, unit to unit device parameter variations, component tolerances and temperature.

Threshold Accuracy Improvement

In the above example on output filtering, the two external threshold levels were selected for turn on conditions at V_+ = 122.5V (75%) and turn off at V_- = 81.5V (50%). The calculated external resistor values were R_X = 17.4 kΩ and R_P = 1.2 kΩ. Using standard 5% resistors of 18 kΩ and 1.2 kΩ respectively, the upper threshold voltage was actually 126.6V nominal.

Examination of the worst possible combination of variations of the HCPL-3700 optocoupler V_{TH+}, I_{TH+}, levels from unit to unit, and the ± 5% variations of R_X and R_P can result in the V_+ level changing +23% to −25% from design nominal.

If higher threshold accuracy is desired, it can be accomplished by decreasing the value of R_P in order to allow R_P to dominate the input resistance variations of the optocoupler. Using a 1% resistor for R_P and resistance of sufficiently small magnitude, the V_+ tolerance variations can be significantly improved. The following analysis will allow the designer to obtain nearly optimum threshold accuracy from unit to unit. It should be noted that the HCPL-3700 demonstrates excellent threshold repeatability once the external resistors are adjusted for a particular level and unit. The compromise which is made for the added control on threshold accuracy is that more input power must be consumed within the R_P, R_X resistors.

In Figure 14, assume the circuit is at the upper threshold point. At constant V_{TH+}, it is desired to maintain I_+ to within ± 5% variation of nominal value while allowing ± 1% variation in I_{P+}. With this requirement, Equations (31) and (32) can be written and solved for the magnitude of I_{P+} which is needed to maintain the desired condition on I_+. I_+ is the sum of I_{P+} and I_{TH+}.

$$1.05\, I_+ = 1.01\, I_{P+} + I_{TH+\,(max)} \quad (31)$$

$$0.95\, I_+ = 0.99\, I_{P+} + I_{TH+\,(min)} \quad (32)$$

} at constant V_{TH+}

where

$$I_{TH+\,(max)} = 3.11mA$$

$$I_{TH+\,(min)} = 1.96mA$$

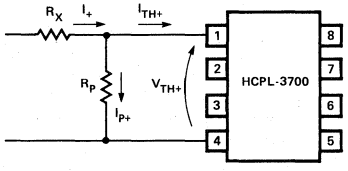


Figure 14. Threshold Accuracy Improvement through the Use of External R_X and R_P Resistors

Solving for I_{P+} yields

$$I_{P+} = 11.2mA,$$

and

$$R_P = \frac{V_{TH+}}{I_{P+}} \quad (33)$$

$$= \frac{5.1V}{11.2mA}$$

$$R_P = 433\Omega \qquad \textbf{(use 453Ω, 1% resistor)}$$

This new value of R_P replaces the earlier R_P = 1.2 kΩ, and the circuit requires a new R_X value to maintain the same V_+ threshold level.

$$R_X = \frac{V_+ - V_{TH+}}{I_+} \quad \text{where } I_+ = I_{P+} + I_{TH+} \quad (34)$$

$$= 11.2mA + 2.5mA$$

$$= \frac{122.5V - 5.1V}{13.7mA}$$

$$R_X = 8.57\ k\Omega \qquad \textbf{(use 8.66 kΩ, 1% resistor)}$$

With the possible variation of ± 1% in R_P and R_X, as well as unit to unit variations in the optocoupler V_{TH+}, I_{TH+}, the upper threshold level V_+ will vary significantly less than in the 5% resistor design case. The variations in V_+, which is given by $V_+ = R_X I_+ + V_{TH+}$, where $I_+ = I_{P+} + I_{TH+}$, are compared in Table 1.

Table 1 illustrates the possible improvements in V_+ tolerance as R_X and R_P are adjusted to limit the variation of the external input threshold current, I_+, to the resistor network and optocoupler. This table is centered at a nominal external input threshold voltage of V_+ = 122.5V. It is the designer's compromise to keep power consumption low, but threshold accuracy high.

NOTE: The above method for selection of R_P and R_X can be adapted for applications where larger sense currents (wet sensing) may be appropriate.

Example 4. Dedicated Lines for Remote Control

In situations involving a substantial separation between the signal source and the receiving station, it may be desirable to lease a dedicated private line metallic circuit (dc path) for supervisory control of remote equipment. The HCPL-3700 can provide the interface requirements of voltage threshold detection and optical isolation from the metallic line to the remote equipment. This greatly reduces the expense of using a sophisticated modem system over a convention telephone line.

R_x	T O L.	R_P	T O L.	I_+ TOLERANCE	V_+ TOLERANCE		MAXIMUM TOTAL POWER IN $R_x + R_P$ (RMS)
18 kΩ	5%	1.2 kΩ	5%	+17.5% −21.2%	+ 23%	− 25%	0.69 W
8.66 kΩ	1%	453Ω	1%	±5%	+12.7%	−19.3%	1.45 W
4.32 kΩ	1%	205Ω	1%	±3%	+11.2%	−18.9%	2.92 W
2.15 kΩ	1%	97.5Ω	1%	±2%	+10.6%	−18.8%	5.89 W

Table 1. Comparison of the V_+ Threshold Accuracy Improvement versus R_x and R_p and Power Dissipation for a Nominal V_+ = 122.5 V

Figure 15 represents the application of the HCPL-3700 for a line which is to control tank levels in a water district.

Some comments are needed about dedicated metallic lines. The use of a private metallic line places restrictions upon the designer's signal levels. The line in this example would be used in the interrupted dc mode (duration of each interruption greater than one second), the maximum allowed voltage between any conductor and ground is ≤ 135 volts. Maximum current should be limited to 150mA if the cable has compensating inductive coils in it. Balanced operation of the line is strongly recommended to reduce possible cross talk interference as well as to allow larger signal magnitudes to be used. Precaution also should be taken to protect the line and equipment. The line needs to be fused to ensure against equipment failure causing excessive current to flow through telephone company equipment. In addition, protection from damaging transients must be taken via spark gap arrestors and commercial transient suppressors. Details of private line metallic circuits can be founded in the American Telephone and Telegraph Company publication 43401.

In this application, a 48V dc floating power source supplies the signal for the metallic line. The HCPL-3700 upper voltage threshold level is set for V_+ = 36V (75%). Consequently, R_x is

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (35)$$

$$= \frac{36V - 3.8V}{2.5mA}$$

$$= 12.9\ k\Omega \quad \textbf{(use } R_x/2 = 6.49\ k\Omega, 1\% \textbf{ resistor in each input level)}$$

The resulting lower voltage threshold level is

$$V_- = R_x I_{TH-} + V_{TH-} \quad (36)$$

$$= 13\ k\Omega\ (1.3mA) + 2.6V$$

$$V_- = 19.5V$$

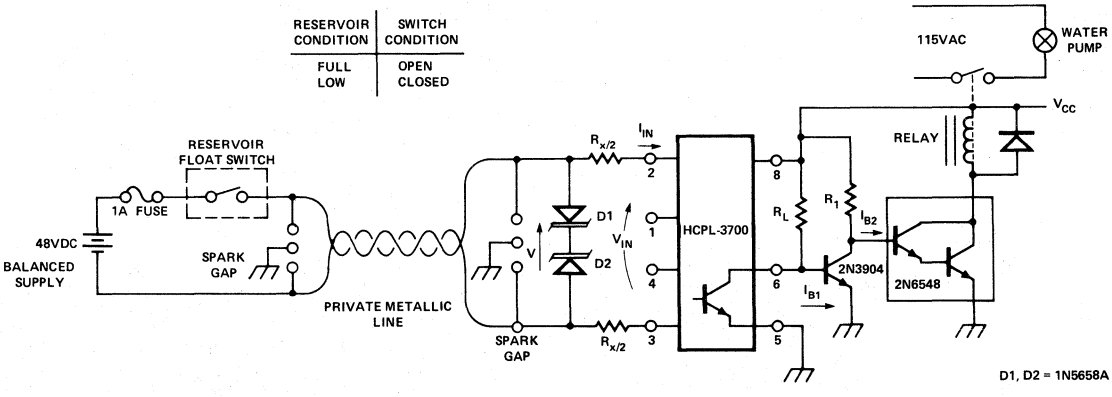


Figure 15. Application of the HCPL-3700 to Private Metallic Telephone Circuits for Remote Control

yielding V_{HYS} = 16.5V. The average induced ac voltage from adjacent power lines is usually less than 10 volts (reference ATT publication 43401) which would not falsely turn on, or off, the HCPL-3700, but could affect conventional optocouplers.

Under normal operation (full reservoir), the optocoupler is off. When the float switch is closed (low reservoir), the optocoupler output (V_{OL}) needs inversion, via a transistor, to drive the power Darlington transistor which controls a motor starting relay. The relay applies ac power to the system water pump. With V_{CC} = 10V, I_{B2} = 0.5mA, I_{B1} = 0.5mA.

$$R_1 = \frac{V_{CC} - 2V_{BE}}{I_{B2}} \quad (37)$$

$$= \frac{10V - 1.4V}{0.5mA}$$

$$R_1 = 17.2\ k\Omega$$

$$(R_1 = 18\ k\Omega)$$

$$R_L = \frac{V_{CC} - V_{BE}}{I_{B1}} \quad (38)$$

$$= \frac{10V - 0.7V}{0.5mA}$$

$$R_L = 18.6\ k\Omega$$

$$(R_L = 18\ k\Omega)$$

For this application, the ac inputs could also be used, which would remove any concern about the polarity of the input signal.

General Protection Considerations for the HCPL-3700

The HCPL-3700 optocoupler combines a unique function of threshold level detection and optical isolation for interfacing sensed signals from electrically noisy, and potentially harmful, environments. Protection from transients which could damage the threshold detection circuit and LED is provided internally by the Zener diode bridge rectifier and an external series resistor. By examination of Figure 1, it is seen that an input ac voltage clamp condition will occur at a maximum of a Zener diode voltage plus a forward biased diode voltage.

At clamp condition, the bridge diodes limit the applied input voltage at the device and shunt excess input current which could damage the threshold detection circuit or cause excessive stress to the LED.

The HCPL-3700 optocoupler can tolerate significant input current transient conditions. The maximum dc input current into or out of any lead is 50mA. The maximum input surge current is 140mA for 3ms at 120 Hz pulse repetition rate, and the maximum input transient current is 500mA for 10μs at 120 Hz pulse repetition rate. The use of an external series resistor, R_X, provides current limiting to the device when a large voltage transient is present. The amplitude of the acceptable voltage transient is directly proportional to the value of R_X.

However, in order to protect the HCPL-3700 when the input voltage to the device is clamped, the maximum input current must not be exceeded. An external means by which to enhance transient protection can be seen in Figure 16.

A transient R_XC_P filter can be formed with C_P chosen by the designer to provide a sufficiently low break point for the low pass filter to reduce high frequency transients. However, the break point must not be so low as to attenuate the signal frequency. Consider the previous ac application where no filtering was used. In that application, R_X = 37.4 kΩ, and if the bandwidth of the transient filter needs to be 600 Hz, then C_P is:

$$C_P = \frac{1}{2\pi f R_X} \quad (39)$$

$$C_P = 0.0071\mu F \quad \textbf{(use 0.0068}\mu\textbf{F capacitor @ 50V dc)}$$

Should additional protection be needed, a very effective external transient suppression technique is to use a commercial transient suppressor, such as a Transzorb ®, or metal oxide varistor, MOV ®, at the input to the resistor network prior to the optocoupler. The Transzorb ® will provide extremely fast transient response, clamp the input voltage to a definite level, and absorb the transient energy. Selection of a Transzorb ® is made by ensuring that the reverse stand off voltage is greater than the continuous peak operating voltage level. Transzorbs ® can be stacked in series or parallel for higher peak power ratings. Depending upon the designer's potential transient problems, a solution may warrent the expense of a commercial suppression device.

Thermal Considerations

Thermal considerations which should be observed with the HCPL-3700 are few. The plastic 8 pin DIP package is designed to be operated over a temperature range of –25°C to 85°C. The absolute maximum ratings are established for

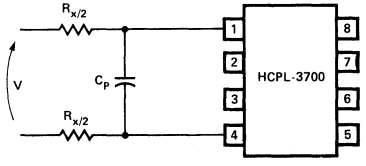


Figure 16. R_XC_P Transient Filter for the HCPL-3700

a 70°C ambient temperature requiring slight derating to 85°C. In general, if operation of the HCPL-3700 is at ambient temperature of 70°C or less, no heat sinking is required. However, for operation between 70°C and 85°C ambient temperature, the maximum ratings should be derated per the data sheet specifications.

Mechanical and Safety Considerations

Mechanical Mounting Considerations

The HCPL-3700 optocoupler is a standard 8 pin dual-in-line plastic package designed to interface ac or dc power systems to logic systems. This optocoupler can be mounted directly onto a printed circuit board by wave soldering.

Electrical Safety Considerations

Special considerations must be given for printed circuit board lead spacing for different safety agency requirements. Various standards exist with safety agencies (U.L., V.D.E., I.E.C., etc.) and should be checked prior to PC board layout. The HCPL-3700 optocoupler component is recognized under the Component Program of Underwriters Laboratories, Inc. in file number E55361. This file qualifies the component to specific electrical tests to 220V ac operation.

The spacing required for the PC board leads depends upon the potential difference that would be observed on the board. Some standards that could pertain to equipment which would use the HCPL-3700 are UL1244, Electrical and Electronic Measuring and Testing Equipment, UL1092, Process Control Equipment, and IEC348, Electronic Measuring Apparatus. Spacing for the worst case in an uncontrolled environment with a 2000 volt-amperes maximum supplying source rating must be 3.2mm (0.125 inches) for 51 – 250 volts RMS potential difference over a surface (creepage distance), and 3mm (0.118 inches) through air (bare wire). These separations are between any uninsulated live part and uninsulated live part of opposite polarity, or uninsulated ground part other than the enclosure or an exposed metal part.

An uncontrolled environment is an environment which has contaminants, chemical vapors, particulates or any substances which would cause corrosion, decrease resistance between PC board traces or, in general, be an unhealthy environment to human beings.

For 0 – 50 volts RMS, the spacing is 1.6mm (0.063 inches) through air or over surfaces.

Electrical Connectors

The HCPL-3700 provides the needed isolation between a power signal environment and a control logic system. However, there exists a physical requirement to actually interconnect these two environments. This interconnection can be accomplished with barrier strips, edge card connectors, and PCB socket connectors which provide the electrical cable/field wire connection to the I/O logic system. These connectors provide for easy removal of the PC board for repair or substitution of boards in the I/O housing and are needed to satisfy the safety agency (U.L., V.D.E., I.E.C.) requirements for spacing and insulation. Connectors are readily available from many commercial manufacturers, such as Connection Inc., Buchanan, etc. The style of connector to choose is dependent upon the application for which the PC board is used. If possible it is wise to choose a style which does not mount to the PC board. This would enable the PC card to be removed without having to disconnect field wires. The use of connectors which are called "gas tight connectors" provide for good electrical and mechanical reliability by reducing corrosion effects over time.

APPENDIX I. List of Parameters

V ≡ Externally Applied Voltage
V_+ ≡ External Upper Threshold Voltage Level
V_- ≡ External Lower Threshold Voltage Level
V_{IHC1} = Device* Input Voltage Clamp Level; Low Voltage DC Case
V_{IHC2} = Low Voltage AC Case
V_{IHC3} = High Voltage DC Case
I_{IN} = Device Input Current
V_{IN} = Device Input Voltage
V_{TH+} = Device Upper Voltage Threshold Level
V_{TH-} = Device Lower Voltage Threshold Level
I_{TH+} = Device Upper Input Current Threshold Level
I_{TH-} = Device Lower Input Current Threshold Level
R_x = External Series Resistor for Selection of External Threshold Level
R_P = External Parallel Resistor for Simultaneous Selection/Accuracy Improvement of External Threshold Voltage Levels
I_+ = Total Input Current at Upper Threshold Level to External Resistor Network (R_x, R_P) and Device
I_{P+} = Current in R_P at Upper Threshold Levels
V_{peak} = Peak Externally Applied Voltage
V_O = Output Voltage of Device
V_{OL} = Output Low Voltage of Device
V_{OH} = Output High Voltage of Device
I_{OH} = Output High Leakage Current of Device
I_{OL} = Output Low Sinking Current of Device
I_{IH} = Input High Current of Driven Gate
I_{IL} = Input Low current of Driven Gate
V_{CC} = Positive Supply Voltage
R_{IN} = Input Resistance of HCPL-3700
V_{T+} ≡ Schmitt Trigger Upper Threshold Voltage of TTL Gate (7414)
R_L = Output Pullup Resistance
C_L = Output Filter Capacitance
C = Input Filter Capacitor
TH_+ = Upper Threshold Level
TH_- = Lower Threshold Level
PR_x = Power Dissipation in R_x
P_{IN} = Power Dissipation in HCPL-3700 Input IC
PA = Input Signal Port to P.I.A.
t_+ = Turn On Time
t_- = Turn Off Time
T = Period of Waveform
C_P = Similar to R_P

*Device = HCPL-3700

HEWLETT PACKARD

APPLICATION NOTE 1005

Operational Considerations for LED Lamps and Display Devices

In the design of a display system, which incorporates LED lamps and display devices, the objective is to achieve an optimum between light output, power dissipation, reliability, and operating life. The performance characteristics and capabilities of each LED device must be known and understood so that an optimum design can be achieved. The primary source for this information is the LED device data sheet.

The data sheet typically contains Electrical/Optical Characteristics that list the performance of the device and Absolute Maximum Ratings in conjunction with characteristic curves and other data which describe the capabilities of the device. A thorough understanding of this information and its intended use provides the basis for achieving an optimum design.

This application note presents an in-depth discussion of the theory and use of the electrical and optical information contained within a data sheet. Two designs using this information in the form of numerical examples are presented, one for dc operation and one for pulsed (strobed) operation. The calculated results for each example are underlined and accented by an arrow (←) for each identification. Specific information on operation without derating and the soldering of plastic LED devices is also presented.

Typical Data Sheet Information

A data sheet typically contains Absolute Maximum Ratings, Electrical/Optical Characteristics, and typical operating graphs. The Absolute Maximum Ratings list such items as the maximum allowed forward currents, power dissipation, and operating ambient temperature range. The Electrical/Optical Characteristics list such data as the luminous intensity specification (I_V), forward voltage (V_F), peak wavelength (λ_{PEAK}), dominant wavelength (λ_d), and the device thermal resistance LED junction-to-pin on a per LED element basis ($R\theta_{J-PIN}$).

The five graphs that are usually contained within a data sheet are:

Figure 1: Pulsed Mode Operating Curves
Figure 2: Current Derating vs. Temperature
Figure 3: Relative Luminous Efficiency
Figure 4: Forward Voltage Characteristic
Figure 5: Light Output vs. DC Drive Current

The data sheet also provides an equation to calculate the expected maximum forward voltage at a given current.

Design Criteria

This application note assumes that the objective of a specific design is to achieve a maximum light output from a display that is operated in an elevated ambient temperature. The two criteria that establish the operating limits are the maximum drive current and the maximum LED junction temperature. The maximum drive current has been established to ensure a long operating life and the maximum LED junction temperature is governed by the device package. The data sheet will list the maximum allowed drive currents for a specific device. The absolute maximum allowed LED junction temperature (T_J MAX) differs for the various device package configurations. For most plastic display devices, T_J MAX = 100° C; for most plastic lamps, T_J MAX = 110° C; and for alphanumeric PC board monolithic displays, T_J MAX = 110° C (for some PC board monolithic displays, T_J MAX = 80° C).

Thermal Resistance

The LED junction temperature is the sum of the ambient temperature (T_A) and the temperature rise above ambient (ΔT_J), which is the product of the power dissipated within the junction (P_D) times the thermal resistance LED junction-to-ambient ($R\theta_{JA}$).

$$T_J\ (°C) = T_A + \Delta T_J \qquad (1)$$
$$T_J\ (°C) = T_A + P_D\ R\theta_{JA}$$

The cathode pins of an LED device are the primary thermal paths for heat dissipation from the LED junction into the surrounding environment. The data sheet lists the thermal resistance LED junction-to-pin ($R\theta_{J-PIN}$) for the device. This device junction-to-pin thermal resistance is added to the thermal resistance-to-ambient of the PC board mounting assembly ($R\theta_{PC-A}$) to obtain the overall value of $R\theta_{JA}$ on a per LED element basis. (NOTE: For monolithic displays, thermal resistance is calculated on a per digit basis.)

$$R\theta_{JA} = R\theta_{J-PIN} + R\theta_{PC-A} \qquad (2)$$
$$= °C/W/LED\ Element$$

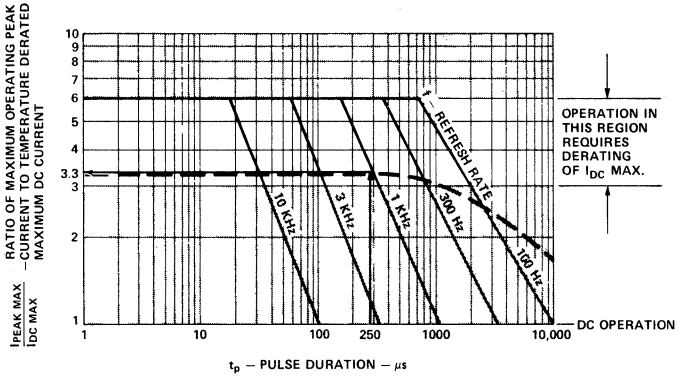


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

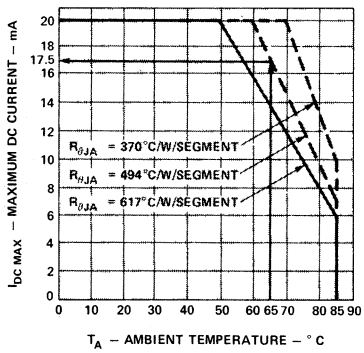


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. $T_J MAX = 100°C$

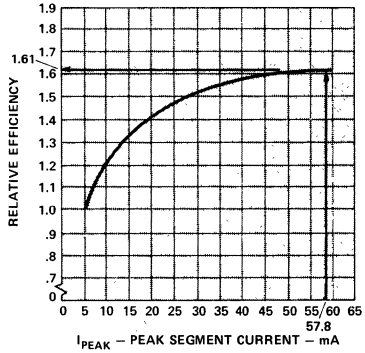


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

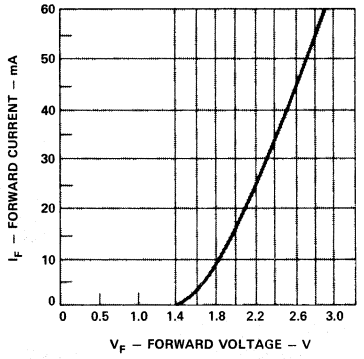


Figure 4. Forward Current vs. Forward Voltage Characteristic

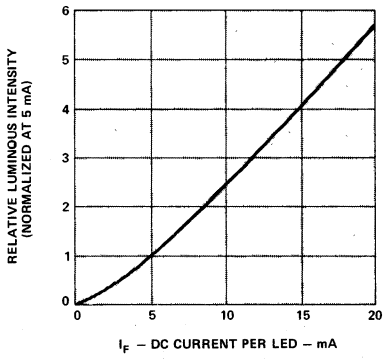


Figure 5. Relative Luminous Intensity vs. DC Forward Current

APPLICATION NOTES

For reliable operation, it is recommended that the value of $R\theta_{PC-A}$ be designed low enough to ensure that the LED junction temperature does not exceed the maximum allowed value.

Derating vs. Temperature

The derating vs. temperature, Figure 2, is derived from the LED junction temperature rise above ambient as estab- by the maximum allowed power dissipation (P_D MAX) which is derated linearly to zero power when $T_A = T_J$ MAX. The values of $R\theta_{JA}$ shown on Figure 2 are derived from the quotient of ΔT_J and P_D MAX for a specified operating temperature.

$R\phi_{JA}$ (°C/W/LED) = (3)

$$\frac{\Delta T_J\ (°C)}{P_D\ MAX\ (W)} = \frac{T_J\ MAX - T_A\ OPERATING}{P_D\ MAX}$$

The value of P_D MAX is the power dissipation within a maximum forward voltage device when driven at the maximum data sheet current. Thus, $R\theta_{JA}$ is determined on the basis of worst case power dissipation.

The derating curve with the largest $R\theta_{JA}$ value in Figure 2, normally a derating from $T_A = 50°C$, represents a mandatory derating for a typical application that utilizes a single sided PC board with 0.51mm (0.020 inch) wide traces, assuming that no other provision is provided for heat dissipation. The other derating curves from higher ambient temperatures, shown as dashed lines on Figure 2, represent allowed increased drive currents when the design incorporates a more elaborate PC board mounting assembly to obtain a lower $R\theta_{JA}$ value for increased heat dissipation. The temperature deratings of Figure 2 ensure reliable operation for both dc and pulsed mode operation.

Worst Case Power Calculation

The worst case power is that power dissipated within the junction of a maximum forward voltage device. The worst case power is used for determining the worst case T_J that will result from a specific drive current and thermal resistance, see Equation 1. The expected maximum forward voltage (V_F MAX) at a selected drive current is determined by an equation on the data sheet of the form:

$V_F MAX = V_{ON} + (I_{PEAK})$(LED Dynamic Resistance) (4)

The worst case power is the product of the time average current under pulsed operation (dc current for dc operation) times V_F MAX:

$P_{WORST\ CASE} = (I_{DC})(V_F\ MAX)$; For DC Operation (5)

$P_{WORST\ CASE} = (I_{PEAK})$(DUTY FACTOR)($V_F$ MAX at I_{PEAK}); For Pulsed Operation

Current Limiting

An LED is a current operated device and some kind of current limiter must be incorporated as part of the drive circuitry. This current limiter usually takes the form of a resistor placed in series with the LED. The typical forward voltage characteristic of Figure 4 is used to calculate the series current limiter for each LED element.

$R_{LIMITER}$ = (6)

$$\frac{V_{CC(POWER\ SUPPLY)} - V_{SAT(DRIVE\ TRANSISTORS)} - V_{F(FIGURE\ 4)}}{I_{PEAK\ CURRENT\ PER\ LED\ ELEMENT}}$$

Light Output

The time averaged luminous intensity (I_V) at $T_A = 25°C$ for a particular drive condition may be calculated using the relative luminous intensity characteristic of Figure 5 for dc operation or the relative efficiency characteristic ($\eta_{I_{PEAK}}$) of Figure 3 for pulsed operation. For dc operation, I_V (T_A = 25°C) is equal to the product of the data sheet luminous intensity specification times the relative factor for a specific dc current from Figure 5.

I_V DC = (7)

(I_V DATA SHEET)(FACTOR FROM FIGURE 5)

FOR: $T_A = 25°C$

For pulsed operation, the time averaged luminous at T_A = 25°C is calculated using the following equation:

I_V TIME AVG = (8)

$$\left[\frac{I_{AVG}}{I_{AVG\ DATA\ SHEET}}\right] [\eta_{I_{PEAK}}]\ [I_V\ DATA\ SHEET]$$

Where: I_{AVG} = The average forward current through an LED element

$I_{AVG\ DATA\ SHEET}$ = The average current at which I_V DATA SHEET is measured

The luminous intensity value at $T_A = 25°C$ is adjusted by the following exponential equation to obtain the light output value at the operating ambient temperature.

$$I_V\ (T_A\ OPERATING) = I_V\ (25°C)e^{[k(T_A - 25°C)]} \quad (9)$$

LED	k
Standard Red	−.0188/°C
High Efficiency Red	−.0131/°C
Yellow	−.0112/°C
Green	−.0104/°C

Pulsed Mode vs. DC Operation

When operating an LED device under dc drive conditions, the junction temperature is a linear function of the dc power dissipation multiplied by $R\theta_{JA}$. The light output is proportional to the dc drive current as expressed in Equation 7.

The use of a 50 or 60 Hertz half or full-wave rectified ac as the drive current for LED devices is not recommended, since the rms power in a rectified sine wave is greater than the time averaged power of a rectangular waveform of an equivalent peak value. Pulsed drive conditions are based on the assumption that the drive current pulses are a rectangular waveform. If a rectified sine wave is to be used, in no case should the value of the peak current exceed the maximum allowed dc current value.

When operating an LED device in a pulsed mode, it is the peak junction temperature (not the average) that governs

the performance of the device as to the allowed time average power dissipation and light output. The lower the peak junction temperature (T_J PEAK) is in relationship to the time average junction temperature (T_J AVG), the greater is the light output of the device. At slow refresh rates (the number of times per second a device is pulsed) in the range of 100 Hz, T_J PEAK is greater than T_J AVG. As the refresh rate approaches 1000 Hz, the value of T_J PEAK approaches the value of T_J AVG. Therefore, it is recommended that whenever possible LED devices be refreshed at a 1 KHz rate or faster, since at these faster pulse rates T_J PEAK is assumed to be equal to T_J AVG and the light output is a function of T_J AVG.

Design Steps

In order to determine the derated drive conditions from the data sheet for an elevated ambient temperature, a value for $R\theta_{JA}$ must be selected. Once a value for $R\theta_{JA}$ has been selected, the required current derating can be determined for the operating ambient temperature directly from Figure 2. As illustrated in the pulsed mode design example, the dc derating is used to determine the pulsed current derating.

The four basic design steps are:

1. Determine derated drive currents.
2. Calculate the required value of $R\theta_{PC-A}$ for the PC board mounting configuration.
3. Calculate the value of the current limiting resistor. Use the nearest standard value resistor larger than the calculated value.
4. Calculate the light output.

DC Design Example

A high efficiency red seven segment display is to be operated in an ambient of T_A = 65° C. Pertinent data for this device are:

Maximum DC Current per segment (T_A = 50° C) = 20mA

Maximum Average Power Dissipation (T_A = 50° C) = 81mW

I_V TYPICAL = 300μcd per segment at I_{DC} = 5mA

$R\theta_{J-PIN}$ = 282° C/W/Segment

V_F MAX = 1.60V + I_{DC} (45Ω); for 5mA ≤ I_{DC} ≤ 20mA

T_J MAX = 100° C

The data sheet curves on page 2 apply to this device. It is assumed that a value of $R\theta_{JA}$ = 494° C/W/Segment or less will be incorporated into the display system design.

Step 1.
The derated dc drive current is determined from Figure 2.

At T_A = 65° C and $R\theta_{JA}$ ≤ 494° C/W/Segment,

I_{DC} MAX = 17.5mA ◄——— I_{DC} MAX

Step 2.
The required maximum thermal resistance for the PC board assembly is calculated from Equation 2:

$R\theta_{PC-A} \leq$ (494-282) = 212° C/W/Segment ◄—— $R\theta_{PC-A}$

Step 3.
A value of V_{SAT} = 0.4 volts is assumed for the LED drive transistors. From Figure 4,

V_F TYP (17.5mA) = 2.0V

From Equation 6 and assuming V_{CC} = 5.0V:

$$R_{LIMITER} = \frac{5.0V - 0.4V - 2.0V}{0.0175A} = 149\Omega \leftarrow R_{LIMITER}$$

Use a 150Ω standard value resistor.

Step 4.
From Figure 5, the normalized light at 17.5mA is a factor of 4.4 x the light output at 5mA.

From Equation 7:

I_V (25° C) = (300μcd)(4.4) = 1320 μcd/segment

Using Equation 9 to adjust the light output for T_A = 65° C:

I_V (65° C) = (1320μcd)$e^{[-.0131/°C\ (65-25)°C]}$

I_V (65° C) = (1320)(0.592) = 782μcd/segment ◄——— I_V

Pulsed Mode Design Example

A four digit display using the same high efficiency red seven segment display described in the DC Design Example is to be operated in a pulsed mode in an ambient of T_A = 65° C. Additional pertinent data for this device are:

Maximum Peak Current per Segment

(T_A = 50° C, Pulse Width = 2ms) = 60mA

V_F MAX = 1.75V + I_{PEAK} (38Ω); for I_{PEAK} ≥ 20mA

It is assumed that a value of $R\theta_{JA}$ = 494° C/W/segment or less will be incorporated into the display system design.

Figure 1 is used to select the refresh conditions for pulsed operation. These refresh conditions are junction temperature related to the dc current deratings of Figure 2. Figure 1 relates the ratio of maximum-peak current to temperature derated maximum dc current (I_{PEAK} MAX/I_{DC} MAX) and pulse duration (t_p) as a function of refresh rate (f). The allowed average power dissipation decreases below f = 1kHz since the difference between T_J PEAK and T_J AVG increases with decreasing refresh rates. This condition is illustrated by the dashed line shown on Figure 1, which shows the ratio of I_{PEAK} MAX to I_{DC} MAX decreasing with slower refresh rates with the duty factor fixed at 1 of 4.

Step 1.
For best performance, a refresh rate of 1kHz will be used:

f = 1kHz ◄——— f

A four digit display sets the duty factor (D.F.) at one of four:

D.F. = 1/4 ◄——— D.F.

t_p = (1/f)(D.F.) = (1/1000 Hz)(1/4) = 250μs ◄——— t_p

From Figure 1:
I_{PEAK}/I_{DC} MAX = 3.3; for t_p = 250μs and f = 1kHz

From Figure 2:
I_{DC} MAX, at T_A = 65° C and $R\theta_{JA}$ = 494° C/W/Segment, is 17.5mA

I_{PEAK} = (I_{PEAK} MAX/I_{DC} MAX)(I_{DC} MAX from Figure 2)

I_{PEAK} = (3.3)(17.5mA) = 57.8mA per Segment ◄—— I_{PEAK}

I_{AVG} = (I_{PEAK})(D.F.) = (57.8mA)(1/4) = 14.5mA ◄—— I_{AVG}

These are the maximum pulsed mode drive currents for this design as defined by T_A = 65° C and $R\theta_{JA} \leq$ 494° C/W/segment.

APPLICATION NOTES

Step 2.
The required maximum thermal resistance for the PC board assembly is calculated from Equation 2:

$R\theta_{PC-A} \leq (494-282) =$
$212°C/W/segment \longleftarrow R\theta_{PC-A\ MAX}$

Step 3.
A value of V_{SAT} = 1.2 volts is assumed for the LED drive transistors. From Figure 4,

V_F TYP (57.8mA) = 2.85V

From Equation 6 and assuming V_{CC} = 5.0V:

$$R_{LIMITER} = \frac{5.0V - 1.2V - 2.85V}{0.578A} = 16\Omega \longleftarrow R_{LIMITER}$$

Use a 17Ω standard value resistor.

Step 4.
From Figure 3, the relative efficiency for I_{PEAK} = 57.8mA is:

$\eta_{I_{PEAK}} = 1.61$

From Equation 8:

$$I_V(25°C) = \left[\frac{14.5mA}{5mA}\right][1.61][300\mu cd] =$$

1401μcd per segment

Using Equation 9 to adjust the light output for T_A = 65°C:

$I_V(65°C) = (1401\mu cd)e^{[-.0131/°C\ (65-25)°C]}$

I_V (65°C) = (1401)(0.592) = 829μcd per Segment ← I_V

Operation Without Derating

LED lamp and display devices may be operated in elevated ambient temperature environments without derating only when the PC board mounting configuration is designed for a sufficiently low thermal resistance. The critical criterion is that the LED junction temperature must not exceed the T_J MAX value for the device. This low thermal resistance design will typically include such items as a maximum metallized PC board and possible heat sinking to ensure adequate heat dissipation. In no situation should the absolute maximum current limitations be exceeded.

The necessary thermal resistance requirements for operation without derating are calculated using the value for worst case power dissipation. A numerical example using the LED display device from the above two examples will illustrate the calculation procedure.

Step 1.
Determine the maximum permissible value for $R\theta_{JA}$.

The absolute maximum power dissipation as listed on the data sheet for this particular LED device is 81mW. The operating ambient temperature is to be 65°C.

Referring to Equation 3

$$R\theta_{JA\ MAX} \leq \frac{T_J\ MAX - T_A\ OPERATING}{P_{MAX}\ DATA\ SHEET}$$

For this example:

$$R\theta_{JA\ MAX} \leq \frac{100°C - 65°C}{.081W} = 432°C/W/Segment$$

The required limit on the thermal resistance for the PC board mounting configuration is derived by rewriting Equation 2:

$R\theta_{PC-A\ MAX} \leq R\theta_{JA\ MAX} - R\theta_{J-PIN}$

For this example:

$R\theta_{PC-A} \leq (432-282) = 150°C/W/segment \longleftarrow R\theta_{PC-A\ MAX}$

The particular LED display device used in this example may be operated at maximum power dissipation in an ambient of T_A = 65°C without derating as long as the PC board mounting configuration is designed to have $R\theta_{PC-A} \leq 150°C/W/Segment$.

CAUTION: Since these calculations are based on only T_J AVG and exclude the consideration of T_J PEAK, pulsed operation without derating is only recommended for refresh rates of 1kHz or faster.

Soldering Plastic LED Devices

Because plastic LED devices utilizing a lead frame construction have the LED dice attached directly to the cathode lead, the cathode lead is the direct thermal and mechanical stress path to the LED dice. For this reason, it is necessary to carefully control the solder temperature and dwell time in the solder wave to ensure subsequent reliable operation. LED devices can be effectively wave soldered with a wave temperature of 245°C and a dwell time of 1½ to 2 seconds.

The post solder cleaning process is also crucial to ensuring reliable performance. In order to optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

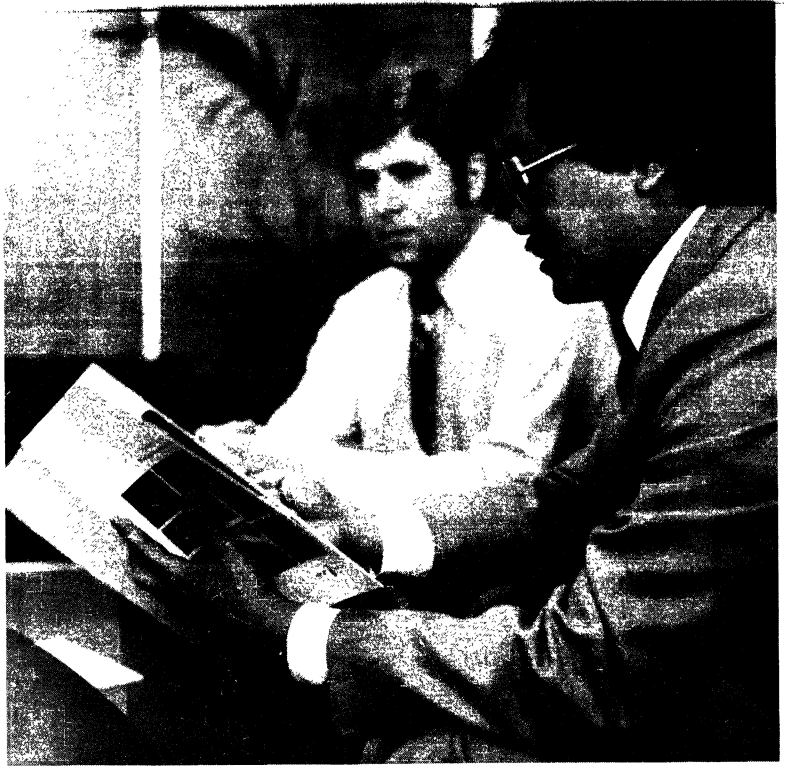
Some LED devices may require special handling during soldering, during post solder cleaning, or may not lend themselves to a wave soldering process. Three specific considerations are:

1. Plastic LED Lamps: The plastic encapsulant that forms the lamp package is the only supporting element for the leads. It is important to prevent stresses from entering the device package which could damage the LED die attach and wire bonds. The leads of a lamp may be bent to a desired angle by observing the following procedure. Firmly grasp the leads at the base of the lamp package with a pair of needle nose pliers to support the lamp while bending the leads. Overheating during soldering will cause melting of the plastic, allowing possible lead movement to occur which may result in the catastrophic failure of the die attach or wire bonds. Care should be taken to ensure that no stresses are applied to the leads during the soldering process. External stresses applied to the leads during soldering could induce strains within the device package that may induce latent failure. Once properly soldered in place, an LED lamp will typically exhibit a very high degree of reliability.

2. PC Board Monolithic Displays: Many PC board monolithic displays do not lend themselves to a wave soldering process. The plastic lens that covers the LED chips and wire bonds is attached to the PC board without forming a seal. The chemicals used in a wave soldering process can collect underneath the lens. The post solder cleaning process may not remove all of the trapped chemicals and prolonged exposure of the LED dice and wirebonds to these chemicals can cause permanent damage. Also, the plastic used to make some of the lenses is susceptible to damage from rosin fluxes and hydrocarbon cleaners. The two recommended installation procedures are either to hand solder flexible cable to the display contacts or use solderless connector pins such as the 022-002 series supplied by JAV Manufacturing, 125 Wilbur Place, Bohemia, NY 11716. Effective room temperature cleaning may be accomplished using Freon TP-35 or TE-35, solvent temperature $\leq 30°C$ and an immersion time ≤ 2 minutes.

3. Silver Lead Frames: Many plastic LED devices utilize a silver plated lead frame. Silver plating provides excellent solderability as long as the leads are kept free from tarnish buildup due to coming in contact with sulfur compounds. Application Bulletin 3 offers specific information on the effective use and soldering of silver lead frame devices.

   It is suggested that the device data sheet be consulted for specific information on wave soldering.



Appendix

- Hewlett-Packard Components Franchised Distributor and Representative Directory
- Hewlett-Packard Sales and Service Offices
- Profile and Inquiry Card

HP Components Franchised Distributor And Representative Directory

March 1980

United States

Alabama

Hall-Mark Electronics
4733 Commercial Drive
Huntsville 35805
(205) 837-8700

Hamilton/Avnet
4692 Commercial Drive
Huntsville 35805
(205) 837-7210

Arizona

Hamilton/Avnet
505 South Madison
Tempe 85281
(602) 894-2594

Wyle Distribution Group
8155 North 24th Avenue
Phoenix 85021
(602) 249-2232
In Tucson (602) 884-7082

California

Hamilton/Avnet
4545 Viewridge Avenue
San Diego 92123
(714) 279-2421

Hamilton/Avnet
1175 Bordeaux Drive
Sunnyvale 94086
(408) 743-3355

Hamilton Electro Sales
3170 Pullman Street
Costa Mesa 92626
(714) 641-4120

Hamilton Electro Sales
10950 Washington Boulevard
Culver City 90230
(213) 558-2121

Schweber Electronics
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San Diego 92123
(714) 565-9171

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Santa Clara 95052
(408) 727-2500

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Denver 80216
(303) 534-1212

Wyle Distribution Group
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Commerce City 80022
(303) 287-9611

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Hamilton/Avnet
643 Danbury Road
Georgetown 06829
(203) 762-0361

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury 06810
(203) 792-3500

Wilshire Electronics
Village Lane
P.O. Box 200
Wallingford 06492
(203) 265-3822

Florida

Hall-Mark Electronics
1302 W. McNab Road
Ft. Lauderdale 33309
(305) 971-9280

Hall-Mark Electronics
7233 Lake Ellenor Drive
Orlando 32809
(305) 855-4020

Hamilton/Avnet
3197 Tech Drive No.
St. Petersburg 33702
(813) 576-3930

Schweber Electronics
2830 N. 28th Terrace
Hollywood 33020
(305) 927-0511

Georgia

Hamilton/Avnet
6700 I-85 Suite IE
Norcross 30071
(404) 448-0800

Schweber Electronics
4126 Pleasantdale Road
Atlanta 30340
(404) 449-9170

Indiana

Pioneer-Standard
6408 Castleplace Drive
Indianapolis 46250
(317) 849-7300

Illinois

Hall-Mark Electronics
1177 Industrial Drive
Bensenville 60106
(312) 860-3800

Hamilton/Avnet
3901 N. 25th Avenue
Schiller Park 60176
(312) 678-6310

Schweber Electronics
1275 Brummel Avenue
Elk Grove Village 60007
(312) 364-3750

Kansas

Hall-Mark Electronics
11870 West 91st Street
Shawnee Mission 66214
(913) 888-4747

Hamilton/Avnet
9219 Quivira Road
Overland Park 66215
(913) 888-8900

Maryland

Hall-Mark Electronics
6655 Amberton Drive
Baltimore 21227
(301) 796-9300

Hamilton/Avnet
7235 Standard Drive
Hanover 21076
(301) 796-5000

Schweber Electronics
9218 Gaither Road
Gaithersburg 20760
(301) 840-5900

Wilshire Electronics
1037 Taft Street
Rockville 20850
(301) 340-7900

Massachusetts

Hamilton/Avnet
50 Tower Office Park
Woburn 01801
(617) 273-7500

Schweber Electronics
25 Wiggins Avenue
Bedford 01730
(617) 890-8484

Wilshire Electronics
One Wilshire Road
Burlington 01803
(617) 272-8200

Michigan

Hamilton/Avnet
32487 Schoolcraft Road
Livonia 48150
(313) 522-4700

Schweber Electronics
33540 Schoolcraft Road
Livonia 48150
(313) 583-9242

Minnesota

Hall-Mark Electronics
9201 Penn Avenue, So.
Suite 10
Bloomington 55431
(612) 884-9056

Hamilton/Avnet
7449 Cahill Road
Edina 55435
(612) 941-3801

Schweber Electronics
7402 Washington Avenue, So.
Eden Prairie 55343
(612) 941-5280

Missouri

Hall-Mark Electronics
13789 Rider Trail
Earth City 63045
(314) 291-5350

Hamilton/Avnet
396 Brookes Lane
Hazelwood 63042
(314) 731-1144

New Jersey

Hamilton/Avnet
1 Keystone Avenue
Cherryhill 08003
(609) 424-0100

Hamilton/Avnet
10 Industrial Road
Fairfield 07006
(201) 575-3390

Schweber Electronics
18 Madison Road
Fairfield 07006
(201) 227-7880

Wilshire Electronics
1111 Paulison Avenue
Clifton 07015
(201) 340-1900

Wilshire Electronics
102 Gaither Drive
Mt. Laurel 08057
(609) 234-9100

New Mexico

Hamilton/Avnet
2524 Baylor S.E.
Albuquerque 87106
(505) 765-1500

New York

Hamilton/Avnet
16 Corporate Circle
East Syracuse 13057
(315) 437-2641

Hamilton/Avnet
5 Hub Drive
Melville 11746
(516) 454-6000

Hamilton/Avnet
167 Clay Road
Rochester 14623
(716) 442-7820

Schweber Electronics
2 Townline Circle
Rochester 14623
(716) 424-2222

Schweber Electronics
Jericho Turnpike
Westbury 11590
(516) 334-7474

Wilshire Electronics
10 Hooper Road
Endwell 13760
(607) 754-1570

Wilshire Electronics
110 Parkway So. Drive
Hauppauge, L.I. 11787
(516) 543-5599

Wilshire Electronics
1260 Scottsville Road
Rochester 14624
(716) 235-7620

North Carolina

Hall-Mark Electronics
1208 Front Street, Bldg. K
Raleigh 27609
(919) 832-4465

Hamilton/Avnet
2803 Industrial Drive
Raleigh 27609
(919) 829-8030

Ohio

Hall-Mark Electronics
6969 Worthington-Galena Road
Worthington 43085
(614) 846-1882

Pioneer-Standard
4800 East 131st Street
Cleveland 44105
(216) 587-3600

Pioneer-Standard
1900 Troy Street
Dayton 45404
(513) 236-9900

Schweber Electronics
23880 Commerce Park Road
Beachwood 44112
(216) 464-2970

Oklahoma

Hall-Mark Electronics
5460 South 103rd E. Avenue
Tulsa 74145
(918) 835-8458

Oregon

Representative

Northwest Marketing
Associates, Inc.
9999 S.W. Wilshire Street
Suite 211
Portland 97225
(503) 297-2581
(206) 455-5846

Pennsylvania

Hall-Mark Electronics
458 Pike Road
Huntingdon Valley 19001
(215) 355-7300

Pioneer-Standard
560 Alpha Drive
Pittsburgh 15238
(412) 782-2300

Schweber Electronics
101 Rock Road
Horsham 19044
(609) 964-4496
(215) 441-0600

Texas

Hall-Mark Electronics
10109 McKalla Road
Suite F
Austin 78758
(512) 837-2814

Hall-Mark Electronics
11333 Pagemill Drive
Dallas 75222
(214) 234-7400

Hall-Mark Electronics
8000 Westglen
P.O. Box 42190
Houston 77042
(713) 781-6100

Hamilton/Avnet
10508 A. Boyer Boulevard
Austin 78757
(512) 837-8911

Hamilton/Avnet
4445 Sigma Road
Dallas 72540
(214) 661-8661

Hamilton/Avnet
3939 Ann Arbor
Houston 77063
(713) 780-1771

Schweber Electronics
14177 Proton Road
Dallas 75240
(214) 661-5010

Schweber Electronics
7420 Harwin Drive
Houston 77036
(713) 784-3600

Utah

Hamilton/Avnet
1585 West 2100 South
Salt Lake City 84119
(801) 972-2800

Washington

Hamilton/Avnet
14212 N.E. 21st Street
Bellevue 98005
(206) 746-8750

Wyle Distribution Group
1750 132nd Avenue, N.E.
Bellevue 98005
(206) 453-8300

Representative

Northwest Marketing
Associates, Inc.
12835 Bellevue-Redmond Road
Suite 203E
Bellevue 98005
(206) 455-5846

Wisconsin

Hall-Mark Electronics
9625 South 20th Street
Oakcreek 53154
(414) 761-3000

Hamilton/Avnet
2975 Moorland Road
New Berlin 53151
(414) 784-4510

International

Australia

CEMA ELECTRONICS PTY. LTD.
170 Sturt Street
Adelaide, S.A.
(61) 8 516483

CEMA ELECTRONICS PTY. LTD.
208 Whitehorse Road
Blackburn, Victoria
(61) 3 8775311

CEMA ELECTRONICS PTY. LTD.
22 Ross Street
Newstead, Queensland
(61) 72 524261

CEMA ELECTRONICS PTY. LTD.
21 Chandos Street
St. Leonards, N.S.W. 2065
(61) 2 4394655

Austria

Transistor V.m.b.H.
Auhofstr. 41a
1130 Wien
(43) 222 829451

Belgium

Diode Belgium
Rue Picard 202
1020 Bruxelles
(32) 2 4285108

Brazil

Datatronix Electronica LTDA
Av. Pacaembu, 746-C11
São Paulo, Brazil
(55) 11 8260111

Canada

Hamilton/Avnet
3688 Nashua Drive
Units G & H
Mississauga, Ontario L4V 1M5
(416) 677-7432

Hamilton/Avnet
2670 Sabourin Street
St. Laurent
Montréal, Québec H4S 1M2
(514) 331-6443

Hamilton/Avnet
1735 Courtwood Crescent
Ottawa, Ontario K2C 3J2
(613) 226-1700

Zentronics, Ltd.
1355 Meyerside Drive
Mississauga, Ontario L5T 1C9
(416) 676-9000

Zentronics, Ltd.
5010 Pare Street
Montréal, Québec H4P 1P3
(514) 735-5361

Zentronics, Ltd.
141 Catherine Street
Ottawa, Ontario K2P 1C3
(613) 238-6411

Representatives

Cantec Reps, Inc.
28 Eastmoor Cresent
Dollard Des Ormeaux
Montréal, Québec H9G 2N1
(514) 620-6313

Cantec Reps, Inc.
83 Galaxy Boulevard
Unit 1A
Toronto (Rexdale)
Ontario M9W 5X6
(416) 675-2460

Cantec Reps, Inc.
1573 Laperriere Avenue
Ottawa, Ontario K1Z 7T3
(613) 725-3704

Denmark

Distributoeren

Interelko A.P.S.
Hovedgaden 16
4622 Havdrup
(45) 3 385716

Finland

Field OY
Veneentekijantie 18
00210 Helsinki 21
(90) 6922577

France

Almex
Zone Industrielle d'Antony
48, rue de l'Aubepiné
92160 Antony
(33) 1 6662112

ETS. F. Feutrier
rue des trois Glorieuses
42270 St-Priest-en-Jarez
St. Etienne
(33) 77 746733

F. Feutrier
29 rue Ledru Rollin
92150 Suresnes
(33) 1 7724646

S.C.A.I.B.
80 rue d'Arcueil
Zone-Silic
94150 Rungis
(33) 1 6872313

Germany

EBV Elektronik
Vertriebs GmbH
Oberweg 6
8025 Unterhaching
(49) 89 611051

Ingenieurbuero Dreyer
Flensburger Strasse 3
2380 Schleswig
(49) 4621 23121

Jermyn GmbH
Postfach 1180
6277 Camberg
(49) 6434/23-1

RTG E. Springorum Kg
GmbH & Co.
Bronnerstrasse 7
4600 Dortmund
(49) 231 54951

RTG Distron
Behaimstr. 3
Postfach 100208
1000 Berlin 10
(49) 30 3421041/45

Holland

Diode B.V.
Hollant Laan 22
3526 Am Utrecht
(31) 30 88 4214

India

Blue Star Ltd.
Blue Star House
11/11A Magarath Road
Bangalore
560 025

Blue Star Ltd.
Sahas
414/2 Viv Savarkar Marg
Prabhadevi
Bombay 400 025
45 78 87

Blue Star Ltd.
Bhandari House
7th and 8th Floor
91 Nehru Place
New Delhi 110 024
634 770
635 166

Israel

Electronics and Engineering
Div. of Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
Tel Aviv 67899
(97) 23 338973

Italy

Celdis Italiana S.p.A.
Via F. Ili Gracchi, 36
20092 Cinisello B.
(39) 2 6120041

Eledra S.p.A.
Viale Elvezia 18
20125 Milano
(39) 3493041

Japan

Ryoyo Electric Corporation
Meishin Building
1-20-19 Nishiki
Naka-Ku, Nagoya, 460
(81) 52 2030277

Ryoyo Electric Corporation
Taiyo Shoji Building
4-6 Nakanoshima
Kita-Ku, Osaka, 530
(81) 6 4481631

Ryoyo Electric Corporation
Konwa Building
12-22 Tsukiji, 1-Chome
Chuo-Ku, Tokyo
(81) 3 5437711

New Zealand

CEMA ELEKON LTD.
7-9 Kirk Street
Grey Lynn, Auckland
(64) 4 761169

Norway

Ola Tandberg Elektro A/S
Skedsmogt. 25
Oslo 6
(47) 2 197030

Spain

Diode España
Avda de Brasil 7
Edif. Iberia Mart
Madrid 20
(34) 1 4550139/40

So. Africa

Fairmont Electronics (Pty.) Ltd.
P.O. Box 41102
Craighall 2024
Transvaal
(27) 11 7891230

Sweden

Distributoeren

Interelko A.B.
Box 32
122 21 Enskede
(46) 8 132160

Switzerland

Baerlocher AG
Förrlibuckstrasse 110
8021 Zürich
(41) 1 429900

United Kingdom

Celdis Ltd.
37-39 Loverock Road
Reading
Berkshire RG3 1ED
(44) 734 585171

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Vestry Estate
Seven Oaks
Kent TN14 5EU
(44) 732 500144

Macro Marketing Ltd.
396 Bath Road
Cippheham
Slough
Berkshire SL1 6JD
(44) 6286 4422

Sales/Service Offices

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Empresa Técnica de Equipamentos Eléctricos, S.A.R.L.
R. Barbosa Rodrigues, 41-1° DT.°
Caixa Postal, 6487
Luanda
Tel: 35515/6

ARGENTINA
Hewlett-Packard Argentina S.A.
Santa Fe 2035, Martinez
6140 **Buenos Aires**
Tel: 792-1239, 798-6086
Telex: 122443 AR CIGY

Biotron S.A.C.I.y M.
Avda. Paseo Colon 221
9 piso
1399 **Buenos Aires**
Tel: 30-4846/1851/8384
34-9356/0460/4551
Telex: (33) 17595 BIO AR

AUSTRALIA

AUSTRALIA CAPITAL TERR.
Hewlett-Packard Australia Pty. Ltd.
121 Wollongong Street
Fyshwick, 2609
Tel: 804244
Telex: 62650

NEW SOUTH WALES
Hewlett-Packard Australia Pty. Ltd.
31 Bridge Street
Pymble, 2073
Tel: 4496566
Telex: 21561

QUEENSLAND
Hewlett Packard Australia Pty. Ltd.
5th Floor
Teachers Union Building
495-499 Boundary Street
Spring Hill, 4000
Tel: 2291544

SOUTH AUSTRALIA
Hewlett-Packard Australia Pty. Ltd.
153 Greenhill Road
Parkside, 5063
Tel: 2725911
Telex: 82536

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Hewlett-Packard Australia Pty. Ltd.
31-41 Joseph Street
Blackburn, 3130
Tel: 89-6351
Telex: 31024 MELB

WESTERN AUSTRALIA
Hewlett-Packard Australia Pty. Ltd.
141 Stirling Highway
Nedlands, 6009
Tel: 3865455
Telex: 93859

AUSTRIA
Hewlett-Packard Ges.m.b.H.
Wehlistrasse 29
P.O. Box 7
A-1205 **Vienna**
Tel: 35-16-21-0
Telex: 13582/135066

Hewlett-Packard Ges.m.b.H.
Wehlistrasse, 29
A-1205 **Wien**
Tel: 35-16-21
Telex: 135066

BAHRAIN
Medical Only
Wael Pharmacy
P.O. Box 648
Bahrain
Tel: 54886, 56123
Telex: 8550 WAEL GJ

Al Hamidiya Trading and Contracting
P.O. Box 20074
Manama
Tel: 259978, 259958
Telex: 8895 KALDIA GJ

BANGLADESH
The General Electric Co. of Bangladesh Ltd.
Magnet House 72
Dilkusha Commercial Area
Motijheil, Dacca 2
Tel: 252415, 252419
Telex: 734

BELGIUM
Hewlett-Packard Benelux S.A./N.V.
Avenue du Col-Vert, 1, (Groenkraaglaan)
B-1170 **Brussels**
Tel: (02) 660 50 50
Telex: 23-494 paloben bru

BRAZIL
Hewlett-Packard do Brasil I.e.C. Ltda.
Alameda Rio Negro, 750
Alphaville
06400 **Barueri** SP
Tel: 429-3222

Hewlett-Packard do Brasil I.e.C. Ltda.
Rua Padre Chagas, 32
90000-**Pôrto Alegre**-RS
Tel: 22-2998, 22-5621

Hewlett-Packard do Brasil I.e.C. Ltda.
Av. Epitacio Pessoa, 4664
22471-**Rio de Janeiro**-RJ
Tel: 286-0237
Telex: 021-21905 HPBR-BR

CANADA

ALBERTA
Hewlett-Packard (Canada) Ltd.
11620A - 168th Street
Edmonton T5M 3T9
Tel: (403) 452-3670
TWX: 610-831-2431

Hewlett-Packard (Canada) Ltd.
210, 7220 Fisher St. S.E.
Calgary T2H 2H8
Tel: (403) 253-2713
TWX: 610-821-6141

BRITISH COLUMBIA
Hewlett-Packard (Canada) Ltd.
10691 Shellbridge Way
Richmond V6X 2W7
Tel: (604) 270-2277
TWX: 610-925-5059

MANITOBA
Hewlett-Packard (Canada) Ltd.
380-550 Century St.
St. James,
Winnipeg R3H 0Y1
Tel: (204) 786-6701
TWX: 610-671-3531

NOVA SCOTIA
Hewlett-Packard (Canada) Ltd.
P.O. Box 931
800 Windmill Road
Dartmouth B3B 1L1
Tel: (902) 469-7820
TWX: 610-271-4482

ONTARIO
Hewlett-Packard (Canada) Ltd.
1020 Morrison Dr.
Ottawa K2H 8K7
Tel: (613) 820-6483
TWX: 610-563-1636

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
Mississauga L4V 1M8
Tel: (416) 678-9430
TWX: 610-492-4246

Hewlett-Packard (Canada) Ltd.
552 Newbold Street
London N6E 2S5
Tel: (519) 686-9181
TWX: 610-352-1201

QUEBEC
Hewlett-Packard (Canada) Ltd.
275 Hymus Blvd.
Pointe Claire H9R 1G7
Tel: (514) 697-4232
TWX: 610-422-3022

FOR CANADIAN AREAS NOT LISTED:
Contact Hewlett-Packard (Canada) Ltd. in Mississauga.

CHILE
Jorge Calcagni y Cia. Ltda.
Arturo Burhle 065
Casilla 16475
Correo 9, **Santiago**
Tel: 220222
Telex: JCALCAGNI

COLOMBIA
Instrumentación
Henrik A. Langebaek & Kier S.A.
Carrera 7 No. 48-75
Apartado Aéreo 6287
Bogotá, 1 D.E.
Tel: 269-8877
Telex: 44400

Instrumentación
H.A. Langebaek & Kier S.A.
Carrera 63 No. 49-A-31
Apartado 54098
Medellin
Tel: 304475

COSTA RICA
Cientifica Costarricense S.A.
Avenida 2, Calle 5
San Pedro de Montes de Oca
Apartado 10159
San Jose
Tel: 24-38-20, 24-08-19
Telex: 2367 GALGUR CR

CYPRUS
Kypronics
19 Gregorios Xenopoulos Street
P.O. Box 1152
Nicosia
Tel: 45628/29
Telex: 3018

CZECHOSLOVAKIA
Hewlett-Packard
Obchodni zastupitelstvi v CSSR
Pisemny styk
Post. schranka 27
CS 118 01 **Praha** 011
CSSR

Vyvojova a Provozni Zakladna
Vyzkumnych Ustavu v Bechovicich
CSSR-25097 **Bechovice u Prahy**
Tel: 89 93 41
Telex: 12133

Institute of Medical Bionics
Vyskumny Ustav Lekarskej Bioniky
Jedlova 6
CS-88346 **Bratislava-Kramare**
Tel: 44-551
Telex: 93229

DENMARK
Hewlett-Packard A/S
Datavej 52
DK-3460 **Birkerod**
Tel: (02) 81 66 40
Telex: 37409 hpas dk

Hewlett-Packard A/S
Navervej 1
DK-8600 **Silkeborg**
Tel: (06) 82 71 66
Telex: 37409 hpas dk

ECUADOR
CYEDE Cia. Ltda.
P.O. Box 6423 CCI
Av. Eloy Alfaro 1749
Quito
Tel: 450-975, 243-052
Telex: 2548 CYEDE ED

Medical Only
Hospitalar S.A.
Casilla 3590
Robles 625
Quito
Tel: 545-250

EGYPT
I.E.A.
International Engineering Associates
24 Hussein Hegazi Street
Kasr-el-Aini
Cairo
Tel: 23 829
Telex: 93830

SAMITRO
Sami Amin Trading Office
18 Abdel Aziz Gawish
Abdine-Cairo
Tel: 24932

EL SALVADOR
IPESA
Bulevar de los Heroes 11-48
Edificio Sarah 1148
San Salvador
Tel: 252787

ETHIOPIA
Abdella Abdulmalik
P.O. Box 2635
Addis Ababa
Tel: 11 93 40

FINLAND
Hewlett-Packard Oy
Revontulentie, 7
SF-02100 **Espoo** 10
Tel: (90) 455 0211
Telex: 121563 hewpa sf

FRANCE
Hewlett-Packard France
Zone d'activites de Courtaboeuf
Avenue des Tropiques
Boite Postale 6
91401 **Orsay**-Cédex
Tel: (1) 907 78 25
TWX: 600048F

Hewlett-Packard France
Chemin des Mouilles
B.P. 162
69130 **Ecully**
Tel: (78) 33 81 25
TWX: 310617F

Hewlett-Packard France
20, Chemin de La Cépière
31081 **Toulouse**
Le Mirail-Cédex
Tel: (61) 40 11 12

Hewlett-Packard France
Le Ligoures
Place Romée de Villeneuve
13100 **Aix-en-Provence**
Tel: (42) 59 41 02
TWX: 410770F

Hewlett-Packard France
2, Allee de la Bourgonette
35100 **Rennes**
Tel: (99) 51 42 44
TWX: 740912F

Hewlett-Packard France
18, rue du Canal de la Marne
67300 **Schiltigheim**
Tel: (88) 83 08 10
TWX: 890141F

Hewlett-Packard France
Immeuble péricentre
rue van Gogh
59650 **Villeneuve** D'Ascq
Tel: (20) 91 41 25
TWX: 160124F

Hewlett-Packard France
Bâtiment Ampère
Rue de la Commune de Paris
B.P. 300
93153 **Le Blanc Mesnil-Cédex**
Tel: (01) 931 88 50
Telex: 211032F

Hewlett-Packard France
Av. du Pdt. Kennedy
33700 **Merignac**
Tel: (56) 97 01 81

Hewlett-Packard France
Immeuble Lorraine
Boulevard de France
91035 **Evry**-Cédex
Tel: 077 96 60
Telex: 692315F

Hewlett-Packard France
23 Rue Lothaire
57000 **Metz**
Tel: (87) 65 53 50

GERMAN FEDERAL REPUBLIC
Hewlett-Packard GmbH
Vertriebszentrale Frankfurt
Berner Strasse 117
Postfach 560 140
D-6000 **Frankfurt** 56
Tel: (06011) 50041
Telex: 04 13249 hpffm d

Hewlett-Packard GmbH
Technisches Büro Böblingen
Herrenberger Strasse 110
D-7030 **Böblingen,**
Württemberg
Tel: (07031) 667-1
Telex: 07265739 bbn

Hewlett-Packard GmbH
Technisches Büro Düsseldorf
Emanuel-Leutze-Str. 1 (Seestern)
D-4000 **Düsseldorf**
Tel: (0211) 5971-1
Telex: 085/86 533 hpdd d

Hewlett-Packard GmbH
Technisches Büro Hamburg
Kapstadtring 5
D-2000 **Hamburg** 60
Tel: (040) 63804-1
Telex: 21 63 032 hphh d

APPENDIX

Hewlett-Packard GmbH
Technisches Büro Hannover
Am Grossmarkt 6
D-3000 **Hannover** 91
Tel: (0511) 46 60 01
Telex: 092 3259

Hewlett-Packard GmbH
Technisches Büro NUrnberg
Neumeyerstrasse 90
D-8500 **Nürnberg**
Tel: (0911) 52 20 83
Telex: 0623 860

Hewlett-Packard GmbH
Technisches Büro MUnchen
Eschenstrasse 5
D-8021 **Taufkirchen**
Tel: (089) 6117-1
Telex: 0524985

Hewlett-Packard GmbH
Technisches BUro Berlin
Kaithstrasse 2-4
D-1000 **Berlin** 30
Tel: (030) 24 90 86
Telex: 018 3405 hpbln d

GREECE
Kostas Karayannis
8 Omirou Street
Athens 133
Tel: 32 30 303/32/37 731
Telex: 21 59 62 RKAR GR

GUAM
Guam Medical Supply, Inc.
Suite C, Airport Plaza
P.O. Box 8947
Tamuning 96911
Tel: 646-4513

GUATEMALA
IPESA
Avenida Reforma 3-48
Zona 9
Guatemala City
Tel: 316627, 314786,
66471-5, ext. 9
Telex: 4192 Teletro Gu

HONG KONG
Hewlett-Packard Hong Kong Ltd.
11th Floor, Four Seas Bldg.
212 Nathan Rd.
Kowloon
Tel: 3-697446 (5 lines)
Telex: 36678 HX

Medical/Analytical Only
Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
Hong Kong
Tel: 5-455644
Telex: 74766 SCHMX HX

INDIA
Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
Bombay 400 025
Tel: 45 78 87
Telex: 011-4093

Blue Star Ltd.
Band Box House
Prabhadevi
Bombay 400 025
Tel: 45 73 01
Telex: 011-3751

Blue Star Ltd.
Bhavdeep
Stadium Road
Ahmedabad 380 014
Tel: 43922
Telex: 012-234

Blue Star Ltd.
7 Hare Street
Calcutta 700 001
Tel: 23-0131
Telex: 021-7655

Blue Star Ltd.
Bhandari House
91 Nehru Place
New Delhi 110 024
Tel: 682547
Telex: 031-2463

Blue Star Ltd.
T.C. 7/603 'Poornima'
Maruthankuzhi
Trivandrum 695 013
Tel: 65799
Telex: 0884-259

Blue Star Ltd.
11 Magarath Road
Bangalore 560 025
Tel: 55668
Telex: 0845-430

Blue Star Ltd.
Meeakshi Mandiram
XXXXV/1379-2 Mahatma Gandhi Rd.
Cochin 682 016
Tel: 32069
Telex: 085-514

Blue Star Ltd.
1-1-117/1 Sarojini Devi Road
Secunderabad 500 033
Tel: 70126
Telex: 0155-459

Blue Star Ltd.
133 Kodambakkam High Road
Madras 600 034
Tel: 82057
Telex: 041-379

ICELAND
Medical Only
Elding Trading Company Inc.
Hafnarnvoli - Tryggvagötu
P.O. Box 895
IS-**Reykjavik**
Tel: 1 58 20/1 63 03

INDONESIA
BERCA Indonesia P.T.
P.O. Box 496/Jkt.
Jln. Abdul Muis 62
Jakarta
Tel: 349255, 349886
Telex: 46748 BERSIL IA

BERCA Indonesia P.T.
P.O. Box 174/Sby.
23 Jln. Jimerto
Surabaya
Tel: 42027

IRELAND
Hewlett-Packard Ltd.
Kestrel House
Clanwilliam Place
Lower Mount Street
Dublin 2, Eire

Hewlett-Packard Ltd.
2C Avongberg Ind. Est.
Long Mile Road
Dublin 12
Tel: 514322/514224
Telex: 30439

Medical Only
Cardiac Services (Ireland) Ltd.
Kilmore Road
Artane
Dublin 5, Eire
Tel: (01) 315820

Medical Only
Cardiac Services Co.
95A Finaghy Rd. South
Belfast BT10 0BY
GB-Northern Ireland
Tel: (0232) 625566
Telex: 747626

ISRAEL
Electronics Engineering Div.
of Motorola Israel Ltd.
16, Kremenetski Street
P.O. Box 25016
Tel-Aviv
Tel: 38973
Telex: 33569, 34164

ITALY
Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio, 9
20063 **Cernusco Sul Naviglio** (MI)
Tel: (2) 903691
Telex: 334632 HEWPACKIT

Hewlett-Packard Italiana S.p.A.
Via Turazza, 14
35100 **Padova**
Tel: (49) 664888
Telex: 430315 HEWPACKI

Hewlett-Packard Italiana S.p.A.
Via G. Armellini 10
1-00143 **Roma**
Tel: (06) 54 69 61
Telex: 610514

Hewlett-Packard Italiana S.p.A.
Corso Giovanni Lanza 94
I-10133 **Torino**
Tel: (011) 659308
Telex: 221079

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43 G/C
I-95126 **Catania**
Tel: (095) 37 05 04
Telex: 970291

Hewlett-Packard Italiana S.p.A.
Via Nuova san Rocco A
Capadimonte, 62A
80131 **Napoli**
Tel: (081) 710698

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/111
I-40132 **Bologna**
Tel: (051) 402394
Telex: 511630

JAPAN
Yokogawa-Hewlett-Packard Ltd.
29-21, Takaido-Higashi 3-chome
Suginami-ku, **Tokyo** 168
Tel: 03-331-6111
Telex: 232-2024 YHP-Tokyo

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg., 4th Floor
4-20, Nishinakajima 5-chome
Yodogawa-ku, Osaka-shi
Osaka, 532
Tel: 06-304-6021
Telex: 523-3624

Yokogawa-Hewlett-Packard Ltd.
Sunitomo Seimei Nagaya Bldg.
11-2 Shimosasajima-cho,
Nakamura-ku, **Nagoya,** 450
Tel: 052 571-5171

Yokogawa-Hewlett-Packard Ltd.
Tanigawa Building
2-24-1 Tsuruya-cho
Kanagawa-ku
Yokohama, 221
Tel: 045-312-1252
Telex: 382-3204 YHP YOK

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Building
105, 1-chome, San-no-maru
Mito, Ibaragi 310
Tel: 0292-25-7470

Yokogawa-Hewlett-Packard Ltd.
Inoue Building
1348-3, Asahi-cho, 1-chome
Atsugi, Kanagawa 243
Tel: 0462-24-0452

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi
Hachijuni Building
4th Floor
3-4, Tsukuba
Kumagaya, Saitama 360
Tel: 0485-24-6563

JORDAN
Mouasher Cousins Co.
P.O. Box 1387
Amman
Tel: 24907/39907
Telex: SABCO JO 1456

KENYA
ADCOM Ltd., Inc.
P.O. Box 30070
Nairobi
Tel: 331955
Telex: 22639

Medical Only
International Aeradio (E.A.) Ltd.
P.O. Box 19012
Nairobi Airport
Nairobi
Tel: 336055/56
Telex: 22201/22301

Medical Only
International Aeradio (E.A.) Ltd.
P.O. Box 95221
Mombasa

KOREA
Samsung Electronics Co., Ltd.
4759 Shingil-6-Dong
Yeong Deung POU
Seoul
Tel: 833-4122, 4121
Telex: SAMSAN 27364

KUWAIT
Al-Khaldiya Trading & Contracting
P.O. Box 830-Safat
Kuwait
Tel: 42 4910/41 1726
Telex: 2481 Areeg kt

LUXEMBURG
Hewlett-Packard Beneluz S.A./N.V.
Avenue du Col-Vert, 1
(Groenkraaglaan)
B-1170 **Brussels**
Tel: (02) 660 5050
Telex: 23 494

MALAYSIA
Hewlett-Packard Sales
(Malaysia) Sdn. Bhd.
Suite 2.21/2.22
Bangunan Angkasa Raya
Jalan Ampang
Kuala Lumpur
Tel: 483680, 485653

Protel Engineering
P.O. Box 1917
Lot 259, Satok Road
Kuching, **Sarawak**
Tel: 53544

MEXICO
Hewlett-Packard Mexicana, S.A. de C.V.
Av. Periférico Sur No. 6501
Tepepan, Xochimilco
Mexico 23, D.F.
Tel: 905-676-4600
Telex: 017-74-507

Hewlett-Packard Mexicana, S.A. de C.V.
Rio Volga #600
Col. Del Valle
Monterrey, N.L.
Tel: 78-32-10

MOROCCO
Dolbeau
81 rue Karatchi
Casablanca
Tel: 3041 82
Telex: 23051/22822

Gerep
2, rue d'Agadir
Boite Postal 156
Casablanca
Tel: 272093/5
Telex: 23 739

MOZAMBIQUE
A.N. Goncalves, Ltd.
162, 1° Apt. 14 Av. D. Luis
Caixa Postal 107
Maputo
Tel: 27091, 27114
Telex: 6-203 NEGON Mo

NETHERLANDS
Hewlett-Packard Benelux N.V.
Van Heuven Goedhartlaan 121
P.O. Box 667
1181KK **Amstelveen**
Tel: (20) 47 20 21
Telex: 13 216

NEW ZEALAND
Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
Kilbirnie, Wellington 3
P.O. Box 9443
Courtney Place
Wellington
Tel: 877-199

Hewlett-Packard (N.Z.) Ltd.
P.O. Box 26-189
169 Manukau Road
Epsom, **Auckland**
Tel: 687-159

Analytical/Medical Only
Northrop Instruments & Systems Ltd.,
Sturdee House
85-87 Ghuznee Street
P.O. Box 2406
Wellington
Tel: 850-091
Telex: NZ 31291

Northrup Instruments & Systems Ltd.
Eden House, 44 Khyber Pass Rd.
P.O. Box 9682, Newmarket
Auckland 1
Tel: 794-091

Northrup Instruments & Systems Ltd.
Terrace House, 4 Oxford Terrace
P.O. Box 8388
Christchurch
Tel: 64-165

NIGERIA
The Electronics Instrumentations Ltd.
N6B/770 Oyo Road
Oluseun House
P.M.B. 5402
Ibadan
Tel: 461577
Telex: 31231 TEIL NG

The Electronics Instrumentations Ltd.
144 Agege Motor Road, Mushin
P.O. Box 481
Mushin, **Lagos**

NORWAY
Hewlett-Packard Norge A/S
Ostendalen 18
P.O. Box 34
1345 **Osteraas**
Tel: (02) 1711 80
Telex: 16621 hpnas n

Hewlett-Packard Norge A/S
Nygaardsgaten 114
P.O. Box 4210
5013 Nygaardsgaten,
Bergen
Tel: (05) 21 97 33

PANAMA
Electrónico Balboa, S.A.
Aparatado 4929
Panama 5
Calle Samuel Lewis
Edificio "Alfa," No. 2
Ciudad de Panama
Tel: 64-2700
Telex: 3483103 Curundu,
Canal Zone

PERU
Compañía Electro Médica S.A.
Los Flamencos 145
San Isidro Casilla 1030
Lima 1
Tel: 41-4325
Telex: Pub. Booth 25424
SISIDRO

PAKISTAN
Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
Karachi-3
Tel: 511027, 512927
Telex: 2894

Mushko & Company, Ltd.
10, Bazar Rd.
Sector G-6/4
Islamabad
Tel: 28264

PHILIPPINES
The Online Advanced Systems
Corporation
Rico House
Amorsolo cor. Herrera Str.
Legaspi Village, Makati
P.O. Box 1510
Metro **Manila**
Tel: 85-35-81, 85-34-91,
85-32-21
Telex: 3274 ONLINE

RHODESIA
Field Technical Sales
45 Kelvin Road North
P.O. Box 3458
Salisbury
Tel: 705231 (5 lines)
Telex: RH 4122

POLAND
Biuro Informacji Technicznej
Hewlett-Packard
Ul Stawki 2, 6P
PL00-950 **Warszawa**
Tel: 39 59 62, 39 51 87
Telex: 81 24 53

PORTUGAL
Telectra-Empresa Técnica de
Equipamentos Eléctricos
S.a.r.l.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-**Lisbon** 1
Tel: (19) 68 60 72
Telex: 12598

Medical Only
Mundinter
Intercambio Mundial de
Comércio S.a.r.l.
P.O. Box 2761
Avenida Antonio Augusto
de Aguiar 138
P-**Lisbon**
Tel: (19) 53 21 31/7
Telex: 16691 munter p

PUERTO RICO
Hewlett-Packard Inter-
Americas
Puerto Rico Branch Office
Calle 272,
#203 Urb. Country Club
Carolina 00630
Tel: (809) 762-7255
Telex: 345 0514

QATAR
Nasser Trading & Contracting
P.O. Box 1563
Doha
Tel: 22170
Telex: 4439 NASSER

ROMANIA
Hewlett-Packard
Reprezentanta
Bd.n. Balcescu 16
Bucuresti
Tel: 15 80 23/13 88 85
Telex: 10440

SAUDI ARABIA
Modern Electronic
Establishment (Head Office)
P.O. Box 1228, Baghdadiah
Street
Jeddah
Tel: 27 798
Telex: 40035
Cable: ELECTA JEDDAH

Modern Electronic
Establishment (Branch)
P.O. Box 2728
Riyadh
Tel: 62596/66232
Telex: 202049

Modern Electronic
Establishment (Branch)
P.O. Box 193
Al-Khobar
Tel: 44678-44813
Telex: 670136
Cable: ELECTA AL-KHOBAR

SINGAPORE
Hewlett-Packard Singapore
(Pte.) Ltd.
6th Floor, Inchcape House
450-452 Alexandra Road
P.O. Box 58
Alexandra Post Office
Singapore 9115
Tel: 631788
Telex: HPSG RS 21486

SOUTH AFRICA
Hewlett-Packard South Africa
(Pty.), Ltd.
Private Bag Wendywood,
Sandton, Transvaal, 2144
Hewlett-Packard Centre
Daphne Street, Wendywood,
Sandton, 2144
Tel: 802-5111/25
Telex: 8-4782

Hewlett-Packard South Africa
(Pty.), Ltd.
P.O. Box 120
Howard Place,
Cape Province, 7450
Pine Park Centre, Forest Drive,
Pinelands,
Cape Province, 7405
Tel: 53-7955 thru 9
Telex: 57-0006

SPAIN
Hewlett-Packard Española,
S.A.
Calle Jerez 3
E-**Madrid** 16
Tel: (1) 458 26 00 (10 lines)
Telex: 23515 hpe

Hewlett-Packard Española S.A.
Colonia Mirasierra
Edificio Juban
c/o Costa Brava, 13
Madrid 34

Hewlett-Packard Española,
S.A.
Milanesado 21-23
E-**Barcelona** 17
Tel: (3) 203 6200 (5 lines)
Telex: 52603 hpbe e

Hewlett-Packard Española,
S.A.
Av Ramón y Cajal, 1
Edificio Sevilla, planta 9°
E-**Sevilla** 5
Tel: 64 44 54/58

Hewlett-Packard Española S.A.
Edificio Albia II 7° B
E-**Bilbao** 1
Tel: 23 83 06/23 82 06

Hewlett-Packard Española S.A.
C/Ramon Gordillo 1
(Entlo.)
E-**Valencia** 10
Tel: 96-361.13.54/361.13.58

SRI LANKA
Metropolitan Agencies Ltd.
209/9 Union Place
Colombo 2
Tel: 35947
Telex: 1377METROLTD CE

SUDAN
Radison Trade
P.O. Box 921
Khartoum
Tel: 44048
Telex: 375

SURINAM
Surtel Radio Holland N.V.
Grote Hofstr. 3-5
P.O. Box 155
Paramaribo
Tel: 72118, 77880

SWEDEN
Hewlett-Packard Sverige AB
Enighetsvägen 3, Fack
S-161 **Bromma** 20
Tel: (08) 730 05 50
Telex: 10721
Cable: MEASUREMENTS
Stockholm

Hewlett-Packard Sverige AB
Frötallsgatan 30
S-421 32 **Västra**
Frölunda
Tel: (031) 49 09 50
Telex: 10721 via Bromma
office

SWITZERLAND
Hewlett-Packard (Schweiz) AG
Zürcherstrasse 20
P.O. Box 307
CH-8952 **Schlieren-**
Zürich
Tel: (01) 7305240
Telex: 53933 hpag ch
Cable: HPAG CH

Hewlett-Packard (Schweiz) AG
Château Bloc 19
CH-1219 **Le Lignon-**
Geneva
Tel: (022) 96 03 22
Telex: 27333 hpag ch
Cable: HEWPACKAG Geneva

SYRIA
General Electronic Inc.
Nuri Basha-Ahnaf Ebn Kays
Street
P.O. Box 5781
Damascus
Tel: 33 24 87
Telex: 11215 ITIKAL
Cable: ELECTROBOR
DAMASCUS

Medical only
Sawah & Co.
Place Azmé
B.P. 2308
Damascus
Tel: 16 367-19 697-14 268
Telex: 11304 SATACO SY
Cable: SAWAH, DAMASCUS

Suleiman Hilal El Mlawi
P.O. Box 2528
Mamoun Bitar Street, 56-58
Damascus
Tel: 11 46 63
Telex: 11270
Cable: HILAL DAMASCUS

TAIWAN
Hewlett-Packard Far East Ltd.
Taiwan Branch
Bank Tower, 5th Floor
205 Tun Hau North Road
Taipei
Tel: (02) 751-0404 (15 lines)

Hewlett-Packard Far East Ltd.
Taiwan Branch
68-2, Chung Cheng 3rd. Road
Kaohsiung
Tel: (07) 242318-Kaohsiung

Analytical Only
San Kwang Instruments Co.,
Ltd.
20 Yung Sui Road
Taipei
Tel: 3615446-9 (4 lines)
Telex: 22894 SANKWANG

TANZANIA
Medical Only
International Aeradio (E.A.), Ltd.
P.O. Box 861
Dar es Salaam
Tel: 21251 Ext. 265
Telex: 41030

THAILAND
UNIMESA Co. Ltd.
Elcom Research Building
2538 Sukumvit Ave.
Bangchak, Bangkok
Tel: 39-32-387, 39-30-338

TRINIDAD &
TOBAGO
CARTEL
Caribbean Telecoms Ltd.
P.O. Box 732
69 Frederick Street
Port-of-Spain
Tel: 62-53068

TUNISIA
Tunisie Electronique
31 Avenue de la Liberte
Tunis
Tel: 280 144

Corema
1 ter. Av. de Carthage
Tunis
Tel: 253 821
Telex: 12319 CABAM TN

TURKEY
TEKNIM Company Ltd.
Riza Sah Pehlevi
Caddesi No. 7
Kavaklidere, **Ankara**
Tel: 275800
Telex: 42155

Teknim Com., Ltd.
Barbaros Bulvari 55/12
Besikyas, **Istanbul**
Tel: 613 546
Telex: 23540

E.M.A.
Muhendislik Kollektif Sirketi
Mediha Eldem Sokak 41/6
Yüksel Caddesi
Ankara
Tel: 17 56 22

Yilmaz Ozyurek
Milli Mudafaa Cad 16/6
Kizilay
Ankara
Tel: 25 03 09 - 17 80 26
Telex: 42576 OZEK TR

UNITED ARAB
EMIRATES
Emitac Ltd. (Head Office)
P.O. Box 1641
Sharjah
Tel: 354121/3
Telex: 8136

Emitac Ltd. (Branch Office)
P.O. Box 2711
Abu Dhabi
Tel: 331370/1

UNITED KINGDOM
Hewlett-Packard Ltd.
King Street Lane
Winnersh, Wokingham
Berkshire RG11 5AR
GB-England
Tel: (0734) 784774
Telex: 84 71 78/9

Hewlett-Packard Ltd.
Fourier House,
257-263 High Street
London Colney
St. Albans, Herts
GB-England
Tel: (0727) 24400
Telex: 1-8952716

Hewlett-Packard Ltd.
Trafalgar House
Navigation Road
Altrincham
Cheshire WA14 1NU
GB-England
Tel: (061) 928 6422
Telex: 668068

Hewlett-Packard Ltd.
Lygon Court
Hereward Rise
Dudley Road
Halesowen,
West Midlands, B62 8SD
GB-England
Tel: (021) 501 1221
Telex: 339105

Hewlett-Packard Ltd.
Wedge House
799, London Road
Thornton Heath
Surrey, CR4 6XL
GB-England
Tel: (01) 684-0103/8
Telex: 946825

Hewlett-Packard Ltd.
14 Wesley St
Castleford
Yorks WF10 1AE
Tel: (0977) 550016
TWX: 5557335

Hewlett-Packard Ltd.
Tradax House
St. Mary's Walk
Maidenhead
Berkshire, SL6 1ST
GB-England

Hewlett-Packard Ltd.
Morley Road
Staplehill
Bristol, BS16 4QT
GB-England

Hewlett-Packard Ltd.
South Queensferry
West Lothian, EH30 9TG
GB-Scotland
Tel: (031) 331 1188
Telex: 72682

UNITED STATES

ALABAMA
700 Century Park South,
Suite 128
Birmingham 35226
Tel: (205) 822-6802

P.O. Box 4207
8290 Whitesburg Dr.
Huntsville 35802
Tel: (205) 881-4591

ARIZONA
2336 E. Magnolia St.
Phoenix 85034
Tel: (602) 273-8000

2424 East Aragon Rd.
Tucson 85706
Tel: (602) 273-8000

ARKANSAS
Medical Service Only
P.O. Box 5646
Brady Station
Little Rock 72215
Tel: (501) 376-1844

CALIFORNIA
1579 W. Shaw Ave.
Fresno 93771
Tel: (209) 224-0582

1430 East Orangethorpe Ave.
Fullerton 92631
Tel: (714) 870-1000

APPENDIX

5400 West Rosecrans Blvd.
P.O. Box 92105
World Way Postal Center
Los Angeles 90009
Tel: (213) 970-7500
TWX: 910-325-6608

3939 Lankershim Boulevard
North Hollywood 91604
Tel: (213) 877-1282
TWX: 910-499-2671

3200 Hillview Av
Palo Alto, CA 94304
Tel: (408) 988-7000

646 W. North Market Blvd.
Sacramento 95834
Tel: (916) 929-7222

9606 Aero Drive
P.O. Box 23333
San Diego 92123
Tel: (714) 279-3200

363 Brookhollow Dr.
Santa Ana, CA 92705
Tel: (714) 641-0977

3003 Scott Boulevard
Santa Clara 95050
Tel: (408) 988-7000
TWX: 910-338-0518

454 Carlton Court
So. San Francisco 94080
Tel: (415) 877-0772

***Tarzana**
Tel: (213) 705-3344

COLORADO
5600 DTC Parkway
Englewood 80110
Tel: (303) 771-3455

CONNECTICUT
47 Barnes Industrial Road
Barnes Park South
Wallingford 06492
Tel: (203) 265-7801

FLORIDA
P.O. Box 24210
2727 N.W. 62nd Street
Ft. Lauderdale 33309
Tel: (305) 973-2600

4080 Woodcock Drive #132
Brownett Building
Jacksonville 32207
Tel: (904) 398-0663

P.O. Box 13910
6177 Lake Ellenor Dr.
Orlando 32809
Tel: (305) 859-2900

P.O. Box 12826
Suite 5, Bldg. 1
Office Park North
Pensacola 32575
Tel: (904) 476-8422
110 South Hoover Blvd.
Suite 120
Tampa 33609
Tel: (813) 872-0900

GEORGIA
P.O. Box 105005
450 Interstate North Parkway
Atlanta 30348
Tel: (404) 955-1500
TWX: 810-766-4890

Medical Service Only
***Augusta** 30903
Tel: (404) 736-0592

P.O. Box 2103
1172 N. Davis Drive
Warner Robins 31098
Tel: (912) 922-0449

HAWAII
2875 So. King Street
Honolulu 96826
Tel: (808) 955-4455

ILLINOIS
211 Prospect Rd.
Bloomington 61701
Tel: (309) 663-0383

5201 Tollview Dr.
Rolling Meadows
60008
Tel: (312) 255-9800
TWX: 910-687-2260

INDIANA
7301 North Shadeland Ave.
Indianapolis 46250
Tel: (317) 842-1000
TWX: 810-260-1797

IOWA
2415 Heinz Road
Iowa City 52240
Tel: (319) 351-1020

KENTUCKY
10170 Linn Station Road
Suite 525
Louisville 40223
Tel: (502) 426-0100

LOUISIANA
P.O. Box 1449
3229-39 Williams Boulevard
Kenner 70062
Tel: (504) 443-6201

MARYLAND
7121 Standard Drive
Parkway Industrial Center
Hanover 21076
Tel: (301) 796-7700
TWX: 710-862-1943

2 Choke Cherry Road
Rockville 20850
Tel: (301) 948-6370
TWX: 710-828-9684

MASSACHUSETTS
32 Hartwell Ave.
Lexington 02173
Tel: (617) 861-8960
TWX: 710-326-6904

MICHIGAN
23855 Research Drive
Farmington Hills 48024
Tel: (313) 476-6400

724 West Centre Ave.
Kalamazoo 49002
Tel: (616) 323-8362

MINNESOTA
2400 N. Prior Ave.
St. Paul 55113
Tel: (612) 636-0700

MISSISSIPPI
322 N. Mart Plaza
Jackson 39206
Tel: (601) 982-9363

MISSOURI
11131 Colorado Ave.
Kansas City 64137
Tel: (816) 763-8000
TWX: 910-771-2087

1024 Executive Parkway
St. Louis 63141
Tel: (314) 878-0200

NEBRASKA
Medical Only
7101 Mercy Road
Suite 101
Omaha 68106
Tel: (402) 392-0948

NEVADA
***Las Vegas**
Tel: (702) 736-6610

NEW JERSEY
Crystal Brook Professional
Building
Route 35
Eatontown 07724
Tel: (201) 542-1384

W. 120 Century Rd.
Paramus 07652
Tel: (201) 265-5000
TWX: 710-990-4951

NEW MEXICO
P.O. Box 11634
Station E
11300 Lomas Blvd., N.E.
Albuquerque 87123
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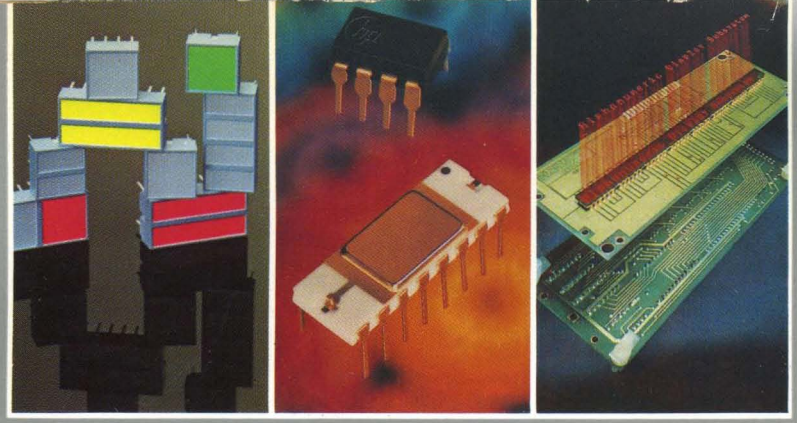

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